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DESIGN OF CMOS COMPRESSIVE SENSING IMAGE SENSORS

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B.Sc., Chittagong University of Engineering and Technology, 2013

A Thesis
Submitted in Partial Fulfillment of the Requirements for the
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THESIS APPROVAL

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Approved by:

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Graduate School
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TITLE: DESIGN OF CMOS COMPRESSIVE SENSING IMAGE SENSORS

MAJOR PROFESSOR: Dr. Haibo Wang

This work investigates the optimal measurement matrices that can be used in compressive sensing (CS) image sensors. It also optimizes CMOS current-model pixel cell circuits for CS image sensors. Based on the outcomes from these optimization studies, three CS image senor circuits with compression ratios of 4, 6, and 8 are designed with using a 130 nm CMOS technology. The pixel arrays used in the image sensors has a size of 256X256. Circuit simulations with benchmark image Lenna show that the three images sensors can achieve peak signal to noise ratio (PSNR) values of 37.64, 33.29, and 32.44dB respectively.

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CHAPTER 1

INTRODUCTION

1.1 IMAGE SENSORS

Nowadays, people use different types of sensors in modern electronic devices. Sensors generally are used to measure physical quantities and convert them electronic signals for further processing. Among various sensors, the image sensors are particularly critical and used in many intelligent modern electronic devices. Thanks to their wide applications. Image sensors attracted significant research efforts over the past two decades, which have significantly improved image sensor resolution and power efficiency.

One main application of the image sensor was digital cameras in the past. But now its application is not confined to digital cameras anymore. It is now being widely used in different types of imaging devices which are used in different purposes in industrial, medical, security media, educational applications. Researchers are continuously improving the existing image sensors mainly in decreasing the pixel size, increasing the pixel counts and increasing the resolution and performances. In the market, there are basically two types of image sensors, CCD image sensor (Charge Coupled Device) and CMOS image sensor. Because of low power, low cost, high scalability, CMOS image sensor is now being more popular over CCDs. Now the CMOS image sensors have a higher annual revenue growth rate in the market than the CCDs.

The number of widespread application of CMOS image sensors is increasing day by day because of its low cost and scalability. However, with the demand of high resolution in the image, the total pixel count is being increased. As a result, the power consumption and hardware to process the increased number of the pixel are also increasing. In particular, converting the large number pixels to digital data by analog to digital converter demands significant power

consumption. Recently emerged compressive sensing (CS) CMOS image sensor techniques provide a promising solution to address this problem.

CS image sensors are actually implemented by adding the pixel values according to the compression ratio. Compression ratio is the number of available pixels over the number of CS measurement. There are lots of published designs [22-26] based on the CS technique. But most of the designs actually used random measurement matrix, to add the pixel values. However, designs with random measurement matrix require very complex circuit implementation and also gives lower Peak Signal to Noise Ratio (PSNR) value. However, we recently found the very regular matrix which can be used to implement CS instead of random matrix. Using this regular matrix, we can implement CS with the simplified circuit, and also we can ensure higher PSNR than other designs with random measurement matrix. In this work, we conduct studies to further optimize the regular matrix optimization used in CS operation. Also, we study the optimal pixel cell design for CS operation. Those developed circuits are evaluated via extensive circuit simulation and compared with conventional implementations.

1.2 THESIS ORGANIZATION

The rest of the thesis is organized as follows: Chapter 2 provides an overview of CMOS image sensors designs and their operations. It also briefly discuss compressive sensing technique, including mathematical theory and existing CS image sensor implementations. Chapter 3 describes our used regular measurement matrix and discusses our studies on the optimization of number of overlapped pixels in pixel summation during CS measurement operation. Chapter 4 discusses pixel cell optimization. Analytical equations are derived in this chapter to model how summation linearity is affected by the pixel cell design and simulation results are provided to validate our analysis. Chapter 5 presents two CS image sensor circuits, their simulation setup and

simulation results. Finally Chapter 6 concludes the thesis and discusses future research directions.

CHAPTER 2

RELATED WORK

2.1 CCD AND CMOS IMAGE SENSOR

An image is a special type of sensors that detects and conveys information used to make an image. The market for energy efficient image sensor is growing day by day. There are two ways to convert this optical signal into electrical. The first one is Analog Charged Coupled device (CCD) and the second one is the Complementary metal oxide semiconductor (CMOS) technology. The analog CCD performs the photon-to-electron conversion. On the other hand, a digital CMOS image sensor performs photon-to-voltage conversion. Although CCDs had been dominant image sensor technology, recent advancements inCMOS image sensor technology makes it more attractive mainly due to its low cost advantage. The other advantages of the CMOS image sensor areits ability to integrate the sensor devices with analog and digital processing circuits. Table1 summarizes the main differences between the CCD and CMOS image sensor technologies.

2.2 TYPES OF CMOS IMAGE SENSOR PIXEL CIRCUITS

There are different types of pixel circuits used in CMOS image sensor, including passive pixel sensor (PPS), Active Pixel Sensor (APS), Diagram Pixel Sensoretc. The PPS circuit generally has a photodiode and a row select transistor as shown in Figure 1. Although the PPS circuit has a simple architecture and thus a high fill factor, its performance suffers from short noise and non-uniformity (pattern noise) due to process variation across the pixel array [1-2]. Also pixel read out operation for PPS cell is slow.

Table 1 Charged Coupled devices and CMOS image sensors comparison [3]

CCDs	CMOS image sensors
Creates higher quality image	Comparatively lower quality
Less susceptible to noise	More susceptible to noise
Higher fill factor	Lower fill factor because of higher number of transistor
Requires higher power	Needs lower power
Lower scalability	Higher scalability
higher cost	Lower cost
Needs higher response time	Requires less response time
Analog to digital converter cannot be integrated.	Analog to digital converter can be integrated with it.

To speed up the readout process, active pixel sensor (APS) are developed for CMOS image sensors.Among various APS circuits, the 3-transistor (3T) and 4T implementation are particularly popular. 3T APS has a source follower transistor, a reset transistor to isolate the sensing node from the capacitance in column bus, and a row select transistor. The schematic of the 3T APS cell is shown in figure 02. In general, 3T APS has high dark current and high temporal noise. To address this problem, 4T APS cell was introduced which includes a pinned diode which incorporates a floating diffusion node and a transfer gate to the basic 3T APS pixel transistor [1-2]. 4T APS cell is depicted in figure 03. By the way, It isolates the read

and rest operation from the integration period. The buried photodiode has lower dark current and the newly added switch transistor allows to implement the correlated double sampling (CDS).

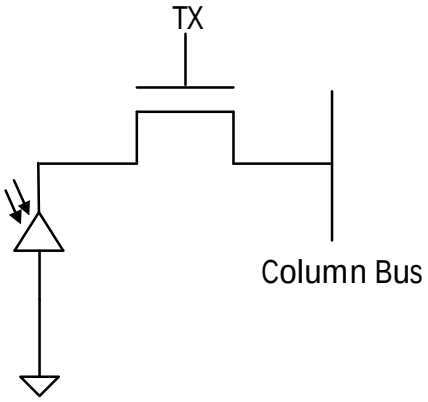


Figure 1: PPS Architecture

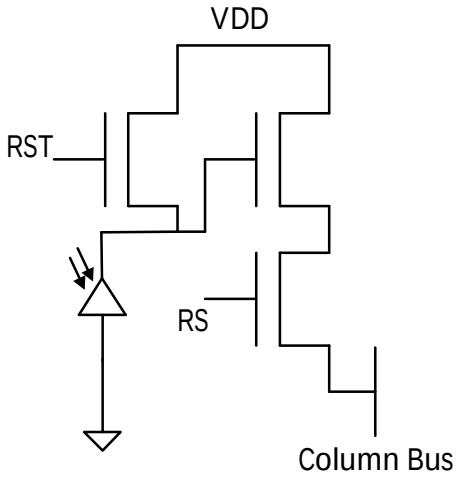


Figure 2: APS 3T Architecture

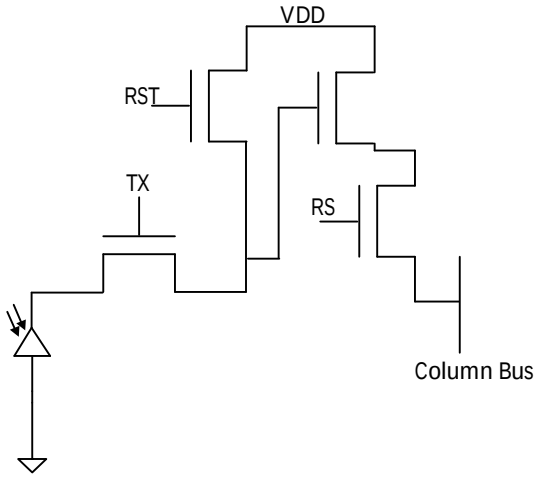


Figure 3: APS 4T Architecture

There is another architecture that produces nonlinear output. This architecture is called logarithmic image sensor. Some designs produce output signal which is proportional to the logarithm of the photo signal [1-2]. This type of pixel circuit is shown in figure 04.

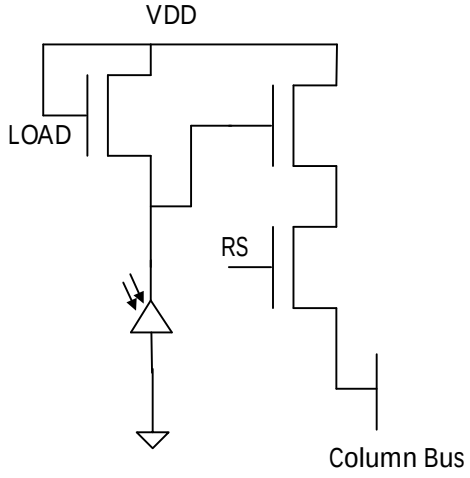


Figure 4: Logarithmic Pixel Architecture

Based on the output signal the CMOS image sensor can be divided into two types: current mode and voltage mode. Voltage mode image sensor includes a source follower transistor that buffers the photo accumulated voltage on a photodiode and produces the linear output voltage signal in the output bus [4-8]. On the other hand, current mode CMOS image sensor includes a transconductor transistor, which transforms photo accumulated voltage into a current signal [9-14]. Current mode image sensor basically used as the computational sensor because they can provide with high frame rate read-out. However, these types of image sensor have lower image quality due to high temporal and spatial noise in comparison with voltage mode imagers [15].

An typical CMOS image sensor reads and digitizes every pixel values. However, with the increase in the resolution of pictures, the number of pixels is being increased. So to reduce the power of high-resolution imager, compressive sensing technique is adopted. Here, we designed a current mode CMOS image sensor with compressive sensing.

2.3 MATHEMATICAL BACKGROUND OF COMPRESSIVE IMAGE SENSING

Compressive sensing is a intuitive method that allows us not to digitize every pixel values of CMOS image sensor. Generally, CMOS image sensor digitizes every pixel values. But with the growth of high demand in the picture's resolution, the number of pixels is being increased. As a result, it needshigh power consumption to digitize every value in a conventional way. However, by implementing compressive sensing technique on the imager, it is possible to reconstruct the picture with high fidelity.

Let’s think about the following equation:

$$y = A.x \tag{1}$$

Here, x is a vector with N elements and A is a matrix with P rows and Q columns. In generally way, x cannot be recovered from y, because A has P rows instead of needed Q rows. In

the other word, there are less number of equations (not Q number of equations). But if x becomes k sparse and A maintains certain number of conditions, we can still recover vector x with good accuracy [16-17].There are several conditions for selecting A such that x can be recovered. Those conditions are related to coherence, sparse, restricted isometry property (RIP) etc. Also to reconstruct x, there are several methods are followed, like l_1 minimization (basis pursuit), adaptive binary search, greedy pursuit etc. But for CS, RIP condition and l_1 minimization are frequently used. A matrix obeys RIP with constant δ_k if [17]

$$(1-\delta_k)\|x\|_2^2 \leq \|A.x\|_2^2 \leq (1+\delta_k)\|x\|_2^2 \quad (2)$$

Where, x is a vector with k sparse and $\|\|_2^2$ denotes l_2 – norm on R^d.

X can be recovered properly if δ_k becomes smller and remains within certain limit. δ_k indicates how well the linear equations (A.x) indicates the energy of signal x [19]. The general equation of RIP [18]

$$(1-\delta_k)\|x\|_b \leq \|A.x\|_p \leq (1+\delta_k)\|x\|_b \quad (3)$$

Here, b=1 denotes the RIP 1 and p =2 denotes RIP 2. If A matrix maintains the RIP-1 or RIP-2 conditions that signal x can be recovered properly. But if A matrix follows the RIP -1, it may not follow RIP-2 condition or vice versa [19]. Again in original form, the signal x may not be sparse. However, to make it sparse we can transform it into another basis like Fourier, Inverse Discrete Cosine Transform (IDCT). The ralation can be showed as $x = \psi.c$, where x indicates original signal, c denotes coordinate vector of x which depends on basis ψ, ψ is the sparse basis[19]. By using compressive sensing technique, if we are able to recover c, then we can easily reconstruct y from c using sparse basis ψ.

2.4 LITERATURE REVIEW

Recently CS implementation has been very popular to make the existing image sensor more power efficient and scalable. There are lots of CMOS image sensor design have already been reported, where CS is the key factor. Most of them use random measurement matrix to implement CS. They generally require adding the outputs of randomly selected pixels. And also they follow the different mechanism to implement random matrix and the summation of pixels.

Some designs uses the conventional 4T pixel sensor and per column [22]. In each x modulation cycle, the pixel cell output or generally reference voltage is used as an input of the ADC. By the way, the measurements of compressed sensing are done via a complicated column multiplexer. On the other hand, a block based CS imager was implemented in [23]. Here, they used 3T active pixel sensor and also Switched Capacitor to do an analog implementation of CS encoding in a CMOS sensor. It also uses random pixel summation for CS implementation. To do the random summation, each pixel cell includes its own read-line. These individual line affect the scalability of the whole design. Some CS imager uses weighted sum of pixel output. In [24] the correct weight is maintained by the differential voltage in row drive V_r^+, V_r^- as well as the parameter stored in the analog voltage matrix multiplier. It uses the fractional weighting system. So other CS imager uses binary weighting nodes like 1,-1 or 1 and 0. In [25] CS imager is designed with a shift register which uses the pseudo-random configuration. Also [26] uses the binary weighting values for pixel summation. Both uses LFSR (Linear Feedback Shift Register) and they have bit line I_j^+, I_j^- which values depend on the value of LFSR. In the last, Current of Two bits lines I_j^+, I_j^- are subtracted. But it involve very complicated design and there also be signal swing problems generated from adding a large number of pixels.

CHAPTER 3

STUDY OF COMPRESSIVE SENSING MEASUREMENT METHODS

3.1 INTRODUCTION OF CS MEASUREMENT OPERATION

In CS measurement, Compression is done by adding pixel value according to CS ratio. As mentioned before, people generally add pixel value randomly, which needs a very complicated circuit for implementation. For example, consider the following matrix of 8 ×8pixels which is depicted in figure 5. If we use random measurement matrix figure 6, pixel values will be added like figure 7 , whereas we see that there is no regularity in the addition of pixel values. In our design, we used the regular measurement like figure 8, whereas pixel values are added like figure 9.

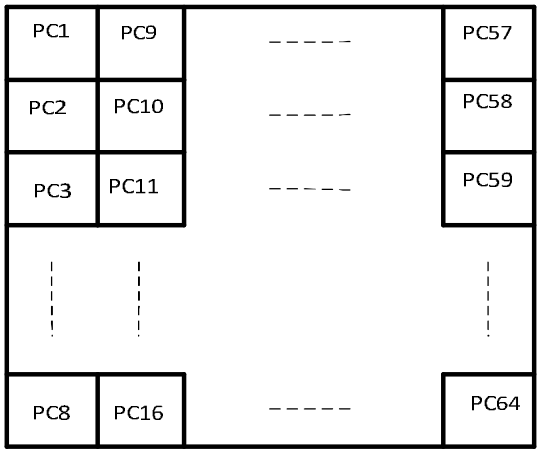


Figure 05: 8× 8 Pixel Matrix

$$\begin{pmatrix} 10110011 \\ 01001011 \\ \dots \end{pmatrix}$$

Figure 06: Random Measurement Matrix

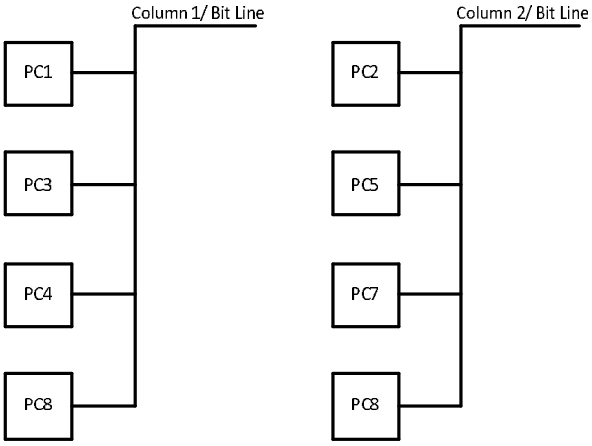


Figure 7: Pixel Cell (PC) addition for Random measurement matrix

$$\begin{pmatrix} 11110000 \\ 00111100 \\ \dots \end{pmatrix}$$

Figure 8: Regular Measurement Matrix

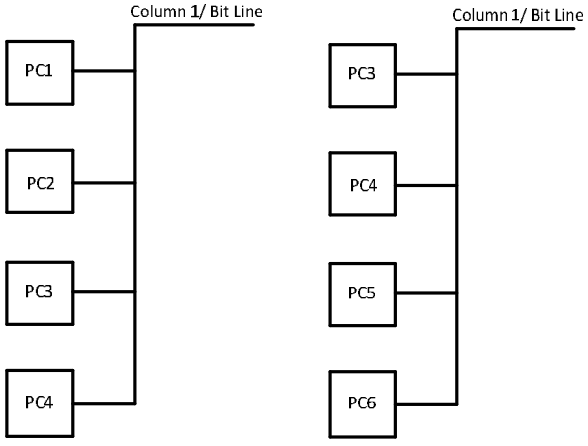


Figure 9: Pixel Cell (PC) addition for Random measurement matrix

3.2 VARIATION OF MEASUREMENT MATRIX

Measurement matrix differs according to the number of overlapping pixels. However, It has very slight effect on overall PSNR of reconstructed images. In the following, the variation of measurement matrix has been depicted for CR 4. For other CRs, the whole method would be similar.

If we consider one image of 256 × 256 pixels and divide that image into several blocks of the same size (256×16), eventually we would get 16 blocks. For each block, we would consider the same measurement matrix. For CR=4, we get a measurement matrix of size 64 ×256. However, in the measurement matrix, we can consider overlapped pixel number 0,1,2,3,4 etc. For example,

CR=4, Overlap=0, the measurement matrix:

$$\begin{pmatrix} 1111000000 \dots 000000 \\ 0000111100 \dots 000000 \\ \dots \\ 0000000000 \dots 001111 \end{pmatrix}$$

Now if we increase the number of overlapping pixel number, in the last row of measurement matrix we do not have sufficient number of pixels to add. So we can add pixel from the columns from the beginning of matrix again. Here, we call this method as Round-back. We can consider the Round-back = True or False.

CR=4, Overlap=1, Round-back = False, the measurement matrix:

$$\begin{pmatrix} 1111000000 \dots 000000 \\ 0001111100 \dots 000000 \\ \dots \\ 0000000000 \dots 001111 \end{pmatrix}$$

CR=4, Overlap=1, Round-back = True, the measurement matrix:

$$\begin{pmatrix} 1111000000 \ldots 000000 \\ 0001111100 \ldots 000000 \\ \ldots \\ 1000000000 \ldots 001111 \end{pmatrix}$$

CR=4, Overlap=2, Round-back = False, the measurement matrix:

$$\begin{pmatrix} 11111100000 \ldots 000000 \\ 00001111110 \ldots 000000 \\ \ldots \\ 0000000000 \ldots 001111 \end{pmatrix}$$

CR=4, Overlap=2, Round-back = True, the measurement matrix:

$$\begin{pmatrix} 11111100000 \ldots 000000 \\ 00001111110 \ldots 000000 \\ \ldots \\ 11000000000 \ldots 001111 \end{pmatrix}$$

CR=4, Overlap=3, Round-back = False, the measurement matrix:

$$\begin{pmatrix} 111111100000 \ldots 000000 \\ 000011111110 \ldots 000000 \\ \ldots \\ 00000000000 \ldots 001111 \end{pmatrix}$$

CR=4, Overlap=3, Round-back = True, the measurement matrix:

$$\begin{pmatrix} 111111100000 \ldots 000000 \\ 000011111110 \ldots 000000 \\ \ldots \\ 11100000000 \ldots 001111 \end{pmatrix}$$

Likewise, we consider different overlap with Round-back and not Round-back for CR = 6 and 8. We did the Matlab simulation for CR = 4, 6, and 8 with different measurement matrix. Those results are showed in Table 2, 3, 4, 5.

Table 2 PSNR with different measurement matrix for CR=4

Image	Overlap								
	0	1		2		3		4	
	RB not Possible	No RB	With RB	No RB	With RB	No RB	With RB	No RB	With RB
Lenna	36.87	37.32	37.45	37.22	37.45	36.32	37.19	36.92	36.03
Camera Man	27.46	27.81	27.83	28	28.03	27.65	27.75	27.46	26.23

Table 3 PSNR with different measurement matrix for CR=6 with total rows 42

Image	Overlap								
	0	1	2	3	4	5		6	
	RB not Possible	RB not Possible	RB not Possible	RB not Possible	RB not Possible	No RB	With RB	No RB	With RB
Lenna	32.57	32.25	27.47	34.25	33.05	33.6	33.76	29.35	30.52
Camera Man	24.84	25.17	25.04	25.61	25.2	25.3	25.29	24.61	24.69

Table 4 PSNR with different measurement matrix for CR=6 with total rows 43

Image	Overlap									
	0		1		2		3		4	
	No RB	With RB	No RB	With RB	No RB	With RB	No RB	With RB	No RB	With RB
Lenna	29.70	30.85	27.28	29.76	19.23	21.6	24.65	25.11	32.22	34.30
Camera Man	24.77	24.84	25.17	25.16	22.82	24.81	25.1	25.77	25.51	25.69

Table 5 PSNR with different measurement matrix for CR=8 with total rows 32

Image	Overlap												
	0	1		2		3		4		5		6	
	RB not Possible	No RB	With RB	No RB	With RB	No RB	With RB	No RB	With RB	No RB	With RB	No RB	With RB
Lenna	31.47	31.6	31.48	31.72	31.58	31.83	31.65	31.98	31.84	31.73	32.17	31.33	31.94
Camera Man	23.76	23.71	23.77	23.93	23.88	24.06	24.03	24.11	24.16	24.17	24.24	24.01	24.12

From the previous table 2-5, we have seen in regular measurement matrix with the variation of overlap has very slight effect on overall PSNR of reconstructed image and that is about 0.2 to 1 dB variation.

3.2 SELECTION OF MEASUREMENT MATRIX FOR DIFFERENT CRs

We basically designed our circuit for compression ratio (CR) 4,6,8. Compression ratio is described as the ratio of total number of pixels (Q) over the number of CS measurement (P). In

every design, we used images having 256 by 256 pixels (256 rows and 256 columns). Then we divided that into 16 blocks, and each block size is 256 * 16 (256 rows and 16 columns). According to [20], for CR 4, we used the regular pattern of measurement matrix whereas we added 6 neighboring pixels except the first CS measurement. The size of measurement matrix for one block is 64 * 256. The number of overlapping pixel between two CS measurement is two except the first row of measurement matrix. In the following figure 10, it has been shown.

$$\begin{pmatrix} 1110000000000000000 \dots \dots 00000000000111 \\ 0111111000000000000 \dots \dots 00000000000000 \\ 0000011111100000000 \dots \dots 00000000000000 \\ \dots \\ \dots \\ 0000000000000000000 \dots \dots 0000011111100000 \\ 0000000000000000000 \dots \dots 0000000001111110 \end{pmatrix}$$

Figure 10: Measurement Matrix for one block with

$$\begin{pmatrix} 1111111110000000000000000 \dots \dots 0000000000000000000 \\ 0000001111111110000000000 \dots \dots 0000000000000000000 \\ 0000000000001111111110000 \dots \dots 0000000000000000000 \\ \dots \\ \dots \\ 0000000000000000000000000 \dots \dots 0011111111100000000 \\ 0000000000000000000000000 \dots \dots 0000000001111111111 \end{pmatrix}$$

Figure 11: Measurement Matrix for one block with CR=6

$$\begin{pmatrix} 1111110000000000000000 \dots \dots 00000000000000000111111 \\ 0011111111111100000000 \dots \dots 00000000000000000000000 \\ \dots \dots \\ \dots \dots \\ 0000000000000000000000000 \dots \dots 00000000111111111111100 \end{pmatrix}$$

Figure 12: Measurement Matrix for one block with CR=8

For CR 6, The size of the measurement matrix is 42 * 256. we added 9 neighboring pixels in every CS measurement except the last one (last row of measurement matrix). In the last row, we added 10 neighboring pixels and every time the number of overlapping pixels is 3. It has been shown in figure 11.

Accordingly for CR 8, the size of the measurement matrix is 32 *256. In this case we added 12 neighboring pixels in every CS measurement except the first one (first row of measurement matrix).The size of measurement matrix for one block is 32 * 256. The number of overlapping pixel between two CS measurements is four except the first row of measurement matrix. It has been shown in figure 12.

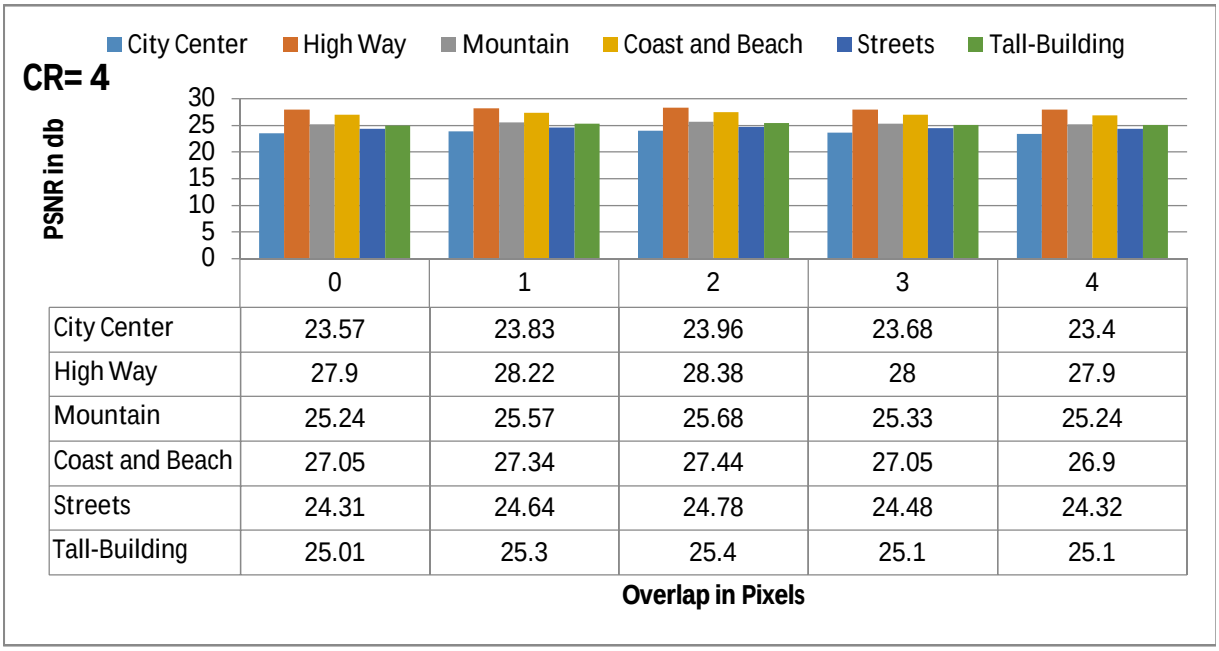
3.3 SIMULATION RESULTS WITH BENCHMARK IMAGES

In the measurement matrix for implementing CS, we used 2, 3, 4 as overlapping pixels for CR 4,6,8. By the way, the number of overlapping pixels is the pixels that remain common in two neighboring CS measurements. For example, in the following figure 13, the number of overlapping pixels is 2.

Here, we optimized the number of overlapping pixels based on the Peak Signal to Noise Ratio (PSNR) value from MATLAB simulation on individual 125 images from different six categories like City Center, Highway, Mountain, Coast and Beach, Streets and Tall Building from [27]. In the following figure 14, 15,16, the PSNR variation with the number of overlapping pixels with different image categories has been shown.

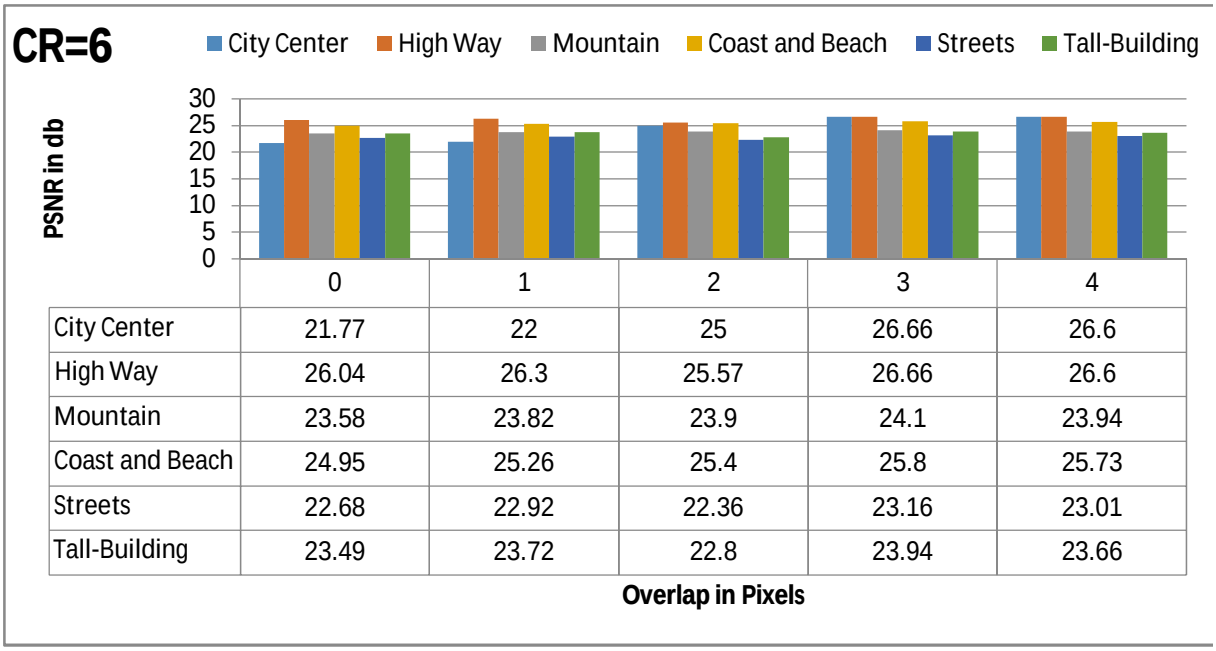
$$\begin{pmatrix} 111100000 \ldots \ldots .000000 \\ 001111000 \ldots \ldots 000000 \\ \ldots \ldots \\ 0000000 \ldots \ldots 00001111 \end{pmatrix}$$

Figure 13: Measurement matrix with 2 pixels overlap



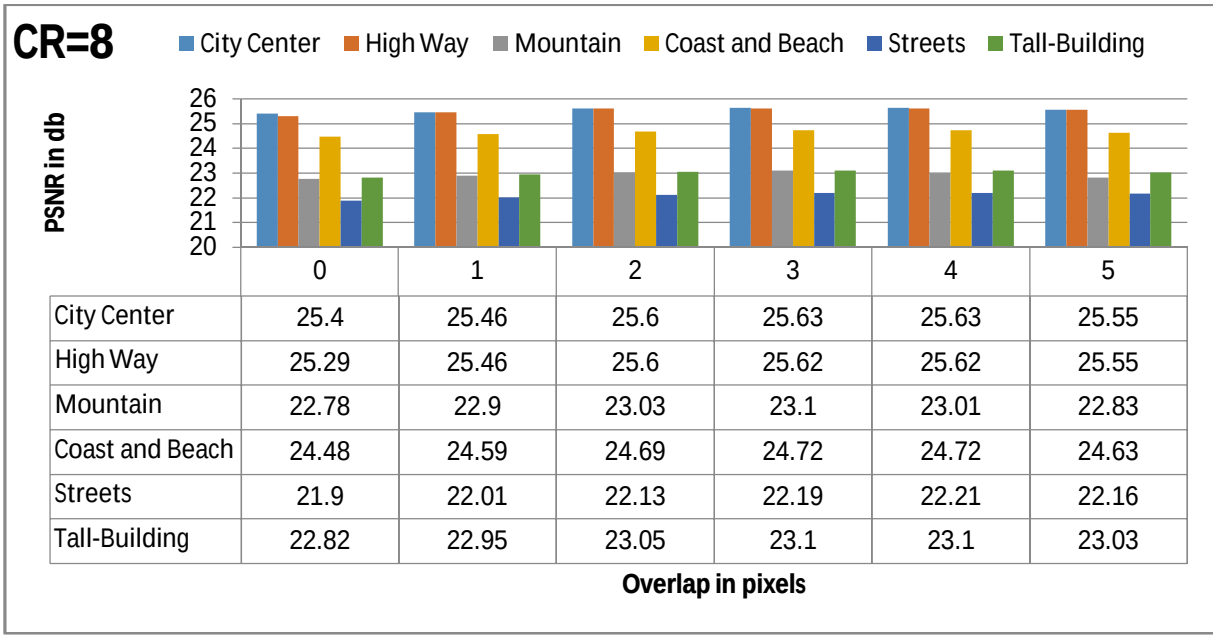
	0	1	2	3	4
City Center	23.57	23.83	23.96	23.68	23.4
High Way	27.9	28.22	28.38	28	27.9
Mountain	25.24	25.57	25.68	25.33	25.24
Coast and Beach	27.05	27.34	27.44	27.05	26.9
Streets	24.31	24.64	24.78	24.48	24.32
Tall-Building	25.01	25.3	25.4	25.1	25.1

Figure 14: PSNR with different overlap when CR=4



	0	1	2	3	4
City Center	21.77	22	25	26.66	26.6
High Way	26.04	26.3	25.57	26.66	26.6
Mountain	23.58	23.82	23.9	24.1	23.94
Coast and Beach	24.95	25.26	25.4	25.8	25.73
Streets	22.68	22.92	22.36	23.16	23.01
Tall-Building	23.49	23.72	22.8	23.94	23.66

Figure 15: PSNR with different overlap when CR=6



	0	1	2	3	4	5
City Center	25.4	25.46	25.6	25.63	25.63	25.55
High Way	25.29	25.46	25.6	25.62	25.62	25.55
Mountain	22.78	22.9	23.03	23.1	23.01	22.83
Coast and Beach	24.48	24.59	24.69	24.72	24.72	24.63
Streets	21.9	22.01	22.13	22.19	22.21	22.16
Tall-Building	22.82	22.95	23.05	23.1	23.1	23.03

Figure 16: PSNR with different overlap when CR=8

3.3 SIMULATION RESULTS OF DIFFERENT TYPES OF IMAGES

In this thesis, we designed CS imager for CR 4, 6, 8 with overlapping pixels 2,3,4 respectively. Here, we discuss the Matlab Simulation result for same CR and overlapping pixels that we used for circuit design without Round-back.

The original images are:

Figure 17: Cameraman (Original, CR=4, CR=6, CR=8)

Figure 18: Lenna (Original, CR=4, CR=6, CR=8)

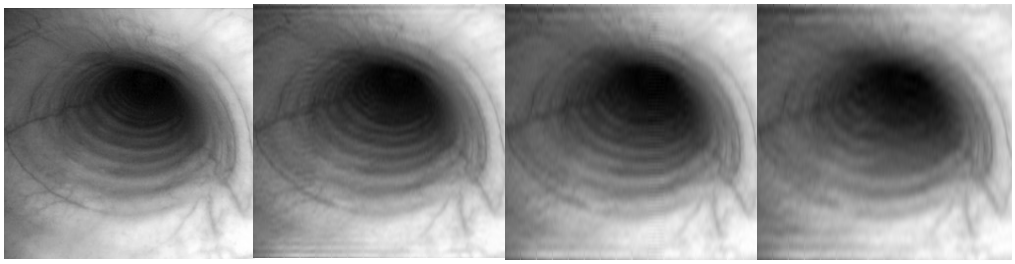


Figure 19: Medical image (Original, CR=4, CR=6, CR=8)

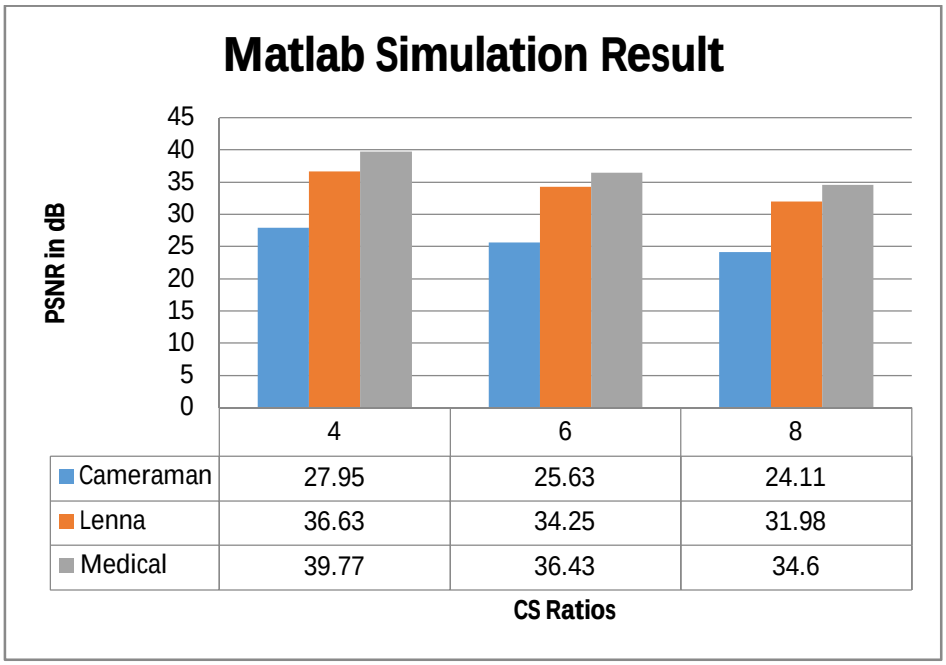


Figure 20: Matlab Simulation Result with respective PSNR.

CHAPTER 4

OPTIMAL PIXEL CELL DESIGN FOR CS OPERATION

4.1 PIXEL CELL OPTIMIZATION

In our design we used 3T APS pixel cell which is shown in figure 21. Here, PT is Pixel Transistor, AT is Access Transistor. In this design, we implemented Correlated Double Sampling (CDS) to lower the Fixed Pattern Noise (FPS), whereas we need the difference in drain current (I_{diff}) of PT when its gate voltage is at reset voltage and when is at normal pixel voltage. We always want high I_{diff} value to maintain proper noise margin. Also we need higher PSNR value to ensure higher performance. Those I_{diff} and PSNR value actually mainly depend on the size of AT, PT, Bit Voltage (V_{bit}). In this section, we discuss the optimization of pixel cell by selecting proper size of AT, PT and Bit Voltage (B_{bit}).

4.2 MODEL CIRCUIT AND EQUATION

We have a model circuit for a portion of 3T Pixel Cell, which includes PT, AT and V_{bit}. The model circuit is shown in figure 22. Here, AT is represented by R (on resistance). Also, gate

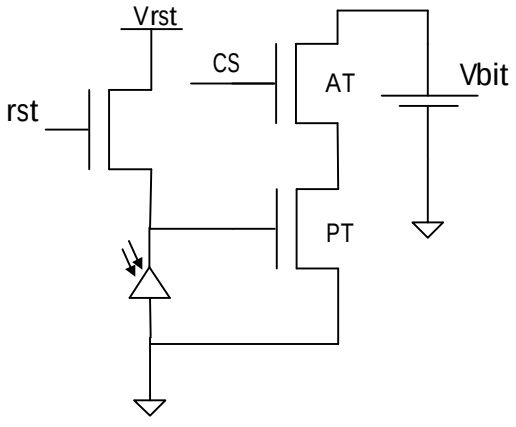


Figure 21: 3T Active Pixel Sensor

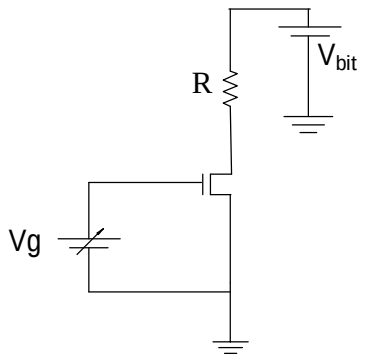


Figure 22: Model Circuit for PT, AT and V_{bit}

voltage of PT varies according to the light intensity. So, gate terminal of PT is connected with a variable voltage source Vg in figure 22.

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

$$\approx \beta[(V_g - V_{th})(V_{bit} - I_{ds}R)] \qquad [\text{If } \beta = \mu_n C_{ox}\tfrac{W}{L}]$$

$$\approx \frac{\beta V_{bit} V_{od}}{1+\beta R V_{od}} \qquad [\text{If } V_{od} = V_g - V_{th}]$$

For correlated double sampling, we get:

$$\Delta I_d = I_{ds\,(reset)} - I_{ds\,(pixel)}$$

If $V_{odr} = V_{reset} - V_{th}$ and V_Δ is the gate voltage variation due to photo diode (after integration)

$$= \frac{\beta V_{bit} V_{odr}}{1 + \beta R V_{odr}} - \frac{\beta V_{bit}(V_{odr} - V_\Delta)}{1 + \beta R(V_{odr} - V_\Delta)}$$

$$= \frac{\beta V_{bit} V_{odr}}{(1 + \beta R V_{odr})^2 - (1 + \beta R V_{odr})\beta R V_\Delta}$$

$$\Delta I_d = \frac{P}{Q - S V_\Delta} \qquad (6)$$

If we follow the above equation for image reconstruction, we can have higher PSNR. But that relation is only application for single cell connected to Bit line. Since we are designing CS

imager, we need to add multiple cells with single Bit line for implementing matrix addition. However, we did not find any equation which would correctly describe the ΔI_d when multiple cells are connected with single bit line. For that reason, we followed polynomial curve fitting approach to find out the relation (or equation) between ΔI_d and V_Δ when multiple cells are connected with bit line instead of single cell.

4.3 BIT VOLTAGE OPTIMIZATION (V_{bit})

The Bit Voltage also determines Pixel cell PSNR and I_{diff} value. If we select very high bit voltage, it would lead to higher I_{diff} and PSNR, which are desirable. However, that also leads to higher power consumption, which we want to reduce. Therefore, we need to optimize bit voltage to ensure higher PSNR and I_{diff} with not too much power consumption. Here, I_{diff} is the difference in drain current of PT, when gate of PT is in reset voltage and the voltage after photocell integration period respectively. For optimization of V_{bit}, we can consider the following figure 23

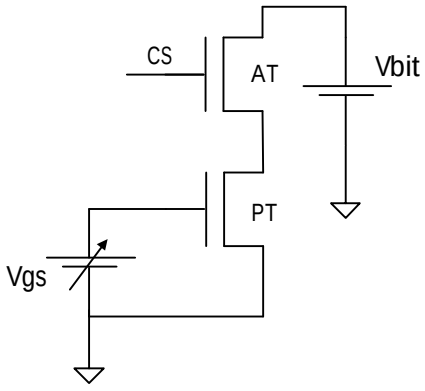


Figure 23: V_{bit} Optimization

Table 6 PSNR Values for different V_{bit}

V_{gate} Variation ,Vr (V)	PSNR (dB) @ Vbit =0.1V	PSNR (dB) @ Vbit =0.08V	PSNR (dB) @ Vbit =0.06V	PSNR (dB) @ Vbit =0.04V	PSNR (dB) @ Vbit =0.035V	PSNR (dB) @ Vbit =0.03V
0.1	63.1795	62.8770	62.6521	62.4769	62.4388	62.4028
0.2	56.8203	55.6094	54.7191	54.0225	53.8698	53.7241
0.3	49.1408	51.7098	53.2859	53.5200	53.3991	53.2267
0.4	34.3811	36.2072	38.0864	39.9814	40.4621	40.9477
0.5	26.0749	27.0862	28.2214	29.4466	29.7639	30.0857
0.6	26.0749	27.0862	28.2214	29.4466	29.7639	30.0857
0.7	26.0749	27.0862	28.2214	29.4466	29.7639	30.0857
0.8	26.0749	27.0862	28.2214	29.4466	29.7639	30.0857

According to previous discussion, figure 24-25 and table 6-7 depicts the PSNR value and I_{diff} (max) when different V_{bit} are applied and when AT (480n/120n) and PT (Thick Oxide Transistor, 360n/120n) and 130 um PDK Technology.

Table 7 Idiff (max) Values for different V_{bit}

V_{gate} Variation ,Vr (V)	Idiff (max)(A) @ Vbit =0.1V	Idiff (max)(A) @ Vbit =0.08V	Idiff (max)(A) @ Vbit =0.06V	Idiff (max)(A) @ Vbit =0.04V	PSNR (dB) @ Vbit =0.035V	PSNR (dB) @ Vbit =0.03V
0.1	0.1965E-5	0.1581E-5	0.1192E-5	0.0798E-5	0.0699E-5	0.0600E-5
0.2	0.3994E-5	0.3224E-5	0.2438E-5	0.1638E-5	0.1435E-5	0.1233E-5
0.3	0.5856E-5	0.4763E-5	0.3624E-5	0.2447E-5	0.2148E-5	0.1847E-5
0.4	0.7141E-5	0.5889E-5	0.4536E-5	0.3095E-5	0.2723E-5	0.2347E-5
0.5	0.7640E-5	0.6356E-5	0.4949E-5	0.3419E-5	0.3017E-5	0.2608E-5
0.6	0.7640E-5	0.6356E-5	0.4949E-5	0.3419E-5	0.3017E-5	0.2608E-5
0.7	0.7640E-5	0.6356E-5	0.4949E-5	0.3419E-5	0.3017E-5	0.2608E-5
0.8	0.7640E-5	0.6356E-5	0.4949E-5	0.3419E-5	0.3017E-5	0.2608E-5

From figure 24 and 25, we see, PSNR and I_{diff} decrease with the decrease of V_{bit}, although PSNR decreases very slightly. Since we need to lower Vbit because of lower power consumption, we chose 0.35 V for the rest of our design which provides 2.723 uA at gate voltage variation 0.4 V. Basically, gate voltage variation 0.4 V is enough for us, we do not go beyond 0.4V (0.1 to 0.4).

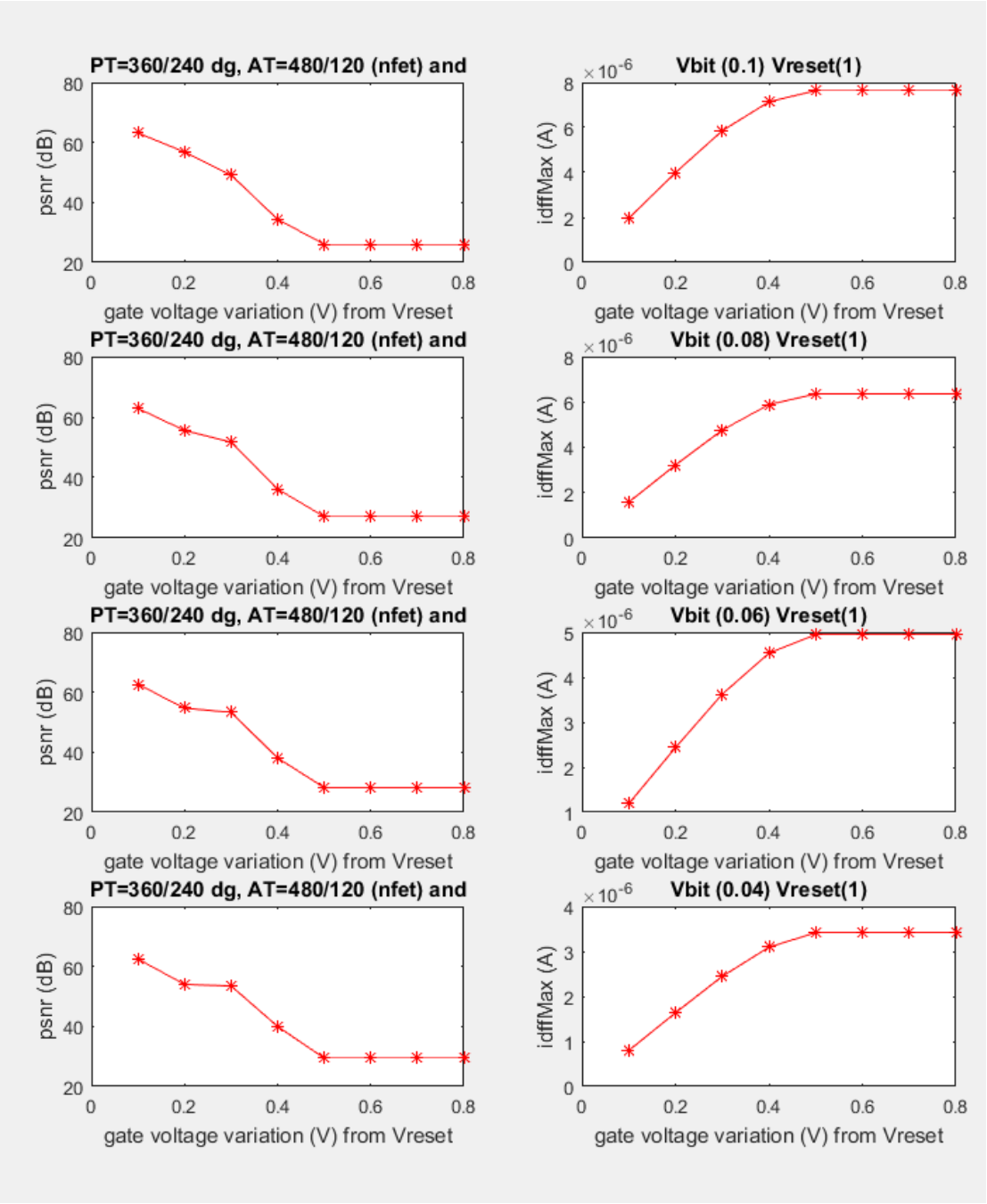


Figure 24: PSNR and I_{diff}variation with V_{gate} Variation (Vbit 0.1 to 0.04V)

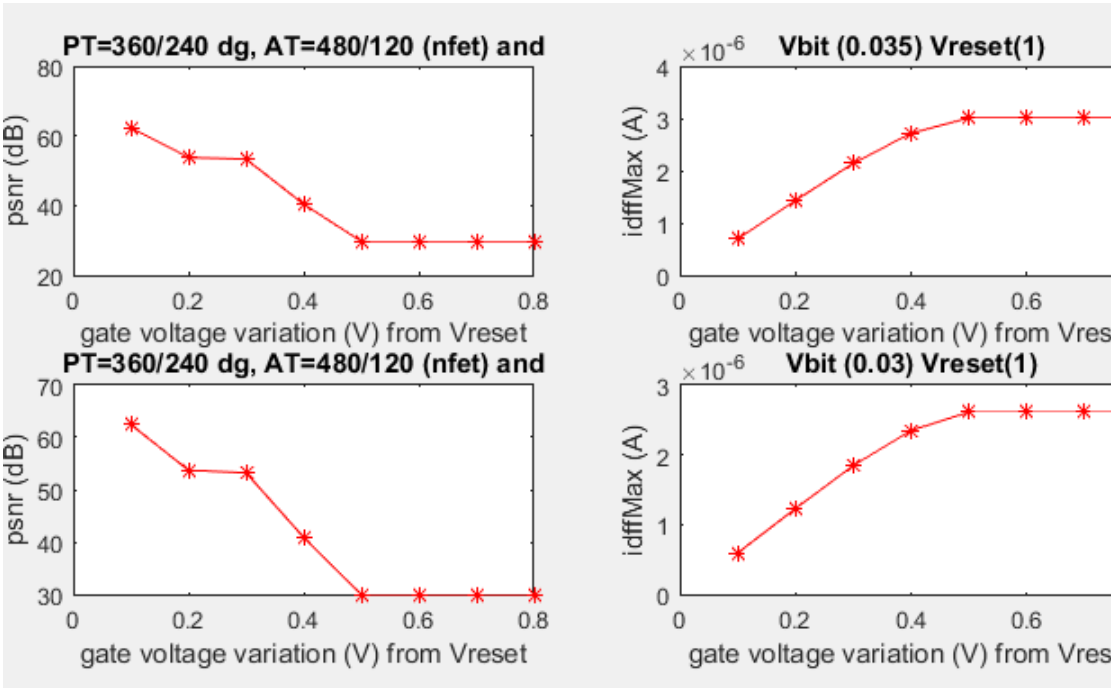


Figure 25: PSNR and I_{diff}variation with V_{gate} Variation (Vbit 0.035 to 0.03V)

Table 8 I_{diff} (max) for different width of PT

V_{gate} Variation ,Vr (V)	Idiff (max)(A) @ PT=360/240	Idiff (max)(A) @ PT = 380/240	Idiff (max)(A) @ PT=400/240
0.1	0.0699E-05	0.0736E-05	0.0773E-05
0.2	0.1436E-05	0.1515 E-05	0.1593E-05
0.3	0.2148E-05	0.2271E-05	0.2393E-05
0.4	0.2724E-05	0.2886E-05	0.3046E-05
0.5	0.3017E-05	0.3203E-05	0.3385E-05
0.6	0.3017E-05	0.3203E-05	0.3385E-05
0.7	0.3017E-05	0.3203E-05	0.3385E-05
0.8	0.3017E-05	0.3203E-05	0.3385E-05

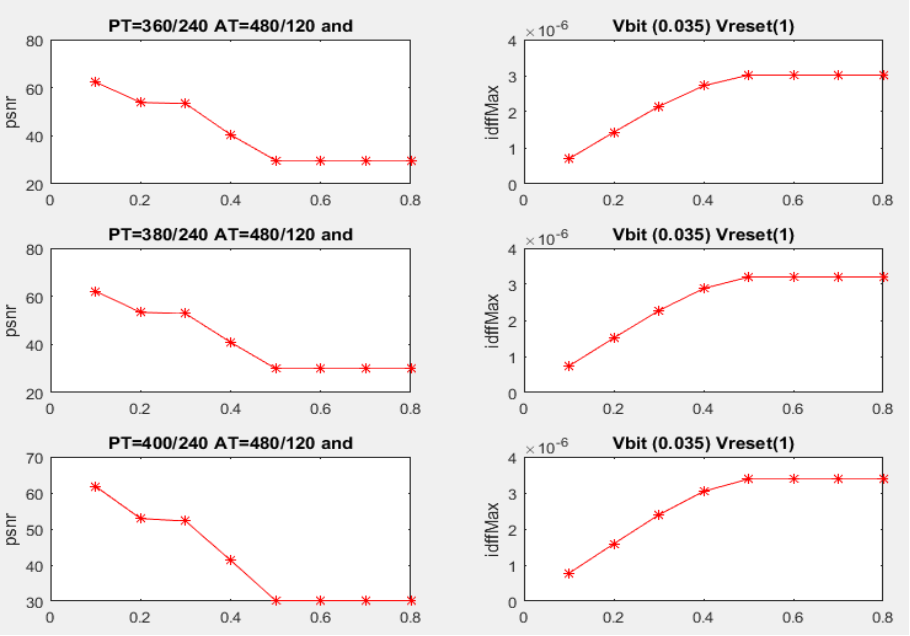


Figure 26: PSNR and $I_{diff(max)}$ variation with V_{gate} Variation (PT, W=360n to 400n)

Table 9 PSNR Values different widths of PT

V_{gate} Variation ,Vr (V)	PSNR (dB) @ PT=360/240	PSNR (dB) @ PT = 380/240	PSNR (dB) @ PT=400/240
0.1	62.4437	62.1303	61.8439
0.2	53.8773	53.3668	52.9168
0.3	53.4067	52.8162	52.2004
0.4	40.4577	40.9150	41.3184
0.5	29.7623	29.9851	30.1761
0.6	29.7623	29.9851	30.1761
0.7	29.7623	29.9851	30.1761
0.8	29.7623	29.9851	30.1761

4.4 TRANSISTOR SIZING (PT):

The size of pixel transistor also determine overall PSNR value of pixel cell and I_{diff}. Table [8-9] and figure 26 show the variation of PSNR and I_{diff} (max) with the width of pixel transistor. We see, with the increase of width, the PSNR value decrease although $I_{diff\ (max)}$increases. We see $I_{diff\ (max)}$ is 2.7 uA (what is quite enough) even when Vgate variation is 0.4V at PT(360n/240n). So, we keep our transistor size of PT as (360n/240n). Again, PT length variation has effect on overall PSNR and $I_{diff(max)}$. Table 10-11 and figure 27 show the variation of PSNR and $I_{diff(max)}$ with the change in length of PT. We see, with the increase of Length of PT, the PSNR value increase slightly but $I_{diff(max)}$ increases decreases about 0.15 to 0.17 uA. So, we keep our PT length 240nm.

Table 10 I_{diff} (max) for different Length of PT

V_{gate} Variation ,Vr (V)	Idiff (max)(A) @ PT=360/240	Idiff (max)(A) @ PT = 360/260	Idiff (max)(A) @ PT=360/280	Idiff (max)(A) @ PT=360/300
0.1	0.0699E-05	0.0654E-05	0.0615E-05	0.0580E-05
0.2	0.1436E-05	0.1341E-05	0.1259E-05	0.1187E-05
0.3	0.2148E-05	0.2008E-05	0.1885E-05	0.1777E-05
0.4	0.2724E-05	0.2550E-05	0.2399E-05	0.2267E-05
0.5	0.3017E-05	0.2829E-05	0.2667E-05	0.2526E-05
0.6	0.3017E-05	0.2829E-05	0.2667E-05	0.2526E-05
0.7	0.3017E-05	0.2829E-05	0.2667E-05	0.2526E-05
0.8	0.3017E-05	0.2829E-05	0.2667E-05	0.2526E-05

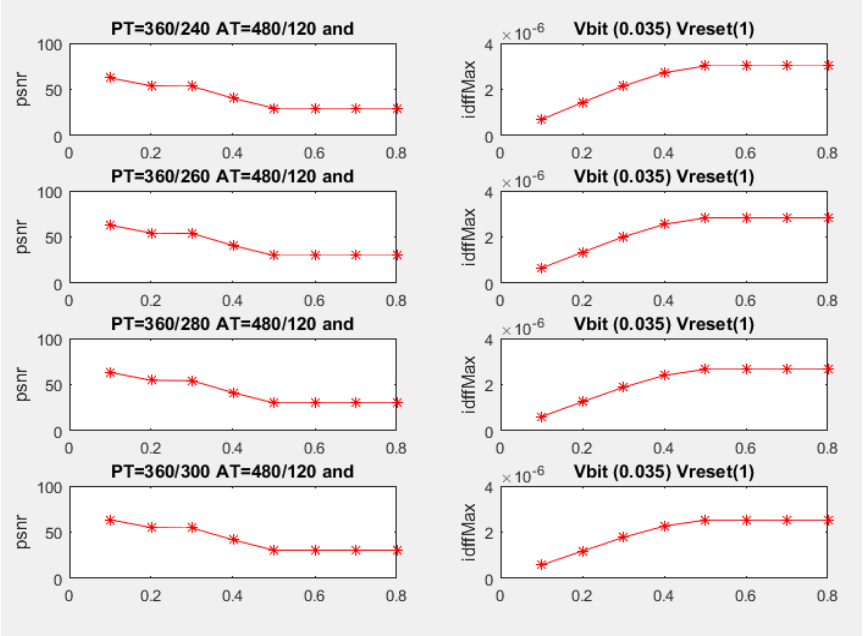


Figure 27: PSNR and $I_{diff(max)}$ variation with V_{gate} Variation (PT, L=240n to 300n)

Table 11 PSNR Values different lenghts of PT

V_{gate} Variation ,Vr (V)	Idiff (max)(A) @ PT=360/240	Idiff (max)(A) @ PT = 360/260	Idiff (max)(A) @ PT=360/280	Idiff (max)(A) @ PT=360/300
0.1	62.4437	62.8791	63.2748	63.6349
0.2	53.8773	54.3370	54.7295	55.0621
0.3	53.4067	53.8706	54.2646	54.5904
0.4	40.4577	40.8354	41.2742	41.7712
0.5	29.7623	29.9590	30.2062	30.5014
0.6	29.7623	29.9590	30.2062	30.5014
0.7	29.7623	29.9590	30.2062	30.5014
0.8	29.7623	29.9590	30.2062	30.5014

CHAPTER 5

CS IMAGE SENSOR DESIGN WITH DIFFERENT CR

5.1 OPTIMAL IMAGE SENSOR CIRCUIT AND TRANSISTOR SIZING

Our CMOS image sensor circuit is composed of three parts, 3T Pixel cell, Current Conveyor, and DDS and TIA. Here, we would discuss about those sections. The figure [28] shows the image sensor circuit with one pixel.

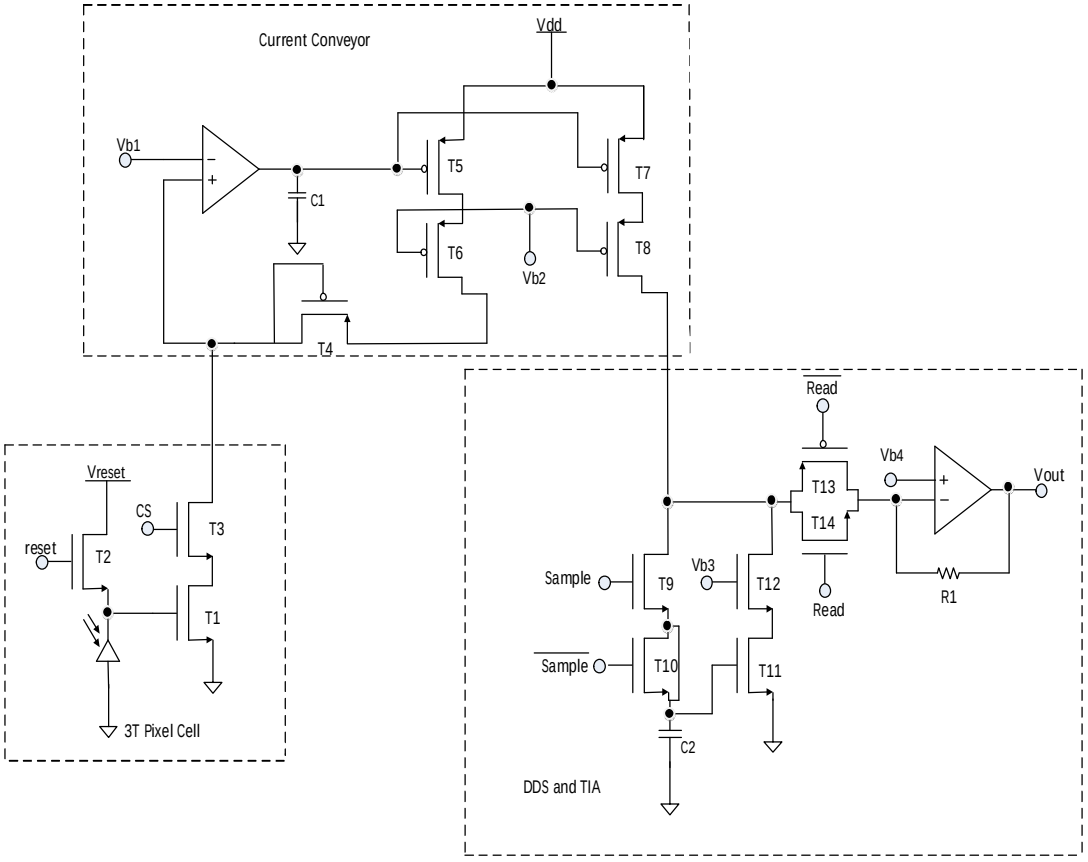


Figure 28: Image sensor circuit with single pixel

3T Pixel cell is consists of one switching transistor T2, access transistor T3, one pixel transistor T1, and a photodiode. Accroding to the pulse reset, T2 resets photodiode voltage or the gate voltage of T2. T3 is used to select the column of the pixel array and connect it to the bit line.On the other hand, the current conveyor is used to copy the bit line current and pass it in different output lines. It has one input, although the number of output varies depending on the compression ratios. In figure [28] It has one input and one output. It consists of an amplifier A1, diode-connected transistor T4, cascaded current mirror (consists of T5, T6, T7, T8). To copy current very precisely, T6 and T8 drain voltage should be same.T4 transistor is used to make the drain voltages of T6 and T8 are equal. The third part of our image sensor circuit is DDT and TIA. Here to remove the final pattern noise we used the DDS (Delta double semple) [28]. Here, At first it samples the pixel current I_1 in normal phase and again it sample the pixel output current I_2 in reset phase. Then two currents are deducted and finally the difference of both currents is fed up to trans-impedance amplifier (TIA). The output voltage V_{out}varies linearly with the difference between I_1 an I_2 value. Table 12 shows the sizes of transistor showed in figure 27, DC bias voltage and other parameters. Figure 28 also contains two amplifier A1 and A2. A1 is a one stage operational amplifier and A2 is the two-stage operational amplifier.

There are several control signals such as CS_i, $reset_i$, Sample, read are used in this circuit. we used two types of clock signal (CLK 1 and CLK 2) and D flip-flop to generate those control signal. Figure 29 shows the circuit of those control signal generation and figure 30 shows actual control signal waveforms.

Table 12 Instance name and values

Instances	Values
T2*, T1*	360n/240n
T3	480n/120n
T4	2.1u/360n
T5, T6, T7, T8	7.2u/360n
T9	640n/120n
T10	320n/120n
T12	1.8u/360n
T11	1.77u/2.15u
T13, T14	1.6u/120n
R1	15k
C1, C2	100f
V_{b1}	35m
V_{b2}	600m
V_{b3}	750m

* Thick Oxide transistor

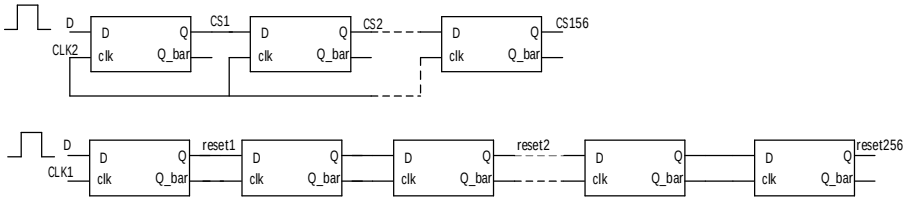


Figure 29: reset and CS signal generation circuit

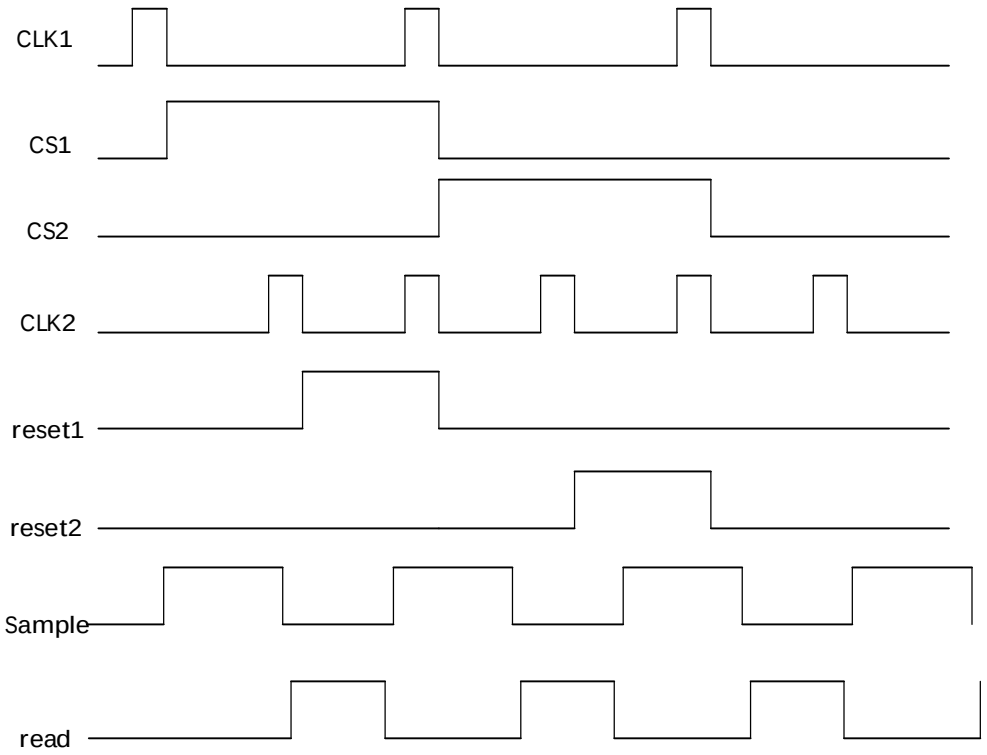


Figure 30: Control Signal waveforms

Table 13 Amplifier A1 and its Characteristics

Gain	54.368 dB
-3dB frequency	11.08 kHz
Phase Margin	75 deg

Table 14 Amplifier A2 and its Characteristics

Gain	78.049 dB
-3dB frequency	12.38 kHz
Phase Margin	102.44 deg

5.2 COMPRESSION RATIO 4

For compression ratio 4, we used regular measurement matrix with 64 rows and 356 columns. In our design, we implement CS measurement block by block. That means we divide the whole image into several equal sized blocks. For every compression ratio, we use the block size is 156 ×16. Therefore, from an image having 256 *256 arrays, we would get 16 blocks. In CS 4, we add 6 neighboring pixel values whereas two are overlapping pixels. In the circuit, this addition is implemented in two places, before Current conveyor (CC) and after the CC. For CS4 we added two-pixel values with one another and then we did another addition after the CC operation, basically, we added three outputs of CC outputs. As a result, we get 64 number of outputs instead of 256. In this way, the data is compressed. Figure 31 shows a block diagram showing how we add the pixel values.

5.3 COMPRESSION RATIO 6

For compression ratio 6, the size of the measurement matrix is 42 *256. we add 9 neighboring pixel values in one column whereas the number of overlapping pixel is three. Before that the current conveyor operation, we add 3pixels values and after the current conveyor, we add three current conveyor's outputs together. So that we get 43 output instead of 256.Figure 32 shows a block diagram for CR 6.

5.4 COMPRESSION RATIO 8

In compression ratio 8, we add 12 neighboring pixel values whereas the four are overlapping pixels. To implement the CR 8, we add two pixels values before the current conveyor and after the current conveyor, we add six outputs of current conveyors together. As a result, we find 32 number of output.Figure 33 shows whole block diagram showing how the pixel values are added in the circuit.

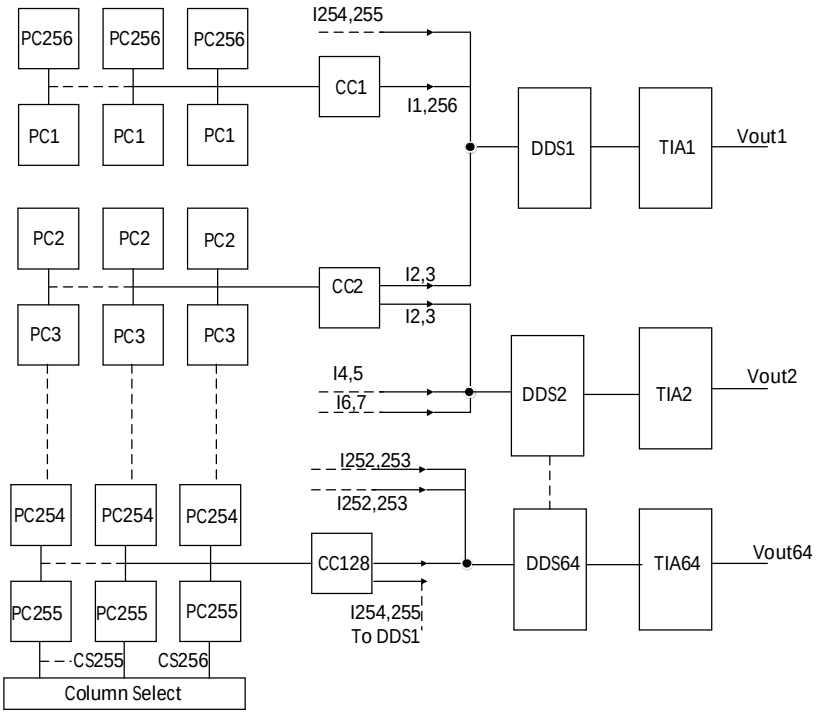


Figure 31: Block diagram for CR 4

5.5 RESULTS

From the previous table 15, we have observed that the PSNR for reconstructed image has been increased approx. 5 to 7 dB, if we use the regular matrix instead of a random matrix. Also, it relaxed the extra required hardware to implement the random measurement matrix. So, the overall design has been more scalable and power efficient.

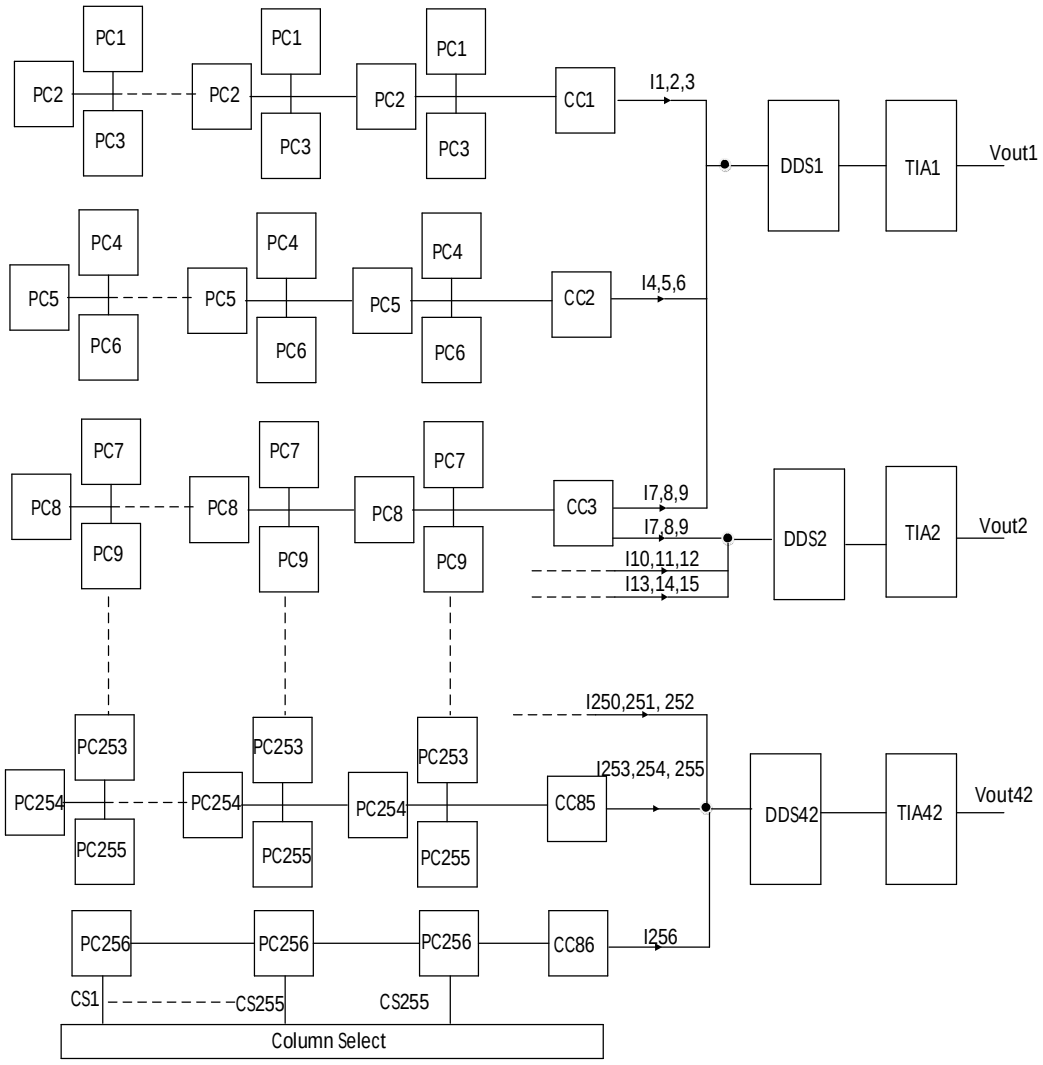


Figure 32: Block diagram for CR 6

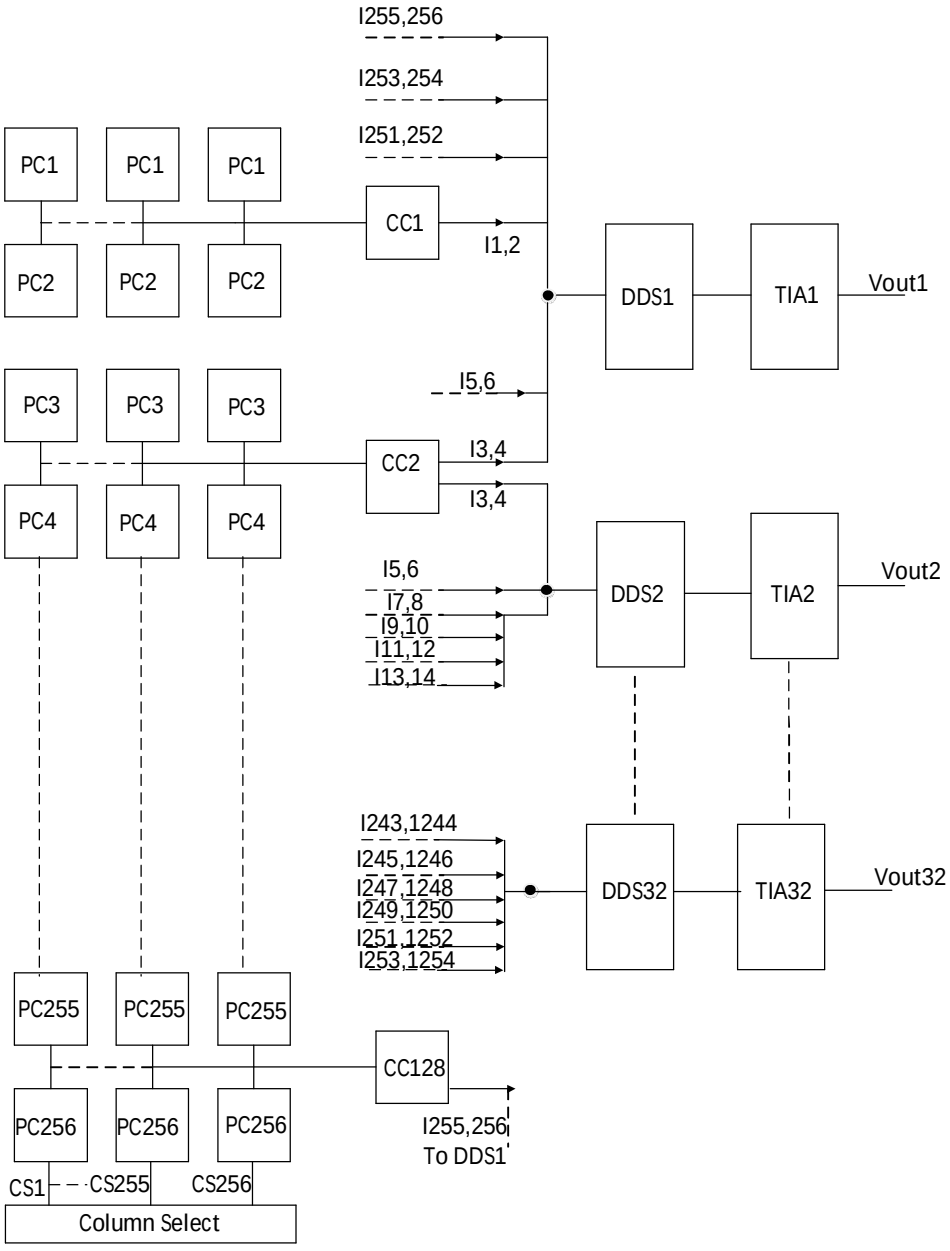


Figure 33: Block diagram for CR 8

Table 15 PSNR Values for different images with different CR and measurement matrix.

CR	Image	Measurement Matrix	PSNR
4	Cameraman	Random	22
4	Cameraman	Regular	28
4	Lenna	Random	30.25
4	Lenna	Regular	37.64
6	Cameraman	Random	19.9
6	Cameraman	Regular	25.44
6	Lenna	Random	27.49
6	Lenna	Regular	33.29
8	Cameraman	Random	18.73
8	Cameraman	Regular	24.16
8	Lenna	Random	25.83
8	Lenna	Regular	32.44

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 SUMMARY

In this work, we investigated different variations of regular measurement matrixes to be used in CS image sensors. These variations include the number of pixels overlapped between two adjacent measurement groups as well as if the last measurement group should include pixels at both ends of the pixel array, which is referred to as round-back in the thesis. Extensive simulations were conducted with a large number of benchmark images. Simulation results show that having an overlap of CR/2 typically leads to the best image quality, where CR is the compression ratio. It also shows that round-back having negligible impact on the quality of the reconstructed image, Hence, it is recommended not to have round-back in the measurement matrixes for the consideration of simplified hardware structure.

In addition, extensive circuit simulations were conducted to find the optimal pixel cell design for CS image sensors. Two or three sentences to summarize the finding. Based on the outcomes from these optimization studies, three CS image senor circuits with compression ratios of 4, 6, and 8 are designed with using a 130 nm CMOS technology. The size of pixel arrays used in these sensors is 256×256. The circuit operate with a power supply voltage of 1.5V. Circuit simulations with benchmark image Lenna show that the three images sensors can achieve PSNR values of 37.64dB, 33.29dB, and 32.44dB for CR= 4, 6 and 8 respectively. With benchmark image Cameraman, the achieved PSNR values by the three sensors are 28dB, 25.44dB and 24.16dB for CR =4, 6, and 8 respectively. Compared to convention CS images with using conventional random measurement matrixes, PSNR improvement is about 5 to 7dB increase.

6.2 FUTURE WORK

In this work, individual CS image sensors with CR of 4, 6 and 8 are developed. Future efforts can be directed towards a single CS image sensors with programmable compression ratios. So users can select desirable CR values according to different requirements.At present, only gray scale images are used in the study and the CS image sensor circuits are designed for gray scale images. Future study can investigate how to apply the developed techniques to CS image sensors that capture color images.

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