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Digital LDO modelling techniques for performance estimation at early design stage

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Abstract: This work studies the transient responses and steady-state ripples of digital low dropout (LDO) voltage regulators. Simulation models as well as closed-form expressions are provided for estimating the LDO output settling behaviour after load current or reference voltage changes. Estimation equations for the magnitude and frequency of LDO output steady-state ripples are also presented. The accuracy of the developed models is verified by comparing estimation data with results obtained from circuit simulations. The use of the developed estimation equations in design space exploration is also demonstrated.

1 Introduction

With the wide use of fine-grain power management in modern VLSI circuits [1, 2], digital low dropout (LDO) voltage regulators are gaining significant research interests and a large number of digital LDO circuits are recently reported [3–17]. The transition from analog to digital LDOs is mainly due to the difficulties in designing power-efficient high-gain amplifiers at low-voltage and advanced technology nodes. Such high-gain amplifiers are crucial in analogue LDOs for minimising the difference between the LDO output voltage and input reference V_{ref}. Such difference is called error voltage and denoted as V_{err} [18].

In digital LDO circuits, comparators [3] or voltage controlled oscillators [4] are often used to detect or measure V_{err}. Also, instead of a single large power device, a digital LDO uses an array of small power transistors, which can be individually controlled by digital signals. Fig. 1 shows a simplified digital LDO circuit to illustrate its operation [3]. If the LDO output is higher than V_{ref}, the comparator output will cause the digital control logic to decrease the number of conducting power devices; otherwise, the control circuit turns on more power devices. By this feedback mechanism, the digital LDO output is kept at the level of V_{ref}.

Unlike the high-gain amplifier in an analogue LDO circuit, whose output is proportional to V_{err}, the comparator in a digital LDO circuit only detects if $V_{err} > 0$ or $V_{err} < 0$. As a result, the feedback factor of the digital LDO control loop is not constant, making it more challenging to derive the closed-loop transfer function of the digital LDO control loop. Meanwhile, estimating digital LDO transient behaviour from its open-loop transfer function is not accurate because previously established methods for predicting transient behaviour from open loop transfer functions are all based on the assumption that the feedback factor does not change during the system settling process [19]. Our early work developed a piecewise analytical model for predicting digital LDO output settling behaviour after a load change [20]. With approximating the on-resistance of the power devices as constant R, closed-form expressions for estimating the maximum ripple voltage and settling time are derived [20]. In this work, the previous piecewise analytical model is improved by considering the dynamic changes of the equivalent on-resistance of the power device array. Also, the model is extended to predict the LDO transient behaviour after voltage reference changes. Furthermore, this work studies the steady-state output ripples and presents estimation equations for ripple magnitude and frequency. The accuracy of the developed models and equations is validated by comparing with circuit simulations. The use of the developed model for early design space exploration is also demonstrated.

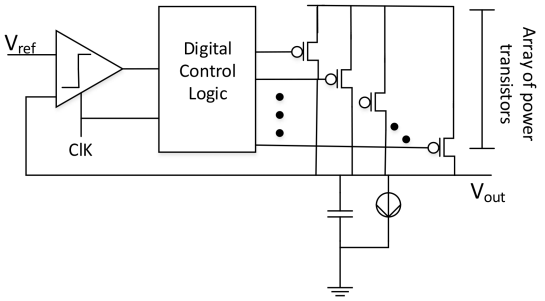

Fig. 1 *Simplified digital LDO circuit*

This paper is organised as follows: Section 2 reviews related work on modelling digital LDO circuits. The model developed in our early work is also briefly discussed in this section. The improved model that considers the changes of equivalent on-resistance of the power device array is discussed in Section 3. Techniques to model LDO transient behaviour in responding to reference voltage changes are presented in Section 4. Methods for estimating digital LDO steady-state ripples are described in Section 5. The validation of the developed models and the application of the models in design space exploration are presented in Section 6. The paper is concluded in Section 7.

2 Related work

A number of works that develop analytical models for LDO circuits have been reported in literature. In [21, 22], comprehensive frameworks for analysing the stability of LDOs with active feedback compensation techniques are presented. Also, techniques for modelling LDO susceptibility to electromagnetic interference are discussed in [23]. Complimentary to these techniques, this work develops models for estimating digital LDO transient behaviours, such as ripple magnitudes after load current or voltage reference changes. Recently, various techniques to enhance LDO transient response, such as using dual control loops in [22], dynamic biasing in [24], or event-driving logic in [25], have been reported. Such enhance techniques can be included LDO modelling as shown in [22, 25].

To capture the discrete-time behaviour of circuit blocks used in digital LDOs, z-domain models are often used in digital LDO models. For the circuit shown in Fig. 1, the comparator and the control logic can be modelled by z-domain expressions. Meanwhile, the circuit at the LDO output node is a continuous-time circuit that can be described by an s-domain function. Fig. 2 shows the system-level model of the digital LDO, assuming that the digital control logic is implemented by bi-directional shift

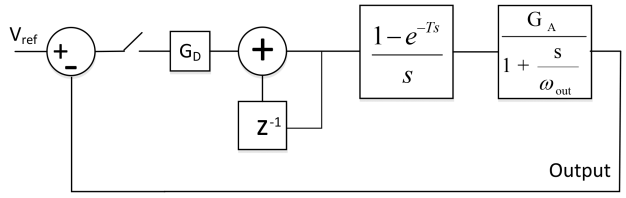

Fig. 2 *Digital LDO system-level model [6]*

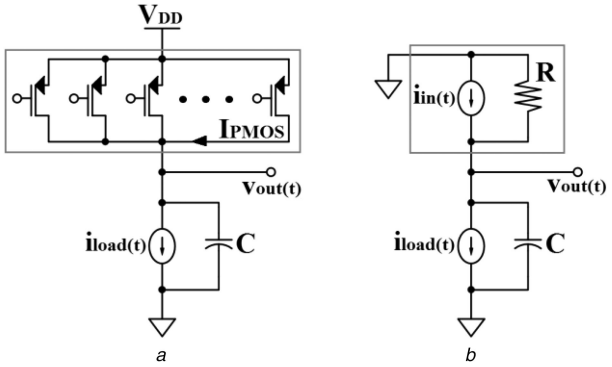

Fig. 3 *Circuit model for LDO output node*
(a) LDO output node circuit, ***(b)*** Simplified circuit model

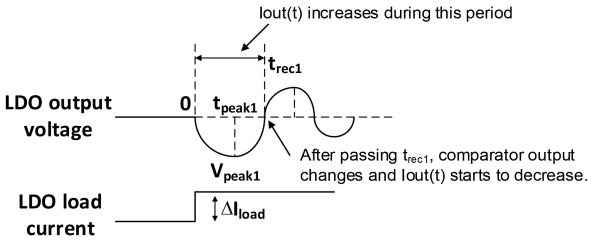

Fig. 4 *LDO output response to a load current increase*

registers [3]. In the model, the comparator is represented by a subtraction operation. The output of the control logic is effectively the accumulation of the comparator output over time and hence is modelled by a digital integrator followed by a zero-order hold function. G_D represents the gain of the control logic, which is larger than one when LDO transient response enhancement techniques are used.

The LDO output node is modelled by a first-order linear system with transfer function $(G_A/1 + (s/\omega_{\text{out}}))$, where $\omega_{\text{out}} = (1/R \cdot C)$, R and C are the LDO output resistance and load capacitance, respectively. G_A is the proportional constant that relates the numerical value of the digital control output and the LDO output voltage. By translating the above s-domain expressions into z-domain functions, the z-domain open-loop transfer function of the digital LDO can be derived as [6]

$$\text{TF}(z) = \frac{G_{\text{D}} \cdot G_A}{(z-1)\left(z - \text{e}^{-(\omega_{\text{out}}/f_{\text{clk}})}\right)} \tag{1}$$

where f_{clk} is the clock frequency of the circuit. The open-loop transfer function has two poles: one is located at the unit cycle and the other is at $\text{e}^{-(\omega_{\text{out}}/f_{\text{clk}})}$. The expression of the second pole reveals some insights about the digital LDO settling behaviour as discussed in [6]. Alternatively, if we substitute z^{-1} by $\text{e}^{-s/f_{\text{clk}}}$, the above transfer function can be translated into an s-domain expression and it is used to study the LDO stability in [5]. Nevertheless, the difficulty to use such open-loop transfer functions to predict digital LDO transient responses after load or reference changes is that the feedback factor is not constant during the settling process as discussed earlier.

The piecewise analytical model developed in [20] focuses on the voltage and current relation in time domain. It models the LDO output node using the circuit in Fig. 3*b*. Following the small signal analysis principle, it treats steady values as 0 and focuses on the changes of signals. Hence

$$i_{\text{in}}(t) - \frac{v_{\text{out}}(t)}{R} = i_{\text{load}}(t) + C \cdot \frac{\text{d}(v_{\text{out}}(t))}{\text{d}t} \tag{2}$$

$$\frac{\text{d}(i_{\text{in}}(t))}{\text{d}t} = \kappa \cdot I_{\text{PMOS}} \cdot f_{\text{clk}} \tag{3}$$

where i_{in} and i_{load} are the currents conducted by the power devices and the load current, respectively; R is the equivalent on-resistance of the combined conducting power devices; I_{PMOS} is the current conducted by a single power transistor; and κ is 1 or −1 depending on whether the number of conducting power transistors is increasing or decreasing. Both this approach and the modelling techniques in [25] start from the current and voltage relation in time domain. However, they focus on different perspectives of LDO operation and use different analysis methods. The discussion in [25] focuses on LDO stability and relies on a state space model. Our model in [20] focuses on LDO settling parameters and involves deriving piecewise expressions to approximate LDO output waveforms.

Fig. 4 illustrates the LDO output response to a step increase on the load current. Immediately after the load current increase, the LDO output $V_{\text{out}}(t)$ becomes lower than V_{ref} and the LDO starts to turn on more power devices, hence $\kappa = 1$. When $V_{\text{out}}(t)$ reaches its valley denoted by V_{peak1} in Fig. 4, $i_{\text{in}}(t)$ is increased to the level of $i_{\text{load}}(t)$. However, the LDO will continue to increase $i_{\text{in}}(t)$ before $V_{\text{out}}(t)$ crossing the V_{ref} level; and the extra current helps bring $V_{\text{out}}(t)$ back to the desired V_{ref} level. After $V_{\text{out}}(t)$ exceeds the V_{ref} level at time t_{rec1}, $V_{\text{out}}(t)$ will continue to increase because $i_{\text{in}}(t) > i_{\text{load}}(t)$. Meanwhile, the LDO starts to decrease the number of conducting power devices and $\kappa = -1$. This mechanism leads to the voltage ripples at the LDO output when it responds to a load current change.

Owing to the changes of κ value, the $V_{\text{out}}(t)$ expression has to be derived in a piecewise manner. For the example illustrated in Fig. 4, the $V_{\text{out}}(t)$ expression during the time period from 0 to t_{rec1} can be derived as [20] (see (4)) where

$$\begin{aligned} X &= -\Delta i_{\text{load}} \cdot R - I_{\text{PMOS}} \cdot f_{\text{clk}} \cdot R^2 \cdot C \\ Y &= I_{\text{PMOS}} \cdot f_{\text{clk}} \cdot R \\ Z &= \Delta i_{\text{load}} \cdot R^2 \cdot C + I_{\text{PMOS}} \cdot f_{\text{clk}} \cdot R^3 \cdot C^2 \end{aligned} \tag{5}$$

With the help of the above equations, the peak voltage value V_{peak1} and the time that it reaches the peak, t_{peak1}, during this selected time period can be solved by $(\text{d}v_{\text{out}}(t)/\text{d}t) = 0$. Similarly, the voltage peaks and their corresponding times within other time periods can be derived. The work in [20] also shows that the peaks of the voltage ripples in LDO settling process decay exponentially with time and an expression for estimating LDO settling time after load change is also derived.

3 Modelling LDO transient response to load current change

The previous piecewise analytical model [20] assumes that R has a constant value during the LDO output transition period. Since R is

$$\begin{aligned} v_{\text{out}}(t) &= X + Y \cdot t + \frac{Z}{R \cdot C}\text{e}^{-(t/R \cdot C)} \\ &= I_{\text{PMOS}} \cdot f_{\text{clk}} \cdot R \cdot t - \left(\Delta i_{\text{load}} \cdot R + I_{\text{PMOS}} \cdot f_{\text{clk}} \cdot R^2 \cdot C\right) \cdot \left(1 - \text{e}^{-(t/R \cdot C)}\right) \end{aligned} \tag{4}$$

affected by the number of conducting power transistors, which can change dramatically in responding to large load changes, the actual R value in real circuits often exhibits large changes in LDO output settling process. This section enhances the early model by considering such changes on R value. In the following discussion, we use $R(t)$ to denote the equivalent on-resistance of the power device array. For a digital LDO circuit with relatively high input voltage, e.g. $V_{\mathrm{DD}} \geq 0.7\,\mathrm{V}$ [4, 5, 8], the conducting power devices typically operate in linear region and hence these devices can be treated as resistors and the equivalent on-resistance can be estimated as

$$R(t) = \frac{V_{\mathrm{DD}} - V_{\mathrm{out}}(t)}{I_{\mathrm{in}}(t)} \tag{6}$$

However, when the LDO is operating with a very low input voltage [3, 6, 9], the conducting power devices are likely operating in saturation region. The output resistance of a single conducting power device is $r_{\mathrm{o}} = (V_{\mathrm{A}}/I_{\mathrm{PMOS}})$, where V_A is the Early voltage of the MOS device. Thus

$$R(t) = \frac{V_{\mathrm{A}}}{I_{\mathrm{PMOS}} \cdot N(t)} = \frac{V_{\mathrm{A}}}{I_{\mathrm{in}}} \tag{7}$$

where $N(t)$ is the number of conducting power transistors. The two equations can be put into a uniformed format as

$$R(t) = \frac{V_{EQ}}{I_{\mathrm{in}}(t)} = \frac{V_{EQ}}{I_{\mathrm{in}} + i_{\mathrm{in}}(t)} \tag{8}$$

where $V_{EQ} = V_{DD} - V_{\mathrm{out}}$ when power devices operate in linear region; and $V_{EQ} = V_A$ when power devices operate in saturation region. Note that $I_{\mathrm{in}}(t)$ is written as the sum of two terms in the above equation. The first term is the steady-state current before the transient response; the second term is the current deviation from the steady state during its transient response.

Substituting $R(t)$ expression in (8) to (2), we obtain:

$$\frac{\mathrm{d}(v_{\mathrm{out}}(t))}{\mathrm{d}t} + v_{\mathrm{out}}(t)\left(\frac{I_{\mathrm{in}}}{V_{EQ} \cdot C} + \frac{i_{\mathrm{in}}(t)}{V_{EQ} \cdot C}\right) = \frac{i_{\mathrm{in}}(t) - i_{\mathrm{load}}(t)}{C} \tag{9}$$

Steps of solving this differential equation are provided in Appendix 1. The obtained $V_{\mathrm{out}}(t)$ expression is presented in (10). Clearly, this model considers the fact that the equivalent on-resistance of the power device array exhibits different values along the process of the LDO circuit adjusting the number of conducting devices. Since $R(t)$ is affected differently by load current increase or decrease, $\mathrm{sign}(\Delta i_{\mathrm{load}})$ is used in (10) to distinguish the two scenarios. If load current increases, $\mathrm{sign}(\Delta i_{\mathrm{load}}) = 1$; otherwise $\mathrm{sign}(\Delta i_{\mathrm{load}}) = -1$. Similar to the piecewise analytical equation in [20], the expression in (10) can be used in a piecewise manner to numerically compute LDO transient responses following the steps discussed in [20]. Since the new model more precisely captures the equivalent on-resistance of the power device array during the LDO transient responses, it is more accurate compared to the previous model in [20].

4 Modelling LDO transient responses to reference voltage change

Digital LDOs are often used in dynamic voltage scaling applications, where the output voltage is frequently changed [1, 2, 10] by varying LDO reference input V_{ref}. An important parameter that characterises the LDO transient response in such scenarios is rise time t_{rise}, which is defined as the time interval that the LDO output departures from its original level and reaches the new reference voltage level for the first time. Interestingly, the model developed in the previous section also applies to this situation. This is due to the fact that the LDO system relies on the same mechanism to respond the load current change or reference voltage change. For example, after a load current increase, the LDO output voltage drops below V_{ref} and the LDO feedback loop starts to increase the number of conducting power transistors until the LDO output reaches V_{ref}. Similarly, after a reference voltage increase, the LDO output becomes smaller than V_{ref} and the LDO feedback loop responses similarly. To use the developed model numerically computing the LDO output waveform after reference voltage change ΔV_{ref}, we need set $\Delta i_{\mathrm{load}} = 0$ and replace $\mathrm{sign}(\Delta i_{\mathrm{load}})$ by $\mathrm{sign}(\Delta V_{\mathrm{ref}})$, where $\mathrm{sign}(\Delta V_{\mathrm{ref}}) = 1$ for voltage reference increase and $\mathrm{sign}(\Delta V_{\mathrm{ref}}) = -1$ for voltage reference decrease (see (10)) . When ΔV_{ref} is small, the $v_{\mathrm{out}}(t)$ expression given in (4) can be approximated by the third-order Taylor series expansion. Subsequently, equation $v_{\mathrm{out}}(t_{\mathrm{rise}}) = \Delta V_{\mathrm{ref}}$ can be simplified to:

$$a \cdot t_{\mathrm{rise}}^3 + b \cdot t_{\mathrm{rise}}^2 + d = 0 \tag{11}$$

where

$$a = \frac{X}{6 \cdot (R \cdot C)^3}, \quad b = -\frac{X}{2 \cdot (R \cdot C)^2}$$
$$d = -\Delta V_{\mathrm{ref}} \tag{12}$$

Note that the expression of X is given in (5). The derivation of the above equation as well as steps to solve it is provided in Appendix 2. The obtained expression for t_{rise} is directly listed as follows:

$$t_{\mathrm{rise}} = \frac{-(b + a \cdot t_0) + (\mathrm{sign}(d))\sqrt{b^2 - 2 \cdot a \cdot b \cdot t_0 - 3 \cdot a^2 \cdot t_0^2}}{2 \cdot a} \tag{13}$$

where t_0 is given in (35) in Appendix 2. This expression will be useful in the prediction of LDO output steady-state ripples as discussed in the next section.

5 Modelling LDO output steady-state ripple

Even in the steady state, digital LDO output always exhibits small ripples, which become power supply noise for circuits powered by the LDO output. The steady-state ripples are caused by the finite control resolution of the discrete-time feedback loop. In this study, we use t_ζ to represent the time that the LDO output voltage is at the peak or nadir of the ripples as shown in Fig. 5. In addition, we use N_ζ to represent the number of conducting power devices at time t_ζ; and use N^* to represent the ideal N value such that the total current conducted by the power device array equals the load current. Since

$$\begin{aligned} v_{\mathrm{out}}(t) = {} & V_{EQ}\left(1 - \mathrm{e}^{-(1/V_{EQ} \cdot C)\left(I_{\mathrm{in}} \cdot t + \mathrm{sign}(\cdot\, i_{\mathrm{load}}) \cdot I_{\mathrm{PMOS}} \cdot f_{\mathrm{clk}} \cdot (t^2/2)\right)}\right) \\ & + \sqrt{\frac{\pi \cdot V_{EQ}}{2 \cdot \mathrm{sign}(\cdot\, i_{\mathrm{load}}) \cdot I_{\mathrm{PMOS}} \cdot f_{\mathrm{clk}} \cdot C}} \\ & \times \mathrm{e}^{-\left((I_{\mathrm{in}}^2/2 \cdot V_{EQ} \cdot C \cdot \mathrm{sign}(\times i_{\mathrm{load}}) \cdot I_{\mathrm{PMOS}} \cdot f_{\mathrm{clk}}) + (1/V_{R0} \cdot C)\left(I_{\mathrm{in}} \cdot t + \mathrm{sign}(\cdot\, i_{\mathrm{load}}) \cdot I_{\mathrm{PMOS}} \cdot f_{\mathrm{clk}} \cdot (t^2/2)\right)\right)} \cdot (\Delta i_{\mathrm{load}} + I_{\mathrm{in}}) \\ & \times \left[\mathrm{erfi}\left(\frac{I_{RO}}{2 \cdot V_{EQ} \cdot C} \cdot \sqrt{\frac{2 \cdot V_{EQ} \cdot C}{\mathrm{sign}(\Delta i_{\mathrm{load}}) \cdot I_{\mathrm{PMOS}} \cdot f_{\mathrm{clk}}}}\right)\right. \\ & \left. - \mathrm{erfi}\left(\frac{I_{\mathrm{in}} + \mathrm{sign}(\Delta i_{\mathrm{load}}) \cdot I_{\mathrm{PMOS}} \cdot f_{\mathrm{clk}} \cdot t}{2 \cdot V_{EQ} \cdot C} \cdot \sqrt{\frac{2 \cdot V_{EQ} \cdot C}{\mathrm{sign}(\Delta i_{\mathrm{load}}) \cdot I_{\mathrm{PMOS}} \cdot f_{\mathrm{clk}}}}\right)\right] \end{aligned} \tag{10}$$

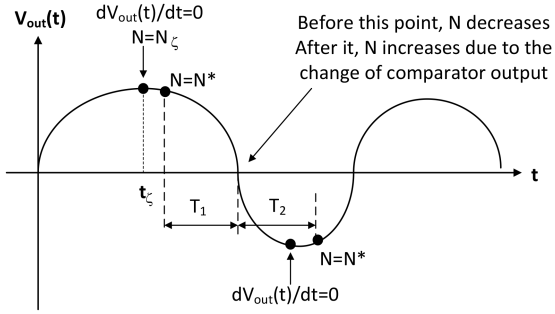

Fig. 5 *LDO output steady-state ripples*

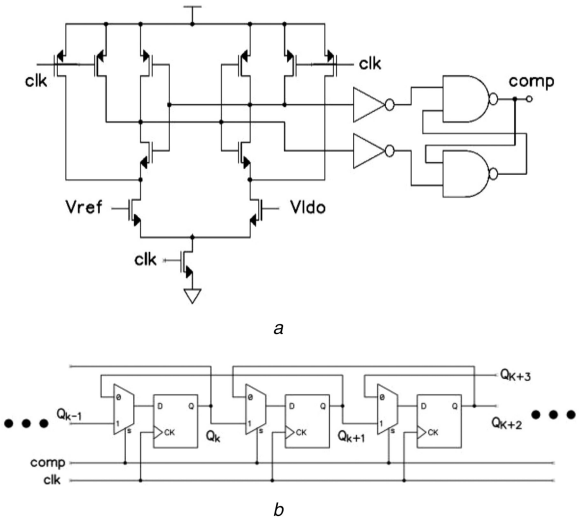

Fig. 6 *Circuits used in LDO implementations*
(a) Comparator used in LDO circuits, ***(b)*** Bi-directional shift register for LDO control

$(\mathrm{d}v_{\mathrm{out}}(t)/\mathrm{d}t)|_{t=t_\zeta} = 0$, there is no current charging or discharging capacitor C at time t_ζ, referring to Fig. 3. From (2), we have:

$$v_{\mathrm{out}}(t_\zeta) = \left(i_{\mathrm{in}}(t_\zeta) - i_{\mathrm{load}}\right) \cdot R = \left(N_\zeta - N^*\right) \cdot I_{\mathrm{PMOS}} \cdot R \tag{14}$$

At the peak of the ripple, the LDO output is above the reference level and $v_{\mathrm{out}}(t_\zeta) > 0$. Thus, (14) indicates $N_\zeta > N^*$. Similarly, at the nadir of the ripple, $N_\zeta < N^*$. Meanwhile, the N value always decreases during the time that the LDO output is above the reference level. This is because the LDO feedback loop is working on bringing the LDO output down to the reference level by reducing the number of conducting power devices. For a similar reason, the N value always increases when the LDO output is below the reference level. These observations lead to the conclusion that the peak or nadir always occur before $N = N^*$ as shown in Fig. 5. In the figure, we also use T_1 and T_2 to denote the intervals between the times that the LDO control has the ideal N^* value and the time that the LDO output crosses the reference level, where the changing trend of N is reversed. Since the LDO control decreases or increases N at the same rate, we have $T_1 = T_2$. This implies that at the steady-state N_ζ should be as close to N^* as possible. However, due to the finite control resolution, N_ζ may not reach the exact N^* value (which may not be an integer) and hence the maximum of $N_\zeta - N^*$ is 1. Substituting this value to (14), we obtain the upper bound of the steady-state ripple magnitude:

$$V_{\mathrm{RIPPLE_{MAX}}} = I_{\mathrm{PMOS}} \cdot R \tag{15}$$

The LDO output behaviour starting from time $t = t_\zeta$ is similar to the system response to a reference voltage change of $V_{\mathrm{RIPPLE_{MAX}}}$. The duration from $t = t_\zeta$ to the time that the LDO output reaches the reference level is t_{rise}. As illustrated in Fig. 5, t_{rise} is approximately one-quarter of the ripple period. Thus, we have:

$$f_{\mathrm{RIPPLE_{MIN}}} = \frac{1}{4 \cdot t_{\mathrm{rise}}(V_{\mathrm{RIPPLE_{MAX}}})} \tag{16}$$

where $t_{\mathrm{rise}}(V_{\mathrm{RIPPLE_{MAX}}})$ can be estimated using (13). Since the upper bound of the ripple magnitude is used in the above estimation, the obtained result should be the lower bound of the ripple frequency, noting that the larger the ripple magnitude is, the larger t_{rise} is.

6 Simulation results

To verify the accuracy of the derived models, three digital LDO circuits were designed using a 0.13 μm CMOS technology. The designs use the topology in Fig. 1. The schematics of the comparator and control logic are depicted in Fig. 6. The control logic is similar to that in [3] and it consists of a 256-bit bidirectional shift register. Each bit of the shift register controls a power device. The left input of the shift register is tied to 0 and its right side input is connected to logic 1. If the comparator output is 1, indicating $V_{\mathrm{LDO}} < V_{\mathrm{ref}}$, the register shifts in 0's from it left input to turn on additional power devices; otherwise, the register shifts in 1's from its right input for turning off excessive power devices. For the convenience of discussion, the three designs are referred to as Designs I, II and III and their key design parameters are listed in Table 1. The designed LDO circuits were simulated using Cadence spectre tool with net lists generated from schematics. Since the LDO circuits operate with low clock frequencies and their output node capacitance is dominated by the large load capacitance, the schematic simulation should be reasonably accurate.

Fig. 7 shows the transient response of Design I when its load current is changed from 50 to 250 μA at 100 μs. The LDO reference input is 0.3 V in this case. The LDO output waveform obtained from circuit simulation is depicted by the solid line in the figure. The waveforms computed by the previous and proposed analytical models are shown by thin dash line and thick dash-dot line, respectively. Clearly, it shows that the analytical model developed in this work more accurately estimates the LDO transient response compared to the model in [20]. Additional circuit simulations with different load changes were also conducted for all the three LDO circuits with various V_{ref} values. The maximum ripple voltages $V_{\mathrm{r,max}}$ obtained from circuit simulation and estimated by the model developed in this work are compared in Table 2. It shows that the estimations from the proposed model are fairly close to the results from circuit simulations.

Circuit simulations were also conducted to investigate the accuracy of using the developed model to predict LDO transient responses after reference voltage changes. Table 3 compares the model estimations with results obtained from circuit simulation for rise time and the maximum overshoot voltage after LDO reference voltage changes. Note that the reference voltage of LDO Design II is switched from 0.45 to 0.35 V and hence its overshoot voltages have negative values, indicating that the LDO output will first go <0.35 V and then gradually settle at the reference level in its transient response. The comparison in Table 3 shows that the values estimated by the developed model and the results obtained from circuit simulations are reasonably close, which validates the claim that the developed model is also applicable to estimating digital LDO transient responses to voltage reference changes.

Circuit simulations were also conducted to examine the accuracy of the estimation equations for the steady-state output ripple magnitude and frequency. The LDO circuit used in this study

Table 1 Key design parameters of LDO circuits used in circuit simulation

LDO circuits	I	II	III
V_{DD}, V	0.5	0.5	0.5
power device (W/L)	0.4/0.12	0.8/0.12	1.2/0.12
f_{clk}, MHz	2	2	2.5
C_{load}, nF	100	50	100

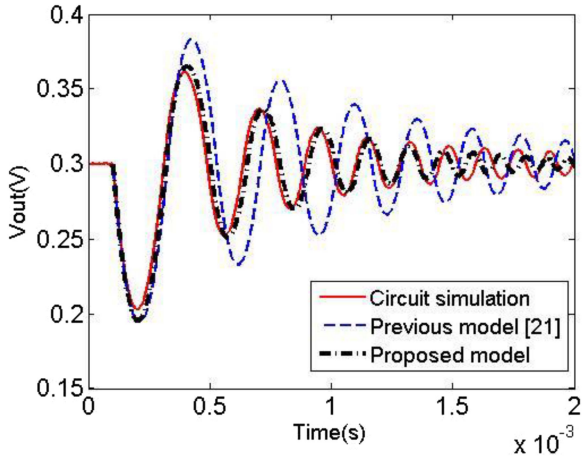

Fig. 7 *Simulated and estimated transient response to load current change*

has power transistor size as 0.4 µm/0.12 µm. Different clock frequencies, load currents and output capacitance are selected in simulations to have four test cases as summarised in Table 4. As discussed in Section 5, the results from (15) and (16) are the upper bound of the ripple magnitude and lower bound of the ripple frequency, respectively. The comparisons in Table 4 confirm the above statements. To examine how load current affects steady-state behaviour, Test Cases I and II were selected such that they only differ by load current values. The comparison between the two shows that the ripple magnitude decreases with the increase of load current. Increased load current results in more conducting power devices and hence reduced R value. Therefore, the ripple magnitude is reduced as indicated in (15). The comparison also shows that the steady-state ripple frequency is increased with the increase of load current, which is mainly due to the decrease of

Table 2 Comparison of simulated and predicted maximum ripple voltage after load changes

LDO circuits	I	II	III
V_{ref}, V	0.45	0.4	0.3
I_{load} change, µA	75→150	100→300	100→600
simulated $V_{\text{r,max}}$, mV	12.4	4.7	70.1
predicted $V_{\text{r,max}}$, mV	10.6	4.9	74.5

Table 3 Comparison of simulated and predicted rise time and maximum overshoot voltage after V_{ref} change

LDO circuits	I	II	III
I_{load}, µA	200	300	500
V_{ref} change, V	0.3→0.35	0.45→0.35	0.35→0.4
simulated t_{rise}, μs	61.3	61.1	27.1
predicted t_{rise}, μs	57.4	53.5	29.2
simulated V_{os}, mV	38.2	−57.5	23.8
predicted V_{os}, mV	38.6	−57.4	29.8

Table 4 Comparison of simulated and predicted steady-state output ripple voltage and ripple frequency

Test cases	I	II	III	IV
V_{ref}, mV	450	450	480	400
f_{clk}, MHz	2	2	1	1
C, nF	100	100	50	50
I_{load}, μA	50	200	100	100
V_{RIPPLE}, mV from simulation	1.25	0.32	0.18	4.1
predicted upper bound for V_{RIPPLE}, mV	1.3	0.33	0.2	7.3
f_{RIPPLE}, kHz from simulation	22.13	48.47	45.55	14.2
predicted lower bound for f_{RIPPLE}, kHz	20.95	40.95	37.1	10.9

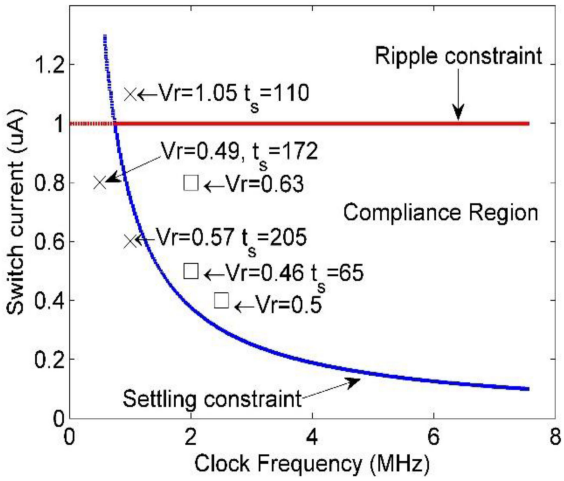

Fig. 8 *Design space partition to simultaneously satisfy steady-state ripple and settling time constraints*

ripple voltage and hence reduced t_{rise} value. Test Cases III and IV only differ by their output voltage for examining the effect of the reference voltage on the steady-state behaviour. It shows that reducing the reference voltage increases the ripple magnitude and decreases the ripple frequency, which is mainly due to the increase of R at the LDO output node.

Finally, the derived models and estimation equations can be used to locate the ranges of key LDO design parameters for meeting the targeted transient performance. This helps designers effectively explore the design space at early design stage. The following illustrates how to use the developed models to partition the design space with multiple design constraints. It assumes that the LDO power supply, reference voltage, and load capacitance are selected as: $V_{\text{DD}} = 0.5\,\text{V}$, $V_{\text{ref}} = 0.45\,\text{V}$, $C = 200\,\text{nF}$. Also, the minimum LDO load current is expected to be 50 μA in the targeted applications. The targeted performance specifications include: (i) the steady-state ripple magnitude should be smaller than 1 mV; (ii) after 50 µA load current change the LDO output settling time should be smaller than 150 µs with settling error $V_\epsilon < 5\,\text{mV}$. As discussed earlier, the steady-state ripple magnitude strongly depends on I_{PMOS}, the current conducted by a single power switch; the settling behaviour after load change is affected by both I_{PMOS} and clock frequency f_{clk}. Thus, the design space in this example is a two-dimensional space with f_{clk} and I_{PMOS} as its horizontal and vertical axes as shown in Fig. 8.

When the LDO experiences the minimum load current, it has the largest output resistance R and hence the largest steady-state ripple magnitude. From the above selected design parameters, we know the LDO output resistance is 1 kΩ when it has the minimum load current. Thus, to satisfy the steady-state ripple magnitude requirement, the current of a single power switch should be smaller than 1 µA according to (15). This defines the ripple constraint boundary of the design space shown in Fig. 8. To satisfy the settling time requirement, the method discussed in our early work [20] was used to generate a curve that further partition the design space as shown in Fig. 8. To verify the obtained design space partition, six design configurations were simulated with using Cadence spectre tool. The three configurations located outside of the compliance region are indicated by symbol '×' and the other three within the compliance region are represented by '□'. The settling time and steady-state ripple magnitude measured from actual circuit simulations are listed beside the symbols. The units of the settling time and steady-state ripple magnitude are microsecond and millivolt, respectively. Due to limited space in the plot, the units are not displayed in the figure. Also, for two design configurations located in the compliance region, their maximum ripple voltages after load change are smaller than the error voltage used to determine settling time. Hence, they automatically satisfy the settling time requirement and their settling times are not displayed. These design cases and their circuit simulation results confirm the validity of the design space partition.

7 Conclusion

This work develops analytical models and closed-form equations for estimating digital LDO transient performance as well as steady-state ripples. The accuracy of the developed models and equations is validated by comparing estimation results with data obtained from circuit simulations. The use of the estimation equations for design space exploration is also demonstrated in the paper. The developed models and equations can be integrated into design automation tools or directly used by designers to predict LDO transient performance at early design stage.

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10 Appendix

10.1 Appendix 1

This appendix provides the key steps of solving (9). Assume that there is a function $\mu(t)$ satisfying (17) listed below. Multiplying both sides of (9) by $\mu(t)$ results in a perfect derivative expression on the left hand side of the resultant equation. Thus with the help of $\mu(t)$, (9) can be solved by integration

$$\frac{\mathrm{d}(\mu(t))}{\mathrm{d}t} = \left(\frac{I_{RO}}{V_{EQ}\cdot C} + \frac{i_{\mathrm{in}}(t)}{V_{EQ}\cdot C}\right)\cdot \mu(t) \tag{17}$$

Using $(1/\mu(t))(\mathrm{d}(\mu(t))/\mathrm{d}t) = (\mathrm{d}/\mathrm{d}t)\log|\mu(t)|$ and substituting (3) into (17) yields:

$$\int \frac{\mathrm{d}}{\mathrm{d}t}\log|\mu(t)|\mathrm{d}t = \int \frac{I_{RO}}{V_{EQ}\cdot C} + \frac{\mathrm{sign}(\Delta i_{\mathrm{load}})\cdot I_{\mathrm{PMOS}}\cdot f_{\mathrm{clk}}\cdot t}{V_{EQ}\cdot C}\mathrm{d}t \tag{18}$$

In the above expression, $\mathrm{sign}(\Delta i_{\mathrm{load}})$ is used to indicate if load current increases or decreases as discussed earlier.

Performing integration on both sides of (18) gives:

$$|\mu(t)| = \mathrm{e}^{(1/V_{EQ}\cdot C)\left(I_{RO}\cdot t + \mathrm{sign}(\Delta i_{\mathrm{load}})\cdot I_{\mathrm{PMOS}}\cdot f_{\mathrm{clk}}\cdot (t^2/2)\right) + \mathrm{Constant}} \tag{19}$$

It can be further simplified to:

$$\mu(t) = \mathrm{e}^{(1/V_{EQ}\cdot C)\left(I_{RO}\cdot t + \mathrm{sign}(\Delta i_{\mathrm{load}})\cdot I_{\mathrm{PMOS}}\cdot f_{\mathrm{clk}}\cdot (t^2/2)\right)} \tag{20}$$

Multiplying (9) by the obtained $\mu(t)$ expression leads to (21). Introducing substitution terms given in (22) and integrating both sides of (21) yields the definite integral expressed in (23). Finally, evaluating the integral in the given interval and dividing it by $\mathrm{e}^{CA\cdot t + CB\cdot t^2}$ yields $v_{\mathrm{out}}(t)$ expression given in (24). Back substituting the terms in (22) leads to (10)

$$\begin{aligned}&\frac{\mathrm{d}\left(\mathrm{e}^{(1/V_{EQ}\cdot C)\left(I_{RO}\cdot t + \mathrm{sign}(\Delta i_{\mathrm{load}})\cdot I_{\mathrm{PMOS}}\cdot f_{\mathrm{clk}}\cdot (t^2/2)\right)}\cdot v_{\mathrm{out}}(t)\right)}{\mathrm{d}t}\\ &= \mathrm{e}^{(1/V_{EQ}\cdot C)\left(I_{RO}\cdot t + \mathrm{sign}(\Delta i_{\mathrm{load}})\cdot I_{\mathrm{PMOS}}\cdot f_{\mathrm{clk}}\cdot (t^2/2)\right)}\cdot \frac{i_{\mathrm{in}}(t) - i_{\mathrm{load}}(t)}{C}\end{aligned} \tag{21}$$

$$\begin{aligned}&CA = \frac{I_{RO}}{V_{EQ}\cdot C} \quad CB = \frac{\mathrm{sign}(\Delta i_{\mathrm{load}})\cdot I_{\mathrm{PMOS}}\cdot f_{\mathrm{clk}}}{2\cdot V_{EQ}\cdot C}\\ &CC = \frac{\mathrm{sign}(\Delta i_{\mathrm{load}})\cdot I_{\mathrm{PMOS}}\cdot f_{\mathrm{clk}}}{C} \quad CD = \frac{\Delta i_{\mathrm{load}}}{C}\end{aligned} \tag{22}$$

$$+CB\cdot t^2}\cdot v_{\text{out}}(t)=\int_0^t \mathrm{e}^{CA\cdot t+CB\cdot t^2}\cdot(CC\cdot t-CD)\mathrm{d}t$$

$$=\frac{\mathrm{e}^{-(CA^2/4\cdot CB)}}{4\cdot CB^{(3/2)}}\Big(2\cdot\sqrt{CB}\cdot CC\cdot\mathrm{e}^{((CA+2\cdot CB\cdot t)^2/4\cdot CB)} \quad (23)$$

$$-\sqrt{\pi}\cdot(CA\cdot CC+2\cdot CB\cdot CD)\cdot\mathrm{erfi}\Big(\frac{CA+2\cdot$$

$$)=\frac{CC}{2\cdot CB}\Big(1-\mathrm{e}^{-\left(CA\cdot t+CB\cdot t^2\right)}\Big)$$

$$+\frac{\mathrm{e}^{-((CA+2\cdot CB\cdot t)^2/4\cdot CB)}}{4\cdot CB^{(3/2)}}\sqrt{\pi}\cdot(CA\cdot CC+2\cdot CB\cdot CD)\Big(\mathrm{erf}i\Big(\frac{(24)}{2}$$

$$-\mathrm{erfi}\Big(\frac{CA+2\cdot CB\cdot t}{2\cdot\sqrt{CB}}\Big)\Big)$$

10.2 Appendix 2

This appendix derives the third-order Taylor series expansion to approximate the LDO output trajectory. Express the third-order series expanded at $t=0$ with unknown coefficients as

$$v_{\text{out}}(t)=a\cdot t^3+b\cdot t^2+c\cdot t \quad (25)$$

By definition of the expansion it follows that:

$$a=\frac{\mathrm{d}^3(v_{\text{out}}(t))}{6\cdot\mathrm{d}t^3}\bigg|_{t=0}=\frac{X}{6\cdot(R\cdot C)^3}\Big(\mathrm{e}^{-(t/R\cdot C)}\Big)\bigg|_{t=0}=\frac{X}{6\cdot(R\cdot C)^3} \quad (26)$$

$$b=\frac{\mathrm{d}^2(v_{\text{out}}(t))}{2\cdot\mathrm{d}t^2}\bigg|_{t=0}=-\frac{X}{2\cdot(R\cdot C)^2}\Big(\mathrm{e}^{-(t/R\cdot C)}\Big)\bigg|_{t=0}=-\frac{X}{2\cdot(R\cdot C)^2} \quad (27)$$

$$c=\frac{\mathrm{d}(v_{\text{out}}(t))}{\mathrm{d}t}\bigg|_{t=0}=Y+\frac{X}{R\cdot C}\Big(\mathrm{e}^{-(t/R\cdot C)}\Big)\bigg|_{t=0}=Y+\frac{X}{R\cdot C} \quad (28)$$

The LDO response to a reference voltage change is computed via (4) by setting Δi_{load} to zero. The rise time t_{rise} of the LDO output after a step change ΔV_{ref} of the reference voltage can be approximated via $v_{\text{out}}(t_{\text{rise}})=\Delta V_{\text{ref}}$. From (25), the rise time is one of the three roots of:

$$a\cdot t^3+b\cdot t^2+c\cdot t-\Delta V_{\text{ref}}=0 \quad (29)$$

Introducing notation $d=-\Delta V_{\text{ref}}$ and noticing that $c=0$ when $\Delta i_{\text{load}}=0$, the above equation is written as

$$a\cdot t^3+b\cdot t^2+d=0 \quad (30)$$

If the magnitude of d is not too large, (30) has three real roots. Thus an arbitrary solution of (30) may or may not be the rise time to $\pm\Delta V_{\text{ref}}$. For the special case where the linear term of a third degree polynomial equation is zero, the simplified cubic formula is given as

$$t_0=\sqrt[3]{\left(-\frac{b^3}{27\cdot a^3}-\frac{d}{2\cdot a}\right)+\sqrt{\frac{b^3\cdot d}{27\cdot a^4}+\frac{d^2}{4\cdot a^2}}}$$
$$+\sqrt[3]{\left(-\frac{b^3}{27\cdot a^3}-\frac{d}{2\cdot a}\right)-\sqrt{\frac{b^3\cdot d}{27\cdot a^4}+\frac{d^2}{4\cdot a^2}}}-\frac{b}{3\cdot a} \quad (31)$$

Also, within the domain of interest, the term under the square root is always negative. Thus with the substitutions:

$$A=\left(-\frac{b^3}{27\cdot a^3}-\frac{d}{2\cdot a}\right),\quad B=\sqrt{\left|\frac{b^3\cdot d}{27\cdot a^4}+\frac{d^2}{4\cdot a^2}\right|} \quad (32)$$

Equation (31) can be simplified to:

$$t_0=\sqrt[3]{A\pm B\cdot i}+\sqrt[3]{A\mp B\cdot i}-\frac{b}{3\cdot a} \quad (33)$$

The complex result is then easily evaluated in polar form:

$$t_0=\sqrt[6]{A^2+B^2}\cdot\left(\mathrm{e}^{\pm(i\cdot\arctan((B/A))/3)}+\mathrm{e}^{\mp(i\cdot\arctan((B/A))/3)}\right)-\frac{b}{3\cdot a} \quad (34)$$

As expected imaginary components cancel out in the equation. For the real component, $\arctan(x)$ naturally only reveals one of two possible solutions, located in the first and fourth quadrants of the complex plane. The desired solution depends on the sign of A. If $A>0$, $\mathrm{sign}(A)=1$ and the solution lies within quadrant one. However, if $A<0$, $\mathrm{sign}(A)=-1$ and π is added to the argument of the cosine function in (35), describing the solution in the third quadrant of the complex plane. (Due to the factor 1/3 resulting from the cubic root, the argument is still kept within the first quadrant.)

$$t_0=-\frac{b}{3\cdot a}+2\cdot\sqrt[6]{A^2+B^2}$$
$$\times\cdot\cos\left(\frac{\arctan((B/A))+\pi((1-\mathrm{sign}(A)/2))}{3}\right) \quad (35)$$

As mentioned earlier, in the domain of interest there exist three real roots, two of which are positive. t_0 in (35) yields the positive root not corresponding to the rise time of the LDO output. Since t_0 is a root of (30), $(t-t_0)$ must be a factor of (30). Performing polynomial division gives the second-order polynomial:

$$a\cdot t_{\text{RISE}}^2+(b+a\cdot t_0)\cdot t_{\text{RISE}}+(b+a\cdot t_0)\cdot t_0=0 \quad (36)$$

Finally, the positive root of (36) corresponds to the rise time of the LDO output to $\pm\Delta V_{\text{ref}}$. Its solution is given explicitly in (13).