Enabling Technologies for 3D ICs: TSV Modeling and Analysis

By

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Enabling Technologies for 3D ICs: TSV Modeling and Analysis

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Abstract

Through silicon via (TSV) based three-dimensional (3D) integrated circuit (IC) aims to stack and interconnect dies or wafers vertically. This emerging technology offers a promising near-term solution for further miniaturization and the performance improvement of electronic systems and follows a *more than Moore* strategy.

Along with the need for low-cost and high-yield process technology, the successful application of TSV technology requires further optimization of the TSV electrical modeling and design. In the millimeter wave (mmW) frequency range, the root mean square (rms) height of the TSV sidewall roughness is comparable to the skin depth and hence becomes a critical factor for TSV modeling and analysis. The impact of TSV sidewall roughness on electrical performance, such as the loss and impedance alteration in the mmW frequency range, is examined and analyzed following the second order small perturbation method. Then, an accurate and efficient electrical model for TSVs has been proposed considering the TSV sidewall roughness effect, the skin effect, and the metal oxide semiconductor (MOS) effect.

However, the emerging application of 3D integration involves an advanced bio-inspired computing system which is currently experiencing an explosion of interest. In neuromorphic computing, the high density membrane capacitor plays a key role in the synaptic signaling process, especially in a spike firing analog implementation of neurons. We proposed a novel 3D neuromorphic design architecture in which the redundant and dummy TSVs are reconfigured as membrane capacitors. This modification has been achieved by taking advantage of the metal insulator semiconductor (MIS) structure along the sidewall, strategically engineering the fixed oxide charges in depletion region surrounding the TSVs, and the addition of oxide layer around

the bump without changing any process technology. Without increasing the circuit area, these reconfiguration of TSVs can result in substantial power consumption reduction and a significant boost to chip performance and efficiency. Also, depending on the availability of the TSVs, we proposed a novel CAD framework for TSV assignments based on the force-directed optimization and linear perturbation.

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Chapter 1

Introduction

1.1 Motivation

The relentless demand for higher semiconductor I/O accounts and data rates, while maintaining power consumption and form factors diminished or unchanged, has motivated an enormous amount of research efforts toward developing novel packaging technologies. Compared with different emerging technologies, such as graphene, carbon nanotube, on-chip optical interconnects, and traditional two-dimensional (2D) integrated circuit (ICs), the three dimensional integrated circuit (3D IC) has the potential capability to bring unique opportunities for highly efficient and sophisticated system. The 3D package on chip has successively manifested as the next prominent trend for increasing the device count within existing semiconductor process technologies [1 – 6]. The current semiconductor process technology is fully compatible with this promising 3D integrated circuit technology and its fabrication with greater functionality can be achieved by introducing a few additional manufacturing processes with the conventional 2D technology. Therefore, over the last several years, the semiconductor industry is paying more attention and showing tremendous interest in the design and implementation of three dimensional integrated circuits (3D IC).

However, due to the growing demand for the miniaturization of electronic devices, the transistors in the integrated circuits (ICs) continue to scale to smaller dimensions and now the limits of the scaling tends to be reached. The interconnect which are very significant components in the integrated circuit do not scale as well as transistors and these long interconnects are the dominant

factors for causing circuit delay and higher power consumption [7]. Hence, the 3D integration system which enables the stacking of multiple layers of active devices are only solutions that can overcome these limitations by significantly reducing the length of the interconnects. The TSV enabled 3D IC have the potential to allow the formation of high signal bandwidth, high interconnect density, and smaller form-factor that dramatically boost the chip performance, and functionality. This emerging technology not only provides the microchip architecture but also facilitates the integration of heterogeneous materials and devices to form different electromechanical subsystems. With this trend, TSV is regarded as one of the most promising 3D chip stacking technologies and plays a key role in determining the performance of the corresponding 3D IC. Along with the need for low-cost and high-yield process technology, the successful implementation of 3D IC requires further optimization of TSV's electrical design, which needs careful consideration of the complex TSV electrical modeling and analysis.

1.2 3D Integration Technology

This section discussed about the overview of 3D integrated circuit technology, the basic building block of 3D integrated circuit technology – TSV, and the benefits of employing TSV in 3D integrated systems.

1.2.1 3D IC Overview

Three-dimensional integration technology for electronic circuit enables the stacking of several silicon wafers/dies and interconnect them vertically so that the whole stacked bonding acts as a single "multi-storey" device. It can be considered as the analogous of the skyscrapers where a huge number of people can effectively communicate with each other in a reduced path compared to a group of neighboring single houses. Likewise, 3D IC exploits the z-direction to enable a very

compact and efficient coupling of different functional units in a single device for the benefits of enhanced electrical performance. A cross sectional view of a mmW transceiver module in 3D silicon interposer technology is shown in Figure 1.1(a) which composed of antennas, ICs, TSV, interposer, flip chip bumps, package substrate etc. Depending on the stacking method, the integration technology in 3D IC can be categorized into three types such as, die-level integration, wafer-level integration, and device-level integration [8]. At this type, after processing the wafer, it has been cut into several dies and these are tested individually. Then the Known-Good-Dies (KGDs) are aligned and stacked to each other to form the 3D IC. The wire bonding is basically being used to stack the dies though the microbumps are also used sometimes. As the yield issue is related to KGDs, therefore the overall chip yield is improved in this assembly method. It has been widely used during long time but suffers from a low interconnect density. Due to the testing and pre-selection of KGDs, this method is not suitable for a cost effective solution.

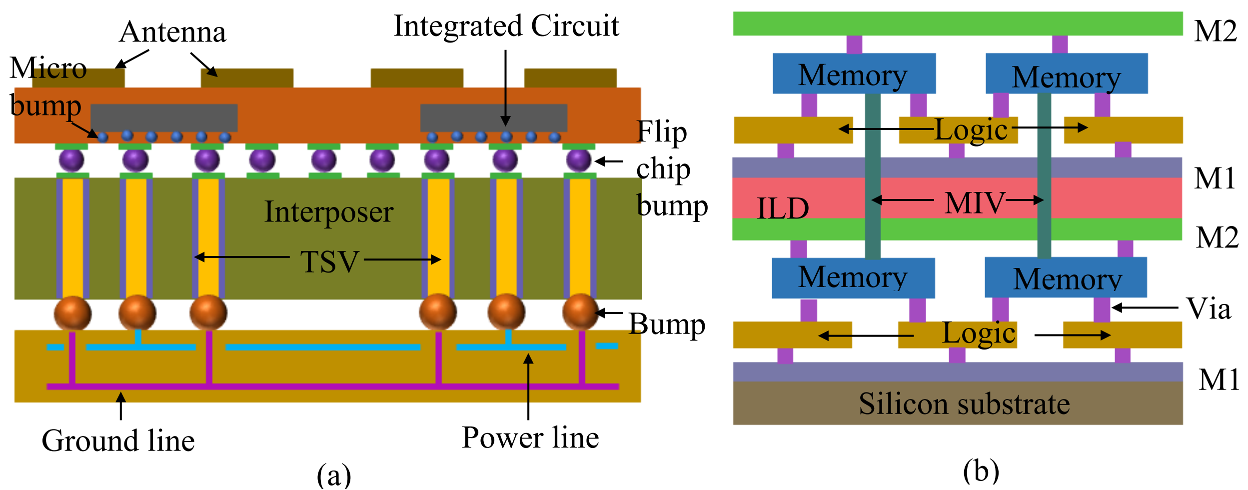


Figure 1.1: 3D Integrated Circuit (a) TSV based 3D IC (b) Monolithic 3D IC

The TSV enabled 3D integration is known as wafer-level integration. In this bonding type, wafers are bonded together first and then cut into several dies which requires higher process complexity

[9]. The die selection and testing cannot be performed prior to the bonding and therefore bad dies might be bonded with the good dies which ultimately decreases the overall yield. It offers the highest throughput where the corresponding inputs and outputs of the 3D IC are situated on top of the active layer. It can overcome the shortcomings of the die-level integration by providing higher interconnect density with enhanced performance using TSVs as interconnect. The wafer-level integration is shown in Figure 1.1 (a).

The device-level integration is different from the die-level and wafer-level integration. It is also known as monolithic 3D integration and shown in Figure 1.1(b). Here, the multiple transistor layers are stacked vertically with ultra-high density interconnect. These interconnects are termed as monolithic inter tier vias (MIVs) and has the dimensions at nanoscale range which uses much smaller area than the TSV. This integration approach is poised to minimize the spaces between the transistors and maximize the number of transistor per unit area. This is not matured yet and still in the preliminary stage of exploration which requires higher complexity in manufacturing compared to die level and wafer level integration. In monolithic 3D IC, sequential integration of two or more tiers of devices are applied [10], whereas, parallel integration technique is being used in TSV based 3D IC.

1.2.2 Through Silicon Via (TSV)

The basic building block of the 3D package on chip is the through silicon vias (TSVs); the electrical characteristics of TSVs have a crucial effect on the overall performance of any given 3D integrated circuits (ICs). The effect becomes even more significant and pronounced when data rates are pushed into the Terabits region [11] [12]. TSVs are essentially metal insulator semiconductor (MIS) devices in which a dielectric layer SiO_2 is deposited for the electrical isolation between the conducting metal and silicon substrate [13] [14]. In a real 3D package

configuration, such as illustrated in Figure 1.2, TSVs are buried within silicon substrates (Si substrate). Consequentially, their electrical performance depends upon not merely their geometrical parameters, but also the characteristics of the Si substrate and the SiO_2 isolation layer [15].

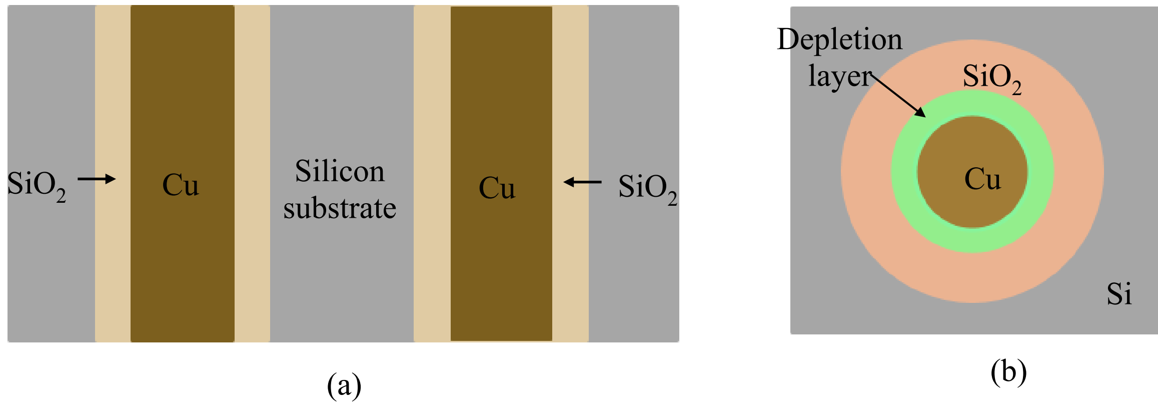


Figure 1.2: Representation of TSV Cross-sectional view (a) Side view (b) Top view

Depending on the manufacturing process of order, there are two different types of TSVs such as front-end-of-the-line (FEOL) and back-end-of-the-line (BEOL) approach. These are also known as via-first and via-last TSVs respectively. In a FEOL process, TSVs are embedded into the substrate before the metallization and the processing of active device layers. As the TSVs are implanted prior to the bonding process, there will be a better areal usage and higher TSV density with the reduction of TSV parasitics. In a BEOL process, the TSVs are formed after the metallization and active layers so that there is a blockage to the metal layers which reduces the via density [16]. However, in all processes of fabrication technology the TSVs are required to be exposed when these are buried into the semiconductor substrate. Compared to each other, the FEOL approach is highly efficient though there is a more process complexity in it.

Once the dies are fabricated, these can be stacked and bonded sequentially by two different approaches — face-to-face (F2F) and face-to-back (F2B). In F2F bonding, the front sides of two

dies are stacked such that the outermost metal layers of two dies in top sides are connected or the metal layer of one die is connected to the TSV of other die as illustrated in Figure 1.3 (a).

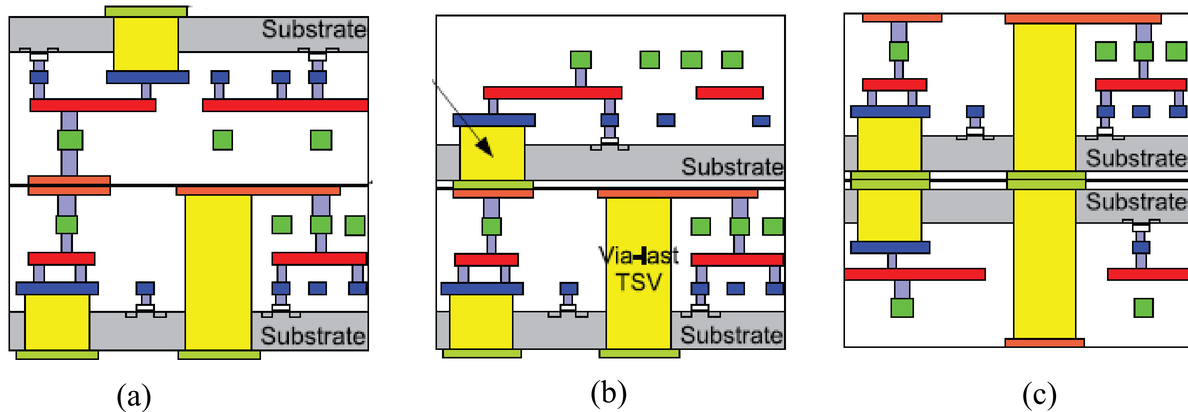


Figure 1.3: Types of die stacking (a) face-to-face (b) face-to-back (c) back-to-back [17]

In F2B bonding, the front side of a die and back side of other die are connected so that both the bottom and top tiers are facing up. The F2F stacking offers to reduce the size and number of TSVs for performance enhancement, but limited to two dies only in a stack. On the other hand, more than two dies can be stacked in F2B bonding but the TSV density is reduced. Rather than these, another type of die stacking also exists which is back-to-back bonding. In this case, the back side of two dies are bonded and the signal goes through two TSVs but this is not a common approach.

1.2.3 Benefits of 3D Integration

There are numerous benefits of 3D integration to using TSVs as vertical interconnects. The main advantages using 3D integrated circuits are high density and heterogeneous integration, smaller form factor, enhanced power consumption and overall cost reduction. These are described as below:

- The continuous demand of miniaturization of electronic technology is increasing day by day where the portability and the form factors of semiconductor devices are becoming the main factors now a days. Therefore, a new design methodology shift from the conventional 2D

circuit design paradigm is necessary to fulfill the overwhelming expectation of miniaturized microelectronic system with enhanced performance. Three dimensional integration enables this opportunity by stacking multiple dies to build a high density integrated system. Therefore, vertically stacking multiple dies with short interconnect provides small footprint and enhance the functionality of the system [10] [18].

- To merge different heterogeneous functions like data processing, sensing, memory, data transmission etc. in an advanced integrated circuit requires different fabrication process with very complex and costly procedure. However, 3D integration has the potential capability to incorporate the devices with multiple fabrication processes into a stacked 3D system through these from different vendors. The modern TSV based 3DIC provides potential alternative to the conventional 3D process and thus reduces the complexity greatly.

- Power consumption is one of the most important issues in modern electronic circuital system. In high speed electronic system, higher power density is realized which is directly related to the thermal issues of on-chip temperatures and pose a risk to circuit integrity. A significant amount of on-chip power is consumed through the long interconnect in ICs which can be reduced by using fast switching signal through a short interconnect. 3D integrated system enables short interconnect to connect the different tiers of the stacked device and thus leads to a lower dynamic power consumption. Also, the I/O power of signal transmission through the vertically stacked multiple chips can be decreased greatly.

- The high density integration in conventional 2D integrated circuit is directly related with the smaller size of the transistors. However, the transistor scaling is becoming very complex and costly due to the sophisticated fabrication and development process. In addition, the die yield is degraded with increased physical die size to incorporate higher functionality in traditional

2D IC. Therefore, the production cost increases significantly. But in 3D integrated system, the dies are much smaller than the 2D counterpart which increases the yield and reduces the cost for very large system design.

1.3 Challenges in 3D IC

Though 3D IC brings enormous opportunity, there are still several challenges exist from different aspect. Therefore, the issues pertaining to this technology needed to be focused and resolved. From the perspective of design and test, several issues are identified like, thermal management, system-level and design exploration of different 3D architecture, yield and reliability challenges, testing and fault tolerant etc. [20]. From the physical design point of view, the associated issues are coupling issues, 3D floorplanning, designing of multi-granularity 3D IC, placement, optimization, routing of TSV, topology variation etc. However, the most challenging issues are linked with the modeling and extraction of electrical parasitic. As the TSVs are buried in lossy semiconductor substrate, therefore, it is intuitive that the complexity in propagating the EM wave will be arisen. In addition to this, there are some other important issues like high frequency effect, roughness effect, MOS effect etc.

This dissertation focused on the surface roughness issue of TSV at millimeter wave frequency. The surface roughness can severely impact the TSVs by producing a significant amount of leakage current in the high frequency range. Therefore, the biggest challenge of modeling TSVs in 3D millimeter wave (mmW) ICs comes from the need of an accurate broadband model which captures the high frequency effect, frequency dependent loss, coupling, and mismatch.

Rather than this, there are some other technical challenges and concerns about the implementation when applying this promising technology in a very complex and sophisticated system like brain–

inspired computing. A significant part of this dissertation deals with this massively parallel processing computing system.

1.4 Contributions

Overall, the contributions of this dissertation are divided into two phases. First phase includes the analytical modeling and analysis of rough surface TSV in 3D IC considering the high frequency and MOS effect. In second phase, the emerging application of 3D integration is explored in neuromorphic computing with novel approach of utilizing TSVs in spiking neuron design. The detail contributions are listed as following:

First phase:

- Most of the recent work pertaining to TSV modeling and design focuses on RF applications at an operational frequency up to 40 – 50 GHz; whereas TSV modeling and design specifically for mmW applications incorporating surface roughness and nonlinear capacitance is far from being fully explored. In this work, we concentrate our research efforts upon accurately modeling the impact of TSV sidewall roughness. Our research incorporates an electrical model to quantify the TSV sidewall roughness. We employ the second order small perturbation method (SPM2) to obtain the analytical equations for calculating the enhancement factor of the roughness. In our approach, the magnetic field in the presence of surface roughness is represented in the spectral domain. We leverage approaches commonly applied in quantum mechanics to quickly identify a perturbation coefficient. Each parameter in the model is analytically calculated. Then the effectiveness of the model is evaluated through a comparison between the equivalent circuit simulation and full wave predicted scattering parameters for the TSVs up to 100 GHz.

Second phase:

- Until now, there have been a few works utilizing TSVs for purposes other than signal, power or heat delivery, but mainly for 3D inductors. We propose a novel 3D neuromorphic computing architecture by exploring TSV configurations to adapt them for use as membrane capacitors and building an optimized CAD framework to enable full utilization of these devices and circuits. Due to the lower capacitance in TSV depletion region, we proposed new methodologies to enhance the TSV capacitance to supply sufficient membrane capacitance for the synaptic signaling process, especially in a spike firing analog implementation of neurons in a proposed 3D system. In addition, a commensal membrane potential for a 3D neuromorphic system is derived to closely resemble the required membrane charge distribution characteristics and accounting for the target TSV capacitance. The electrical performance of the 3D neuromorphic chip is compared against 2D counterpart designs.

- For proper signal transmission and power dissipation as well as to maintain parallelism between the layers in 3D neuromorphic chip, a critical investigation is needed that ensures the minimized crosstalk from the signal/ground TSV. It is quite challenging to find out an optimal differential signal assignment from a massive number of arrays that will reduce the crosstalk. We studied the force directed optimization algorithm that compares the electrical performance of differential signal pairs of TSV array with the distributed ground and find out the optimal one. An electrical model of the optimal differential signal TSV array is proposed and the optimized TSV array is being verified by comparing with EM simulation.

1.5 Thesis Outline

This dissertation is organized as follows:

Chapter 2 presents the important factors for modeling the TSV in 3D IC along with the previous research on TSV modeling and analysis.

Chapter 3 details the application of the small perturbation method to analyze the impact of the surface roughness in the mmW frequency range, and addresses the power enhancement factor of the TSV induced by sidewall roughness. It presents an analytical model for a TSV pair considering the roughness and high frequency effects and compares the performance of the TSVs, with and without considering the sidewall roughness effect. Finally demonstrates the validation of the proposed models for two TSV arrangements.

Chapter 4 highlights the introduction of neuromorphic hardware system, the necessity of applying 3D integration in neuromorphic computing, and the proposed 3D neuromorphic system.

Chapter 5 details the TSV based neuronal membrane capacitance in the proposed 3D neuromorphic system with two new methodologies for the enhancement of TSV capacitance. Next, a derivation of TSV membrane potential model from TSV physical properties is described. The proposed models along with the simulation results are illustrated for effectively utilizing the TSV in 3D neuromorphic systems.

Chapter 6 discussed about the optimized TSV array assignment for the minimization of crosstalk in neuromorphic 3D structure, an electrical model of the optimized TSV array and the validation of the TSV array assignment.

Chapter 7 summarizes and concludes this dissertation with future research opportunity.

Chapter 2

Preliminaries of TSV Modeling and Analysis

2.1 Wave Propagation Modes in TSV

The wave propagation along the microstrip line on a silicon substrate requires the solution of an extremely complicated Eigen value problem and supports the three basic modes of operation. The modes are known as quasi-TEM mode, skin effect mode, and slow-wave mode. All three modes depend on the geometry and material parameters with operational frequency of microstrip line [21]. However, the microstrip line is based on metal-insulated-semiconductor (MIS) structure, it is quite similar to the TSV structure. Therefore, all the three fundamental propagation modes are also applicable for TSV where each mode is clarified on the resistivity of substrate – frequency plane as shown in Figure 2.1.

In a signal-ground pair of TSV, each conductor is coated with the oxide layer and two pairs are separated by the silicon substrate. Depending upon the variation of substrate resistivity and frequency, different substrate behavior can be found which forms the propagation mode on the surface-passivated semiconductor substrate. Both the semiconductor substrate resistivity and the operational frequency are increased and when their product is able to produce a small dielectric loss angle, the semiconductor substrate behaves as a dielectric material [22]. Therefore, two of the dielectric layers (SiO_2 and Si) exist between the TSV pair and in this scenario, the fundamental mode closely resembles the "quasi-TEM" mode. When the product of silicon substrate conductivity and the operational frequency is large enough to have a small depth of penetration

into the semiconductor for EM field, the silicon substrate acts like a lossy conductor wall [21]. In this case, the TSVs are considered as embedded in the imperfect ground plane (silicon substrate) which can be treated as "skin effect" mode.

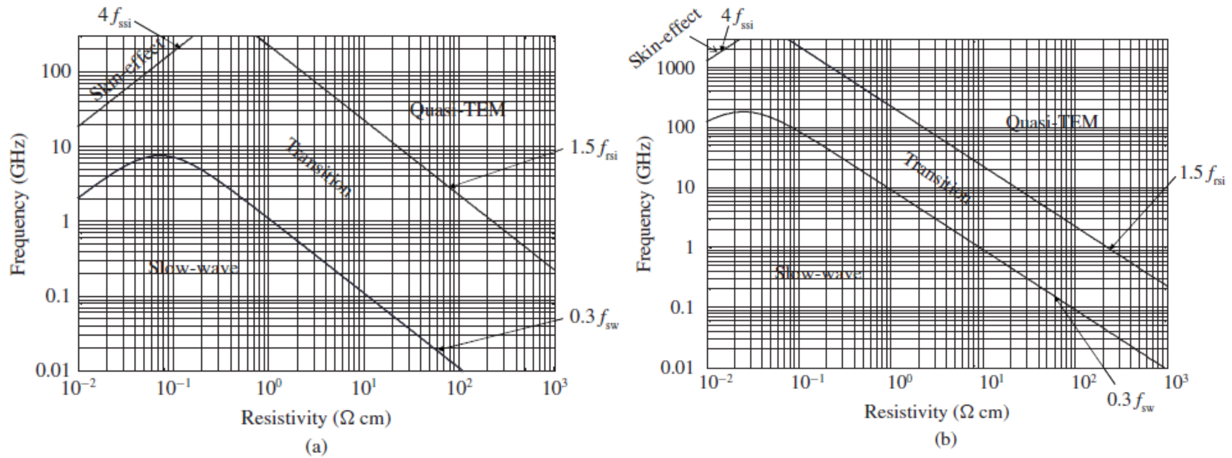


Figure 2.1: Frequency-resistivity chart for (a) Interposer, and (b) Chip-level TSV [23]

Rather than this another propagation mode known as "slow wave mode" appears when the product of frequency and the resistivity of the silicon substrate is moderate. The electromagnetic field partially penetrates the silicon substrate that causes strong interfacial polarization across the SiO_2 liner and therefore the "slow wave mode" occurs. This mode is characterized by slow phase velocity of propagating signals due to the Maxwell-Wagner effect that contributes to make a very small layer of space-charge in the silicon – oxide surface at lower frequencies [24]. The Maxwell-Wagner effect is an interfacial relaxation process between the two material interface that accounts for charge distribution and could explain the characteristics of slow wave and dielectric mode very well [25].

As the TSVs are MIS structure, the study of all the above mentioned propagation modes is very important because of the penetration of electric and magnetic field can ensure the appropriate design guideline in a given frequency range.

2.2 TSV MOS Capacitance

In the MIS structure of TSV, a doped silicon substrate is biased and therefore based on the voltage difference between the metal conductor and substrate, the metal oxide semiconductor (MOS) capacitor appears as shown in Figure 2.2. It is an important phenomena in TSV based 3D IC which could overcome the misestimation that occurs in determining the cylindrical capacitance. According to the physical mechanisms of charge distribution in TSV, the MOS capacitance can be classified into three regions like accumulation, depletion, and inversion.

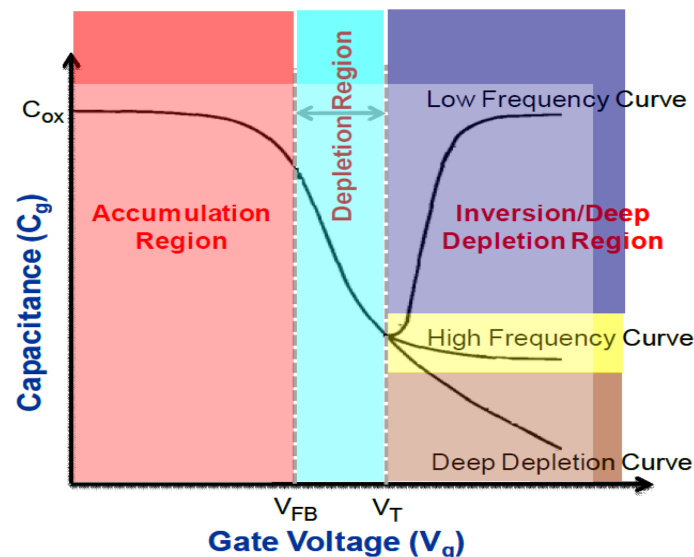


Figure 2.2: TSV MOS capacitor – voltage characteristics for p – type substrate [24]

2.2.1 Accumulation region

When a voltage is applied at the conductor of TSV with p – type Si substrate and the applied voltage is less than the flat – band voltage, the valence band edge bends upward near the surface. The majority carrier exponentially depends on the bend bending and therefore, these carriers are accumulated near the interface of oxide and silicon substrate. In this case, the MOS capacitor will be equal to the oxide capacitance of TSV.

2.2.2 Depletion region

If the applied voltage is increasing and once this voltage exceeds the flat – band voltage, the energy band bends downward. Hence, the majority carriers are depleted and a carrier free region is formed near the interface of oxide and substrate. Now this region behaves like a dielectric material and forms the depletion capacitance. The depletion capacitance strongly depends on the width of the depletion region. This capacitance is connected in series with the oxide capacitance and forms the total MOS capacitance.

2.2.3 Inversion region

Further increasing the applied voltage causes more band bending to downward. When this voltage reaches the threshold voltage, the minority carriers are attracted at the surface and become larger in number compared to the majority carriers. Thus the surface is inverted and this region is gradually shielded by the minority carriers. The capacitance starts increasing again in inversion region.

When TSVs are operated in the low frequency range, the MOS effect in TSVs can be quite satisfactorily modeled as MOS capacitances [26]; whereas, when TSVs are operated in the ultra-broad band frequency range, the electrical behavior is considerably altered and deviated into a domain of scarcely imaginable complexity. High speed switching can dynamically bias the TSV-MIS interface and result in regions of electronic accumulation or depletion; the capacitance becomes a nonlinear function of signal bias. In 3D ICs, the MOS capacitance plays a significant role to decrease the total capacitance due to biased substrate and thus it reduces the leakage current into the silicon material [24].

2.3 Millimeter Wave Frequency in TSV Modeling

In electromagnetic spectrum, the millimeter wave is defined as the range of wavelength starting from 10 mm to 1 mm which is narrower than microwaves and broader than infrared waves. It corresponds to the radio band frequency from 30 GHz – 300 GHz and its unique characteristics make it beneficial for numerous application like computer data transfer, cell phone, satellite, radar etc.

However, most of the TSV modeling approaches focus on the radio frequency (RF) applications with operation frequency of several GHz or even lower, whereas the TSV technology specifically for millimeter wave range (mmW)/THz applications is seldom reported. The mmW communication has emerged as an enabling technology to resolve the spectrum shortage issue due to significant growth of mobile data traffic [27 – 28]. There are some outstanding challenges due to EM effects that are associated with the mmW technology such as impedance mismatching, signal reflections, crosstalk, and radiation [30] [31]. It is therefore a prudent consideration to address the critical issues which influence the properties of the TSVs in ultra-high and extremely-high frequency range [2]. These challenges can be addressed by properly modeling and designing the TSVs considering those effects in emerging and attractive 3D integration approach.

2.4 High Frequency and Surface Roughness Effect

The electrical performance of TSVs depends upon not merely their geometrical parameters, but also the characteristics of the Si substrate and the SiO_2 isolation layer [15]. Therefore, the TSV characteristics are frequency dependent [38]. At low frequency, the MOS capacitance of the TSV dominates the performance; while their characteristics are very much controlled by the propagation

modes they support, the skin effect becomes appreciable at higher frequency [26 – 32]. Hence, the effect of roughness needs to be considered in millimeter wave frequency range due to the skin effect. The skin effect phenomenon causes the alternating current to flow more towards the surface rather than the center where the majority current flows within a thin layer at the conductor surface [32]. In high frequency, the current flowing through conductor is more concentrated towards the surface of the conductor that causes skin effect more significant. As the frequency increases, the skin depth starts decreases which can be seen from the Figure 2.3 below. The resistance of TSV will increase as the operating frequency increases due to the skin effect phenomena. When the operating frequency increases to tens of GHz, the skin depth will be compared to the root-mean-square (*rms)* height of the rough sidewall [33].

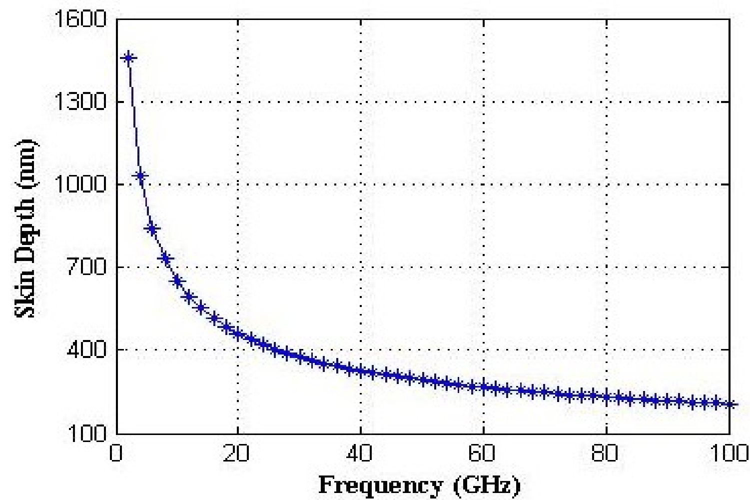


Figure 2.3: Skin depth for the selected frequency ranges

To design interconnects/TSVs for their optimal performance, it is instructive to consider this critical issue. The EM wave propagates through TSV generally introduces ohmic loss due to the attenuation. However, when the surface roughness appears in the TSV sidewall, it causes additional loss which can be modeled as frequency dependent resistance and inductance.

For the analysis of power absorption behavior, the calculation of power absorption enhancement factor is very important which relates the power absorbed by rough surface to its smooth counterpart. To accurately predict such conductor loss in the TSV, the surface roughness must be carefully modeled. We emphasize the significant research conducted to investigate the impacts of surface roughness on power loss and wave propagation of interconnects.

2.5 A Synopsis of Previous Works on TSV Modeling

A considerable amount of research work on TSV modeling and analysis have been performed to address the impact of TSVs on high speed signals, to analyze the TSV crosstalk, to study the TSV resistance, as well as to apply the full-chip extraction and optimization [15] [23] [34 – 39]. Reasonably comprehensive TSV models have been constructed which characterized resistance, inductance, capacitance, and conductance.

Electromagnetic models of differential and complex multi-TSVs are proposed to extract electrical parasitics and obtain analytic equations for lumped model analysis in the frequency domain [34 – 36]. Numerical, analytical, and measurement based methods have been extensively applied to extract the TSV parameters and validate EM simulations. High frequency analytical efforts have generated TSV models that include parametric studies of skin and proximity effects towards a comprehension of propagation characteristics [23], [37]. The impacts of differing TSV geometries and structures upon signal integrity can be quantified and the performance of the TSVs can be optimized by using coaxial configuration.

Coupling and cross talk are another important issues in large TSV arrays; such impacts can be analyzed in both time and frequency domain through eye margin analysis [38], [39]. These ref. [38], [39] presents analysis for electrical modeling and measurement of TSV coupling capacitance

by following the formation of TSV's processing. Rather than this electrical modeling is developed by considering the MOS capacitance effect [26], [36] which has an influential dominance on TSV mutual capacitance.

Also, new basis functions are introduced to capture the effect of TSV oxide liner that could simulate a large number of TSVs with less computation time [15]. The full wave analysis methods are accurate, but will be computationally intensive due to the large number and multi-scale dimensions (oxide thickness and aspect ratio) of TSVs in the 3D mmW integrated circuits. Another bottleneck of the full wave methods is that it is difficult to be compatible with SPICE simulators. The equivalent circuit methods with lumped Resistance (R), inductance (L), conductance (G), and capacitance (C) elements could be a good alternative and can provide good compatibility with SPICE simulators. However, most of these TSV modeling approaches and analysis focus on the RF applications with frequency of several GHz or even lower.

Chapter 3

Rough Surface TSV Modeling

3.1 Introduction

To analyze the electrical performance of 3D ICs, it is crucial to model and design the TSVs accurately and efficiently because of their critical roles in the overall communication architecture of 3D IC. To design TSVs for their optimal performance, it is instructive to consider some critical issues which may greatly influence the TSV electrical properties. One important issue is the surface roughness, which can severely impact the TSVs by producing a significant amount of leakage current in the high frequency range [40]. In mmW frequency range, the sidewall roughness becomes a critical factor for TSV modeling and analysis. In this chapter, the impact of TSV sidewall roughness on electrical performance, such as the loss and impedance alteration in the mmW frequency range, is examined and analyzed. The second order small analytical perturbation method (SPM2) is applied to obtain a simple closed-form expression for the power absorption enhancement factor of the TSV. We also proposed an electrical model of the TSV which considers the TSV sidewall roughness effect, the skin effect, and the MOS effect. [41 – 42].

3.2 Surface Roughness in TSV

Unlike the conventional interconnects, TSVs are essentially metal insulator semiconductor (MIS) devices [13] wherein the dielectric layer (typically SiO_2) is deposited to isolate the conductive metals from the substrate [14]. It is crucially important to consider the effect of rough sidewall in

TSVs modeling;   particularly when the root mean square (rms) height of the rough sidewall is comparable to the skin depth at extremely high frequency.

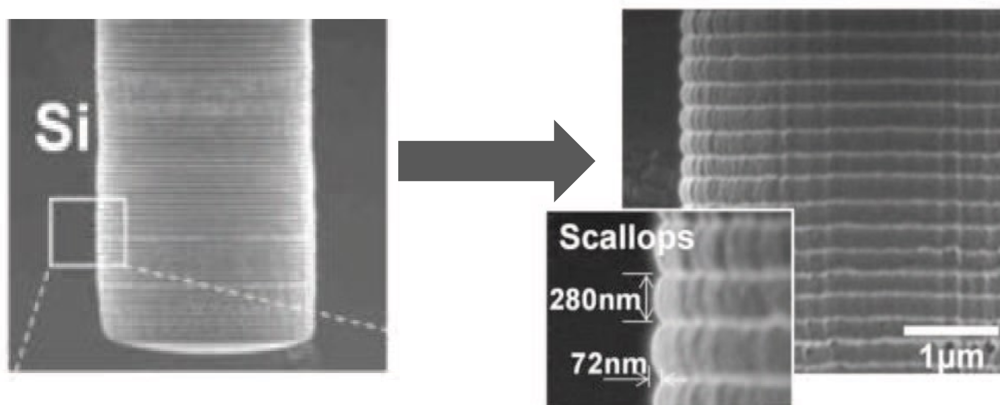


Figure 3.1: Cross-sectional scanning electron microscopy (SEM) image of TSV with sidewall roughness [40]

The sidewall roughness of the TSV is invariably a byproduct of the etching process and poor polymer deposition during passivation. For instance, the sidewall roughness shown in Figure 3.1 was created during a process of “Bosch etching” (with SF_6 and C_4F_8); it has a period and a depth of 280 nm and 72 nm, respectively. Another process technology, such as “direct etching” may obtain a smoother sidewall [40]. In some instances, sidewall roughness is deliberately induced to enhance mechanical adhesion.

The sidewall roughness of TSVs can severely impact the current flowing through the TSVs by producing significant amount of leakage current at high frequency [40]. Therefore, the biggest challenge of modeling TSVs in 3D mmW ICs comes from the need of an accurate broadband model which captures the high frequency effect, frequency dependent loss, coupling, and mismatch.

3.3 Analysis of Surface Roughness using SPM2

The equations which arise from mathematical models conceived to represent the TSVs cannot be solved in exact form. Therefore, we must resort to approximation and numerical methods. Foremost among approximation techniques are perturbation methods. These methods lead to an approximate solution for problems when the model equations have terms that are small. In this work, we assume the side wall roughness is relatively small compared to TSVs size. Second-order small perturbation method (SPM2) [33] [43 – 45] is applied in our case to solve the field propagation when the rough surface is considered. Bracket notations [46] that represent particular vector spaces are used to demonstrate system state.

3.3.1 H Field Spectrum using SPM2

The roughness considered in this work assumes a profile which can be expressed by a Gaussian correlation function in both the *x* and *y* direction as:

$$f_G(x,y) = h^2 e^{-\left(\frac{(x^2+y^2)}{l^2}\right)}. \tag{3.1}$$

where h is the rms height of the roughness and l is the correlation length.

When a plane wave propagates within conducting medium in the *y* direction as illustrated in Figure 3.2, the Helmholtz equation for the magnetic field becomes:

$$\nabla^2 \boldsymbol{H} = j\omega\mu\sigma\boldsymbol{H}. \tag{3.2}$$

where $\boldsymbol{H}$ is the magnetic field vector, μ is the permeability, σ is the conductivity, and ω is the angular frequency.

In the spectral-domain, the magnetic field can be represented as:

$$H(x,y,z) = \int_{-\infty}^{\infty} e^{(j\omega_x x + j\omega_y y + j\omega_z z)}\,\psi(\omega)d\omega \tag{3.3}$$

where ψ is the spectral representation of the field and

$$\omega = \sqrt{\omega_x^2 + \omega_y^2 + \omega_z^2} \tag{3.3-a}$$

The magnetic field $H(x, y, z)$ is subject to the boundary condition of $H = H_0$ on the surface. H_0 is a constant and can be expressed as:

$$H_0 = \int_{-\infty}^{\infty} e^{(j\omega_x x + j\omega_y y + j\omega_z f(x,y))}\, \psi(\omega) d\omega \tag{3.4}$$

The spectral representation of ψ is:

$$\psi_n(\omega) = H_0 \delta(\omega) \tag{3.5}$$

Apparently $\psi_n$is independent of frequency and follows the Schrodinger time–independent wave equation. Applying bracket notation, equation (3.5) can be written as:

$$H_0 \delta(\omega) \left|n^{(0)}\right\rangle = \psi_n(\omega) \left|n^{(0)}\right\rangle \qquad n = 1,2,3\ldots \tag{3.6}$$

A weak disturbance Z can be introduced to the magnetic field due to the surface roughness and μ as a dimensionless parameter that can vary the value from no perturbation to full perturbation.

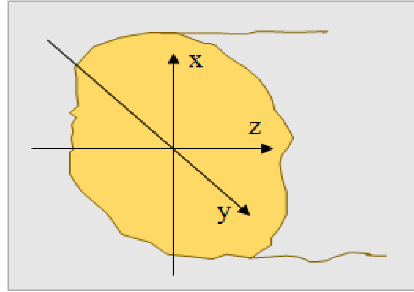


Figure 3.2: Regions showing the boundary condition in rough surface TSV conductor

Then the perturbed magnetic field becomes:

$$H\delta(\omega) = H_0 \delta(\omega) + \mu Z \tag{3.7}$$

The spectrum and Eigen states of the perturbed magnetic field are given by the Schrodinger equation as:

$$(H_0 \delta(\omega) + \mu Z)|n\rangle = \psi_n(\omega)|n\rangle \tag{3.8}$$

The zeroth order equation representing the unperturbed system while the first order equation can be written as:

$$H_0\delta(\omega)\left|n^{(1)}\right\rangle + Z\left|n^{(0)}\right\rangle = \psi_n^{(0)}(\omega)\left|n^{(1)}\right\rangle + \psi_n^{(1)}(\omega)\left|n^{(0)}\right\rangle \quad (3.9)$$

The first order energy shift, which is the expectation value of the perturbed magnetic field while the system is in unperturbed state becomes:

$$\psi_n^{(1)} = \left\langle n^{(0)}\middle|Z\middle|n^{(0)}\right\rangle \quad (3.10)$$

However, the true energy shift is slightly different, because the perturbed eigenstate is not exactly the same as $\left|n^{(0)}\right\rangle$. These further shifts are given by the second and higher order corrections to the energy. Using the resolution of identity from the first order coefficient μ:

$$Z\left|n^{(0)}\right\rangle = \sum_{k\neq n}\left|k^{(0)}\right\rangle\left\langle k^{(0)}\middle|Z\middle|n^{(0)}\right\rangle + \psi_n^{(1)}\left|n^{(0)}\right\rangle \quad (3.11)$$

The first order correction along with $\left|k^{(0)}\right\rangle$, the first-order change in the *n*-th energy eigenket, is obtained that has a contribution from each energy eigenstate $k \neq n$.

$$\left|n^{(1)}\right\rangle = \sum_{k\neq n}\frac{\left\langle k^{(0)}\middle|Z\middle|n^{(0)}\right\rangle}{\psi_n^{(0)}(\omega)-\psi_k^{(0)}(\omega)}\left|k^{(0)}\right\rangle \quad (3.12)$$

The normalization prescription gives:

$$2\left\langle n^{(0)}\middle|n^{(2)}\right\rangle + \left\langle n^{(1)}\middle|n^{(1)}\right\rangle = 0 \quad (3.13)$$

The 2nd order approximation of ψ_n which reflects more exact energy perturbed state is given as:

$$\psi_n(\omega) = \psi_n^{(0)}(\omega) + \mu\left\langle n^{(0)}\middle|Z\middle|n^{(0)}\right\rangle + \mu^2\sum_{k\neq n}\frac{\left\langle k^{(0)}\middle|Z\middle|n^{(0)}\right\rangle}{\psi_n^{(0)}(\omega)-\psi_k^{(0)}(\omega)} \quad (3.14)$$

3.3.2 Power Absorption in the Rough Surface

Since the magnetic field has minimum effect on the dielectric, the magnetic field spectrum in the dielectric can be found as:

$$\psi_m(\omega) = H_0\delta(\omega) - jkH_0F(\omega) \quad (3.15)$$

where $F(\omega)$ is the Fourier transform of the roughness height function.

For the derivations listed above, the spectral representation of the total magnetic field of TSV is given as:

$$\psi_n(\omega) = \psi_n(\omega) + \psi_m(\omega) = 2H_0\delta(\omega) - jkH_0F(\omega) + \mu Z\left(\sqrt{\frac{n^{(0)}}{2}}\delta_n + \sqrt{\frac{n^{(0)}+k^{(0)}}{2}}\delta_k, \delta_{n+1}\right) \tag{3.16}$$

The power absorbed by the TSV is:

$$P_s = \frac{A}{2\sigma} Re \int \frac{\partial\psi(\omega)}{\partial n}\psi^*(\omega)d\omega \tag{3.17}$$

Consequentially, the power absorbed to the zeroth $P_s^{(0)}$, the first order $P_s^{(1)}$, and the second order $P_s^{(2)}$ can be calculated as:

$$P_s^{(0)} = \frac{A}{2\sigma}|H_0|^2\frac{\mu Z}{n^{(0)}}\delta_n \tag{3.18-a}$$

$$P_s^{(1)} = 0, \tag{3.18-b}$$

$$P_s^{(2)} = \frac{A}{2\sigma}\frac{h^2}{2}|H_0|^2\frac{\mu Z}{\left(n^{(0)}\right)^2}\delta_{n+2}\left[1 - \frac{\delta}{h^2}\int_{-\infty}^{\infty} H(\omega)d\omega\right] \tag{3.18-c}$$

The total power absorbed by the TSV due the surface roughness becomes:

$$P_a = P_s^{(0)} + P_s^{(1)} + P_s^{(2)}. \tag{3.19}$$

The enhancement factor of the TSV with rough surface: k_s, which represents the ration of power dissipated per unit length with or without roughness, is determined as:

$$k_s = 1 + \frac{h^2}{2}\frac{1}{n^{(0)}}\frac{\delta_{n+2}}{\delta_n}\left[1 - \frac{\delta}{h^2}\int_{-\infty}^{\infty} H(\omega)d\omega\right] \tag{3.20}$$

The spectral representation of the magnetic field $H(\omega)$ asymptotically approaches an exponential correlation function; hence the overall integral converges to an exponential correlation function. As demonstrated above and further manifested within equation (3.20), the enhancement factor representing the absorption ratio can be calculated by analytical small perturbation method and is

directly correlated to the spectral density of the random surface roughness. How the power absorption varies with the frequency and the surface roughness height is demonstrated in Figure 3.3.

The surface roughness not only introduces more loss, but also impacts the value of the TSV impedance. Of most importance, the extraction of effective impedance and conductivity also telegraph the potential value for the case of the rough surface. For the sinusoidal disturbances in rough surfaces, impedance of power loss and conductivity effects arise which depend upon on TSV parameters; this topic is addressed in the next section.

Integrating the Poynting vector over the entire volume of the TSV, the time averaged power dissipated inside volume V is:

$$W = -\frac{1}{2} Re\left[\oint_{\partial V} d\Gamma \bar{n} \cdot (\bar{E} \times \overline{H^*})\right] \tag{3.21}$$

It can be written inside the conducting volume per unit length as,

$$W = -\frac{j\Delta}{\omega\varepsilon} \left\langle \frac{\partial}{\partial x} |H|^2 \right\rangle \tag{3.22}$$

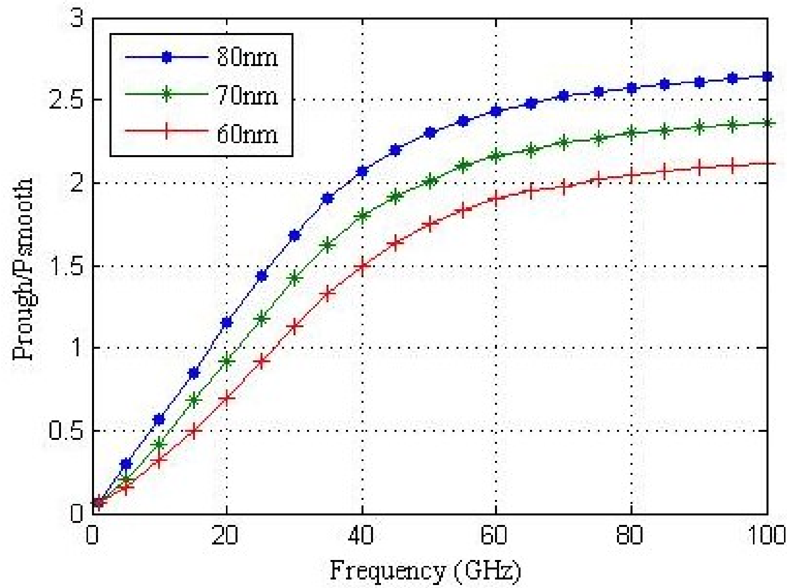


Figure 3.3: Power absorption ratio as a function of frequency by varying the roughness correlation height

The application of the small perturbation method on TSV quantitatively captures how the surface roughness impacts the interconnect loss.

Under an assumption of a shallow penetration, the power absorption of the conductor can be expressed as:

$$P_S = \frac{1}{2} R_S |H|^2 == \frac{1}{2\delta\sigma} |H|^2 \tag{3.23}$$

As analyzed above that, the presence of the roughness increases the power dissipation as a ratio of the power absorption enhancement factor given as:

$$k_S = \frac{P_{rough}}{P_{smooth}} \tag{3.24}$$

Besides additional power loss, the surface roughness also changes the impedance of the TSV as:

$$Z_{rough} = R_{rough} + jX_{rough} \tag{3.25}$$

3.4 Electrical Modeling of TSV

Three different approaches including analytical, numerical, and physical observation are commonly used to extract the Resistance (*R*), inductance (*L*), conductance (*G*), and capacitance (*C*) of the TSVs. In [47], assumptions inherent within these differing approaches are provided; their corresponding accuracy and limitations are clearly specified and validated by EM modeling and measurement.

To model the TSVs, analytical expressions of *RLGC* parameters are required; these are derived from the two wire transmission line equations [23], [48]. Analytical expressions of frequency dependent *RLGC* elements incorporated within the model account for differing geometric parameters, dielectric materials, electromagnetic permeability, effects of "lossy" substrate materials, and the medium. The frequency dependent resistance of a two wire transmission line can be expressed by:

$$R_t(f) = \frac{1}{r}\sqrt{\frac{\mu_0 f}{\pi\sigma}}\left[\frac{D}{\sqrt{D^2-(2r)^2}}\right] \quad (3.26)$$

where D is the pitch, r is the TSV radius, μ_0 is the permeability of the free space, and σ is the conductivity of the conductor.

The frequency dependent inductance can be calculated as:

$$L_t(f) = \frac{1}{\pi}\left[\mu_0 ln\left(\frac{1}{2r}\left[D+\sqrt{D^2-(2r)^2}\right]\right)+\frac{R_t(f)}{2f}\right] \quad (3.27)$$

The capacitance can be estimated as:

$$C_t(f) = Re\left(\frac{\pi(\omega\epsilon_0\epsilon_{Si}-j\sigma_{Si})}{\omega ln\left(\frac{1}{2r}\left[D+\sqrt{D^2-(2r)^2}\right]\right)}\right) = \frac{\pi\varepsilon_{ox}\varepsilon_{Si}}{ln\left(\frac{1}{2r}\left[D+\sqrt{D^2-(2r)^2}\right]\right)} \quad (3.28)$$

where ε_{0x} is the permittivity of the dielectric, ε_{Si} and σ_{Si} are the permittivity and conductivity of the substrate material, respectively.

Similarly, the conductance of TSV is given as:

$$G_t(f) = -\omega Im\left(\frac{\pi(\omega\varepsilon_{ox}\varepsilon_{Si}-j\sigma_{Si})}{\omega ln\left(\frac{1}{2r}\left[D+\sqrt{D^2-(2r)^2}\right]\right)}\right)$$

$$= \frac{\pi\sigma_{Si}}{\omega ln\left(\frac{1}{2r}\left[D+\sqrt{D^2-(2r)^2}\right]\right)} \quad (3.29)$$

To account the presence of the SiO_2 layer, a coaxial configuration of a single TSV conductor with a SiO_2 layer acting as an insulator is conceived. The coaxial capacitance is given as [2]:

$$C_{SiO_2} = 2\pi\varepsilon_o\frac{\varepsilon_{ox}}{ln\left(\frac{r}{r_{ox}}\right)} \quad (3.30)$$

where r_{ox} is the radius of SiO_2 layer and ε_o is the permittivity of the vacuum.

The depletion capacitance of the TSV can be calculated from:

$$C_{dep} = \frac{2\pi\varepsilon_{si}h}{ln\left(\frac{r_{ox}+w_{dep}}{r_{ox}}\right)} \quad (3.31)$$

where h is the TSV height and w_{dep} is the depletion width.

The depletion width is determined as:

$$W_{dep} = \frac{2\varepsilon_{si}}{3\varepsilon_{ox}}\left(-t_{ox} + \sqrt{t_{ox}^2 + \frac{3\varepsilon_{ox}^2}{\varepsilon_{si}}\frac{V-V_{FB}}{qN_a}}\right) \quad (3.32)$$

where $t_{ox} = r_{ox} - r$ is the SiO_2 liner thickness, V is the applied voltage, V_{FB} is the flat band voltage, N_a is the silicon doping concentration, and q is the electronic charge.

The variation of supply voltage could significantly change the depletion width; the equivalent circuit model considers the effects of voltage dependence and nonlinear capacitance. The equation for calculating the total TSV capacitance [36] in depletion and accumulation regions is summarized within the table I below.

Table 3.1: Total TSV capacitance

Region	**Depletion**	**Accumulation**
V	$V - V_{FB} > 0$	$V - V_{FB} < 0$
Cap	$C_{TSV}(V) = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{dep}}}$ $C_{dep} = \frac{2\pi\varepsilon_{Si}h}{ln\left(\frac{r_{ox} + w_{dep}}{r_{ox}}\right)}$	$C_{TSV} = C_{ox}$

Sidewall roughness adds an additional resistance to the TSV. The rough surface is characterized by the correlation length *l*, rms height of roughness *h*, and the correlation function. Two types of correlation functions, exponential and Gaussian, are generally used to characterize a rough surface of random profile. The exponential correlation function is significantly rougher than the Gaussian [43]. To generate the roughness profile, the spectral density, or the Fourier transformation of the correlation function is utilized.

For a 2D random roughness profile, the spectral density of the Gaussian correlation function is given as:

$$W(k_x) = \left(\frac{h^2 l^2}{4\pi}\right) exp(-\frac{k_x^2 l^2}{4}) \tag{3.33}$$

And the spectral density of the exponential correlation function can be calculated as:

$$W(k_x) = \left(\frac{h^2 l}{\pi}\right)(1 + k_x^2 l^2)^{-1} \tag{3.34}$$

The spectral density of the exponential correlation function decays very slowly with increasing k_x, indicating multi-scale roughness. From the analysis of power absorption in rough surface, the enhancement factor of the TSV is obtained as below:

$$k_s = 1 + \frac{h}{2}\left(1 - \frac{\delta}{h^2}\right) \tag{3.35}$$

It represents the ratio of power dissipated per unit length with and without roughness.

When the proximity effect is neglected, the TSV resistance can be expressed as:

$$R_{ac}(f) = \frac{h}{\sigma\pi\left[r^2 - \left(r - \delta_{Cu_skin}\right)^2\right]} = \frac{hf\mu_0}{d\sqrt{\pi f \mu_0 \sigma_{Cu}} - 1} \tag{3.36}$$

Table 3.2: Frequency dependent RL parameters

***RL* Parameter**	$f_{s_1} < f < f_{s_2}$	$f > f_{s_2}$
$R(f)$	$R_t(f)$	$R_t(f) + R_s(f)$
$L(f)$	$L_t(f)$	$L_t(f) + L_s(f)$

To model the resistance induced by the rough sidewall of TSV, equation (36) is utilized according to:

$$R_s(f) = k_s R_{ac}(f) \tag{3.37}$$

Considering the roughness effect, the additional inductance can be accounted as:

$$L_s(f) = \frac{R_S(f)}{2\pi f} \tag{3.38}$$

The presence of the roughness increases the power dissipation as a ratio of the power absorption enhancement factor as well as changes the impedance of the TSV as,

$$Z_{rough}(f) = R_{rough}(f) + jX_{rough}(f) \tag{3.39}$$

An analytical equivalent circuit model is created to model the TSV pair as illustrated in Figure 3.4. The model includes the parasitic elements that represent the loss, as well as the inductive and capacitive coupling in the conductor and insulating sidewall. Frequency dependent RL parameters of the model are listed within Table I for the skin effect and roughness, for two critical frequencies: f_{s1} is the frequency over which the skin depth becomes a quarter of the TSV radius (r) or smaller ($\delta \leq r/4$), and f_{s2} is the frequency beyond which the skin depth becomes comparable to the roughness.

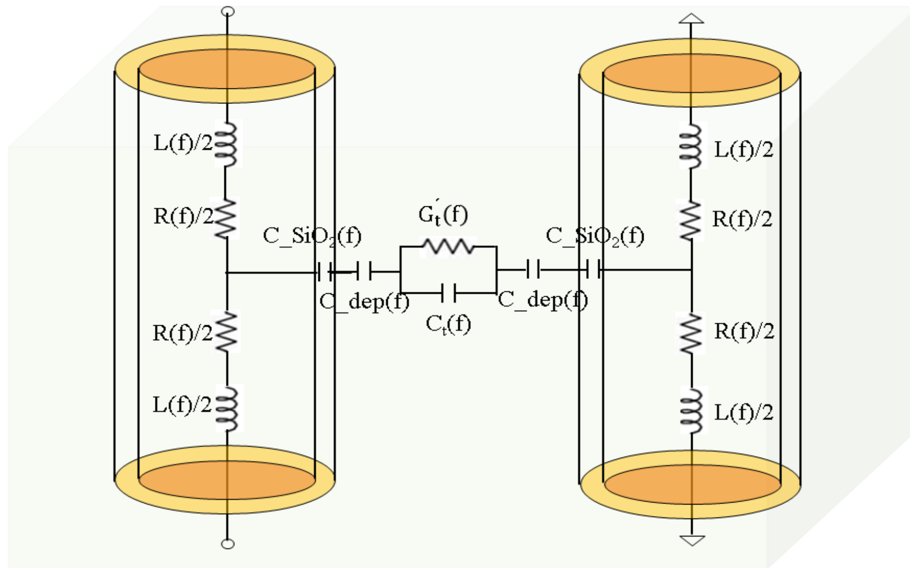


Figure 3.4: Equivalent circuit by considering the impact of sidewall roughness

The roughness height can be compared to the skin depth (δ) for $h_{roughness} = 11.6\%\ of\ \delta$ to $h_{roughness} = 24.6\%\ of\ \delta$ for the frequency 10 – 100 GHz in this model. The accuracy of the analytical model of TSV will be verified by comparison against the 3D field simulation based model. The simulation results are presented subsequently.

3.5 Simulation Results

This section describes simulation results accomplished with the 3D field solver High Frequency Structural Simulator (HFSS). The scattering parameters and coupling analysis for different TSV arrangements were performed. The proposed TSV circuit model is then validated by comparison to the full wave electromagnetic field simulation for accuracy.

3.5.1 Frequency Domain Electrical Performance

There are three different levels of bonding/stacking in a 3D integration using TSVs including wafer level, chip level, and interposer. Each level has its own criteria pertaining to characteristic TSV dimensions such as diameter, pitch, and height. Since the chip level and the wafer level have similar dimensions, only the chip level TSV is considered in the simulation. To investigate the impact of the sidewall roughness, the TSV structures with and without sidewall roughness are created as illustrated in Figure 3.5 and Figure 3.6. In each structure, a signal TSV is paired with a ground TSV.

The TSVs considered for the chip level have a radius of 10 µm, a pitch of 30 µm, and a length of 60 µm, respectively; while the TSVs for the interposer level have a radius of 30 µm, a pitch of 80 µm, and a length of 150 µm. The height of the roughness is chosen to be 72 nm which is comparable to the skin depth in the selected frequency range. Furthermore, some practical

measurement data of the sidewall roughness of TSV performed in [16] including the period of the scallop and the depth were utilized for the simulation. The TSVs were excited on the top and bottom surface with the lumped port.

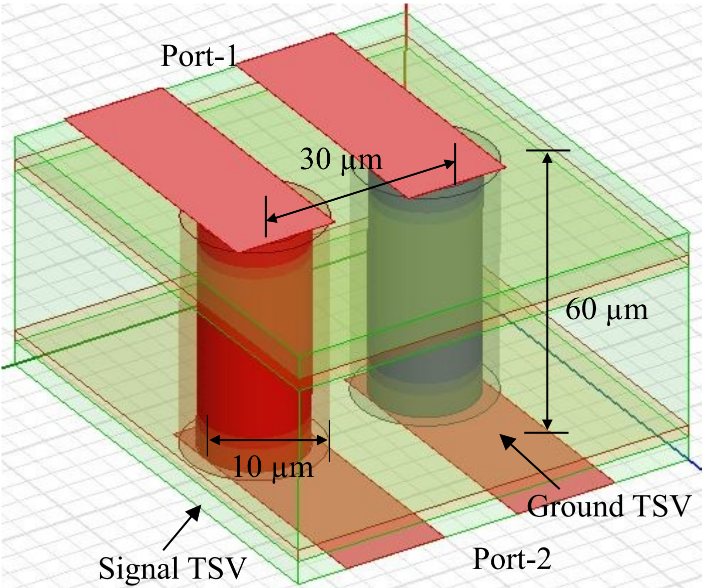


Figure 3.5: TSV pair (chip level) without sidewall roughness

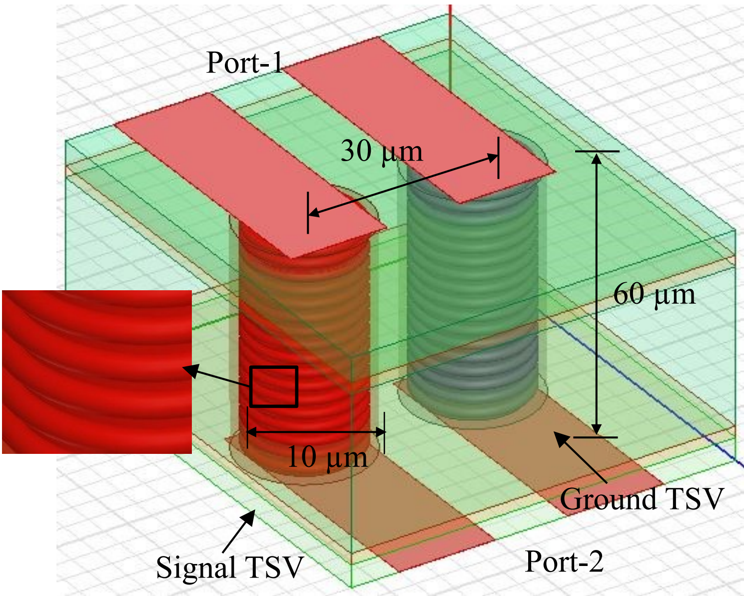


Figure 3.6: TSV pair (chip level) with sidewall roughness

The top and bottom surface were assigned as port 1 and port 2 respectively. The return loss (S_{11}) and insertion loss (S_{21}) of the structures are simulated by HFSS [49].

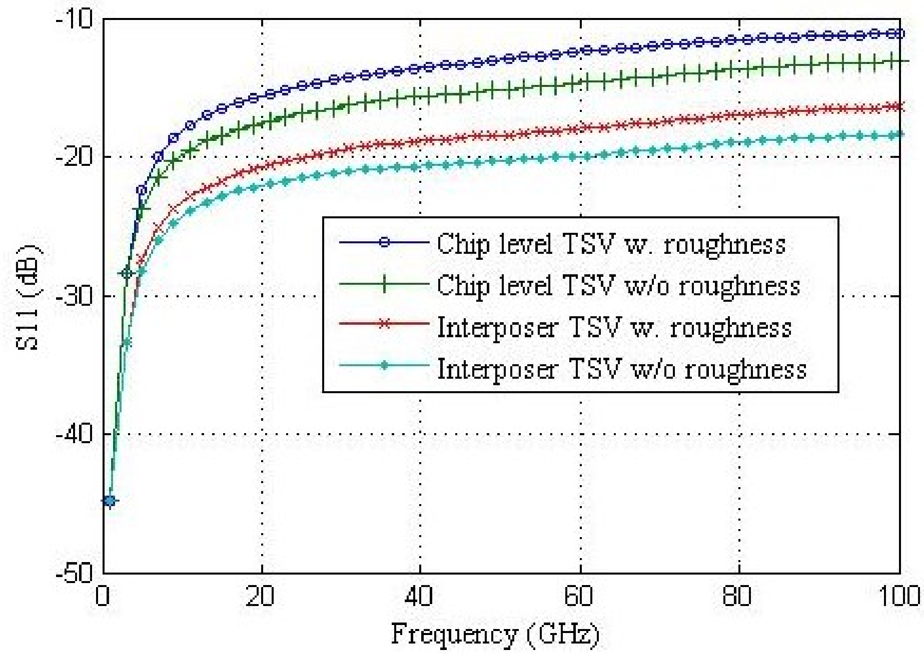


Figure 3.7: Comparison of S parameter (S_{11}) of TSV pair with and without roughness

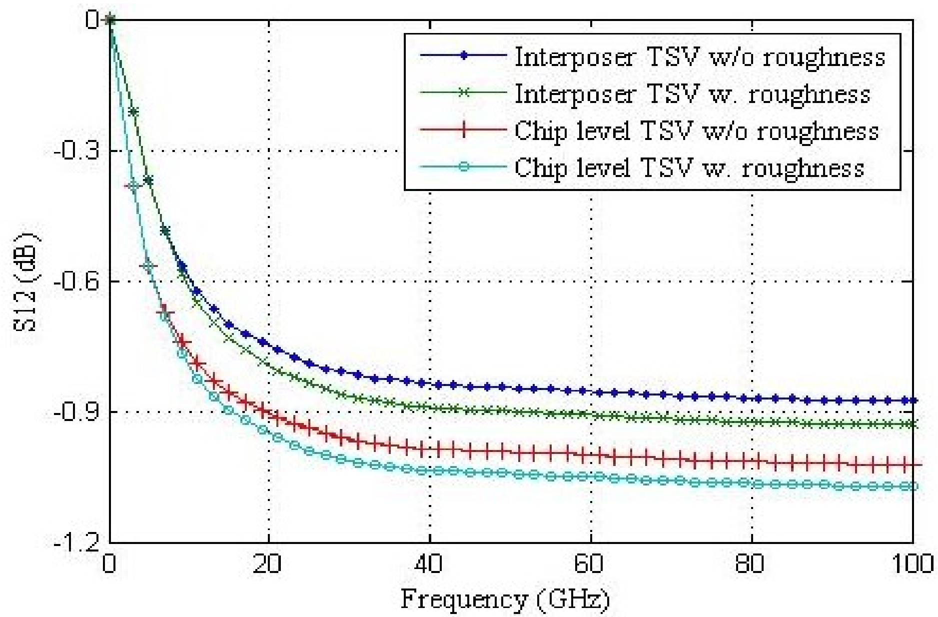


Figure 3.8: Comparison of S parameter (S_{12}) of TSV pair with and without roughness

The simulation results are presented within Figure 3.7 and Fig. 3.8. At a frequency lower than 10 GHz, no sufficient difference is perceived in either the return loss S_{11} or the insertion loss S_{21} between these two structures. However, the discrepancy in both S_{11} and S_{21} for these structures becomes appreciable when the frequency exceeds 10 GHz. As explained in Section III, the sidewall roughness alters the TSV impedance and induces additional loss.

These results substantiate that impedance matching becomes a critical issue for rough surface TSVs in the mmW frequency range. This difference between the rough surface and the smooth surface can be minimized by designing the TSVs appropriately with the assistance of an accurate model. Chip level and interposer TSVs have different electrical responses because their physical dimensions are different. Increasing the cross sectional area of TSVs lowers the impedances and hence decreases the insertion loss. Also a reduction in pitch increases the insertion loss; whereas a longer TSV has more attenuation. All these physical parameters affect the insertion loss of the TSV, and keep the insertion loss of any interposer TSV lower than the chip level TSV.

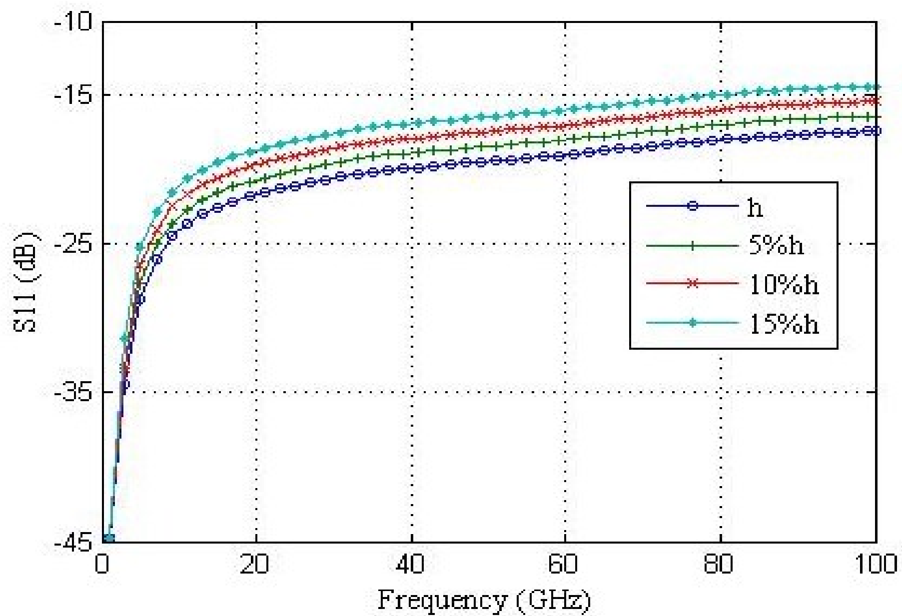


Figure 3.9: Variation of the height of the surface roughness interposer TSV to obtain S_{11}

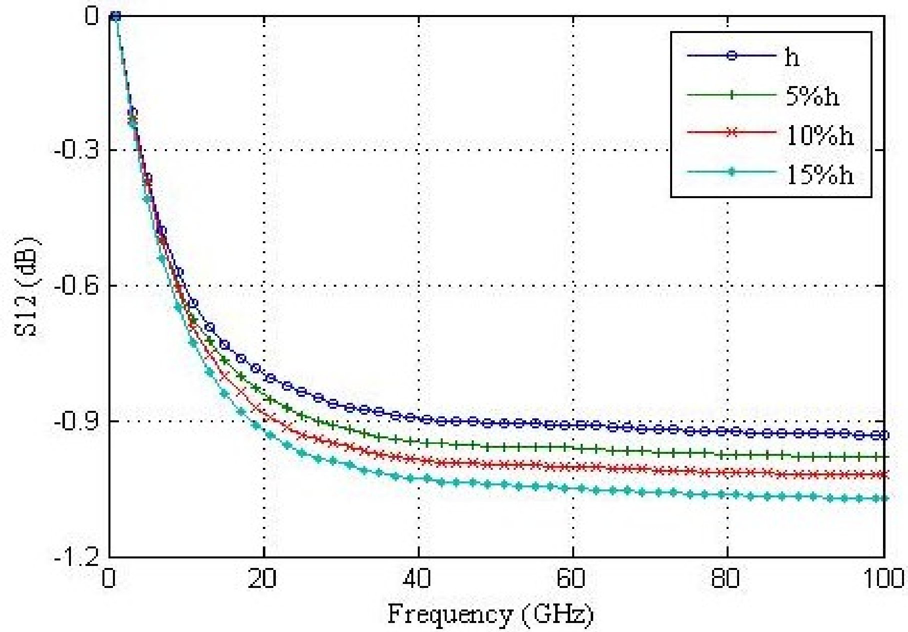


Figure 3.10: Variation of the height of the surface roughness interposer TSV to obtain S_{12}

On the other hand, a higher return loss that describes the good matching of a device results in lower insertion loss. The sharp slopes observed in S_{11} and S_{12} in below 10 GHz are caused by the transition from slow wave mode propagation to quasi dielectric TEM mode. The deviation between curves with and without the surface roughness is attributed to the additional impedance and power loss caused by the rough sidewall. Also, the structures are parametrically simulated with different roughness heights. In the simulation, the average height of the roughness varies 5%, 10%, and 15%, respectively. The return loss S_{11} and insertion loss S_{12} with different roughness are presented in Figure 3.9 and Figure 3.10. The variation of the roughness height results in noticeable changes in both the insertion and return loss at a frequency beyond 10 GHz. This finding substantiates that roughness indeed alters both the impedance and the loss characteristics of the TSVs. Also, S-parameter variations with respect to the surface roughness are illustrated in Figure 3.13 and Figure 3.14 in order to make a better comparison.

3.5.2 Validation of the Proposed Model

To validate the proposed models and estimate their accuracy, the model predicted S-parameters are compared to HFSS simulations for the TSV structures considered within this work. Figure 3.11 and Figure 3.12 show the comparison between S-parameters in magnitude.

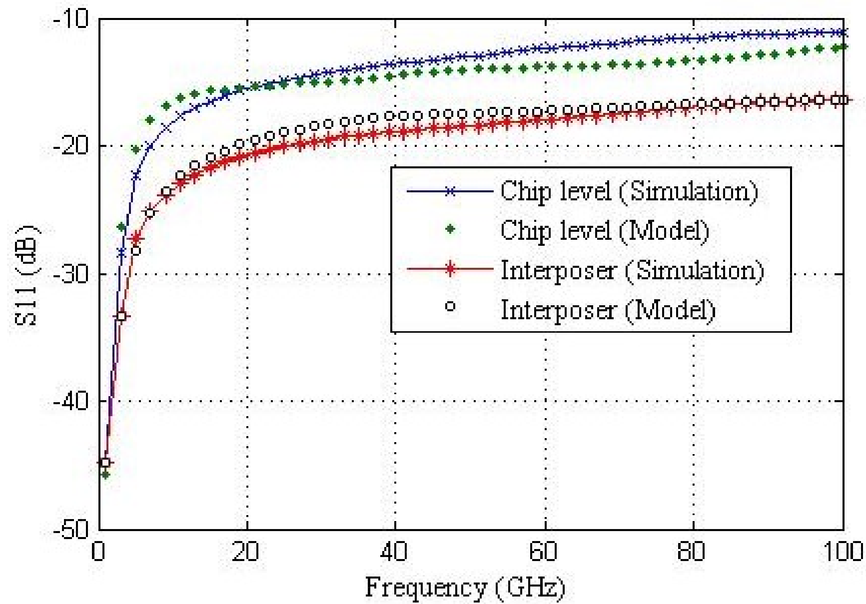


Figure 3.11: HFSS simulation versus analytical model of TSV pair (S_{11}) with surface roughness

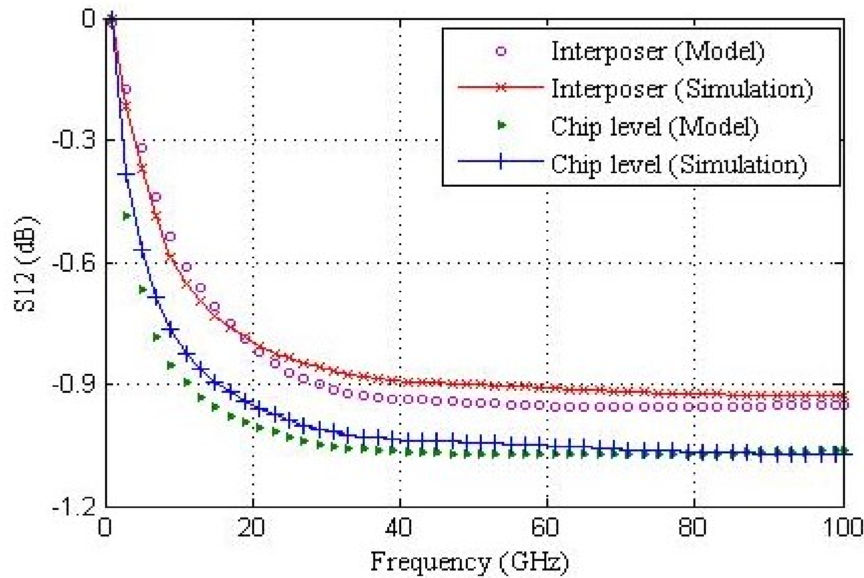


Figure 3.12: HFSS simulation versus analytical model of TSV pair (S_{12}) with surface roughness

In general, good correlations between the model and HFSS simulations are observed for both the chip level TSVs and interposer TSVs. Figure 3.15 and Figure 3.16 demonstrate the comparison between S-parameter in phase, which also shows a better agreement between the modeling and simulation.

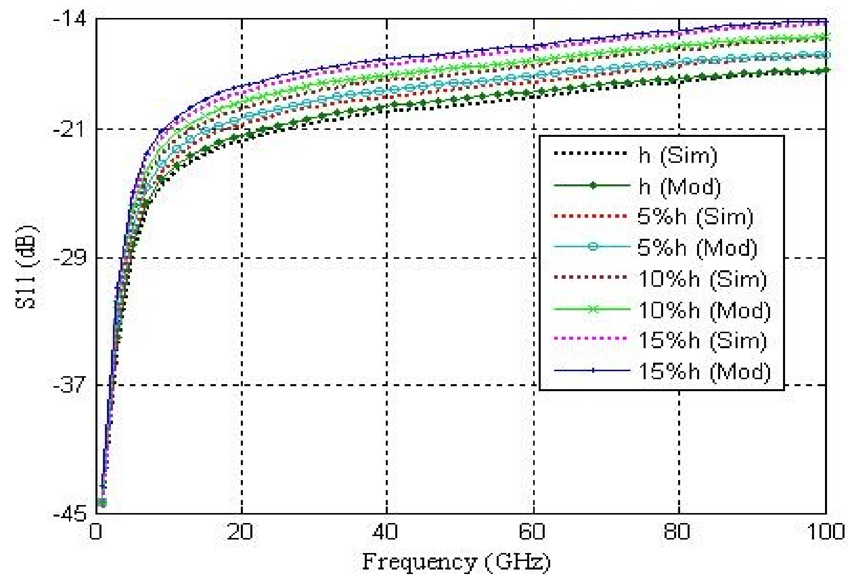


Figure 3.13: HFSS simulation versus analytical model of TSV pair (S_{11}) by the variation of roughness parameter

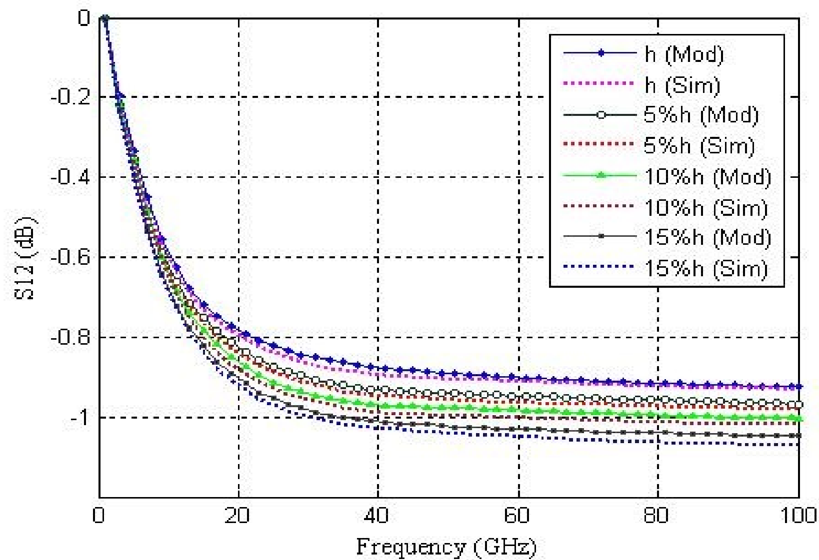


Figure 3.14: HFSS simulation versus analytical model of TSV pair (S_{12}) by the variation of roughness parameter

However, small deviations between the models and HFSS predictions are observed. Rather than this, the modeling of S-parameter is plotted in Figure 3.13 and Figure 3.14 by varying the roughness parameter which agrees with the simulation result plotted in Figure 3.9 and Figure 3.10, respectively.

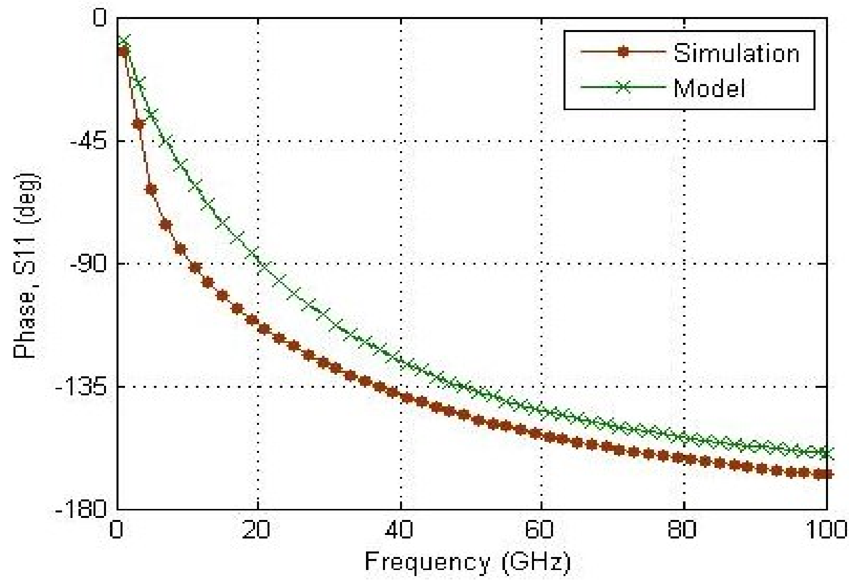


Figure 3.15: HFSS simulation versus analytical model of TSV pair (S_{11}) considering the phase

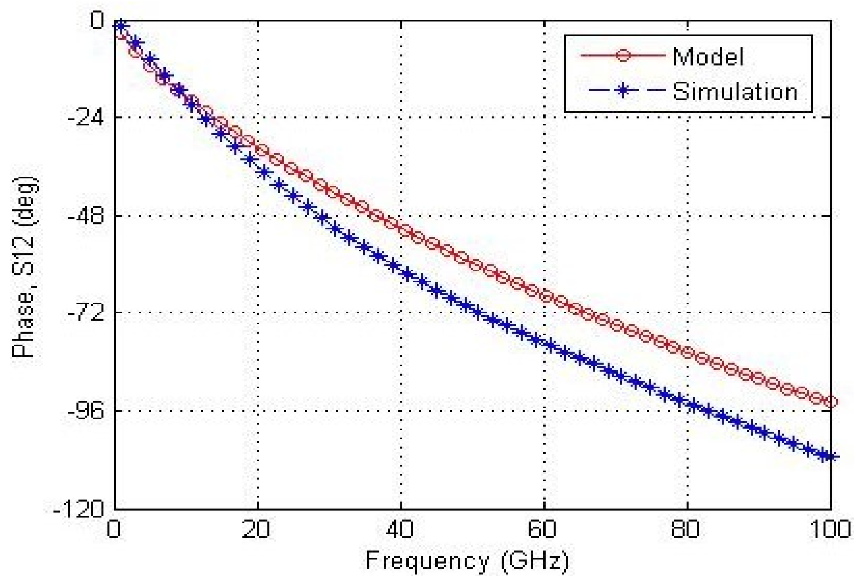


Figure 3.16: HFSS simulation versus analytical model of TSV pair (S_{12}) considering the phase

As shown in Figure 3.11 and Figure 3.12, the maximum relative error at 50 GHz in S_{11} is 12.8% for chip level TSV and 5.40% for the interposer TSV. While for S_{12}, a maximum relative error of 6.61% for interposer TSV and 11.43% for chip level TSV is obtained. The causative factors for the small discrepancies originate from considerations involving boundary conditions and excitation method. Regardless of the small discrepancy, the good correlations between the model and HFSS predicted S-parameters appear to validate the accuracy of the proposed model.

Chapter 4

Investigation of 3D Neuromorphic Computing System

4.1 Introduction

Neuromorphic computing refers to the alternative physical model of biological neural system that provides electronic implementation of artificial neural network and significantly contribute towards the development of neuro-biological architecture. It could mimic and implement the relative characteristics of biological neural networks in their physical layout and applicable to different system that accelerates the computation of neural network and machine learning algorithm [50]. Neural hardware systems have recently become very popular that describes the deep understanding between the morphology of neurons, electrical circuit model and overall architectures of biological nervous system which requires a very precise and intelligence computation. In this chapter, we studied about the neuromorphic hardware systems and the necessities of their implementation in 3D integrated system. Finally, we explored a novel 3D neuromorphic system that utilizes the TSV interconnects to build the complicated hardware neural structure.

4.2 Simple Spiking Neuron Model

The fundamental unit of neural system is neuron where the biological neuron consists of soma, dendrite, synapses and axon. Inside the neuron, a transient potential difference produces a signal

and it travels along the axon to the central nervous system. The neuronal information transmission and processing happen through electrical and chemical signals which are the basic independent units in a neural system. Synapses are the connections between two neurons and being used for the regulation of signal transmission among the connected neurons.

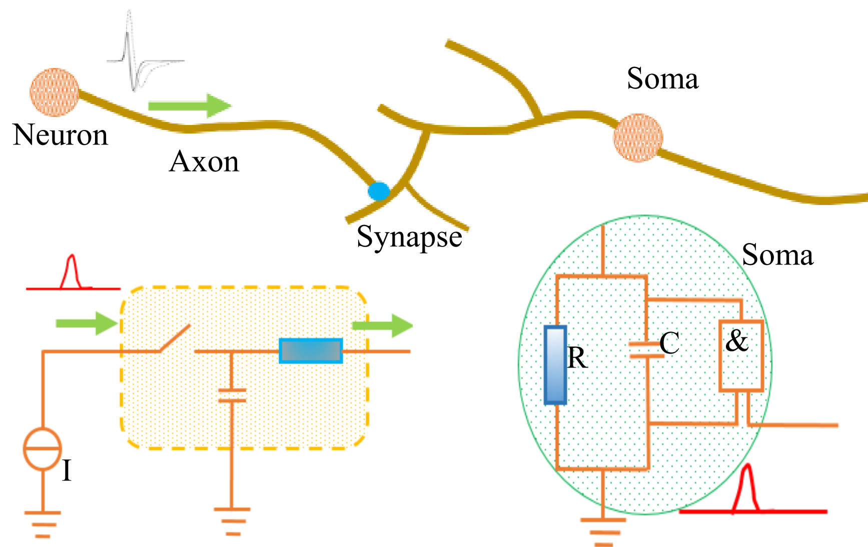


Figure 4.1: Simple example of formal spiking neuron model [51]

To understand the different electrophysiological behavior in neuromorphic system, it is necessary to learn about the electrical model of neuron with associated synaptic signaling process and membrane firing activity. A formal spiking neuron model is shown in Figure 4.1, which produces the voltage difference that provides a basis for electrical signal transmission between different parts of the neuron. There are different neuron models like integrate-and-fire (IF) model [52], leaky integrate and fire (LIF) model [53], Hodgkin-Huxley (HH) model [54], Fitzhugh-Nagumo (FN) [55] model are available and very well-known [56]. Among different neuron models, LIF model is the most popular one due to its simple structure and high accuracy.

4.3 Neuromorphic Computing System

Neuromorphic computing could exploit the properties of brain–inspired computing system by using integrated CMOS technology. To reproduce the biophysical process, neuro-computing approaches attempt to model the fine detail of neural architecture and the computational principles as well. This section describes about the neuromorphic hardware system, and the state-of-art of current neuromorphic systems.

4.3.1 Neural Hardware System

Neuromorphic technology and artificial neural network computation has been immensely popular during the last couple of decades, but its hardware implementation is running into stones in the pass-ways [57].

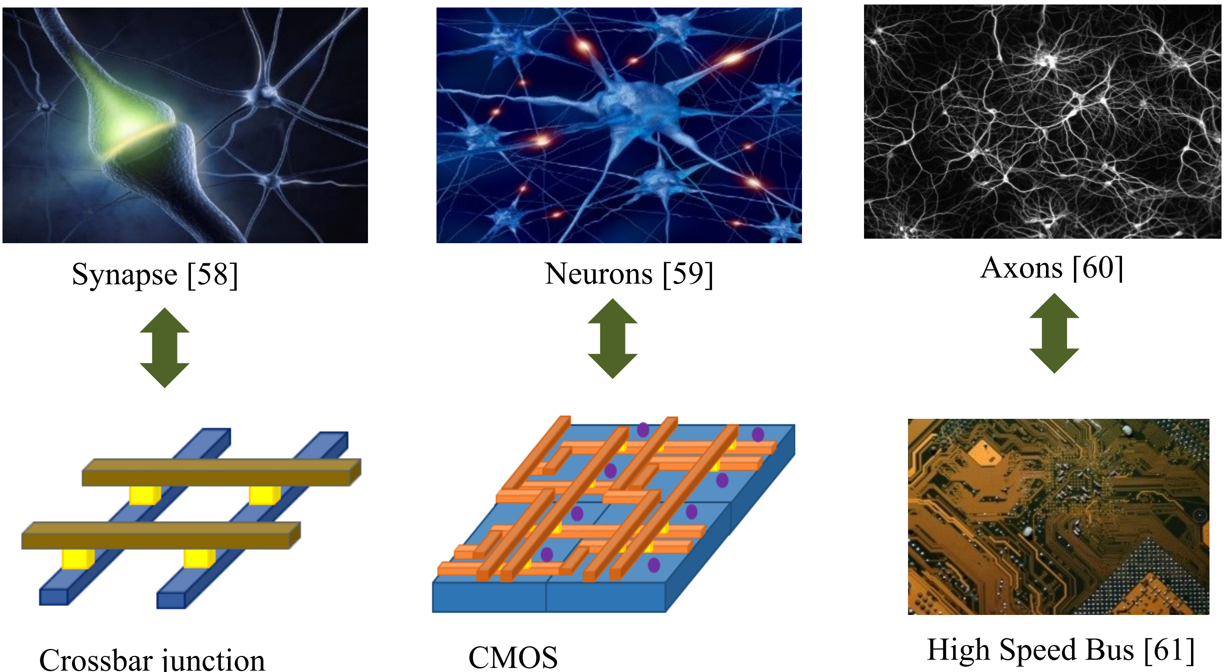


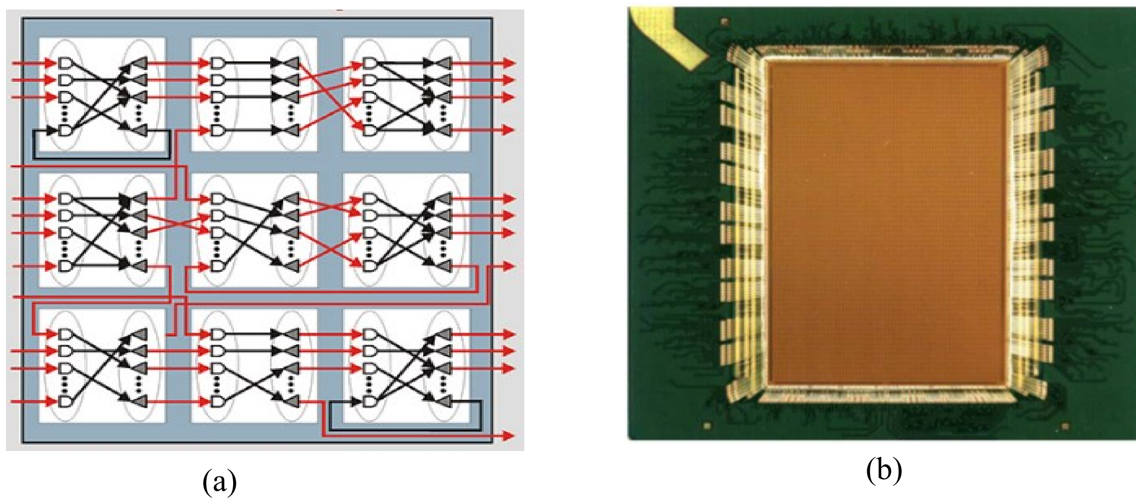
Figure 4.2: Hardware implementation of biological neural system

In order to realize the true potential of neuromorphic computing, very-large-scale integration (VLSI) technology is very important, which relies on analog, digital, and mixed-signal integrated

circuit (IC) systems [62]. In a neural hardware system, neurons can be represented by CMOS substrate, while axons and dendrites are implemented by nanowires as high speed bus; the junctions of crossing wires constitute synapses. Figure 4.2 illustrates the hardware implementation of biological neural system. Compared to conventional computing schemes, neuromorphic chips can operate faster and more efficiently, because they apply circuits and system principles of neuronal computation and learning dynamics. Synaptic configurabilities and basic operations for rudimentary neural chips with a large number of synapses have already been tested and verified by associative learning experiments.

4.3.2 Neuromorphic Chips: The State of the Art

The existing neuro-computing hardware is mainly 2D integrated circuitry, as illustrated in Figure 4.3, and it can all be categorized as spike based VLSI chips for signal transmission [63], pulse based neural multichip systems [64], and memristor based integrated neuromorphic architectures [65]. To reproduce biophysical processes, there are some promisingly potential neural chips, such as the TrueNorth chip; neural chips have also been devised by IBM, Neurogrid, Stanford University, and by the EU FET HBP BrainScales project [66].



(a) (b)

Figure 4.3: TrueNorth Chip (a) Architecture of logical representation [70] (b) Die Photo [71]

The brain inspired TrueNorth chip is fabricated with Samsung's 28 nm LPP CMOS process technology, and contains 5.4 billion transistors and 4096 interconnected neurosynaptic cores, which integrate 1 million programmable spiking neurons and 256 million configurable synapses [67]. The power density of this neural chip is 20 mW per cm^2, which is significantly lower than a typical desktop or laptop central processing unit (CPU).

The Neurogird chip system used 180 nm process technology which consists of 16 neurocores of 12×14 mm^2, that are organized in a tree routing network fashion [68]. The neurocores are assembled on a 6.5×7.5 in^2 circuit board, where each core can support up to 256×256 silicon neurons. The European Union BrainScale neuromorphic hardware system is based on wafer-scale integration of mixed-signal circuital system where silicon wafers with identical and tightly connected arrays of chips are used. Each 20 cm diameter silicon wafer contains 384 HICANN chips (High Input Count Analog Neural Network) of 180 nm CMOS technology with 200,000 neurons and 49 million synapses [69]. All of these neuromorphic hardware design and implementation are based on traditional 2D integration and may be incapable of ever emulating the massive parallelism inherent to biological neurons.

4.4 Why 3D Integration in NC IC

Neural systems are highly complex; the connectivity densities and massively parallel processed circuital systems are required to engage in highly demanding computational tasks; 2D circuits may not fulfill these requirements. 3D integrated circuit technology offers a promising solution to meet these requirements, while being contemporaneously compatible with current fabrication technology. For the realization of innumerable connections among neurons in the brain, high-density 3D synaptic networks rather than 2D ones will be essential. Figure 4.4 compares the low

density 2D synaptic network and the 3D implementation; the integration density significantly increases toward that of the biological ideal.

Applying 3D integration technology to create a neuromorphic hardware system addresses the 2D neuron routing congestion problem, thereby increasing interconnectivity and scalability of the NC network and reducing critical-path lengths. This emerging technology not only allows numerous 3D interconnections between hardware layers for offering high device interconnection density but also ensures low power density, and broad channel bandwidth using fast and energy efficient links.

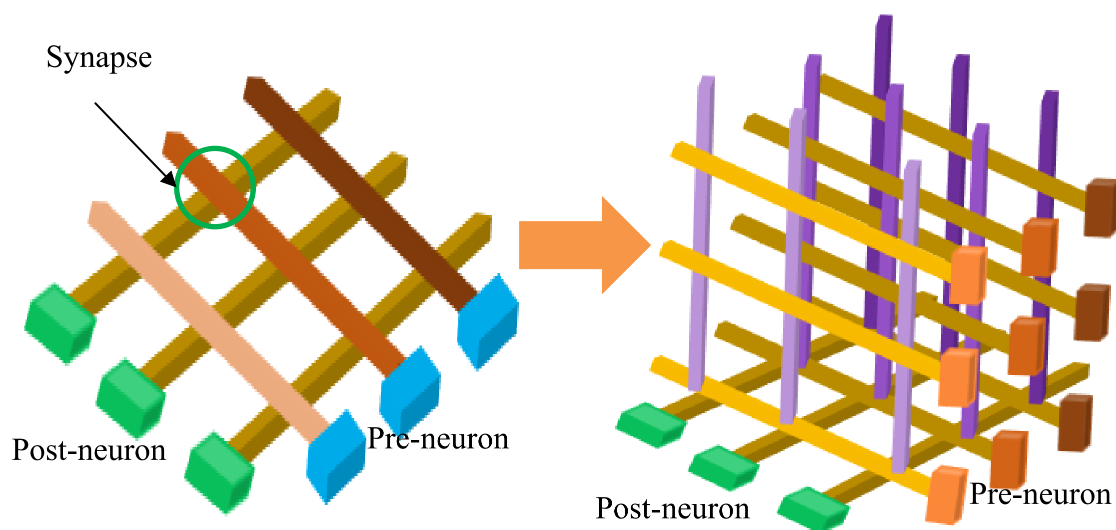


Figure 4.4: 2D synaptic network → high density 3D synaptic network in biological system [72]

To maintain design rules and constraints involving adverse electromagnetic side effects, numerous TSVs will be required within any 3D IC; this results in parasitic capacitance behavior. However, a propitiously adventitious circumstance has arisen, because analog neurons require large capacitance values. Hence the TSVs are complementarily beneficial to the circuitry of the analog neuron.

Moreover, to model the information processing capability of the human brain, especially that capability commensurate to the brain's image processing and pattern recognition processes, a huge array of interconnected parallel memory is required. The only currently feasible way to achieve such an advanced parallel processing network is to interconnect layered structural modules, wherein the basic modular processing units is the spiking neural network.

4.5 Proposed 3D Neuromorphic Structure

Neuromorphic 3D structures basically consist of hybrid circuitry that integrates conventional CMOS chips with several layers of nanoscale devices using high density vertical interconnects as shown in Figure 4.5 and Figure 4.6. The 3D neuromorphic device is mounted on a semiconductor substrate and each chip in the 3D structure represents a functional unit.

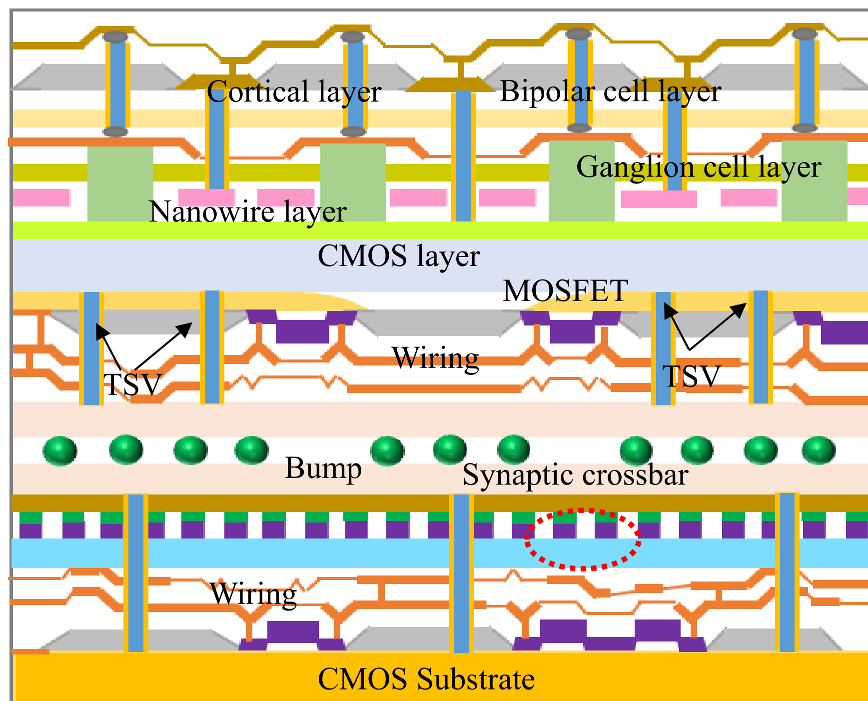


Figure 4.5: Cross-section of 3D neuromorphic structure (Face to face)

Neurons are represented by CMOS substrate, axons and dendrites are composed of nano-wires illustrated as high speed bus, and synapses are denoted by crossbar junctions. Figures 4.5 and 4.6 reveal some details of face to face and face to back neuromorphic structures, respectively. In neuromorphic 3D circuits, a memristive device is used to provide the high density interconnect with a crossbar circuit, as shown in Figure 4.7. Because of their nano scale dimensions, their capacity to store multiple bits of information per element, and the low energy required for writing distinct states, crossbar circuits are regarded as a particularly promising solution for simulating key features of the biological synapse.

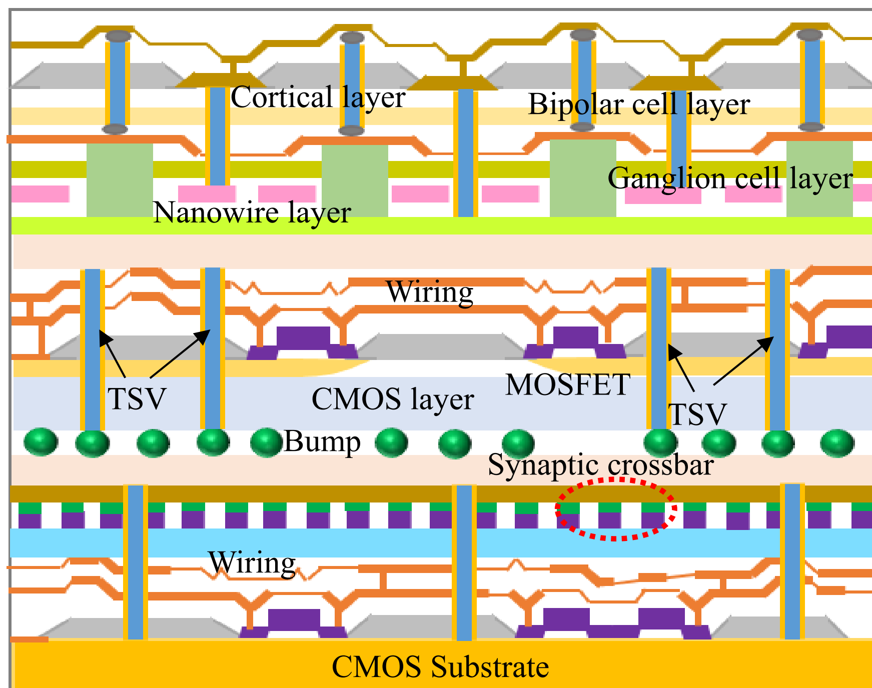


Figure 4.6: Cross-section of 3D neuromorphic structure (Face to back)

A synaptic crossbar circuit is a two terminal resistive switching device, and consists of parallel network of nanowires above and below, with nano-devices sandwiched between the layers at each crossing point. By applying voltage between the nanowires, the interstitial nano-devices can show high conductivity or resistive states successively. The CMOS substrate that presents the neuron

can be implemented by the trans-conductance mode, where the CMOS input and output neurons are connected by a bipolar synaptic device. This permits the use of tunable synapses in the circuit; but this CMOS implementation of the neuron necessitates a large membrane capacitance to store the internal voltage. Whereas 3D circuits with CMOS substrate could enable unprecedented transistor densities (up to 5×10^8 transistors/cm^2 and 500 transistors/neuron) and aggregate a huge number of spiking neurons at manageable power dissipation. The axons and dendrites are implemented by a high speed bus operating at multi Gbit/sec and interconnected by the wires. The footprint of the axons and dendrites could be very small and essentially defined by the micro-circuits in 3D implementation.

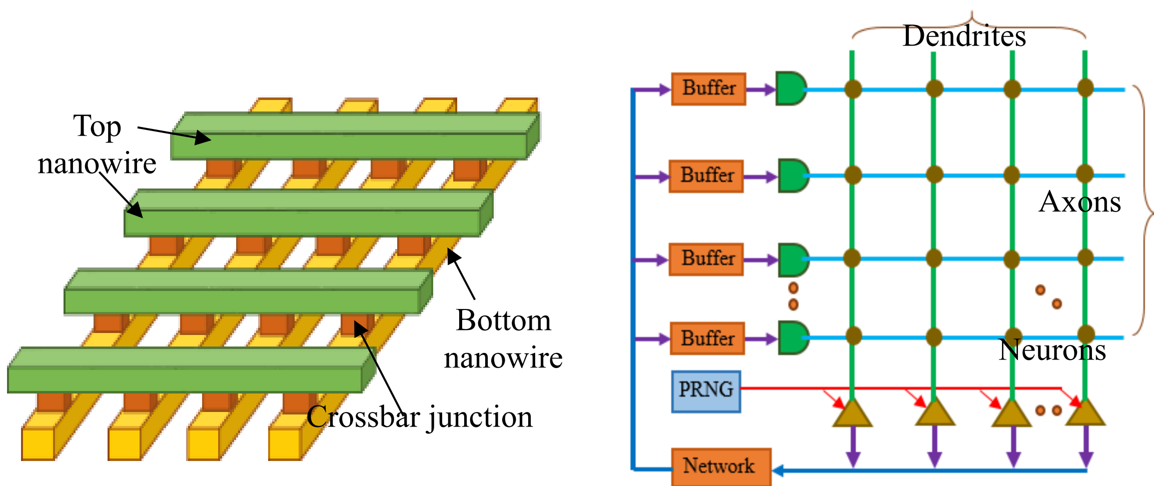


Figure 4.7: Neuromorphic synaptic crossbar structure

The 3D structures illustrated in Figures 4.5 and 4.6 are intended to represent a brain and retina, and contain a cortical layer, a crossbar junction, a bipolar cell layer, and a ganglion cell layer. Operational amplifiers and a resistor network are connected to form the bipolar and ganglion cell layers. The cortical cell layer consists by combining simple and complex cells, and performs the function of orientation and directional detection. The signals in every pixel are simultaneously transferred and processed in parallel in each layer. The neuromorphic electronic architecture of the

brain and retina is fabricated by using CMOS IC; as a result it contains a myriad of microcircuit and TSV interconnects. These TSV structures, heretofore overlooked, can be engineered to offer a great deal of benefits for a neuromorphic 3D IC.

Chapter 5

TSV Based 3D Neuronal Membrane Model

5.1 Introduction

This chapter details neuronal membrane electrical activities, and relate how a 3D neuromorphic system can be implemented with TSV capacitance. We propose a novel 3D neuromorphic computing architecture by exploring different TSV configurations; we subsequently adapt them into the role of augmented capacitors, and then we conceive an optimized CAD framework to model the complexities of these devices and circuits. We arrived at two new methodologies to enhance TSV capacitance to supply sufficient membrane capacitance for the synaptic signaling process, especially in a spike firing analog implementation of neurons in a proposed 3D system. In addition, a commensal membrane potential for a 3D neuromorphic system is derived to closely resemble the required membrane charge distribution characteristics and accounting for the target TSV capacitance. The electrical performance of the 3D neuromorphic chip is compared against 2D counterpart designs.

5.2 Neuronal Membrane Capacitance

The membrane is a fundamental unit of a neuron in a neural system. Figure 5.1 illustrates the structure of the cell membrane of a neuron. In a neuronal cell body, the transportation of ions happens through the membrane which consists of bi-layer lipid and regulates the vital cell characteristics. The ions penetrate the lipid layers through some specific ion channels composed of proteins. These ion channels have significant contributions for signaling the central nervous

system and some electrical excitability to some other particular cells. Figure 5.2 demonstrates the transportation of ions through the membrane where the concentration gradient of ion drives the movement of ion through the cell layer.

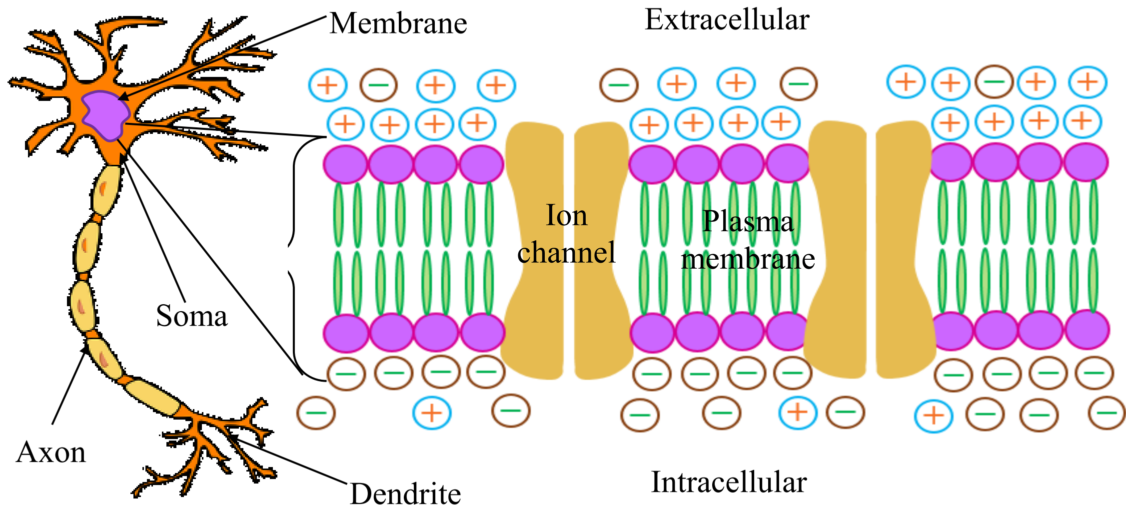


Figure 5.1: Structure of the cell membrane of a neuron

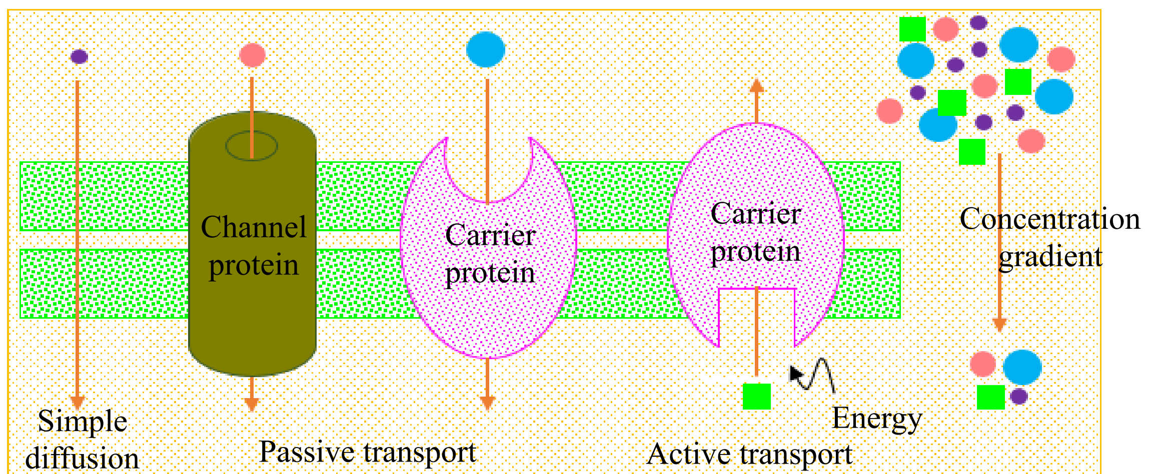


Figure 5.2: Ionic transportation through membrane

The membrane capacitance is the stored charge of ions across either side of the cell that results from the membrane composition of bilayer phospholipids. The membrane has unique

characteristics such as accumulating ions at intracellular and extracellular side and inhibiting their movements passing through the membrane. Thus the cell membrane serves as an insulating dielectric between the intracellular and extracellular fluid. Ionic charges exist on each side of the dielectric can be realized from Figure 5.1. This disequilibrium ionic charge on each side of the membrane generates a potential difference by the existing electric field which forms the membrane capacitance C_m as shown in Figure 5.3.

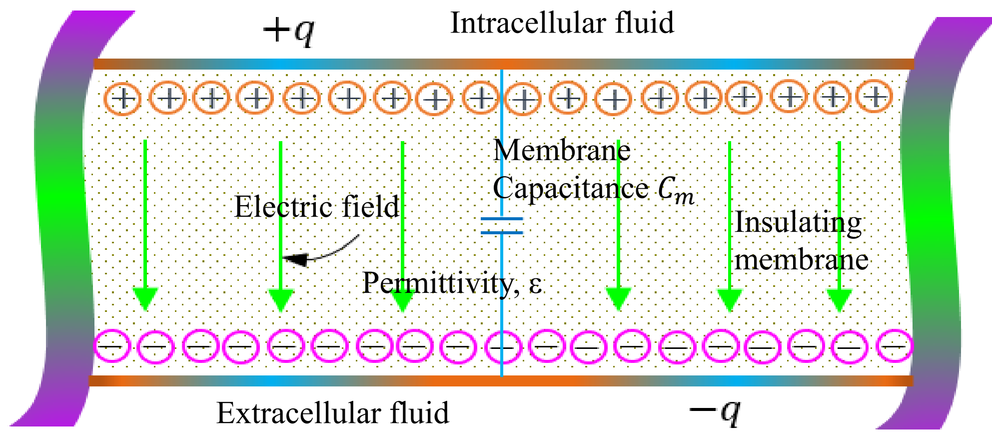


Figure 5.3: Capacitance formation at Neuron membrane

5.3 TSVs in Neuromorphic 3D IC

TSVs are being used in 3D neuromorphic system for enabling the vertical connections that route the signals through the layers of the neuron chip and provide lower interconnect lengths with a smaller footprint. However, there are numerous redundant and dummy TSVs along with the regular TSVs and we proposed these unused TSVs to reconfigure as membrane capacitance.

5.3.1 Dummy TSVs in 3D IC

Dummy TSVs are required in 3D ICs because foundries impose a minimum TSV density rule to maintain the planarity of the wafer during chemical and mechanical polishing (CMP). This rule

results in a nimiety of redundant, superfluous, or dummy TSVs; for example, the 3D-MAPS processor contains 2,240 dummy TSVs [73] [74]. These redundant TSVs are also used to enhance chip yield because unused TSVs can automatically replace defective TSVs; in this manner a good balance between yields and design overhead can be maintained. Researchers employed different grouping ratios of regular and redundant TSVs for the improvement of yield and reliability in 3D IC. Such an example is illustrated by Figure 5.4.

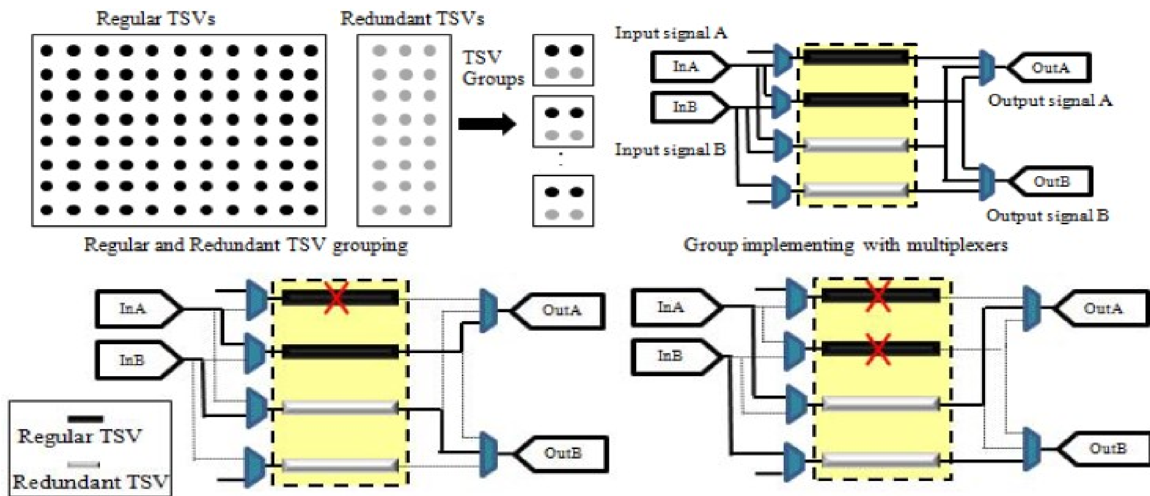


Figure 5.4: Grouping technique of regular and redundant TSVs [78]

However, TSV failure is a low probability event; it has been reported that only 15% – 25% of the redundant TSVs in 3D chips are truly necessary [75 – 77]. Therefore, redundant TSVs occupy a significant portion of design area in 3D IC.

5.3.2 TSVs as Membrane Capacitance

The TSVs in a 3DIC are composed of a metal conductor lined with insulating dielectric, and buried in a silicon substrate; analogous to the MIS structure shown in Figure 5.5. The charges in a TSV under a bias condition closely resembles the ions in the lipoprotein structure of a cell membrane which is under an active transportation. Therefore, depending on the substrate doping and voltage

applied, a capacitance is formed between the metal and the substrate in different regions, according to accumulation, depletion, and inversion. We proposed to use this TSV capacitance as membrane capacitance in the neuromorphic 3D system.

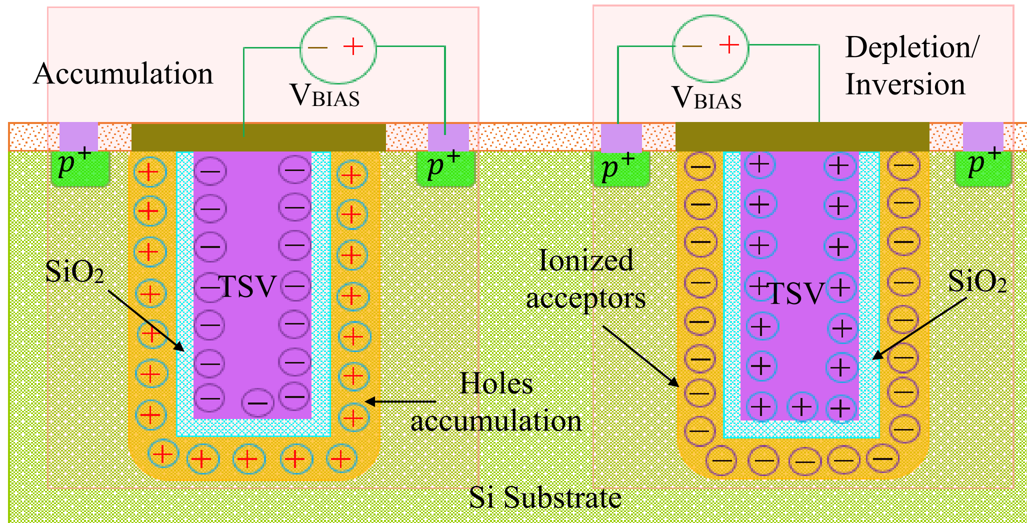


Figure 5.5: MIS capacitance formed by a TSV in silicon substrate

The realization of desired membrane capacitance consumes a significant portion of the design footprint for neuromorphic chips. According to various state of the art IC implementations of neurons, these capacitors occupy from ¼ to ¾ of the total design area [79 – 83]; Table 1 summarizes some of this data.

Table 5.1: Neuromorphic membrane capacitance

Neuron Tech	Cap Value	Area	Ref
Analog	1.1 pF	29%	[79]
Mixed	N/A	56%	[80]
Analog	860 fF	49%	[81]
Analog	300 fF	26%	[82]
Analog	200 fF	73%	[83]

We designed and fabricated the first generation of analog spiking neuron encoder in 2015; a second generation of the temporal analog neural encoder followed in 2016 and these are presented in Figure 5.6 [84]. As shown in Figure 5.7 which is the layout of a single neuron in the fabricated neural encoder, the capacitor consumes a significant portion of the neural encoder's design area.

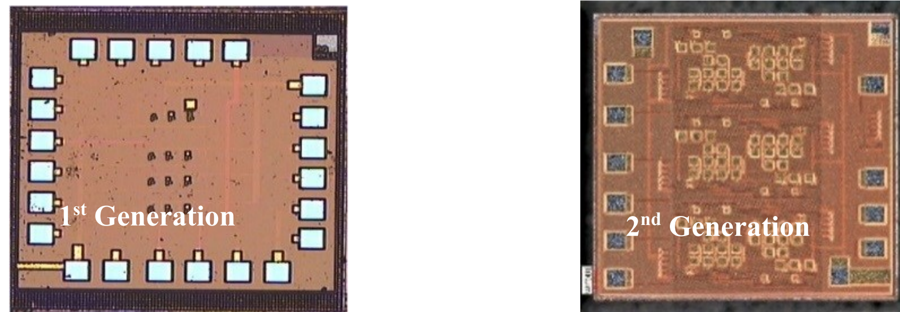


Figure 5.6: Fabricated chips of designed neural encoder [84]

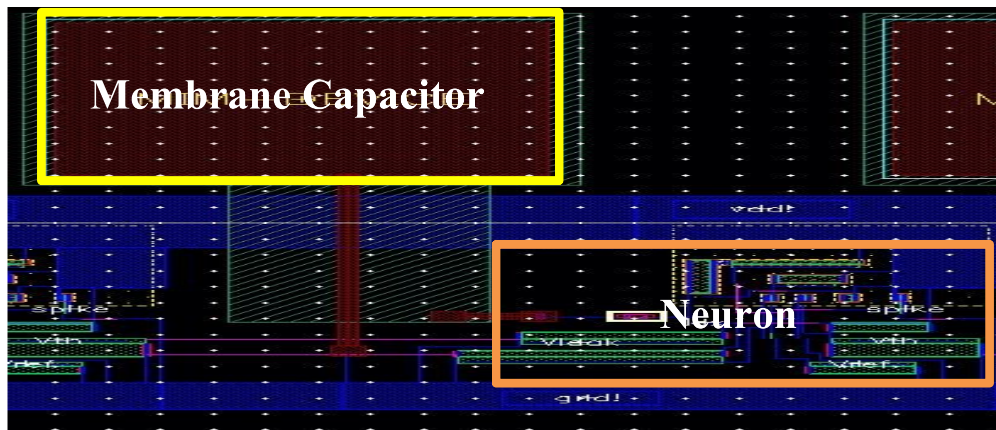


Figure 5.7: Layout of a single neuron in neural encoder [84]

As the membrane capacitance occupies a significant portion of area in neuromorphic chip and dummy TSVs also do same in 3D system; therefore, incorporating TSVs as membrane capacitance in a 3D system offers enormous opportunities for neuromorphic system design.

The physical architecture of utilizing the dummy TSVs as membrane capacitance is shown in Figure 5.8, where active TSVs are also used as interconnects to transmit signals.

TSV capacitors start showing their ineffectiveness at frequencies higher than 100 Hz because TSV capacitance at typical operating voltages is dominated by the depletion capacitance, which is much less than the oxide capacitance.

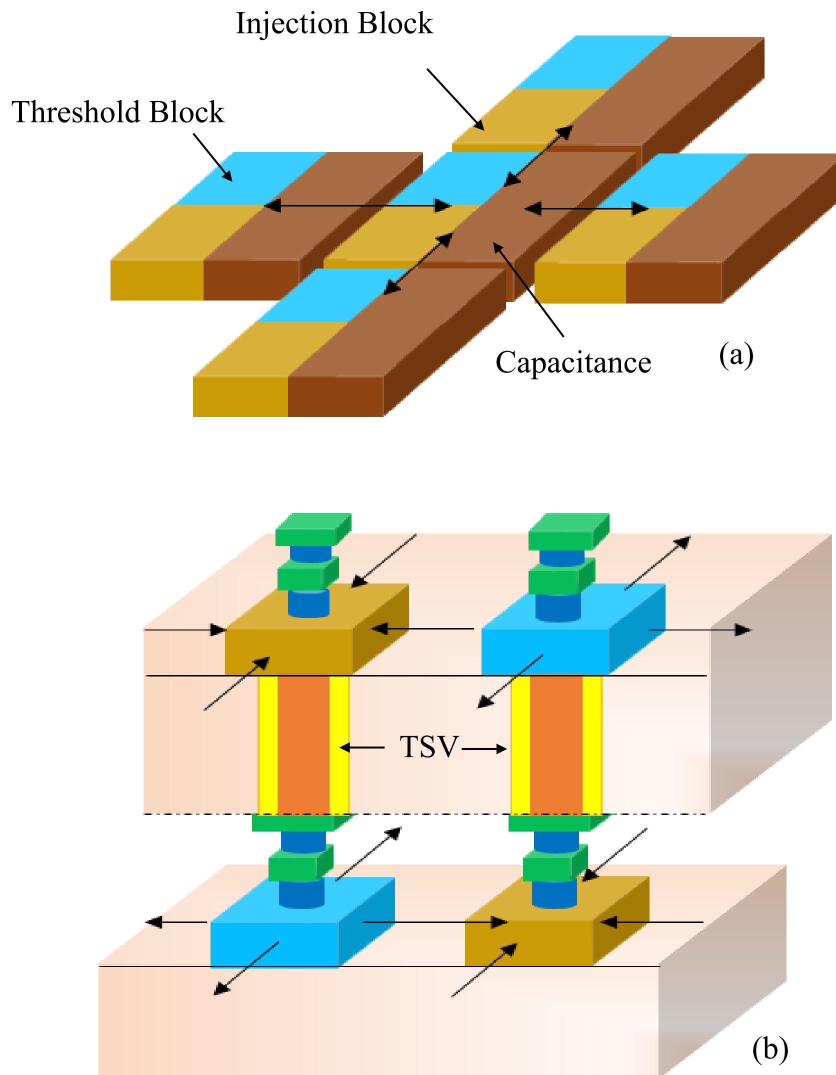


Figure 5.8: Neuromorphic architecture introduces capacitance (a) 2D (b) TSV based 3D IC [85]

Hence, it is necessary to increase the parasitic capacitance of the TSV in the depletion region, as well as the total capacitance, in order to enhance the performance of NM 3DIC. Without changing any physical geometry and process mechanism, increasing the capacitance of TSV can be

accomplished merely by introducing an oxide layer circumscribing the bump, and by reducing of the width of the depletion region.

5.4 TSV Capacitance Enhancement

In this section, two new techniques, such as an additional bump oxide [86], and a reduction of the depletion region [87] are described. The analytical equations of the capacitance for each of the techniques are discussed.

5.4.1 Addition of Bump Oxide

As illustrated in Figure 5.9, the metallic connection for an electrical path that stacks the vertical dies consists of TSVs, redistribution layer (RDL), inter-metal dielectric (IMD) layer, and the physical solder "bumps" between the chips beneath the TSVs.

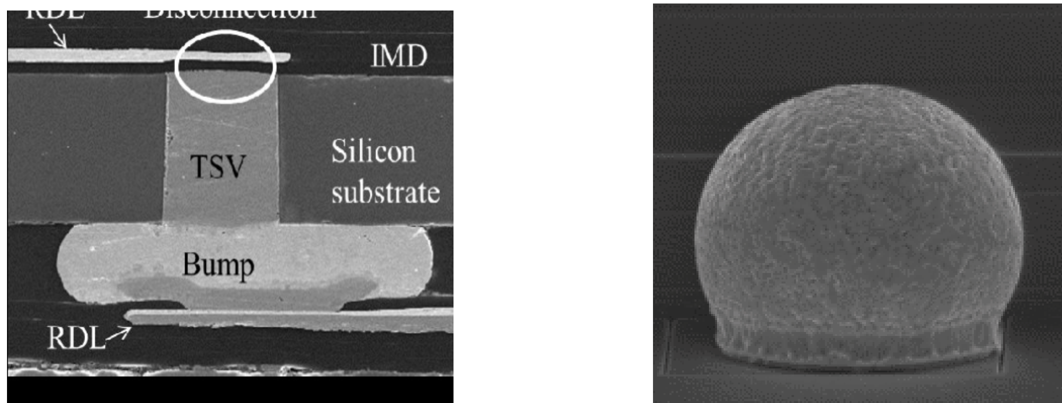


Figure 5.9: Cross-sectional SEM image of TSV bump [89]

A high reliability for this bump interconnection characteristic within TSV based 3D IC is proven [88]. The physical dimensions of the bump are significantly larger than the effective dimensions of the TSV proper, as related in [89]. It was found that the height and diameter of the TSV averaged 63.7 μm and 40 μm, respectively; while the height and diameter of the bump were 22 μm and 150

μm respectively. In addition, the height and diameter of a micro-bump in a 3D power distribution network architecture, as shown in Figure 5.10, were measured in [90] as 14.4 μm and 20 μm respectively, while the height and diameter of the TSV were 50 μm and 10 μm.

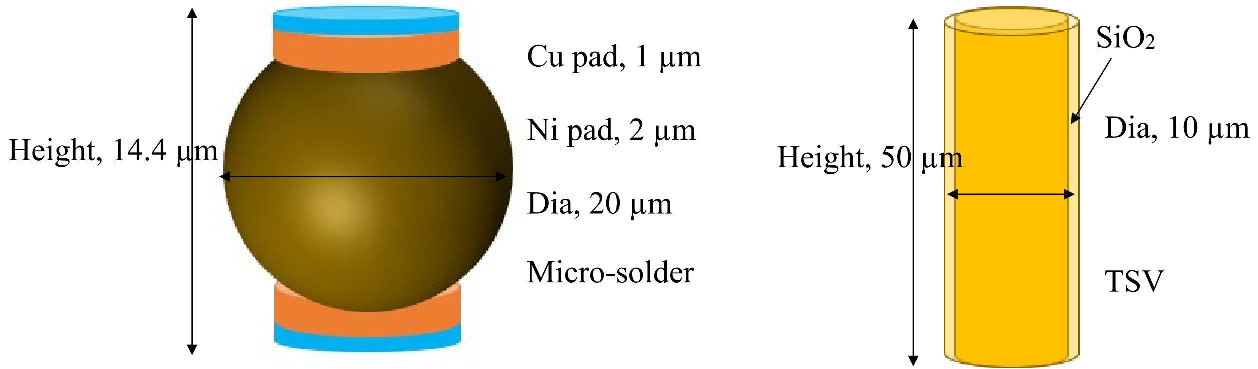


Figure 5.10: Micro-bump and TSV used in 3D power network architecture [90]

Thus, in both cases, the bump area is significant larger than the TSVs' area. Hence, adding an additional crust of oxide around the bump increases its capacitance appreciably; as a consequence the overall TSV capacitance is increased.

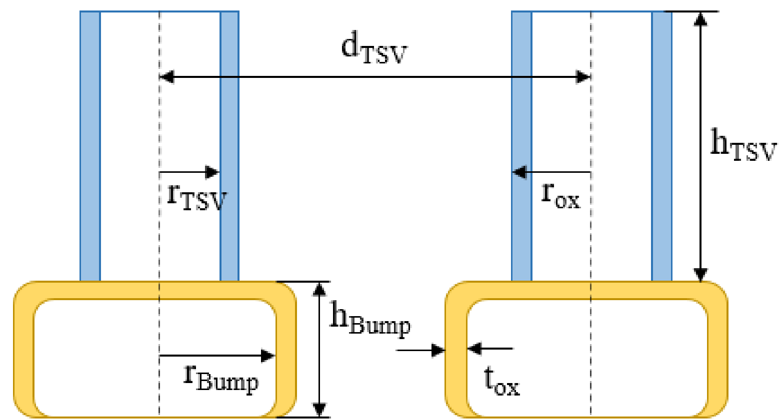


Figure 5.11: Proposed TSV structure with oxides around the bumps

A new TSV structure, which uses the dummy and redundant TSVs as membrane capacitors, is proposed for 3D neuron chips, as depicted within Figure 5.11. In this portrayed structure, isolation

silicon dioxide outside the bump contact area has been introduced; this will contribute an additional parasitic capacitance due to the higher dielectric constant of SiO_2 compared to the small air gap surrounding the bump. This capacitance is formed between the lateral side of the bump and the conductive silicon substrate, and will be accounted and summed toward the determination of the total TSV parasitic capacitances.

When TSV is buried in Si substrate, the TSV capacitance is the capacitance of two wire transmission line with dielectric loss layer and is given by the equation below,

$$C_{TSV} = \frac{\pi \varepsilon_0 \varepsilon_{Si}[1 - j(tan\delta_d + 1/\omega \varepsilon_0 \varepsilon_{Si} \rho_{Si})]}{ln\left[\left(\frac{d_{TSV}}{2r_{0x}}\right) + \sqrt{\left(\frac{d_{TSV}}{2r_{0x}}\right)^2 - 1}\right]} \tag{5.1}$$

where d_{TSV} is the pitch between the TSV and r_{Bump} is the radius of bump.

The per unit length capacitance for an silicon dioxide layer of conventional TSV structure can be found by applying the formula of capacitance for a coaxial transmission line. The cylindrical capacitance with the TSV conductor radius of r_{TSV} and oxide outer radius of r_{ox} is given by equation (3.30).

Similarly, when an oxide layer is introduced to the lateral side of the bump, capacitance is manifest and can be expressed as:

$$C_{Bump_ox} = \frac{\pi \varepsilon_0 \varepsilon_{0x}}{ln\left(\frac{r_{Bump} + t_{ox}}{r_{Bump}}\right)} \tag{5.2}$$

where t_{ox} is the thickness of oxide at bump.

For the estimation of total capacitance of the proposed TSV structure, we need to sum the capacitance of the conventional TSV, the bump, and the capacitance induced by the bump oxide. The proposed TSV capacitance will be,

$$C_{TSV_total} = \frac{(C_{ox} + C_{Bump_ox})C_{TSV}}{C_{ox} + C_{Bump_ox} + C_{TSV}} \quad (5.3)$$

In our proposed methodology, silicon dioxide and air are the dielectric between the bump of the TSV. Hence the total capacitance of the bump can be calculated as

$$C_{Bump_proposed} = C_{Bump_ox} + C_{Bump_air} \quad (5.4)$$

As shown in equation (5.4), our proposed bump structure could significantly increase the bump capacitance; which increases the total TSV capacitance.

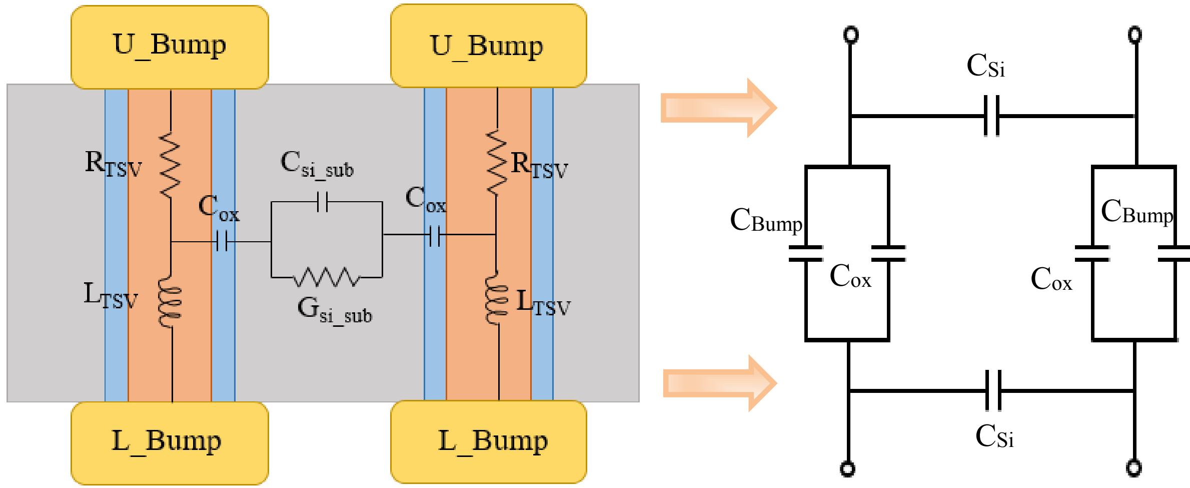


Figure 5.12: Equivalent capacitance model of TSV pair

The equivalent capacitance model of the two TSV structure is presented in Figure 5.12, which shows the additional oxide and depletion capacitances in series with the top and bottom bump capacitance. Also, the TSV-Si substrate-TSV capacitance is presented as parallel plate capacitance. Therefore, the total TSV capacitance is enhanced, which is of course required to maintain the internal membrane voltage.

For this methodology, we only encrusted oxide to the lateral sides of the bump, this encrustation is very negligible compared to the overall dimension of the bump (oxide layer is 0.1 um where bump diameter is 20 um). Our proposition will not require any exotic or esoteric fabrication

process change; and we maintain this oxide bump crust will not have any impact on component reliability.

5.4.2 Reduction of Depletion Region

When the electric potential difference between the metal and semiconductor substrate of the TSV exceeds flat-band voltage, TSVs with typical MOS (metal-oxide-silicon) configurations operate in the depletion region. As this potential difference increases very fast, the generation of minority carriers can no longer keep up with the rate of change of the TSV gate voltage, therefore the depletion capacitance decreases [91]. For the MOS capacitors, different types of oxide charges such as interface-trapped charge, fixed-oxide charge, oxide-trapped charge, and mobile-ionic charge exist in the oxide region (shown in Figure 5.13), which could affect MOS characteristics [92]. By tailoring the thickness of isolation oxide layer, the oxide-trapped charges can be manipulated, and the desired C-V characteristics can be obtained.

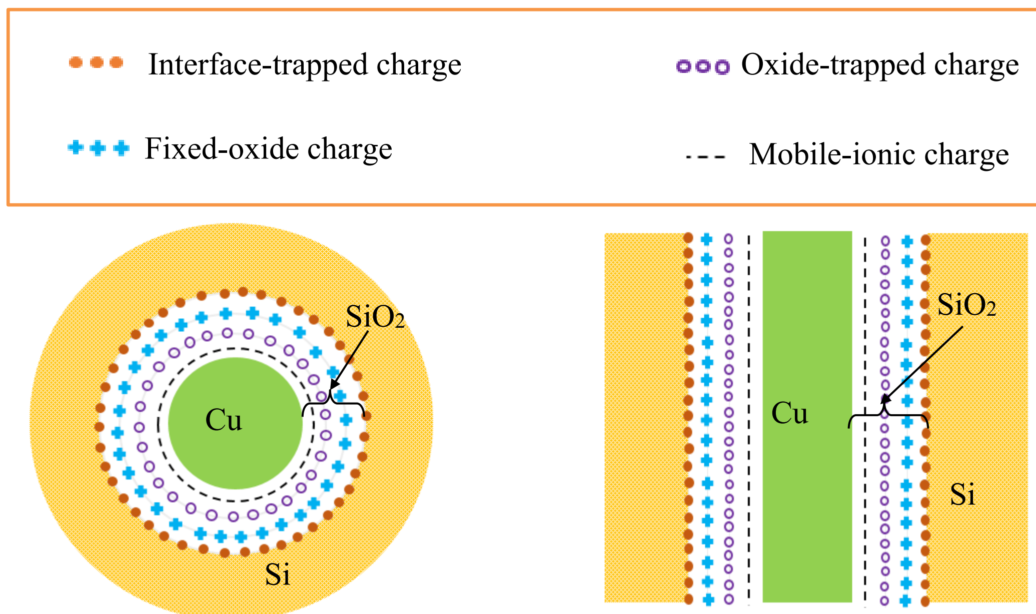


Figure 5.13: Different oxide charges of MOS capacitor in TSV

As shown in Figure 5.13, the fixed oxide charges are located near the interface between silicon dioxide and silicon. The desired minimum depletion of TSV can be obtained by tailoring the isolation oxide charges during the TSV fabrication process. Among these different oxide charges, the fixed oxide charge is chiefly responsible for maintaining the negative interface states which ensures the nature of the depletion region. For a given TSV structure in p-silicon substrate, such as that studied for the work of Figure 5.14, the presence of positive fixed-oxide charges offsets the flat band voltage in negative fashion. If the fixed positive oxide charge is reduced for a p-Si substrate, the TSV C-V characteristics will be shifted right, offering higher TSV capacitance for 3D circuit operation. The value of the fixed oxide charge depends on the ambient temperature of the oxidizing environment, the silicon orientation, the cooling rate from the elevated process temperature, the final ambient environmental component temperature, and the temperature history incurred by subsequent anneal cycles.

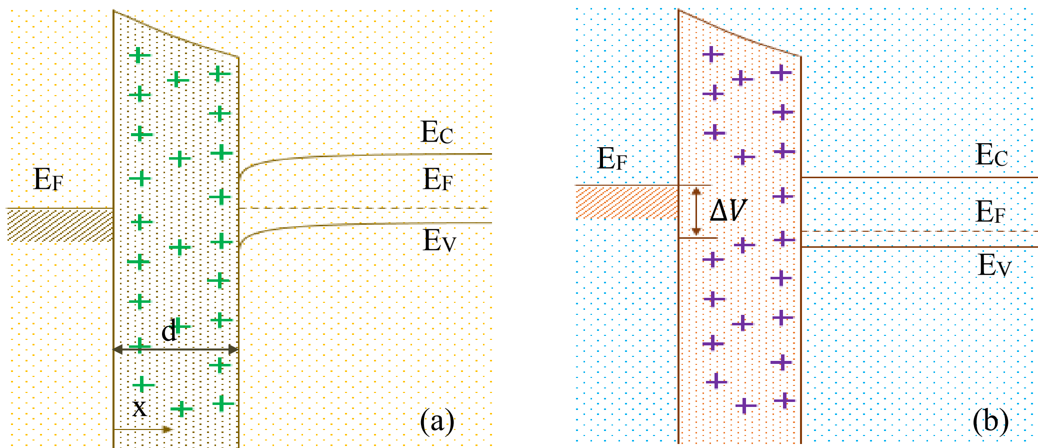


Figure 5.14: Band diagram in TSV (a) Positive oxide charges (b) Flat-band voltage shift

An increase in the atomic concentration of oxygen gives rise to more efficient reaction with less carbon incorporation in films, which in turn leads to lower fixed oxide charges in the film. However, in TSV fabrication process, it is targeted to maintain specific temperature, pressure, and

gas flow rates in a chemical vapor deposition process, in order to obtain minimum fixed oxide charges; thereby achieving minimum depletion region.

The MOS effect in TSVs is modeled by solving Poisons equation without considering mobile charge carriers in the depletion region [26] [93]. Under a condition of applying a bias voltage to the TSV, the Poisson's equation in cylindrical coordinates needs to be solved with appropriate electrical field and surface charge boundary conditions to represent the depletion region [94]. The electrical field, which is continuous at the oxide region, is attenuated to zero at the edge of the depletion region. A voltage is applied to the TSV; the applied voltage and the potential must satisfy equation (5.5)

$$V - V_{FB} = \varphi \tag{5.5}$$

Solving the Poisson’s equation in cylindrical coordinates, the non-linear and time invariant relationship between the applied voltage and depletion width can be obtained as [36],

$$V - V_{FB} = qN_a \left(\frac{W_{dep} t_{ox}}{\varepsilon_{ox}} + \frac{3W_{dep}^2}{4\varepsilon_{Si}} \right) \tag{5.6}$$

where V_{FB} is the flat band voltage, W_{dep} is the depletion region width, and t_{ox} is oxide thickness. For a p-type substrate, the net flat-band voltage due to the voltage shift by oxide charges becomes,

$$V_{FB} = \varphi_{ms} - \Delta V \tag{5.7}$$

where φ_{ms} is the work function difference of metal and semiconductor, and ΔV is flat-band voltage shift which can be found by looking at Figure 5.14.

The fixed oxide charges are independent of bias and can shift along the voltage axis in the C-V characteristic curve. Using Gauss’s law, the flat band voltage shift due to oxide charge is given as [92]

$$\Delta V = -\frac{1}{C_{ox}} \left[\frac{1}{d} \int_0^d x\rho(x)dx \right] \tag{5.8}$$

where $\rho(x)$ is the charge density per unit volume and d is is the thickness of insulator.

This shift in flat band voltage depends on the position of the oxide charge, i.e. the shift magnitude is inversely proportional to the distance of oxide-semiconductor surface. Solving equation (5.8), the voltage shift can be derived as

$$\Delta V_i = -\frac{1}{C_{ox}} Q_i \tag{5.9}$$

Where i indicates either for fixed oxide, mobile ionic, or oxide trapped charge.

The total voltage shift due to all the oxide charges can be found by summation:

$$\Delta V = \Delta V_f + \Delta V_m + \Delta V_{ot} \tag{5.10}$$

Ignoring the work function difference in metal-semiconductor in p-type substrate, the total voltage shift by oxide charges is:

$$\Delta V = -\frac{1}{C_{ox}} \left(Q_f + Q_m + Q_{ot} \right) \tag{5.11}$$

where, Q_f is the fixed oxide charge, Q_m is the mobile ionic charge, and Q_{ot} is the oxide trapped charge.

Substituting these equations, we get the relationship between depletion width and fixed oxide charges as below,

$$Q_f + Q_m + Q_{ot} = C_{ox} \left[\varphi_{ms} - V - qN_a \left(\frac{W_{dep} t_{ox}}{\varepsilon_{ox}} + \frac{3W_{dep}^2}{4\varepsilon_{Si}} \right) \right] \tag{5.12}$$

The flat band voltage V_{FB} is affected by the fixed oxide charges which is already related above. Without taking into consideration this voltage-dependent characteristic, a substantial misestimation can occurs while calculating the total TSV capacitance. The positive fixed-oxide charge is equivalent to the positive gate bias for the TSV substrate. When the bias voltage exceeds the flat-band voltage, the depletion region is formed and it extends according to increasing voltage.

Thus the fixed oxide charge affects the width of the depletion region through its influence upon the offset voltage. The fixed oxide charges can be regarded as a charge "sheet", caused by the non-bridging oxygen close to $Si - SiO_2$interface. Besides impacting the potential in the silicon, the presence of the fixed charge affects the carrier mobility, which ultimately affects the high frequency behavior of the TSV capacitor.

By using the methods mentioned above, the TSV capacitance can be enhanced significantly. This enhancement, heretofore overlooked, is not merely adventitious, but fortuitous. A model which incorporates the membrane capacitance and the membrane voltage into the TSV structure are described in the next section.

5.5 Membrane Voltage Model in Neuromorphic 3D System

VLSI circuits can be exploited to fabricate neuromorphic 3D chips to emulate biophysical processes. But a neural system requires numerous effective channels for excellent communications. And a neural network is a massively reticulated, wire dominant system; inexorably prone to substantial parasitic losses.

The spiking neuron model has become an essential key computational unit for neuronal action potential across the cell membrane. For the integration of electrical inputs of a neuron, it is necessary to estimate the membrane capacitance that determines the neuronal time constant. However, it is challenging to find out a perfect spiking neuron model that is computationally efficient as well as biologically accurate. The most common Hodgkin-Huxley model [95] is a very popular neuron model that is defined by a set of ordinary differential equations. It describes the ionic transportation of a squid neuron through the cell membrane where the parameters are obtained through voltage clamped experiments [54].

Another most commonly used model known as leaky integrate-and-fire (LIF) model [96 – 98] describes the neuron as a passive capacitor connected by a linear leaky resistor. The LIF model is a formal spiking neural model stimulated by external current and is regarded as a valuable tool for analyzing key neuron properties. Using LIF model in a 3D system will change the key features of neurons membrane. Therefore, neuronal membrane voltage will be changed accordingly. From the TSV property serving as membrane capacitor in this work, we modified the LIF model to obtain a membrane voltage model.

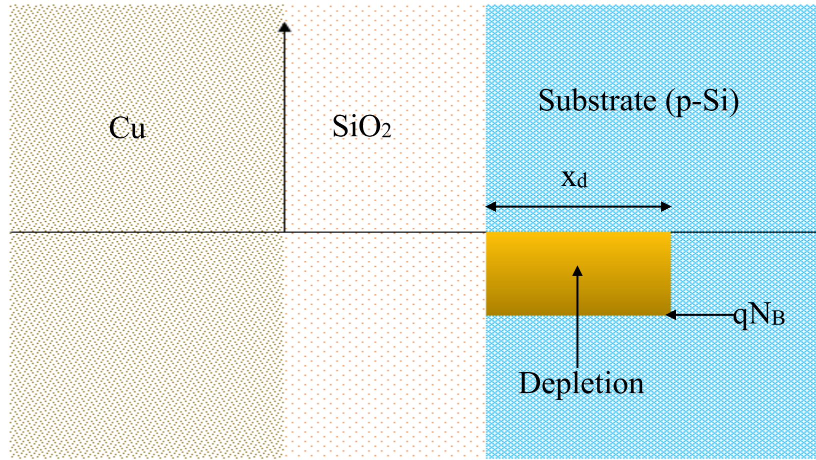


Figure 5.15: Charge distribution for MOS operation in TSV

The membrane voltage model basically describes the electrical activity of neuron corresponding to the ionic charge diffusion through the membrane. For a TSV, the space charge and surface potential of the MIS structure of TSV determine its capacitance-voltage characteristics. The oxide–Si surface potential and total space-charge density are related by Poisson's equation. The space charge is given by,

$$\rho(x) = p(x) - n(x) - n_a \tag{5.13}$$

where $p(x)$ and $n(x)$ are free carrier density and controlled by the intrinsic carrier concentration n_i and the separation between intrinsic and doped fermi levels.

At the insulator-semiconductor surface, the intrinsic voltage is zero and the carrier densities are as follows;

$$p(x=0) = p_0 \; = n_i exp\left(\frac{qV_F}{kT}\right) \tag{5.14}$$

$$n(x=0) = n_0 \; = n_i exp\left(\frac{-qV_F}{kT}\right) \tag{5.15}$$

where V_F is Fermi potential, T is temperature, and k is Boltzmann constant.

The semiconductor surface potential and surface charge can be obtained by solving Poisson's equation,

$$\frac{d^2\psi_p}{dx^2} = -\frac{q}{\varepsilon_{Si}\varepsilon_0}(p(x) - n(x) - n_a) \tag{5.16}$$

where $\psi_p(x)$ is defined as the potential at position x with respect to the potential in the bulk of the semiconductor.

Integrating Poisson's equation from bulk to surface of the semiconductor, gives

$$\int_0^{\frac{d\psi_p}{dx}} \left(\frac{d\psi_p}{dx}\right) d\left(\frac{d\psi_p}{dx}\right) = -\frac{q}{\varepsilon_{Si}\varepsilon_0}\int_0^{\psi_p} \rho(x) \tag{5.17}$$

The surface field and space charge in TSV structure are related by the free carrier condition. It is important to obtain the electric field equation that is required to calculate the total areal charge.

The electric field is defined as,

$$E = -\frac{d\psi_p}{dx} \tag{5.18}$$

By solving the equation (5.17) and simplifying it, the electric field can be obtained as

$$E = \sqrt{2kT\frac{n_i}{\varepsilon_{Si}\varepsilon_0}\left[e^{\frac{-q\psi_p}{kT}} + e^{\frac{q\psi_p}{kT}} - 2\right]} \tag{5.19}$$

The electric field as a function of x can be rewritten as

$$E(x) = \pm\sqrt{2kT\frac{n_i}{\varepsilon_{Si}\varepsilon_0}F\left(\frac{q\psi_p}{kT}\right)} \quad (5.20)$$

where

$$F\left(\frac{q\psi_p}{kT}\right) = \sqrt{\left[e^{\frac{-q\psi_p}{kT}} + e^{\frac{q\psi_p}{kT}} - 2\right]} \quad (5.21)$$

From Gauss's law, the electric field at surface is related to the charge as;

$$Q = -\varepsilon_{Si}\varepsilon_0 E(x) \quad (5.22)$$

Therefore, the total space charge per unit volume is determined as.

$$Q = \mp\sqrt{2\varepsilon_{Si}\varepsilon_0 n_i kT}F\left(\frac{q\psi_p}{kT}\right) \quad (5.23)$$

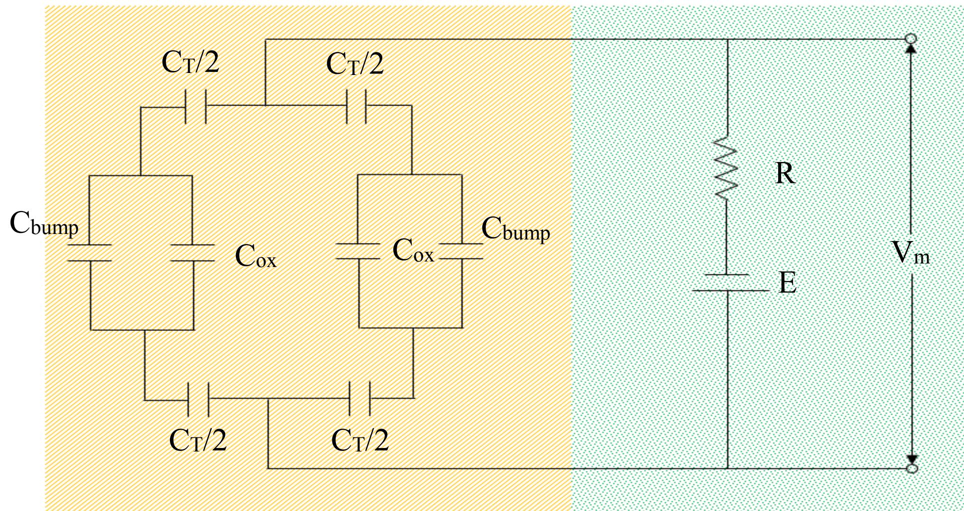


Figure 5.16: Circuit Model of neuron membrane in 3D IC

The current through TSV can be calculated by computing total charge. The total charges in silicon include the charges in accumulation, depletion, and inversion region.

$$Q_s = Q_{acc} + Q_{dep} + Q_{inv} \quad (5.24)$$

Therefore, total charge in TSV is the summation of the charge in silicon, metal, and oxide region given as

$$Q_T = Q_s + Q_M + Q_{ox} \tag{5.25}$$

The circuit model of neuron membrane using TSV is shown in Figure 5.16. The current and voltage through the TSV changes over time as the charges accumulate. The rate of changes of the total charge in a TSV gives the current through it. The current through the TSV capacitor is given as

$$I_c = \frac{dQ_T}{dt}$$

$$= (C_s + C_M + C_{ox})\frac{dV_m}{dt} \tag{5.26}$$

Net current passing through in equilibrium condition can be calculated as

$$(C_s + C_M + C_{ox})\frac{dV_m}{dt} + \frac{V_m - E}{R} = 0 \tag{5.27}$$

This is a first order linear differential equation descripting the voltage change over time. Simplifying this equation with algebraic manipulations, the membrane potential can be calculated. The steady current can be applied to the membrane, which transfer the membrane to a new steady membrane potential. The membrane voltage can be derived as,

$$V_m = V_0 + \sum_{k=0}^{\infty} V_k \left[1 - e^{-\left(\frac{t}{\tau_S + \tau_M + \tau_{ox}}\right)}\right] \tag{5.28}$$

where V_0 is the resting potential.

This voltage describes the leakage term due to the resistor while the integration of conduction current results from the TSV capacitance. The total TSV capacitance is parallel to the leakage resistor as demonstrated in Figure 5.16. When the membrane potential reaches the spiking threshold, it is instantaneously reset to a lower value of the reset potential and the leaky integration process starts with the initial value of the reset potential. The simulation results are described in the next section.

5.6 Results and Analysis

To evaluate the effectiveness of the proposed structure and method, the capacitance, the voltage, and the current in a 3D NM IC are simulated and compared to the ones using the conventional method. To conduct the simulation, a simple LIF neuron model is employed.

5.6.1 TSV Capacitance by Proposed Method

The TSV dimensions and their densities in 3D integrated system are determined by the bonding/stacking methods of the layers. However, the neuromorphic 3D system imposed a hybrid approach with heterogeneous dies/wafers connected with high density TSV interconnects. Therefore, it is very important to study about the different TSV types and their characteristics for the proposed system design.

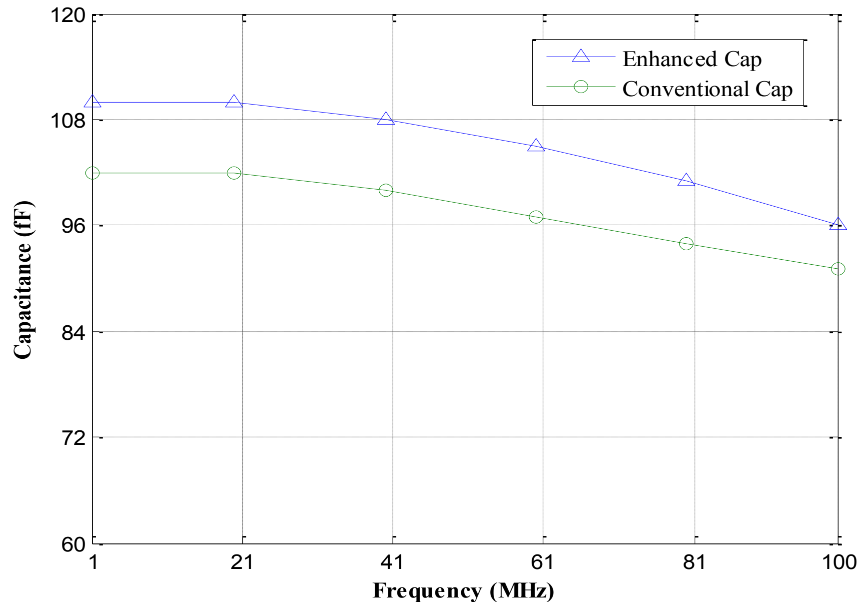


Figure 5.17: TSV capacitance using conventional and proposed method (wafer level TSV)

The membrane capacitance comes from the capacitances of a TSV pair including one signal and one ground using oxide around the bump are plotted in Figures 5.17 – 5.19 for wafer level, chip level, and interposer TSV respectively. The frequency dependent simulation result shows that, the

TSV capacitance is decreasing while frequency is increasing. This is because of the electrical field becoming less confined in *SiO_2* layer and penetrates in Si region.

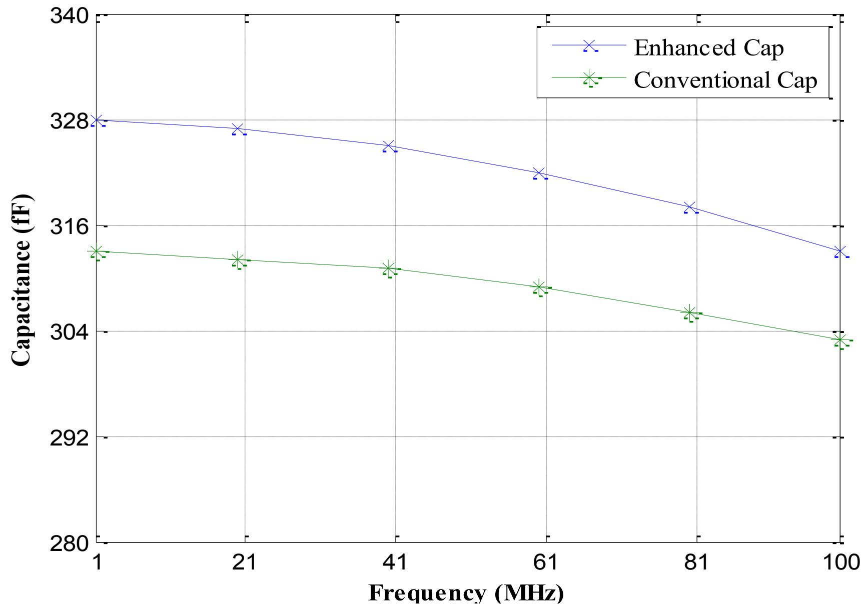


Figure 5.18: TSV capacitance using conventional and proposed method (Chip level TSV)

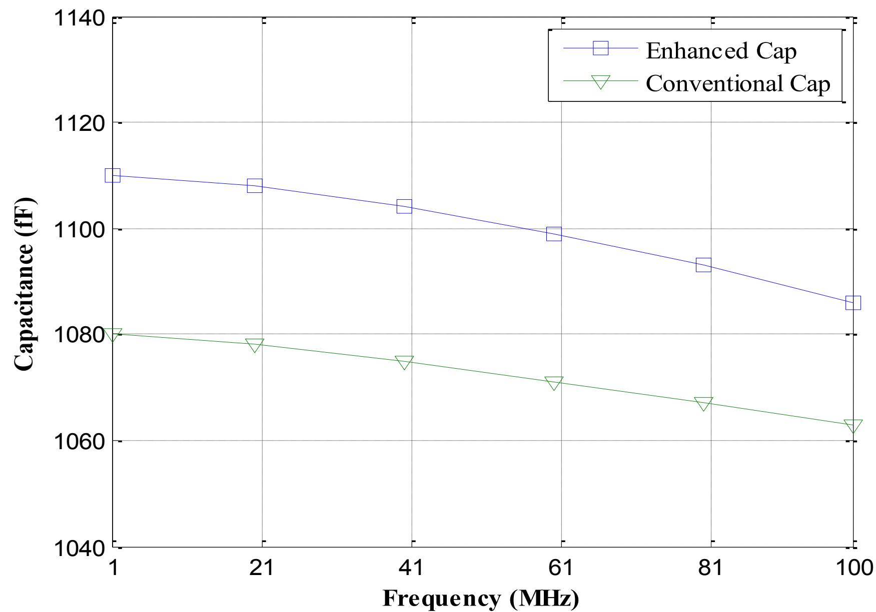


Figure 5.19: TSV capacitance using conventional and proposed method (interposer TSV)

The simulated capacitances using the conventional and the proposed TSV structures show significant differences for all bonding types. The capacitance enhancement of wafer level, chip level, and interposer TSV by addition of bump oxide methodology is increased from ~5% to 8% in the presented simulation result. However, the spiking neuron network consists of neurons with synapse memory and sends the signal in form of spike which are typically produced at lower frequency. For neuron spiking event, the neuromorphic hardware circuit operates in lower MHz range and could communicate and synchronize with the external world in this speed.

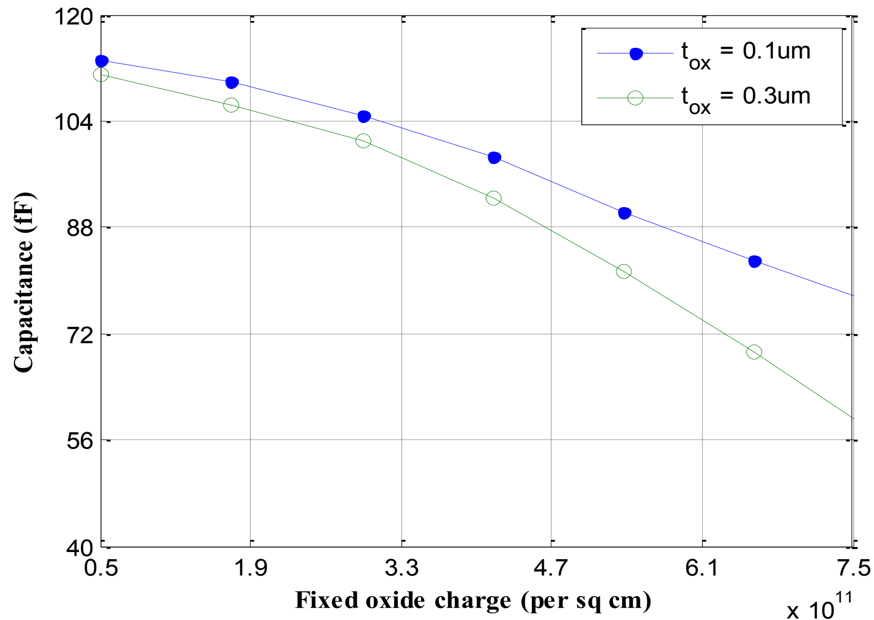


Figure 5.20: TSV capacitance w.r.t to fixed oxide charges for different oxide thickness

To investigate the potency of the fixed oxide charge engineering, the capacitances with two different oxide thickness are simulated and presented in Figure 5.20. It is found that a higher TSV capacitance is obtained for lowing the fixed oxide charge. Besides, it was found that a large amount of positive fixed oxide charges for p-Si substrate maintains enough negative interface states, causes the maximum depletion, and consequently lead to a lower capacitance.

By combining the two proposed methodology (addition of bump oxide and fixed oxide charge engineering) the TSV capacitance can be enhanced up to 30% at lower frequencies. The reconfigured dummy TSV capacitance up to 30% enhancement can fulfill the requirement of the neuronal membrane capacitance in our proposed 3D neuromorphic design. In this case, we assume all dummy TSVs will not be used as membrane capacitance. For the better yield and reliability some of the dummy TSVs may be used as thermal TSV and some other may remain idle for the sudden fault tolerant. Therefore, the obtained enhanced TSV capacitance with redistribution of thermal and other unused TSVs can serve our design purpose and maintains a good design rule for the proposed neuromorphic system.

5.6.2 Validation of the Proposed Method

To validate the accuracy of the proposed analytical capacitance calculation for various capacitances in the equivalent circuit model, the model calculated capacitances are compared to the ANSYS Q3D simulated ones for three different TSV structures considered in this study.

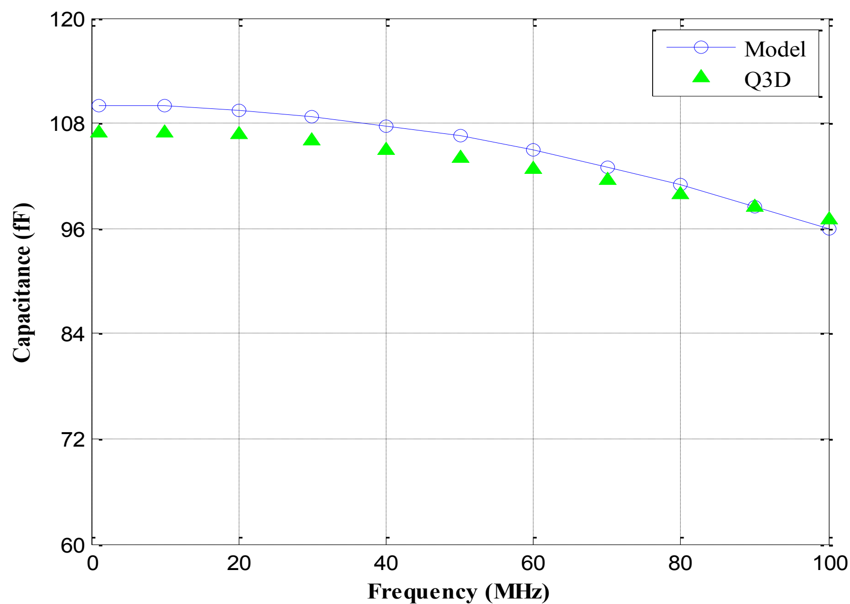


Figure 5.21: TSV capacitance using proposed method and Q3D simulation (wafer level TSV)

ANSYS Q3D is a very famous quasi-static EM field simulation tool used for the extraction of RLGC parameters to be used for electronic design and automation. It uses “finite element methods” and “method of moments” to compute the parasitic matrices and equivalent SPICE sub-circuit model.

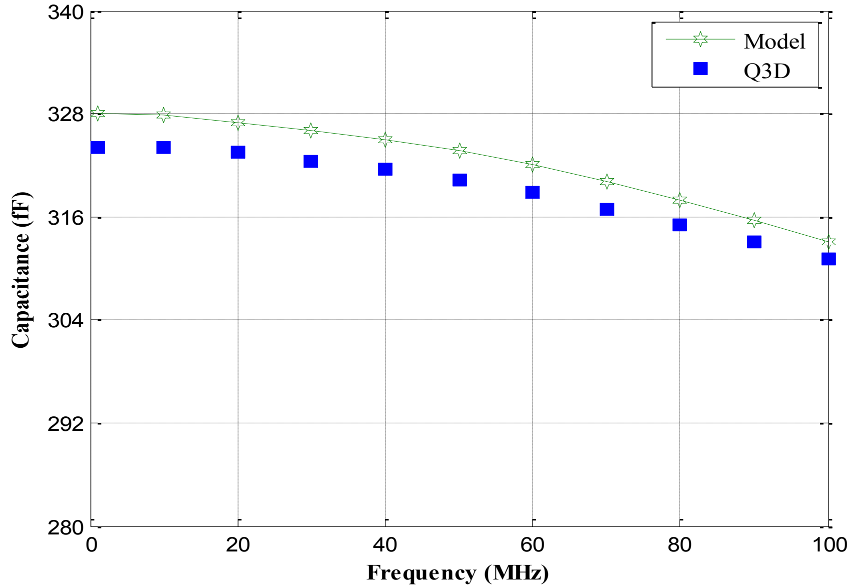


Figure 5.22: TSV capacitance using proposed method and Q3D simulation (chip level TSV)

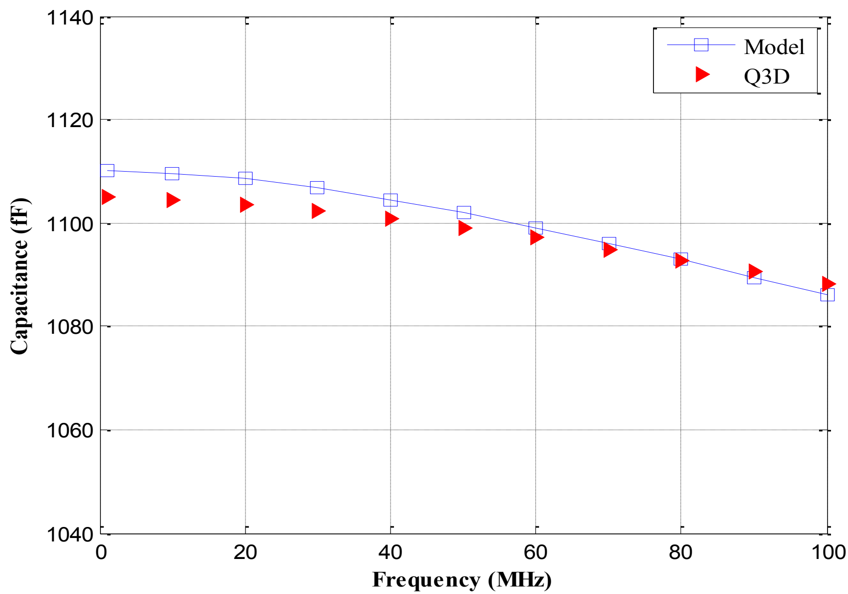


Figure 5.23: TSV capacitance using proposed method and Q3D simulation (Interposer TSV)

These models in Q3D are highly accurate and used as benchmark industry standard tools. The comparison between the proposed capacitance models and Q3D simulation results for wafer level, chip level, and interposer TSV respectively are presented in Figures 5.21 – 5.23. Good correlations between the model and Q3D simulations are observed for all three levels considered in this study.

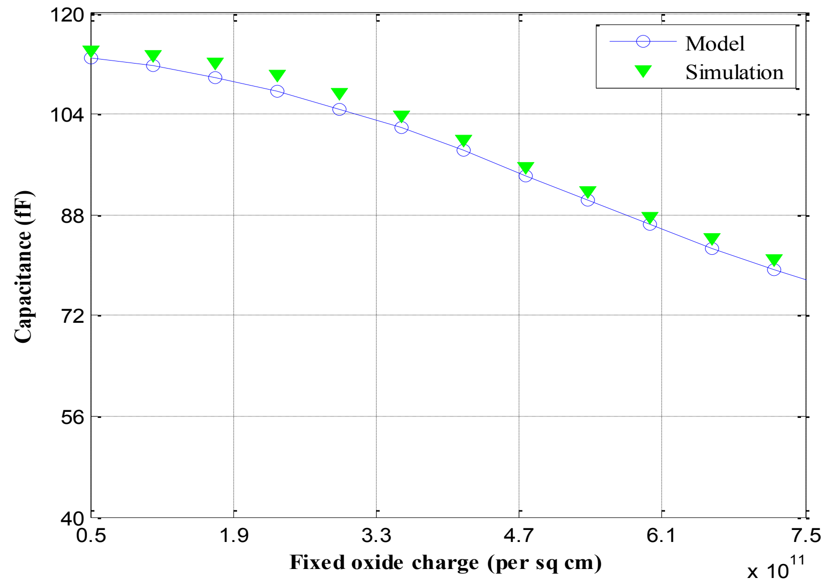


Figure 5.24: TSV capacitance vs fixed oxide charges for proposed model and simulation data by G. Katti

The maximum relative error occurs for wafer level is 2.7%, chip level is 1.2% and interposer TSV is 0.4% respectively. Figure 5.24 demonstrate the comparison between the proposed capacitance model and the obtained SDevice simulation data by G Katti et al [99], which also shows a very good agreement between the modeling and plotted simulation data. Only a deviations as small as 3% between the model and plotted simulation data is observed.

5.6.3 Membrane Voltage and Current

To demonstrate the effectiveness of a neuron, the membrane capacitance implemented by employing TSVs, a 3D model of neuron is constructed and its performance is simulated in SPICE.

The simulation results are compared to the ones using LIF model. The comparisons are illustrated in Figures 5.25 – 5.28. It is clear that the membrane voltage and current of the TSV based neuron proposed in this work are comparable to the LIF model based neuron.

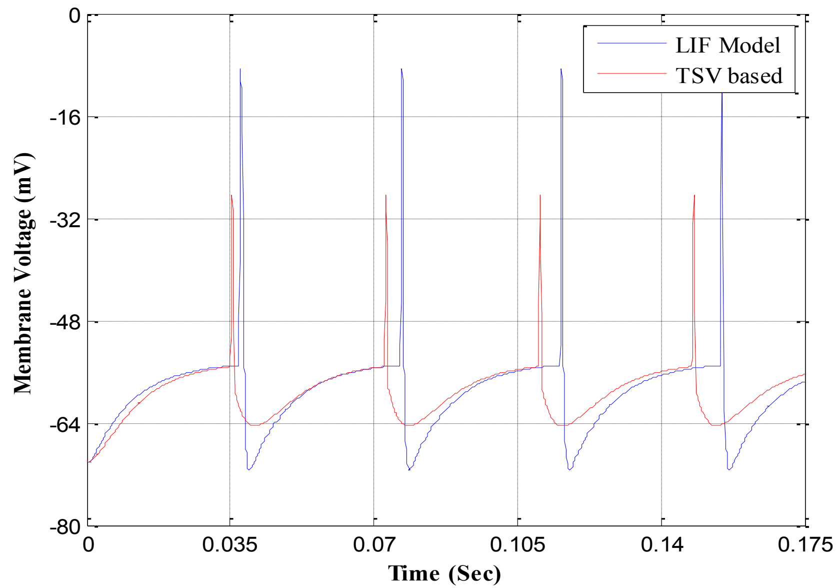


Figure 5.25: Neuronal membrane voltage with LIF model and TSV based model

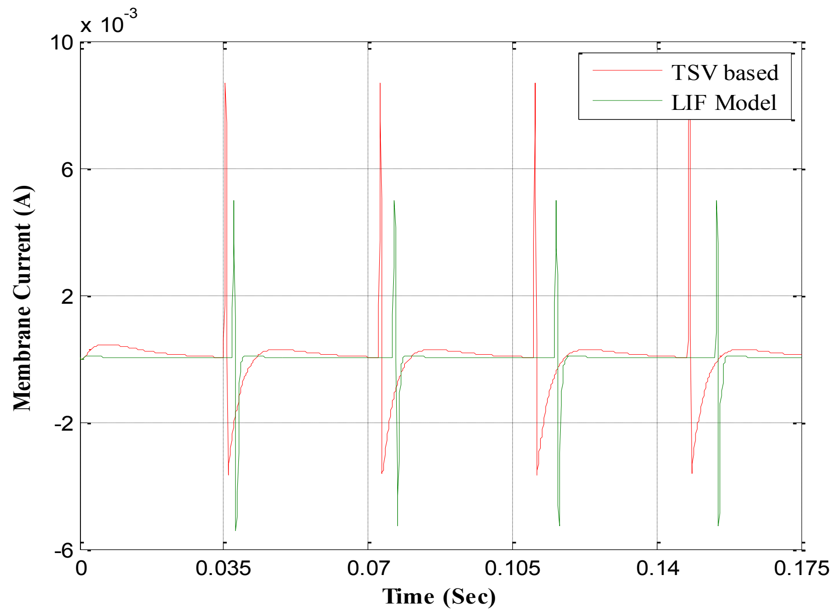


Figure 5.26: Neuronal membrane current with LIF model and TSV based model

It is observed that the spike frequency for both the membrane voltage and current is also increased when the TSV based neuron is used, and which could ensure a higher volume of information. The threshold membrane potentials are the same for both models despite the different in spike length and reset voltage which may potentially result from the difference in their capacitance values. A similar behavior is also observed for the membrane current in both models.

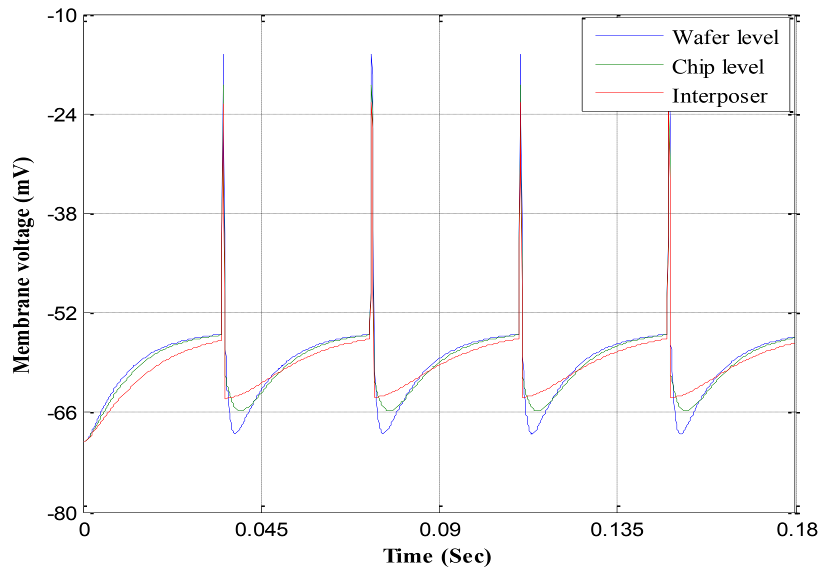


Figure 5.27: Neuronal membrane voltage using wafer level, chip level and interposer TSV

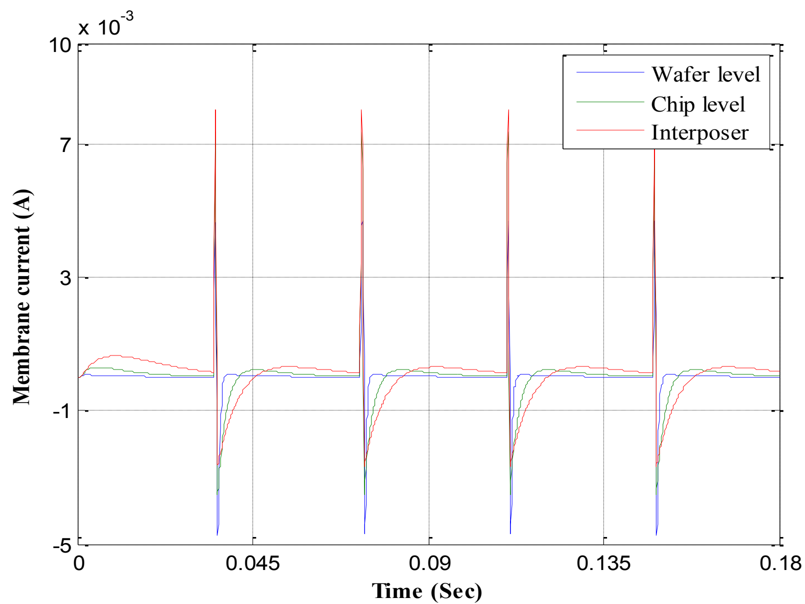


Figure 5.28: Neuronal membrane current using wafer level, chip level and interposer TSV

The membrane voltage and current of the TSV based neuron model for three considered bonding levels are compared and demonstrated in Figure 5.27 and Figure 5.28 respectively. We compared the simulated membrane voltage and current before and after capacitance enhancement of TSV using proposed methodology and presented in Figures 5.29 – 5.30.

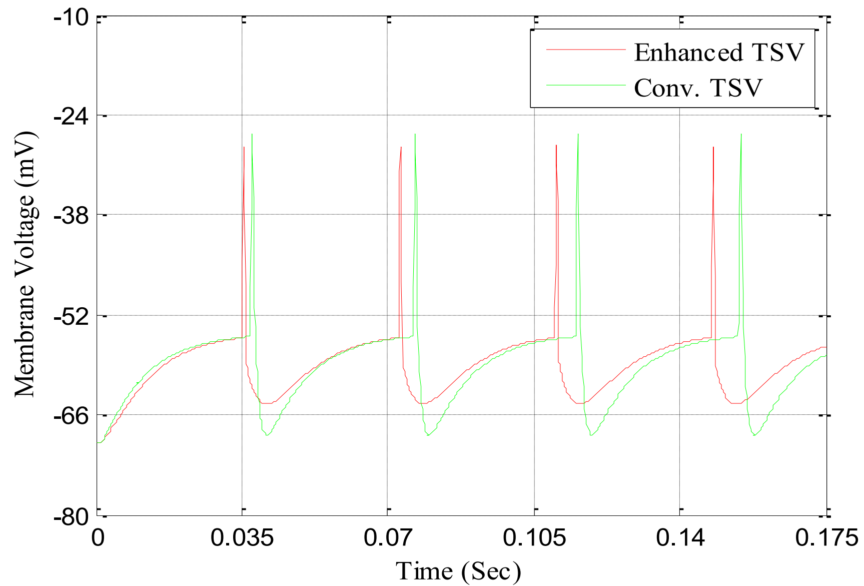


Figure 5.29: Neuronal membrane voltage with conventional and enhanced TSV

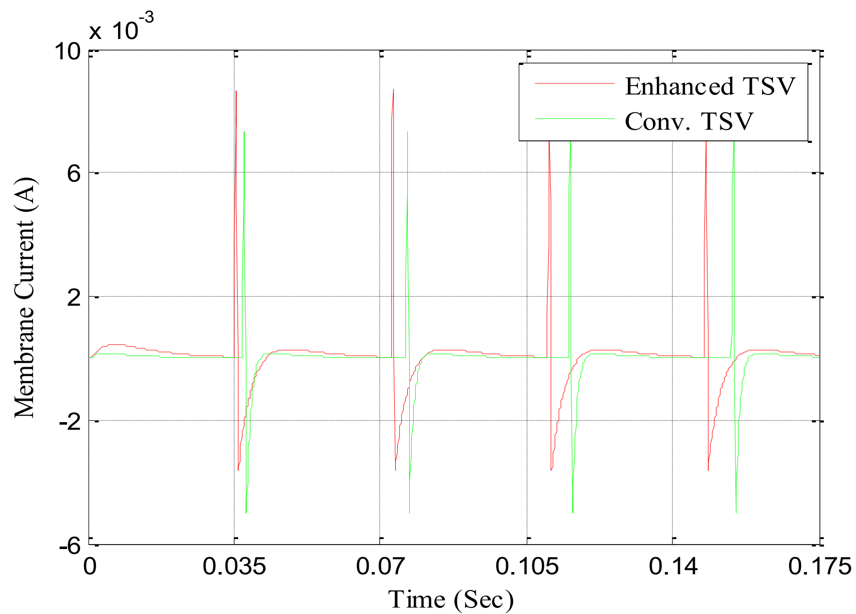


Figure 5.30: Neuronal membrane current with conventional and enhanced TSV

It is found that the spike frequency is also increased here for both the membrane voltage and current when the capacitance enhanced TSV is served as membrane capacitance in the neuron model. The purpose of this study is to gain an insightful information on how a TSV physical structure affects the behavior of the neuron.

5.6.4 Comparison of 2D and 3D Neuron Design

As we mentioned earlier, neural systems require high complexity, connectivity, and massively parallel processing circuital system where 3D circuits could bring lot of benefits. The most sisgnificant benefit of 3D integration in implementation of the proposed neuromorphic circuit enables to supply the TSV property as membrane capacitance. Using this TSV membrane capacitance in the spiking neuron, the proposed neuron circuit enhances the spiking response. In addition with improving the spiking response, our proposed neuron circuit reduces it's area significantly. For our study, we compared a 2D neuron design with its 3D counterpart. The 2D neural encoder (shown in Figs 5.6 – 5.7) is designed and fabricated in our lab which contains total four neurons.

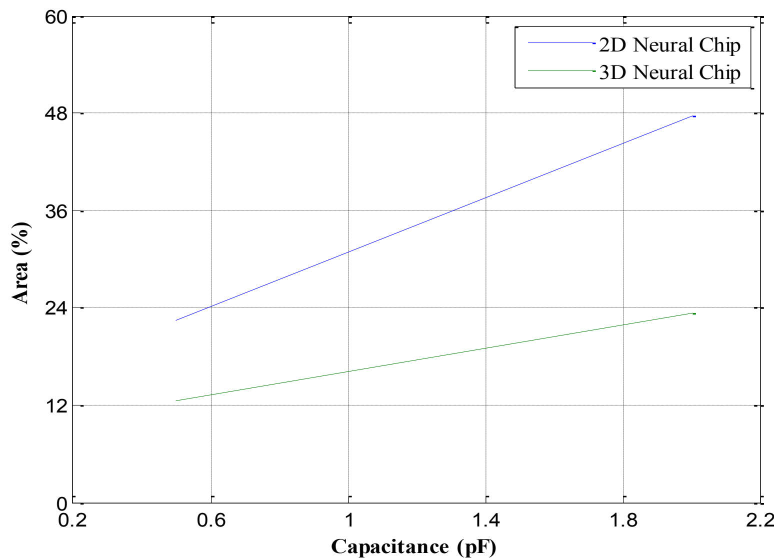


Figure 5.31: Comparison of area occupied by 2D and 3D neuron design

The total occupied area by the fabricated chip is 2.56 mm^2 and its 3D counterpart occupied 1.96 mm^2. It is found that, due to different membrane capacitance, 2D neuron encoder takes more 10% to 23% silicon area comparing to 3D enhanced TSV based design put forward in this work as shown in Figure 5.31.

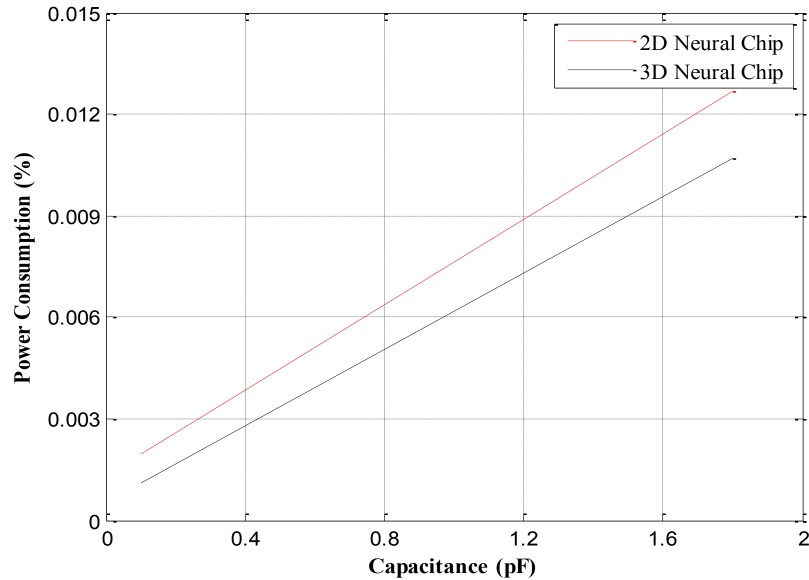


Figure 5.32: Comparison of power consumption by 2D and 3D neuron design

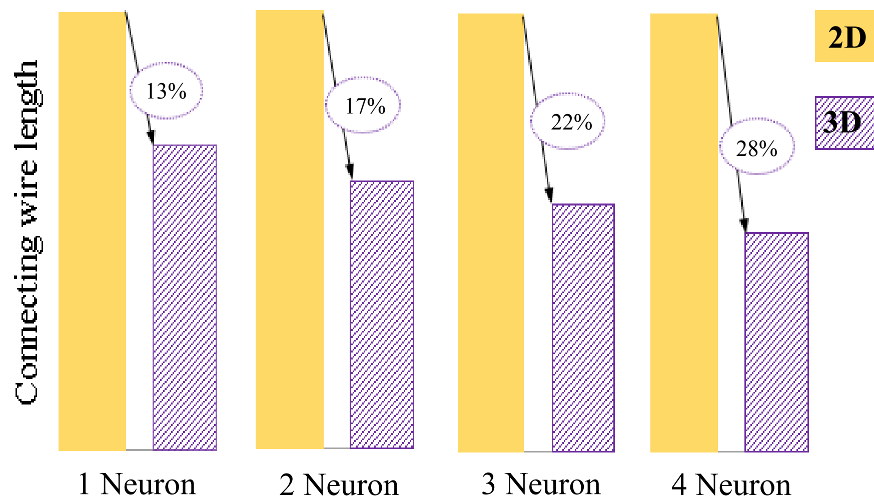


Figure 5.33: Comparison of connecting wire length by 2D and 3D neuron design

Also, the power consumption by the 2D neural encoder is analyzed and compared to the 3D implementation studied. We found that the 2D neural encoder consumes 0.265 mW power for 1950 fF of membrane capacitance where the 3D neural implementation consumes 0.234 mW power for same capacitance. As demonstrated in Figure 5.32, the membrane capacitance in 2D encoder requires 10% more power than the 3D implement does.

Rather than this, we have performed more experiments on 2D and 3D neuron design and compared the connecting wire length used in both design. It has been found from Figure 5.33 that the total connecting wire length can be reduced by 28% for 4 neurons in our designed neural encoder. This is a significant amount of improvement in our proposed design. Therefore, it can be concluded that the proposed 3D neural system not only adapts the idle TSVs as membrane capacitors, but also results in substantial design-area reduction and a significant boost to chip performance and efficiency.

Chapter 6

TSV Array Assignment in Neuromorphic 3D IC

6.1 Introduction

Due to the massive number of TSVs involved to realize huge parallelism, crosstalk is induced in TSV arrays of 3D neural chips and it is one of the biggest reliability issues because of strong coupling network [100 – 102]. Comparing to the magnetic coupling, the electrical coupling is stronger in 3D neuromorphic system attributing to the silicon substrate conductance and the thickness of the dielectric material used in TSV. For pursuing large bandwidth and high density TSV array design, the size of TSV is shrinking down continuously and is approaching nanometer scale [65]. It can causes an increase in crosstalk and limits the performance of the device if the improper physical design and geometric arrangement of TSV arrays are employed.

Having a high degree of integration while maintaining a small form factor imposes significant challenges on TSV array design in a neuromorphic system since the TSV array can take a significant portion of a die area. However, the cost of large area does not necessarily guarantee the performance of a TSV array due to the existence of the crosstalk among signal pairs [103 – 104]. To suppress the crosstalk, more ground pins are generally employed to lower the signal to ground ratio, which consequently increases TSV count drastically and results in a larger die area. To maintain a small factor while not sacrificing the performance of a TSV array, it is highly desirable to be able to identify an optimal TSV array arrangement giving the signal to ground ratio. It is very difficult to employ conventional approach to find out an optimized TSV arrays from a huge amount of redundant arrays for crosstalk reduction. Therefore, it would be helpful to apply an algorithm

that will find the different signal assignment [105], [106]. Fundamentally, this algorithm engaging force directed optimization algorithm is set forth to identify an optimal TSV signal and ground arrangement which results in the least overall electrical coupling among signals to achieve the minimum crosstalk.

In this chapter, using the force directed optimization algorithm, an optimal interconnect array pattern is identified for a proposed structure that could mitigate significant amount of crosstalk. For the analysis of crosstalk, an electrical model of the optimal array structure is proposed and it has been validated by comparing its simulation results with those extracted from commercial tools.

6.2 TSV Array Optimization

To demonstrate the effectiveness of this algorithm, a TSV array of 16 pairs of signal TSVs with 12 ground TSVs is studied as shown in Figure 6.1. Then the extraction of capacitance matrix of each differential signal assignment is performed to find out the maximum mutual capacitance to compare the performance of each pair.

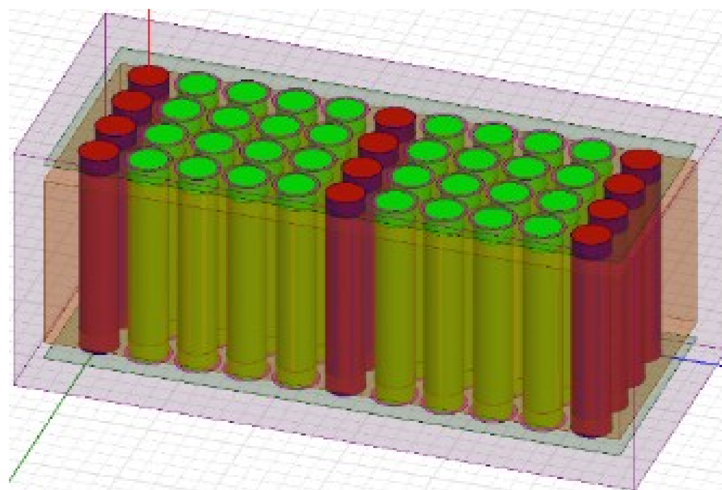


Figure 6.1: Differential signal assignment of non-optimized TSV array

For the optimization of differential signal/ground assignment, all the TSVs need to be taken into account as total points where each points can either be ground or signal TSV. To look for the array structure that would give minimum crosstalk, an algorithm is needed that find all possible pairing combination. In algorithm 1 [106] [107], the pairing of differential signal TSVs were performed by using linear perturbation where pairing of each signal is checked and it is recursively executed for all signals sequentially.

Algorithm 1: Signal pairing by linear perturbation

```
1   A signal sequence Q[1 ….z], the set of possible pairing neighbor A_i for every signal S_i
2   if current_signal_index = = 0 do
3   |    Current_combination ← ∅ ;
4   |    Signal_array ← ∅ ;
5   |    current_signal_index ← 0 ;
6   if current_signal_index = = z then
7   |    Output current_combination;
8   |    Current_signal_index ← current_signal - 1
9   if current_signal_index is not ∈ current_combination then
10  |    forall s_j ∈ A_i do;
11  |    |    current_combination ← current_combination + (current_signal_index, s_j);
12  |    |    signal_array ← signal_array + current_signal_index;
13  |    |    current_signal_index ← current_signal_index + 1
14  |    |    Pairing (current_signal_index);
15  else
16  |    signal_array ← signal_array + current_signal_index;
17  |    current_signal_index ← current_signal_index + 1
18  signal_array ← signal_array - current_signal_index;
19  current_combination ← current_combination – the pair with the current_signal_index
    being it's first element;
20  current_signal_index ← current_signal_index - 1
```

It basically says, for the proper signal conduction, the grounds are distributed nearly uniformly over the whole region of array. Then by applying resisting force and force balancing optimization, the new coordinates of the pins are obtained. Once all the ground vias are distributed uniformly, then the differential vias are taken for execution of available pairing combination. After that, algorithm 2 [106] [107] is applied which found the best optimized signal/ground TSV distribution from all available signal pairing combination.

Algorithm 2: Benchmark differential signal assignment

---

1 Optimize ground distribution by force-directed optimization
2 **for** *all ground distribution* **do**
3 Ground the ground pins;
4 Get all possible signal pair assignments by linear perturbation;
5 **for** *all possible signal pair assignments* **do**
6 Extract a 2N × 2N S-parameter matrix;
7 Transform the S-matrix to a 2N × 2N Y-matrix by shorting one side of all signals to form a current loop;
8 Reduce the size of Y-matrix to N × N by assuming right hand side of all signals ports shorted;
9 Transform the N × N Y-matrix to matrix $C_{SE} = \frac{imag(Y)}{2\pi f}$;
10 Transform the C_{SE} matrix to matrix $C_{diff} = QC_{SE}Q^T$;
11 Compute $C_{i,total}$ of each pair and get C_{max};
12 **return** Optimal ground distribution and signal pairings with lowest C_{max};

Due to the material characteristics, structural formation and frequency of operation, a large capacitive network is formed in neuromorphic hardware system. Therefore, mutual capacitance is

the dominating factor which is mostly responsible for electrical coupling and crosstalk in neural hardware system. In addition to that, neuromorphic system introduces significant amount of parasitic capacitance due to massive parallelism.

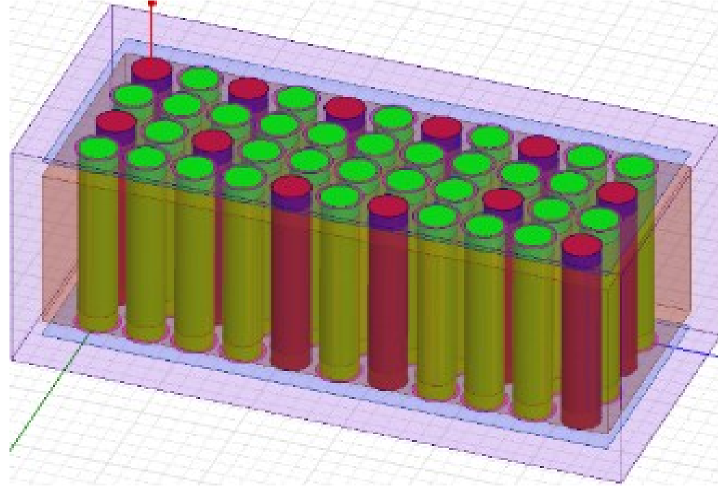


Figure 6.2: Differential signal assignment of optimized TSV

Here, in 32 signal TSVs, there are 16 differential pairs available and S parameter matrix for both port is extracted. This S parameter is transformed to Y parameter and the single ended TSV capacitance matrix can be obtained from the formula below,

$$C_{SE} = \frac{imag(Y)}{2\pi f} \tag{6.1}$$

Now, the differential signal pair assignment from the single ended one can be obtained by the equation,

$$C_{diff} = QC_{SE}Q^T \tag{6.2}$$

where, the Q matrix corresponds to the differential pair by equation (6.2),

$$Q = \begin{bmatrix} 1 & -1 & 0 & 0 & \cdots & 0 & 0 \\ 0 & 0 & 1 & -1 & & 0 & 0 \\ & & \vdots & & \ddots & & \vdots \\ 0 & 0 & 0 & 0 & \cdots & 1 & -1 \end{bmatrix}_{16\times 32} \tag{6.3}$$

Here, +1 and -1 represents the complementary pair of differential TSV. The mutual coupling coefficient for the differential pair i and j can be written as $C_{diff}[i,j]$ and the total coupling is computed by,

$$C_{i,total} = \sum_{j \neq i} \left| C_{diff}[i,j] \right| \tag{6.4}$$

After getting total coupling coefficient, maximum one can be computed as,

$$C_{max} = max\left(C_{i,total}\right) \tag{6.5}$$

The worst victim differential pair is obtained by using the formula (6.5) and the best case different signal assignment is one which has minimum C_{max}.

Using the algorithm, the capacitance matrix for all available pair is calculated and the optimal differential TSV pair is found by lowest C_{max} and this optimized TSV array is shown in Figure 6.2.

6.3 Modeling of Optimal TSV Array

Exploiting the physics of silicon technology using VLSI circuits, neuromorphic 3D chips can be fabricated for the production of biophysical process. Being the wire dominated system, hardware implementation of neural network contains large number of parasitics.

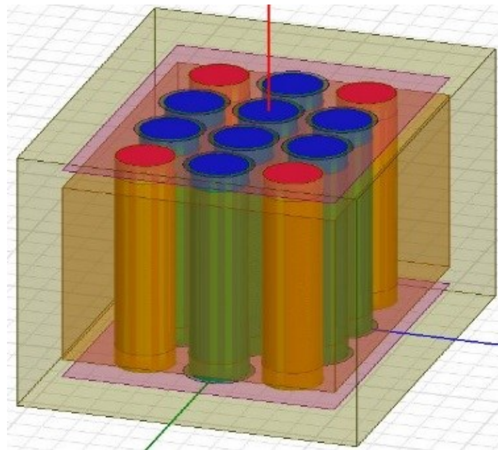


Figure 6.3: Particular portion of optimized differential signal TSV

Also, the neural system maintains numerous effective channels for excellent communication. Therefore, electronic model of 3D neuromorphic system that uses TSV for signal transmission can get benefited from transmission line theory. The transmission line parameters are needed to build the analytical model of the optimized TSV array. For the modeling purpose and simplicity of the circuit, a particular portion of the optimized TSV array has been selected from the large 4×11 optimized TSV array. Figure 6.3 represents the particular section where 4 pairs of differential signal TSVs are surrounded by 4 ground TSVs and it maintains the same differential pair sequences that is found by the optimized structure in Figure 6.2.

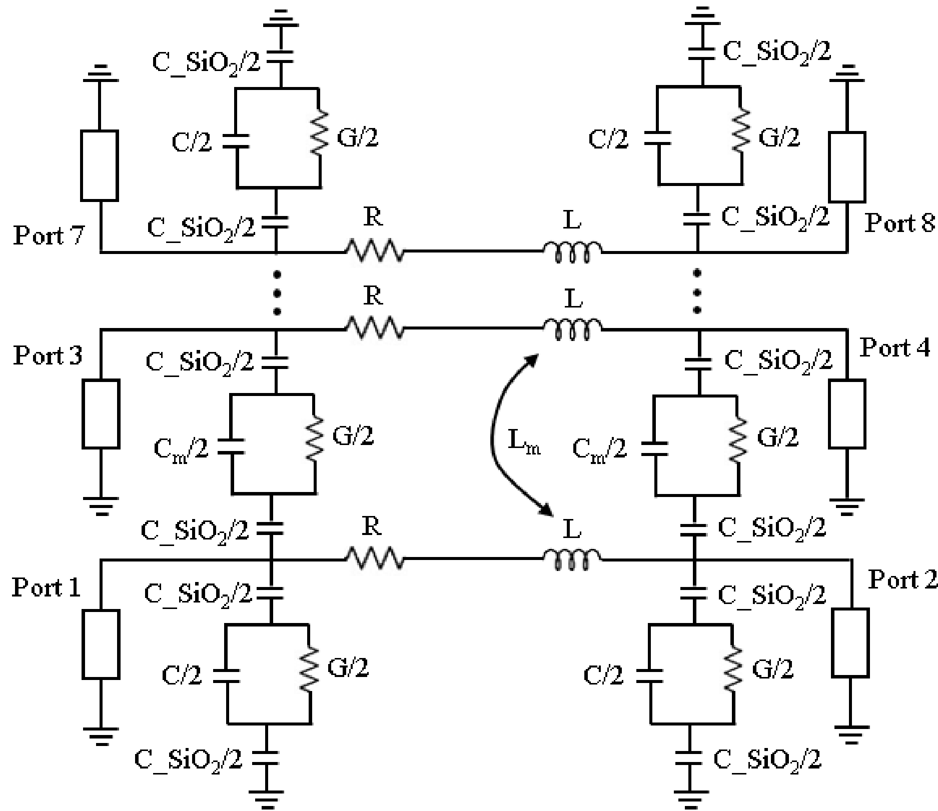


Figure 6.4: Equivalent circuit model of optimized TSV array

From the physical configuration of the differential signal TSV array, the equivalent circuit model in Figure 6.4 is proposed which is composed of different electrical parameters of TSV. The

inductance and resistance of the TSV is characterized by R and L, C_SiO2 represents the capacitance of the dielectric layer between the conductor of TSV and the substrate. The parallel conductance of the silicon substrate is denoted by G and C respectively where G represents the lossy characteristics of the semiconductor substrate.

Each of the port represents the pair of input and output part of the differential signal TSV. Assuming a homogenous medium, the mutual inductance between the two adjacent differential signal pair TSV is calculated by the coupling coefficient k,

$$k = \frac{L_m}{L} \tag{6.6}$$

where, L_m is the mutual inductance and L is the self-inductance of TSV.

The mutual capacitance used for two TSV pair is represented by the equation,

$$C_m = \frac{2\pi\varepsilon_0\varepsilon_r}{ln\left(\frac{d^2}{r^2}\right)} \tag{6.7}$$

where, ε_0 represents the permittivity of the vacuum, ε_r is the relative permittivity of the substrate material, d is the pitch between two TSV, and r is the radius of the TSV.

Using SiO_2 as a dielectric between the TSV conductor and silicon substrate, a capacitance of coaxial form is obtained from equation (3.30).

Two wire transmission line RLGC formulas are applied here for the modeling of our TSV array [2] [23] [47]. All the parameters are expressed in per unit length. The proposed model of optimized differential TSV array includes the parasitic elements that represents loss and coupling.

6.4 Analysis of Results

This section represents the frequency domain and time domain simulation results for analysis of crosstalk of optimized TSV array. The proposed model of the optimized differential signal TSV is

validated by comparing the frequency domain simulation using HFSS. Time domain simulation is being performed to compare the crosstalk of optimized and non-optimized TSV array.

6.4.1 Frequency Domain Analysis

To perform the crosstalk analysis, two adjacent differential signal TSVs are considered in the optimized TSV array. The modeling and simulation results are demonstrated in frequency domain by means of near and far end crosstalk. Due to the coupled electromagnetic field, the strong mutual capacitance is more important of closely spaced TSVs for the selected frequency range of the 3D neuromorphic structure.

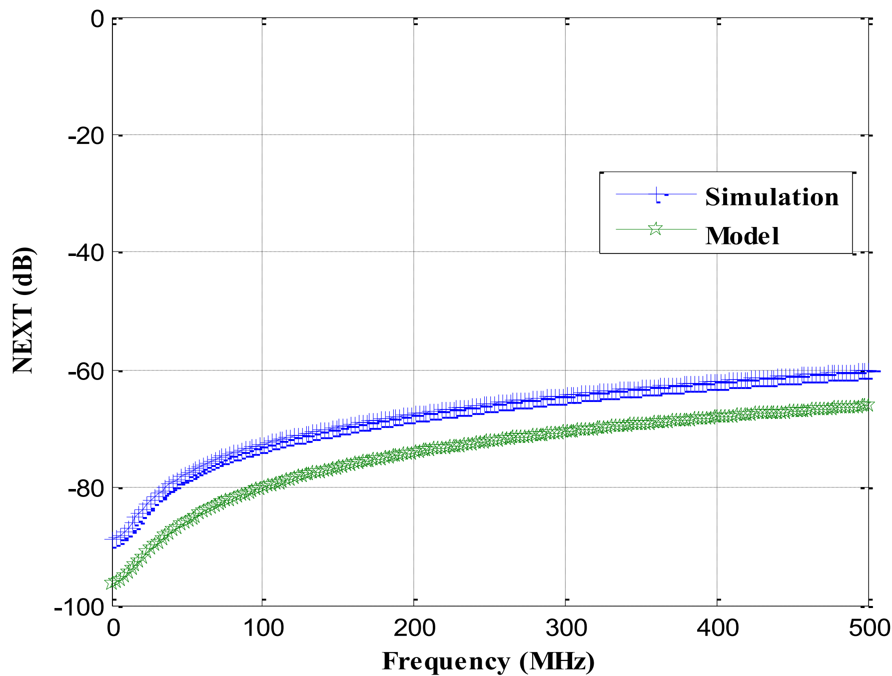


Figure 6.5: Analytical model and simulation of Near-end crosstalk for optimized TSV array

Among different factors for coupling, we have considered the geometric arrangement which one is the most important factor especially for large number of TSVs in neuromorphic chip. Because it produce a larger capacitance and hence an increased capacitive coupling that leads to higher mutual capacitance and coupling noise that results a larger crosstalk. The equidistance signal

ground-signal is considered in both the model and simulation. The magnitude for near end and far end crosstalk are plotted in Figure 6.5 and Figure 6.6 for two adjacent differential signal pairs. It can be seen from these plots that there is a decent correlation and nice agreement between the proposed circuit model and the simulation results.

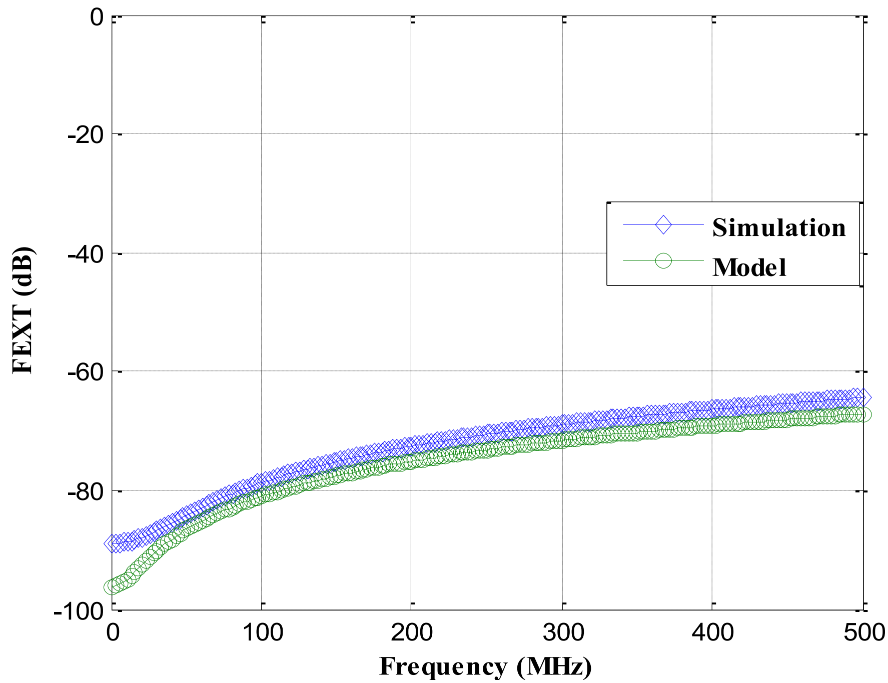


Figure 6.6: Analytical model and simulation of Far-end crosstalk for optimized TSV array

Though there is a little bit difference in the model and simulation results but it's not more than 6% which is quite acceptable. Far end crosstalk is reduced compared to the near end crosstalk because of the capacitive coupling that is constructive at near end and destructive at far end. Far end crosstalk from the circuit model is reduced by 5 dB compared to near end crosstalk and the far end cross crosstalk from simulation is reduced by 2 dB at 500 MHz.

6.4.2 Time Domain Analysis

To compare the performance between the optimized and non-optimized differential signal TSV array obtained through force directed optimization algorithm, a SPICE simulation is being

performed. The transient noise for both the non-optimized and optimized TSV array is plotted in Figure 6.7 and Figure 6.8 respectively from the step response simulation.

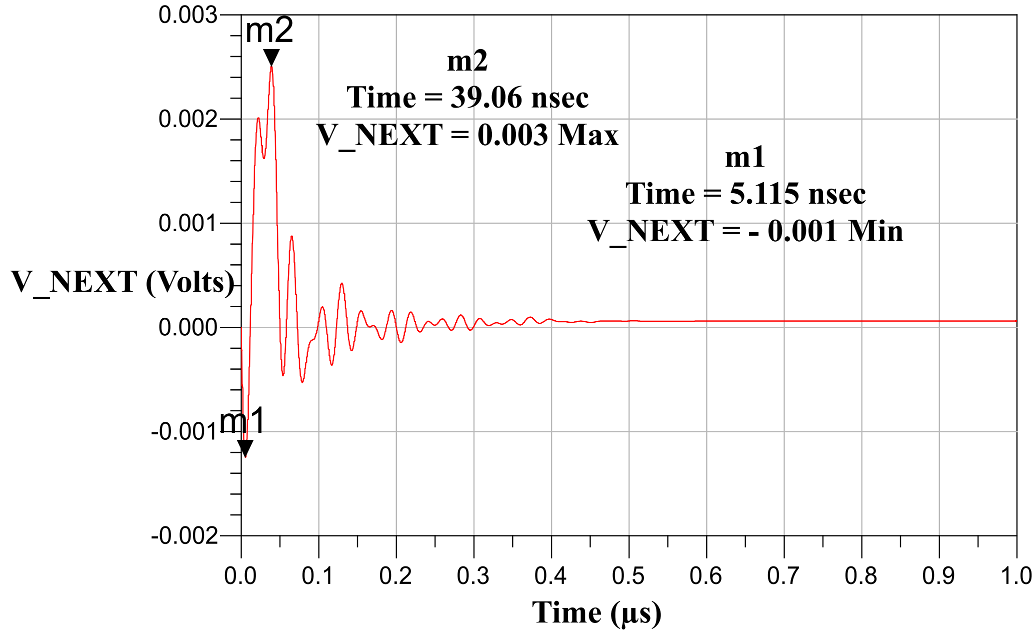


Figure 6.7: Step response simulation in near end crosstalk for non-optimized TSV pattern

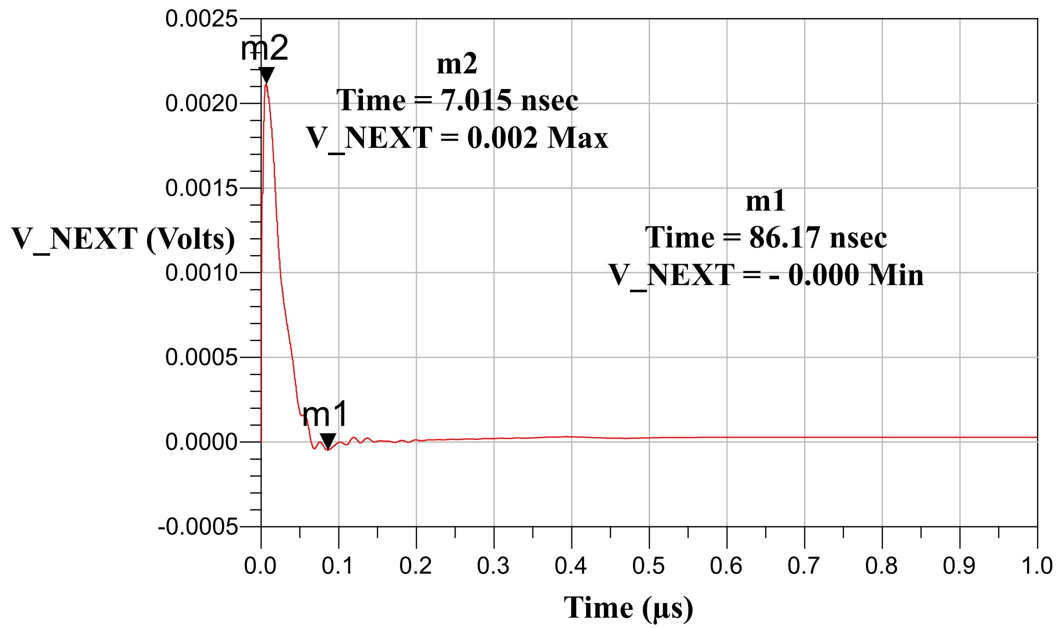


Figure 6.8: Step response simulation in near end crosstalk for optimized TSV pattern

From Figure 6.7, it is visible that the peaks of the transient noise voltages are ~0.003 V max and –0.001 V min, where the peak to peak noise voltage is 4 mV. For the optimized TSV array in Figure 6.8, peak to peak transient voltage is 2 mV. Therefore, it is clear that the optimized TSV array has 2 mV less crosstalk compared to the non-optimized one. In low power application, especially for neuromorphic computing this different is very significant.

Chapter 7

Conclusion

7.1 Summary

Through Silicon Via (TSV) based Three-dimensional (3D) integration technology brings a revolution in semiconductor industry with ultra-miniaturization of electronic system, heterogeneous integration, lower power consumption, bandwidth improvement, and so on. In this dissertation, primarily we aim to model TSVs in 3D IC accurately by considering all the significant factors that appear in mmW frequency. In previous studies of TSV modeling and analysis, all the factors and ultra-high frequency effect have not properly taken into account.

Apart from this, it has been pointed out that the previous research initiates in 3D IC are mostly applicable and limited to conventional memory and processor design/implementation. Over the past few years there has been a significant progress of research in this area. Therefore, beyond this current research trend of 3D integration, we investigate and explore the unique research opportunities of TSV based 3D integration in brain-inspired computing. We proposed novel concept and methodologies by using 3D integration in neuromorphic computing and provide the model and analysis.

In the first phase of this dissertation, we have demonstrated the modeling and analysis of rough surface TSVs in 3D ICs. In this work, we obtained a simple closed-form expressions for the absorption enhancement factor through the application of the second order small perturbation method commonly applied in Quantum physics. We represented the magnetic field in the presence of a roughness conductor surface in its spectral-domain form to mathematically take advantage

offered by the Schrodinger time independent to greatly simplify the derivation. We also proposed an analytical model incorporating the surface roughness, the depletion capacitance, and other effects often neglected in the TSV modeling to analyze the performance of the TSVs. The proposed model is analytically calculated and validated by comparing the S-parameters predicted by both the model and the HFSS simulation up to 100 GHz. The impact of roughness on the TSV in the ultra-broad band range is also investigated. Our investigation revealed that the TSV sidewall roughness not only increases the losses in the mmW frequency range, but also impacts the impedance of the TSVs. This is first time that the impedance alterations induced by surface roughness has been formally explained and discussed. Our study also emphasizes that the effect of TSV sidewall roughness becomes a paramount factor when modeling TSV within the extremely high frequency band.

In the second phase of this dissertation, we explored the necessity of 3D system integration in neuromorphic hardware implementation and proposed a novel TSV based 3D neuromorphic system. Due to process technology constraints, a certain amount of redundant TSVs and dummy TSVs are always required in a 3D integrated system. In this research, we propose to use these redundant and dummy TSVs to supply the neuronal membrane capacitance that maps the membrane electrical activity in a hybrid 3D neuromorphic system. This proposition could also serve the need of neuronal ion transportation dynamics. We also investigate two new methodologies that could significantly enhance the TSV capacitance in a 3D neuromorphic system. We demonstrated that the enhanced TSVs can be used effectively to realize membrane capacitance and the neuron implanted by the proposed technology is comparable to the ones using LIF. We derived analytical equations to calculate the capacitance. The proposed analytical model facilitates the calculation for a very large-scale neuromorphic computing. The analytical equation gives us

the sense of parameters to be tuned to achieve the desired capacitance before we design the physical structure of the TSVs. Having such model with parameters helps us to effectively identify the tuning parameters so we can design the TSV with much short designing time and effort. We also showed that our approach does not require an additional silicon area while boosting chip performance. The proposed techniques were verified through simulations. This increasing capacitance is necessary to maintain the neuronal membrane potential and to perform the key activity in 3D neural systems. The advantage of using the TSVs to mimic membrane capacitance in a 3D neuromorphic chip is demonstrated through comparisons of silicon area, connecting wire length and energy consumption against their 2D counterpart designs.

However, due to the realization of huge parallelism in neuromorphic 3D system, a critical investigation is highly required to obtain minimized crosstalk from the signal/ground TSVs. Therefore, in this dissertation, we have demonstrated an optimal TSV array pattern by applying the force directed optimization algorithm. And when the performance of the optimized TSV array pattern is compared to the non-optimized version, we articulate that the optimized TSV pattern preponderates in signal crosstalk noise suppression.

Finally, it can be concluded that, with the trend of energy efficiency in a modern computing, TSV based 3D neuromorphic chip can realize a higher performance competitive for the next generation potential technology in neuromorphic hardware system.

7.2 Future Work

The future research opportunity in neuromorphic 3D integrated system could follow several directions. One of the interesting directions could be yield and reliability issue, because the complicated process technology and fabrication methodology of TSV based 3D system introduces

significant yield and reliability challenges. The yield in 3D neuromorphic IC depends on die yield, TSV yield, and the bonding yield and these yields are mainly affected by the process variation and changing the physical structure of dies/TSVs. The process variation and optimization are the key issues that causes Cu extrusion and hence the TSV parasitic characteristics are changed. Besides this, misalignment and random open defects can happen in TSV bonding and fabrication process respectively which severely impact the TSV yield. Whereas, the reliability comes from the associated thermal issues and fabrication process.

In addition, due to the massively parallel processing distributed system, the hardware implementation of 3D neuromorphic IC possess an inherent defect and fault tolerance. Defects occur near the border of two adjacent cells will affect the neighboring cells as well as TSVs. Fault might be local or global and might affect a single cell to malfunction or the whole circuit.

To reconfigure some dummy TSVs as neuron capacitance, assign some dummy TSVs as thermal TSV and others remains left for fault tolerant structure will impact the overall yield of the neuromorphic system. Insertion of new spare/ground TSVs and sharing the redundant TSVs across the neighboring die could change the yield in neuromorphic 3D system. By changing the signal to ground ratio or the number of the TSVs or their physical sizes also changes yield. Therefore, it will be very important to study the yield and reliability assessment demonstration in neuromorphic 3D IC.

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