Charge Transport in Field-Effect Transistors based on Layered Materials and their Heterostructures

By

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Abstract

In the quest for energy efficiency and device miniaturization, the research in using atomically thin materials for device applications is gaining momentum. The electronic network in layered materials is different from 3D counterparts. It is due to the interlayer couplings and density of states because of their 2D nature. Therefore, understanding the charge transport in layered materials is fundamental to explore the vast opportunities these ultra-thin materials offer. Hence, the challenges targeted in the thesis are: (1) understanding the charge transport in layered materials based on electronic network of quantum and oxide capacitances, (2) studying thickness dependence, ranging from monolayer to bulk, of full range-characteristics of field-effect transistor (FET) based on layered materials, (3) investigating the total interface trap charges to achieve the ultimate subthreshold slope (*SS*) theoretically possible in FETs, (4) understanding the effect of the channel length on the performance of layered materials, (5) understanding the effect of substrate on performance of the TMDC FETs and studying if the interface of transition metal dichalcogenides (TMDCs)/hexagonal-boron nitride (h-BN) can have less enough trap charges to observe ambipolar behavior, (6) Exploring optoelectronic properties in 2D heterostructures that includes understanding graphene/WS_2 heterostructure and its optoelectronic applications by creating a *p-n* junction at the interface. The quality of materials and the interface are the issues for observing and extracting clean physics out of these layered materials and heterostructures. In this dissertation, we realized the use of quantum capacitance in layered materials, substrate effects and carrier transport in heterostructure.

Acknowledgements

I want to express my deepest appreciation to Prof. Hui Zhao. Under his guidance, I have learnt the philosophy of life, troubleshooting skills and patience in stressful situation. I have learnt various lab techniques, group-work, data-analysis and work ethics. I have done research work with Dr. Hsin-Ying Chiu, who has guided me the philosophy and discipline to run marathon of research work. I learnt in order to finish run, one needs preparation, pace and running extra mile than your comfort zone. I also express my thanks to Prof. Judy Wu. She has been constant help in the research and support to me. I identified by first monolayer graphene by microscope in her lab. My special thanks to Prof. Siyuan Han for his unconditional support. Whether it was quantum mechanics course work, physics questions to any topic in condensed matter or feedback in Applied Physics Seminars, i always have learnt and it has helped me to grow. Even while working and presenting my work now in industry I appreciate his remarks. It has helped me to be objective. Thanks to him. I also would like to express my deep acknowledgements to Prof. Rongqing Hui and Dr. Wai-Lun Chan for their input and support in my research work and feedback.

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Chapter 1

Introduction

Transistors have been shrinking in size exponentially for more than four decades. This phenomenon was predicted in 1965 by Moore's Law.[3] It states that transistor density of integrated circuit should double every 18 months. Recently, there has been extensive development in next-generation metal-oxide-semiconductor field effect transistors (MOSFETs) such as multigate transistors.[4] In the next decade, transistor improvement will encounter serious issues. In the last few years graphene and other two-dimensional materials become one of the most researched topics in physics and material science. The increase in publications per year about two dimensional (2D) materials is outrunning previous alternate materials. These alternate materials include carbon allotropes like fullerenes and nanotubes.[5] This chapter will introduce relevant properties of graphene, hexagonal boron nitride (h-BN), other 2D materials and graphene-based heterostructures.

1.1 Two-Dimensional Materials

Materials behave differently in reduced dimensions when compared with their bulk counterparts. The transition from bulk graphite to 2D-graphene and one-dimensional (1D) carbon nanotube results in the materials with different properties from each other. For example, graphene can be stretched up to 20% without structural damage. Every time we write with a pencil, we transfer

graphite (multilayer graphene) onto paper. The doping can be used to modify 3D crystals. On the other hand, the 2D material band structure can be modified by shear and strain.[6] In late 1930s, researchers began to study the thermal stability of single-atom-thickness sheet. It was shown that, thermal fluctuations should destroy long-range order. It results in melting of a 2D lattice at any finite temperature.[7] Theoretically, it was thought that perfect 2D atomic crystals cannot exist.

1.2 Graphene

Monolayers such as graphene have two surfaces no bulk in between. It presents with the most ultimate case of surface science. Graphene is the most researched material among 2D crystals. It is composed of a single layer of carbon atoms arranged in a two-dimensional honeycomb lattice. A graphene sheet is one million times thinner than a sheet of paper. There is widespread interest in graphene for many reasons that can be summarized in two discrete properties. First, investigation of the fundamental physics of graphene is very simple and clean. Researchers can produce sheets with defect densities as low[8] as 1 in 10^8. In this near defect-free material, many other interesting phenomena can be observed. Electrons and holes are massless relativistic-like particles in graphene. Graphene shows integer and fractional quantum Hall effects in magnetic field.[9]

The second reason for extensive interest in graphene in its potential. It can be utilized in a variety of applications including displays and optoelectronics.[10] It can also be used in computing.[11] It has high mechanical strength, crystal quality and electronic quality. When graphene is sandwitched in h-BN graphene exhibits micrometer-scale ballistic transport, even at room temperature.[12] It is one of the strongest material known[6] and has a zero band gap. It is an excellent candidate for detection technologies because of its two-dimensional nature. For example, it is ideal for gas sensing[13] because its conductivity is highly sensitive to the chemical environment.[14] Furthermore, graphene can act as a heat sink material, since it has good thermal conductivity.[15]

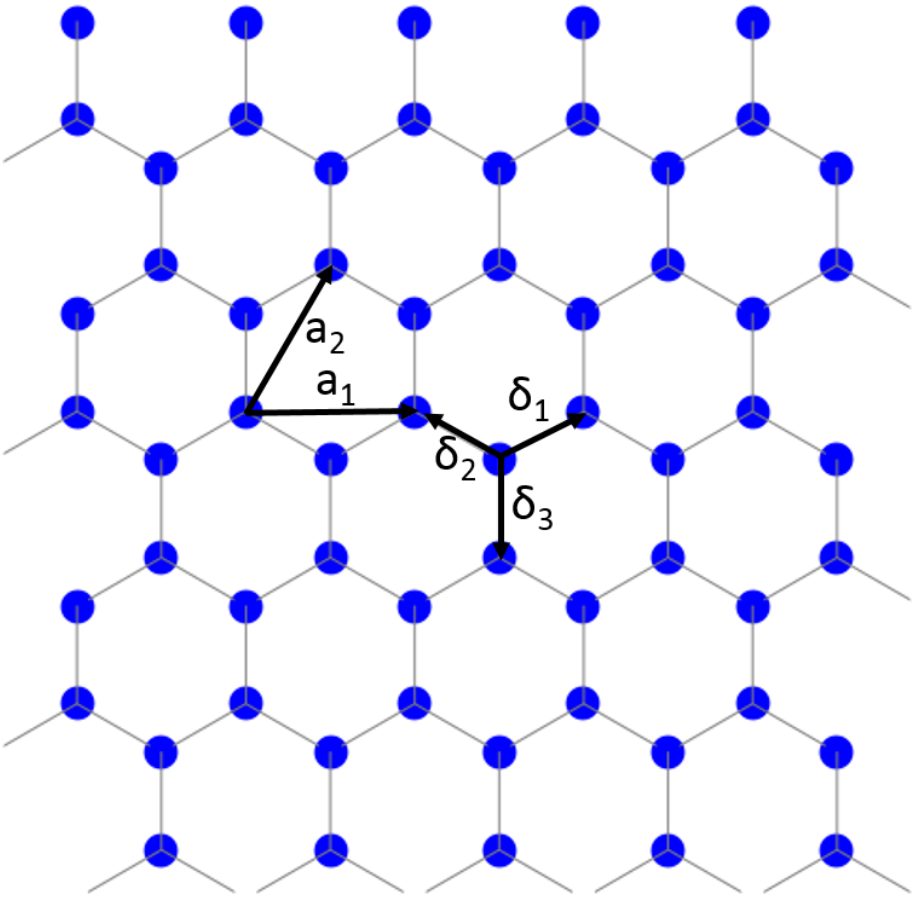

Figure 1.1: Honeycomb lattice of graphene. The vectors δ_1,δ_2 and δ_3 connect *nn* carbon atoms, separated by distance 0.142 nm. The vectors $\boldsymbol{a}_1$ and $\boldsymbol{a}_2$ are basis vectors of triangular Bravais Lattice.

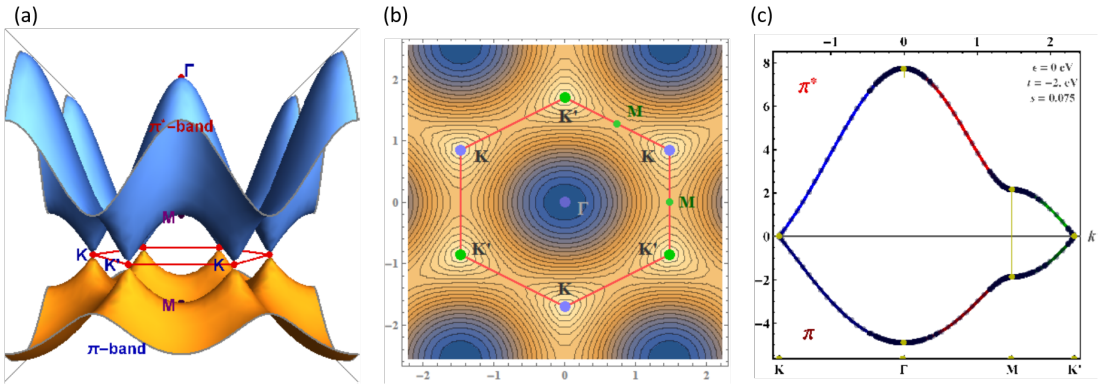

Figure 1.2: Energy dispersion obtained within tight-binding approximation. The Fermi level is situated at the points where the π and π^* touches. (a) Energy dispersion as a function of the wave vector where the vertical axis is energy and horizontal planes are k_x and k_y. (b) Reciprocal lattice of the triangular lattice. Inside region of red-colored hexagon is the first Brillouin zone, with its center Γ and two corners K and K^1. The zone is formed by cutting through the energy dispersion characteristic lines (connecting the points K to Γ to M to K). (c) Band structure of graphene using nearest neighbor and tight binding approximation. The energy is measured in units of t and the wave vectors in the units of $1/a$. Plots made using *Mathematica*.

1.2.1 Crystal Structure of Graphene

The carbon atoms in graphene are sp^2 orbital hybridized. The π electrons in $2p_z$ orbital dominate electronic transport through the lattice. The carbon atoms in graphene are densely packed in a regular hexagonal pattern. The atoms are 1.42 Å apart.

The band structure of graphene can be calculated by tight binding approach. The analytical solution can be approached by assuming that only hopping of electrons between nearest neighbor carbon atoms. There are four valence electrons in carbon with orbitals $2s$, $2p_x$, $2p_y$ and $2p_z$. In the graphene lattice $2s$, $2p_x$ and $2p_y$ hybridize to form single hybrid orbital. Full derivation of tight-binding approximation has been previously published.[16] A lattice is a periodic array of points in real space. A Fourier transformation can give another periodic array of points in reciprocal space. The principle vectors with length a_i in real space as shown in Fig. 1.1. The Brillouin zone is primitive cell in the reciprocal space. The boundaries of this cell are found by the same method as for the Wigner-Seitz cell in the Bravais lattice. The band structure can be defined as the dependence of allowed energies of the electrons in the lattice. It depends on their momentum k in the reciprocal lattice.

To model by a tight-binding model, we can start by assuming only nearest-neighbor hopping. The relevant atomic π orbital as explained above is left unfilled by the bonding electrons. It is oriented normal to the plane of the lattice. The main results of the tight binding calculations are as follows. The energy band is given by,

$$E(\overrightarrow{k}) = \frac{\varepsilon_{2p} \pm t\omega(\overrightarrow{k})}{1 \pm s\omega(\overrightarrow{k})}, \tag{1.1}$$

and

$$\omega(\overrightarrow{k}) = \sqrt{1 + 4\cos\frac{\sqrt{3}k_x a}{2}\cos\frac{k_y a}{2} + 4\cos^2\frac{k_y a}{2}} \tag{1.2}$$

where, k_x and k_y are the x and y components of momentum of the electrons. $\boldsymbol{a}_i$ is the length of the primitive vector vector in real space as shown in Fig. 1.1. The term s is the energy overlap of the wavefunctions of nearest neighbors and t is the energy for an electron to jump between nearest neighbors. The values of s and t used for plotting in Fig. 1.2 are 0.075 and -2 eV, respectively. Energy is measured in units of t and the wave vectors in the units of $1/\boldsymbol{a}$. Using onsite energy ε_{2p} as zero, energy dispersion plot, reciprocal lattice and band structure of graphene at high symmetry point as shown in Fig. 1.2. Around the edge of the first Brillouin zone the bands touch at six points [Fig. 1.2]. Close to these points the bands are linear, giving rise to linear dispersion relation of graphene. The valence and conduction bands touch at K and K'. The direct result of the linear dispersion relation is that the density of states (*DOS*) is linearly dependent on the energy near the Dirac point.

Despite the advantages of high mobility and ultra-thin material, the current ON-OFF ratio of transistors made of graphene is $\approx$ 10-100 at room temperature. This is due to graphene's zero band gap.[17,18] To use a material for digital electronics, a current ON-OFF ratio of greater than 10^4 is required. By confining dimensions of graphene, a current ON-OFF ratio of 10^7 can be achieved in graphene nanoribbons. However, it is at the price of decreases the mobility to 100- 200 cm^2/Vs with a band gap of 150 meV at room temperature.[19] A few of two dimensional materials with large band-gaps are discussed in Sections 1.4 and 1.5.

1.3 Heterostructure

The 2D materials can be stacked together to form heterostructures. To make a heterostructure, take a monolayer (ML) or few-layer (FL) crystal and put it on top of another ML or FL crystal, as required. In these heterostructures, strong covalent bonds provide in-plane stability of 2D crystals. The van der Waals (vdW) forces are sufficient to keep these heterostructures stacked together. The choice of materials ranges from semiconductors, insulators, and metals to build heterostructures with required properties. This makes it possible for researchers to work on 2D materials with diverse electronic properties easily.

The fabrication of heterostructures may require techniques such as molecular beam epitaxy, or chemical vapor deposition. Many techniques are used to create clean and abrupt interfaces. However, these processes takes time and chemistry to create clean heterostructure. There is another easy way of working fundamentally on these heterostructures and also maintains good quality. The 2D vdW heterostructures here do not require the lattice-match condition, unlike heterostructures grown epitaxially. It is because of the weak interlayer bonding in 2D vdW heterostructures.[20,21,22] These structures play a important role in modern semiconductor technologies. At the interfaces of different 2D layered materials, the band offset provides an effective way for the manipulation of carriers. It leads to revolutionary devices such as optoelectronics (discussed in Chapter 6) and tunneling field effect transistors.[23,24,25] It is also used in double-heterostructure semiconductor lasers at room temperature.[26]

The vdW heterostructures on flexible substrates may be useful for applications in future electronic and optoelectronic devices. At present, the main factor limiting the technological development of such heterostructures is the lack of scalable synthesis strategies. Nevertheless, it is encouraging that large-scale techniques for the growth of simple vdW heterostructures and for the mechanical transfer of 2D layers have been shown. It suggests that this difficulty might eventually be overcome. Indeed, we recently fabricated and investigated such a vdW heterostructure (in Chapters 4 and 6). Any new composite materials can be achieved by arranging 2D stacks on each other, because of simplicity of procedure to transfer one material on top of other.[27]

1.4 Transition Metal Dichalcogenides

Among alternative semiconductors for transistors, transition metal dichalcogenides (TMDCs),[28,29] black phosphorus[30] and silicene[31] are becoming center of attraction to physicists. Layered TMDC materials have been known and studied for decades. Their properties as atomically thin, 2D forms are a relatively new and exciting area for nanotechnology. They have many promising applications in nanoelectronics and optoelectronics. Atomically thin films of one of most well-studied families of van der Waals solids is the layered TMDCs, after recent advances in exfoliation and synthesis techniques.

Semiconducting TMDCs (general formula MX_2; M = Mo or W and X = S, Se or Te) in particular are promising candidates. These 2D layered structures have sizable band gaps. It changes from indirect band gaps in multilayer crystals to direct band gaps in monolayers. The large band gaps seen in several members of the TMDC family make them attractive channel materials in logic transistors. The direct band gaps in several single-layer TMDCs open up many opportunities in optoelectronics.

Semiconducting TMDCs generally possess a sandwich type structure in which a layer of metal M atoms is located in between two layers of chalcogen X atoms. Atoms within these three layers are bonded covalently. The individual sheets are bound by van der Waals interactions. This unique crystal structure promotes chemical stability. The absence of out-of-plane dangling bonds, minimizes the interlayer trap density. Use of TMDCs allows steep subthreshold swing (*SS*) (shown in Chapter 3). Semiconducting TMDCs permits assembly of vdW heterostructures.[32] In the transistor industry, devices with steep *SS* are desirable. They consume less power. They have reduced leakage current. Power dissipation is a big difficulty to increased integrated circuit density. Two-dimensional MoS_2 and WS_2 have been used in transistors with high current ON-OFF ratios and integrated circuits with logic operation. They are also used in chemical and gas sensors.[33,34,13]

Ideally, TMDC-based FETs can operate in both the electron- and hole-accumulation modes. It depends on the polarity of the gate voltage. They survive bending because of their flexibility.[35,36] Overall they may have an advantage over silicon in the applications requiring flexible electronics

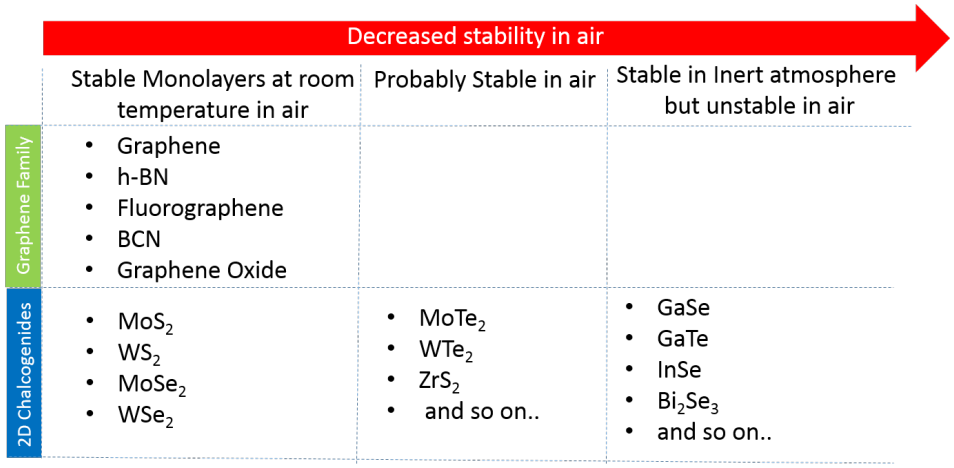

Figure 1.3: Comparison of stability in air of materials belonging to graphene and 2D chalcogenide families.

and optoelectronics.

The 2D TMDCs have many distinctive properties that are not seen in other material systems. In studying the science of 2D TMDCs, researchers are able to utilize the previous understanding on the bulk TMDCs material processing and characterization. Historically, techniques for device fabrication and nanoscale characterization were developed with carbon nanotubes and graphene. This dissertation will describe heterostructure carrier transport properties of TMDC materials like WS_2 and heterostructures. We explored full-range electrical characteristics[37,38,39] of these 2D materials for the first time in our studies. Quantum capacitance models fitted well to our WS_2/SiO_2 devices and similar carrier density values were further confirmed by WS_2/h-BN/SiO_2 devices. h-BN is described in detail in Section 1.5. Further, low-defect devices and heterostructures were achieved on back-gated SiO_2 and are presented in this dissertation (in Chapters 3 and 4).

1.5 Hexagonal Boron Nitride

Two-dimensional h-BN is composed of a honeycomb lattice. It has strong ionic bond of boron and nitrogen with band gap of approximately 5.9 eV.[40] h-BN mono- and multilayers can be exfoliated by mechanical exfoliation. The use of h-BN as an alternative gate dielectric compared to SiO_2 is practical. It is because the dielectric constant of h-BN is $\varepsilon \approx$ 3-4 and breakdown field is about 0.7

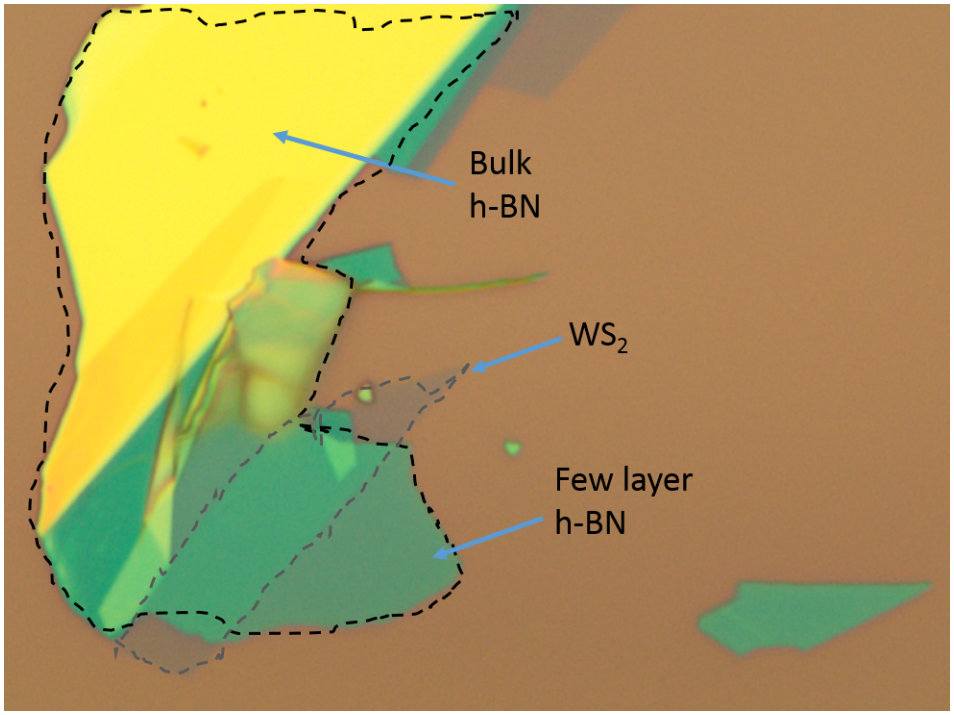

Figure 1.4: Optical image of Few layer WS_2/h-BN heterostructure on 300-nm SiO_2. Bulk h-BN is also shown in the picture as marked. The effect of improved properties of such heterostructure is shown in chapter 5 of this dissertation.

V/nm. These are similar to SiO_2 dielectric constant ε about 3.9 and breakdown field.[41]

Using SiO_2 as gate dielectric, the graphene carrier mobility is limited by scattering from charged surface states and impurities due to SiO_2 substrate surface roughness,[42,43,44] charged surface states, impurities,[45,16,46] and SiO_2 surface optical phonons.[47] On the other hand, hexagonal boron nitride (h-BN) has an atomically smooth surface. It is relatively free of dangling bonds and trap charges; hence it can act as appealing substrate for graphene.[48]

h-BN is an exceptional substrate for graphene. It increases graphene's electronic quality ten-fold.[49] h-BN based graphene devices have improved high electric field performance of h-BN based graphene devices compared to those using graphene/SiO_2. The surface optical phonon modes of h-BN have energies two times to similar modes in SiO_2.[48] Also, the atomically planar surface would suppress rippling in graphene. h-BN has been shown to mechanically conform to corrugated substrates.[42,50] Fig. 1.4 shows the optical image of few layer WS_2/h-BN heterostructure on 300-nm SiO_2. Bulk h-BN is also shown in the picture as marked. We observed improved electrical

properties with WS_2/h-BN heterostructure as shown in Chapter 4 of this dissertation. h-BN has been shown to mechanically conform to corrugated substrates.[42,50] We observed low interface trap charges and higher current ON-OFF ratio in WS_2/h-BN devices compared to control experiment of WS_2 only. Fig. 1.4 shows optical image of h-BN and WS_2/h-BN heterostructure on 300-nm SiO_2.

1.6 Conclusion

This chapter introduced to 2D materials. Further, it showed one demonstration of the variety of physics that can be explored using heterostructures. In the remainder of this dissertation, we describe investigations into whether heterostructure fabricated by a wet transfer process, retains the basic functionality of the original 2D materials from which they were made. We wished to confirm wet transfer heterostructures functionality before applying the process to other heterostructures. The results described herein will open up possibilities for new type of devices other than MOSFETs. To prove that the basic material electronic transport of constituent layers is still valid after wet process, we fabricated heterostructure and measured graphene I-V characteristics. As described in Section 1.2, our heterostructure retained characteristics of graphene and supports the feasibility and efficacy of the wet transfer technique.

There is a vast potential of the proposed interface engineering. We can modify the physical and chemical properties of TMDCs and other 2D materials. However, the physics of these heterostructures is different than conventional MOSFETs. A detailed knowledge of the electronic properties of the interface between TMDCs and metal electrodes is lacking. It is essential in order to implement TMDCs in efficient device applications. Indeed, interfaces play a key role in the performance of a device constructed from low-dimensional materials because the injection, collection, concentration, and mobility of the charge carriers are mainly determined by the interfaces.[32] Our studies will help in furthering understanding of these materials and devices.

Chapter 2

Fabrication and Characterization of Layered Semiconducting Materials

2.1 Overview

The two dimensional (2D) materials are crystalline materials consisting of a single layers of atoms. These 2D materials characterized by strong covalently bonded planar geometry. Relatively weak van-der-Waals (vdW) forces enforce stacking of individual 2D sheets. There are many available bottom-up synthesis and top-down methods available to create 2D materials. Each has their own merits. For example, chemical vapor deposition can grow 2D materials as thin as monolayers using large scale industrial device fabrication devices. However, the quality of crystal made by exfoliation is generally superior. This chapter discusses 2D material preparation methods like mechanical exfoliation with scotch tape (Section 2.2.1) and chemical vapor deposition (Section 2.2.2). Methods to find the number of layers easily in these materials is important. The physics behind layer countings is discussed in Section 2.3.1, where the contrast obtained by an optical interferometer at different interfaces is also discussed. Transfer processes (Section 2.4), material characterization (Section 2.5) and contact resistance (Section 2.8) measurements are explained in this chapter.

2.2 Material Preparation

The following two sections explore two methods, mechanical exfoliation and chemical vapor deposition to achieve 2D materials.

2.2.1 Mechanical Exfoliation

In general, 2D materials are not found in nature because of their instability. Some 3D materials found in nature, such as graphite, are composed of many stacked layers of 2D planar material. The purpose of exfoliation is to peel flakes of 2D materials as thin as one atom from bulk crystal. The bonding forces between planes of layered materials are much weaker than the bonding between the atoms within the planes. Because of this, we can exfoliate them with adhesive tape. In this method, tape is pressed against a 2D crystal so that the top few layers stick to it. The tape then is pressed against a substrate and peeled off, leaving the bottom 2D layer on the surface. Nature has produced 3D materials such as graphite which are composed of many stacked layers of 2D planar materials. In general, 2D materials are rarely found in nature because of their instability. In layered materials, bonding force between the planes are much weaker than the bonding between the carbon atoms within the planes. Because of this, we can exfoliate them by scotch tape.

For our studies, the substrate was wafers of SiO_2 cut into small pieces of approximately 1 cm^2. We used two type of tapes depending on the nature, quality, and quantity of materials required on the SiO_2 substrate. We used scotch tape when flakes longer than 10 μm were not necessary and glue on the substrate was not a major issue. The glue can be removed by acetone and isopropyl alcohol (acetone/IPA) or H_2/Ar annealing. We used thermal release tape for exfoliating materials like GaSe. In our experience, it is easier to exfoliate a few monolayers with this tape. Upon heating, the adhesive in thermal release tape becomes weak and material monolayers are released.

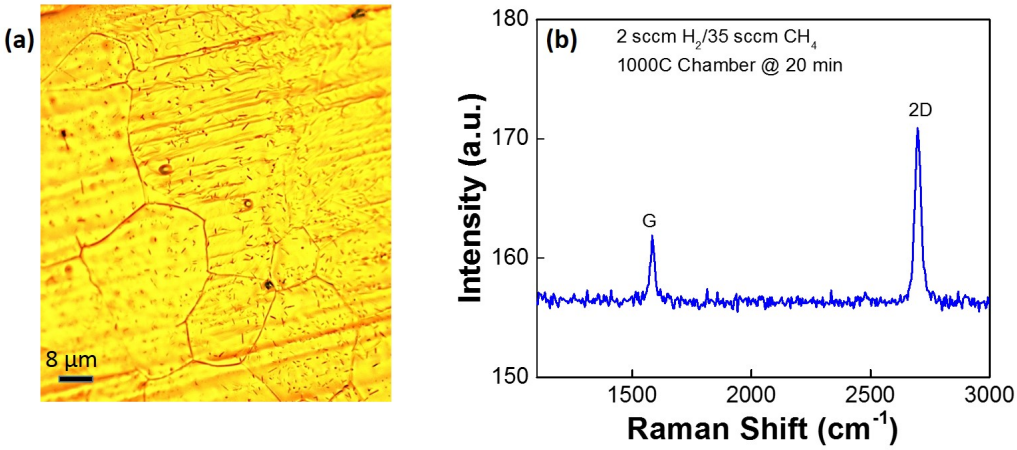

Figure 2.1: (1) Optical image of chemical vapor deposition (CVD) Graphene on 25 μm Copper foil; (2) Raman Spectroscopy of same CVD graphene with excitation laser 488 nm after transferred on Si substrate. Monolayer graphene can be identified with ratio of height of its G (1583.8 cm^{-1}) and 2D (2698.3 cm^{-1}) peaks.

2.2.2 Chemical Vapor Deposition (CVD)

The formation of few layered graphene has been known for nearly 50 years.[51] The CVD method is one of the most practical methods for synthesizing large areas of graphene.[52,53,54,55,56,55] The analogues of graphene like hexagonal boron nitride (h-BN)[57] and boron carbon nitride nanosheets[58] are also synthesized using this method. The CVD method has also been used in efforts to make thin layers of MoS_2[59,60] and WS_2[61] method also been explored. However, the transfer process may degrade the quality of CVD 2D materials transferred onto substrate.

Our method involves the creation of CVD graphene on a copper (Cu) substrate. It was first reported in 2008 and 2009[62,55,52] for preparation of graphene by CVD method. It has emerged as major way to produce large scale sheets of graphene. Two main substrates for CVD graphene used by researchers are Nickel and Copper. Both monolayer and multilayer graphene can be grown on polycrystalline Ni films. By using single-crystalline Ni (111), smooth substrate without grain boundaries, the percentage of monolayer graphene on Ni can be increased. However, Cu can be used for more efficient growth of monolayer graphene only. Hence, we used CVD to grow graphene on a Cu substrate. Our method is explained in detail in the following paragraphs.

First, we cleaned Cu foil with acetone/isopropyl alcohol (IPA). We placed the Cu foil in a furnace tube and flushed it with Ar 3-4 times at 100 mTorr pressure. To initiate graphene growth, we annealed 25 μm thick Cu foils at 1000 °C followed by 2 sccm H_2 and 35 sccm of CH_4 mixture for 20 minutes. Finally, we cooled the chamber protecting the graphene with and Argon atmosphere. An optical image of CVD graphene on Cu foil is shown in Fig. 2.1(a).

Graphene growth on Cu is self-limiting.[63] Cu, unlike Ni has ultralow carbon solubility. Only a very small amount of carbon dissolved in Cu even if the hydrocarbon concentration is high. Thus catalytically decomposed hydrocarbon on Cu surfaces are a major carbon source for graphene formation. Once the Cu surface is fully covered with the first layer of graphene, there is no Cu catalyst exposed to hydrocarbon to promote decomposition and growth.

During CVD, the reaction occurs between the copper substrate and the graphene. It creates a hydrostatic compression, coupling the graphene to the substrate. We used poly(methyl methacrylate) (PMMA) as a support polymer to facilitate the transfer of graphene from Cu onto a Si substrate. With this method, graphene is coated with PMMA, the Cu is etched and, rinsed with DI water and the graphene is transferred onto another substrate. This can be done without damaging the material. Raman spectroscopy of CVD graphene is shown in Fig.2.1(b). By calculating the ratio of peak intensities,,[64] I_{2D}/I_G we can identify monolayer graphene. $I_{2D}/I_G > 1$ indicates monolayer graphene.[64] A method of direct growth of graphene on insulating substrates like Si/SiO_2 would be attractive for better quality interfaces. Breakthroughs in graphene-based technology may be achieved by further understanding and better control of CVD of 2D materials.

2.3 Making Thin Films Visible

2.3.1 Optical Interferometry

Thickness identification of two dimensional materials[65] like graphene[1] and MoS_2[66] has been demonstrated[65,1,66] by a non invasive method to find the contrast. The number of layered materials on given substrate is used by the method of optical interferometry. Thin flakes of graphene

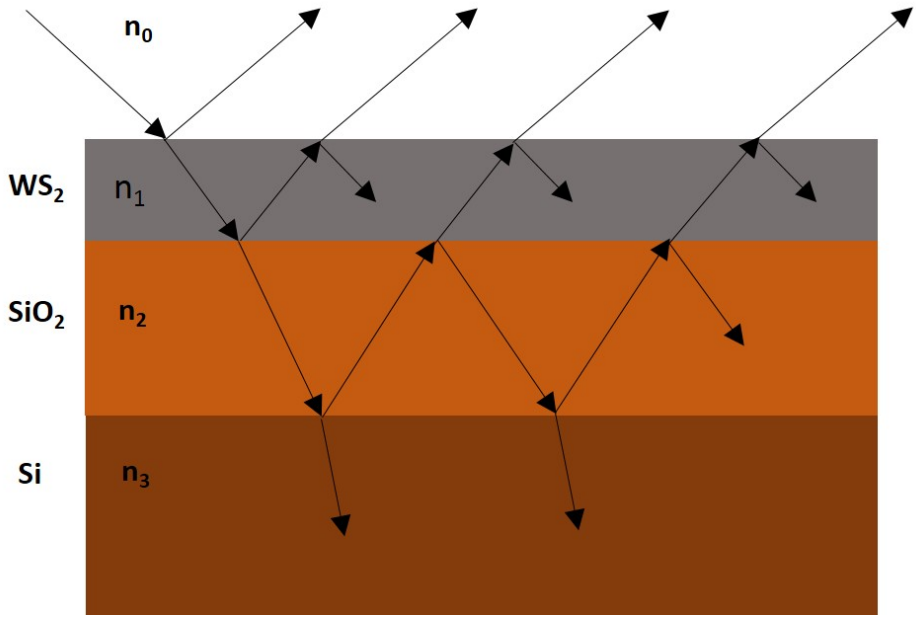

Figure 2.2: The reflection of light at two interface: Schematic of thin film reflection and interference where n_0, n_1, n_2 and n_3 are the refractive indices of air, WS_2, SiO_2 and Si respectively.

and other semiconductor TMDCs are sufficiently transparent to add an optical path, which changes their interference color. Even a single layer of two dimensional materials on certain thickness of SiO_2, was found to give maximum contrast. It is used to allow spot their layer thickness. By maximizing the contrast, this understanding would allow us to find thickness of two-dimensional materials on any substrate by using different wavelengths. We will extend the idea to reflection of light at more than two interfaces in later sections of this dissertation. It would be interesting to see how can we use this technique to find monolayers on any thickness of dielectric using PMMA as top layer. The theory of optical interference and hence contrast to find thin layers of these materials are given below.

2.3.1.1 Reflection of Light at Three Interfaces (Air/Thin-Film/SiO_2/Si)

In this section, we discuss the interference and optical contrast of thin films on different substrates of different thickness. We first describe the reflection of light at two interfaces, then explain our approach and results. "Two interface" implies a succession of three optical media of refractive indices n_0, n_1, and n_2 as shown in the Fig. 2.2, where radiation is partially reflected and transmitted.

A thin film can be defined if the separation between these boundaries is an order of magnitude of a wavelength of the incident light. We can assume that the film is plane parallel, homogeneous and, non-absorbing. If the reflectance is given by R and transmittance by T, then the energy equation is,

$$R + T = 1. \tag{2.1}$$

There are three methods to understand how a incident light on a system of films is reflected: (a) Using Maxwell equations with appropriate boundary conditions, a boundary value problem may be set up and solved, (b) Using knowledge of the solution at each interface between optical media (the Fresnel coefficients), the proportion of the wave reflected from the boundary may be calculated in amplitude and phase, and (c) An analogy between the electrical theory of transmission lines and the optical system may be exploited.

Method (b) used in the derivation for the reflection of light for thin films is close to the method described by Anders.[67] It has been tested experimentally as well as theoretically on graphene with different thickness of oxides and incident lights of different wavelengths.[1] We followed the same method and extend it to more than two interfaces in Section (2.3.2).

2.3.1.2 Optical Contrast in graphene/SiO_2/Si

Optical contrast appears due not only to an increased optical path but also to the significant opacity of graphene. By using the Fresnel equations, we investigated the dependence of contrast on SiO_2 thickness and light wavelength λ. This understanding allowed us to maximize the contrast and, by using narrow-band filters, to find graphene crystallites on practically any thickness of SiO_2 and also on other thin films. The contrast is given by,

$$Contrast = \frac{I_{Graphene+ox} - I_{ox}}{I_S}, \tag{2.2}$$

where, ox represents SiO_2.

Graphene visibility depends strongly on both thickness of SiO_2 and light wavelength [Fig. 2.3].

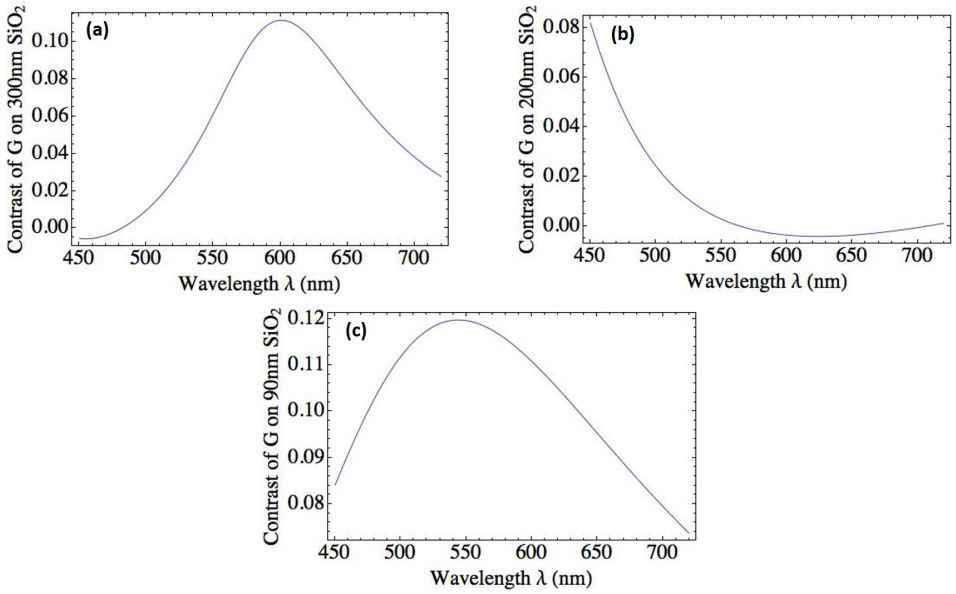

Figure 2.3: Thin film reflection and interference of graphene/SiO_2/Si: Contrast of graphene as a function of wavelength for (a) 300 nm thick of SiO_2, (b) 200 nm thickness of SiO_2, and (c) 90 nm thickness of SiO_2. Plot made using *Mathematica*. Results are similar to the reference.[1] This figure is presented here to confirm our baseline before moving to other materials and then to more interfaces.

By using monochromatic illumination, we isolated graphene for any SiO_2 thickness; however, 300-nm or 90-nm thick SiO_2 gave the most suitable contrast for its visual detection as seen in [Fig. 2.3]. We confirming that we could use this method to plot contrast for many thicknesses of SiO_2, we proceeded to investigate other substrate materials.

2.3.1.3 Optical Contrast in WS_2/SiO_2/Si

Locating layers of materials, such as graphite or semiconducting transition metal dichalcogenides, and identifying their thicknesses are the first steps in the study and practical applications of these materials. When light encounters an interface, e.g. air/WS_2, WS_2/SiO_2, SiO_2/Si, a part of it reflects back. The quantity and direction of reflected light depends on the properties of the interface materials. If r_1, r_2 and r_3 are relative indices of reflection of WS_2, SiO_2, and Si respectively, then,

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1}, \tag{2.3}$$

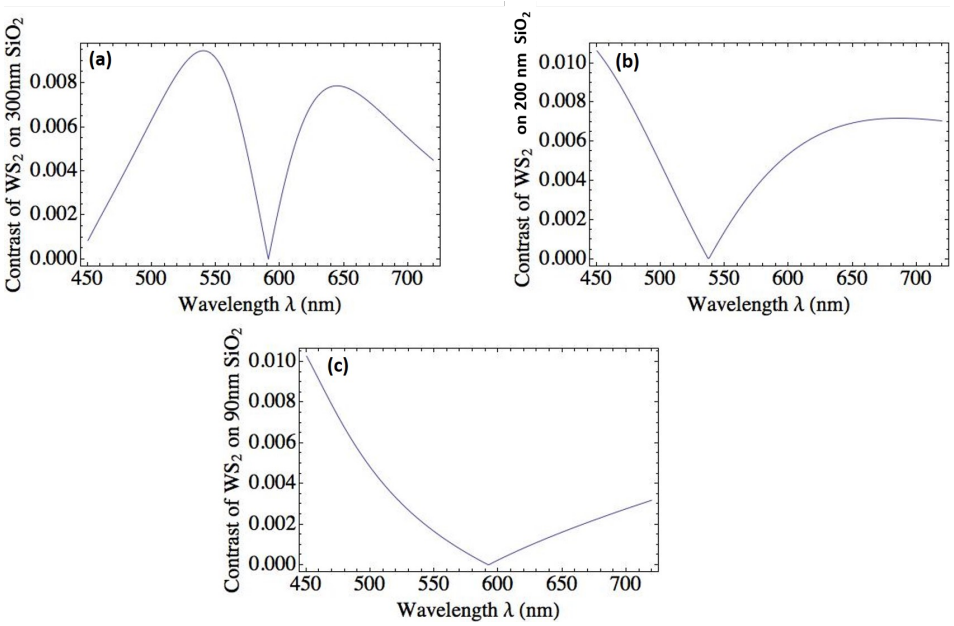

Figure 2.4: Thin film reflection and interference $WS_2/SiO_2/Si$: Contrast of WS_2 as a function of wavelength for (a) 300-nm thickness of SiO_2, (b) 200-nm thickness SiO_2, (c) 90-nm thickness SiO_2. Plot made using *Mathematica*.

$$r_2 = \frac{n_1 - n_2}{n_1 + n_2}, \tag{2.4}$$

and

$$r_3 = \frac{n_2 - n_3}{n_2 + n_3} \tag{2.5}$$

where, $n_0 = 1$ is the refractive index of air, $n_1 = 1.67$ is the refractive index of WS_2, $n_2 = 1.47$ is the refractive index of SiO_2 and $n_3 = 5.6\text{-}4i$ is the refractive index of Si. The phase difference is given by,

$$\phi_1 = \frac{4\pi n_1 d_1}{\lambda}, \tag{2.6}$$

and

$$\phi_2 = \frac{4\pi n_2 d_2}{\lambda}. \tag{2.7}$$

Reflected light intensity can be found by,

$$I(n_1) = |(r_1 e^{i(\phi_1+\phi_2)} + r_2 e^{-i(\phi_1-\phi_2)} + r_3 e^{-i(\phi_1+\phi_2)} + r_1 r_2 r_3 e^{i(\phi_1-\phi_2)})$$

$$\times(e^{i(\phi_1+\phi_2)}+r_1r_2e^{-i(\phi_1-\phi_2)}+r_1r_3e^{-i(\phi_1+\phi_2)}+r_2r_3e^{i(\phi_1-\phi_2)})^{-2}|^2, \tag{2.8}$$

and contrast is given by,

$$Contrast = \frac{I_{TMD+ox}-I_{ox}}{I_{ox}}, \tag{2.9}$$

where, *ox* represents SiO_2 and *TMD* represents WS_2. As shown in Fig. 2.4, contrast of a monolayer WS_2 was maximum at $\sim$ 550 nm of wavelength of filter used in optical microscope. This analysis on WS_2 is important to find monolayer of WS_2 on different substrate and wavelength of light used. To explore and as a prove of concept, we explored the contrast method in heterostructure materials four interfaces. Our results are described in the next section.

2.3.2 Reflection of Light at Four Interfaces (Air/PMMA/WS_2/SiO_2/Si)

Making graphene and other 2D materials visible on different substrates is not easy with most light filters. However, we investigated interference in materials with four interfaces. The results will be helpful in developing methods to identify thin films on any substrate. If we assume r_1, r_2, r_3, and r_4 are relative indices of reflection of graphene, WS_2, SiO_2, and Si respectively, then

$$r_1 = \frac{n_0-n_1}{n_0+n_1}, \tag{2.10}$$

$$r_2 = \frac{n_1-n_2}{n_1+n_2}, \tag{2.11}$$

$$r_3 = \frac{n_2-n_3}{n_2+n_3}, \tag{2.12}$$

and

$$r_4 = \frac{n_3-n_4}{n_3+n_4}, \tag{2.13}$$

where, $n_0 = 1$ is the refractive index of air, $n_1 = 2.6\text{-}1.3i$ is refractive index of graphene, $n_2 = 1.67$ is refractive index of WS_2, $n_3 = 1.47$ is refractive index of SiO_2, and $n_4 = 5.6\text{-}4i$ refractive index of

Si. Relative indices of reflection are given by,

$$\phi_1 = \frac{4\pi n_1 d_1}{\lambda}, \tag{2.14}$$

$$\phi_2 = \frac{4\pi n_2 d_2}{\lambda}, \tag{2.15}$$

and

$$\phi_3 = \frac{4\pi n_3 d_2}{\lambda}. \tag{2.16}$$

The amplitudes can be given by,

$$A_3 = \frac{r_3 + r_4 exp(-i\phi_3)}{1 + r_3 r_4 exp(-i\phi_3)}, \tag{2.17}$$

$$A_2 = \frac{r_2 + A_3 exp(-i\phi_2)}{1 + r_2 A_3 exp(-i\phi_2)}, \tag{2.18}$$

and

$$A_1 = \frac{r_1 + A_2 exp(-i\phi_1)}{1 + r_1 A_2 exp(-i\phi_1)}. \tag{2.19}$$

Intensity is given by,

$$I = A_1 A_1^*, \tag{2.20}$$

$$I = \frac{(1 + e^{i\phi_1} r_1 r_2)(e^{i\phi_3} r_3 + r_4) + e^{i\phi_2}(e^{i\phi_1} r_1 + r_2)(e^{i\phi_3} + r_3 r_4)}{(r_1 + e^{i\phi_1} r_2)(e^{i\phi_3} r_3 + r_4) + e^{i\phi_2}(e^{i\phi_1} + r_1 r_2)(e^{i\phi_3} + r_3 r_4)}, \tag{2.21}$$

and contrast is given by,

$$Contrast = \frac{I_{PMMA+TMD} - I_{PMMA}}{I_{PMMA}}, \tag{2.22}$$

where, *TMD* represents WS_2.

We plotted the contrast as a function of the wavelength of the filter used in the optical microscope [Fig. 2.5(a)]. We used these plots to find the wavelength of light corresponding to maximum contrast.

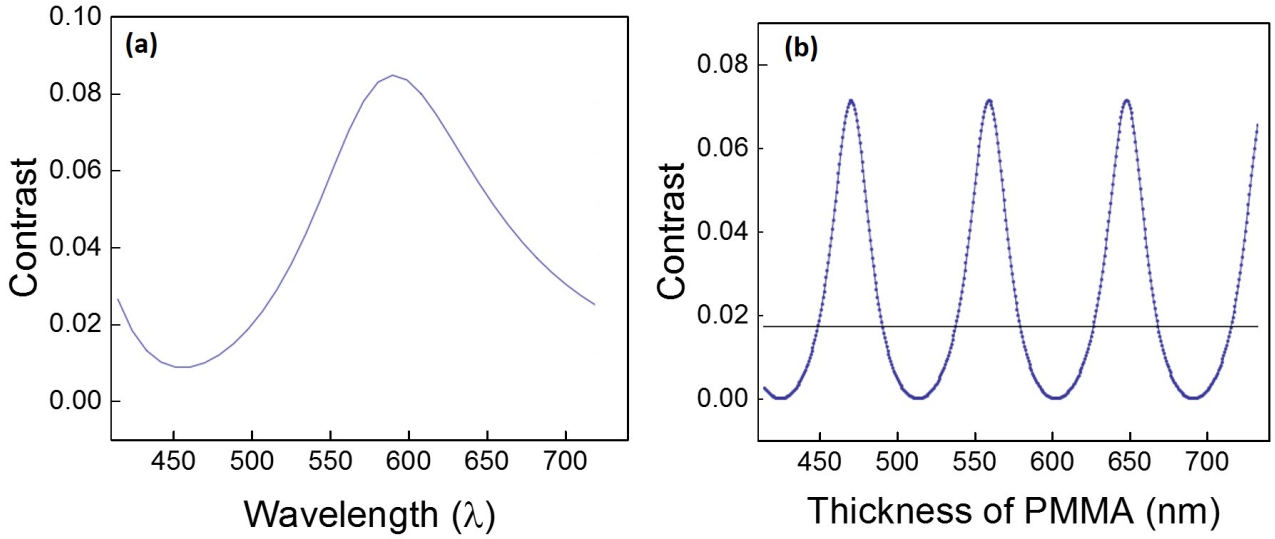

Figure 2.5: Reflection of light at four interfaces in air/PMMA/WS_2/SiO_2/Si heterostructure: (a) Plot of contrast versus wavelength of light to determine wavelength maximizes contrast for 100-nm PMMA/ML-WS_2/300-nm SiO_2/Si, and (b) Contrast versus thickness of PMMA on top of Monolayer WS_2/300-nm SiO_2/Si at $\lambda\sim$ 633-nm. Contrast is maximized when the thickness of PMMA is $\sim$ 90-nm, 225-nm and 375-nm. Plot made by using *Mathematica*.

The set preconditions we used were 100-nm thick PMMA on top of monolayer WS_2 (ML WS_2) overlaid on 300-nm SiO_2. Under these conditions, 600-nm wavelength light gave the maximum contrast. We used red light of wavelength $\sim$ 633 nm to find out what thickness of PMMA would maximize the contrast produced by monolayer WS_2. As shown in Fig. 2.5(b) $\sim$ 90 nm, 225 nm, 375 nm thick of PMMA gave maximum contrast. We confirmed the presence of monolayer WS_2 by photoluminescence, shown in Section 2.5.2 of this dissertation.

2.4 Transfer Process: Wet Transfer by PMMA

There has been improvement in heterostructure fabrication techniques, including transfers using PMMA, 4-phenyl-4-(1-piperidinyl)cyclohexanol (PPC) and polydimethylsiloxane (PDMS). Each of these transfer techniques has its own advantages and drawbacks as explained in the following sections. We optimized the PMMA technique and the PPC technique to successfully transfer single layer of material onto another thin layer [Fig. 2.6].

2.4.1 Preparation of PVA Layer and Transfer by PVA/PMMA/2D-material

We prepared 8% poly(vinyl alcohol) (PVA) and 5% PMMA solutions. We spun 8% PVA solution, at 6000 revolutions per minute (rpm) on a 90-nm SiO_2 substrate. We heated the PVA coated substrate on preheated hot plate at 100 °C for five minutes. We then allowed the substrate cool to room temperature, before spinning another coating on it. This cooling step is imperative for any spinning process.

We exfoliated any 2D material, say graphene or WS_2, onto the PVA/PMMA-coated substrate and took images of the thin flakes with an optical microscope. After locating a flake of 2D material on the substrate, we scraped off the PMMA/PVA along the edges of substrate. This step removes the inhomogeneous coating of polymers that is often found at the edge. It also provides a route of entry under the PMMA for deionized (DI) water to dissolve the PVA. While scraping the PMMA, we scratched a small mark near the exfoliated flake to assist with visually locating it in later steps.

We added DI water to a beaker to a height just a bit shorter than length of our substrate. The reason for incomplete submersion is that, as water dissolves the PVA, the PMMA layer begins to separate from the substrate. Since substrate is heavy and does not float, when the PMMA detaches the substrate can topple or damage the PMMA.

After the PVA was fully dissolved in Fig. 2.6(c-d), the PMMA with the exfoliated flake on top of it, floated on the surface of water. We slowly added water along the sides of the beaker until it was full, taking care not to disturb or roll the PMMA. We customized a fishing scoop with a hole of diameter approximately 4 mm to scoop the floating PMMA such that the exfoliated flake was in the middle of the hole in the scoop. We used the mark we made on the PMMA to center the flake on the hole.

After we retrieved the PMMA with the exfoliated flake on top, we heated it slowly at 10 °C per minute ramp-up until it is reached approximately 100 °C to completely evaporate the water. During this heating, we monitored the PMMA for changes in color or visible wrinkling. If the temperature has not yet exceeded 45 °C, we placed the wrinkled PMMA back in water to straighten and repeated the scooping and heating process.

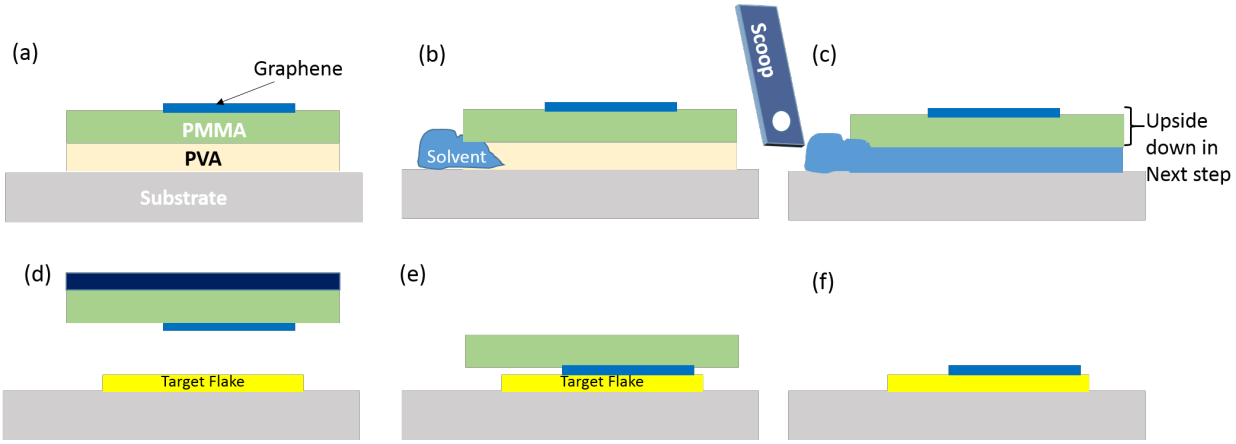

Figure 2.6: Dry transfer process: (a) Graphene exfoliated on PMMA/PVA, (b) PMMA is immersed in solvent (DI water), (c) Water selectively dissolves PVA underneath the graphene/PMMA. (d) The PMMA with graphene is flipped upside down and precisely stacked on the target flake by a micromanipulator, (e) PMMA/graphene is transferred onto target flake, and (f) PMMA is removed by IPA/acetone.

For example, graphene/$MoSe_2$/graphene heterostructure FETs were originally made as TFETs as shown in Fig. 2.7. We fabricated these heterostructures on SiO_2 using our dry transfer method and measured graphene $I\,V$ characteristics. Graphene shows expected n- and p-carrier transport, proving validity of our transfers for FETs. The bottom graphene/SiO_2 FET acts as a parallel-plate capacitor. in which applied gate voltage introduces a charge of opposite sign in graphene. The Fermi level of the graphene with respect to the Dirac point moved as a function of induced carrier concentration n as $\varepsilon_F = \sqrt{n\pi}\hbar v_F$ where $\hbar$ is reduced Plank constant and v_F is the Fermi velocity with value $\sim 10^6$ ms^{-1}. The Fermi level can be moved into valence band or conduction band depending on the direction of V_G. With a change in number of available charge carriers, I_D/V_G decreases as shown in Fig. 2.7. For $V_G <$ -26 V charge carriers are holes while $V_G >$ -26 V charge carriers are electrons. The Dirac point lies close to $V_G =$ -26 V instead of at $V_G = 0$ as happens for undoped graphene. That is because of residual doping due to organic compounds like poly (methyl methacrylate) (PMMA) used in the transfer process Fig. 2.7. The density of state (*DOS*) vanishes at the Dirac point, thus it is expected that the resistance would approach infinite at this point. However, there is always some finite value of resistance at that point as also shown by Fig.(2.7). The reason is the existence of electron hole puddles in that region.[68]

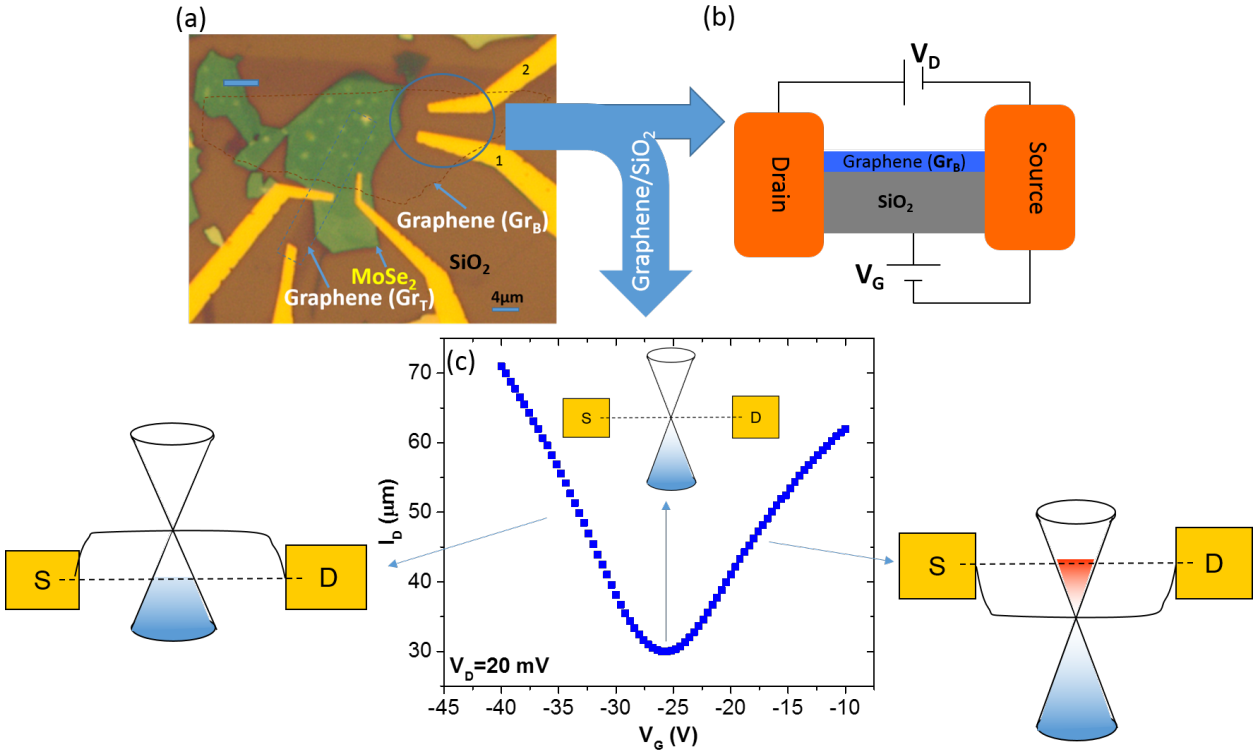

Figure 2.7: (a) Optical image of a graphene/$MoSe_2$/graphene heterostructure FET on 300-nm SiO_2 obtained by the PMMA method (described in detail in section 2.4). Even bottom graphene is transferred by PMMA method. 5/100-nm Ti/Au electrode achieved by electron beam evaporator lithography process (described in Chapter 2), (b) Schematic diagram of typical FET shows source, drain, channel and gate, (c) Only graphene-*I V* characteristics corresponding to label 12 on bottom graphene-only is shown with correspondin*D*- bending. Since this graphene went through wet heterostructure transfer by PMMA, it is *n*-doped.

Most importantly, even after undergoing two transfer processes, first $MoSe_2$ on targeted monolayer Gr_B and then Gr_T on $MoSe_2/Gr_B$, graphene $I-V$ still retain its basic characteristics in our heterostructure. Our working wet transfer technique is described in detail in Chapter 2 of this dissertation. In the introduction chapter, It serves to proves the field that our technique reproduces the baseline results of control device (graphene).

Wrinkles are more likely to occur when, during fishing and scooping, the scoop contacted the PMMA layer at a large angle. It was best to use as small angle between the fishing scoop and the PMMA as possible and be vigilant not to disturb the water in beaker too much. With the help of micro manipulator, we positioned the flake on our target substrate. We heated the substrate to 180 °C with ramp up speed of 10 °C per minute to transfer the flake onto the desired place. With this method, the flake was transferred to the target site with precision around 1 μm. We immersed the transferred chip in acetone and incubated it for 30 minutes. Finally, we cleaned it with IPA and dried with nitrogen.

2.4.2 Transfer by PPC

We used another transfer technique, transfer by PPC. In our modified method for transferring by PPC, we first exfoliated the two-dimensional material and transferred it to substrate without-alignment marks. We found on alignment marked substrate, the PPC got into the trenches of the alignment marks, and became difficult to remove during the transfer process. After cleaning, annealing and locating the exfoliated material, we spun the PPC at 4000 rpm and heated it on a hot plate at 50 °C. If we baked it at higher temperature, it was difficult to peel off the PPC in the transfer process due to polymerization. We have successfully achieved transfer by PDMS as well. However, most of the heterostructure in this dissertation were achieved by PMMA/2D-material transfers. Hence, we restrict our detailed discussion to transfer by PMMA only. Once we isolated 2D materials and constructed heterostructures, we considered the best way to characterize the layers and the quality of the sample by characterization tools as following section describes.

2.5 Material Characterization

2.5.1 Raman Spectroscopy

Raman spectroscopy is an ideal non-invasive characterization tool. It offers high resolution, and gives structural and electronic information. It is used to study vibrations and rotations of molecules. It probes vibrations of lattice in crystals. Raman spectroscopy involves shining monochromatic laser onto a sample and inspecting the spectrum of light reflected back. The Raman effect occurs when electromagnetic radiation impinges on a molecule. It interacts with the polarizable electron density, and the bonds of the molecule. It is specific to the phase (solid, liquid or gaseous). It is also specific to environment in which the molecule is found. Raman Spectroscopy is especially interesting in graphene. It is because graphene is composed entirely of surface atoms. So, all off them are equally influenced by environmental changes, which Raman spectroscopy can observe.

Raman spectroscopy is a standard tool for characterizing graphene samples because of graphene's distinct features.[64] The specific features depend strongly on the number of layers and stacking order. Upon laser excitation, the Stokes phonon energy shift creates two peaks in graphene: a primary in-plane vibrational mode, and *2D* (2698.27 cm^{-1}), and a second-order overtone of a different in-plane vibration, *G* (1583.78cm^{-1}). However, we observe very sharp *2D*-band for monolayer graphene compared to three layers. Monolayer has also the lowest *G*-band intensity as shown in Fig. 2.8. As the number of layers increase the intensity of *2D* peak diminishes compared to *G* peak.

Thickness of graphene is also determined by optical contrast method as discussed in section 2.3.1. The 2*D*-peak occurs due to double resonance Raman process that involves inter valley scattering of an electron by two transverse optical phonons. It has the highest intensity in single layer graphene on SiO_2.

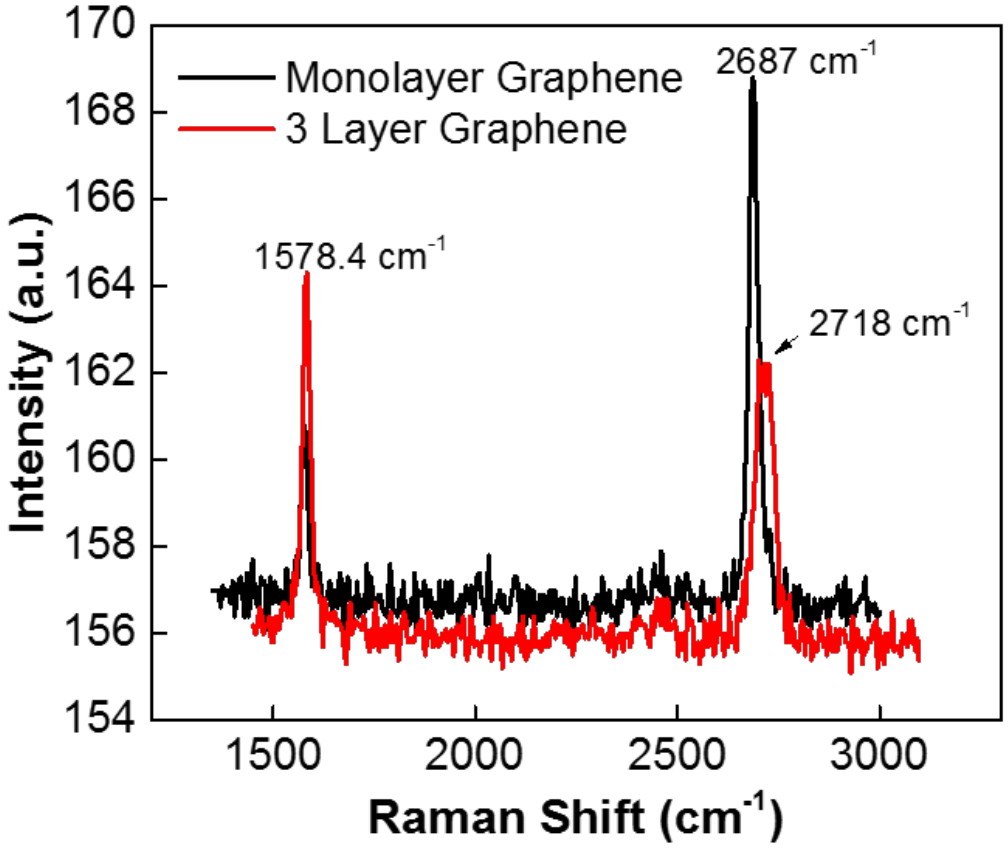

Figure 2.8: Raman Spectra for a single-layer graphene sample and three layer graphite using 480-nm excitation wavelength laser. By position and shape of *G* and *2D* peaks graphene can be identified.

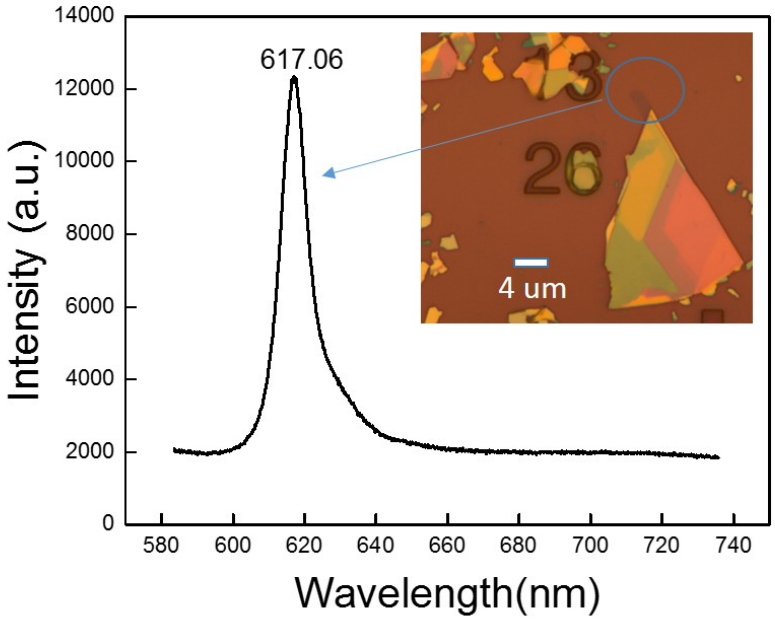

Figure 2.9: Room-temperature photoluminescence of monolayer WS_2.

2.5.2 Photoluminescence

K point WS_2 undergoes transition from an indirect-gap semiconductor in a multilayered form to a direct gap semiconductor in a monolayer form.[69] Our photoluminescence (PL) experiment shown in Fig. 2.9 are consistent with such transition (few-layered or bulk PL is not shown). In monolayer WS_2, we observed a single sharp PL peak at 2.01 eV with full width at half-maximum (FWHM) of $\sim$ 35.7 meV is observed [Fig. (2.9] when we used an excitation laser $\lambda_{exc} = 405$-nm. However, few-layered samples exhibit very weak or no PL near 2.01 eV (not shown here), consistent with the indirect band gap of few-layer and bulk WS_2. For WS_2, PL quantum yield drops 100 folds when the thickness is increased from monolayer to bilayer and gradually reduces with further increase in thickness.[69] Direct electronic transitions in WS_2 originate from exiting radiative relaxation. For this reason the PL signal always appears at energies slightly lower then 2.03 eV direct band gap of WS_2. In the single layer form, WS_2 possesses exciton energy of 2.02 eV.

The reason behind weak PL signal from bulk WS_2 versus monolayer WS_2 has to do with direct versus indirect band gap. For semiconductors with a direct band gap, photons with energy greater

than the band gap energy can be readily absorbed or emitted. For indirect band gaps, an additional phonon must be absorbed or emitted to supply the difference in momentum. It makes the photon absorption or emission process much less efficient. The PL was very intense for a monolayer WS_2. It exhibited a single peak corresponding to the direct excitonic transition at the K point. As the layer number increases, the indirect transition between the local minimum of the conduction band and the local maximum of the valence band at decreases in energy. This causes an indirect transition between these two electronic states starts to compete with the direct transition at the K point. This competition between direct and indirect electronic transitions dramatically reduces the PL quantum efficiency.

Many of single-layer TMDCs have primarily direct semiconducting band gaps. They are of great interest for applications in optoelectronics. It is because they are atomically thin and processable. They have great potential for flexible and transparent optoelectronics, because they are atomically thin and processable. During the past few years, major progress has been made in studying atomically thin-layered molybdenum disulfide (MoS_2).[70] It is the most explored layered material among the TMDC family.

2.6 Annealing

Surface contamination has been a major problem associated with exfoliation by scotch tape and using PMMA or PDMS to create thin 2D flakes and heterostructures. The electron beam resists applied during lithography, like PMMA. They undergoes scission of the polymer chains. It is when they are exposed to an electron beam. It can be a major issue in device performance. Even after annealing, PMMA cannot be removed entirely from graphene. This contamination is highly mobile. It remains unnoticeable in scanning probe microscopy (SPM). In heterostructures, isolated 2D flakes are stacked together. The interfacial contamination becomes trapped between the layers. Contaminants like water, and hydrocarbons cover every surface, during preparation of exfoliated samples or heterostructures.[71,72,73] Thus heterostructures, rather than comprising layers held to-

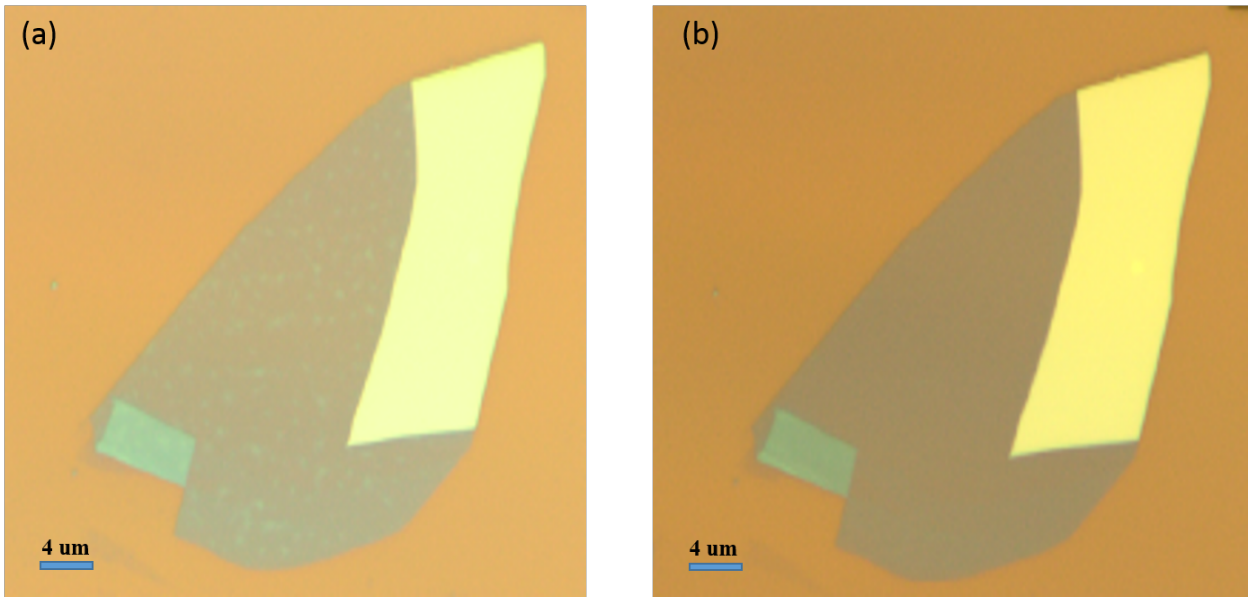

Figure 2.10: Forming gas annealing: (a) Optical image of a flake of h-BN on 90-nm SiO_2. (b) Optical image of same h-BN after H_2/Ar annealing at 250 °C. Much of the organic residue left over from exfoliation is removed.

gether by van der Waals forces, can be layer cakes glued together by contamination. They should be prepared under highly surface science conditions.[74] However, some heterostructures have a self-cleaning mechanism.[75,76,77]

2.6.1 Forming Gas Annealing

The polymer residues leave surface contamination. Heat treatment at 350 °C is used to remove adhesive residues on 2D materials left from exfoliation and lithography techniques. However, at high temperature thermal annealing in air can result in oxidation of the semiconductor surface. To reduce this oxidation, annealing is carried out in a special atmosphere, It can be atmosphere such as in forming gas, a mixture of hydrogen and argon.

The flake in Fig. 2.10(a) was exposed to adhesive during exfoliation. Organic residue is visible in the optical image. We applied H_2/Ar at 10/100 sccm and heated the flake at 250 °C for 2 hours at base pressure of furnace 3 Torr. Following forming gas annealing, we observed no visible residue under an optical microscope [Fig. 2.10(b)]. However, we still saw residues by SEM imaging as

shown in Fig. 2.12(b). Additionally, Raman analysis showed a remarkable blue-shift of the 2D mode after annealing, implying an anneal-induced band structure modulation in graphene with defects. Forming gas is used as an atmosphere for processes that need the properties of hydrogen gas. We thus developed a thermal annealing method, described in the next section, the result of which was residue-free structure [Fig. 2.12(c)].

2.6.2 Thermal Annealing

In thermal annealing, material is heated to a high temperature for a period of time, and then cooled. This process can be effective in situations where oxidation from heating under air is not a concern. In the case of h-BN, we used oxidation to our advantage to oxidize. It removed tape adhesive residue. Thermal annealing can induce ductility, and relieve internal stresses. It can refine the structure by making it homogeneous. The basic principal behind thermal annealing is that in high temperatures atoms diffuse within a solid material, so that the material progresses towards its equilibrium state.[78,79,80,81] Heat increases the rate of diffusion. It occurs by providing the energy needed to break bonds. The movement of atoms has the effect of redistributing, and decreasing the dislocations in metals and semiconductors.[82]

Two important results come from h-BN thermal annealing in our conditions: (1) Annealing exfoliated h-BN on SiO_2 at 750 °C removed the scotch tape residue from the h-BN as well as from the SiO_2 substrate [Fig. 2.11]. Since a sample that looks clean in optical microscopy may still have some residue, we used SEM to examine the h-BN for additional residue.

(2) Our thermal annealing process removed all detectable residue [Fig. 2.12(c)]. Our annealing method produced a clean h-BN surface.

2.7 Electron Beam Lithography

Electron beam lithography (EBL) is technique for pattering at the nano meter scale. A focussed energetic beam of electrons on a resist create a pattern of gaps into which metal is deposited.

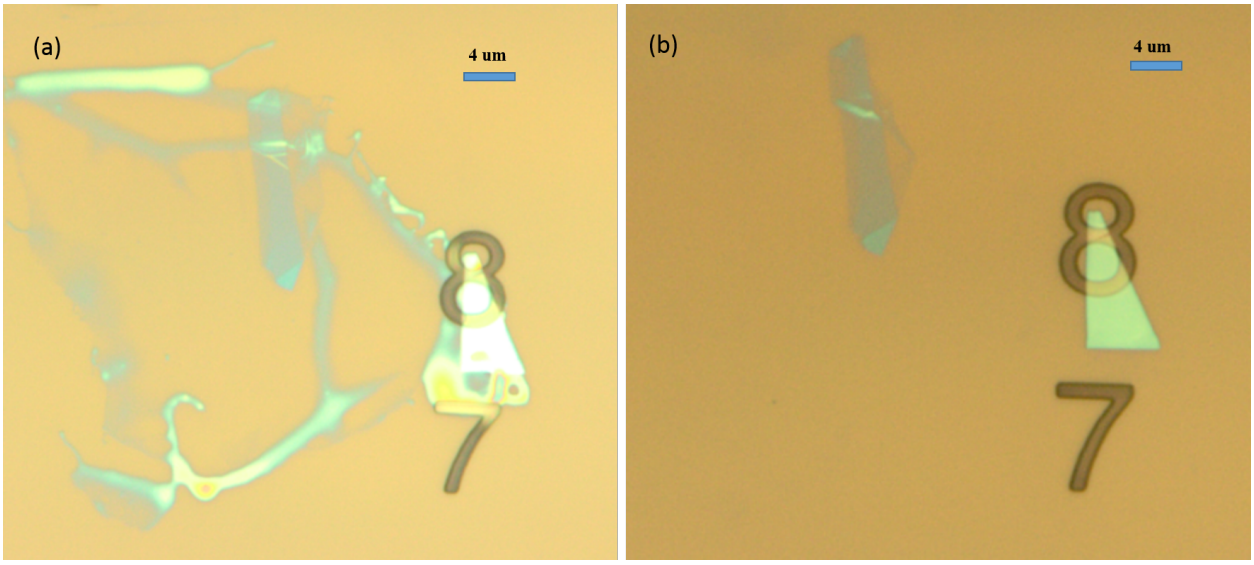

Figure 2.11: Thermal Annealing: (a) Optical image of h-BN transferred by exfoliation but not cleaned with IPA/acetone, (b) Optical image of h-BN after treatment at 750 °C in air for 30 minutes. Many of the hydrocarbon surface contaminants are removed by oxygen. Clearly the residues are removed just by thermal annealing.

Both bottom-up and top-down techniques are used in manufacturing various devices. The top-down approach is based on three elements: pattering, etching and deposition in order to define the whole fabrication processes. During the fabrication of complex systems both approaches to work together.

We deposited PMMA/MMA in electron beam lithography (EBL) technique. Polymers PMMA and MMA act as positive e-beam resists [Fig. 2.13]. They consist of long polymer chains of carbons atoms of various molecular weights . The polymers like PMMA/MMA are commonly used in EBL for lift-off purposes because they can be deposited with an under-cut resist profile to avoid metal coating metal coating the side wall of the resist. We used Ti/Au for source and drain electrodes to WS_2 FETs. We used e-beam to etch the resist and then applied Ti and Au metal to form electrodes.

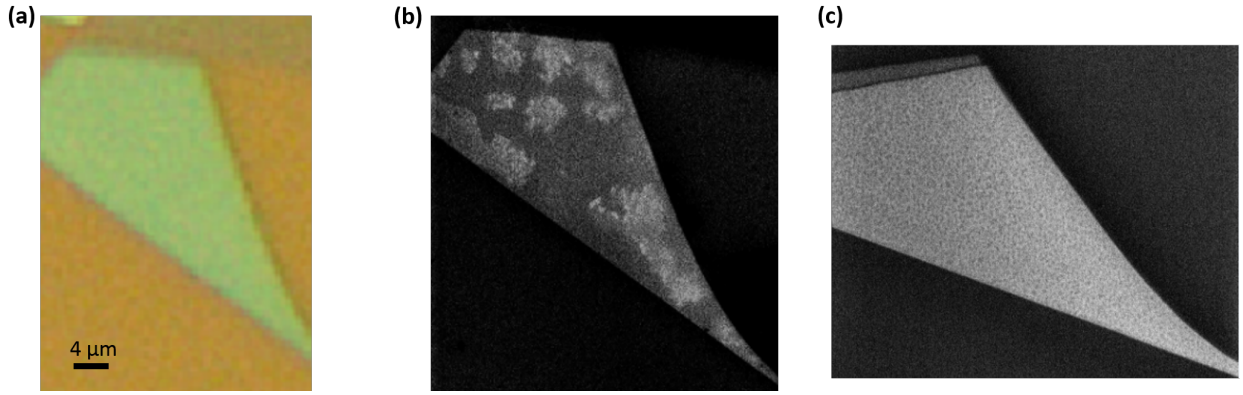

Figure 2.12: (a) Optical image of h-BN on 90-nm SiO_2. (b) SEM image of the same h-BN on 90-nm SiO_2. (c) Annealed at 750 °C in air, and again took SEM image of the same flake. Notice the residue are gone now thus achieving residue free surface.

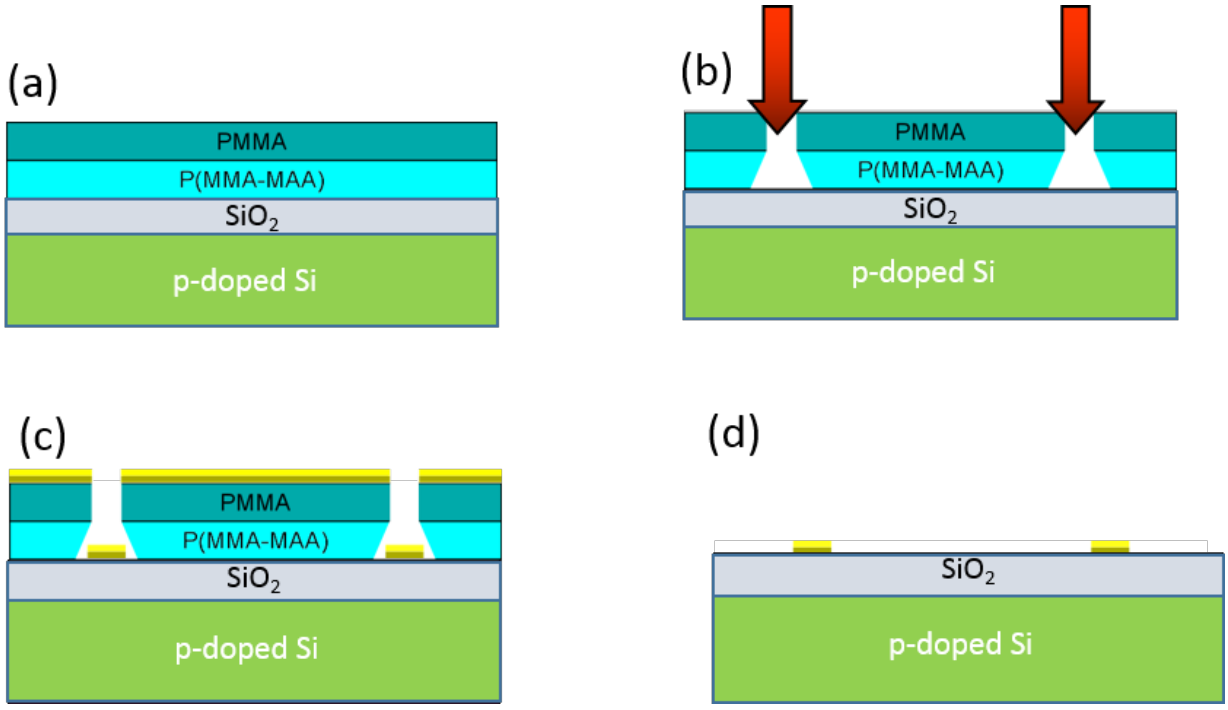

Figure 2.13: Electron Beam Lithography Process: (a) PMMA and P(MMA-MAA) deposited on SiO_2/Si substrate. (b) After exposure to electron beam, and developing with a mixture of MiBK:IPA::1:3. (c) Metal deposition. (d) lift off with suitable solvent (acetone) to leave the metal film on the substrate.

2.8 Four-Probe Measurement: Contact Resistance Measurement of a Field-Effect Transistor

In graphene heterostructures, one dimensional contact enables high electronic performance. It includes low-temperature ballistic transport over distances longer than 15 μm. It also includes high room-temperature mobility comparable to the theoretical phonon-scattering limit.[83] The contact resistance of MoS_2 FETs has been reduced (by five times). An optimized TiO_2 Fermi level de-pinning layer was used, which reduced the effective Schottky barrier height to 0.1 eV.[84,85]

To measure the contact resistance of our heterostructures, we used a four-point probe rather than a two-point probe. It is because this configuration eliminates the influence of the contact resistance from the probe, irrespective of whether the probe contacts are ohmic or not (i.e. Schottky type). In Four-point probe measurement, a current is passed through outside two points of the probe and the voltage is measured across the inside two points. In the voltage probes, the current is zero.

As compared to the two-probe measurement, the four-probe measurement is favorable. It is because it excludes probe contact resistance. Additionally, the resistance measurement does not depend on the size or shape of the source or drain. It is unlike conventional two-probe resistance for bulk material.

For our device [Fig. 2.14(a)], two voltage probes, A and B, were placed along a channel separating it into three segments (denoted as SA, AB, and BD) with equal lengths of 2 μm. We carefully analyzed the contribution of contact resistance to the subthreshold swing (SS). We conclude that contact resistance will only deteriorate the values of SS. For example, the $SS_{2P} = 460$ mV/dec and $SS_{4P} = 660$ mV/dec are acquired from the channel conductance and total conductance, respectively, as plotted in Figure 2.14. For a MOSFET SS can be defined as,

$$SS = \frac{k_B T}{q}(ln(10))b \tag{2.23}$$

where, k_B is the Boltzmann constant, T is the temperature in Kelvin, q is the charge of an electron

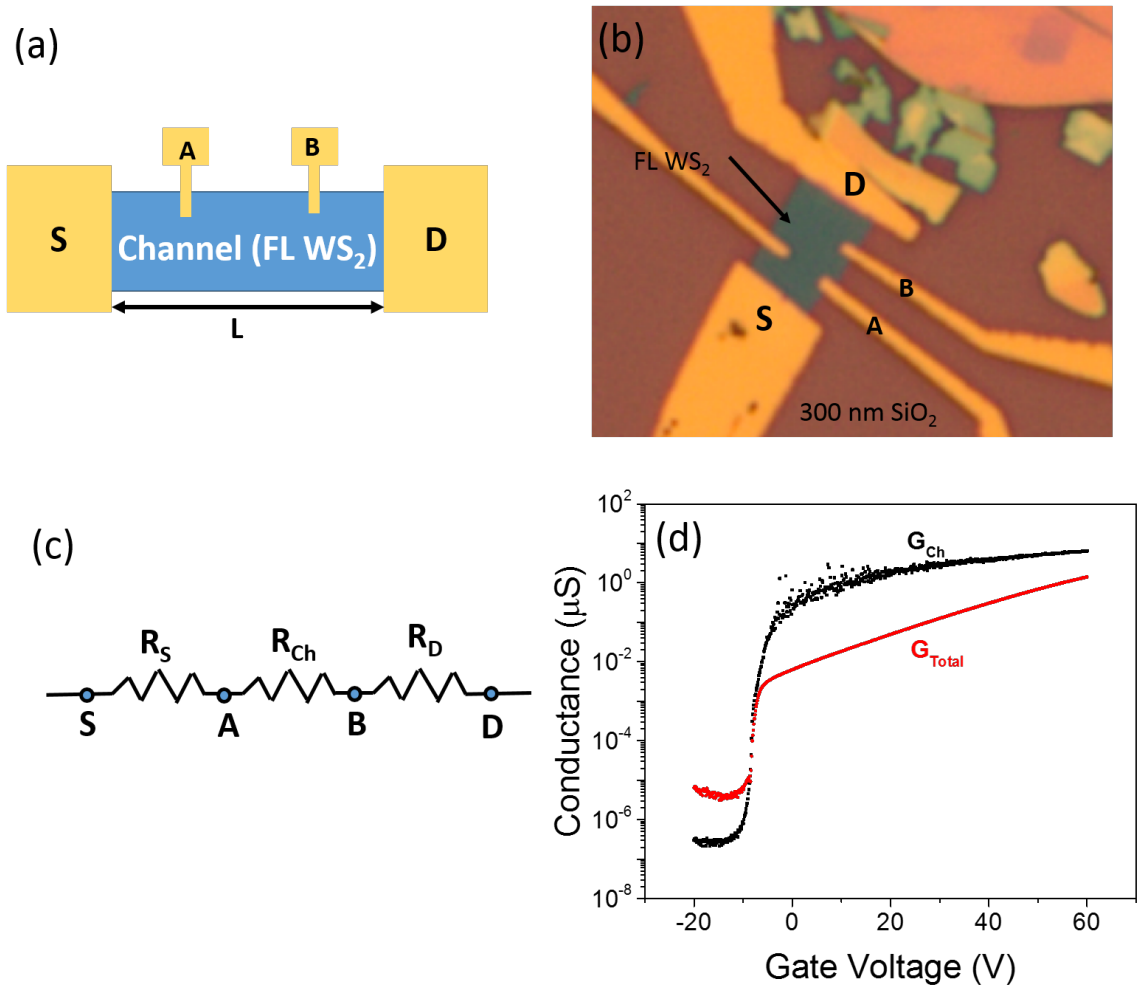

Figure 2.14: Schematic diagram of four probe measurements where S is source, D is drain, A and B are voltage probes where $I = 0$. The source is grounded. (b) Optical image of a four-probe diagram of our WS_2/300-nm SiO_2. The metal electrodes on S, D, A and B are 5/100 nm Ti/Au deposited by an electron beam evaporator. Length $L = 4.5$ μm between S and D. The distances SA, AB and BD are equidistant. (c) Equivalent resistance diagram of four probe measurements, where R_S is resistance between S and A, R_{Ch} is channel resistance means between A and B. R_D is resistance between B and D. (d) Conductance (G) versus gate voltage (V_G) for total conductance (G_{Total}) and channel conductance G_{Ch}.

and b is body factor which represents the efficiency with which the gate voltage electrostatically controls the channel region. The body factor is proportional to the change in gate voltage with a change in channel potential (ϕ_{ch}) given by:

$$n = \frac{dV_G}{d\phi_{ch}}. \tag{2.24}$$

In the best possible scenario, if the electrostatic coupling between the gate and the channel region is 100 percent effective, the body factor $b = 1$. We found that similar to earlier reports in other 2D materials, the ON-state intrinsic source or drain contact resistance (R_S or R_D) exhibited a gate-voltage dependence [Fig. 2.14(d)]. Contact resistances become nearly two orders of magnitude larger than the channel resistance, so that $V_G \sim 0$ V. They decreased faster than channel resistance as gate voltage increased. Measurements near the OFF-state suggested that channel resistance dominated in that regime resulting in very high values of R_S and R_D [Fig. 2.14(d)]. Contact resistance is originated from the interface between two dissimilar materials. Interestingly, the ON-state contact resistance did not vary much in our multilayer system, indicating that the intrinsic contact resistance was associated with electrostatic screening and interlayer resistance. Despite the significant contribution from contact resistance, intrinsic channel conductance showed nearly similar *SS* (see Fig. 2.14(d)).

2.9 Conclusion

As described in this chapter, we tested promising methods for identifying thin layers involving multiple interfaces. We also developed fabrication methods for heterostructures and demonstrated the quality of our fabricated materials, and characterized their precise composition. Further, we summarized channel length conductance distinct from device contact resistance. We addressed three main problems in 2D heterostructure materials science.

(1) We measured the thickness of two-dimensional materials[65] like graphene[1] and WS_2 by a non-invasive method to find the contrast and hence number of layered materials on given substrate

is used by the method of optical interferometry and correlating the results with the results with the number of layered materials on a given substrate. We extended this idea and used it successfully for thin layers of multiple materials and for heterostructure materials with more interfaces.

We investigated the problem of visibility of WS_2 on SiO_2/Si substrate. Using the concept of Fresnal theory, we demonstrated that the contrast is maximized at 540 nm and 630 nm on 300-nm SiO_2. However, we observed no sharp and high contrast on 200-nm or 90-nm SiO_2 substrate. We extended the Fresnal theory to account for four interfaces between air/PMMA/WS_2/SiO_2. This was crucial for identifying the thickness of flakes being prepared to transfer. We found $\sim$90-nm, 225-nm, or 375-nm thick PMMA gave maximum contrast for finding monolayer WS_2. This technique is useful to the field of 2D material identification. Theoretically, this method can be extended for any material and substrate to find a monolayer or a few layers of material.

(2) The quality of 2D materials on substrates after exfoliation, is marred by contamination from transfer processes. To create a resist-free interface we employed a method to clean transferred 2D monolayers and a method to verify the flakes on a substrate. Two important results came from h-BN thermal annealing in our conditions: (i) Annealing exfoliated h-BN on SiO_2 at 750 °C eliminated scotch tape residue from the h-BN as well as SiO_2 substrate, and (ii) We used SEM to confirm the absence of any residue. Our annealing condition and SEM imaging confirmation more reliably create residue-free materials on a substrate.

(3) In two-point probe contact resistance measurements it is difficult to separate the effect of contact resistance from total resistance. We used four-probe probe measurements to evaluate channel conductance versus total conductance. This is the first such study of G_{Total} versus G_{Ch} on semiconducting 2D TMDCs. Contact resistance became nearly two orders of magnitude larger than the channel resistance at saturation voltage. To our knowledge, these are the first such measurements on 2D TMDCs. The values $SS_{2P} = 460$ mV/decade and $SS_{4P} = 660$ mV/decade were acquired from the channel conductance and total conductance. This is by far steepest *SS* demonstrated from WS_2 fabricated on 300-nm SiO_2 substrates. Our analysis can be used to to select electrodes such that contact resistance can be minimized to improve performance of devices. Such

high performance will be helpful in creating energy efficient devices.

Chapter 3

Electrical Characteristics of Layered Materials

3.1 Motivation

Many two-dimensional (2D) materials exist in bulk form as stacks of strongly bonded layers. It is with weak van der Waals interlayer attraction. It allows exfoliation into individual, atomically thin layers. Graphene is a monolayer counterpart of graphite. It is receiving the most attention today. It is an electrical and thermal conductor.[15] It has a high carrier mobility.[12] Many other 2D materials are known such as Transition Metal Dichalcogenides (TMDCs) and h-BN show a wide range of electronic, and optical properties.[86,87] These materials have researched for decades. However, the recent resurgence in scientific community can be attributed to: (i) recent advances in sample preparation, optical detection (discussed in Chapter 2), (ii) methods for transfer of 2D materials to form heterostructures, and (iii) better understanding of electrical characteristics of 2D materials learned from graphene studies.

One use for alternative materials is in the silicon industry, where devices with steep subthreshold swings (*SS*) are required. They consume less power from lower voltages. They have reduced leakage current. Power dissipation is a big hurdle to higher levels of integration in integrated circuit

technologies. Among alternative solutions, TMDCs,[28,29] black phosphorus[30] and silicene,[31] are extensively researched on. Semiconducting TMDCs in particular are one of promising candidates in 2D layered materials. Their layered structures and sizable band gaps change from indirect band gap in multilayers to direct band gap in monolayers.

Atoms within these layers of TMDCs are bonded covalently while individual sheets are bound by vdW interactions. This unique arrangement of crystal structure promotes chemical stability. The absence of out-of-plane dangling bonds intrinsically minimizes the interlayer trap states. These characteristics allow us to assemble vdW heterostructure and achieve a steep *SS* in devices.[32] Ideally, the TMDC-based field-effect transistors (FETs) can operate as *n*- or *p*-doped material depending on the polarity of the gate voltage. They survive bending because of their flexibility.[35,36] They have advantage over silicon technology in the applications of flexible electronics and optoelectronics.

Although TMDCs have been widely studied for decades, their use as near-atomically thin materials is new. The details of electron transport in FETs made with these layered materials as channels are not widely researched yet. This chapter aims to introduce all the essential capacitances in layered materials to formulate the effects of the quantum capacitance (described in Section 3.7) related to density of states (*SS*) in these layers and to further describe electron transport in these materials.

3.2 Band Structure and Density of States of TMDCs

3.2.1 Band Structure

A single layer WS_2 contains a layer of *W* atoms with 6-fold coordination symmetry. The *W* atoms are hexagonally packed between two trigonal atomic layers of *S* atoms. The 2H-WS_2 polytype crystalline structure has the hexagonal space group. It has lattice parameters of $a = 3.1532$ Å and $c = 12.323$ Å.[88]

Bulk WS_2 is an indirect-gap semiconductor with band gap of 1.3 eV. The electronic states in-

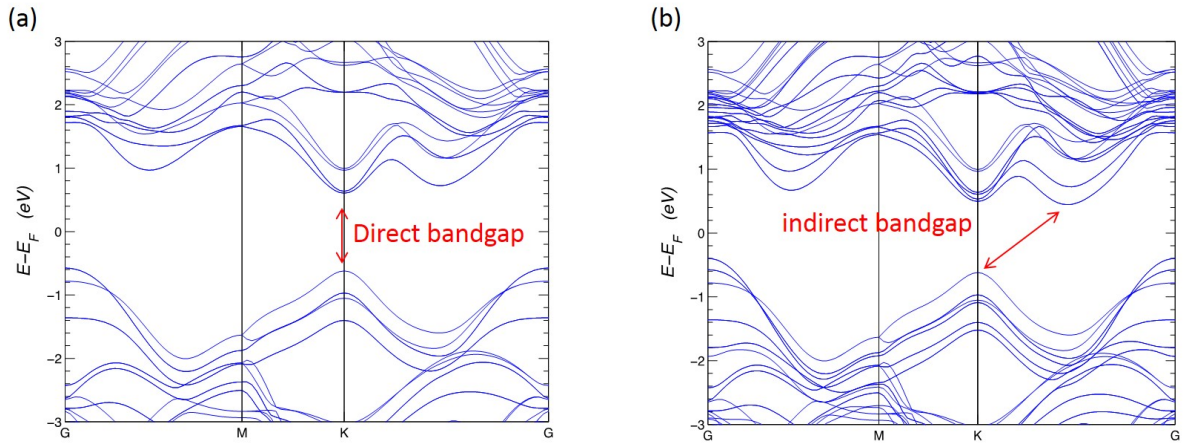

Figure 3.1: Band structures calculated from first-principles density functional theory for (a) monolayer, and (b) multilayer WS_2. The arrows indicate whether the fundamental band gap is direct or indirect. Our collaborator Marcelo A. Kuroda from the Auburn University did the calculations and plotted.

volved in the indirect transition (i.e., the valence band maximum at Γ and the conduction band minimum at Γ). It originate from linear combinations of tungsten d-orbitals and sulfur p_z-orbitals. A strong interlayer coupling exist between electronic states. Their dispersion depends on the number of layers. As the number of WS_2 layers decreased, it transitioned from indirect gap (in bulk) to direct gap (in a monolayer), as shown in Fig. 3.1. For a monolayer, the indirect gap between these states was larger than the direct transition at K. Thus, it makes the material a direct band gap semiconductor Fig. 3.1. The conduction and valence states at K are mainly due to tungsten d-orbitals. Their energies are not very sensitive to the number of WS_2 layers. We found the experimental direct band gap at the K point was ~ 2.05 eV (in our monolayer WS_2).

3.2.2 Density of States

We can model a semiconductor as an infinite quantum well (2D) with sides of length (a). Electrons of mass m^* are confined in the well. The time independent Schroedinger equation of electron moving in one direction with energy E is given by,

$$\left(-\frac{\hbar^2}{2m}\nabla^2 \right) \psi(x) + V(x)\psi(x) = E\psi(x), \tag{3.1}$$

and it can be modified when a particle move with zero potential energy $V(x) = 0$, resulting in quantum mechanical description of free motion in one dimension. It can thus, be written as,

$$\left(-\frac{\hbar^2}{2m}\nabla^2 \right) \psi(x) = E\psi(x). \tag{3.2}$$

The general solution of above equation can be written as,

$$\psi(x) = A\,sin(kx) + B\,cos(kx), \tag{3.3}$$

where A, B, and k are constants. We can use boundary conditions to find particular solution to system. By boundary condition, probability to find particle at $x = 0$ or $x = a$ is zero. The physically acceptable solution requires wave function to be continuous, vanish outside the interval, [0, a], and to be normalized. By solving the Schreodinger equation, wave vector (k) is given by,

$$k = \sqrt{\frac{2mE}{\hbar^2}}, \tag{3.4}$$

the wave function (ψ) is given by,

$$\psi(x,y) = \sqrt{\frac{2}{a}}\, sin\frac{n_x \pi x}{a}, \tag{3.5}$$

the allowable energies given by,

$$E = \frac{n^2 h^2}{8m^* a^2} = \frac{\hbar^2 k^2}{2m^*}, \tag{3.6}$$

here, the energy of a particle is quantized and lowest possible energy is not zero.

Similarly, in two-dimension wave function is given by,

$$\psi(x,y) = \frac{2}{a}\, sin\frac{n_x \pi x}{a}\, sin\frac{n_y \pi y}{a} \tag{3.7}$$

with corresponding energies,

$$E = \frac{n^2 h^2}{8m^* a^2} = \frac{\hbar^2 k^2}{2m^*}, \tag{3.8}$$

where, $n^2 = n_x^2 + n_y^2$ and $k^2 = k_x^2 + k_y^2$. The density of states $D(E)$ function describes the number of states that are available in a system and was essential for determining the carrier concentrations and energy distributions of carriers within a semiconductor. Density of states for two-dimensional materials $D(E)$ is given by,

$$D(E) = x^2 \frac{g_c m_c^*}{2\pi\hbar^2}, \tag{3.9}$$

where, the constants g and m^* are the degeneracy and effective masses of the valence (v) and conduction (c) bands. It is significant that the 2D density of states does not depend on energy. Immediately, as the top of the energy-gap is reached, there is a significant number of available states.

Assuming parabolic valence and conduction bands, the density of states in 2D is constant above the conduction and below the valence band edges [Fig. 3.8.1(a)]. It is separated by the band gap E_g. The net carrier density (in terms of electron charge) can be obtained analytically from the Fermi-Dirac distribution. Contribution of electrons in carrier density can be written as,

$$n_e = \int_{E_c}^{\infty} D(E)\, f(E) dE \tag{3.10}$$

where, $f(E)$ is the Fermi function and $D(E)$ is Density of states. The Fermi function $f(E)$ is given by,

$$f(E-\mu) = \frac{1}{1 + e^{(E-\mu)/k_B T}} \tag{3.11}$$

which is, 1 for energies far below electrochemical potential (μ) and 0 for energies far above μ. If the source and drain regions are coupled to the channel (with V_D held at zero), then electrons will flow in and out of the device. It will bring them all in equilibrium with a common electrochemical potential μ just as two materials in equilibrium acquire a common temperature.

Using Equation 3.9 in Equation 3.10, we get,

$$n_e = \int_{E_c=\frac{E_g}{2}}^{\infty} x^2 \frac{g_c m_c^*}{2\pi\hbar^2} \frac{1}{1+e^{\frac{E-\mu}{k_B T}}} dE \tag{3.12}$$

$$= \frac{g_c m_c^*}{2\pi\hbar^2} k_B T \ln\left(\frac{1}{1+e^{\frac{E-\mu}{k_B T}}}\right). \tag{3.13}$$

Contribution of holes in carrier density is given by,

$$n_p = \int_{-\infty}^{E_v} D(E)(1-f(E))\, dE \tag{3.14}$$

$$= \int_{-\infty}^{E_v=-\frac{E_g}{2}} x^2 \frac{g_c m_c^*}{2\pi\hbar^2} \frac{1}{1+e^{\frac{E-\mu}{k_B T}}} dE \tag{3.15}$$

$$= \frac{g_v m_v^*}{2\pi\hbar^2} k_B T \ln\left(\frac{1}{1+e^{-\frac{E+\mu}{k_B T}}}\right). \tag{3.16}$$

Net carrier density is given by,

$$n(\varepsilon_f = \mu) = n_e + n_p \tag{3.17}$$

$$= \frac{g_c m_c^*}{2\pi\hbar^2} k_B T \ln\left(\frac{1}{1+e^{\frac{E-\mu}{k_B T}}}\right) + \frac{g_v m_v^*}{2\pi\hbar^2} k_B T \ln\left(\frac{1}{1+e^{-\frac{E+\mu}{k_B T}}}\right) \tag{3.18}$$

where, k_B and $\hbar$ are Boltzmann's and the reduced Planck constants, respectively. The first and second terms on the right-hand side of Eq. 3.18 correspond to the contributions from electrons and holes, respectively. We use the center of the band gap as energy reference.

3.3 Device Fabrication

Our WS_2 flakes were mechanically exfoliated from bulk synthetic WS_2. The WS_2 crystals were supplied by *2DSemiconductors* on a highly doped silicon wafer covered with 300-nm of silicon dioxide with adhesive tape. The adhesive tape glue was removed by putting exfoliated samples in acetone for 30 minutes at 50 °C followed by an Isopropyl alcohol (IPA) rinse and nitrogen blow

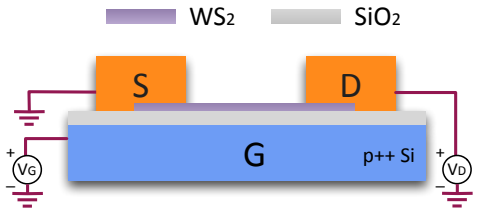

Figure 3.2: Schematic of WS_2 Field-Effect Transistor: Source (S), through which the carriers enter the channel; Drain (D), through which the carriers leave the channel; Gate (G), the terminal that modulates the channel conductivity; WS_2 acts as channel material in the diagram.

dry. Samples were later placed in a quartz tube in a furnace at a base pressure of 3 Torr with a mixture of 10 sccm of H_2 and 100 sccm of Ar flowing at 220 °C for 3.5 hours. Monolayer flakes were identified by optical contrast and later confirmed by photoluminescence (PL) measurements. The thickness of FL and bulk WS_2 were measured by atomic force microscope (AFM) as well as optical contrast for flakes less than 5 layers.

All devices are sufficiently long to prevent the short channel effect and measurements were made in high vacuum at 300 K. The typical device schematic is depicted in Figure a. Source (S) and drain (D) electrodes of all devices presented herein are defined by electron beam lithography and consist of a Ti/Au (5-nm/70-nm) metal stack. Moreover, the drain voltage (V_D) and the back-gate voltage (V_G) were applied with respect to the grounded source voltage (V_S). The carrier density in the channel will be modulated by V_G via electrostatic coupling similar to the operation of FETs.

The metal deposition of Ti/Au: 5-nm/70-nm, was performed to make S and D electrodes after e-beam lithography. These devices were annealed in high vacuum of 2×10^{-6} Torr for four hours at 400 K in a commercial (Agilent's) probe station. Later, they were cooled down overnight to room temperature prior any electrical measurement. Electrical characterization was of devices were done by the standard steady-state current-voltage measurement. We used an Agilent B1500A Semiconductor Device Parameter Analyzer. Both source and drain SMUs are HRSMUs in this analyzer have minimum 1 fA measurement resolution while gate SMU is MPSMU with minimum 10 fA measurement resolution.

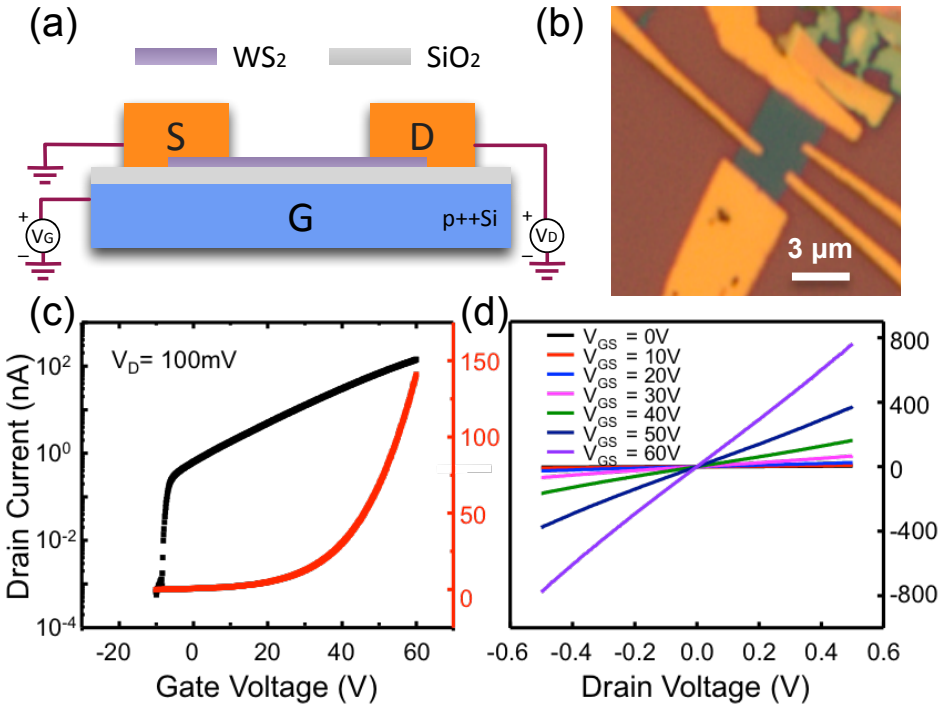

Figure 3.3: (a) Device Schematic, (b) optical image of FL WS_2 transistor (Device 1), (c) the current versus gate voltage curves of a FL WS_2 transistor (Device 2 with trapezoid shape, $L = 6$ μm and $W_{ave} = 2.7$ μm) at drain bias as 100 mV in both linear (right) and logarithmic (left) scales, and (d) the current versus drain voltage curves.

3.4 Electrical Characterization of Few Layer WS_2 Field Effect Transistors

An optical image of a few-layered (FL) WS_2 device with additional voltage probes is shown in Fig. 3.3, and the shapes of our flakes are chosen to have defined crystalline edges. The I-V_G characteristic curves of this WS_2 device is shown in Fig. 3.3(c). It exhibits an n-type semiconductor behavior with a 10^6 current ON-OFF ratio, and negligible hysteresis. Moreover, its I-V_D characteristic curves are shown in Fig. 3.3(d), and at low drain bias, the device appears to have approximately symmetric Ohmic contacts, similar to the previous report after vacuum annealing.

Interestingly, it yields a SS of 440 mV/dec, by far the sharpest demonstrated from WS_2 fabricated on 300-nm SiO_2 substrates. To the extent of our knowledge, there are only few studies on WS_2 transistors made by exfoliated single crystals.[89] In literature, an ambipolar ionic liquid-gated

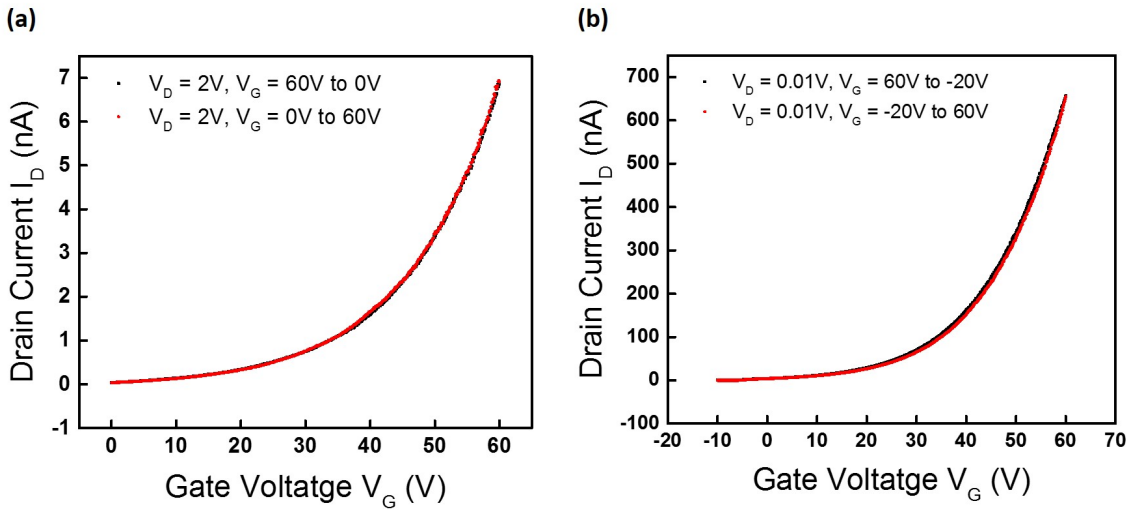

Figure 3.4: Hysteresis of (a) monolayer WS_2, and (b) few-layer WS_2 FETs.

WS_2 FETs with subthreshold voltage swings of 90 mV/decade was achieved, with the electron mobility $\mu_e = 20$ cm^2/V sec at carrier density $n_e = 10^{14}$ cm^{-2}.[89] It is close to the ultimate room-temperature value of 60 mV/decade. However, the double-layer capacitance of ionic liquid gate is approximately three orders of magnitude larger than that of a 300-nm SiO_2 substrate that we used here. We further perform four-terminal measurements to isolate the contribution from the contact resistance.

The reliability of atomically thin WS_2 devices for FETs is important for scientific community. It can be very sensitive to external chemical environment and illumination conditions. However, such effects are undesirable for WS_2-based FETs. It is related to electronic device architecture. It needs to be minimized in order to improve the device stability. In our experiment we performed hysteresis for both the monolayer and few layer WS_2 and they show no significant hysteresis as seen in Fig. 3.4

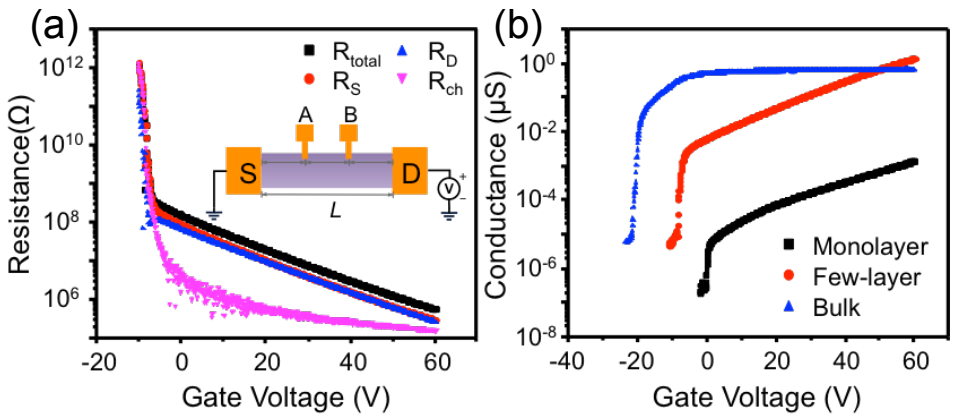

Figure 3.5: Resistance of a FL WS_2 (Device 2) versus gate voltage as obtained from four-terminal measurement: R_{total}, R_S, R_D and R_{ch} are the total, source contact, drain contact and channel resistances, respectively. Inset: schematic of device configuration with contacts (S and D) and voltage probes (A and B). (b) Conductance on Monolayer ($L = 1.8$ μm, $W = 2.3$ μm), few-layered with trapezoid shape ($L = 6$ μm, $W_{ave} = 2.7$ μm) and 40-nm thick WS_2 devices ($L = 4.1$ μm, $W = 10$ μm). Because the contact resistances may differ in various channel thicknesses, here we only focus on their SS and threshold voltages but not their relative conductivity.

3.5 Gate -Voltage Dependent Contact Resistance of Few Layer WS_2 FET

The total resistance of FET is defined as $R_{total} = R_S + R_{ch} + R_D$, where R_{ch} is the entire channel resistance (i.e. WS_2.) and R_S (R_D) is the contact resistance from source (drain) contact. As shown in our device geometry shown in the inset of Fig. 3.5, two voltage probes, A and B, were placed along the channel separating it into three segments (denoted as SA, AB, and BD) with equal lengths of 2 μm. The contact resistances, R_S and R_D, are extracted. After carefully analyzing the contribution of contact resistance to the SS, we conclude that contact resistance will only deteriorate the values of SS. For example, the $SS_{2P} = 460$ mV/dec and $SS_{4P} = 660$ mV/dec are acquired from the channel conductance and total conductance, respectively, as plotted in Fig. 3.5(b).

Furthermore, we find that similar to the earlier reports in other 2D materials, the ON-state intrinsic source (drain) contact resistance R_S (R_D) exhibits a gate-voltage dependence playing a major role. Contact resistances become nearly two orders of magnitude larger than the channel resistance e.g. $V_G \sim 0$ V and they decrease faster than channel resistance does as gate voltage

increases. Measurements near the OFF-state suggest that channel resistance dominates in that regime. It results in the abnormally high value of R_S and R_D in the Fig. 3.5. It is because this contact resistance is intrinsically originated from the interface between two dissimilar materials. Interestingly, the ON-state contact resistance did not vary much in a thick multilayer system (the blue curve in Fig. 3.5(b)). It indicates the intrinsic contact resistance is associated to electrostatic screening and interlayer resistance. Further investigations are ongoing into this gate-dependent phenomenon, and will not be discussed here in details. Despite the significant contribution from contact resistance, intrinsic channel conductance shows nearly similar *SS* in Fig. 3.5(a).

3.5.1 Thickness Independent Subthreshold Slope *SS*

Our entire set of WS_2 devices are made under the exact fabrication process and on same substrate with various WS_2 thicknesses. The thickness ranging from monolayer, few-layered to bulk- show very comparable values of *SS* from 450 to 670 mV/dec. To understand this nearly thickness-independent *SS* behavior, we come to realize that our samples have little defects and impurities. It is unlike the case of MoS_2, and our WS_2 devices reaches a low interface trap density. If a single crystal has a constant volume density of intrinsic defects or impurities, the total surface trap density will depend on the thickness of the materials. To an extreme degree, both our bulk and monolayer devices display similar values of *SS*. It justifies that we have a high-quality WS_2 single crystal to begin with. Hence, we reason that most localized traps reside at the interface between the bottom layer of WS_2 and the SiO_2. As we show later, the *SS* of a FET (i.e. when the carrier density is low) is governed by the ratio of the interface trap capacitance to the oxide capacitance. In this work we approach two extreme cases with different thickness of oxide on purpose. The thin oxide is employed to demonstrate the feasibility of achieving the theoretical limit of *SS* by a simple back-gate FETs while the thick oxide is used to roughly quantify the interface trap density.

3.5.2 Thickness Dependence of Threshold Voltage

The threshold voltage (V_{th}) of a field-effect transistor (FET) is the minimum gate to source voltage that is needed to create a conducting path between *S* and *D*. The material parameters that effect V_{th} include (i) the gate conductor material, (ii) the gate insulation material (SiO_2), (iii) The thickness of the gate material, and (iv) the channel doping concentration. In Figure 3.5(b), as the thickness increases from monolayer, to few-layers to bulk of WS_2, more negative value of gate voltage V_G is needed. We attribute the thickness-dependent threshold voltage to the inefficient depletion of the top most layers with the inevitable metal doping.

3.6 Capacitive Network Modelling in Layered Materials

To model this 2D multilayer system, we consider that the system behaves like a capacitor network Fig. 3.7(b) consisting of the oxide capacitance (C_{ox}), the interface trap capacitance (C_{it}), the layer quantum capacitance (C_α with $\alpha = 1$ to N), and the interlayer capacitance (C_{il}). The oxide and interlayer capacitances are described by the classical capacitance i.e. $C_{ox} = \varepsilon_{ox} \,/\, d_{ox} = 11.5$ nF/cm^2 with $d_{ox} \sim$ 300-nm SiO_2 and $C_{il} = \varepsilon_0 \,/\, d_{il} = 1433$ nF/cm^2 with $d_{il} \sim 0.618$ nm for WS_2. The capacitance of the interface traps and TDMC layers are expressed in terms of the quantum capacitance of the system and C_α can vary from layer to layer due to differences in the local electrostatic potential as we describe next.

3.7 Quantum Capacitance

A pair of conductors (metals), separated by an insulating material forms simplest type of capacitor. Capacitors store separated equal and opposite charges. In their most common form, capacitors are made from two conductors with charge $+q$ on one metal and charge $-q$ on the other. The potential difference ($\Delta V_{geometric}$) between metals is linearly dependent on charge q; that is, $q \propto \Delta V_{geometric}$. The density of states in metals is essentially infinite. Thus, if we double the charge, we double

the potential difference between the two metals, so that the ratio of q to $\Delta V_{geometric}$ is constant. This constant ratio $q/\Delta V_{geometric}$, can be called as the geometric capacitance $C_{geometric}$. The name $C_{geometric}$ is given here, because, it depends on shape and geometry of the two conductors of the capacitor, and on the material between the metals.

The most basic two parallel plate capacitor is shown in Fig. 3.6(a). It consists of metal/dielectric/metal geometry with metals of area A, separated by distance d, with charges $+q$ and $-q$ respectively, distributed uniformly over the plates. If dimensions of plate are large compared with d, then the electric field between plates is to a very good approximation constant. The field between the plates has magnitude, $E_{geometric} = \sigma_{geometric}/\varepsilon$, where $\sigma_{geometric}$ is charge density q/A and ε permittivity of material. The capacitance of this two parallel plate capacitor is given by, $C_{geometric} = q/\Delta V_{geometric} = \varepsilon A/d$, is a constant value.

If we replace one or both of metal plates from Fig. 3.6 (a) with a semiconductor, resultant configuration will be either semiconductor/dielectric/semiconductor, or semiconductor/dielectric/metal, as shown in Fig. 3.6 (b). Unlike geometric capacitance, the potential difference between plates, where one of plates is semiconductor, is no longer linearly dependent on charge. As negative charge on semiconductor plate capacitor changes, electrons in higher energy states in the band structure starts filling in. So, the potential difference changes at different rate than the $V_{geometric}$. In such situation, where one or both plates are semiconductor (with low density of states (ρ)), electron band (U_b) effect needs to be considered (effect of band filling energy is discussed later in this section in modeling charge transport in 2D layered materials). This band filling effect acts as if there is second capacitor in series. This second capacitance is called quantum capacitance. The word "quantum" comes in this capacitance, as it is related to energy of an electron in quantum wave function of an electron.

To measure electronic devices, voltmeter does not measure total electric potential. Instead, it measures fermi level (μ) difference. The fermi level is a thermodynamic quantity, that measures amount of work required to add one electron to system. So, the observed difference by voltmeter

between two points A and B, is given by,

$$\Delta V = V_A - V_B = -\frac{\mu_A - \mu_B}{e}. \tag{3.19}$$

The electron moves from high μ (low voltage) to low voltage μ (high voltage), till electronic circuit is in thermodynamic equilibrium, that is, μ is constant throughout its connected parts. The fermi level difference is total free energy, that includes electric potential energy as well as other forces on electrons. In Fig. 3.6 (a), geometric capacitance is given by, $C_{geometric} = q/\Delta V_{geometric}$. Also, quantum capacitance is given by, $C_{quantum} = q/\Delta V_{quantum} = \rho e^2$, where $\Delta V_{quantum} = \Delta\mu_{chemical}/e$. The total capacitance is equivalent to these two capacitors in series. When two capacitors are arranged in series, the total capacitor is given by the reciprocal of $C_{geometric}$ and $C_{quantum}$, and this capacitance is less than any of these individual capacitances. Since, $C_{quantum}$ is directly proportional to density of states, quantum capacitance dominates in low-density-of-states materials.

In Fig. 3.6 (c), three-plate metal/dielectric/2D-electron-gas/dielectric/metal configuration is shown to further understand quantum capacitance. The quantum capacitance is property of a 2D Fermi system, whereas, classical parallel plate capacitance depends on electric field that penetrates through insulator between metal electrodes. The quantum capacitance can also be explained by three-plate capacitor. The charge on plate 1 induces charge on plate 2, which penetrates through 2D metal plate Q. The individual capacitances of Fig. 3.6 (c) can be given by,

$$C_1 = \frac{\varepsilon_1}{4\pi d_1}, \tag{3.20}$$

$$C_2 = \frac{\varepsilon_2}{4\pi d_2}, \tag{3.21}$$

and

$$C_Q = \frac{g_v m e^2}{\pi\hbar^2}, \tag{3.22}$$

where, C_1, C_2 and C_Q are capacitance at node 1, node 2 and quantum capacitances at plate Q respectively. The effective charge mass is m and g_v is the valley degeneracy factor. The Eq. 3.22

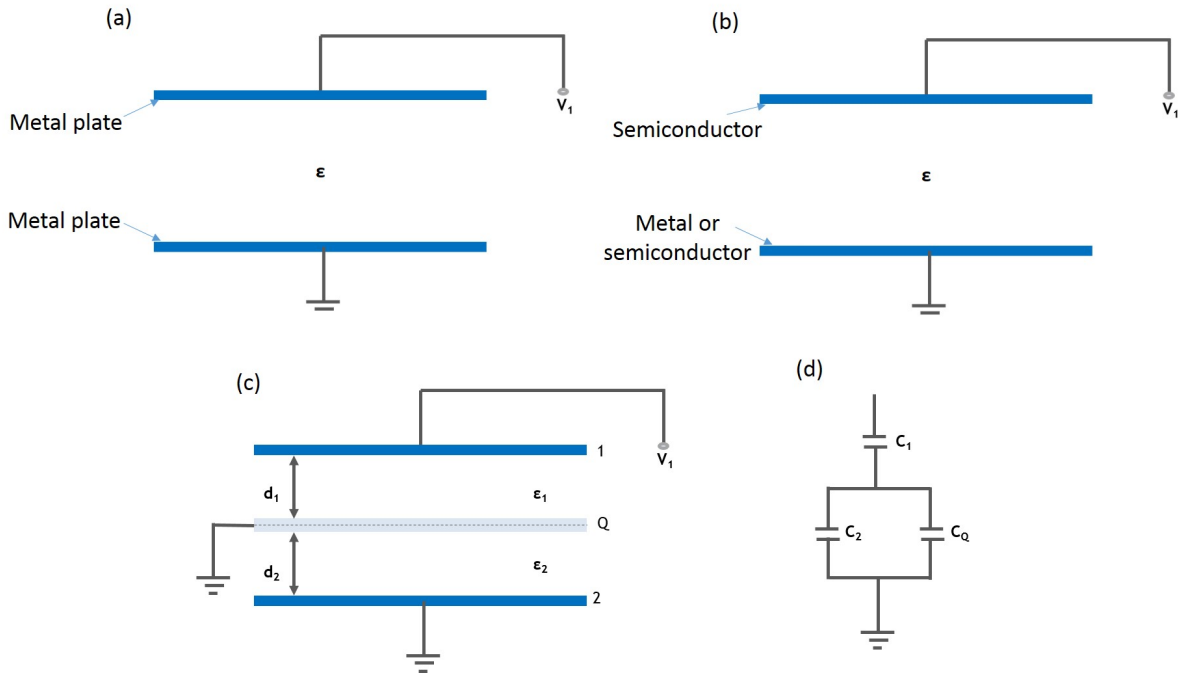

Figure 3.6: (a) Parallel plate capacitor with metal/dielectric/metal configuration. $C_{geometric}$ dominates in this geometry, (b) semiconductor/dielectric/semiconductor or semiconductor/dielectric/metal capacitor configuration. $C_{quantum}$ dominates in this configuration, (c) Three plate capacitor, where middle plate is a 2D metal. The dielectric materials with permittivity of ε_1 and ε_2 are filled in this three plate capacitor as shown,[2] and (d) Corresponding equivalent circuit diagram of three plate capacitor is shown.

is quantum capacitance in three-plate capacitor. However, in 2D layered system, as described with detail in our theoretical work on 2D layered materials [Eq. 3.26], quantum capacitance depends on the position of the Fermi level relative to the band edges of individual layers in FETs.

The σ_1, σ_1, and σ_Q are charge densities on plates 1, 2 and quantum well Q respectively [Fig. 3.6(c)]. The charge neutrality condition,

$$\sigma_1 + \sigma_2 + \sigma_Q = 0, \tag{3.23}$$

is met in equivalent circuit [Fig. 3.6 (d)]. The detailed analysis has been done in literature.[2,90]

The quantum capacitance (C_Q) is directly proportional to the $D(E)$ of a material. The $D(E)$ of 2D layered materials is already explained in Section 3.2.2 of this dissertation. Quantum capacitance is important for low $D(E)$ systems.[91] The low value of $D(E)$ results in low quantum

capacitance. So, for small capacitance, conductance is low and the entire voltage appears across C_Q, as it can be deduced from equivalent circuit diagram of capacitances in Fig. 3.6 (d). In a 2D electronic system in a semiconductor surface or interface, the quantum capacitance is very important, as they have low $D(E)$. This three-plate capacitor shows interaction of two capacitors with each other in metal/2D-gas/metal configuration.

Discussing our case of 2D layered materials [Fig. 3.7(a)], in the presence of a local electrostatic potential ϕ_α at layer α, the Fermi level shifts to,

$$\varepsilon_{F,\alpha} = \varepsilon_F^0 + q\phi_\alpha, \tag{3.24}$$

which result in band bending (re-position to the global Fermi level) and is the isolated intrinsic the Fermi level of the layer. We can then define the quantum capacitance of the layer α as ,

$$C_\alpha = q\frac{dn_\alpha}{d\phi_\alpha} = q^2\frac{dn_\alpha}{d\varepsilon_{F,\alpha}}, \tag{3.25}$$

and by using Eq. (4.5) in Eq. (4.6), layer quantum capacitance is given by:

$$C_\alpha = C_0\left(\frac{g_c\frac{m_c^*}{m_e}}{1+e^{\frac{E_g-2\varepsilon_F}{2k_BT}}} + \frac{g_v\frac{m_v^*}{m_e}}{1+e^{\frac{E_g+2\varepsilon_F}{2k_BT}}}\right) \tag{3.26}$$

$$where, C_0 = \frac{e^2 m_e}{2\pi\hbar^2} = 33.5\,\mu F cm^{-2} \tag{3.27}$$

where, $m_C{}^*$ ($m_v{}^*$) is the conduction (valence) band effective mass and m_e is the free-electron mass. Note that this constant is considerably large compared to typical oxide capacitances. However, the actual quantum capacitance of an individual layer [Eq. 3.28] can differ significantly from the value of C_0. It depends on the position of the Fermi level relative to the band edges. In addition to the charge carriers among layers, the interface traps also play a role in the effective capacitance of the system. However, these charges do not necessarily participate in transport. In our WS_2 system we model them as a fixed step-like defect level. The density can be expressed (in term of electron

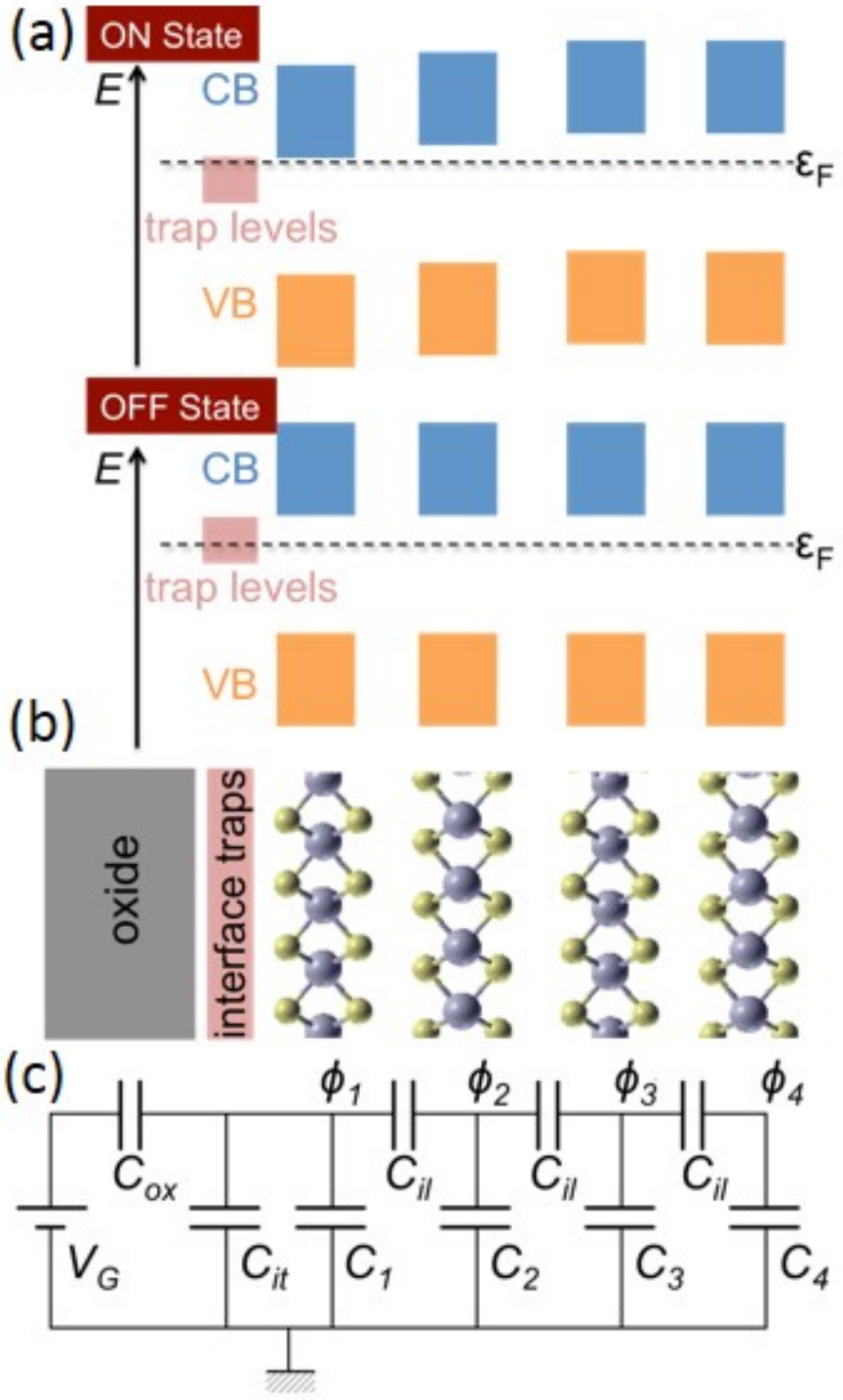

Figure 3.7: Model of a four-layer TMDC system. (a) the density of states (*DOS*) of individual layers and interface traps in the multilayer structure near OFF-state, *DOS* of all four layers are at same level; the *DOS* of individual layers and interface traps in the multilayer structure near ON-state, the layer closest to gate turns ON first where, ε_F is the Fermi level, a stack consisting of the oxide (SiO_2), traps at the interface between the oxide and the TMDC, and a four-layer TMDC. (c) Equivalent capacitor network includes oxide C_{ox}, interface trap C_{it}, TMDC's layer C_α with $\alpha = 1$ to 4 and the interlayer (C_{il}) capacitances.

charge) as,

$$n_{it} = n_{it}^{0} \frac{k_B T}{\delta \varepsilon_{it}} \ln(1 + e^{\frac{\varepsilon_F - \varepsilon_{it} - \delta\varepsilon_{it}/2}{k_B T}}) - \ln(1 + e^{\frac{\varepsilon_F - \varepsilon_{it} + \delta\varepsilon_{it}/2}{k_B T}}) \tag{3.28}$$

where, n_{it}^{0}, ε_{it}, and $\delta\varepsilon_{it}$ are the interface trap density, energy level, and width, respectively, and

$$n_{it} = n_{it}^{0} \frac{k_B T}{\delta \varepsilon_{it}} \ln\left(\frac{1 + e^{\frac{\varepsilon_F - \varepsilon_{it} - \delta\varepsilon_{it}/2}{k_B T}}}{1 + e^{\frac{\varepsilon_F - \varepsilon_{it} + \delta\varepsilon_{it}/2}{k_B T}}}\right). \tag{3.29}$$

The quantum capacitance of these trap states can be obtained by the method similarly to the case of the TMDCs [Eq. 4.7]. The transconductance of the system is modeled by assuming that the localized-trap states do not participate in transport. The mobility in each layer is the same and independent of carrier density is assumed. Due to low interface trap density, we omit scattering by Coulomb impurities that degrades mobility in ultra thin TMDCs.[92] The curve fitting for the transfer characteristic of a WS_2 device in the full range (both below and above the threshold for the electron conduction branch) is obtained. The curve fitting is obtained by using number of WS_2 layers to be $N = 4$, and an effective electron mass of approximately 0.3 m_e from first-principles calculations.

We acquire the best-fit parameters in the full range of electron conduction, i.e., the trap density $\approx 6 \times 10^{11}$ cm^{-2} spread over a width ≈ 0.2 eV residing at ~ 0.12 eV from the bottom of the conduction band. These values are in agreement with the thermally activated energy found in WS_2. It must be pointed out that this approach is valid to solely model the channel conduction. In other words, contact resistance is not being included and if dominates, the applicability of this model could be limited only in the ON-state.

A potential difference V_G between the gate and FL WS_2 induces a two dimensional charge density, $Q_0 = CV_G$ at the gate. All the layers of the FL WS_2 are in equilibrium, so they share the same fermi level. In a layered structure charges carriers distribute themselves to minimize the total energy, $U = U_{el} + U_b$. It consists of two competing effects: the electrostatic interaction between layers (U_{el}) and the band-filling energy (U_b). The former tends to converge charges as close to

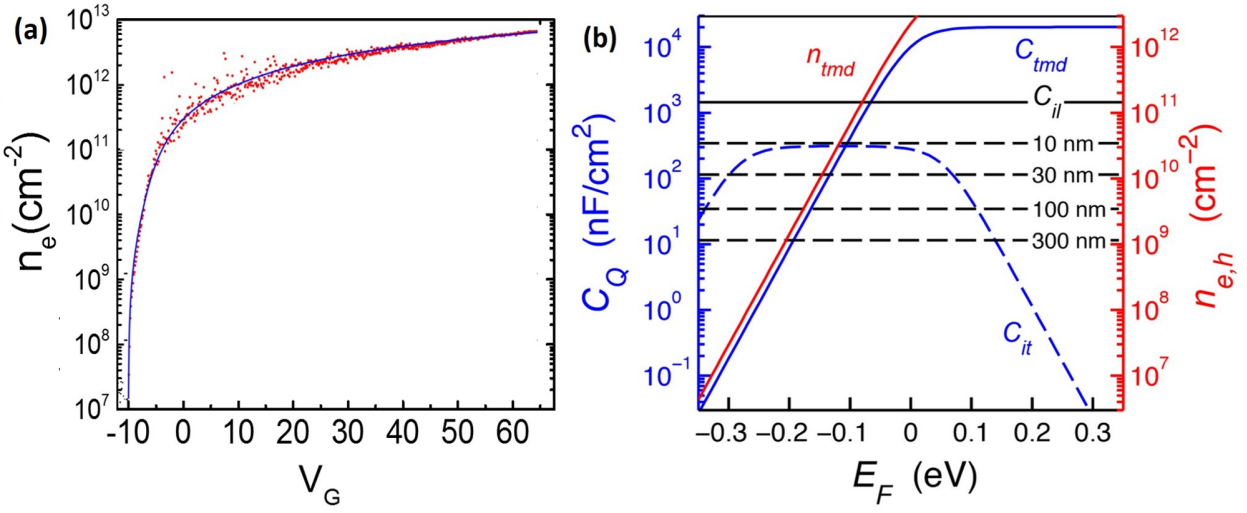

Figure 3.8: Model of a four-layer TMDC system. (a) Comparison of carrier density estimated from channel resistance (R_{ch}) shown in Figure (dots) and model (solid line), (b) Total carrier density (n_{tmd}) in WS_2 and calculated gate dependent quantum capacitances (C_{tmd}, and C_{it}) in this multilayer system. As reference oxide capacitances for different thicknesses (SiO_2: 10, 30, 100, and 300-nm) and C_{il} are plotted.

the gate as possible while the latter tends to spread charges across different layers. As charges are located at a thin plane, the electric field in between planes is constant and U_{el} is given by,

$$U_{el} = \frac{d_0}{2\varepsilon_0}\Sigma_{i=1}^{n-1}(Q_0 - Q_i)^2 \tag{3.30}$$

where ε_0 is the vacuum permittivity and $Q_i = \Sigma_{j=1}^{i} q_j$ is the cumulative charge up to ith layer.

We note that (i) the band position α relative to Fermi level of each layer can vary by the carrier density due to the quantum capacitance. The conduction edge of the bottom layer is close to the energy level of the interface traps, (ii) in the low charge-density limit in the TMDC, charge carriers tend to distribute uniformly and the band energy position of each layer will be the same. Thus, with the decrease of the gate voltage (to the negative side), all layers will be turned off simultaneously, and (iii) In the high charge-density limit, the charges carriers tend to accumulate in layers near the gate and the band energy position of each layer will be altered according to their quantum capacitance (i.e. carrier density).

The Fig. 3.8 (b) shows the quantitative comparison among all the capacitances, C_{tmd}, C_{il}, and

C_{it}. It is shown as function of the Fermi level (reference to the conduction band edge) in addition to the SiO_2 capacitances (of 300, 100, 30 and 10-nm thickness). Based on the amount of charges in the TMDC, we identify three operational regimes. First, when the device is off (Fermi level is far from the conduction band edge), the quantum capacitance will be the smallest ($C_\alpha \ll C_{ox} \sim C_{it} \ll C_{il}$). Next, as the gate voltage increases the quantum capacitances will also increase and eventually become comparable to those of the oxide or the interface trap density ($C_\alpha \sim C_{ox} \sim C_{it} \ll C_{il}$). It is dependent on the geometry and sample quality, respectively. Because C_{il} is much larger than any other capacitance, all the individual layers can be approximated to have the same local electrostatic potential. With the further increase of the Fermi level position, the device will be turned on, e.g. charge density is in the order of 10^{11} cm^{-2}. Above this point, the interlayer capacitance cannot be omitted and the Fermi level resides very close to the conduction band edges.

3.8 Subthreshold Slope (*SS*) of TMDCs Field-Effect Transistors

3.8.1 Modeling of *SS*

To consider the full range of transport characteristic, we define the reciprocal value of the change of logarithmic conductivity versus grate voltage in TDMC-based FETs as,

$$S = log(10)\frac{dV_G}{d(\log\sigma)}. \tag{3.31}$$

This *S* equation simply represents the change in gate voltage needed to obtain an order of magnitude increase in conductivity. However, it is conventionally known in the sub threshold region and called *SS* below the threshold voltage. Because the contribution from interlayer capacitances (C_{il}) can be neglected along with the assumption of constant mobility in each layer $\sigma = n\,e\,\mu$, thus we

have,

$$SS = log(10)\frac{dV_G}{d(logn_{tmds})}, \tag{3.32}$$

and for a MOSFET it can be defined to be

$$SS = \frac{k_B T}{q}(ln(10))b \tag{3.33}$$

where k_B is the Boltzmann constant, T is the temperature in Kelvin, q is the charge of an electron and b is body factor which represents the efficiency with which the gate voltage electrostatically controls the channel region. The body factor is proportional to the change in gate voltage with a change in channel potential (ϕ_{ch}) as given by:

$$n = \frac{dV_G}{d\phi_{ch}}. \tag{3.34}$$

In the best possible case, if the electrostatic coupling between the gate and the channel region is 100 percent effective, then body factor $b = 1$. Plugging $b = 1$ and using Equation 3.34 in 3.33, we get,

$$SS = \frac{k_B T}{q}(ln(10))(1) = 59.6\, mV/decade \tag{3.35}$$

which is the fundamental limit of achieving SS at room temperature of a MOSFET. Due to thermodynamic reasons, it is not possible to reduce SS below 59.6 mV/decade. However, this limit can be breached using quantum-tunneling effects and with ferroelectric gate materials. In two-dimensional materials, the carrier densities are non-degenerate and the each layer approximately has the same electrostatic potential $\phi_\alpha \sim \phi_1$ as we discussed earlier, so,

$$\frac{d(logn_{tmds})}{dV_G} \approx \frac{1}{n_{tmds}}\frac{dn_{tmd}}{d\phi_1}\frac{d\phi_1}{dV_G} = \frac{q}{k_B T}\left(\frac{C_{ox}}{C_{ox}+C_{it}+C_{tmd}}\right) \tag{3.36}$$

where, C_{tmds} accounts for the quantum capacitance of all the layers. Substituting Eq. (3.36) into Eq. (3.32), the band energy position of each layer is approximately same, as the interlayer

capacitance can be omitted, we get the subthreshold slope in TMDCs is

$$SS = log(10)\frac{k_B T}{q}\left(1+\frac{C_{it}+C_{tmd}}{C_{ox}}\right) \tag{3.37}$$

More generally, *SS* of TMDCs can be written as

$$SS = log(10)\frac{k_B T}{q}\left(1+\frac{C_{it}+\Sigma_{\alpha=1}^{n} C_{\alpha}}{C_{ox}}\right) \tag{3.38}$$

Equation 3.38 which is equivalent to the *SS* equation in MOSFETs.[93]

When the Fermi level is far from the band edges i.e. $V_G \sim$-8 V in C_{tmd} becomes very small ($C_{\alpha} \ll C_{it} \ll C_{il}$), and any deviation from the ideal subthreshold slope can be attributed to these interface traps between the bottom layer of WS_2 and SiO_2. This is the advantage of the high quality of the basal planes in layered materials, free of impurity and defects. As the oxide thickness becomes smaller, the *SS* should get close to the ideal case 60 mV/decade, which previously observed in top-gated devices. As the gate voltage increases carrier density quickly exceeds 10^9 cm^{-2} [Fig. (b)], resulting in a larger C_{tmd} that degrades the value of *S*. Finally when the device is fully ON, the *S* becomes very large.

3.8.2 Effects of thin dielectrics: Achieved Almost Ideal *SS*

The gate oxide must become thin to control adequately the electrostatics of the MOSFET channel. Let us try using extreme high value of C_{ox} i.e. if we let $C_{ox} \rightarrow \infty$ in Equation 3.38. The subthreshold swing of a conventional device yields to be 60 mV/dec at room temperature 300 K approaching the theoretical limit of *SS* of a MOSFET. Based on the fitting result of the interface trap density shown in a thin SiO_2 substrate can allow us to achieve a nearly ideal *SS* in WS_2. Hence, we fabricate FL WS_2 devices on 10-nm SiO_2 substrate. We successfully obtained the values of *SS* about 64 mV/dec very close to the theoretical limit of a TMDC-based FET at 300 K even in the presence of contact resistance. This is the first demonstration to the best of our knowledge of achieving such steep *SS*

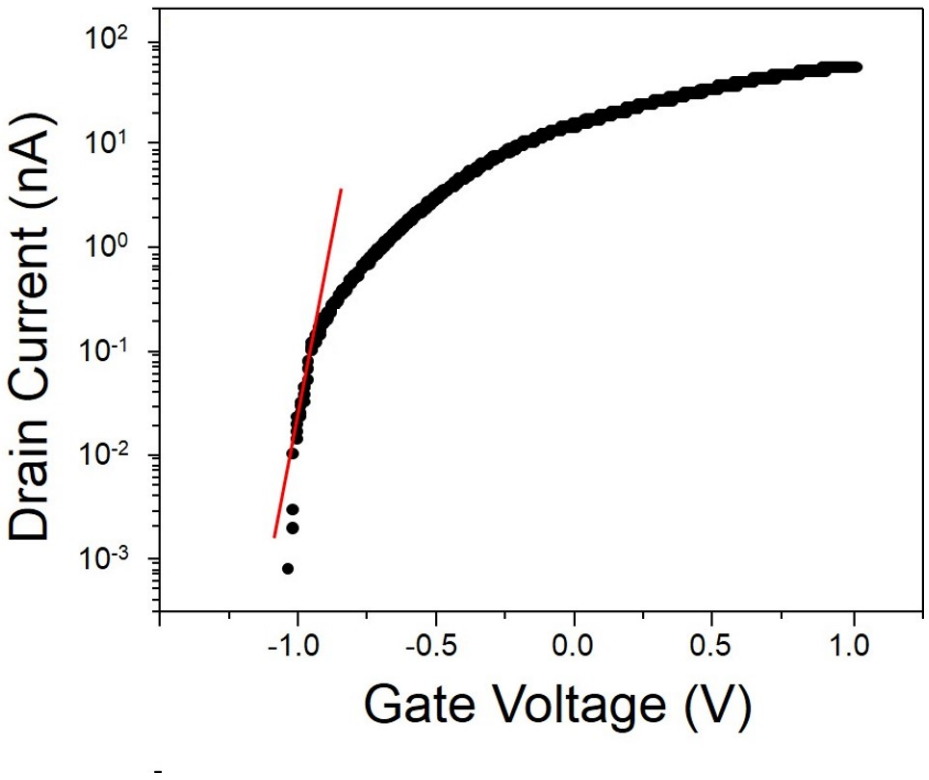

Figure 3.9: Transfer characteristic curve of few-layer WS_2 on 10-nm SiO_2 shows *SS* of 70 mV/decade.

in TMDC-based fabricated on back-gate device geometry. Compare this to the D_{it} we found in the 300-nm SiO_2, this 10-nm SiO_2 device reaches even lower total interface trap density than the case of 300-nm SiO_2. With the assumption of having similar interface trap density between WS_2 and SiO_2, the thin oxide likely has lower surface defect density than the thick one based on the same argument we have earlier. In prior studies nearly ideal *SS* results have only been achieved by increasing the oxide capacitance. In those studies top-gated systems were used employing high-κ dielectrics[70,94] with much smaller dielectric thicknesses, or electric double layers[89] formed by liquid electrolytes.

3.9 Conclusions

In the next few years, progress in this field will require advances in understanding electron transport in layered materials and the effects of quantum capacitance along with developing defect-free devices. It is very important to understand the phenomena governing good electrical contacts based on the band alignments and the interactions between electrodes and layered materials. Charge injection between these metals electrodes and vdW systems can be probed by extending the theoretical model we have established. In layered materials 2D TMDCs have many distinctive properties that are not seen in other materials systems. As researchers learn more about them, there are sure to be unexpected and exciting applications.

We fabricated low trap charge FETs ranging from monolayer to bulk WS_2. Understanding full range characteristics of 2D FETs led us to fabricate devices approaching ideal energy efficiency in FETs. The problem statement and conclusions along with brief impact to field is described.

Our entire set of WS_2 devices made under identical fabrication processes and on the same substrate with varying WS_2 thicknesses ranging from monolayer to bulk- show very comparable values of *SS* from 450 to 670 mV/dec. We realized that our samples have small defects and impurities and our devices reached a low interface trap density. This finding is important to field because it demonstrates similar performance of devices independent of thickness. This implies

that thickness of 2D materials is flexible for device performance.

We were the first to characterize the full range of characteristics of 2D material FETs. We found that the quantum capacitance of an individual layer [Eq. 3.28] can differ significantly from the value of C_0 depending on the position of the Fermi level relative to the band edges. The transconductance of a system can be modeled by assuming that the localized-trap states do not participate in transport and that mobility in each layer is the same and independent of carrier density. We acquired the best-fit parameters in the full range of electron conduction, the trap density $\approx 6\times10^{11}$ cm^{-2} spread over a width ≈ 0.2 eV residing at ~ 0.12 eV from the bottom of the conduction band. These values are in agreement with the thermally activated energy found in WS_2. Our capacitive model proved by our experiments are extremely important to the field for basic understanding of carrier transport in 2D FETs.

Further investigation is required to understand the field-dependent contact resistance that could become a limiting factor for the ON-current in vdW layer-based devices. We successfully obtained *SS* values of 64 mV/dec. This is very close to the theoretical limit of a TMDC-based FET at 300 K even in the presence of contact resistance. This is the first demonstration to the best of our knowledge of achieving such steep *SS* in TMDC-based device fabricated on back-gate device geometry. In prior studies nearly ideal *SS* results have only been achieved by increasing the oxide capacitance. The impact to the field of our study, then is, by carefully designing interface trap charges, energy-efficient devices with the steepest possible *SS* can be achieved.

Chapter 4

Substrate Effects - How h-BN affects WS_2

4.1 Overview and Background: Motivation for Using a Thin-Film/h-BN Heterostructure

This chapter focuses on the electronic properties of transition metal dichalcogenides (TMDCs) like WS_2 on hexagonal boron nitride (h-BN) heterostructures. The transport properties of layered devices may dominate by surface effects. The interplay between quantum and oxide capacitances mainly determines transfer characteristics of heterostructures as shown in Eq. (3.38). Understanding the effects is critical for successful real world applications based on these materials.

Chapter 3 discussed the contributions of quantum and oxide capacitances in TMDCs on SiO_2 substrates. We achieved subthreshold slope (*SS*) values close to the ideal for a metal-oxide semiconductor field-effect transistor (MOSFET). The carrier mobility on SiO_2 substrates is limited by three main characteristics: (i) scattering from charged surface states and impurities,[45,16] (ii) substrate surface roughness[42] and (iii) SiO_2 surface optical phonons.[47,46]

In layered materials like graphene, electron transport is subject to microscopic perturbations in substrate materials that can cause backscattering. This greatly decreases carrier mobility (μ). Graphene obtained by mechanical cleavage and layered on top of an oxidized Si wafer has $\mu \sim 10{,}000$ cm^2/Vs.[95] For typical carrier concentrations $n \approx 10^{12}$ cm^{-2}, this quality translates into a mean free

path,

$$l = (h/2e)\mu(n/\pi)^{1/2} \tag{4.1}$$

on the order of 100 nm, where n is carrier concentration, h is the Planck constant and e is the electron charge. One way to eliminate substrate effects in graphene transport is to remove the substrate entirely. Several groups have reported freestanding graphene sheets suspended over a trench.[7] The mobility of graphene reaches at room temperature can reach 200,000 cm^2/Vs the electron density of $\sim 2 \times 10^{11}$ cm^{-2} due to weak electro - phonon interactions.[44] For $n \sim 10^{11} cm^{-2}$, μ exceeds 100,000 cm^2/V.s at room temperature. These particular values were demonstrated in suspended graphene annealed by high electric current.[96,44]

The suspended graphene is fragile and difficult to handle. Finding an alternative substrate to SiO_2/Si that maintains the transport properties of suspended graphene devices was important for device applications. An atomically smooth substrate was achieved using h-BN for graphene.[48] h-BN is exceptional substrate, increasing graphene's electronic quality tenfold. It has an atomically smooth surface that is comparatively free of dangling bonds and charge traps. h-BN is an attractive alternative to SiO_2 for gate dielectrics because of its physical properties. The dielectric constant of h-BN is $\kappa \approx$ 3-4 and the dielectric constant of SiO_2 is $\kappa \approx 3.9$.

h-BN is probably one of the best materials to use as the dielectric layer in miniature electronic devices. Demonstrated graphene/h-BN heterostructures are already an improvement over more traditional devices.[12] Less studied, however, is the utility of h-BN as substrate for other two-dimensional (2D) semiconductors, including TMDCs. Herein, we describe investigations of WS_2 heterostructures that contain h-BN as a substrate sandwiched between the TMDC and SiO_2. Chapter 3 investigated how the surface/interface properties of WS_2 contribute to carrier transport in WS_2-based electronic devices.

4.2 Capacitance in Back Gated TMDC/h-BN/SiO_2 FETs

In theory, the capacitance of a parallel plate capacitor can be calculated if the geometry of the electrodes and the dielectric properties of the insulator (in this chapter, few layered h-BN/300-nm SiO_2 and 300-nm SiO_2) between the electrodes are known. For example, the capacitance of a parallel-plate capacitor composed of two parallel plates of area A separated by a distance d is approximately equal to the following:

$$C = \frac{\varepsilon_0 \varepsilon_r}{d} \tag{4.2}$$

where C is the thickness of the oxide per unit area A of each electrode plate, ε_r is the relative static permittivity i.e., the dielectric constant (ε_r=$\varepsilon_{SiO2} \approx 3.9$) of the material between the electrode plates, ε_0 is the permittivity of free space ($\varepsilon_0 = 8.854 \times 10^{-12}$ F/m), d is the distance between the plates. For bare 300-nm-thick SiO_2 dielectric, Eq. (4.2) yields $C_{SiO2} = 11$ nF/cm^2.

For a h-BN/300nm-SiO_2 heterostructure, the equivalent capacitance can be considered as two capacitors in series composed of few-layer (FL) h-BN and 300 nm SiO_2, with capacitance written as:

$$\frac{1}{C_{hBN/SiO2}} = \frac{1}{C_{hBN}} + \frac{1}{C_{SiO2}} \tag{4.3}$$

where C_{hBN} is the capacitance of h-BN ($\varepsilon_{hBN} \approx 3.9$) comparable to that of the same thickness of SiO_2. However, we used around 20 layer h-BN. One layer thickness of h-BN is 0.33 nm, so the capacitance of 20-layer was less than capacitance of 300-nm SiO_2 (C_{SiO2}). For our h-BN/300-nmSiO_2 heterostructure, the capacitance, $C_{h-BN/SiO2}$ was lower than the lowest value of C_{h-BN} or C_{SiO2}. Consequently, the equivalent capacitance of $C_{h-BN/SiO2}$ for FL h-BN on 300 nm SiO_2 was less than either capacitance of 300-nm SiO_2 or FL h-BN. Hence, the gate control of h-BN/SiO_2 heterostructure should be less than FET on 300 nm SiO_2. However, our experimental data shows us interesting results as discussed in the remainder of this chapter.

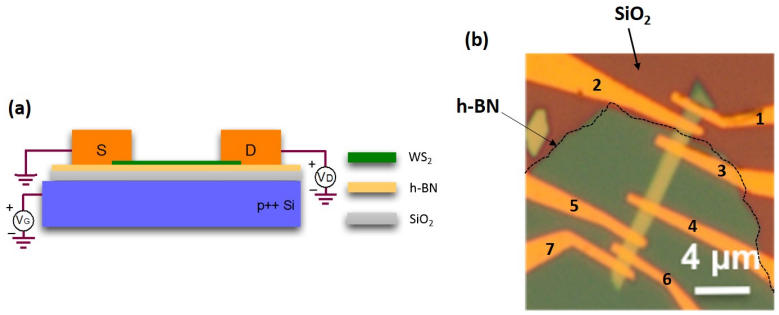

Figure 4.1: (a) Schematic diagram of a WS_2/h-BN heterostructure bottom gate field-effect transistor on 300 nm-SiO_2 gate oxide as shown in the diagram. (b) A ribbon of WS_2 was transferred onto h-BN using PDMS; 5/70 nm Ti/Au was deposited for metal contacts; electrodes 1 and 2 are for the control experiment for WS_2/SiO_2. Electrodes 3-4, 4-5, 5-6 and 6-7 are on WS_2/h-BN distances of 3 μm, 1.5 μm, 500 nm and 200 nm part.

4.3 Device Fabrication

Transferring any flake using on of the transfer methods described in Chapter 2, introduces impurities, defects and charge traps. We transferred parts of same WS_2 flake onto h-BN and SiO_2 to investigate the effects of identical WS_2 flakes on two different substrates. Although finding the desired geometry and configuration could be difficult, our experience with 2D material preparation and stacking made it possible and we used WS_2 uniform ribbons to minimize random geometrical effects. Furthermore, we were able to make low hysteresis devices.

We exfoliated h-BN (supplied from 2DSemiconductors) onto a 300-nm SiO_2 substrate. We thermally annealed the samples at 220 °C for 2 hours under a H_2/Ar gas mixture (20 sccm H_2/100 sccm Ar) flowing through a quartz tube, reaching a base pressure of $\sim$3 Torr. We mechanically exfoliated WS_2 flakes onto a clear, flexible polydimethylsiloxane (PDMS) substrate using adhesive tape. Then, we directly transferred the WS_2 flakes onto the thin h-BN using a micromanipulator and a microscope with long working distance objectives. The heterostructures were again thermally annealed under the same conditions.

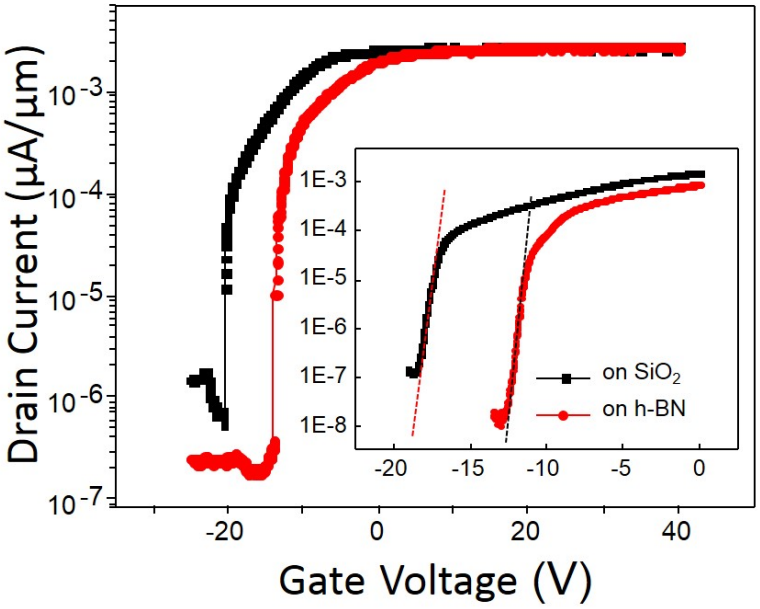

Figure 4.2: Drain current (per unit channel length) versus gate voltage between same flake of WS_2 on bare 300-nm SiO_2 with WS_2 on h-BN/300-nm SiO_2, both at drain voltage $V_D = 100$ mV. Inset shows more data points within the range $V_G \sim 0$ to -20 V to measure sub-threshold slopes (*SS*) precisely.

4.4 Improved Subthreshold Swing and Higher Current ON-OFF Ratio

While h-BN has proven to be an ideal substrate for graphene, few reports have demonstrated its usage on TMDCs. Based on our experience, the crystal quality of h-BN is variable and needs to be carefully examined before use. In the comparison to the control group (devices made from the same WS_2 flake on SiO_2 but without h-BN), the devices on h-BN displayed lower OFF-current, decreases by an order of magnitude. We observed similar ON-current to the control, thus the ON-OFF current ratio improved by about an order of magnitude. The threshold voltage when WS_2 is on h-BN is $\sim$-13V less negative than its value of $\sim$-19 V when same flake is on Si_2 indicating that WS_2 is less n-doped when on h-BN than on SiO_2 [Fig. 4.2].

With the h-BN device had a smaller total oxide capacitance due to the additional h-BN layer ($\sim$ 20 nm), we obtained a better value of *SS* for h-BN than for control devices [Fig. 4.2 inset]. The

SS of TMDCs is discussed in detail in Chapter 3 and can be written as:

$$SS = log(10)\frac{k_B T}{q}\left(1+\frac{C_{it}+\Sigma_{\alpha=1}^{n} C_{\alpha}}{C_{ox}}\right). \tag{4.4}$$

Eq. 4.4 is equivalent to the *SS* equation for MOSFETs.[93] When the Fermi level is far from the band edges in C_{tmd} becomes very small ($C_{\alpha} \ll C_{it} \ll C_{il}$), and any deviation from the ideal *SS* can be attributed to interface traps between the bottom layer of WS_2 and h-BN.

4.5 Characteristics of WS_2 on h-BN Versus SiO_2: Ambipolar Behavior

We found the *SS* was better when WS_2 was on h-BN compared to SiO_2. However, we found a more interesting feature when we further pushed gate voltage to $V_G = 60$ V. A p-branch appeared indicating ambipolar behavior for the WS_2/h-BN field-effect transistor (4.3). The steep increase in drain current I_D at large (absolute) V_D and small V_G visible in Fig. (4.3) is clear manifestation of ambipolar operations.

Based on our observations, devices on h-BN are less n-doped than devices on SiO_2. The effects of substrate doping allowed us to observe the p-branch without reaching the dielectric breakdown field.

In the presence of a local electrostatic potential ϕ_{α} at layer α, the Fermi level shifts to,

$$\varepsilon_{F,\alpha} = \varepsilon_F^0 + q\phi_{\alpha}, \tag{4.5}$$

and results in band bending (re-positioning the global Fermi level). We can define the quantum capacitance of the layer α as ,

$$C_{\alpha} = q\frac{dn_{\alpha}}{d\phi_{\alpha}} = q^2\frac{dn_{\alpha}}{d\varepsilon_{F,\alpha}}. \tag{4.6}$$

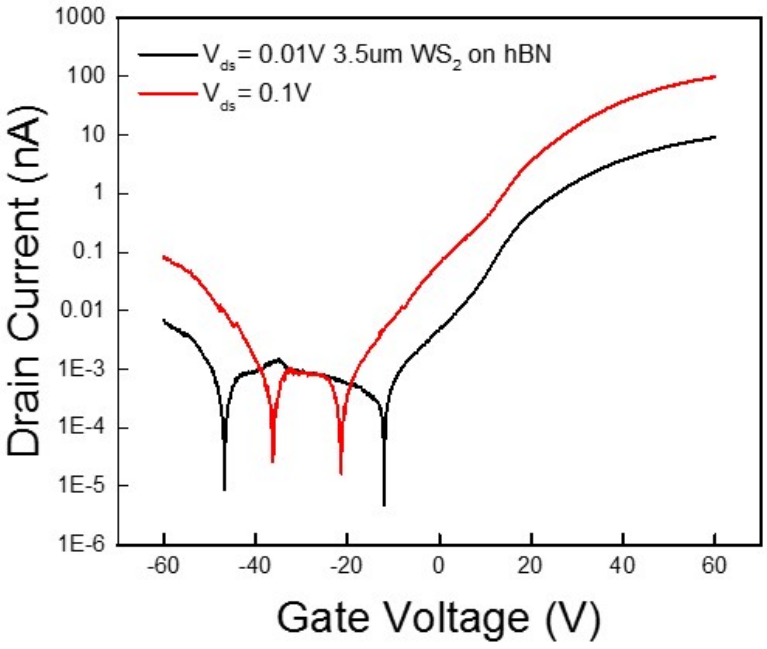

Figure 4.3: The current versus gate voltage curves of a FL WS_2 transistor at drain bias as 10 mV and 100 mV in logarithmic scales.

Using Eq. (4.5) in Eq. (4.6), layer quantum capacitance is given by:

$$C_\alpha = C_0 \left(\frac{g_c \frac{m_c^*}{m_e}}{1 + e^{\frac{E_g - 2\varepsilon_F}{2k_B T}}} + \frac{g_v \frac{m_v^*}{m_e}}{1 + e^{\frac{E_g + 2\varepsilon_F}{2k_B T}}} \right), \tag{4.7}$$

where,

$$C_0 = \frac{e^2 m_e}{2\pi\hbar^2} = 33.5\,\mu F cm^{-2} \tag{4.8}$$

where m_c^* is the conduction band effective mass, m_v^* is the conduction band effective mass and m_e is the free-electron mass. This constant is large compared to typical oxide capacitances. The charge density n can be written as:

$$n = \frac{C_G V_G}{e} \tag{4.9}$$

where C_G is gate capacitance, V_G is gate voltage and e is electronic charge. In a FET, the change

in gate voltage equals the change in the semiconductor Fermi level ΔE_F plus the variation in the electrostatic potential $e\,\Delta\phi$, which is given by,

$$e\Delta\phi = \frac{e^2 n}{C_G} \tag{4.10}$$

thus,

$$e\Delta V_G = \Delta E_F - e\Delta\phi \tag{4.11}$$

$$= \Delta E_F - \frac{e^2 n}{C_G} \tag{4.12}$$

where n is usually known as the accumulated charge density of a FET in the ON-state. However, Eq. (4.12) can be applied to the V_G interval corresponding to the OFF-state of a FET. Upon onset of electron ${V^e}_T$ and hole conduction ${V^p}_T$. The change in onset of electron and hole conduction is given by,

$$e\Delta V_{GAP} = V_T^e - V_T^h. \tag{4.13}$$

Theoretically speaking, with a high gate capacitance, e.g. liquid electrolytes an accurate value for band gap of a WS_2 monolayer versus few layers (e.g., 10 layers) can be found by using Eq. (4.2). For example, for ten layers of WS_2, capacitance will be 1/10 times of monolayer of the same material. Then simply using Eq. (4.3), the equivalent capacitance of a system is lower than the least capacitance for capacitances in series. In our example, ten layers of WS_2 capacitance will dominate more than a monolayer. In other words, in OFF-state of a high gate capacitance situation, $e\Delta V_{GAP} = \Delta E_F = \Delta_{WS2}$ the term $\frac{e^2 n}{C_G}$ can be neglected. However, if gate dielectric capacitance C_G is small, this method cannot be used to find the band gap of material.

To restate above calculations in more general way, extracting the band gap of a semiconductor from the transfer characteristics of a conventional transistor using I_D versus V_G is not possible. Instead calculations must include (i) contact effects, (ii) the influence of localized energy gap states on charge transport and (iii) the small capacitance of conventional solid-state dielectrics.

The importance of the last two phenomena can be understood by the fact that the change in the FET gate bias (V_G) is related to the change in Fermi position level of semiconductor.

We applied these theoretical considerations to our heterostructure. Since n is related to the finite density of states in the band gap either due to defects the materials or at interfaces (i.e., charge is populated in localized states inside the band gap), when the oxide capacitance is relatively small, a change of Fermi level ΔE_F equivalent to an ideal band gap of the semiconducting material (1.35 V in the case of WS_2) can be neglected. Thus, the term $e\,\Delta V_{GAP}$ can be approximated.

We measured an interface trap density less than 8×10^{11} cm^{-2} at $V_D = 10$ mV within the entire band gap including the possible trap in thick SiO_2. This value was in agreement with the fitting parameter discussed in Chapter 3 of this dissertation. Thus, to generate the ambipolar TMDC-based FETs required minimizing surface trap density in the energy gap with an additional concern for matching suitable contact metal for both branches. Finding the band gap of FL WS_2 was more accurate than finding the band gap for monolayer WS_2 with the condition that the interface traps were the same and the gate capacitance was high.

4.6 Channel Length Scaling of WS_2/h-BN Heterostructures

We investigated electrical transport properties in WS_2/h-BN 2D heterostructure with channel lengths ranging from $\sim 3\ \mu$m down to 200-nm. We compared the short channel behavior of sets of MOS-FETs of the same flake of uniform ribbon WS_2 on h-BN. To do this, we measured ΔV_{GAP} for a WS_2 flake of uniform width on h-BN with channel lengths 3 μm, 1.5 μm, 500 nm and 200 nm [Fig. 4.4]. We conducted the experiment with drain voltages $V_D = 10$ mV, 40 mV, 70 mV, 100 mV, 130 mV and 160 mV at room temperature. The change in onset of electron $V^e{}_T$ and hole conduction $V^p{}_T$ is given by $e\,\Delta V_{GAP} = V^e{}_T - V^p{}_T$. The value of ΔV_{GAP} was maximum for for 3 μm, ranging from goes from $\Delta V_{GAP} = 35$ V to $\Delta V_{GAP} = 23$ V for $V_D = 10$ mV to 40 mV [Fig. 4.4].

The data (Fig. 4.4) could be fitted to the Arrhenius equation, which gives the quantitative basis for the relationship between the activation energy and the rate at which a reaction proceeds. From

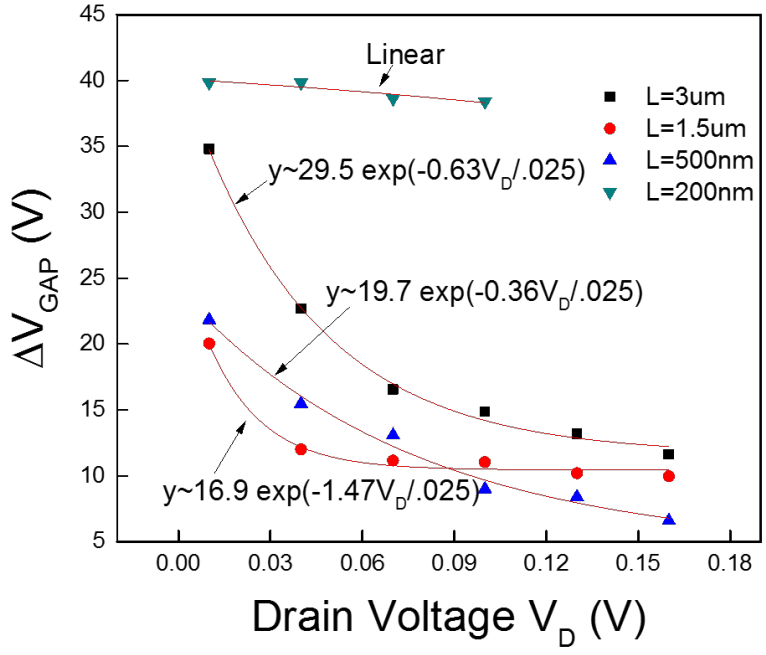

Figure 4.4: Drain voltage vs ΔV_G of FL WS_2 transistor on hBN/300-nm SiO_2 with ribbon like uniform shape, transistor lengths $L = 3$ μm, 1.5 μm, 500 nm and 200 nm with uniform $W_{ave} = 1.2$ μm.

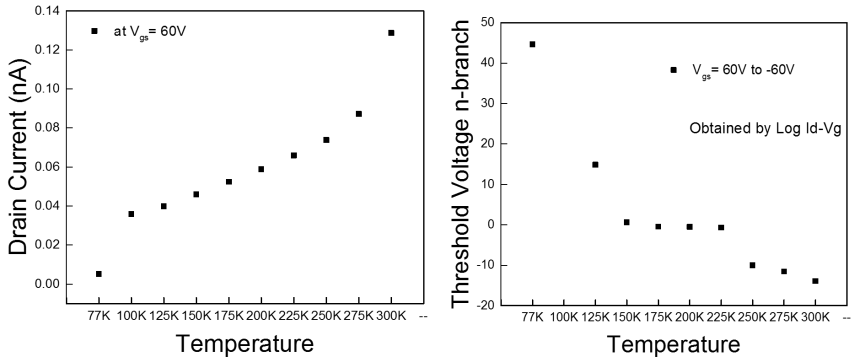

Figure 4.5: Temperature dependence of drain current for transistor length of $L = 3$ μm with uniform $W_{ave} = 1.2$ μm at $V_D = 100$ mV.

the Arrhenius equation, activation energy can be found through the relation,

$$k = Aexp(\frac{E_a}{RT}) \tag{4.14}$$

where A is the frequency factor for the reaction, R is the universal gas constant, T is the temperature (in Kelvin), and k is the reaction rate coefficient. As channel length decreases from $L = 3$ μm to 200 nm, the frequency factor (A) decreased as well (Fig. (4.5). The activation energy E_a increased as the channel length decreased from 3 μm to 500 nm. However, for the 200 nm channel, the short channel length scaling phenomenon diminished gate control. However, the change in ΔV_{GAP} was least when channel length was 200-nm. Any deviation in SS [Eq. 4.4] in our heterostructure was caused by interface trap charges between the WS_2 layer and the h-BN surface in our heterostructure. Considering the fact that for the 200-nm channel length we were observing short channel effects, the drain voltage did not have any pronounced effect on ΔV_{GAP}. Thus, that short channel effect dominated over interface trap charges for shorter channel lengths.

For longer channel lengths, e.g., 3 μm, the change in ΔV_{GAP} was highest for low bias implies that activation energy of interface trap charges between WS_2 and h-BN is of order of few $k_B\mathrm{T} \sim 25$ meV, where k_B is the Boltzmann constant and T is temperature. Once the drain voltage was large enough to over come the energy barrier of these interface trap charges, the difference in ΔV_{GAP} for any other consecutive difference in drain voltage bias (40 mV to 70 mV, 70 mV to 100 mV,

100 mV to 130 mV, or 130 mV to 160 mV) was not as big as it was for the 10 mV to 40 mV difference. Lastly, the saturated current at $V_G \sim 60$V decreased as temperature decreases from 300 K to 77 K (Fig. 4.5). However, the threshold voltage V_{TH} of the n-branch increased as temperature decreased from 300 K to 77 K indicating that electron conduction was dominated by thermally activated charged carriers.

4.7 Conclusion and Future Work

In brief, our work shows that h-BN can be used as a substrate in TMDC semiconductors for improved current ON-OFF ratio and better *SS*. It provides surface with relatively fewer trap charges and confers ambipolar behavior even on relatively low capacitance substrates, compared to liquid electrolytes. We explored interface trap charges and the quality of our heterostructure. Our interesting results may be helpful to the field FET devices for both n-type and p-type carrier are required.

In our experiments, we fabricated high quality heterostructure with low interface trap charges. We used them to explain, carrier transport for both electrons and holes in devices with low gate capacitances. In comparison to the control group (devices made from the same WS_2 flake on SiO_2 but without h-BN), the devices on h-BN had lower OFF-currents. However, we achieved similar ON-currents, overall improving the current ON-OFF ratio by about an order of magnitude. It is interesting to note that for a smaller total oxide capacitance due to the additional 20-nm h-BN layer, we obtained a similar value of *SS* on hBN devices as on control devices.

Our study describes the first WS_2/h-BN transistors to achieve ambipolar behavior. We attributed this mainly to low interface trap charges. We measured the interface trap density of h-BN/SiO_2, and found the value is less than 8×10^{11} cm^{-2} within the entire bandgap including the possible trap in thick SiO_2 oxide. Previously, this has been achieved only with high gate voltage,[89,97] proving the low trap charge heterostructures in our and high quality devices. The contribution to the field from this research is a practical process for acquiring low trap charge

heterostructures that show ambipolarity even at low backside gate capacitances.[89,97]

One objective of our experiments was to use h-BN to improve device interfaces. Carrier density n is related to the finite density of states in band gap due to defects in the materials or at interfaces. In interfaces the charge is populated in localized states inside the band gap. Our h-BN/300-nm SiO_2 capacitance was small, so a change of the Fermi level ΔE_F equivalent to an ideal bandgap of semiconducting material (1.35 V in WS_2 case) could be neglected. More work is required to minimizing surface trap density in the energy gap with an additional concern for matching suitable contact metal for both branches. Moreover, in the future, transferring and annealing conditions of h-BN can be improved to most easily utilize h-BN as substrate. Quality and doping of h-BN can be tuned to make TMDC/h-BN heterostructures of desired electronic and optoelectronic properties.

Chapter 5

Channel Length Scaling

5.1 Introduction

Over the past four decades, the challenge of very large scale integration has been the integration of increasing numbers of devices. Finding alternative channel materials like TMDCs for future logic devices beyond the 10-nm node are needed for silicon based transistors. It is because, scaling of them is reaching its physical limits. These efforts have focussed on Ge and III-V materials because of their superior carrier mobilities.[98,99] The discovery of graphene has opened up opportunity to explore another material family with layered structures, which includes boron nitride, and transition metal dichalcogenides like MoS_2, WS_2, and $NbSe_2$.[100,9,101,102]

Graphene has shown a superior carrier mobility as high as to 200,000 cm^2/Vs, but it has zero band gap. It limits its application in logic devices. Due to this, graphene transistors cannot have high ON-OFF current ratios. On the other hand, TMDCs (such as WS_2) are another type of layered structure material that has great potential in device applications. This is due to their carrier mobility, and compatibility with silicon complementary metal-oxide-semiconductor processing.[70]

The issues in high performance of TMDC FETs involve elimination of short channel effects and high quality dielectric deposition. The performance of these devices is limited by Shottky barrier height at TMDCs/metal interface. It is important to find metal (we used Ti/Au) so that work

function is close to conduction band for n-type transistors (valence band for p-type). The characteristic length for short channel TMDCs like WS_2 transistors is small due to the low dielectric constant of them. However, as device reaches of the order of characteristics length, the characteristics of a conventional MOSFET change. The goal is therefore to achieve scaling of any device with high yield and reliability.

5.2 Why scaling is Important

Moore's law has held quite well. The materials science is now encountering minimum size limits for traditional devices. The continually smaller scaling is of utmost importance to the field. One of the key use of scaling is to reduce the dimensions of the chip. It is for same functionality of the circuit. This will allow an increase in circuit density on a chip. In order to double the density of transistors on a chip, we need to reduce the transistors' linear dimensions. If we want to double the double the density of transistors on substrate, that would mean reducing the dimensions (length and width), has been achieved for κ equal to $\sqrt{2}$ for two dimensional scaling. However, for example, in our case if WS_2 channel length scaling by two, it would imply we are reducing the size of length of channel only. That implies, κ equal to 2 in our one dimensional scaling of WS_2, by definition. This scaling law implies a reduction in the supply voltage by a factor of κ, as well as a reduction in the threshold voltage by κ.

5.3 Short-Channel Length

When drain voltage is increased, penetration of electrical charge in the region between the gate, and on on other side source and drain, is amplified. Therefore, the gate electrode no longer alone controls the potential in the channel region. Therefore, gate electrode no longer controls the resultant concentration of electrons. The potential is also affected by the distance between the source and the drain and by the voltage applied to the drain. This loss of charge control due to short channel length by the gate modification of the threshold voltage is called drain-induced barrier

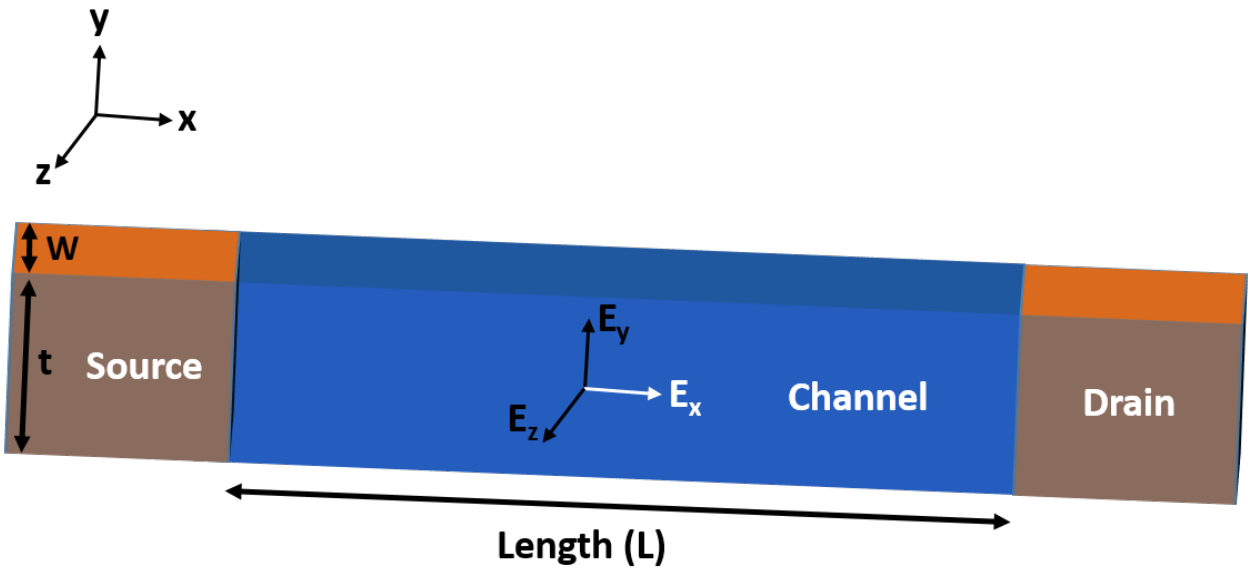

Figure 5.1: Electric fields within the channel region: The vertical component of the electric field E_y arises from bottom gate (Our devices had only a bottom gate, no top gate). The lateral component E_z arises from side gates along the z-axis (also not applicable for our bottom-gated WS_2 devices). The longitudinal component E_x from the source and the drain regions. L is channel length, t is thickness of the 2D materials (in our case TMDCs like WS_2), and W is the width of the channel).

lowering (*DIBL*). The value of *DIBL* decreases the threshold voltage, when the drain voltage increases with short channel length. The consequence of the *DIBL*, is that it imposes electron drift characteristics in the channel and thus degrades *SS*. It increases the leakage current of transistors with short-channel. They constitute a serious hinderance to further scaling of MOSFETs.

5.4 Natural Length of back-gated Semiconductor Devices

Poisson's equation describes how the gates compete with the source and the drain for the charge in the channel. It provides an analytical method to find the potential distribution WS_2 semiconductor,

$$\frac{d^2\phi}{dx^2} + \frac{d^2\phi}{dy^2} = \frac{qN_A}{\varepsilon_{WS2}}, \tag{5.1}$$

where, $\phi(x,y)$ is the potential distribution in WS_2 film, N_A is WS_2 doping and ε_{WS2} is the dielectric constant of WS_2 with $0 \leq x \leq L_{eff}$ where L_{eff} is the effective channel length. We used a sim-

plification of the 2D Poisson's equation to describe the potential distribution as a one-dimensional potential distribution along the WS_2/SiO_2 interface only. The Maxwell equations gave the distribution of electric potential in the channel region more simply by,

$$\vec{\nabla} \cdot \vec{E} = \frac{\rho}{\varepsilon}, \tag{5.2}$$

where, $\vec{E}$ is the electrical field, ε is the permittivity of the material under use, and ρ is the local density of charge in charge per unit volume. The Poisson Eq. 5.1 for electric field can be written as,

$$\frac{dE_x}{dx} + \frac{dE_y}{dy} + \frac{dE_z}{dz} = -\frac{\rho}{\varepsilon} = constant, \tag{5.3}$$

to represent the control of source and the drain. The gate control is in the direction of the y-axis and z-axis [Fig. 5.1]. It competed with variations in the electric field from the source and drain in the x-direction. As shown in Eq. 5.3, all the terms of the Poisson equation add up to a constant. This implied that any increase in control by the bottom gate (we did not have a top gate in our devices), any increase in control by the left and the right hand sides

$$\frac{dE_y}{dy}, \tag{5.4}$$

bottom gate

$$\frac{dE_z}{dz}, \tag{5.5}$$

would control the source and the drain electric fields deep within the channel region by the component of the Poisson equation,

$$\frac{dE_x}{dx}. \tag{5.6}$$

We used a simple parabolic function in the y-axis to describe the potential distribution,

$$\phi(x,y) \approx c_0(x) + c_1(x)y + c_2(x)y^2, \tag{5.7}$$

that requires three conditions in the vertical direction to a have a non-trivial solution. It has four boundary conditions two along the x-axis: potential along the bottom interface of the WS_2 film ϕ_b(x) and potential along front end of the WS_2 film and two along y-axis: electrical field at $y = 0$ and $y = t_{WS2}$. We assumed that the air on the front end of the WS_2 stretched to infinity so that any finite difference induced across it led to a negligible field.

5.4.1 Fabrication of Devices with Different Lengths

We fabricated sets of WS_2 MOSFETs with various channel lengths. We exfoliated samples from a single commercially available defect free tungsten disulphide (2H WS_2) crystal (2D Semiconductors) onto 300-nm SiO_2 using the scotch tape micro-mechanical cleavage method. We intentionally fabricated from the same rectangular WS_2 flake. It is because, that way, we do not need correction factor accounting for variation in geometry and thickness. We mechanically exfoliated the flakes from a bulk WS_2 cyrstal, as described in previous chapters, and transferred them to a 300-nm SiO_2/Si substrate. We removed scotch tape glue by putting exfoliated samples in acetone for 30 minutes at 50°C.

The heavily doped silicon substrate served as the global back gate and the 300-mn SiO_2 as the dielectric. Due to variations in geometry, of TMDC, it was difficult to compare the device performance directly. We selected as a sample WS_2 devices fabricated on one ~ 10 nm-thick crystal. These devices have ~ 6 layers and were rectangular in shape. We did not reduce the thickness of the WS_2 crystals to a single layer intentionally. It is because, the larger band gap of a monolayer may have reduced electron mobility that would have limited our ability to see significant channel length scaling characteristics. An optical microscope image of the 10-nm thick devices and showed channel lengths from 2 μm to 180-nm.

5.4.2 Experimental Results

We performed electrical characterization of our device at room temperature using a semiconductor device analyzer. We carried out all measurements under ultra high vacuum conditions (10^{-6} mbar).

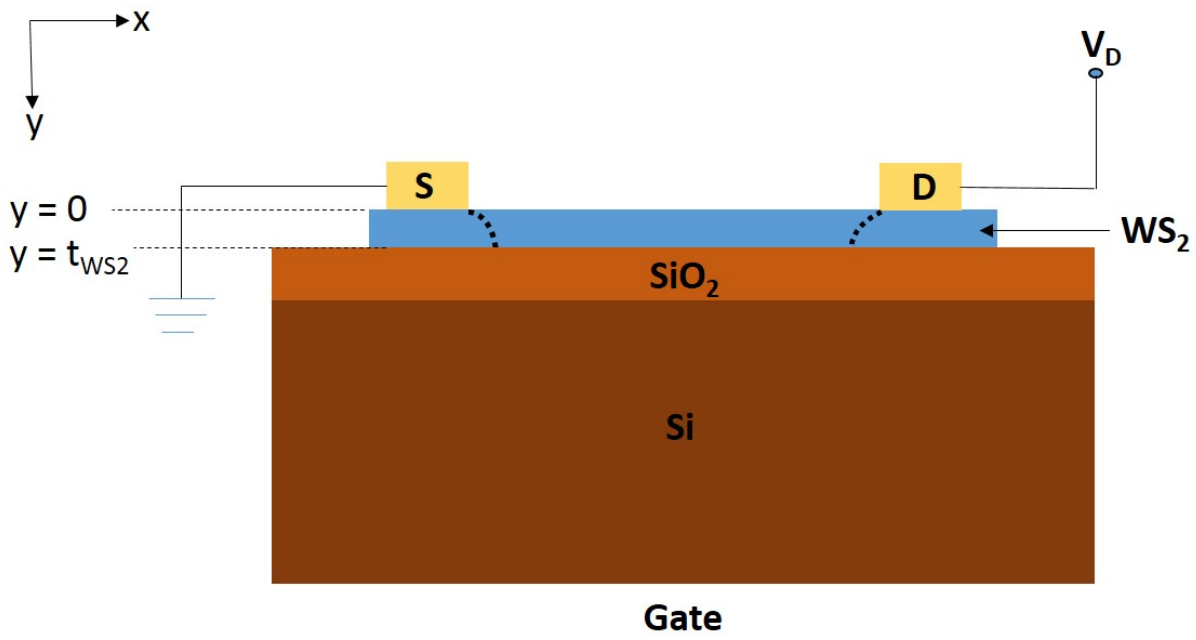

Figure 5.2: Cross sectional view of the structure of a WS_2 MOSFET device.

We applied the gate voltage (V_G) at the silicon back gate. All of the WS_2 transistors we fabricated, showed behavior typical of FET devices with n-type channels. It did not matter much the number of layers or contact material. Changing the direction of V_G sweeps on the same device did not show significant hysteresis. It indicated that the bottom gate was not accumulating charge during measurements.

We fabricated four-probe devices as well. We extracted the low field ($V_D = 100$ mV) contact resistance from devices with channel length larger than the carrier mean free path in the channel (>400 nm). The electron transport could be considered to be mostly in the diffusive regime for $L_{Channel} > 400$-nm. The contact resistance showed a strong dependence on the back gate bias because the WS_2 crystal was electrically doped under high gate bias (as shown in Chapter 3). It leads to smaller contact resistance at higher values of V_G.

We examined the transistor characteristics of both long-channel and short channel WS_2 MOSFETs. We carried out this study on the same set of devices used in contact resistance measurements. Monolayer WS_2 has shown a larger band gap and, and thus a lower mobility and larger contact re-

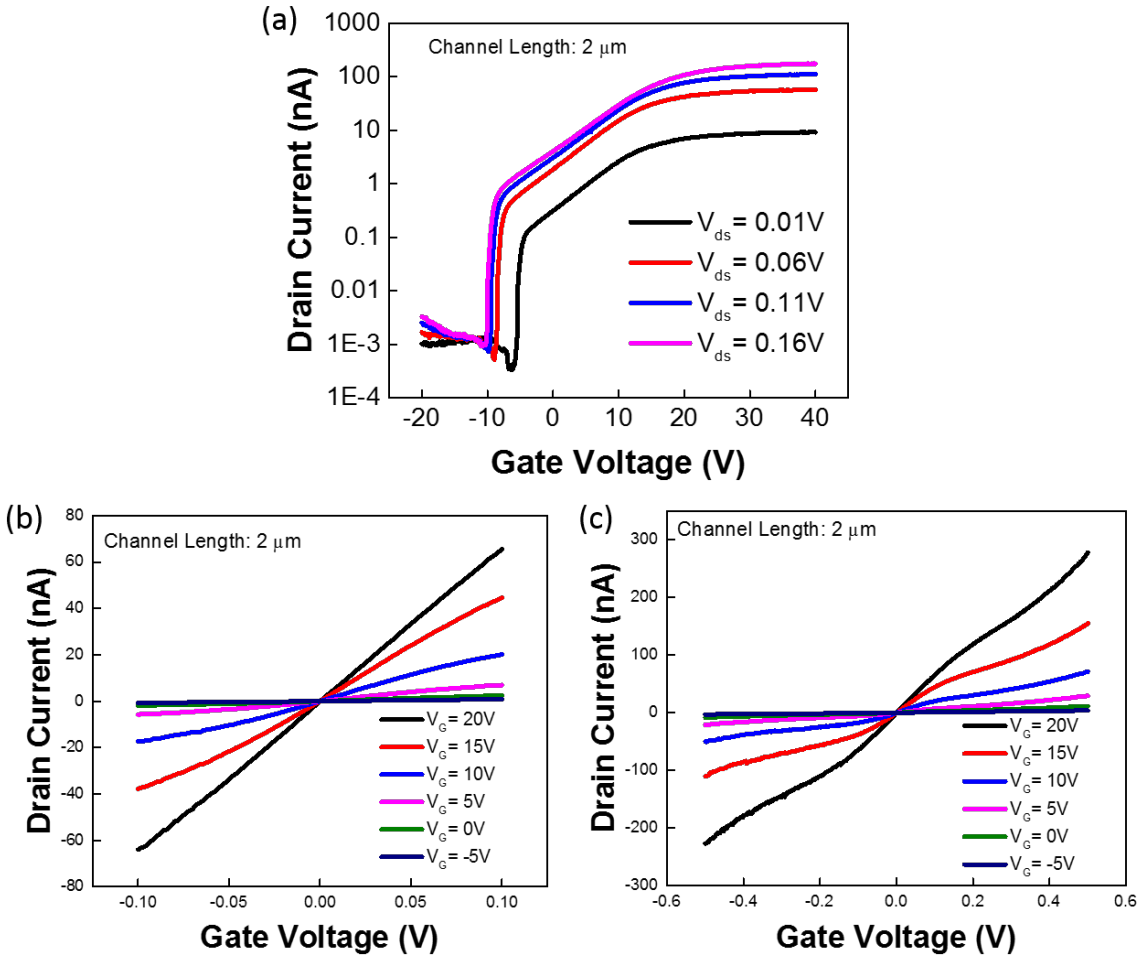

Figure 5.3: (a) Drain current versus gate voltage for channel length $L = 2$ μm at $V_D = 10$ mV, 60 mV, 110 mV and 160 mV; (b) Drain current versus drain voltage for different drain voltage in the range of $V_D = $-100 mV to 100 mV; (c) I-V_D for the drain voltage of $V_D = $-0.5 V to 0.5 V.

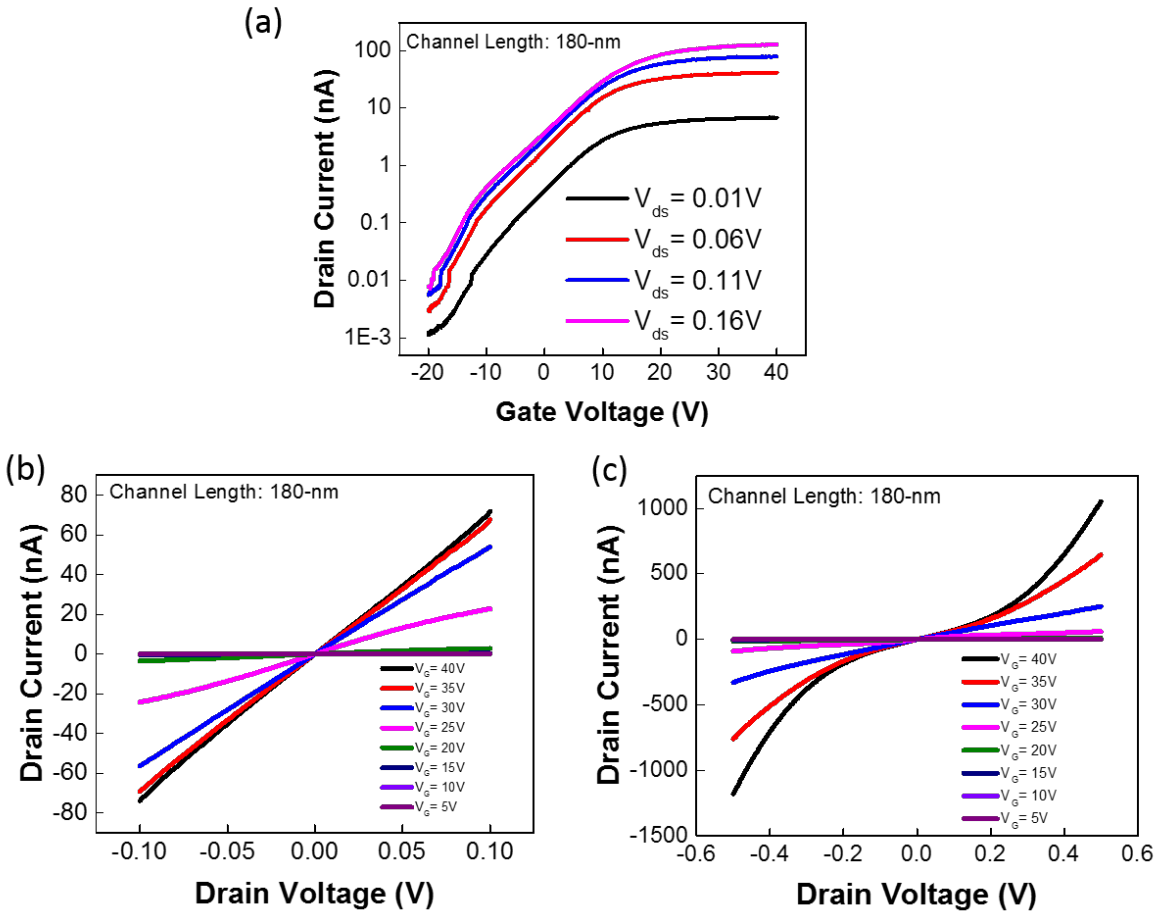

Figure 5.4: (a) Drain current versus gate voltage for channel length $L = 180$ nm at $V_D = 10$ mV, 60 mV, 110 mV and 160 mV; (b) Drain current versus drain voltage for different drain voltage in the range of $V_D = -100$ mV to 100 mV; (c) I-V_D for the drain voltage of $V_D = -0.5$ V to 0.5 V.

sistance than a few-layered (FL) WS_2. For this reason, we fabricated devices on FL crystal for a more favorable balance between the current ON-OFF ratio and device performance. The dielectric constant of WS_2 is only around 3.5, so a 10 nm-thick crystal was thin enough for channel devices to turn off completely. Figures 5.3 and 5.4 show the transfer and output characteristics for 2μm and 180-nm channel lengths, respectively. Unlike graphene, these devices could be easily turned OFF, because of their large band gap. The gate dielectric was very large for 300-nm, that resulted in a lesser electrostatic control and short-channel effects were evident when channel lengths decreased to 180-nm. The ON-current conductivity reached to 1000 nA/V for all the channel lengths ranging from 2 μm to 180-nm.

We conducted detailed I_D-V_D measurements, where I_D and V_D are the drain-source current and bias.. Figure 5.3 shows transfer and output curves for the 2 μm At low voltages ($V_D = 110$ mV), I_D-V_D values near room temperature at all values of V_G were linear for Ti/Au [Fig. 5.4(b)]. The I_D-V_D characteristics became nonlinear at large V_D [Fig. 5.4 (c)]. The symmetric nature of I_D-V_D around $V_D = 0$ enabled us to eliminate any possibility of Schottky contact in our operating V_D range. This was supported by the observed magnitude of the differential carrier mobility (μ) is given by,

$$\mu = \frac{1}{C}\frac{d\sigma}{dV_G}, \tag{5.8}$$

where, C is the gate capacitance per unit area (here, 1.2×10^4 F/m^2 for 300-nm SiO_2). The value of linear conductivity (σ) at low V_D is given by,

$$\sigma = \frac{L}{W} \times \frac{I}{V_D}, \tag{5.9}$$

where, the terms L and W are the length and width of the WS_2 channel. For channel lengths from 2 μm to 400-nm, we observed consistent current ON-OFF ratio of 10^5 at $V_D = 110$ mV. The current ON-OFF ratio, benefiting from the ultrathin WS_2 format, did not drop much showing good immunity to short-channel effect down to 400-nm channel length. Our observation of transistors showed signature of short channel effects on 300-nm SiO_2. It may be possible to increase of

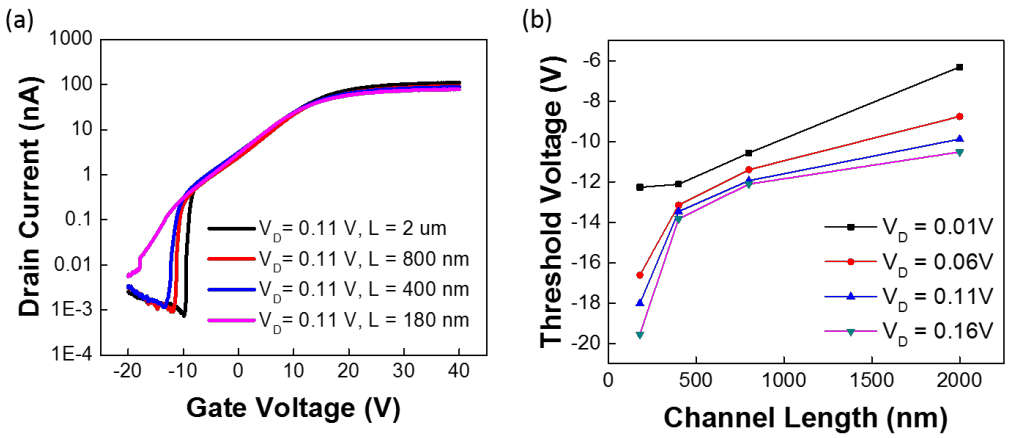

Figure 5.5: (a) Conductivity versus gate voltage of different channel lengths $L = 2$ μm, 800-nm, 400-nm, 180-nm with uniform $W_{ave} = 1.2$ μm at $V_D = 110$ mV; (b) Threshold voltage versus channel length at variable drain voltages, $V_D = 10$ mV, 60 mV, 110 mV and 160 mV.

electrostatic control of gate by reducing the gate dielectric way smaller than our 300-nm thick SiO_2 gate. It may restrict the scaling of channel lengths down to sub- 10-nm for WS_2 devices. However, we observed the superior immunity of WS_2 to short channel effects up to 400-nm. It is due to ultrathin body nature and low dielectric constant of WS_2.

Fig. 5.5(a) shows conductivity versus back-gate voltage V_G for different channel lengths (2 μm, 800-nm, 400-nm and 180-nm) at fixed drain voltage $V_D = 110$ mV. Channel length scaling has two characteristics and our experimental results confirmed both: (i) as the channel length decreased, threshold voltage decreased (to a more negative value) [Fig. 5.5(b)]; (ii) *SS* degraded as the channel length decreased, implying, the control of gate on the channel decreases for shorter $L_{channel}$.

The characteristic length of short-channel transistors with planar structures is,

$$\lambda = \sqrt{\frac{\varepsilon_{WS2}}{\varepsilon_{ox}} t_{WS2} t_{ox}}, \tag{5.10}$$

where, λ is natural length, which represents the extension of the electric field lines from the source, and the drain into the channel region.

The natural length λ depends on permittivity of WS_2 (ε_{WS2}), permittivity of oxide dielectric (ε_{ox}), thickness of layers of WS_2 (t_{WS2}) and t_{ox} the thicknesses of gate oxide. It is affected by a

dielectric medium. More electric flux exists in a medium with a low permittivity (per unit charge). The permittivity of WS_2 is given by $\varepsilon_{WS2} = k\varepsilon_0$. For $t_{WS2} = 10$-nm thick WS_2 on oxide thickness of $t_{ox} = 300$ nm with dielectric constant (k) of WS_2 as 1.67, natural length (λ) is solved as given by,

$$\lambda = \sqrt{\frac{1.67\varepsilon_{ox}}{\varepsilon_{ox}} 10 \times 300} \approx 70.8\ nm, \tag{5.11}$$

which is shorter than the channel length of the shortest of our devices. If we were to replace our 300-nm SiO_2 with 5-nm HfO_2, we would expect the characteristics length of only 3-nm. It is beyond the 10-nm technical node. The effective value of t_{WS2} could be even smaller further reducing the characteristic length of WS_2 FETs. The characteristic lengths of bulk semiconductors can be proposed for cases, when the carrier transport is almost isotropic. In 2D layered materials layer to layer transport is more resistive than the plane transport, as explained by the capacitive network model in Chapter 3. Therefore, the effective t_s for 2D crystals could be even smaller. So, it is possible to decrease the characteristic lengths of WS_2 transistors.

The DIBL for these set of devices demonstrated a increase once the channel length approached the characteristic length. It is typical for short channel effects [Fig. 5.5]. For long channel-devices, where L_{ch} was much larger than the length of the electron mean free path, the transistors worked in the diffusive regime totally, where field effect mobility remained constant from 2 μm to 400-nm channel lengths. The decrease in field effect mobility as channel length decreased to 180-nm can be attributed to two factors. One is the substantial contact resistance which does not scale with channel length but is present in the device whenever the contact resistance is comparable to channel length. The second factor, if we do not consider channel resistance, at shorter channel lengths, the mobility decreases. It is because the carriers are reaching their saturation velocity at shorter channel lengths. In general, the electric field in the channel leads to higher carrier velocities,

$$v = \mu E, \tag{5.12}$$

where, v is carrier velocities at reduced channel length. In our devices, carrier velocity approached

saturation with increasing electric field [Fig. 5.5(a)]. The field-effect mobility decreased at the same time as the drain current became saturated. Conductivity showed a decreasing trend when L_{ch} was less than 400-nm [Fig. 5.5(a)]. It indicates that short-channel transistors with $L_{ch} < 400$ nm were showing carrier saturation behaviors [Fig. 5.5(a)].

5.5 Conclusion

In summary, we created field-effect transistors with multilayer, two-dimensional semiconductor WS_2 as the conductive channel and 300-nm SiO_2 as the back gate insulator. We used the devices to study performance of WS_2 short-channel transistors. Although our devices were fabricated on a 300-nm thick SiO_2 gate dielectric, we demonstrated their superior immunity to short channel effects down to 400-nm channel lengths. We observed a similar value of saturation current but a sharp increase in DIBL for the device with a channel length smaller than the 400-nm length. We also performed transport studies and observed a field-effective mobility decrease and maximum current saturation at short channel lengths attributable to carrier velocity saturation. To achieve high-performance WS_2 short channel transistors, a detailed study on metal/WS_2 junctions is needed.

Chapter 6

Graphene/WS_2 Heterostructure Field-Effect Transistors

6.1 Motivation

Optoelectronic devices can generate, detect, interact with or control light. The quantum efficiency of graphene is 100 % for coverting light-to-current. It is due to long mean free path and high Fermi velocity of graphene.[103] However, graphene absorbs only 2.3 % visible light.[104] To enhance light absorption in graphene, many approaches have been employed. It includes graphene plasmons,[105,106] microwave cavities[107] and metallic plasmons.[108] No significant photogain has been reported for these graphene based photodetectors. The photoresponse mechanisms in different types of graphene-based devices include the photovoltaic effect,[109,110,111,112] the thermal Seeback effect[113,114,115] and the bolometric effect.[116] The reasons for the low photoresponsivity of graphene ($\sim 1 \times 10^{-3}$ A/W) are the fast recombination of photoexcited carriers. The large enough p-n or metal-graphene junctions are required for photoresponsivity of graphene. They are necessary for electron-hole separation in two-dimensional (2D) materials.

Van der Waals (vdW) heterostructures consist of various 2D materials, such as graphene, WS_2, and hexagonal boron nitride (h-BN) phenomena. It has not only enriched our physical understand-

ing of 2D materials into artificial heterostructures in tunneling field-effect transistors (TFETs) has been used to demonstrate noval properties of 2D structures.[23] For example, a graphene/WS_2/graphene heterostructure device with a WS_2 thickness of 5 - 50 nm exhibits a photoresponsivitiy of 0.1 A/W.[23] In this work, we fabricate a phototransistor based on a graphene/WS_2 heterostructure.

6.2 Sample Preparation

One critical problem in vdW heterostructures is the formation of interfacial bubbles and wrinkles, which lowers the performance of the devices. The contaminants are usually trapped at the interface between graphene/2D layered materials. The device fabrication with identification of bubble- and wrinkle-free areas for use is needed. One strategy for avoiding interfacial contamination is the wet transfer method. In this method, sacrificial polymer layers, mainly, poly (methyl methacrylate) (PMMA), are dissolved. We used 950K A4 PMMA for graphene transfer. We adapted the transfer technique to prepare the stack of graphene on WS_2. During the transfer process, we found that hydrocarbons contaminants, introduced during fabrication process were sometimes encapsulated at interfaces hindering pure interaction between vdW materials.

We investigated whether strong coupling at interfaces alters the Raman signature of graphene. We carefully performed Raman spectroscope before and after annealing. Our samples were placed in quartz tube at a base pressure of 3 Torr and exposed to gas flow of 10 sccm of H_2 and 100 sccm of Ar (H_2/Ar forming gas). We then raised the temperature to 200 °C and let the H_2/Ar forming gas flow for 2.5 hours. The samples in the vacuum tube were allowed to cool to around 50 °C over 30 minutes interval. We turned the vacuum pump off, waited 10 minutes, and removed the sample from the vacuum tube.

6.3 Raman Spectroscopy of Graphene/WS_2 Heterostructures

In the past decade, there have been significant advances in Raman spectroscopy of graphene on doping,[117,118,119,120,121] and strain and stress.[122,123] Controlling the charge injection process and

the electronic structure at the interface between the graphene sheet and TMDCs is essential. Interactions at interface in metal/graphene heterostructure containing ferromagnetic metals (like Co) are strong enough to modify π bands of graphene, but interactions at heterostructures containing noble metals like Au, and Cu are negligibly weak.[124,125,126] Less is known about the interfacial interactions and the electronic structures of graphene in metal-deposited heterostructures. Raman spectroscopy has ignited results on edges,[127,128,128] oxidation,[129] electrical mobility, thermal conductivity,[15,130] electron-phonon,[130] and electron-electron interactions[131,132,133] of 2D materials. It has also ignited the results on interlayer coupling[134,135] and magnetic field[136,137] in 2D materials and heterostructures.

In the present work, we investigated interface-related phenomenon and the electronic structure of graphene in graphene/WS_2 heterostructures, by employing confocal microscopy. Raman spectroscope considering the following two issues. Raman spectroscopy is very useful techniques for investigating chemical interactions and the electronic structure of graphene. It quantifies the vibrational properties at a specific spot with less than 1 μm diameter.

There were added forces from the interactions between layers of *AB*-stacked graphene. The number of graphene layers can be estimated from ratio of peak intensities for *AB*-stacked graphene. I_{2D}/I_G, as well as the position and shape of these peaks can determine number of graphene layers. Single intense 2*D* peak irrespective of thickness may occur in a decoupled multilayer graphene.[138] From Fig. 6.1(b) the value of the ratio I_{2D}/I_G is greater than one, confirming monolayer graphene.[64,139] In pristine graphene, a first order *D* peak is not visible because of crystal symmetries. For a *D* peak to occur is a charge carrier must be excited. They must be inelastically scattered by a phonon. For recombination to occur, a second elastic scattering by a defect (or zone boundary) should happen. The second-order overtone *2D*-mode is always allowed.

Raman is an inelastic phenomena. The energy or frequency or wavelength of incident light is not the same as scattered due to the material on which this light falls. It is a quantum phenomena. When light comes in contact with the material, it either gains by some quanta or loses some quanta. It does so, by interacting with the vibrational modes of the material, called phonons. If it gains

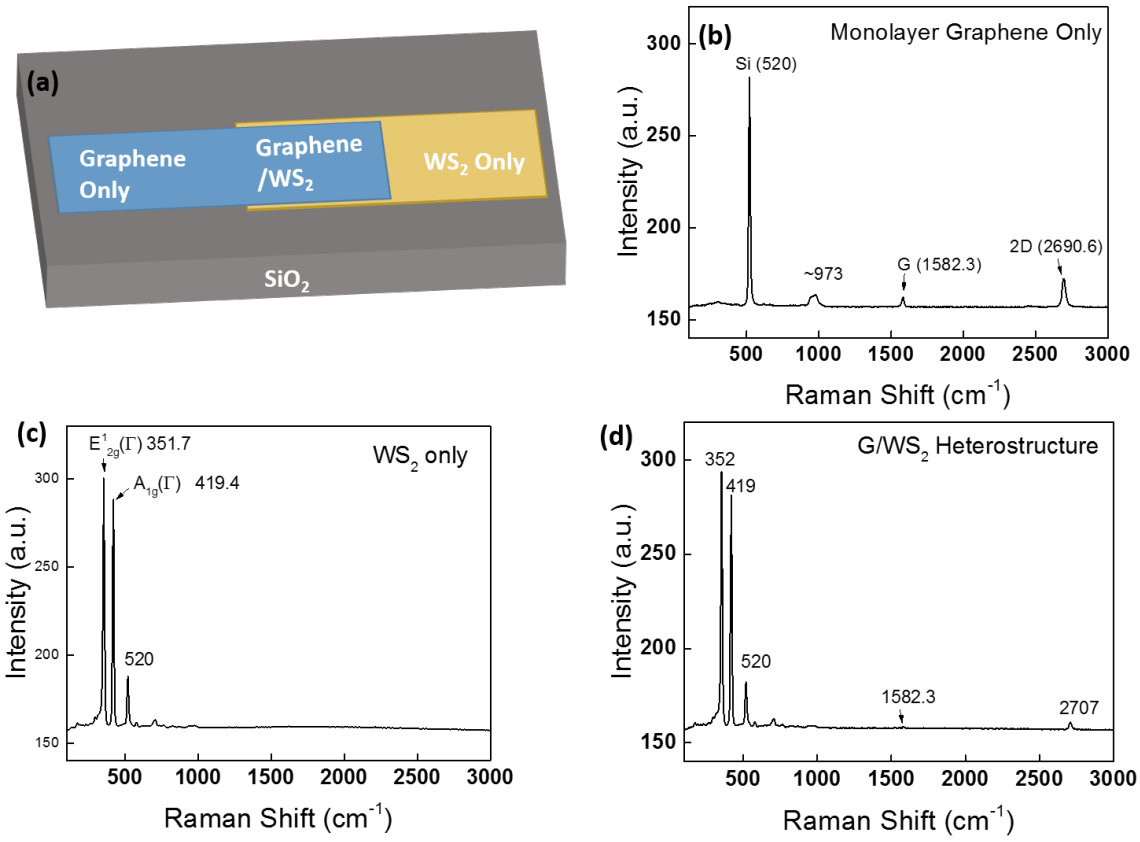

Figure 6.1: (a) Schematic diagram of monolayer graphene/few-layer WS_2 on 300-nm SiO_2 substrate. (b) Raman spectrum for a single-layer graphene sample using a 488-nm excitation laser. Graphene can be identified by the position and the shape of its *G* (1582 cm^{-1}) and *2D* (2691 cm^{-1}) peaks. The *2D* peak involves double phonon scattering either on a single electron/hole or on an electron-hole pair. (c) Room temperature Raman spectrum from a few layered WS_2 region, using 488-nm laser excitation. The atomic displacements for the in-plane phonon mode ${E_{2g}}^1(\Gamma)$ and the out of plane phonon mode $A_{1g}(\Gamma)$ for two adjacent layers. (d) Raman spectrum for monolayer graphene/few-layered WS_2. The *G* peak of graphene diminished and the *2D* peak had lower intensity, reflecting coupling between graphene and the WS_2 layers. There were weak interlayer vdW interactions between graphene and adjacent WS_2 layers. We observed a blue shift of *2D* peak in graphene/WS_2 heterostructure.

energy, it gets blue shifted and if it loses, it is red shifted.

The 2D Raman band of graphene is up- or -down shifted by electron or hole doping, respectively. In contrast, the G band is up-shifted by both electron and hole doping. It is because of nonadiabatic removal of the Kohn anomaly at the zone center.[140,141] The *G* peak experiences a red shift as the number of layers increases.[142] We can thus simultaneously evaluate the amount of charge transfer based on the changes in Raman parameters at the specified spot using confocal Raman system.

Upshift of the 2D band in our graphene/WS_2 heterostructure can be reasoned due to small modification of electronic structure of graphene around *K* point. It is related to upshift of the 2D band through the following process. Changes in the π and π^* band dispersion can affect the wave vector $\mathbf{k}$ which satisfies the relation,

$$\hbar\omega_L = \varepsilon(\pi^*,\mathbf{k}) - \varepsilon(\pi,\mathbf{k}), \tag{6.1}$$

for Raman activation, where $\hbar\omega_L$ is the photon energy of the excitation laser, and $\varepsilon(\pi^*,\mathbf{k})$ and $\varepsilon(\pi,\mathbf{k})$ are the electron energies of the π^* and π at $\mathbf{k}$, respectively. Since the *2D* band is caused by double-resonance process, the wave vectors k and q of electrons and phonons measured from the *K* point satisfy the relationship $q \approx 2k$. In pristine graphene, the phonon energy $\hbar\omega_q$ increases with increases in q near the *K* point. Thus, a change in the π band can influence Pos(*2D*) ($= 2\hbar\omega_q$). In turn, $\hbar\omega_q$ shifts to higher wave number without the significant modification of the phonon dispersion around the *K* point. We proposed that the *2D* band upshift in the graphene/WS_2 heterostructure mainly came from the small but non-negotiable π-band modification induced by the formation of the graphene/WS_2 interface.

We considered the impact of doping on our spectra. An unintentional hole doping to graphene is induced inhomogeneously even within the same graphene sheet. It can be interpreted from the large variations of the Raman parameters that depends on the position of probing laser spot.[119] It has been reported that the peaks of the *G* and *2D* bands show the shift of the peak position and the modification of the spectral features.[143] It occurs when the graphene sheet is transferred onto the

insulator substrate SiO_2.[143] They have pointed out that these spectral changes are closely related to changes in the charge accumulation, and the nature and defect density of the defects. It is, therefore can be consider intentional doping and/or the changes in the graphene nature by our graphene/WS_2 formation, in order to discuss the spectroscopic changes induced even by transferring graphene on WS_2 (TMDCs) properly.

To investigate unintentional doping in graphene sheets, we fabricated a specially arranged specimen composed of the two different regions; the graphene/WS_2 heterostructure region, a pristine graphene region, and a pristine WS_2 [Fig. 6.1(a)]. In the case of graphene/WS_2/SiO_2, no trace of graphene *G* peak and a small sign of *2D* peak is observed [Fig. 6.1(d)]. We believe the reason for the reduced 2*D* peak was that the graphene coupled more strongly with WS_2, a similar vdW materials, than with silicon oxide. We noticed roughness of the graphene surfaces that may simply reflect the contours of the the underlying substrate. We carefully performed forming gas annealing to improve the quality of interface. We concluded that the coupling between graphene and WS_2 may have been strong enough to alter graphene's atomic structure, directly affecting phonon band structure and vibrations.

Heterostructures based on layered materials have attracted a lot attention since the rapid development of graphene, h-BN, and TMDCs. These heterostructures have great potential for applications in optoelectronic devices. However, the performance of these devices is strongly affected by interfacial interactions, which are little understood. Our study will help increase understanding these interactions. Theoretically, the physical properties of a 2D heterostructure can be tailored to meet specific device needs, but more effort is needed to outline principles for engineering functional heterostructure combinations.

6.4 Optoelectronics

The recent advances in nanoscale device fabrication and materials characterization have opened up applications for 2D layers of thin TMDCs in optoelectronics. Semiconducting TMDCs have

sizable band gaps that is different from indirect in bulk to direct in single layers. The electronic band structures of semiconductors influence their property to absorb and emit light. The photons with energy greater than the band gap energy can be absorbed or emitted for direct band gap semiconductors. For indirect band gaps, an additional phonon must be absorbed or emitted to supply the difference in momentum, making the photon absorption or emission process much less efficient. The direct band gaps in single-layer TMDCs allow their use in transistors, photodetectors, and electroluminescent devices, and make them of great interest for optoelectronics. Because they are atomically processable, they have great potential for flexible and transparent optoelectronics.

6.5 Graphene/WS_2 Carrier Transport for Optoelectronic Devices

Several members of the TMDC family, particularly MoS_2 and WS_2, are layered semiconductors. They make natural partners with graphene for optically active heterostructures. The electronic band structures of semiconductors directly influence their ability to absorb and emit light. Their direct band gaps in the visible range make them attractive as the light-absorbing material in alternative thin-film solar cells, including flexible photovoltaics. Thin films of MoS_2 and WS_2 are photosensitive. Strong optical absorption and a visible range band gap (2.1 eV and 1.35 eV for single- and multilayer WS_2, respectively) allow an exceptional photoresponse in graphene-TMDC heterostructures, with large quantum efficiency and photocurrent generation.

The multilayered heterostructures with trap-free interfaces can be formed in 2D vdW heterostructures. TMDCs can be mechanically exfoliated down to single molecular layers. It can be non-invasively physically attached to graphene and still preserves the electronic quality in graphene. This facilitates transport of charge across the interface under the influence of external electric fields. In addition to its field-effect properties, the uniqueness of WS_2, lies in the field-dependent nature of its electronic states. It can be tuned from localized to extended regimes with the gate voltage. Thin films of MoS_2 and WS_2 are photosensitive.

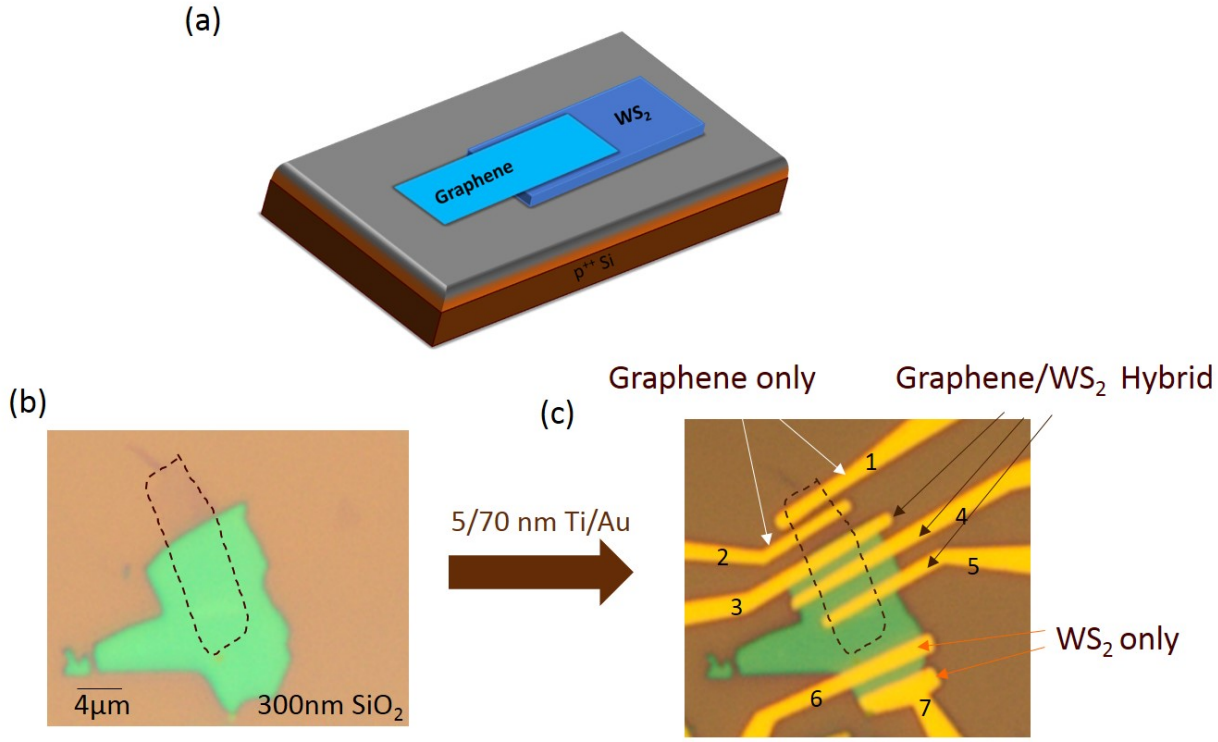

Figure 6.2: (a) Schematic of graphene on few layer WS_2. (b) Optical image of graphene-on-WS_2 transferred flakes on 300 nm SiO_2. Dotted lines indicate the boundary of monolayer graphene. (c) After metal deposition with 5/70-nm Ti/Au, we took a final optical image of the device: between electrodes 1 and 2 is graphene only, 3-4 and 4-5 are graphene-on-WS_2 and 6-7 were WS_2 only. Devices 1-2 and 6-7 were experiment controls.

Understanding graphene-only and WS_2-only optoelectronic devices necessary for understanding graphene/WS_2 heterostructure. We fabricated FETs with a graphene/WS_2 heterostructure and graphene-only and WS_2-only regions of the same layer [Fig. 6.2]. For the graphene-only region, charge neutrality point voltage V_{CNP} was $\sim$-8 V [Fig. 6.3(a)]. We attributed this value to conventional doping attained by transfer methods to make heterostructure. For graphene-only, 2-probe mobility was ~ 300 cm^2/V.s and had negligible photoconductivity due to a very short carrier recombination lifetime. Graphene-only did not show significant photocurrent. The minimum gate-to-source voltage differential that is needed to create a conducting path between the source and the drain terminals i.e. threshold voltage (V_T) was $\sim$-42 V for graphene-only.

To measure the mobility of our bottom gated WS_2/300-nm SiO_2, we used the relationship of drain current to gate voltage for fixed value of drain current and channel length as,

$$I_D = \frac{\mu C}{L^2}(V_G - V_T)V_D, \tag{6.2}$$

where I_D is drain current, μ mobility, V_G gate voltage, V_T threshold voltage, V_D drain voltage, C capacitance and L is the channel length. The field effect mobility (μ_{FE}) is given by,

$$\mu_{FE} = \frac{1}{n}\frac{d\sigma}{dn} \tag{6.3}$$

$$= \frac{1}{c_G}\frac{d\sigma}{dV_G} \tag{6.4}$$

$$= \frac{1}{C/LW}\frac{(L/W)dG}{dV_G} = \frac{L^2}{C}\frac{dG}{dV_G}, \tag{6.5}$$

and

$$\mu_{FE} = \frac{L^2}{CV_D}\frac{dI_D}{dV_G}. \tag{6.6}$$

The 2-probe mobility for WS_2 is $\mu_{FET} = 0.52$ cm^2/Vs. For WS_2 only, current ON-OFF ratio of

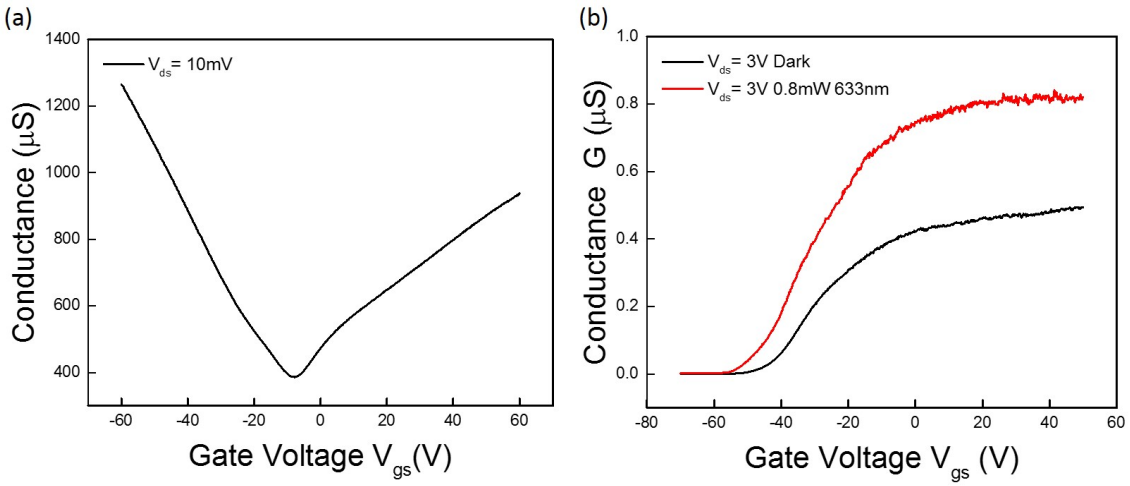

Figure 6.3: Control experiments of graphene-only and few-layered WS_2-only (a) Conductance of bare graphene on 300 nm SiO_2 versus gate voltage (b) Conductance of bare WS_2 on 300-nm SiO_2 vs gate voltage, The G-V_G curve in the presence of light is shown by the solid red line and in dark is shown by black.

10^3. The gate voltage required to change the drain current by one order of magnitude (one decade), termed the sub threshold slope was 5 V/decade for our WS_2-only devices. The WS_2-only photocurrent as shown in Fig. 6.3(b).

When $V_G < V_T$, the Fermi level (E_F) lies deep within the localized states and results in very low conductivity. Although illumination with light results in raising quasi Fermi level of the electrons, it is presumably still stuck within the localized states. Thus free electron carrier concentration in the conduction band is negligible even when the sample is illuminated. However, for $V_G > V_T$, E_F is pushed closer to the conduction band edge which consists of extended states. A slight increase in the quasi Fermi level (as result of illumination) is now detectable as a conductivity change.

6.6 Optoelectronics of Graphene/WS_2 Heterostructures

Many semiconductor structures exhibit a persistent conductivity after photoexcitation has terminated. This persistent photoconductivity indicates long lifetimes. We followed the theoretical treatment given by Queisser et al.[144] who translated spatial separation into time dependence.

Our model relies on the excess number of electrons left behind in graphene at the Fermi energy

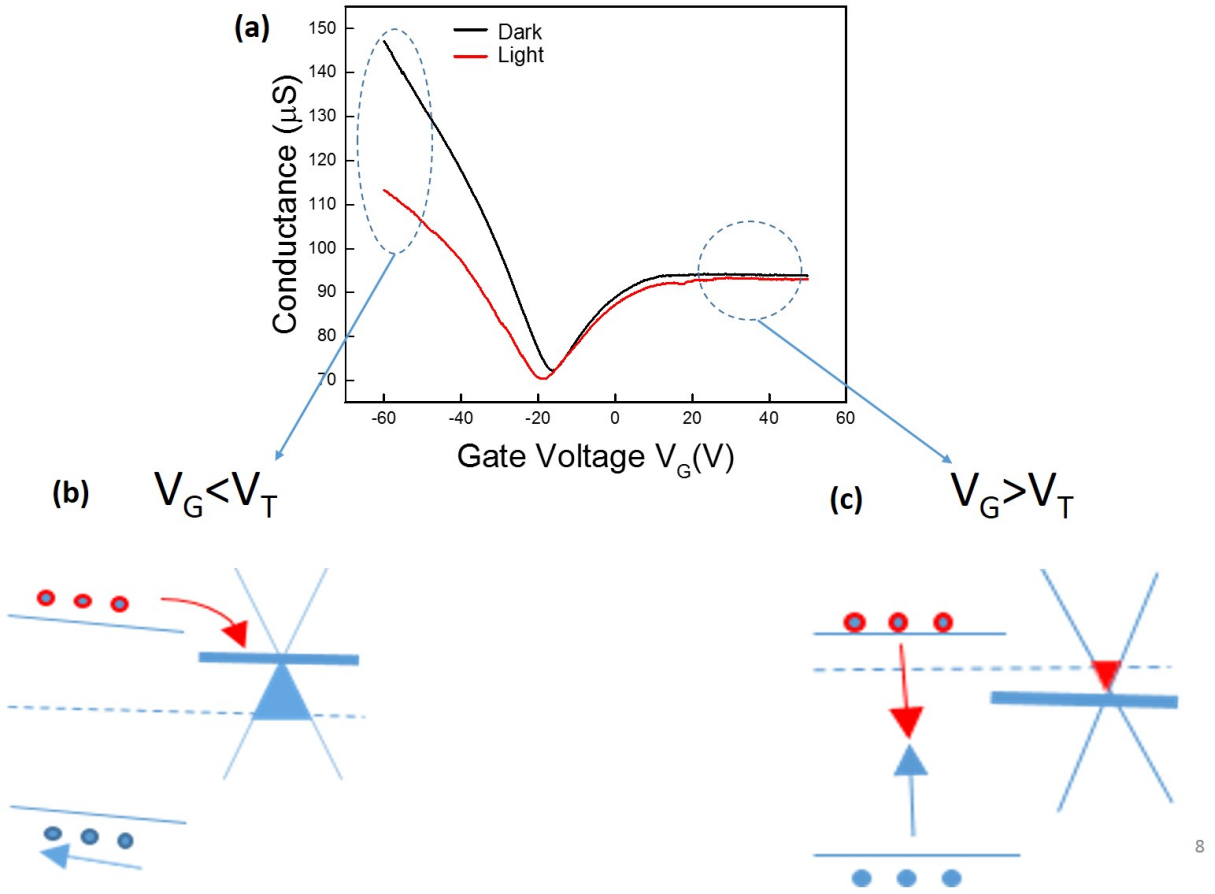

Figure 6.4: (a) The conductance (G)- gate voltage (V_G) curve for monolayer graphene on WS_2. The G-V_G curve in the presence of light is shown by the solid red line and in dark is shown by black. (b) Band bending inside WS_2 when gate voltage is less than threshold voltage ($V_G < V_T$). (c) Band bending inside WS_2 when gate voltage is greater than threshold voltage ($V_G > V_T$)

E_F. These excess electrons are necessarily equal to the number of trapped holes in WS_2 at E_F. This number is proportional to the joint probability of two events: (i) quantum tunneling mediated electron-hole recombination, which results in the time dependent probability density $p(x, t)$ of finding a trapped hole at distance x inside WS_2 from the WS_2/graphene interface at time t, and second, (ii) the probability of thermal excitation of a hole from the hole-doped graphene to WS_2. The latter involves excitation across the energy barrier $\Delta E = -E_c - (-E_F) = E_F - E_c$, where the signs indicate for the excitation of a hole state, and E_c represents the mobility edge.

Two-probe conductance (G) of graphene on WS_2 as a function of gate voltage V_G in Fig. 6.4(a). In the absence of light (black trace in Fig. 6.4(a)) measurements to the left side of the Dirac point showed typical conductance-gate voltage (G - V_G) characteristics of graphene where as on the right side the effect of gate voltage becomes insignificant after some threshold value. This asymmetric response can be explained by WS_2 itself is known to acting as a transistor. The nature of WS_2 changes from dielectric to near-metallic as V_G ranges from very negative to very positive voltages. The value of V_G beyond which the underlying WS_2 transistor turns ON is denoted as V_T. Thus for $V_G \gg V_T$, the metallic nature of WS_2 effectively screened V_G and caused the G - V_G curve of the overlying graphene to saturate beyond a certain value [Fig. 6.4(a)]. There was a pronounced difference between light and dark conditions only on the negative side of the Dirac curve where resistance increased in the presence of light. We inferred that some of the photo-generated carriers created inside WS_2. These photo-generated carriers are transferred to graphene at negative gate biases.

When $V_G > V_T$, WS_2 had a significant metallic character which results in negligible electric field in WS_2. When illumination generated electron-hole pair, a significant percentage of them recombined within the bulk. They recombine before being transferred to graphene. We postulate that this is the reason for diminished photoconductivity for $V_G > V_T$. The difference in the band bending inside WS_2 are shown schematically in Fig. 6.4(b and c). It is the reason for the asymmetry in the photoresponse of the system. Since the graphene work function is lower than the WS_2 work function we neglected the formation of a Schottky barrier in graphene-WS_2 interface. The electric

filed induced inside WS_2 by the gate electric field determines the charge transfer mechanism.

Isolating various 2D materials has created a new paradigm in material science. In this chapter, we demonstrated that the photoactive devices can be made by using graphene/TMDCs stacks. We anticipate that graphene/WS_2 heterostructure can be used for future optoelectronic devices.

6.7 Conclusion

We investigated the interactions of single layer graphene with WS_2 is investigated for the graphene/WS_2 heterostructure fabricated by transferring graphene on WS_2. Changes of Raman parameters and optoelectronic properties in the heterostructures with WS_2 and graphene reveals the following: (i) Characteristics of charge carrier doping in single layer graphene, carrier doping in graphene and the type of doped carriers i.e. electrons, governed by the interfacial interactions, (ii) There are specific interface interactions in graphene/WS_2 heterostructure. Reduced $2D$ peak intensity in graphene/WS_2 indicates the graphene coupled more strongly with WS_2, a similar vdW materials, than with silicon oxide, and (iii) We inferred that the photo-generated carriers created inside WS_2 were transferred to graphene at negative gate biases. When electron-hole pairs were generated as a result of illumination, a significant percentage of them recombined with the WS_2 before being transferred to graphene. We postulate that this is the reason for diminished photoconductivity when $V_G > V_T$.

We believe the present study provides important information for improving the performance of graphene-based devices. This work exemplifies the evolution of structural parameters in layered materials when changing from one 2D material to a 2D-heterostructure regime. Heterostructures have great potential for applications in optoelectronic devices, however, the performance of these devices is strongly affected by interfacial interaction. Our study will help in understanding these interactions further.

Chapter 7

Summary of Results and Future Directions

7.1 Introduction

Classic metal-oxide-semiconductor field-effect transistor (MOSFETs) are the building blocks of the microelectronics industry. Microelectronics have changed our society in ways that no one could have predicted 50 years ago. Nevertheless, classical devices are reaching their functional limits, and innovations in material sciences are necessary for further technological advancement. The transition to the next generation of devices poses design and fabrication control challenges.

Gordon E. Moore[3] co-founded Intel and Fairchild Semiconductor predicted that the density of integrated circuits on transistors would double approximately every 18 months. Multigate transistors were fabricated in early 1990s. They were largely considered exotic devices worthy of academic research, but not suitable for industrial mass production. Yet planar MOSFET scaling is reaching its limits and study of short-channel effects in various materials and architecture is necessary. Short-channel effects cannot be controlled using modern devices using conventional transistor architecture. A lot of Intel's publications on tri-gate devices deal with silicon-on-insulator (SOI) devices, but Intel decided to move forward with bulk substrate instead of SOI substrate for its 22-nm tri-gate process, in May 2011. The company foresees that this will reduce costs and minimize self-heating problems, since SOI devices require thermal insulation from substrate by

buried oxide.

Research on two-dimensional (2D) materials and their heterostructures is exciting and can pave the way for continued use of planar MOSFET devices. The compactness of atomically thin 2D materials could make it possible to realize extremely compact circuit element. In January 2013, the European Union announced graphene as a billion euro technology to advance the development of the revolutionary material. The scientific research would need to work with industry and market leaders to ensure development progresses towards industrially viable applications. Semiconductor giants like Intel, Lam Research Corporation and Applied Materials, are also making huge efforts to develop technology based on 2D materials for their next generation products.

7.2 Experimental Results in the Context of Transistor Literature

7.2.1 Device Fabrication

We addressed issues related to heterostructure device fabrication. We performed experiments designed to optimize annealing conditions and to visualize single- and few-layered 2D materials on substrates. We found two important results while experimenting with h-BN thermal annealing: (i) Annealing exfoliated h-BN on SiO_2 at 750 °C gets rid of scotch tape residues from the h-BN as well as the SiO_2 substrate. Forming gas annealing resulted in optically clean surfaces that often still had small amount of residue. (ii) We used SEM to detect remaining residue. We observed that residue could be completely cleaned by our thermal annealing conditions. Using thermal annealing and SEM imaging to detect residue adhesive is effective for creating residue free 2D materials on substrate.

It is difficult to visualize 2D materials on WS_2/SiO_2 substrates. Using the concept of Fresnal theory, we demonstrated that the contrast of monolayer WS_2 is maximized at 540 nm and 633 nm on 300-nm SiO_2. Conversely, we observed no sharp and high contrast on 200-nm or 90 nm SiO_2

substrates. We extended the Fresnal theory to four interfaces between air/PMMA/WS_2/SiO_2 order to identify the thickness of WS_2 flake to be transferred. We found that 90-nm, 225-nm and 375-nm PMMA thickness gives maximum contrast of monolayer WS_2. We anticipate that this technique will be very useful in the field for 2D material identification. For any material and substrate, parameters can be identified to find monolayer or few-layer material.

7.2.2 Hexagonal-Boron Nitride as a Substrate

The atomically layered materials[94,16,70] and their heterostructure[145,146] have been researched for decades. The research in this dissertation was possible because of recent resurgence in scientific community.[29,14] It can be attributed to, (1) recent advances in sample preparation,[19,146,1] and (2) transfer of 2D materials to form heterostructure.[147,148]

Hexagonal boron nitride (h-BN) is an attractive substrate material because of its physical properties compared to SiO_2. h-BN is an atomically smooth surface providing comparatively free of dangling bonds and trap charge material. We researched the effects of h-BN on device performance and found two important results. First, h-BN can be used with TMDCs as a substrate to improve current ON-OFF ratios and subthreshold swings (*SS*). In comparison to devices made from same WS_2 flake on SiO_2 but without h-BN, the devices on h-BN had lower OFF-currents. However, their similar ON-currents meant an improved current ON-OFF ration by about an order of magnitude. It is interesting to note that in spite of smaller total oxide capacitance in these devices due to additional h-BN layer, we obtained values of *SS* on h-BN devices similar to the values for devices with WS_2 on SiO_2 only.

Second, compared to liquid electrolytes, h-BN serves as a relatively low capacitance substrate that can achieve ambipolar behavior. Our studies reports the first ambipolar WS_2/h-BN transistors. Semiconductor FET devices can operate in both the electron- and holde-accumulation modes, depending on the polarity of the gate voltage. When we applied positive gate voltage, WS_2 acted as an n-type material and when we applied negative voltage, it behaved as p-type material.

We attribute the ambipolarity mainly to low interface trap charges. The carrier density n is

related to finite density of states in the band gap due to defects in materials or at interfaces. At interfaces, the charge is populated in localized states inside the band gap. We measured the interface trap density in h-BN/SiO_2. The value is less than 8×10^{11} cm^{-2} at $V_D = 10$ mV within the entire band gap including the possible trap in thick SiO_2 oxide. Our h-BN/SiO_2 capacitance was small, so the change of the Fermi level ΔE_F and the term $e\,\Delta V_{GAP}$ can be approximated. In the literature, ambipolar behavior has been achieved only with high gate voltage[89,97] Our study illustrates a process for acquiring low trap charge heterostructures and able to see ambipolarity even at low backside gate capacitance unlike only so far achieved at high gate voltage.[89,97] However, more work is required to minimizing surface trap density in the energy gap with an additional concern for matching suitable contact metal for both branches.

In future, transferring and annealing conditions of h-BN can be improvised utilize h-BN as better substrate. The quality and doping of h-BN can be tuned to make TMDCs/h-BN heterostructure of desired electronic and optoelectronic properties. As transistors become ever smaller, h-BN is probably one of the best material to use as the dielectric layer in such miniature electronic components.

7.2.3 Electrical Properties of our 2D and Their Heterostructure devices

We are the first researchers to characterize the full range of properties of 2D material FETs. To begin, electrostatic screening in TMDCs were not explored in literature.[66,149] Our study is first such study of 2D materials. Due the nature of charge transport in layered materials, the effects of classical and quantum capacitance becomes important. Using a discrete model,[150] we studied charge screening normal to the layers in TMDCs. Our model fit well with our few-layer WS_2/SiO_2 FETs. We found that (i) the band position α relative to the Fermi level of each layer varied by the carrier density due to quantum capacitance, (ii) at the low charge-density limit in the TMDCs, charge carriers tended to distribute uniformly and the band energy position of each layer is the same. With a decrease in the gate voltage, all layers turned off simultaneously, and (iii) a high charge-density limit, charges carriers tended to accumulate in layers near the gate and the band energy position of

each layer was altered according to its quantum capacitance (i.e. carrier density).[37] This study is extremely important to understand basic physics of 2D material carrier transport.

In our WS_2 /SiO_2 devices the current ON-OFF ratio of 10^5 was achieved at merely low drain voltage of $V_D = 10$ mV. To our knowledge, this is best current ON-OFF ratio. We find no significant hysteresis in back-gated 2D devices at such low V_D. We observed in the OFF-state the interface trap density ($< 10^{12}$ cm^{-2}) is a limiting factor for the gate voltage required to change the drain current by one order of magnitude. We compared the behavior of sets of FETs with various channel thicknesses. We revealed that the charge density depends on gate voltage. We find that unlike the 3D materials, the quantum capacitance related to the density of states in layers is important in electrical transport due to its 2D nature regardless of the device thickness. Further, four-probe measurement revealed strong gate-voltage dependence.

We analyzed device dependence on thickness of the TMDC. We fabricated an entire set of WS_2 devices made with the same fabrication process and on same substrate. We observe very comparable values of *SS* from 450 to 670 mV/decade on all of the devices. We realize that our samples had few defects and impurities, unlike the case of MoS_2, and our WS_2 devices reached a low interface trap density. This finding implies flexibility of thickness of 2D material for device performance. To model 2D material FETs, we considered that the system behaves like a capacitor network consisting of the C_{ox}, C_{it}, C_α with $\alpha = 1$ to N, and C_{il}. We found, that the quantum capacitance of an individual layer differed significantly from the value of C_0 depending on the position of the Fermi level relative to the band edges. We acquire the best-fit parameters in the full range of electron conduction, i.e. trap density $\approx 6\times10^{11}$ cm^{-2} spread over a width ≈ 0.2 eV residing at ~ 0.12 eV from the bottom of the conduction band. These values were in agreement with the thermally activated energy found in WS_2. Our capacitive model validated by our experiments is extremely important to the field for basic understanding of carrier transport in 2D FETs.

Energy efficient and low power consumption are required for high performance devices in the semiconductor Industry. In the silicon industry, devices with steep *SS* are desirable since they result in low power consumption from lower voltage and reduced leakage current. Power dissipation is

a big roadblock in front of the IC technology's ever increasing march toward an ever higher level of integration. *SS* is defined as the gate voltage required to change by one order of magnitude (i.e., per decade). In prior studies nearly ideal *SS* results have only been achieved by increasing the oxide capacitance, for example, top-gated systems employing high-κ[70,94] with much smaller thicknesses, or in electric double layers[89] formed by liquid electrolytes.

We made energy efficient heterostructure devices on 10-nm SiO_2. We successfully obtained *SS* values of about 70 mV/decade, very close to the theoretical limit of a TMDC-based FET at 300 K even in the presence of contact resistance. This is the first demonstration if such steep *SS* in a TMDC-based device fabricated with back-gate geometry. Compared to the D_{it} we found on 300-nm SiO_2, our 10-nm SiO_2 device reached a lower total interface trap density. Assuming similar interface trap densities between WS_2 and SiO_2, the thin oxide likely had lower surface defect density than the thick one. We expect our results to have a valuable impact on the field by carefully designing interface trap charges, energy efficient devices with the best possible *SS* can be achieved.

We created field-effect transistors with multilayer, two-dimensional semiconductor WS_2 as the conductive channel and 300-nm SiO_2 as the back gate insulator. We showed a comparison of WS_2 for different channel lengths. We used the devices to study performance of WS_2 short-channel transistors. Although our devices were fabricated on a 300-nm thick SiO_2 gate dielectric, we demonstrated their superior immunity to short channel effects as small as 400-nm channel lengths. We observed a similar value of saturation current but a sharp increase in DIBL for the device with a channel length smaller than 400-nm channel length. We also performed transport studies and observed a field-effective mobility decrease and maximum current saturation attributable to carrier velocity saturation. To understand high-performance WS_2 short channel transistors, a comprehensive study on metal/WS_2 junctions is required. Thus, our study could be extremely important for the use of 2D materials in new technology nodes.

We investigated the interactions of single layer graphene with WS_2 is investigated for the graphene/WS_2 heterostructure fabricated by transferring graphene on WS_2. Changes of Raman

parameters and optoelectronic properties in the heterostructures with WS_2 and graphene revealed characteristics of charge carrier doping in single layer graphene, carrier doping in graphene and the type of doped carriers i.e. electrons, governed by the interfacial interactions. There are specific interface interactions in graphene/WS_2 heterostructure. Reduced $2D$ peak intensity in graphene/WS_2 indicates the graphene coupled more strongly with WS_2, a similar vdW materials, than with silicon oxide.

We inferred that the photo-generated carriers created inside WS_2 were transferred to graphene at negative gate biases in our graphene/WS_2 optoelectronic devices. When electron-hole pairs were generated as a result of illumination, a significant percentage of them recombined with the WS_2 before being transferred to graphene. We postulate that this is the reason for diminished photoconductivity when $V_G > V_T$. We believe the present study provides important information for improving the performance of graphene-based devices. This work exemplifies the evolution of structural parameters in layered materials when changing from one 2D material to a 2D-heterostructure regime. Heterostructures have great potential for applications in optoelectronic devices, however, the performance of these devices is strongly affected by interfacial interaction. Our study will help in understanding these interactions further.

7.3 Future Work

In the next few years, access to high-quality samples will enable more researchers to investigate the physical and chemical properties of TMDCs, and heterostructures of these layered materials as well as pursue a wide variety of applications. The vision driving the construction of vdW heterostructures is, the ability to precisely engineer heterostructure. These devices can reveal entirely new physical phenomenon. The design of tailor-made materials that can not be generated by classical high-temperature solid-state chemistry. The commonality in these two goals is, the ability to sculpt and create new materials at will. If it can be done at an unprecedented level, we can control the form of the smallest building blocks we can imagine, 2D layers.

The choice of next-generation 2D materials and their heterostructure is restricted by the required anisotropic nature of respective bulk materials. It means, strong covalent bonding within the layers held together by weak interlayer interactions. Individual layers from the parent bulk crystal needs to be isolated with minimum structural disruption. Also, low number of defects is usually achievable only by mechanical exfoliation from layered vdW solids. It features very weak dispersive interactions between the layers (~ 40 - 70 meV). In future, the bottleneck of only focussing on vdW solids can be achieved by considering another class of materials. One such example is ionic layered materials that have alternative anisotropic bonding modes.

In the next few years, progress in the 2D semiconductor field will require advances in understanding of electron transport in layered materials, and the effects of quantum capacitance, as well as the development of defect-free devices. Achieving these goals will be very important for describing phenomena governing good electrical contacts based on band alignments and the interactions between electrodes and layered materials. Charge injection between metals electrodes and vdW systems can be probed into by extending the theoretical model we have established in Chapter 3. In layered materials 2D TMDCs have many distinctive properties that are not seen in other materials systems, and as researchers learn more about them, there are sure to be unexpected and exciting applications.

Most importantly, advances in scalable and controllable sample preparation are needed to allow large amount of atomically thin and uniform layered materials for use in the semiconductor industry. These will include new crystal growth methods to achieve large surface areas, large grain sizes, uniformity and control of layer number. The properties and applications of layered materials like TDMCs are a relatively new but rapidly expanding area of research.

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