High-Power T/R circuits for a Multichannel VHF/UHF/HF Ice Imaging Radar

By

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Abstract

This thesis presents the design and implementation of high-power wide-bandwidth transmit/receive (T/R) switches and modules for use in multi-channel ice-penetrating imaging radars. The switches were designed to address the lack of standard off-the shelf (COTS) devices that meet our technical requirements.

The design of these switches was accomplished using electronic design automation (EDA) tools and implemented with quadrature hybrids and actively-biased PIN diodes. Three different circuits were developed for three different frequency bands: 160-230 MHz (VHF band), 150-600 MHz (VHF/UHF), and 10-45 MHz (HF band). The circuits are capable of transmitting at least 1000 W of peak power and exhibit an insertion loss lower than 1.3 dB for 160-230 MHz, 1.6 dB for 150-600 MHz, and 2.39 dB for 10-45 MHz ranges. A fourth, miniaturized prototype for the 160-230 MHz range was implemented for use in future multi-channel systems. The circuits developed exhibit turn-on times better than 1.3 μs for the VHF/UHF circuits; and 1.5 μs for the HF circuits. The turn-off times were better than 200 ns for the first two bands and 1.36 μs for the HF band. Both the VHF and VHF/UHF have been demonstrated in field operations with two different radar systems.

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Chapter 1: Introduction

1.1 Motivation

Airborne radars with synthetic aperture radar (SAR) capabilities operating at HF, VHF, and UHF are a powerful tool for measuring ice thickness and imaging its internal structure [3,7,19]. Such radar systems are often equipped with antenna arrays in the cross-track direction to enable advanced array processing techniques that reduce the effects of surface clutter in areas where the ice surface is rough [17,24,12,9]. In some configurations, it is desirable to time share the same antenna elements for transmit/receive operations, which requires a transmit/receive (T/R) switch or duplexer[1].

Figure 1 shows an illustration of the operation of an airborne ice sounding radar with transmit/receive capabilities.

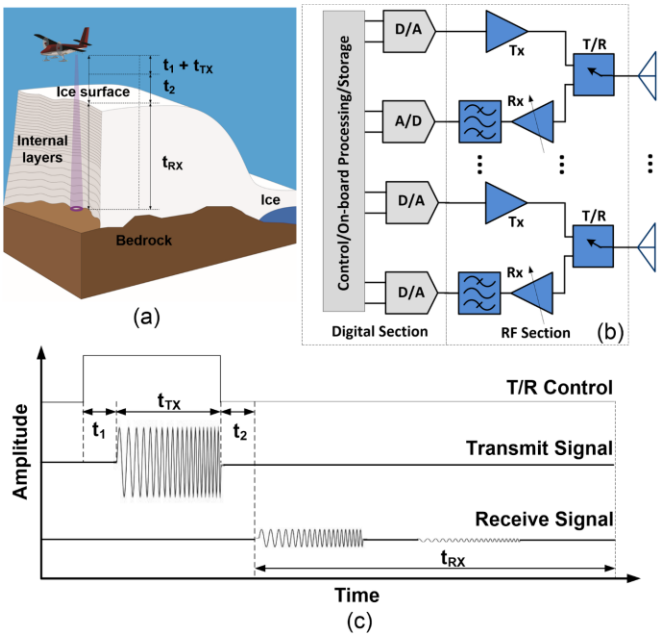

Figure 1.1: : (a) Illustration of airborne ice sounding radar; (b) Simplified system block diagram (c) Transmit/receive timing diagram [14]

[1] The term duplexer is not to be confused with diplexer, a circuit that distributes power to different ports based on their frequency [23].

The aircraft flies at a constant altitude above the ice surface while it illuminates the target. During transmission, the digital section generates a signal, t_{TX}, which is amplified and transmitted through the antenna. The T/R switch ensures that the amplified signal is outputted through the antenna with minimal insertion loss. The switch also protects the receiver from the high power transmitted signal by providing high isolation between transmit and receive sections.

During receive mode, the reflecting signal of the surface is collected by the antenna and fed into the receiver. The T/R switch ensures that the antenna signal gets to the receiver with minimal insertion loss and high isolation from the transmitter.

The timing between transmit and receive modes of the T/R switch is controlled by the T/R control signal, as shown in Figure 1c. The antenna transmits when the T/R control signal is high and receives when the T/R control signal is low. Turn-on time, t_1, is measured from 50% T/R control to 10% and turn off time, t_2, is measured from 50% T/R control to 90% RF at the receiver. The goal is to minimize the turn-on time, t_1, the time it takes for the radar to be ready to start transmitting, and turn off time, t_2, so that the receive time window is maximized.

The aircraft has a set flight altitude of 500 m above the surface. In order for the antenna to detect signals at 500 m, the switching of antenna between transmit and receive mode has to be less than 2.3 μs for a 1 μs transmitted pulse. Short pulses (1 μs) are used to map the ice surface and shallow internal layers, while longer pulses (3 μs, 10 μs) are used to map ice-bedrock interface and deep internal layers [14]. Mapping of internal layers and bedrock requires high power and resolution, which is inversely related with bandwidth. High bandwidth leads to better resolution.

Traditional solutions for T/R switches were limited by power, bandwidth, or switching time. Some examples are shown in Table 1.1 below .

Table 1.1: Summary of Recent ice-sounding radars with T/R capabilities

Reference	# of elements	Center Frequency	Bandwidth	Pulse Duration	Duty Cycle	Peak Power (per channel)	Average power (per channel)
A low-cost glacier-mapping system [3]	1	60 MHz	4 MHz	250 ns	0.25%	600 W	1.5 W
ATRS [17]	2	60 MHz	15 MHz	1 µs	0.64 %	7 kW	44.8 W
Multichannel Coherent Radar Depth Sounder/Imager (MCoRDS) [19]	8	195 MHz	30 MHz	1-30 µs	12 %	250 W	30 W
Multichannel Coherent Radar Depth Sounder/Imager4 (MCoRDS) [24]	8	320 MHz	260 MHz	1,3,10 µs	12%	250 W	30W

The radar system, described in "A low-cost glacier-mapping system", was limited by the power and bandwidth. It contained 1 antenna element capable of transmitting 1.5 W of average power and had a bandwidth of 4 MHz [3]. The system was used for mapping ice sheets in Greenland and Antarctica. The Advanced Technology for Radar Sounding of Polar Ice (ATRS) system had 2 antenna elements and was capable of transmitting 44.8 W of average power per channel with a bandwidth of just 15 MHz [17]. Previous versions of MCoRDS have supported 8 elements but have only been able to transmit 30 W of average power. Previous versions also had slow turn off times of 4.2 µs and turn on times of 2.4 µs.

The following section describes three different T/R switches capable of transmitting 1 kW peak power with high bandwidth and fast switching times. These were developed to improve radar sensitivity and allow operation at lower altitudes.

1.2 This Work

This thesis presents the design of three different T/R switch optimized for ice penetrating radar operating at three different frequency bands: 160-230 MHz (VHF band), 150-600 MHz (VHF/UHF), and 10-45 MHz (HF band). These frequencies were dictated by the operating frequency of the radar system for which they were developed. Table 2 shows a summary of relevant specifications of the three T/R switches developed as a part of this thesis. A fourth prototype was implemented to demonstrate miniaturization and integration of the VHF band T/R switch into a smaller package.

Table 1.2: Summary of Relevant specifications of the circuits developed in connection with this thesis

Frequency Band	Radar System	# of elements	Center Frequency	Bandwidth	Pulse Duration	Duty Cycle	Peak Power (per channel)	Average power (per channel)	Switching Time
VHF	MCoRDS	6-8	190 MHz	70 MHz	1,3,10 µs	15%	1000 W	150 W	1.3 µs
VHF/UHF	UWB ICE	6-8	375 MHz	450 MHz	1,3,10 µs	15 %	1000 W	150 W	1.3 µs
HF	HF Sounder	1	15 or 35 MHz	1 MHz	1 µs	1.2 %	1000 W	20 W	1.5 µs

The designs are based on the balanced configuration proposed by Cofrancesco et al [4] and later expanded by our group [24]. They use 90° quadrature hybrids and actively-biased PIN diodes[2]. Besides achieving wider bandwidth and increasing peak power handling capability, the switching time of the newly developed circuits has been significantly improved. For the VHF and VHF/UHF circuits, the turn-on time is 1300 ns and turn-off time is 200 ns. The initial prototype developed for the HF band has a turn on time of 1.5 µs and a turn-off time of 1.35 µs. This is much faster than traditional high power T/R switches which could have switching time as high as 10 µs [1] and 7 µs [21].

Advanced Design Systems (ADS) was used to perform low level, high level, and circuit/electromagnetic co-simulations on each circuit. The designs were then manufactured and tested. Two of the circuits

[2] An earlier version without active biasing was implemented by R. Crowe [5]. However, this was limited to only 100-W of peak power.

developed have been used in the field for extensive operation. The last two prototypes can be integrated in future systems after some additional optimization.

1.3 Thesis Outline

The thesis is divided into seven chapters. Chapter 2 gives an overview of the T/R switch design, previous work that has been done on this topic, and design requirements for T/R switches. Chapters 3, 4, and 5 explain the designs of VHF, VHF/UHF, and HF T/R switches, respectively. The miniaturized version of VHF T/R switch is described in chapter 6. Chapter 7 presents conclusions and discusses future work.

Chapter 2: Background

2.1.1 T/R Switch Design Overview

A block diagram of a T/R switch is shown in Figure 2.1. This design builds on the T/R switch used in MCoRDS4, as described in "Multichannel Wideband Synthetic Aperture Radar for Ice Sheet Remote Sensing: development and the First Deployment in Antarctica" [24], did not incorporate active biasing of the switching elements. This design consists of four main parts: quadrature hybrids, PIN diodes, RF blocking inductor, and DC blocking capacitor.

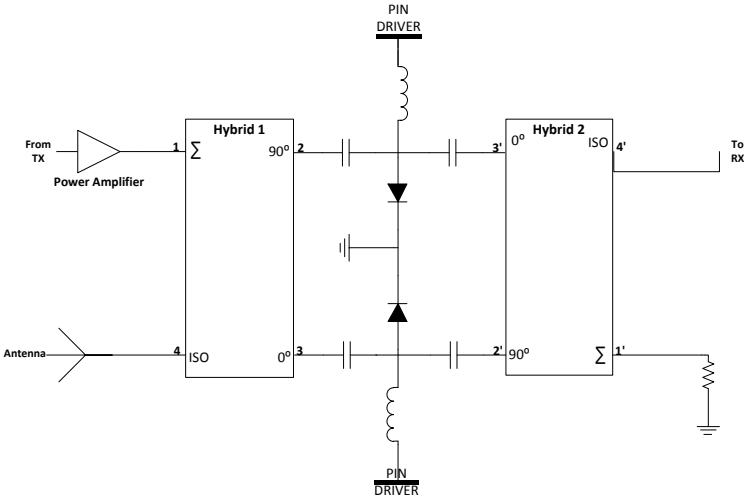

Figure 2.1: T/R switch block diagram

During transmission, the signal generated by the digital system is amplified and injected into port 1 of Hybrid 1. The signal is split equally into in-quadrature (I/Q) and phase components at ports 2 and 3 of the quadrature hybrid. During transmission mode, the diodes are forward biased, which reflects the RF signal back into ports 2 and 3 of the Hybrid 1. The signals adds constructively at port 4 and is transmitted through the antenna.

In transmission mode, there needs to be high isolation between the receiver port, port 4', power amplifier and antenna ports, and ports 1 and 4 in order to lower the power of the feedthrough signal, which can damage or saturate the receiver.

During receive mode, the signal coming from the antenna has to be driven into the receiver with minimal loss. The received signal from the antenna is driven into port 4 of the hybrid where it is split equally into in-quadrature and phase (I/Q) components at ports 2 and 3 of the quadrature hybrid. In receive mode, the diodes are reverse biased, which allows the signals coming from ports 2 and 3 to be driven into ports 3' and 2', respectively. The signal then adds constructively at port 4' and is provided to the receiver.

In receive mode, it is essential to have low insertion loss between the antenna port, port 4, receiver port, and port 4' since the power level of the received signal obtained from the antenna is low. Having high isolation between the power amplifier port and antenna and receive ports prevents any additional noise from coupling with the received signal[3].

The biasing of the PIN diodes is done through a driver circuit. A transistor – transistor logic (TTL) signal provided by the digital system is injected into the driver circuit. The driver circuit conditions the signal to necessary voltages and currents to drive the diodes between forward and reverse bias stages. In this

[3] Ideally the power amplifier is completely turned-off during transmit, however, high power amplifiers may not be completely turned off after the transmit even, which drives the requirement for high isolation during receive.

particular case, the T/R switch is in the transmit state when the control line is set to “high”. Conversely, it is in receive mode when the control signal is set to “low”. A timing diagram that illustrates this is shown in Figure 1c. To reduce the switching time between transmit and receive modes, the driver provides a negative voltage to the PIN diodes when switching between forward and reverse bias modes.

To prevent RF signal from entering the driver circuit and the DC signal from entering the hybrid, RF choke inductors and DC blocking capacitors are used as well, as shown in Figure 2.1. This part of the circuit is also referred to as “bias tee”.

2.2 Previous Work

The balanced duplexer topology with active biasing has been used for radar and nuclear magnetic resonance (NMR) applications. All systems developed in the past using this configuration were either limited by bandwidth, power, or switching time.

Cofrancesco et al. [4] describes a NMR duplexer for frequency range of 90 – 500 MHz capable of handling 0.5 kW RF power. The duplexer had a 1.3 dB insertion loss in receiver mode and 7 dB insertion loss in transmit mode. Agarwal et al. [1] describes a duplexer made for atmospheric radars operating at 53 MHz and capable of transmitting 120 kW peak power and 3 kW average power. Switching was done using four PIN diodes biased through a driver circuit that was driven with a pulse. Turn off time for the duplexer was 7 µs. Vaughan et al. [21] describes the transmitter and duplexer designed for NMR application. It was capable of transmitting 15 kW of peak power and 750 W average power over the frequency ranges of 40 – 80 MHz and 160 – 180 MHz. It had a switching time of 10 µs.

Lemette et al [10] describe a T/R switch built for use in an air defense radar. The T/R module was capable of handling more than 1.2 kW peak power and 180 W average power. Rodriguez-Morales et al. [19] outlines a radar system operating over 160 – 230 MHz capable of transmitting 250 W of peak power. Wang et al. [24] outlines a radar system for measuring ice sheets operating over the frequency

range of 190 – 450 MHz and capable of transmitting 250 W of peak power. Crowe [5] discusses the use of circulators along with the duplexer used in NMR application [24] to achieve 50 dBm of transmitted power with a 4 ns switching time.

2.3 Design Requirements

Each T/R switch has to sustain up to 1 kW of peak power and up to 150 W of average power over the specified frequencies during the transmit stage. The T/R switch developed for HF frequencies has to sustain at least 20 W of average transmit power. Low loss and high isolation are also required, depending on the state of the switch.

Lastly, switching between transmit and receive states has to be done in less than 2.3 μs in order to keep the blind range less than 500 m[4]. More specific details on specifications, design considerations, and performance of each design will be presented in the ensuing chapters.

Chapter 3: 150-600 MHz T/R switch

This chapter discusses the design and implementation of a high-power transmit/receive (T/R) switch for a frequency range of 150 to 600 MHz. The design is based in the balanced duplexer introduced in Chapter 2. The circuit was further integrated into a bank of switches and ultimately deployed with the CReSIS UWB ice radar during the 2015 spring campaign (onboard the NASA C-130) and during the 2015 test campaign (onboard a Basler aircraft).

3.1 Design Requirements

The primary design requirements for this version of the T/R switch are summarized in the Table 3.1.

[4] The turn on time is typically measured from 50% T/R control to 10% RF and the turn off time is measured from 50% T/R control to 90% RF.

Table 3.3: Design requirements for 150 - 600 MHz T/R switch

Frequency	150 – 600 MHz
Peak power	1000 W
Average power	150 W
Insertion loss during transmit	< 1.5 dB
Isolation during transmit	> 60 dB
Insertion loss during receive	< 1.5 dB
Isolation during receive	> 40 dB
Switching time between transmit and receive	< 2.3 µs

The T/R switch operates between 150 - 600 MHz and handles up to 1000 W of peak power and 150 W of average power for 15% duty cycle. Low insertion loss is required between the power amplifier and antenna and high isolation between the power amplifier and receiver when transmitting for the entire frequency range. During receive mode, low insertion loss between the antenna and receiver and high isolation between power amplifier and antenna and power amplifier and receiver is required. Isolation requirements are based on protecting the receiver from the power amplifier during transmission and protecting the integrity of the low powered signal during receive mode. Switching time between transmit and receive has to be less than 2.3 µs for a 1 µs pulse length in order to keep the blind range less than 500 m.

3.2 Design Overview

3.2.1 Design description

Figure 3.1 shows the block diagram of the T/R switch. Three ports are available to the user: denoted PA (power amplifier input); ANT (antenna input/output); and Rx (output to the receiver), respectively. The design consists of two quadrature hybrid couplers, one series PIN diode in the transmit path, three shunt PIN diodes, and a termination resistor along with DC blocking capacitors and RF chokes. For protection of the receiver and improved performance, a limiter, a high pass filter and an isolation switch were also integrated into the design.

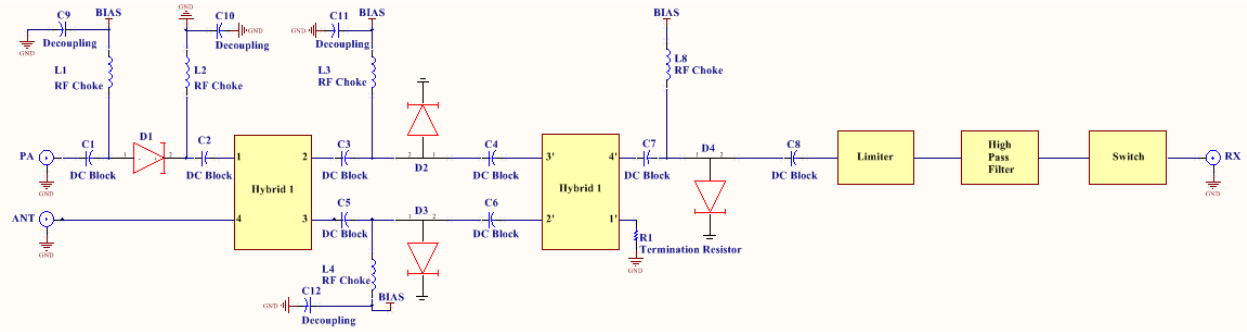

Figure 3.2: Schematic diagram of the 150-600 MHz T/R switch

The basic principle of operation of the circuit is as follows: In transmit mode, the signal from the power amplifier is injected into the PA port. The signal first encounters the series diode switch, D1, which is forward biased with a constant current, presenting a low impedance to the RF signal. The signal then passes to port 1 of the quadrature hybrid coupler (denoted Hybrid 1). The signal is split equally into in-quadrature and phase (I/Q) components at ports 2 and 3 of the quadrature hybrid. Shunt diodes D2 and D3 are forward biased, presenting a reflective low impedance to the RF signal, which is then fed back into ports 2 and 3. The reflected signals are then recombined at port 4 of Hybrid 1, which is connected to the antenna. Shunt diode, D4, is also be forward biased. D4 together with the isolation switch provide extra isolation between the receiver and power amplifier during the transmit event.

In receive mode, the signal from the antenna enters port 4 of Hybrid 1 and is split equally in I/Q components at ports 2 and 3. The shunt diode switches, D2 and D3, are reversed biased, behaving essentially as an open circuit. The I/Q signals enter ports 3’ and 2’ on hybrid 2, where they recombine at port 4’. D4 is reversed biased and the signal passes through the limiter, high pass filter, and an isolation switch before entering the receiver. Series diode D1 would be reverse biased to provide extra isolation between power amplifier and the rest of the circuit. A 50 ohm resistor is also present at port 1 of Hybrid 2 to terminate any residual power caused by phase imbalances in the hybrids.

The switching between transmit and receive states is accomplished by means of a driver circuit controlled by a digital pulse. Specific details regarding the driver circuit will be given in Section 3.4.

A limiter is used to protect the receiver from unexpected transients and high power signals. The limiter allows certain power below a threshold to pass with minimal insertion loss. Switching the diodes causes a transient response which creates low frequency transients that can affect radar performance. To suppress these transients, a high pass filter was added to the receiver chain. Finally, an isolation switch was incorporated into the receiver chain to increase isolation between receiver and the power amplifier during transmit. The switch is controlled by the same logic controlling the PIN diodes.

To allow for broadband high-power operation, each of the components in the circuit had to be carefully chosen. The following sections provide more details on the components used to implement the design.

3.2.1.1 Quadrature *Hybrids*

Two QH8849 quadrature hybrids from Werlatone Inc. were chosen for this design. The quadrature hybrids are capable of operation in the 80-1000 MHz range, which covers the desired 150-600 MHz range. The typical parameters presented in the data sheet are also given for the frequency range above. Werlatone provided measured typical S-parameters for these components, from which we extracted relevant parameters (Table 3.2).

Table 3.4: Summary of relevant parameters for the Werlatone QH8849

Frequency	150-600 MHz
Power	250 W continuous
Insertion Loss	0.45 dB maximum
Isolation between ports 2 and 3	16 dB minimum
Isolation between ports 1 and 4	19 dB minimum
Phase imbalance	$90^{\circ} \pm 2.12^{\circ}$ maximum
Amplitude imbalance	0.579 dB maximum
VSWR	1.36:1 maximum

For a 15% duty cycle, the power amplifier provides an average power of up to 150 W. These quadrature hybrids can handle up to 250 W of continuous power. We also verified with the manufacturer that operation with 1 kW peak power would be safe. The maximum insertion loss for a single hybrid coupler

is 0.45 dB with a minimum isolation of 16 dB between ports 2 and 3 and 19 dB between ports 1 and 4 across the entire range of interest.

3.2.1.2 PIN Diodes

The MEST2G-150-020-CM26 device from Cobham Metellics (formerly Aeroflex) was chosen as the series switching element, and the MSWSH-100-30 device was chosen as the shunt switching element. The following sections go over the specifications of each diode.

3.2.1.2.1 Series diode MEST2G-150-020-CM26

Table 3.3 lists relevant characteristics of this diode.

Table 3.5: Summary of specifications for the Cobham Metellics MEST2G-150-020-CM26 PIN diode

Frequency	DC – 10 GHz
Power	150 W continuous
V_R	500 V
V_{BR}	500 V
V_F (I_F = 50 mA)	1850 mV
I_{FDC}	250 mA
R_S (I_F = 100 mA; F = 500 MHz)	0.8 Ω
C_j (V_R = -50 V; F = 1 MHz)	0.19 pF
W	80 um
τ (I_F = 10 mA; I_R = 6 mA)	1800 ns
Insertion loss (I_F = 100 mA)	0.4 dB maximum
Isolation (V_R = -10 V)	18 dB minimum
T_J	-40 to +175 °C

This PIN diode is usable up to 10 GHz and can handle up to 150 W of continuous power. Series diode D1 takes the highest power, since it is the first component after the power amplifier and it is essential that it can handle at least 150 W average power and at least 1,000 W peak.

The measured forward bias current vs. bias voltage for this device is shown in Figure 3.2. The current was measured through a multimeter placed in series with power supply. To achieve forward bias current

of 100 mA, approximately 2 V forward bias voltage is required. It has been shown that PIN diodes behave essentially as a short circuit with a forward bias current of just 100 mA [25].

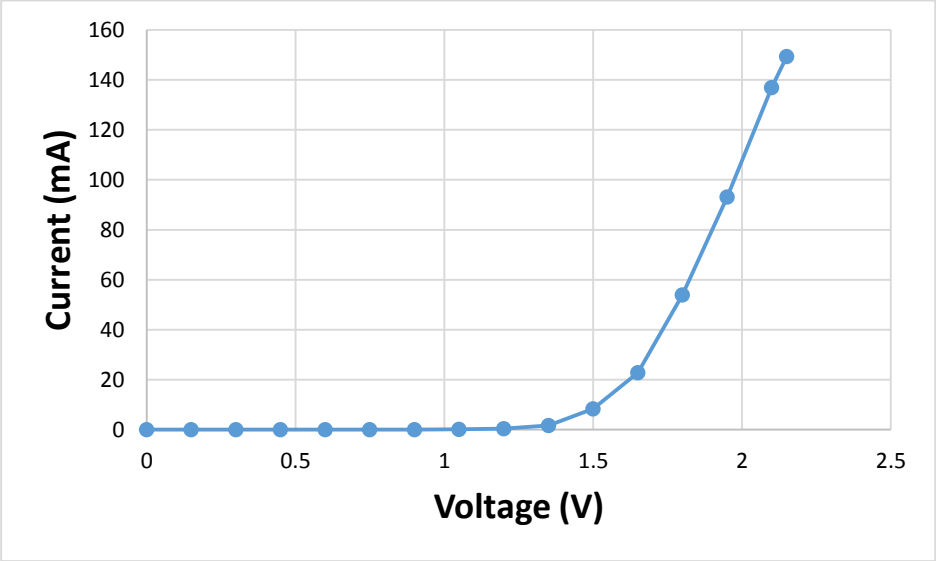

Figure 3.3: Measured I-V curve for the MEST2G-150-020-CM26 series PIN diode

Intrinsic layer width is 80 µm. The series resistance, R_s, at 500 MHz and 100 mA of forward bias current is 0.8 Ohm. Rs is a ratio of the width of the intrinsic layer over electron mobility, hole mobility, carrier lifetime, and forward bias current. As forward bias current increases, forward series resistance tends to decrease. At higher frequencies it is a constant value, which does not change with frequency.

The junction capacitance, C_j, is 0.19 pF at 1 MHz and reverse bias voltage of -50 V. Junction capacitance is a ratio of silicon dielectric constant and junction area, over width of the intrinsic layer. It is not dependent on the reverse bias voltage, and at microwave frequencies, it is not dependent on frequency [25]. As the width of the intrinsic layer increases, junction capacitance decreases, but the forward resistance increases.

In the forward bias condition, ideally the diode would look like short circuit, but realistically there is a small resistance modeled by Rs as shown in Figure 3.3a [18]. During reverse bias, ideally the diode would look like an open circuit. Realistically, there is high impedance caused by the junction capacitance as

shown in Figure 3.3b [18]. As junction capacitance decreases, impedance increases [25]. Parasitic inductance and reverse resistance are usually very small and can be generally neglected if the frequency of operation is low enough.

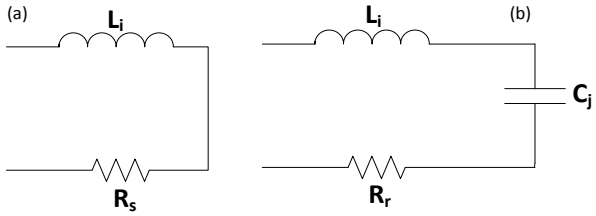

Figure 3.4: PIN diode equivalent circuits: (a) forward bias; (b) reverse bias [18]

The carrier lifetime for this device is 1800 ns as stated by the manufacturer, measured from 10 mA of forward bias current to 6 mA of reverse bias current. Switching time is dependent on carrier lifetime and forward and reverse bias currents. Carrier lifetime is the recombination rate of the minority carrier, and it affects the bias current required to keep a charge density in the intrinsic region [25]. Shorter carrier lifetime requires higher bias current to maintain a charge density, but generally leads to a faster switching time. A reverse bias current can help reduce the effects of a long carrier lifetime by increasing the dissipation rate of the charge in the intrinsic region. A practical rule of thumb in White [25] states that the switching speed of the diode is limited to about 1/10 of the carrier lifetime. In this case, the diode can ideally switch states in 180 ns, which is adequate for our application.

The maximum insertion loss is 0.4 dB at 100 mA of forward bias current, and minimum isolation is 18 dB at -10 V of reverse bias voltage.

The junction temperature has a range from -40 °C to 175 °C. The operating temperature of the diodes needs to be kept well below the maximum Tj for high reliability of the circuit.

3.2.1.2.2 Shunt PIN diode MSWSH-100-30

The PIN diode MSWSH-100-30 from Cobham Metellics was chosen as shunt switching elements: D2, D3, and D4. Table 3.4 lists a summary of relevant characteristics of this diode.

Table 3.6: Summary of specifications for the Cobham Metellics MSWSH-100-30 PIN diode

Frequency	0.1 – 6 GHz
Power	100 W continuous
V_F (I_F = 100 mA)	850 mV
V_{BR}	700 V
R_S (I_F = 100 mA; F = 500 MHz)	0.6 Ω maximum
C_j (V_R = -50 V; F = 1 MHz)	0.4 pF
W	80 um
τ (I_F = 10 mA; I_R = 6 mA)	3400 ns
Insertion loss (V_R = -10 V)	0.25 dB maximum
Isolation (I_F = 100 mA)	28 dB minimum
T_J	-40 to +175 °C

The diode has a frequency range from 0.1 GHz to 6 GHz and can handle up to 100 W of continuous power. Since the amplifier power is divided in half by the quadrature hybrid at its output, shunt diodes D2 and D3 need to only handle up 75 W of average power. We also checked with the manufacturer and verified that this element could safely handle up to 1000-W peak power.

The measured forward bias current as a function of bias voltage for this device is shown in Figure 3.4. Approximately 1.05 V is required to achieve 100 mA of forward bias current.

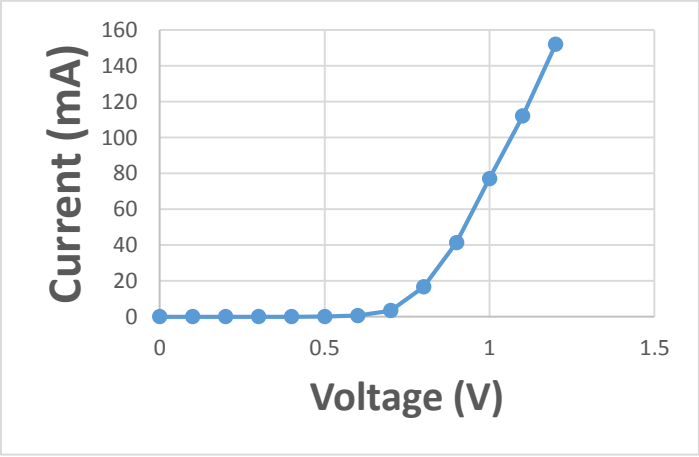

Figure 3.5: Measured I-V curve for THE MSWSH-100-30 PIN diode

3.2.1.2.3 Series and Shunt diode Models

Table 3.5 lists the parameter values of the series and shunt diode SPICE models used in the circuit simulations conducted in the context of this work. These values were provided by the manufacturer Cobham Metellics (formerly Aeroflex).

Table 3.7: Diode ADS model

	MEST2G-150-020	**MSWSH-100-30**
I_S (mA)	2e-8	1.2e-6
I_{knee} (mA)	100	60
R_{epi} (Ω)	1000	1000
C_j (pF)	0.19	0.47
R_{lim} (Ω)	0.8	0.25
t (ns)	2200	2800
W (um)	115	80
R_S (Ω)	1.8	0.4

3.2.1.3 Limiter: LM200802-M-A-300

The limiter, LM200802-m-A-300, was added to the receiver chain. The limiter had a frequency range of 20 to 8000 MHz and could handle 42 dBm of continuous power and 50 dBm of peak power with a pulse width of 1 μs and duty cycle of .001. Insertion loss was less than 0.4 dB below 1 GHz.

3.2.1.4 High Pass Filter

A high pass filter, shown in Figure 3.4, was designed to suppress switching transients at the receiver port. The design goals for the filter were a 3 dB point of 61 MHz and an insertion loss of less than 0.2 dB at 150 MHz. The out-of-band attenuation had to be at least 20 dB at 40 MHz. The circuit was designed using Keysight Genesys and measured using a vector network analyzer (VNA). The simulated and the measured responses of the filter are shown in Figure 3.5. The measured response has a 3 dB point at 61.5 MHz and an insertion loss of less than 0.172 dB above 150 MHz. Attenuation at 40 MHz is 25 dB.

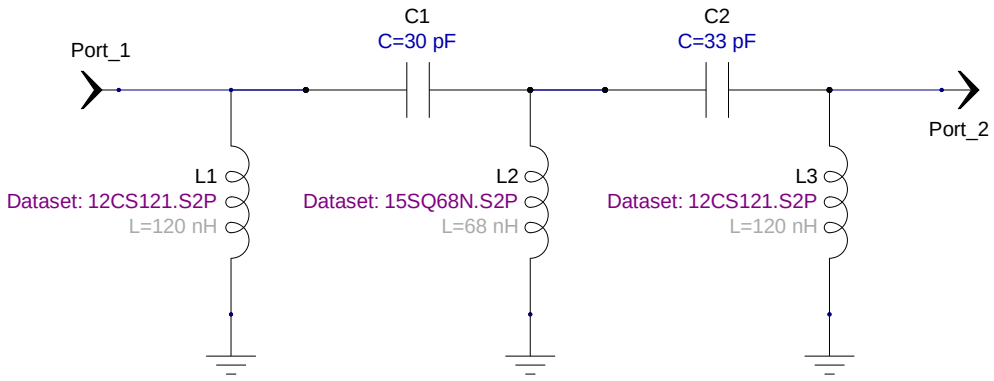

Figure 3.4: Schematic circuit of the High Pass Filter used for low-frequency transient suppression

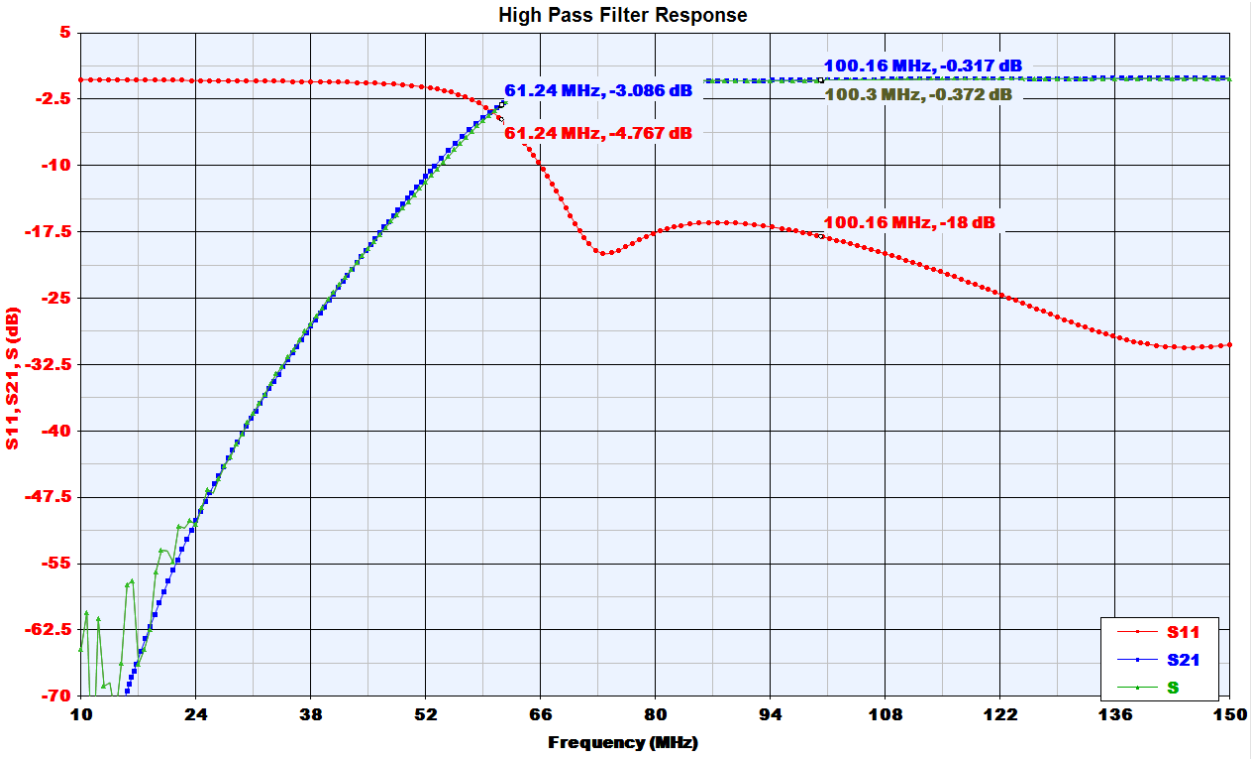

Figure 3.6: Simulated (Blue) vs measured (Green) high pass filter response

High Q value inductors were chosen from the Air Core Springs line by Coilcraft. Q value is a ratio of energy stored over energy lost per cycle. For an inductor, this a ratio of inductive reactance over inductive series resistance. Series resistance is dependent on skin effect of the wire, DC resistance of the

wire, and the core losses [22]. Higher Q value indicates a lower series resistance and hence lower losses [22].

3.2.1.5 Isolation Switch

ADG901, a single-pole, single-throw absorptive switch, was used to provide extra isolation between the receiver and amplifier ports. Insertion loss was 0.45 dB at 150 MHz and 0.7 dB at 600 MHz. Isolation below 600 MHz was at least 40 dB. This switch was chosen due to its low video leakage [13].

3.2.1.6 Bias Tee

Each diode is actively biased using a tee circuit composed of DC blocking capacitors and an RF choke. This circuit had to be optimized to obtain a resonant-free response over the wide band of interest.

300 pF capacitors from American Technical Ceramics (800B series) were used for DC blocking. These capacitors can handle high RF power and have extremely low equivalent series resistance, which is important for high power applications. 300 pF capacitor has an impedance of 3.53 Ohms at 150 MHz and 0.88 Ohms at 600 MHz. 100 pF bypass capacitors were also used to provide a low-resistance path to ground for the AC component (noise) of the bias DC signal from the PIN diode drivers.

Two high Q value series Air Core Springs Coilcraft inductors were used as RF chokes. A 491 nH in series with a 15 nH inductor were used to provide around an impedance of around 476 Ohms at 150 MHz and around 1907 Ohms at 600 MHz. Two inductors were used in series in order to provide high impedance for the entire bandwidth [8].

3.2.2 Computer Simulations

Keysight Advanced Designs Systems (ADS) was used to perform low level, high level, and electromagnetic (EM) simulation of the circuits presented in this chapter. The printed circuit board (PCB) layout was done in Altium Designer.

3.2.2.1 Low level simulation

The design of the T/R switch was first simulated under semi-ideal conditions using a linear s-parameter simulation, only taking into account the response of the Werlatone QH8849 hybrids. Figure 3.6 shows the simulation setup for the circuit in transmit mode, in which the forward-biased PIN diodes are modeled as a perfect short circuit.

A similar simulation was performed for the receive mode. The diodes D2 and D3 are modeled as a perfect open circuit, as shown in Figure 3.7. The simulated insertion gain (power amplifier to antenna) in transmit mode, as well as in receive mode (antenna to receiver) are presented in Figure 3.8. Isolation during receive mode is shown in Figure 3.9.

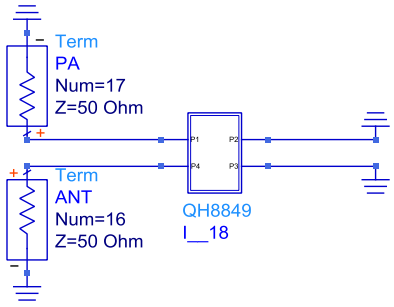

Figure 3.7: Simulation setup representing semi-ideal behavior in transmit state

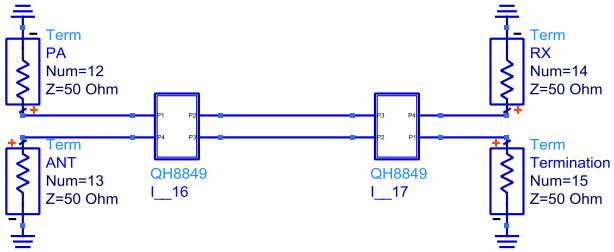

Figure 3.8: Simulation setup representing semi-ideal behavior of the circuit in receive state

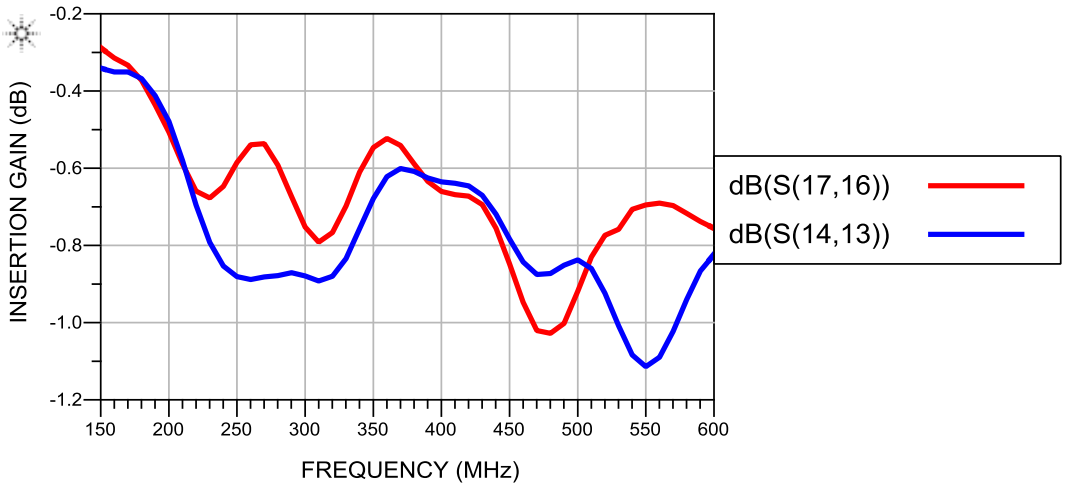

Figure 3.9: Simulated response for the insertion gain during (a) Transmit between PA and ANT ports (S(17,16)); (b) Receive between ANT and RX ports (S(13,14))

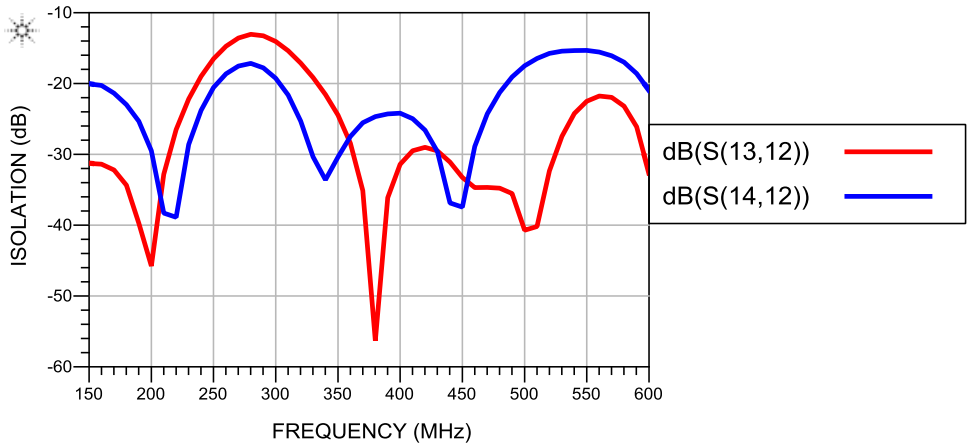

Figure 3.10: Simulated isolation in receive mode between: (a) PA and ANT ports (S(13,12)); (b) PA and RX ports (S(14,12))

During transmit, the maximum simulated insertion loss caused by the ideal circuit is 1.028 dB at 480 MHz. In receive mode, the maximum simulated insertion loss is 1.114 dB at 550 MHz, and isolation is greater than 13 dB between PA and ANT and 15 dB between PA and RX. These simulations give the upper bound for the losses across this frequency range. To model the circuit more accurately, higher level simulations were performed. These include the effects of the rest of the components used in the design.

3.2.2.2 High Level Simulations

After verifying the circuit concept using the simulation outlined in the previous subsection, the effects of the remaining components were integrated into the simulated design, as shown in Figure 3.10. Scattering parameters for the hybrids, PIN diodes, and inductors were provided by the manufacturer. This particular simulation does not include the effects of interconnects yet.

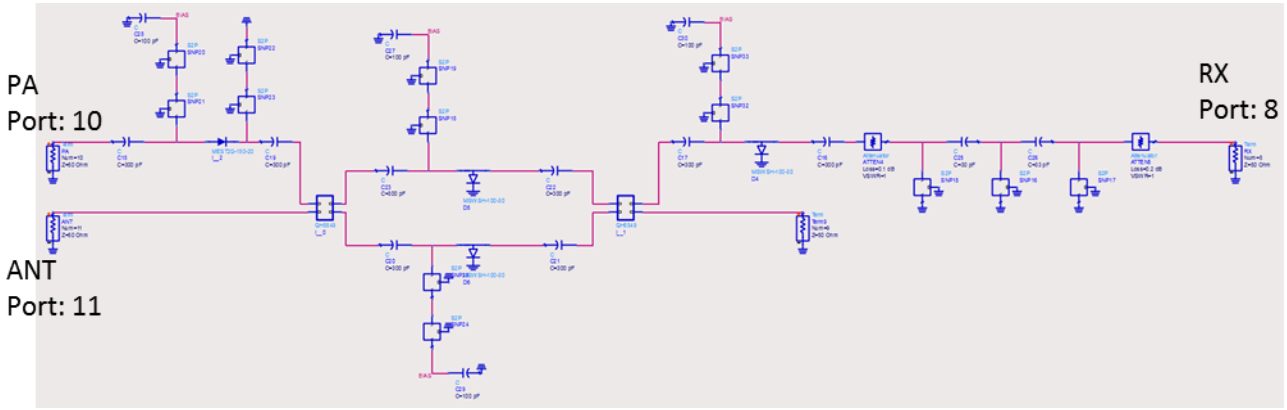

Figure 3.11: ADS simulation setup including first order effects in all the components.

A linear s-parameter simulation was also performed using this setup. During transmit mode, there was low loss between the power amplifier (PA) and antenna (ANT) ports, and high isolation between power amplifier and receive (RX) ports and antenna and receive ports. This is shown in Figure 3.11 and 3.12.

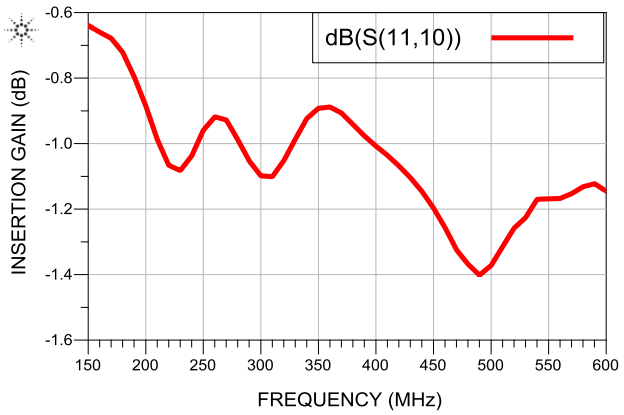

Figure 3.12: Simulated insertion gain between PA and ANT ports (S(11,10) during transmit

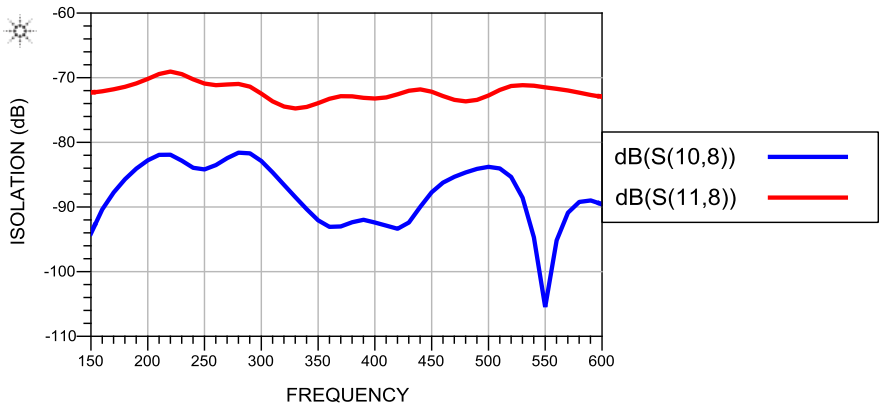

Figure 3.13: Simulated coupling between (a) PA and RX ports (S(10,8)); (b) ANT and RX ports (S(11,8)) during transmit

The maximum simulated insertion loss predicted by this simulation is 1.402 dB at 490 MHz. The minimum simulated isolation between PA and RX port is 109 dB at 500 MHz and between ANT and RX is 96 dB at 540 MHz.

During receive mode, there is low loss between ANT and RX ports, as shown in Figure 3.13, and high isolation between PA and ANT and PA and RX ports, as shown in Figure 3.14.

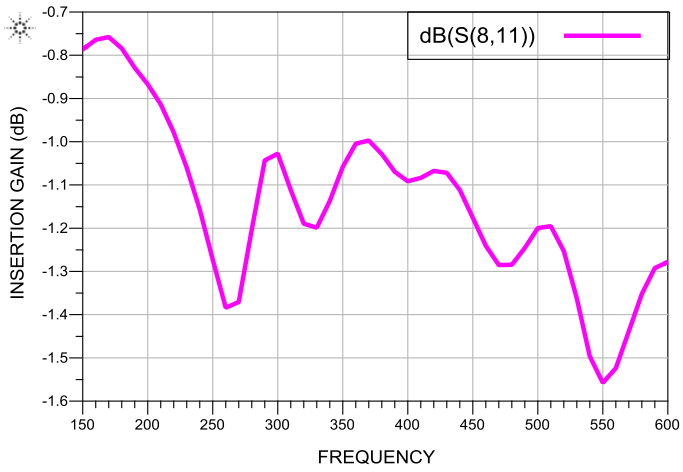

Figure 3.14: Simulated insertion gain between ANT and RX ports (S(8,11)) during receive

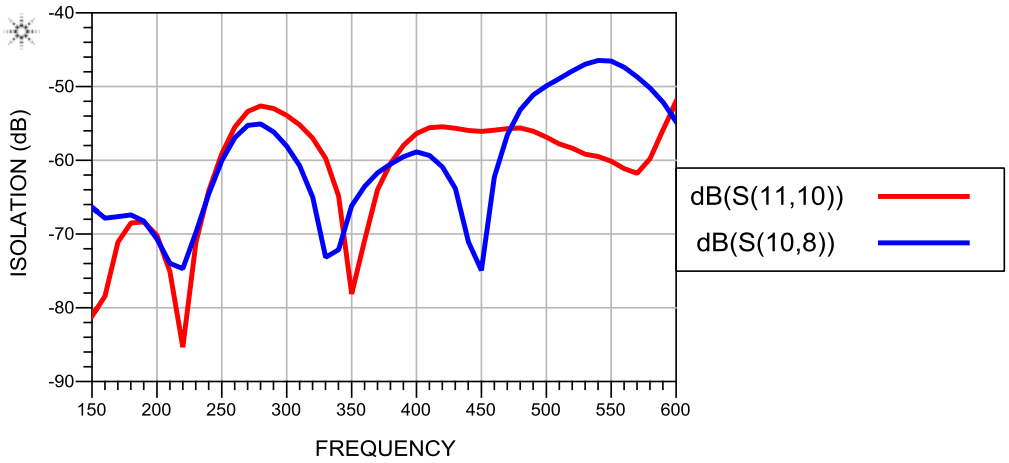

Figure 3.15: Simulated coupling between (a) PA and ANT ports (S(11,10); (b) PA and RX ports (S(10,8)) during receive

The maximum simulated insertion loss predicted by this simulation is 1.543 dB for 550 MHz. Minimum simulated isolation between PA and ANT ports is around 51 dB at 600 MHz and 46 dB at 540 MHz between PA and RX.

3.2.2.3 EM/circuit co- simulations

To provide a more accurate simulation of the circuit, all PCB effects were modeled using a EM simulation in Momentum. The EM simulation results are then included in an EM/circuit co-simulation that includes both PCB layout effects and linear circuit behavior.

3.2.2.3.1 Board Design

The prototype printed circuit board (PCB) was designed in Altium Designer on a 1 oz. FR4 substrate. The FR4 material has a typical dielectric constant of 4.7, relative permittivity of 4.8, substrate thickness of 64 mils, and trace thickness (copper) of 1.4 mils. To keep a 50 Ohm impedance and good isolation between traces, Grounded Coplanar Waveguide (CPWG) was used for the RF transmission lines. The line width and gap were calculated to be 119 mils and 115 mils, respectively. Instead of microstrip, CPWG was employed to increase isolation between each section [20]. The board layout design is shown in Figure

3.15. All components were surface mounted, with the exception of the PIN diodes and quadrature hybrid couplers, which were drop-in components.

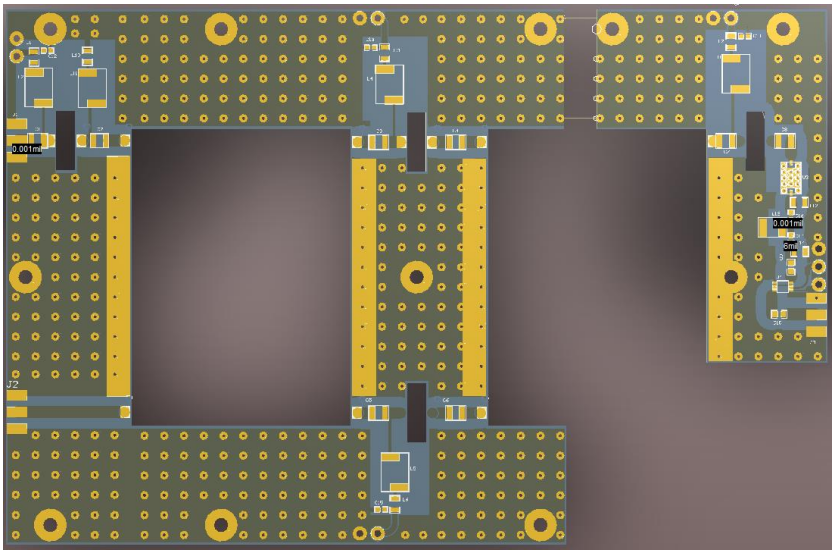

Figure 3.16: T/R switch PCB layout in Altium Designer

3.2.2.3.2 Circuit/EM Co-Simulation

The board layout was imported into ADS to perform electromagnetic simulations. Figure 3.16 shows the simulation setup used in ADS.

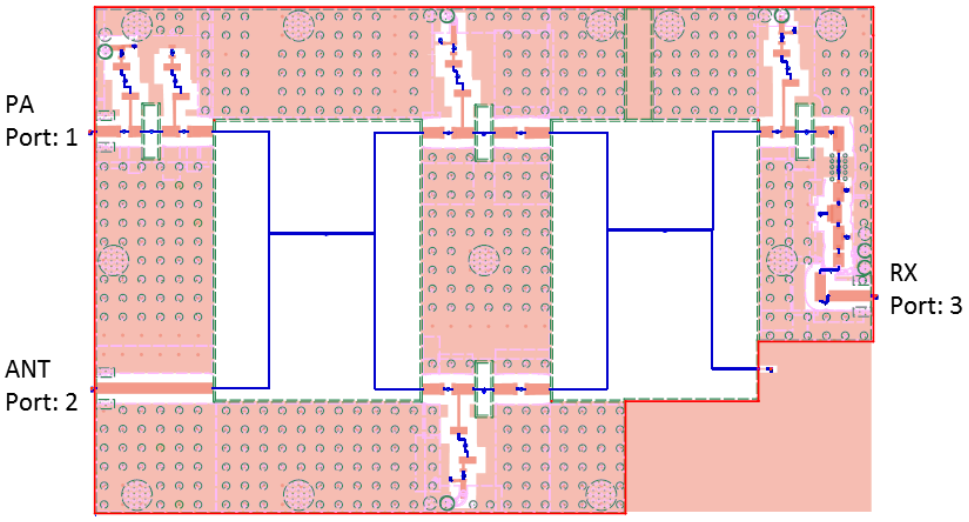

Figure 3.17: Circuit/EM co-simulation setup in ADS

During transmit mode, there is low loss between the PA and ANT ports (as shown in Figure 3.17) and high isolation between PA and RX ports and ANT and RX ports (as shown in Figure 3.18).

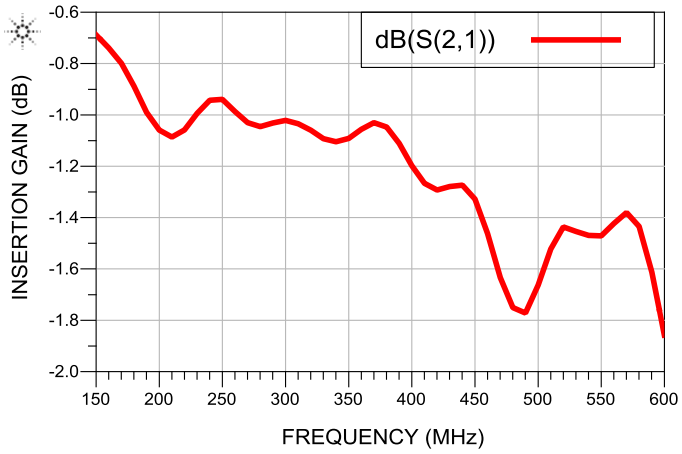

Figure 3.18: Simulated insertion gain between PA and ANT ports during transmit

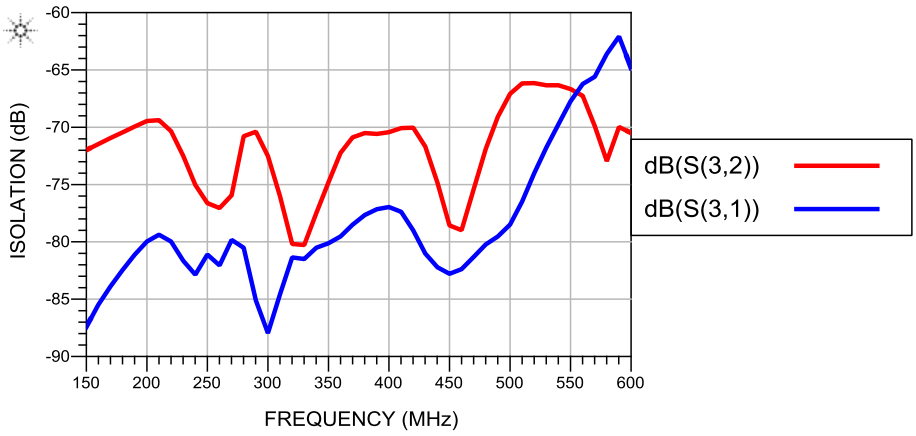

Figure 3.19: Simulated coupling between (a) ANT and RX (S(3,2)); (b) PA and RX (S(3,1)) during transmit

The maximum simulated insertion loss is 1.859 dB at 490 MHz. Minimum simulated isolation between PA and RX ports is 72 dB at 600 MHz and 72 dB at 600 MHz between ANT and RX ports.

During receive mode, there is low loss between ANT and RX ports (as shown in Figure 3.19), and high loss between PA and ANT and PA and RX ports (as shown in Figure 3.20).

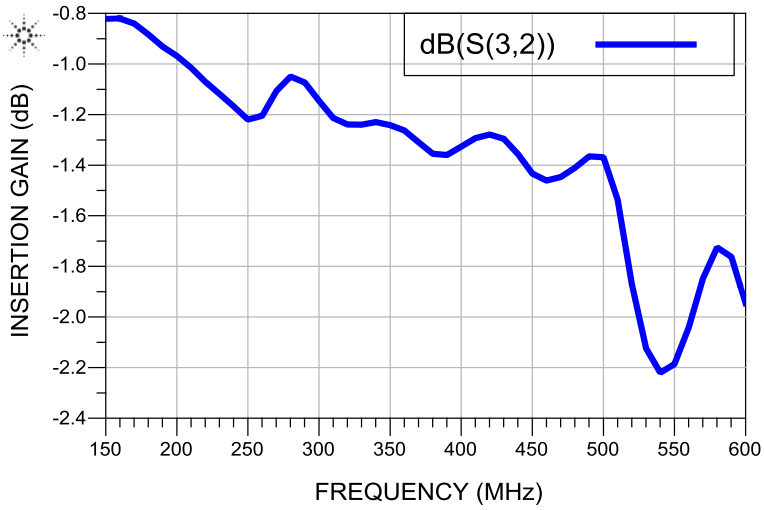

Figure 3.20: Simulated insertion gain between ANT and RX ports during receive

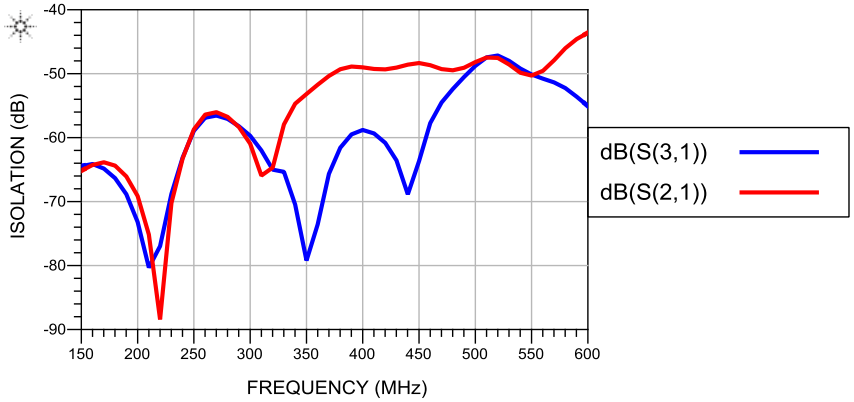

Figure 3.21: Simulated coupling between (a) PA and ANT (S(2,1); (b) PA and RX (S(3,1)) during receive

The maximum simulated insertion loss is 2.22 dB at 540 MHz. The minimum simulated isolation between PA and RX port is 47 dB at 600 MHz and 43 dB at 520 MHz between PA and ANT ports.

Figure 3.21 shows the insertion gain difference between low level, high level, and EM simulation during transmit. Figure 3.22 shows it during receive. The losses added by simulated transmission lines increases the insertion loss between high level simulation and EM/circuit co-simulation by 0.713 dB at 600 MHz during transmit and 0.628 dB at 550 MHz during receive. These are the maximum differences in insertion loss.

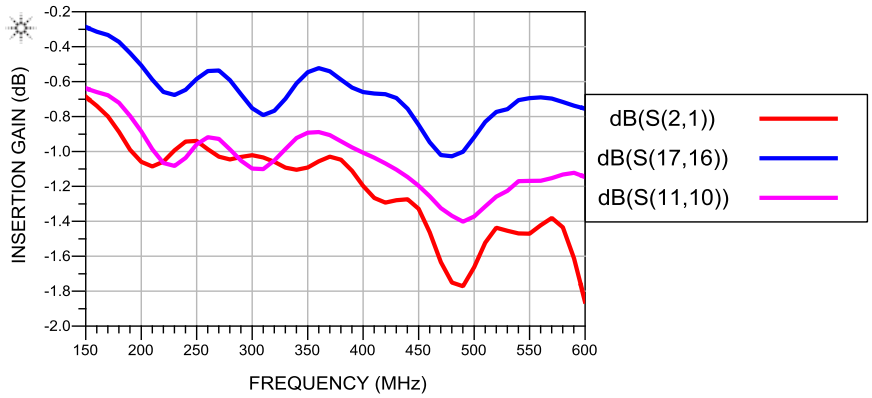

Figure 3.22: Simulated insertion gain between PA and ANT during transmit (a) Ideal (S(17,16)); (b) High level (S(11,10)); (c) EM/Circuit Co-simulation (S(2,1))

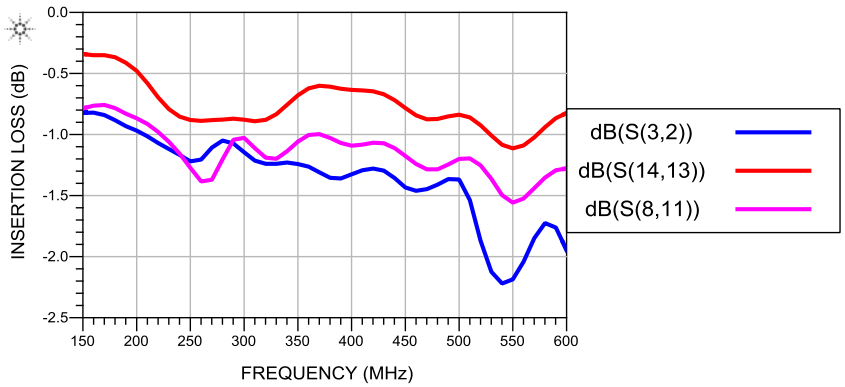

Figure 3.23: Simulated insertion gain between ANT and RX during receive (a) Ideal (S(14,13)); (b) High level (S(8,11)); (c) EM/Circuit Co-simulation (S(3,2))

3.3 Small signal measurements

A 4-port Vector Network Analyzer was used to measure the scattering parameters of the transmit/receive switch. The PIN diodes were connected to a power supply and biased with 100 mA of a constant forward bias current during transmit. For convenience, the receive state was tested using 0 V reverse bias voltage. Reverse bias voltages as low as -15 Volts were checked without a noticeable difference in response.

Figure 3.23 show the insertion gain of the device along with low level, high level, and EM simulation results during transmit and Figure 3.25 shows it during receive. Figures 3.24 and 3.26 show the isolation during the transmit and receive phase of the prototype device. Due to limitations in signal-to-noise ratio

in the measurement, isolation values below 80 dB could not be accurately measured without changing the VNA settings.

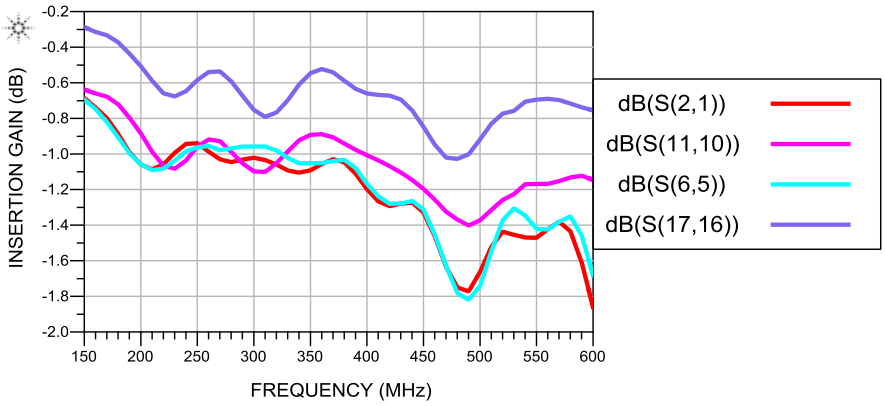

Figure 3.24: Simulated vs measured insertion gain between PA and ANT during transmit (a) Ideal (S(17,16)); (b) High level (S(11,10)); (c) EM/Circuit Co-simulation (S(2,1)); (d) measured (S(6,5))

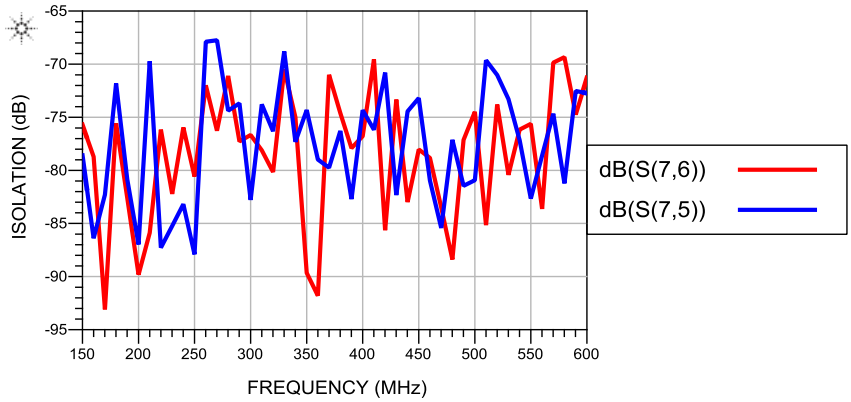

Figure 3.25: Measured coupling during transmit between (a) PA and RX (S(7,6)); (b) ANT and RX (S(7,5))

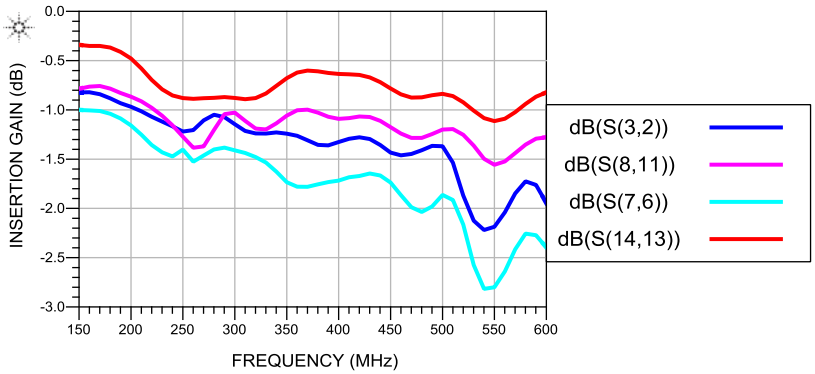

Figure 3.26: Simulated vs measured insertion gain between ANT and RX during receive (a) Ideal (S(14,13)); (b) High level (S(8,11)); (c) EM/Circuit Co-simulation (S(3,2)); (d) Actual (S(7,6))

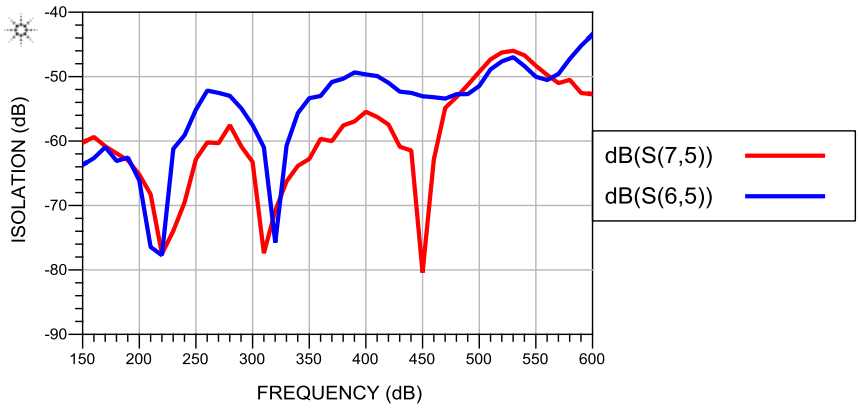

Figure 3.27: Measured coupling during receive between: (a) PA and ANT (S(7,5)); (b) PA and RX (S(6,5))

The measured response of the prototype matched up well with the EM/circuit co-simulation results. The maximum variance in insertion loss between EM/circuit simulation and prototype response was 0.15 dB during transmit and 0.4 dB during receive.

3.4 PIN diode Driver Circuit

A driver circuit that can quickly toggle the biasing state of the diodes is needed to switch the PIN diodes and the receiver switch from transmit to receive in less than 2.3 µs. The following sections describe the driver circuit employed in the design in more detail.

3.4.1 Description of the driver

The input to the driver circuit is a logic signal provided by the digital system that swings between 0 and 5 V (standard TTL logic). Transistors are used to condition the signal since the TTL signal cannot provide enough current for forward or reverse bias stages. Transistors need to be able to handle the voltages and currents of the PIN diode as well as be fast in order to maintain a fast switching time. Having a low transistor parasitic capacitance leads to a faster switching time.

The driver has to be able to provide at least 100 mA of forward biasing current and up to -40 V of reverse bias voltage. In other words, during forward bias, the driver has to fill intrinsic layer with charge and the current has to high enough so that the forward series resistance is as low as possible. During

reverse bias, the charge has to be depleted from the intrinsic layer, and the junction capacitance has to be low enough to provide high enough impedance. The transition has to take place fast.

The control signal from the digital system is set to high during transmit and low during receive. The timing diagram shown in Figure 1.1. The driver for the switch has to invert the TTL signal and ensure that the input voltage to control pin of ADG901 does not exceed 2.75 V, which is the maximum allowed voltage. The driver has to also provide the supply voltage V_{DD} of 2.5 V.

The PIN diode driver design was based upon the circuit developed by Brorsson [2] with some adaptations for our application. The driver is able to switch two PIN diodes with a carrier lifetime of 2000 ns in 237 ns. It provides 100 mA of forward bias current and up to -40 V of reverse bias voltage. The design is detailed below.

3.4.1.1 PIN Diode Driver Functionality

Figure 3.27 shows the schematic of the adapted Brorsson design [2].

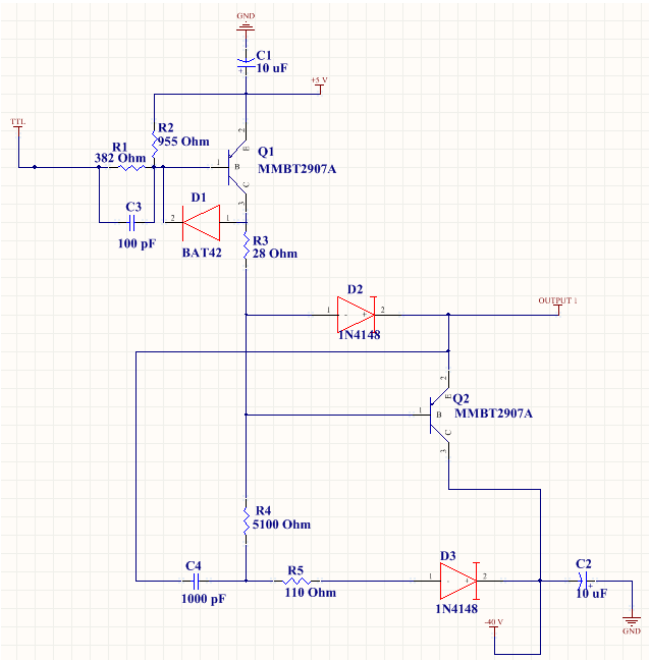

Figure 3.28: Schematic circuit for the PIN diode driver

When the TTL signal is low, transistor Q1 is in saturation mode and current flows through resistor R3, and diode D2 to the output. The diode D2 also ensures that the transistor Q2 would be in cutoff, since the voltage drop across the diode results in the emitter base voltage of Q2 to be below 0. When the TTL signal is high, only Q1 is active, and when it is low, only Q2 is active. This prevents the load from seeing positive and negative voltages at the same time. Resistor R3 ensures that maximum current draw would be 100 mA during forward bias. Capacitor C3 is used to speed up switching of Q1. C3 helps discharge the base pin of Q1 when it switches from saturation to cutoff. It also provide charge to speed up Q1 during its switch from cutoff to saturation. The Schottky diode D1 keeps the voltage drop between base and collector of Q1 to be around 0.4 V.

When the TTL signal is high, transistor Q1 is in cutoff because of R1 and R2. When TTL is high, it is at 5 V, and the voltage drop across R1 in parallel with R2 would not be enough to ensure emitter to base voltage be higher than 0 V. Since Q1 is in cutoff, current does not flow from R3 and D2 is therefore reversed biased. Since the voltage drop from D2 is no longer keeping Q2 in cutoff, it enters saturation mode. Hence, negative voltage is applied to the load and the PIN diode is reverse biased. R4 and R5 are used to provide correct biasing for Q2 so it stays in saturation. R4 voltage is maintained when Q2 is connected to the load by C4 thus ensuring Q2 does not leave saturation. The diode D3, prevents R5 from draining C4.

3.4.1.2 Switch Driver Functionality

Figure 3.28 shows the schematic of the switch driver. BSS123 is an N-channel MOSFET and AD525BRT is a voltage reference chip that converts 5 V into +2.5 V.

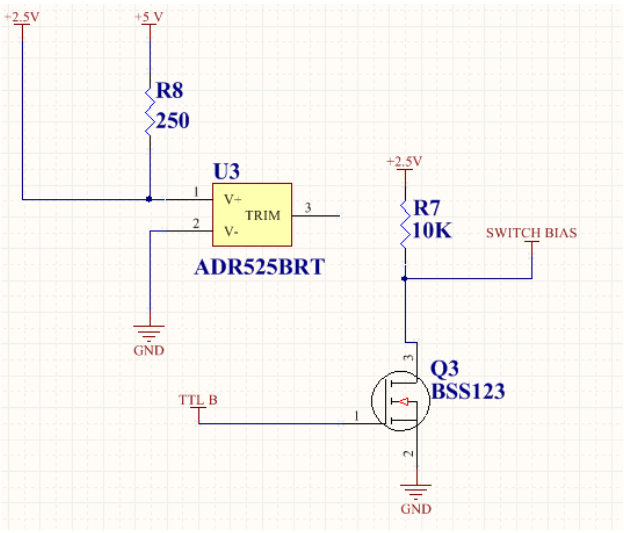

Figure 3.29: Schematic circuit of the isolation switch driver

When the TTL signal is low, gate to source voltage is 0 and the MOSFET is cutoff. The drain current would be 0 as well. Hence, the bias voltage would be 2.5 V, which drives the switch into receive mode.

When the TTL signal is high, MOSFET switches into triode mode. Drain current flows from voltage source to source port to ground. Value of R7 ensures that voltage across the resistor would be 2.5 V, which results in the output voltage to be 0 V. Figure 3.29 shows the TTL signal along the switch bias voltage.

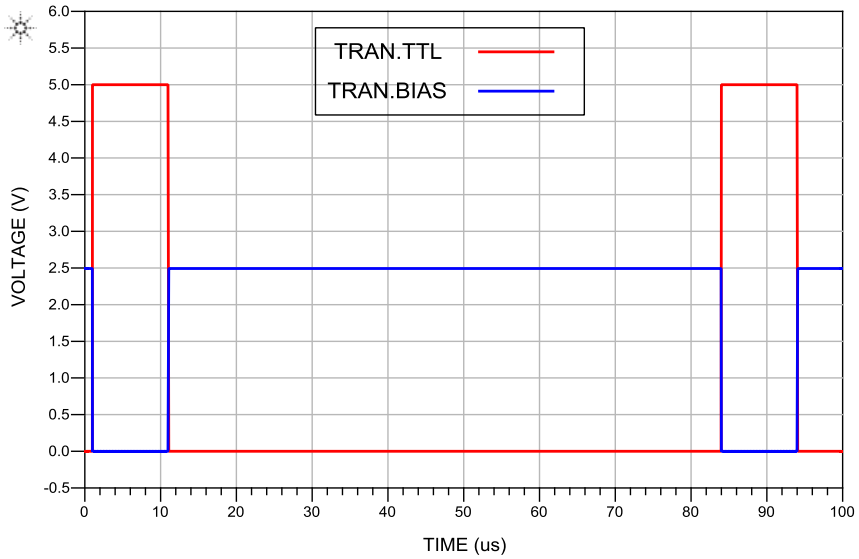

Figure 3.30: Simulated results for the receiver switch driver: TTL input (Red) vs. Switch signal (Blue)

3.4.2 Computer Simulations

The transient simulation feature of ADS was used to simulate the performance of the driver circuit shown in Figure 3.27. Input TTL signal was provided by a pulsed source. It had a frequency of 12 kHz, switched between 0 and 5 V, rise and fall time of 1 ns, pulse width of 10 µs, and period of 83 µs. This signal represents the signal provided by the radar's digital system. The simulation uses spice models for transistors and diodes, but uses ideal resistors and capacitors. This assumption is adequate because we use resistors and transistors with high-Q and because the switching frequency is well below the self-resonant frequency of the lumped elements used in this circuit. We chose a reverse voltage of -12V because it offered the best trade-off between a relatively low voltage and fast switching. Voltages larger than -12 VDC resulted in significant degradation in switching time.

Figure 3.30 shows the simulated driver response with no load for VR=-12 V.

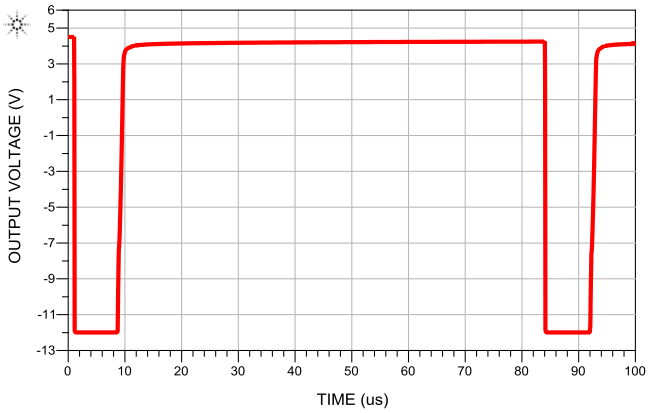

Figure 3.31: Simulated results obtained for the PIN diode circuit driven by a TTL signal at 12 kHz

Without load, the output voltage fluctuates between 4.2 V and -11.9 V. The switch on time ranges from -12 V to 3.6 V is 420 ns and the turn off time ranges from 4.242 V to -12 V is 140 ns. Switching time was measured from fully on to fully off and vice versa.

Attaching a PIN diode as a load with the parameters given for the MEST2G-150-20 decreased the switch on time to 370 ns and switch off time to 110 ns, as shown in Figure 3.31. Including the bias tee network increased switch on time to 420 ns and switch off time to 380 ns as shown in Figure 3.32.

Changing the PIN diode model to MSWSH-100-30 resulted in the switch on time to be 480 ns and switch off time to be 140 ns, as shown in Figure 3.33. Including the bias tee network changed the switch on time to 540 ns and switch off time to 410 ns, as shown in Figure 3.34.

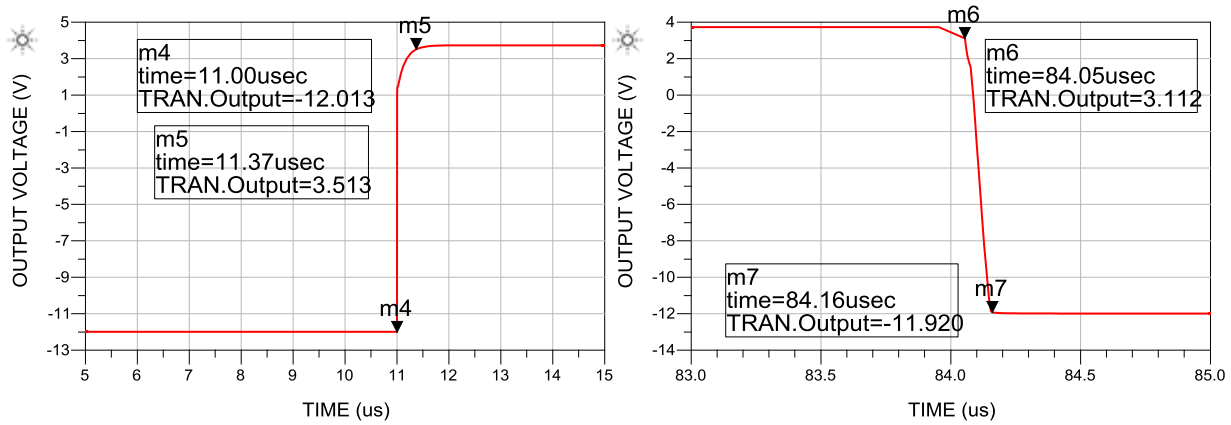

Figure 3.32: Simulated switching time for series diode element

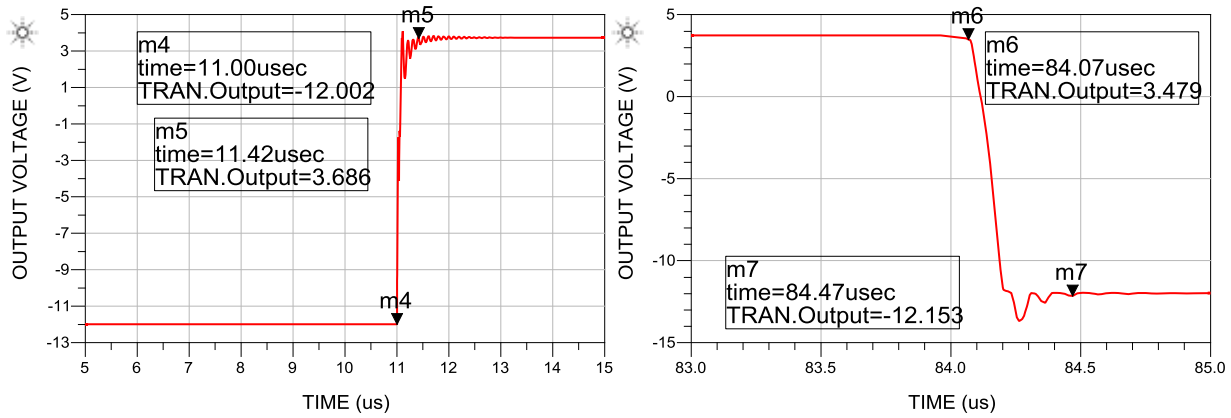

Figure 3.33: Simulated switching time for series diode element with bias tee

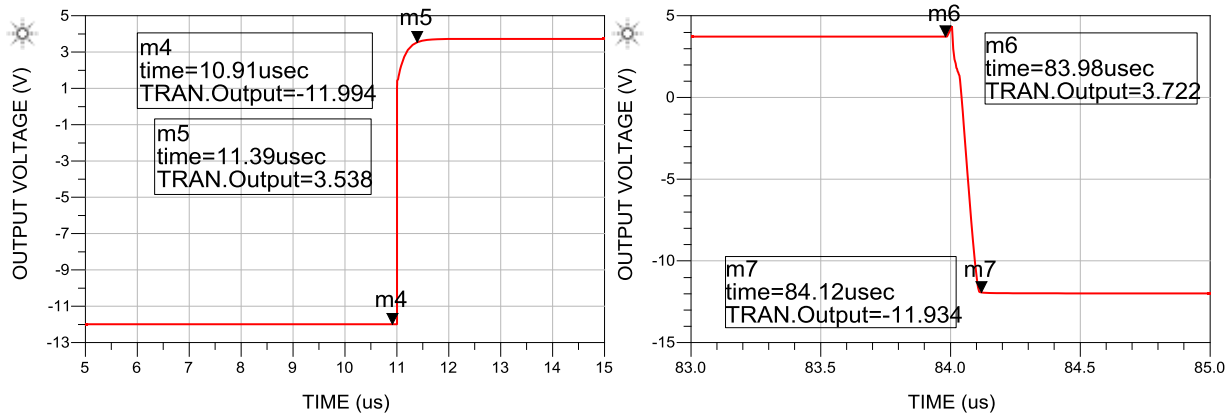

Figure 3.34: Simulated switching time for shunt diode element

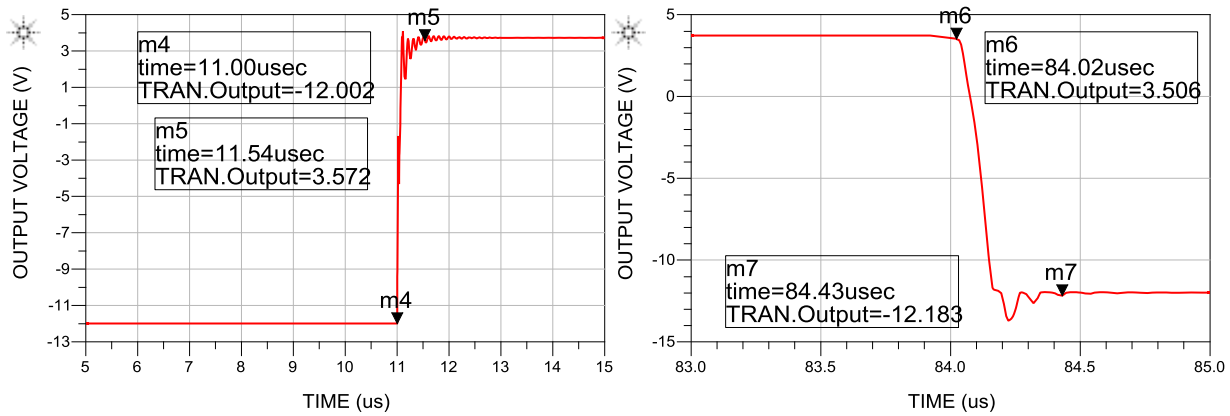

Figure 35: Simulated switching time for shunt diode element with bias tee

3.4.3 Driver Components

The adapted design is shown in Figure 3.35.

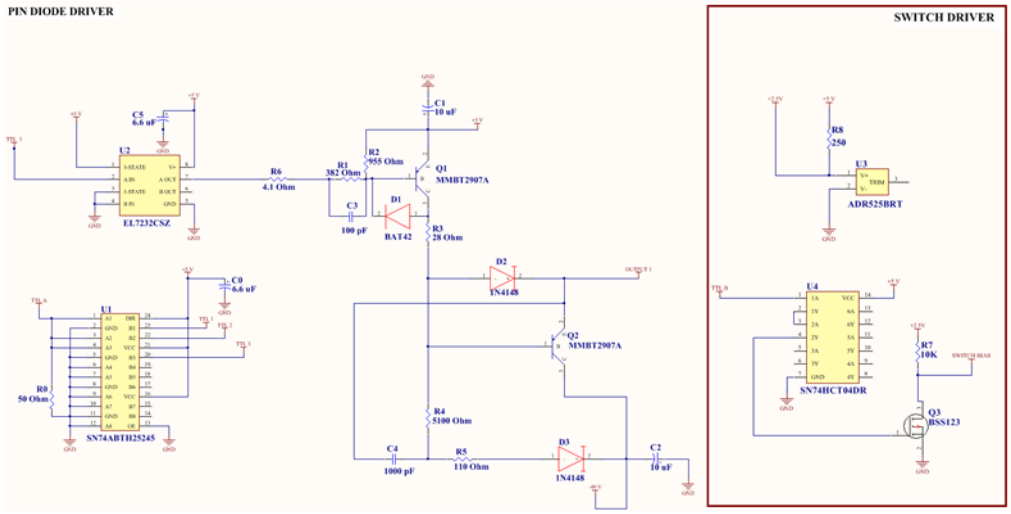

Figure 3.36: Schematic circuit of the design

Since the TTL signal had to be split between three drivers, a non-inverting transceiver chip SN74ABTH25245DWR was used as a buffer for the signal. Table 3.6 lists the important parameters of this transceiver chip. The chip has low delay, relatively high output current, and low high-level input voltage. A low high-level input voltage is required because the TTL signal swings from 0 to 3.3 V. Low delay benefits the overall switching speed of the driver.

Table 3.8: Summary of specifications for the SN74ABTH25245DWR line driver

Parameter	Characteristics	Unit
V_{CC}	4.5 – 5.5 (used at 5)	V
V_{IH}	2	V
V_{IL}	0.8	V
I_{OH}	-80	mA
I_{OL}	188	mA
t_{PHL}	4.3	ns

In order to drive Q1 into cutoff, the TTL signal needs to be 5 V, since the emitter pin of Q1 has a 5 V source. The output of SN74ABTH25245DWR provides a signal that swings between 0 and 3.3 V. Another issue is that the driver circuit switches the logic. When TTL is high, the diodes are reversed biased and when it is low, it forward biased. The timing diagram in Figure **1** shows that the T/R switch needs to transmit when TTL is high and receive when it is low. To combat these issues, an inverting buffer chip, EL7232, was used before the driver circuit as shown in Figure 3.35. Table 3.7 lists the important parameters of this chip.

Table 3.9: EL7232 specifications

Parameter	Characteristics	Unit
V_{CC}	4.5-16 (used at 5)	V
V_{IH}	2.4	V
V_{IL}	0.8	V
I_{PK}	2	A
t_{PHL}	25	ns

This design utilizes two MMBT2907A PNP transistors. The transistors had a collector to emitter breakdown voltage of 60 V, handled high collector currents up to 800 mA, and had a delay of 10 ns, making it ideal for the selected PIN diodes.

Diode 1N4148 by Fairchild Semiconductors was used for D2 and D3. The diode can handle 150 mA of continuous forward current and 300 mA of peak forward current. Its breakdown voltage is 100 V at

reverse bias current of 100 μA. Forward bias voltage at 100 mA is 1 V. Switching time is less than 4 ns with forward bias current of 10 mA and reverse bias current of 60 mA applied to a 100 Ohm load.

Schottky diode BAT42XV2 by Fairchild Semiconductors was used for D1. Its breakdown voltage was 30 V at reverse bias current of 100 μA. Forward bias voltage at 50 mA was 1 V. Switching time was less than 5 ns with forward bias and reverse bias current of 10 mA applied to a 100 Ohm load.

Inverter chip SN74HCT04 was used as a buffer. Propagation delay through the chip was 13 ns. BSS123 was capable of providing 0.17 A of continuous drain current which was enough for the switch. Keeping a low switching time for each of the components was key to reducing the switching time of the PIN diodes.

3.4.4 Board design

Four driver circuits were required for each of the diodes: one series, and three shunt. The final driver design is shown in Figure 3.36. The board with drivers 1, 2, and 3 was used in the high power section while the board with driver 4 and switch driver was used in the receiver section. The section that is not highlighted was the circuitry for drivers that were not used due to low switching time. The board was designed on a 1 oz. FR4 board.

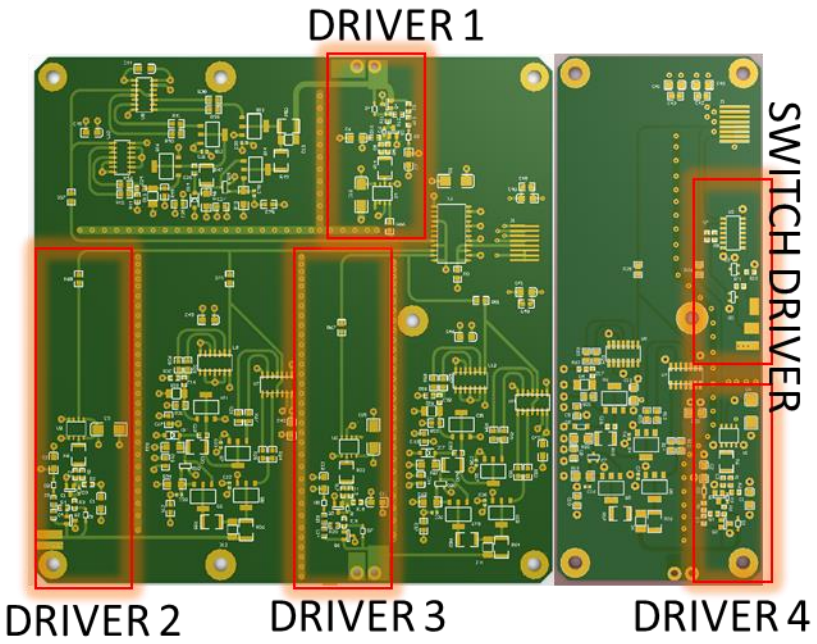

Figure 3.37: Driver PCB layout

3.4.5 PIN Diode Switching Time Measurements

The switching time of the driver was verified using a digitizing oscilloscope. The input TTL signal to the driver was provided by a pulsed source. Its frequency was set to 12 kHz. It switched between 0 and 3.3 V, and had a rise and fall time of 66 ns, pulse width of 10 µs, and period of 83 µs. The output of the driver was connected to the PIN diode via the Bias point shown in Figure 3.1.

The PIN diode driver was tested with no load first as shown in Figure 3.37. Turn on time from -12 V to 2 V was 295 ns and turn off time from 2.6 V to -12 V was 140 ns.

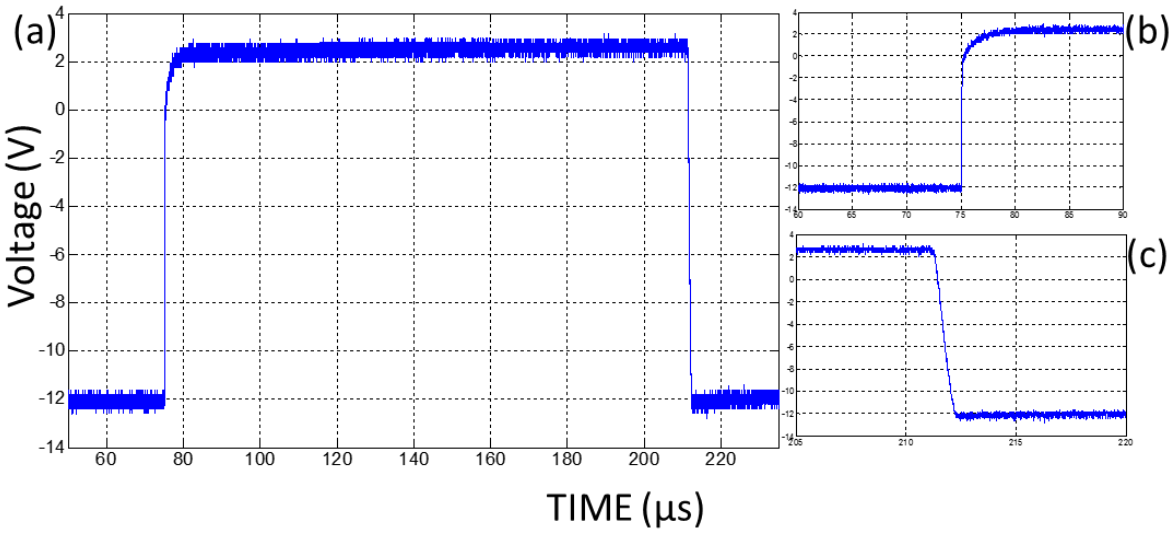

Figure 3.38: Measured switching time of PIN diode driver with no load: (a) Rise and fall time; (b) rise time; (c) fall time

The driver was then tested with series and shunt diodes. For the series diode, turn on time from -11.8 V to 2.6 V was 109 ns and turn off time from 2.1 V to -11.8 V was 120 ns, as shown in Figure 3.38. For shunt diode, turn on time from -11.8 V to steady 1 V was 513 ns, and turn off time from 1 V to -11.8 V was 650 ns, as shown in Figure 3.39.

The series diode has a faster switching time than the shunt diode. Switching time is dependent on the forward bias current, reverse bias current, and the carrier lifetime. Since the forward bias current and reverse bias current are equivalent, the series diode will have a faster switching time since its carrier lifetime is less than carrier lifetime of the shunt diode.

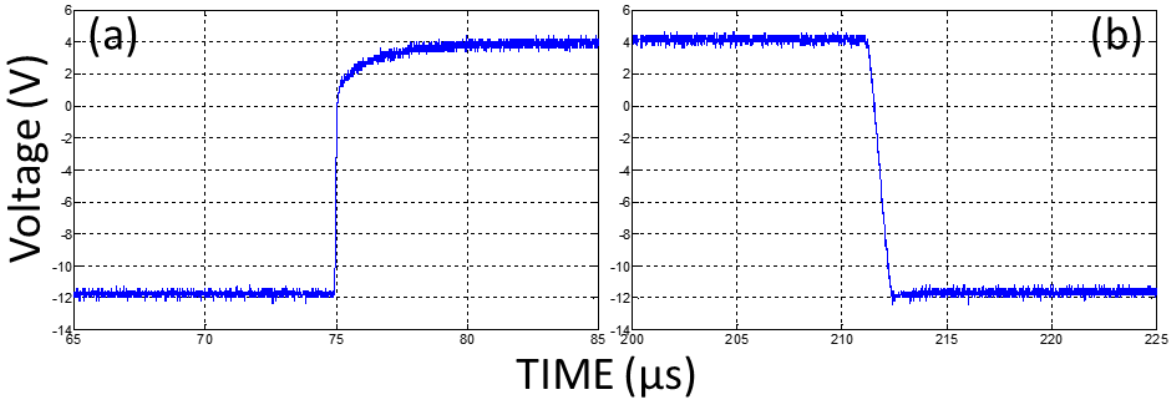

Figure 39: Measured switching time of PIN diode driver with series diode as load: (a) rise time; (b) fall time

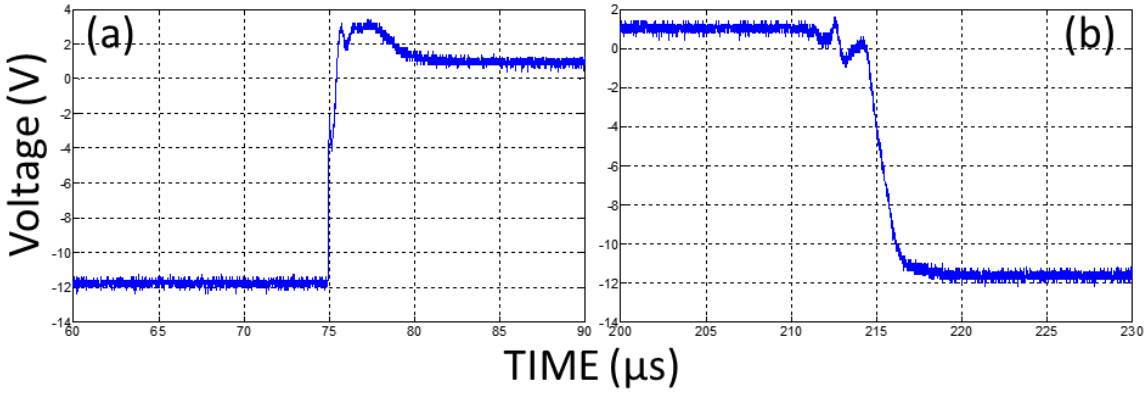

Figure 40: Measured switching time of PIN diode driver with shunt diode as load: (a) rise time; (b) fall time

3.5 System integration, Laboratory tests, and field tests

3.5.1 Board and Chassis design

The T/R switch was integrated into a single module. The high power section of the circuit was separated from the low power section using a milled cavity. This was done to increase isolation between the receiver and transmitter. One side of the chassis contained the T/R switch and the other side housed the driver circuitry. The interface between the two sides was done via vertical interconnects. Four cooling fans, one for each PIN diode, were attached to the housing lid to keep them at a temperature well below the maximum junction temperature. Two six pin mini d-sub connectors were used to supply

power and TTL control signal to each driver board. Figure 3.40 shows photographs of the T/R switch module.

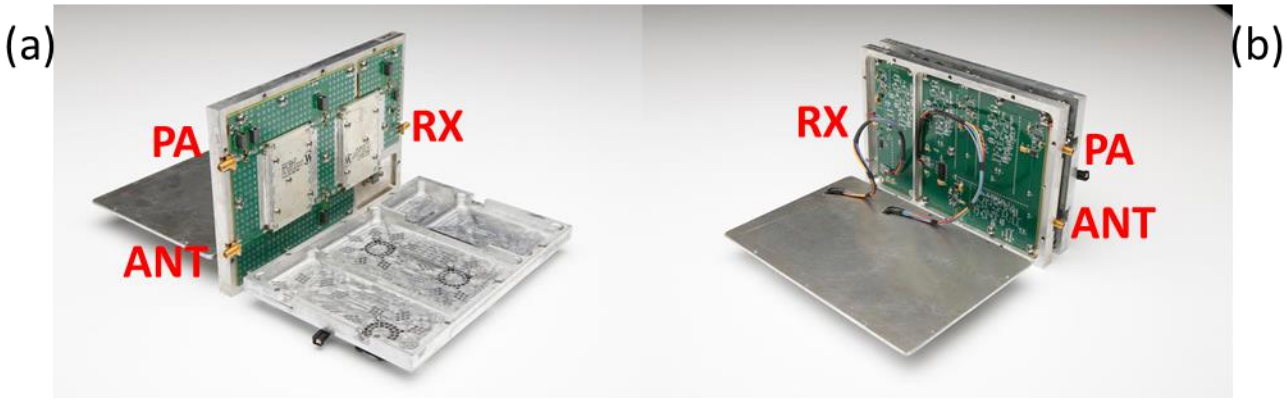

Figure 3.41: Photographs of the circuit developed (a) T/R switch side; (b) Driver side

Eight T/R switches were integrated into a multi-channel chassis, as shown in Figure 3.41. Low-noise power supplies were used to provide +5 V and -12 V to the voltage distribution board, which in turn distributed power and TTL to the driver boards. Another +12V power supply distributed power to the cooling fans.

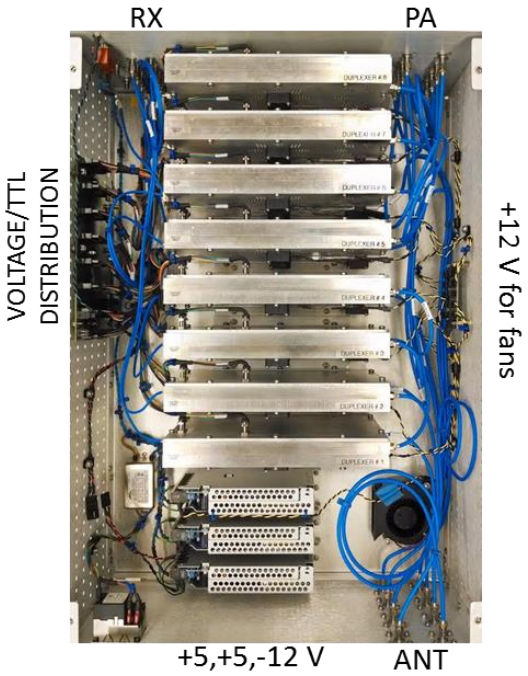

Figure 3.42: T/R switches for 8 channels

3.5.2 Characterization of the Complete Modules

3.5.2.1 Integrated system VNA test

A 4-port VNA was used to measure the insertion loss and isolation during transmit and receive. Figures 3.42 and 3.43 shows the insertion gain and isolation, respectively, during receive, and Figures 3.44 and 3.45 show it during transmit. Included are the ideal simulation, high level simulation, EM/circuit co-simulation, first prototype, and final design results.

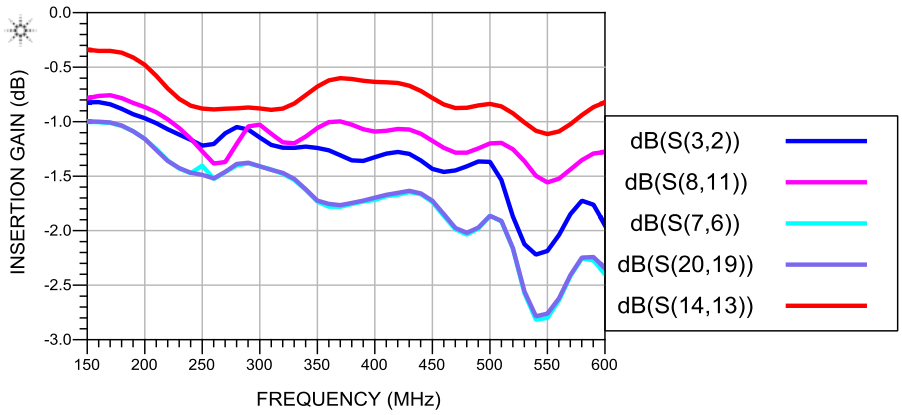

Figure 3.43: Simulated vs measured insertion gain between ANT and RX during receive for: (a) Ideal (S(14,13)); (b) High level (S(8,11)); (c) EM/circuit co-sim (S(3,2)); (d) Prototype (S(7,6)); (e) Final design (20,19)

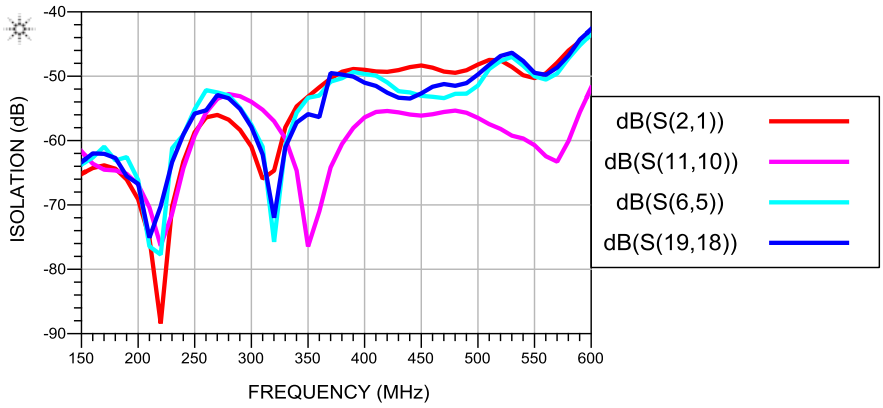

Figure 3.44: Simulated vs measured coupling between PA and ANT: (a) High level (S(11,10)); (b) EM/circuit co-sim (S(2,1)); (c) Prototype (S(6,5)); (d) Final design (19,18)

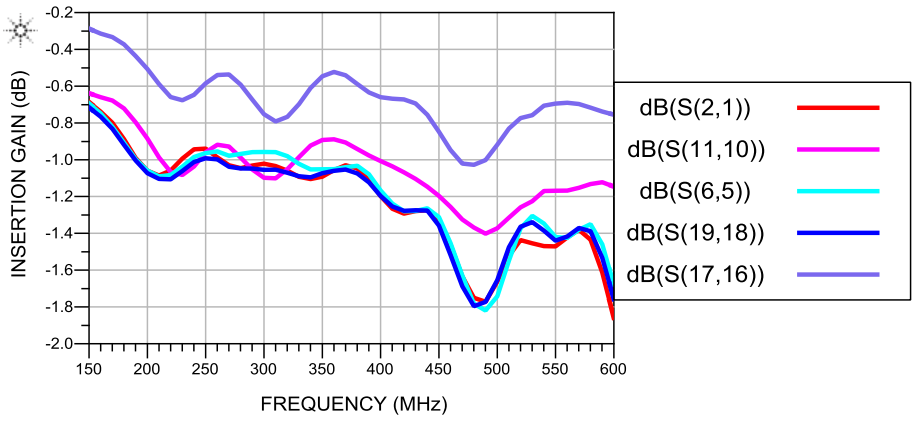

Figure 3.45: Simulated vs measured insertion gain between PA and ANT during transmit: (a) Ideal (S(17,16)); (b) High level (S(11,10)); (c) EM/circuit co-sim (S(2,1)); (d) Prototype (S(6,5)); (e) Final design (19,18)

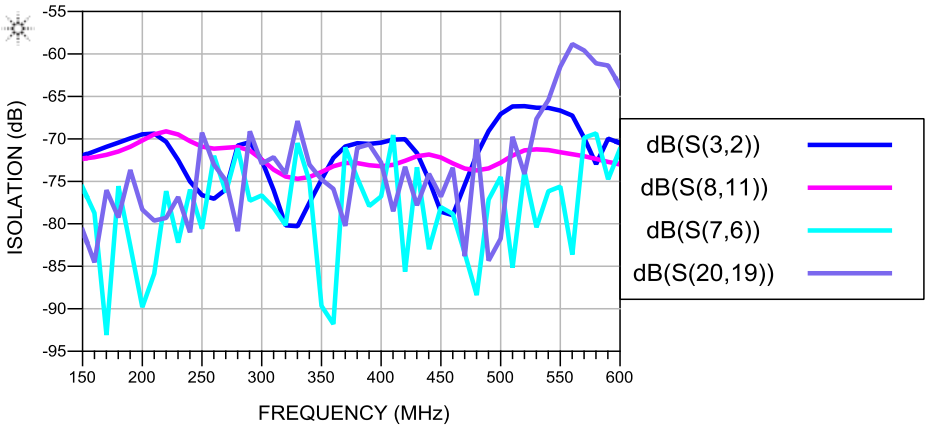

Figure 3.46: Simulated vs measured coupling between ANT and RX during transmit for: (a) High level (S(8,11)); (b) EM/circuit co-sim (S(3,2)); (c) Prototype (S(7,6)); (d) Final design (20,19)

The maximum variance in insertion loss between the EM simulation and final design is 0.15 dB during transmit and 0.4 dB during receive. The prototype and final design response match up very well.

3.5.2.2 Switching time

Switching time was measured by injecting a long pulse into the antenna port of T/R switch to simulate a continuous wave, while the diodes were toggled by the driver. The TTL signal had a width of 10 µs. Switching time of the series PIN diode was monitored, as well as the signal at the receiver port.

Turn off time was measured from 50% TTL to 10% RF at the receiver port. Inversely, turn on time was measured from 50% TTL to 90% RF at the receiver port. Turn off time was found to be 200 ns, and the turn on time was 1300 ns as shown in Figure 3.46. The COTS switch used in the old radar system had a turn on time of 2.4 µs and turn off time of 4.1 µs.

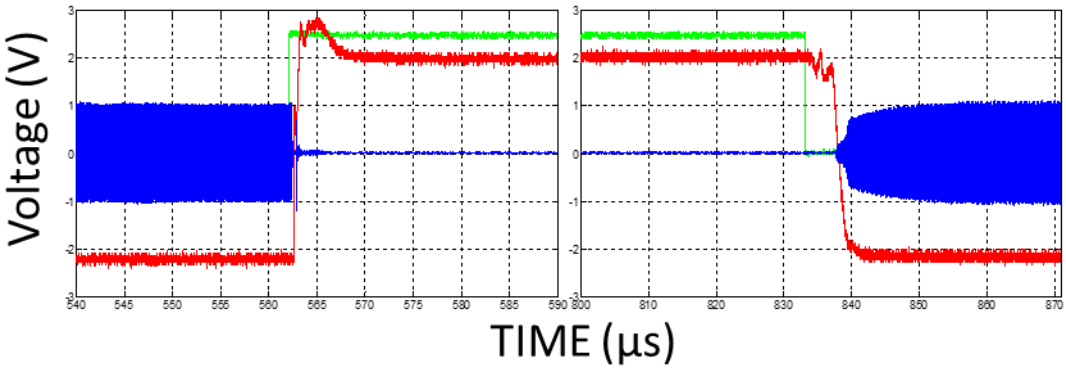

Figure 3.47: Measured switching time: (a) Turn off time measured from 50% TTL (Green) signal to 10% RF (Blue) signal; (b) Turn on time measured from 50% TTL (Green) signal to 90% RF (Blue); Also shown is the shunt diode response (Red)

We also verified that increasing the reverse bias voltage beyond -12 V does not reduce the switching time significantly. Instead, it increased the transient response of the switching of the diodes. The ideal point was -12 V, as predicted from simulations.

3.5.2.3 Output power vs. input power in Transmit mode

Loss through the T/R switch during transmission was measured through the test setup shown in Figure 3.47. All tests were performed for a frequency range of 150 – 600 MHz. A signal generator (Direct Digital Synthesizer (DDS)) was used to provide a 10 µs pulse with 12% duty cycle at different power levels. The signal was amplified and injected into the PA port of the T/R switch. The output signal at the ANT port was attenuated by 50.35 dB and fed into the oscilloscope.

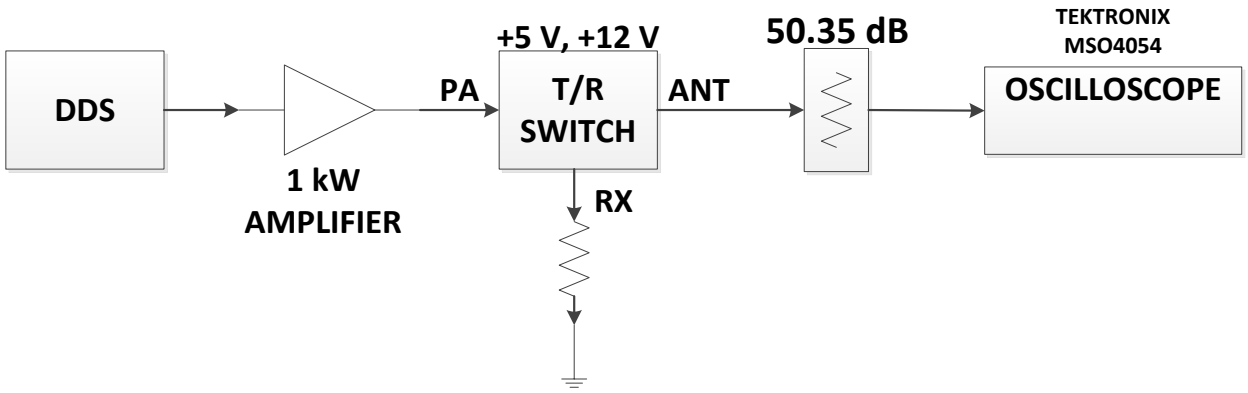

Figure 3.48: Power test setup

Power at the outputs of the DDS and 1 kW amplifier were measured first to calculate the gain and exact power being received at the PA port. The DDS signal was directly measured with an oscilloscope. The amplifier output was attenuated by 50.35 dB before being measured by the oscilloscope. Figure 3.48 shows the output power and gain of the amplifier. A 0 dBm input signal resulted in approximately 58 dBm of peak power at the amplifier output.

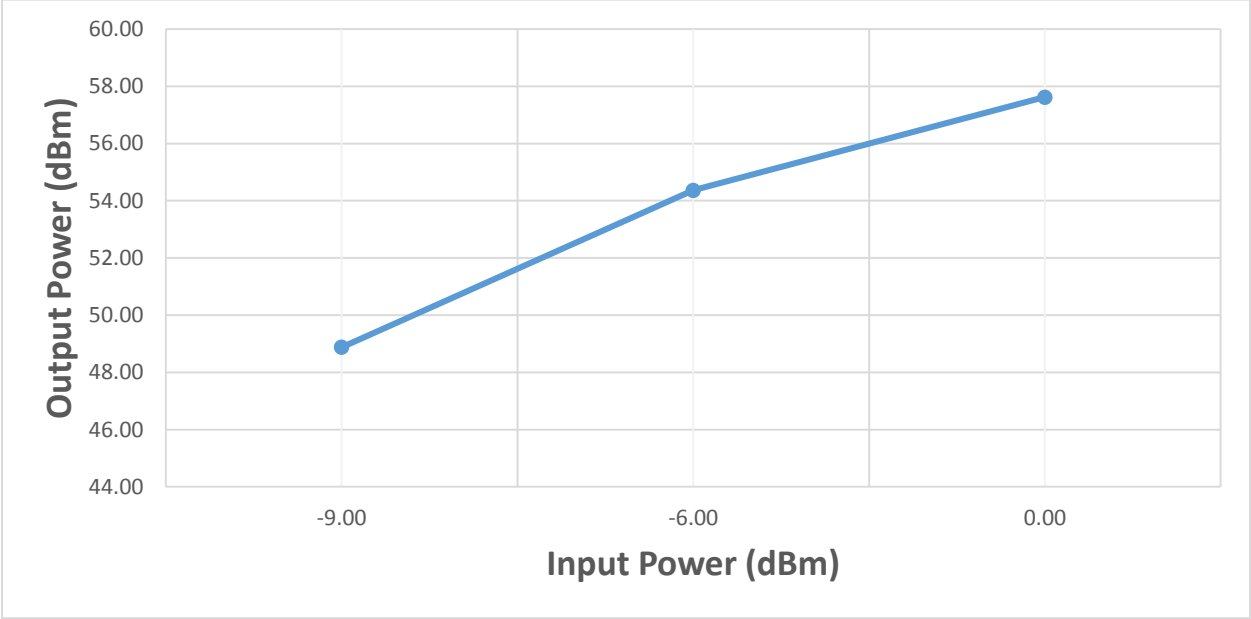

Figure 3.49: Measured Input power vs 1 kW power amplifier output power

The amplifier was then connected to the T/R switch to measure the loss during transmission. Figure 3.49 shows the comparison of the input power at the PA port and the output power at the ANT port. Figure

3.50 shows the loss during transmission. At 1 kW peak power, loss is less than 0.025 dB through the transmission pathway.

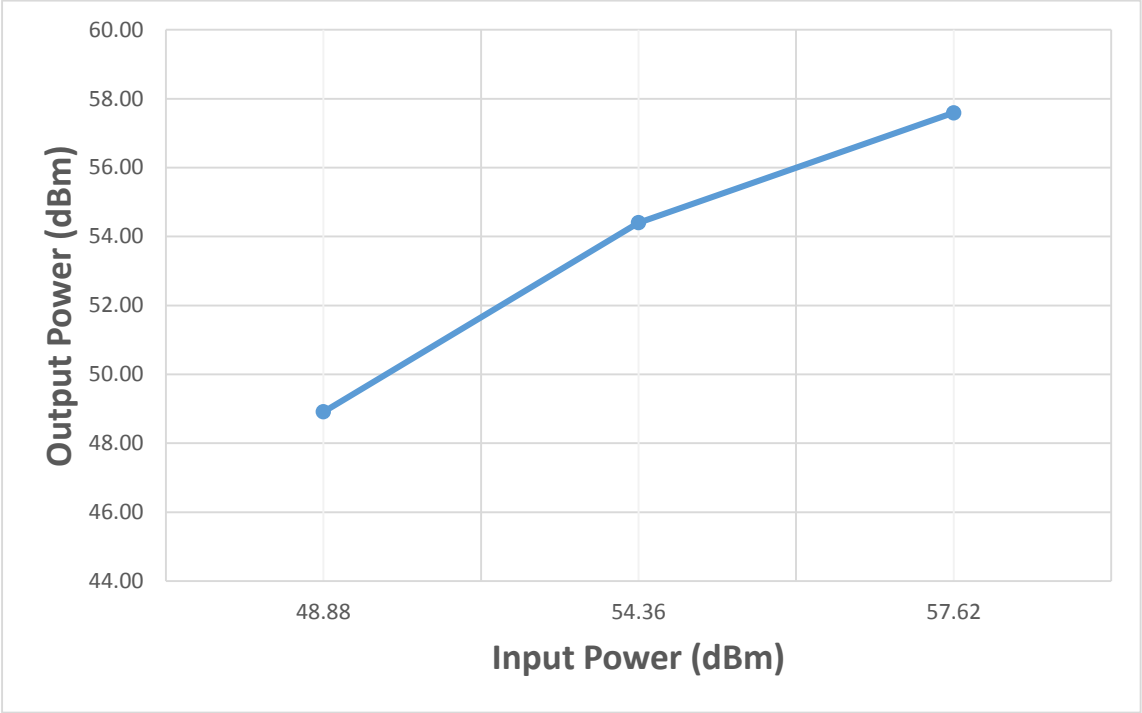

Figure 3.50: Measured Input (PA) power vs output (ANT) power during transmission

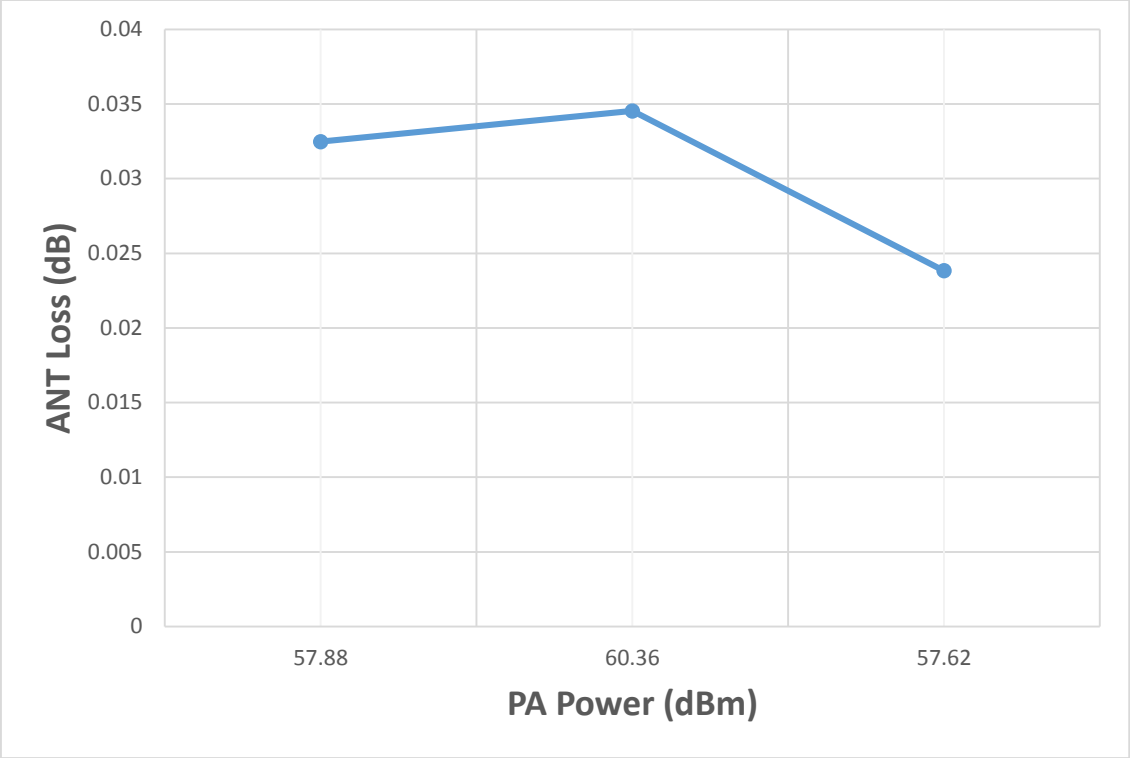

Figure 3.51: Measured Loss between PA and ANT ports of T/R switch during transmission

3.5.2.4 PIN diode temperature vs peak power with different duty cycles

PIN diode temperature was measured at 1 kW peak power, with pulse repetition frequency (PRF) of 10 kHz, 12 kHz, and 15 kHz. Pulse length was set to 10 µs. This corresponded to average power of 100 W, 120 W, and 150 W, respectively. Temperature was measured using a FLIR i7 camera.

Figures 3.51 show the thermal image of the hottest PIN diode, D1 (series diode), at PRF of 10 kHz, 12 kHz, and 15 kHz.

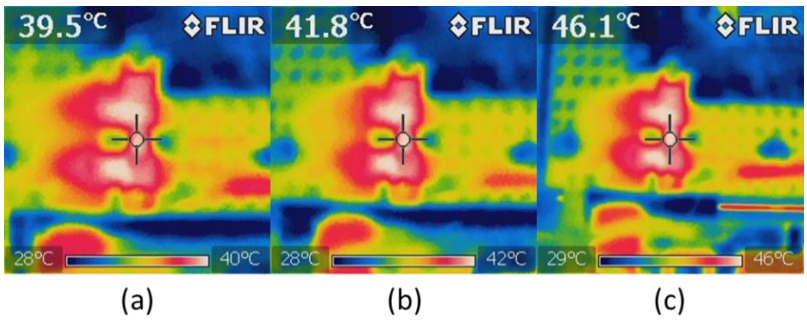

Figure 3.52: Series pin diode thermal image at PRF of: (a) 10 kHz; (b) 12 kHz; (c) 15 kHz

The highest temperature was around 46 °C for a PRF of 15 kHz. This is well below the PIN diode junction temperature of 175 °C.

3.5.2.5 Loopback Test

The performance of the system equipped with the T/R switch was evaluated by performing a loopback test with a delay line. The radar's waveform generator was used to provide a 10 µs pulse with a PRF of 12 KHz and frequency range of 150 to 450 MHz which was amplified and injected into the T/R switch. The upper operating frequency was set by the waveform generator. The 1 kW peak power output signal at the antenna port was attenuated by 80 dB and fed into the directional coupler. The output of the direction coupler goes through a delay line and is fed back into the directional coupler. The delay line has a delay of 11.9 µs which represents a target at a free space range of 1785 m [24]. The signal then travels through the directional coupler, then the 80 dB attenuator, and back into the antenna port and outputs through the receiver port. Figure 3.52 shows the measured response after 1000 coherent integrations. The SNR was close to 60 dB.

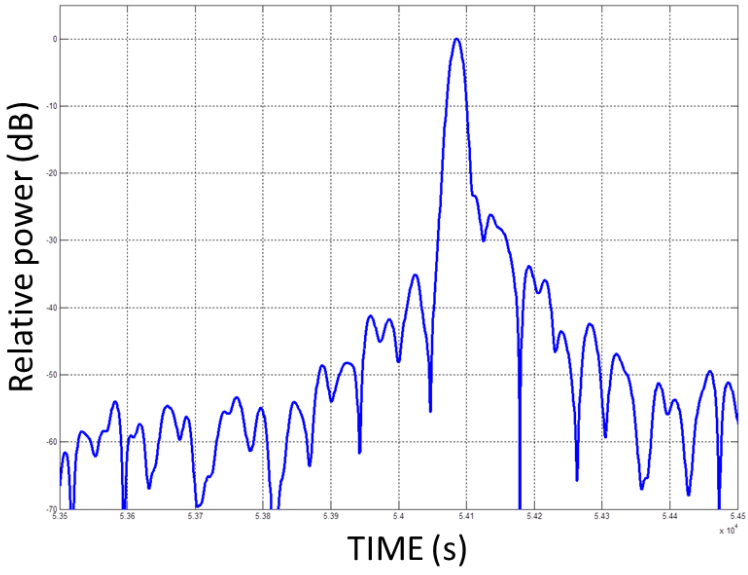

Figure 3.53: Measured impulse response with a delay line

3.5.3 Sample Field results

A two-channel system based on the new T/R switches was deployed to Greenland on an NASA C-130H aircraft in the Spring of 2015. The RF section included two of the newly T/R switches operating between 180 – 450 MHz. The lower limit was set by the antenna response, while the upper limit was set by the DDS, as mentioned earlier [24]. Each T/R module was outputting 1 kW of peak power with a pulse repetition frequency of 12 kHz and bandwidth of 270 MHz. 1 µs pulses were used to measure ice surface and 3 and 10 µs were used to sound the bedrock.

Figure 3.53 and 3.54 shows sample results obtained from data collected with a radar equipped with the new T/R modules. From the A-scope shown Figure 3.54, it can be seen that the noise floor is approximately -90 dB while the bedrock return is detected by more than 36 dB signal-to-noise ratio.

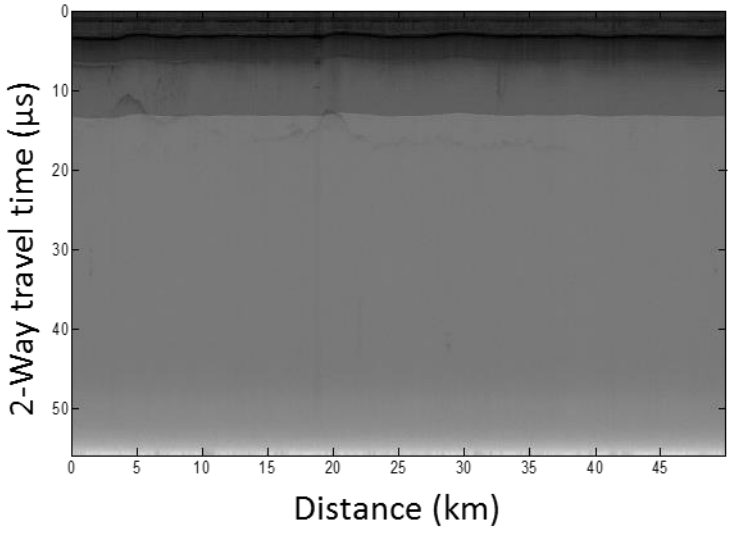

Figure 3.54: Sample echogram obtained from data collected with the system equipped with the new T/R switch with bandwidth of 270 MHz and total peak power of 2 kW

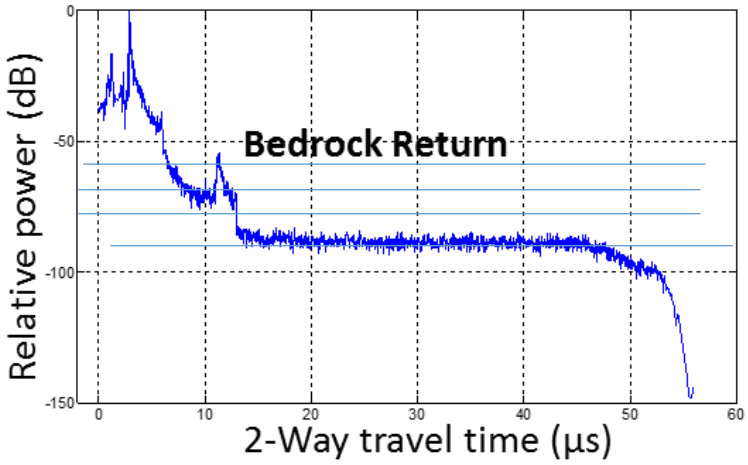

Figure 3.55: A-Scope obtained from the echogram shown in Figure 3.53.

4 160-230 MHz T/R switch

This chapter discusses the design and implementation of a high power transmit/receive (T/R) module in the frequency range of 160 to 230 MHz. This T/R module was developed to achieve a compact, modular RF assembly that would operate with the new antennas developed for the NASA DC-8, which operate in the 165-215 MHz range.

The module also includes the high-power amplifier, driver amplifier as well as the required biasing circuitry. The close integration of the power amplifier and driver reduces interconnection losses while miniaturizing and integrating one of the RF subsystems of the radar.

A set of six of these modules were integrated into a six 19” rack mountable chassis with low-noise switching power supplies. The six chassis combined weigh 30% less than older system, providing four times as much RF power.`

4.1 Design overview

The module consists of a 50 W driver amplifier, a 1 kW high-power amplifier along with a T/R switch similar to that described in Section 3.2.1, except that it was optimized for a different frequency range. This section provides an overview of the two components of the T/R switch that are different from those already described in Section 3.2.1. It also describes the integration of high-power amplifier and driver developed by R.Crowe [5].

4.1.1 Quadrature Hybrids

Two QH8100 quadrature hybrids from Werlatone Inc. were used for this design. The quadrature hybrids are capable of operation in the 100-512 MHz range. Table 1 lists the relevant parameters of this quadrature hybrids for the frequency range of 160 – 230 MHz. These values were extracted from the datasheet, as well as the scattering parameters supplied by Werlatone.

Table 4.10: Summary of relevant parameters for the Werlatone QH8100

Frequency	160 – 230 MHz
Power	250 W continuous
Insertion Loss	0.4 dB maximum
Isolation	20 dB minimum
Phase Balance	$90^{\circ} \pm 1.04^{\circ}$ maximum
Amplitude Balance	± 0.286 dB maximum
VSWR	1.05:1 maximum

For the 15% duty cycle, the power amplifier provides average power of 150 W. These quadrature hybrids can handle up to 250 W of continuous power over the operating frequency range of 100 to 512 MHz. For a frequency range of 160 – 230 MHz, the maximum insertion loss is 0.4 dB and minimum isolation is 20 dB between all ports.

4.1.2 High Power Amplifier and Driver

For the power amplifier stage, we relied mostly on previous work performed by R. Crowe [5] and others. A 1-kW amplifier reference design provided by Freescale for VHF Digital TV Broadcast was tuned to extend its lower operating frequency down to 160 MHz. The amplifier uses the Freescale MRFE6VP61K25H transistor. The gate bias voltage was adjusted till it operated as a class-C amplifier. The class-c amplifier was chosen due to narrow-band pulse operation, efficiency, and linearity of the gain [5].

The driver circuit is a two-stage assembly based on discrete modules from Polyfet RF devices. The combined driver/power amplifier is capable of providing peak power level in excess of 60 dBm with an input close to 0 dBm.

4.1.3 Computer Simulations of the T/R switch

Advanced Designs Systems (ADS) were used to perform low level, high level, and electromagnetic (EM) simulation of the T/R switch. The printed circuit board (PCB) layout was done in Altium Designer.

4.1.3.1 Low level simulation

The design of the T/R switch was first simulated under semi-ideal conditions using a linear s-parameter simulation, only taking into account the response of the Werlatone QH8100 hybrids. Figure 4.1 shows the simulation setup for the circuit in transmit mode, in which the forward-biased PIN diodes are modeled as a perfect short circuit.

For receive mode, diodes D2 and D3 are modeled as perfect open circuit, as shown in Figure 4.2. The simulated insertion gain (power amplifier to antenna) in transmit mode, as well as in receive mode (antenna to receiver) are presented in Figure 4.3. Isolation during receive mode is shown in Figure 4.4.

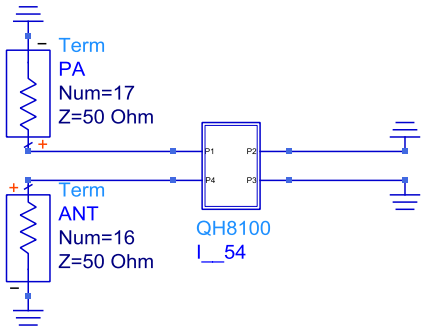

Figure 4.56: Simulation setup representing semi-ideal behavior in transmit state

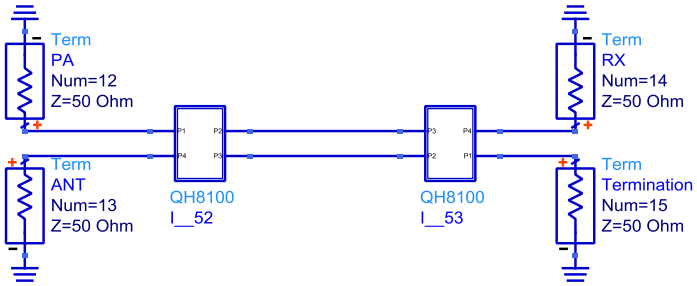

Figure 4.57: Simulation setup representing semi-ideal behavior of the circuit in receive state

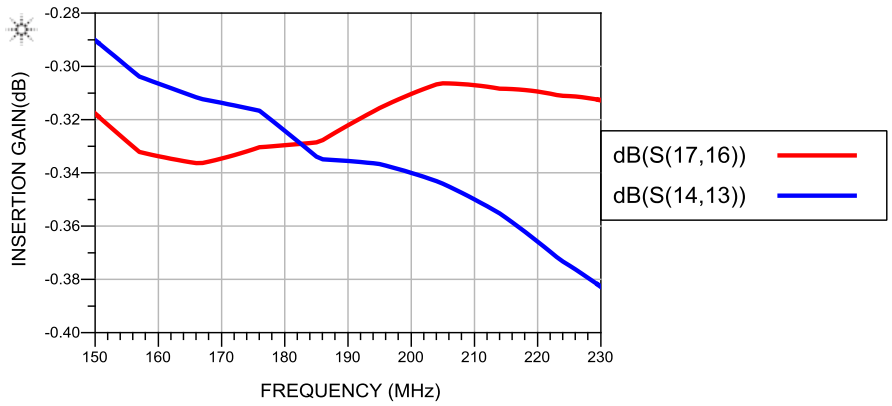

Figure 4.58: Simulated response for the insertion gain during: (a) Transmit between PA and ANT ports (S(17,16)); (b) Receive between ANT and RX ports (S(14,13))

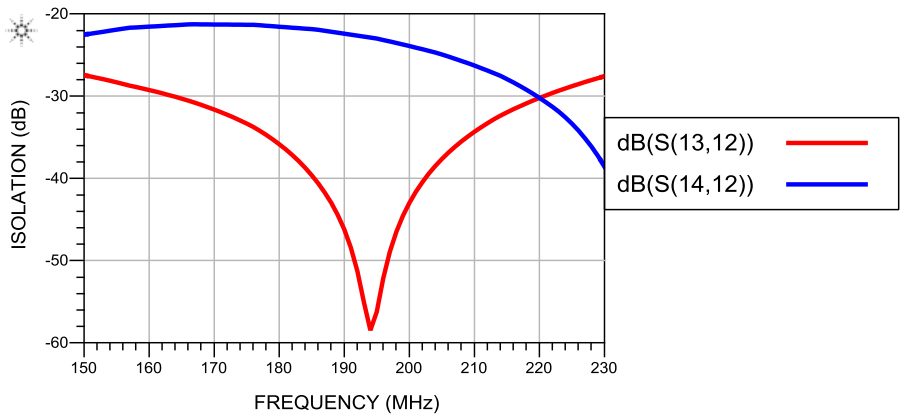

Figure 4.59: Simulated isolation in receive mode between: (a) PA and ANT ports(S(13,12)); (b) PA and RX ports (S(14,12))

Maximum simulated insertion gain caused by ideal circuits is 0.336 dB at 166 MHz during transmit and 0.383 dB at 230 MHz during receive. During receive mode, minimum simulated isolation was 27 dB between power amplifier (PA) and antenna (ANT) ports and 21 dB between the power amplifier and receive (RX) ports. To include the effects of the components, higher level simulations were performed.

4.1.3.2 High Level Simulations

After verifying the circuit concept with QH8100 hybrids, the effects of the remaining components were integrated into the simulated design as shown in Figure 4.5. Scattering parameters for the hybrids, PIN diodes, and inductors were provided by the manufacturer. This simulation does not include the effects of interconnects.

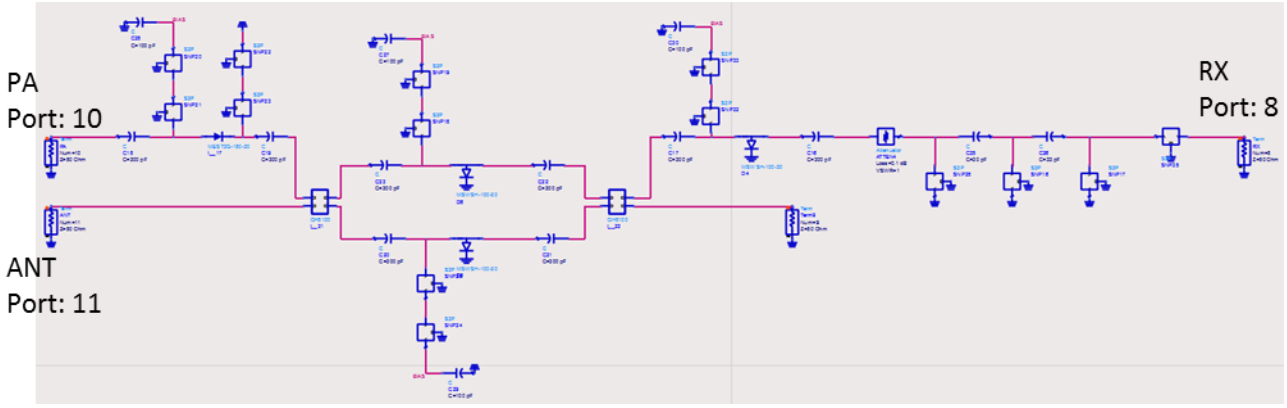

Figure 4.60: ADS simulation setup including first order effects in all the components.

A linear s-parameter simulation was performed using this setup. Figures 4.6 and 4.7 show the insertion gain and isolation during transmit and Figures 4.8 and 4.9 show it during receive.

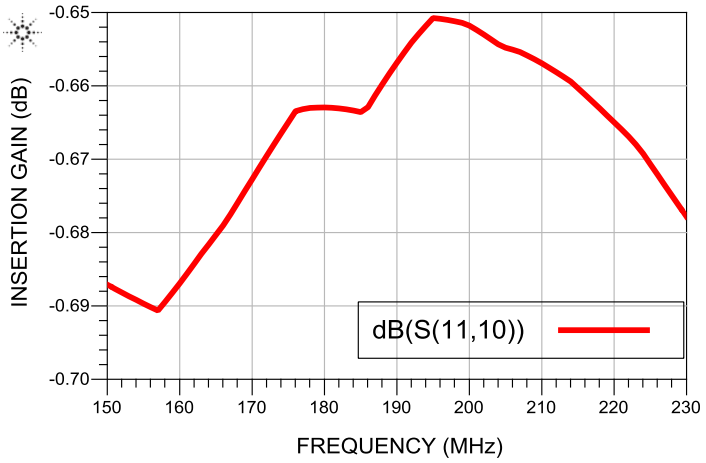

Figure 4.61: Simulated insertion gain between PA and ANT ports (S(11,10) during transmit

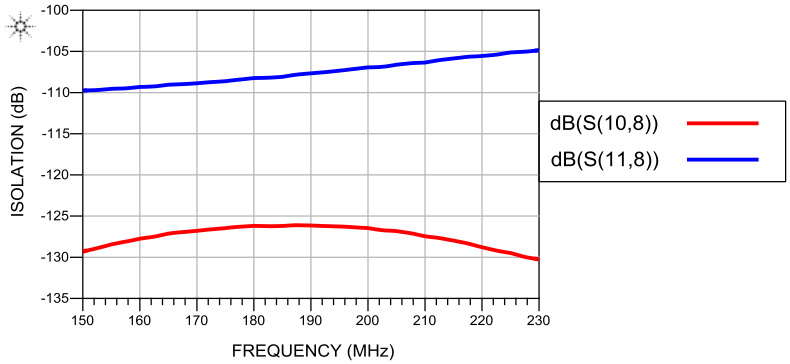

Figure 4.62: Simulated coupling during transmit between: (a) PA and RX ports (S(10,8)); (b) ANT and RX ports (S(11,8))

During transmit, there was low loss between PA and ANT ports and high isolation between PA and ANT ports and PA and RX ports. Maximum simulated insertion loss during transmit is 0.691 dB at 157 MHz. Minimum simulated isolation between PA and RX ports predicted by the simulation is 126 dB at 188 MHz and between ANT and RX ports is 104 dB at 230 MHz.

During receive mode, there is low loss between ANT and RX ports, as shown in Figure 4.8, and high loss between PA and ANT and PA and RX ports, as shown in Figure 4.9.

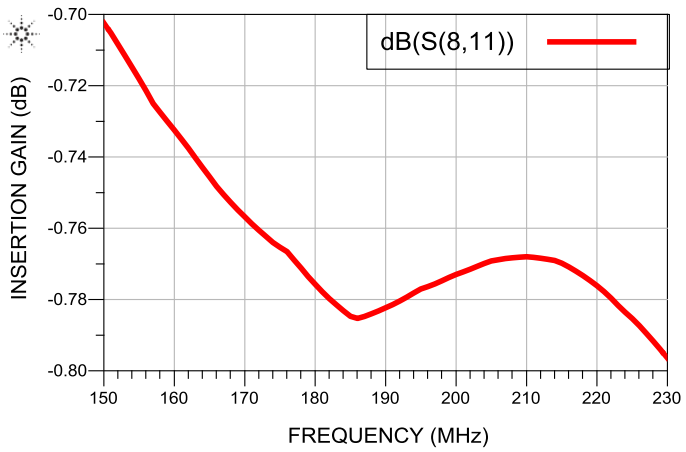

Figure 4.63: Simulated insertion gain between ANT and RX ports (S(8,11)) during receive

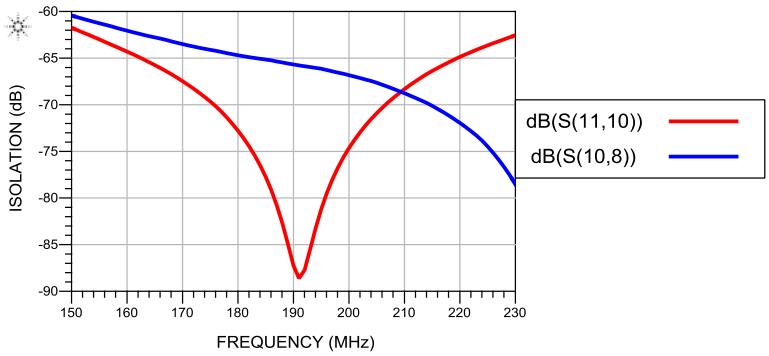

Figure 4.64: Simulated isolation during receive between: (a) PA and ANT ports (S(11,10)); (b) PA and RX ports (S(10,8))

Maximum simulated insertion loss during receive is 0.8 dB at 230 MHz. Minimum simulated isolation between PA and RX (as predicted by the simulation) is 60 dB at 150 MHz and 61 dB at 150 MHz between PA and ANT.

4.1.3.3 EM simulations

To provide a more accurate simulation of the circuit, all the PCB effects were modeled using an EM simulation in Momentum. The EM simulation results are then included in an EM/circuit co-simulation with both PCB layout effects as well as the linear circuit behavior.

4.1.3.3.1 Board Design

The board was designed on a 1 oz. FR4 board, as described in Section 3.2.2.3.1. The line width and gap of the CPWG were calculated to be 119 mils and 100 mils, respectively. The board layout is shown in Figure 4.10.

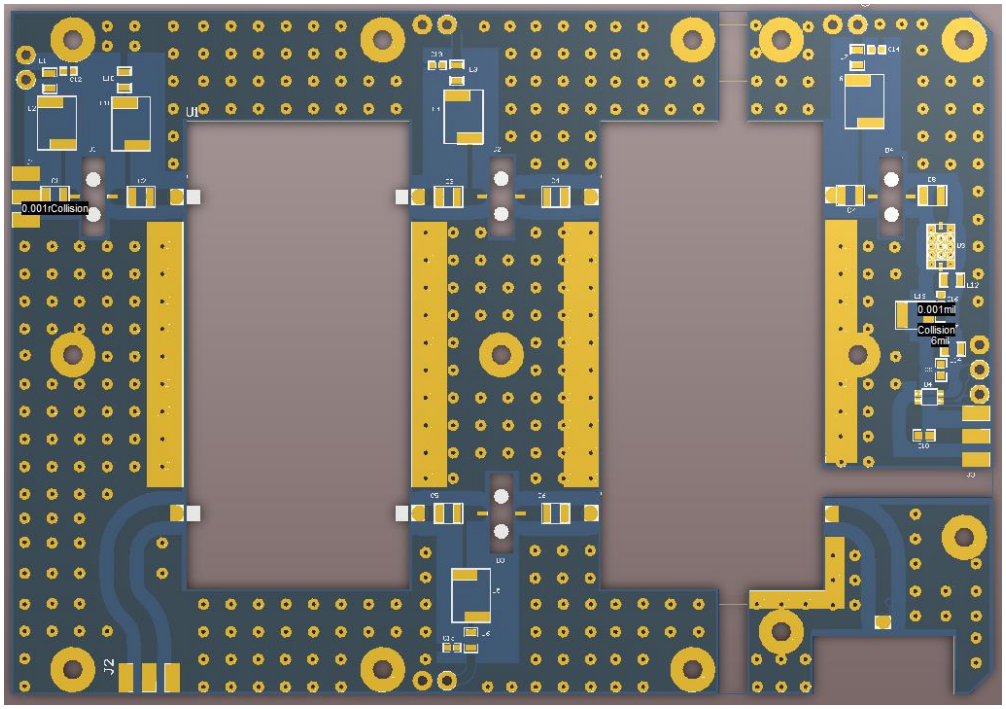

Figure 4.65: T/R switch PCB layout in Altium Designer

4.1.3.3.2 Circuit/EM Co-Simulation

The board was imported into ADS to perform electromagnetic simulations. Figure 4.11 shows the simulated design in ADS.

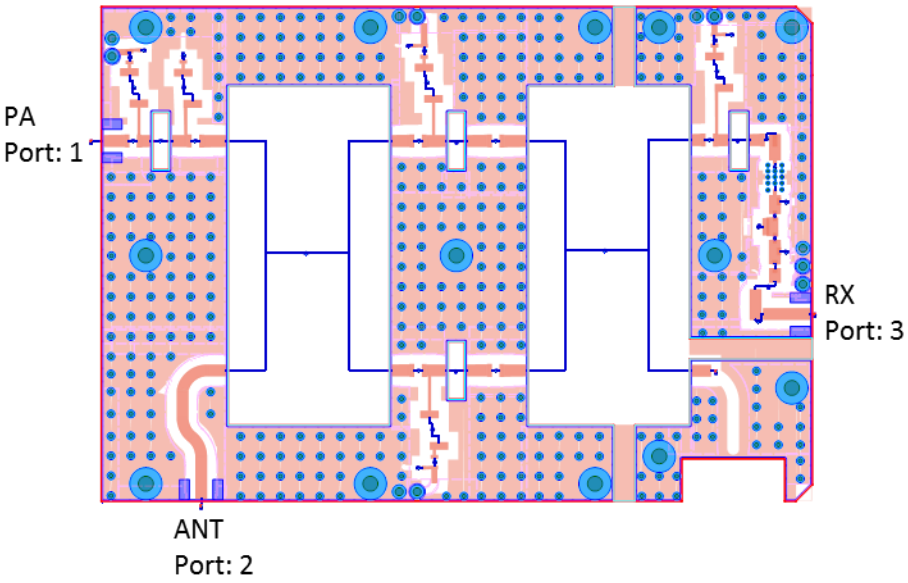

Figure 4.66: Circuit/EM co-simulation setup in ADS

During transmit mode, there is low loss between the PA and ANT ports, as shown in Figure 4.12, and high loss between PA and RX ports and ANT and RX ports, as shown in Figure 4.13.

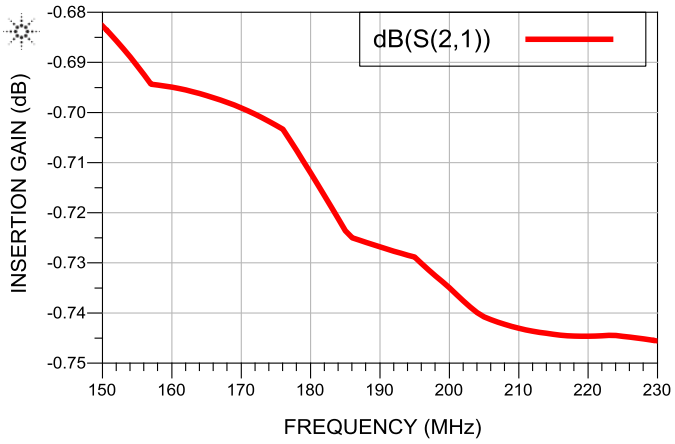

Figure 4.67: Simulated insertion gain between PA and ANT ports during transmit

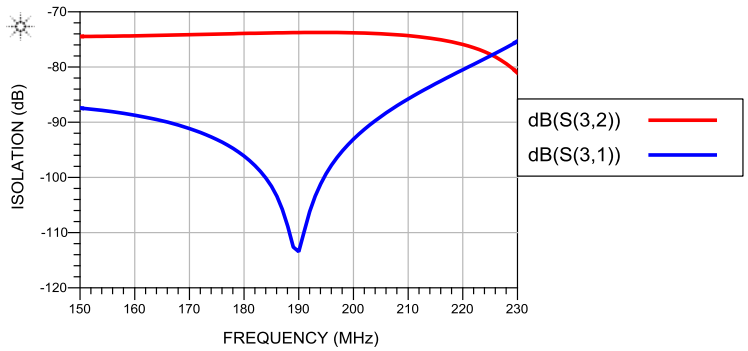

Figure 4.68: Simulated isolation between (a) ANT and RX (S(3,2)); (b) PA and RX (S(3,1))

The maximum simulated insertion loss is 0.746 dB at 230 MHz. The minimum isolation between PA and RX ports and ANT and RX ports, as predicted by the simulation, are 77 dB at 230 MHz and 73 dB at 194 MHz, respectively.

During receive mode, there is low loss between ANT and RX ports, as shown in Figure 4.14, and high loss between PA and ANT and PA and RX ports, as shown in Figure 4.15.

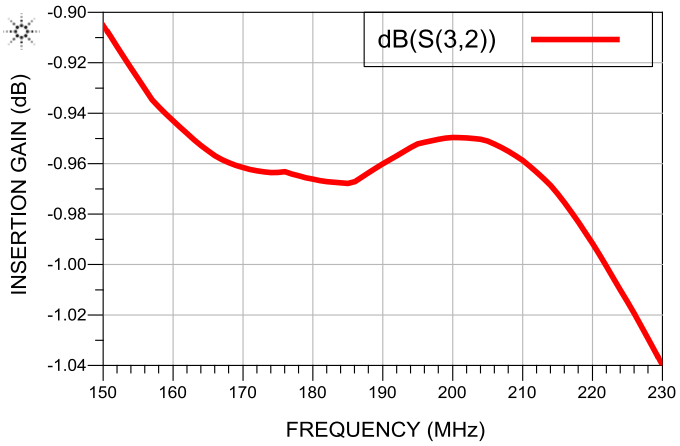

Figure 4.69: Simulated insertion gain between ANT and RX ports during receive

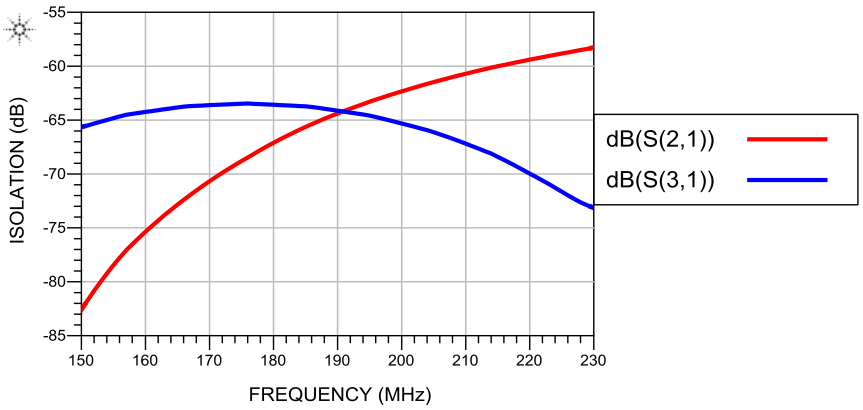

Figure 4.70: Simulated isolation between (a) PA and ANT ports (S(2,1); (b) PA and RX ports(S(3,1)) during receive

The maximum simulated insertion loss is 1.04 dB at 230 MHz. The minimum simulated isolation between PA and RX port is 63 dB at 176 MHz and between PA and ANT ports is 58 dB at 230 MHz.

Figure 4.16 shows the insertion gain difference between low level, high level, and EM/circuit co-simulation during transmit and Figure 4.17 shows it during receive. Losses added by simulated transmission lines increase the insertion loss between the high level simulation and EM/circuit co-simulation by 0.244 dB at 230 MHz during transmit and 0.09 dB at 204 MHz during receive.

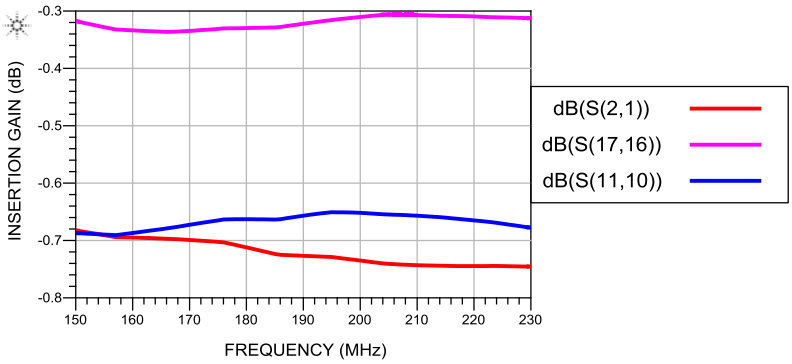

Figure 4.71: Simulated insertion gain between PA and ANT during transmit (a) Ideal (S(17,16)); (b) High level (S(11,10)); (c) EM/Circuit Co-simulation (S(2,1))

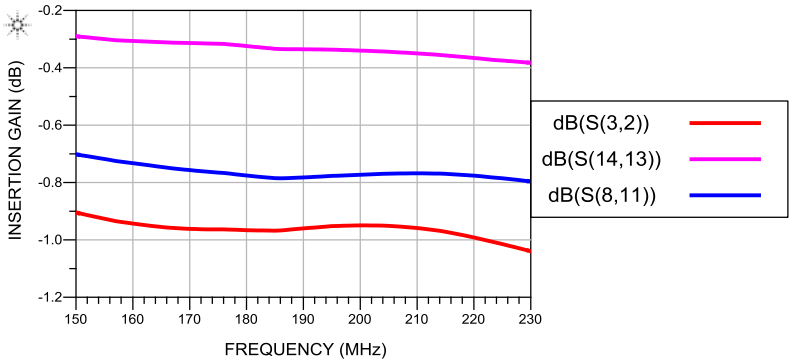

Figure 4.72: Simulated insertion gain between ANT and RX during receive (a) Ideal (S(14,13)); (b) High level (S(8,11)); (c) EM/Circuit Co-simulation (S(3,2))

4.2 Small signal measurements

A 4-port Vector Network Analyzer was used to measure the scattering parameters of the transmit/receive switch. PIN Diodes were connected to a power supply and biased with 100 mA of forward bias current during transmit and 0 V reverse bias voltage during receive.

Figure 4.18 shows the insertion gain of the device along with low level, high level, and EM/circuit co-simulation results during transmit and Figure 4.20 shows it during receive. Figure 4.19 and 4.21 show the isolation during transmit and receive of the actual device. Due to limitations in signal-to-noise ratio in the measurement, isolation value below 80 dB could not be accurately measured without changing the VNA settings.

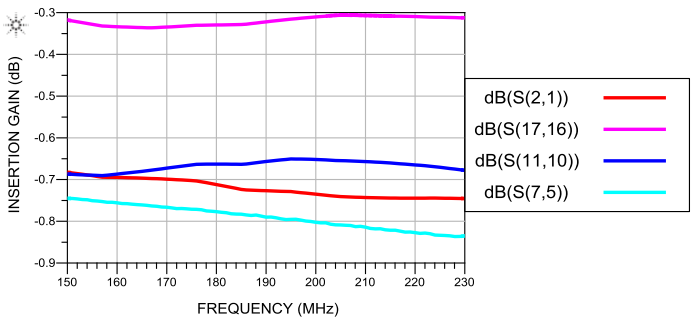

Figure 4.73: Simulated vs measured insertion gain between PA and ANT ports during transmit (a) Ideal (S(17,16)); (b) High level (S(11,10)); (c) EM/Circuit Co-simulation (S(2,1)); (d) Actual (S(7,5))

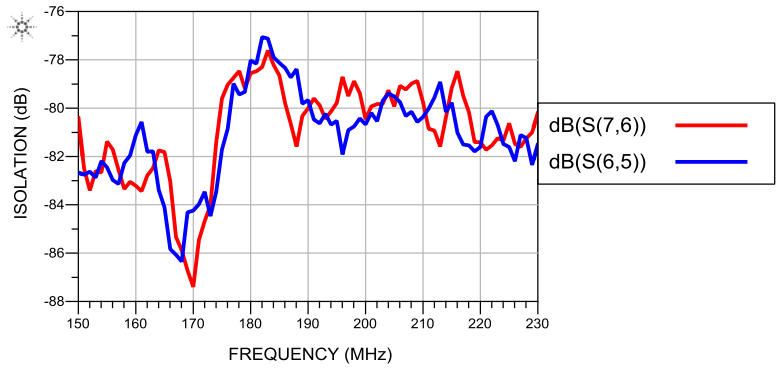

Figure 4.74: Measured isolation during transmit between (a) PA and RX ports (S(7,6)); (b) ANT and RX ports (S(6,5))

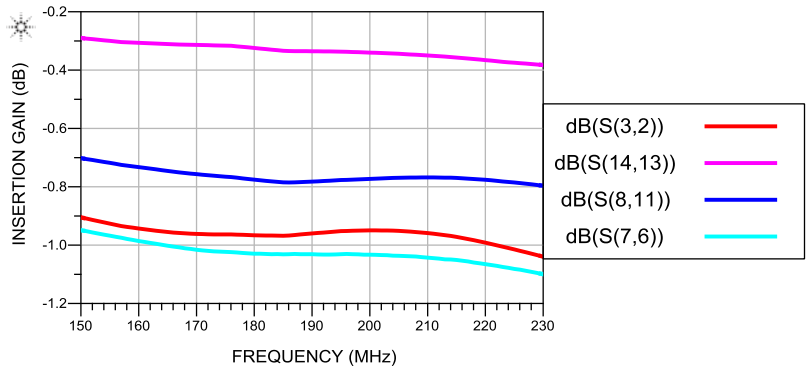

Figure 4.75: Simulated vs measured insertion gain between ANT and RX ports during receive (a) Ideal (S(14,13)); (b) High level (S(8,11)); (c) EM/Circuit Co-simulation (S(3,2)); (d) Actual (S(7.6))

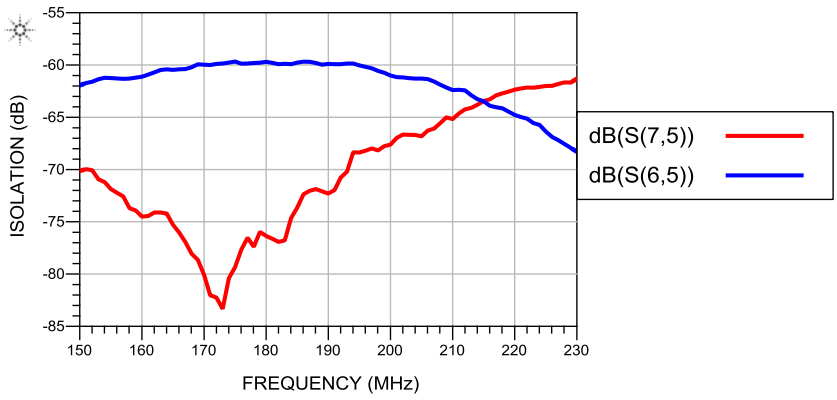

Figure 4.76: Measured isolation during receive between: (a) PA and ANT ports (S(7,5)); (b) PA and RX ports (S(6,5))

The EM/Circuit co-simulation response and actual response match up very well. The maximum variance in insertion loss between EM/Circuit co-simulation simulation and measured response is 0.088 dB during transmit and 0.084 dB during receive.

4.3 System integration, Laboratory tests, and field tests

4.3.1 Board and Chassis design

Figure 4.22 shows the final design of the chassis. It consists of driver amplifier, 1 kW amplifier, T/R switch, and the T/R switch driver. One side of the chassis contained the T/R switch and the other side housed the driver circuitry. To increase isolation between the receiver section and the transmit section, a wall was built into the chassis around the low power side. The design only consisted of the three RF connectors: input, antenna, and receive. The amplifiers and the T/R switch were connected using RF cables instead of connectors to decrease loss. Figure 4.23 shows the overall chassis design.

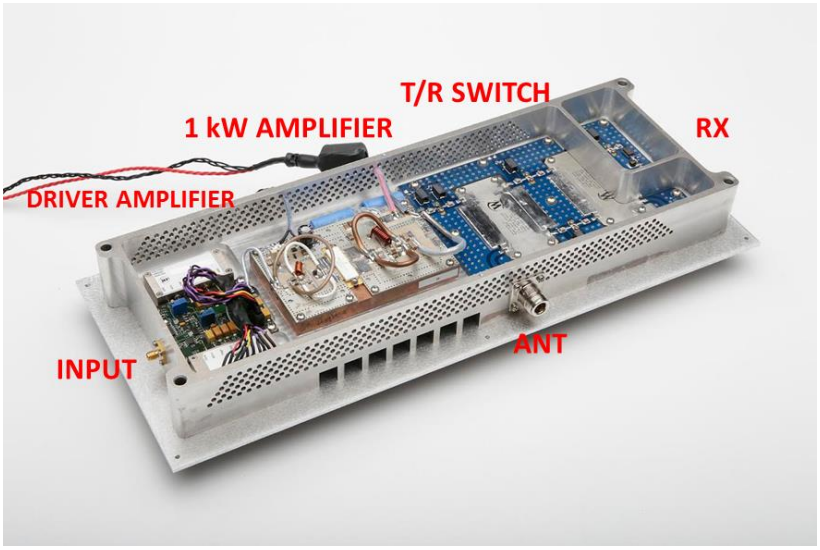

Figure 4.77: Photograph of the T/R switch

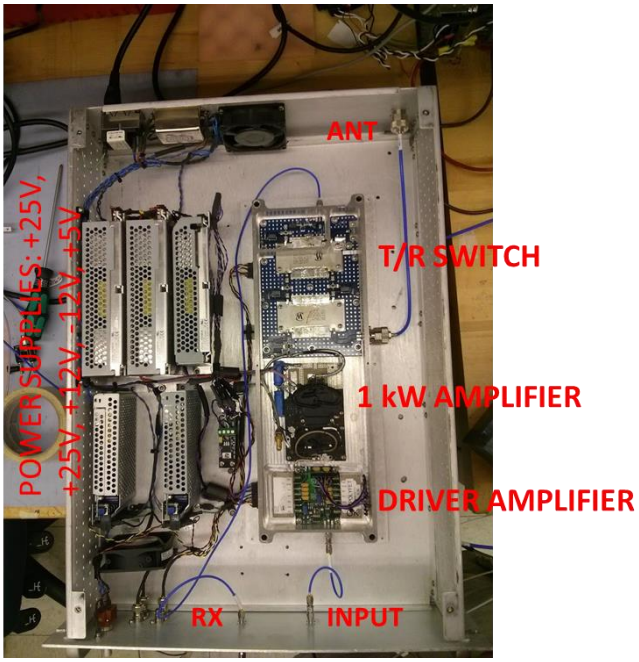

Figure 4.78: Photograph of the T/R switch box

Low-noise power supplies were used to provide +25 V, -12 V, +12 V, and +5 V. Two +25 V supplies were connected in series to provide + 50 V to the 1 kW amplifier. LM317 voltage regulators were used to provide the necessary gate voltage to achieve 25 mA of quiescent current for the 1 kW amplifier. Gate voltages ranged from 4 V to 6 V for different 1 kW amplifiers. The power and TTL signals were distributed through C-Grid connectors. The consumption from the AC line during peak power operation ranged from around 5.2 to 5.41 amps for full output power.

4.3.2 Characterization of the Complete Modules

4.3.2.1 Output power vs. input power in Transmit mode

Loss at the antenna port of the T/R switch was measured through the test setup shown in Figure 4.24. All tests were done for a frequency range of 180 – 215 MHz. A signal generator (Direct Digital Synthesizer (DDS)) was used to provide a 10 µs pulse with 12% duty cycle at different power levels. The signal was amplified and injected into the PA port of the T/R switch. The output signal at the ANT port

was attenuated by 53 dB and fed into the oscilloscope. The video feedthrough signal was directly measured with the oscilloscope.

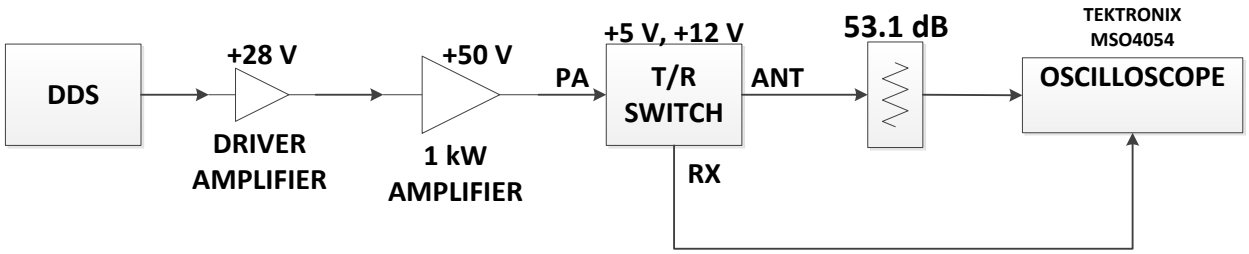

Figure 4.79: Power test setup

Power levels at the output of the DDS and 1 kW amplifier were measured first to calculate the gain and exact power at the PA port. The signal generator signal was directly measured with an oscilloscope. The amplifier output was attenuated by 53 dB before being measured by the oscilloscope. Figure 4.25 shows the output power vs input power and the gain of the amplifier. A -8.79 dBm signal input signal resulted in 1 kW peak power at the amplifier output. At this point, the amplifier is in saturation (P1dB = 57 dBm), but harmonic distortion does not affect radar performance, since the harmonics are filtered out by the output matching network of the power amplifier. The residual power at the second and third harmonic frequencies fall outside the band of operation of the system.

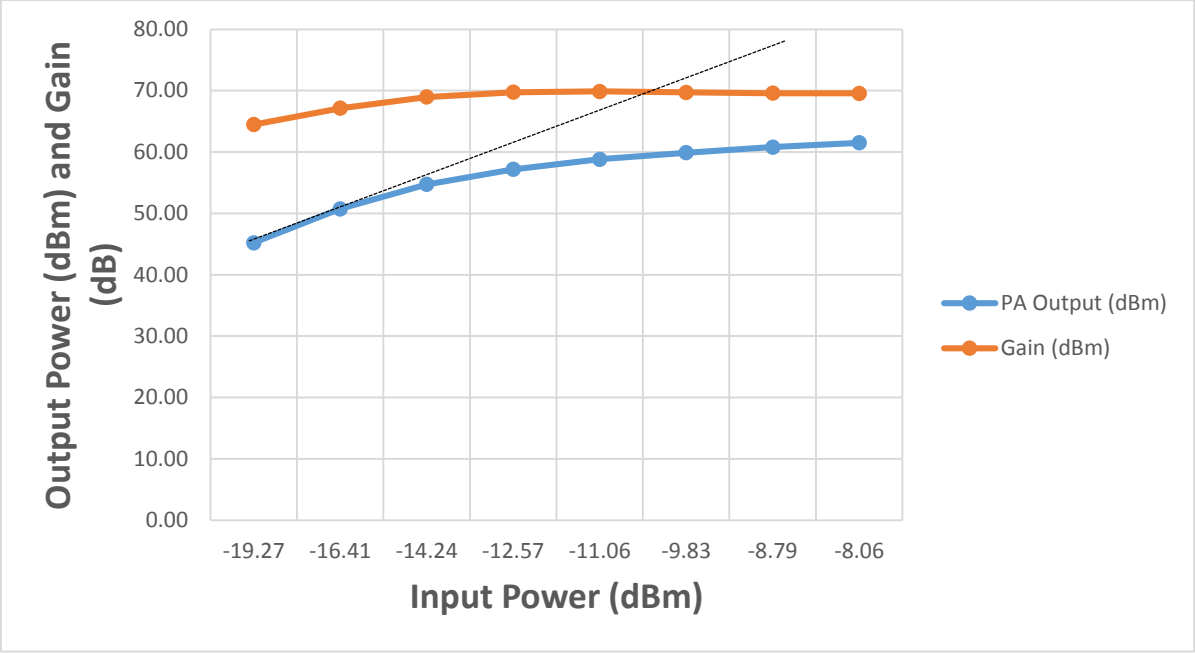

Figure 4.80: Measured power amplifier (PA) output power and gain vs input power. The black dotted line represents the linear response of the amplifier

The amplifier was then connected to the T/R switch to measure the loss during transmit and the feedthrough signal. Figure 4.26 shows a comparison of the input power at the PA port and the output power at the ANT port. Figure 4.27 shows the loss during transmission. The loss is nearly constant between 1.2 and 1.4 dB (0.2 dB variation) across power levels, indicating that the T/R switch does not introduce gain compression effects.

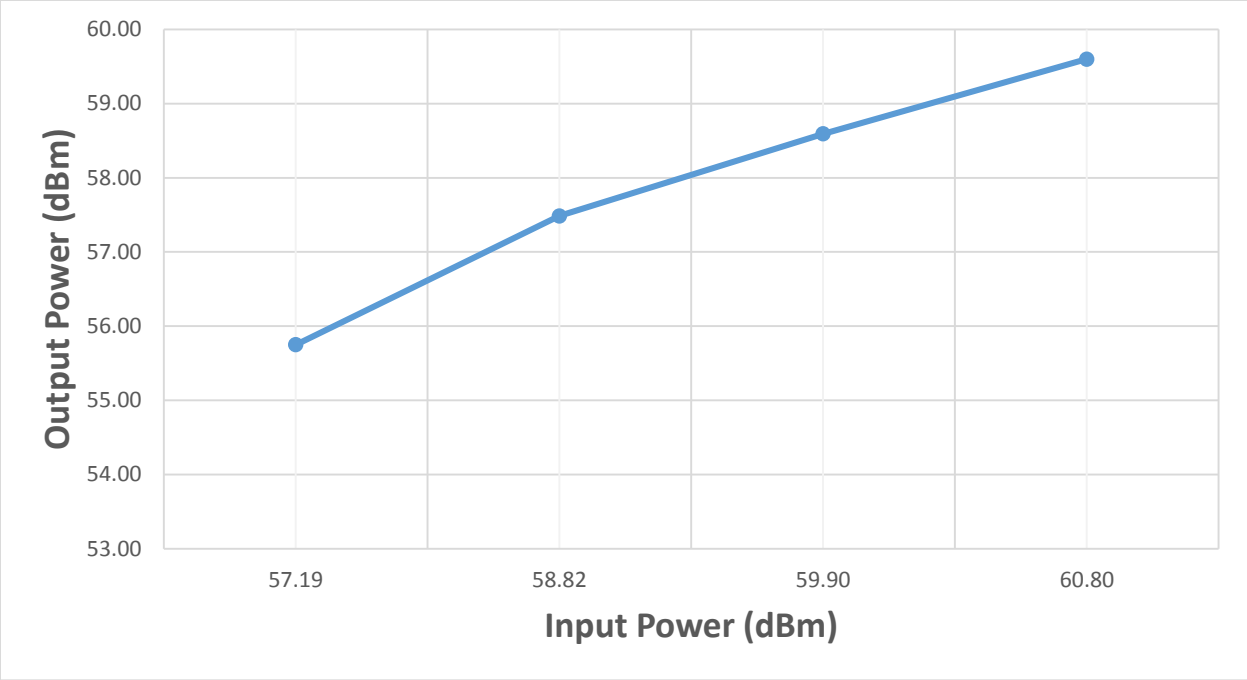

Figure 4.81: Measured Input (PA) power vs output (ANT) power during transmission

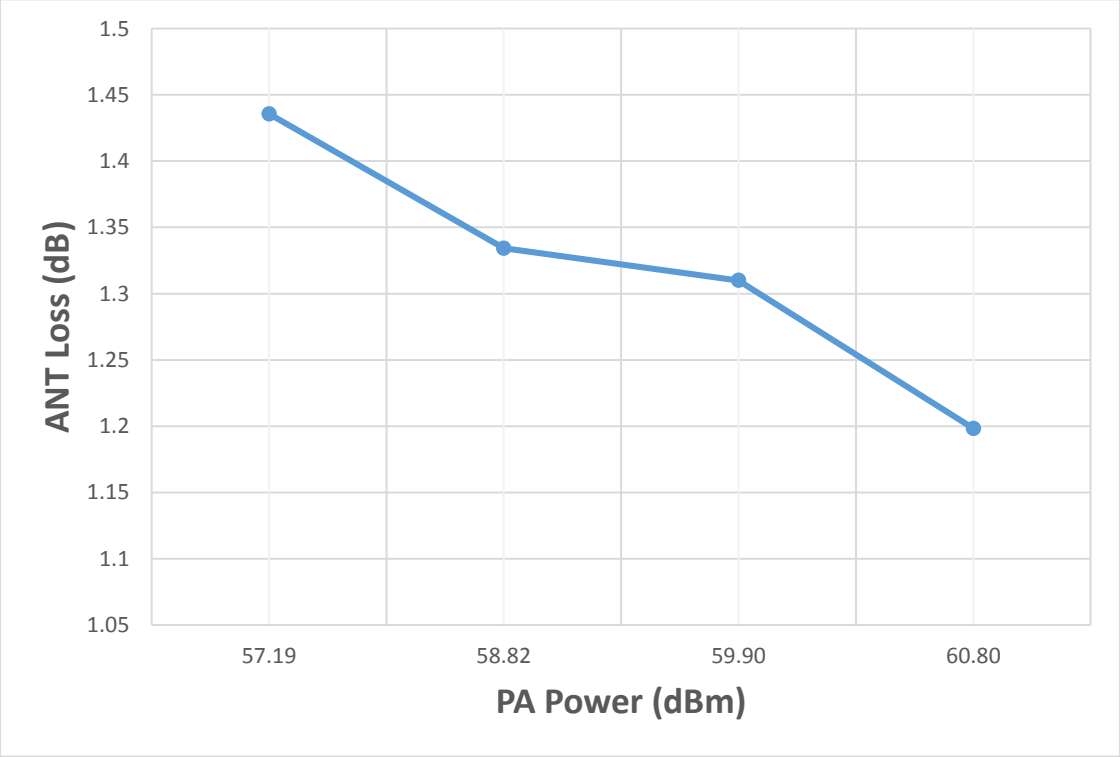

Figure 4.82: Measured Loss between PA and ANT ports of T/R switch during transmission

Figure 4.28 shows the feedthrough signal at the RX port during transmission. The power level at the Rx port changes almost linearly as the transmit power changes, which indicates that the isolation is independent of RF drive level.

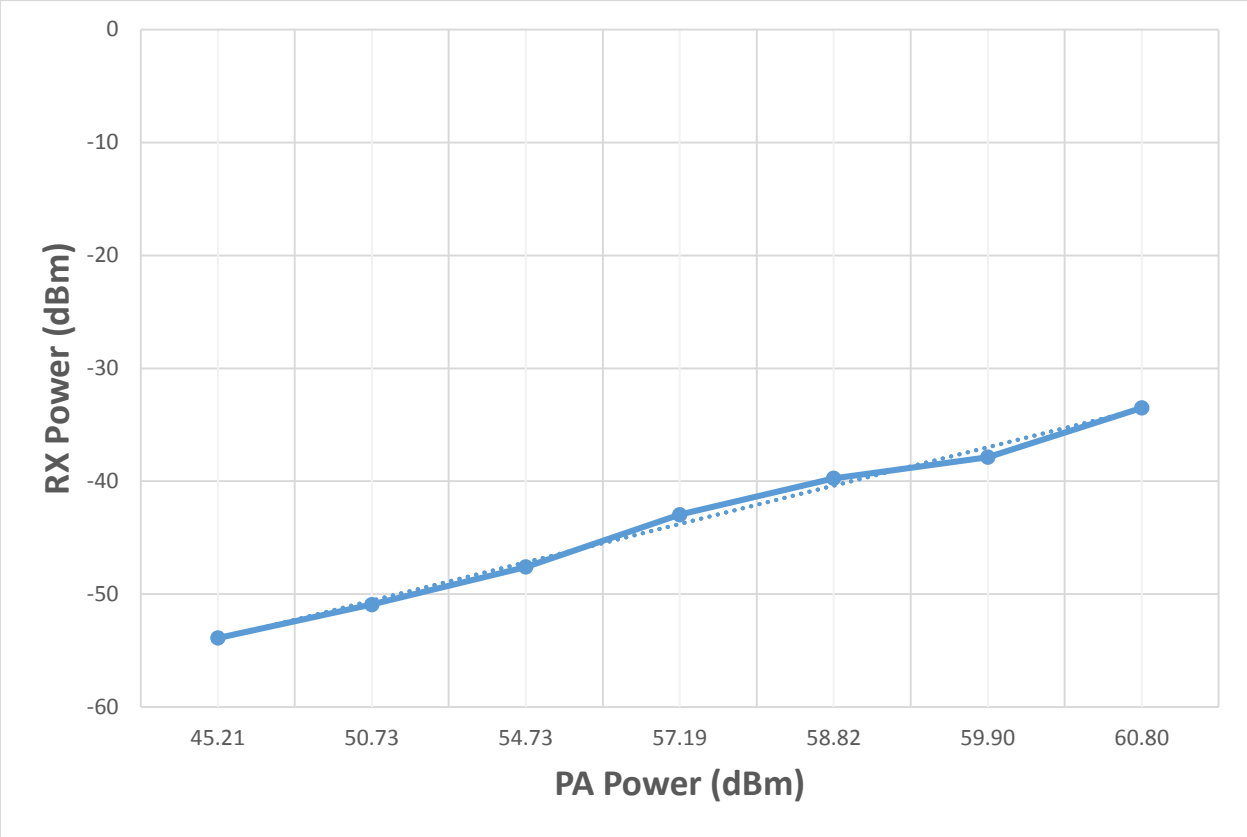

Figure 4.83: Measured feedthrough at RX port during transmission

The amplifier is capable of providing at least 60 dBm of output power. At this power level, the loss in the transmit path is less than 1.2 dB during transmit, while the isolation between PA and RX ports and ANT and RX ports is around 94 dB. These isolation levels are comparable to the small signal measurements presented in Section 4.2.

4.3.2.2 Switching time

The switching characteristics were verified using the test setup shown in Figure 4.30. A signal generator (Direct Digital Synthesizer (DDS)) was used to provide CW signal at 195 MHz at the antenna port. The

output at the receive port was connected to the oscilloscope and peak to peak voltage was measured while the control signal of the switch toggled between logic levels. The PA port was terminated with a 50 ohm termination load. The switching times were very close to those presented in Section 3.5.2.2. The turn on time was 1300 ns and turn off 200 ns.

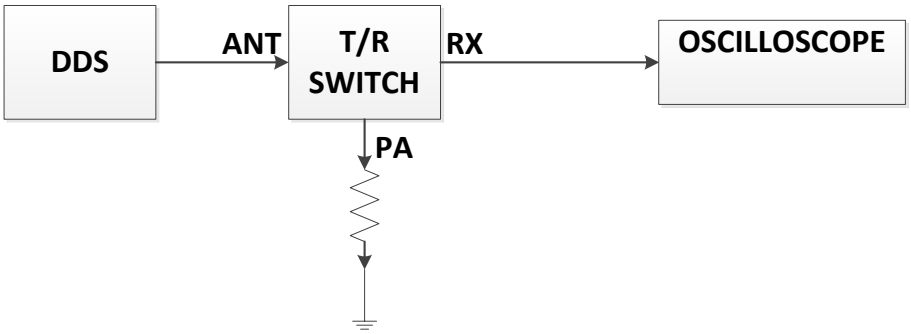

Figure 4.84: Receiver power test setup

4.3.3 Sample Field Results

This system was deployed to Antarctica on an NASA DC-8 aircraft. The six T/R chassis were installed in racks and operated with the rest of the system. The nominal peak output power at the antenna port was 1 kW with a pulse repetition frequency of 12 kHz and bandwidth of 50 MHz. 1 µs pulses were used to map the ice surface and shallow internal layers while 3 and 10 µs were used to sound the bedrock and map deep internal layers.

Figures 4.30 and 4.31 shows a sample echogram and A-scope, respectively, obtained with data collected with a system equipped with the old COTS T/R switch in Antarctica. The noise floor in the A-scope is at approximately -90 dB while the bedrock return appears 40 dB above the noise level. Figure 4.32 and 4.33 shows that from data collected with a radar equipped with the new T/R modules. The A-scope reveals the bed is detected with a signal to noise ratio close to 50 dB.

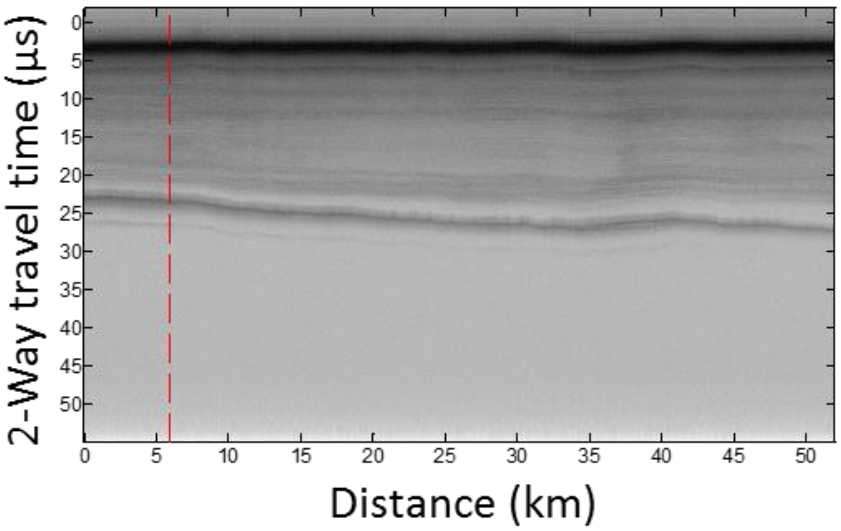

Figure 4.85: Echogram obtained from data collected with a radar equipped with the old T/R switches with bandwidth of 9.5 MHz and total peak power of 1 kW (5 antenna elements). Red line marks the location of A-scope data

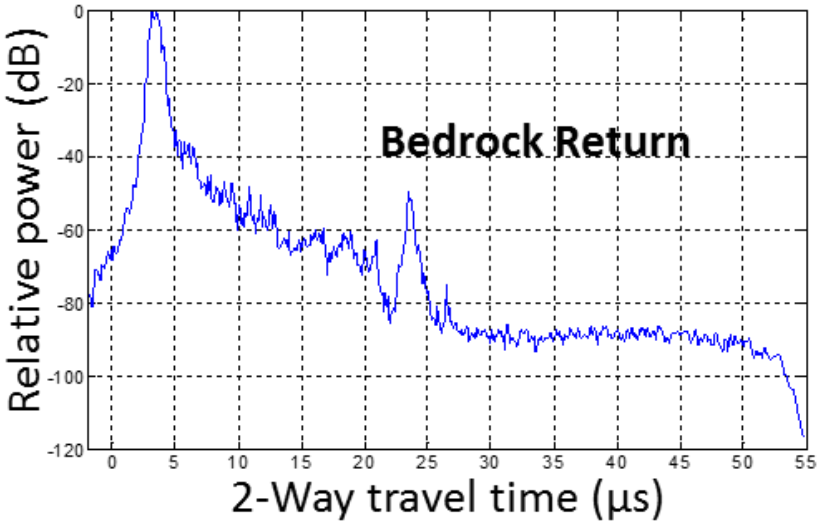

Figure 4.86: A-Scope showing 40 dB signal to noise ratio for the bed return using the old COTS T/R switch.

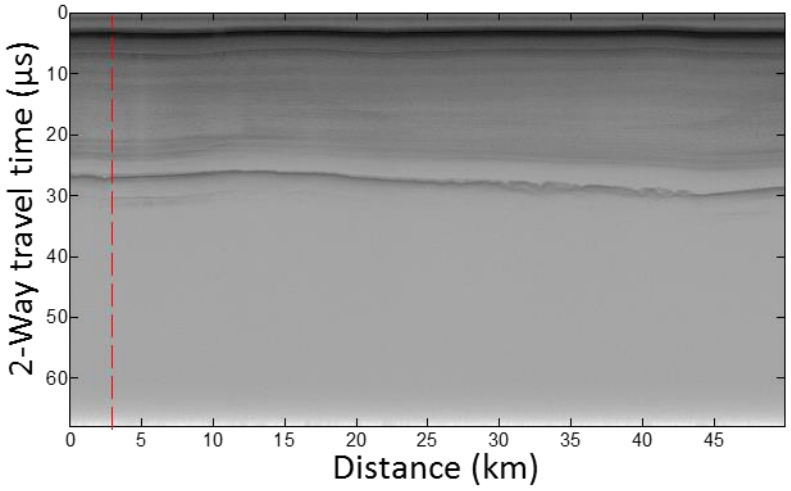

Figure 4.87: Echogram obtained from data collected using a system equipped with the new T/R switch with bandwidth of 50 MHz and total peak power of 6 kW (6 antenna elements). Red line marks the location of A-scope data

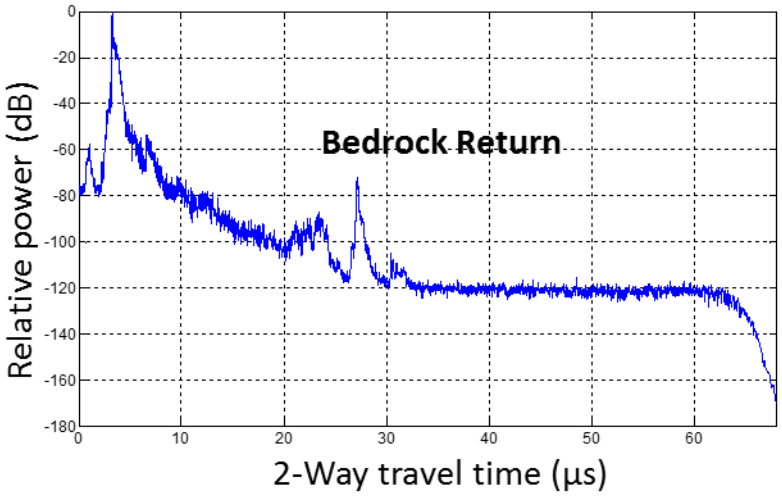

Figure 4.88: A-Scope showing 50 dB signal to noise ratio for the bed return using the system equipped with the new T/R switch.

The bandwidth was increased from 9.5 MHz to 50 MHz which implies a 7.2 dB improvement in signal to noise (SNR) ratio. The number transmitters also increased from 5 to 6 channels which would increase the SNR by 0.8 dB. The power transmitted by each channel also increased from 250 W to 1 kW peak power which increased the SNR by 6 dB. The calculated SNR improvement is approximately 14 dB. The internal layers are also better defined in Figure 4.32.

Another issue solved with the new T/R switch was degradation of surface response due to change in altitude. The old T/R switch had a switching time of 2.4 μs which leads to a blind range of 510 m. The new T/R switch has a switching time of 1.3 μs which leads to a blind range of 345 m.

5 10-40 MHz T/R switch

This chapter discusses the design and implementation of a high power transmit/receive (T/R) switch for frequency range of 10 to 40 MHz. The T/R switch module consists of a high-power amplifier, T/R switch, and the T/R switch driver.

This module was developed for the HF sounder radar [14] which is used in an unmanned aerial system (UAS). The old system operated at 14 MHz or 35 MHz and was capable of transmitting 100 W peak power. Pulse length was set to 1 μs and the PRF varied between 10 to 20 kHz. The maximum average power was 2 W.

The current prototype T/R switch module was designed to fit the footprint of the old module. It's capable of transmitting 1 kW peak power and at least 20 W average power which leads to an increase in the sensitivity. Even though the T/R switch is optimized for frequency range of 10 to 40 MHz, it will be operated at 15 MHz or 35 MHz with bandwidth of 1 MHz to 4 MHz. The entire range was covered so it could be compatible with the previous settings while giving extra flexibility to operate at other frequencies in the same range.

This design is a first functional prototype to demonstrate the concept. Future work will reduce the switching time as well as decrease losses.

5.1 Design Requirements

The primary design requirements for this version of the T/R switch are summarized in the Table 5.1.

Table 0.1: Design requirements for 10 – 40 MHz T/R switch

Frequency	10 – 40 MHz
Peak power	1000 W
Average power	20 W
Insertion loss during transmit	< 2 dB
Isolation during transmit	> 60 dB
Insertion loss during receive	< 2 dB
Isolation during receive	> 20 dB
Switching time between transmit and receive	< 2.3 µs

The T/R switch has to operate between 10 - 40 MHz and handle up to 1000 W of peak power and 20 W of average power for 20 % duty cycle. Switching time between transmit and receive has to be less than 2.3 µs for a 1 µs pulse length in order to keep the blind range less than 500 m.

5.2 Design Overview

The design of the T/R switch is similar to the design described in Section 3.2.1 but is optimized for a frequency range of 10 – 45 MHz. Due to frequency of operation, the quadrature hybrids on the high power and low power sides had to be changed to QH10239 and JSPQ-80, respectively.

All the shunt PIN diodes were changed to series PIN diode MEST2G-150-020-CM26 due to its faster switching time as shown in Section 3.4.5. Series diode, D1, was eliminated since the design provides enough isolation during receive mode. The amplifier is also turned off during receive mode therefore no additional noise is injected to the receiver. Elimination of D1 also made the integration of the module easier.

High pass filter and bias tee were also changed due to frequency of operation. The following section provides more detail about each of the changes as well as the integration of the 1 kW amplifier.

5.2.1 High Power Side Quadrature Hybrid

The QH10239 quadrature hybrid from Werlatone Inc. was chosen for high power side. The quadrature hybrid is capable of operation in the 10-50 MHz range. Table 5.2 lists the relevant parameters, extracted from scattering parameter provided by Werlatone, for a frequency range of 10 to 40 MHz.

Table 0.2: Summary of relevant parameters for the Werlatone QH10239

Frequency	10-40 MHz
Power	20 W continuous
Insertion Loss	0.56 dB maximum
Isolation between ports 2 and 3	29 dB minimum
Isolation between ports 1 and 4	27 dB minimum
Phase imbalance	$90^{\circ} \pm 3^{\circ}$ maximum
Amplitude imbalance	0.615 dB maximum
VSWR	1.06:1 maximum

For 20% duty cycle, the power amplifier provides an average power of up to 20 W. These quadrature hybrids can handle up to 20 W of continuous power. The maximum insertion loss is 0.56 dB with minimum isolation of 29 dB between ports 2 and 3 and 27 dB between ports 1 and 4 across the entire range of interest.

5.2.2 Low Power Side Quadrature Hybrid

The JSPQ-80 quadrature hybrid from Mini-Circuits was chosen for low power side. The quadrature hybrid is capable of operation in the 10-80 MHz range. Table 5.3 lists the relevant parameters for a frequency range of 10 to 40 MHz.

Table 0.3: Summary of relevant parameters for the JSPQ-80

Frequency	10-40 MHz
Power	1 W continuous
Insertion Loss	0.45 dB maximum
Isolation between ports 1 and 2	42 dB minimum
Phase imbalance	$90^{\circ} \pm 1.62^{\circ}$ maximum
Amplitude imbalance	0.17 dB maximum
VSWR	1.32:1 maximum

The quadrature hybrid on the low power side is only active during receive mode, and hence, only need to handle the low powered antenna signal. These quadrature hybrids can handle up to 1 W of continuous power. The maximum insertion loss is 0.45 dB with minimum isolation of 42 dB between the two output ports across the entire range of interest.

5.2.3 High Pass Filter

A high pass filter, shown in Figure 5.1, was designed to suppress switching transients at the receiver port. The design goals for the filter were a 3 dB point of 9.5 MHz and an insertion loss of less than 0.7 dB at 15 MHz. The out of band attenuation had to be at least 20 dB at 7 MHz. The circuit was designed using Keysight Genesys and measured using a vector network analyzer (VNA). The simulated response of the filter is shown in Figure 5.2 and the measured in Figure 5.3. The measured response has a 3 dB point at 9.3 MHz and an insertion loss of less than 0.8 dB above 15 MHz. Attenuation at 7 MHz is 22 dB.

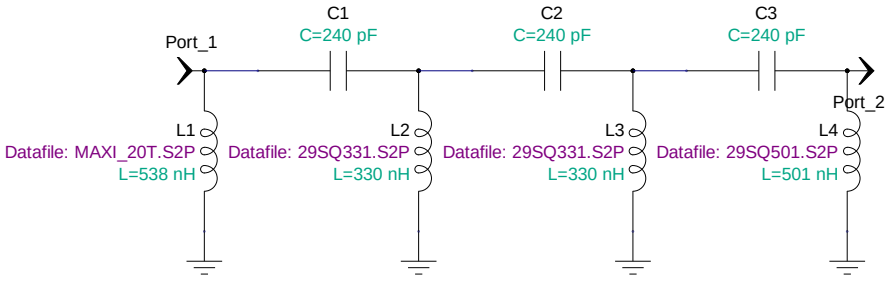

Figure 5.89: Schematic circuit of the High Pass Filter used for low-frequency transient suppression

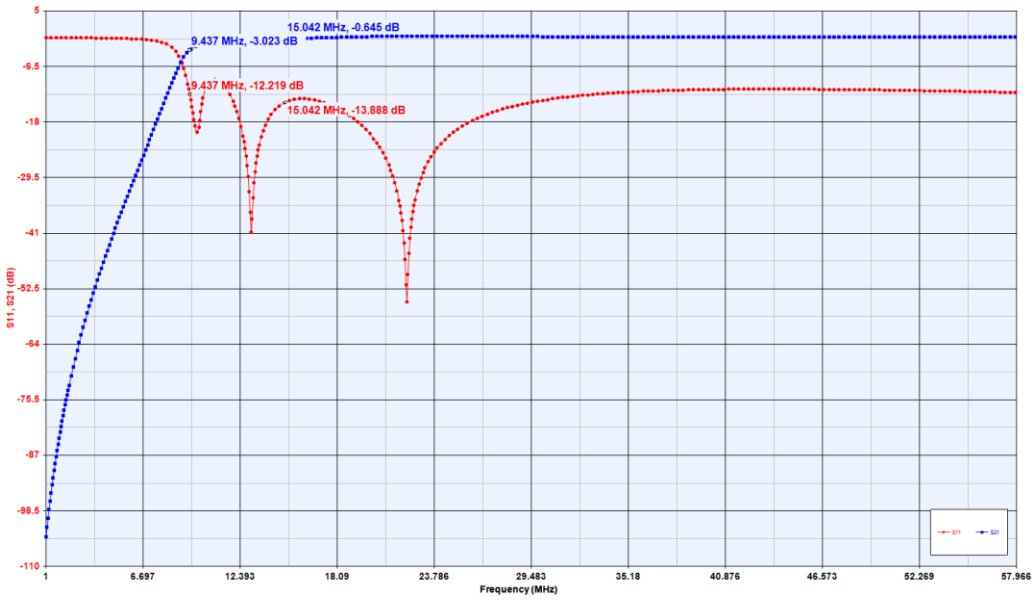

Figure 5.90: Simulated high pass filter response

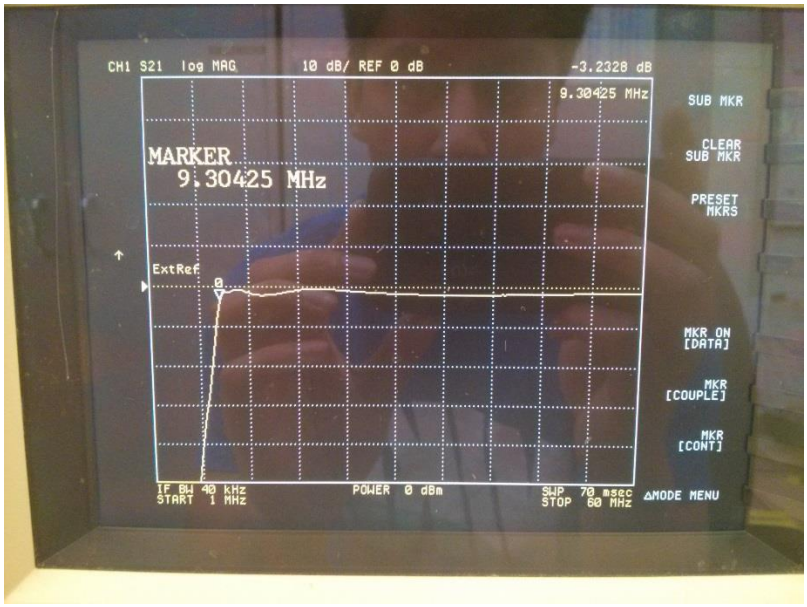

Figure 5.91: Measured high pass filter response

5.2.4 Bias Tee

Each diode is actively biased using a tee circuit composed of DC blocking capacitors and an RF choke. This circuit had to be optimized to obtain a resonant-free response over the wide band of interest.

1000 pF capacitors from American Technical Ceramics (800B series) were used for DC blocking. 1000 pF capacitor has an impedance of 16 Ohms at 15 MHz and 4.54 Ohms at 35 MHz. 390 pF bypass capacitors

were also used to provide low resistance path to ground for the AC component (noise) of bias DC signal from the PIN diode drivers.

A 1.3 µH RF choking inductor from Coilcraft was used to provide around an impedance of around 122 Ohms at 15 MHz and around 285 Ohms at 35 MHz.

Values for RF choke and DC blocks were chosen based on a compromise between T/R switch response and the switching time. High inductor and capacitor values resulted in slower switching time but better response and low inductor and capacitor values resulted in degradation of the response but better switching time.

5.2.5 High Power Amplifier

The high power amplifier was based on a BLF188XR transistor provided by NXP Semiconductors. The amplifier features a built in driver amplifier and is capable of producing 60 dB of gain for the HF band. It also features onboard voltage regulation for adjustment of the gate bias voltage. The power amplifier is capable of providing peak power level in excess of 60 dBm with an input close to 0 dBm.

5.3 Computer Simulations

The same CAD tools used in previous designs, were employed to simulate the performance of this version of the T/R switch.

5.3.1 Low level simulation

The design of the T/R switch was first simulated under semi-ideal conditions using a linear s-parameter simulation, only taking into account the response of the quadrature hybrids. Figure 5.4 shows the simulation setup for the circuit in transmit mode, in which the forward-biased PIN diodes are modeled as a perfect short circuit.

For receive mode, diodes, D2 and D3, are modeled as perfect open circuit, as shown in Figure 5.5. The simulated insertion gain (power amplifier to antenna) in transmit mode, as well as in receive mode (antenna to receiver) are presented in Figure 5.6. Simulated isolation during receive mode is shown in Figure 5.7.

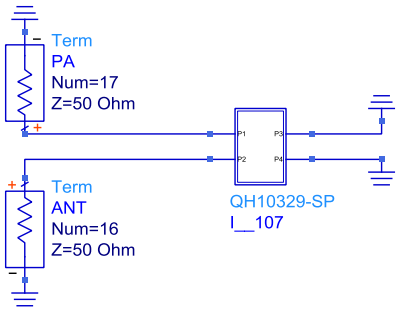

Figure 5.92: Simulation setup representing semi-ideal behavior in transmit state

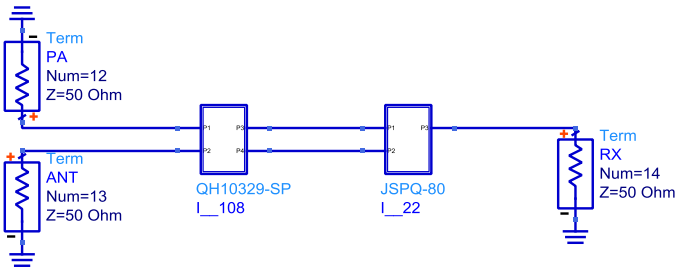

Figure 5.93: Simulation setup representing semi-ideal behavior of the circuit in receive state

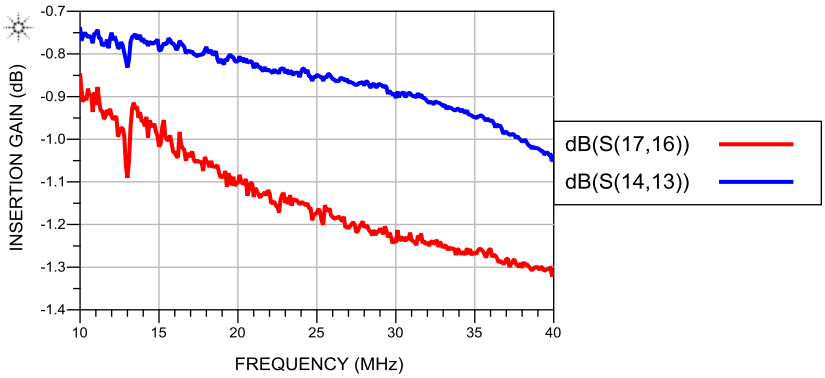

Figure 5.94: Simulated response for the insertion gain during: (a) Transmit between PA and ANT ports (S(17,16)); (b) Receive between ANT and RX ports (S(13,14))

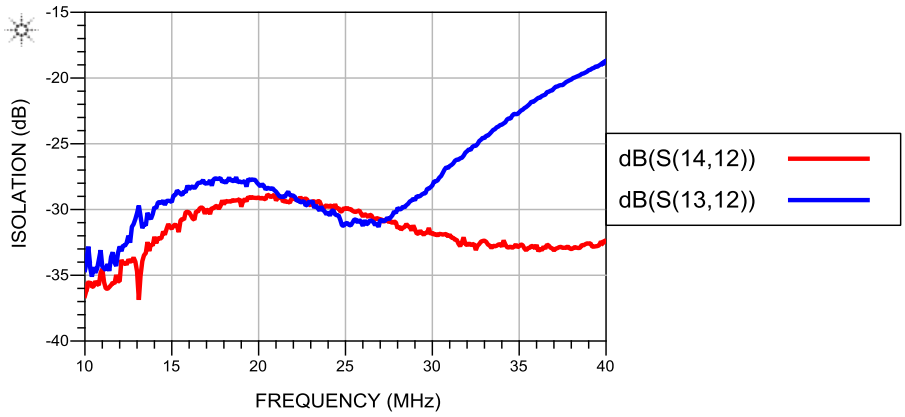

Figure 5.95: Simulated isolation in receive mode between: (a) PA and ANT ports(S(13,12)); (b) PA and RX ports (S(14,12))

Maximum simulated insertion gain caused by ideal circuits is 1.05 dB at 40 MHz during transmit and 1.32 dB at 40 MHz during receive. During receive mode, minimum isolation, as predicted by the simulation, is 18 dB between power amplifier (PA) and antenna (ANT) ports and 28 dB between power amplifier and receive (RX) ports. To include the effects of the components, higher level simulations were performed.

5.3.2 High Level Simulations

After verifying the circuit concept with both of the quadrature hybrids, the effects of the remaining components were integrated into the simulated design as shown in Figure 5.8. Scattering parameters for the hybrids and PIN diodes were provided by the manufacturer. ADS had to interpolate the scattering parameters for 15-40 MHz for the PIN diodes since the scattering parameters provided by the manufacturer were not available below 50 MHz. This simulation does not include the effects of interconnects.

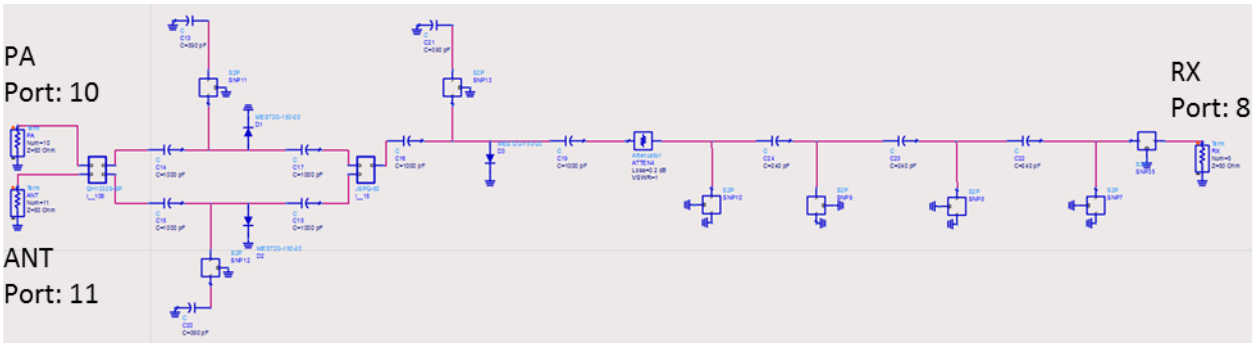

Figure 5.96: ADS simulation setup including first order effects in all the components.

A linear s-parameter simulation was performed using this setup. Figures 5.9 and 5.10 show the insertion gain and isolation during transmit and Figures 5.11 and 5.12 show it during receive.

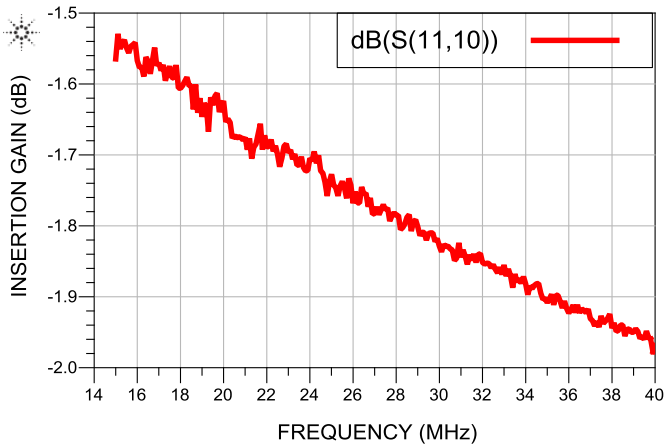

Figure 5.97: Simulated insertion gain between PA and ANT ports (S(11,10) during transmit

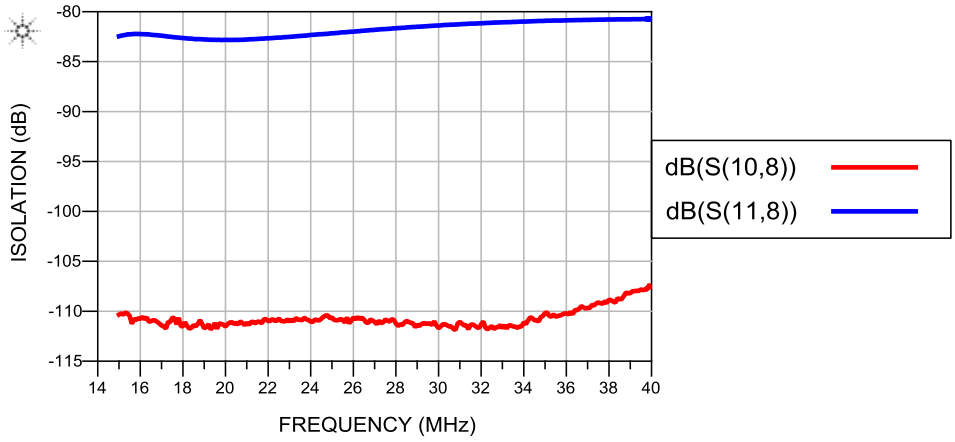

Figure 5.98: Simulated coupling during transmit between: (a) PA and RX ports (S(10,8)); (b) ANT and RX ports (S(11,8))

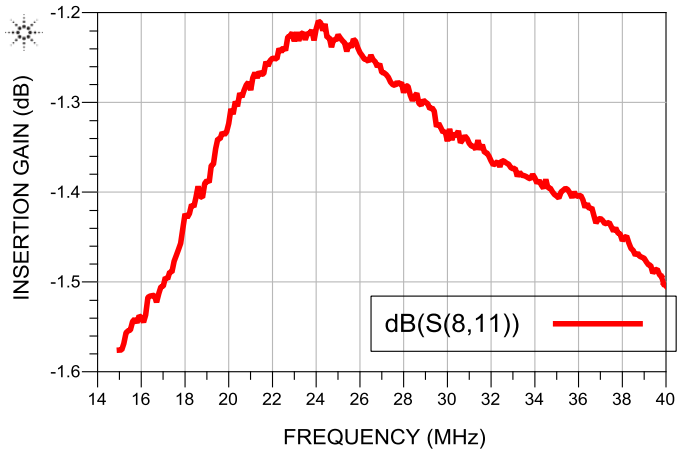

Figure 5.99: Simulated insertion gain between ANT and RX ports (S(8,11)) during receive

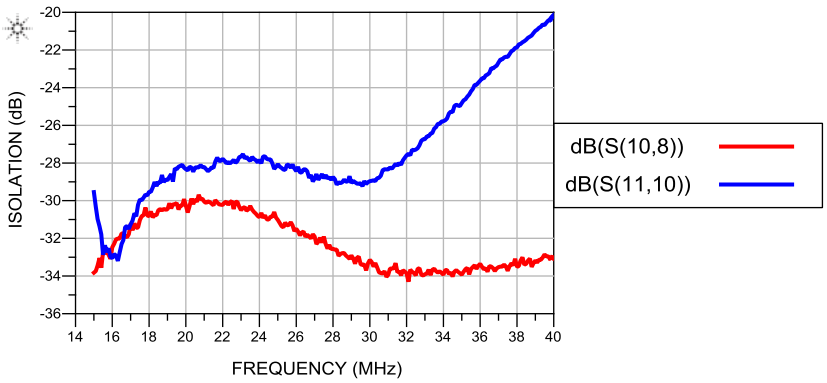

Figure 5.100: Simulated isolation during receive between: (a) PA and ANT ports (S(11,10)); (b) PA and RX ports (S(10,8))

During transmit, there is low loss between PA and ANT ports and high isolation between PA and ANT ports and PA and RX ports. Maximum simulated insertion loss during transmit is 1.978 dB at 40 MHz. The Minimum isolation between PA and RX ports, as predicted by this simulation, is 107 dB at 40 MHz and between ANT and RX ports is 80 dB at 40 MHz.

During receive mode, there is low loss between ANT and RX ports and high loss between PA and ANT and PA and RX ports. Maximum simulated insertion loss during receive is 1.576dB at 15 MHz. Minimum isolation between PA and RX ports, as predicted by this simulation, is 30 dB at 20 MHz and 20 dB at 40 MHz between PA and ANT.

5.3.3 EM simulations

To provide a more accurate simulation of the circuit, all the PCB effects were modeled using a EM simulation in Momentum. The EM simulation results are then included in a EM/circuit co-simulation that includes both PCB layout effects as well as the linear circuit behavior.

5.3.3.1 Board Design

The board was designed on a 1 oz. FR4 board as described in Section 3.2.2.3.1. The line width and gap of the CPWG were calculated to be 119 mils and 15 mils, respectively. The board layout is shown in Figure 5.13. The design only consists of components after the high power quadrature hybrid, QH10239.

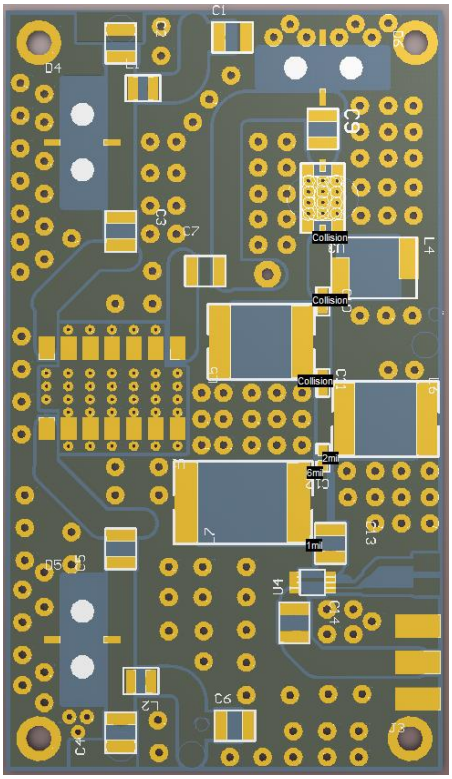

Figure 5.101: T/R switch PCB layout in Altium Designer

5.3.3.2 Circuit/EM Simulation

The board was imported into ADS to perform electromagnetic simulations. Figure 5.14 shows the simulated design in ADS.

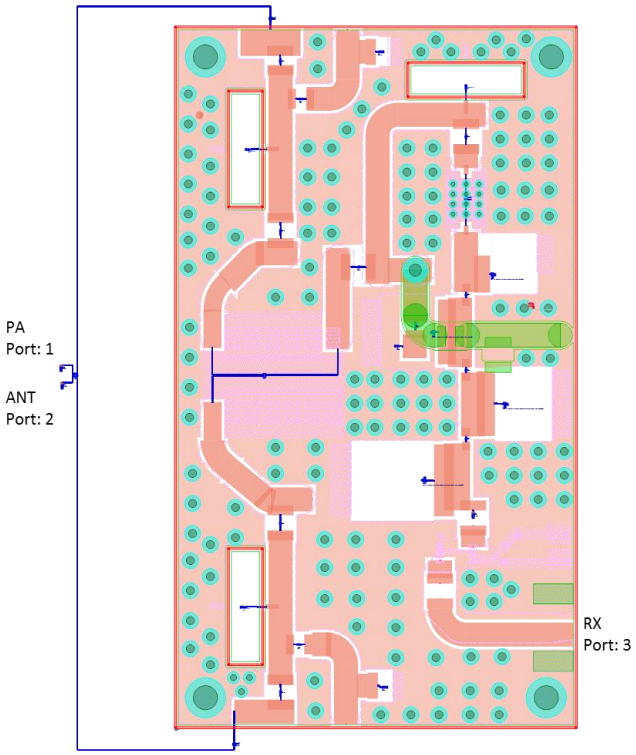

Figure 5.102: Circuit/EM co-simulation setup in ADS

During transmit mode, there is low loss between the PA and ANT ports, as shown in Figure 5.15, and high loss between PA and RX ports and ANT and RX ports, as shown in Figure 5.16.

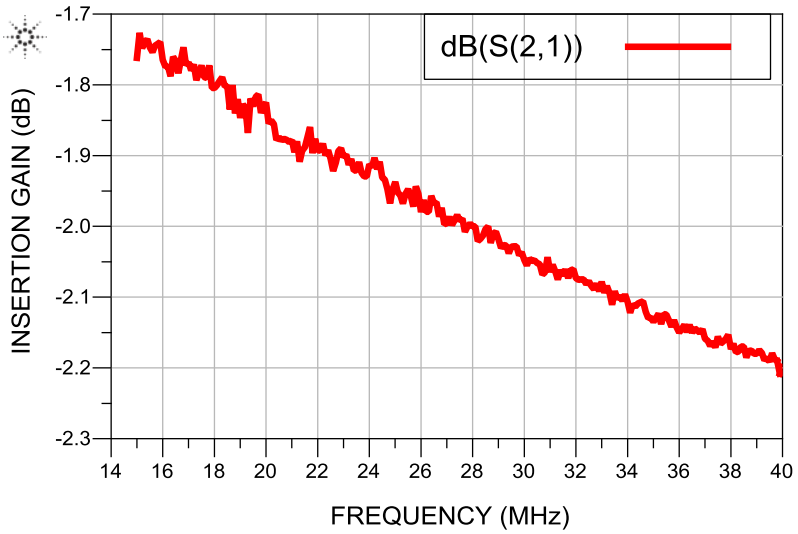

Figure 5.103: Simulated insertion gain between PA and ANT ports during transmit

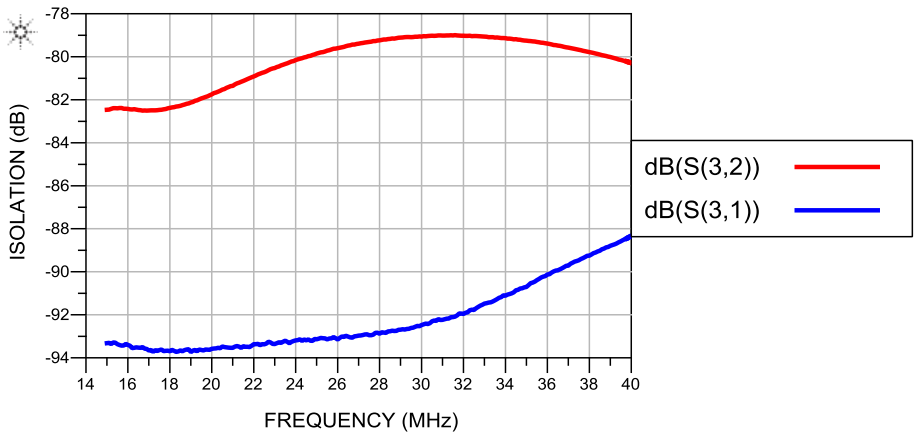

Figure 5.104: Simulated isolation between (a) ANT and RX (S(3,2)); (b) PA and RX (S(3,1))

The maximum simulated insertion loss is 2.2 dB at 40 MHz. Minimum simulated isolation between PA and RX ports is 88 dB at 40 MHz and between ANT and RX ports is 79 dB at 31 MHz.

During receive mode, there is low loss between ANT and RX ports, as shown in Figure 5.17, and high loss between PA and ANT and PA and RX ports, as shown in Figure 5.18.

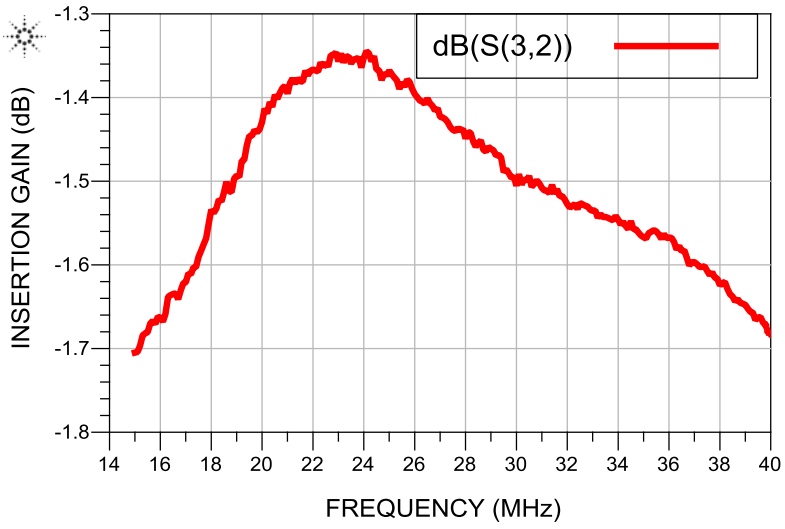

Figure 5.105: Simulated insertion gain between ANT and RX ports during receive

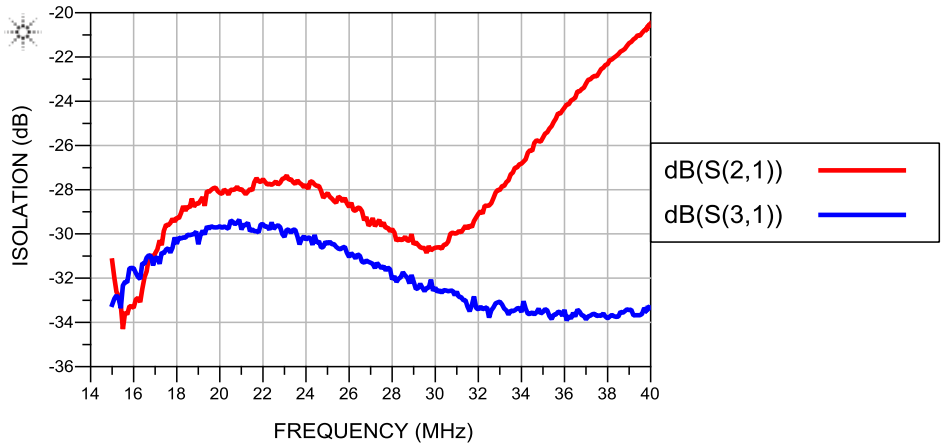

Figure 5.106: Simulated isolation between (a) PA and ANT ports (S(2,1); (b) PA and RX ports(S(3,1)) during receive

Maximum simulated insertion loss is 1.70 dB at 15 MHz. Minimum simulated isolation between PA and RX port is 30 dB at 21 MHz and between PA and ANT ports is 21 dB at 40 MHz.

Figure 5.19 shows the insertion loss difference between low level, high level, and EM/circuit co-simulation during transmit and Figure 5.20 shows it during receive. Losses added by simulated transmission lines increases the insertion loss between high level simulation and EM/circuit co-simulation by 0.24 dB at 40 MHz during transmit and 0.161 dB at 29 MHz during receive.

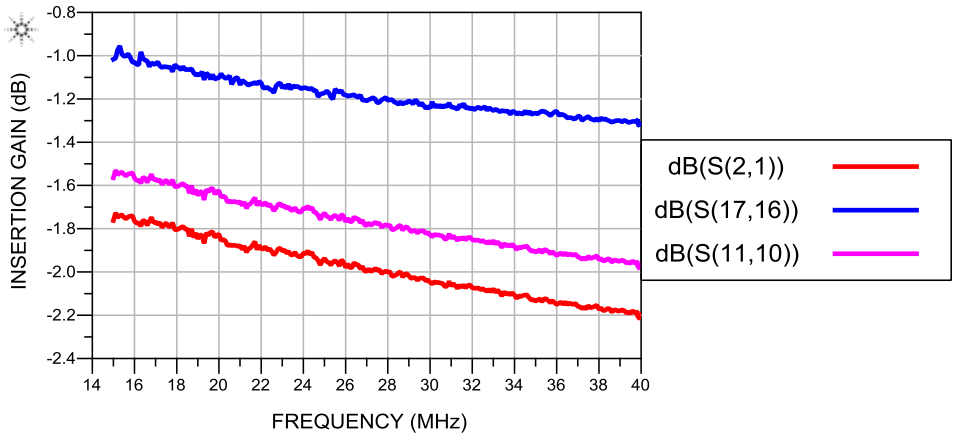

Figure 5.107: Simulated insertion loss between PA and ANT during transmit (a) Ideal (S(17,16)); (b) High level (S(11,10)); (c) EM/Circuit Co-simulation (S(2,1))

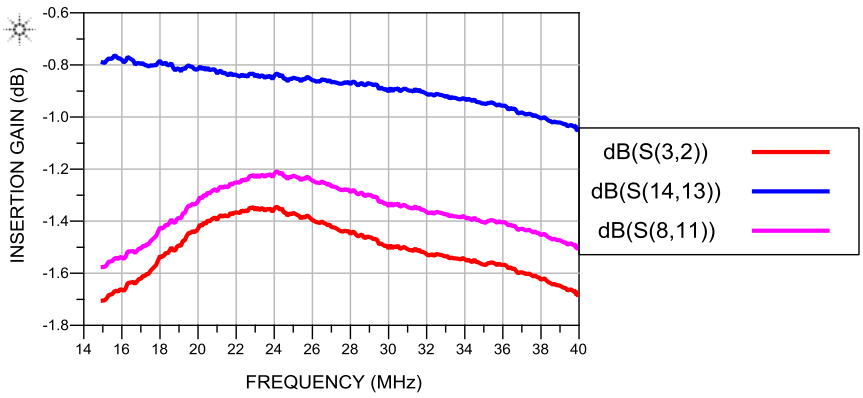

Figure 5.108: Simulated insertion loss between ANT and RX during receive (a) Ideal (S(14,13)); (b) High level (S(8,11)); (c) EM/Circuit Co-simulation (S(3,2))

5.4 Small signal measurements

A 4-port Vector Network Analyzer was used to measure the scattering parameters of the transmit/receive switch. PIN Diodes were connected to a power supply and biased with 100 mA of forward bias current during transmit and 0 V reverse bias voltage during receive. Due to an error during milling process, the receiver switch had to be bypassed during the testing.

Figure 5.21 shows the insertion loss of the device along with low level, high level, and EM/circuit co-simulation results during transmit and Figure 5.23 shows it during receive. Figure 5.22 and 5.24 show the isolation during transmit and receive of the actual device.

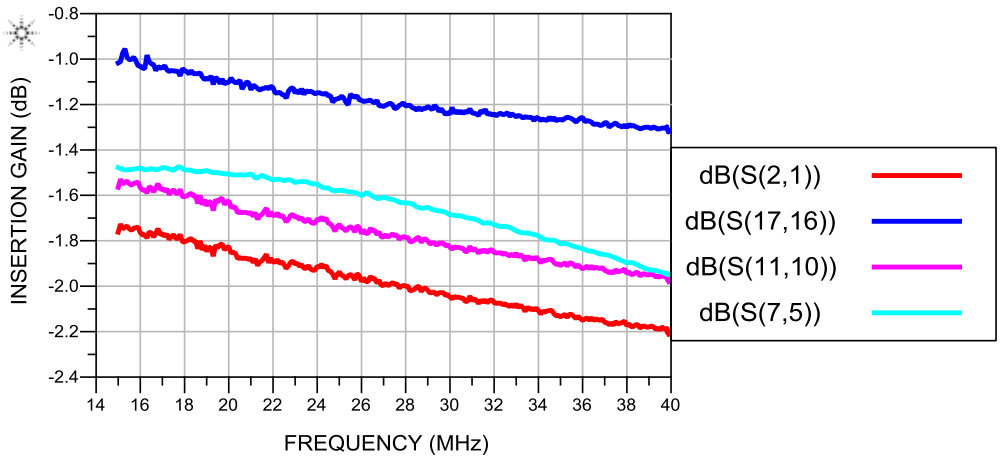

Figure 5.109: Simulated vs measured insertion loss between PA and ANT ports during transmit (a) Ideal (S(17,16)); (b) High level (S(11,10)); (c) EM/Circuit Co-simulation (S(2,1)); (d) Actual (S(7,5))

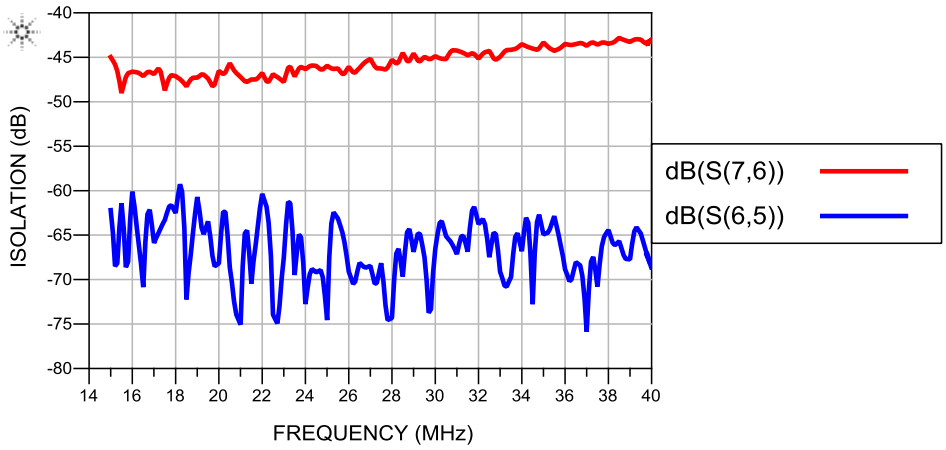

Figure 5.110: Measured isolation during transmit between (a) PA and RX ports (S(7,6)); (b) ANT and RX ports (S(6,5))

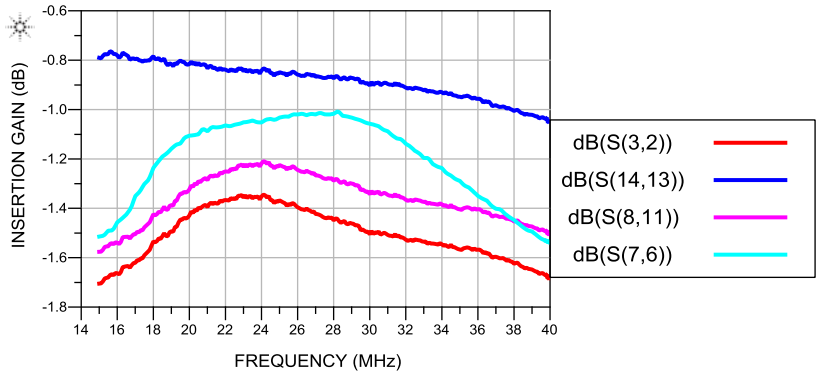

Figure 5.111: Simulated vs measured insertion gain between ANT and RX ports during receive (a) Ideal (S(14,13)); (b) High level (S(8,11)); (c) EM/Circuit Co-simulation (S(3,2)); (d) Actual (S(7.6))

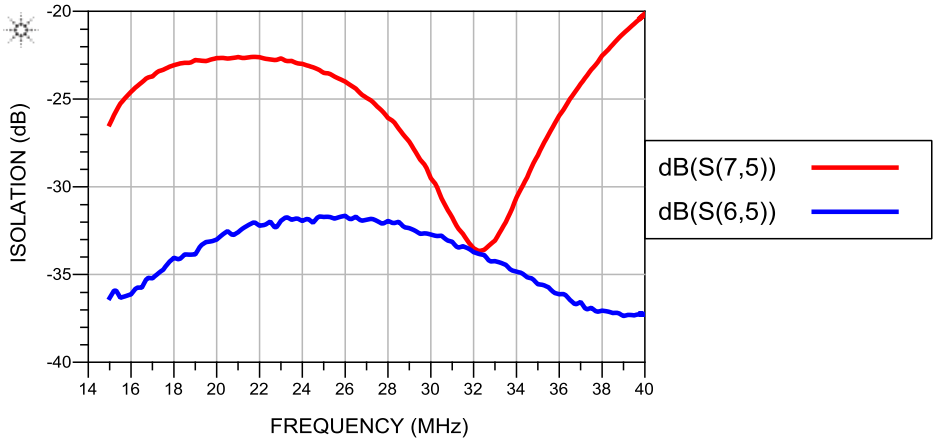

Figure 5.112: Measured isolation during receive between: (a) PA and ANT ports (S(7,5)); (b) PA and RX ports (S(6,5))

During transmit, the maximum measured insertion loss is 1.951 dB at 40 MHz. The measured isolation between PA and RX ports is 60 dB at 18 MHz and between ANT and RX ports is 42 dB at 38 MHz.

Isolation during transmit would increase by at least 40 dB with an addition of the receiver isolation switch.

During receive, the maximum measured insertion loss is 1.539 dB at 40 MHz. The measured isolation between PA and ANT ports is 20 dB at 40 MHz and between ANT and RX ports is 31 dB at 26 MHz.

The maximum variance in insertion loss between EM/Circuit co-simulation simulation and measured response is 0.173 dB during transmit and 0.434 dB during receive. There is greater variance between the simulated and the measured response due to the necessity of interpolation of the PIN diodes scattering parameter for 15 – 40 MHz.

5.5 System integration, Laboratory tests, and field tests

5.5.1 Board and Chassis design

Figure 5.25 shows the final design of the chassis. It consists of 1 kW amplifier, T/R switch, and the T/R switch driver. For the prototype, the driver is placed on top of the low power section of the T/R switch. The final version will have the driver underneath the low power section of the T/R switch. The high power quadrature hybrid is connected with the PIN diodes and the low power section via RF cables.

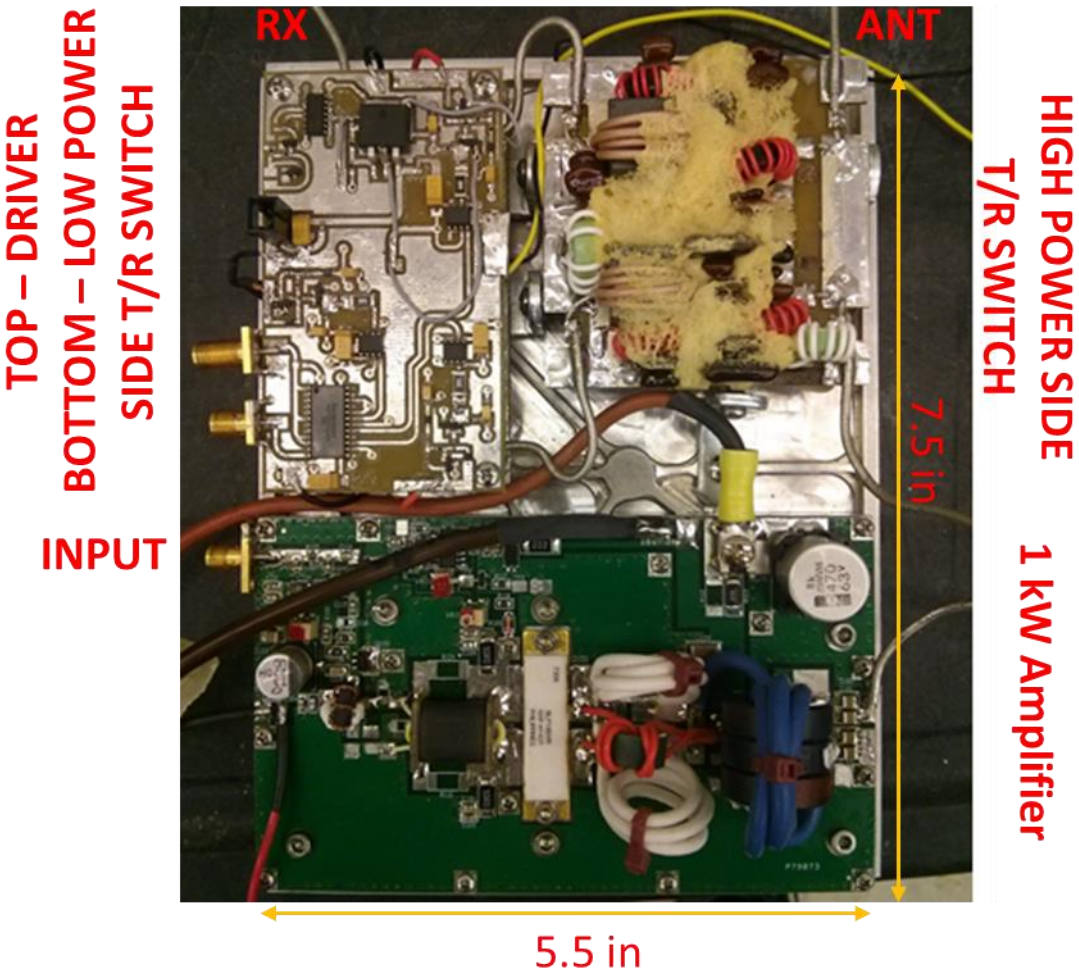

Figure 5.113: Photograph of the T/R switch

5.5.2 Characterization of the Complete Modules

5.5.2.1 Output power vs. input power in Transmit mode

Loss at the antenna port of the T/R switch was measured through the test setup shown in Figure 5.26. The tests were conducted for 15 MHz and 35 MHz. A signal generator (Direct Digital Synthesizer (DDS)) was used to provide a 1 µs pulse with 12% duty cycle at different power levels. The signal was amplified and injected into the PA port of the T/R switch. The output signal at the ANT port was attenuated by 50 dB and fed into the oscilloscope. The video feedthrough signal was directly measured with the oscilloscope.

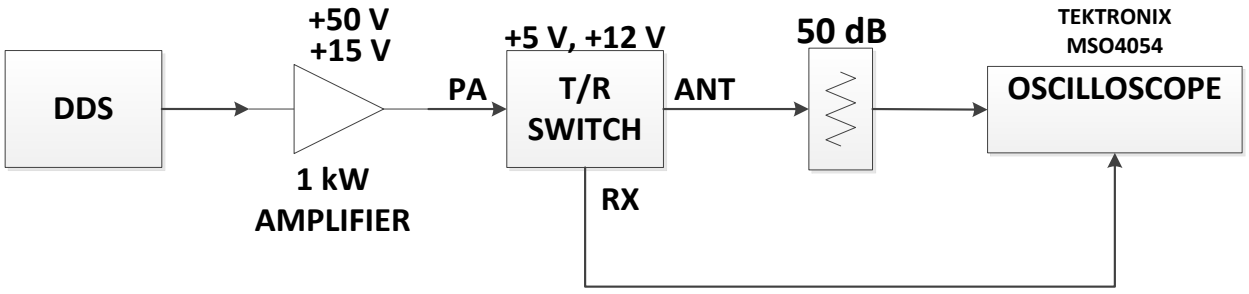

Figure 5.114: Power test setup

Power levels at the output of the DDS and 1 kW amplifier were measured first to calculate gain and the exact power at the PA port for different quiescent currents. The signal generator signal was directly measured with an oscilloscope.

The 1 kW amplifier was characterized for different quiescent currents by adjusting the gate bias voltage. Output power was measured at 15 MHz and 35 MHz. The output was attenuated by 50 dB before being measured by the oscilloscope. Figures 5.27 and 5.28 shows the output power vs input power of the amplifier for different quiescent currents for 15 MHz and 35 MHz, respectively.

At 15 MHz, for quiescent current of 250 mA, a -6.25 dBm signal input signal resulted in 1 kW peak power at the amplifier output. At 35 MHz, for quiescent current of 250 mA, a -4.25 dBm signal input signal resulted in 58 dBm of peak power at the amplifier output.

At these points the amplifier is in saturation (P1dB = 55 dBm for 15 MHz and P1dB = 53 dBm for 35 MHz), but harmonic distortion does not affect radar performance, since the harmonics are filtered out by the output matching network of the power amplifier.

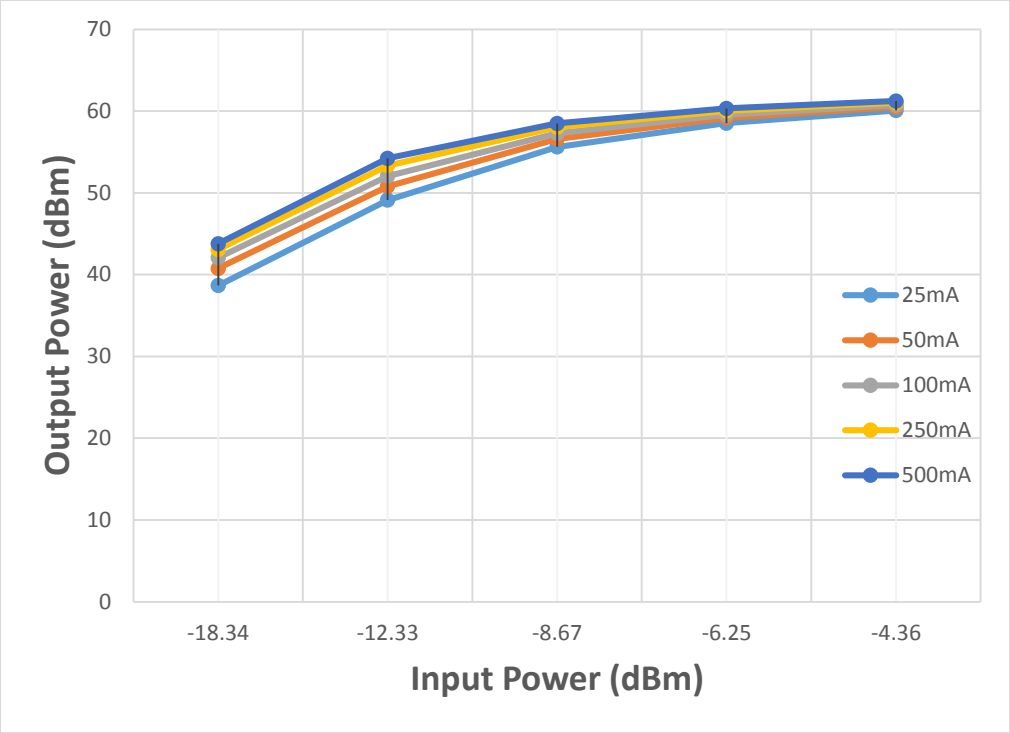

Figure 5.115: Measured power amplifier (PA) output power and gain vs input power at 15 MHz for different quiescent currents

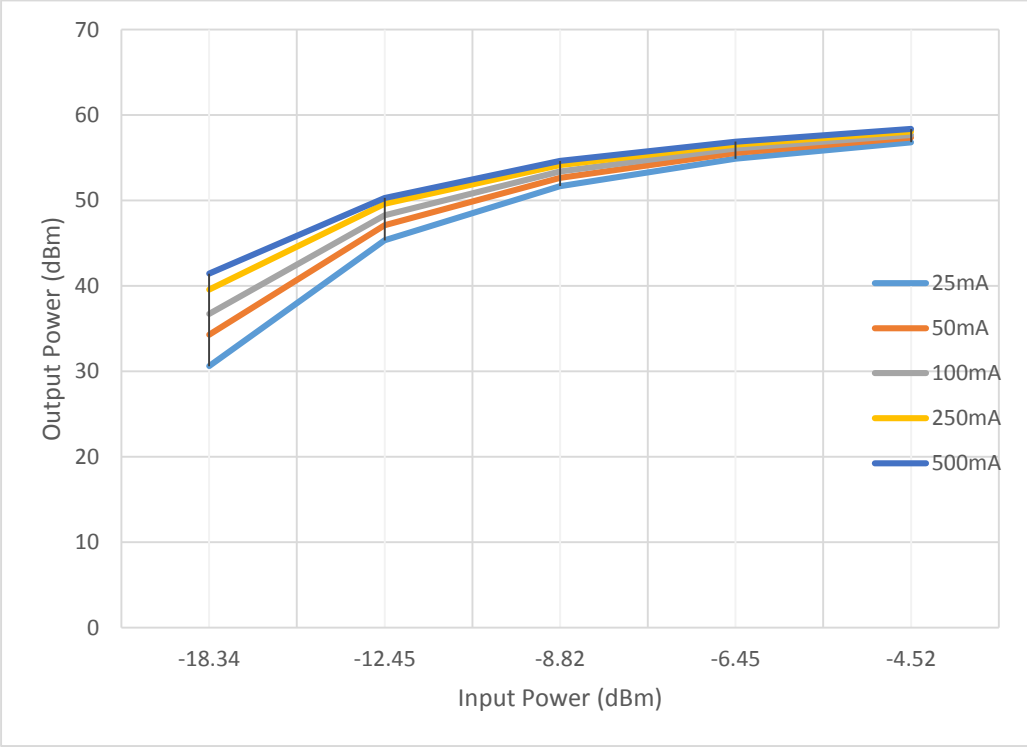

Figure 5.116: Measured power amplifier (PA) output power and gain vs input power at 35 MHz for different quiescent currents

The amplifier was then connected to the T/R switch to measure the loss during transmit as well as the feedthrough signal. Figures 5.29 and 5.30 show the comparison of the input power at the PA port and the output power at the ANT port for 15 MHz and 35 MHz, respectively. Figure 5.31 and 5.32 show the loss during transmission for 15 MHz and 35 MHz. The loss is between 1.76 dB and 2.34 dB (0.58 dB variation) at 15 MHz and between 2.36 dB and 2.39 dB (.03 dB). The low variation indicates that the T/R switch does not introduce gain compression effects.

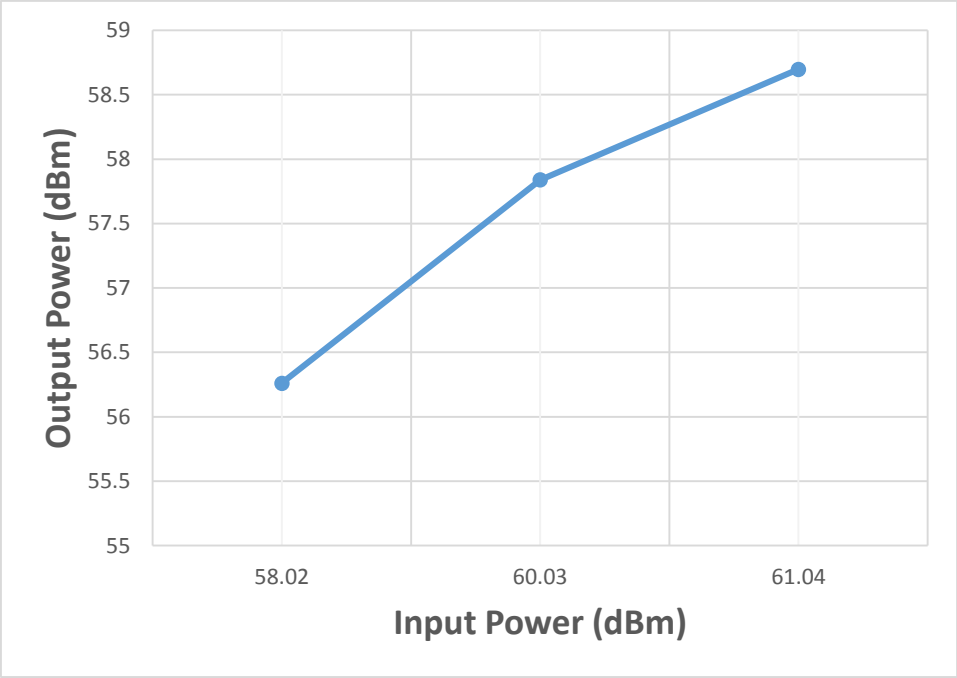

Figure 5.117: Measured Input (PA) power vs output (ANT) power during transmission at 15 MHz

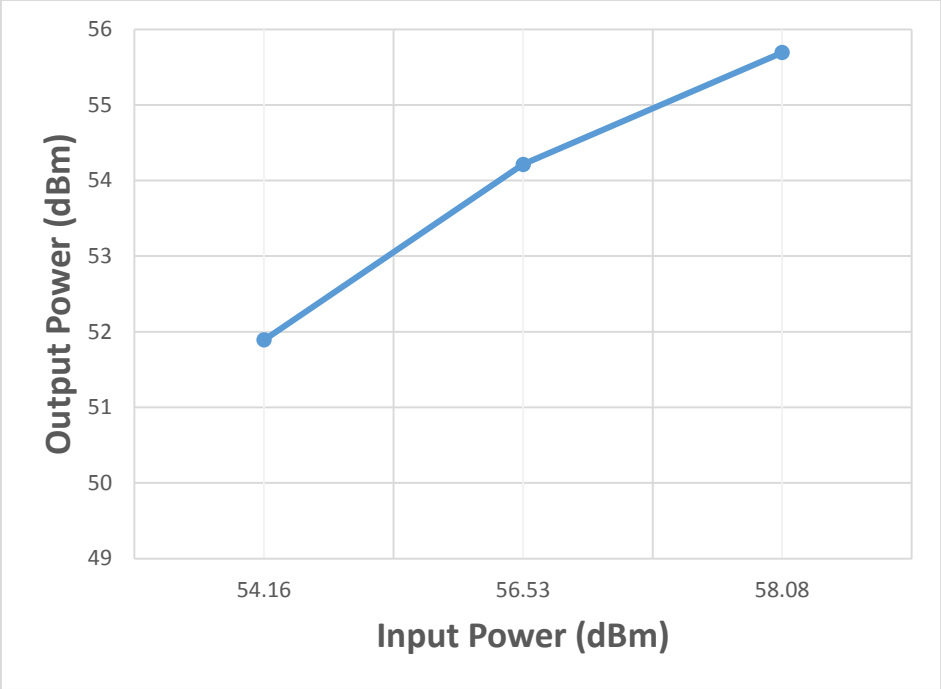

Figure 5.118: Measured Input (PA) power vs output (ANT) power during transmission at 35 MHz

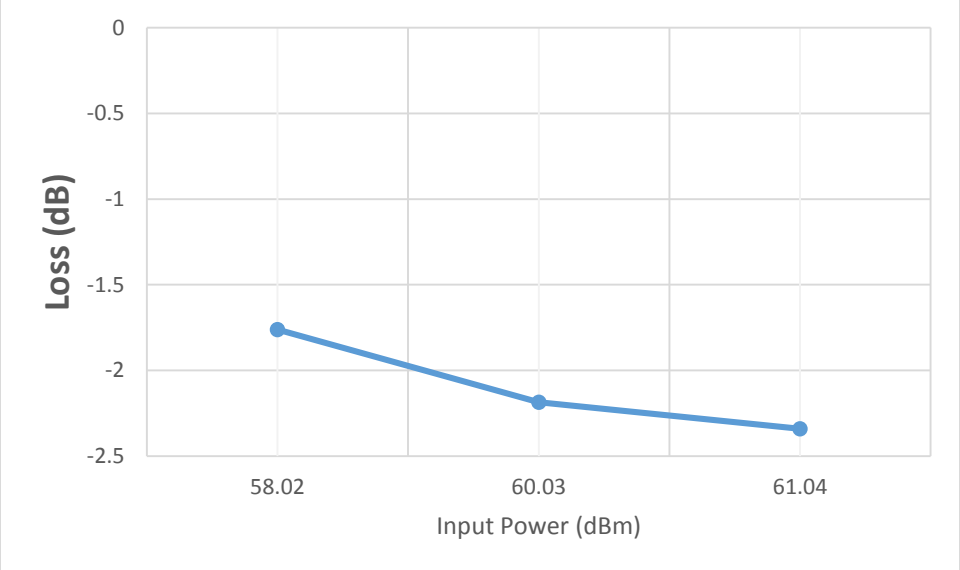

Figure 5.119: Measured Loss between PA and ANT ports of T/R switch during transmission for 15 MHz

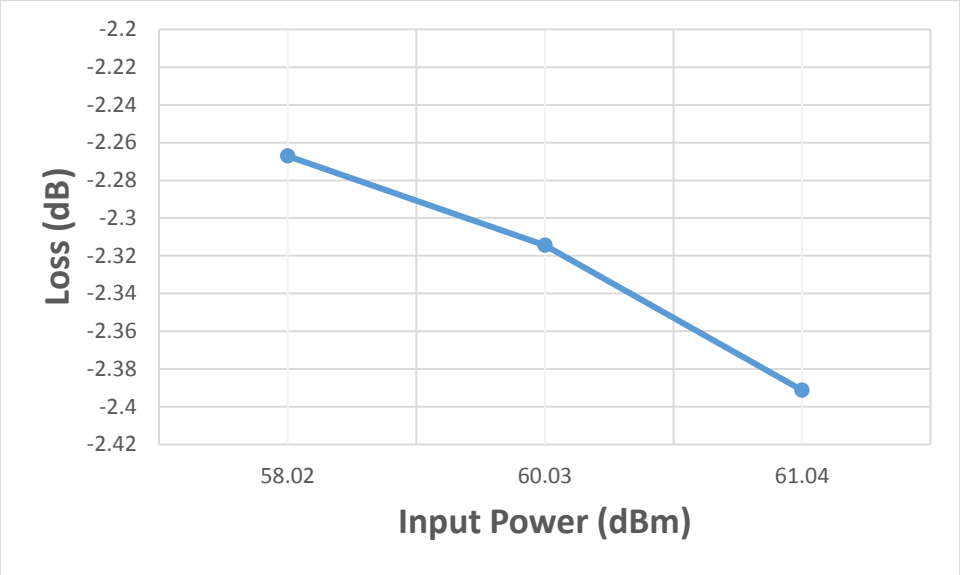

Figure 5.120: Measured Loss between PA and ANT ports of T/R switch during transmission for 35 MHz

Figure 5.33 and 5.34 show the feedthrough signal at the RX port during transmission for 15 MHz and 35 MHz, respectively. The power level at the Rx port changes almost linearly as the transmit power changes, which indicates that the isolation is independent of RF drive level.

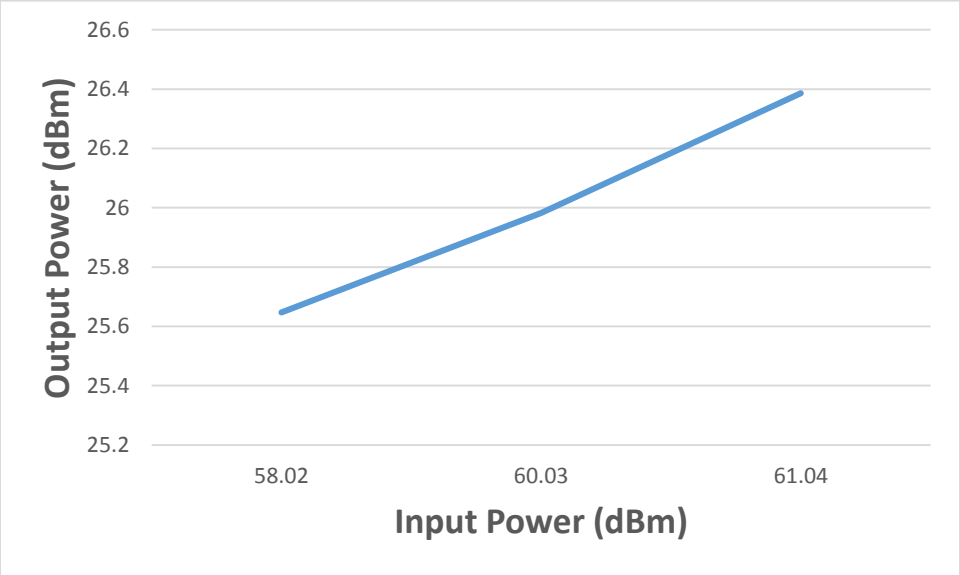

Figure 5.121: Measured feedthrough at RX port during transmission at 15 MHz

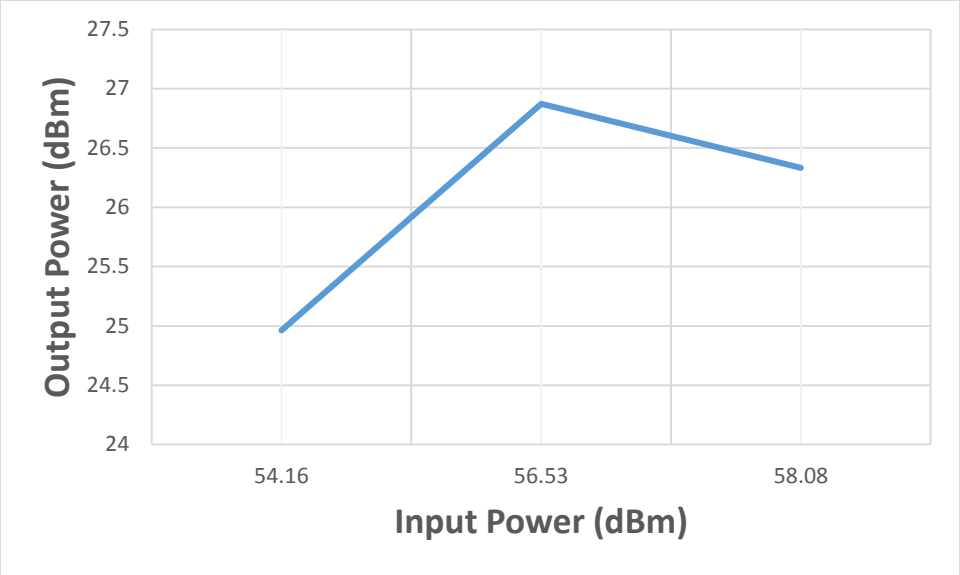

Figure 5.122: Measured feedthrough at RX port during transmission at 35 MHz

The amplifier is capable of providing at least 60 dBm of output power. At this power level, the loss in the transmit path is less than 2.3 dB for 15 MHz and 35 MHz. These measurements are comparable to the small signal measurements presented in Section 5.4.

5.5.5.2 Switching time

The switching characteristics were verified using the test setup shown in Figure 5.35. A signal generator (Direct Digital Synthesizer (DDS)) was used to provide CW signal at 15 MHz and 35 MHz at the antenna port. The output at the receive port was connected to the oscilloscope and peak to peak voltage was measured while the control signal of the switch was toggled between logic levels. The PA port was

terminated with a 50 ohm termination load. Turn off time was found to be 1.35 µs and the turn on time was 1.5 µs as shown in Figure 5.36.

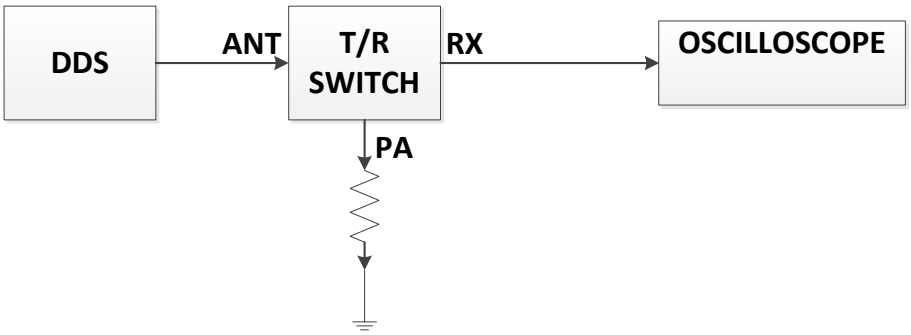

Figure 5.123: Receiver power test setup

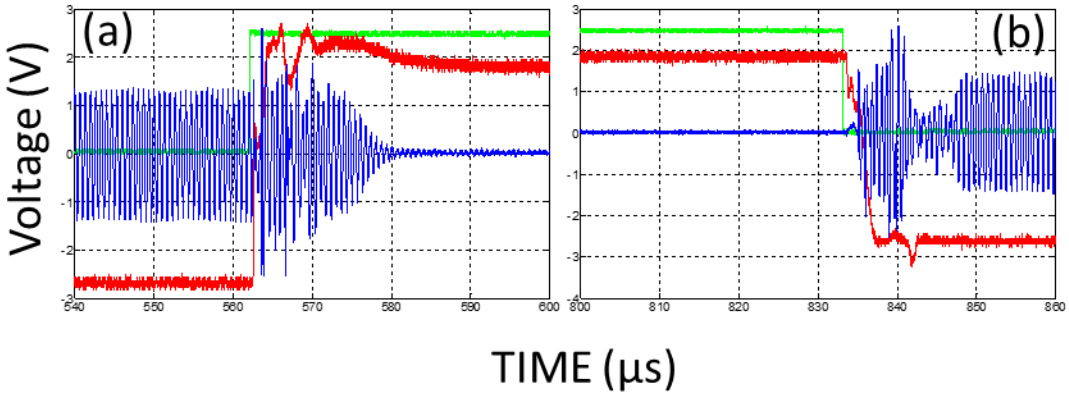

Figure 5.124: Measured switching time: (a) Turn off time measured from 50% TTL (Green) signal to 10% RF (Blue) signal; (b) Turn on time measured from 50% TTL (Green) signal to 90% RF (Blue); Also shown is the series diode response (Red)

6 160-230 MHz Miniaturized T/R switch

This chapter discusses the design and implementation of a miniaturized high power transmit/receive (T/R) switch for a frequency range of 160 to 230 MHz. The goal of this design is to explore miniaturization of the T/R switch and its driver while maintaining the design requirements mentioned in Section 3.1.

6.1 Design Overview

The same design used in Section 3.2.1 was used for the miniaturized 160 -230 MHz T/R switch except for changes in quadrature hybrids, PIN diodes, and the isolation switch. The quadrature hybrids were changed to QH9304 due to its smaller size and the frequency of operation. All the shunt PIN diodes were changed to series PIN diode MEST2G-150-020-CM26 due to its faster switching time as shown in Section 3.4.5. Finally the receiver switch was changed to PE4245 to reduce some of the driver circuitry and due to faster switching time.

6.1.1 Quadrature Hybrids

Two QH9304 quadrature hybrids from Werlatone Inc. were used for this design. The quadrature hybrids are capable of operation in the 60-1000 MHz range. Table 6.1 lists the relevant parameters of this quadrature hybrids for the frequency range of 160 – 230 MHz.

Table 6.4: Summary of relevant parameters for the Werlatone QH8849

Frequency	160 – 230 MHz
Power	150 W continuous
Insertion Loss	1 dB maximum
Isolation	18 dB minimum
Phase imbalance	$90^{\circ} \pm 1.19^{\circ}$ maximum
Amplitude imbalance	± 0.568 dB maximum
VSWR	1.19:1 maximum

For 15% duty cycle, the power amplifier provides an average power of up to 150 W. These quadrature hybrids can handle up to 150 W of continuous power over the operating frequency range of 60 to 1000 MHz. Maximum insertion loss for a single hybrid coupler is 1 dB and minimum isolation is 18 dB between all ports. Even though the insertion loss is greater by 0.55 dB (1 dB vs 0.45 dB) in comparison to old quadrature hybrid, QH8100, the area of the device is smaller by 150%.

6.1.2 Receiver switch

To reduce the driver size as well as increase the switching speed, PE4245, a single pole double throw switch, was used to provide extra isolation between the receiver and amplifier ports. It had less than 0.75 dB of insertion loss below 1000 MHz. Isolation between input and the two outputs was less than 42 dB below 1000 MHz. Isolation between the two outputs was less than 36 dB below 1000 MHz. Switch on time was less than 200 ns measured at 2 GHz and switch off time was less than 90 ns for 2 GHz. This chip has better performance than the ADG901 used in the designs presented in Section 3.2.1.5.

6.2 Computer Simulations

The same CAD tools used in previous designs, were employed to simulate the performance of this version of the T/R switch.

6.2.1 Low level simulation

Figure 6.1 shows the simulation setup for the circuit in transmit mode, in which the forward-biased PIN diodes are modeled as a perfect short circuit. For receive mode, diodes, D2 and D3, are modeled as perfect open circuit, as shown in Figure 6.2. The simulated insertion gain (power amplifier to antenna) in transmit mode, as well as in receive mode (antenna to receiver) are presented in Figure 6.3. Isolation during receive mode is shown in Figure 6.4.

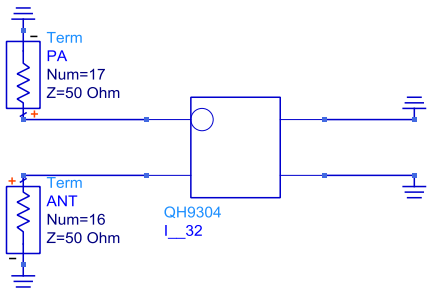

Figure 6.125: Simulation setup representing semi-ideal behavior in transmit state

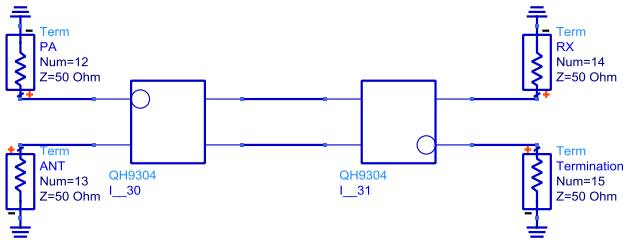

Figure 6.126: Simulation setup representing semi-ideal behavior of the circuit in receive state

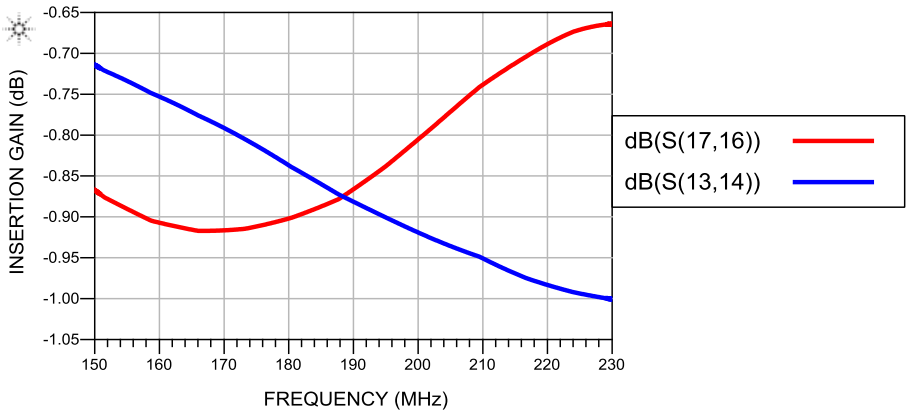

Figure 6.127: Simulated response for the insertion gain during (a) Transmit between PA and ANT ports (S(17,16)); (b) Receive between ANT and RX ports (S(13,14))

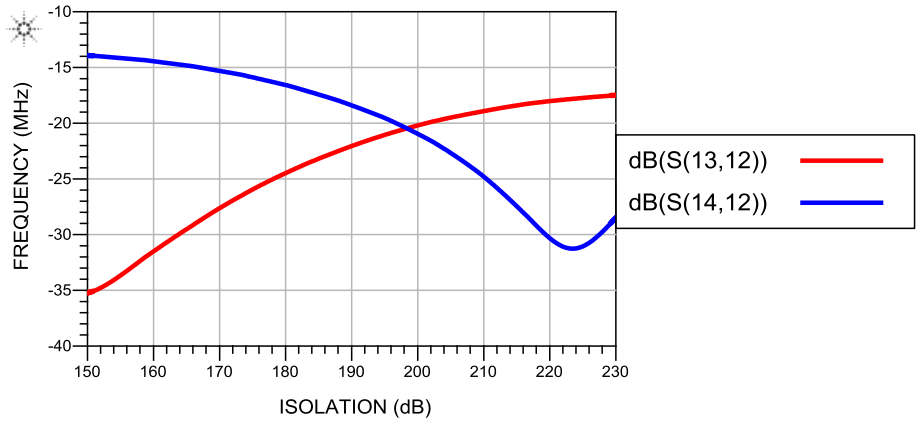

Figure 6.128: Simulated isolation in receive mode between: (a) PA and ANT ports (S(13,12)); (b) PA and RX ports (S(14,12))

During transmit, the maximum insertion loss caused by the ideal circuit is 0.917 dB at 166 MHz. In receive mode, maximum insertion loss is 1.001 dB at 230 MHz and isolation is greater than 17 dB between PA and ANT and 14 dB between PA and RX. These simulations give the upper bound for the

losses across this frequency range. To model the circuit more accurately, higher level simulations were performed. These include the effect of the rest of the components used in the design.

6.2.2 High Level Simulations

After verifying the circuit concept using the simulation outlined in the previous subsection, the effects of the remaining components were integrated into the simulated design as shown in Figure 6.5. Scattering parameters for the hybrids, PIN diodes, and inductors were provided by the manufacturer. This particular simulation does not include the effects of interconnects yet.

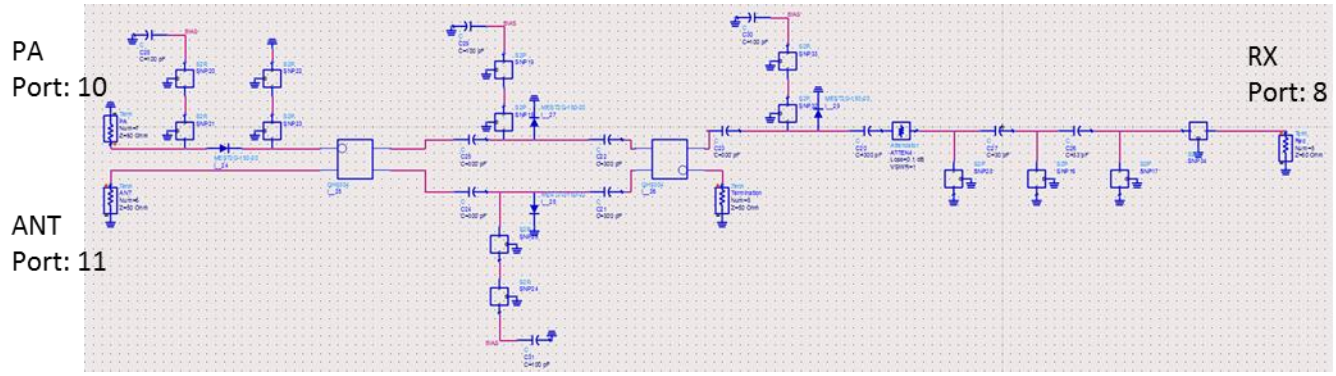

Figure 6.129: ADS simulation setup including first order effects in all the components.

Figures 6.6 and 6.7 show the insertion gain and isolation during transmit and Figures 6.7 and 6.8 show it during receive.

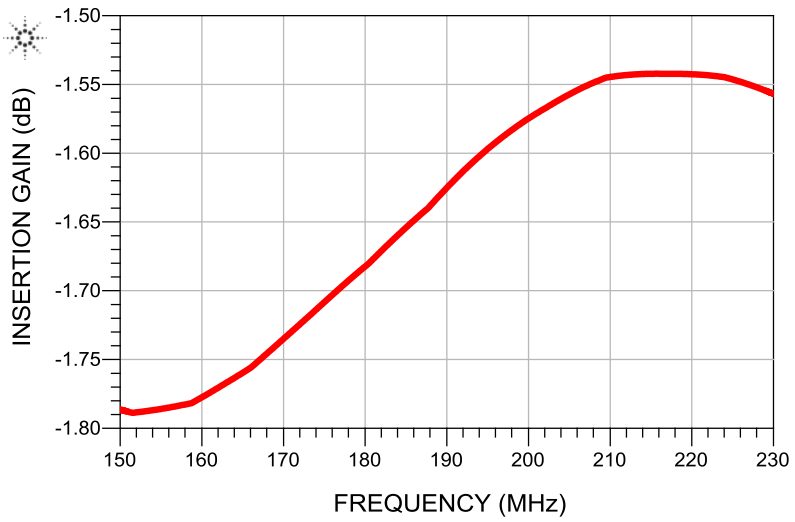

Figure 6.130: Simulated insertion gain between PA and ANT ports during transmit

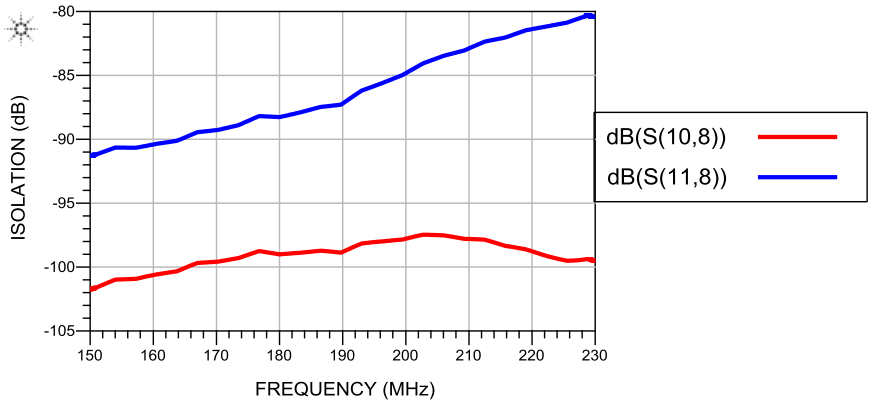

Figure 6.131: Simulated coupling during transmit between: (a) PA and RX ports (S(10,8)); (b) ANT and RX ports (S(11,8))

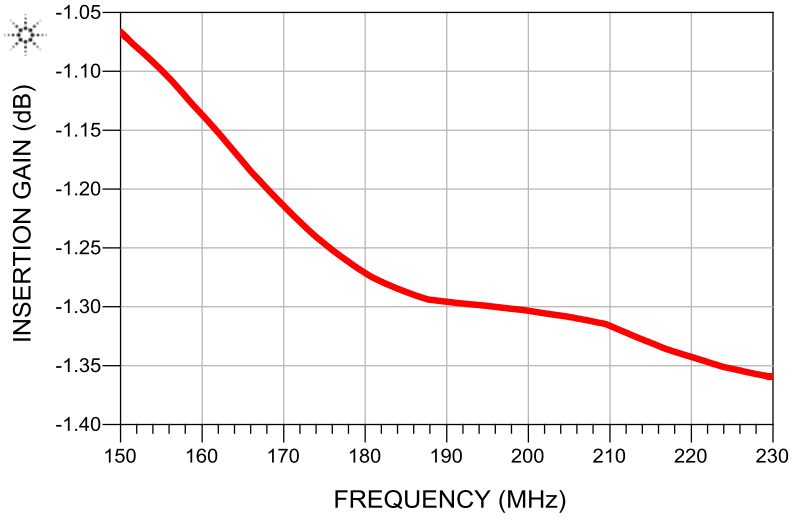

Figure 6.132: High level simulated insertion gain between ANT and RX ports during receive

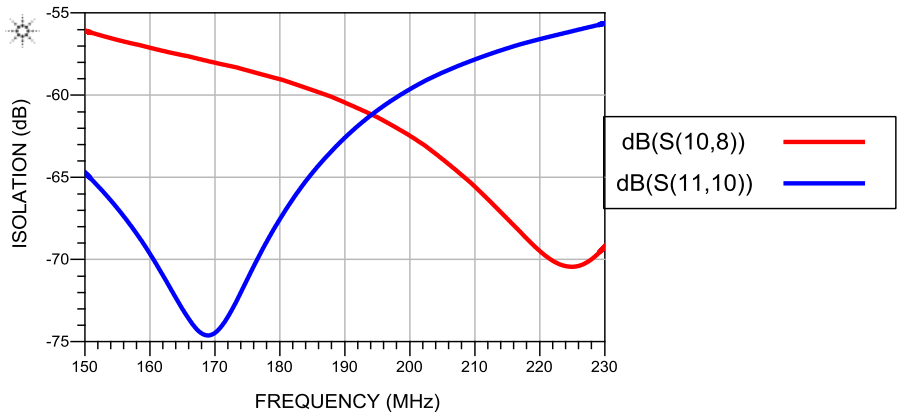

Figure 6.133: Simulated isolation between (a) PA and ANT (S(11,10); (b) PA and RX (S(10,8)) during receive

During transmit, there is low loss between PA and ANT ports and high isolation between PA and ANT ports and PA and RX ports. Maximum insertion loss during transmit is 1.789 dB at 157 MHz. Minimum isolation between PA and RX ports is 97 dB at 202 MHz and between ANT and RX ports is 80 dB at 230 MHz.

During receive mode, there is low loss between ANT and RX ports, as shown in Figure 6.8, and high loss between PA and ANT and PA and RX ports, as shown in Figure 6.9. Maximum insertion loss during receive is 1.36 dB at 230 MHz. Minimum isolation between PA and ANT ports is around 55 dB at 230 MHz and 56 dB at 150 MHz between PA and RX ports.

6.2.3 EM simulations

To provide a more accurate simulation of the circuit, all the PCB effects were modeled using a EM simulation in Momentum. The EM simulation results are then included in a EM/circuit co-simulation that includes both PCB layout effects as well as the linear circuit behavior.

6.2.3.1 Board Design

The prototype printed circuit board (PCB) was designed in Altium Designer on a 1 oz. FR4 substrate is described in Section 3.2.2.3.1. Due to an error in calculations, the width and gap of the CPWG were set

to 119 mils and 15 mils instead of 119 mils and 100 mils, respectively. This resulted in an impedance of 37 Ohms instead of 50 Ohms.

The board layout is shown in Figures 6.10 and 6.11. All components were surface mount with the exception of the PIN diodes and quadrature hybrid couplers, which were drop-in components. The boards were designed around the quadrature hybrids. To keep a small footprint, the board was designed to take advantage of height instead of length. Therefore, the high power and the low power sides were broken into two boards and stacked on top of each other. The two boards were connected with RF cables.

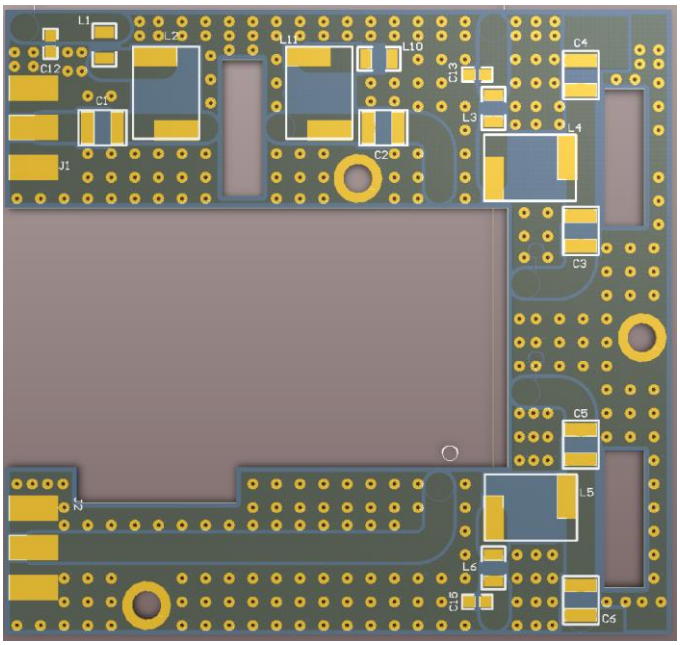

Figure 6.134: Mini T/R switch high power side PCB layout in Altium Designer

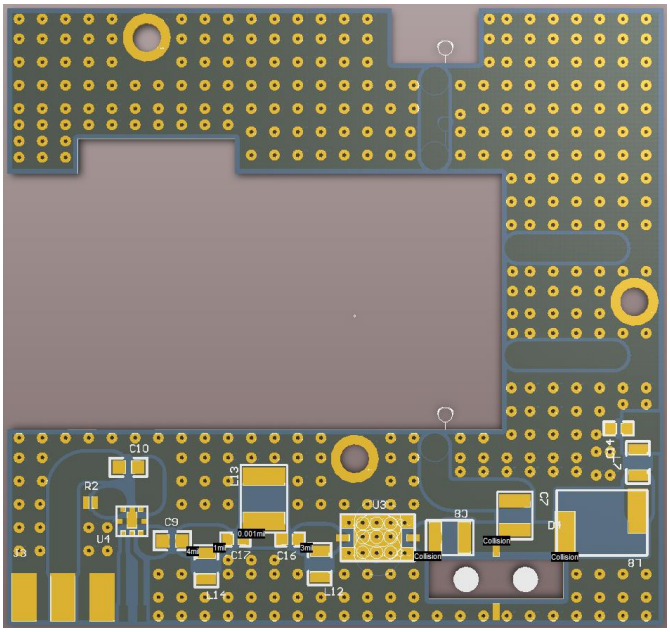

Figure 6.135: Mini T/R switch low power side PCB layout in Altium Designer

6.1.2.3.2 Circuit/EM Co-Simulation

The board layout was imported into ADS to perform electromagnetic simulations. Figure 6.12 shows the simulation setup used in ADS.

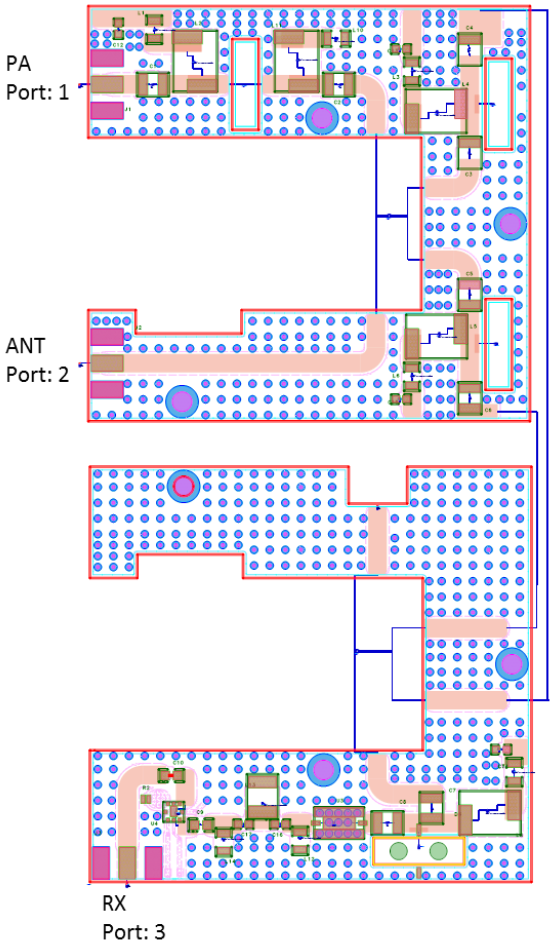

Figure 6.136: Circuit/EM co-simulation setup in ADS

During transmit mode, there is low loss between the PA and ANT ports, as shown in Figure 6.13, and high loss between PA and RX ports and ANT and RX ports, as shown in Figure 6.14.

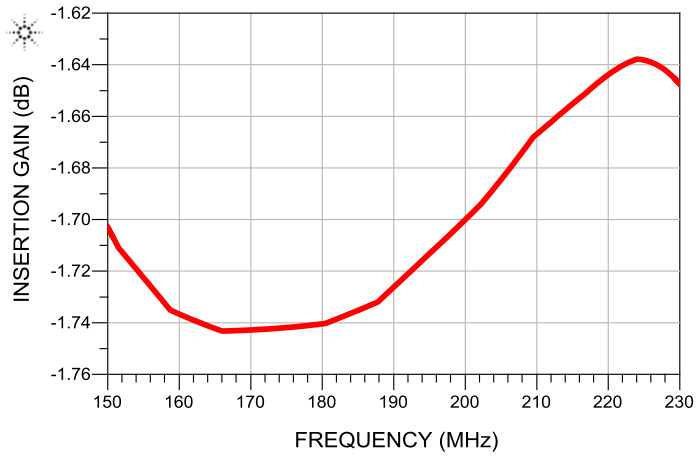

Figure 6.137: Simulated insertion gain between PA and ANT ports during transmit

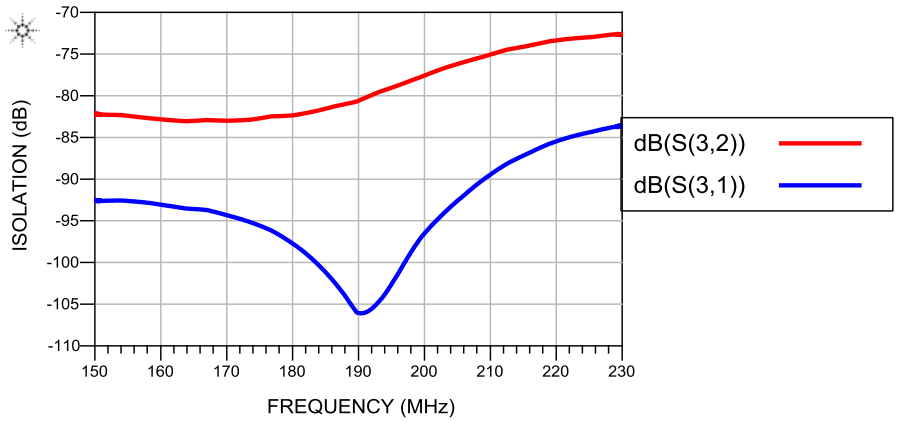

Figure 6.138: Simulated coupling between (a) ANT and RX (S(3,2)); (b) PA and RX (S(3,1)) during transmit

Maximum insertion loss during transmit is 1.743 dB at 166 MHz. Minimum isolation between PA and RX ports is 83 dB at 230 MHz and 72 dB at 228 MHz between ANT and RX ports.

During receive mode, there is low loss between ANT and RX ports, as shown in Figure 6.15, and high loss between PA and ANT and PA and RX ports, as shown in Figure 6.16.

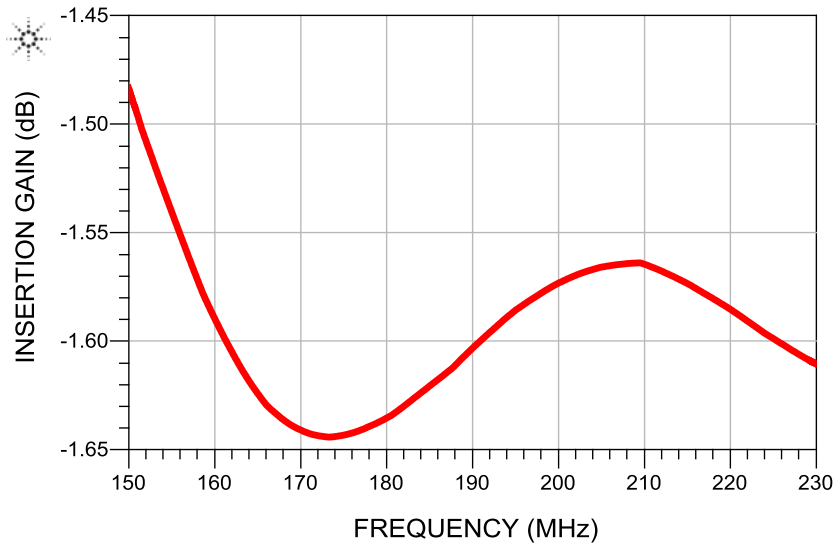

Figure 6.139: EM/Circuit Co-simulation simulated insertion gain between ANT and RX ports during receive

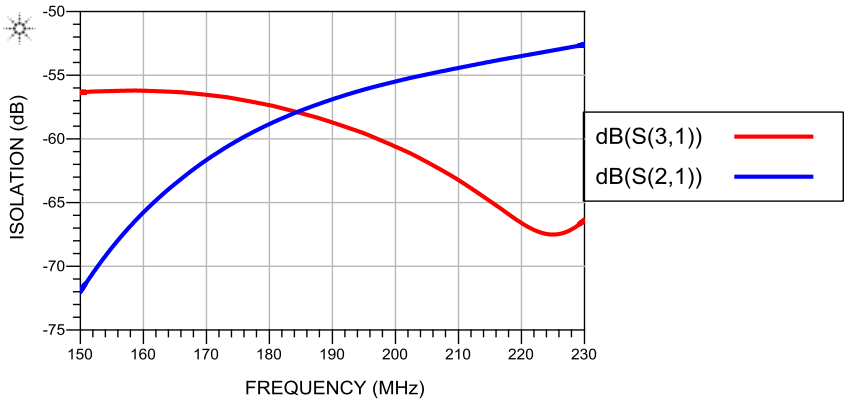

Figure 6.140: EM/Circuit Co-simulation simulated isolation between (a) PA and ANT (S(2,1); (b) PA and RX (S(3,1)) during receive

Maximum insertion loss during receive is 1.644 dB at 173 MHz. Minimum isolation between PA and RX ports is 56 dB at 158 MHz and 52 dB at 230 MHz between PA and ANT ports.

Figure 6.17 shows the insertion gain difference between low level, high level, and EM simulation during transmit and Figure 6.18 shows it during receive. Losses added by simulated transmission lines increases the insertion loss between high level simulation and EM/circuit co-simulation by 0.26 dB at 206 MHz during transmit and 0.436 dB at 168 MHz during receive. These are maximum difference in insertion loss.

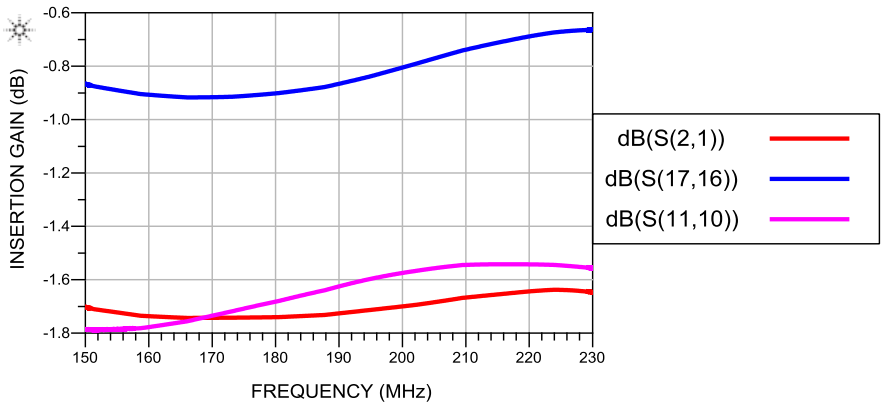

Figure 6.141: Simulated insertion gain between ANT and RX during receive (a) Ideal (S(17,16)); (b) High level (S(11,10)); (c) EM/Circuit Co-simulation (S(2,1))

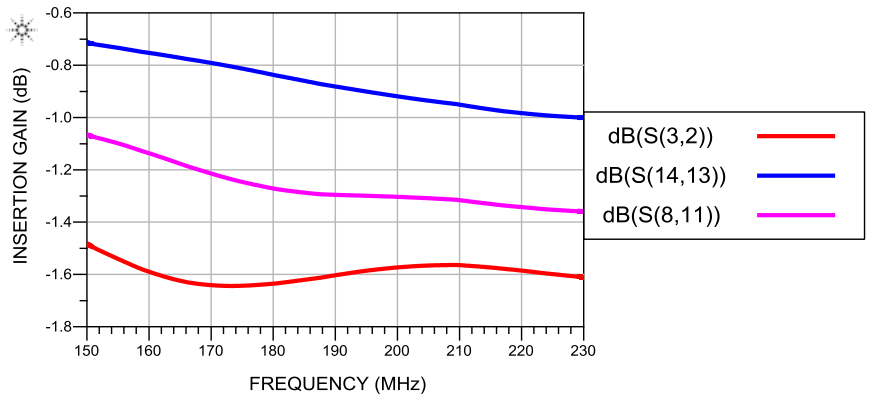

Figure 6.142: Simulated insertion gain between PA and ANT during transmit (a) Ideal (S(14,13)); (b) High level (S(8,11)); (c) EM/Circuit Co-simulation (S(3,2))

6.3 Small signal measurements

A 4-port Vector Network Analyzer was used to measure the scattering parameters of the transmit/receive switch. PIN Diodes were connected to a power supply and biased with 100 mA of forward bias current during transmit and 0 V reverse bias voltage during receive.

Figure 6.19 shows the insertion gain of the device along with low level, high level, and EM/circuit co-simulation results during transmit and Figure 6.21 shows it during receive. Figure 6.19 and 6.21 show the isolation during transmit and receive of the actual device.

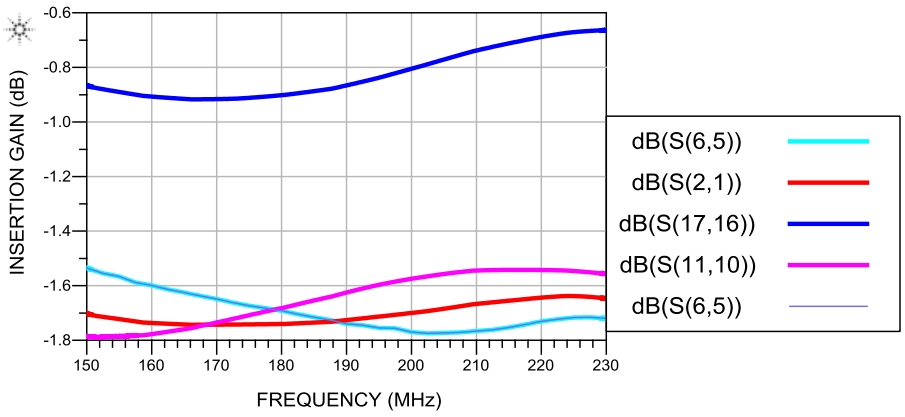

Figure 6.143: Simulated vs measured insertion gain between PA and ANT during transmit (a) Ideal (S(17,16)); (b) High level (S(11,10)); (c) EM/Circuit Co-simulation (S(2,1)); (d) measured (S(6,5))

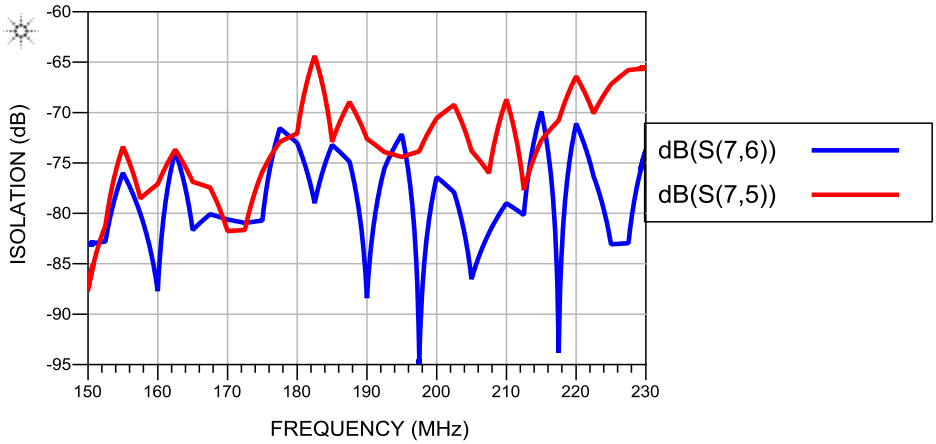

Figure 6.144: Measured coupling during transmit between (a) PA and RX (S(7,6)); (b) ANT and RX (S(7,5))

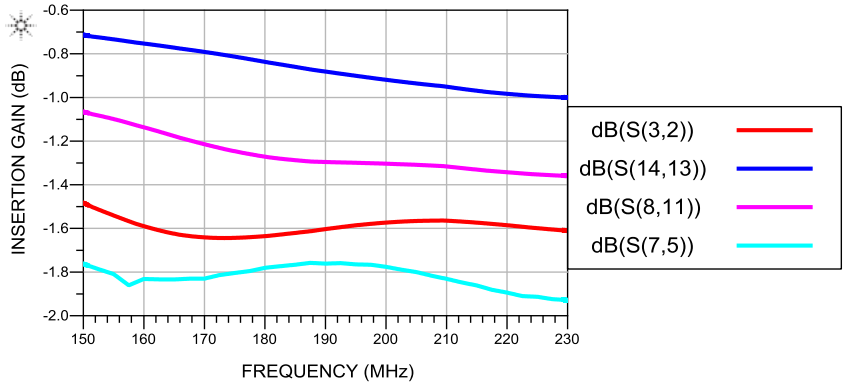

Figure 6.145: Simulated vs measured insertion gain between ANT and RX during receive (a) Ideal (S(14,13)); (b) High level (S(8,11)); (c) EM/Circuit Co-simulation (S(3,2)); (d) Actual (S(7,5))

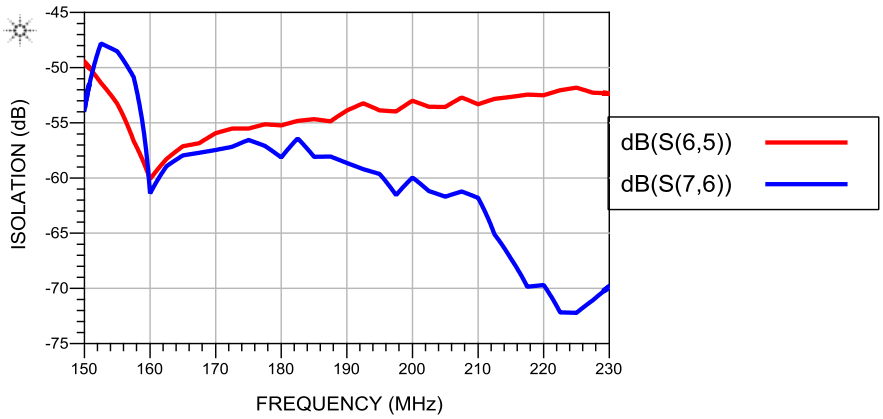

Figure 6.146: Measured coupling during receive between: (a) PA and ANT (S(6,5)); (b) PA and RX (S(7,6))

The measured response of the prototype matches up well with the EM/circuit co-simulation results. The maximum variance in insertion loss between EM/circuit simulation and prototype response is 0.124 dB during transmit and 0.318 dB during receive.

6.4 PIN Diode Driver Circuit

The PIN diode driver size was reduced by selecting components with smaller footprint. The non-inverting transceiver chip, used to buffer the signal, was changed to CD74HCT243M. Table 6.2 lists the important parameters of this transceiver chip.

Table 6.5: Summary of specifications for the CD74HCT243M line driver

Parameter	Characteristics	Unit
V_{CC}	4.5 – 5.5 (used at 5)	V
V_{IH}	2	V
V_{IL}	0.8	V
t_{PHL}	33	ns

The driver circuitry for the old isolation switch was also eliminated. The new switch, PE4245, only required +3.3 V, which was provide by ADR530BRT, a voltage reference chip that converts +5 V to +3.3 V.

Additionally, voltage regulation was added to the driver to provide +5 V and -12 V. LM317 was used to convert +12 V to +5 V and TPS63700, an inverting DC/DC converter, was used to convert +5 V to -12 V.

The PIN driver board was split into two boards just like the T/R switch. The driver for the high power side contained three PIN diode drivers as well as the input for the TTL signal as shown in Figure 6.23a. Driver for low power side contained the PIN diode driver as well as the voltage regulators as shown in Figure 6.27b. The two boards were connected with 24 gauge wires.

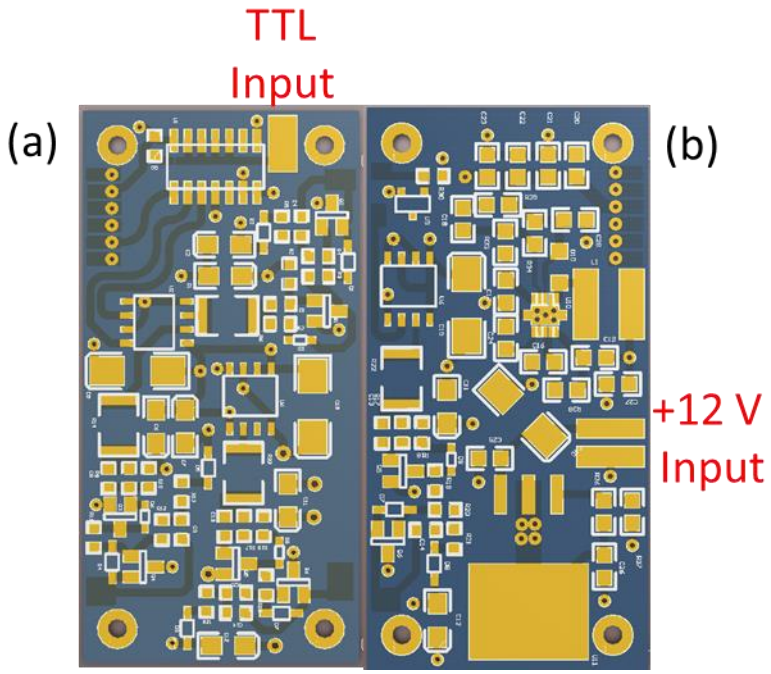

Figure 6.147: PIN diode driver for: (a) High power side of the T/R switch; (b) Low power side of the T/R switch

6.5 System integration, Laboratory tests, and field tests

6.5.1 Board and Chassis design

The T/R switch and the PIN diode driver were integrated into a single module. Figure 6.24 shows photographs of the module, presenting the high power, low power side, as well as a comparison between the old and the new T/R switch. The high and the low power sides are connected with RF cables. PIN diodes and its drivers are connect with 22 gauge wires. The drivers are placed on top of the

quadrature hybrids on standoffs. The high and low power side drivers are connected with 24 gauge wires that goes through the chassis. A volume reduction of 5 times was accomplished through this design while maintaining electrical performance.

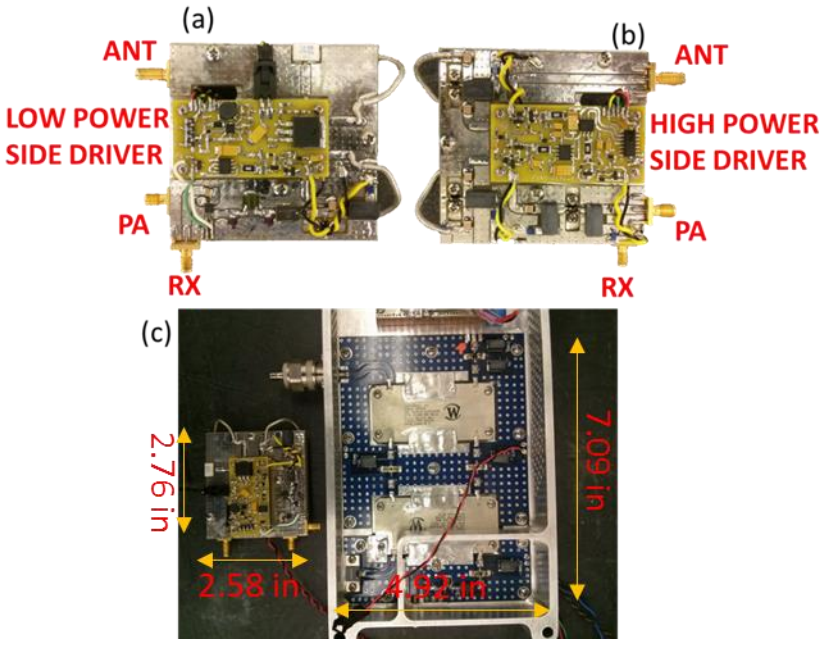

Figure 6.148: Photographs of the circuit developed (a) T/R switch and driver low power side; (b) T/R switch and driver high power side; (c) comparison between the miniaturized and old T/R switch

6.5.2 Characterization of the Complete Modules

6.5.2.1 Output power vs. input power in Transmit mode

Loss at the antenna port of the T/R switch was measured through the test setup mentioned in Section 4.3.2.1. All tests were done for a frequency range of 180 – 215 MHz. The same amplifier used in Section 4.3.2.1 was used for this test.

The amplifier was connected to the T/R switch to measure the loss during transmit as well as the feedthrough signal. Figure 6.26 shows the comparison of the input power at the PA port and the output power at the ANT port. Figure 6.27 shows the loss during transmission. Again, the isolation switch was placed in receive mode for this test due to an issue with its control signal.

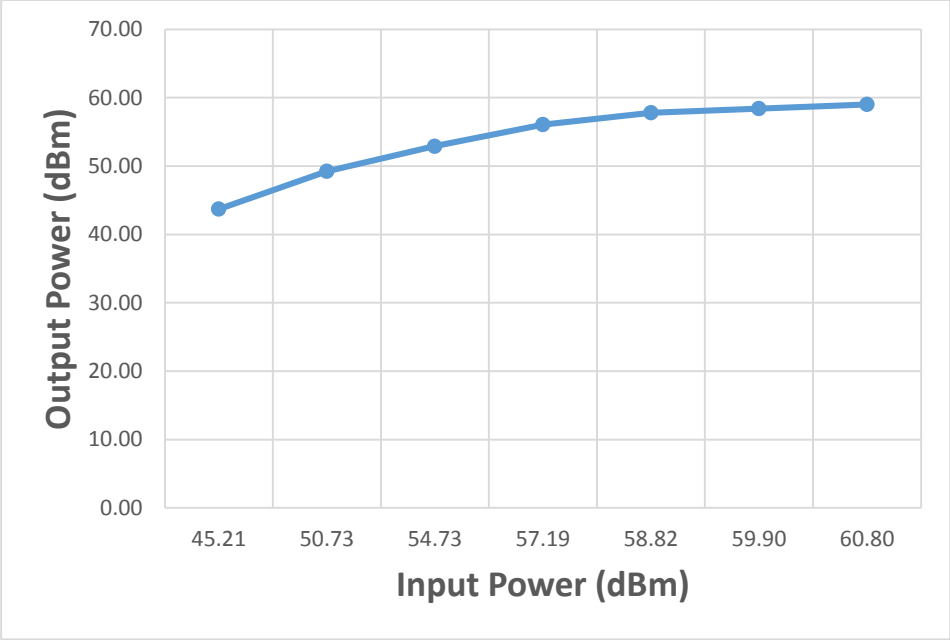

Figure 6.149: Measured power amplifier output power (ANT) vs input power (PA)

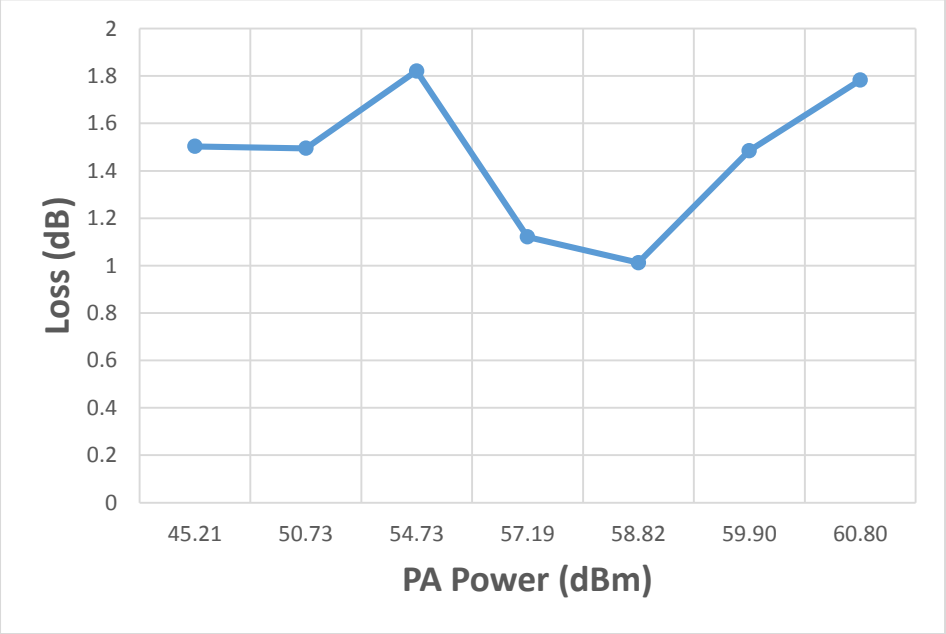

Figure 6.150: Measured Loss between PA and ANT ports of T/R switch during transmission

Figure 6.28 shows the feedthrough signal at the RX port during transmission. Since the isolation switch is set to receive, it enters into compression for power levels greater than 57 dBm.

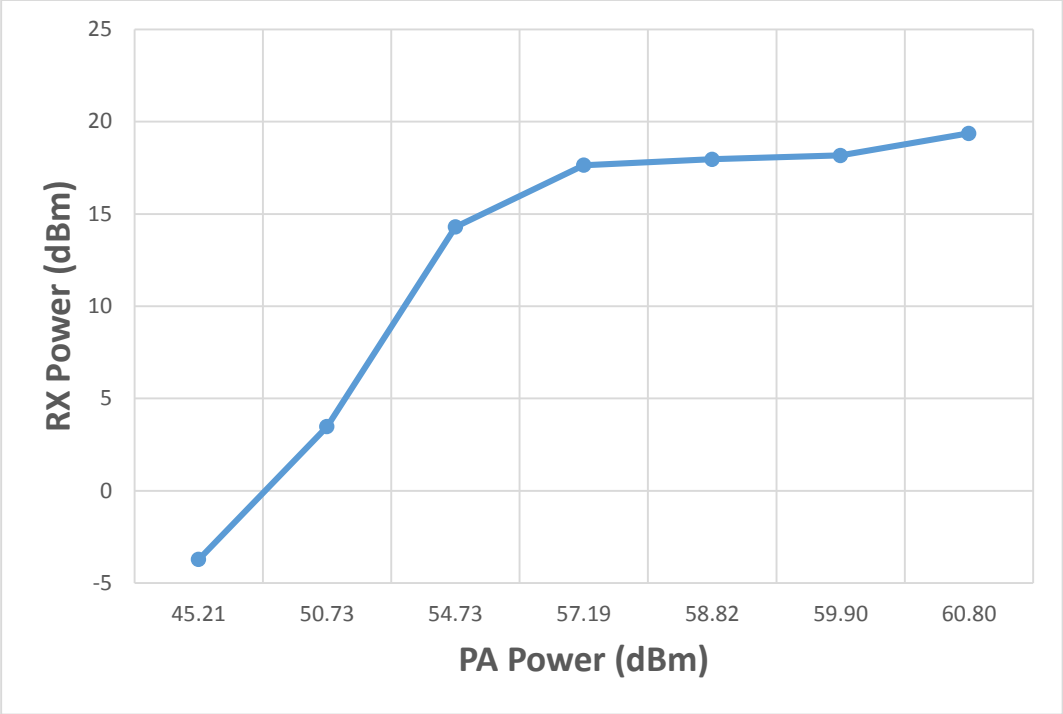

Figure 6.151: Measured feedthrough at RX port during transmission

At 1 kW peak power, loss is less than 1.8 dB during transmit and isolation between PA and RX ports and ANT and RX ports is around 40 dB. Isolation would increase by at least 40 dB with the enabling of the isolation switch. These losses are comparable to the small signal measurements.

6.5.2.2 Switching time

Switching time was measured by injecting a long pulse into the antenna port of T/R switch to simulate a continuous wave while the diodes were being toggled by the driver. The TTL signal had a time duration of 10 µs. Switching time of the series PIN diode was monitored as well as the signal at the receiver port.

Turn off time was measured from 50% TTL to 10% RF at the receiver port. Inversely, turn on time was measured from 50% TTL to 90% RF at the receiver port. Turn off time was found to be 1.4 µs and the turn on time was 350 ns as shown in Figure 6.25. Since the switching time is dominated by the response of the PIN diodes, the isolation switch was permanently set to receive mode for this test.

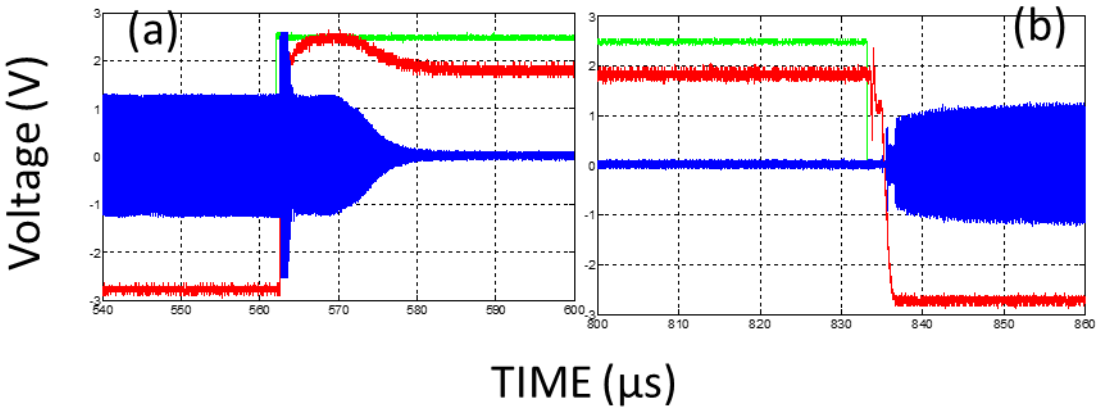

Figure 6.152: Measured switching time: (a) Turn off time measured from 50% TTL (Green) signal to 10% RF (Blue); (b) Turn on time measured from 90% RF (Blue) signal to 50% TTL (Green) signal; Also shown is the series diode response (Red)

7 Conclusion and Future work

Three different T/R switches were successfully developed for three different frequency bands: 160-230 MHz (VHF band), 150-600 MHz (VHF/UHF), and 10-45 MHz (HF band). The circuits are capable of transmitting at least 1000 W of peak power and exhibit an insertion loss lower than 1.3 dB for 160-230 MHz, 1.6 dB for 150-600 MHz, and 2.39 dB for 10-45 MHz ranges. A fourth, miniaturized prototype for the 160-230 MHz range was implemented and had a insertion loss of 1.8 dB . The circuits developed exhibit turn-on times better than 1.3 µs for the VHF/UHF circuits; and 1.5 µs for the HF circuits. The turn-off times were better than 200 ns for the first two bands and 1.36 µs for the HF band.

Future work will include optimization of the 10-45 MHz T/R switch to decrease loss and increase switching speed. The miniaturized 160-230 MHz T/R switch will be expanded to a frequency range of 150-230 MHz.

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