A LINEARIZATION METHOD FOR A UWB VCO-BASED CHIRP GENERATOR USING DUAL COMPENSATION

BY

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ABSTRACT

Ultra-Wideband (UWB) chirp generators are used on Frequency Modulated Continuous Wave (FMCW) radar systems for high-resolution and high-accuracy range measurements. At the Center for Remote Sensing of Ice Sheets (CReSIS), we have developed two UWB radar sensors for high resolution measurements of surface elevation and snow cover over Greenland and Antarctica. These radar systems are routinely operated from both surface and airborne platforms. Low cost implementations of UWB chirp generators are possible using an UWB Voltage Controlled Oscillator (VCO). VCOs possess several advantages over other competing technologies, but their frequency-voltage tuning characteristics are inherently non-linear. This nonlinear relationship between the tuning voltage and the output frequency should be corrected with a linearization system to implement a linear frequency modulated (LFM) waveform, also known as a chirp. If the waveform is not properly linearized, undesired additional frequency modulation is found in the waveform. This additional frequency modulation results in undesired sidebands at the frequency spectrum of the Intermediate Frequency (IF) stage of the FMCW radar. Since the spectrum of the filtered IF stage represents the measured range, the uncorrected nonlinear behavior of the VCO will cause a degradation of the range sensing performance of a FMCW radar. This issue is intensified as the chirp rate and nominal range of the target increase.

A linearization method has been developed to linearize the output of a VCO-based chirp generator with 6 GHz of bandwidth. The linearization system is composed of a Phase Lock Loop (PLL) and an external compensation added to the loop. The nonlinear behavior of the VCO was treated as added disturbances to the loop, and a wide loop bandwidth PLL was designed for wideband compensation of these disturbances. Moreover, the PLL requires a loop filter able to attenuate the reference spurs. The PLL has been designed with a loop bandwidth as wide as possible while maintaining the reference spur level below 35 dBc. Several design considerations were made for the large loop bandwidth design. Furthermore, the large variations in the tuning sensitivity of the oscillator forced a design with a large phase margin at the average tuning sensitivity. This design constraint degraded the tracking performance of the PLL. A second compensation signal, externally generated, was added to the compensation signal of the PLL. By adding a compensation signal, which was not affected by the frequency response effects of the

loop compensation, the loop tracking error is reduced. This technique enabled us to produce an output chirp signal that is a much closer replica of the scaled version of the reference signal. Furthermore, a type 1 PLL was chosen for improved transient response, compared to that of the type 2 PLL. This type of PLL requires an external compensation to obtain a finite steady state error when applying a frequency ramp to the input. The external compensation signal required to solve this issue was included in the second compensation signal mentioned above.

Measurements for the PLL performance and the chirp generator performance were performed in the laboratory using a radar demonstrator. The experimental results show that the designed loop bandwidth was successfully achieved without significantly increasing the spurious signal level. The chirp generator measurements show a direct relationship between the bandwidth of the external compensation and the range resolution performance.

ACKNOWLEDGMENTS

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CHAPTER 1: INTRODUCTION

1.1 SCIENCE BACKGROUND

According to recent studies, the polar ice sheets' contribution to sea level rise due to mass loss has increased by 40% in the last decade [1]. Surface elevation changes constitute an important indicator in estimates of mass balance changes [1][2][3]. To estimate mass balance changes on the ice sheet from surface elevation measurements, corrections for the variable firn compaction and the bedrock motion should be applied [4][5]. A wide range of measurement techniques have been developed in past decades to monitor surface elevation changes in Polar Regions. These include the use of radar and laser altimeter instruments with high-resolution measurement capabilities.

1.1.1 Laser Altimeters

Laser altimeters operating from both aircraft and satellite platforms are used for topographic mapping of various targets with vertical range resolution of tens of centimeters or less. Their principle of operation relies on measuring the round-trip propagation time of nanosecond pulses emitted by solid state laser sources [6]. Laser altimetry represents a valuable tool for precise mapping and monitoring of Polar Regions [7].

In 2003, the National Aeronautics and Space Administration (NASA) launched the Ice, Cloud and Land Elevation Satellite (ICESat) carrying the Geoscience Laser Altimeter System (GLAS). The laser altimeter GLAS' primary mission was to measure the elevation changes in the Antarctic and Greenland ice sheets. Many different methods have been developed for deriving surface elevation changes using ICESat data [4][5]. Moreover, ICESat's unprecedented level of accuracy of elevation measurements has been used to characterize for range errors in satellite radar altimeters, such as the European Remote Sensing 2 Satellite (ERS-2) and the Environmental Satellite (Envisat) [8].

1.1.2 Radar Altimeters

Although laser altimeters such as GLAS possess high accuracy and high precision, they do not operate well when fog, smoke or any precipitation is present in their line of sight [9]. In contrast, radar altimeters, with the exception of some frequency ranges of operation, have the ability to perform measurements under these conditions [10].

An example of a system designed for altimetry measurements from a satellite platform is the Synthetic-Aperture-Radar Interferometric Radar Altimeter (SIRAL). SIRAL is an instrument on board the European Space Agency's (ESA) Cryogenic Satellite 2 (CryoSat-2), which provides altimetry information with a range resolution of 40 m/pixel [11].

Satellite radar altimeters are not devoid of shortcomings, as they are affected by both topography and penetration [12]. Radar altimeter signals may penetrate through snow, firn and ice, causing an accuracy error in the elevation measurement [12][14]. The backscatter signals for subsurface interfaces can be stronger than the actual surface return [14]. The CryoSat-2 altimeter includes a delay-Doppler technology to overcome the steep-slop error common on typical radar altimeters, such as the ESR-2 and Envisat [11][13].

Ground based and airborne radar altimeters with higher accuracy can be used to characterize and validate data from satellite altimeter radars. Ground based altimeters have been developed to provide high accuracy elevation data, but they are not very practical for large coverage measurements as airborne altimeters. Airborne altimeters validated by ground based systems would provide accurate measurements of surface elevations, as long as they have the sufficient resolution to resolve subsurface layers and identify the actual surface return.

1.2 CRESIS UWB RADARS

The Center for Remote Sensing of Ice Sheets (CReSIS) has developed two Ultra-Wideband (UWB) Microwave Radars for airborne and surface-based platforms: The Snow Radar, which operates over the 2-8 GHz range and the Ku-Band Radar, which operates over the 12-18 GHz range. The Snow Radar was primarily developed for measuring the thickness of

snow over sea ice [16]. The Ku-band radar altimeter is used for high-accuracy surface elevation measurements over land and sea ice [16]. Both the Snow and Ku-Band Radars also provide high resolution information about the near-surface internal layers. Both systems are operated as part of the CReSIS instrumentation package and operate routinely on board of various airborne platforms, such as the NASA P-3 and DC-8 Airborne Science Laboratories, as well as a DHC-6 Twin Otter [16][17]. Measurements on board of the NASA aircraft are conducted in the context of Operation IceBridge (OIB), an airborne program launched to operate on the period between the loss of ICESat I and the launch of ICESat II [17].

An essential component of these radars is the UWB chirp generator, which synthesizes the transmit waveform at microwave frequencies. This thesis discusses the development of an UWB chirp generator with improved frequency linearity implemented with high-speed analog design techniques. The linearization scheme relies on a PLL operating in conjunction with an external compensation added to the loop.

1.3 THESIS OUTLINE

This thesis is composed of 5 Chapters: Chapter 2 provides the theoretical framework that has been considered for the design of the proposed chirp generator. The background concepts described in Chapter 2 include theory of radar systems, linear control systems, and phase lock loops. Chapter 3 describes the design and implementation of the chirp generator. Specifically, Chapter 3 explains the design and implementation considerations for the phase lock loop and the pre-distorted voltage generator. Chapter 4 presents the results from the performance characterization of system. Lastly, Chapter 5 presents the conclusions and discusses suggestions for future work.

CHAPTER 2: BACKGROUND

2.1 UWB FMCW RADAR BACKGROUND

2.1.1 Radar Overview

2.1.1.1 Radar Basics and Impulse Radar

The word RADAR is the acronym for Radio Detection And Ranging. It is the standard name for the technology that uses electromagnetic signals to detect distant targets and to measure their range. In radar terminology, a target is the object detected and the range is the distance of the object to the sensor. Radar sensors can detect targets beneath certain materials which would not be detected with optical techniques. Besides detecting objects and measuring their range, modern radar systems have the ability to measure other properties of the target such as radial speed and radar cross section [18].

A typical impulse radar waveform is composed of a train of narrow pulses modulated by a sinusoidal carrier [18]. The radar system transmits the waveform as an electromagnetic signal. The signal propagates through the medium, gets reflected at the target and then travels back to the receiver. The range (R) of the target can be determined from the roundtrip signal delay (T_R) and the speed of the signal in the propagation medium (v) using equation (2.1) [18].

$$R = \frac{v \cdot T_R}{2} \tag{2.1}$$

On an impulse radar system, the roundtrip delay of the received signal is measured directly with respect to the transmit signal. On this type of radar, the time between pulses is known as the pulse repetition interval (PRI). During this interval, the radar transmits a pulse for a limited amount of time known as the pulse length. The radar then listens during the rest of the

PRI for the received signal. It can be shown that there exists range ambiguity for targets with roundtrip delays larger than the PRI [18].

The carrier tone that modulates the pulse signal can be modulated further in frequency and amplitude. The most common technique to improve range resolution, which also improves the signal to noise ratio of the signal, is to frequency modulate the signal. If the waveform is linearly frequency modulated, it is also known as a chirp. Regardless of the shape of the signal, a technique known as pulse compression uses a matched filter to improve the range resolution and the signal to noise ration. If the waveform is a chirp, the signal to noise ratio gets improved by the bandwidth-pulse-length product and the range resolution becomes inversely proportional to the bandwidth [18].

Impulse radar systems apply pulse compression either with a real-time processor or at a post-processing stage after having recorded the received data. The pulse compression can be applied with digital, analog or mixed signal devices [19][20][21]. However, digital post processing of the recorded raw data continuous being the most robust method since it allows the ability to reprocess the data with improved techniques. In order to apply any type of pulse compression by digital means, the digitizer's sampling rate should be at least twice the signal bandwidth [22]. This fact poses a limitation on the bandwidth of impulse radars.

2.1.1.2 Continuous Wave Radar

Typical continuous wave (CW) radars or unmodulated continuous wave radars have a signal composed of an unmodulated single tone. CW radars make use of the Doppler Effect to measure radial speed of targets. The Doppler Effect is the description of the behavior of the frequency content of a signal when it is reflected off a moving target [18]. The frequency content on a signal reflected off a moving target gets shifted by the Doppler frequency (f_d). The Doppler frequency depends on the wavelength (λ) of the carrier signal and the radial speed (v) of the moving target with respect to the sensor. Equation (2.2) describes this relationship.

$$f_d = \frac{2 \cdot v}{\lambda} \tag{2.2}$$

CW radar sensors are used when the target velocity is the main parameter to be measured. CW radar sensors for short range and moderate ranges are much simpler systems than pulse radar systems [18]. However, the transmit power of CW radar systems is limited by the amount of transmit leakage to the receiver that can be tolerated. Moreover, CW radars with a single transmit tone do not have the ability to unambiguously measure range. Multi-tone CW radars have the ability to measure range with accuracy and ambiguity limited by the number of tones selected and their frequencies [23][18].

2.1.1.3 Frequency Modulated Continuous Wave RADAR

Frequency Modulated Continuous Wave (FMCW) Radar, as the name implies, uses a frequency modulated waveform. Typically, this waveform is linearly frequency modulated, also known as a chirp. In contrast to the unmodulated CW radars, the frequency content of the received signal from FMCW radars may be used to extract both the range and the radial speed of the target [18].

The block diagram shown in Figure 2.1 represents a typical FMCW system and illustrates the paths which the FMCW waveform goes through. Each stage on the paths has a frequency dependent system response that will affect the waveform signal. The FMCW waveform goes through two paths: the reference path and the transmit/receive path. The transmit/receive path comprises the radio frequency transmit (RF TX) stage, the antenna, the roundtrip channel to and from the target, the target return loss and the radio frequency receive (RF RX) stage. The reference path includes the conditioning stage for the waveform to drive the Local Oscillator (LO) port on the mixer.

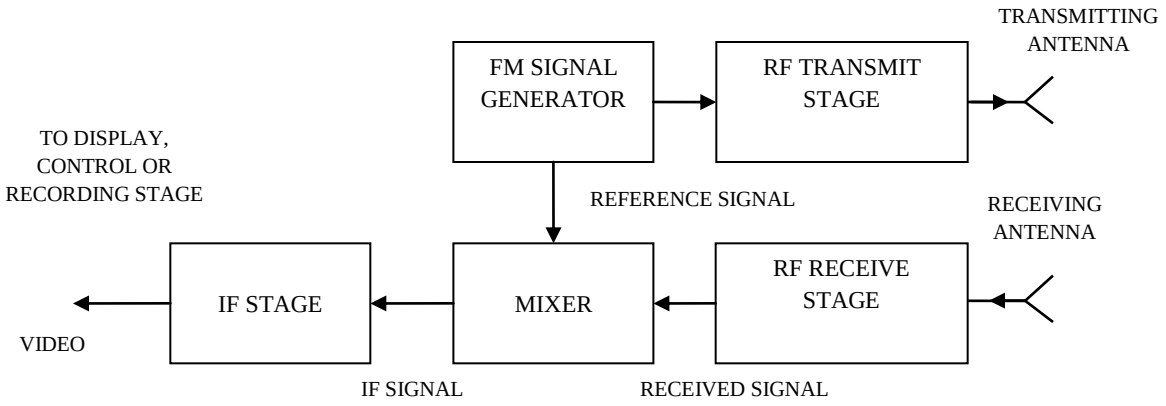

Figure 2-1: Block Diagram of FMCW Radar

The output signals of both paths, the reference and the received signals, are applied to the mixer followed by the Intermediate Frequency (IF) stage. The output of the IF stage goes to a display, control or recording stage.

The FMCW radar makes use of the ideal behavior of the mixer as a signal multiplier. The output of the mixer becomes the multiplication of the reference and the received signals. The IF stage then filters and conditions the IF signal which contains information about the range and radial speed of the target.

The chirp waveform is the most common one for FMCW radars. A plot of the frequency behavior over time for the reference and receive signals is shown in Figure 2.2. For simplicity, both amplitude and frequency modulations that may affect the shape of the frequency signals are neglected. The frequency of the reference signal is an identical copy of that of the FMCW generated waveform delayed by the reference path delay. The reference path delay is the time it takes the waveform to go from the waveform generator to the LO port of the mixer. Similarly, the frequency waveform of the received signal is also an identical copy of the generated waveform delayed by the transmit-receive path delay. The difference between these two delays is represented by τ in Figure 2.2.

On the bottom plot of figure 2.2, the beat frequency (f_b) is shown. The beat frequency is the difference between the reference and the received frequencies [18]. The difference between both delays can be extracted from the beat frequency by considering the similar triangles formed.

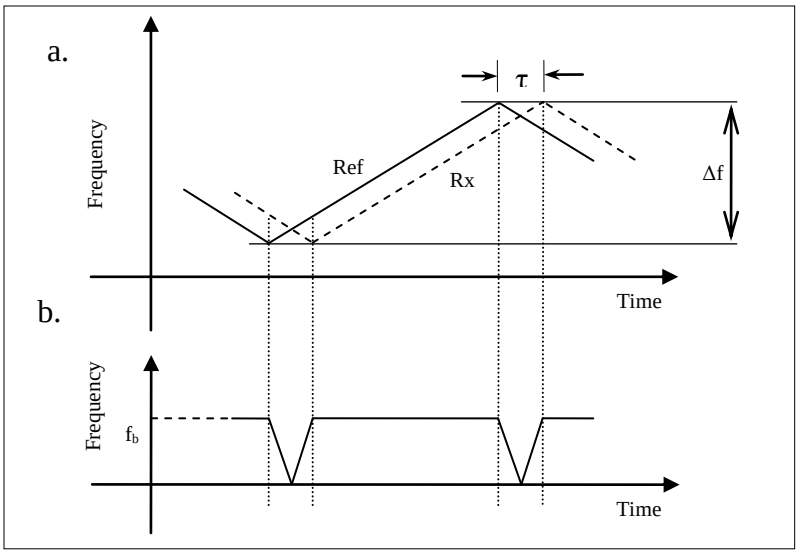

Figure 2-2: a. FMCW Frequency Plots of Reference (Ref) and Received (Rx) signals for a stationary target. b. FMCW beat frequency (fb) resulting from the difference of the reference and receive signal frequencies

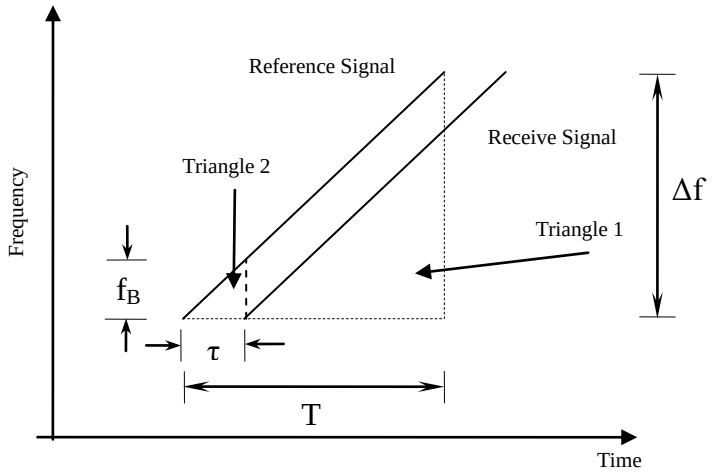

Figure 2-3: Frequency of Reference and Receive Signals for similar triangle analysis to determine the beat frequency

As shown in Figure 2.3, two right-angled similar triangles are formed out of the frequency plots of the received and reference signals. Triangle 1 is formed by the chirp bandwidth (Δf) as the height cathetus and the chirp time length (T) as the base cathetus. Triangle 2 is formed by the beat frequency (f_B) as the height cathetus and the delay difference between the reference and received signals (τ) as the base cathetus. The beat frequency (f_B) can be solved as shown on equation (2.3).

$$f_B = \tau \cdot \frac{\Delta f}{T} \tag{2.3}$$

On equation (2.4), τ corresponds to the delay difference between the reference and the received signal. The reference and received signals are delayed from the waveform generator output by τ_{REF} and τ_{RX} respectively. Moreover, the target range may be inferred from the delay difference between the delay to the transmit antenna ($\tau_{TX\_ANTENNA}$) and the delay to the receive antenna ($\tau_{RX\_ANTENNA}$).

$$\tau = \tau_{RX} - \tau_{REF} \tag{2.4}$$

$$\tau_o = \tau_{RX\_ANTENNA} - \tau_{TX\_ANTENNA} \tag{2.5}$$

Typically for analysis purposes, we may assume the following approximation:

$$\tau_o \approx \tau \tag{2.6}$$

In practice, all the previously mentioned delays should be measured and a delay correction should be applied to the data for accurate range measurements.

Once the actual roundtrip delay to the target is found, the target range can be calculated using equation (2.1).

For the case when the target range is not stationary, either the receiver or the target moves with a radial speed towards or away from each other, the beat frequency will be shifted by the Doppler frequency (f_D) [18]. The Doppler frequency is added or subtracted to the range component of the beat frequency depending on the sign of the chirp rate (μ). Both cases are illustrated on equations (2.7) and (2.8).

$$f_B(\mu > 0) = f_R - f_D \tag{2.7}$$

$$f_B(\mu < 0) = f_R + f_D \tag{2.8}$$

On equations (2.7) and (2.8), f_R corresponds to the range part of the beat frequency and can be extracted by averaging the beat frequency of two chirps with chirp rates equal in magnitude but opposite sign.

As mentioned earlier, FMCW radar systems use the ideal behavior of the mixer as a multiplier to extract range and radial speed information. To do so, it only needs to extract the beat frequency using the reference and receive signals. Normalizing the amplitude terms for simplicity and setting the reference initial phase as zero, both signals may be described by equations (2.9), (2.10) and (2.11) for a linear frequency modulated waveform.

$$S_{REFERENCE} = \cos\left[2\pi\left(f_o \cdot t + \frac{1}{2}\mu \cdot t^2\right)\right] \tag{2.9}$$

$$S_{RECEIVE} = \cos\left[2\pi\left(f_o \cdot (t-\tau) + \frac{1}{2}\mu \cdot (t-\tau)^2\right)\right] \tag{2.10}$$

$$S_{RECEIVE} = \cos\left[2\pi\left(-f_o \cdot \tau + \frac{1}{2}\mu \cdot \tau^2 + (f_o - \mu \cdot \tau)t + \frac{1}{2}\mu \cdot t^2\right)\right] \tag{2.11}$$

$$S_{IF} = S_{RECEIVE} \cdot S_{REFERENCE} \tag{2.12}$$

$$S_{IF} = \frac{1}{2}\left\{\cos\left[2\pi\left(f_o\tau - \frac{1}{2}\mu \cdot \tau^2 + \mu \cdot \tau \cdot t\right)\right] + \cos\left[2\pi\left(f_o\tau - \frac{1}{2}\mu \cdot \tau^2 + (2f_o + \mu \cdot \tau) \cdot t + \mu \cdot t^2\right)\right]\right\} \tag{2.13}$$

Equations (2.12) and (2.13) describe the resulting IF signal (S_{IF}) out of the ideal mixer. The resulting IF signal has two components. The first component is a tone with frequency ($\mu \cdot \tau$) and initial phase $(f_o\tau - \frac{1}{2}\mu \cdot \tau^2)$. This component signal is also known as the beat frequency signal. The second component is a chirp waveform with initial phase $(f_o\tau - \frac{1}{2}\mu \cdot \tau^2)$, initial frequency $(2f_o + \mu \cdot \tau)$ and chirp rate $(2 \cdot \mu)$. The IF stage filters this IF signal so that only the beat signal passes. The beat frequency then may be used to extract range and radial speed information.

For FMCW radars that measure single stationary targets, the frequency modulation need not be linear. The range of the target can be found by the average frequency of the video signal. However, FMCW radar sensors for multi-target measurements need to have a linear frequency

modulated waveform. The importance of having a linear chirp with no additional frequency or amplitude modulation is explained on the next section.

2.1.2 FMCW Waveform Quality

On the previous section, the effects caused by the amplitude and phase response at each stage have been neglected to simplify the analysis. Moreover, the chirp-based FMCW signal has been assumed to be a perfectly linear frequency modulated waveform. However, the amplitude and phase responses of each stage may affect significantly the performance of the radar. Since the waveform frequency is swept over a time period, the amplitude and phase responses over frequency gets mapped over the chirp period and then delayed for each path. In addition, the frequency nonlinearity and amplitude modulation at the generation point will also affect the radar range resolution performance.

The range resolution is the minimum range difference between two distinguishable targets. In other words, the range resolution defines the ability of a radar sensor to distinguish close targets. For an FMCW radar system, the target range response is described by the frequency spectrum of the video signal over the overlapping interval (T_{OL}) between the reference and the received signals.

$$T_{OL} = T_{chirp} - 2 \cdot \tau \tag{2.14}$$

Equation (2.14) describes the overlapping interval of the reference and the received chirp signals. On equation (2.14), T_{chirp} is the chirp time length or just chirp length and τ is the difference in time delay between the reference and the received signals. The value of τ will be approximated to the roundtrip time delay of the transmitted signal to simplify the analysis on this section.

For a digitally recorded video signal over the overlapping time interval, the frequency spectrum of the video signal can be computed using the Fast Fourier Transform (FFT) [22]. For the FFT of the video signal time gated by the overlapping time interval, the FFT frequency

resolution equals the inverse of the overlapping time interval. This relationship is described on equation (2.15).

$$\delta f = \frac{1}{T_{OL}} \tag{2.15}$$

$$\delta f_B = \frac{\Delta f \cdot \delta \tau}{T} = 2 \cdot \frac{\Delta f \cdot \delta R}{Tv} \tag{2.16}$$

Equation (2.16) shows the relationship between a small difference on the beat frequency (δf_B) and the range resolution (δR). On equation (2.16), Δf is the bandwidth of the chirp, v is the signal propagation speed, T is the overlapping time interval and $\delta \tau$ is a small difference in the roundtrip.

$$\delta R = \frac{v}{2 \cdot \Delta f} \tag{2.17}$$

Since the minimum frequency difference will be described by the frequency resolution of the FFT output, the range resolution can be solved by combining equations (2.15) and (2.16). The range resolution is shown on equation (2.17).

Equation (2.17) describes the range resolution as the equivalent range difference between two FFT bins, known as range bins. Another way to define the range resolution performance of a radar system is to define the difference in range between two distinguishable peaks. Thus, by measuring a single target response two distinguishable peaks can be defined as the distance between the mainlobe and the first sidelobe. The sidelobe level dictates the dynamic range for close targets. As it will be seen on the next section, the sidelobe performance can be degraded by sidebands added by the system's imperfections. Moreover, the sidelobes can be suppressed using weighting techniques on the time gated video signal at the expense of widening the range resolution. Therefore, a more complete description of the range resolution performance can be expressed by indicating the mainlobe to first sidelobe range difference, the first sidelobe level and the weighting being used.

This section discusses the amplitude and frequency modulation applied by system imperfections to the chirp and their effects on the range resolution performance on an FMCW radar system.

2.1.2.1. Amplitude Modulation

Assuming a perfectly linear chirp and ideal phase responses at each stage, only the effects from amplitude are considered. From communication theory, double sideband amplitude modulation occurs when a high frequency carrier gets multiplied by a Direct Current (DC) biased low frequency signal [24]. Thus, the low frequency signal appears on the envelope of the carrier. A chirp has amplitude modulation when its envelope magnitude varies with time.

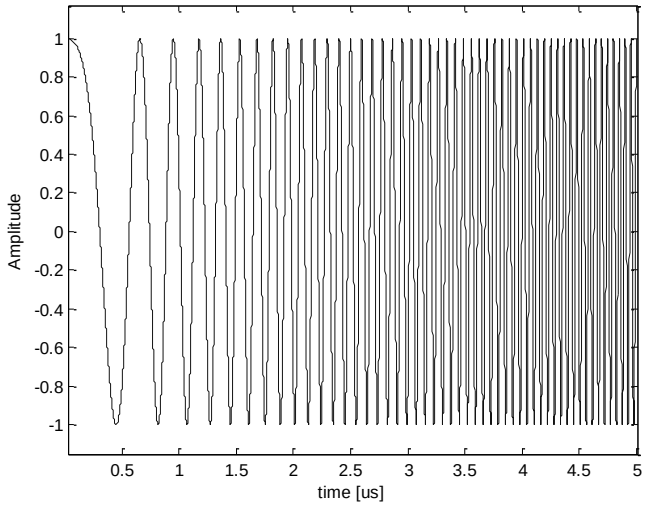

Figure 2-4: Example of a Chirp Waveform with no amplitude modulation

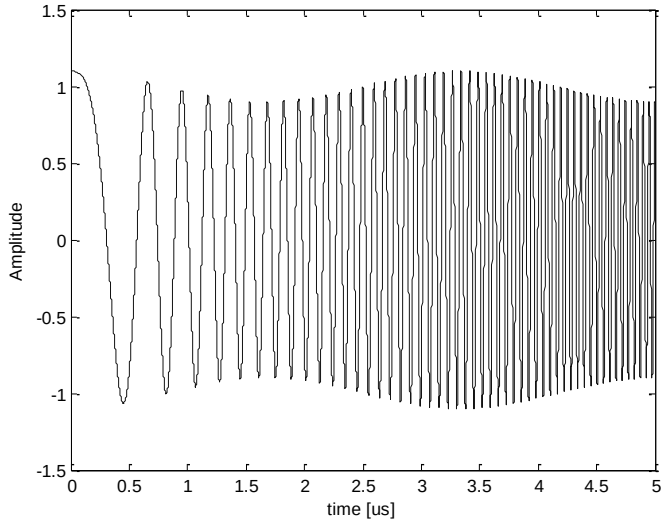

Figure 2-5: Example of a Chirp Waveform with amplitude modulation

Figure 2-4 and Figure 2-5 show examples of an unmodulated chirp and an amplitude modulated chirp, respectively.

The chirp may contain amplitude modulation at the generation stage or it may be added at one of the FMCW signal paths. Each stage's amplitude response will modulate the amplitude of its input waveform which may already be modulated. Then, the amplitude modulation can be analyzed in terms of many amplitude waveforms, where each amplitude waveform will be multiplied to its input signal.

Table 2-1: List of Amplitude Waveforms

Source of Amplitude Modulation	Amplitude Waveform Variable
Chirp Generator amplitude waveform at the Ref. Point	a_{CG_REF}
Chirp Generator amplitude waveform at the Rx. point	a_{CG_Rx}
Transmit Stage and Transmit antenna amplitude response	a_{TX}
Channel amplitude response	a_{CH}
Target Reflection amplitude response	a_{TR}
Receive Stage and Receive antenna amplitude response	a_{RX}
Reference Path Amplitude Waveform	a_{REF}
Mixer Conversion Factor amplitude response	K
IF Stage amplitude response	a_{IF}

Assuming a linearly frequency modulated signal, the amplitude waveforms in Table 2-1 correspond to the gain or attenuation that gets added (in dB) by each stage over the sweep time. The amplitude waveforms in Table 2-1 are related to the amplitude response over frequency that gets mapped for the chirp frequency sweep. To simplify the analysis, the amplitude waveforms take into account the delay of the chirp up to that point.

Then the amplitude waveform of the IF stage output signal can be expressed as follows:

$$a_{VIDEO} = a_{IF} \cdot k \cdot (a_{CG\_RX} \cdot a_{TX} \cdot a_{CH} \cdot a_{TR} \cdot a_{RX}) \cdot (a_{CG\_REF} \cdot a_{REF}) \tag{2.18}$$

As shown on equation (2.18), the amplitude waveforms corresponding to the different stages on the radar become a chain of potential amplitude modulation signals.

In order to analyze the effects of a generated amplitude modulated chirp waveform on the radar range resolution, the following example neglects any added amplitude modulation caused by the amplitude response at any other stage.

As an example, a generated amplitude modulated chirp, which has an amplitude waveform a_{CG}, is mixed with its delayed version to result in the amplitude waveform of the

video signal (a_{video}). For this example, the amplitude waveform of the generated chirp is composed of a DC-biased tone signal with a DC offset of 1 and a tone frequency of 1 MHz. The amplitude modulation index that scales the tone signal has been set to a value of 0.1. The amplitude waveform of the chirp is described on equation (2.19).

$$a_{CG} = 1 + 0.1 \cdot \cos(2 \cdot \pi \cdot f_o \cdot t) \tag{2.19}$$

$$a_{VIDEO} = a_{CG}(t) \cdot a_{CG}(t - \tau) \tag{2.20}$$

$$a_{VIDEO} = 1 + 0.1 \cdot \cos(2\pi f_o t) + 0.1 \cdot \cos[2\pi f_o (t - \tau)] + \frac{0.01}{2}\{\cos[2\pi f_o (2t - \tau)] + \cos[2\pi f_o \tau]\} \tag{2.21}$$

Equation (2.20) and (2.21) describe the resulting amplitude waveform of the video signal for this example.

A computer simulation for a single target response has been completed to illustrate the effects of an amplitude modulated chirp to the frequency spectrum of the video signal. The simulation uses the amplitude modulation waveform described on the example above. The relevant radar parameters used for the simulation are shown in Table 2-2. The FMCW radar simulation assumes an ideal mixer. The computer simulation was realized using Matlab [25].

Table 2-2: Parameters for a FMCW Radar Simulation using a Chirp Waveform with Added Amplitude Modulation

Parameter	Value	Units
Start Frequency (f_{start})	12	GHz
Stop Frequency (f_{stop})	18	GHz
Chirp Length (T)	5	μs
Roundtrip Delay (τ)	44	ns
Chirp Amplitude Modulation Index	0.1	

The simulation used a single target with a roundtrip delay of 44 μs, which is 4.4% the modulation signal wavelength. Since the roundtrip delay is much shorter than the wavelength of the modulation signal in this case, the amplitude waveform of the video signal may be approximated as shown on equation (2.22).

$$a_{VIDEO} \approx 1.005 + 0.2 \cdot \cos(2\pi f_o t) + 0.005 \cdot \cos[2\pi (2 f_o) t] \tag{2.22}$$

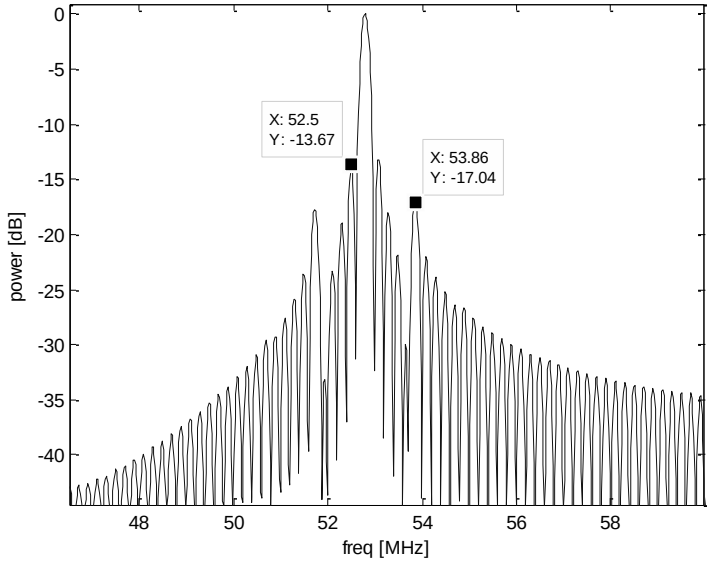

Figure 2-6: Simulation Plot for the Effects on the video signal caused by amplitude modulation on the chirp waveform

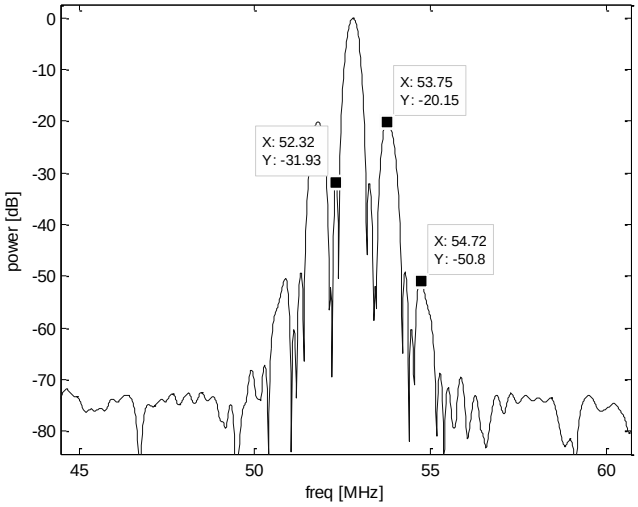

Figure 2-7: Simulation Plot for the Effects on the video signal caused by amplitude modulation on the chirp waveform using a Hanning Weighting

Figure 2-6 and Figure 2-7 show the frequency spectrum of the video signal for the radar parameters described in Table 2-2. The approximated frequency spectrum plots have been computed using the FFT. Figure 2-6 shows the FFT plot of the video signal with no weighting. Figure 2-7 shows the FFT of the same waveform weighted by a Hanning window for sidelobe suppression.

In Figure 2-6, the sidebands caused by the amplitude modulation are at 17 dBc as expected by the first modulation term on equation (2.22). In Figure 2-7, the sidelobes have been suppressed by the amplitude weighting. The sidelobes decreased from 13 dBc to about 32 dBc. However, the sidebands, caused by amplitude modulation, decreased only by about 3 dB. The sidelobe suppression also uncovered the sidebands caused by the second amplitude modulation term on equation (2.22).

For these results, it can be seen that the amplitude modulation of the chirp waveform translates into amplitude modulation at the video signal. This amplitude modulation on the video signal forms sidebands around the target response. Since the video signal on an FMCW radar represents the targets response, these sidebands degrade the target response. For a multi-target FMCW radar, these sidebands may be erroneously interpreted as targets if they are not expected. If the sidebands have been measured on a single target and they are expected, they degrade the dynamic range for close targets. Moreover, the simulations show that the sidelobe suppression by weighting techniques does not significantly reduce the sidebands caused by amplitude modulation.

2.1.2.2 Frequency Modulation

Frequency modulation added at any point on the signal paths also affects the range performance of an FMCW radar. Like amplitude modulation, frequency modulation may get introduced at any stage of the radar paths. If the phase response on any of the components has a linear shape, the component only adds a group delay to the input signal [22]. When the phase response of a component is non-linear over frequency and the input corresponds to a linear chirp, the output signal will have some phase modulation. This phenomenon is also known as dispersion [18]. Since frequency is the rate of change of the phase with time, nonlinear phase modulation also leads to frequency modulation. Moreover, if the chirp is not a perfectly linear frequency modulated waveform, this could also be seen as a form of frequency modulation added to the linear chirp.

Since any stage containing a non-linear phase response will change the frequency linearity of the chirp, the chirp will not have a direct mapping from the frequency response to the sweep time. Therefore the compound effects of the frequency modulation cannot be analyzed with a simple multiplication or addition of frequency waveforms. The equations and analysis required to do so are beyond the scope of this document.

On the other hand, the effects caused by a single source of frequency modulation will be analyzed. The most significant source of frequency modulation is encountered at the chirp generator.

$$f(t) = f_o + \mu \cdot t + f_m(t) \tag{2.23}$$

$$f_m(t) = \beta \cdot f_c \cdot m(t) \tag{2.24}$$

$$x(t) = \cos[2 \cdot \pi \cdot \int (f_o + \mu \cdot t + f_m(t))dt] \tag{2.25}$$

On equation (2.23), $f_m(t)$ is the frequency modulation signal, f_o is the chirp start frequency, t is the time variable, and μ is the chirp rate. The waveform $f_m(t)$ can be further decomposed with the factors shown on equation (2.24). On equation (2.24), β is the frequency modulation index, f_C is the chirp center frequency and m is the frequency modulation signal. Equation (2.25) corresponds to the normalized chirp with frequency modulation.

The video signal then becomes the multiplication of the reference signal with the received signal. Using the analysis assumption that the delay difference at the mixer ports equals the target roundtrip delay, the video signal is described on equation (2.26) after being filtered at the IF stage.

$$x_{video}(t) = \cos\{2 \cdot \pi \cdot [f_o \cdot \tau - \frac{1}{2}\mu \cdot \tau^2 + \mu \cdot \tau \cdot t + \int_{t-\tau}^{t} f_m(t)dt]\} \tag{2.26}$$

On equation (2.26), the last term in the cosine argument corresponds to the resultant phase modulation caused by the chirp frequency modulation. To analyze the effect of the frequency modulation on the chirp to the output video signal, the next example uses a single tone signal with frequency f_X for the frequency modulation signal. The frequency modulation signal *(m)* is described on equation (2.27).

$$m(t) = \cos(2 \cdot \pi \cdot f_X \cdot t) \tag{2.27}$$

$$pm(t) = \int_{t-\tau}^{t} f_m(t)dt = \int_{t-\tau}^{t} \beta \cdot fc \cdot m(t)dt \tag{2.28}$$

$$pm(t) = \frac{\beta \cdot f_c}{2\pi \cdot f_X} \cdot [\sin(2\pi \cdot f_X t) - \sin(2\pi \cdot f_X (t-\tau))] \tag{2.29}$$

Equations (2.28) and (2.29) show the equivalent expression for the phase modulation on the video signal caused by a single tone frequency modulation on the chirp. By calculating the root-mean-square (RMS), the magnitude of the varying phase modulation can be measured.

$$PM_{RMS}(\tau) = \frac{\beta \cdot f_c}{2\pi \cdot f_X} \cdot \sqrt{\frac{1}{1/f_X} \int_0^{1/f_X} [\sin(2\pi \cdot f_X t) - \sin(2\pi \cdot f_X (t-\tau))]^2 dt} \tag{2.30}$$

$$PM_{RMS}(\tau) = \frac{\beta \cdot f_c}{2\pi \cdot f_X} \sqrt{1 - \cos(2 \cdot \pi \cdot f_X \cdot \tau)} \tag{2.31}$$

Equation (2.30) and (2.31) show the RMS expression for the phase modulation on the video signal caused by the single tone frequency modulation on the chirp. This RMS is dependent on the roundtrip delay of the FMCW signal. From equation (2.31), it can be inferred that the RMS peaks at every odd multiple of half the frequency modulation tone period.

For a 5 μs sweep time and a frequency modulation given by a single tone at 1 MHz, the RMS of the phase modulation as a function of the roundtrip delay is plotted and shown in Figure 2-8. The plot in Figure 2-8 shows that the RMS increases as a function of the delay from the origin up to half the period. The RMS also peaks at odd multiples of 0.5 μs, which corresponds to half the period.

This example shows that the phase modulation effects on the video signal are a function of the roundtrip delay where the RMS changes periodically for the given periodic frequency modulation waveform. For non-periodic frequency modulation waveforms, the RMS will continue to increase as the delay increases. This example shows that for applications with large roundtrip delay relative to the chirp time length, the effects caused by frequency modulation added to the chirp waveform translate on a phase modulation of a larger magnitude on the video

signal. This is an important concept to have in mind when designing FMCW chirp generators for large range applications.

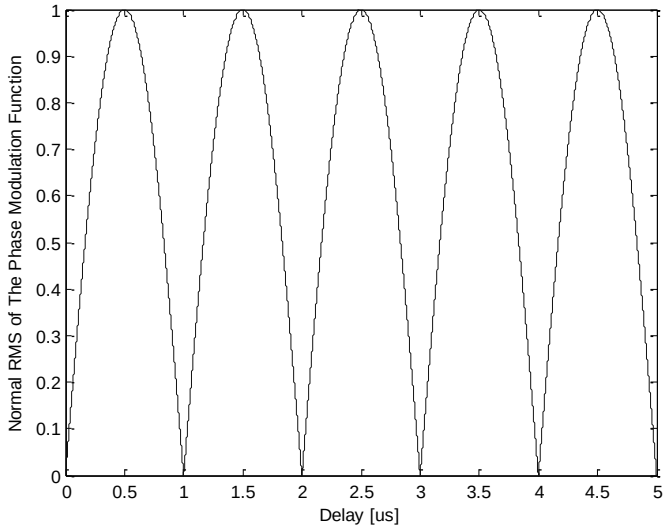

Figure 2-8: Root Mean Squared of The Phase Modulation Function

A computer simulation has been run to see the effects on the video signal caused by frequency modulation on the chirp at the chirp generator stage for various cases. The parameters shared by all cases are shown in Table 2-3. The simulations have been performed using Matlab [25].

Table 2-3: Radar Parameters for a FMCW Radar Simulation using a Chirp Waveform with Added Frequency Modulation

Parameter	Value	Units
Start Frequency (f_{start})	12	GHz
Stop Frequency (f_{stop})	18	GHz
Chirp Length (T)	5	μs

For all the simulated cases, the frequency modulation signal is a single tone with a carrier frequency of 1 MHz. For a first case, the chirp has a frequency modulation with index (β) of

5×10^{-5}. This first case has been simulated with a target roundtrip delay of 250 ns, which equals a quarter of the period of the frequency modulation waveform. Figure 2-9 is a plot of the resulting video signal frequency spectrum for the first case simulation. The plot shows sidebands at 1 MHz apart from the mainlobe. The sidebands which correspond to the frequency modulation have a power of about 5.4 dBc. The example uses a delay of only a quarter of the period of the frequency modulation signal and an FM index of only 5×10^{-5} and the effects on the resolution performance of the video signal are already unsatisfactory for most multiple-target applications.

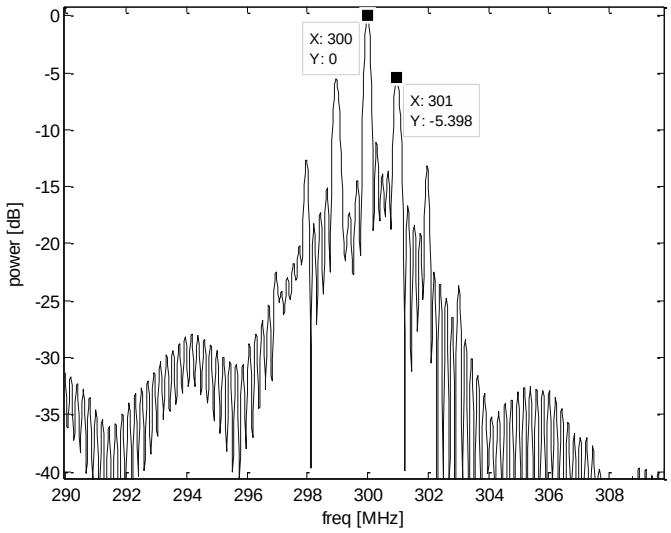

Figure 2-9: Video Signal Frequency Spectrum for Case 1

For a second case, the simulation uses a roundtrip delay of 500 ns, which is equivalent to half the period of the modulating signal. As it has been shown, this is the delay for which the effects caused by the phase modulation are maximized. This second case uses the same modulation index as the first case.

Figure 2-10 shows the frequency spectrum of the video signal for the second case. The power of the sidebands from the frequency modulation has been increased up to about 0.8 dBc.

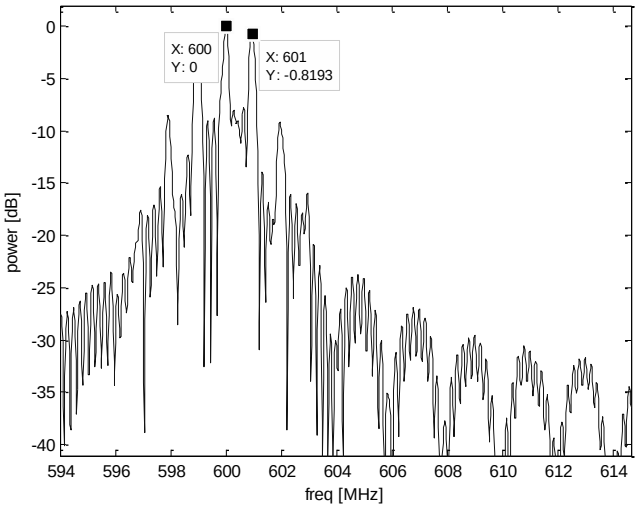

Figure 2-10: Video Signal Frequency Spectrum for Case 2

The frequency spectrum plot in Figure 2-10 uses no weighting in time to improve sidelobe performance. Figure 2-11 shows the frequency spectrum for case 2 using a Hanning window on the video waveform. The plot shows that windowing techniques may reduce the power on the sidelobes, but it has little effect on the sidebands caused by frequency modulation. This is an example of how the effects of the non-linear behavior of the chirp may not be improved with standard sidelobe reduction techniques.

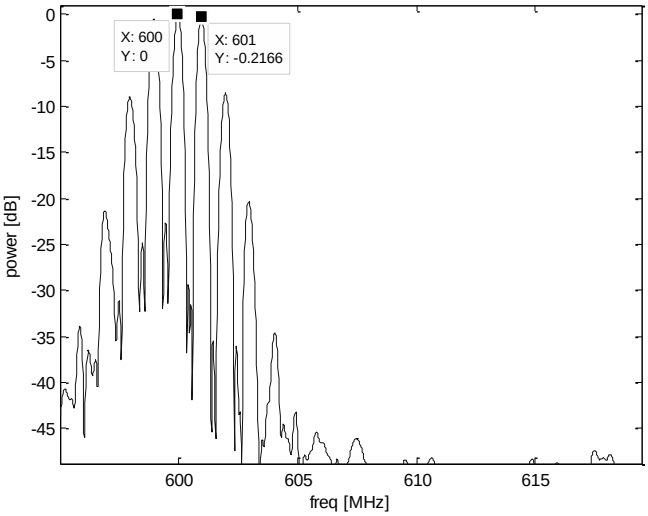

Figure 2-11: Video Signal Frequency Spectrum for Case 2 with Windowing for Sidelobe Suppression

For the applications we are interested in, the delay is nowhere near half the period of the frequency modulation waveform. These two simulation cases are illustrated to show how the phase modulation effects on the video signal worsen as the roundtrip delay increases. Although the previous examples used fairly long relative delays, the modulation index was very small.

A third case considers a roundtrip delay of only 50 ns which corresponds to a twentieth of the period. The frequency modulation index in this case is 5×10^{-4}. A plot of the video signal for this case is shown in Figure 2-12. This example uses a fairly small relative delay and a very small frequency modulation index. This example shows that the video signal is very sensitive to the effects of frequency modulation added to the chirp at the generation point.

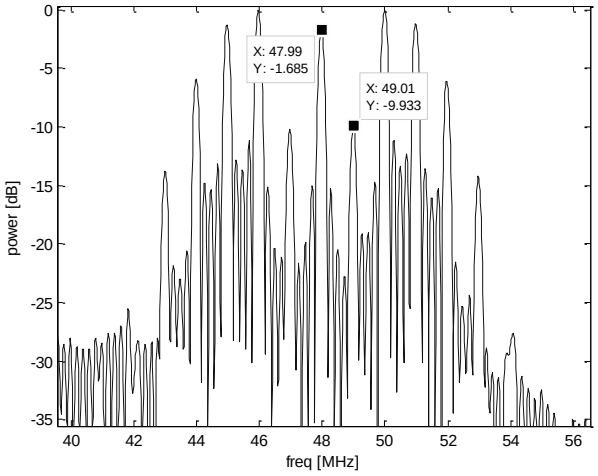

Figure 2-12: Video Signal Frequency Spectrum for Case 3

From these examples it has been seen that frequency modulation added to the chirp waveform degrades the target range response performance. As in the amplitude modulation case, sidebands close to the mainlobe degrade the range resolution and dynamic range for close targets. Moreover, the simulations showed that standard sidelobe suppression techniques using amplitude weighting does not have a significant effect on these sidebands.

2.1.2.3 Amplitude and Frequency Modulation Treatment

As explained on the previous sections, amplitude and frequency modulation added to the chirp waveform at any point on the signal paths can greatly degrade the range resolution performance of FMCW radar systems. In addition, it has been shown that the effects caused by the frequency modulation on the chirp increase with the roundtrip delay. Thus, the design of FMCW radars with nominal ranges that correspond to large roundtrip delays relative to the chirp length should have more severe linearity requirements on the chirp waveform.

Amplitude modulation can be improved by using Variable Gain Amplifiers (VGAs). By measuring the resultant amplitude waveform at each path of the FMCW radar, the effects of amplitude modulation can be compensated using VGAs. By forcing an amplitude modulation with the inverse amplitude waveform of each path, the VGAs would compensate for the amplitude effects on each path.

The frequency and amplitude modulations may also be improved with digital signal processing (DSP). DSP techniques can be applied both in real-time and post processing. If there are measuring tools available to digitize the chirp waveform for each FMCW path, both the resulting amplitude and frequency modulation on the video signal may be estimated at any delay. This information can be used to correct the frequency and amplitude on the video signal. Unfortunately, digitizing tools for wideband radars are expensive and may not be available. For this case, the video signal can be digitized and used for processing. By measuring a single target response at the nominal delay, both the resulting amplitude and frequency modulation on the video signal can be extracted for the nominal delay. Then, the amplitude and frequency corrections can be applied on the data. Using the video signal to correct for modulation effects is not optimal due to the range dependent nature of the modulations.

Considering the drawbacks of the signal processing techniques and their limitations, the quality of the data of FMCW radar systems depends to a great extent on the hardware performance.

2.1.3 FMCW Waveform Generation and Frequency Synthesizers

FMCW waveforms generators use some kind of frequency synthesis which may include digital, analog or both techniques. This section describes direct frequency synthesis methods and synthesis methods requiring a voltage controlled oscillator (VCO).

2.1.3.1 Direct Analog Synthesis

A Direct Analog Synthesizer (DAS) generates a coherent wideband signal using only analog devices and no closed loop operations. A DAS uses a stable source such as a crystal oscillator and a variety of components for the application of arithmetic operations in the frequency domain of the source signal. A DAS may include a crystal oscillator, comb generators, frequency multipliers, frequency dividers, frequency mixers and filters [26].

By applying frequency operations to the source signal, very wideband frequency waveforms can be obtained. However, depending performance of the filters used, the frequency operations may add spurious noise to the signal. Thus, the synthesizer will be limited to a number of operations for a given spur level requirement. Since the DAS usually requires many components for the frequency operations, this type of synthesizer is often costly, bulky and has high power requirements [26].

2.1.3.2. Direct Digital Synthesis

A Direct Digital Synthesizer uses digital data processing blocks to generate a frequency or phase tunable output signal. The DDS has a phase accumulator, which is basically a digital ramp generator implemented with an address counter. The digital output of the address counter represents the current phase. On a frequency-tunable DDS, the update rate of the counter is controlled by a frequency tuning word that may vary with time. The tuning word defines the frequency of the output signal. The output of the phase accumulator then gets fed to a phase-to-

amplitude converter. Finally, a Digital-to-Analog converter takes the amplitude data to generate the analog signal [26][27].

Since the Nyquist Theorem indicates that at least two samples per cycle are required to reconstruct a waveform, the sampling rate should be at least twice that of the DDS output bandwidth. The DDS output signal spectrum contains images of the positive and negative frequency components of the fundamental spaced by multiples of the sampling frequency. The images that correspond to the negative component of the fundamental are considered the odd numbered images whereas the images from the positive component of the fundamental are the even numbered images. Thus, the first image corresponds to the first image of the negative component of the fundamental. The frequency spacing between these images becomes half of the sampling rate or the Nyquist Bandwidth. Then, a reconstruction filter may be used to filter frequencies on any of the images of the fundamental. Moreover, the power amplitude of the spectrum harmonics follows a sinc function envelope with nulls at multiples of the sampling rate. The main drawback of using frequencies on one of the images is the amount of attenuation caused by the sinc function envelope response [27].

DDS synthesizers have many advantages with respect to other synthesizers. DDS systems allow a high frequency tuning resolution. The digital nature of a DDS makes it independent of aging and temperature drift, common on analog devices. However, the DDS signal output bandwidth is limited by the reference clock. DDS systems are considered a very good choice for chirp generators with bandwidth lower than half the sampling rate [27].

As of the October 2011, the digital to analog data converters with highest sampling rate available in the market are the MAX5881, the AD9739A and the DAC5670-SP with 4.3 Giga Samples per Second (GSPS), 2.5 GSPS and 2.4 GSPS respectively. These three products are manufactured by Maxim Integrated Products, Analog Devices Inc. and Texas Instruments Inc, respectively. Thus, the maximum bandwidth attained for a synthesizer with available data converters is less than 2.15 GHz.

2.1.3.3 Phase Lock Loops and other VCO based Frequency Synthesizers

As mentioned previously, digital synthesize is mainly limited by bandwidth and direct analog synthesis by its spurious performance, power requirements and cost. As alternative to these techniques, a common indirect wideband synthesizer uses a wideband voltage controlled oscillator on a frequency control loop also known as a Phase Lock Loop (PLL). A PLL-based synthesizer uses a direct synthesizer as the reference signal. A description of the PLL system and its components is given in Section 2.2.

An FMCW signal with the desired frequency waveform can be implemented by controlling the tuning voltage of the VCO, as will be discussed in Section 2.2.2. The tuning characteristic is the curve that describes the mapping between the tuning voltage and the output frequency. Since this relationship is nonlinear, a ramp voltage input will not output a linear frequency modulated output as it is required for chirp-based FMCW radars. Then, either an open loop or a closed loop system should be used to control the tuning voltage to output the required waveform.

Different open loop techniques have been implemented to linearize the VCO output depending on the resources available at the time.

Burke P.E. implemented an open loop VCO linearization technique based on a circuit realization of a pre-distorted voltage [28]. The system uses a third order polynomial function generator based on a voltage controlled voltage ramp generator. The ramp slope, which corresponds to the first polynomial coefficient, is controlled both externally and by a feedback signal. The quadratic and cubic terms are outputted by a quadratic and a cubic generator respectively. These two terms are added to the ramp, where the second and third polynomial coefficients are given by the potentiometers used for the adder. Thus, the system works as a polynomial regression system that tries to generate the required non-linear tuning voltage to match that of the inverse function of the tuning characteristic. The system also uses a PLL synchronized to the chirp repetition rate to maintain a coherent output.

Since wideband voltage controlled oscillators have tuning characteristics with several small variations, a polynomial fitting that matches exactly the inverse function would require

several coefficients. Moreover, the number of coefficients that can be implemented is limited by the circuit and coefficient calibration complexity.

An example of an earlier open loop linearization technique implemented at the CReSIS is described on [29]. The linearization technique uses a frequency counter to measure the output frequency to discrete input voltages. The measured relationship between voltage and output frequency of the VCO is then used to find the inverse function. Lastly, the inverse function is directly applied to the VCO [29]. This technique has many drawbacks. First, in order to account for small variations in the VCO tuning curve, the measurement should be made with very small voltage steps. Since many measurement repetitions are taken and averaged to account for time variations, it would require a very long time to take all the necessary measurements. Moreover, this technique takes static measurements of the output frequency. However, the tuning characteristic of the VCO for static voltages may not be the same as that for a ramp input voltage. The tuning characteristic may even vary for different chirp rates.

Closed loop techniques have also been implemented to linearize the output frequency of the voltage controlled oscillator. By using a phase lock loop, as explained previously, the output frequency of the VCO may follow a multiple of the reference frequency. A PLL based chirp generator previously developed at CReSIS is described on [30]. This system uses a third order type 2 PLL. The type 2 nature of the PLL implemented with a differential amplifier makes it possible to achieve all the required voltage levels for the designed amplifier bandwidth. A differential amplifier is used for error compensation as well as for driving the VCO. This technique was demonstrated as part of a microwave altimeter operating with 1 GHz of bandwidth. The performance of the chirp generator using this implementation suffered from high range sidelobes for bandwidths larger than 1 GHz. Since not enough considerations were taken to improve the tracking performance of the synthesizer, the PLL designed was not able to compensate for the VCO nonlinearity using higher chirp bandwidths.

2.2 PHASE LOCK LOOP OVERVIEW

This section discusses the analysis of phase lock loops using linear system techniques. It also describes the functionality of the main PLL components as to determine their system response.

2.2.1 PLL Analysis as a Linear System

A Phase Lock Loop (PLL) is a Frequency and Phase control system. Linear control system techniques can be used to analyze linear time invariant control systems. Each linear system is represented with a transfer function, which is the Laplace transform of the output to input ratio [31]. Since the VCO has a non-linear input-output relationship, as will be explained, a PLL system may be considered a non-linear control system. However, it can be approximated to be linear over a narrow bandwidth of the VCO. Also, the response of most devices will vary with time due to temperature and aging. These changes will not be significant and will be neglected for the analysis. Applying these linear approximations, the PLL may be analyzed using linear control system theory.

A PLL is composed of essentially three components: the phase detector, the loop filter and the Voltage controlled Oscillator (VCO). Frequency synthesizers based on PLLs use a frequency divider in the feedback path to output a multiple of the reference frequency. Figure 2-13 shows a linear system block diagram of a simple PLL.

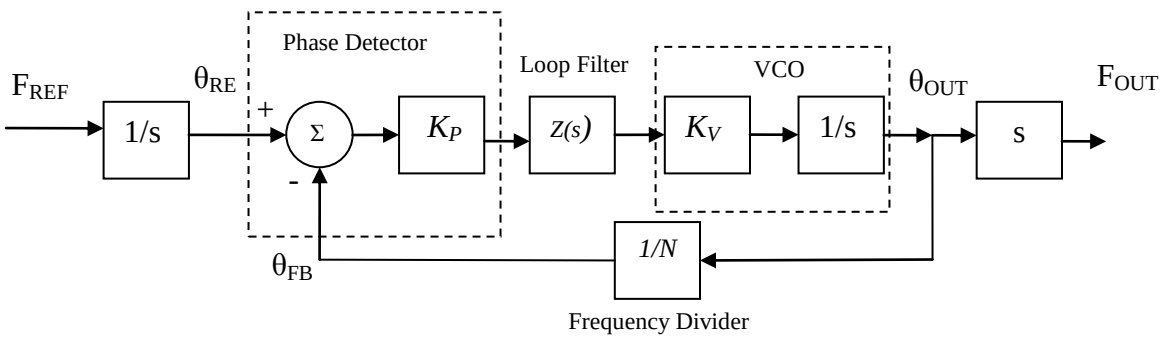

Figure 2-13: Block Diagram of PLL Transfer Function

When the PLL is in the lock state, the output phase tracks the input phase. Either a change in the input phase or a change in the output phase is sensed by the phase detector. The phase detector outputs a signal which average is proportional to the phase difference between the input signal and the feedback signal. The phase detector gain is symbolized by K_P. The functionality of the phase detector is further explained in Section 2.2.2.2.

K_V represents the voltage-to-frequency conversion gain of the VCO, also known as the frequency sensitivity of the VCO. The frequency divider block shows the division factor equal to N. *Z(s)* corresponds to the transfer function of the PLL compensator, also known as the PLL loop filter. The use of the letter Z for the loop filter transfer function comes from the fact that the typical charge pump PLLs use trans-impedance loop filters. However, the letter Z will be used throughout this document regardless the type of input signal of the loop filter.

Equations (2.32) through (2.35) show the forward path *A(s)*, feedback path *B(s)*, open loop *G(s)* and closed loop *H(s)* transfer functions for the PLL described in Figure 2-13.

$$A(s) = \frac{K_P \cdot Z(s) \cdot K_V}{s} \tag{2.32}$$

$$B(s) = \frac{1}{N} \tag{2.33}$$

$$G(s) = A(s)B(s) = \frac{K_P \cdot Z(s) \cdot K_V}{s \cdot N} \tag{2.34}$$

$$H(s) = \frac{A(s)}{1 + A(s)B(s)} = \frac{\frac{K_P \cdot Z(s) \cdot K_V}{s}}{1 + \frac{K_P \cdot Z(s) \cdot K_V}{s \cdot N}} = N \cdot \frac{\frac{K_P \cdot Z(s) \cdot K_V}{N}}{s + \frac{K_P \cdot Z(s) \cdot K_V}{N}} \tag{2.35}$$

The open loop gain transfer function is the product of the forward and feedback paths transfer functions [31]. The closed loop transfer function is then solved to the standard negative feedback loop equation shown on equation (2.35) [31][32]. An effective closed loop control system has more poles than zeros and its frequency response resembles that of a low-pass filter [31][33]. By inspection of equation (2.35), the closed loop transfer function of the PLL has a

gain equal to the division factor (N) over its pass band. The PLL impulse response is the Laplace inverse transform of the closed loop transfer function. The step, ramp and parabola responses may also be calculated by integrating the designed closed loop transfer function. The closed loop transfer function may be designed to fit the transfer function of a specific function. For instance, a Gaussian response is used to design a fast settling type 2 PLL on [34].

The linear approximation used to apply linear system analysis techniques to PLLs assumes a constant value for the VCO sensitivity (K_V). This is not the case for wideband applications. Therefore, the time performance of the PLL will also vary with respect to the output frequency. Thus, the PLL should be designed such that an acceptable time response is maintained for all possible values of K_V.

2.2.1.1 Type and Order of a PLLs

The type of a transfer function refers to the number of integrators or poles at the origin. In the PLL terminology, the type of the PLL refers to the type of the open loop transfer function and not the closed loop transfer function [35].

The order of a transfer function refers to the number of poles. Similar to the type, the order of the PLL is the order of the open loop transfer function.

2.2.1.2 Transient Response and Stability of PLLs

Instability in a control system occurs when the open loop transfer function equals negative 1 [31]. This means that the open loop gain equals 0 dB at -180 degrees. Even though the open loop does not reach this point, there are parameters that measure the degree of stability. The phase margin indicates the difference between the open loop phase and -180 degrees when the gain crosses 0 dB. Similarly, the gain margin is the gain of the open loop at -180 degrees [31]. The former occurs at the gain crossover frequency and the latter at the phase crossover

frequency. The gain crossover frequency will be referred to as only the crossover frequency on this document.

Designs where the PLL open loop crosses the phase crossover frequency more than once are rarely found. According to the Bode stability criterion, the system is stable if the open loop gain is less than 0 dB over the phase crossover frequency [31]. Thus, the Bode stability criterion can be used to claim stability on a PLL.

Moreover, the phase margin is related to the transient response. The phase margin provides an estimate of the damping of the system. For second order systems it is directly related to the damping factor. For other order systems, it is just an estimate. In general, a phase margin larger than 45 degrees indicates an over-damped system. Likewise, a phase margin smaller than 45 indicates an under-damped system. A transient refers to a sudden change in the system input or within the system. An under-damped system overshoots when there is a transient creating an error peak on the output. An over-damped system reacts slowly to a transient causing also an error on the output. Moreover, a heavily under-damped system, equivalent to a small phase margin, may become unstable with a small change in the system open loop phase.

The phase margin will be used throughout this document to provide a measure of stability and transient behavior.

2.2.1.3 Steady State Errors on PLLs

Consider the control system described on the block diagram in figure 2.14. The diagram shows the a simple control loop with a forward path system *(A)*, a feedback path system *(B)*, an input signal *(X)*, an output signal *(Y)* and an error signal *(E)*. Equations (2.36) and (2.37) describe the error signal Laplace Transform.

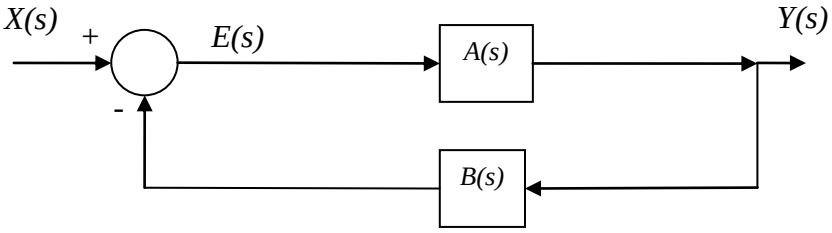

Figure 2-14: Simple Control System Block Diagram Showing Error Signal

$$E(s) = X - YB = X - EAB \tag{2.36}$$

$$E(s) = \frac{X}{1 + AB} \tag{2.37}$$

$$e_{ss} = \lim_{t \to \infty} e(t) = \lim_{s \to 0} s \cdot E(s) \tag{2.38}$$

$$e_{ss} = \lim_{s \to 0} s \cdot \frac{X}{1 + AB} \tag{2.39}$$

By the final value theorem, the steady state error can be determined from its Laplace transform using the relationship shown on equations (2.38) and (2.39). For this simple control loop, the steady state error depends on the input signal and the open loop transfer function for the limit of the function as the variable ‘s’ approaches zero. Thus, the number of zeros and poles at the origin on both the input signal and the open loop transfer function define whether the steady state error is a constant, zero or approaches infinity.

Since the number of integrators on the open loop transfer function of the PLL relates to its type, the steady state error can be classified for PLL of different types. Likewise, the steady state error can be classified for different types of input signals. The steady state errors for each relevant case have been computed and are shown in Table 2-4. Since, the constant expressions depend on the expression of the loop filter, which can take many forms, it is not explicitly described in Table 2-4.

Table 2-4: Steady State Error for Different Types of PLLs

	Step	Ramp	Parabola
Type 1	0	Constant	Infinite
Type 2	0	0	Constant
Type 3	0	0	0

As mentioned earlier, a PLL is a phase control system when it is on the lock state. Thus, a parabola in the phase input corresponds to a ramp in input frequency. This is the type of frequency input that this document is interested in. For this case, the analysis dictates that a type 3 is the optimal choice for a steady state error equal to zero. However, a constant error in the phase will not affect the linearity of the waveform. Thus, a type 2 PLL would suffice.

Moreover, type 1 PLLs have attractive properties when implementing wideband PLLs. Wideband PLLs are described on the next section. For this reasons, a control technique that overcomes the steady state error issue of type 1 PLL needs to be used.

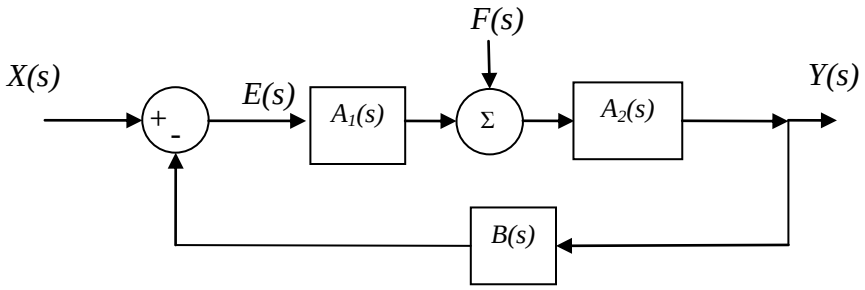

Figure 2-15: Control Loop with Added Signal for Type 1 Steady State Error Improvement

Figure 2-15 illustrates a block diagram of a control loop with an external signal *(F)* being added to the forward path. The forward path has been divided in two systems: $A_1(s)$ and $A_2(s)$. For the PLL, the first block on the forward path will contain the phase detector gain and the second block will contain the VCO gain. The loop filter may be found on any of the two. Equations (2.40) and (2.41) illustrate the Laplace transform of the error signal for the system depicted in Figure 2-15.

$$E(s) = X - YB = X - (EA_1 + F)A_2B \tag{2.40}$$

$$E(s) = \frac{X - FA_2B}{1 + A_1A_2B} \tag{2.41}$$

$$X(s) = \frac{1}{2}\mu \cdot \frac{2!}{s^3} = \frac{\mu}{s^3} \tag{2.42}$$

$$e_{ss} = \lim_{s \to 0} s \cdot \frac{\frac{\mu}{s^3} - FA_2B}{1 + A_1A_2B} \tag{2.43}$$

For simplicity, the frequency ramp or phase parabola signal is assumed to have initial phase and initial frequency equal to zero. Equation (2.42) describes the input phase parabola signal in the Laplace domain, where μ is the frequency ramp rate or chirp rate.

Equation (2.43) shows the steady state error expression for this control loop in terms of the Laplace transfer functions using the final value theorem. Since the VCO transfer function is a factor in A_2, both summand terms in the denominator and the numerator that contain this function will have at least one integrator.

Considering a type 1 PLL with the only open loop integrator in the A_2 function, equation (2.43) has been evaluated for different number of integrators in the external signal. From this analysis, it has been found that the steady state error only becomes zero when the second summand on the numerator equals the inverse of the first summand. Since A_2 already contains an integrator, the external signal needs to be a ramp. The external signal ramp rate needs to be selected so that the term FA_2B becomes a frequency ramp with exactly the same rate as the input frequency ramp.

Thus, for type 1 PLLs an external signal has to be applied to compensate for the phase parabola term on the input phase signal. As pointed out in Table 2-4, the type 1 PLL output signal will approach a finite value for the phase ramp and the phase step terms on the input.

2.2.1.4 Narrow Loop Bandwidth and Wide Loop Bandwidth PLLs

As mentioned, the frequency response of an effective PLL is that of a low pass filter. The loop bandwidth of the PLL is a critical parameter for its performance [33]. In fact, wide loop bandwidth and narrow loop bandwidth PLLs are designed for different purposes [33]. The narrow loop bandwidth PLLs are used when the expected value of the reference frequency does not change significantly or does not change at all [33]. The PLL then works as a filter that attenuates the high frequency noise on the reference signal. Phase locked local oscillators use this type of PLL.

On the other hand, if there are high frequency fluctuations on the oscillator output, a wide loop bandwidth PLL is desired to quickly compensate for these. For instance, an oscillator may have remarkable properties that are desired for a specific design such as wideband or high power output, however, it may suffers from poor stability of frequency or other issues [33]. For this case a wide loop bandwidth PLL should be used. Thus, wide loop bandwidth PLLs have the ability to quickly compensate changes that would disturb the system. This kind of PLL has desirable capabilities when there is need to track a moving reference or compensate for disturbances on the loop. The tracking ability of wideband PLLs is described further in Section 2.3.

2.2.2 PLL Components Overview

2.2.2.1 Voltage Controlled Oscillator

A voltage controlled oscillator has an output frequency that can be tuned by the input voltage, as the name implies.

In simple terms, any oscillator can be constructed with a resonator in a closed loop with a negative resistance. Equation (2.44) shows the transfer function of a simple positive feedback closed loop system, where A is the forward gain and β is the feedback gain. If the product of both has the value of 1 at a particular frequency, the combination of the forward and feedback path circuits form a resonator. A lossless resonator will continually oscillate when the closed loop is exited at the resonant frequency. However, real devices have loss due to positive resistance. Then, an amplifying device should be used to maintain oscillation. Thus, the amplifier is said to have negative resistance at the resonant frequency [36].

$$H(j\omega) = \frac{A(j\omega)}{1 - A\beta(j\omega)} \tag{2.44}$$

One type of resonator can be constructed with the combination of capacitive and inductive devices, where the resonant frequency is dependent of the product of both. The voltage controlled oscillator uses a varactor diode as part of the resonator. A varactor diode has a capacitance that is tunable with input voltage. This way the resonant frequency becomes tunable with input voltage [37].

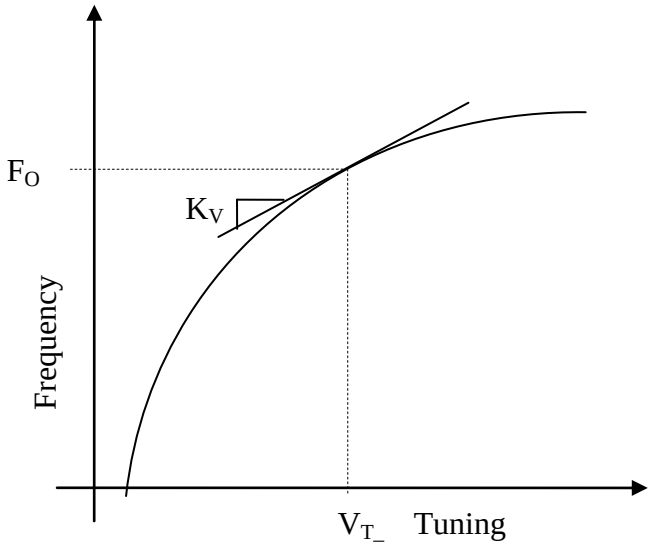

Figure 2-16: Tuning Curve of a Voltage Controlled Oscillator

Figure 2-16 shows a typical plot of the relationship between the tuning voltage and the output frequency of a VCO with positive tuning voltage. The relationship between the output frequency and the tuning voltage is also known as the tuning characteristic or tuning curve. VCOs inherently have a non-linear tuning characteristic. This limits the frequency output range. The VCO output frequency varies with temperature and aging. This long term instability is usually measured in parts-per-million (ppm). In addition, there exits short term instabilities which make the output frequency vary randomly around the expected carrier. This type of instability, also known as phase noise, is measured by the average power of the signal at that frequency. The phase noise then is defined as the power with respect of the carrier at a frequency offset from the carrier in dBc/Hz. Fluctuation in the output frequency may also be caused by the variations in both the load coupled to the VCO and the voltage supply. These two effects are called frequency pulling and frequency pushing respectively [38].

When designing a PLL the slope of the tuning curve (Kv) is used as a constant gain in the linear system analysis by applying a linear approximation valid for very narrow bandwidths. However, for wideband applications the PLL design should consider the large variations in K_V.

K_V is also known as the tuning sensitivity. Also, the relationship between the tuning sensitivity and the output frequency is called the tuning sensitivity curve [35].

2.2.2.2 Phase Detector

A phase detector is a device which output can be related to the difference between the phases of the two inputs. Phase detectors are used in phase lock loops to sense the difference in phase between the reference and the feedback signals [32].

The three most typical phase detectors are the double balanced mixer, the XOR gate and the phase-frequency detector. The first two types of phase detectors mentioned have a limited lock range. Thus, they are not convenient for wideband implementations using PLLs. The description of these types of phase detectors can be found on [32].

A Phase-Frequency detector, the third type of phase detector previously mentioned, is a device specially designed for phase lock loops where both the phase and frequency need to be detected and corrected for [35]. Figure 2-17 illustrates the basic functionality of a phase frequency detector. Both signals are connected to the clock ports of the rising edge flip-flops. A rising edge on any of the two signals stores a logic '1' on the corresponding flip-flop. If both flip-flops have a logic '1' stored on the output, then the AND gate outputs a logic '1'. The output of the AND gate resets the stored values on the flip flops to logic '0' [35].

Figure 2-18.a shows the UP and DOWN output waveforms for the case when both input signals have equal frequency but signal 1 leads signal 2. The output waveform of UP has a duty cycle proportional to the phase difference, whereas the DOWN output shows a zero duty cycle. For the case when signal 1 lags signal 2, the output waveforms would be swapped. Figure 2.18.b shows the output of UP and DOWN waveforms for the case when signal 1 has higher frequency than signal 2. For this case the UP waveform has a duty cycle proportional to the difference in frequency. The way the phase-frequency detector is implemented is by subtracting the two output waveforms. For the case when both signals have the same phase and frequency, a glitch forms for both outputs at every cycle. This glitch corresponds to the difference in the delay path for the two flip-flop outputs. This issue is known as the dead-zone phenomenon. A dead-zone elimination circuitry is added to phase-frequency detectors to solve this problem [39].

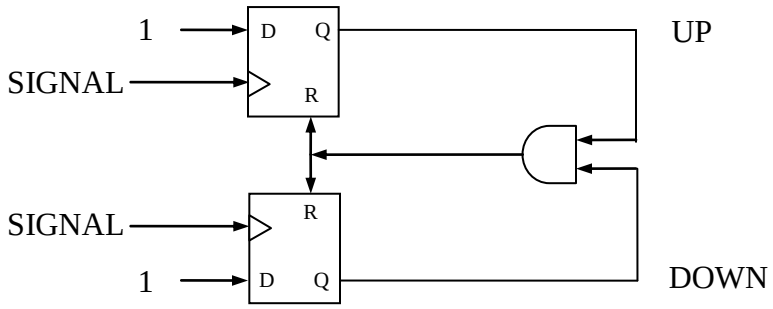

Figure 2-17: Phase Frequency Detector Typical Digital Circuit

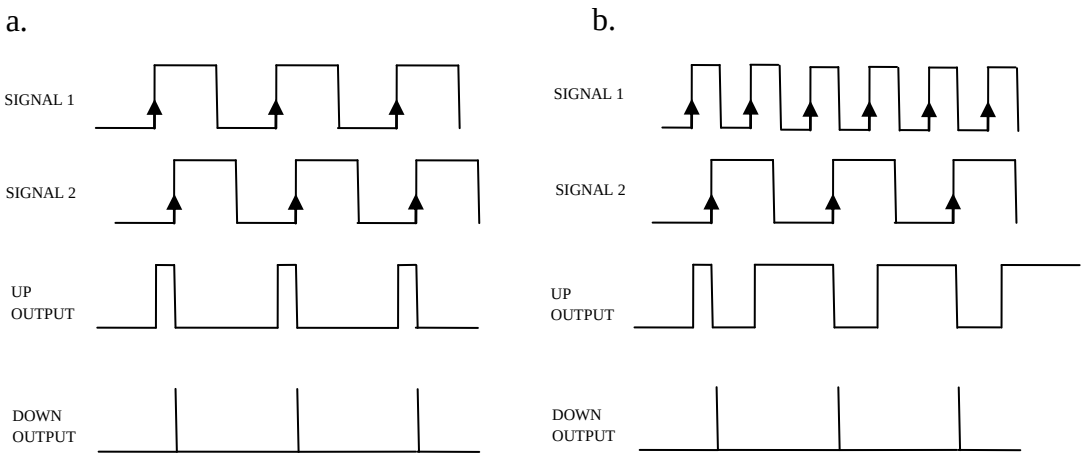

Figure 2-18: a. Phase Frequency Detector Waveforms for the two Cases: a. Phase Difference Only. b. Phase and Frequency Difference

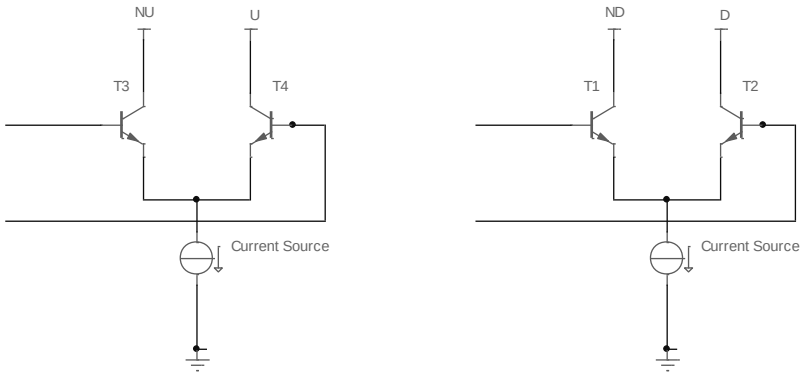

Figure 2-19: Charge Pump Circuits for UP and DOWN outputs

Modern Phase-Frequency detectors have a charge pump stage coupled to the digital outputs of the flip-flops. Both the regular output and its complement (not shown in Figure 2-17) of the flip-flops are used to drive the transistors shown in Figure 2-19. The charge pump then converts the digital voltage signal to a current signal. Usually, there is a small capacitance associated to these outputs that works as an integrator on the output signal. Figure 2-20 illustrates this effect.

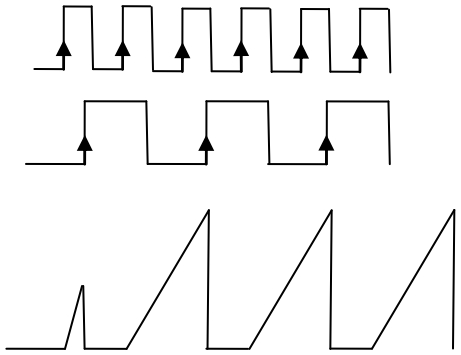

Figure 2-20: Phase Frequency Detector Output using Integrator

The charge pump output may have a pull-up or pull-down resistor to convert back the output to a voltage output. It can also have a single ended output or a differential output.

The proportionally factor that relates the phase difference to the output signal is called K_P. Depending of the output signal type, it can have units of voltage per radians or current per

radians. It is usually given in terms of 2π radians because the 2π factor cancels out when K_V is given in Hertz per volt and not radians per volt [39].

The phase frequency detector has two modes of operation. If there is a difference in frequency between the two signals, it provides an output proportional to the difference in frequency. Otherwise, the detector output a signal proportional to the difference in phase. If a PLL is designed using a phase frequency detector, it is tracking either the frequency or the phase of the reference at some point. The PLL is said to be phase-locked if it is tracking the phase of the reference signal.

2.2.2.3 Frequency Divider

In PLL based frequency synthesizers, the output frequency is usually higher than the reference frequency. To compensate for this gain in the PLL transfer function, a frequency divider is used on the feedback path. A frequency divider scales down its input frequency by a divider factor.

A digital frequency divider may be implemented with ripple counters. A simple divider consists of a J-K flip flop, where the J and K inputs are set to logic '1' and the input is connected to the clock [32]. The output changes its state at every rising edge. Therefore, the output digital waveform has a frequency that is half the frequency of the input digital waveform. Frequency dividers with higher division factors multiples of 2 can be accomplished by cascading more than one of these circuits. This compound circuit is known as a ripple counter.

In order to implement frequency dividers with odd division factors and fractional division factors, more advanced techniques need to be used. A description of these can be found on [32].

2.2.2.4 Loop Filter

The Loop Filter of the phase locked loop has two main objectives: to filter the high frequency spurs on the output of the phase detector and to compensate the open loop transfer function to achieve the given transient response requirements. Because of the first task of the loop filter, it is usually designed using frequency response techniques [39]. Thus, the PLL time response and stability performance are also achieved using frequency response design techniques. The compensation provided by the loop filter to the open loop transfer function improve the high frequency noise attenuation, may improve the steady state error and modifies the phase margin for a designed transient response.

For the reasons described above, all loop filters are essentially lag compensators. On the magnitude response of the open loop transfer function, the lag compensator attenuates the high frequency magnitude compared to the low frequency magnitude. On the phase response of the open loop, the lag compensator lags the phase over a desired region. A simple lag compensator can be achieved with one pole. However, an additional zero at a higher frequency than the pole is added to prevent the system on becoming unstable or having a small phase margin. One or more poles may be added at higher frequencies than the frequency location of the zero. For this case, the loop filter becomes a lag-lead compensator. This compensator can be used to adjust the phase margin with the second pole when the zero has been already set for other purposes. For instance, the zero may be used to set the crossover frequency. Because the lag-lead compensator can have many poles beyond the zero, it has a better attenuation of high frequencies than the pole-zero lag compensator. This is an attractive feature for loop filter designs for attenuating high frequency noise and spurious signals.

PLL loop filter transfer functions differ with the type of the PLL. The typical type 1 PLL loop filter is a lag compensator with no zeros. Since the type 1 PLL loop filter has no integrators, this kind of loop filter has the transfer function of a low pass filter with flat band pass gain. The main advantage of this type of loop filter is that its transient response has no overshoots. Thus, it adds no peak errors. Moreover, it has faster settling capability. These properties make this kind of PLL very desirable for fast tracking applications. The main disadvantage of this kind of loop filter is that it does not provide good steady state error for frequency ramp responses. However, it

has been shown in section 2.2.1.3 that this can be solved with control techniques. In contrast to this typical type 1 PLL, the type 1 PLL loop filter with zeros may have a peaking transient response [39]. This type of loop filter is not as fast as the typical type 1 PLL loop filter. It does not have an optimum transient error as the typical type 1 PLL loop filter. However, the zero provides an additional degree of freedom to set the crossover frequency or modify the phase margin [40]. Type 1 PLL loop filters can be design to achieve a performance close to that of the typical type 1 PLL and at the same time being able to set both the phase margin and the crossover frequency adequately. Type 1 PLL loop filters are known as averaging loop filters, because they provide the average of the output of the phase detector.

Type 2 PLL loop filters have one integrator. This feature results in a zero steady state error for a frequency input step and a constant steady state error for an frequency input ramp. Since this kind of steady state performance can be achieved without any additional compensation, this type of PLL loop filter is used for many simple applications. The main disadvantage of this type of PLL loop filter is that it provides the PLL with higher transient errors and a slower transient response than the type 1 PLL. This type of loop filter is also known as an integrator loop filter.

A type 3 PLL has zero phase parabola steady state error. This is beneficial when zero phase difference between the input and output of the PLL is desired. The loop filter required for this type of PLL has great complexity [33]. Moreover, type 2 and type 3 PLLs have about the same phase transient error for a frequency ramp input [33].

As mentioned in section 2.2.2.2, the phase detector output may be a voltage signal or a current signal. If the loop filter is directly connected to the output of the phase detector, its input signal will be of the same type as that of the output signal of the phase detector. Assuming the output of the loop filter will be connected to a device that expects a voltage signal, such as a VCO, the loop filter transfer function describes either a voltage filter or a trans-impedance filter.

The loop filter may be implemented using only passive devices or using a combination of active and passive devices. The former implementation refers to passive loop filters and the latter to active loop filters. Voltage passive loop filters are limited to type 1 PLL loop filters. In contrast, type 2 PLL trans-impedance passive loop filters can be implemented. The main limitation on passive loop filters is that they cannot output larger voltages than the ones provided

by the phase detector output. The phase detector output voltage is usually low compared to the VCO required voltage. Thus, an additional amplifier or level shifter may be needed to reach the required voltages.

Active loop filters can be implemented either as type 1 PLL loop filters or as type 2 PLL loop filters and they can have either a current or a voltage input signal. Active loop filters have the main advantage of adding gain to the input signal regardless of the kind of signal. The high open loop gain at low frequencies allows the implementation of an almost ideal type 2 loop filter. Also, active loop filters using a differential input can be implemented to combine a phase detector differential output. Additionally, active loop filters can output large voltages which are usually required at the VCO input. On the other hand, active loop filters add noise, distortion and have limited small signal bandwidth. Active loop filters are typically implemented with operational amplifiers (opamps). These devices have a limited slew rate, which defines the maximum large signal bandwidth without distortion. Moreover, the small signal bandwidth of opamps is gain dependant. This means that a wideband active loop filter will limit the gain of the active loop filter. A solution for this issue is to cascade various wideband loop filters with a moderate gain. The main drawback of this technique is that each amplifying stage may add noise and distortion.

The bode plots of a typical type 2 PLL loop filter are shown in Figure 2-21. This loop filter is a lag-lead compensator. The zero has been placed to set the crossover frequency and the second pole has been designed for a specific phase margin. The pole at the origin changes the type of the open loop to type 2 for an improved steady state response. Moreover, the second pole improves the attenuation at higher frequencies.

Figure 2-22 shows an example of Bode plots for an uncompensated open loop transfer function. Figure 2-23 shows the Bode plots of the compensated open loop transfer function for the example loop filter described above. The phase margin has been modified to be 50 degrees and the crossover frequency is located at 1 MHz.

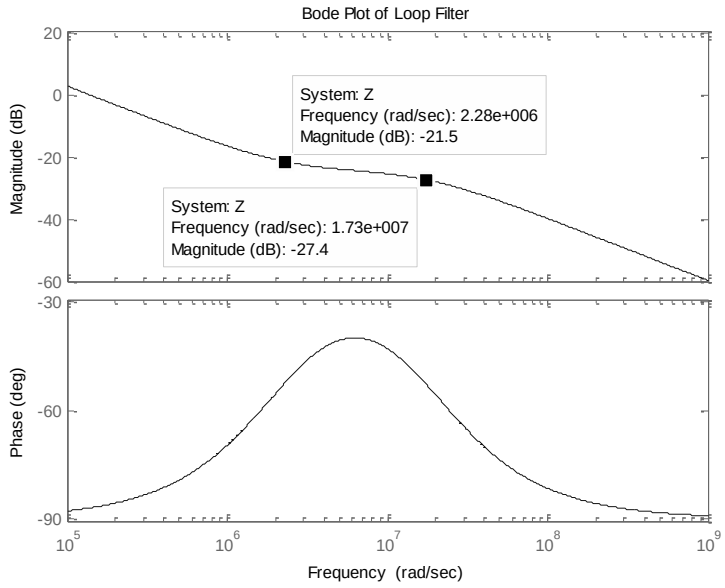

Figure 2-21: Example Bode Plots for a Type 2 Loop Filter Transfer Function

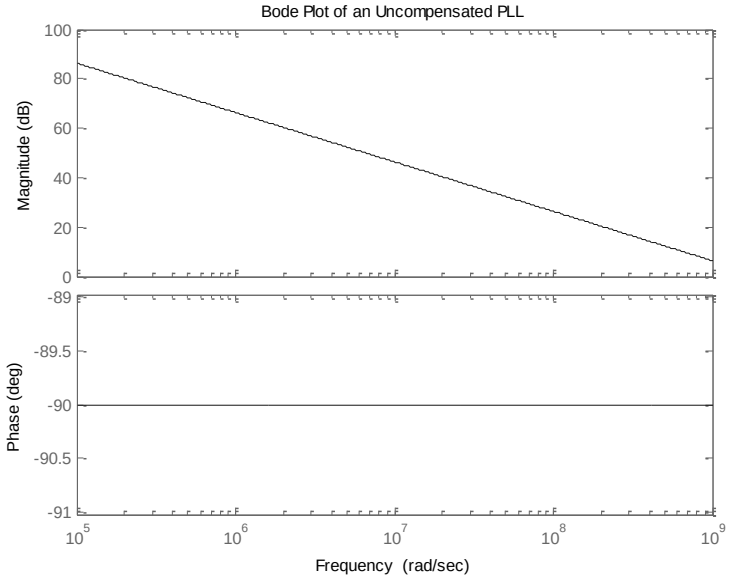

Figure 2-22: Example Bode Plots for an Uncompensated PLL Open Loop Transfer Function

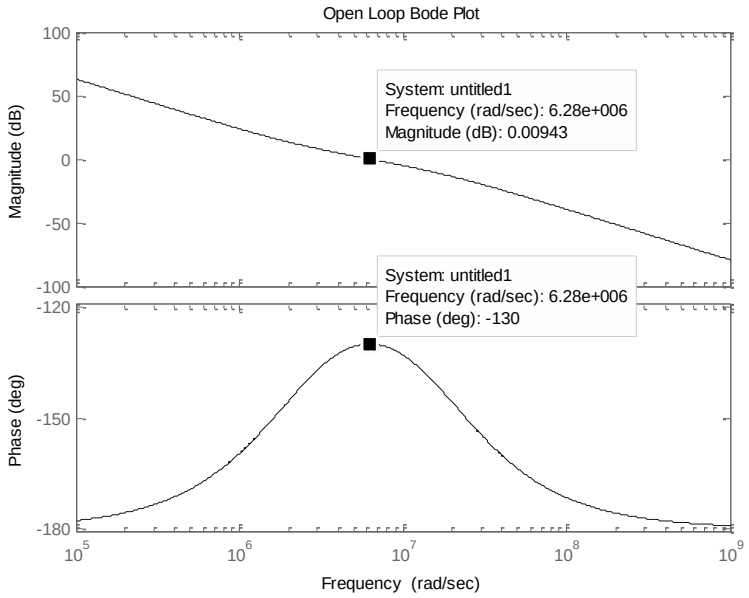

Figure 2-23: Example Bode Plots for a Compensated PLL Open Loop Transfer Function

2.3 LOOP TRACKING ERROR REDUCTION TECHNIQUES

Tracking on a feedback control system with unity feedback is the ability of the system to replicate the input. On a PLL based synthesizer with a constant divider on the feedback path, tracking becomes the ability of the system to output the desired multiple of the input.

The tracking ability of a system can be analyzed in terms of the input changes and in terms of changes in the loop. In the absence of disturbances in the loop, the feedback tracking performance is defined by the steady state performance. As explained in Section 2.2.1.3, the number of integrators on the open loop transfer function dictates the steady state error. However, the number of integrators does not assure the ability of the system to compensate for disturbances added to the loop.

On a PLL, a number of disturbances may be added to the loop. Although there may be a number of external disturbances that add to the loop, such as noised coupled to one of the loop signals, the main source of disturbances for a PLL based synthesizer sweeping over a wide band

is the VCO. The VCO has a very nonlinear tuning curve. For a PLL that sweeps over wide bands, this nonlinear behavior can be modeled as an added disturbance to the loop.

As mentioned in Section 2.2.1.4, PLLs with wide loop bandwidth are the kind of PLL required to decrease the tracking error caused by disturbances. Figure 2-24 illustrates a block diagram of a closed loop control system with added disturbances at the output, similar to those caused by the VCO nonlinearity.

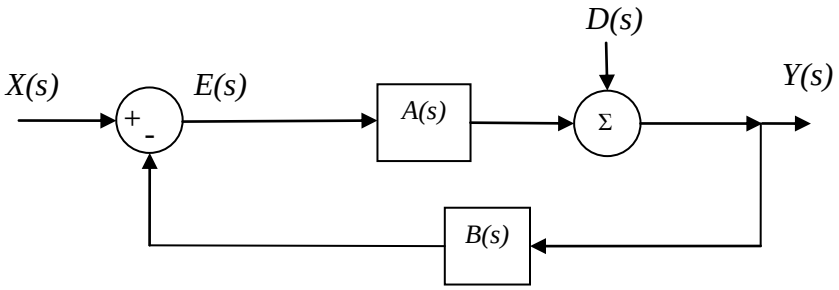

Figure 2-24: Closed Loop System Block Diagram with Added Disturbances

$$Y = X\frac{A}{1+AB} + D\frac{(1+AB)-(AB)}{1+AB} \tag{2.45}$$

$$Y = \frac{X}{B} \tag{2.46}$$

The transfer function of the output of the system (Y) has been solved in terms of the transfer functions of the input signal (X), the disturbance signal (D), the forward path (A) and the feedback path (B). Equation (2.45) shows the resulting expression for the output signal. For an open loop transfer function (AB) with a magnitude much larger than one, the output signal then becomes equal to the input signal scaled by the feedback path system. This ideal result is described on equation (2.46). This result indicates that on the condition that the open loop gain is much larger than one, the disturbance will be compensated.

PLLs have generally high gain on their passband, so that they can compensate successfully for disturbances that fall within their loop bandwidth. Wide loop bandwidth PLLs are designed to compensate for wideband disturbances. The importance of the bandwidth on the

PLL transfer function can be better understood by analyzing the closed loop transfer function. Equation (2.47) describes the closed loop transfer function.

$$H(s) = \frac{Y(s)}{X(s)} = \frac{A(s)}{1 + A(s)B(s)} \tag{2.47}$$

For an open loop transfer function with a magnitude much smaller than one, the closed loop transfer function becomes that of the forward path. Thus, the feedback compensation becomes ineffective.

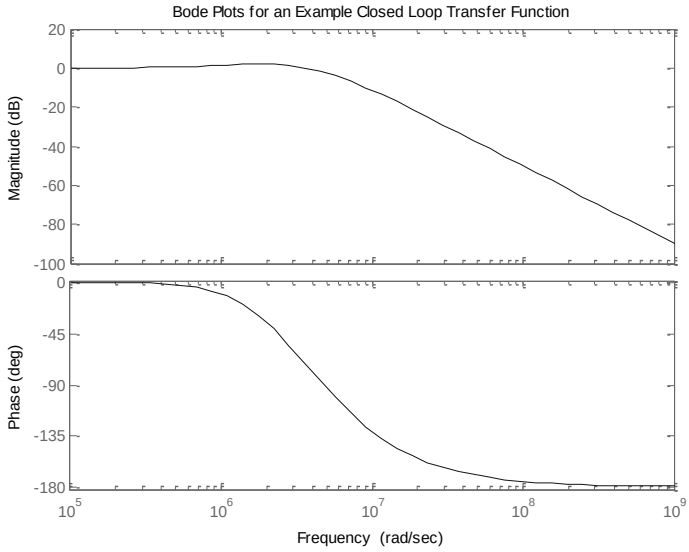

Figure 2-25: Bode Diagram of an Example Closed Loop Transfer Function for a PLL

Figure 2-25 shows the Bode diagram of an example closed loop transfer function for a PLL. This closed loop transfer function corresponds to a second order type 2 PLL with unity feedback gain. The exact performance figures of this PLL are not important for this discussion, so they are not mentioned or pointed out on these plots. From figure 2-25, it can be seen that the magnitude of the closed loop transfer function at low frequencies is closed to 0 dB, which is the ideal value for a unity feedback PLL. Likewise, the phase is close to zero and remains somewhat constant over the low frequency range. This is also the desired behavior of the output of the PLL. However, at high frequencies the amplitude is low and the phase shifts from 0 to -90 degrees. Moreover, the amplitude and the phase over the transition differ slightly from those at low frequencies. This means that near the corner frequency the compensation is not ideal.

A large phase margin corresponds to a larger transition over the corner frequency region. For this case, the compensation of the PLL will be less effective over the passband as the disturbance frequency content approaches the corner frequency. As mentioned in Section 2.2, the PLL can be approximated as linear for small regions over the tuning sensitivity. Thus, the large variations on the tuning sensitivity can be thought of many small linear regions. A design using this approximation should assure that the PLL will remain with a desired transient response and stability for all the values of the tuning sensitivity. In order to achieve this, the PLL should be design with enough phase and gain margins. The large phase margin requirement to implement a wideband synthesizer corresponds to a larger transition region near the corner frequency of the PLL frequency response. As mentioned earlier, this degrades the tracking performance.

Sometimes the loop disturbances are deterministic or can be measured. In this case, a signal that subtracts the disturbance can be added to the loop. Since this signal has not been affected by the loop frequency response, it will represent a more synchronized compensation signal. Using this compensation the resulting output will match closer to ideal output signal. Figure 2-26 shows a block diagram of a closed loop system with added disturbance (*D*) and added external compensation (*F*). On the block diagram the forward path is composed of two systems: A_1 and A_2. The feedback path system, the input signal, the error signal and the output signal maintain the same symbols as in the previous example.

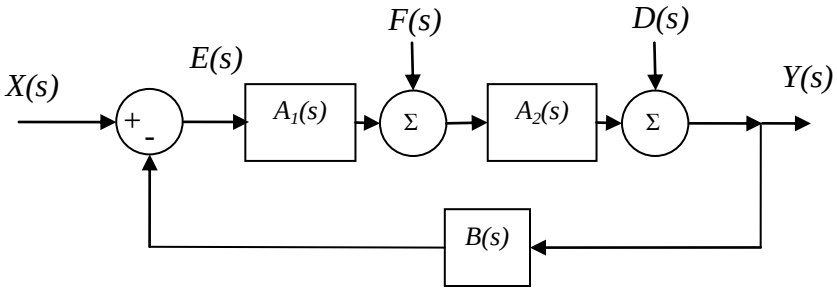

Figure 2-26: Example of a Closed Loop Control System Block Diagram with Disturbance and External Compensation

$$Y = X\frac{A_1A_2}{1+A_1A_2B} + (D + A_2F)(1 - \frac{BA_1A_2}{1+BA_1A_2}) \tag{2.48}$$

$$F = -\frac{D}{A_2} \tag{2.49}$$

Equation (2.48) represents the output signal in terms of the loop systems, the input signal, the external compensation and the disturbance signal. Consider a PLL transfer function for this analysis. Assuming that the loop has the bandwidth and the steady state convergence capability to track the input signal, the first summand term will approach the ideal output value. The second summand term includes two products. The second product of this summand will approach zero at low frequencies where the open loop gain is much greater than 1. On the other hand, at large frequencies where the open loop magnitude drops, this product will be significant. Moreover, if the expression shown on equation (2.49) holds where the PLL compensation is not effective, the second summand on equation (2.48) becomes zero. Thus, the output signal will approach the ideal output over the frequency region where equation (2.49) holds.

CHAPTER 3: DESIGN AND IMPLEMENTATION

This chapter will discuss the design and implementation of a chirp generator using a linearization technique with dual compensation. First, the chirp generator design requirements are established. Then, the linearization method is explained. Lastly, a description of the design and implementation of both compensations systems is described.

3.1 CHIRP GENERATOR DESIGN REQUIREMENTS

The UWB chirp generator developed for the context of this work will be used as the waveform generator for high resolution airborne FMCW radar sensors. The required bandwidth of the chirp generator is 6 GHz.

The nominal airborne altitude and therefore nominal range of operation is 1500 ft. This range corresponds to a roundtrip signal propagation delay of about 3 μs in free space.

The UWB radars described here use a data acquisition system (DAQ) to digitize the IF output signal. The analog to digital converter (ADC) has a minimum sampling rate of 62.5 MHz with a memory buffer capable of storing 16384 points. This number of points and the minimum sampling rate limits the IF recording time to a maximum of 262.14 μs. A sweep time of 250 μs is chosen to stay within this recording time limit.

The VCO based chirp generator should be designed with a linearization system such as the range resolution is minimally affected by the VCO non-linear behavior at the nominal roundtrip delay of about 3 μs, a chirp sweep time of 250 μs and a chirp bandwidth of about 3 μs. The most relevant parameters for the chirp generator are summarized in Table 3-1.

Table 3-1: Chirp Generator Parameters

Parameter	Value	Units
Bandwidth	6	GHz
Sweep Time	250	μs
Nominal Operating Target Delay	3.048	μs

3.2 PROPOSED LINEARIZATION TECHNIQUE

The microwave chirp generator developed for this application is a VCO based linear frequency modulated synthesizer. An UWB VCO operating at the Ku-band is used to achieve the required 6 GHz of bandwidth. The importance on the linearity of the chirp for multi-range applications has been described on chapter 1. Moreover, the airborne platform operating at a nominal altitude of 1500 ft, corresponding to a free-space delay of about 3 μs, poses severe requirements on the linearity of the chirp. In order to achieve a high level of linearity, the chirp generator will be designed with a dual-compensation system.

Figure 3-1 shows a block diagram of the linearization system. A phase-frequency closed loop control system or Phase Lock Loop tracks a scaled reference frequency and phase. A large range in the sensitivity curve of the VCO is expected due to the wide bandwidth utilized. Moreover, wideband variations on the sensitivity curve are also expected. The PLL will be designed with a high enough loop bandwidth to compensate for these wideband variations. However, the wide range of the tuning sensitivity will lower the loop bandwidth at some VCO frequencies. Moreover, the PLL should be designed with a large enough phase margin at the average value of K_V, so that phase margin does not lower significantly. If this were to happen the system could becomes unstable or at least increase significantly the peaking on the transient response. The PLL loop filter will be designed to improve the tracking error and to filter high frequency noise and spurious signals.

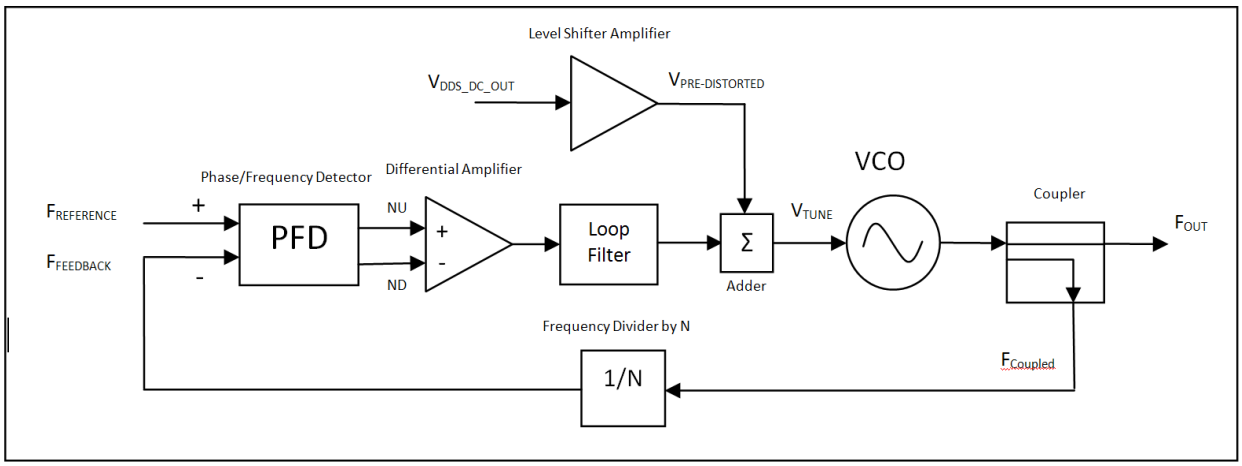

Figure 3-1: VCO Based Chirp Generator Dual Compensation System

Due to the severe requirements on the phase margin, the tracking error compensation from the PLL is not sufficient. Thus, an external pre-distorted signal will be used to improve the tracking error. On frequencies near the loop bandwidth, the gain and phase responses of the closed loop system affect the tracking ability of the PLL. The PLL compensation signal can be measured at the output of the loop filter. This signal can then be filtered on different frequency bands, amplified and phased adjusted. By applying these adjustments on the signal, a signal which will not be severely affected by the frequency response effects of the PLL can be reconstructed. This pre-distorted signal can then be used to compensate more effectively the VCO and reduce the PLL tracking error.

3.3 UWB VCO: HMC733

The UWB Voltage Controlled Oscillator chosen for this application is the HMC733 VCO from Hittite Microwave. The HMC733 VCO is a Wideband MMIC VCO with buffer amplifier that operates on the 10 to 20 GHz range. The HMC733 was primarily chosen because of the tuning voltage requirement at Ku-band frequencies. Figure 3-2, extracted from the HMC733 datasheet [41], shows the typical tuning curve of the VCO. The tuning curve shows that the voltage range required for the VCO operation on the Ku-band goes from about 3.3 V to 13.3 V. All the sub-systems on the control loop should use components with high speed and high

bandwidth requirements to achieve the PLL design requirements. The adder which is in the forward path of the control loop is implemented with an operational amplifier (opamp). Since there are opamps with the required high speed and high bandwidth capabilities that can output up to around 14 Volts, this VCO is a viable choice for this design.

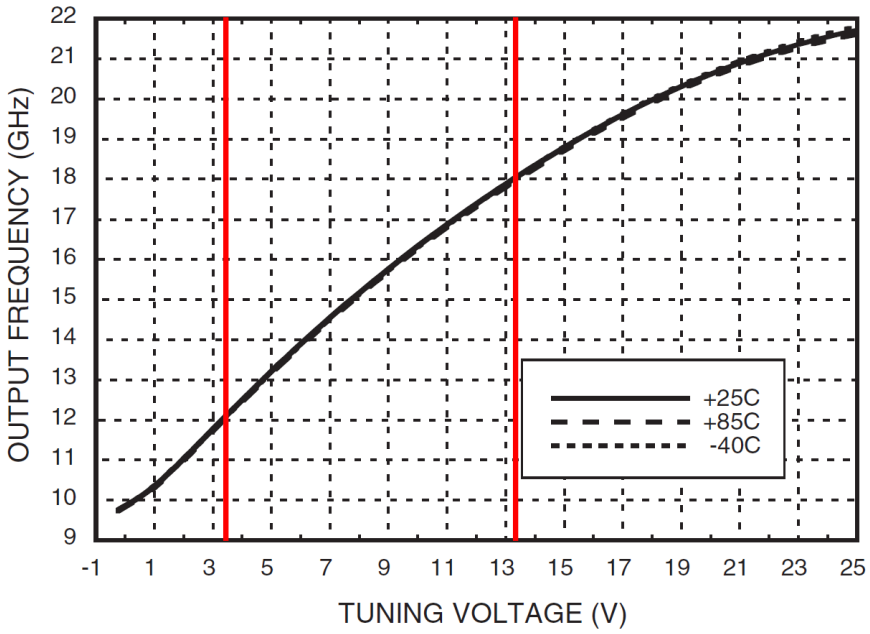

Figure 3-2: Typical Tuning Curve for the HMC733 VCO [41]

The tuning sensitivity (K_V) of the HMC733 VCO, defined as the slope of the tuning curve, is plotted in Figure 3-3. An approximate tuning sensitivity curve over the range of frequencies of interest has been extracted using the data sheet plot points and plotted in figure 3-4.

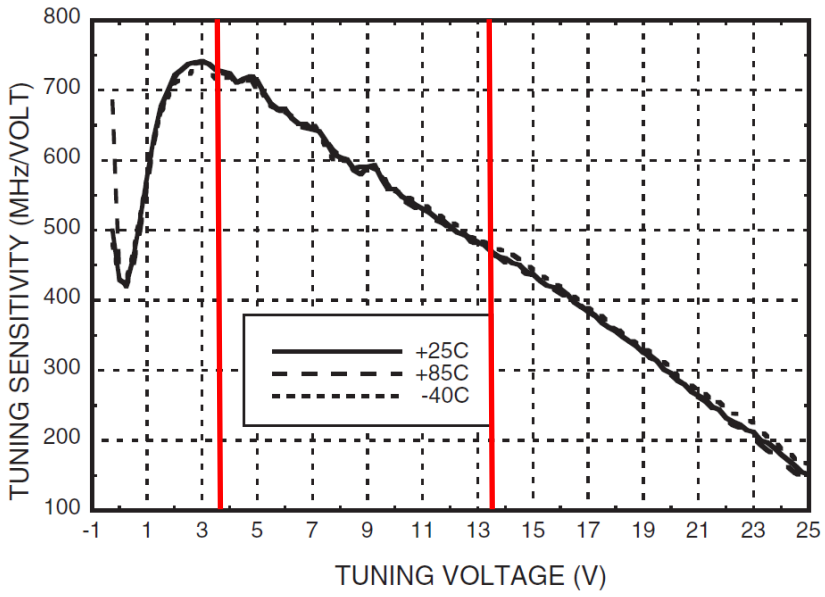

Figure 3-3: Typical Tuning Sensitivity Curve for the HMC733 VCO [41]

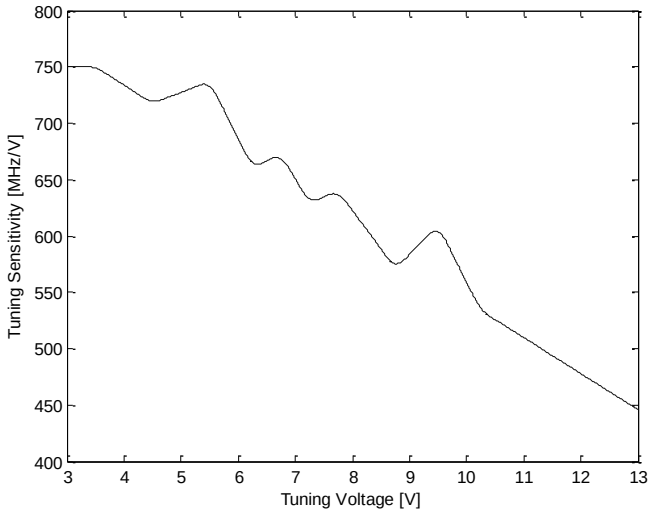

Figure 3-4: Tuning Sensitivity Curve

By integrating the tuning sensitivity plot data over the voltage range of interest, we can plot a more detailed tuning curve as shown in Figure 3-5.

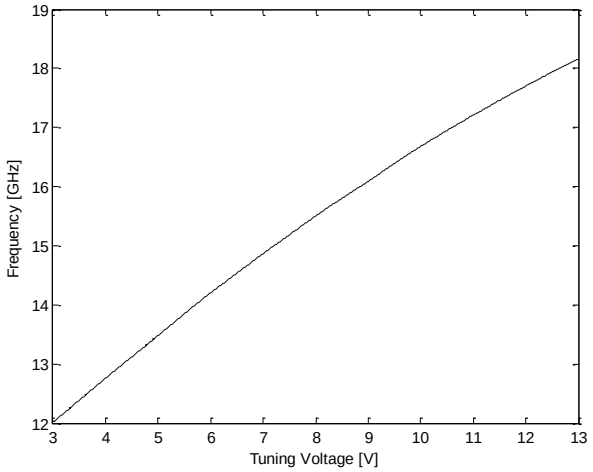

Figure 3-5: Tuning Curve Generated from Sensitivity

The tuning curve can be used to create a voltage signal that would output a linear frequency waveform as a function of time. Figure 3-6 shows a plot of the tuning voltage signal over the sweep time of 250 μs required to output a linear frequency modulated waveform over the frequency range of interest.

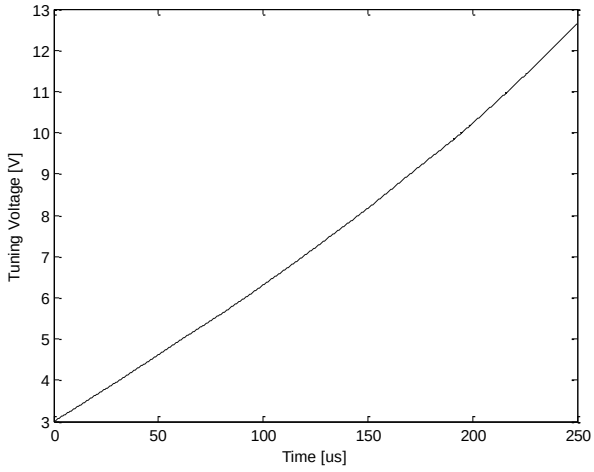

Figure 3-6: Tuning Voltage Required To Linearize the Tuning Curve given by the HMC733 Datasheet

Also, a plot showing the voltage rate of change over time can be generated with previous plot points. Figure 3-7 shows this plot. It has a maximum rate of change of about 52.5 kV/s. This plot was inferred from the approximate low resolution points on the plot of the datasheet. Thus, it

is not an optimal indicator of the high frequency requirements, but provides useful information about the rate of change for large voltages. Small wideband variations on the tuning curve are expected. Therefore, these are expected to be compensated for at the tuning voltage to effectively output a linear frequency waveform.

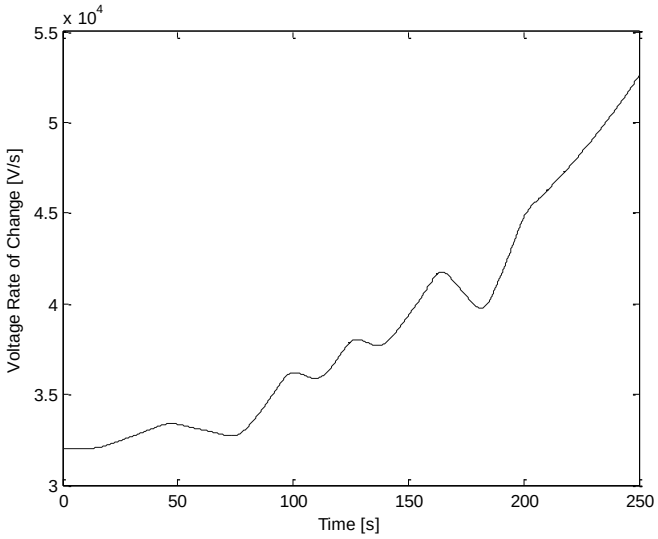

Figure 3-7: Voltage Rate of Change over Time Plot

From the tuning sensitivity curve and the expected tuning voltage over the sweep time to linearize the VCO, the tuning sensitivity over time has been plotted. These approximate variations on K_V over the sweep time can be sampled to time intervals. Figure 3-8 is a plot of the approximate large variations of K_V over the sweep time. Both the approximate continuous points and the sampled points are shown in Figure 3-8.

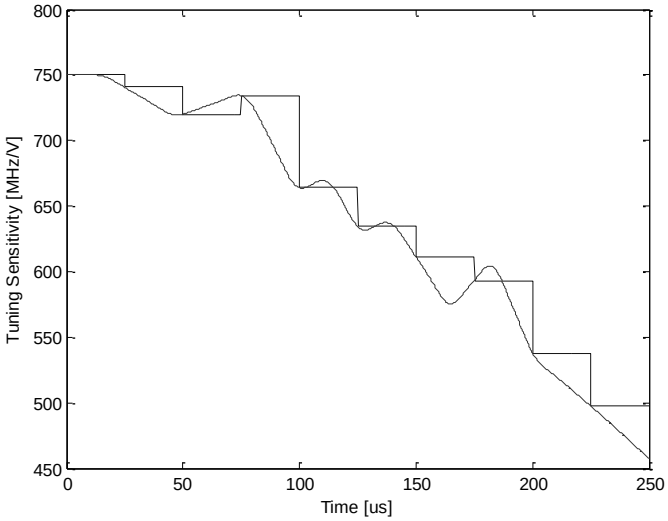

Figure 3-8: Tuning Sensitivity over the Expected Sweep Time

In order to use linear control system analysis techniques, the value of K_V is assumed constant for a small time interval. Although the PLL performance will differ at different intervals, the design should meet the specifications over the entire range. Since a linear frequency modulated signal is expected over the sweep time, the time axis in Figure 3-8 is linearly related to the chirp frequency. Thus, K_V can be thought of having different values at different chirp sub-bands. This property will be exploited to measure the frequency spectrum performance at different frequencies.

The compensation signal produced by the loop filter will be amplified differently by the K_V over the different time intervals. However, the small variation in K_V will occur roughly around an approximated constant magnitude of K_V. Thus, they can be modeled as disturbances added to the output of the VCO, similarly to other plant disturbances that occur on control system outputs. A PLL block diagram including the model of the small variations on the VCO as disturbances added is shown in figure 3-9.

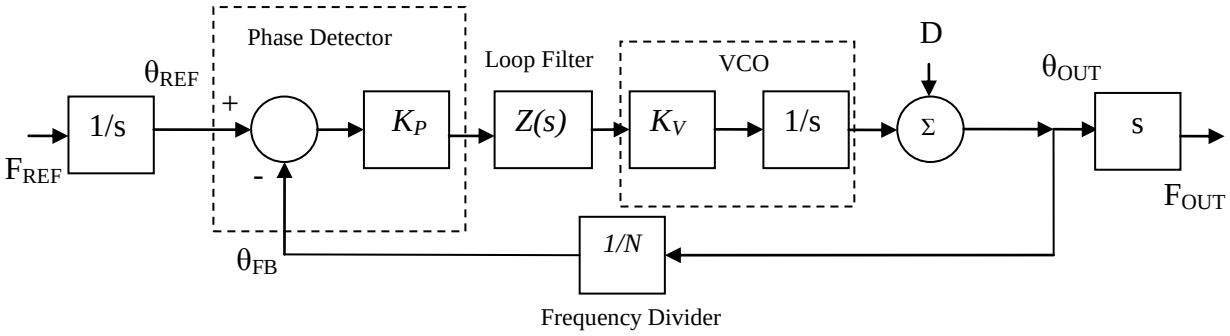

Figure 3-9: PLL Block Diagram with Added Disturbance

3.4 PLL DESIGN

3.4.1 PLL Design Requirements and Considerations

The requirements and considerations for the design of the PLL can be summarized as follows:

- From the manufacturer's data sheet, the tuning sensitivity for the chosen VCO varies from about 450 to 700 MHz/V over the frequency range of interest.
- A 2-channel DDS board described on Appendix A will be used to synthesize the reference linear frequency waveform. The DDS operates with a quantization rate of 1 GHz. This will limit the bandwidth and the minimum frequency of the reference signal. Moreover, the PLL will be designed with available programmable and fixed dividers. This also needs to be considered to determine the reference frequency range.
- An available phase-frequency detector specified for the chosen reference frequency range needs to be selected.
- The PLL should be design with a wide loop bandwidth to compensate for the modeled wideband disturbances caused by the VCO nonlinear tuning sensitivity.
- The loop filter should be designed such that the high frequency noise and spurious signals are attenuated properly.

- The PLL should be designed with a large enough phase margin such that the large variations in the tuning sensitivity do not drive the system unstable and do not increase the transient peak errors significantly.
- The PLL should be designed such that the steady state error for an input frequency ramp converges to a finite value.

3.4.2 Reference Frequency and Divider Selection

The reference signal of the control loop should be a linearly frequency modulated waveform at a fraction of the output frequency. As mentioned earlier, a 2-Channel Direct Digital Synthesizer (DDS) board, developed at CReSIS, will be used to synthesize this reference signal. The 2-Channel DDS Board functionality is described in Appendix A.

The phase detector output of the Phase Lock Loop is coherent to the reference signal. This signal contains unwanted spurious noise. One of the tasks of the loop filter is to attenuate this spurs. Regardless of the filter order used, the further away these spurs are in frequency with respect to the loop bandwidth, the more the attenuation given by the filter. These spurs appear as sidebands on the output frequency spectrum of the PLL. A maximum acceptable spurious signal will be 35 dBc.

For the reasons given, the maximum possible reference signal should be utilized. In order to choose the start and end frequencies of the reference chirp, both the frequency divider availability and the DDS limitations should be considered.

The 1 GHz quantization rate of the DDS sets the Nyquist bandwidth to 500 MHz. As explained in chapter 1, the images of the fundamental are spaced by the Nyquist bandwidth. The odd harmonic image spaces are mirrored versions of the fundamental.

At the X-band (12-18 GHz) and the Ku-band (8-12 GHz) frequency ranges, most available dividers have division factors that are multiples of two. At frequencies less than 6.5 GHz, programmable dividers are readily available.

Taking these two limitations into consideration, a divider chain with a division factor of 20 was chosen. The divider chain is composed of a divider by 4 and a programmable divider set to 5. This division results in a reference start and stop frequencies of 600 to 900 MHz for an output of 12 to 18 GHz. Both frequencies are in the same DDS Nyquist image zone. A reconstruction filter will be needed to filter the 600 to 900 MHz band produced by the DDS in consideration. Also, there is a need to amplify the signal to the required level of the phase detector input port.

The dividers selected to divide by 4 and by 5 are the HMC493LP3 and the HMC705LP4. Both are manufactured by Hittite Microwave Inc. [42][43]. The evaluation boards manufactured by Hittite for both dividers were used for the implementation of the prototype system.

3.4.3 Phase Frequency Detector Selection

The phase detector should function over the frequency range specified by the reference frequencies. It should also add minimum noise to the system and have a linear proportional gain. The HMC439QS16G is a phase-frequency detector developed and manufactured by Hittite Microwave Inc. that meets all these requirements [44]. This phase-frequency detector was designed for low noise phase-lock loop applications. It works over the frequency range from 10 to 1300 MHz. The evaluation board available for this phase detector was chosen to be used for the prototype of the system.

The phase detector has a differential charge pump output of $10/2\pi$ mA/rads. The evaluation board contains 200 ohm pull-up resistors on both outputs. The pull-up resistors convert the output back to voltage for a next stage with high input impedance. For this case, each output is limited between 3 and 5 Volts for charge pump currents between 0 and 10 mA. The differential output range becomes 4 Volts for an entire 2π phase shift when connected to a high impedance load. For cases where the input impedance is comparable with the pull-up resistors, the output voltage will be scaled. Thus, the phase detector gain depends on the input impedance of the next stage. This will be analyzed on the next section.

3.4.4 Differential Amplifier Design

As explained on the previous section, the phase detector contains a differential output. Therefore it requires to be coupled to a differential device to combine the signals. A differential amplifier will be used for this purpose. A unity gain amplifier will initially be used for high voltage amplifier bandwidth. The amplifier gain will be changed if the PLL design requires it.

Whenever possible it is best to realize a differential amplifier using an opamp. The closed loop implementations of amplifiers with opamps provide a stable gain, improved input and output impedances, and improved distortion. From all different loop implementations for opamp based feedback amplifiers, the two most common circuits are the inverting and non-inverting configurations. Because these two configurations are linear, they can be combined with superposition. Figure 3-10 shows a differential amplifier implementation by combining these two configurations. A voltage divider has been added to the non-inverting input to balance the gains. Equation (2.33) shows a description of the circuit in Figure 3-10. For R_4 equal to R_3 and R_2 equal to R_1, the voltage gain for inverting and non-inverting inputs becomes the same. Equation (2.34) describes the input to output relationship for a balanced differential amplifier.

$$V_{out} = V_+ \cdot \left(1 + \frac{R_3}{R_1}\right) \cdot \left(\frac{R_4}{R_2 + R_4}\right) + V_- \cdot \left(-\frac{R_3}{R_1}\right) \tag{2.33}$$

$$V_{out} = (V_+ - V_-) \cdot \left(\frac{R_3}{R_1}\right) \tag{2.34}$$

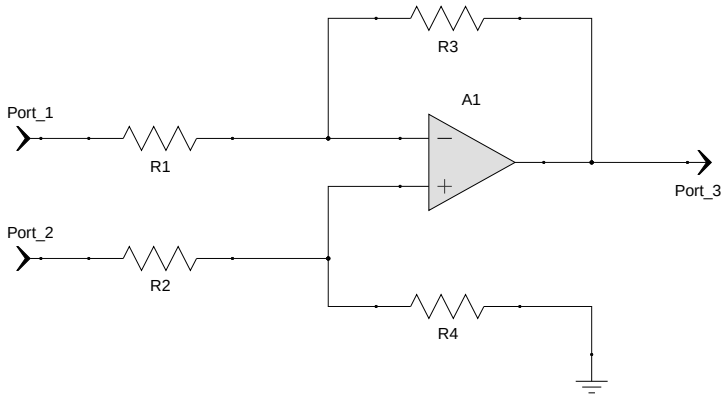

Figure 3-10: Schematic Circuit for a Differential Amplifier Circuit

If no poles are added to the amplifier circuit, the gain-bandwidth product of the op-amp sets the small signal bandwidth of a op-amp loop implementation for a specific gain. For low gains, the bandwidth may increase to the point where it gets too close to an internal pole. This will decrease the phase margin and may drive the circuit to an unstable state [45].

Another, common source of oscillation for high speed op-amp circuits is related to capacitive loading. Capacitive loading occurs when the op amp output is coupled to a device with high capacitance on the input. Two main compensation techniques exist to solve this issue. By adding a pole at a frequency much lower than the resonant frequency, the oscillation may be avoided. The second technique consists of forcing a high noise gain. The noise gain is related to the feedback path, so changing it would not necessarily affect the loop gain. Being a factor of the open loop gain, increasing the noise gain improves the gain margin [46].

Since oscillations do not necessarily occur close to the opamp small signal bandwidth, the first compensation technique requires lowering substantially the loop bandwidth of the amplifier. This is not desired since a high PLL forward path bandwidth is required. The second technique cannot be accomplished without changing the balance on the differential amplifier. This is also not desired either. For this case, an inductive component can be added to the capacitive load in series. This inductor should increase the resonant frequency to a high enough value where its signal level has been severely attenuated.

The bandwidth of the differential amplifier, which is on the forward path, should be much higher than the loop bandwidth. The THS3001 operational amplifier is a high speed device developed and manufactured by Texas Instruments Inc. [47]. This device has a small signal gain-bandwidth product of 420 MHz. At a differential amplifying gain of 1, the bandwidth becomes 420 MHz. The loop bandwidth will be set low enough to attenuate the spurious signals from the phase detector by at least 35 dBc. The reference spurious signals are in the 600 to 900 MHz range. A 420 MHz small signal bandwidth is much higher than the loop bandwidth required for attenuating the spurious signals. Moreover, 420 MHz is below the reference signals, so the amplifier high frequency attenuation will improve the spurious rejection. The THS3001 has a 6500 V/μs slew rate, which provides a high speed limit that will not be reached by the compensation signal. This slew rate corresponds to a jump of about 1 V in 153 ps [47]. This is

much faster than the rise time for the loop bandwidth expected. Also, this slew rate corresponds to an opamp full power bandwidth of 32 MHz for a voltage swing of 20 V. Thus, large signals below this bandwidth will not be distorted by the opamp. Thus, the opamp will not pose a speed limitation on the forward path for a PLL bandwidth lower than 32 MHz. This property will be exploited to indirectly measure the time performance from frequency measurements.

The THS3001 opamp is a current feedback amplifier (CFB). In bipolar transistors, currents can be switched faster than voltages [48]. For this reason CFB have high slew rates that correspond to large signal bandwidths similar to its small signal bandwidth [48]. Although CFB opamps have this clear advantage over voltage feedback amplifiers (VFB) opamps, they need to be implemented with a fixed feedback resistor for best performance. This value is usually given by the manufacturer. Moreover, they cannot have a feedback capacitor, which limits its ability to design filters. The filter topology of choice for these amplifiers is Sallen Key-filters [48].

The THS3001 datasheet suggest a feedback resistor value of 680 ohms for optimal phase margin performance at a gain of 1 [47]. Figure 3-11 shows a schematic of the differential amplifier circuit. R_5 is a zero ohm resistor and will be used to add inductance to the capacitive input. The operational amplifier should be biased with positive and negative 15 Volts for improved performance, compared to a bias voltage of positive and negative 5, according to THS3001 datasheet [47]. The supply voltage should be filtered at the input with tantalum capacitors ceramic capacitors. The tantalum capacitors provide good filtering of the low frequencies, but their low self-resonant frequency makes them inductive at high frequencies. Ceramic capacitors can be used to filter both middle and high frequencies, depending on the capacitor value and resonant frequency. Capacitors with high self-resonant frequencies should be placed closed to the power supply pins of the op amp integrated circuit [46][49].

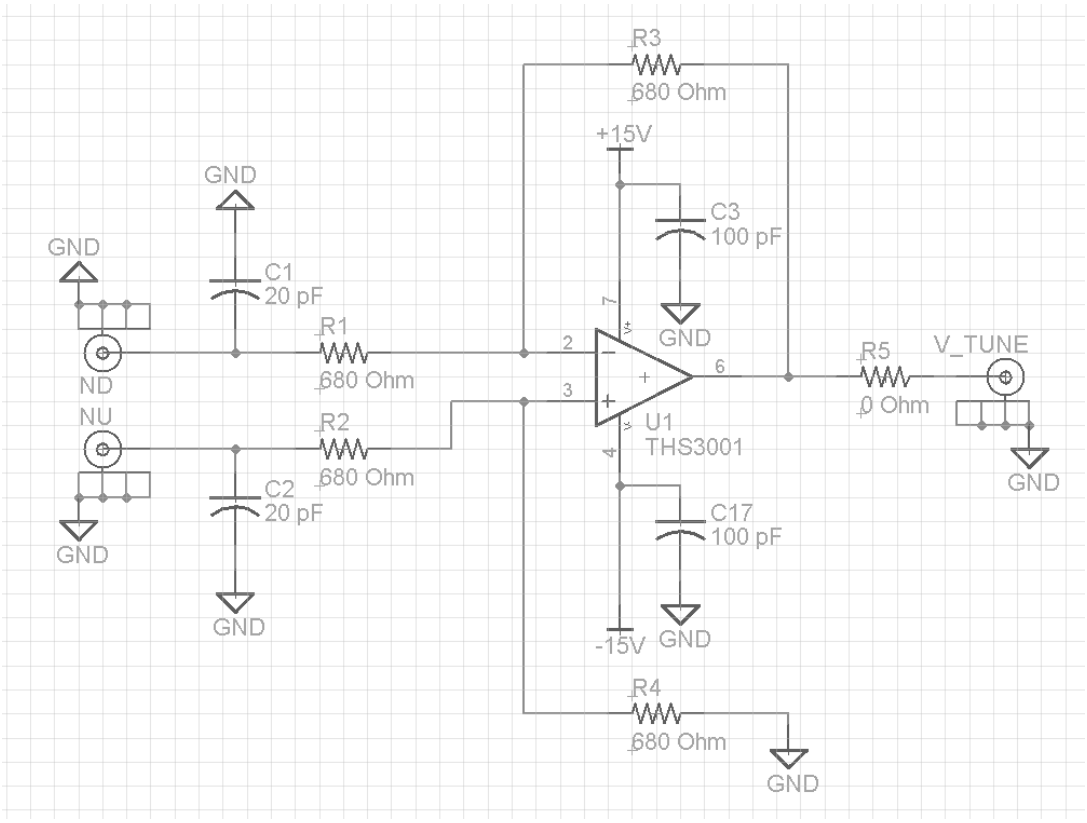

Figure 3-11: Schematic Circuit of the Differential Amplifier

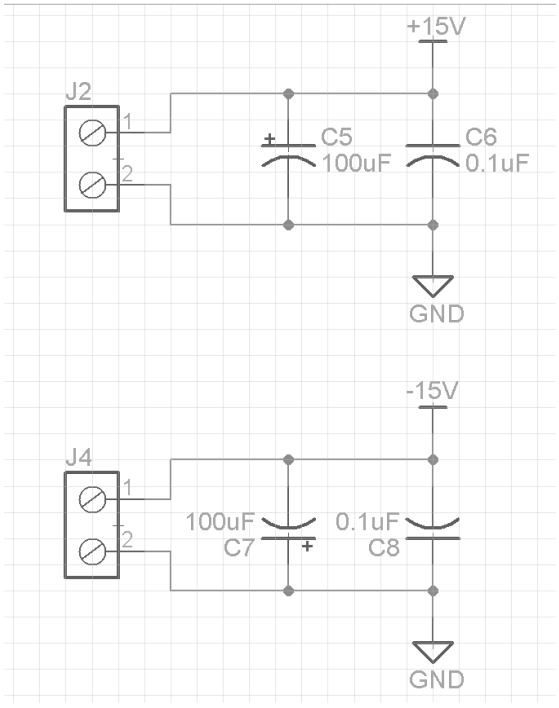

Figure 3-12: Differential Amplifier Power Supply Capacitor Bank

For the expected maximum output voltage range of positive and negative 2 Volts and considering the relatively high input impedance of the loop filter, the expected variations in the supply current come mostly due to changes in temperature. On the datasheet of the THS3001 op amp, the variations of supply current with temperature are specified from 5 to 8 mA [47]. Equation (3.35) relates the maximum common path impedance (Z_{max}) and the current variations (ΔI) to the supply voltage noise level (V_n). Solving for the common path impedance and using equation (3.36) with an estimated value of the power supply wiring inductance (L_{PSW}) , the power supply bandwidth (f_{3dB}) can be computed. Finally, equation (3.37) shows how to solve for the bypass capacitor value (C_{bypass}) . Since this calculation requires knowledge of the wiring inductance, a standard bypass capacitance value of 1 nF has been chosen to filter high frequencies [49].

$$V_n = \Delta I \cdot Z_{\max} \tag{2.35}$$

$$f_{3dB} = \frac{Z_{\max}}{2\pi L_{PSW}} \tag{2.36}$$

$$C_{bypass} = \frac{1}{2\pi \cdot f_{3dB} \cdot Z_{\max}} \tag{2.37}$$

Having decided the design of the differential amplifier, it is possible to calculate its input impedance to determine the phase detector gain. Both input resistors of the differential amplifier are connected to a virtual short. In turn, the positive pin is also connected to ground through another resistor used to balance the differential amplifier. Thus, the input impedance becomes the series combination of the input resistor with the positive pin shunt resistor. With both values being 680 ohms, the input resistance equals 1360 ohms.

An equivalent circuit of one of the phase detector outputs coupled to an input impedance of the differential amplifier is shown in Figure 3-13. The 200 ohms is the pull-up resistor connecting the charge pump output to a 5 Volt supply. The charge pump current can have a value between 0 and 10 mA.

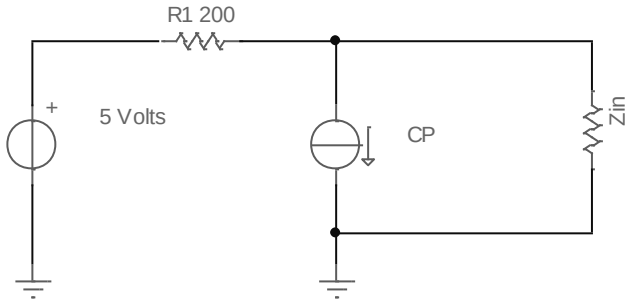

Figure 3-13: Equivalent Phase Detector Output and Differential Amplifier Input Impedance

Applying circuit analysis, the output voltage of a single phase detector differential output varies from 2.6154 Volts to 4.3590 Volts. The magnitude of the voltage range for an entire cycle becomes twice this magnitude of this range or 3.4872 V.

The output impedance (Z_{out}) of the differential amplifier becomes a fraction of the output impedance of the op amp (Z_{out_opamp}) due to the feedback effect, as shown on equation (3.38). In this equation, A_{ol} is the op amp open loop gain equal to 60 dB and B is the feedback gain equal to 0.5. This closed loop effect on the output impedance isolates the current to the next stage: the loop filter. Thus, the loop filter becomes a voltage only device.

$$Z_{out} = \frac{Z_{out\_opamp}}{1 + A_{ol}B} \tag{3.38}$$

Under these conditions, the phase detector gain becomes 3.4872 Volts per 2π radians.

3.4.5 Adder Design

In order to combine the loop compensation voltage with the external pre-distorted voltage, an adder circuit is needed. An adder can be realized with operational amplifiers. As mentioned on the differential amplifier design section, the loop configurations of operational amplifiers have a linear response. By using superposition, two input signals can be combined to

the same inverting input of the inverting amplifier configuration as shown in Figure 3-14. The resultant inverting adder circuit output voltage is described by equation (3.39).

$$V_{out} = (V_1 + V_2) \cdot \left(-\frac{R_3}{R_1} \right) \tag{3.39}$$

Since the adder goes on the forward path of the PLL, it is expected to have the same high speed and high bandwidth requirements as the differential amplifier. Moreover, the output voltage range of the adder is determined by the VCO tuning curve. As seen on the VCO tuning plots [41], the required maximum tuning voltage is about 13.3 V. The THS3001 operational amplifier has the capabilities to provide this output range and satisfy the high bandwidth requirements [48]. For these reasons, the THS3001 will be utilized to implement the adder circuit.

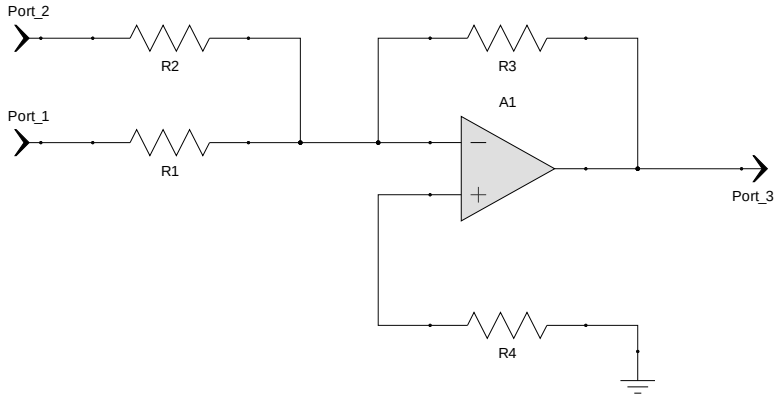

Figure 3-14: Basic Circuit Schematic for an Inverting Adder Amplifier

Additionally, the VCO should be protected against negative input voltages. For this reason, a general purpose diode should be shunted at the output of the adder with the anode connected to ground.

The circuit will have the same capacitor bank and bypass capacitors that were used for the differential amplifier discussed earlier. A schematic of the circuit is shown in Figure 3-15.

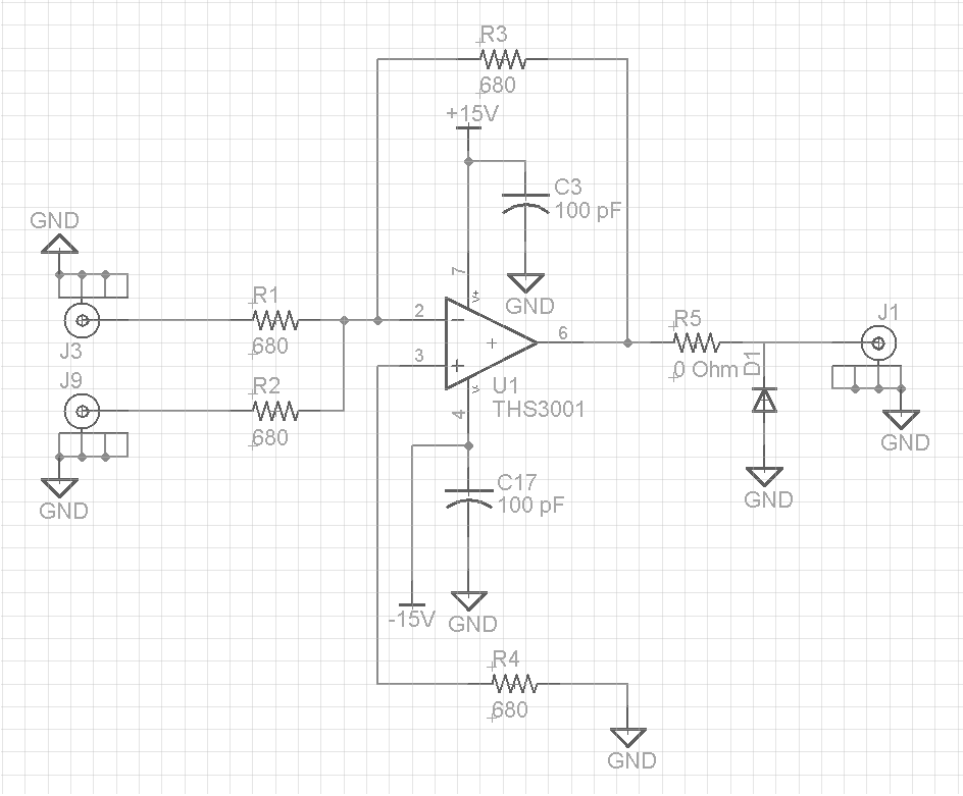

Figure 3-15: Circuit Schematic of the Adder

3.4.6 Loop Filter Design

The loop filter features include filtering the spurious signals of the phase detector output as well as compensating the loop response for given response requirements. Equation (3.40) describes the uncompensated open loop transfer function (G_{UC}) of the PLL.

The simulated Bode plots for the uncompensated open loop transfer function are shown in Figure 3-16.

From all the components analyzed so far, the average PLL component gains are listed in Table 3-2. Since both the adder and the differential amplifier have a gain of 1, they are not mentioned on the table.

$$G_{UC}(s) = K_P \cdot K_V \frac{1}{s \cdot N} \tag{3.40}$$

Table 3-2: Average PLL Component Gains

Parameter	Value	Units
K_V	600	MHz/V
K_P	3.4872	V/(2π rads)
N	20	

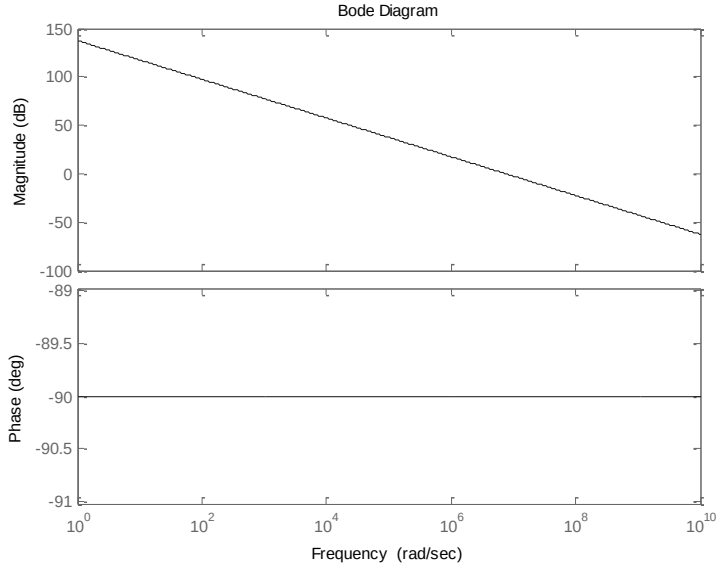

Figure 3-16: Simulated Uncompensated Open Loop Transfer Function

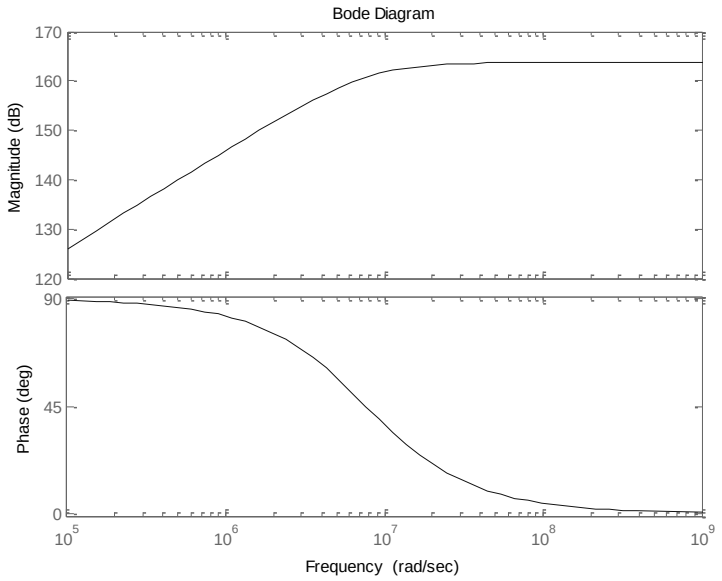

Figure 3-17: Simulated Bode Plots for the Closed Loop Transfer Function of the Uncompensated PLL

Figure 3-17 shows the bode diagram for the compensated closed loop transfer function. The magnitude plot has the shape of a high-pass filter. This phase plot shows close to 90 degree phase offset at low frequencies and close to zero phase offset at high frequencies. Since a low phase offset and a high gain is required at low frequencies for an effective tracking performance, this uncompensated system will not have a good performance for tracking the reference. Moreover the high frequency noise and spurious signals will pass to the output.

In order to have the best possible PLL tracking performance with the given reference signal, it has been noted that the PLL needs to be designed with loop bandwidth as wide as possible. This way, the output of the PLL will track the input and compensate for wideband disturbances added to the loop. The crossover frequency of the open loop can be increased by a wideband passband on the loop filter which increases the gain of the low frequencies with respect to the high frequencies. Moreover, the loop filter bandwidth needs to be low enough so that the reference spurs get attenuated sufficiently. In order to have the best of both requirements, a high order loop filter should be selected.

It has been mentioned on chapter 2 that the type of PLL that has the best transient performance is the typical type 1 PLL. This type of PLL does cause transient errors due to

peaking. The transient performance of a PLL designed with a type 1 PLL loop filter with zeros is not as good as that of the typical type 1 PLL. However, both the phase margin and the loop bandwidth can be designed more conveniently on this type of PLL.

Active loop filters have small signal gain and bandwidth constraints. They also add distortion and noise.

For all these considerations, a passive type 1 PLL loop filter with zeros has been selected.

The passive type 1 PLL loop filter will be designed as a voltage filter. The differential amplifier has low output impedance, so that its output is a voltage signal. Thus, no additional current to voltage converts are needed.

The order of loop filters are limited by both the small value of the capacitors and the complexity of the circuit needed to realized it. On [39] a forth order PLL is suggested to provide an adequate trade-off between high order and the limitations mentioned.

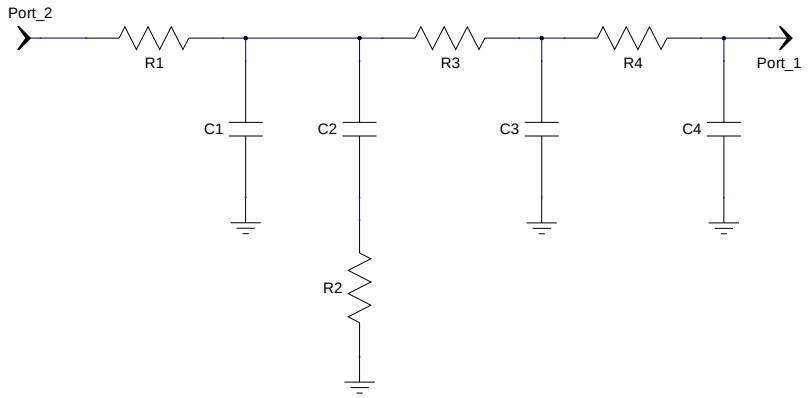

Figure 3-18: Circuit Schematic of the Proposed 4th Order Loop Filter

A suggested circuit realization of a fourth order voltage passive loop filter is shown in Figure 3-18. An approximate transfer function ($Z_{(s)}$) of the loop filter is given by equation (3.41). The approximation is made on the third and forth poles as simple first order RC filters appended to the filter. This approximation holds valid for time constants much smaller than that of the first pole.

$$Z(s) = \frac{1 + s \cdot C_2 \cdot R_2}{\{1 + s[C_2 R_2 + R_1 \cdot (C_1 + C_2)] + s^2 [R_1 R_2 C_1 C_2]\} \cdot (1 + s \cdot C_3 R_3) \cdot (1 + s \cdot C_4 R_4)}$$

(3.41)

The loop filter transfer function can be written in terms of the time constants as shown in equation (3.42) below.

$$Z(s) = \frac{1 + s \cdot T_Z}{(1 + s \cdot T_1) \cdot (1 + s \cdot T_2) \cdot (1 + s \cdot T_3) \cdot (1 + s \cdot T_4)}$$

(3.42)

In equation (3.42), T_Z is the time constant for the zero. T_2 through T_4 are the time constants that correspond to the poles for frequencies higher than the loop bandwidth. T_1 is the time constant for the first pole on the low or medium frequencies. T_1 defines the amplitude level of the loop filter transfer function at the crossover frequency. By setting the magnitude of the open loop transfer function to 1 and evaluating it at the crossover angular frequency (ω_O) using the loop bandwidth defined, the value of T_1 can be solved for. The solution of T_1 to set the open loop magnitude to 0 dB at the designed loop bandwidth is shown on equation (3.43).

$$T_1 = \frac{\sqrt{\left[\frac{K_P K_V}{N \omega_O} \sqrt{\frac{1 + \omega_o{}^2 T_Z{}^2}{(1 + \omega_o{}^2 T_2{}^2) \cdot (1 + \omega_o{}^2 T_3{}^2) \cdot (1 + \omega_o{}^2 T_4{}^2)}}\right] - 1}}{\omega_o{}^2}$$

(3.43)

The phase margin (φ) specified can be set at the crossover frequency by setting the time constant of the second pole to the expression on equation (3.44), which derivation is shown on [39].

$$T_2 = \frac{\sec(\phi) - \tan(\phi)}{\omega_o \cdot (1 + T_{32} + T_{42})} \tag{3.44}$$

$$T_3 = T_{31} \cdot T_2 \tag{3.45}$$

$$T_4 = T_{42} \cdot T_2 \tag{3.46}$$

It is desired for most cases to have the phase peak at the phase margin. Equation (3.47) shows how to set the zero time constant for this purpose. The derivation of this equation is also given on [39].

$$T_Z = \frac{1}{\omega_o \cdot (T_1 + T_3 + T_4)} \tag{3.47}$$

A loop filter was designed using these criteria for a loop bandwidth of 12 MHz and a 75 degree phase margin at a tuning sensitivity (K_V) of 600 MHz/V, which is at the midpoint on the VCO tuning sensitivity curve. Even though a large phase margin such as 75 degrees causes large damping, this design parameter is required to maintain stability and low overshoot. As the value of the tuning sensitivity changes, the crossover frequency will change as well. This will cause the phase margin to drop. The Bode plots for the designed loop filter are shown in Figure 3-19. The amplitude response shows an attenuation of 14.8 dB at 600 MHz, which is the lowest reference frequency.

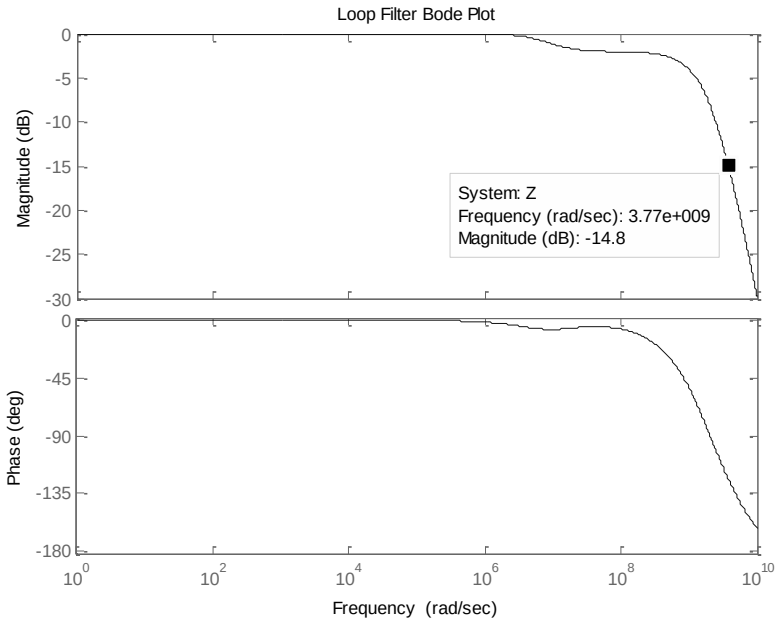

Figure 3-19: Simulated Bode Plots for the Designed Loop Filter

Figure 3-20 shows the Bode plots for the compensated open loop transfer functions. The design has successfully made a phase peak at the designed phase margin. Moreover, the crossover frequency is at the designed loop bandwidth.

Figure 3-21 shows a simulation for the Bode plots of the closed loop transfer function for the compensated PLL. The plots show the specified loop bandwidth. The pass band, which corresponds to the region where the PLL compensation is effective, has a flat amplitude and phase response. These two characteristics will provide a more effective PLL compensation to the variations on the VCO.

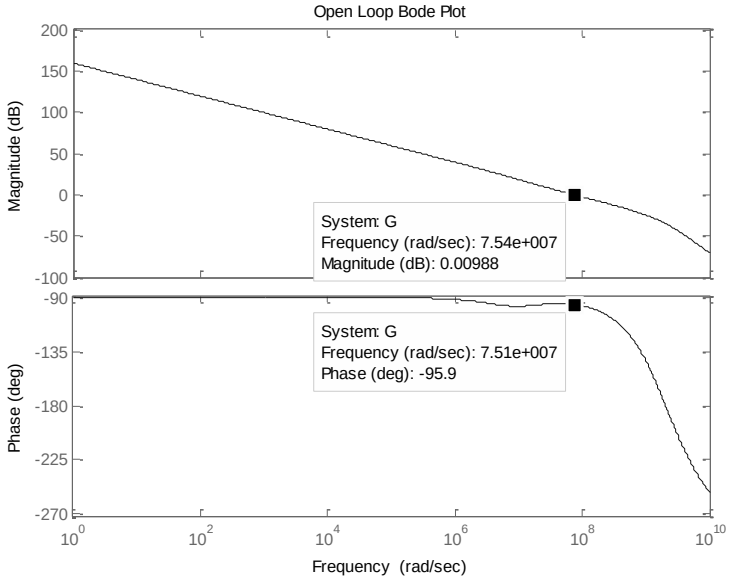

Figure 3-20: Bode Plots for the Compensated Open Loop Transfer Function

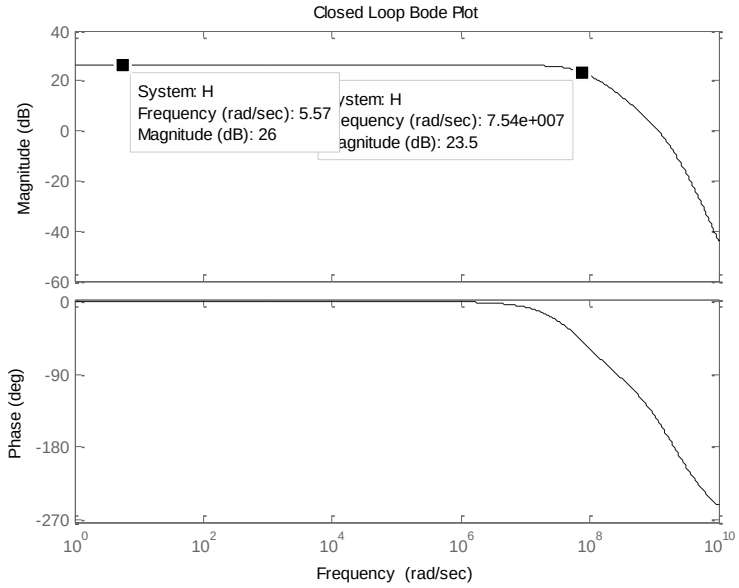

Figure 3-21: Bode Plots for Compensated Closed Loop Transfer Function

Even though the previously mentioned design had a good compensation response, the amount of attenuation on the spurious signals was not sufficient. Therefore, the designed circuit had to be tuned to improve the attenuation level without severely affecting the bandwidth of the PLL.

After various design iterations, the phase margin and loop bandwidth of the PLL for optimal performance became 73 degrees and 14.64 MHz at a K_V of 600 MHz, respectively. In addition, the phase peak near the phase margin on the final design is shifted for an improved attenuation with the high frequency poles. The Bode plots for the final design of the loop filter are shown in Figure 3-22. Figure 3-22 shows an attenuation of 25.2 dB at 600 MHz. The rest of the reference spur signals will be attenuated even further.

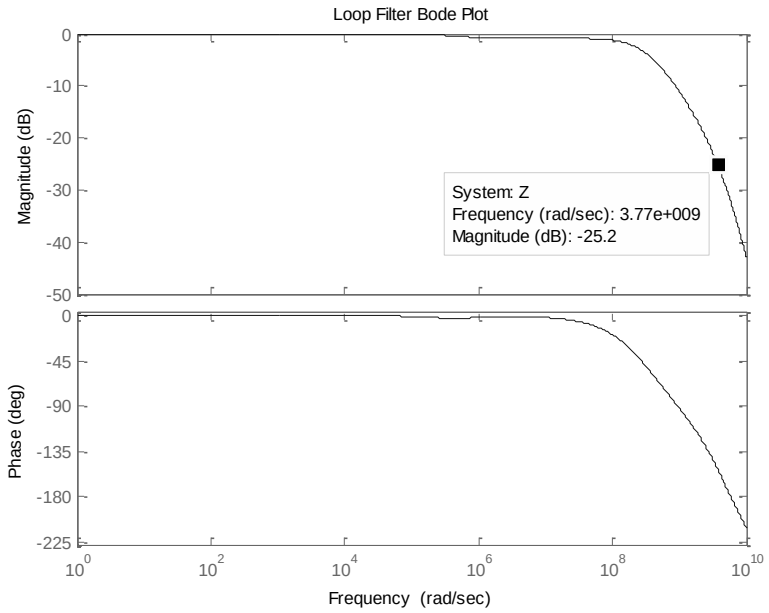

Figure 3-22: Simulated Bode Plots for the Final Design of the Loop Filter Transfer Function

Figure 3-23 shows the Bode plots for the compensated open loop transfer function using the final loop filter design. The crossover frequency is at 14.64 MHz and the phase margin is 73 degrees. The plots in Figure 3-23 correspond to the open loop transfer function for the final design evaluated at a K_V value of 600 MHz/V. To see the effects on the open loop frequency response for the large variation on K_V, figures 3-24 and 3-25 show the Bode plots at values of K_V equal to 450 and 750 MHz/V respectively. For the first case, at K_V equal to 450 MHz/V, the loop bandwidth drops to 11.1 MHz and the phase margin increases to 77 degrees. On the second case, where the value of K_V is 750 MHz/V, the loop bandwidth increases to 17.82 MHz and the phase margin drops to 69 degrees. The phase margin values may seem too high and therefore not optimum. However, decreasing the phase margin would require lowering the frequency of the first pole. This in turn would decrease the amplitude at higher frequencies and the path would require amplification from one of the active devices to maintain the high crossover frequency. However, increasing the gain would decrease the bandwidth of the active devices and the loop bandwidth would drop anyway.

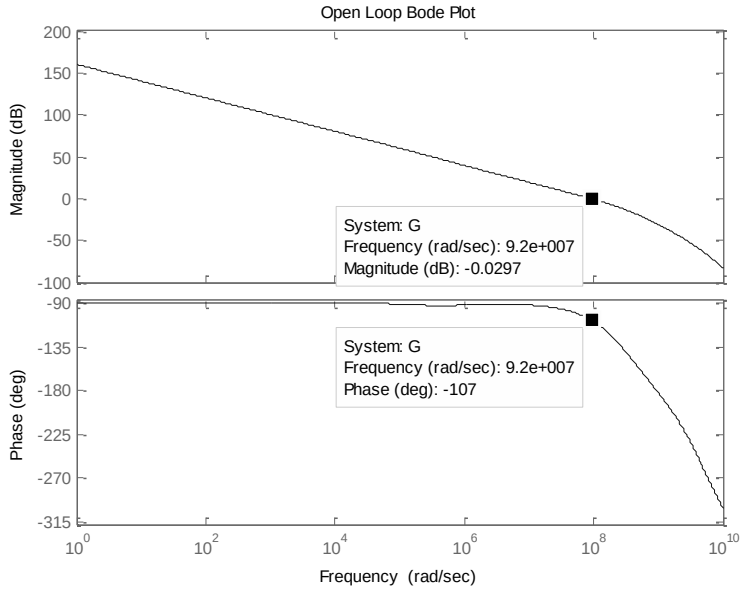

Figure 3-23: Simulated Bode Plots for Compensated Open Loop Transfer Function for Final Loop Filter Design (KV=600MHz/V)

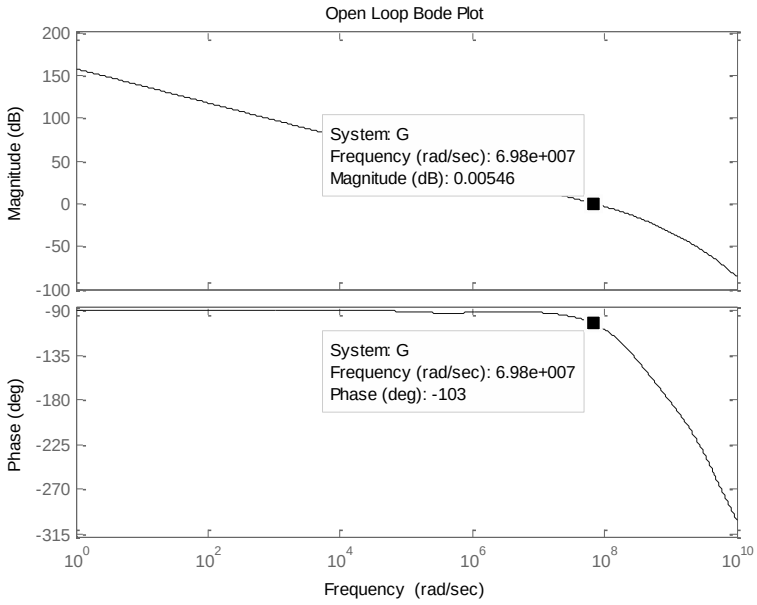

Figure 3-24: Simulated Bode Plots for Compensated Open Loop Transfer Function for Final Loop Filter Design (KV=450MHz/V)

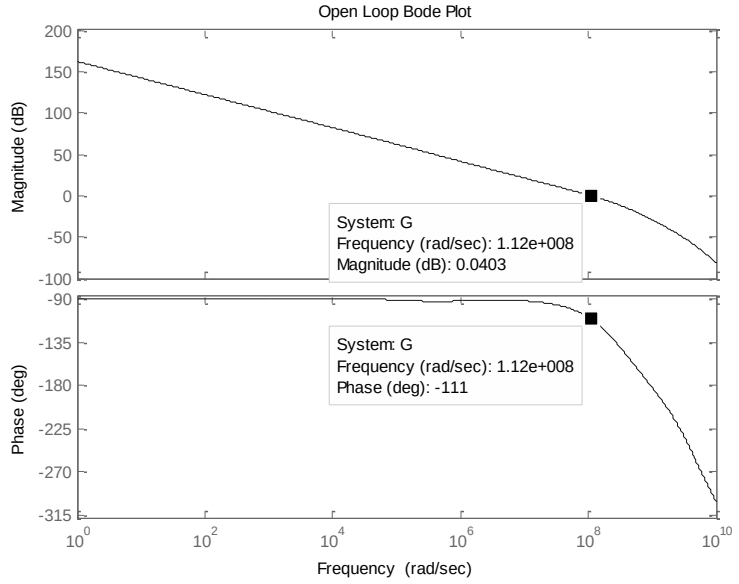

Figure 3-25: Simulated Bode Plots for Compensated Open Loop Transfer Function for Final Loop Filter Design (KV=750MHz/V)

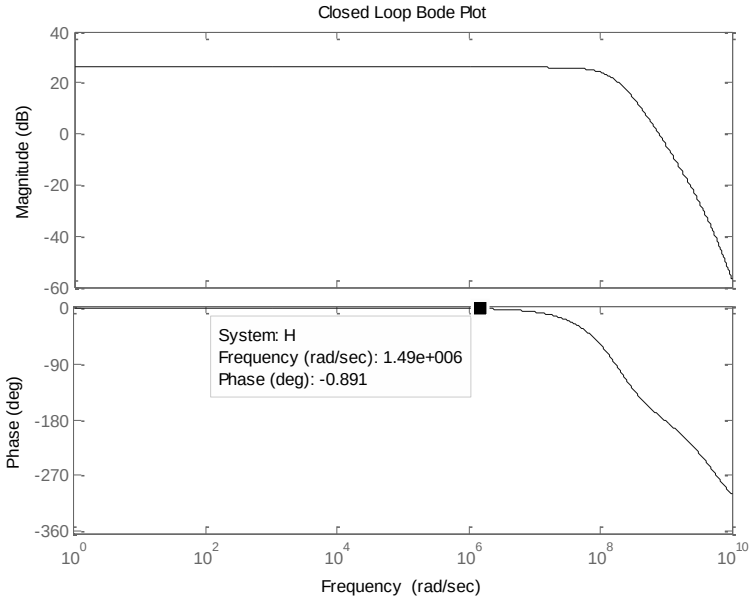

Figure 3-26: Simulated Bode Plots for Compensated Closed Loop Transfer Function for Final Loop Filter Design (KV=600MHz/V)

Figure 3-26 shows the simulated Bode plots for the Compensated Closed Loop Transfer Function. This plot shows a flat amplitude and phase response at low frequencies. This means that the loop filter has effectively compensated both for an improved tracking error at low frequencies. However, the plot shows that starting at about 237 kHz, the phase starts decreasing rapidly. This will cause some dispersion for compensation of broadband signals higher than this frequency. This is caused by the required large phase margin.

Table 3-3 lists the loop filter transfer function frequencies for the poles and the zero on the final design. The values for the resistors and capacitors of the final loop filter design are shown in Table 3-4.

Table 3-3: Solved Time Constants, Zero and Poles of the Final Loop Filter Design

Parameter	Value	Units
ω_{p1}	65.758	kHz
ω_{p2}	53.058	MHz
ω_{p3}	723.42	MHz
ω_{p4}	723.43	MHz
ω_{z}	72.3	kHz

Table 3-4: Solved Lumped Component Values of the Final Loop Filter Design

Parameter	Value	Units
R_1	100	Ω
R_2	1000	Ω
R_3	10	Ω
R_4	10	Ω
C_1	33	pF
C_2	2200	pF
C_3	22	pF
C_3	22	pF

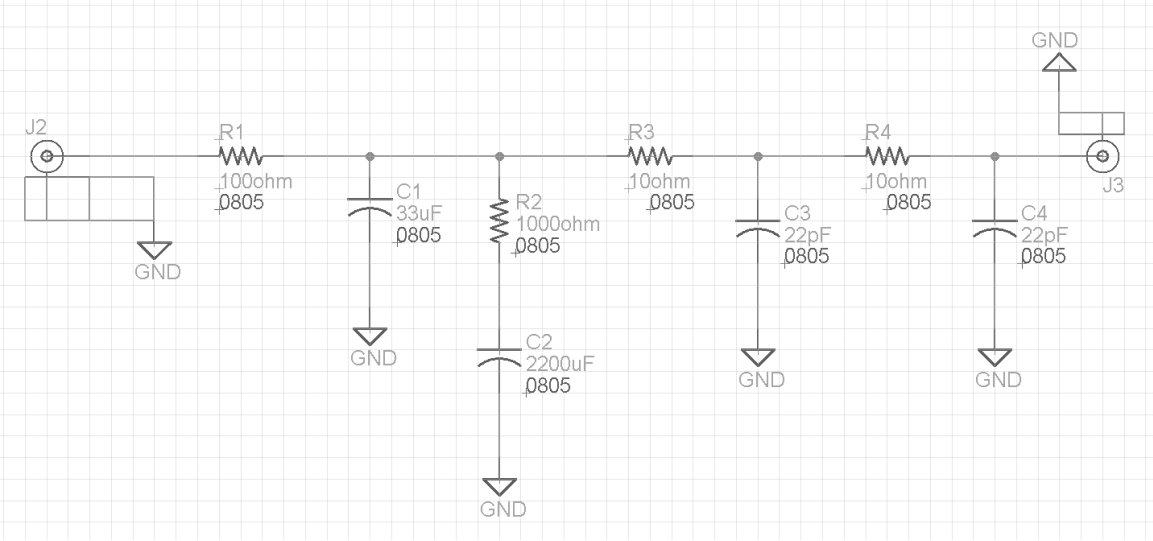

Figure 3-27: Circuit Schematic for the Final Design of the Loop Filter

3.4.7 PLL Circuit Implementation

Prototypes for the differential amplifier, adder and loop filter designs have been implemented on three separate printed circuit boards. This simplified the troubleshooting of each device and the entire forward path. The circuit boards have Sub-Miniature version A (SMA) connectors so that they can be connected with each other as well as with the rest of the evaluation boards using coaxial cables with SMA connectors. The three printed circuit boards (PCBs) have been fabricated on two layer FR4 substrate.

Because of the importance of high bandwidth and high frequency signals on the phase locked loop, some high frequency considerations have been taken in the implementation of the circuits. High speed operational amplifiers are sensitive to capacitive load, as mentioned in Chapter 1. Even though the circuit schematic has already been designed to minimize this issue, the PCB layout should also be considered to avoid this problem. If the output trace is sufficiently thick, a parasitic capacitance will result in a decrease on the amplifier phase margin. Capacitance at the input pins may also decrease the phase margin and even drive the amplifier unstable. For these reasons, the traces at the input and output pins are made very thin. A trace thickness of 10

mils was used for traces at the input and output pins. In addition, the copper from the ground plane has been removed below the input pin pads. This technique is highly suggested in the literature for high speed op amp applications [46].

The capacitors to filter the low frequency noise have been placed near the power supply connectors, whereas the high frequency bypass capacitors are placed as close to the bias voltage pins as possible. The PCB layouts for the differential amplifier, adder and loop filter are shown in Figures 3-28 through 3-32. The bottom layer of the loop filter is not shown, since no milling was required on the ground plane.

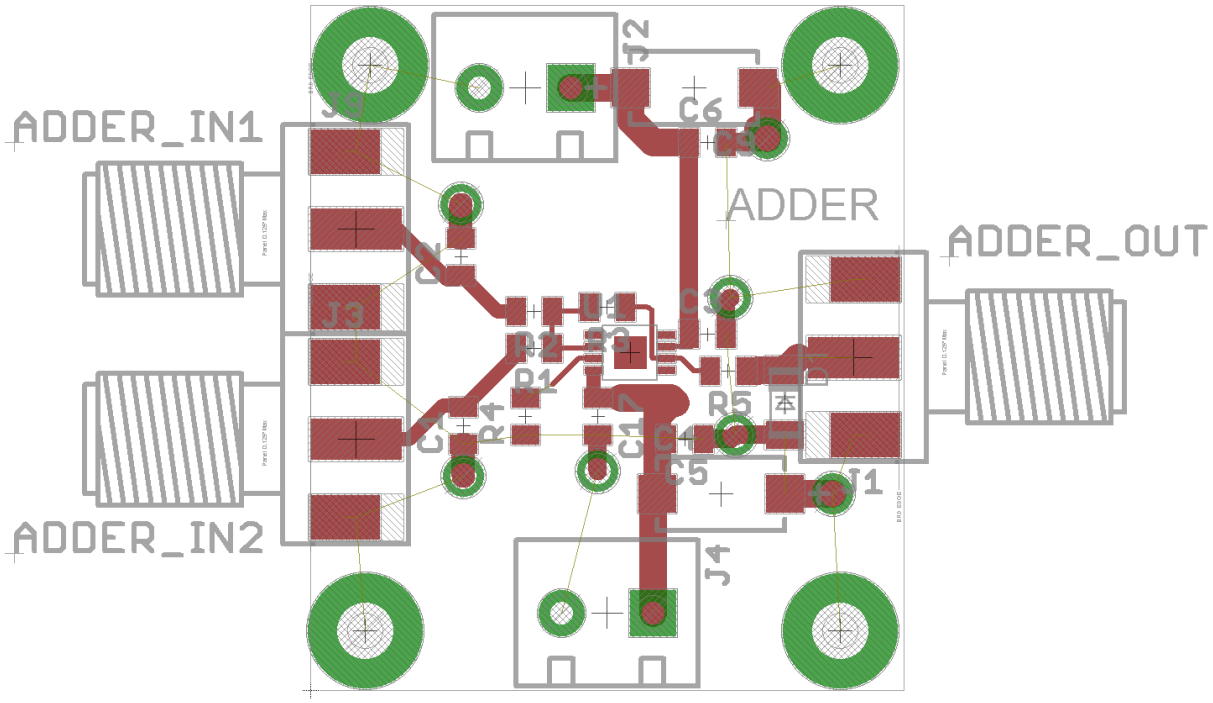

Figure 3-28: Adder Printed Circuit Board Layout

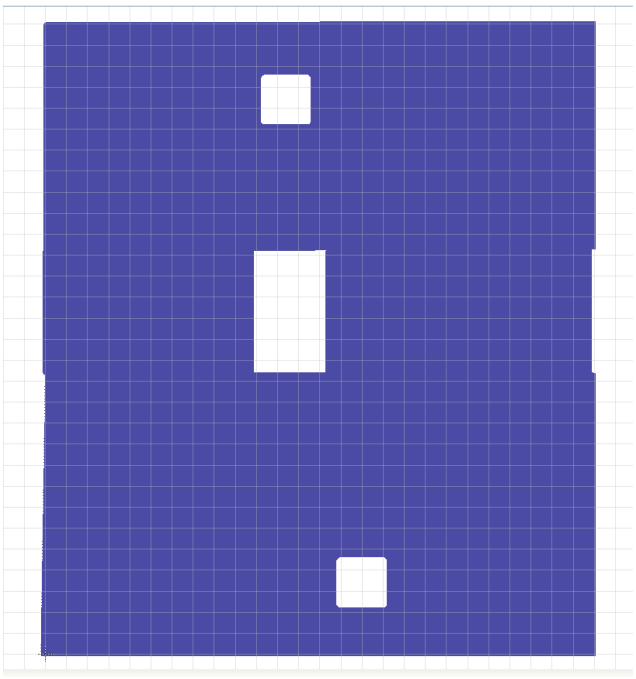

Figure 3-29: Bottom Layer of Adder Printed Circuit Board Layout

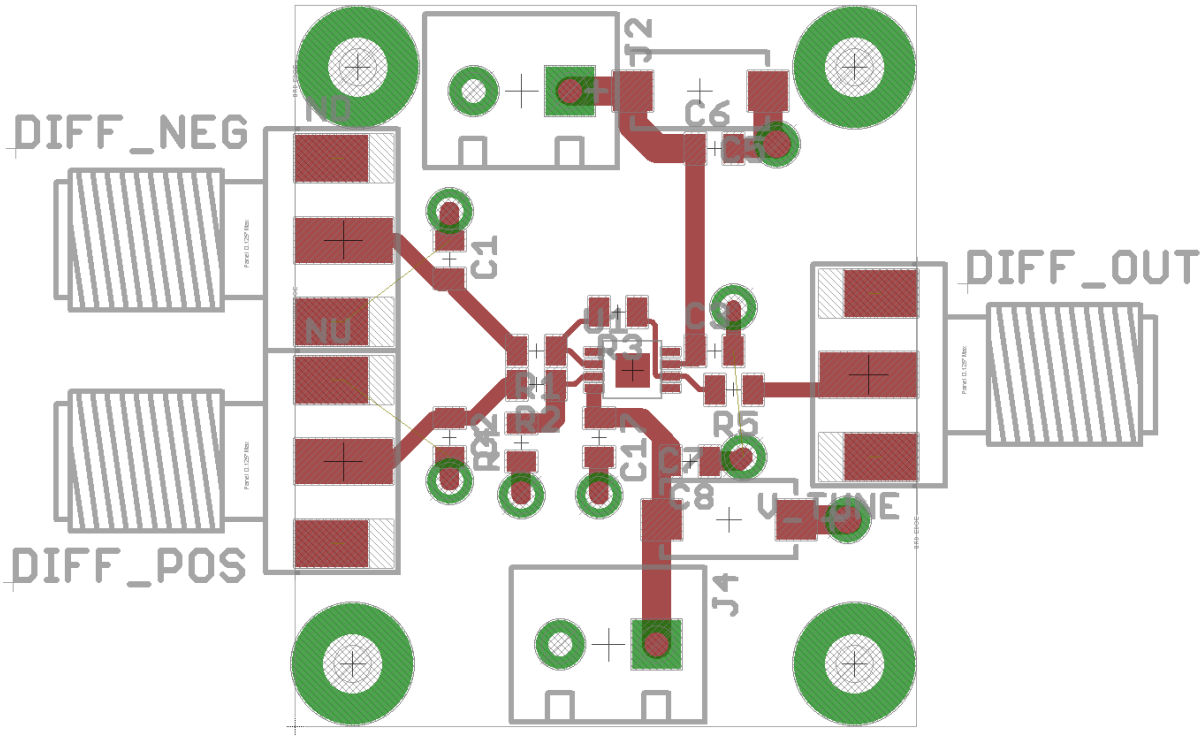

Figure 3-30: Differential Amplifier Printed Circuit Board Layout

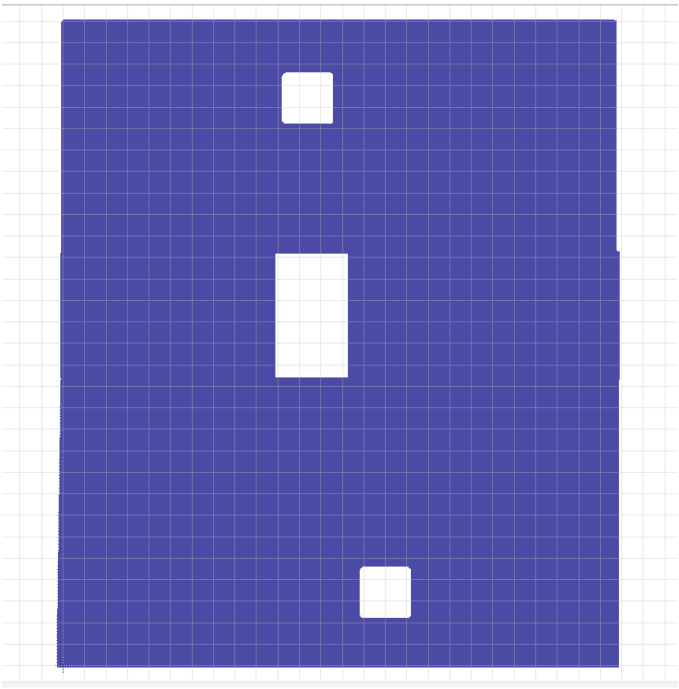

Figure 3-31: Bottom Layer of Adder Printed Circuit Board Layout

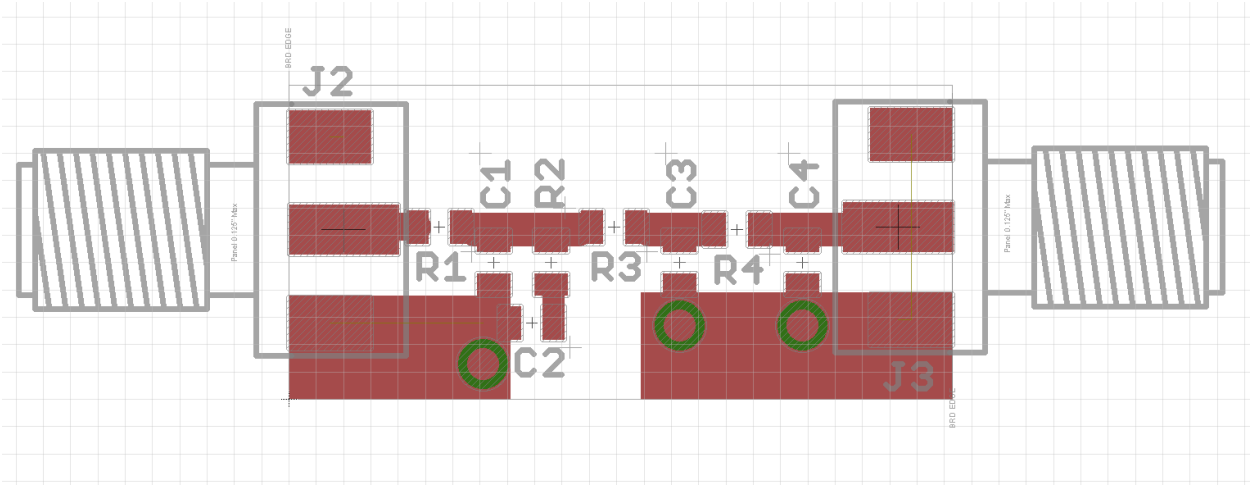

Figure 3-32: Loop Filter Printed Circuit Board Layout

3.5 PRE-DISTORTED VOLTAGE

3.5.1 Pre-Distorted Waveform

A PLL has been designed on the previous section to compensate for the wideband disturbances caused by small variations in the VCO tuning sensitivity. However, the loop filter has been designed with a phase margin of 73 degrees at an average tuning sensitivity of 600 MHz/V. This mean phase margin assures that the transient response will not cause peaking issue during the large variations of the tuning sensitivity. Moreover, the large variations of the tuning sensitivity will lower the loop bandwidth. For all these reasons, the wide loop bandwidth designed for the PLL may not be sufficient to compensate for all the significant disturbances caused by the small wideband variations on the VCO tuning sensitivity.

As mentioned in Chapter 2, the tracking performance can be improved by adding a signal with a fraction of the frequency content of the full compensation. This happens essentially because the externally compensation signal added to the loop has not been affected by the amplitude and phase variations of the control system response over frequency.

Moreover, the PLL designed is a type 1 PLL and the input signal that will be applied to the reference is a frequency ramp. As has been analyzed on Chapter 2, type 1 PLLs have finite phase steady state errors for ramp and step inputs only. It has also been shown that an external signal can be used to compensate for the phase parabola input (frequency ramp input). Then, the type 1 PLL compensates for the residual phase step and phase ramp signals at the input.

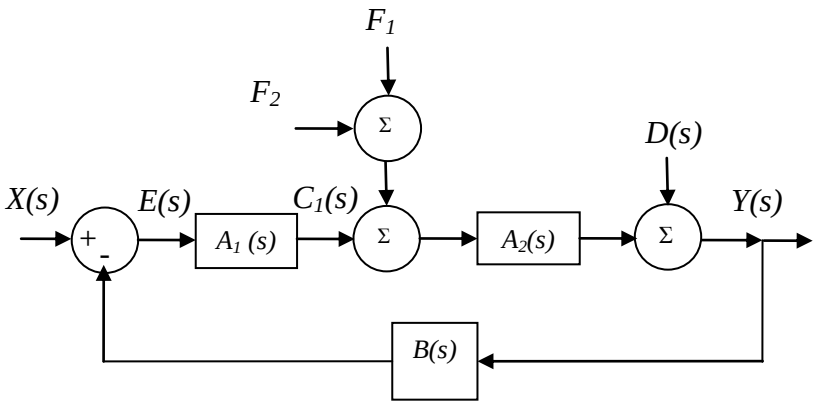

Figure 3-33: Proposed Dual Compensation Control System Block Diagram

$$Y = X_1 \frac{A_1 A_2}{1 + BA_1 A_2} + A_1 A_2 \frac{X_2 - BA_2 F_1}{1 + BA_1 A_2} + (D + A_2 F_2)\left[1 - \frac{A_1 A_2 B}{1 + A_1 A_2 B}\right] \tag{3.48}$$

$$X_1 = \frac{\theta_o}{s} + \frac{f_o}{s^2} \tag{3.49}$$

$$X_2 = \frac{1}{2}\mu \frac{2!}{s^3} \tag{3.50}$$

$$X = X_1 + X_2 \tag{3.51}$$

$$A_1 = K_P \cdot Z \tag{3.52}$$

$$A_2 = \frac{K_V}{s} \tag{3.53}$$

$$B = \frac{1}{N} \tag{3.54}$$

Figure 3-33 is a block diagram that describes the control loop with added compensation and added disturbance. For consistency, this block-diagram uses the same system symbols and signal symbols that have been used earlier for examples. Likewise, the signals and systems are represented by their Laplace transform, as the rest of the linear system block-diagrams on this document. Equation (3.48) describes the output signal of the proposed control system. The input of the system is a frequency ramp or phase parabola with initial phase and initial frequency components. The input signal is described in equations (3.49), (3.50) and (3.51). The equivalence between the block diagram system symbols and the PLL symbols is described in

equations (3.52), (3.53) and (3.54). The first summand on equation (3.48) is related to the phase step and phase ramp inputs being compensated by the PLL. The second summand is related to the frequency ramp input compensated by the first external compensation signal (F_1). The third summand is related to the disturbance being compensated by both the PLL and the second external compensation signal (F_2). In order to make the phase steady state error a finite value, the external compensation F_1 needs to have the expression found in equation (3.55). This means that F_1 is a voltage ramp with a voltage rate equal to the mean voltage rate of the required VCO tuning voltage.

$$F_1 = \frac{X_2}{BA_2} = \frac{\mu N}{K_V} \cdot \frac{1}{s^2} \tag{3.55}$$

The third summand has two products. The second product of the third summand will approach zero over the frequencies in the passband of the PLL. Thus, the third summand will approach zero as well and the disturbances will not affect the output. The first product on the third summand will become zero when equation (3.56) is satisfied. This way the second external signal compensates for the disturbances over some frequency range.

$$F_2 = -\frac{D}{A_2} \tag{3.56}$$

In order to find the right external compensation signal which is described by the ideal expressions in equations (3.55) and (3.56), the PLL compensation signal C_1 can be measured. This compensation signal has suffered the frequency response effects of the PLL loop and it is not a perfect compensation. However, it has the information to improve the compensation. This signal can be measured and equalized to obtain a better compensation signal.

The type 1 PLL cannot achieve a finite steady state response for a ramp frequency input and cannot obtain the required voltage level to drive the VCO without external compensation. Therefore, a type 2 PLL active loop filter should be used for the first measurement of the PLL compensation signal. Equation (3.57) shows the expression for the PLL compensation signal for this first measurement. This signal will approach the expression shown in (3.58) over the passband of the PLL. The expression on equation (3.58) resembles that of the required total external compensation (F). Thus, this signal can be used to generate an external compensation

signal. By applying this first generated compensation signal, the PLL compensation signal can be measured again using the designed type 1 PLL loop filter.

$$C_1 = A_1 \frac{X - DB}{1 + A_1 A_2 B} \tag{3.57}$$

$$C_1 \approx \frac{X_2}{BA_2} - \frac{D}{A_2} \tag{3.58}$$

Since the new measured C_1 corresponds to the residual disturbance signal, which the external compensation is not already correcting for, it can be used to improve the external compensation even further. This signal can be equalized in phase and amplitude and added to the current external compensation signal. The total external compensation signal applied to the PLL is a voltage signal and will be referred as the pre-distorted voltage.

The designed PLL contains a high speed unity gain inverting adder amplifier on the forward path. One of the inputs of the adder is connected to the output of the loop filter. The other input will be used to insert the pre-distorted waveform into the loop.

The DC coupled channel of the 2-Channel DDS described on Appendix A can output a DC waveform between 200 and 2200 mV when coupled to a load with 50 ohms of impedance. Moreover, the AD9910 DDS has a 1024x32 bit of random access memory (RAM) that can be used to modulate the amplitude of the DC coupled channel over a specified time interval. This means that the amplitude of the pre-distorted signal can be sampled with 1024 points at each chirp repetition interval. By sampling 1000 points over the required chirp sweep time of 250 μs, the sampling rate becomes 4 MHz. Thus, a reconstruction filter should be implemented to reject frequencies above 2 MHz.

The VCO tuning voltage range required for the system is between about 3.3 to 13.3 Volts. Thus, a circuit is required to convert the output of the DC-coupled channel to the signal expected by the input of the adder. The circuit should also be able to filter the signal for proper reconstruction.

3.5.2 Level Shifter Amplifier Design and Implementation

A level shifter amplifier is designed to convert the voltage output of the DDS board DC couple channel to an inverted signal of the required tuning voltage. The output of the level shifter amplifier will be connected to the adder with a 1360-ohm input impedance. The DC coupled channel requires a 50-ohm load impedance for proper functionality. Thus, the level shifter amplifier should have a 50-ohm input impedance and output impedance much lower than 1360 ohm.

The level shifter amplifier will be realized with an adder amplifier similar to the one used on the PLL. One of the inputs of the adder will connect to the DDS DC coupled channel, whereas the other input will be connected to a fixed voltage that will set the voltage offset. For an inverting amplifier, the ratio of the feedback resistance to the resistance connected to the inverting pin sets the gain for each input. The equation that relates the two inputs to the output of the adder with different gains is presented in Equation (3.59), where the variables associated with subscript 1 correspond to the offset signal and the variables associated with subscript 2 correspond to the input of the level shifter amplifier.

$$V_{out} = V_1 \cdot \left(-\frac{R_f}{R_1} \right) + V_2 \cdot \left(-\frac{R_f}{R_2} \right) \tag{3.59}$$

A regulated voltage of negative 5 Volts will be used as the input offset signal. For an output voltage range of 3.3 to 13.3 Volts and the input voltage range selected of 662.5 V to 1.9125 Volts, the required gains and resistance values are shown in Table 3-5.

Table 3-5: Solved Gains and Resistor Values for Level Shifter Amplifier Circuit

Parameter	Value
G_1	0.4
G_2	8
R_f	2 kΩ
R_1	5 kΩ
R_2	250 Ω

A two pole filter can be realized on the level shifter amplifier without modifying its original function by adding a feedback capacitor and a low loss RC output filter. A feedback capacitor of 82 pF combined with the 2000 Ω feedback resistor form a pole at 970.5 kHz. An RC filter formed by a 1 ohm resistor and a 100 nF capacitor form a pole at 1.59 MHz. Figure 3-34 shows the Bode plots for the level shifter amplifier from the DC coupled input to the output. The plot shows an attenuation of 15 dB to the first harmonic at 4 MHz.

The input of the amplifier has been terminated with a 50 ohm resistance in shunt. Because of the high impedance of the adder amplifier, the equivalent input impedance of the level shifter amplifier becomes 48.91 Ω. The level shifter amplifier uses a THS4031 operational amplifier [54]. It has a full power bandwidth of 4.6 MHz for a voltage swing of 10 V. This is sufficient for this implementation. Figure 3-35 shows the circuit schematic.

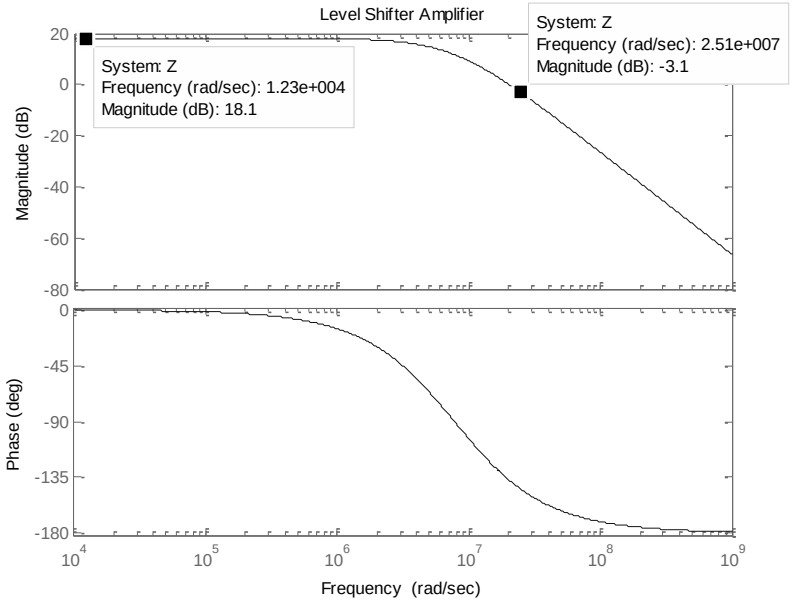

Figure 3-34: Simulated Bode Plots for the Level Shifter Amplifier

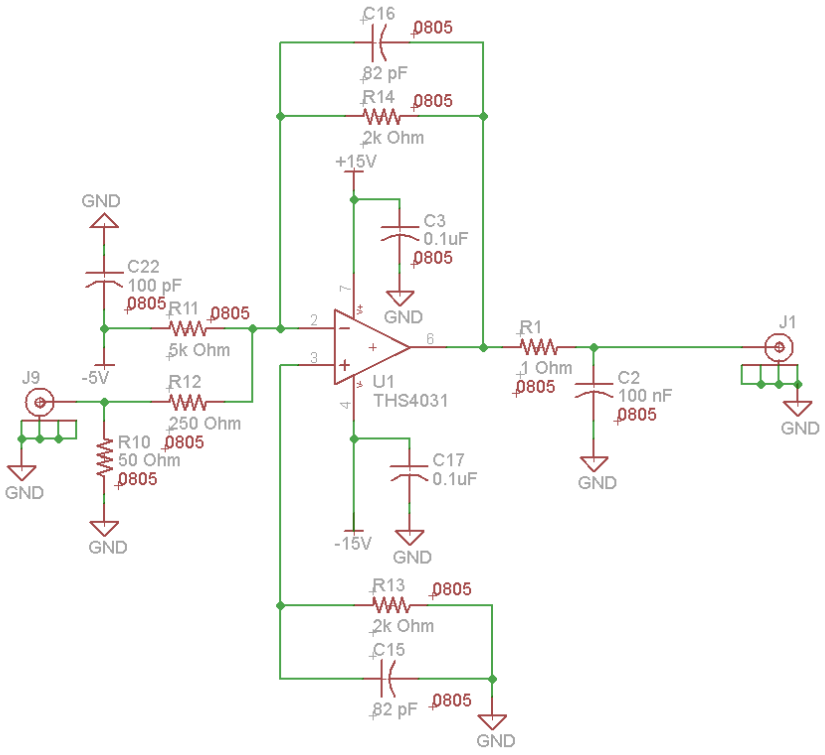

Figure 3-35: Circuit Schematic of the Level Shifter Amplifier

The level shifter amplifier PCB layout is shown in Figure 3-36. The PCB was milled on a two layered copper board with an FR4 substrate. The circuit has bypass capacitors to filter the bias voltages. The input and output have SMA connectors to connect the circuit to the DDS board and the adder amplifier on the PLL.

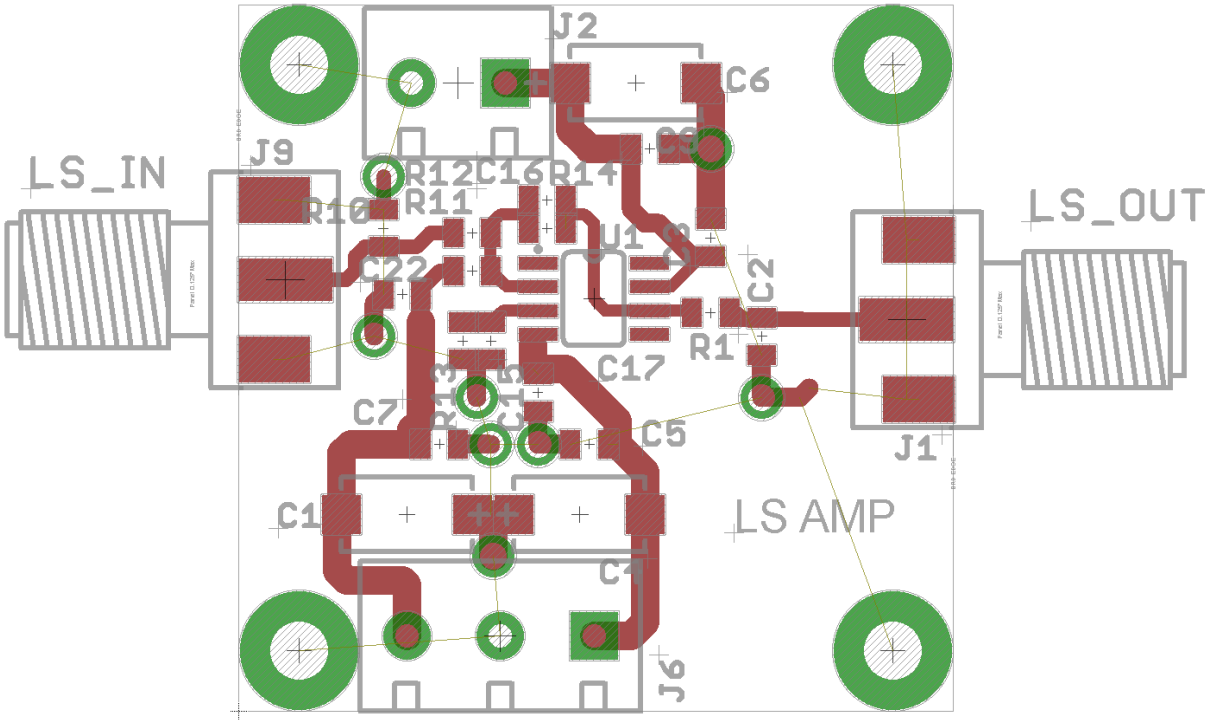

Figure 3-36: Printed Circuit Board Layout for Level Shifter Amplifier

3.5.3 Start up Loop Filter Design and Implementation

As explained in Section 3.5.1, the first measurement of the PLL compensation signal cannot be performed using the designed type 1 PLL loop filter. This is because it cannot output the required voltage level to drive the VCO. Moreover, it is a type 1 PLL loop filter for which the PLL will not achieve a finite steady state error to a frequency ramp input. Thus, an active type 2 loop filter has been selected to be used for the first measurement.

As it has been already explained in Chapter 2, active loop filters are not the optimal choice for high loop bandwidth PLL designs. However, the start-up active loop filter need not have high bandwidth or be designed for a high loop bandwidth PLL.

The start-up active filter is a second order filter designed for the type 2 PLL. The relevant PLL parameters used for the design are listed in Table 3-6.

Table 3-6: PLL Parameters for Start-Up Active Loop Filter

Parameter	Value	Units
VCO Tuning Sensitivity, K_V	600	MHz
Phase Detector Gain, K_P	4	V/2π rads
Division Quotient, N	20	
Loop Bandwidth, F_o	1	MHz
Phase Margin, φ	50	Degrees

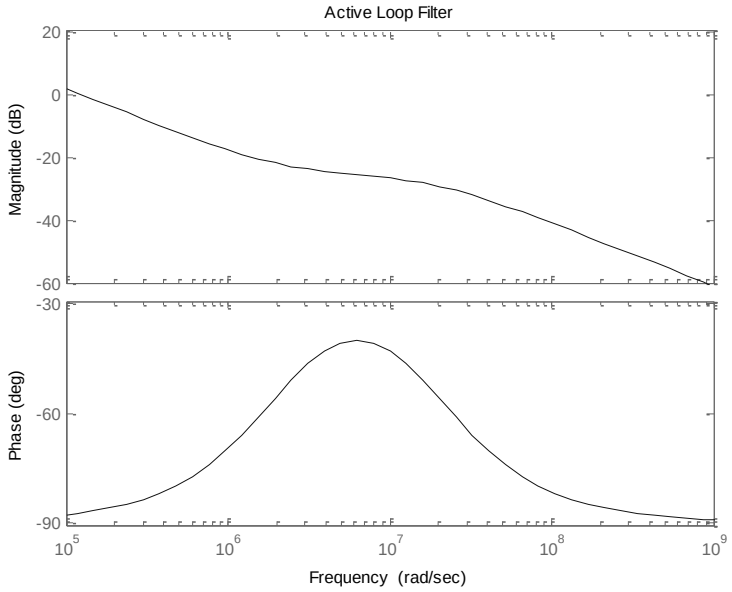

Figure 3-37: Bode Plots for Start-up Active Loop Filter Transfer Function

Since the active loop filter will be directly connected to the output of the phase detector evaluation board, there will be no buffering stage to isolate the current output. Thus, the active loop filter has been designed to have high input impedance. Having high input impedance, the phase detector 10 mA current causes a drop of 2 volts on each of the 200 ohm pull up resistors. This results in a differential phase detector gain of 4 Volts per cycle, as listed in Table 3-6.

Figure 3-37 shows the Bode plots of the start-up active loop filter. The plot shows the typical response of a type 1 loop filter for a type 2 PLL. It has a pole at the origin, a medium frequency zero for phase margin correction and a high frequency pole for high frequency attenuation.

The Bode plots for the compensated open loop transfer function are shown in Figure 3-38. The frequency response shows a crossover frequency at 1 MHz and a phase margin of 50 degrees. The simulation agrees with the design parameters. The solved lumped component values are shown on the schematic.

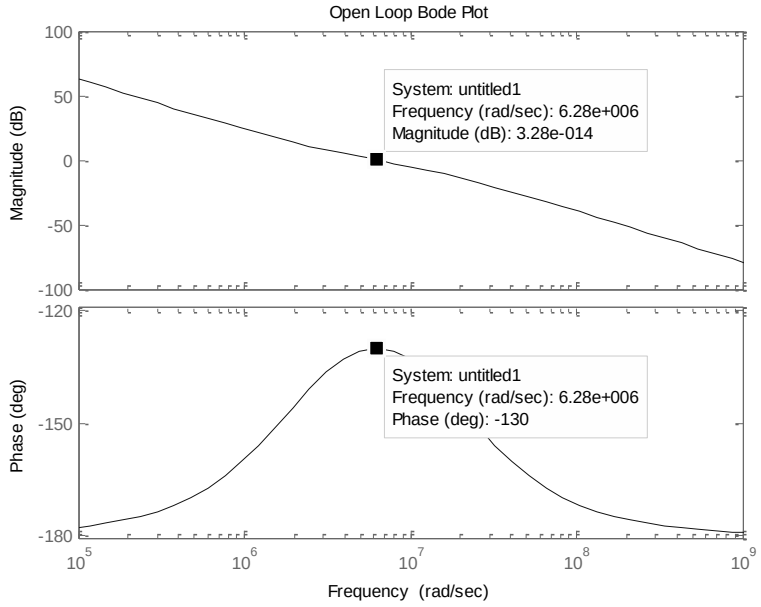

Figure 3-38: Bode Plots for the Open Loop Compensated with the Start-up Loop Filter

The active loop filter has been implemented using the same guidelines used for the differential amplifier for optimal performance. The schematic and layout are shown in Figures 3-39 and 3-40. It has been fabricated using a two-layered copper board with FR4 substrate.

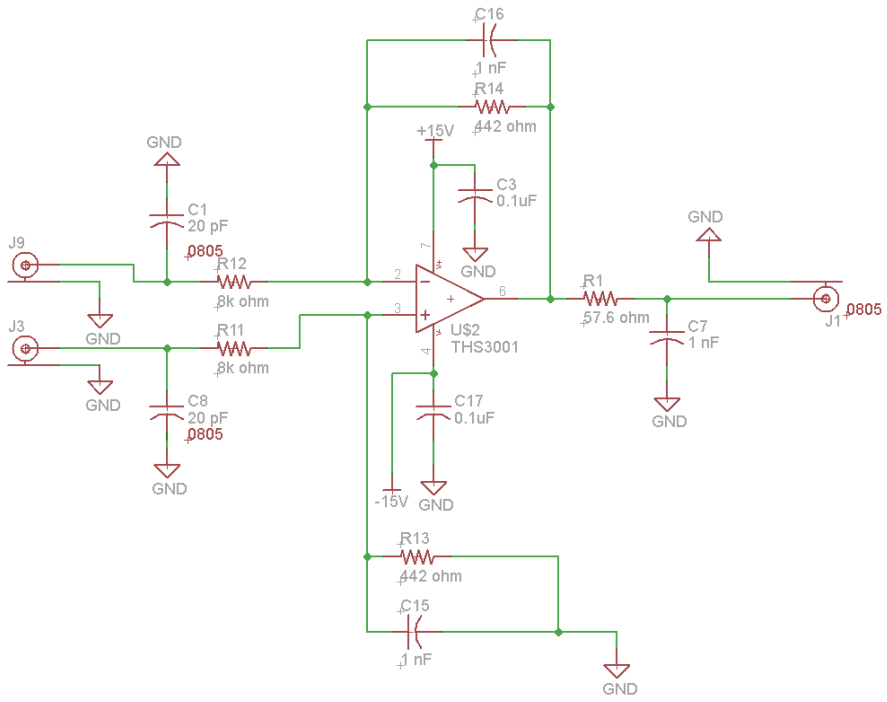

Figure 3-39: Start-up Active Loop Filter Schematic

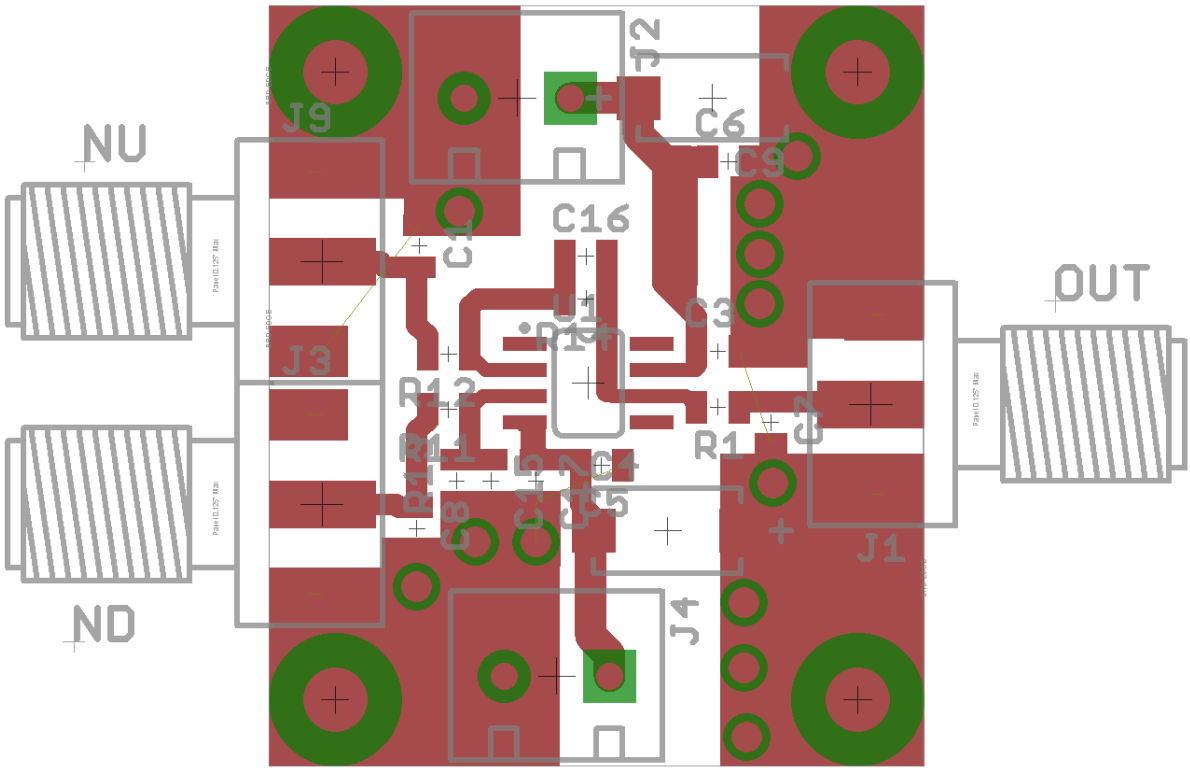

Figure 3-40: Start-up Active Loop Filter Layout

3.5.4 Pre-Distorted Signal Generation Procedure

As explained in Section 3.5.1, the required total external compensation signal can be derived from the PLL compensation signal. This is the signal at the output of the loop filter and the input of the adder.

Figure 3-41 shows a system level block diagram that describes the measurement procedure of the PLL compensation signal (C_1), the processing given to this signal, and the application of the generated pre-distorted voltage (F). The block diagram shows that the PLL compensation signal is measured at the output of the loop filter. This signal is first digitized by an ADC. The output signal of the ADC goes through a digital low pass filter (H). Subsequently, the output signal of the filter is applied to an advance system (z^n) that compensates for the delay introduced by the filter, as well as any other delays caused by the PLL. Similarly, the digital signal then goes through an amplifier with gain K_M to compensate for any attenuation given the inherent frequency response of the PLL compensation signal. This amplified signal goes through another gain stage (K_W) that maps the digital signal magnitude to a digital value accepted by the DAC. This final digital value, which is applied to the input of the level shifter amplifier, should correspond to the desired voltage level at the output of the Level Shifter Amplifier (LSA).

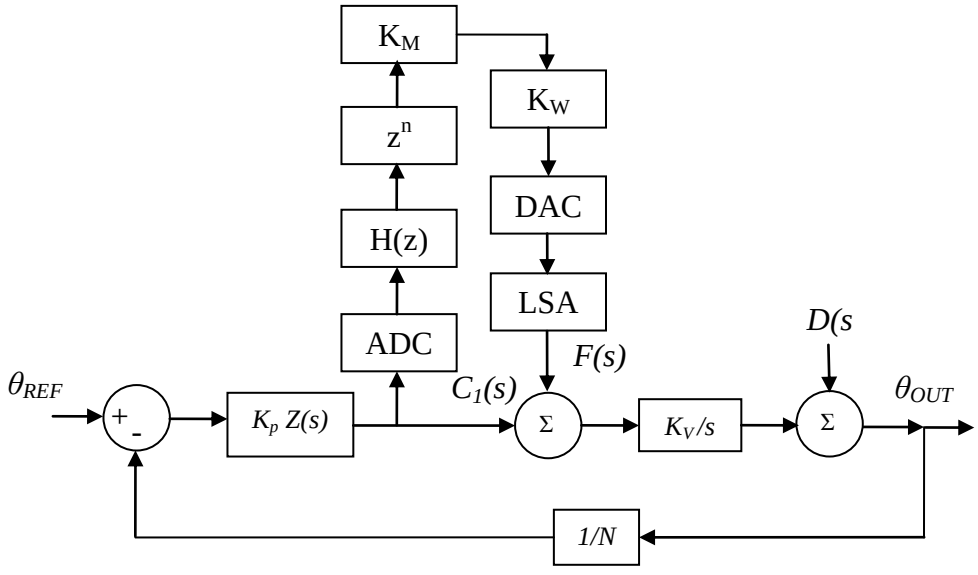

Figure 3-41: System Level Block Diagram for the Pre-Distorted Voltage Generation

In order to realize this measurement, an SMA T-connector has been inserted between the loop filter and the adder. The third end of the T-connector is connected to one of the high impedance channels of a 4 Channel 1 GSPS Tektronix DP02014 Oscilloscope. The extended pulse repetition interval (EPRI) signal provided by the 2 Channel DDS board also connects to one channel of the oscilloscope. The EPRI provides the trigger signal for the oscilloscope; it is also used as a reference point for the measurements. The loop filter output and the trigger signal are recorded by the oscilloscope using a Universal Serial Bus (USB) flash memory drive. Then, a computer is used to read the data and process it. The processed digital points are used to program the DDS DC coupled channel output. The output signal of the DDS DC coupled channel is applied to the level shifter amplifier designed to achieve the required voltage level. A high level block diagram of the measurement setup is shown in Figure 3-42.

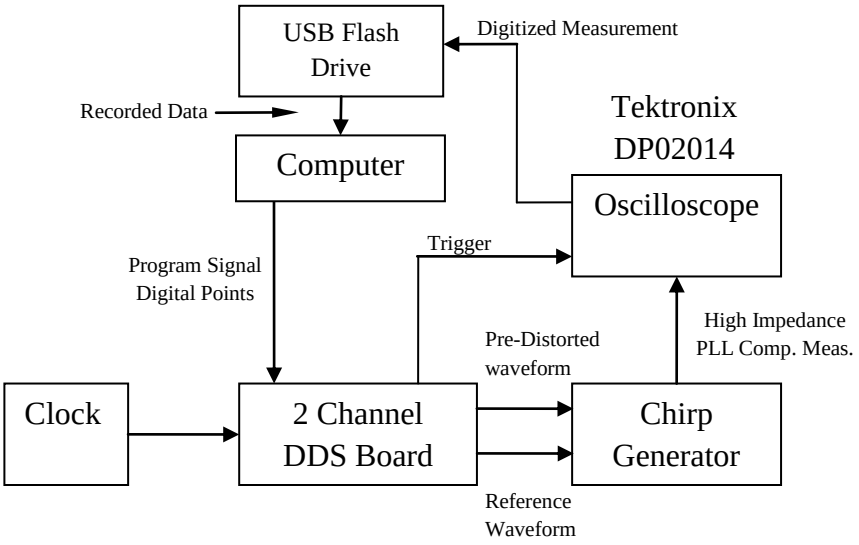

Figure 3-42: PLL Compensation Signal Measurement Setup

In order to improve the compensation given by the PLL, the measured compensation signal needs to be equalized. For this reason a digital low pass filter is used. The digital filter used is a Finite Impulse Response (FIR) filter which has been implemented using Matlab [25]. The filter coefficients have been computed by using the FIR1 function provided by Matlab. The filter was then applied using the FILTER function, also provided by Matlab.

The measurements have been realized in a series of steps. For the first step, the start-up filter was used to measure the PLL compensation without any external compensation. The measured signal was processed to generate the first pre-distorted voltage signal. Then, the loop filter was changed to the type 1 PLL loop filter designed. Then, the PLL compensation signal was measured. This time the pre-distorted voltage was applied. The measured signal on this case corresponded to the residual disturbance. In order to reconstruct an improved version of this signal, the signal had to be divided in frequency regions. To this end, the compensation signal has been measured and processed in many steps, where the low pass filter bandwidth has been increased for every step. For every step, the filtered signal delay and amplitude has been adjusted. This has been done with trial and error by looking at the PLL compensation signal on the oscilloscope.

CHAPTER 4: MEASUREMENTS AND RESULTS

4.1 PHASE LOCK LOOP PERFORMANCE MEASUREMENTS

The PLL time response performance can be indirectly measured from the frequency spectrum performance as long as there are no limitations other than bandwidth. The only possible limitation other than bandwidth for the time response is the slew rate of the operational amplifiers used on the forward path of the loop.

Given the designed loop bandwidth of 14.64 MHz for the system at a K_V of 600 MHz/V, the time constant for a single pole system would be 10.87 ns. A rough estimate of the settling time is about 5 times the time constant, which corresponds to 54.35 ns. Figure 4-1 shows a simulation of the step response of the designed closed loop system at a K_V of 600 MHz/V. The simulated step response shows a settling time of 51.6 ns.

A slew rate of 1 V per 153 ps would not be a lower limitation than the bandwidth. The slew rate for the THS3001 opamp being used corresponds to a full power bandwidth of 32 MHz for a voltage swing of 20 V. This limitation is beyond the crossover frequency. Thus, the opamps will not cause distortion to a signal on the forward path of the PLL.

Moreover, a settling time measurement can only be performed effectively at the free running frequency of the VCO, which is around 10 GHz. This is because the type 1 PLL has a limited pull in range defined by the output voltage of the phase detector. The reference frequency required would be around 500 MHz and the VCO tuning sensitivity would be too high for the designed PLL and could cause high overshoots. Also, the loop filter will not be able to attenuate significantly the 500 MHz reference spurs. Thus, a settling time at the free running frequency would not provide useful information about the time response of the PLL. Thus, the PLL frequency spectrum at discrete frequencies with a tone at the reference port will be used to indirectly measure the response of the PLL.

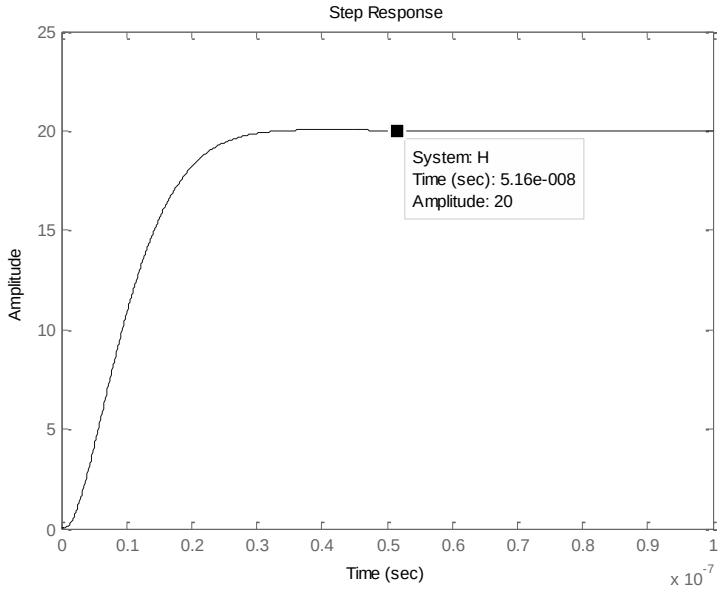

Figure 4-1: Simulated Step Response for PLL with a KV of 600 MHz/V

The loop bandwidth of the PLL is equal to the noise bandwidth on a single tone output of the PLL [39]. The noise bandwidth, along with the noise and spur level, can be measured using the frequency spectrum. Figure 4-2 is a representation of a typical spectral plot for a tone output. The plot shows how to identify the relevant parameters mentioned.

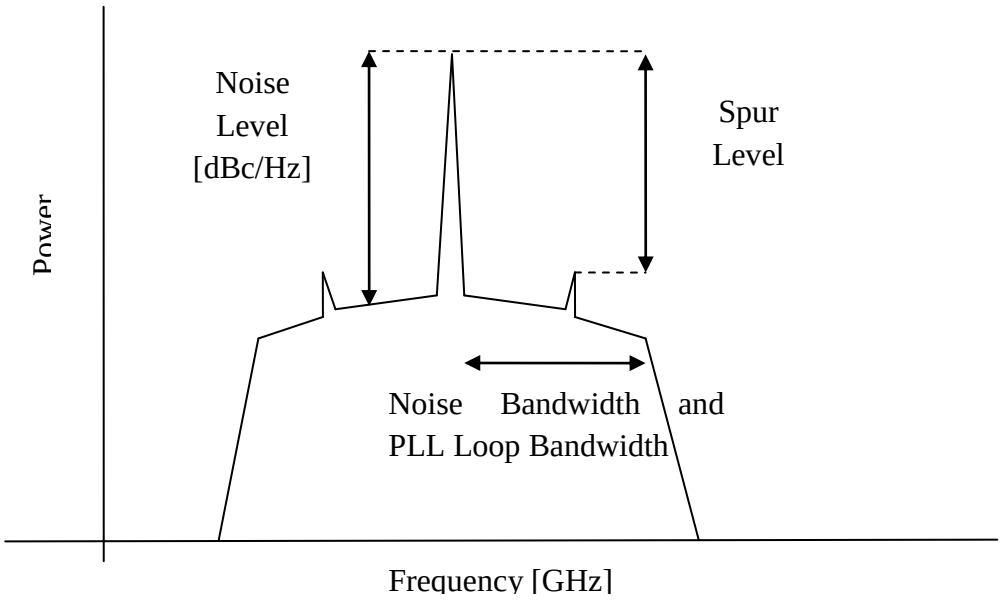

Figure 4-2: Typical Phase Noise Spectral Plot for a PLL

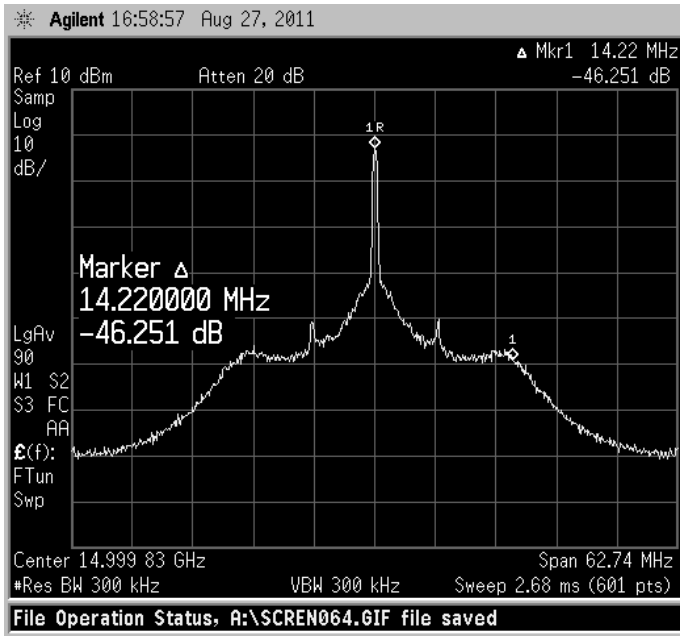

Figure 4-3: PLL Spectral Measurement at 15 GHz

The frequency spectrum measurements were performed on an Agilent E4446A Spectrum Analyzer. Figure 4-3 shows a screenshot of the PLL spectral measurement at 15 GHz on the spectrum analyzer. The screenshots for the all other frequencies measured can be found in Appendix B. Table 4-1 summarizes the PLL performance measurements.

Table 4-1: PLL Spectral Performance Measurements

PLL Frequency [GHz]	Loop Bandwidth [MHz]	Spur Level [dBc]
12	13.67	39
13	15.03	45
14	14.33	48
15	14.22	40
16	15.91	45
17	15.26	45
17.5	13.95	38
18	3	<36.8

The loop bandwidth varies at different PLL output frequencies as expected mainly due to the variations on the VCO tuning sensitivity. The loop bandwidth values are close to the ones expected by design. The loop bandwidth designed for an average tuning sensitivity of 600 MHz/V is 14.64 MHz and the measured loop bandwidth at the center frequency (15 GHz) is 14.22 MHz. The K_V values used in the design were inferred from the VCO manufacturer's datasheet. Each manufactured VCO, however, has a slightly different tuning curve. This could have affected the loop bandwidth slightly.

4.2 PRE-DISTORTED SIGNAL MEASUREMENTS

The measurement procedure was described in Section 3.5.4. Initially, the DC coupled channel output of the DDS has been characterized using a programmed digital ramp input to produce a voltage ramp. This measurement was done over the entire tuning range and used as a reference to map the programming digital words to the output voltage. The related measurements are not shown since they are not related to the performance of the pre-distorted voltage.

As mentioned in Section 3.5.4, a series of steps was performed to generate the pre-distorted voltage. At each step the bandwidth of the digital low pass filter was modified. As has already been mentioned, the sampling rate of the waveform generator is 4 MHz, which corresponds to a Nyquist bandwidth of 2 MHz. For this reason, the digital low pass filter bandwidth was linearly increased at each step up to 2 MHz. At each step, the PLL compensation signal has been amplified and advanced and the amount of amplification and time advancement

was decided by trial and error. At each step, the processes signal, which corresponds to the residual disturbance, was added to the external compensation signal. The sampling rate of the Oscilloscope used was 250 MHz. The measured data was sampled again at 80 MHz. The low pass filters have been designed with the FIR1 function of Matlab using to the sampling frequency and the required bandwidth.

Moreover, there was an issue during the measurements that affected the measurement procedure. The measured compensation voltage at the oscilloscope had an increasing voltage step. This voltage step changed with time and was related to the amount of time that the DC couple channel was turned on. To compensate for this issue, the digital low pass filter bandwidth was lowered to 250 kHz, which helped correct for the step without adding unnecessary high frequency content.

Table 4-2 summarizes the digital low pass filter bandwidths used at each step. Figure 4-4 shows the PLL compensation signal measured using the start-up active loop filter. For this case, this voltage is the tuning voltage applied by active loop filter. Figures 4-5 through 4-12 show the processed PLL compensation signal for each step using the type 1 PLL loop filter.

Table 4-2: Digital Low Pass Filter Bandwidth List

Step #	Bandwidth	Units
1	160	kHz
2	160	kHz
3	528	kHz
4	896	kHz
5	1.26	MHz
6	250	kHz
7	1.63	MHz
8	2	MHz

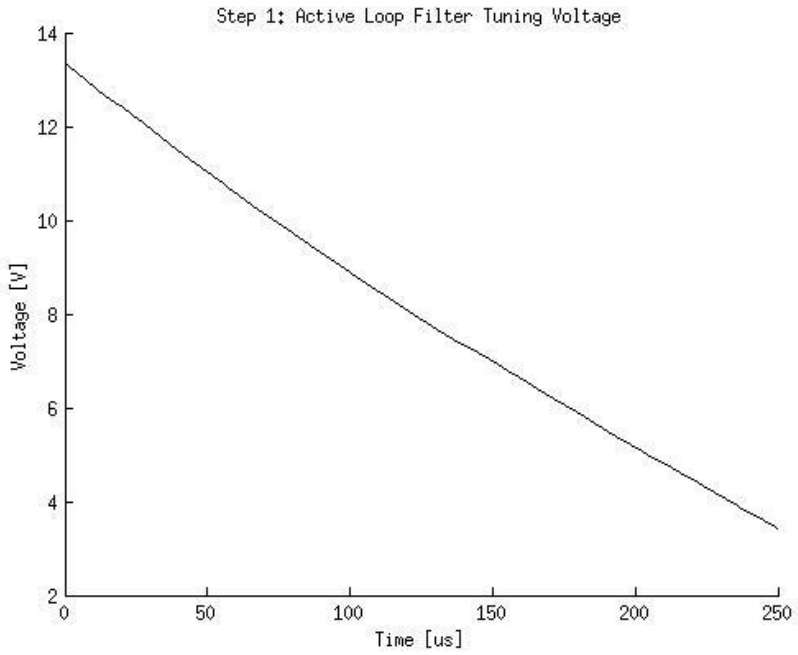

Figure 4-4: Active Loop Filter Tuning Voltage

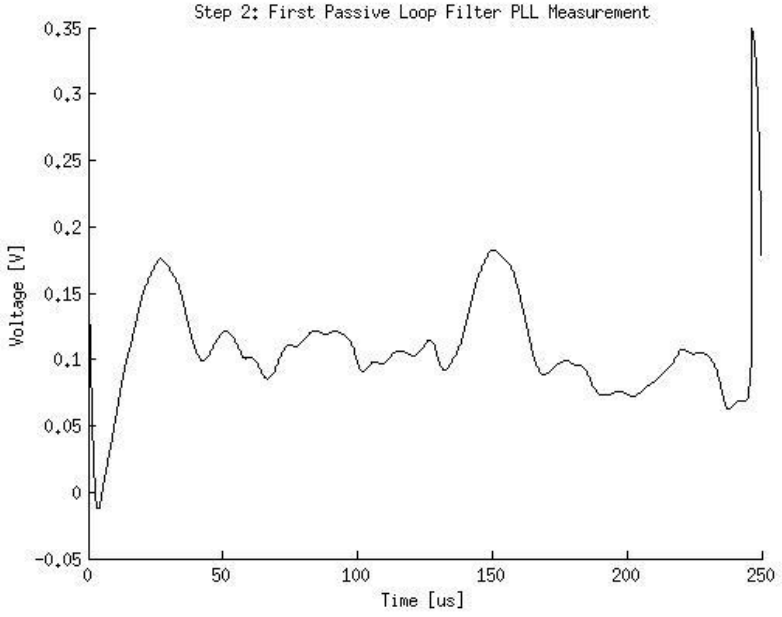

Figure 4-5: Processed Compensation Signal Measurement Step 2

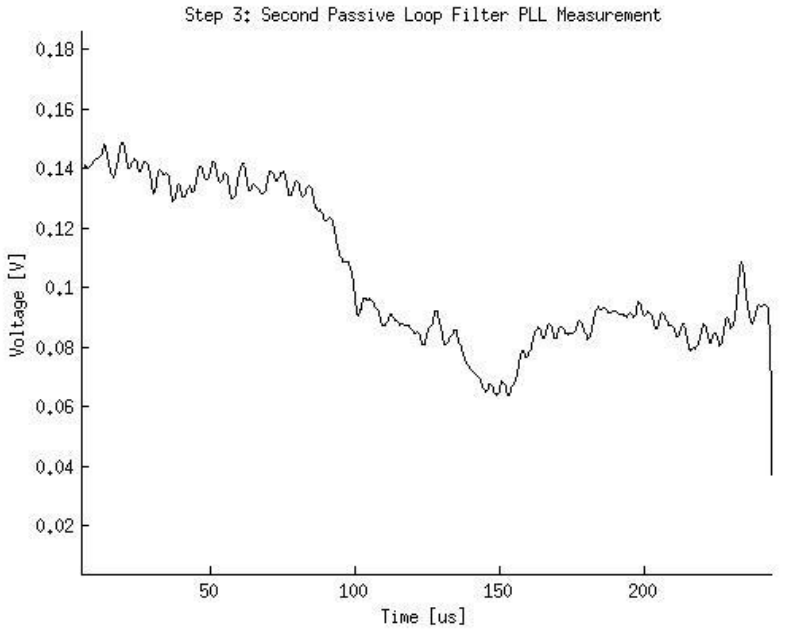

Figure 4-6: Processed Compensation Signal Measurement Step 3

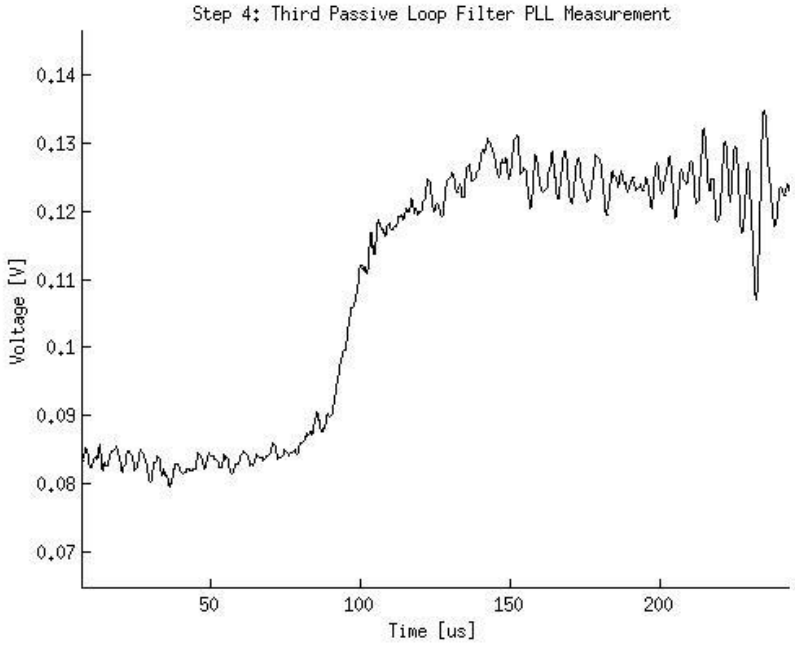

Figure 4-7: Processed Compensation Signal Measurement Step 4

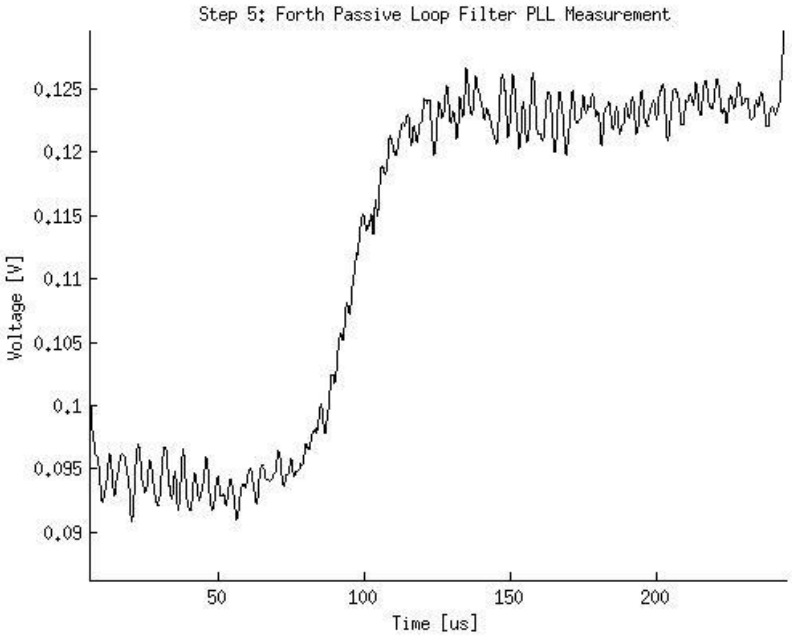

Figure 4-8: Processed Compensation Signal Measurement Step 5

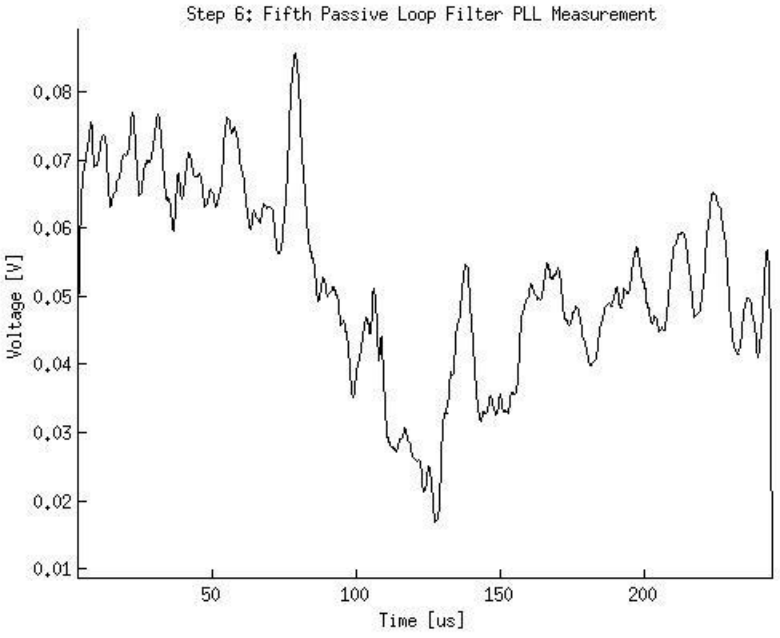

Figure 4-9: Processed Compensation Signal Measurement Step 6

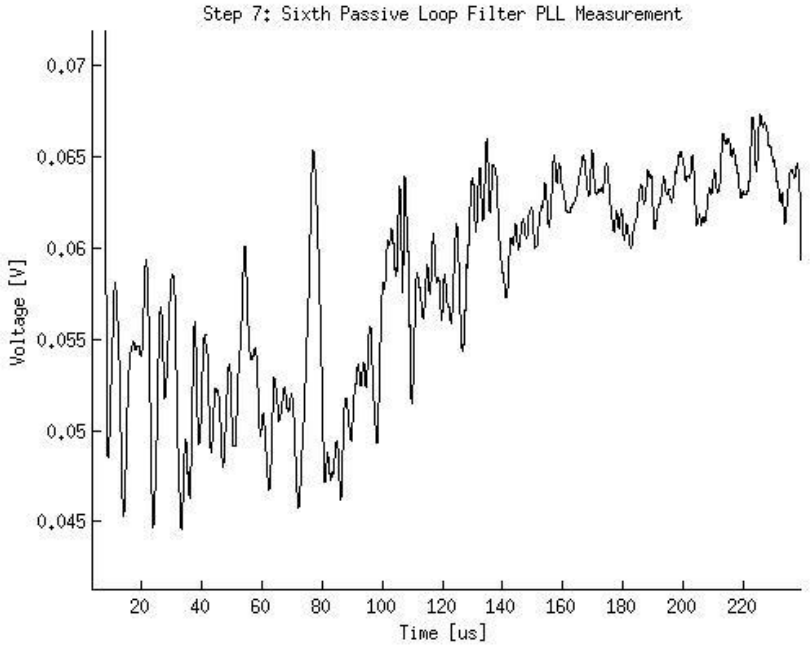

Figure 4-10: Processed Compensation Signal Measurement Step 7

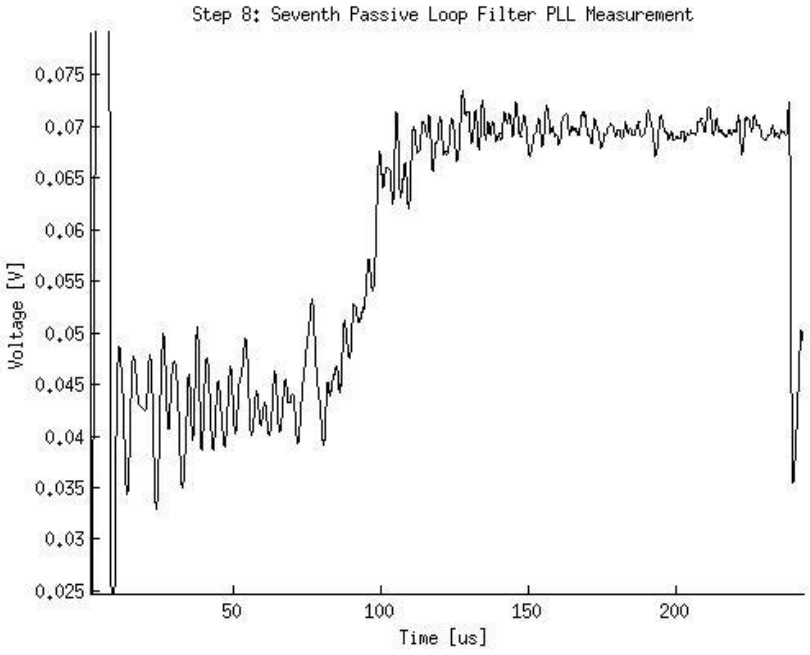

Figure 4-11: Processed Compensation Signal Measurement Step 8

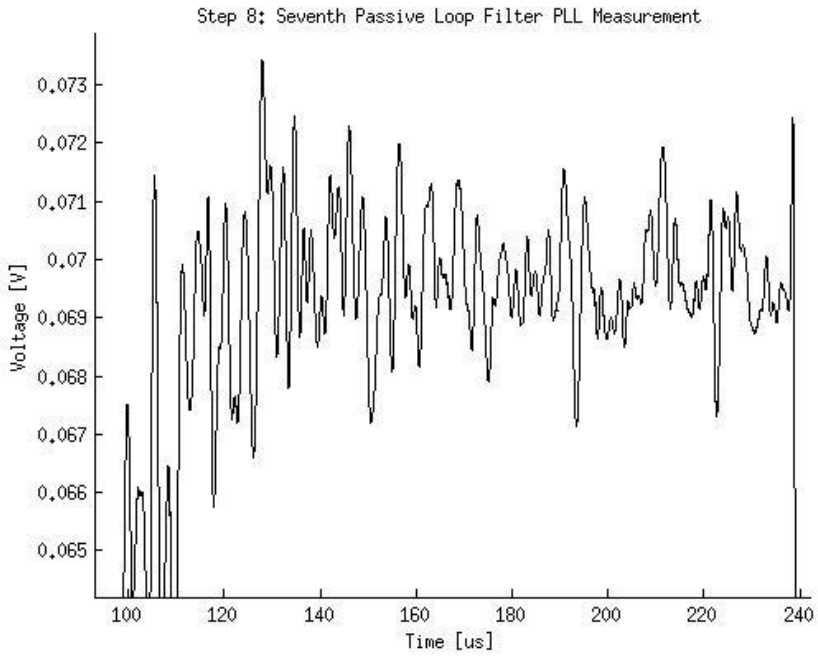

Figure 4-12: Zoomed in Version of Processed Compensation Signal Measurement Step 8

Figures 4-5 through 4-12 show how the PLL compensation voltage was reduced at low frequencies with the pre-distorted signal added to the loop. As has been already mentioned, the largest issue encountered was a voltage step, which added low frequency noise to the compensation signal. As mentioned, this voltage step was related to the amount of time that the DC coupled port was turned on. The fact that a digital low pass filter was used instead of bandpass filters helped to improve this issue by correcting for low frequency deviations at each step. However, low frequency errors will continue to occur and the system will have to rely on the ability of the PLL to compensate for them.

Figure 4-12 shows a zoomed-in version of the last 150 μs of step 8, which corresponds to the upper region of the voltage step. The figure shows that the compensation voltage has a peak-to-peak amplitude of about 4 mV.

A clear limitation of this system is the small sampling rate, which is related to the memory capacity of the DDS. Using a waveform generator with a larger sampling rate could improve further the output signal and thus minimize the PLL compensation level.

4.3 CHIRP GENERATOR MEASUREMENTS

The chirp generator performance was measured with a test FMCW front end RF system and a synthetic target. The synthetic target used is composed of a 2.8167 μs optical delay line and an electro-optical transceiver. The delay of the synthetic target is sufficiently close to the nominal operating delay of 3 μs.

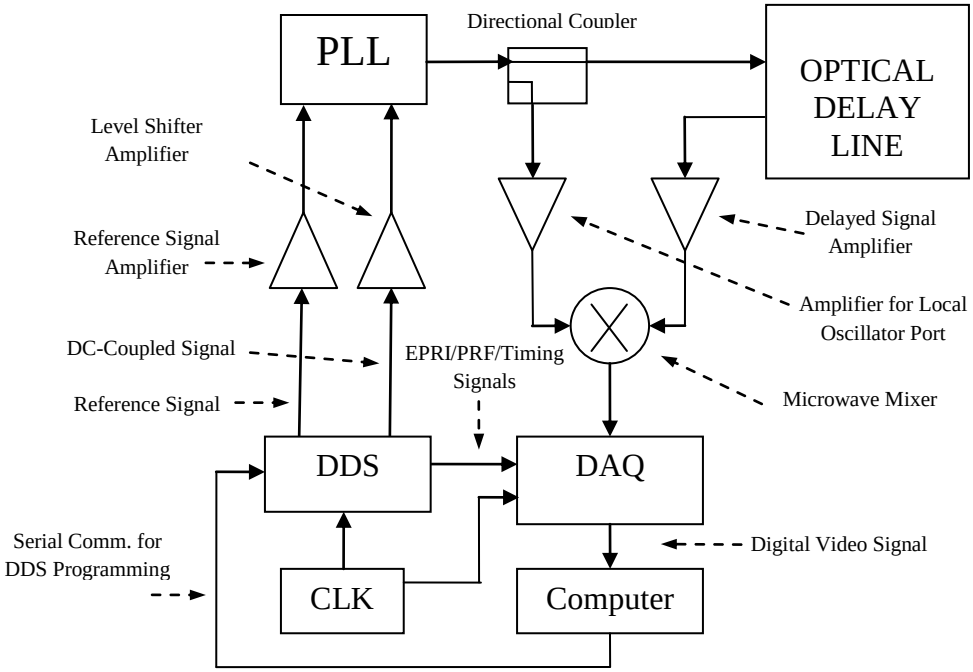

Figure 4-13: Block Diagram of the Set-up for the Measurements of the Chirp Generator Performance

A block diagram of the set-up for the measurements of the chirp generator performance is illustrated in Figure 4-13. For simplicity, the attenuators and filters are not shown on the block diagram. A reconstruction filter is needed for the reference signal generated by the DDS. Ku-band filters are required at each input port of the mixer. An anti-aliasing filter is required at the output of the mixer. Attenuators have been placed at both ports of the mixer before the amplifiers to adjust the gain at these points and avoid saturation of the amplifiers. An attenuator is also used at the output of the reference signal for the same reasons.

For this measurement, the output signal of the PLL is power divided by a 10 dB directional coupler. The through output of the coupler is connected to the input of the delay line. The coupled output of the coupler gets amplified by a microwave amplifier able to operate at the Ku-band. This amplification is needed to reach the power level required by the local oscillator (LO) port of the mixer. The output of the delay line is amplified by a microwave amplifier and then fed to the radio frequency (RF) port of the mixer. The intermediate frequency (IF) port of the mixer outputs the mixed signal. After going through the required anti-aliasing filter, the IF signal is applied to the input of the DAQ. The DAQ samples the data at a sampling rate of 62.5 MHz. The DAQ performs a coherent integration using four samples.

The DAQ then outputs the coherent integrated digital video signal to a computer. The computer is used for interfacing the DDS, the DAQ, as well as recording and processing the digitized video signal.

For the microwave amplification required, the ZX60-183-S wideband amplifier was used. This amplifier is manufactured by Mini-Circuits [50]. The ZX60-183-S has a gain of 24 dB, a maximum power of 18 dBm, and operates over the frequency range of 6-18 GHz. The ZLF-1000H+ amplifier was used for the reference signal amplification. The ZLF-1000H+ amplifier is also manufactured by Mini-Circuits [51]. This amplifier has a gain of 28 dB, a maximum power of 20 dBm and operates over the frequency range of 10-1000 MHz. The directional coupler used at the output of the PLL is the MC0618-10 directional coupler. This is a 10 dB coupler manufactured by Fairview Microwave Inc., which operates over the frequency range of 2-18 GHz [52]. The mixer used is a doubled balanced ultra broadband mixer with model DB0218LA1-R. This mixer is manufactured by Miteq Inc. [53]. It has 6.5 conversion loss and requires a 7 dBm minimum power at the LO port. The mixer's RF and LO ports operate over the frequency range of 2-18 GHz and the IF port operates over the frequency range of DC-750 MHz. The DAQ utilized was implemented at CReSIS and uses an ADC with model AD9640. The AD9640 is manufactured by Analog Devices Inc.

The optical delay line, which is used to simulate the roundtrip delay of a target, has a delay of 2.8167 μs. This delay of 2.8167 μs, the chirp bandwidth of 6 GHz, and the sweep time of 250 μs correspond to a video signal composed of a tone signal with a frequency mean of 67.6 MHz.

The digitized video signal provided by the DAQ to the computer has been recorded to a hard disk drive. In order to measure the performance of the chirp generator, the digitized video signal has been converted to the frequency domain using the FFT algorithm. The FFT function provided by Matlab has been used for this purpose. Since the DAQ sampling rate is 62.5 MHz, its Nyquist bandwidth equals 31.25 MHz. Therefore, the third Nyquist zone corresponds to the frequency range of interest. Assuming that the anti-aliasing filter provides sufficient attenuation outside the third Nyquist zone of the DAQ, the output of the FFT output corresponds to the frequency range between 62.5 MHz and 93.75 MHz.

The chirp generator video signal has been measured for most steps of the pre-distorted voltage generation process to track the improvements made. For all cases, a Hanning weighting has been applied to the time-domain waveform of the video signal. Figures 4-14 through 4-19 show the power magnitude in dB over the frequency spectrum for the recorded video signal at some steps of the pre-distorted voltage generation process. The plots shown in Figures 4-14 to 4-19 only show the frequency range between 66.5 MHz to 68.5 MHz.

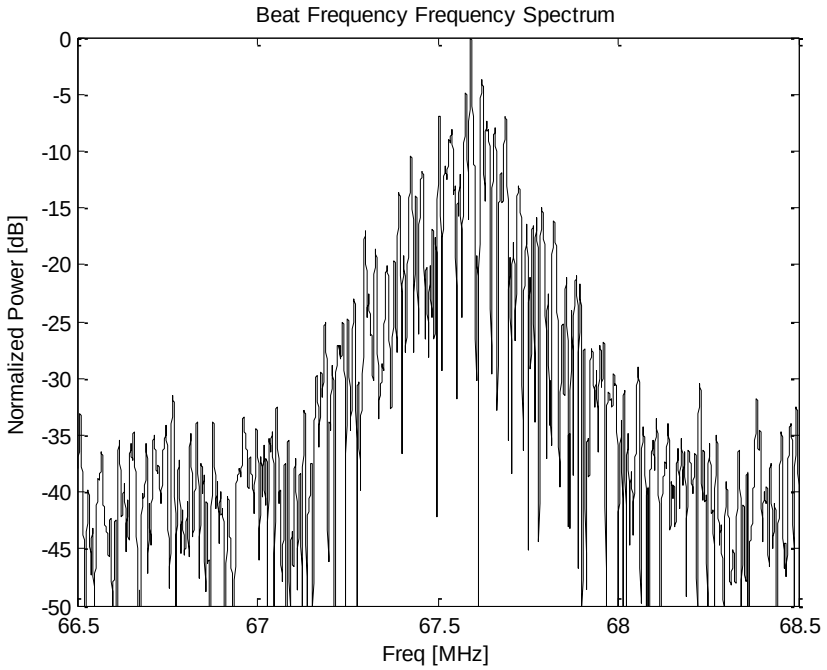

Figure 4-14: Measured Video Signal Recorded at Step 1

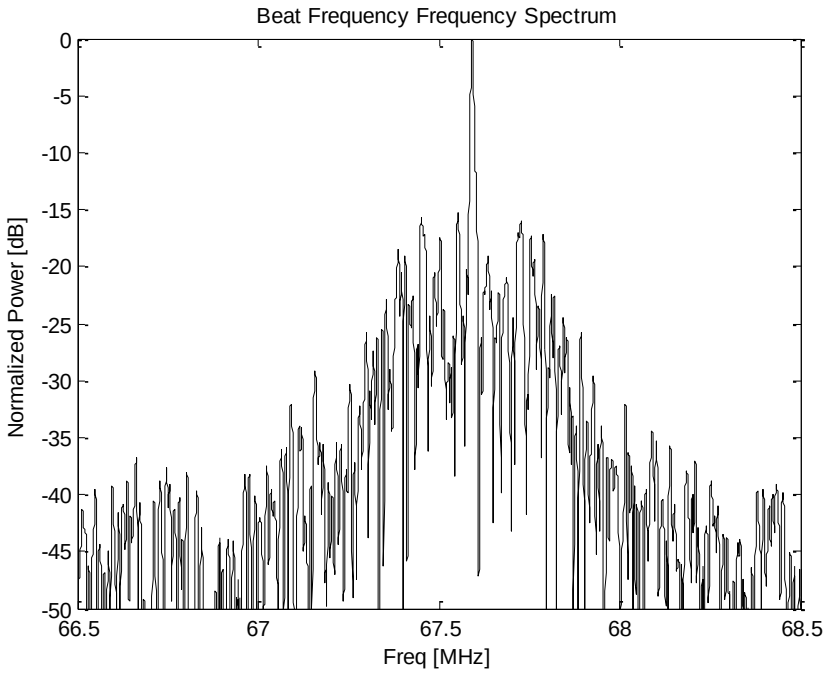

Figure 4-15: Measured Video Signal Recorded at Step 2

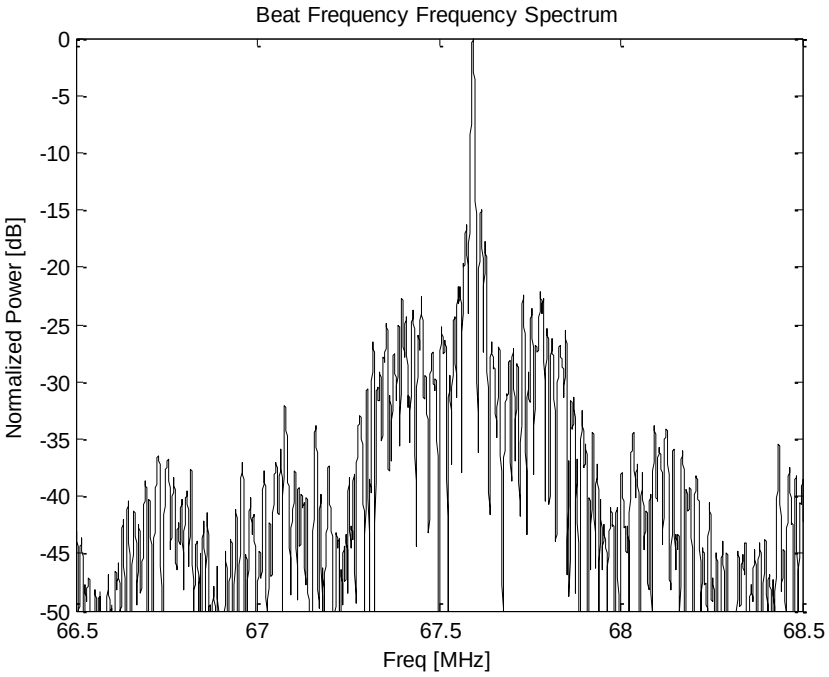

Figure 4-16: Measured Video Signal Recorded at Step 3

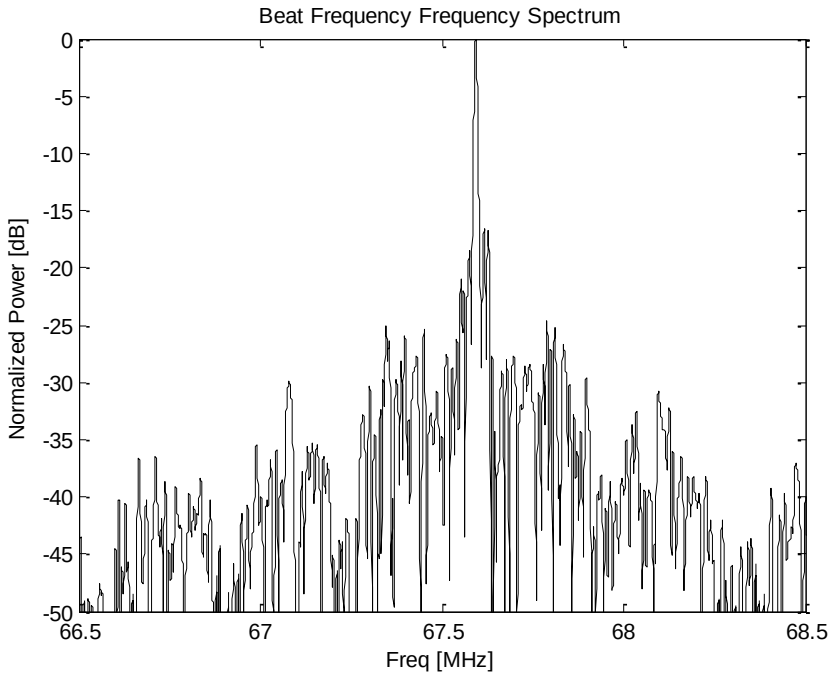

Figure 4-17: Measured Video Signal Recorded at Step 4

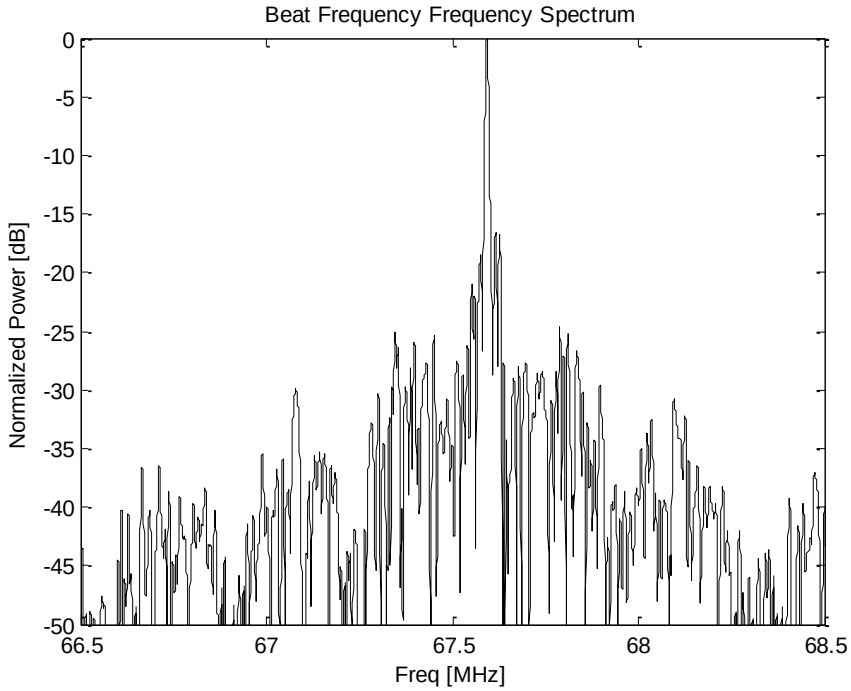

Figure 4-18: Measured Video Signal Recorded at Step 5

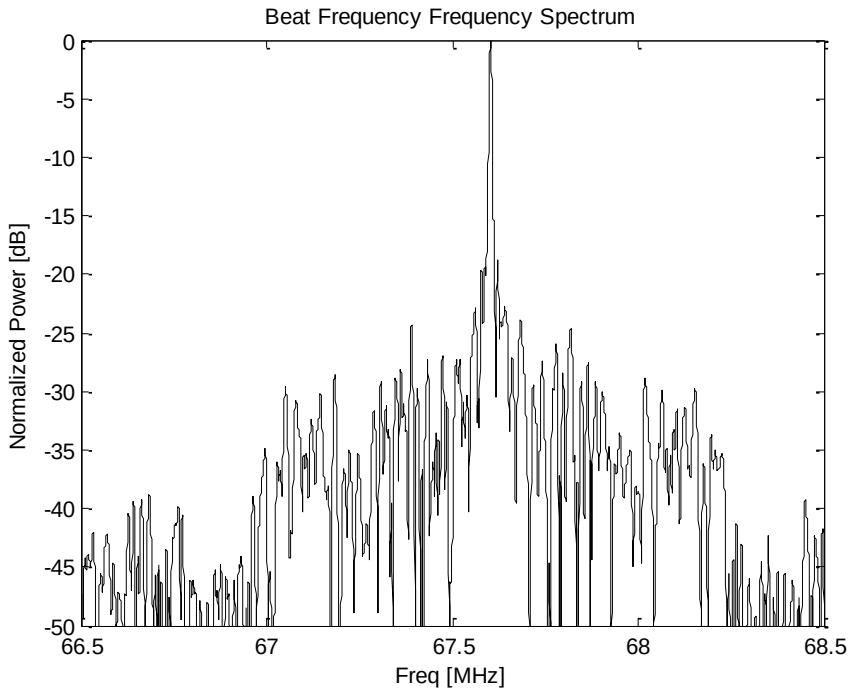

Figure 4-19: Measured Video Signal Recorded at Step 8

Figures 4-14 to 4-19 shows a clear relationship between the external compensation process and the video signal improvement. Further steps would not show any significant improvement since the DC coupled signal bandwidth limit has been reached.

In Section 2.1.2, the range resolution calculation was discussed. In addition, a measure was suggested to determine the range resolution performance in terms of the dynamic range of close targets. The suggested measure is the difference in range between the mainlobe and the first sidelobe for a single target response. The magnitude difference at this point, which is equivalent to the first sidelobe level, provides the dynamic range for close targets. The relationship between the range and the video signal has also been point out in section 2.1.2. The overlapping sweep time interval was defined as the time interval where the reference signal and the received signal overlap, for an FMCW radar system. The chirp modulation frequency, equivalent to the inverse of the overlapping sweep time interval, will equal the frequency resolution of the discrete frequency spectrum. This assertion assumes that the video signal has been time gated over the overlapping time interval. The modulation frequency (f_m) and the overlapping time interval (T_{video}) for the measurements are described on equations (4.1) and

(4.2). In equation (4.1), τ is the roundtrip delay of the synthetic target and T_{chirp} is the total chirp sweep time.

$$T_{video} = T_{chirp} - 2 \cdot \tau = 244.37 \mu s \tag{4.1}$$

$$f_m = \frac{1}{T_{video}} = 4.0922 kHz \tag{4.2}$$

$$\Delta f_{ml} = 2.5 \cdot \frac{1}{T_{video}} = 10.23 kHz \tag{4.3}$$

The modulation frequency described in equation (4.2) will be equal to the frequency difference between the frequency of the mainlobe and the frequency of the null on the measured video signal, given that no time-domain weighting has been applied. The difference in frequency between the mainlobe and the first sidelobe equals 1.5 times the modulation frequency, given that no weighting has been applied. A Hanning window can be applied to weight the time-domain signal. This window will improve the sidelobe level at the expense of increasing the frequency distance between the mainlobe frequency and the first sidelobe frequency. The Hanning window increases this difference to 2.5 times the modulation frequency. Equation (4.3) shows the frequency difference between the mainlobe and the first sidelobe (Δf_{ml}) for a tone using a Hanning window. Figure 4-20 is a matlab simulation made of an ideal tone at 67.6 MHz weighted with a Hanning window. The frequency distance between the mainlobe and the first sidelobe in Figure 4-20 agrees with the result of equation (4.3).

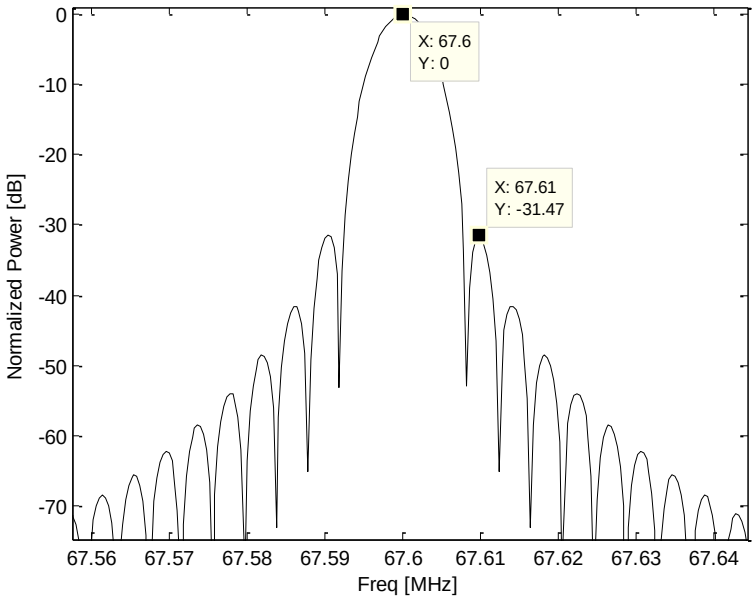

Figure 4-20: Ideal Sidelobe Performance with Hanning Weighting

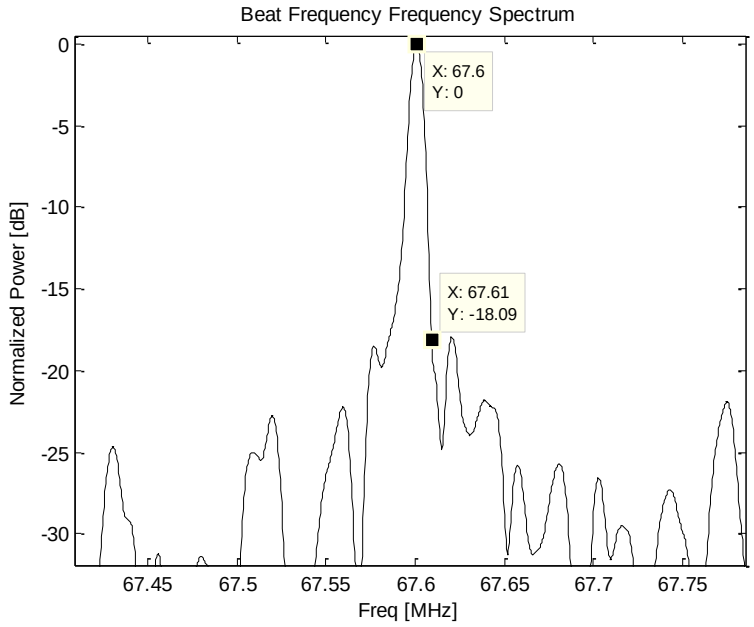

Figure 4-21: Video Signal Sidelobe Performance

Figure 4.21 shows the measured sidelobe performance of the Chirp Generator using 6 GHz of bandwidth. This bandwidth corresponds to an ideal mainlobe to first null range

resolution at free space of 2.5 cm. Equation (4.4) shows the parameters used to determine the range resolution. In equation (4.4), *c* corresponds to the speed of light, which is the approximation given in this case to the signal propagation speed. Additionally, Δf corresponds to the chirp bandwidth.

$$\Delta R = \frac{2 \cdot c}{\Delta f} = \frac{2 \cdot 3 \times 10^{8} [m/s]}{6[GHz]} = 2.5[cm] \tag{4.4}$$

This mainlobe-to-first-null resolution corresponds to a mainlobe-to-first sidelobe resolution of 6.25 cm. Thus, an FMCW using the chirp generator designed would have a mainlobe-to-first sidelobe range resolution of 6.25 cm at 18 dB.

The dynamic range of 18 dB at the range resolution is greatly caused by the nonlinearity of the chirp. Some of this nonlinearity comes from the higher frequency components that are not compensated effectively by the PLL or the external compensation.

As was explained in Chapter 2, the video signal becomes more sensitive to the nonlinear behavior of the chirp as the round trip delay of the target increases. For comparison purposes, the chirp generator performance was tested with a 35.8 ns copper delay line. Figure 4-22 shows the video signal for this delay line. This figure also shows a superior sidelobe performance, but about a 30 dB noise level.

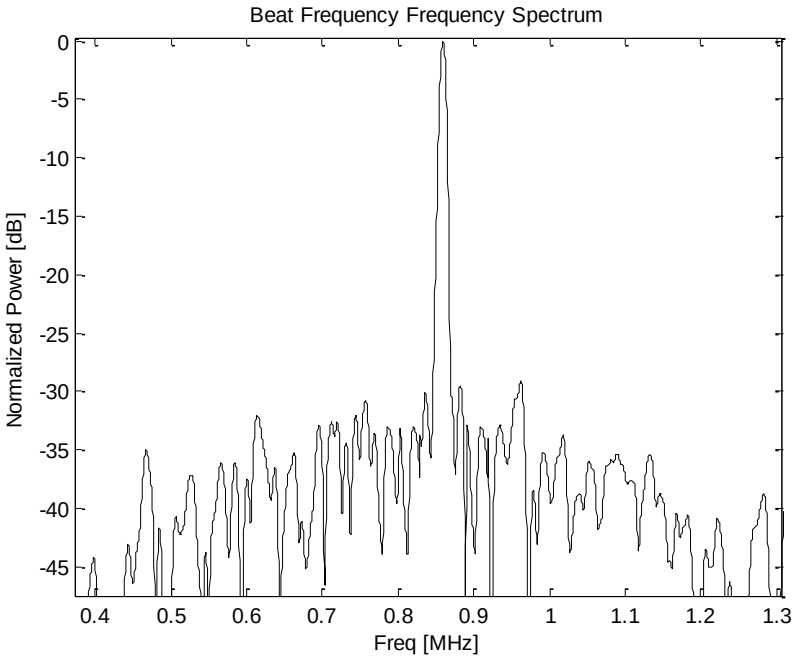

Figure 4-22: Video Signal at 35.8 ns of roundtrip delay

The frequency spectrum of the chirp generator output signal has been measured using an Agilent E4446A spectrum analyzer. The measured frequency spectrum of the chirp shows the 6 GHz of bandwidth from 12 to 18 GHz. This is the expected frequency range for the chirp generator designed. The power level is less than 0 dBm. This power level agrees with the VCO manufacturer's datasheet. This power is not sufficient to drive the LO port of most mixers. Thus, an FMCW radar system using this chirp generator requires an LO amplifier in the reference signal path of the FMCW front end system.

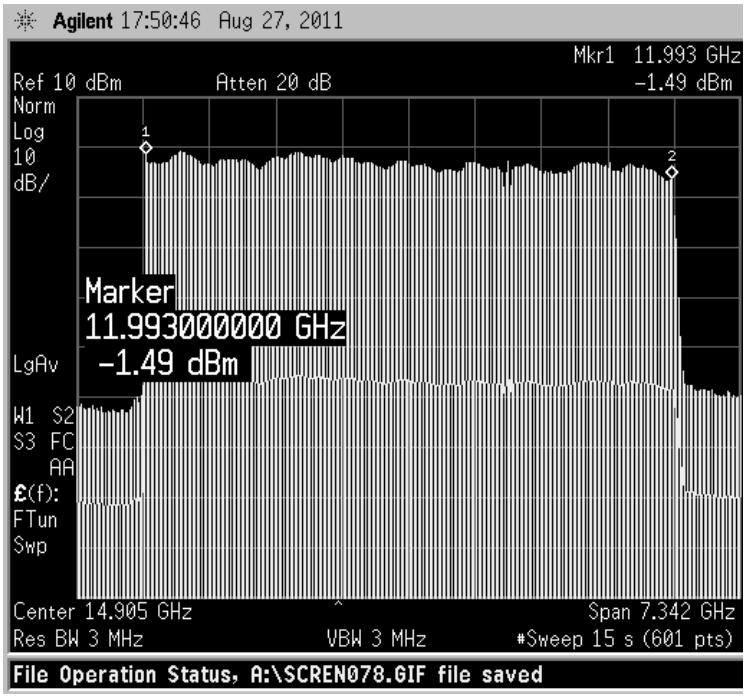

Figure 4-23: Chirp Frequency Spectrum

The results of the chirp generator performance show that the linearization technique proposed successfully compensates for nonlinearities on the tuning curve VCO. The correction applied to the nonlinearities on the implemented chirp generator did not achieve the ideal performance. As mentioned, the sampling rate of the DC-coupled channel waveform generator, which is limited by its RAM capacity, restricted the bandwidth of the external compensation signal. This limitation could be one of the main reasons for not achieving the ideal performance. Similarly, the synthesizer available to generate the reference signal was limited to a bandwidth of less than 500 MHz. For a larger reference bandwidth, a PLL with a wider loop bandwidth could be designed. A PLL with a wider loop bandwidth would compensate better for wideband disturbances as well as provide more information about the disturbances. This information could then be used to improve the compensation with a pre-distorted voltage.

Although the chirp generator did not reach an ideal performance for the required radar parameters, it has a superior performance than the previous chirp generators reported for the application of interest without the use of frequency multipliers.

CHAPTER 5: CONCLUSIONS AND FUTURE WORK

Ultra-Wideband radar sensors are developed for high accuracy and high resolution measurements. At the Center for Remote Sensing of Ice Sheets, UWB FMCW radars are utilized for measuring surface elevation and snow thickness over Greenland and Antarctica. The resolution of FMCW radar sensors depends on the bandwidth and the quality of the transmitted waveform. The nonlinear behavior of VCOs degrades the range resolution performance of FMCW radar sensors developed with VCO-based chirp generators. The range performance of these radars becomes more sensitive to the VCO nonlinear behavior as the target roundtrip delay increases. A linearization technique for VCO-based chirp generators was presented in this investigation. The linearization technique uses a closed loop control system for real time compensation of the VCO with a type 1 Phase Locked Loop along with an added pre-distorted compensation signal generated offline.

Wide loop bandwidth PLLs have a superior tracking performance compared to narrow loop bandwidth PLLs. They have the ability to compensate for wideband disturbances in the loop. Since the VCO nonlinear behavior can be modeled as disturbances added to the loop, a wide loop bandwidth PLL can be utilized to linearize a VCO. On the other hand, the PLL loop filter should be able to significantly attenuate the reference spurs. Type 1 PLLs have a faster transient response than type 2 PLLs. Additionally, unlike type 2 PLLs, type 1 PLLs do not have the high peaking behavior during transients. Thus, the transient errors caused by type 1 PLLs are less significant than those caused by type 2 PLLs. For all these reasons, a wide loop bandwidth type 1 PLL with a loop filter that significantly attenuates the reference spurs has been chosen for the closed loop control system.

Type 1 PLLs suffer from infinite steady state error for phase parabola inputs. However, external compensation can be applied to the loop to solve this problem. Additionally, the PLL controls an ultra-wideband VCO with a tuning sensitivity that varies significantly. The PLL design should consider these large variations such that both stability and low transient errors are maintained. For this reason, the PLL should be designed with a sufficiently large phase margin. Both the large phase margin and the large variations on the tuning sensitivity of the VCO

degrade the tracking performance of the PLL. The PLL compensation signal produced at the output of the loop filter has a magnitude and phase that are dependent on frequency, as is any other signal in the control loop. The tracking performance can be improved by measuring the PLL compensation signal, equalizing it and applying it back into the loop. Since the type 1 PLL already requires an external compensation to achieve a finite phase steady state error for a frequency ramp input, both previously-mentioned external compensation signals can be applied at the same point.

In this investigation, the type 1 PLL was designed with the largest possible loop bandwidth, keeping the spur level below 35 dBc. As expected, the measured loop bandwidth varied over the entire band due to variations in the tuning sensitivity of the VCO. The loop bandwidth of the designed PLL was 14.64 MHz for an average tuning sensitivity of 600 MHz/V. The measured loop bandwidth is 14.22 MHz at 15 GHz and the average measured loop bandwidth is 13.17 MHz. The measured spur level did not increase above 35 dBc, as designed. Therefore, the PLL performs very closely to the design specifications.

The external compensation signal was generated using a DC-coupled channel of a DDS board developed at CReSIS. The PLL compensation signal was digitized by an oscilloscope. The digitized PLL compensation signal has been processed to compensate for the frequency response in a series of steps. The resulting signal was then added to the PLL for improved compensation. The chirp generator performance measurements show a direct relationship between the bandwidth of the external compensation, which was changed for each step, and the quality of the target response. The limited effective sampling rate of the DC-coupled channel of the DDS board, dependent on the DDS memory capacity, limited the bandwidth of the external compensation signal. In the future, this technique can be applied using an arbitrary waveform generator with a larger sampling rate. Moreover, the PLL loop bandwidth may be increased if larger reference frequencies are utilized.

The prototype chirp generator built for this investigation constitutes the basis of the FMCW radar that will be used for surface elevation measurements in the CReSIS 2011-2012 field campaign in Antarctica. Data collected with an FMCW radar sensor using this chirp generator will contain measurements with higher accuracy and finer resolution than that of previous sensors.

Chirp generators with larger bandwidth will continue to be attractive instruments for fine resolution measurements. In the future, we will investigate the implementation of chirp generators with a hybrid combination of digital direct synthesis techniques and direct analog synthesis techniques. Furthermore, an analysis will be made balancing the advantages and disadvantages of both chirp generator designs. The chosen design will be miniaturized for a more convenient integration with the radar.

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APPENDIX A: 2-CHANNEL DDS BOARD

An Eight Channel Waveform Generator was developed at CReSIS as a general purpose waveform generator. The waveform generator uses 8 AD9910 integrated circuits (ICs), which are 1 GSPS DDS chips from Analog Devices. As a subset of this waveform generator, a 2 channel DDS board has also been implemented [53].

The DDS board features a Field Programmable Gate Array (FPGA), which is used to acquire the settings and to transfer the waveform parameters to the DDS ICs. The AD9910 chip has many different data source types that can be used to modulate the phase, frequency and amplitude of the output waveform. The user communicates via a serial port using a defined communication protocol. The user can configure each channel by setting the registers and the random access memory (RAM) of the DDS accordingly.

The differential output of the DDS IC is coupled to a balun for regular AC operation. The differential output can also be coupled to an op-amp based differential amplifier with a voltage gain of 2. These two possible configurations are the AC and DC coupled operating modes of the board.

On the current default configuration of the 2 channel DDS board, one of the channels is AC coupled and the other one is DC coupled. The AC coupled channel on the default configuration uses the digital ramp generator for tuning the frequency on the internal DDS and uses the RAM loaded by the user to modulate the amplitude of the waveform. An IDL source code was written by CReSIS faculty to easily load the digital ramp parameters and define the amplitude waveform.

The DC coupled channel output circuitry is designed for a 50-ohm impedance. This way the DC-coupled channel of the DDS board can be used as an arbitrary waveform generator, where the number of data source points per waveform is given by the DDS RAM. The DDS RAM has 1024 memory locations and 32 bit words. Only 14 bits may be used for amplitude modulation.

APPENDIX B: PLL SPECTRAL MEASUREMENTS

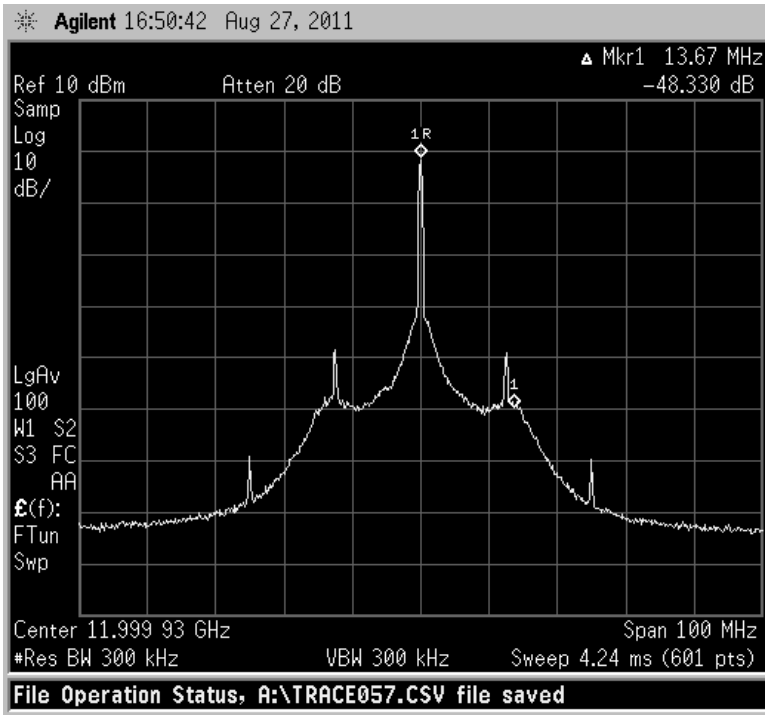

Figure B-1: Measured PLL Spectrum at 12 GHz

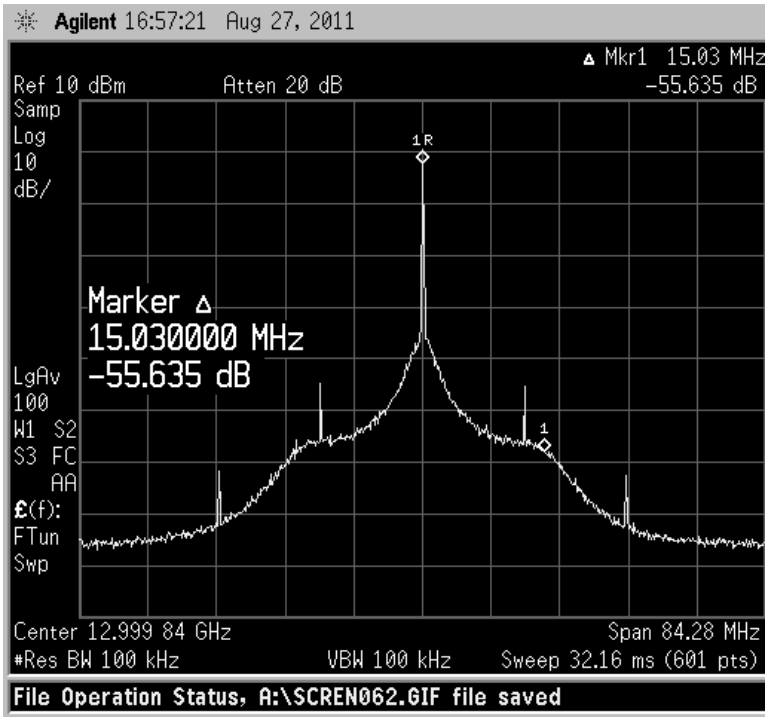

Figure B-2: Measured PLL Spectrum at 13 GHz

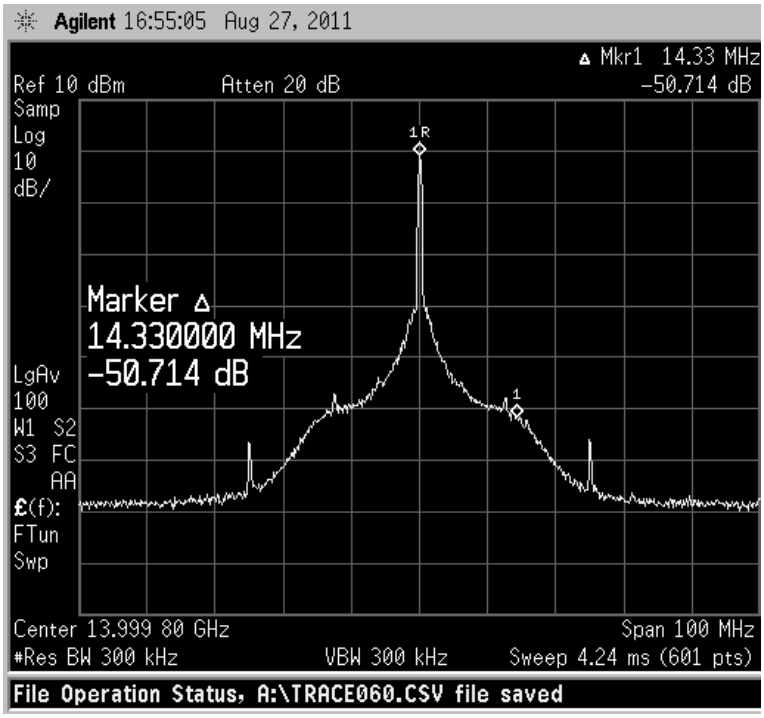

Figure B-3: Measured PLL Spectrum at 14 GHz

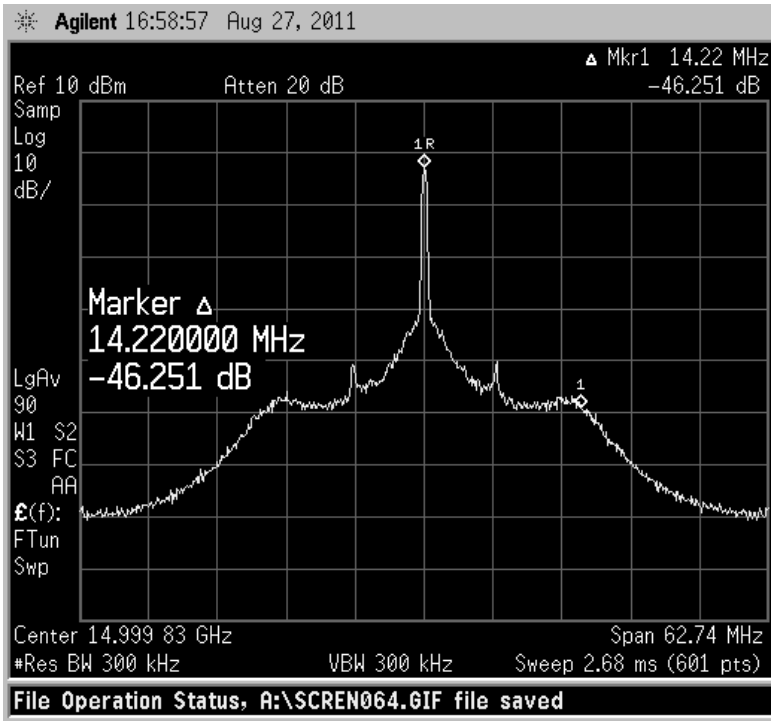

Figure B-4: Measured PLL Spectrum at 15 GHz

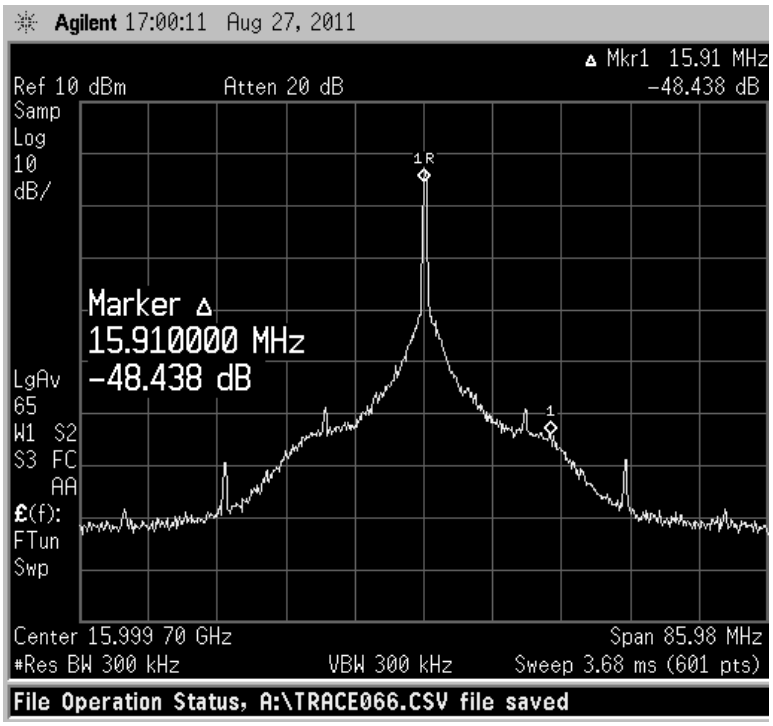

Figure B-5: Measured PLL Spectrum at 16 GHz

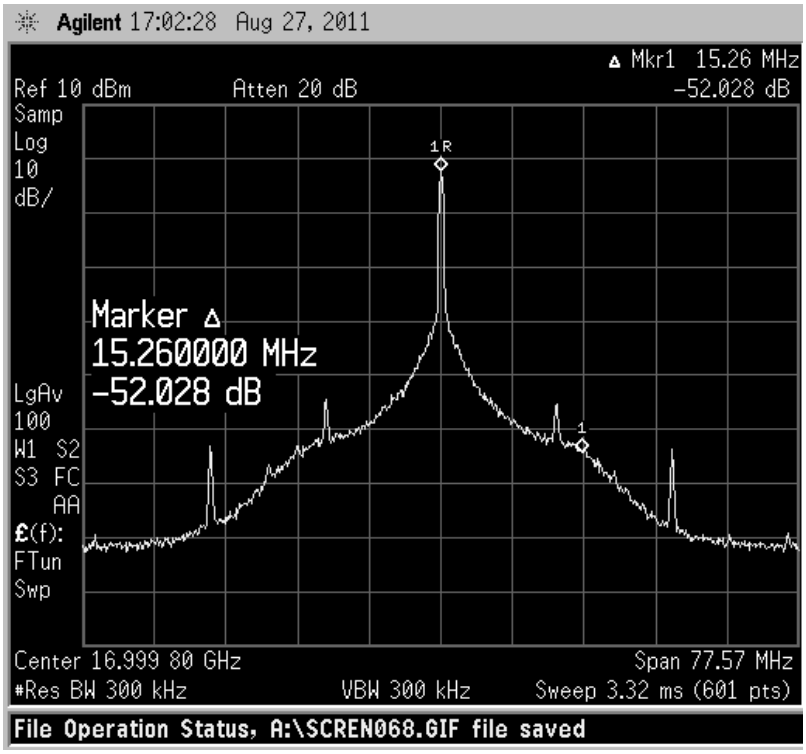

Figure B-6: Measured PLL Spectrum at 17 GHz

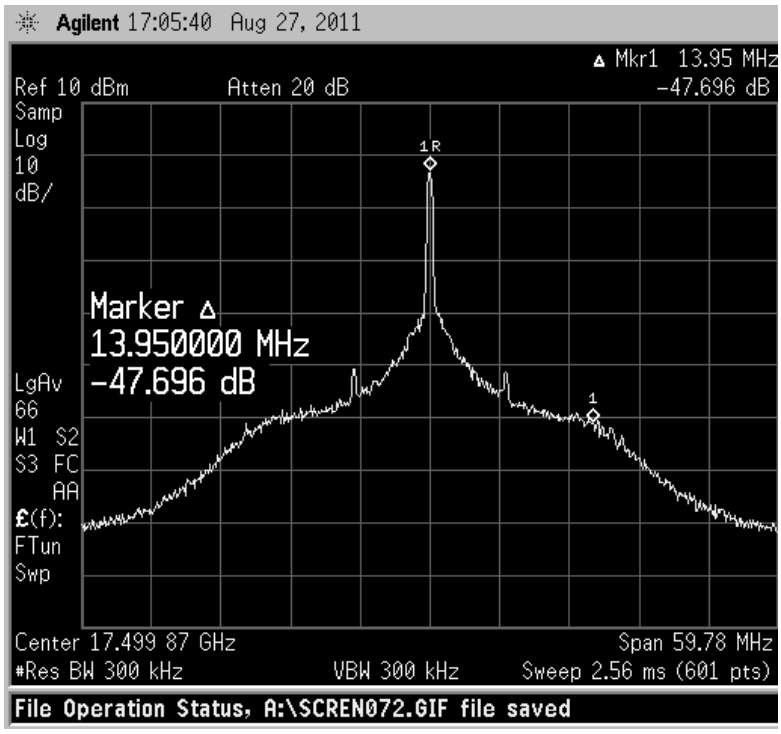

Figure B-7: Measured PLL Spectrum at 17.5 GHz

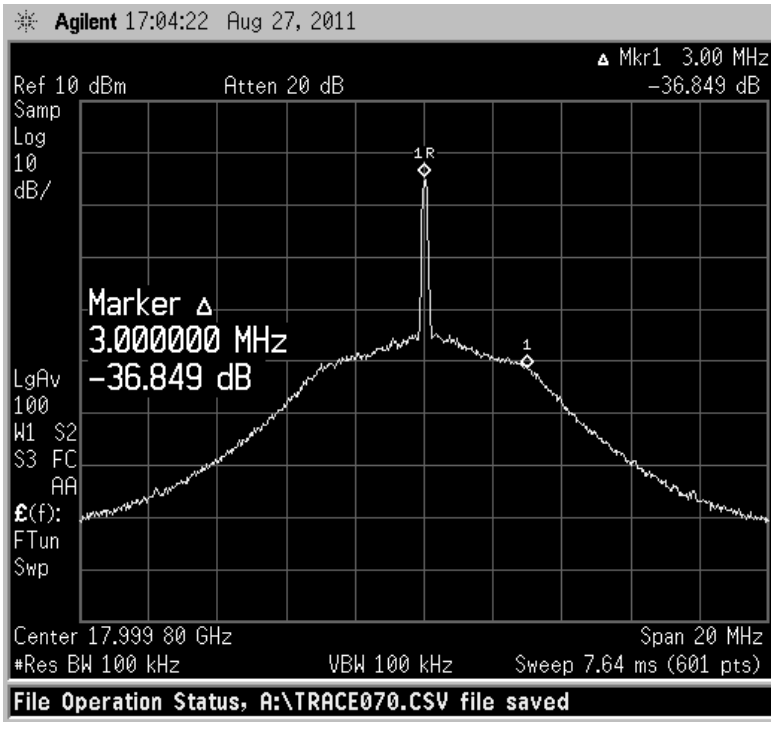

Figure B-8: Measured PLL Spectrum at 18 GHz