DESIGN AND DEVELOPMENT OF AN AMPLITUDE LEVELING SUBSYSTEM FOR FM RADARS

BY

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ABSTRACT

To better understand contributions of large ice sheets to sea level rise, remote sensing radars are used to measure relevant characteristics. The Center for Remote Sensing of Ice Sheets (CReSIS) at the University of Kansas has been developing ultra wideband radars to measure the surface elevation of polar ice sheets, near-surface internal layers in polar firn, and thickness of snow cover on sea ice. There is a need for an amplitude leveling subsystem for these radars to achieve constant transmit power since amplitude distortions degrade range sidelobe performance of these radars. A closed-loop amplitude leveling subsystem for frequency-modulated radars is designed, constructed and tested. This system uses a coupler and power detector to sample transmit power and feedback a control voltage to a variable-gain amplifier that controls the amplitude of the transmit signal. The closed-loop system is able to decrease amplitude variation to ±0.72 dB. Results are presented, and sources of error are analyzed for this system. Measurements of required control voltage versus frequency are presented for an open-loop system that does not use the coupler or power detector. These two systems are compared, and recommendations are given for future work.

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CHAPTER 1: INTRODUCTION

1.1 Motivation

The International Panel on Climate Change (IPCC) reported in 2007 that "warming of the climate system is unequivocal, as is now evident from observations of increases in global average air and ocean temperatures, widespread melting of snow and ice and rising global average sea level" [1]. Global surface temperature increased an average of 0.13°C from 1956 to 2005, and global average sea level rose at an average rate of 3.1 mm per year from 1993 to 2003 [1]. The main contributors to this rise in sea level are thermal expansion of the oceans and melting of glaciers and ice caps. To better understand these contributions, remote sensing can be used to study the surface elevation of polar ice sheets, near-surface internal layers in polar firn, and thickness of snow cover on sea ice.

Sea ice acts as a thermal insulator between the air and the ocean, slowing heat exchange between the warmer ocean water and the cooler air. Thicker sea ice provides greater insulation. Because of its high albedo, sea ice also reflects up to 90% of incident energy from the sun; whereas uncovered ocean water absorbs 85 to 90% of incident energy due to its high albedo [2]. Declining sea ice causes more energy to be absorbed by the ocean and is an indication of increase in global temperature. Sea ice also contributes to convection currents, regulates marine life by blocking solar radiation, and provides a habitat for wildlife [2].

The presence of snow on top of sea ice further increases the thermal insulation between the air and the ocean. The thermal conductivity of snow is approximately an order of magnitude less

than that of sea ice, causing it to provide greater insulation [3]. Because layers of snow give large amounts of additional insulation, the amount of snow cover plays a large role in the extent of heat transferred. In addition to providing extra insulation, the snow reflects almost all incident solar radiation because of its high albedo, preventing it from being absorbed by the sea ice and ocean [3]. Large quantities of snow cover can also act as mechanical loads, depressing the ice and allowing water pockets to form in the sea ice. This causes errors in freeboard measurements of sea ice height above the surface of the ocean and affects heat transfer throughout the system.

1.2 Objectives

CReSIS has developed two radars to monitor sea ice and snow cover over sea ice. The Ku-band Radar is an altimeter that operates between 13 and 15 GHz and is used to measure ice-surface elevation and map near surface internal layers in polar firn, and the Snow-radar operates between 2 and 7.5 GHz and is used to measure the amount of snow cover over sea ice. It can also be used to map near-surface internal layers in the top 10-20 m of polar firn. The wide bandwidths of these radars allow them to have very fine resolution. There is a need for a high-power amplifier with constant amplitude over a wide bandwidth to be used for these systems. Higher transmit power allows the radars to be operated at higher altitudes, and wide amplifier bandwidth allows the systems to retain their fine resolutions. Constant or windowed amplitude over the system bandwidth is necessary to avoid range sidelobes which could bury weak echoes from desired targets.

1.3 Approach

A wide-bandwidth variable-gain amplifier is used to provide the necessary transmit power. Two different approaches are taken. In the first approach, the amplifier is placed in a feedback loop in which transmit power is detected, scaled, and fed to the amplifier as a control voltage to correct variations in amplitude. The goal of this approach is to level the amplitude over the system bandwidth with a closed-loop. In the second approach, amplitude variations in the transmitter are characterized over the system bandwidth, and a digital control voltage is generated and fed to the amplifier to correct for amplitude variations. Windowing can also be applied. The goal of this approach is to level and window the amplitude over the system bandwidth with an open-loop.

1.4 Organization

This thesis is organized into five chapters. Chapter 2 provides background information on the need for amplitude leveling and the leveling process. Chapter 3 describes the design and implementation for the closed-loop system, and Chapter 4 provides the results for this system as well as a discussion of error sources. Chapter 5 describes the open-loop system. Finally, Chapter 6 summarizes the different approaches and results and gives recommendations for future work.

CHAPTER 2: BACKGROUND

2.1 FM Radar

Frequency-modulated (FM) radars transmit waveforms that increase linearly in frequency over time. The transmitted signal can be composed of frequency chirps separated in time or a continuous rising and falling frequency sweep (FM-CW radar). A frequency chirp with no phase offset is given by Equation 2-1 where f_1 is the start frequency of the chirp and k is the chirp rate given by Equation 2-2. The end frequency of the chirp is given by f_2, and τ is the chirp duration.

$$S(t) = A(t)\sin\left[2\pi\left(f_1 t + \frac{1}{2}kt^2\right)\right] \quad \textbf{2-1}$$

$$k = \frac{f_2 - f_1}{\tau} \quad \textbf{2-2}$$

A frequency chirp and its return are shown in Figure 2-1. The transmitted frequency chirp is shown in solid blue, and the return after a 30 μs delay is shown in dotted red. The delay is the difference in time between the transmit signal and the return as marked in the figure. Delay for two-way travel is calculated using Equation 2-3 where R is the one-way range and c is the speed of light. The beat frequency is found by mixing the transmit signal and return signal together and is the difference in frequency between the two signals; this is constant over the chirp duration as long as the frequency chirp is linear. Beat frequency is dependent on chirp rate and delay and is calculated using Equation 2-4. Because beat frequency is dependent on delay, it can be mapped to target range.

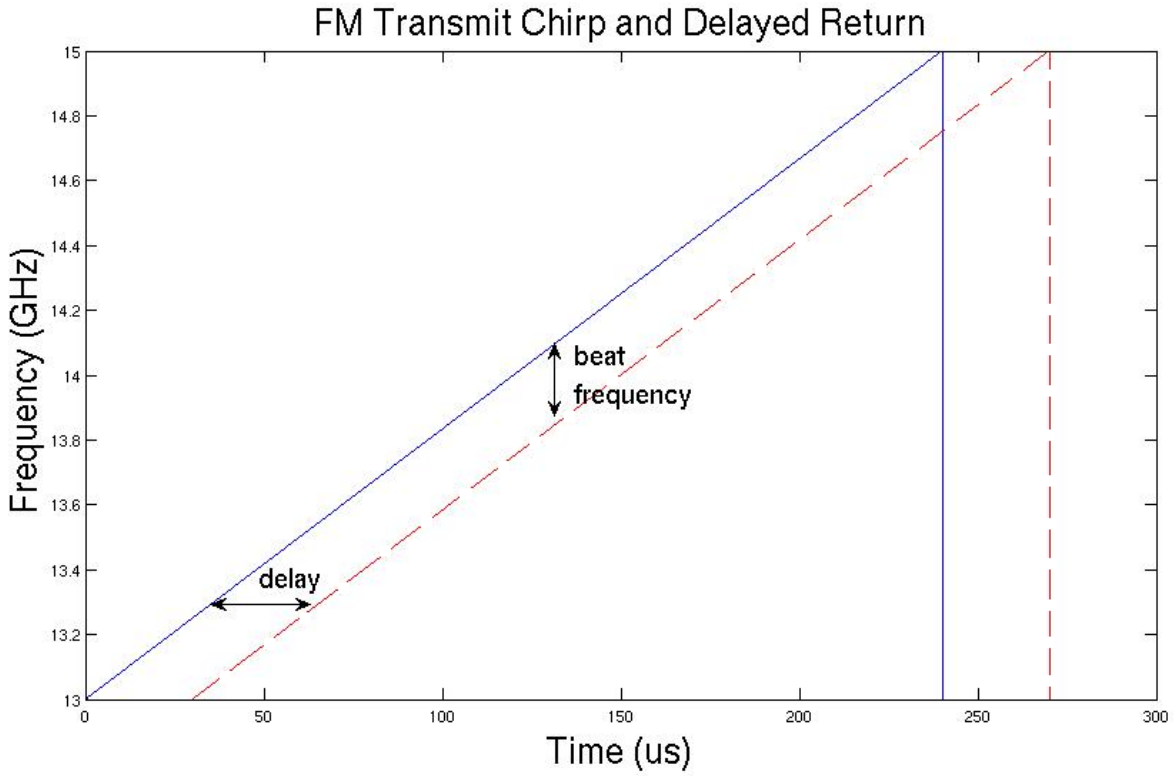


Figure 2-1: FM Transmit Frequency Chirp and Delayed Return

$$delay = \frac{2R}{c} \qquad \textbf{2-3}$$

$$f_b = k \cdot delay = \frac{f_1 - f_2}{\tau} \cdot delay \qquad \textbf{2-4}$$

2.2 Amplitude Distortions

When the amplitude of a chirp is not leveled over frequency, there are effects on the beat frequency spectrum. In this section different amplitude distortions are simulated to see their

effects. The normalized spectrum of a simulated 240 µs frequency chirp from 13 to 15 GHz with constant amplitude is shown in Figure 2-2. The amplitude of the spectrum over frequency is constant except for small oscillations at the beginning and end of the chirp. With a delay of 10 µs, corresponding to a height of 1500 m, the beat frequency spectrum is shown in Figure 2-3. Beat frequency for this frequency chirp and delay is calculated to be 83.333 MHz using Equation 2-4, which agrees with the simulated beat frequency shown in Figure 2-3. A zoomed beat frequency spectrum is shown in Figure 2-4. There is a clear peak in the beat frequency spectrum where the expected beat frequency occurs.

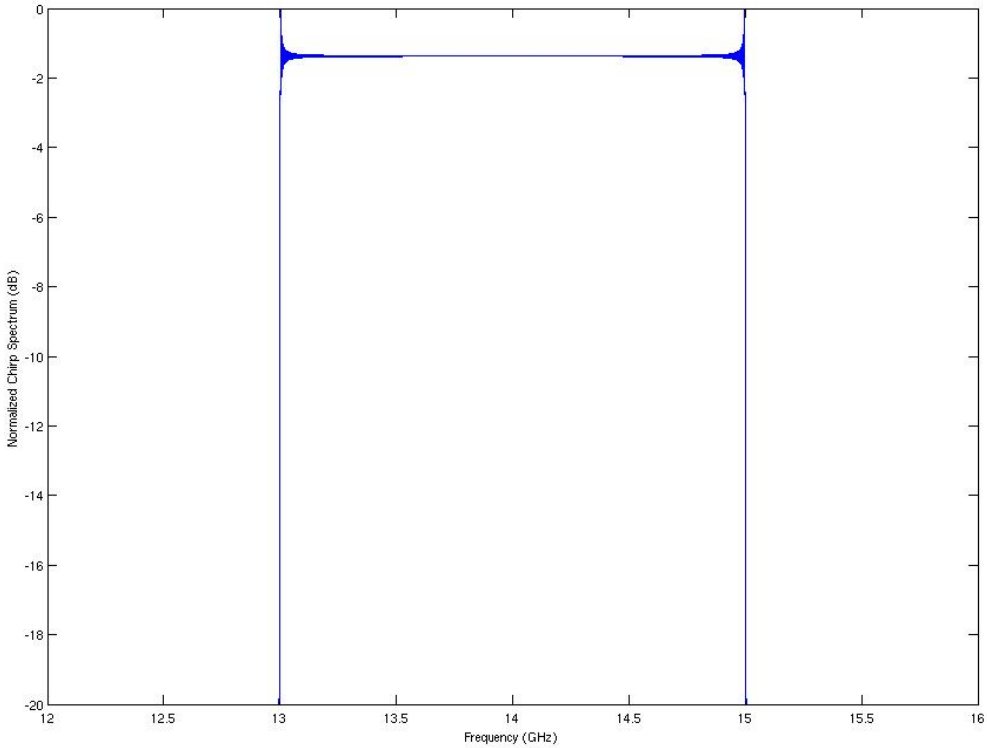


Figure 2-2: Simulated Frequency Chirp Spectrum with Constant Amplitude, 13 to 15 GHz, 240 µs

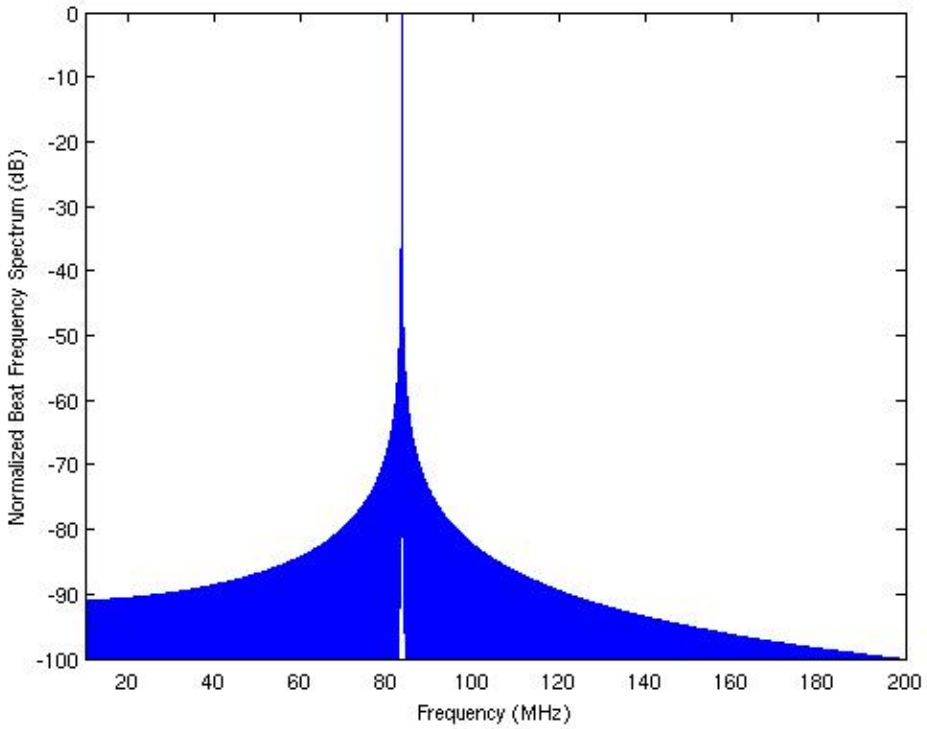


Figure 2-3: Simulated Beat Frequency Spectrum at 1500 m with Constant Frequency Chirp Amplitude

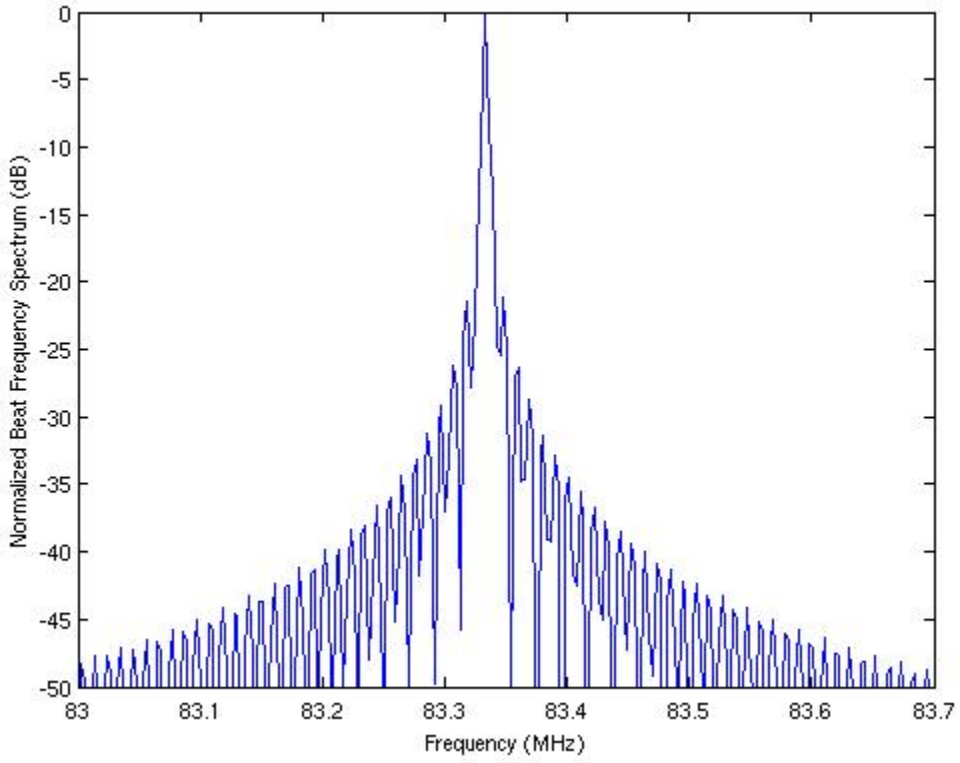


Figure 2-4: Zoomed Beat Frequency Spectrum at 1500 m with Flat Frequency Chirp Amplitude

The normalized spectrum of a simulated 240 µs frequency chirp from 13 to 15 GHz with sinusoidal distortion in amplitude is shown in Figure 2-5. 100 kHz sinusoidal distortion is used in this simulation, which can be seen in the frequency chirp spectrum. For a delay of again 10 µs, the beat frequency spectrum is shown in Figure 2-6. Although there appears to be a clear peak at the expected beat frequency, a zoomed beat frequency spectrum, shown in Figure 2-7, shows that this is not the case. There are sidelobes present on both sides of the expected beat frequency at harmonics of the sinusoidal distortion. This makes it difficult to determine the true beat frequency of the return and can also introduce false returns. A beat frequency error of 100 kHz, in this case, corresponds to a range error of 1.8 m. However, the sidelobe frequencies, and therefore error amounts, depend on the distortion frequencies present in the frequency chirp amplitude for each case.

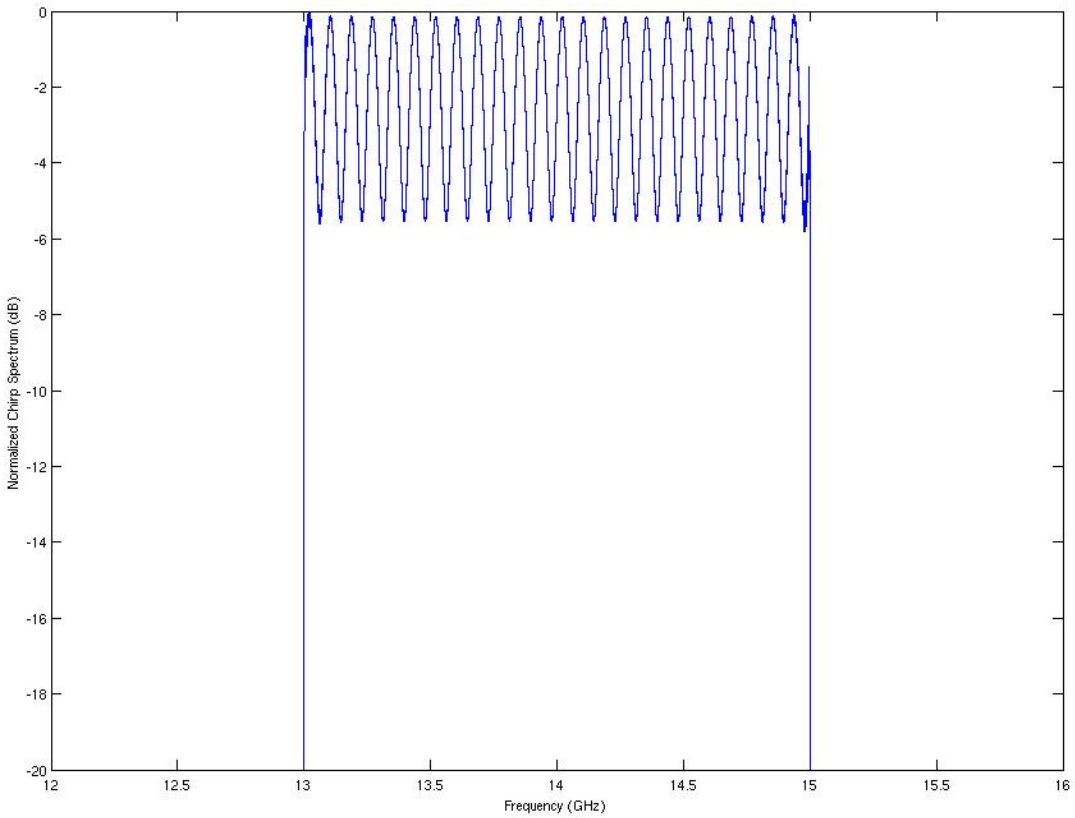


Figure 2-5: Simulated Frequency Chirp Spectrum with Sinusoidal Amplitude, 13 to 15 GHz, 240 µs

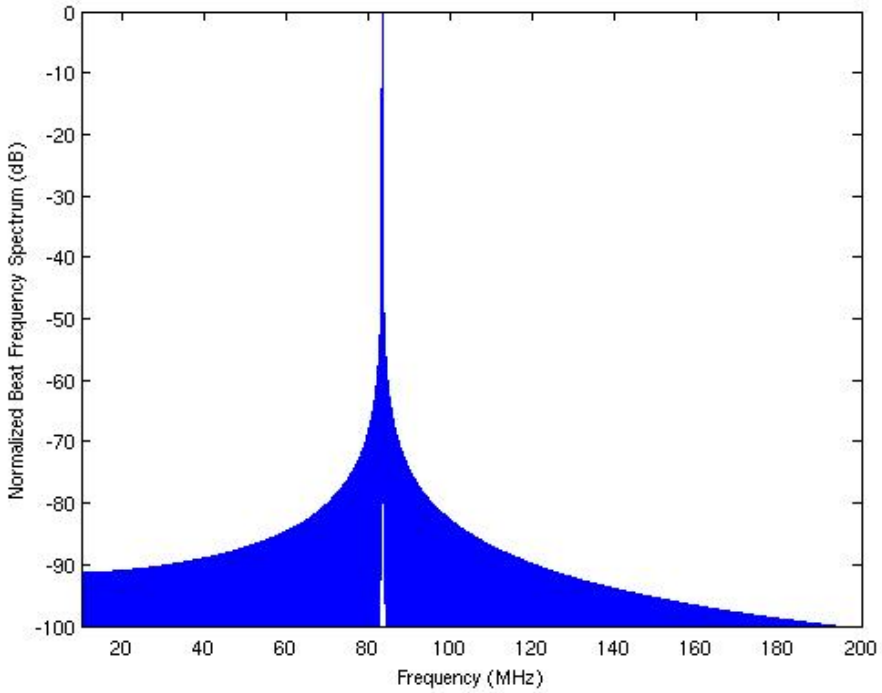


Figure 2-6: Simulated Beat Frequency Spectrum at 1500 m with Sinusoidal Frequency Chirp Amplitude

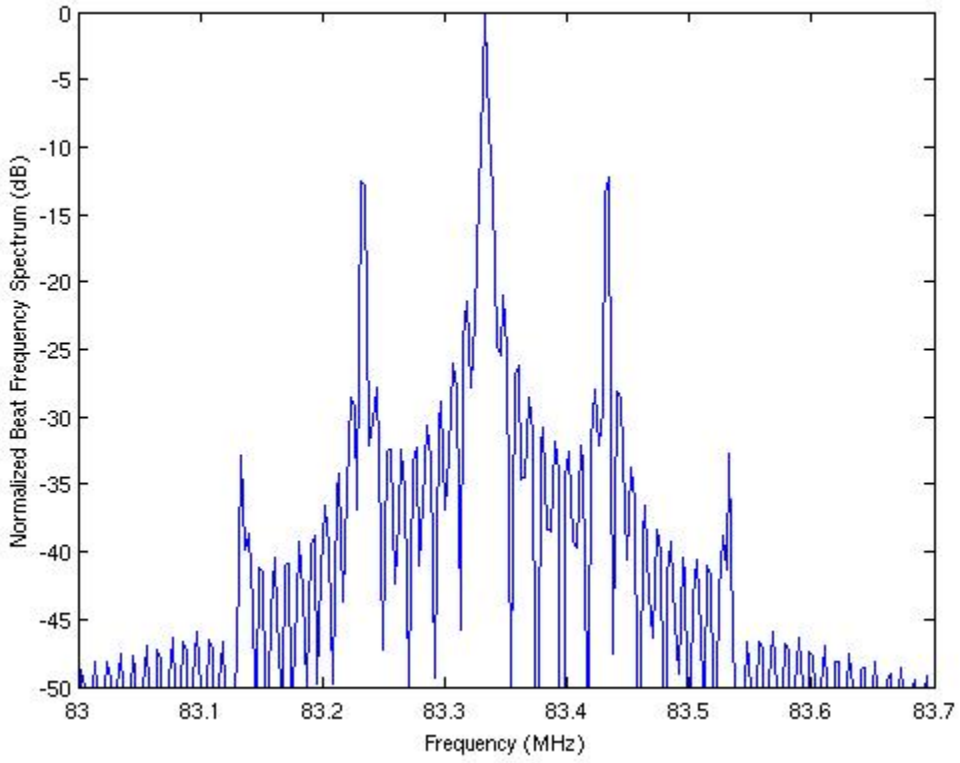


Figure 2-7: Zoomed Beat Frequency Spectrum at 1500 m with Sinusoidal Frequency Chirp Amplitude

Another form of distortion occurs when the amplitude of the frequency chirp falls off over time. The normalized spectrum of a simulated 240 µs frequency chirp from 13 to 15 GHz with exaggerated decay in amplitude is shown in Figure 2-8. The amplitude at the end of the frequency chirp is approximately 10 dB lower than the amplitude at the beginning of the frequency chirp. For a delay of again 10 µs, the beat frequency spectrum is shown in Figure 2-9, with a zoomed beat frequency spectrum shown in Figure 2-10. Although the distortion in beat frequency spectrum is not as apparent as with the sinusoidal amplitude distortion, it can be seen in Figure 2-10 that the peak is wider in frequency than with no distortion and the tails of the peak are approximately 3 dB higher on the edges of the plot. This makes it more difficult to detect multiple target returns that are close in beat frequency.

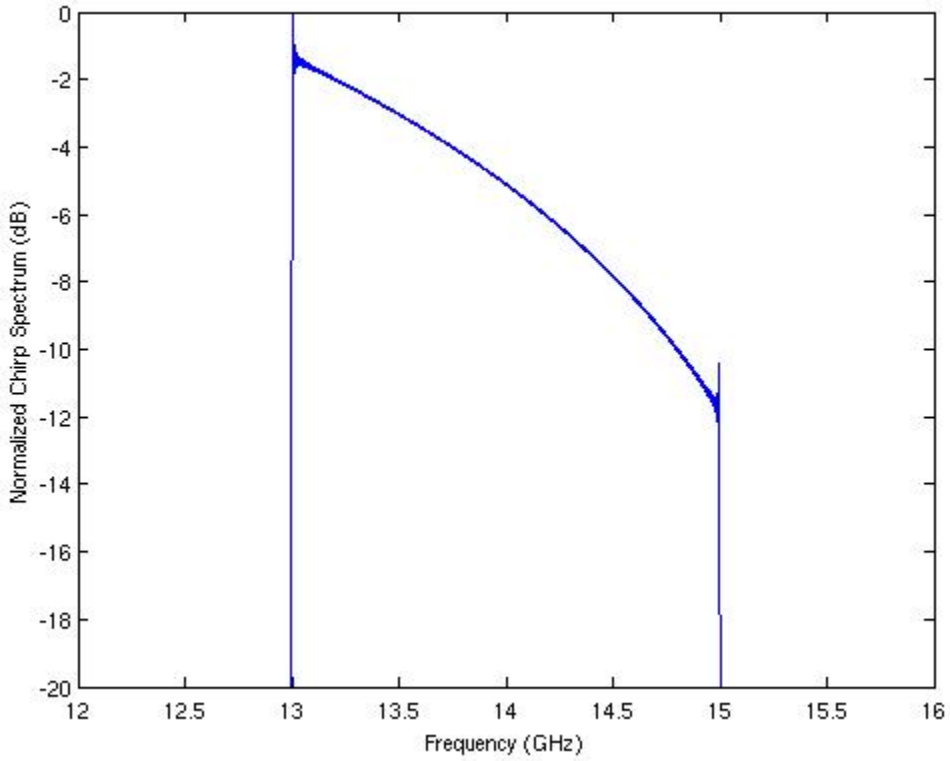


Figure 2-8: Simulated Frequency Chirp Spectrum with Amplitude Decay, 13 to 15 GHz, 240 µs

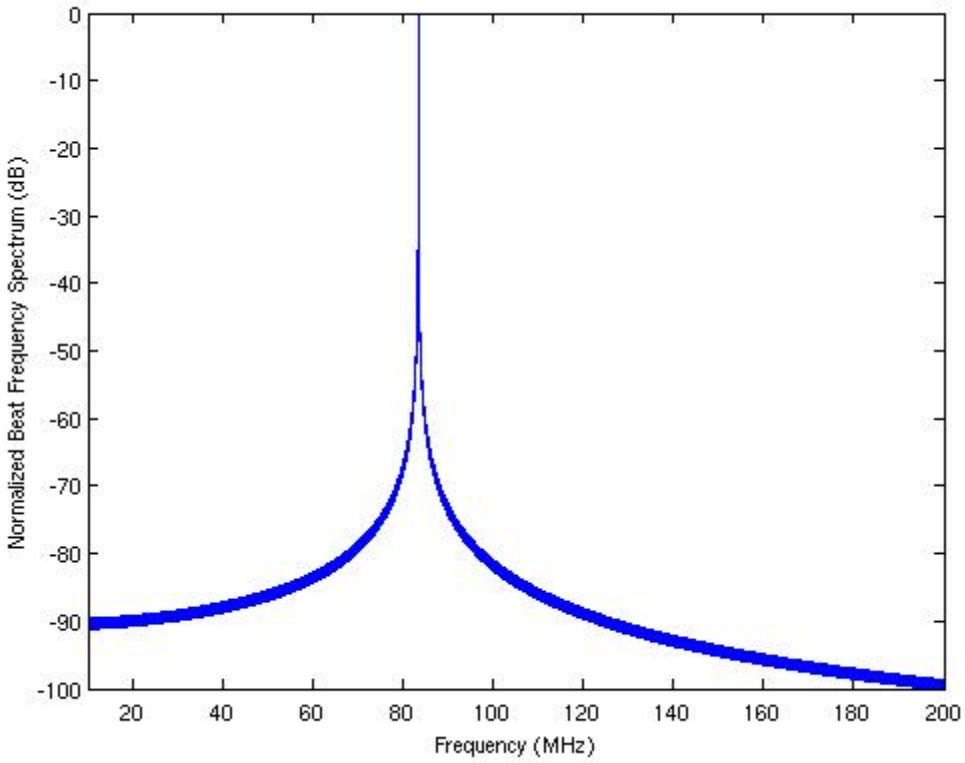


Figure 2-9: Simulated Beat Frequency Spectrum at 1500 m with Decaying Frequency Chirp Amplitude

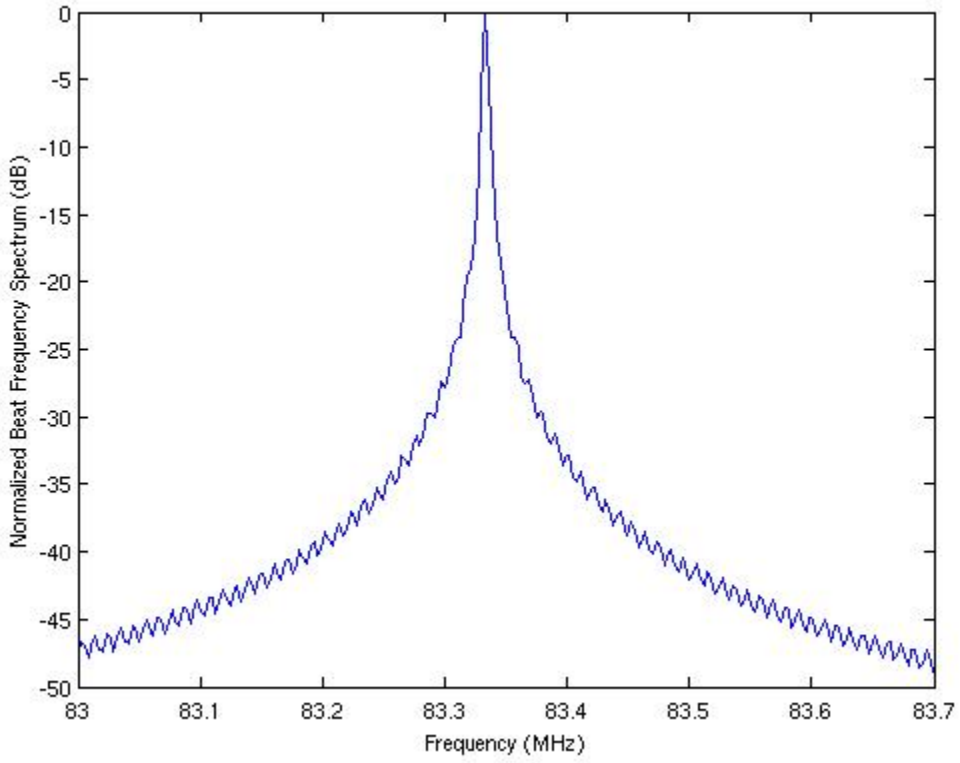


Figure 2-10: Zoomed Beat Frequency Spectrum at 1500 m with Decaying Frequency Chirp Amplitude

2.3 Amplitude Leveling

An example chirp waveform with amplitude distortion is shown in Figure 2-11 in order to explain the process of amplitude leveling using a variable-gain amplifier. The output power of the example chirp decreases over time and has a sinusoidal ripple causing variation in output power. Since there is no additional gain available to boost output power when it begins to drop, gain must be backed off to bring output power over all chirp frequencies down to the minimum output power level. This is illustrated in Figure 2-12.

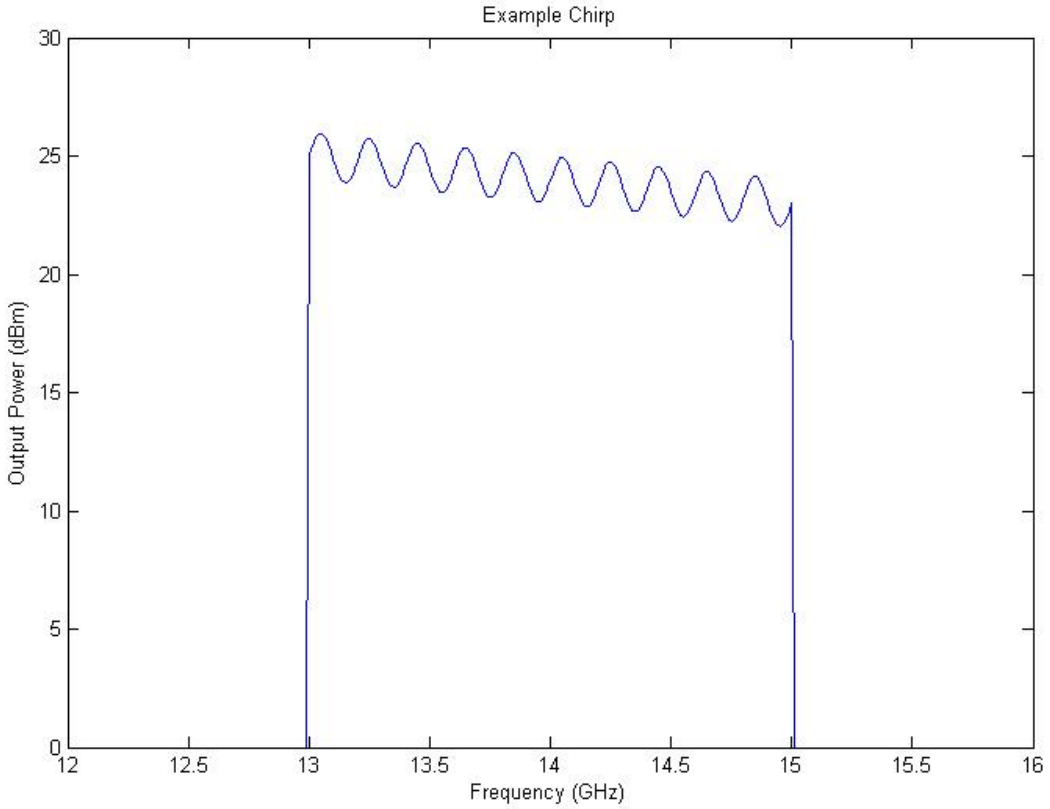


Figure 2-11: Example Chirp Waveform with Amplitude Distortion

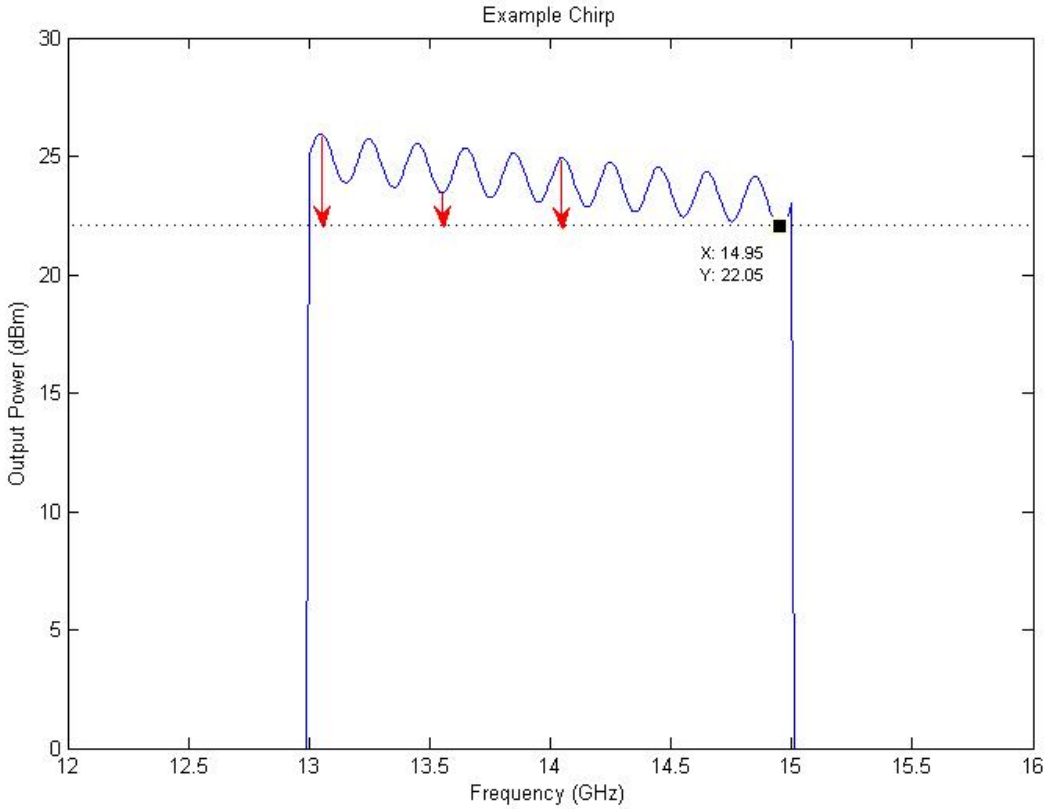


Figure 2-12: Amplitude Leveling for Example Chirp Waveform

Since the minimum output power for the example chirp is 22.05 dBm at 14.95 GHz, after ideal leveling the output power will be 22.05 dBm at all chirp frequencies. The different arrow lengths in the figure show that the gain must be backed off by different amounts at different frequencies. The gain for a variable-gain amplifier is controlled by a control voltage. This voltage is adjusted to different levels over the chirp so that the amplifier gain gives an output power of 22.05 dBm at each frequency. An ideal amplitude leveled version of the example chirp is shown in Figure 2-13.

The control voltage can be determined with different methods. A closed-loop method can be used in which the output power is sensed and then feedback through a system that determines the appropriate control voltage based on the output power and the desired leveled output power. An

open-loop method can also be used. Output power is measured over the chirp, the necessary control voltages are calculated for constant output power, and the calculated control voltage waveform is input to the variable-gain amplifier in sync with the chirp. This method levels the output power without any feedback but is susceptible to changes in the system over time.

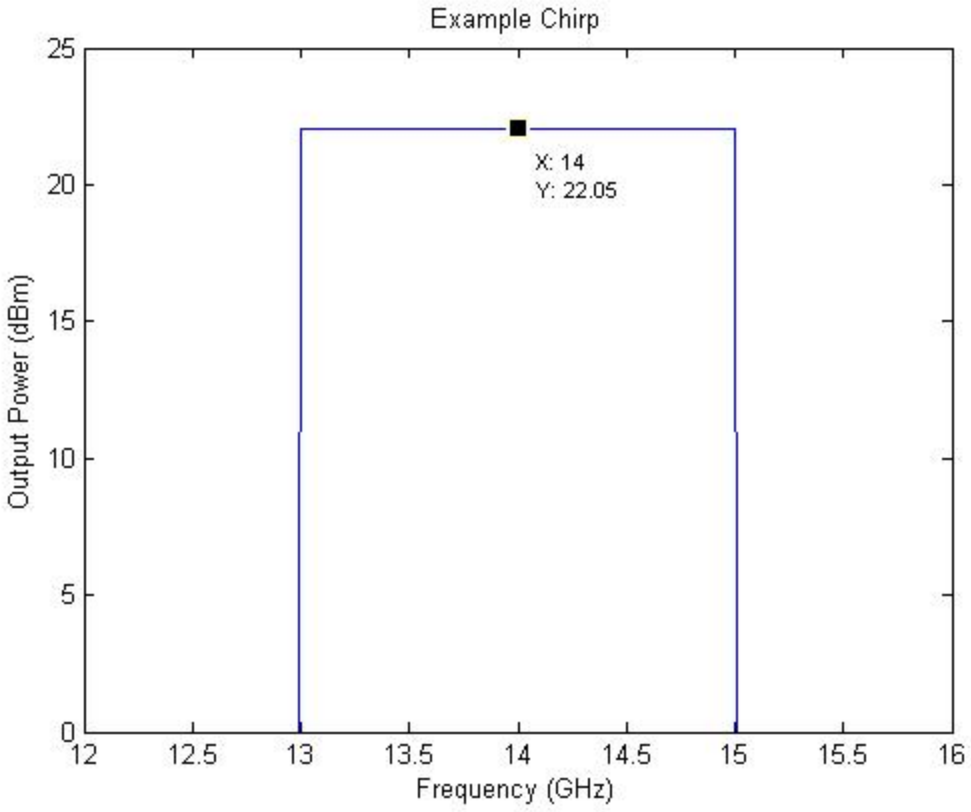


Figure 2-13: Ideal Amplitude Leveled Example Chirp

CHAPTER 3: CLOSED-LOOP DESIGN AND IMPLEMENTATION

3.1 Design Overview

An overall block diagram of the amplitude control subsystem is shown in Figure 3-1. The TriQuint TGA2509 wideband amplifier is used as the power amplifier for the radar system, and the remaining components in the subsystem are used for amplitude leveling. A portion of the transmit signal is coupled off by the RF-Lambda RFDC2G18G30 ultra wideband directional coupler and fed to the Hittite HMC613LC4B successive detection log video amplifier through an attenuator. A voltage proportional to the power of the signal input to the log video amplifier is output to a feedback circuit which scales this voltage for use as a control voltage for the power amplifier. The feedback circuit also controls voltage sequencing for startup of the power amplifier. All components are chosen to have wide bandwidth so that the subsystem can easily be used with different radar systems. Detailed descriptions of the subsystem components are given in this chapter.

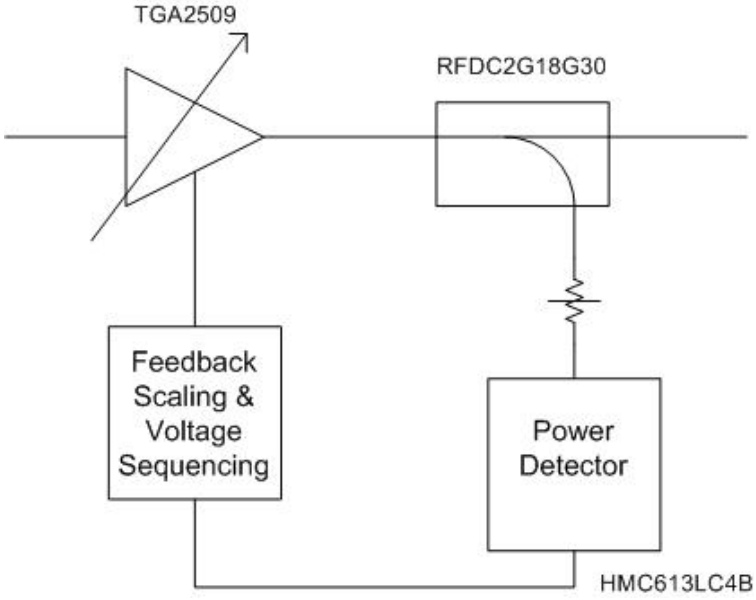


Figure 3-1: Amplitude Control Loop Block Diagram

3.2 Power Amplifier

The variable-gain power amplifier used in the amplitude control subsystem is the TriQuint TGA2509 wideband power amplifier. Key parameters of this power amplifier are summarized in Table 3-1 [4].

Table 3-1: TGA2509 Parameters

Frequency Range	2-20 GHz
P1dB	29 dBm
Nominal Gain	15 dB
AGC Range	25 dB

In order to limit the cost of producing this subsystem, amplifier units were constructed in house instead of purchasing evaluation boards. Printed circuit boards were designed based on the evaluation board layout information provided by TriQuint [5]. These boards were created using Altium Designer 6 and were fabricated using 20 mil Rogers 4003 material. Southwest Microwave Super SMA 5 mil pin end launch connectors are used in construction of the completed amplifiers. A completed amplifier is shown in Figure 3-2, and detailed construction information is given in Appendix A.

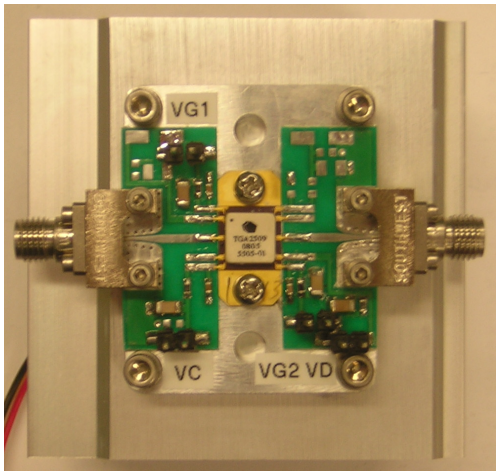


Figure 3-2: Completed Power Amplifier

Measured gain versus frequency for a constructed power amplifier is shown in Figure 3-3. A maximum gain of 18.9 dB occurs at 2 GHz, and a minimum gain of 13.6 dB occurs at 17 GHz. This gives a total variation of 5.3 dB over the 2 to 20 GHz range of the amplifier. Measured gain versus frequency for the same constructed power amplifier is shown in Figure 3-4 for the original frequency range of the Ku-band Radar, 13 to 17 GHz. In this range a maximum gain of 16.9 dB occurs at 13 GHz, and a minimum gain of 13.6 dB occurs at 17 GHz. This gives a total variation of 3.3 dB over the 13 to 17 GHz range of the Ku-band Radar. Measurements for three constructed amplifiers are shown in Figure 3-5 for comparison purposes. The three gain curves agree well over most frequencies. These measurements are taken with the control voltage of the amplifier open using a network analyzer and input power of 0 dBm.

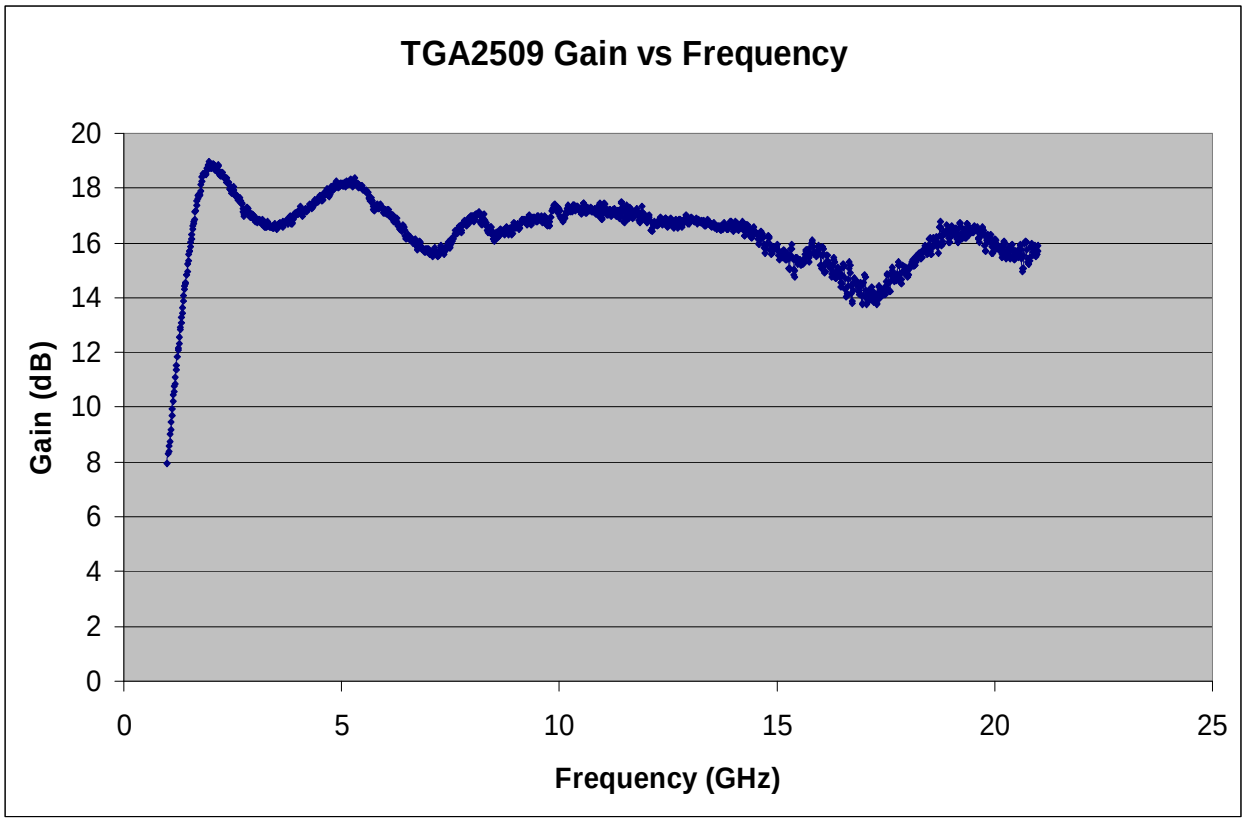


Figure 3-3: TGA2509 Gain versus Frequency for Constructed Power Amplifier

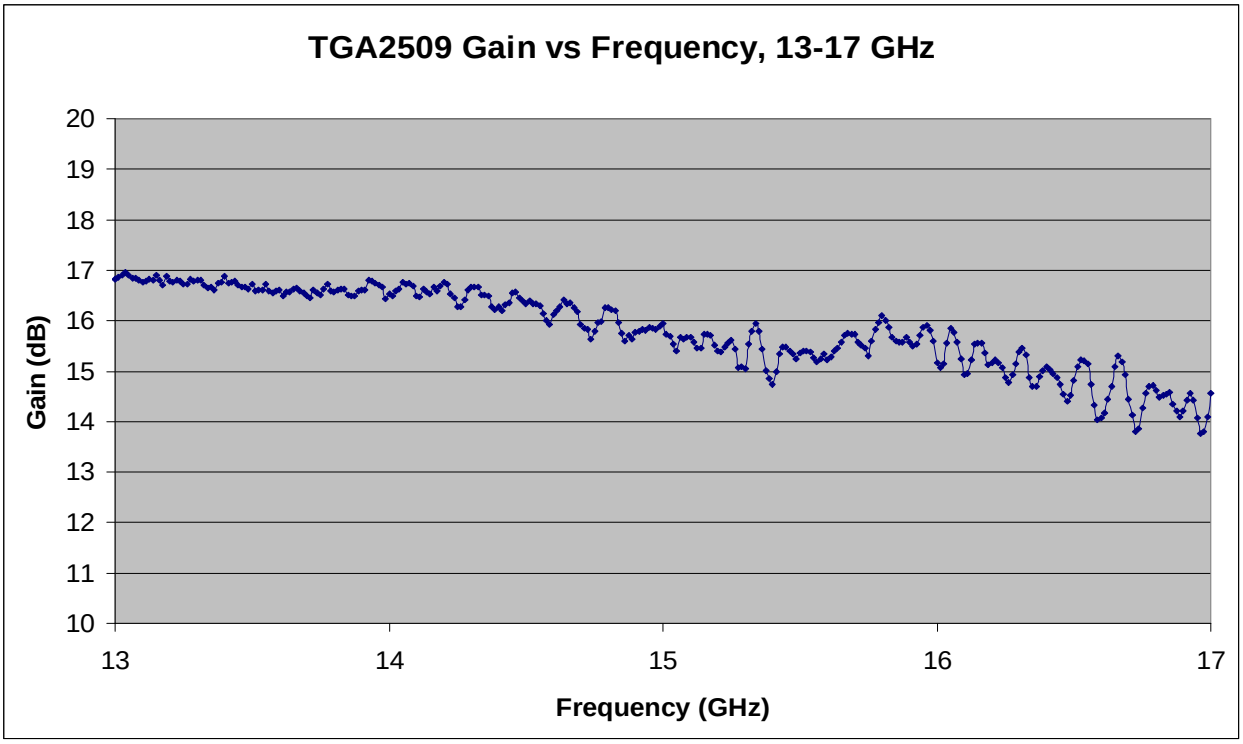


Figure 3-4: TGA2509 Gain versus Frequency for Constructed Amplifier, 13-17 GHz

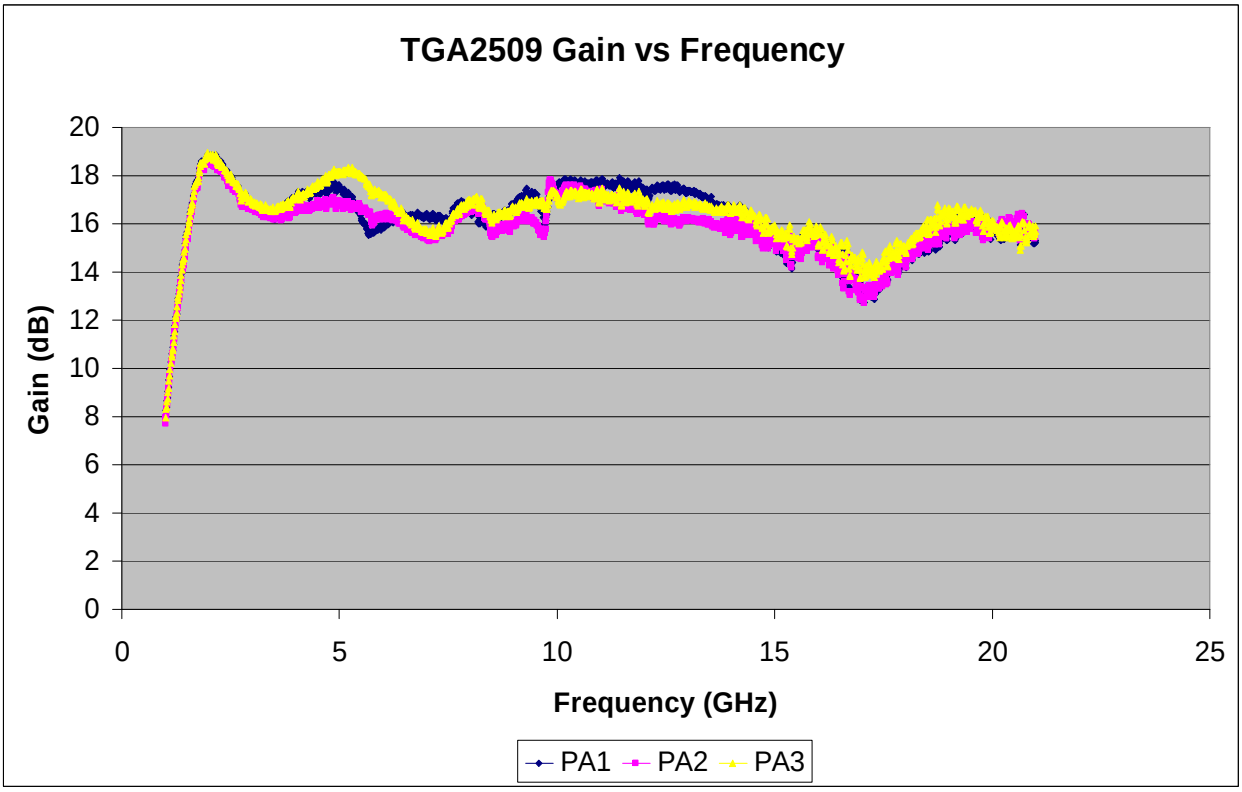


Figure 3-5: TGA2509 Gain versus Frequency for Three Constructed Amplifiers

The gain of the power amplifier can be controlled when a control voltage is applied as opposed to leaving the control voltage open. For the TGA2509 power amplifier, a control voltage between -2 V and 5 V can be used, with higher voltages yielding higher gain values and -2 V yielding the lowest gain values [4]. Gain versus frequency for control voltages between 0.049 V and 0.47 V is shown in Figure 3-6; these measurements were taken with a network analyzer and input power of 0 dBm. The lowest control voltage of 0.049 V produces the lowest gain values, and the highest control voltage of 0.47 V produces the highest gain values. Gain will continue to decrease as the control voltages decreases below 0.049 V; however, gain is at a maximum with a control voltage around 0.6 V and will stay approximately the same as control voltage increases beyond 0.6 V. Gain versus control voltage for different frequencies between 13-17 GHz is shown in Figure 3-7. There is an area of linear increase in gain with increase in control voltage between approximately 0 V and 0.3 V, but as the control voltage increases past 0.3 V the gain begins to saturate, becoming approximately constant beyond 0.6 V. The linear region is shown in Figure 3-8; this range of control voltages is used for amplitude leveling and will be discussed further regarding feedback to the amplifier. Biasing for the amplifier will be discussed in the section on feedback scaling and voltage sequencing.

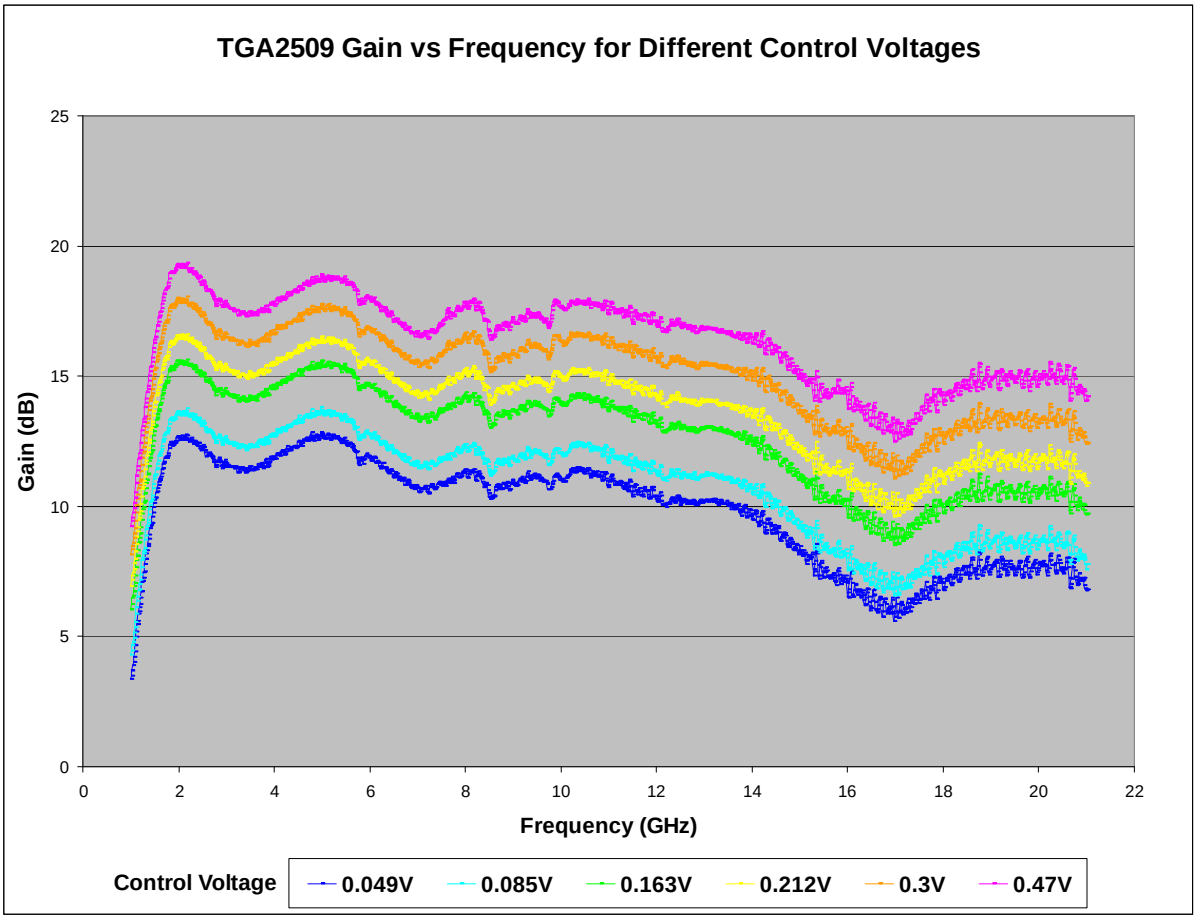


Figure 3-6: TGA2509 Gain versus Frequency for Different Control Voltages

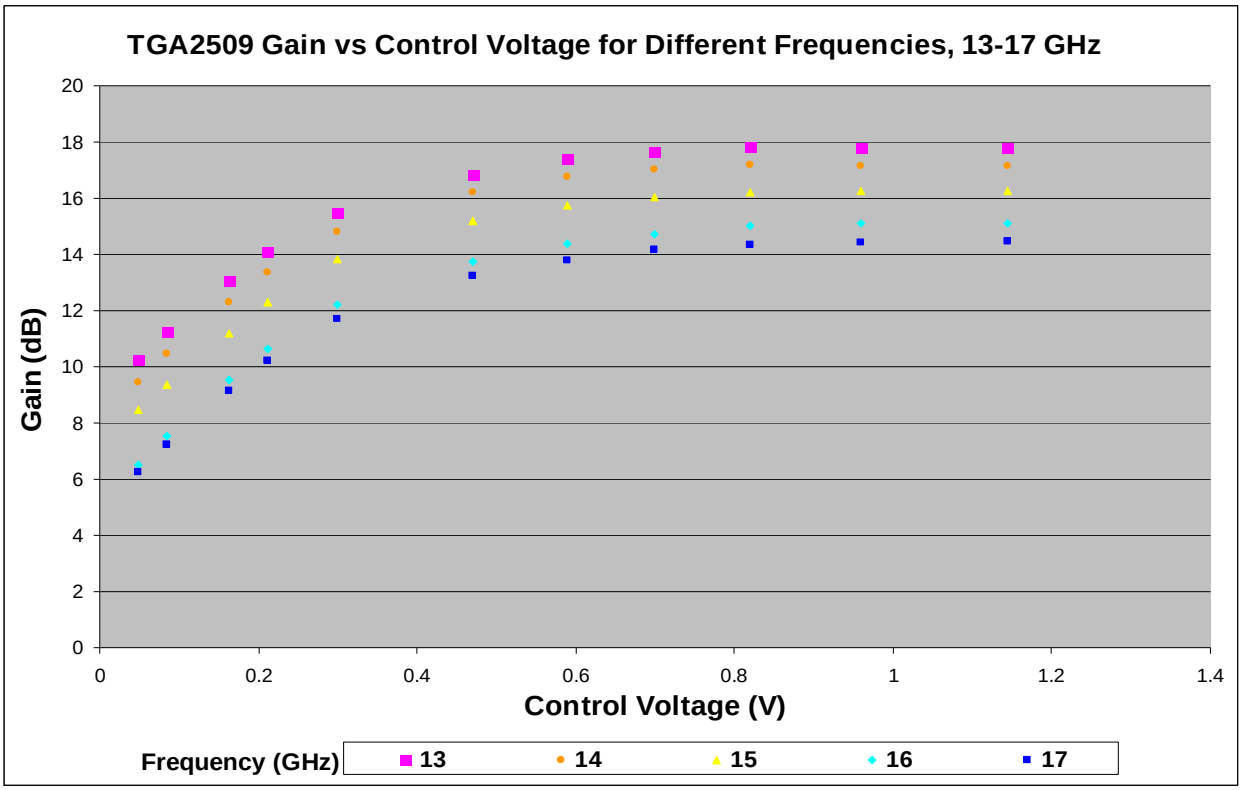


Figure 3-7: TGA2509 Gain versus Control Voltage for Different Frequencies, 13-17 GHz

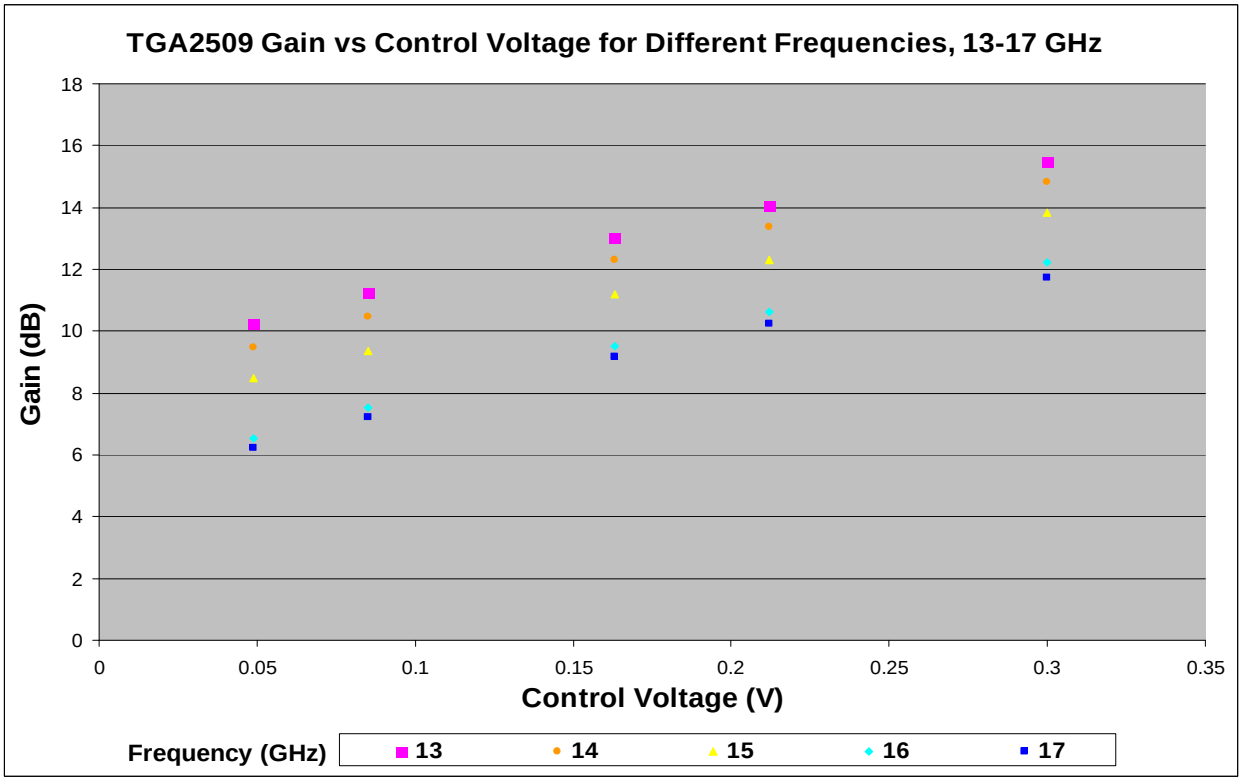


Figure 3-8: Linear Region of TGA2509 Gain versus Control Voltage, 13-17 GHz

3.3 Coupler

The coupler used in the amplitude control subsystem is the RF-Lambda RFDC2G18G30 ultra wideband directional coupler. Key parameters of this coupler are summarized in Table 3-2 [6].

Table 3-2: RFDC2G18G30 Parameters

Frequency Range	2-18 GHz
Power	50 W CW
VSWR	1.5:1
Insertion Loss	0.7 dB
Coupling	30 ± 1.0 dB
Directivity	12 dB

Measured mainline loss and coupling for the directional coupler are shown in Figure 3-9 and Figure 3-10, respectively. These measurements were taken in the lab with a network analyzer. Mainline loss through the coupler is less than 0.9 dB over the frequency range of the coupler, and coupling is approximately 30 dB with around 1 dB of variation. These measurements are within 0.2 dB of the data sheet specifications for the coupler.

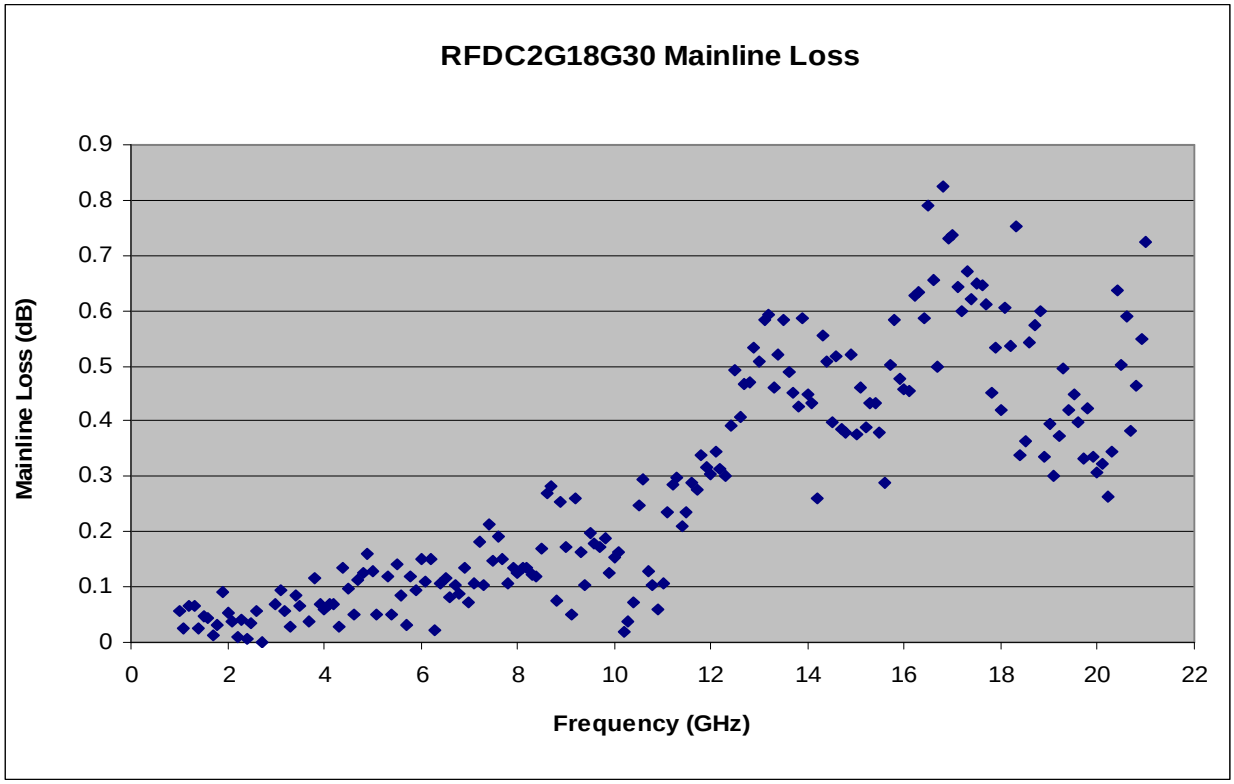


Figure 3-9: RFDC2G18G30 Mainline Loss

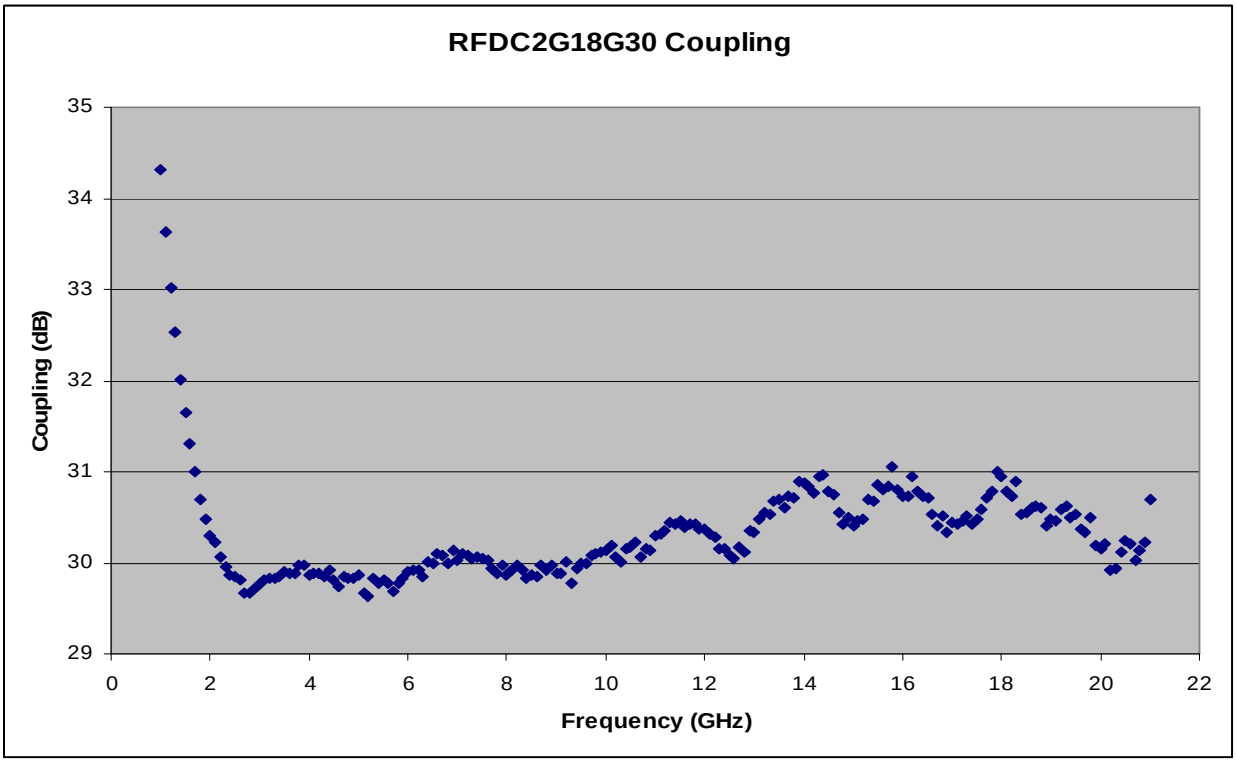


Figure 3-10: RFDC2G18G30 Coupling

3.4 Attenuator

The attenuator in the amplitude control subsystem attenuates the coupled power to an appropriate level for the power detector. The signal power level at the input to the power detector is chosen to be in the middle of the most linear part of the band to minimize error. Video output and error for the HMC613LC4B power detector are shown for 14 GHz in Figure 3-11 [7]. The plot at 14 GHz is used since it is the only provided plot in the frequency range of the Ku-band Radar. In order to minimize errors and keep the video output as linear as possible with respect to input power, the center of the input signal power is chosen to be -31 dBm. Since variation in signal power is 3.3 dB over the 13-17 GHz frequency range, input power levels will range from approximately -33 to -29 dBm. With a maximum output power of 27 dBm and coupling of 30 dB, this gives an attenuation value of 26 dB, as calculated in Equation 3-1. After testing in the lab, this attenuation value was decreased to 20 dB to account for cable losses.

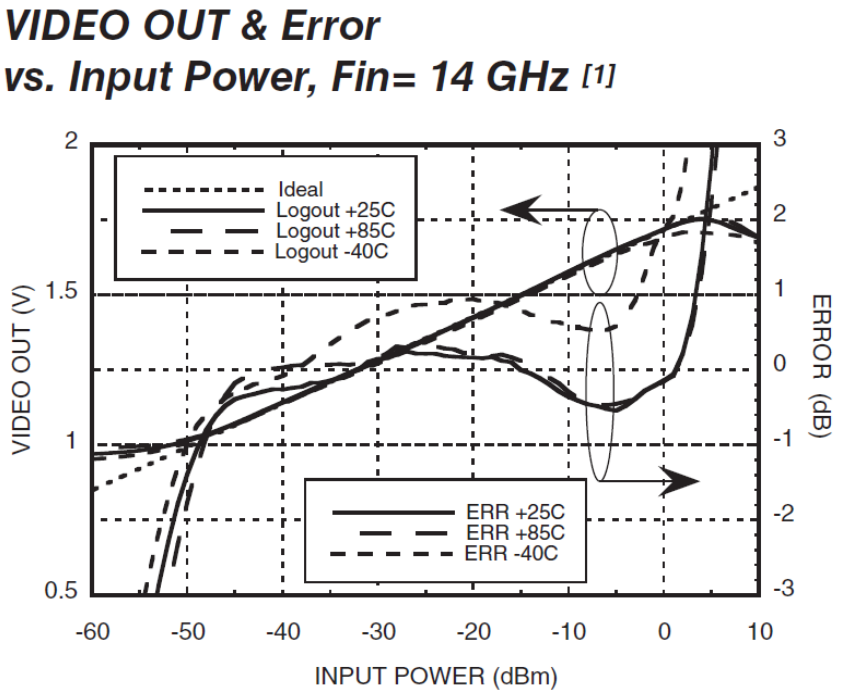


Figure 3-11: HMC613LC4B Video Out and Error at 14 GHz

$$A(dB) = P_{out}^{\max}(dBm) - Coupling(dB) + 29dBm = 27dBm - 30dB + 29dBm = 26dB \quad \textbf{3-1}$$

3.5 Power Detector

The power detector used for this subsystem is the Hittite HMC613LC4B successive detection log video amplifier evaluation board. Key parameters for the HMC613LC4B power detector are summarized in Table 3-3, and a functional diagram is shown in Figure 3-12 [7]. The power detector is operated in single-ended mode on the evaluation board with the negative input terminal connected to ground through a capacitor and resistor and video feedback tied directly to video output. This means that the power detector output is based directly on the power of one input signal only; no comparison of power levels is being done.

Table 3-3: HMC613LC4B Parameters

Frequency Range	0.1-20 GHz
Logging Range	-54 to +5 dBm
Log Linearity	±1 dBm
Output Voltage Range	1.0 to 1.8 V
Output Slope	14 mV/dB

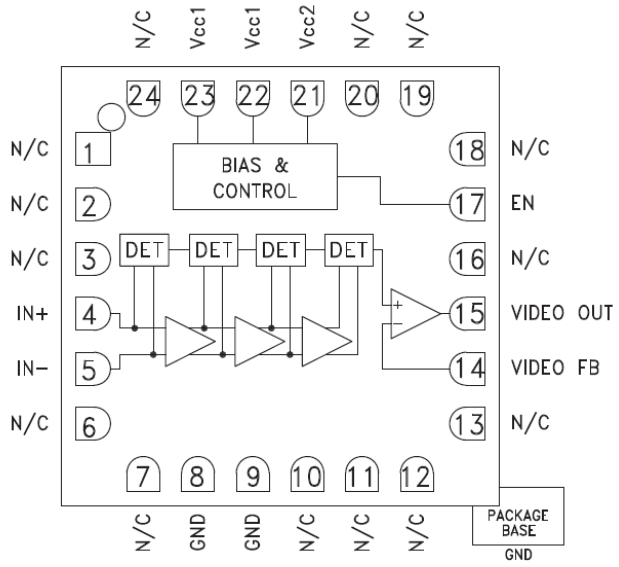


Figure 3-12: HMC613LC4B Functional Diagram

The power detector outputs a voltage between 1.0 and 1.8 V proportional to the input power as long as it is in the logging range. Higher input power corresponds to a higher output voltage. Output voltage versus input power was measured in the lab by inputting measured power levels to the power detector and measuring the output voltages over different frequencies. Results are shown in Figure 3-13 for input powers between -37 and -26 dBm in the Ku-band frequency range. Although there is variation with frequency, there is no definite trend in output voltage as frequency increases. Figure 3-14 shows measurements of input power versus output voltage over all frequencies with a trendline. The average output slope for these input powers is 13.5 mV/dB with an offset of 1.76 V.

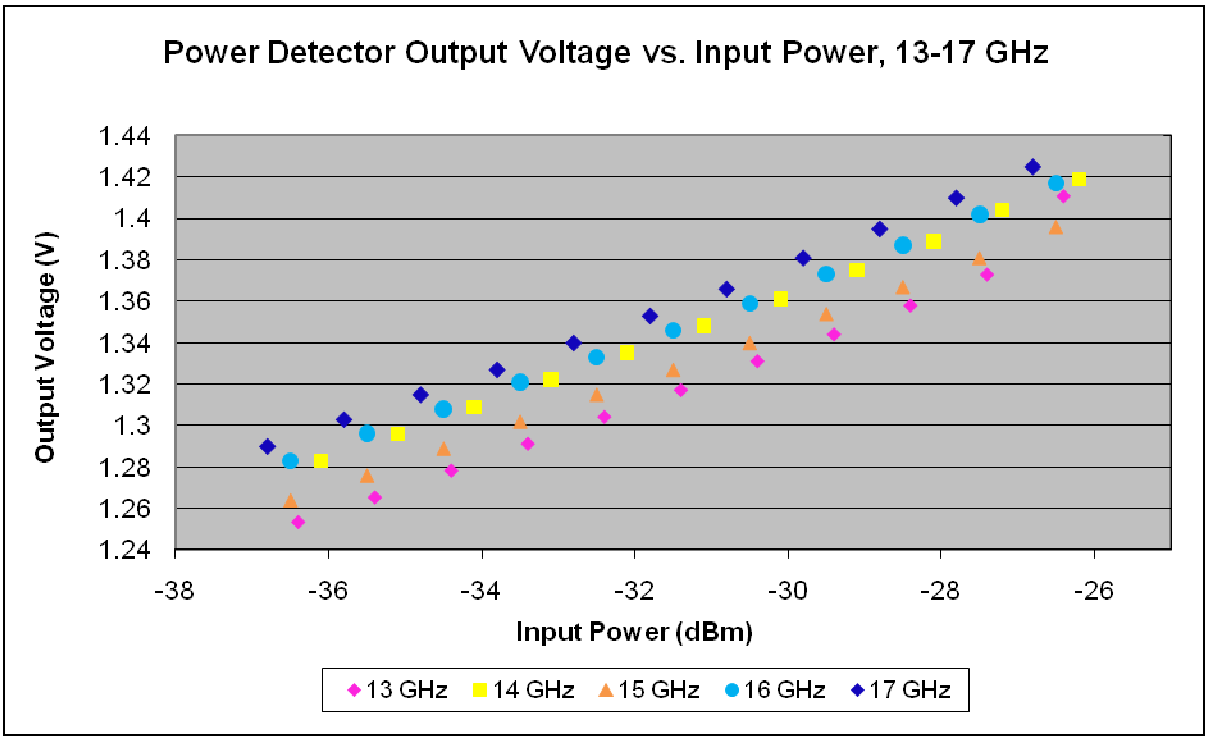


Figure 3-13: HMC613LC4B Output Voltage versus Input Power, 13-17 GHz

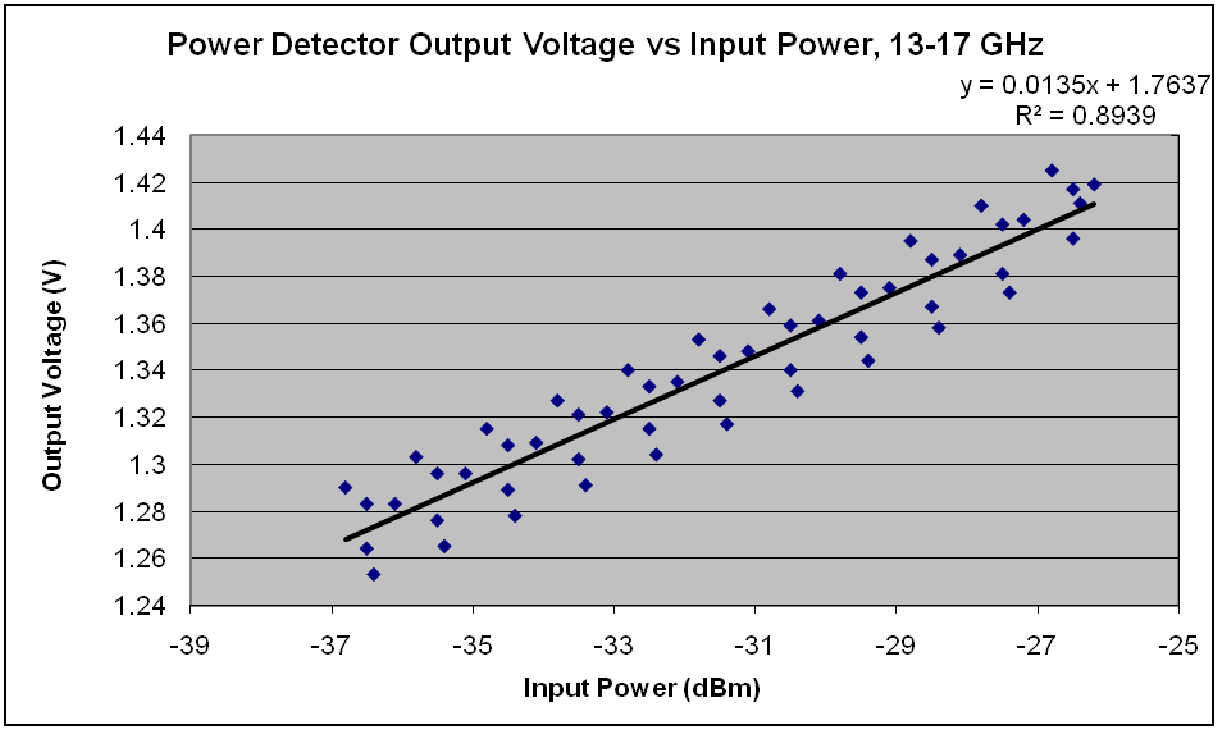


Figure 3-14: HMC613LC4B Output Voltage versus Input Power with Trendline, 13-17 GHz

3.6 Feedback Scaling and Voltage Sequencing

The feedback scaling and voltage sequencing component serves two main purposes which will be discussed in separate sections. This board scales the output of the power detector, which is linear with respect to input power, to the appropriate control voltage for the power amplifier, which is linear with respect to gain. It also provides the correct voltage sequence for powering on and off the power amplifier; this is required to avoid damage to the device.

3.6.1 Feedback Scaling

The feedback scaling portion of the circuit scales the linear output of the power detector to the appropriate linear control voltage for the power amplifier. This is done with one differencing amplifier and one inverting amplifier as shown in Figure 3-15.

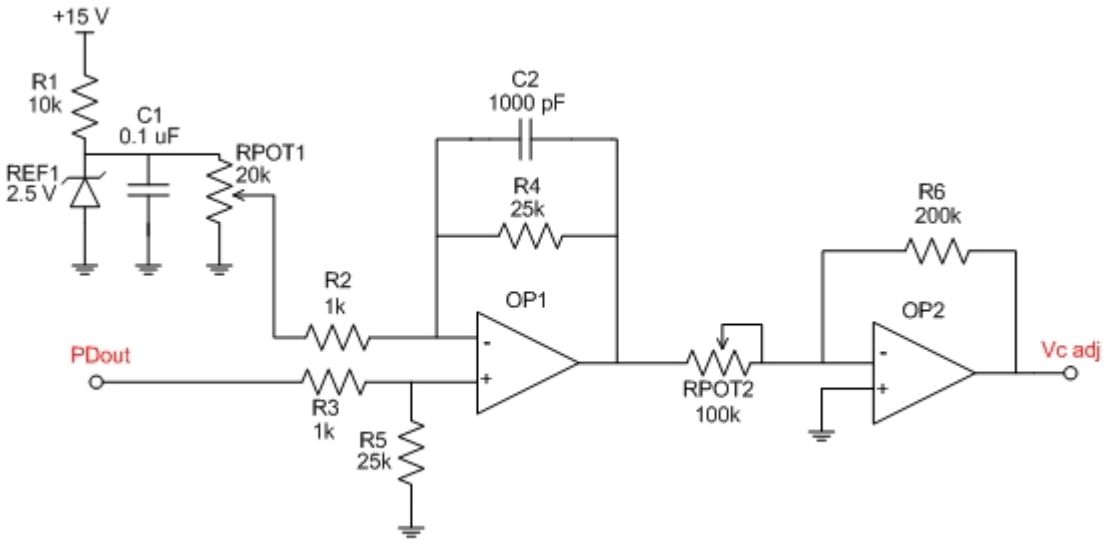


Figure 3-15: Feedback Scaling Schematic

Voltage reference REF1 gives a 2.5 V reference voltage over potentiometer RPOT1, and RPOT1 acts as an adjustable voltage divider to give a reference voltage to the differencing amplifier. Input PD_{out} is the output voltage of the power detector; this is the other input to the differencing amplifier. Differencing amplifier OP1 amplifies the difference between the output of the power detector and the reference voltage from RPOT1. The gain of OP1 is set by $R4/R2 = R5/R3 = 25$, and the output of OP1 is $25(PD_{out} - V_{ref})$. Capacitor C2 and resistor R4 act as a filter to prevent the control voltage from changing too rapidly. Inverting amplifier OP2 provides adjustable gain for fine tuning of the control voltage. This circuit can be adjusted with RPOT1 and OP2 so that the control voltage Vc_{adj} is in the appropriate range.

3.6.2 Voltage Sequencing

The power amplifier requires that its bias voltages be sequenced on and off in a particular order to avoid damage to the device. Bias voltages to the power amplifier include: two separate gate voltages (Vg1 and Vg2), one drain voltage (Vd), and one control voltage (Vc). The recommended sequencing order is given in the list below [4].

For Biasing with AGC Control:

1) Apply -1.2 V to Vg1 and -1.2 V to Vg2
2) Apply +12 V to Vd
3) Apply +2.6 V to Vc
4) Adjust Vg1 to attain 580 mA drain current (Id)
5) Adjust Vg2 to attain 1080 mA drain current (Id)
6) Adjust Vc as needed to control gain level

In order to attain 580 mA drain current, Vg1 is adjusted to -0.3 V; to obtain 1080 mA total drain current, Vg2 is adjusted to -0.4 V. A simplified voltage sequencing schematic is shown in Figure 3-16 for the purposes of explaining the basics of the circuit. A full schematic can be found in Appendix B. When the “IN” pin of a switch is low, the top input is connected to the output, and when the “IN” pin is high, the bottom input is connected to the output. The “Q´” output of the flip-flop is initially low and goes high once a high voltage is applied to the reset pin.

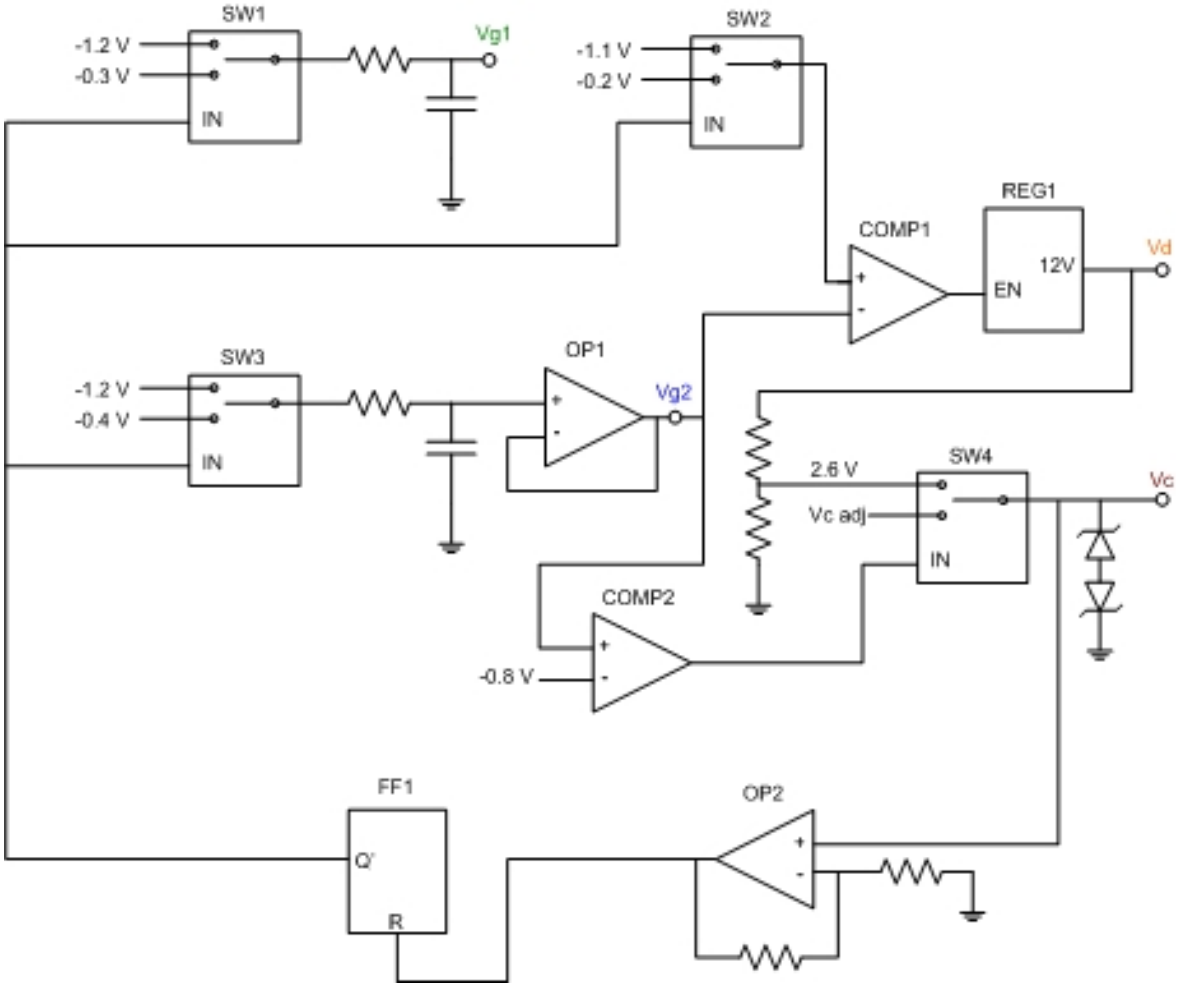


Figure 3-16: Simplified Voltage Sequencing Schematic

When power is first applied to the circuit, the -1.2 V switch inputs of SW1 and SW3 are connected to the switch outputs; Vg1 and Vg2 change from 0 V to -1.2 V with the RC time constants of the resistor and capacitor pairs, satisfying Step 1 of the previous list. Operational amplifier OP1 acts as a voltage follower for Vg2, keeping the gate voltage constant as the second gate current varies. Initially, -1.1 V is applied to the positive input pin of COMP1. Once Vg2 becomes more negative than -1.1 V, the comparator output will go high and enable the 12 V regulator output to Vd. This satisfies Step 2. When the 12 V output is on, 2.6 V will be applied to SW4. Because the output of COMP2 is initially low, 2.6 V will be output to Vc, satisfying Step 3. The Zener diodes on the Vc output protect the amplifier by keeping the control voltage in the allowable range. The 2.6 V output is amplified by OP2 in order to be seen as a high signal by flip-flop FF1. This signal resets the flip-flop, causing the initially low "Q´" output to go high. This high output is input to SW1 and SW3 to switch Vg1 and Vg2 to -0.3 V and -0.4 V, respectively. This satisfies Steps 4 and 5. In order to keep the 12 V Vd output on, the high "Q´" output is also applied to SW2. The new Vg2 voltage of -0.4 V will then be compared to -0.2 V instead of -1.1 V, keeping the 12 V regulator enabled. When Vg2 switches from -1.2 V to -0.4 V, the output of COMP2 will go high. The high output of COMP2 is input to SW4 and causes the adjustable control voltage discussed in the previous section to be connected to Vc. This completes Step 6 and the turn on sequence. Table 3-4 shows the device outputs over time for the voltage sequencing schematic. Changes are highlighted in red.

Table 3-4: Voltage Sequencing Device Outputs over Time

Device	**Time →**					
COMP1	LOW	LOW	HIGH	HIGH	HIGH	HIGH
COMP2	LOW	LOW	LOW	LOW	LOW	HIGH
FF1	LOW	LOW	LOW	LOW	HIGH	HIGH
OP1	LOW	LOW	LOW	HIGH	HIGH	HIGH
REG1 (**Vd**)	0 V	0 V	12 V	12 V	12 V	12 V
SW1 (**Vg1**)	0 V	-1.2 V	-1.2 V	-1.2 V	-0.3 V	-0.3 V
SW2	0 V	-1.1 V	-1.1 V	-1.1 V	-0.2 V	-0.2 V
SW3 (**Vg2**)	0 V	-1.2 V	-1.2 V	-1.2 V	-0.4 V	-0.4 V
SW4 (**Vc**)	0 V	0 V	0 V	2.6 V	2.6 V	Vc adj

In order to keep from damaging the power amplifier when powering down, the drain voltage Vd must be turned off before the gate voltages Vg1 and Vg2. The RC time constants on the outputs of Vg1 and Vg2 keep these gate voltages on after the power is turned off in order to protect the amplifier. The 12 V Vd output does not have a RC circuit on its output and turns off when power is switched off.

CHAPTER 4: CLOSED-LOOP RESULTS

4.1 Results

The output of the subsystem was measured on a spectrum analyzer with and without the control voltage feedback connected; a signal at 11 dBm with a 10 ms sweep from 13 to 15 GHz was input to the power amplifier. The spectrum of the subsystem output without control voltage feedback to the amplifier is shown in Figure 4-1 after 10 dB attenuation. The maximum power output is 12.68 dBm at 13.3475 GHz, shown by Marker 1, and the minimum power output is 9.35 dBm at 14.8925 GHz, shown by Marker 2. This gives a total difference between maximum and minimum of 3.33 dB. Losses through cables, the attenuator, and the coupler total approximately 18 dB without the amplifier in the line; the gain of the amplifier varies between 16.35 dB and 19.68 dB.

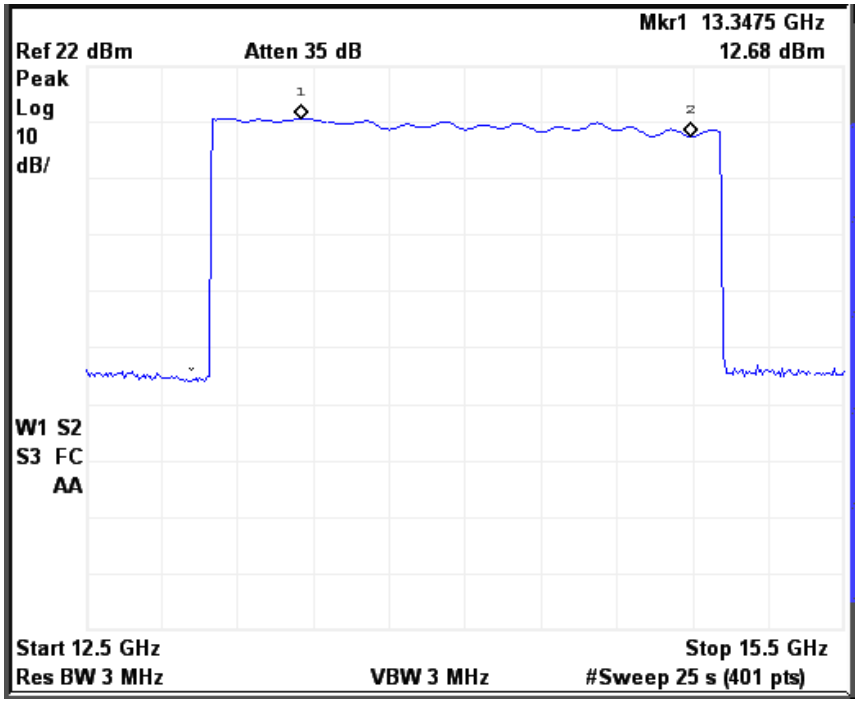


Figure 4-1: Spectrum of Subsystem Output without Control Voltage Feedback

Figure 4-2 shows the same subsystem output spectrum with a trendline. Output power falls off at an average of 1.2113 dB per GHz. Maximum deviation from the linear approximation is +1.21 dB at 14.52 GHz. Maximum deviation below the linear approximation is -1.02 dB at 13.70 GHz; this gives a total difference between positive and negative deviations of 2.23 dB. Without control voltage feedback, output power follows a linear approximation with variation of ±1.21 dB.

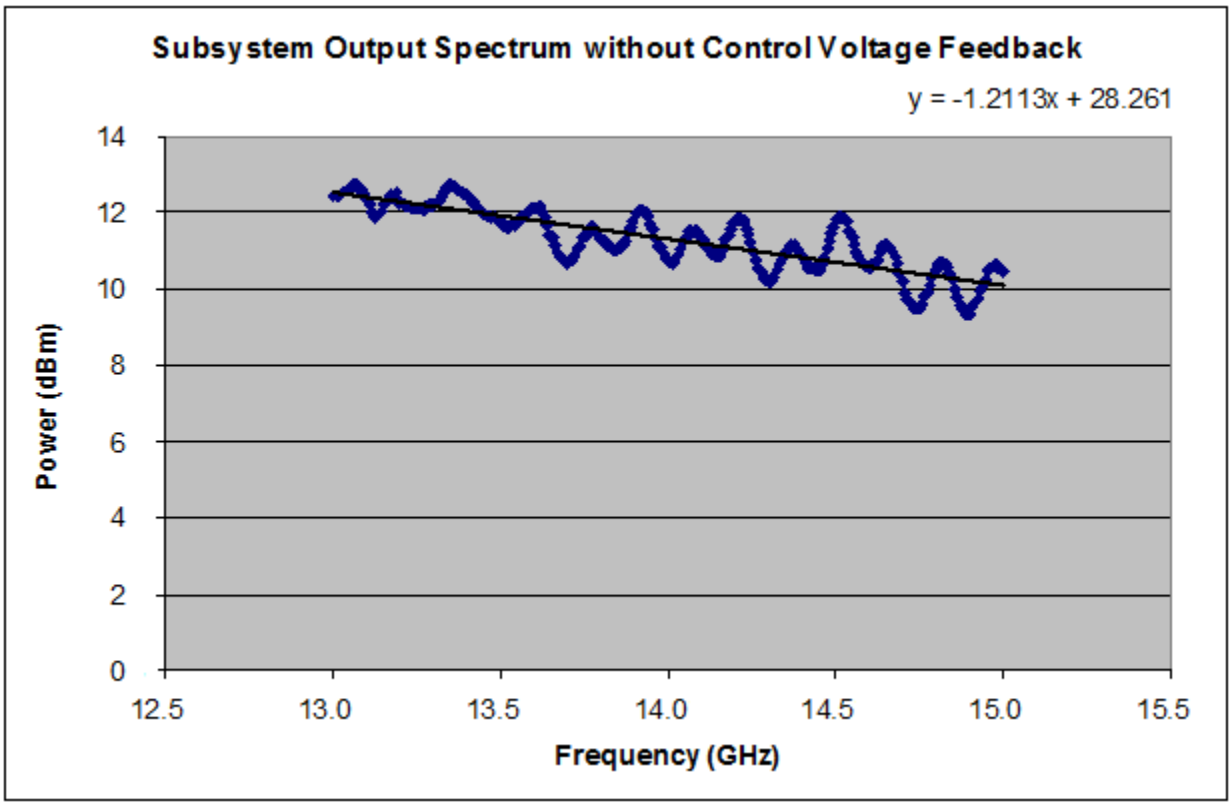


Figure 4-2: Subsystem Output Spectrum without Control Voltage Feedback with Trendline

With the control voltage feedback connected, the subsystem output spectrum is shown in Figure 4-3 after 10 dB attenuation. The maximum power output is 9.37 dBm at 13.3625 GHz, shown by Marker 1, and the minimum power output is 7.49 dBm at 14.9975 GHz, shown by Marker 2. This gives a total difference between maximum and minimum of 1.88 dB. Losses through cables,

the attenuator, and the coupler again total approximately 18 dB without the amplifier in the line so the gain of the amplifier varies between 14.49 dB and 16.37 dB.

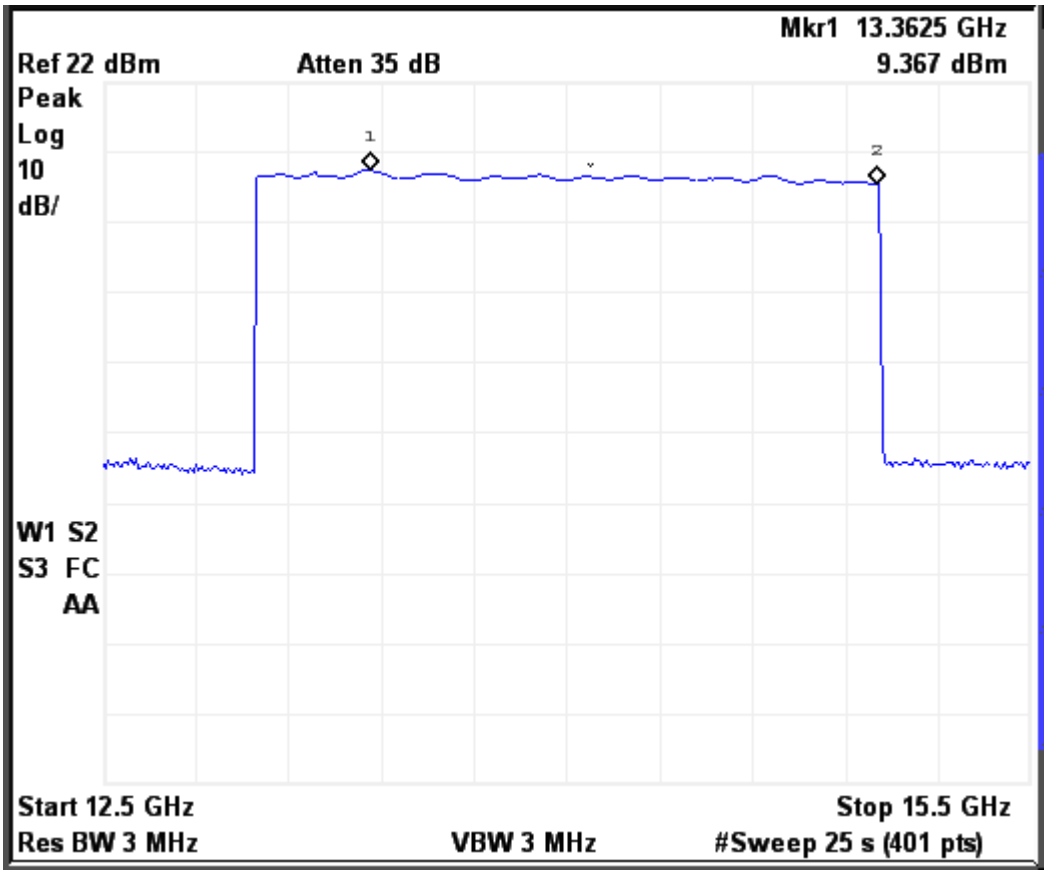


Figure 4-3: Subsystem Output Spectrum with Control Voltage Feedback

Figure 4-4 shows the same subsystem output spectrum with a trendline. Output with control voltage feedback connected falls off at approximately -0.5126 dB per GHz. Maximum deviation from the linear approximation is +0.72 dB at 13.36 GHz. Maximum deviation below the linear approximation is -0.57 dB at 13.12 GHz; this gives a total difference between positive and negative deviations of 1.29 dB. With control voltage feedback, output power follows a linear approximation with variation of ±0.72 dB. This is a smaller variation than without control voltage feedback by ±0.49 dB and a slower output power drop off by 0.6987 dB per GHz.

However, maximum output power when using control voltage feedback is 3.31 dB lower than without feedback. This is necessary since, when using feedback, output power must be backed off to the minimum output power without the feedback.

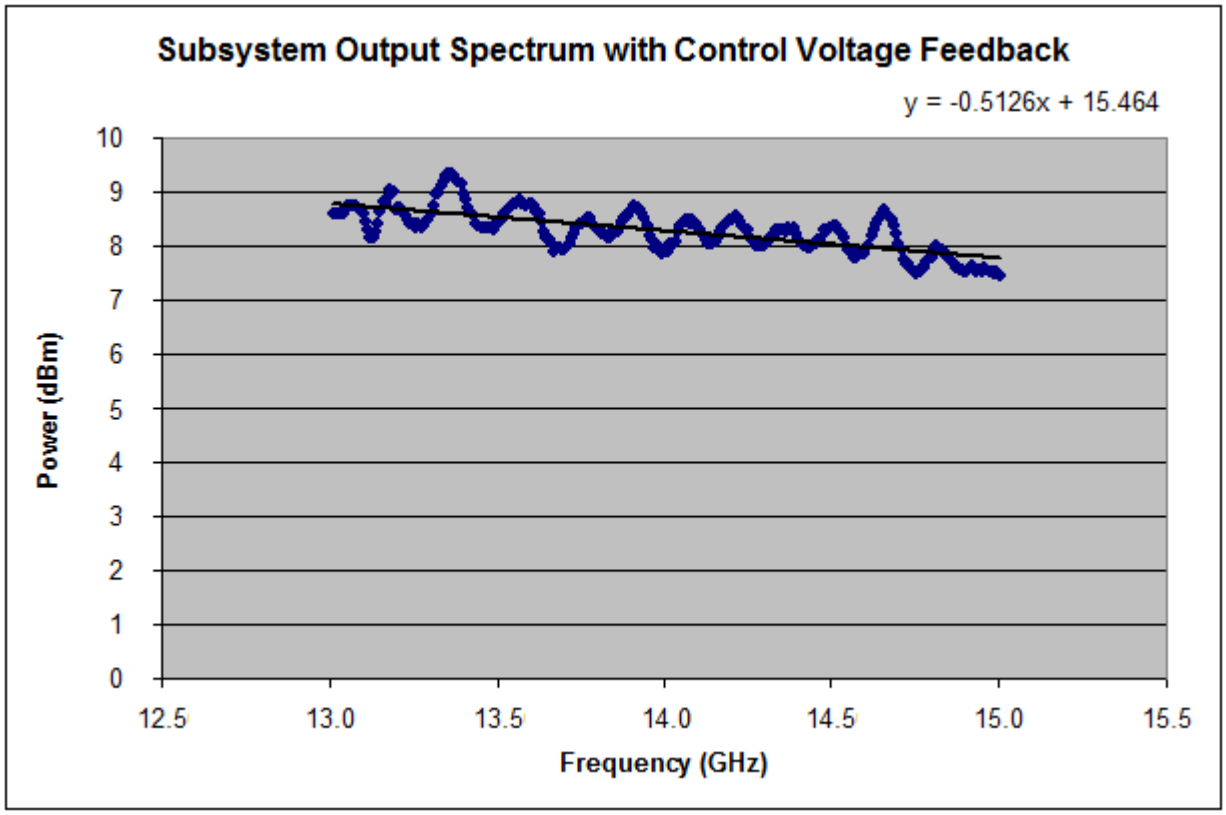


Figure 4-4: Subsystem Output Spectrum with Control Voltage Feedback with Trendline

Control voltage over time is shown in Figure 4-5; the top cursor is at a level of 4.0 V, and the bottom cursor is at a level of -94 mV. When the RF chirp is off and there is no power input to the power detector, the power detector output is 1.054 V. This lower voltage causes the control voltage output to be much higher than when the RF chirp is on. The control voltage output is limited to around 4.0 V by the Zener diode pair protecting the amplifier. When the RF chirp is on, the control voltage is proportional to the output power. A higher output power corresponds

with a lower control voltage. A closer view of the control voltage during the RF chirp is shown in Figure 4-6; the top cursor is at a level of 181 mV, and the bottom cursor is at a level of -50 mV. The control voltage adjusts based on the output voltage of the power detector to back off the gain of the amplifier by the correct amount to level the amplitude. The control voltage is lower at the beginning of the chirp since there is originally higher output power around 13 GHz and increases towards the end of the chirp since there is originally lower output power around 15 GHz.

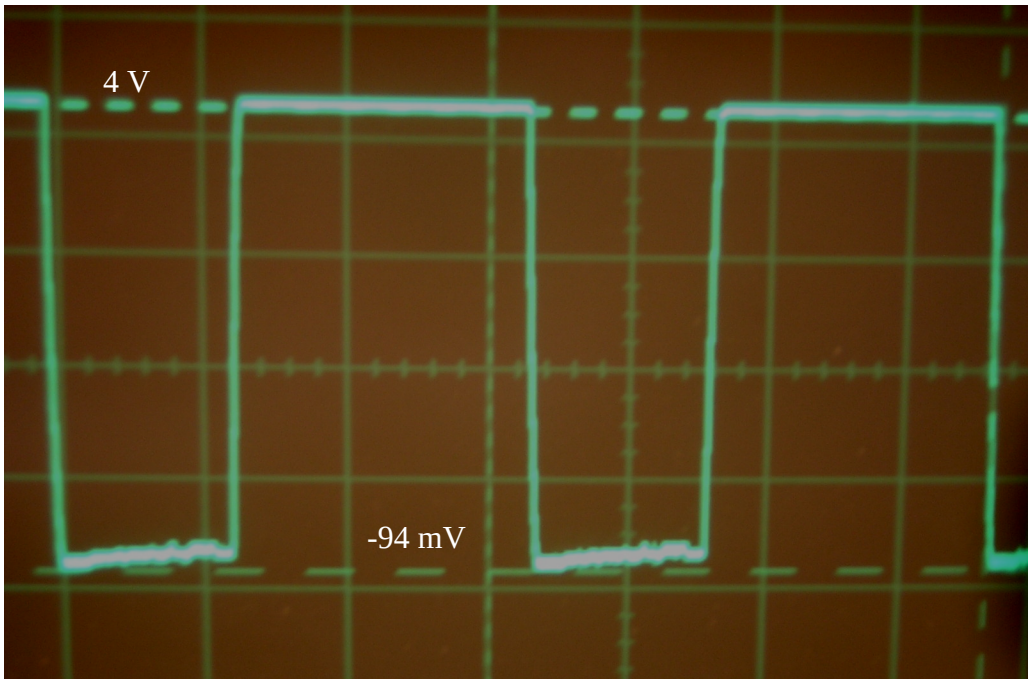


Figure 4-5: Control Voltage over Time with Control Voltage Feedback

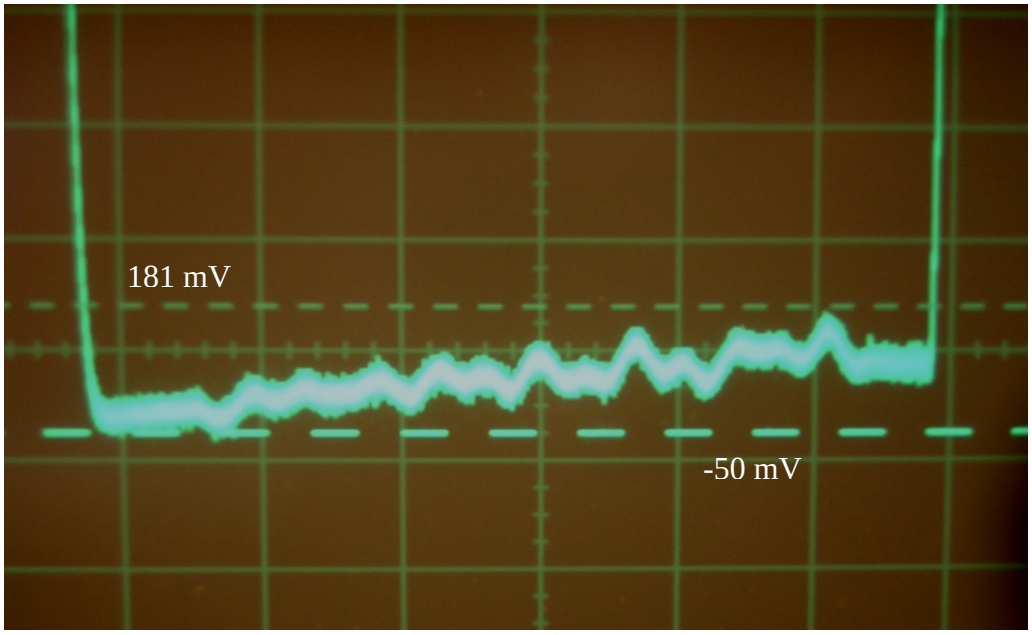


Figure 4-6: Control Voltage during RF Chirp with Control Voltage Feedback

4.2 Sources of Error

The control voltage feedback loop does not level the amplitude completely. There are still variations in amplitude over the frequency sweep that cannot be corrected using this method due to loss through the coupler outside of the loop and linear approximations of the power detector and control voltage. Each source of error along with its contribution will be discussed separately.

4.2.1 Coupler

The coupler introduces error into the subsystem since mainline loss is not constant over frequency and is in the transmit line but outside the feedback loop. These variations in output power will not be measured by the power detector. Another error is introduced by the coupler since coupling is not constant over frequency and is in the feedback loop but not in the transmit

line. These variations will be measured by the power detector and affect the control voltage even though they do not affect the output power.

However, because both mainline loss and coupling follow similar trends over frequency, the two sources of error can somewhat offset each other. For example, S_{21} and S_{31} both generally decrease as frequency increases. Decrease in S_{31} will cause there to be a lower power detected by the power detector than there would be if the coupling was constant, which translates to a higher output power. This, to an extent, compensates for decrease in S_{21}. Since error is based on amount of variation, normalized S-parameters are shown from 2 to 20 GHz in Figure 4-7 to show similarities in trends.

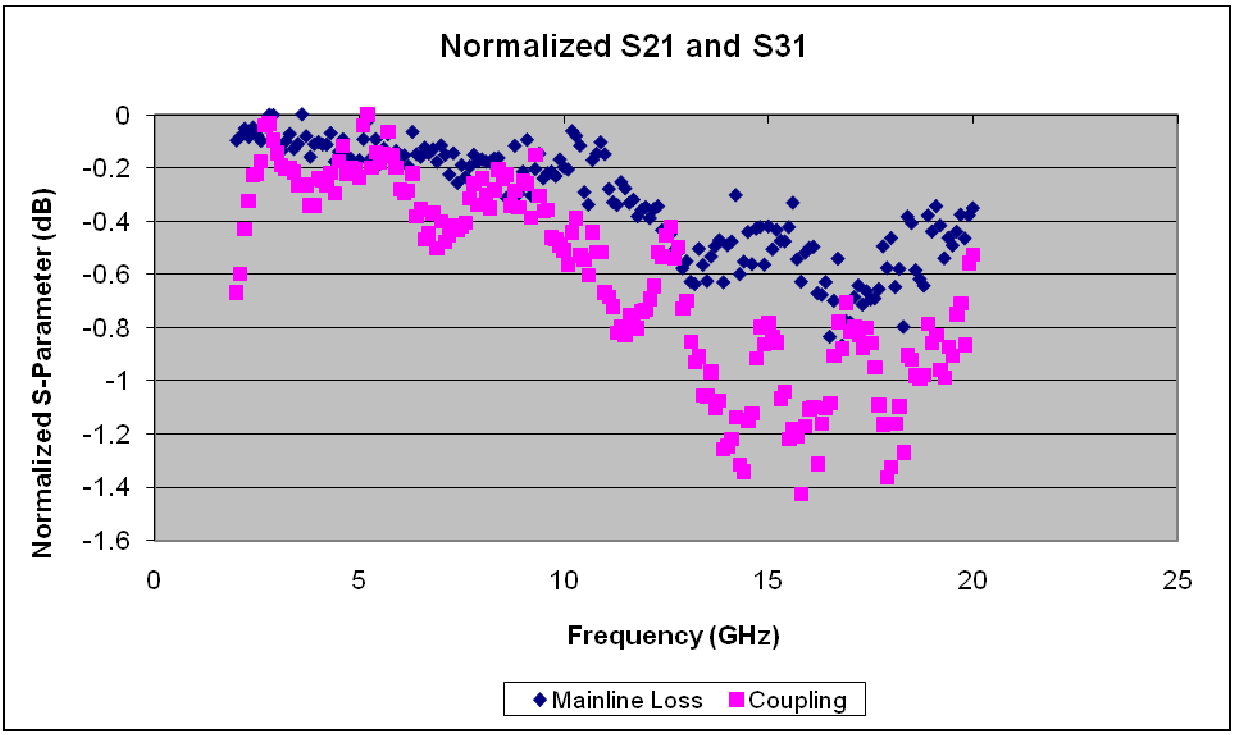


Figure 4-7: Normalized Coupler S-Parameters

Because errors due to S_{21} and S_{31} of the coupler counteract each other to some degree, the total error from the coupler is the difference between the two S-parameters. This difference is shown in Figure 4-8. Between 13 and 15 GHz, the maximum positive error is 0.83 dB at 14.2 GHz and the minimum positive error is 0.15 dB at 13.0 GHz. The difference between maximum and minimum error gives the total error associated with contribution to variation of 0.68 dB.

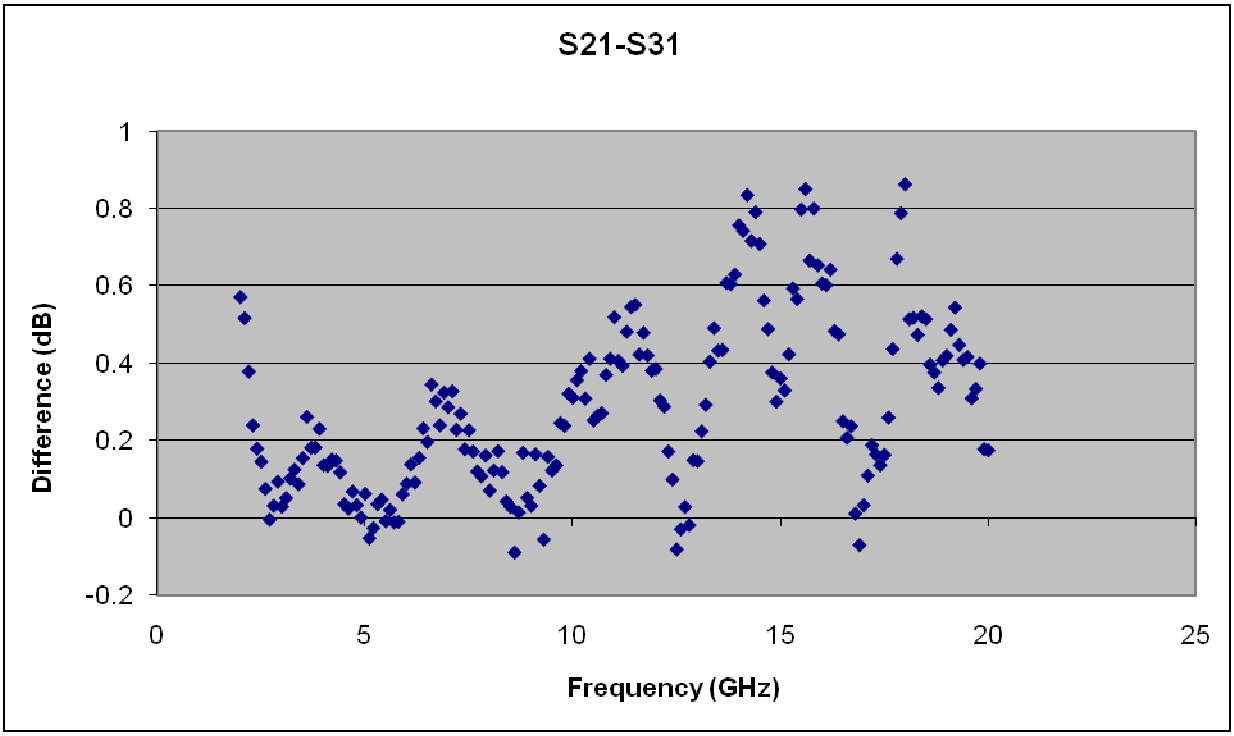


Figure 4-8: Error due to Difference between Normalized Coupler S-Parameters

4.2.2 Power Detector

Error is introduced into the subsystem by the power detector by approximating the relationship between input power and output voltage as linear and constant over frequency. In reality, the output voltage is not exactly linearly proportional to the input power, and the relationship varies slightly with frequency. In Section 3.5, the relationship between the input power and output

voltage for the power detector was described in detail and linearly approximated. Figure 4-9 shows a linear approximation for the frequency range 13 to 15 GHz. Using this approximation will give an error in estimated input power for a given output voltage. The difference between the input power estimated from the output voltage and the actual input power is shown in Figure 4-10. There are three distinct sections of errors; each section corresponds to a different frequency. This results due to shifts in the input power to output voltage relationship over frequency. The most positive set of errors occurs at 14 GHz, the most negative set of errors occurs at 13 GHz, and the smallest set of errors occurs at 15 GHz. Overall, the maximum positive error is 1.25 dB and the maximum negative error is -1.06 dB. This gives a total error range of 2.31 dB for this input power range.

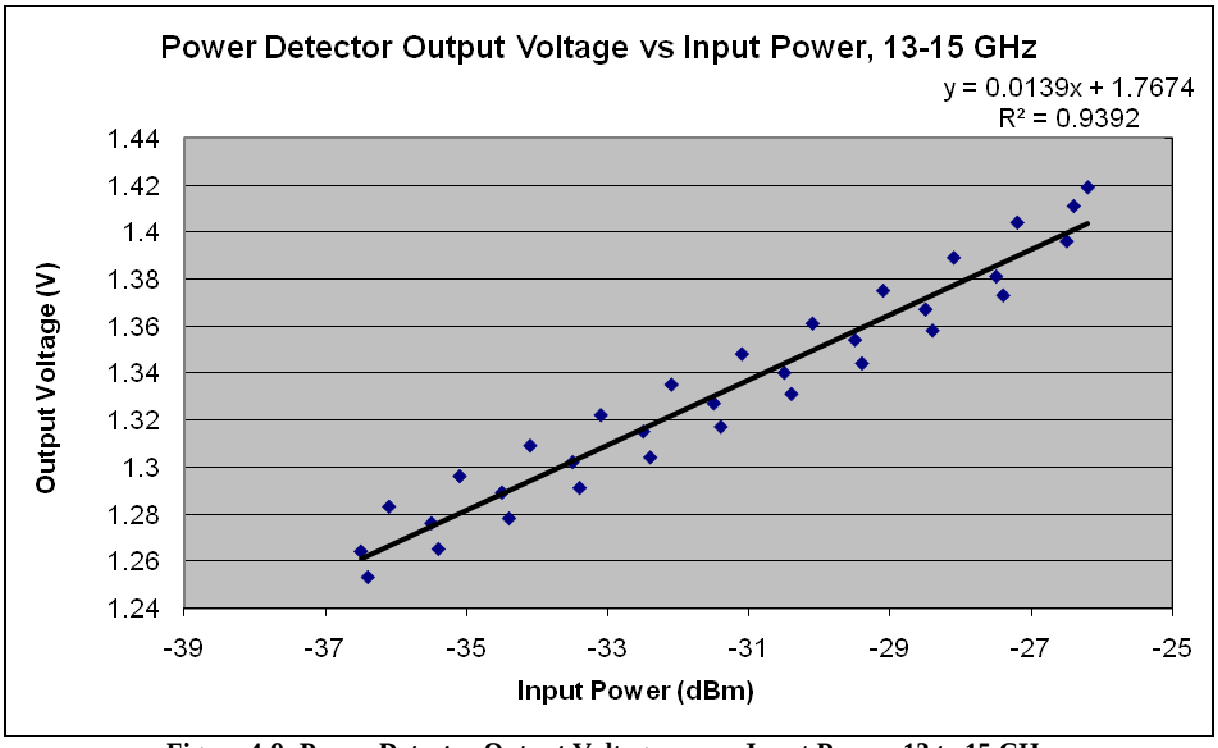


Figure 4-9: Power Detector Output Voltage versus Input Power, 13 to 15 GHz

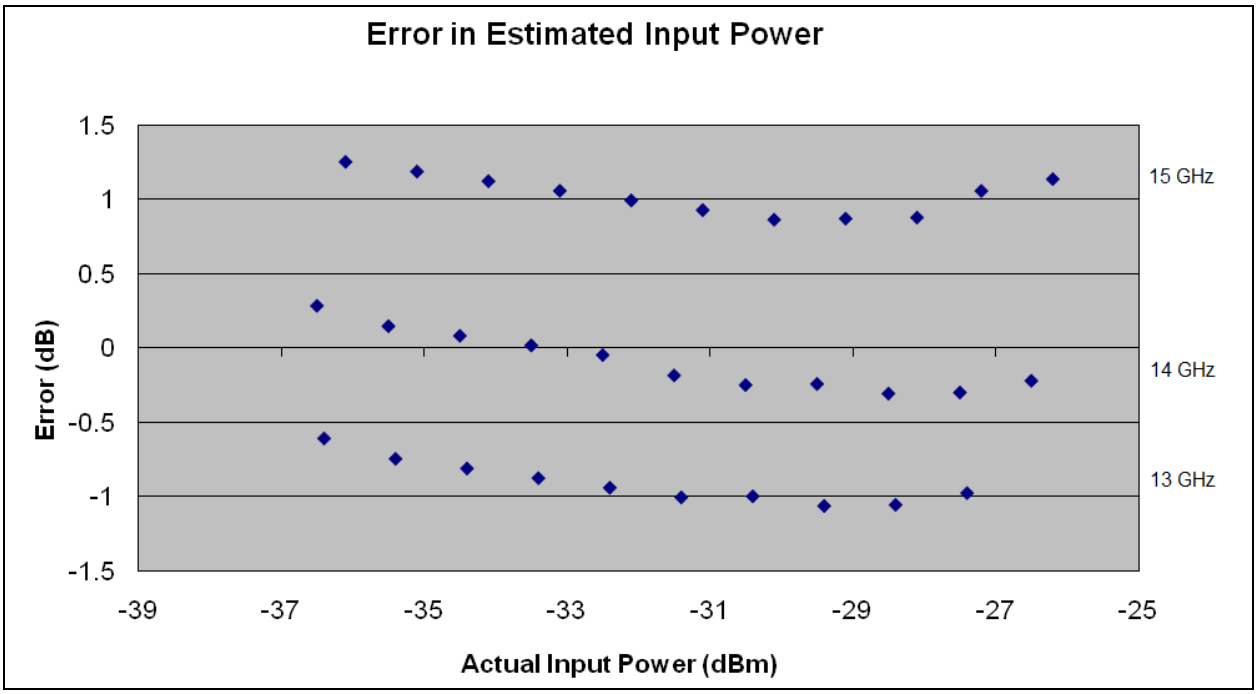


Figure 4-10: Difference between Estimated Input Power and Actual Input Power

4.2.3 Control Voltage

Error is introduced by approximating the control voltage to gain relationship of the power amplifier as linear and constant with frequency. This relationship varies with frequency and is not exactly linear. The relationship between control voltage and gain for the power amplifier was described in Section 3.2. Figure 4-11 shows a linear approximation of the relationship for the frequency range 13 to 15 GHz. These measurements were taken with an input power to the amplifier of 0 dBm. Using this approximation for a given control voltage input will give a gain value that differs from the ideal intended gain value; these errors are plotted in Figure 4-12. Again there are three distinct sections of errors; each section corresponds to a different frequency. This results because of shifts in the relationship over frequency. The most positive errors occur at 15 GHz, the most negative errors occur at 13 GHz, and the smallest set of errors occurs at 14 GHz. Overall, the maximum positive error is 1.10 dB and the maximum negative

error is -1.04 dB. This gives a total error range of 2.14 dB for control voltage range and input power.

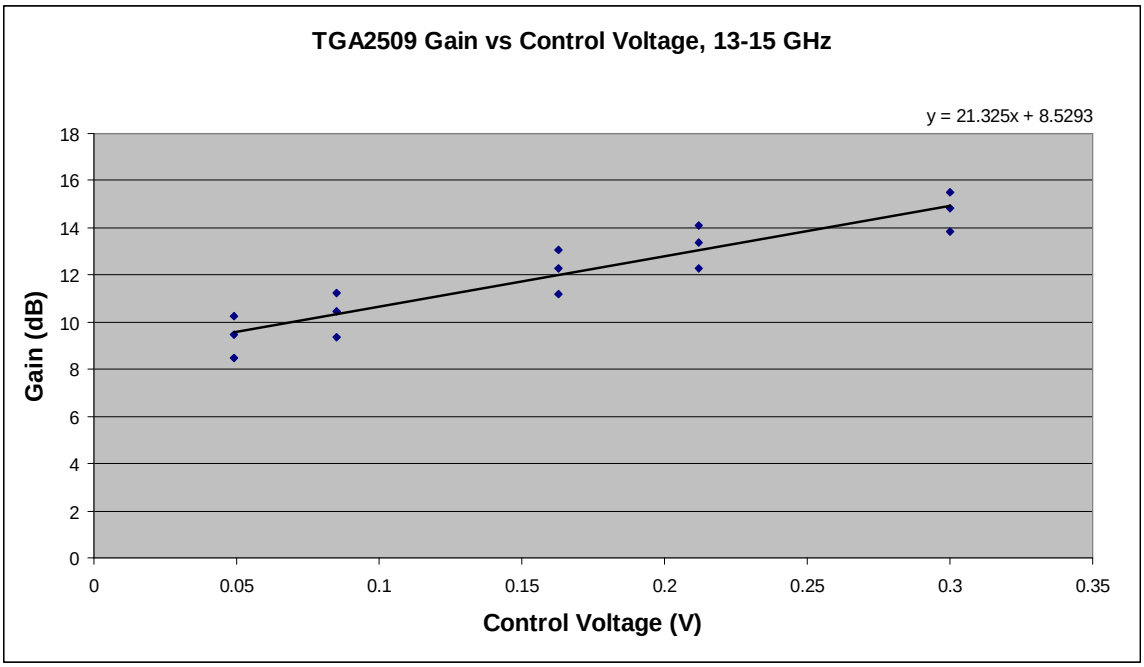


Figure 4-11: TGA2509 Gain versus Control Voltage, 13-15 GHz

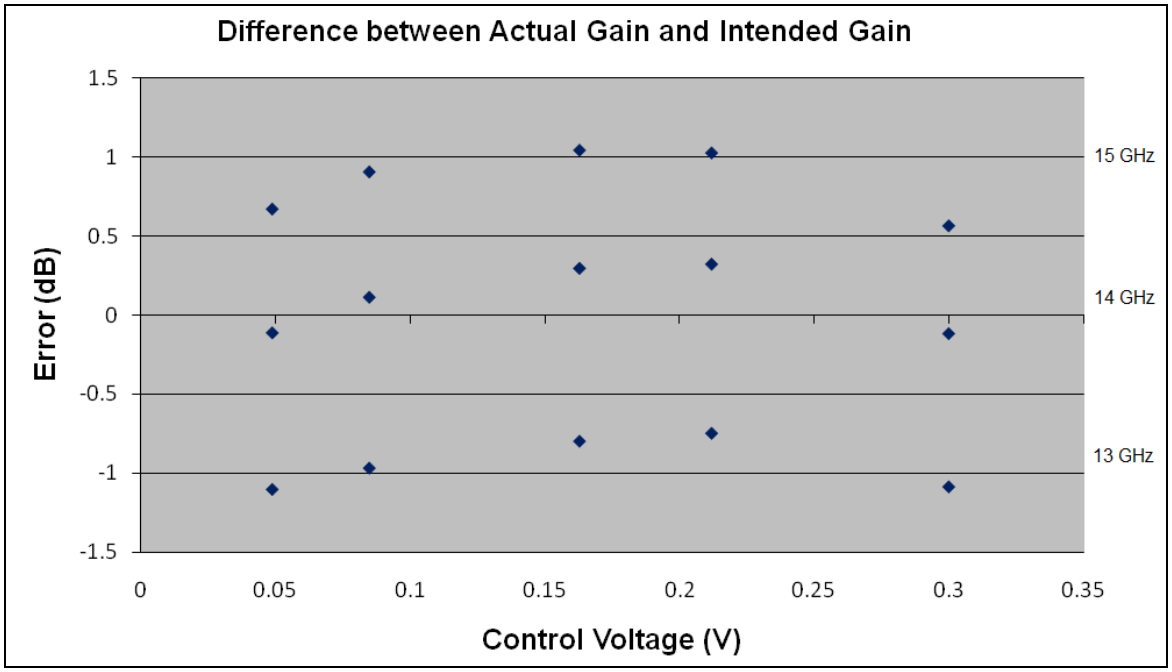


Figure 4-12: TGA2509 Difference between Actual Gain and Intended Gain

CHAPTER 5: OPEN-LOOP DESIGN AND RESULTS

5.1 Design Overview

An open-loop system can be implemented using much of the same design as the closed-loop system. In the closed-loop system, there are errors associated with the coupler, power detector, and control voltage linear approximation that can be removed by switching to an open-loop system. A block diagram of the open-loop system is shown in Figure 5-1. The coupler and power detector are no longer used, but the feedback scaling and voltage sequencing board is still needed in order to apply voltages to the TGA2509 amplifier in the correct order. Using this board also allows the control voltage to always be positive. The required control voltage into the feedback scaling and voltage sequencing board for a given output power is measured across frequency and stored to a device. In order to sync this control voltage with the RF signal, a trigger is needed

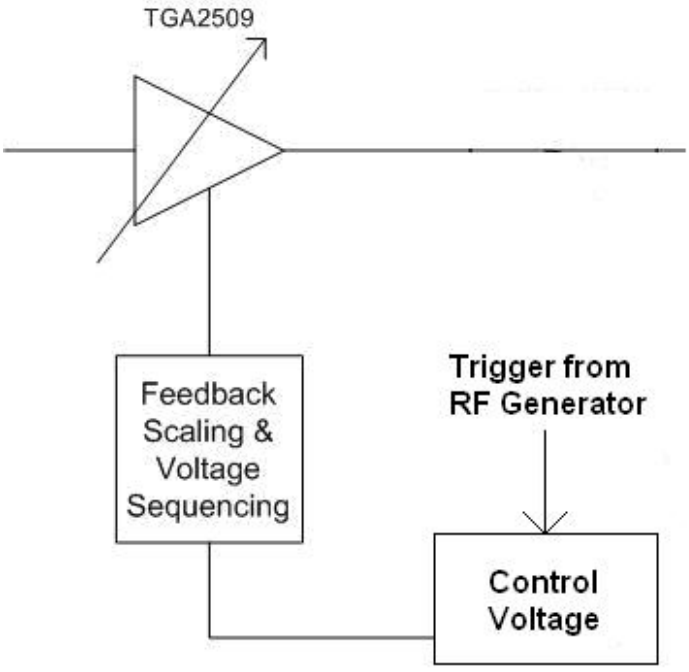


Figure 5-1: Open-loop Amplitude Control System

from the RF signal generator. This open-loop system provides more precise control than the closed-loop system and requires fewer components; however, it relies on measurements taken under certain conditions and is susceptible to temperature variation and change over time.

5.2 Measurements

Using the open-loop block diagram from Figure 5-1 and the same feedback scaling and voltage sequencing board as in the closed-loop system, measurements are taken for the required control voltage for a given input power. For each frequency point, the control voltage to the feedback scaling and voltage sequencing board is adjusted until the output power from the variable-gain amplifier is at a given level. These measurements are recorded in Table 5-1 for input power of 11 dBm and output power of 21 dBm. Input power is programmed on the synthesized sweeper and output power is read from the spectrum analyzer; however, losses through the cables total 5.5 dB. Output power of 21 dBm is chosen since it is the lowest maximum output power over frequency, occurring at 13.95 GHz, therefore output power at all other frequencies must be adjusted down to meet this level.

These control voltages can be stored to a device and input to the feedback scaling and voltage sequencing board in sync with the RF frequency sweep to level amplitude. Since the control voltages are measured directly, amplitude leveling is limited only by accuracy of the measurements and changes over time. There are no errors introduced by linear approximations of the power detector and amplifier control voltage or use of the coupler as in the closed-loop system.

Table 5-1: Control Voltage to Feedback Scaling and Voltage Sequencing Board for 21 dBm Output Power

Frequency (GHz)	Control Voltage for 21 dBm Output Power (V)	Control Voltage to VGA (V)
13	1.353	0.097
13.05	1.353	0.097
13.1	1.353	0.097
13.15	1.352	0.121
13.2	1.352	0.121
13.25	1.352	0.121
13.3	1.351	0.139
13.35	1.351	0.139
13.4	1.351	0.139
13.45	1.351	0.139
13.5	1.350	0.162
13.55	1.350	0.162
13.6	1.352	0.121
13.65	1.351	0.139
13.7	1.349	0.179
13.75	1.350	0.162
13.8	1.351	0.139
13.85	1.351	0.139
13.9	1.353	0.097
13.95	1.352	0.121
14.0	1.349	0.179
14.05	1.349	0.179
14.1	1.351	0.139
14.15	1.351	0.139
14.2	1.351	0.139
14.25	1.350	0.162
14.3	1.348	0.202
14.35	1.348	0.202
14.4	1.351	0.139
14.45	1.351	0.139
14.5	1.348	0.202
14.55	1.346	0.244
14.6	1.347	0.220
14.65	1.346	0.245
14.7	1.346	0.245
14.75	1.344	0.286
14.8	1.344	0.286
14.85	1.347	0.220
14.9	1.340	0.368
14.95	1.324	0.699
15.0	1.341	0.352

CHAPTER 6: CONCLUSION AND FUTURE WORK

6.1 Summary

An amplitude leveling subsystem for FM radar is needed in order to keep the transmit power of a chirped frequency signal constant over time. Radar components can have gains and attenuations that vary over frequency, causing there to be amplitude distortions in the transmit signal. These distortions degrade range sidelobe performance. The amplitude leveling system must correct for these amplitude distortions over a wide bandwidth to accommodate wideband radars.

A closed-loop amplitude leveling subsystem for FM radar was successfully designed, built, and tested. This closed-loop system is implemented using all analog components, including a variable-gain amplifier, coupler, power detector, and a board to control voltage sequencing and feedback scaling. A small portion of the transmit power is coupled off by the coupler and detected by the power detector. The voltage output of the power detector is scaled and fed back to the variable-gain amplifier to control the gain of the transmit signal. Because this closed-loop system operates with all analog components, corrections are made in real time.

When the transmit power of the system is tested without the closed-loop amplitude leveling subsystem, variation in amplitude is ±1.21 dB from a linear decrease in power. The difference between absolute minimum and maximum is 3.33 dB. With the closed-loop amplitude leveling system, variation in amplitude is ±0.72 dB from a linear decrease in power. The difference between absolute minimum and maximum is 1.88 dB. This is an improvement of ±0.49 dB in amplitude variation from a linear decrease in power and an improvement of 1.45 dB in difference

between absolute minimum maximum. Variation in amplitude with the closed-loop system is less than ±1 dB.

Measurements were also taken for the implementation of an open-loop system. This system does not use the coupler or power detector but does require a digitally controlled voltage. The control voltage is input to the voltage sequencing and feedback scaling board and scaled to use as the control voltage for the variable-gain amplifier. In order to determine the needed voltage from the digital device, measurements were taken over the desired frequency range. Voltage was varied until the output power of the amplifier was a given level. In order to implement the open-loop system the measured control voltages would need to be programmed to a device in sync with the transmit chirp.

6.2 Comparison

The closed-loop amplitude leveling subsystem makes corrections in real time and is therefore able to correct over changes in temperature as well as system changes. This subsystem does not need to be changed if components are added to or removed from the transmit line. However, because the variable-gain amplifier must be operated in its linear region, the gain of the power amplifier must be decreased. There is also additional power loss due to the coupler insertion loss. There are many sources of error in this system that keep it from ideally leveling amplitude.

The open-loop amplitude leveling subsystem has the advantage of programmable control voltage. The control voltage can be adjusted and tuned so that the transmit power is level across frequency. It uses fewer components since the coupler and power detector are no longer needed,

and power does not have to be backed down to operate in the linear region of control voltage versus amplifier gain. Also, since the coupler is not used, there is not added insertion loss in the transmit line. However, the open-loop system is very susceptible to change over time and temperature. Without any automatic calibration, new measurements of control voltage must be taken every time a component is added to or removed from the transmitter that need to be corrected for. The digital control voltage must then be carefully synced with the frequency chirp so that control voltage lines up properly with frequency.

The closed-loop system offers real time corrections with a greater number of components and many sources of error. The open-loop system offers more direct control and tuning of the control voltage and could also be used for windowing. However, it does not correct in real time and is susceptible to changes over time and temperature.

6.3 Recommended Future Work

In order to improve the closed-loop system, voltage sequencing could be implemented with timed digital controls if available. The feedback scaling could be done using a microcontroller programmed with the specific transfer functions of the power detector and variable-gain amplifier over frequency. This would eliminate errors due to linear approximations of these devices. This could be done as long as the delay through the controller was small enough to make real time corrections. The closed-loop system could be expanded to correct for reflections from the antenna using two power detectors and a bidirectional coupler.

The open-loop system voltage sequencing could also be implemented with timed digital controls. The voltage sequencing and feedback scaling board would then no longer be needed, and programmed control voltages could be input directly to the variable-gain amplifier. This improved system would require the least amount of components but the greatest amount of digital control. The open-loop system could also be expanded to incorporate windowing, and a system to automatically calibrate the control voltage could be created with feedback from the output.

References

[1] Intergovernmental Panel on Climate Change (IPCC). “Climate Change 2007: Synthesis Report.” Valencia, Spain, November 12-17, 2007.

[2] Kanagaratnam, Pannirselvam. “High-Resolution Radar Backscatter from Sea Ice and Range-Gated Step-Frequency Radar using the FM-CW Concept.” M.S. Thesis, University of Kansas, 1993.

[3] Willyard, Rick. “Airborne Radar for Measuring Snow Thickness over Sea Ice.” M.S. Thesis, University of Kansas, 2004.

[4] “TGA2509-FL Wideband 1 W HPA with AGC.” TriQuint Semiconductor. May 15, 2009.

[5] TriQuint Evaluation Board Information provided by Richard Curtis. January 15, 2009.

[6] “RFDC2G18G30 Ultra Wide Band 50 W Directional Coupler, 2-18 GHz.” RF-Lambda.

[7] “HMC613LC4B Successive Detection Log Video Amplifier (SDLVA), 0.1-20 GHz.” Hittite Microwave Corporation.

[8] TriQuint Base Plate Information provided by Richard Curtis. January 15, 2009.

APPENDIX A: TGA2509 CONSTRUCTION INFORMATION

Construction of the TriQuint TGA2509 amplifier unit is based off of the TGA2509 evaluation board from TriQuint and information provided from TriQuint engineers. The circuit board for the amplifier is laid out in Altium Designer 6.8 with pad dimensions based on board drawings provided by TriQuint. The layout is shown in Figure A-1 with purple representing pads, red representing traces, blue representing the bottom ground plane, and pink representing the mechanical layer. Two of these boards are required for each amplifier. Connectors screw into the holes on the top of the figure, and amplifier pins solder to the pads at the bottom center of the figure. Components are placed on the boards according to Figure A-2; although the layout shown in this figure is not identical to Figure A-1, pads exist for all components. Surface mount header pins are used for Vg1, Vg2, Vd, and Vc connectors with 33 uF capacitors on the Vg1, Vg2, and Vd inputs.

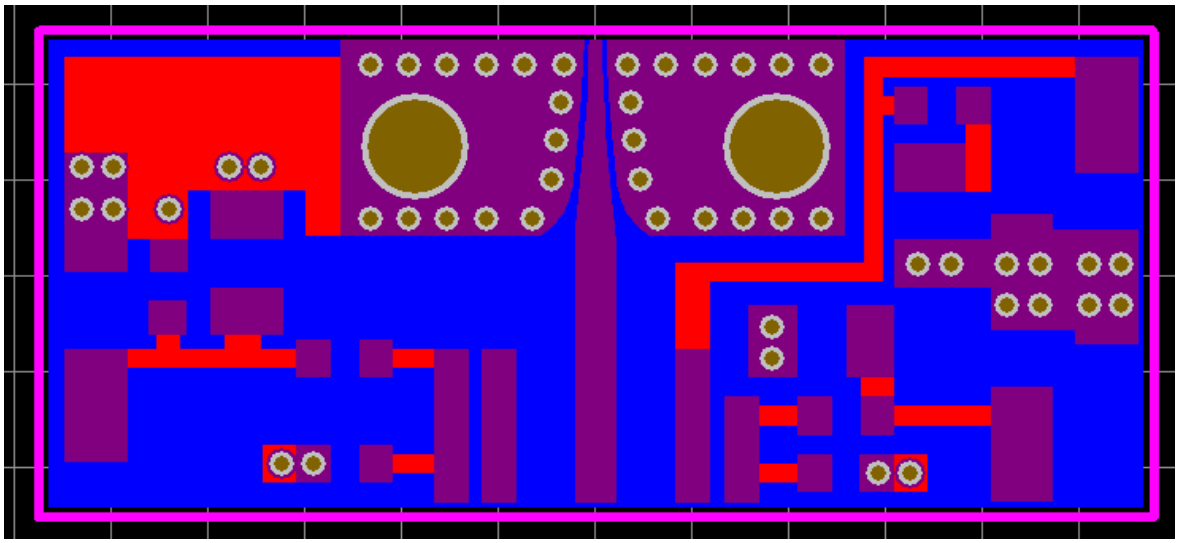
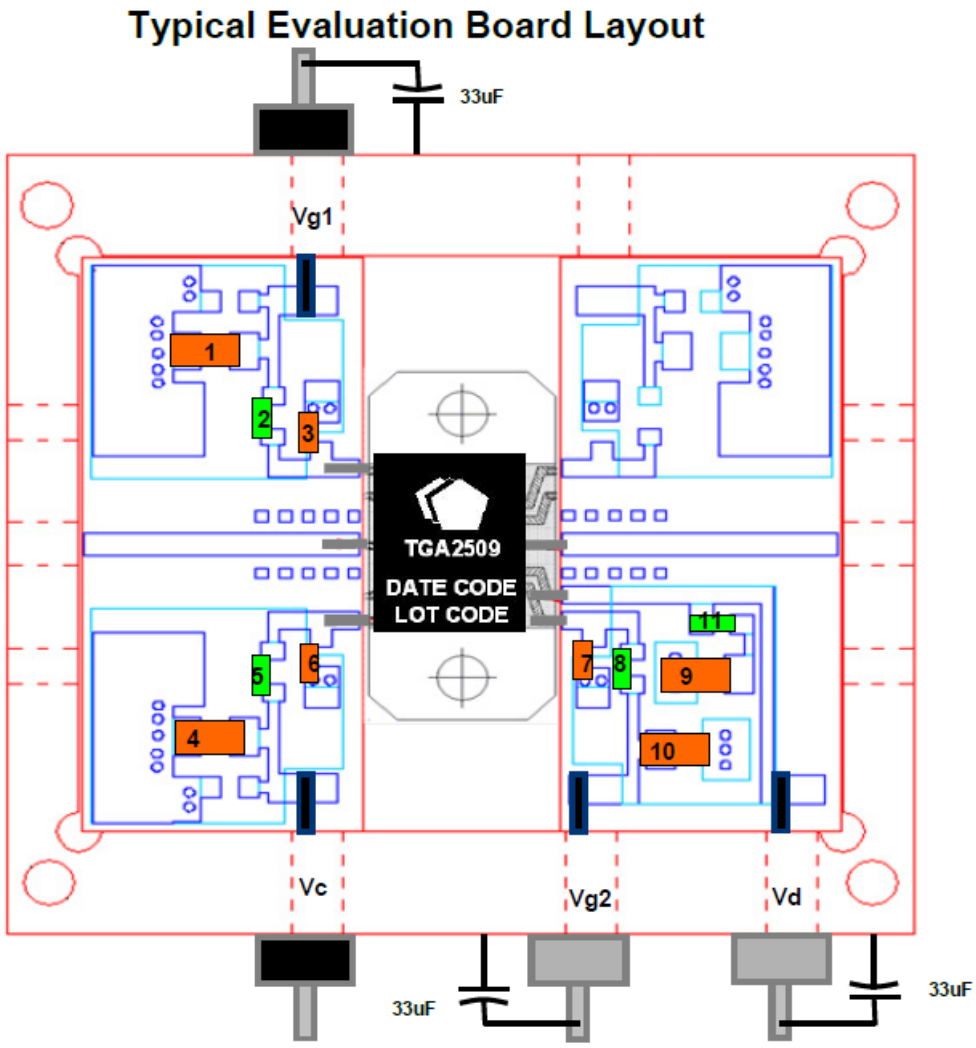


Figure A-1: Printed Circuit Board Layout for TGA2509



COMPONENT	VALUE
1, 4, 9,10	1 uF
2, 5, 9	10 Ω
3, 6, 7	0.01 uF
11	100 Ω

Figure A-2: Typical Evaluation Board Layout [4]

The RF connectors used are Southwest Microwave Super SMA end launch connectors with 5 mil pins. The drawing provided by TriQuint for the amplifier base plate is shown in Figure A-3, and the heat sinks used are Vantec FCE-6040Y heat sinks. The silver epoxy used in construction of the amplifier unit is Tiga Silver 920H.

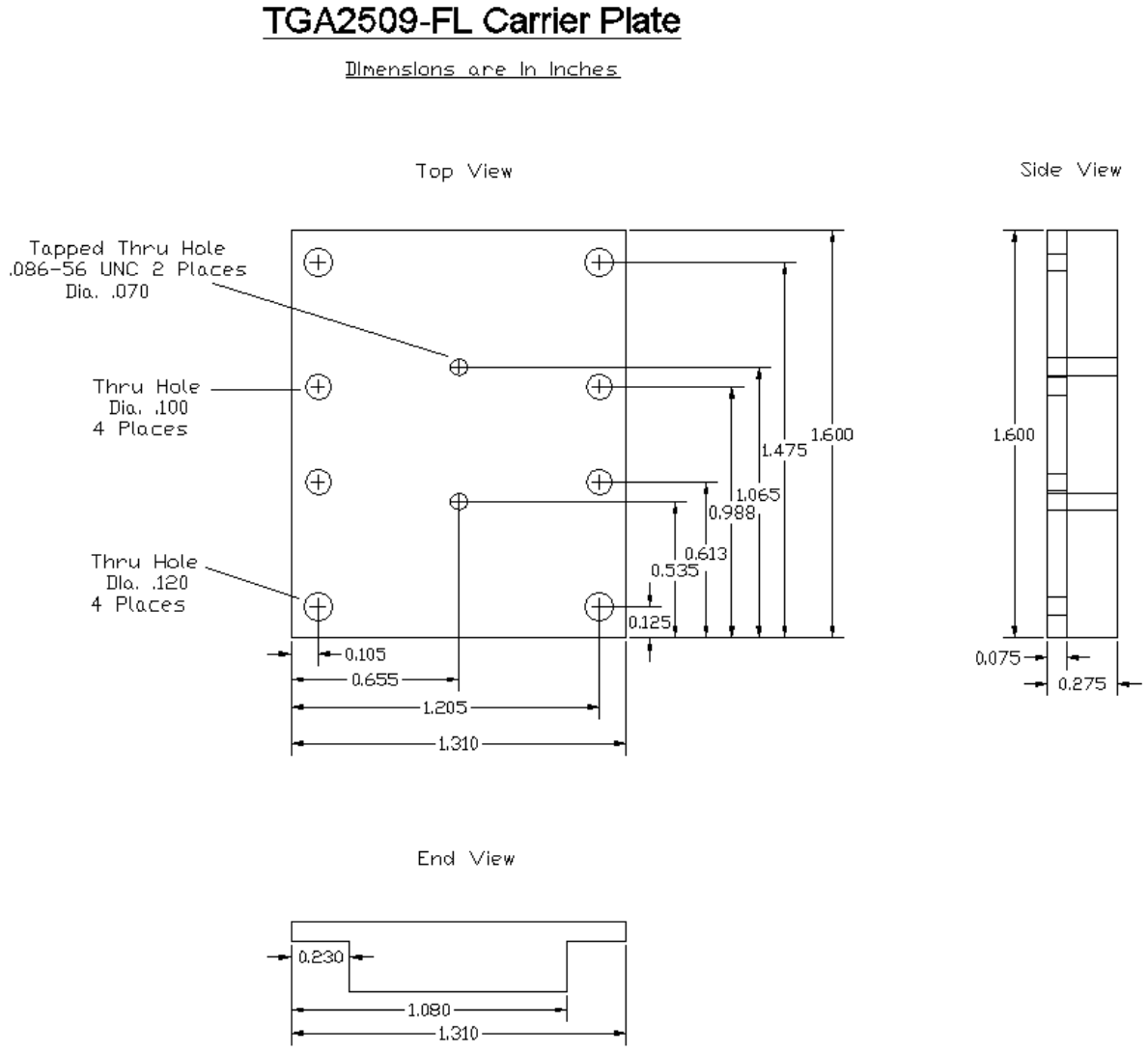


Figure A-3: TGA2509 Base Plate Drawing [8]

The following steps are taken to construct a completed amplifier:

1) Solder resistors, capacitors, and testpoints to amplifier printed circuit boards
2) Apply heat sink paste to the back of a TGA2509 amplifier and attach it to the base plate using two lock washers and two 2-56 1/8 inch screws
3) Apply silver epoxy to bottoms of printed circuit boards and solder all pins of the mounted TGA2509 amplifier to the boards
4) Attach Southwest Microwave connectors, centering the connector center pins on the traces
5) Apply heat sink paste to the back of the base plate and attach it to the large heatsink using four lock washers and four 4-40 1/2 inch screws
6) Add labels for Vg1, Vg2, Vd, and Vc
7) Solder 33 uF electrolytic capacitors to Vg1, Vg2, and Vd input pins
8) Solder twisted wire to input pins and cover connections with heat shrink

APPENDIX B: SCHEMATICS AND BOARD LAYOUTS

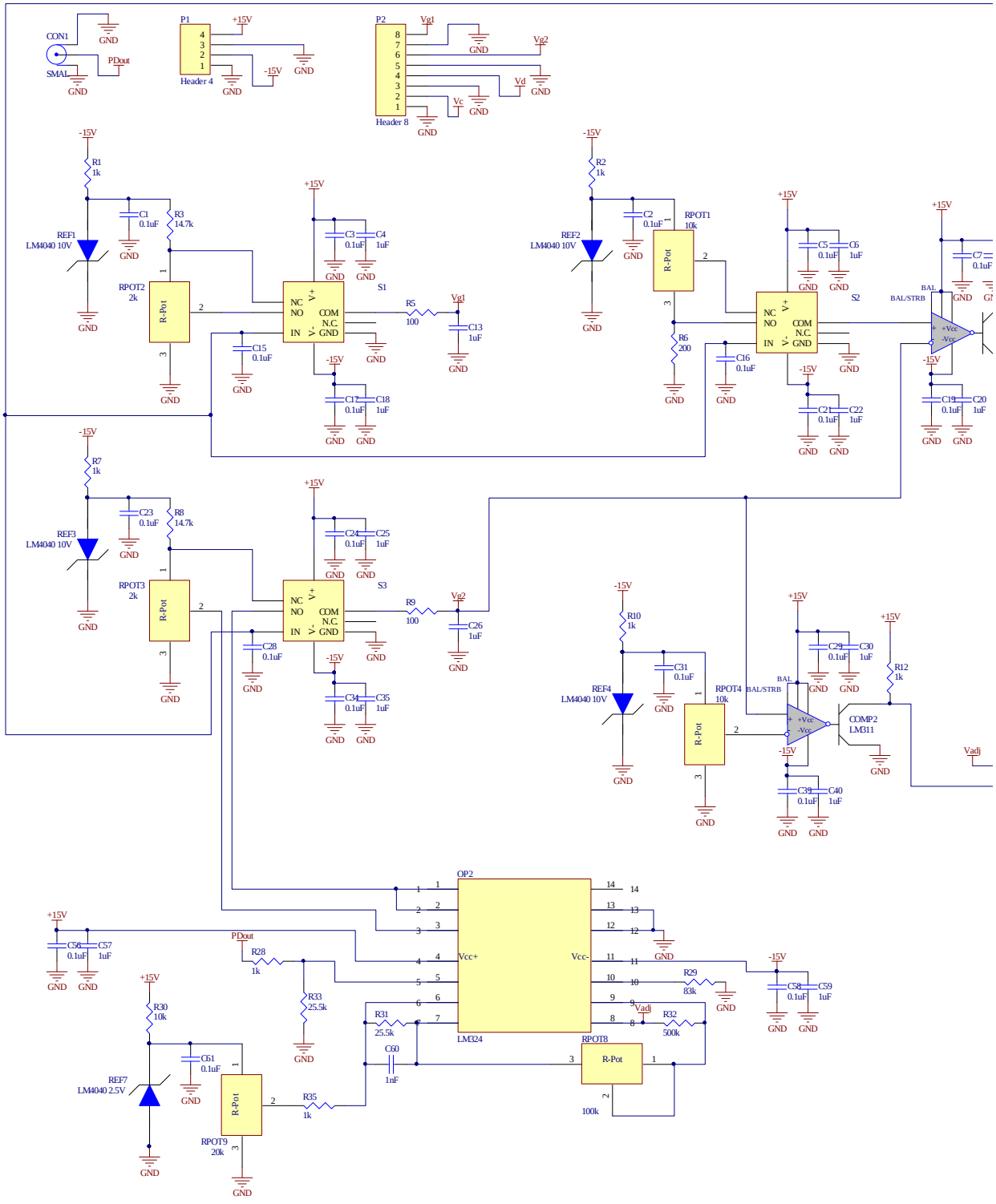


Figure B-1: Feedback Scaling and Voltage Sequencing Schematic, Side 1

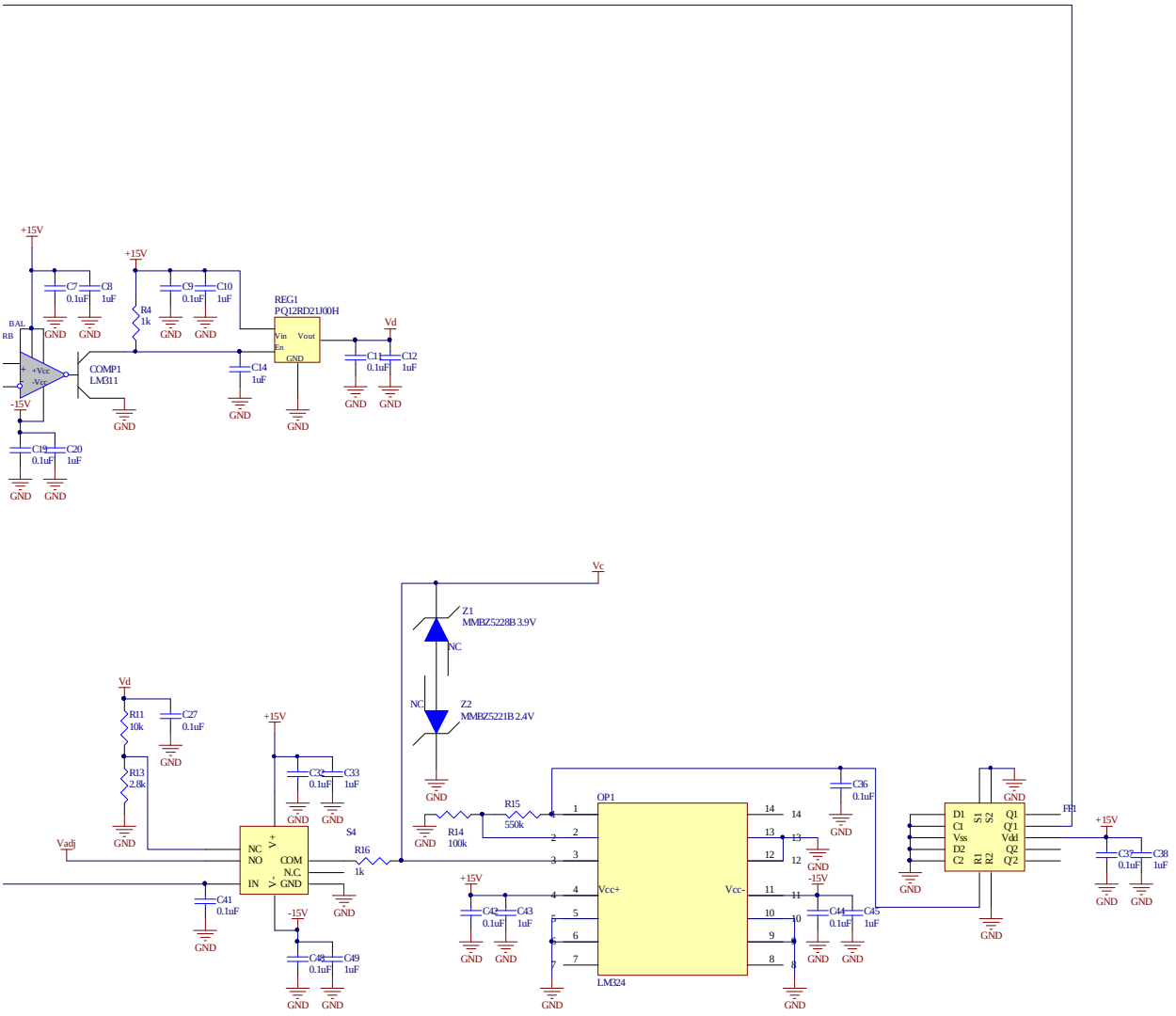


Figure B-2: Feedback Scaling and Voltage Sequencing Schematic, Side 2

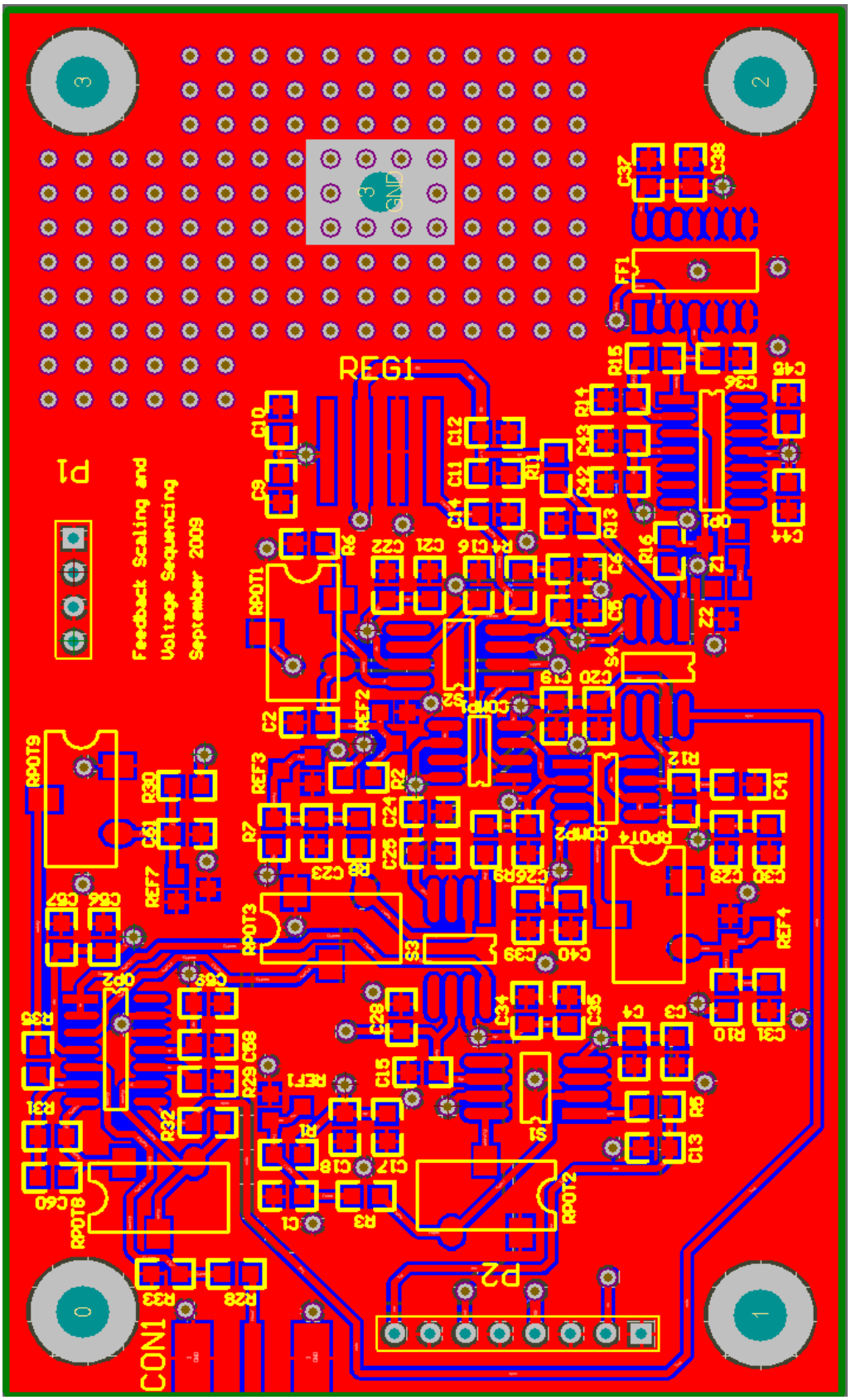


Figure B-3: Feedback Scaling and Voltage Sequencing Board Layout, Top Layer

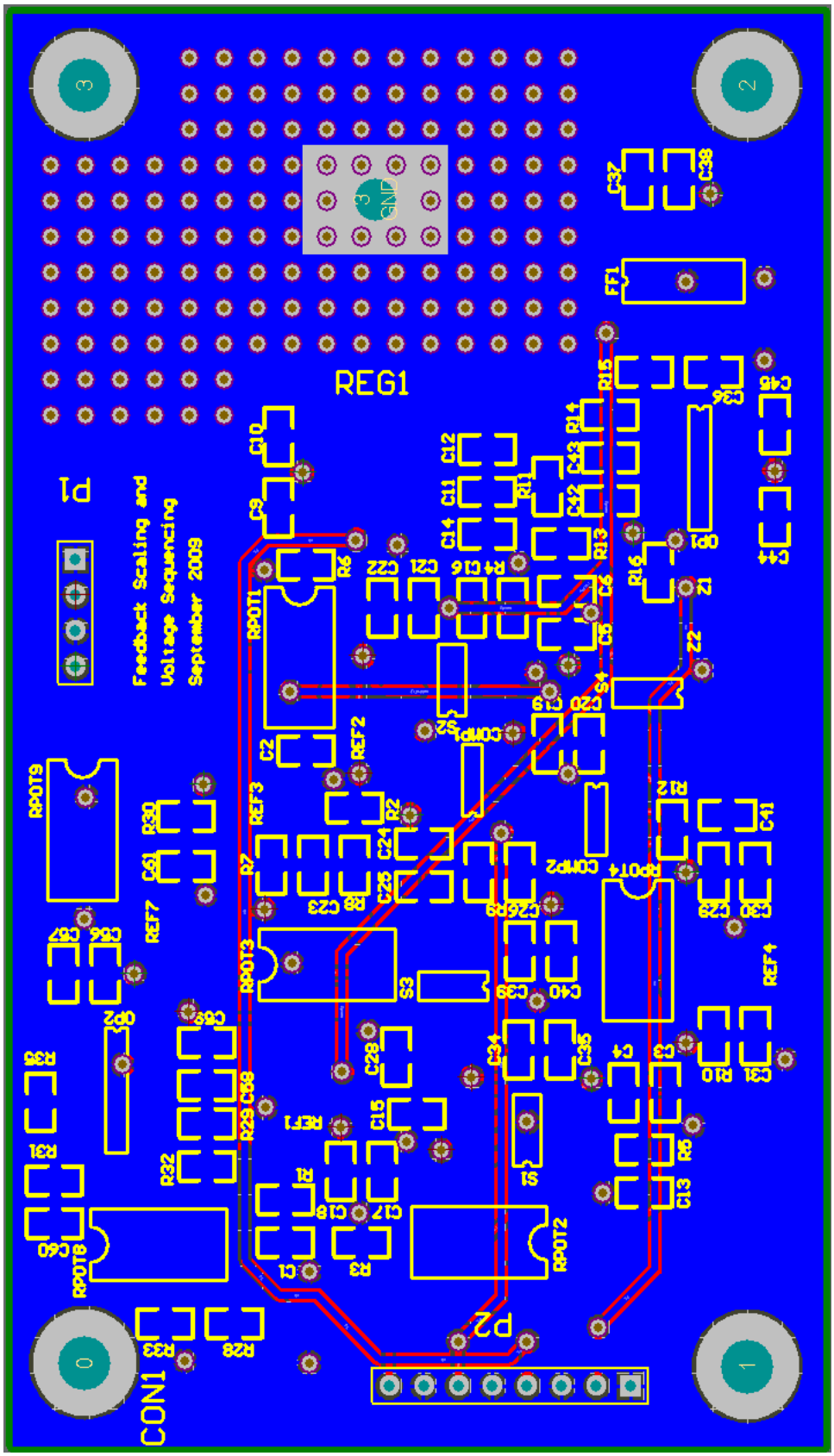


Figure B-4: Feedback Scaling and Voltage Sequencing Board Layout, Bottom Layer

Table B-1: Bill of Materials for Feedback Scaling and Voltage Sequencing Board

Designator	Component	Manufacturer	Part Number
COMP1, COMP2	Comparator	Texas Instruments	LM311D
FF1	Flip-Flop	ON Semiconductor	MC14013BDR2G
OP1, OP2	Quad Op Amp	STMicroelectronics	LM324DT
REF1, REF2, REF3, REF4	10V Reference	National Semiconductor	LM4040CIM3X-10
REF7	2.5V Reference	National Semiconductor	LM4040CIM3-2.5
REG1	LDO 12V Regulator	Sharp Microelectronics	PQ12RD21J00H
RPOT1, RPOT4	10k Potentiometer	Copal Electronics Inc	ST5ETW103
RPOT2, RPOT3	2k Potentiometer	Copal Electronics Inc	ST5ETW202
RPOT8	100k Potentiometer	Copal Electronics Inc	ST5ETW104
RPOT9	20k Potentiometer	Copal Electronics Inc	ST5ETW203
S1, S2, S3, S4	CMOS Analog Switch	Maxim	MAX4659ESA+
Z1	3.9V Zener Diode	Diodes Inc	MMBZ5228B-7-F
Z2	2.4V Zener Diode	Diodes Inc	MMBZ5221B-7-F

All resistors and capacitors use a 0805 footprint and the values shown in the schematic.

APPENDIX C: MATLAB CODE

MATLAB Code for Section 2.2 Simulations:

```
%Heather Owen
%Distortion Examples

clear;
clc;
% close all;

dt=1e-11;
t=0:dt:240e-6;

%rect
%A1=1;
%ripple
%A1=1+0.3*sin(2*pi*100e3.*t);
%linear
A1=1000-700/(240e-6).*t;
delay1=1e-5;
f1=13e9;
f2=15e9;
tau=240e-6;
k=(f2-f1)./tau;

%waveforms
s1=A1.*sin(2.*pi.*(f1.*t+k./2.*t.^2));
s1z=[zeros(1,1000) s1 zeros(1,1000)];

%ffts
Nfft=2^25;
S1Z=20*log10(abs(fft(s1z,Nfft)));
S1Z=S1Z-max(S1Z);
f=1/dt*(0:Nfft/2)/Nfft;

%plots
figure(1);
plot(f*1e-9,S1Z(1:1+Nfft/2))
xlabel('Frequency (GHz)');
ylabel('Normalized Chirp Spectrum (dB)')
axis([12 16 -20 0]);

%processing
s1_delay=A1.*sin(2.*pi.*(f1.*(t-delay1)+k./2.*(t-delay1).^2));
```

```
s1z_delay=[zeros(1,1000) s1_delay zeros(1,1000)];
fbeat1=s1z.*s1z_delay;
Nfft=2^25;
FBEAT1=20*log10(abs(fft(fbeat1,Nfft)));
FBEAT1=FBEAT1-max(FBEAT1);
f1d=1/dt*(0:Nfft/2)/Nfft;

figure(2);
plot(f1d*1e-6,FBEAT1(1:1+Nfft/2),'b')
xlabel('Frequency (MHz)');
ylabel('Normalized Beat Frequency Spectrum (dB)')
axis([10 200 -100 0]);
hold off;

figure(3);
plot(f1d*1e-6,FBEAT1(1:1+Nfft/2),'b')
xlabel('Frequency (MHz)');
ylabel('Normalized Beat Frequency Spectrum (dB)')
axis([83 83.7 -50 0]);
hold off;
```