Signal Generation for FMCW Ultra-Wideband Radar

By

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Submitted to the graduate degree program in Electrical Engineering and Computer Science and the Graduate Faculty of the University of Kansas School of Engineering in partial fulfillment of the requirements for the degree of Master of Science.

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Date of Defense: 20th January, 2009

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ACKNOWLEDGEMENTS

I would like to thank my advisor Dr. Carlton Leuschen for his guidance and expert advice that helped me successfully complete my thesis and my masters. I would like to thank Dr. Prasad Gogineni for giving me an opportunity to be a part of the CReSIS project and guiding me all throughout my research. I would like to thank Dr. Chris Allen for his helpful guidance and inputs during the weekly meetings.

I would like to extend my sincere thanks to Dr. Fernando Rodriguez-Morales for guiding me and being there to help me whenever I needed any. I would like to thank John Ledford for helping me and answering my questions. I would like to extend special thanks Dr. Sarah Seguin for giving me the support I needed.

Finally I would like to thank my husband for being very supportive. I also would like to thank my parents, my brother and my sister for their support and encouragement. I thank all my friends at CReSIS and KU for making my masters studies an enjoyable experience.

ABSTRACT

One of the greatest concerns facing the planet earth today is global warming. Globally the temperatures have risen and this has caused rise in sea level. Since a large percentage of the population lives near the coast sea level rise could have potentially catastrophic consequences. One of the largest uncertainties in projections of sea level rise is the changes of mass-balance of the ice sheets of Greenland and Antarctica. To predict the rise in sea level we need accurate measurements of mass-balance. One of the methods of determining mass-balance is through surface ice elevation measurements. In order to measure surface ice elevation, map near surface internal layers and measure the thickness of snow over sea ice Ultra-Wideband (UWB) Frequency-Modulated Continuous-Wave Radars are being developed at CReSIS. FMCW radars are low-cost low-power solution to obtain very fine range resolution. However, nonlinearities present in the transmit frequency sweep of the FMCW radar can deteriorate the range resolution. The main objective of the thesis was to produce an ultra linear transmit chirp signal for UWB Radars. This was done by using the Voltage-Controlled-Oscillator (VCO) in a Phase-Locked Loop configuration. To check the linearity of the chirp beat frequency was generated using delay line as a synthetic target and captured on the oscilloscope. This beat signal data were further analyzed for linearity and we found that the frequency response of the beat signal was a focused Sinc wave as opposed to a smeared signal in case of nonlinear chirp. Also the phase of the beat signal data was linear with respect to time.

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CHAPTER 1: INTRODUCTION

1.1 Motivation

One of the greatest concerns facing the planet earth today is global warming. Recent reports from the Intergovernmental Panel on Climate Change (IPCC) concluded that the increase in globally averaged temperatures since the mid-20th century is most likely due to the observed increase in anthropogenic greenhouse gas concentrations [1]. Greenhouse gases absorb the thermal infrared radiation, emitted by the earth's surface, by the atmosphere and by clouds. Thus, the greenhouse gases trap heat within the surface-troposphere system that results in thermal expansion of water on the surface of earth and melting of polar ice sheets and glaciers, which in turn leads to rise in sea level.

Globally the sea level has risen at a rate between 0.3 to 0.8 feet per 100 years during the last few centuries. The Environmental Protection Agency (EPA) has estimated that the most probable global sea level rise for the year 2050 will be 0.5 feet greater than the 1995 level and for the year 2100 it will be 1.1 feet greater than 1995 level. This estimate only includes greenhouse warming and other factors are not included [1]. The estimated sea level rise could have devastating consequence on coastal population. Hundreds of millions of people living in coastal areas in many countries are likely to be displaced by sea level rise within this century, and accompanying economic and ecological damage will be severe for many others [2].

Eleven of the world's 15 largest cities lie along the coast. In the United States, around 53% of the population lives near the coast. Analysis of the spatial distribution of population with respect to topography reveals that the number of people and population density diminishes rapidly with increasing elevation and increasing distance from the shoreline. Approximately 400 million people live within 20 m of sea level and within 20 km of a coast, worldwide [3]. Thus, sea level rise can have potentially catastrophic consequences.

1.2 Reason behind studying ice sheets

Melting of small glaciers and polar ice caps is expected to give the second-largest contribution to sea level rise in this century after thermal expansion of water [4]. Although small glaciers make up only 4% of the total land ice area, they may have contributed up to 30% of the sea level rise this past century because of rapid ice volume reduction due to global warming [5]. Also it is estimated that if the entire Greenland ice sheet were to melt, sea levels would rise by about 7 meters (23 feet) [6]. Such an occurrence would submerge coastal cities and displace a large percentage of coastal population.

One of the largest uncertainties in projections of sea level rise is the changes of mass-balance of the ice sheets of Greenland and Antarctica [4]. Ice sheet mass balance is defined as the sum of surface mass balance, mostly solid precipitation and melting leading to runoff and ice discharge into ice shelves and icebergs. Most of the ice discharge occurs through fast flowing ice streams and outlet glaciers, which are a small fraction of the ice sheets, where the velocities reach as high as a km per year.

The flow in the ice streams is rapid because of sliding, due to readily deformable sediment and lubrication by the melting water at the ice bed. During recent years accelerated flow has been observed in some Amundsea Sea ice streams and many Greenland outlet glaciers, leading to increased discharge and positive sea level rise contributions from both the ice sheets. This observed acceleration in flow of ice streams and glaciers gives rise to large uncertainties in projections. This is because there is presently only limited understanding of the controls on ice-stream flow. In order to address this problem, we need models of ice-stream flow to be developed that consider grounding-line migration, the buttressing effect of ice-shelves, and the lubrication of the bed by surface melt-water. Also we need models of ice-shelf surface mass balance and the way in which surface melting may cause disintegration of ice shelves [4]. To construct these models the researchers and scientists require ice-sheet data that give information about ice sheet thickness, basal conditions and accumulation rates.

Center for Remote Sensing of Ice Sheets (CReSIS) at the University of Kansas was established in 2005 by National Science foundation with the mission for developing new technologies and computer models to measure and predict the response of sea level change due to the melt and disintegration of ice sheets in Greenland and Antarctica [7]. Several advanced Radar systems are built at KU that provide accurate ice sheet thickness, map internal layers, image the bedrock etc. The data from measurements on the polar ice sheets are distributed to the scientific community.

The Ultra-Wide Band (UWB) Frequency-Modulated Continuous-Wave (FM-CW), radars with resolution of about 5 cm are being developed at CReSIS. . These radars will be used for high-precision measurements of surface-elevation, fine-resolution mapping of near-surface layers and measurement of thickness of snow over sea ice. In this thesis, a transmit waveform generator for these radar is designed and developed. It operates over the frequencies 8-12.5 GHz and 12-18 GHz. The waveform generator output can be mixed up/down to generate the transmit chirp for required applications and be used in C-, X- or Ku-band radars.

1.3 Objectives and Approach

FM-CW radars operating in upper microwave bands can provide low cost and low power solutions for many applications requiring the fine resolution for separating targets separated by a few cms in range. The bandwidth of the radar must be of the order of a few of gigahertz to obtain range resolution of a few cms and the transmit chirp must be highly linear with respect to time over the desired bandwidth [8]. This is because nonlinearities present in the transmit signal can result in non-focused beat frequency signal that degrades range resolution.

The main objective of the thesis is to produce a transmit chirp signal for UWB radars. To produce an ultra-linear chirp a Voltage-Controlled-Oscillator (VCO) in a fast-settling Phase-Locked Loop (PLL) configuration is used. The oscillator generates an 8-12.5 GHz chirp in response to an error voltage sweep of 0-10 volts generated by the loop filter of the fast-settling PLL. The PLL is driven by an extremely linear DDS sweep.

To check for the linearity of the frequency sweep with respect to time, the chirp generated by the PLL is delayed by passing it through a fiber-optic delay line of sufficient length. The non-delayed version of chirp is mixed with the delayed-version to produce a beat-frequency signal. The beat-frequency signal is low-pass filtered and digitized. The digitized beat frequency signal is saved and analyzed to see if the beat signal frequency response can be described by Sinc function. Test is also carried out to resolve multiple targets by using the delay line set up. .

1.4 Thesis Organization

The thesis is divided into five chapters. Chapter two presents the theory and background of an FM-CW Radar. It also discusses how the non-linearity in the transmit waveform translates into a nonlinear beat frequency signal. Chapter three discusses the basics of a PLL. It also provides a discussion on the design evolution of the PLL that generated linear chirp for FM-CW radars and its simulation using Advanced Design systems (ADS). Chapter four discusses the Implementation of the PLL in the lab. It presents the tests carried out to check for the linearity of the chirp signal and how accurately it resolves multiple targets. It also discusses the PCB design for the PLL. Finally, Chapter five presents conclusions and recommendations for future work.

CHAPTER 2: THEORY AND BACKGROUND

2.1 Introduction

FM-CW radar system transmits a continuous wave signal that is frequency modulated over a certain bandwidth. The signal modulation can be triangular, saw-tooth or sine. The bandwidth of this signal determines the range resolution. The larger the bandwidth the higher is the range resolution. Since for our application we are interested in mapping the near-surface layers with high resolution we require a very large bandwidth.

2.2 Principles of FMCW Radar

In a FM-CW radar the transmit waveform is a frequency-modulated continuous-wave given by the equation

$$S_{Tx}(t) = A\cos\left(2\pi f_o t + \pi k t^2\right) \dots\dots\dots\dots\dots\dots\dots\dots \text{(2.1)}$$

Where A is the amplitude of the transmit signal, f_o is the start frequency and k is the chirp rate.
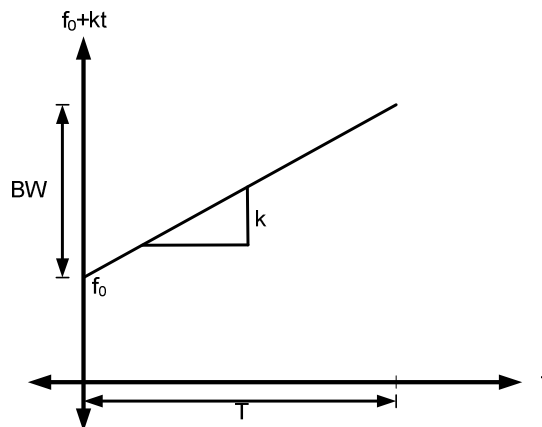

Figure 2.1 - FMCW Radar Sweep

As shown in Figure 2.1 the frequency of the transmit signal linearly increases with time at a constant rate called chirp rate.

Chirp rate can be defined as

$$k = \frac{BW}{T} \quad \text{.....................} \quad (2.2)$$

Where the bandwidth BW is the difference between the start and stop frequencies. T is the pulse width or the time taken for the waveform to cover the given frequency range.

The instantaneous frequency of the above transmit signal can calculated by taking the derivative of the instantaneous phase

$$f_{Inst} = \frac{1}{2\pi}\frac{d\phi}{dt} = \frac{1}{2\pi}\left(2\pi f_o + 2\pi k t\right) = f_o + kt \quad \text{................} \quad (2.3)$$

Also the maximum frequency of the transmit signal is given by

$$f_{Max} = f_o + kT \quad \text{..........................} \quad (2.4)$$

Equations for single target:

Once the transmit signal is radiated it propagates through the medium and hits the target and the target reflects a part of signal back to the radar. The received signal is an attenuated version of the transmit signal that is delayed by a time t_o. The received signal in time domain can be expressed as

$$S_{Rx}(t) = \cos\left(2\pi f_o(t - t_o) + \pi k(t - t_o)^2\right) \quad \text{................} \quad (2.5)$$

As we can see from the above equation that the received signal is same as the transmit signal but is delayed by t_o. The time-delay is the time taken by the signal to propagate to the target and back to the radar i.e. it is the time taken to travel twice the distance between the radar and the target.

$$t_o = \frac{2R}{c} \quad\ldots\ldots\ldots\ldots\ldots\ldots\ldots..\ldots\ldots.. \text{(2.6)}$$

Where R is the distance between the target and the radar and c is the speed of light.
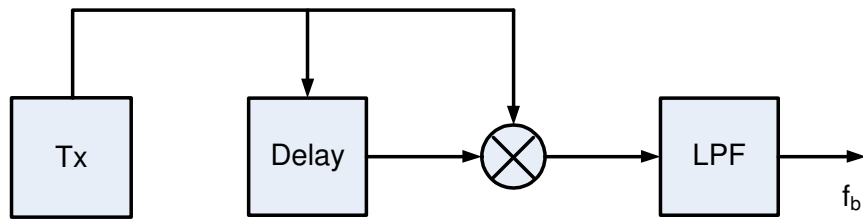
Figure 2.2 – Beat Signal generation

As shown in Figure 2.2 once the signal is received, it is mixed (multiplied) with a sample of the transmit signal in the receiver. This multiplication gives the sum and the difference terms. The difference in frequency between the transmitted and the received signals is called the beat frequency and is proportional to the target range.
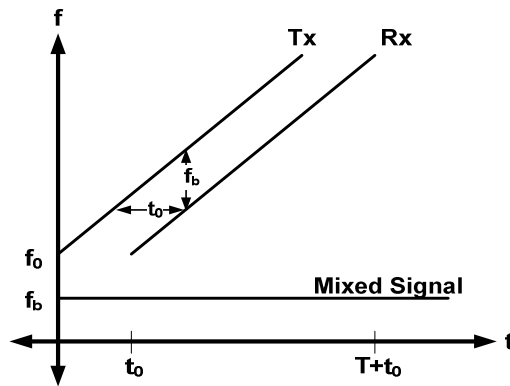
Figure 2.3 – Beat Frequency

Since the information we require is contained in the difference term the higher order terms are filtered using a low-pass filer. The difference term, which is beat signal, is given by

$$S_{Beat}(t) = \cos\left(2\pi f_o t_o + 2\pi k t_o t - \pi k t_o^2\right) \dots\dots\dots\dots\dots\dots (2.7)$$

The frequency of the beat signal can be obtained by the differentiating the phase. Thus, the frequency of the beat signal

$$f_{Beat} = \frac{1}{2\pi}\frac{d\phi}{dt} = k t_o = \frac{BW}{T} t_o \dots\dots\dots\dots\dots\dots\dots (2.8)$$

The delay t_o is two way travel time that can be mapped to range of the target using the equation

$$t_0 = \frac{2R\sqrt{\varepsilon_r}}{c} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (2.9)$$

By taking FFT of the time-domain beat signal we see a peak at the beat frequency in the spectrum. This frequency can transformed to the range of the target using the equations 2.8 and 2.9

Equations for multiple targets

When there are multiple targets, the received signal is a sum of the returns from individual targets with delays of $t_1, t_{2\dots}t_m$.

The received signal from multiple targets in time domain can be expressed as

$$S_{Rx}(t) = \sum_{m=0}^{M-1}\Gamma_m \cos\left(2\pi f_o(t-t_m) + \pi k(t-t_m)^2\right) \dots\dots\dots\dots\dots (2.10)$$

For multiple targets the range resolution of the radar is given by

$$kt_1 - kt_0 = \frac{1}{T} \quad \dots\dots\dots\dots\dots\dots\dots \text{ (2.11)}$$

Implies,

$$T_{min} = t_1 - t_0 = \frac{1}{kT} = \frac{1}{BW} \quad \dots\dots\dots\dots\dots\dots\dots \text{ (2.12)}$$

From this we can say that the minimum separation between two resolvable targets in time must be inversely proportional to the bandwidth of the transmit signal.

2.3 Nonlinearity in the beat signal

FM-CW radar can be used to measure the distance form the target. The non linearity in the transmit signal can have adverse effects on the measurement accuracy. Therefore, it is important that the transmit chirp does not have any higher-order nonlinearities. Otherwise nonlinearities in transmit signal will be translated into nonlinearities in the beat signal.

Suppose $\varepsilon(t)$ is the non linearity in the transmit signal then

$$S_{Tx}(t) = A\cos\left(2\pi f_o t + \pi k t^2 + \varepsilon(t)\right) \dots\dots\dots\dots\dots \text{ (2.13)}$$

Then the received signal becomes

$$S_{Rx}(t) = A\cos\left(2\pi f_o(t - t_o) + \pi t(t - t_o)^2 + \varepsilon(t - t_o)\right) \dots\dots\dots\dots \text{ (2.14)}$$

After mixing the transmit and receive signal at the receiver it becomes

$$S_{Beat}(t) = A\cos\left(2\pi k t_o + \phi_o + \varepsilon(t) - \varepsilon(t - t_o)\right) \dots\dots\dots\dots\dots \text{ (2.15)}$$

From the above equation the beat signal has nonlinearities from transmit and receive signals. These nonlinearities are range dependent. For short delays the nonlinearities in the beat tends to zero since the nonlinearities in transmit and receive signal will

cancel each other out. But they become more significant for longer ranges. Thus, the Fourier transform of the beat signal is an unfocussed Sinc function with widened main lobe and higher side-lobes. Also as the frequency increases nonlinearities become larger and can affect the resolution of FM-CW radar badly [9].

2.4 Signal generation for UWB Radar

FM-CW signal can be generated using a Direct-Digital Synthesizer (DDS). However, DDS are not available to generate chirp signal in the 8-12.5 GHz range. The UWB-radar designed to map near-surface layers with very-high resolution and accuracy needs an ultra-linear wideband chirp. The signal-generation unit of the UWB FM-CW radar in this thesis facilitates the generation of a highly-linear chirp using a fast-settling phase-locked loop driven by a Direct-Digital Synthesizer. Here a Voltage-Controlled Oscillator is used to generate a very wide bandwidth transmit chirp.

CHAPTER 3: PLL DESIGN AND SIMULATION

3.1 Introduction

As mentioned in the previous chapter the UWB radar is designed to map the near surface layers with high resolution. In order to do that the signal-generation unit must generate a highly-linear chirp. This linear-chirp can be generated using various techniques like correction of VCO tuning voltage and phase-locked Voltage-Controlled Oscillator etc. For this thesis a phase-locked oscillator is used to produce a linear chirp. The basic block diagram of a phase-locked loop is given below.

3.2 Phase lock loop Overview

As shown in the figure 3.1 a phase-locked loop consists of a crystal oscillator that generates a stable reference. This is one of the inputs to the phase detector. The other input is the output of the VCO after it is divided by N. The phase-frequency detector compares the phase of the reference signal and the divided VCO signal and the charge pump outputs a current which is proportional to the phase error between them [10].
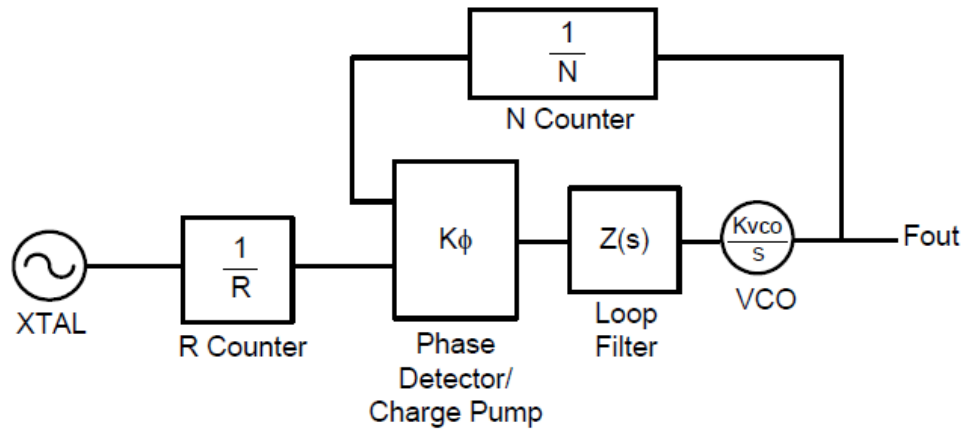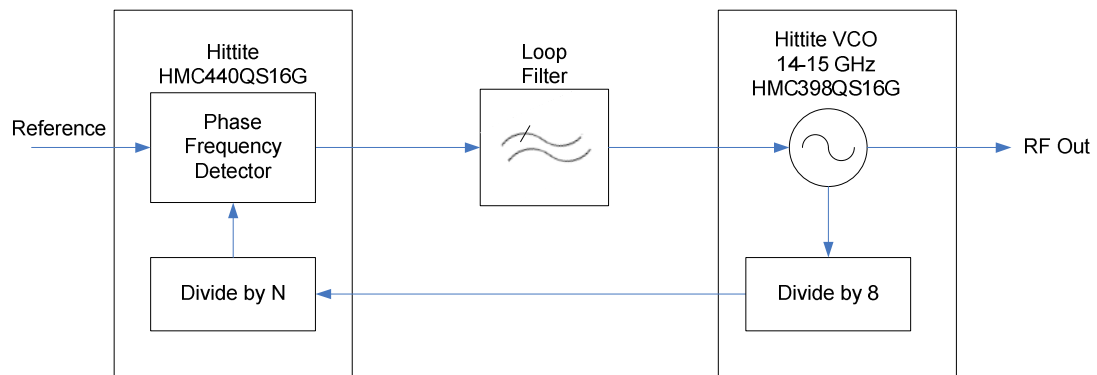
Figure 3.1- Basic Phase Lock Loop

This charge-pump current is passed through the loop-filter where the current is multiplied by the impedance of the loop-filter. The loop-filter outputs a voltage that is proportional to the phase difference between the reference, and the RF signal. This voltage generated by the loop-filter called as the tune voltage is given as an input to the VCO. The tune-voltage adjusts the output frequency of the VCO, such that the RF signal divided by N has same phase as the reference signal. Since phase is an integral of frequency the frequencies will also be matched when the PLL is in locked state.

3.3 PLL Design

The PLL design in thesis is based on Hittite's application note [11]. Figure 3.2 shows the block diagram of the actual circuit in the application notes. In the application notes they use a Hetero junction Bipolar Transistor (HBT) Digital Phase-Frequency Detector with integrated 5-bit counter (HMC440QS16G), a loop filter and a Monolithic-Microwave Integrated Circuit (MMIC) Voltage-Controlled Oscillator

(VCO) with divide-by-8 (HMC398QS16G) from Hittite Microwave Corporation [12]. The phase-detector in combination with the differential loop amplifier generates and output voltage that locks the VCO to a given reference. The reference frequency range of the Phase Detector is 10-1300 MHz [11].

Figure 3.2 - Block Diagram of Phase Lock Loop for 14-15 GHz

In the figure 3.2 the VCO is used to generate the RF output. The RF output is divided by 8 using the divide down internal to the VCO. The divided output of the VCO is given as an RF input to the Phase Detector. The 5-bit counter is used to further divide the RF input to the Phase detector. The Phase Detector compares the phase of the divided RF with the reference and generates a current proportional to the phase error. The loop filter transforms this current to a tune voltage which is given as an input to the VCO. This tune voltage locks the VCO to the given reference.

The PLL circuit in the application notes is as shown in the figure 3.3
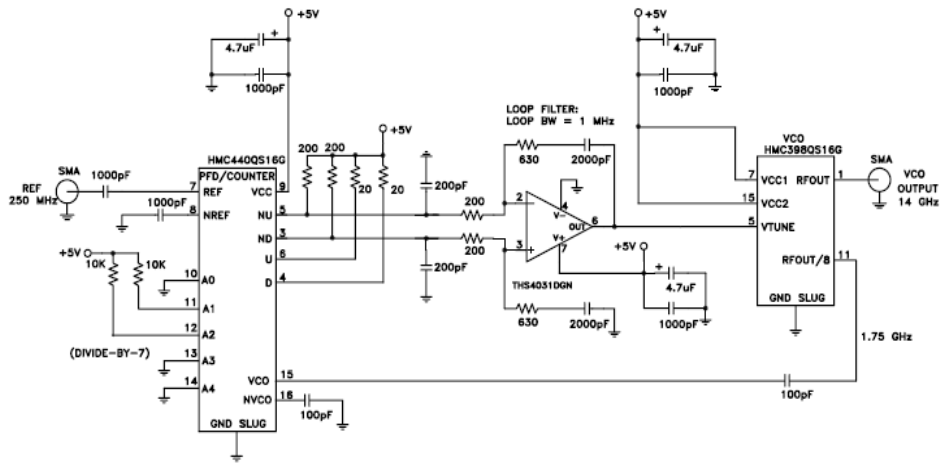
Figure 3.3- PLL circuit from Hittites application notes [11]

The application note uses Hittite evaluation boards for Phase Detector and the VCO. The Phase Detector, VCO and loop Filter are powered by a 5V supply. With VCO's on board divide by 8 and the 5-bit counter on the detector set to divide by 7, the net divide down is 56. A reference of 250 MHz is applied to the Phase Detector to phase lock the VCO at 14 GHz.

3.4 ADS Design and Simulation:

The circuit given in the application notes is simulated first in ADS. This is done to test the response of the loop-filter inside the loop. For this simulation the loop-filter is reproduced in ADS as it is in the application notes. And built-in models are used for phase detector, VCO and divide down. The ADS schematic is shown in figure 3.4.
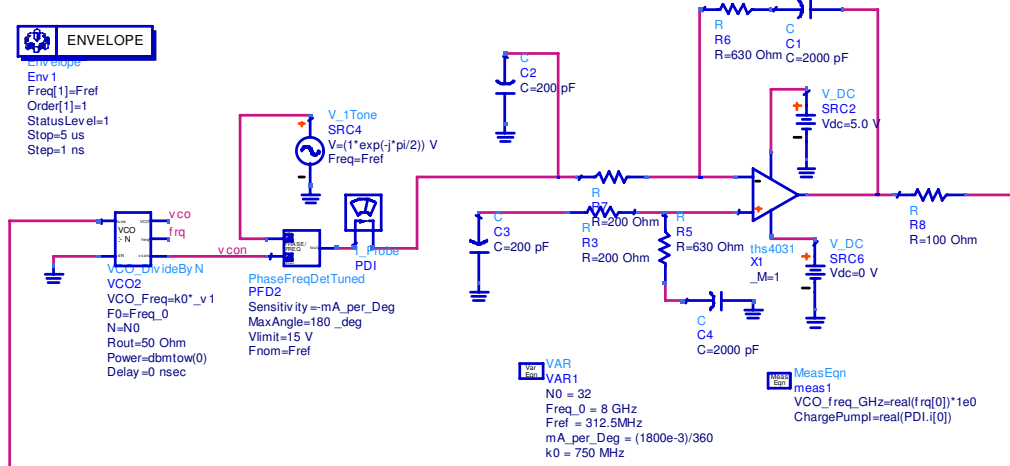
Figure 3.4-ADS Design for PLL

The simulation is carried out to generate a 10 GHz RF signal that is phase locked to the reference using PLL. The reference signal of 312.5 MHz is generated using a frequency source. VCO with built in divide down of 32 generates the RF comparable to the reference. Phase Detector compares the reference with the RF and produced an output proportional to the phase error. The loop filter transforms the output of the Phase Detector to exact tune voltage which locked the VCO to the corresponding reference. Thus, filter must be as low order as is possible. However, in order to correct for the nonlinearities of the VCO we need a wide bandwidth, wide enough so that the loop filter passes the correcting signal. Also the settling time of the PLL depends on the loop-filter bandwidth. In order to reduce the settling time we need a higher bandwidth. Thus, loop filter is very critical part of the PLL design. Since the loop-filter attenuates out spurious signals and noise from the charge pump current, and it presents a DC voltage to the VCO.

Keeping above constraints in mind the bandwidth of the loop filter is changed by changing the capacitor values and its response is observed. By doing this we found that the optimum values of the capacitors for which the PLL locked and a lower settling time is achieved. The results of this simulation are shown in the figures below.

Simulation Results:
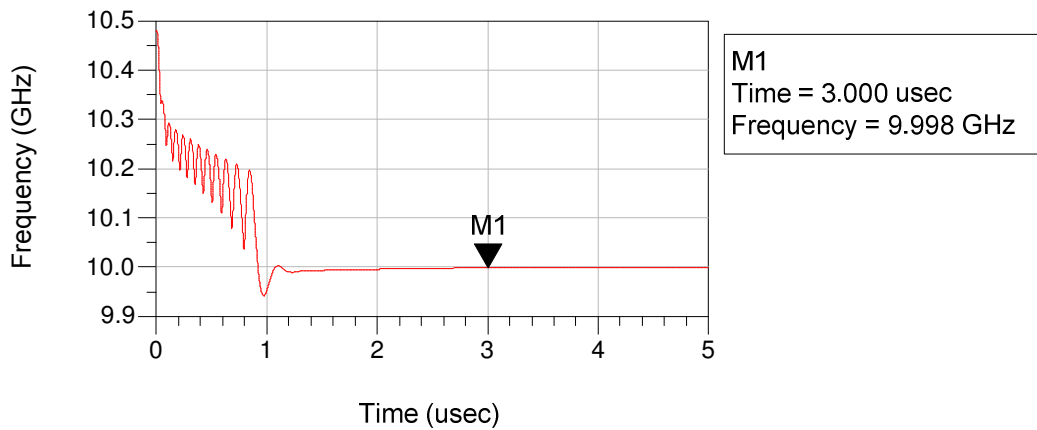
Figure 3.5 - Simulated response of PLL

The figure 3.5 gives the output of the VCO when the loop-filter is reproduced as it is in the application notes i.e. capacitors C2 and C3 are 200 pf and capacitors C1 and C4 are 2000 pf and BW=1 MHz. The figure shows that it takes around 3 us for the PLL to lock to 10 GHz.
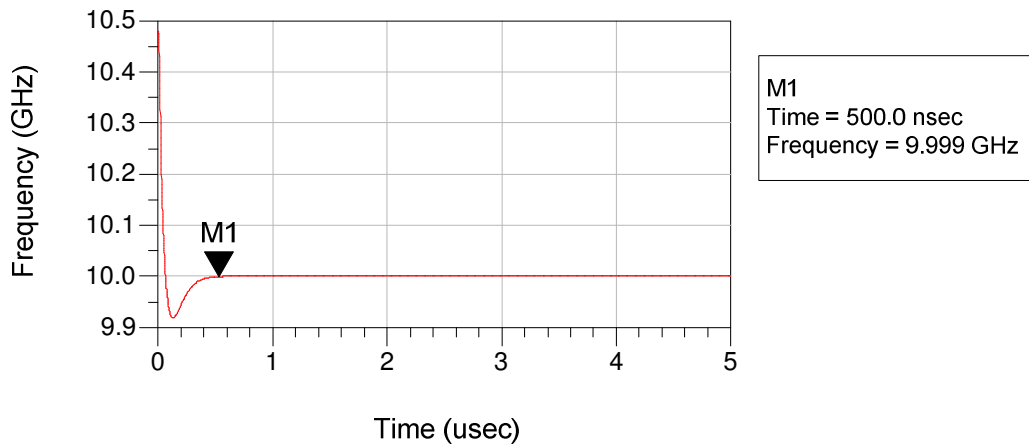
Figure 3.6 - Simulated response of PLL with lower settling time

The figure 3.6 gives the output of the VCO when the input capacitors are changed to increase the BW and thereby decrease the settling time. The values of C2 and C3 are changed from 200 pf to 20 pf and the capacitor C1 and C4 changed from 2000 pf to 200 pf in the ADS design. The figure shows that it takes around 500 ns for the PLL to lock.

3.6 Drawbacks of this design

Although the design of the PLL is based on the application note from Hittite, it went through a number of corrections and modifications before it is finalized for end use. The corrections are based either on the ADS simulations or on experimental tests performed in the lab. The drawbacks of the design in the application notes are mentioned below.

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Loop filter supply too low

The Common Mode Input voltage of the Op-amp THS4031 was 3.8 V when supply was 5 V [13]. And the voltage at the input of the loop-filter is more than the Common Mode Input voltage of the OpAmp. Thus, the supply to the OpAmp is too low. So OpAmp railed to the higher end and could never establish a lock. Therefore, a higher supply voltage to the OpAmp is required.

Also the tuning voltage range of the VCO was 0-10 V. In order to be able to sweep the entire range we needed to output of the loop filter go as high as 10 V. Therefore, instead of a 5 V supply a 15 V supply is given to the loop-filter.

No dual supply on Op-amp

With only positive supply differential loop filter Op-amp was railing to 0.9 V on the lower side. In order to have it go as low as zero the Op-amp was provided with a dual supply. And a diode was connected between the output and the ground in reverse bias in order to protect the VCO from receiving any negative voltage. Also a 10k Ohm pot is connected between pins 1 and 8 of the OpAmp to set the bias.

Apart from those mentioned above the divide down on the phase detector is either N=7 or N=4 as needed. This is done so that the reference frequency falls in the range of the DDS.

The above changes are made to first to 14-15 GHz PLL design to make it lock to the reference in the entire range. And once that worked fine the design is modified for UWB Radar which is given in then next section. The Experimental setup and the results for it are shown in chapter 4.

3.7 PLL Design for UWB Radar

Previous section discussed the PLL design for 14-15 GHz. Some modifications are made to the design to get it to work for our specification.
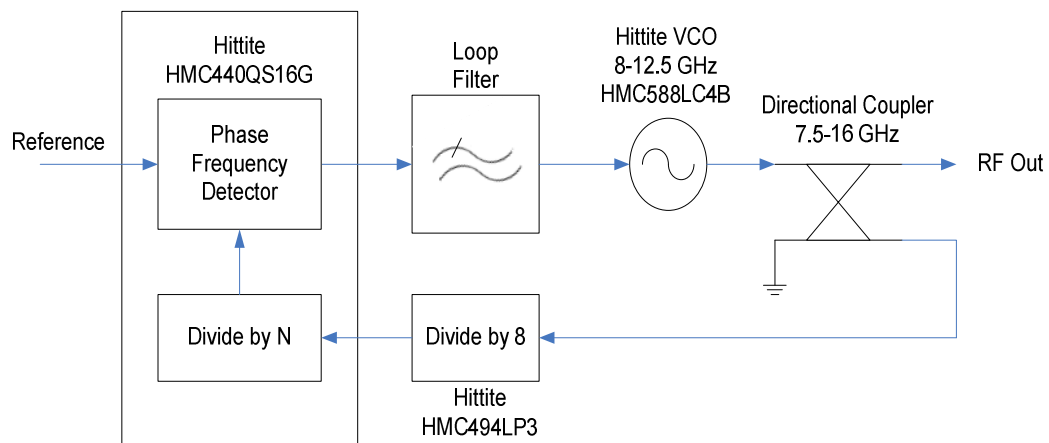
Figure 3.7 - Block Diagram of Phase Lock Loop with 8-12.5 GHz VCO

Since the UWB Radar requires a wide-band chirp so instead of 14-15 GHz VCO a wide-band MMIC VCO 8-12.5 GHz (HMC588LC4B) is used. A 10 dB directional coupler from Midisco 7.5-16GHz is used to provide the necessary feedback to the phase detector. An external pre-scalar is used since the VCO does not

have divide by 8 on board unlike the previous one. The divide by N on the phase

detector is changed from 7 to 4. So the net value of N of 32 is used instead of 56.

CHAPTER 4: IMPLEMENTATION AND RESULTS

Implementation of the phase lock loop is done by first designing a Printed Circuit Board (PCB) layout for loop filter using EAGLE Layout Editor. It is milled in house and populated with components. The loop filter is tested individually and inside the loop in the lab. Due to a few drawbacks in the loop-filter design the PLL did not lock at first. Several changes are made to the loop-filter design to get it to lock. The drawbacks of the loop filter design were discussed in the previous chapter. The Final version of the loop filter design is given below.

4.1 Loop Filter Design

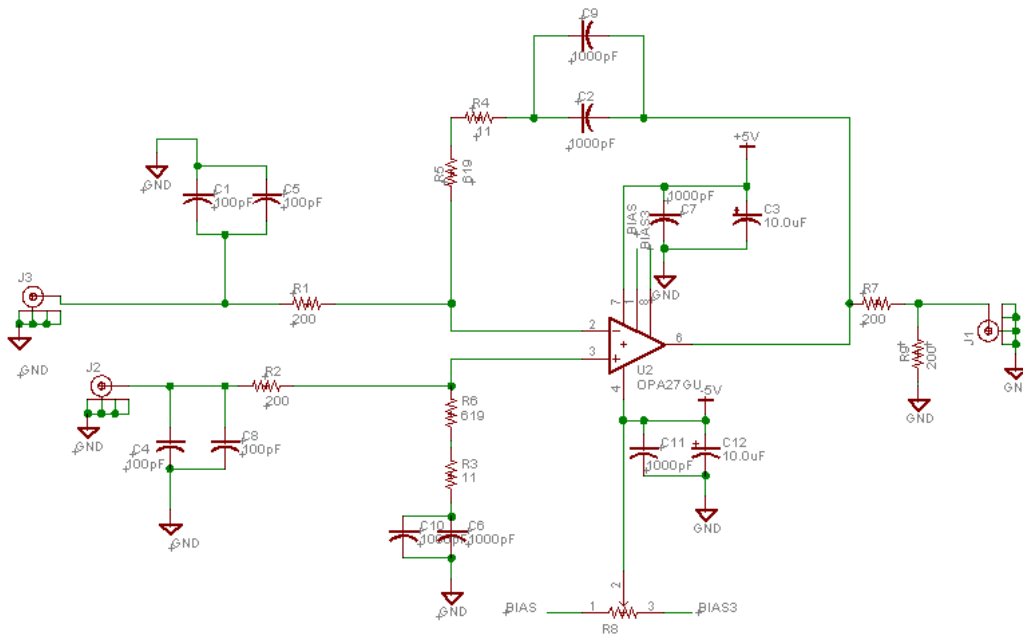The Loop Filter Schematic and its corresponding PCB layout are shown in Figures 4.1 and 4.2.

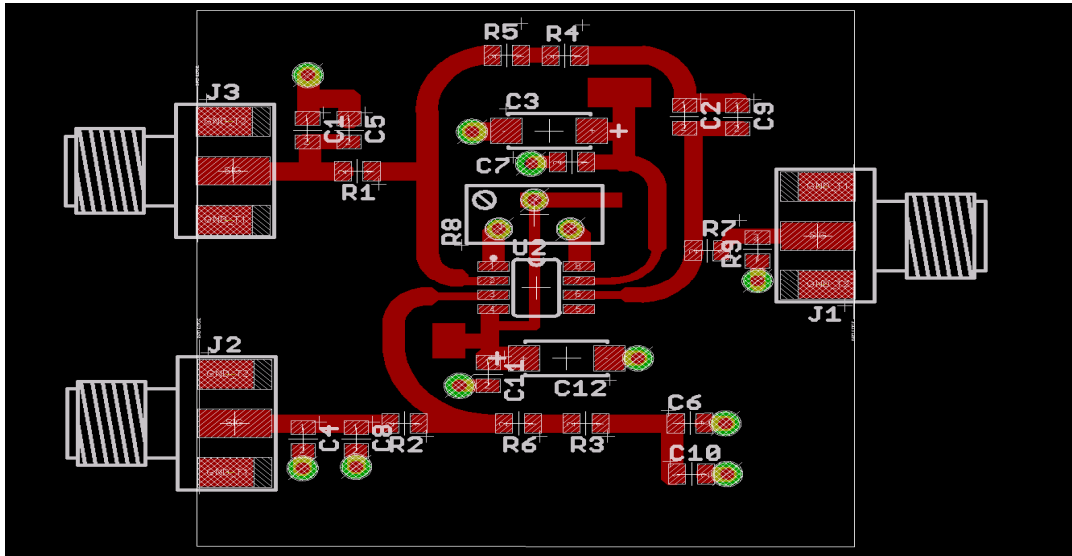**Figure 4.1 – OpAmp Schematic in Eagle**

Figure 4.2- PCB layout of the Loop Filter

4.2 DDS Board settings

Analog Devices AD9910 Direct Digital Synthesizer is used to generate a stable reference. The DDS board lay out is given in figure 4.3.
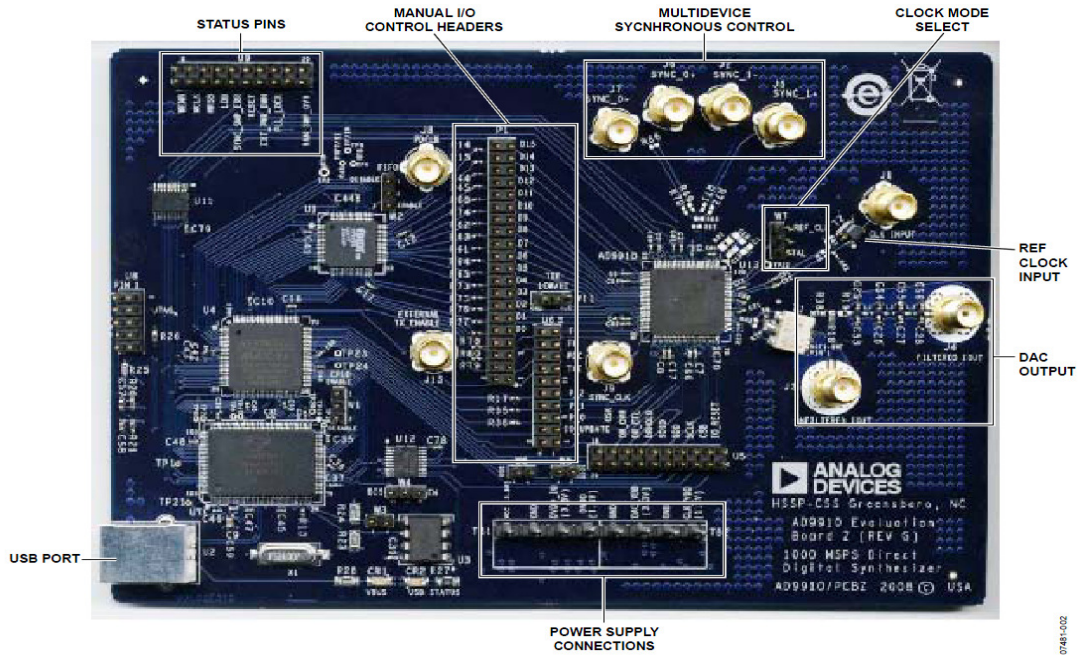

Figure 4.3- DDS board layout

The DDS Evaluation board is given two voltages 1.8 V and 3.3 V using supply connectors TB1 and TB2. TB1 powers the USB interface circuitry, digital I/O interface, and the digital core. TB2 powers DAC and input clock circuitry. The USB port on the board is used to communicate with AD9910 evaluation software. This software is installed on a PC and the DDS board is controlled using this software. The following jumper settings are used for successful functioning of the DDS board [14].

The FIFO jumper on the DDS board is set to disable. The CPLD is set to enable. W1 and W4 are also set to enable. Jumpers on W3 W5 and W6 are used. W7 is set to REF_CLK. Jumpers are also used on RESET and EXT PWR DWN pins.
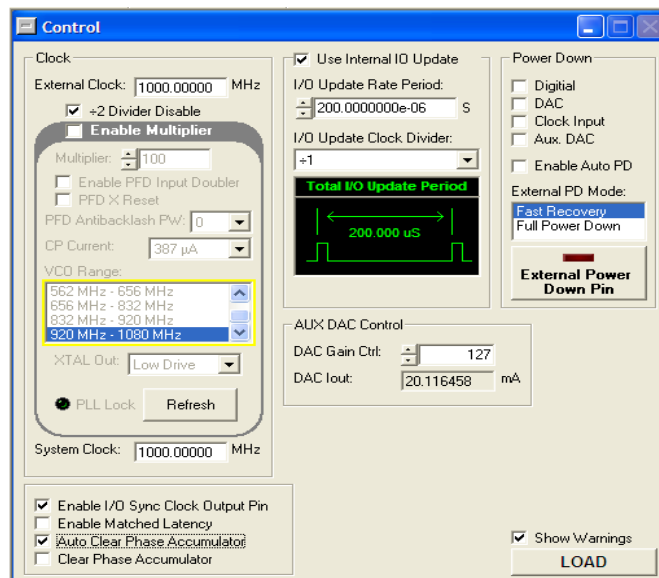
Figure 4.4- AD9910 Evaluation software control window

Apart from the above settings a reference clock input of 1 GHz is given to the DDS using a RF signal generator in the lab. Once all power connections, USB port connection, jumper settings and clock input are set right and when the software is

launched a green window splash appears which displays the status of the board. Green writing in that window indicates that the software is successfully loaded.

Once the software is successfully loaded the board is controlled using the controls on the software. The control window of the software is given in figure 4.4. The External clock input is set to 1 GHz. The divider is disabled and the PLL multiplier is not used for our application. The Enable I/O Sync Clock Output Pin box is checked and the rate of I/O update is programmed. This I/O update is used to load the frequency ramp every t microseconds.

The Profiles window shown in figure 4.5 is used to generate single frequency reference signal. The profile to be activated is selected and is loaded to generate required frequency.
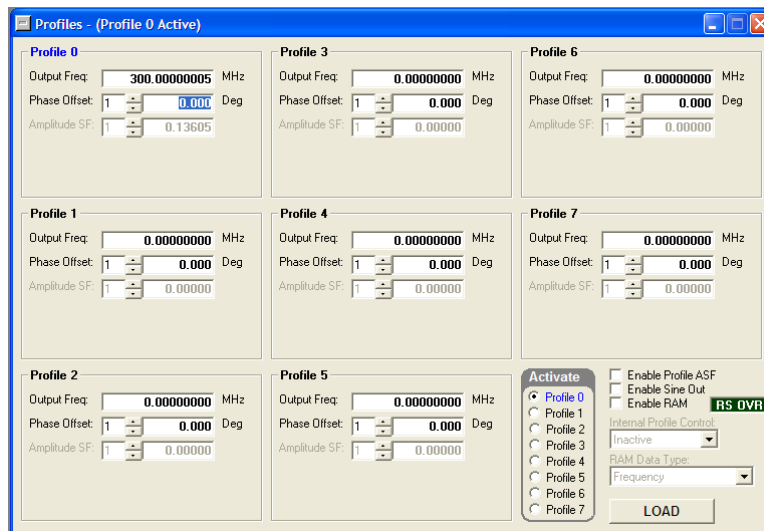
Figure 4.5- AD9910 Evaluation software profiles window

The OSK and Digital Ramp Control window shown in figure 4.6 is used to generate the frequency ramp. The Enable Digital Ramp Generator box on the window

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is checked and frequency mode is selected to generate to generate frequency sweep. The sweep Frequency 0 and sweep Frequency1 are set to sweep from start frequency to stop frequency. The Rising and falling step size and step intervals of the frequency sweep are also set as required. The ramp up button is pushed and the ramp is loaded using LOAD.
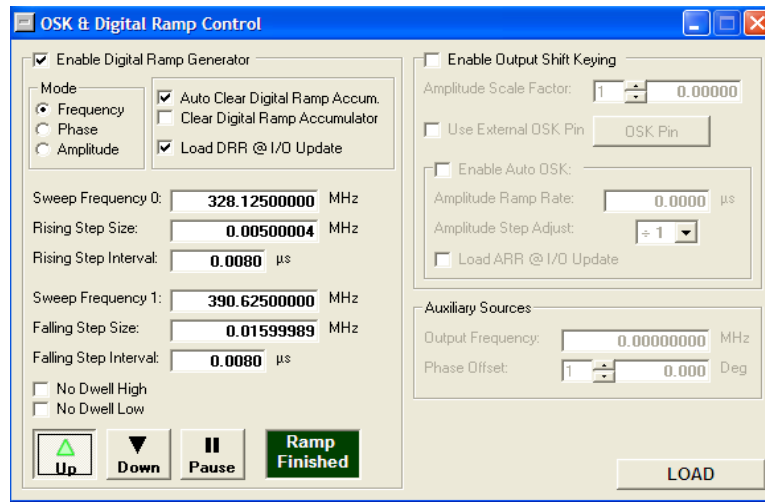
Figure 4.6- AD9910 Evaluation software OSK & Digital Ramp Control

4.3 Lab Setup

As mentioned in the previous chapters in order to generate the ultra linear transmit chirp required by UWB Radar a fast settling PLL is used. The PLL design is discussed in chapter 3. The PLL is set up in the lab as shown in the block diagram in figure 4.7. A wideband VCO from Hittite Microwave Corporation is used to generate a wide-band chirp signal. It accepts wide range of tuning voltages from 0-13 V and has a fast tuning bandwidth of 65 MHz. The VCO's output frequency ranges from 8-12.5 GHz [15]. 10 dB 7.5-16 GHz Coupler from Midisco is used to provide necessary feedback. This RF feedback signal is divided by 8 and further divided in the phase detector counter in order to make the RF signal comparable to the reference. The output of the divide down along with the reference signal from Analog devices DDS is given to the Phase-Frequency Detector.

The phase detector produces charge pump current proportional to phase error. This is given to the loop filter PCB. The loop filter generates a tune voltage which locked the VCO to the given reference. The block diagram explains the set up of evaluation boards in the lab in figure 4.7 and the test set up of evaluation board is given figure 4. 8. The set up is mostly same incase of all three VCO's except that in case of 14-15 GHz VCO a divide by 8 is on VCO board. Thus, an external prescalar is not used.
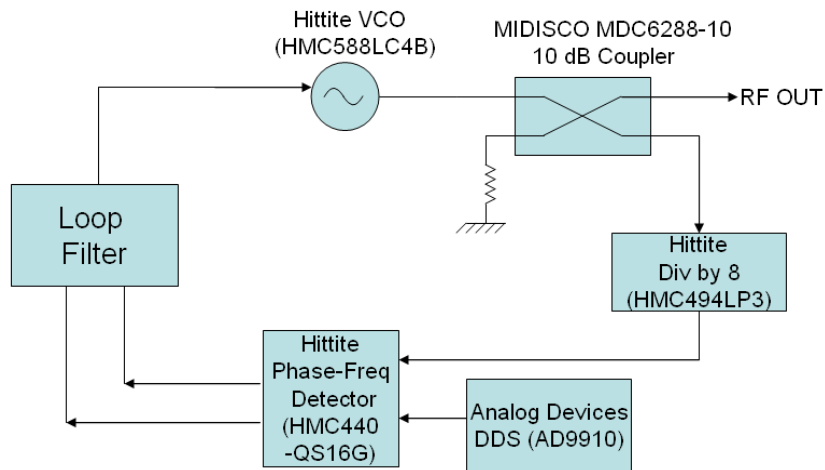
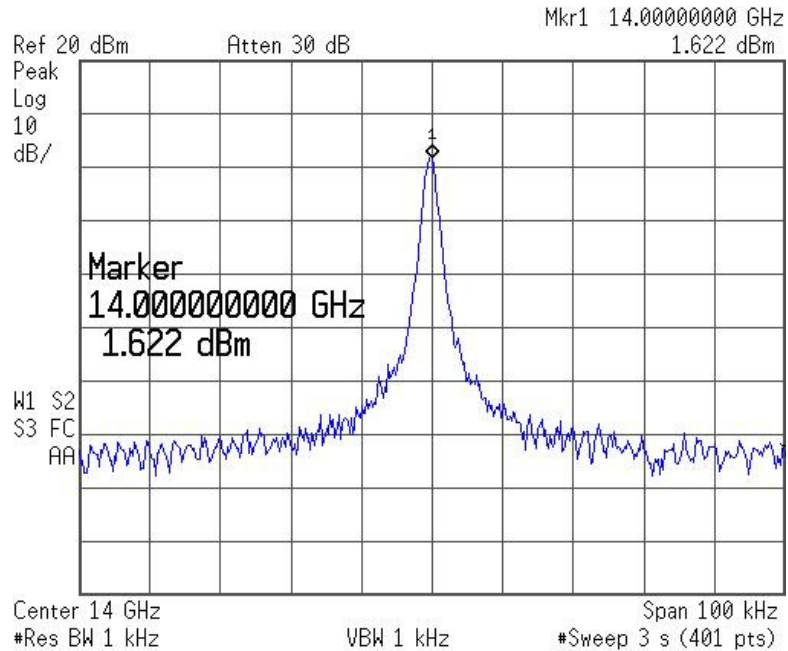**Figure 4.7 –Block Diagram for the PLL set up in the lab**
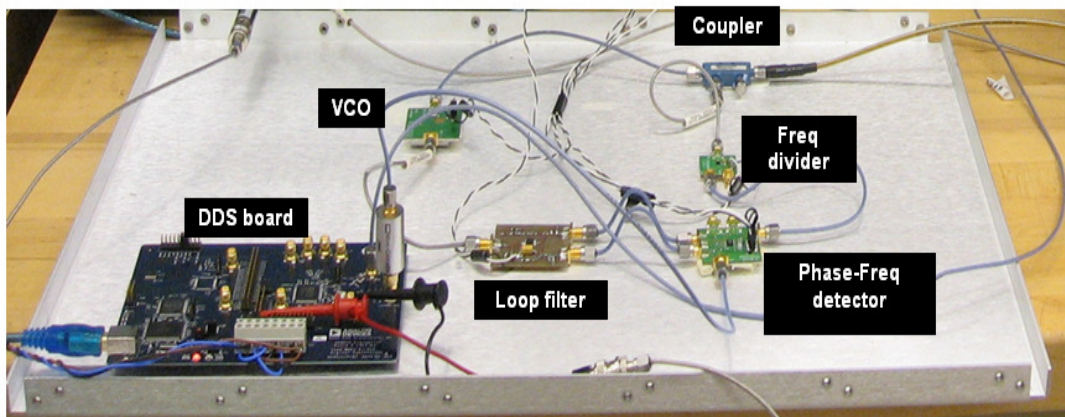
Figure 4.8 – Experimental Set up for the PLL

All the evaluation boards except for the loop filter and DDS are given 5V supply. The loop filter is given +/- 15-V and the DDS board is given 1.8-V and 3.3-V supply. The reference input required by the PLL is given using the DDS board and the RF output of the PLL is viewed on the spectrum analyzer.

4.4 Results for 14-15 GHz VCO

First the PLL with 14-15GHz VCO is tested in the loop. The divide down of the PLL is set to 56. A reference clock of 250 MHz is given to the phase detector. It locked the VCO at 14 GHz.

Mkr1 14.00000000 GHz
Ref 20 dBm   Atten 30 dB   1.622 dBm
Peak
Log
10
dB/

Marker
14.000000000 GHz
1.622 dBm

W1 S2
S3 FC
AA

Center 14 GHz   Span 100 kHz
#Res BW 1 kHz   VBW 1 kHz   #Sweep 3 s (401 pts)

Figure 4.9 -PLL locked to single frequency at 14 GHz

Figure 4.9 shows the PLL locked to 14 GHz. It can be seen from the figure that it's a very nice looking peak in 100 kHz span. The noise floor is 50 dB below the peak. Similar to this the VCO is locked to several discrete frequencies in the range 14-15 GHz by giving a corresponding reference signal.

Once the PLL locked to all discrete frequencies in the range it is tested for small frequency sweeps. The DDS generates small frequency sweeps for the reference to lock the VCO in that range. A reference sweep of 250-259MHz generates

an RF chirp of 14-14. 5 GHz. Figure 4.10 shows the PLL locked in 14-14.5 GHz range. This process is repeated for several small frequency sweeps in the range of the VCO.
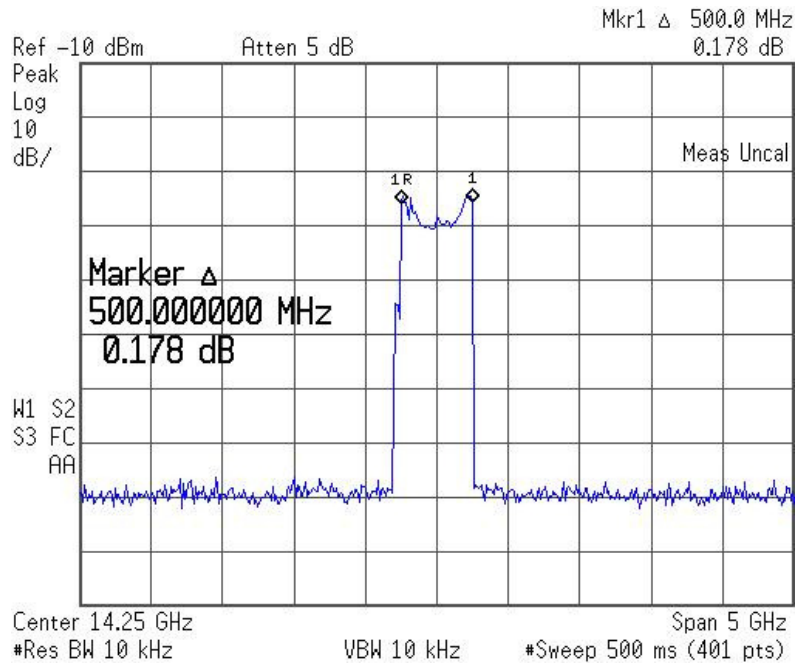
Figure 4.10 -PLL locked to Small frequency sweep
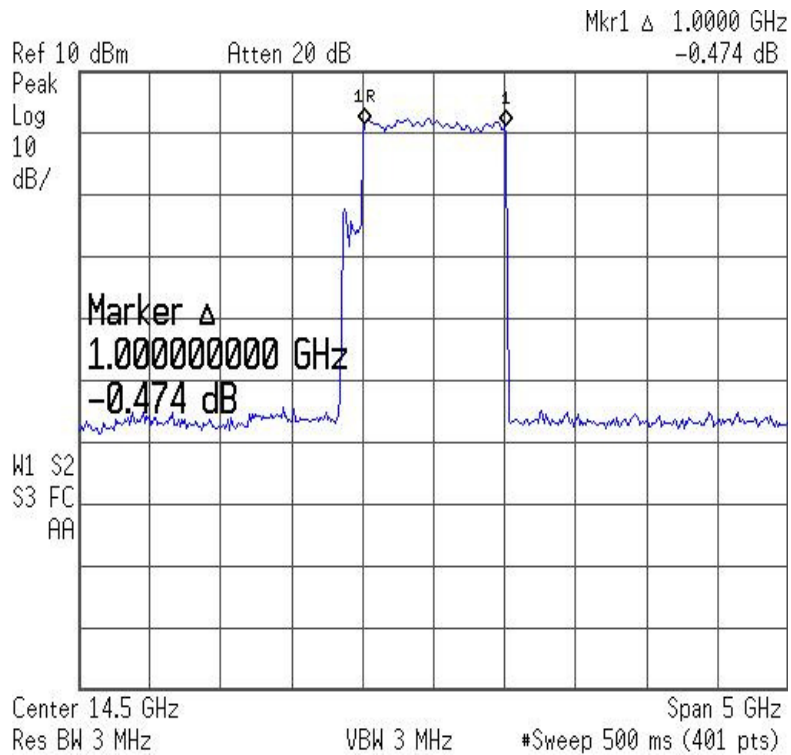
Figure 4.11 -PLL locked to Full frequency sweep from 14-15 GHz

The Figure 4.11 shows the PLL locked to the entire range of VCO from 14-15 GHz when a reference of sweep of 250-267.86 MHz is applied using the DDS. The artifact seen at the starting of the sweep is a transient from PLL trying to attain the lock. This is visible in all plots for frequency sweeps. This can be better visualized in time domain as seen in figure 3.5 in chapter 3.

4.5 Results for 8-12.5 GHz VCO

For this case the VCO is changed to 8-12.5 GHz VCO to generate a wide band chirp for UWB Radar. Also the Divide down in this case is of 32 used instead of 56. Similar to previous case the PLL is made to lock to several discrete frequencies and

small frequency sweeps before trying to lock it to the entire range of the VCO. The spectrum analyzer plots for each of them are given below.

The VCO locked to single frequency and generating 10 GHz RF chirp using a 312.5 MHz reference is given in figure 4.12. Figure 4.13 shows the VCO locked to a smaller frequency sweep. Figure 4.14 shows the VCO locked in the entire range 8-12.8 GHz. The time taken to sweep the entire range is 240 us.

Figure 4.12 -PLL locked to single frequency at 10 GHz
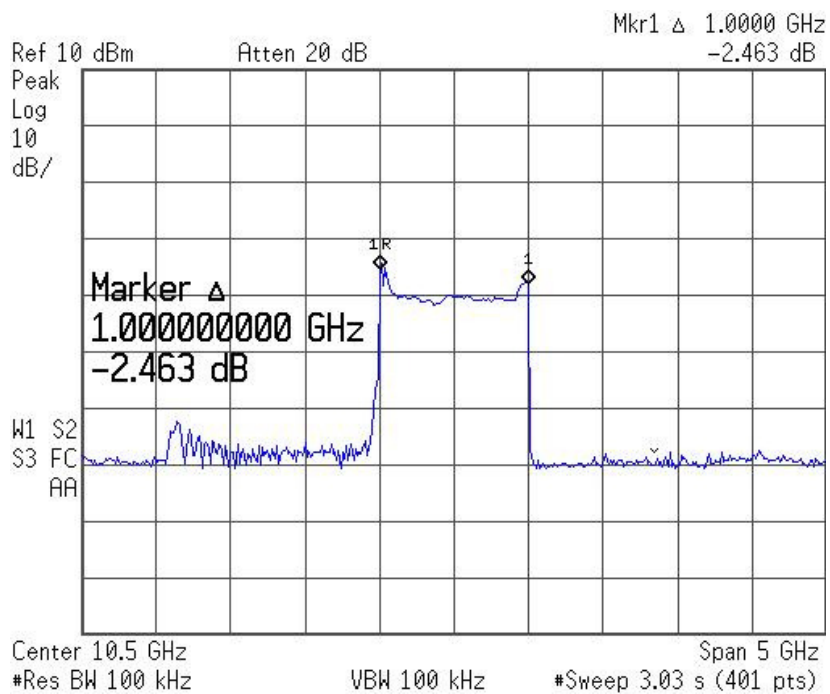
Figure 4.13 -PLL locked to Small frequency sweep
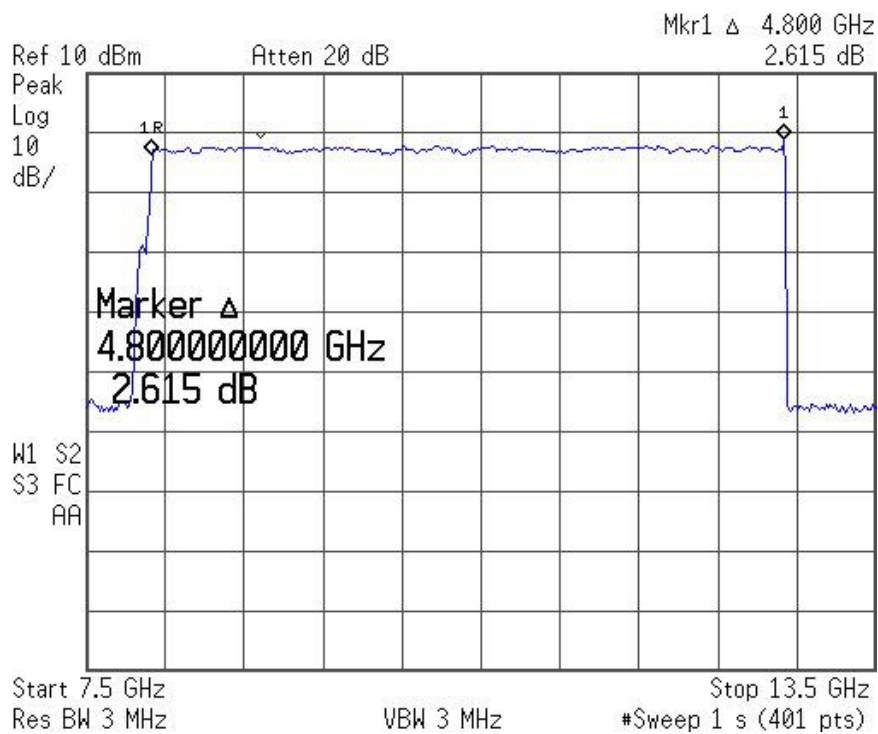
Figure 4.14 -PLL locked to Full frequency sweep from 8-12.8 GHz

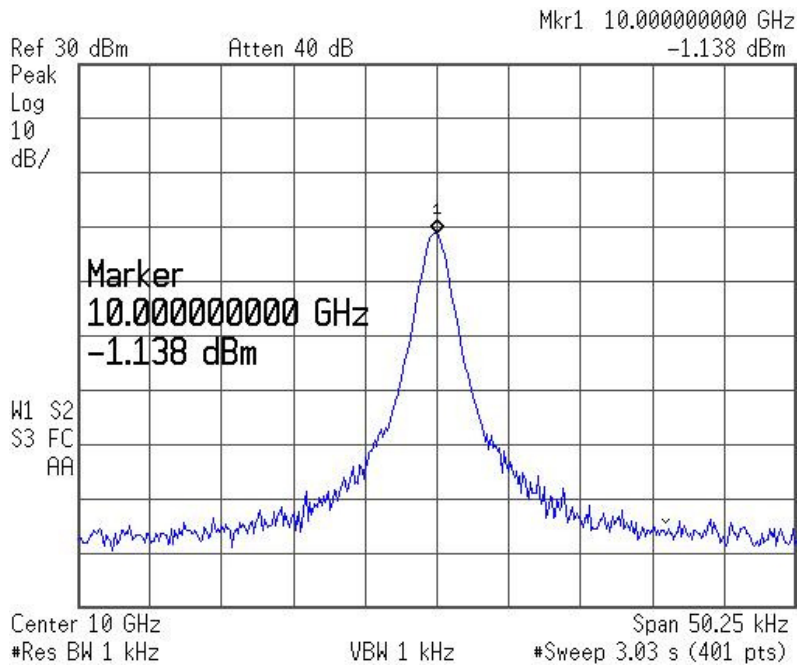**4.6 Results for 12-18 GHz VCO**

To produce a 12-18 GHz sweep a different VCO from Silversima VO3260P/02 is used. Since the same phase detector is used and the VCO had the same K_v as the others the same loop filter worked for this range [16]. Hence the same set up is used as in the previous case except the divide down on the phase detector counter is changed. This is because the DDS generated only up to 400 MHz. Thus to generate a reference chirp for the entire 12-18 GHz range the divide down on the phase detector needs to be configured to divide by 7 which resulted in a total divide down on 56. As in the previous case this VCO is also locked to discrete frequencies first before sweeping the entire range. The spectrum analyzer plots for the phase locked VCO 12-18 GHz are given in figures 4.15 and 4.16.
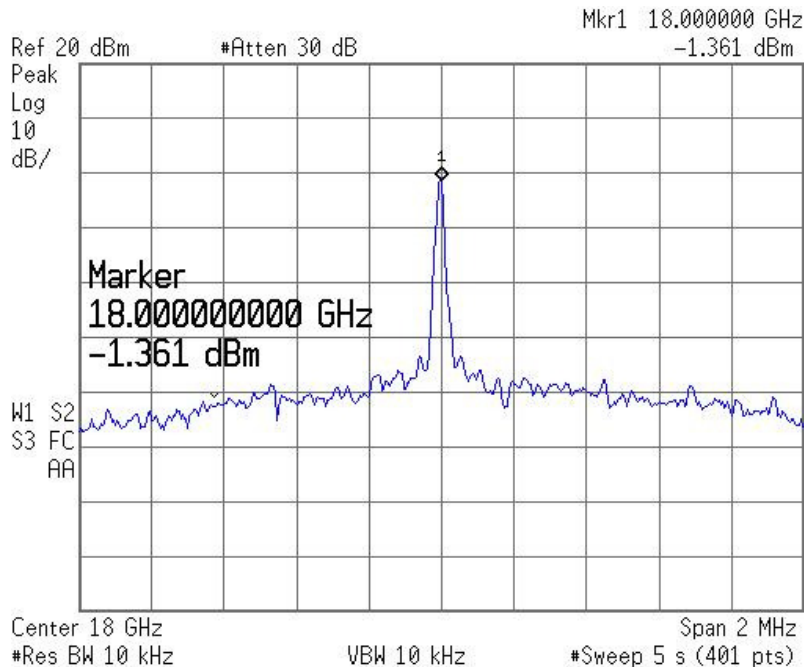
Figure 4.15 -PLL locked to single frequency at 10 GHz
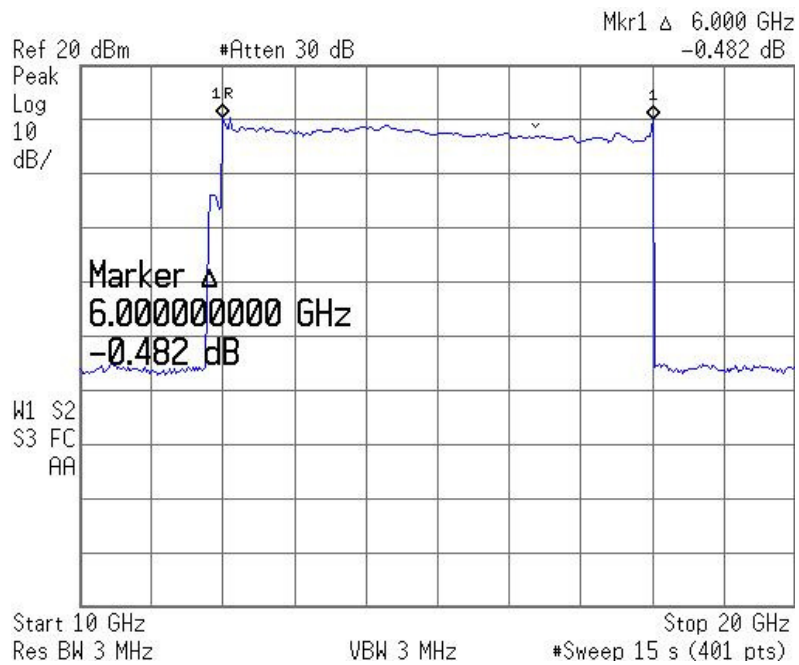
Figure 4.16 -PLL locked to Full frequency sweep from 12-18 GHz

From figure 4.16 we can see that the PLL is locked to the entire range of the VCO 12-18 GHz. There is just a couple of dB of variation in power over the entire range. The artifact at the starting of the sweep is a transient from the PLL trying to attain the lock.

4.7 Measurement of settling time of the PLL in the lab

In order to measure the settling time of the PLL in the lab is set up as shown in the figure4.7 and figure 4.8. A fast digitizing scope is used to measure the settling time. The PLL is locked to single frequency first using the reference frequency signal from the DDS. The reference frequency is then changed by 20 MHz which corresponds to change in RF signal of 620 MHz and the time taken for the PLL to attain lock is measured using the oscilloscope. Instead of looking at the RF output tuning voltage which is a representative of the RF output of the VCO is monitored.

The figure 4.17 is a screen shot from the oscilloscope for tuning voltage to show the settling time. From the figure we can see that the settling time of the PLL is 500 ns. This is same as what we saw in the ADS simulations.
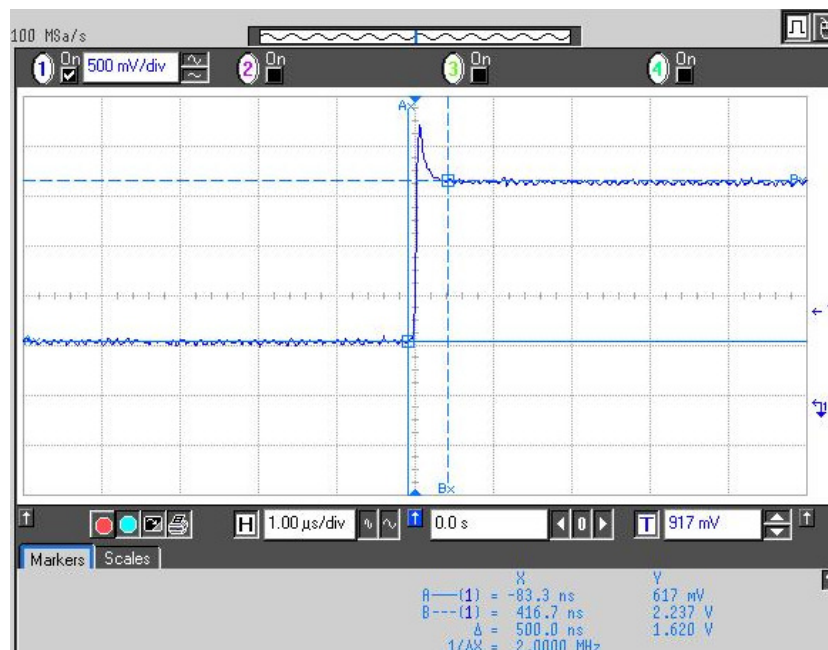

Figure 4.17 –Measurement of settling time of the PLL

4.8 Simulation of synthetic target or Delay line test

To check the linearity of the chirp signal generated by the phase locked VCO, a beat signal is generated using a delay line set up which comprised of a coupler, amplifier, delay line, mixer and low-pass filter. This is also simulation of FMCW radar. The procedure followed to simulate FMCW radar and generate the beat signal is as follows. The transmit chirp T is generated by the phase locked VCO. This is delayed using a delay line and is called the received signal R. Transmit and receive signals are passed through a mixer that generated sum T+R and difference T-R terms. Since we are interested in the difference term the output of the mixer is low pass filter to get rid of the high frequency terms. The output of the low pass filter is beat frequency. This beat signal data are collected and analyzed in Matlab. The beat frequency is the frequency difference between transmit and the receive signals. This difference frequency can be converted to range from the target.

The block diagram of the delay line setup is shown in the figure 4.18. And the experimental set up for lab is shown in figure 4.19. The Hittite HMC588LC4B VCO generates linear sweep 8-12.8 GHz sweep in the phase-locked loop. This transmit chirp is divided into 1.8 GHz bands and mixed down since the delay line and some other components operate in 0.2- 2 GHz range. This down converted 0.2-2 GHz sweep is amplified using Mini-Circuits amplifier before it is passed through delay line. This amplified transmit signal is passed through Mini-Circuits (ZFDC-15-5) coupler. The through signal is amplified again using Mini-circuits ZJL-4HG amplifier and was given to the LO port of the Mini-Circuit (ZFM-150) mixer. The coupled

signal is made to pass through the 685 m long delay line with a maximum attenuation level of about 3 dB over the operating frequency range. This delayed chirp is amplified to the required power level and fed through the RF port of the Mini Circuits mixer. The output of the mixer contains sum and difference frequencies. Since the information we wanted is in the difference frequency the beat signal is passed through a Mini Circuits DC-100 MHz low-pass filter.
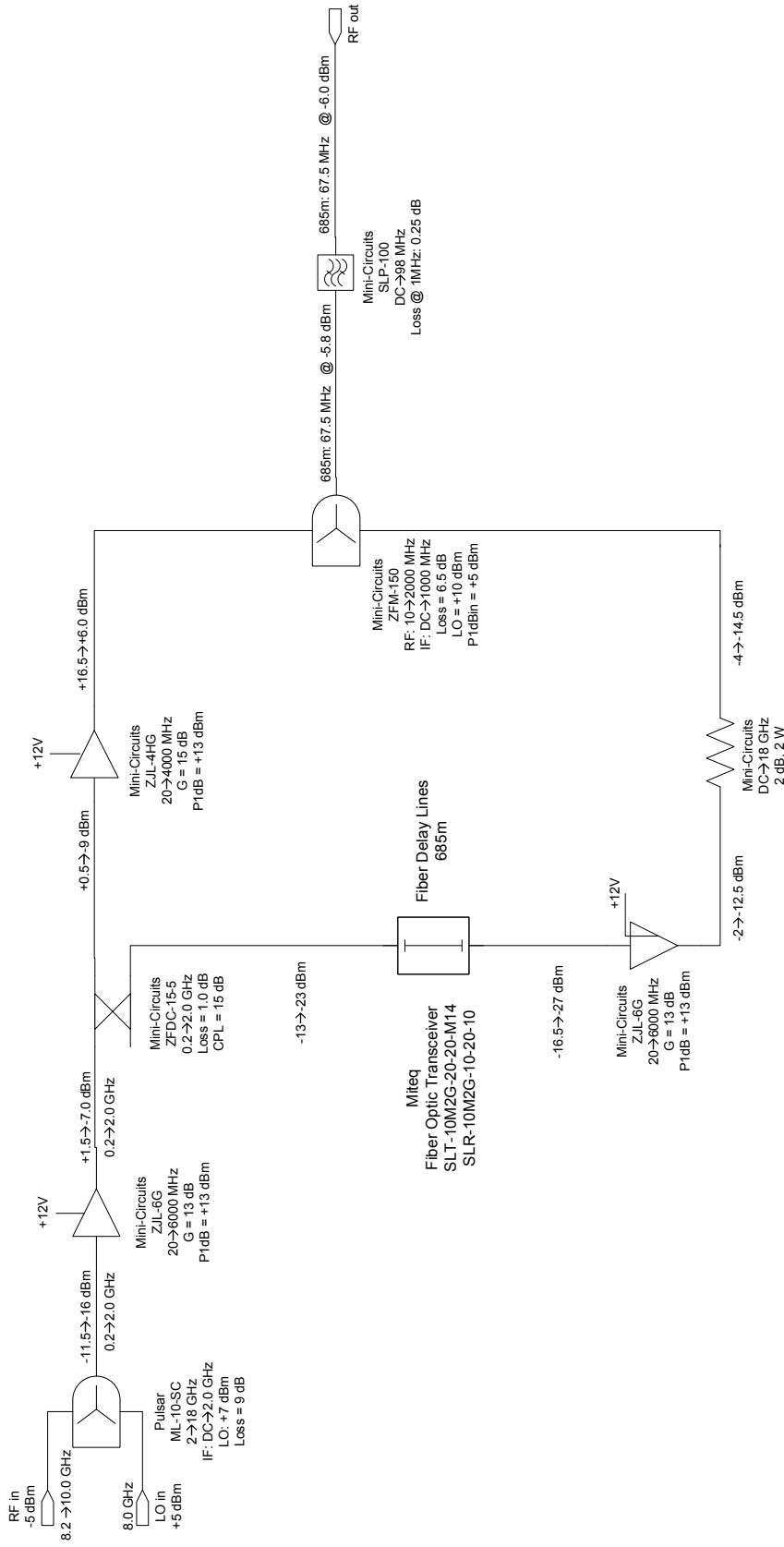
Figure 4.18: Fiber Delay Line and Analog Receiver

RF in
-5 dBm

8.2 →10.0 GHz

8.0 GHz

LO in
+5 dBm

Pulsar
ML-10-SC
2→18 GHz
IF: DC→2.0 GHz
LO: +7 dBm
Loss = 9 dB

-11.5→-16 dBm
0.2→2.0 GHz

+12V

Mini-Circuits
ZJL-6G
20→6000 MHz
G = 13 dB
P1dB = +13 dBm

+1.5→-7.0 dBm
0.2→2.0 GHz

0.2→2.0 GHz

Mini-Circuits
ZFDC-15-5
0.2→2.0 GHz
Loss = 1.0 dB
CPL = 15 dB

+12V

Mini-Circuits
ZJL-4HG
20→4000 MHz
G = 15 dB
P1dB = +13 dBm

+0.5→-9 dBm

+16.5→+6.0 dBm

685m: 67.5 MHz @ -5.8 dBm

Mini-Circuits
SLP-100
DC→98 MHz
Loss @ 1MHz: 0.25 dB

685m: 67.5 MHz @ -6.0 dBm

RF out

Mini-Circuits
ZFM-150
RF: 10→2000 MHz
IF: DC→1000 MHz
Loss = 6.5 dB
LO = +10 dBm
P1dBin = +5 dBm

-4→-14.5 dBm

Mini-Circuits
DC→18 GHz
2 dB, 2 W

-2→-12.5 dBm

Mini-Circuits
ZJL-6G
20→6000 MHz
G = 13 dB
P1dB = +13 dBm

+12V

-16.5→-27 dBm

Miteq
Fiber Optic Transceiver
SLT-10M2G-20-20-M14
SLR-10M2G-10-20-10

Fiber Delay Lines
685m

-13→-23 dBm

39

Figure 4.19 –Linearity check test set up

The test set up used to produce the beat frequency is shown in figure 4.19. The delay line that serves as a synthetic target and the analog receiver are put in a box. The box had two inputs RF IN and LO IN and one output IF OUT. The RF chirp produced by the PLL is given to the RF IN and an LO signal is given to LO port to down convert the RF chirp. The output of this box is the beat signal.

The beat signal is obtained by using delay line as a synthetic target and mixing transmit and receive signals inside the analog receiver box. This beat signal is captured on the LeCroy Oscilloscope. The Fast Fourier Transform (FFT) of the beat signal is view on the oscilloscope using the built in math functions before recording the data. This beat signal is saved on a flash drive in data format for further processing in Matlab.

The spectrum analyzer plots of the beat frequency for a fiber optic delay line 685 m long are given below. The length of the delay line translates into a time delay of 3.425 us. The beat-frequency signal for 3.425 us delay, 1.8 GHz bandwidth and a pulse-width of 90 us is at 67.5 MHz. The plot below shows the beat-frequency signal at 67.22 MHz for the 8-12.5 GHz VCO.
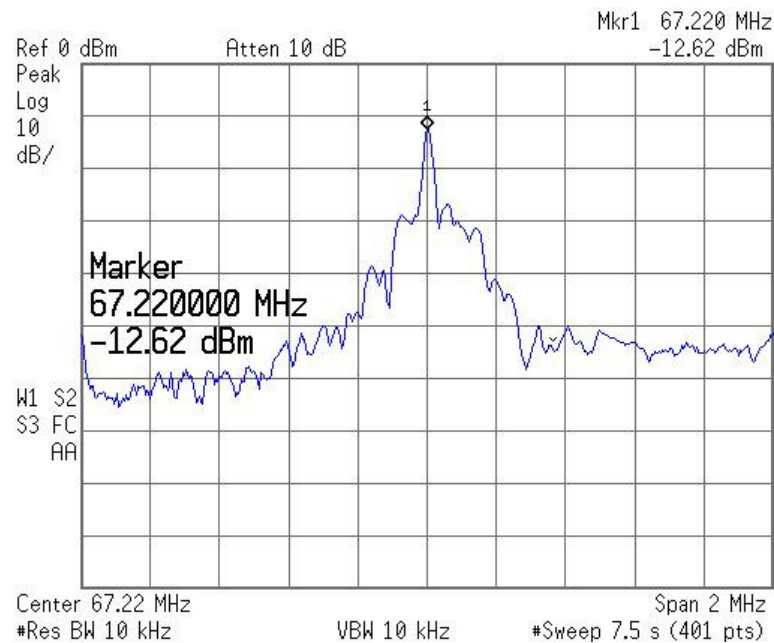
Figure 4.20 –Beat Frequency at 67.22 MHz 3.425 us delay, 1.8 GHz BW, 90 us pulse width using 8-12.5 GHz VCO

The same process of generating the beat frequency is repeated for 12-18 GHz VCO. Since the divide down for 12-18 GHz case is 56 instead of 32 the pulse width was 51.43 us instead of 90 us. Thus, the beat frequency is expected at 118.3 MHz which is very close to what is observed as shown in Figure 4.21.
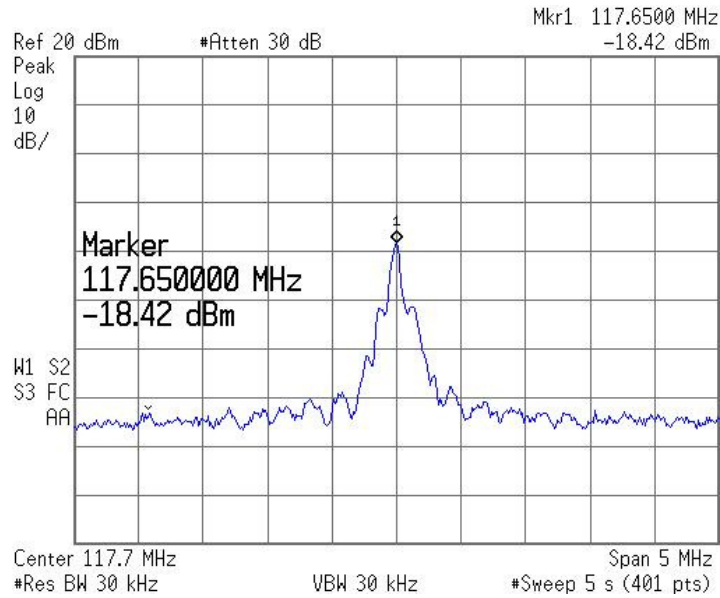
Figure 4.21 –Beat Frequency at 117.65 MHz for 3.425 us delay, 1.8 GHz BW, 51.43 us pulse width using 12-18 GHz VCO

This signal is saved and processed in Matlab. A Hanning window is applied to it to reduce the side-lobes 32 dB below the main lobe and FFT is taken to observe the frequency spectrum. Figure 4.22 shows beat-signal frequency response.

The beat signal from uncompensated frequency sweep for the same 8-12.5 GHz VCO from Nazia Ahmed's thesis work is given in figure 4.23. The figure also shows the compensated beat-frequency signal using hardware techniques [17].

From the figure 4.22 we can see that the frequency response of a beat signal can be described by a Sinc function. It has a sharp main lobe and the sidebands are symmetric about the main lobe. The fact that we see a periodic components equally spaced about the peak indicates that it is coming from amplitude modulation.
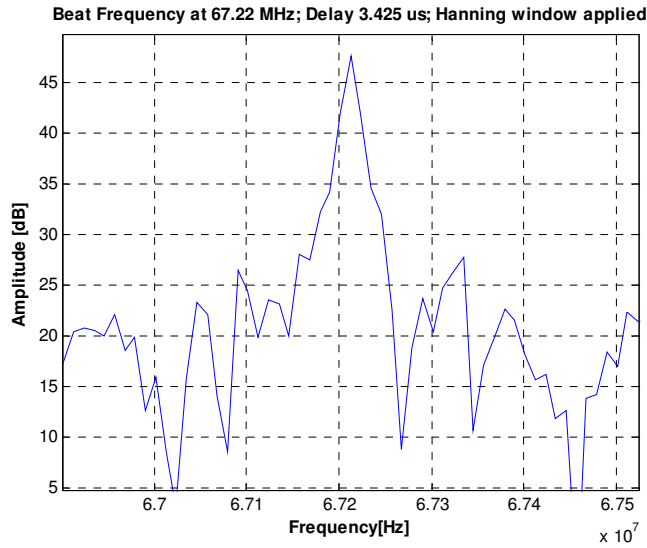
Figure 4.22 – Corrected beat signal using PLL
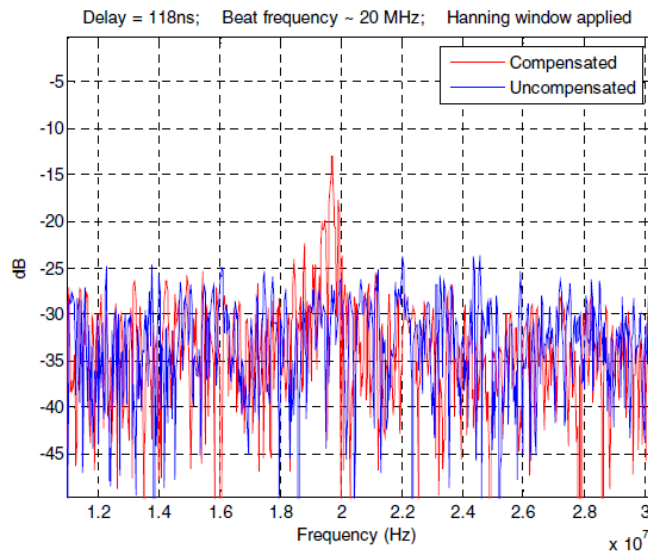
**Figure 4.23 – Uncorrected beat signal and corrected beat signal
using hardware techniques [17]**

Comparing figures 4.22 and 4.23 we find that by using the PLL to correct the

frequency sweep generated by the VCO a focused beat frequency signal is obtained

as opposed to the smeared signal in blue in figure 4.23.

Test is also carried out to differentiate multiple targets. This is done by

splitting the signal in to two paths and making one path longer than other to simulate

two synthetic targets separated by certain distance. To do this at the output of the delay line a power divider is used to split chirp in to two paths using Minibend cables one longer than other and combiner is used to combine the two. This delayed chirp is then mixed with the non delayed chirp to produce beat frequency. The beat-frequency plot for two targets is given figure 4.24.
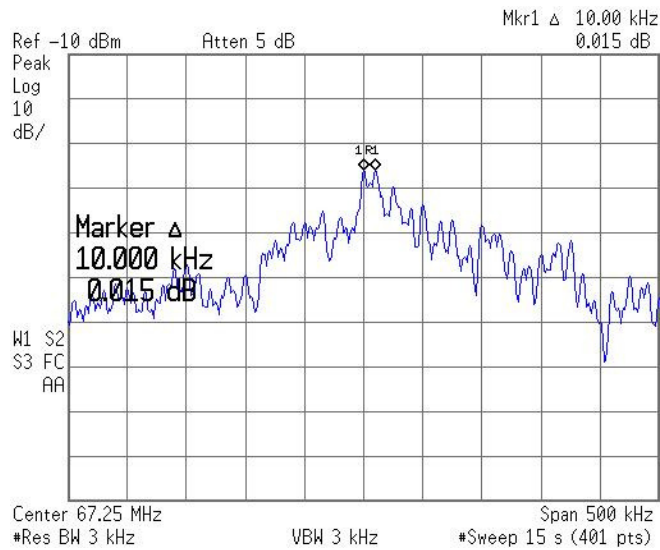
Figure 4.24 Beat frequencies from two synthetic targets

From the figure we see two peaks 10 KHz apart centered at 67.25 MHz. The peaks correspond to two targets that are 3 +/- 0.25 inches apart. The square root of dielectric of the material used is 1.67. The beat-frequency is calculated like in the previous case. The calculated difference in frequency is 9.2 KHz which is very close to what is observed.

Apart from looking at the frequency response of the beat signal data, Hilbert Transform is applied to the data in order to check the linearity in phase. For this the data is divided in to several bands and phase of the beat signal data is calculated from

its Hilbert transform using matlab. The phase data obtained from Hilbert Transform is unwrapped and difference of the phase data is taken. The plot of the difference in the unwrapped phase for one such band is given in figure 4.25.
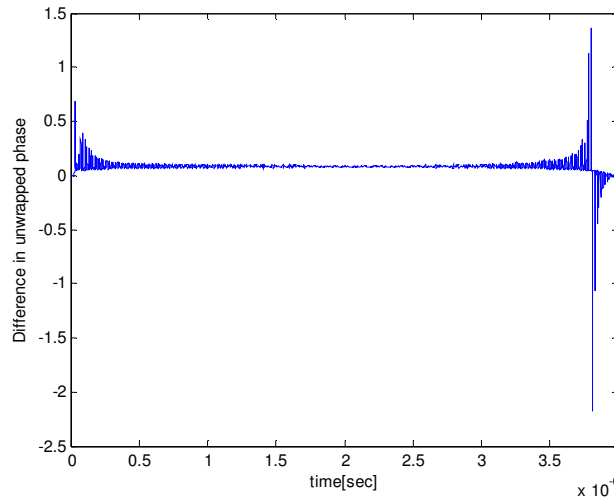
Figure 4.25- Difference in unwrapped phase of the beat frequency data

Mean and Standard deviation is calculated for this difference in phase for each of the bands. The mean and standard deviation for each band of the beat signal data is given below. From the table we can see that it has a constant mean and the standard deviation is fairly small.

Table-4.1 Mean and Standard Deviation for the difference in phase of the beat frequency data

Band	Mean	Standard Deviation
1	0.0844	0.0163
2	0.0844	0.0111
3	0.0845	0.0058
4	0.0844	0.0123
5	0.0844	0.0290

4.9 Implementation of the PLL on PCB

Once the desired results are achieved, a 4-layer PCB was designed to have the entire PLL on one board instead of using several evaluation boards. The PLL PCB accommodated a divide by 8, phase detector w/ integrated 5-bit counter, loop filter, VCO and an amplifier on it. All the components used are surface mount. The top layer is used for routing all the signals. The second layer is the ground plane. The third layer is power plane. It was split into four parts, +5 V analog, +5 V digital, +15 V and -15 V. There is no routing done on the bottom layer. The material used by the board manufacturer is FR4 and the thickness is 62 mils which allowed 25 mils wide trace for 50 ohms line.
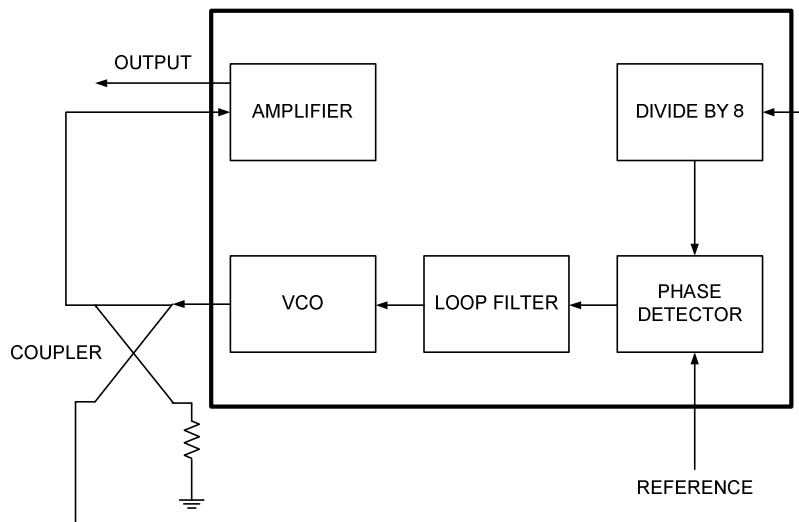
Figure 4.26: Block diagram for PCB

Integrated circuits from Hittite microwave corporation are used for divide by 8, phase detector, VCO and amplifier. Each of the above mentioned components along with the loop filter are organized as shown in the block diagram. An external

reference is given to the phase detector using an SMA connector. The output of the VCO is passed through a coupler outside of the board. The coupled signal is given to the input of the divide down. The through signal is given as an input to the amplifier and the amplified-RF signal is collected using SMA connector. Apart from these couple of more SMA connectors are used on the board for troubleshooting. Jumpers are used to program phase detectors 5-bit counter. And supply connectors are used to bring in the DC supply on the board.

The schematic and the board layout for the PCB are given in Appendix A. Bill of Material is given in Appendix B. Brief description about each of the components is given below

Divide by 8

MMIC from Hittite is used for the divide by 8. It divided the RF signal coming in and produced a digital output whose frequency is divided by 8. Since the input and output to the IC were digital it is placed on the digital side of the board layout.

Phase detector

The phase detector MMIC used had the phase-frequency detector and a 5-bit counter. The 5-bit counter divided the VCO signal coming into the phase-detector. This divide down could be set from 2 to 32 using 5 jumpers. If a jumper is used on the pin then it is pulled to ground i.e. set to '0' otherwise it was set to '1'. Since the inputs and the outputs to the phase detector are also digital. The phase detector is also placed on the digital side of the board.

VCO and Amplifier

The VCO generates an RF chirp in response to the tuning voltage provided by the loop filter. This RF chirp is given to the amplifier which amplified the RF chirp. The VCO and amplifier have analog inputs and outputs therefore these two components are placed on the analog side of the board.

Loop Filter

The loop filter design was same as discussed in chapter 4.

Power distribution and regulation

All the block in the diagram except for the loop filter required a 5 V supply. To achieve this 15 V supply given to the board is regulated down to 5 V. In order to keep the analog and digital signals separate from each other two different regulators are used one for digital and one for analog. The power plane is split into four parts, 5V analog, 5 V digital, +15 and -15. This split is done such that each IC on the board could be provided the required power. The amplifier and the VCO are place analog side of the board and the phase detector and the divide down are placed on the digital side. This is done so that the return currents follow the shortest route to the ground place thus not interfering with each other.

The regulator is chosen based on the current requirements. The VCO and the amplifier together require 190 mA of current and the phase-detector and divide by 8 pulled 353 mA of current. Thus, 1-A regulators are used in the design. An inductor capacitor network is used on either side of the regulator in order to filter out any high frequency component coming from the supply and make the supply quiet. Apart from

the bypass capacitors are placed very close to the supply pins of each of the IC. When theses ICs require quick injection of current these bypass capacitors bypass the supply and provide the large amounts of currents.

Once the PCB design is complete it is sent for manufacturing to Sierra Proto. The manufactured board is tested for continuity. First IC's from Hittite are populated because they have to be reflowed. Then the rest of the components are populated and power connections are given to the board. The board is set up as shown in the figure 4.26. The reference chirp is given using a DDS and the output of the VCO is observed on the spectrum analyzer.

CHAPTER 5 - SUMMARY AND RECOMMENDATIONS

5.1 Summary

When FMCW radar is used to measure the distance to the target or resolve two targets, the nonlinearities in the voltage and frequency relationship of the VCO can have adverse effects on the range measurement. These nonlinearities distort the beat signal thus spreading the target energy over the range of frequencies. There are several schemes to correct the nonlinearities of the VCO for a FMCW Radar. In this thesis nonlinearities of the VCO were corrected in hardware using a fast settling phase lock loop.

In order to generate a linear-transmit chirp a wideband VCO is used in PLL configuration. The phase locked VCO generated 8-12.8 GHz linear transmit chirp. Also in the same set up the 8-12.8 VCO is replaced by a 12-18 GHz VCO since they had the same Kv = 650 MHz/V. Thus, a 12-18 GHz (Ku band) linear transmit chirp was generated.

In order to check the linearity of the transmit chirp generated by the PLL circuitry, beat signal was produced. This was done by using delay line as a synthetic target. The VCO, delay line and analog receiver were set up in FMCW radar configuration. The output of the delay line was treated as received signal which was mixed with the transmit chirp inside the analog receiver. The beat signal thus, generated was captured on oscilloscope and also saved in data format. A hanning window was applied to this data and FFT was applied to observe the beat signal in frequency domain. This beat signal was compared with the beat frequency generated

from uncorrected VCO and VCO whose nonlinearities were corrected using curve tuning. The corrected beat signal frequency response was a nice Sinc with sharp main lobe and lower side lobes when compared to the uncorrected one which was smeared over a range of frequencies. It was also sharper than the one generated using curve tuning and the signal to noise ratio was better than both cases. Thus, the chirp signal generated by the phase locked VCO was fairly linear.

Once the results we expected were achieved using the evaluation boards of various components of PLL. A 4-layer PCB was design to carry entire PLL on a single board. This was done in order to

Apart from the PLL components used in the test set the PCB also included an amplifier to amplifier the chirp signal generated by the phase lock loop.

5.2 Recommendations

Although the PLL designed in this thesis works, modifications can be made in certain areas to achieve better results. The VCO's tuning curve can be characterized and corrected for the nonlinearity. The corrected tuning curve can be saved and a DAC can be used to generate the voltage ramp. This voltage ramp can be amplified to provide the tuning voltage range required by the VCO. In addition to that a correction can be applied by comparing it with a linear reference sweep using a PLL. This can be achieved by including a summer circuit that adds the tune and error voltages.

The other area of the improvement would be board design. The PCB could be designed to have jumper settings to power up individual component of the PLL and SMA connectors to test the outputs of each stage. Thus, each component can be tested individually and trouble shooting becomes easy.

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APPENDIX A: EAGLE SCHEMATIC AND LAYOUT

SCHEMATICS

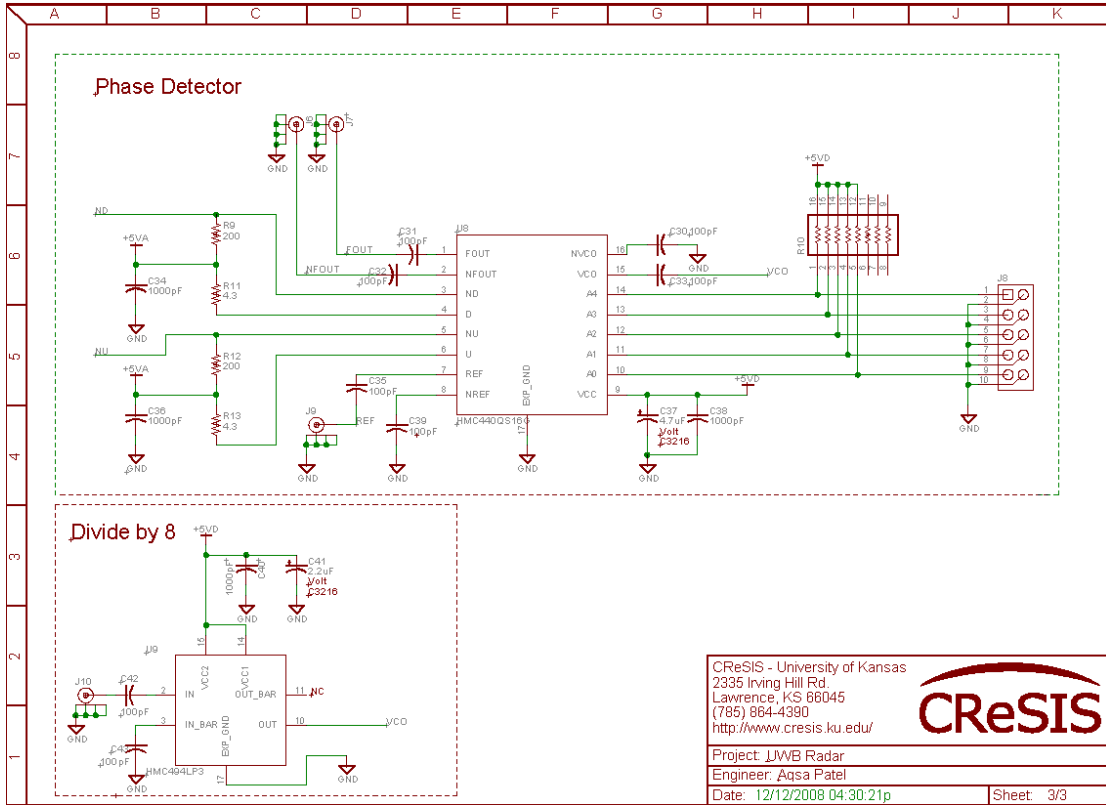Loop Filter

Phase Detector

Divide by 8
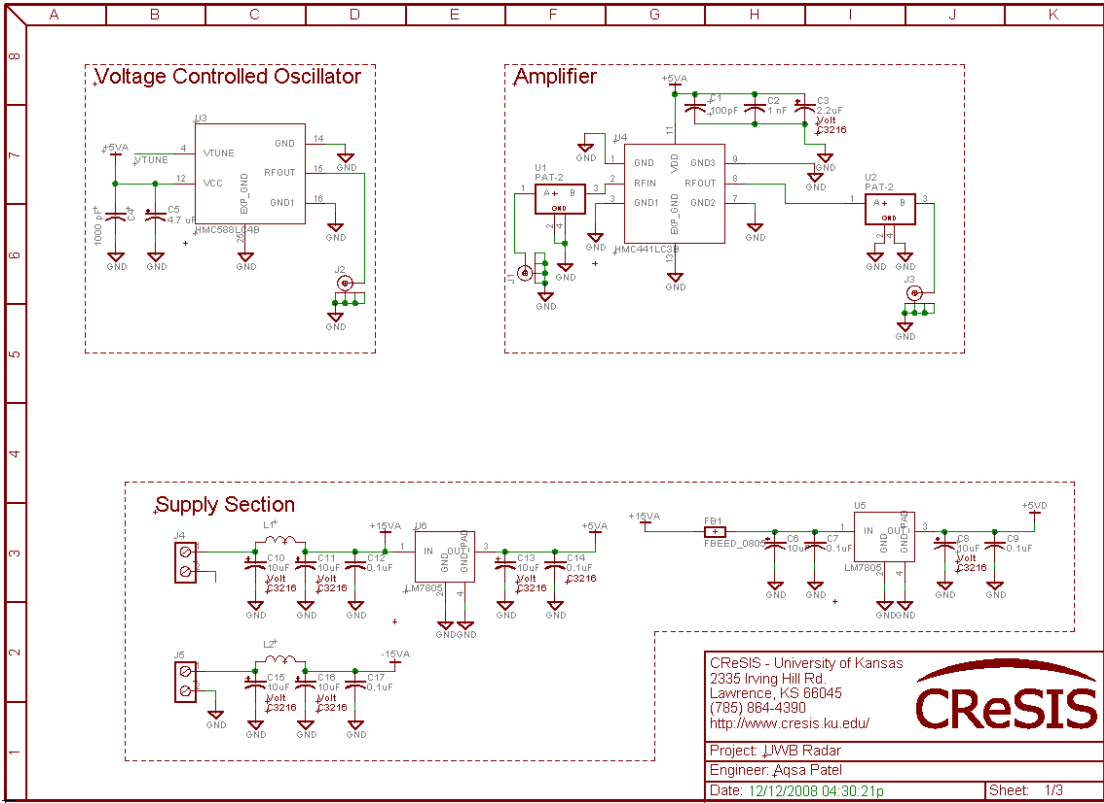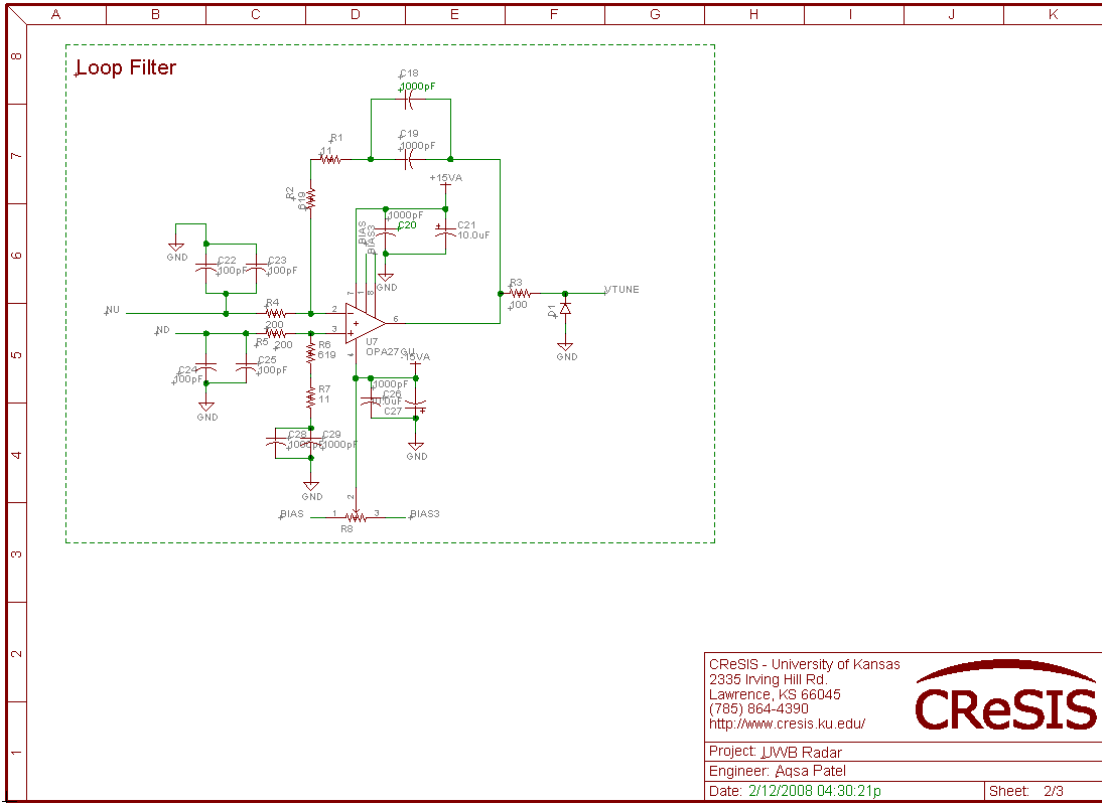
CReSIS - University of Kansas
2335 Irving Hill Rd.
Lawrence, KS 66045
(785) 864-4390
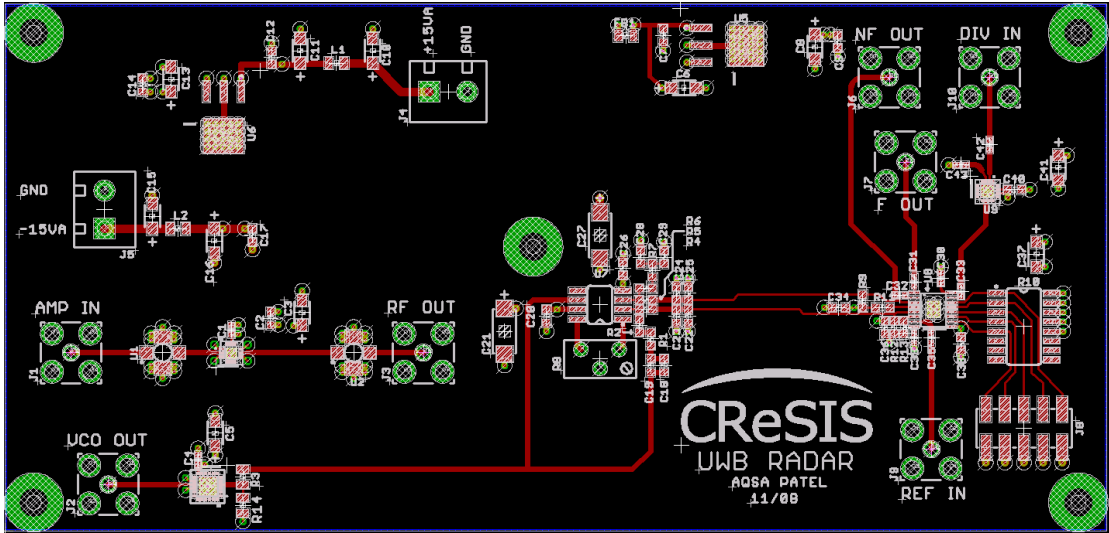http://www.cresis.ku.edu/

Project: UWB Radar
Engineer: Aqsa Patel
Date: 12/12/2008 04:30:21p   Sheet: 3/3

LAYOUT

APPENDIX B - BILL OF MATERIALS

S.No.	Part No.	Description	Quantity	Designator
1	100 pF 0402	100 pF 0402	9	C1, C30, C31, C32, C33, C35, C39, C42, C43
2	1 nF 0603	1 nF 0603	1	C2
3	CT3216	2.2 uF Polarized Capacitor	2	C3, C41
4	1000 pF 0402	1000 pF 0402	1	C4
5	CT3216	4.7 uF Polarized Capacitor	2	C5, C37
6	CT3216	10 uF Polarized Capacitor	8	C6, C8, C10, C11, C13, C15, C16, C17
7	0.1 uF 0603	0.1 uF 0603	4	C7, C9, C12, C14
8	1000 pF 0603	1000 pF 0603	10	C18, C19, C20, C26, C28, C29, C34, C36, C38, C40
9	CT6032	10 uF Polarized Capacitor	2	C21, C27
10	100 pF 0603	100 pF 0603	4	C22, C23, C24, C25
11	100 ohm 0805	100 ohm 0805	1	D1
12	FBEED 0805	Ferrite Beads 0805	1	FB1
13	SMA Connector	SMA Connector Vertical	7	J1, J2, J3, J6, J7, J9, J10
14	Screw Terminal	Screw Terminal	2	J4, J5
15	Pin Header	Pin Header	1	J8
16	0805 Inductor	0805 Inductor	2	L1, L2
17	11 ohm 0603 Resistor	11 ohm 0603 Resistor	2	R1, R7
18	619 ohm 0603 Resistor	619 ohm 0603 Resistor	2	R2, R6
19	100 ohm 0805	100 ohm 0805	1	R3
20	200 ohm 0805	200 ohm 0805 Resistor	2	R4, R5
21	Potentiometer	Potentiometer	1	R8
22	200 ohm 0603	200 ohm 0603	2	R9, R12
23	8 Resistor Network	8 Resistor Network	1	R10
24	4.3 ohm 0603	4.3 ohm 0603	2	R11, R13
25	Pad	PAT family of Pads from Minicircuits	2	U1, U2
26	HMC588LC4B	Hittite VCO	1	U3
27	HMC441LC3B	Hittite VCO	1	U4
28	LM7805	5V Voltage Regulator	2	U5, U6
29	OPA27GU	Op Amp from TI	1	U7
30	HMC440QS16G	Hittite Phase Detector	1	U8
31	HMC494LP3	Hittite Divide by 8	1	U9