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Accepted version. *2016 IEEE Energy Conversion Congress and Exposition (ECCE)* (September 18-22, 2016). DOI. © 2016 IEEE. Used with permission.

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A Fault-Tolerant T-Type Multilevel Inverter Topology with Soft-Switching Capability Based on Si And Sic Hybrid Phase Legs

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Abstract:

The performance of a novel three-phase four-leg fault-tolerant T-Type inverter topology is presented in this paper, which significantly improves the inverter's fault-tolerant capability

regarding device switch faults. In this new modular inverter topology, only the redundant leg is composed of Silicon Carbide (SiC) power devices and all other phase legs are constituted by Silicon (Si) devices. The addition of the redundant leg, not only provides fault-tolerant solution to switch faults that could occur in the T-Type inverter, but also can share load current with other phase legs. Moreover, quasi zero-voltage switching (ZVS) and zero-current switching (ZCS) in the Si Insulated-Gate Bipolar Transistors (IGBTs) of the main phase legs can be achieved with the assistance of SiC Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) in the redundant leg. Simulation and experimental results are given to verify the efficacy and merits of this high-performance fault-tolerant inverter topology.

SECTION I. Introduction

T-Type neutral-point-clamped (NPC) multilevel converters have been regarded as a very promising breed of highperformance power converters in industrial applications. This is because of the relatively lower number of switching devices utilized in their circuit topology and higher efficiency compared with the conventional I-Type NPC converters [1] [2]. However, like other types of multilevel converters, T-Type NPC inverters are not immune to semiconductor device faults. For instance, IGBT open-circuit or short-circuit faults, could potentially cause catastrophic system failures in industrial fields if no fault diagnostic and fault-tolerant solutions are provided. Particularly, the availability of fault-tolerant solutions becomes more critical when such inverters are applied in safety-critical applications, such as Electric Vehicles (EVs), Uninterruptable Power Supplies (UPSs), wind and solar energy conversions, and the like. Although the T-Type NPC inverter has certain inherent fault-tolerant capability due to its unique topology, as reported in [3], the output voltage and linear operating range have to be significantly reduced during fault-tolerant operation, which is not preferred in certain applications (e.g., UPSs, EVs, etc.) where rated output voltage and output power are the stringent requirements. Therefore, it would be of great significance to improve the inverter topology with improved fault-tolerant characteristics, to guarantee full output voltages under post-fault conditions. The existing solutions for the fault-tolerant operation of T-Type inverters are mainly achieved by paralleling multiple redundant inverter legs, such as the topology detailed in [4], which achieves full output voltage under inverter fault-tolerant condition, but at a much higher system cost with decreased inverter efficiency due to a large number of redundant semiconductor devices involved in the circuit. As a matter of fact, most of the redundant semiconductor devices in the existing fault-tolerant topology simply idle in the circuit without contribution to system performance improvement under healthy conditions, which in turn decrease the inverter efficiency due to the associated device losses.

Unlike these existing solutions proposed in the literature [3] [4], a novel three-phase four-leg T-Type inverter topology has been introduced in [5] [6]. This improved topology can not only enhance the fault-tolerant capability of the inverter under faulty conditions, but also can increase the inverter thermal overload capacity as well as achieving soft switching in the IGBT devices. As an extension of [5] [6], this paper will further investigate the three-phase four-leg T-Type inverter with more simulation results and experimental verifications. The remainder content of this paper is organized as follows. In Section II, the fault-tolerant operation characteristics of this new T-Type inverter will be presented for various fault scenarios. In Section III, the soft-switching of the proposed T-Type inverter will be explained. In Section IV and Section V, simulation and experimental results will be demonstrated, respectively, to verify the fault-tolerant operation and the soft-switching capability of the presented T-Type inverter. Finally, conclusions will be given in Section VI.

SECTION II. The Proposed Fault-Tolerant T-Type Inverter

The conventional three-phase three-leg T-Type inverter topology and the proposed four-leg T-Type inverter topology are shown in Fig. 1and Fig. 2, respectively. As can be seen, there is one redundant leg added between the dc bus capacitors and the original T-Type inverter package in the proposed three-phase four-leg inverter as shown in Fig. 2. In this paper, the redundant leg is composed of four SiC MOSFETs, while the original three-leg T-Type inverter package consists of Si IGBT modules. Under normal healthy condition, this redundant leg, marked in yellow shaded area in Fig. 2, outputs zero voltage by keeping the MOSFETs S_2 and S_3 in turn-on state, and shares load current with other phase legs by using the top device (S_1) and bottom device (S_4). Under faulty condition of the inverter, for instance, an open-circuit fault in IGBT S_{a1}, the redundant leg will be utilized to replace the faulty Phase-A leg during fault-tolerant operation. Thus, the whole inverter can still output three-phase voltages without any deratings in the modulation index or voltage amplitude.

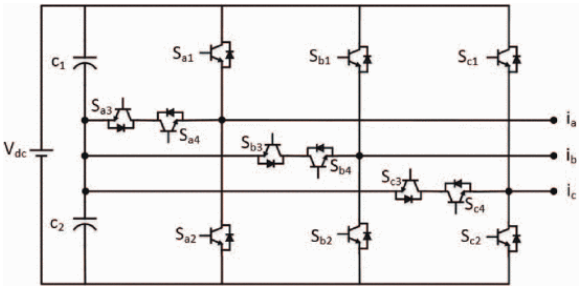

Fig. 1 Conventional three-phase three-level T-type inverter topology.

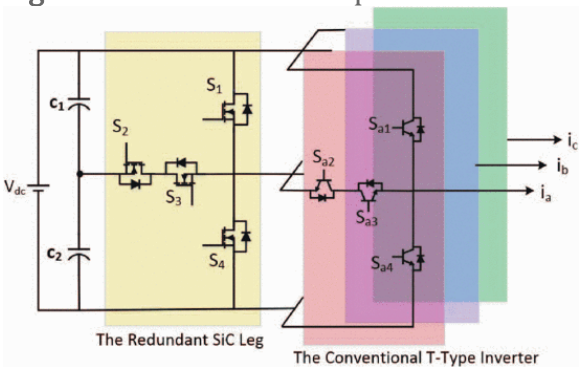

Fig. 2 The proposed fault-fault three-level T-type inverter topology.

Considering the circuit symmetry of the four-leg T-Type inverter, only six cases of device faults are analyzed here to represent all the possible switch fault scenarios that could happen in such a four-leg T-Type inverter. In this paper, only a single device fault is considered for the inverter, and multiple simultaneous device faults is out of the scope here. Although the fault scenario analysis and fault-tolerant solutions discussed below only focus on IGBT devices in the T-Type inverter, they are also applicable for the faults in the related free-wheeling diodes. The fault-tolerant strategy for each fault scenario of the developed T-Type inverter will be detailed next.

A. Case I: Open-Circuit Fault in IGBT S_{a1}

Once an open-circuit fault in IGBT S_{a1} is identified, Phase-A leg of the T-Type inverter will not be able to produce a positive voltage. Under such scenario, IGBT S_{a1} will be replaced by SiC MOSFET S_1 from the redundant phase leg through turning on IGBTs S_{a2} and S_{a3}, while all other SiC MOSFETs (S_2 and S_3) on the redundant leg are turned off, as illustrated in Fig. 3(a). As can be seen,

during such fault-tolerant operation, the three-phase inverter can still output rated voltage, but will have to be modulated as a two-level inverter. Similar fault-tolerant solutions can be applied for open-circuit faults in other IGBTs S_{x1} (where x=b or c) and S_{x4} (where x = a, b, and c). There is no derating required for the modulation index or the output voltages.

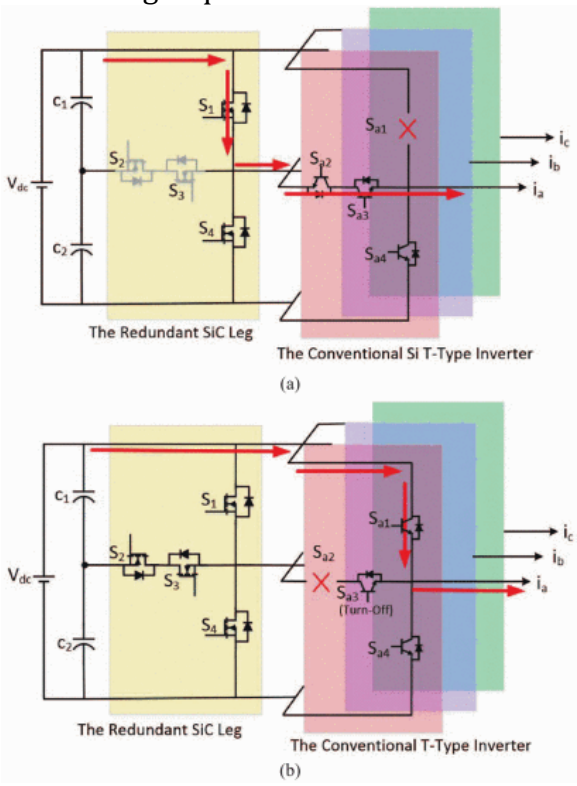

Fig. 3 Current flow during fault-tolerant operation when (a) IGBT S_{a1} has an open-circuit fault (b) IGBT S_{a2} has an open-circuit fault (the devices in grey color refer to turn-off state).

B. Case II: Open-Circuit Fault in IGBT S_{a2}

If an open-circuit fault happens in IGBT S_{a2}, the related faulty leg can only output positive voltage and negative voltage by only using S_{a1} and Sa4 for fault-tolerant operation (the same as the conventional two-level inverter leg), which is due to the loss of the bi-directional switch (constituted by S_{a2} and S_{a3}) accessing the dc-bus middle point for the faulty phase. Under such situation, S_{a3} will be turned off, thus the output of Phase-A leg will be isolated from the dc-bus middle point. However, the other healthy phase legs, namely, Phase-B and Phase-C legs in this case, can still be operated as normal three-level inverter legs. As a result, the line-to-line voltages of the inverter can still exhibit three-level staircase waveforms. There is no derating for the modulation index or voltage output during post-fault operation in this case. Similar fault-tolerant solutions can be applied for open-circuit faults in other IGBTs S_{x2}/S_{x3} in Phase-B and Phase-C legs.

C. Case III: Open-Circuit Fault in the Redudant SiC Leg

It is possible that an open-circuit fault may occur in one of the devices in the redundant SiC phase leg. If the upper/lower SiC MOSFET, S_1 or S_4 has an open-circuit fault, there is no impact on the normal operation of the conventional T-Type inverter. In other words, the original three-phase three-leg T-Type can be still operated as a normal three-level inverter. However, if the middle SiC MOSFETs, S_2 or S_3, have an open-circuit fault, the T-Type inverter has to be modulated as a conventional two-level inverter, which is due to the loss of access to the dc-bus neutral point

through S_2 and S_3. Nevertheless, under such fault condition, no deratings are required on the output voltages.

D. Case IV: Short-Circuit Fault in IGBT S_{a2}

If a short-circuit fault in IGBT S_{a2} is determined, its complimentary switch S_{a3} has to be switched off due to the loss of reverse blocking capability. Accordingly, all the switches in the redundant phase leg should be turned off. Under such scenario, the three-level T-Type inverter will be operated as a conventional two-level inverter by only using S_{x1} and S_{x4} for the post-fault operation. A similar fault-tolerant strategy can be applied for short-circuit faults in IGBTs S_{x2} (where, $x = b$ or c) and S_{x3} (where, x = a, b, or c).

E. Case V: Short-Circuit Fault in the Redundant SiC Leg

If there is any single short-circuit fault occurring in the redundant SiC phase leg, all the other SiC MOSFETs in the redundant leg have to be switched off in case of shorting the dc-bus capacitors. For instance, if S_1 or S_4 has a short-circuit fault, the middle SiC switches (S_2 and S_3) have to be turned off immediately. Correspondingly, the T-Type inverter has to be modulated as a two-level inverter due to the loss of access to the dc-bus middle point. However, if the SiC MOSFET, S_2, or S_3, has a short-circuit fault, there is no impact on the normal operation of the inverter, since access to the dc-bus neutral point is still available. However, under such scenario, S_1 and S_2 should be turned off in case of shorting the dc bus capacitors.

In summary, this developed T-Type inverter can tolerate any open-circuit faults and certain short-circuit faults that could occur in the devices of the inverter. For any of the aforementioned device faults, there is no derating required for the modulation index or output voltage during the fault-tolerant operating region of the inverter. However, such an inverter has to be modulated as a two-level one under some of these fault conditions, which implies a slightly higher harmonic distortion in the output currents and voltages compared to those under three-level healthy operation.

SECTION III. Quasi ZVS and ZCS Soft Switching

Almost all of the existing fault-tolerant converter topologies in the literature achieve the fault-tolerant capability at the cost of decreased efficiency due to commutation of many redundant switching devices. However, one unique feature of the fault-tolerant topology presented in this paper is the soft- switching characteristics for IGBT devices assisted by the SiC devices in the redundant leg. Specifically, the presence of the redundant SiC leg (shown in Fig. 2), provides a quasi-ZVS and ZCS switching strategy for the IGBT switching in the original T-Type inverter, which will be elaborated as follows.

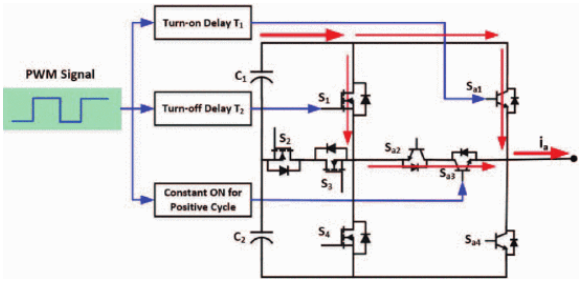

Fig. 4 Quasi ZVS and ZCS switching strategy during positive output voltage of the phase-A leg of the T-type inverter at positive output current condition.

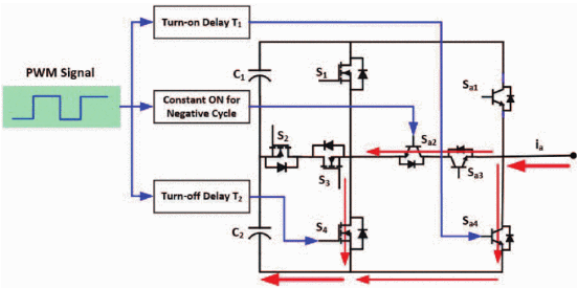

Fig. 5 Quasi ZVS and ZCS switching strategy during negative output voltage of the phase-A leg of the T-type inverter at negative output current condition.

It is well known that SiC MOSFETs have much lower switching losses than their counterpart Si IGBTs. Therefore, when the redundant SiC leg is assigned to share the overload current with other main legs, the SiC MOSFETs S_1/S_4 and the bi-directional Si IGBTs (S_{x2}/S_{x3}) are switched on prior to the turn-on of the upper/lower Si IGBTs (S_{x1}/S_{x4}), in order to provide a very low on-state voltage for the subsequent switching-on (i.e., quasi-ZVS) of the Si IGBTs (S_{x1}/S_{x4}). However, during the turning-on of SiC S_1/S_4 and Si S_{x2}/S_{x3} devices, S_{x2}/S_{x3} should be turned on first at zero switching current (ZCS), and the SiC S_1/S_4 will be turned on later after a short delay to withstand the switching losses. Similarly, regarding the switching-off of the parallel legs, the upper/lower switches Si S_{x1}/S_{x4} are turned off prior to the redundant switches SiC MOSFETs (S_1/S_4) and bi-directional switches Si IGBTs (S_{x2}/S_{x3}) for achieving quasi-ZVS soft switching. Then, during the switching off of the MOSFETs (S_1/S_4) and bi-directional switches IGBTs (S_{x2}/S_{x3}), SiC MOSFETs (S_1/S_4) are switched off first to interrupt the large load current, and accordingly the subsequent switching-off of the Si IGBTs (S_{x2}/S_{x3}) will experience a ZCS switching. Such ZCS and ZVS switching sequence is illustrated in Fig. 4 and Fig. 5, which would significantly reduce the IGBT switching losses in the T-Type inverter. More details about the ZVS switching pattern were introduced in [5]–[6][7][8][9].

SECTION IV. Simulation Results

In this section, simulation results on the fault-tolerant operation of the new three-phase four-leg T-Type inverter will be given under various fault scenarios. Also, the simulation analysis on the soft-switching operation of the IGBT devices assisted by the SiC MOSFETs in the redundant phase leg will be provided as well.

A. PWM Strategy

In this paper, the PWM strategy used for the developed fault-tolerant T-Type inverter is SVPWM, which is implemented by injecting a zero-sequence signal into the sinusoidal reference signals. Assuming that the duty ratio for each phase of the T-Type inverter can be written as follows:

$$\begin{cases} d_a = m_a \cos(\theta) \\ d_b = m_a \cos(\theta - 2\pi/3) \\ d_c = m_a \cos(\theta - 4\pi/3) \end{cases} \quad (1)$$

where, m_a, is the amplitude modulation index, and θ is the initial phase angle. It follows that the instantaneous maximum and minimum duty ratio will be:

$$d_{max} = max(\mathrm{d_a}, \mathrm{d_b}, \mathrm{d_c})$$
$$d_{min} = min(\mathrm{d_a}, \mathrm{d_b}, \mathrm{d_c}) \quad (2)(3)$$

The injected zero-sequence signal is defined as:

$$d_0 = -(d_{max} + d_{min})/2 \quad (4)$$

With the injection of such a zero-sequence signal, the duty ratio for each phase of the T-Type inverter under SVPWM can be written as:

$$\begin{cases} \mathrm{d_{a,SV}} = \mathrm{m_a}\cos(\theta) + \mathrm{d_0} \\ \mathrm{d_{b,SV}} = \mathrm{m_a}\cos(\theta - 2\pi/3) + \mathrm{d_0} \\ \mathrm{d_{c,SV}} = \mathrm{m_a}\cos(\theta - 4\pi/3) + \mathrm{d_0} \end{cases} \quad (5)$$

B. Fault-Tolerant Operation

Simulations for different fault scenarios and their associated fault-tolerant operation are carried out in PLECS software environment, and the simulation results are given in Figs. 6(a)–(d). In Fig. 6(a), the three-phase currents and line-to-line voltage (V_{ab}) waveforms under healthy condition, $\mathrm{S_{a1}}$ open-circuit faulty condition, and the related fault-tolerant operation are demonstrated, which is consistent with the analysis in Case I of Section II. As can be seen, during the open-circuit faulty operation of the inverter (between $t = 0.05$ sec and $t = 0.1$ sec), the line-to-line voltage V_{ab} and the Phase-A current ia lose part of the positive cycle, which is due to the open-circuit fault occurring in $\mathrm{S_{a1}}$ resulting in no access to the positive dc-bus at positive current for Phase-A leg. However, as mentioned in Case I of Section II, the faulty device $\mathrm{S_{a1}}$ can be replaced by the upper device $\mathrm{S_1}$ in the redundant leg to achieve fault-tolerant operation, as shown in the simulation results between $t = 0.1$ sec and $t = 0.15$ sec in Fig. 6(a). It can be observed that the harmonic distortion in the phase currents during fault-tolerant operation is slightly higher compared to that in normal healthy stage, which is caused by the two-level voltage output of the inverter.

The phase currents and line-to-line voltage waveforms under $\mathrm{S_{a2}}$ open-circuit faulty condition are shown in Fig. 6(b). It can be observed that the line-to-line voltage (V_{ab}) still exhibits three-level waveform during fault-tolerant operation (between t=0.1 sec and t=0.15 sec), as analyzed in Case II of Section II. The simulation results for $\mathrm{S_2}$ open-circuit and $\mathrm{S_{a2}}$ short-circuit fault scenarios are shown in Fig 6(c) and (d), respectively, which are consistent with the analysis in Case-III and Case-IV of Section II. It can be seen that the developed fault-tolerant T-Type inverter can output full voltage and current during post-fault operation for any of the device open-circuit faults and certain short-circuit faults.

C. Quasi ZVS and ZCS Operation

Simulation results that demonstrate the ZVS operation of the IGBT $\mathrm{S_{a1}}$ in Phase-A leg of the T-Type inverter are given in Fig. 7. As can been seen, if the IGBT $\mathrm{S_{a1}}$ is switched off prior to the SiC MOSFET $\mathrm{S_1}$, a quasi ZVS operation will be achieved for $\mathrm{S_{a1}}$ due to the near-zero voltage across $\mathrm{S_{a1}}$. The low turn-off voltage value of the $\mathrm{S_{a1}}$ is determined by the on-state voltages of three devices, namely, $\mathrm{S_1}$, $\mathrm{S_{a3}}$and $\mathrm{D_{a2}}$ (anti-parallel diode of $\mathrm{S_{a2}}$), which can be expressed as follows:

$$V_{turn-off(sa1)} = V_{on(S1)} + V_{on(Sa3)} + V_{on(Da2)} \quad (6)$$

where, $V_{turn-off(sa1)}$ refers to the turn-off voltage across S_{a1}, which is typically several volts. $V_{on(S1)}$, $V_{on(Sa3)}$, and $V_{on(Da2)}$ refer to the on-state voltage of the SiC MOSFET S_1, and IGBT S_{a3}, and the free-wheeling diode D_{a2}, respectively.

Also, the load current sharing between the Phase-A leg and the redundant leg under normal conduction mode is also depicted in Fig. 7. Specifically, the current sharing ratio between S_1 and S_{a1} is determined by the resultant on-state resistance of the two conduction paths. If defining the current through S_1 and S_{a1} as I_{s1} and I_{sa1}, respectively, the current sharing in-between can be expressed as follows:

$$\frac{I_{S1}}{I_{sa1}} = \frac{R_{on(Sa1)}}{R_{on(S1)}+R_{on(Sa3)}+R_{on(Da2)}} \quad (7)$$

where, $R_{on(Sa1)}$, $R_{on(S1)}$, $R_{on(Sa3)}$ and $R_{on(Da2)}$ refer to the on-state resistance of devices S_{a1}, S_1, S_{a3}, and D_{a2}, respectively.

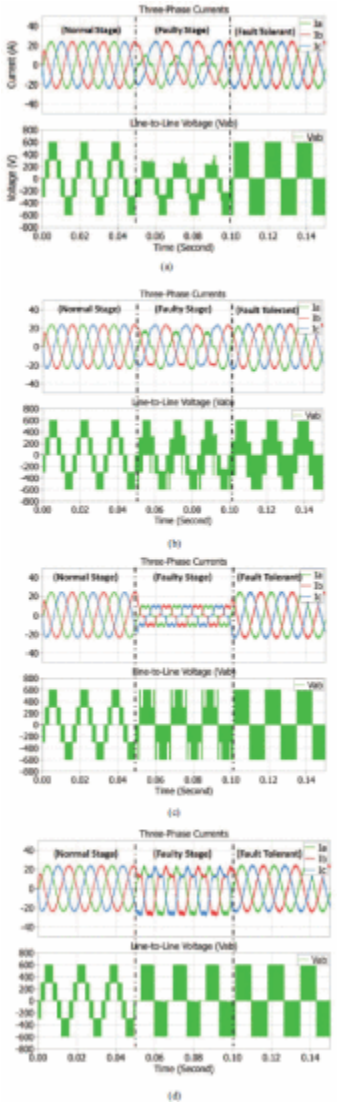

Fig. 6 Simulated three-phase currents (i_a, i_b, and i_c) and line-to-line voltage (V_{ab})during normal operation, faulty operation, and fault-tolerant operation under the conditions of (a) open-circuit

fault in S_{a1}, (b) open-circuit fault in S_{a2}, (c) open-circuit fault in S_2 of the redundant leg and (d) short-circuit fault in S_{a2} of the phase-A leg.

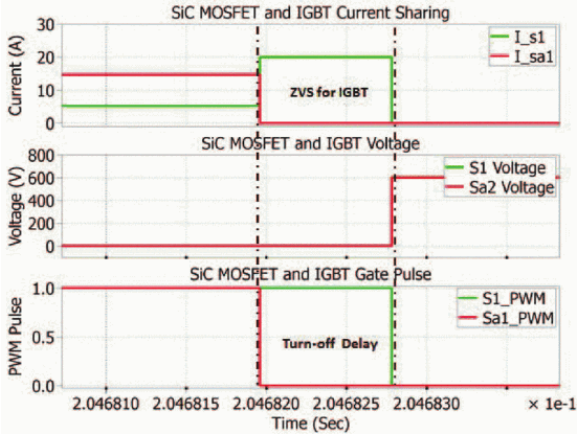

Fig. 7 Current sharing and ZVS switching between SiC MOSFET (S_1) and IGBT (S_{a2}) under positive output voltage and positive output current condition of the T-type inverter.

SECTION V. Experimental Verifications

In order to verify the fault-tolerant operation characteristics, soft switching, and the load current sharing of this developed three-phase four-leg T-Type inverter, a 20-kW adjustable speed drive (ASD) based on this novel inverter topology has been implemented in the laboratory, as shown in Fig. 8. A Fuji T-Type IGBT module (12-in-one package) 12MBI50VX-120-50 (1200V/50A) is used in the prototype to constitute the conventional 3-phase 3-level T-Type inverter. The redundant SiC phase leg is built based on using the SiC MOSFET devices from Wolfspeed C2M0025120D (1200V/60A), with an external anti-parallel SiC Schottky diode connected. All the main operating parameters of the ASD prototype are given in Table-I.

In the experiments, the inverter was connected to a wye-type three-phase resistive-inductive (RL) load. The output fundamental frequency is 60 Hz, and the switching frequency of the inverter is set as 5 kHz. Open-circuit faults are emulated by disabling the PWM signals of the switching devices. The experimental results given in Fig. 9(a)–(d) verified the fault-tolerant capability of this three-phase four-leg T-Type inverter for four representative fault scenarios, namely, open-circuit fault in S_{a1}, open-circuit fault in S_{a2}, open-circuit fault in S_2, and short-circuit fault in S_{a2}. In these test results the first three cycles refer to the normal/healthy operation, the following three cycles exhibit the open-switch faulty operation with distorted currents and voltages, and the last three cycles demonstrate the fault-tolerant operation under the assistance of the redundant leg. It can be seen that the there is no magnitude derating in the output voltages and currents during the fault-tolerant operation stages. Also, it can be observed that the total harmonic distortion (THD) in the phase currents under fault-tolerant operation is slightly higher than these under healthy condition, which is due to the two-level voltage output in the faulty phase leg. All the experimental results given in Fig. 9(a)–(d) are consistent with the simulation results provided in Fig. 6(a)–(d).

Table I System parameters of the 20-kW adjustable speed drive prototype based on the proposed T-type inverter

Parameter	Value
DC-bus voltage	600V
Rated power	20kW

Seitching Frequency	5kHz
Output Fundamental Frequency	60Hz
Modulation Index	0.8
Load Resistance Per Phase	10Ω
Load Inductance Per Phase	500μH

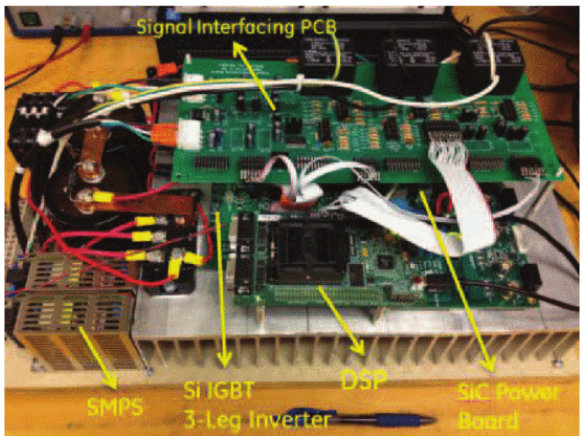

Fig. 8 A 20-kW three-phase ASD prototype based on the proposed three-phase four-leg T-type inverter topology with Si and SiC hybrid phase legs.

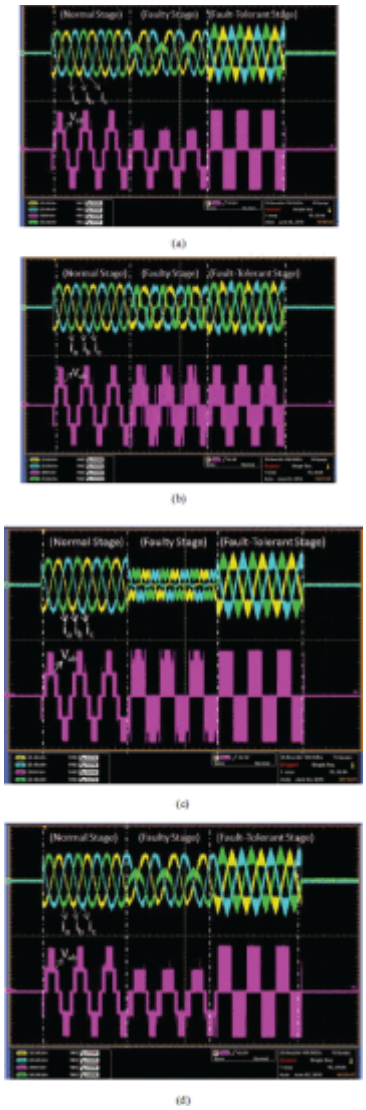

Fig. 9 Measured three-phase currents (i_a, i_b, and i_c) and line-to-line voltage (V_{ab}) during normal operation, faulty operation, and fault-tolerant operation under the conditions of (a) open-circuit fault in S_{a1}, (b) open-circuit fault in S_{a2}, (c) open-circuit fault in S2 of the redundant leg and (d) short-circuit fault in S_{a2} of the phase-A leg.

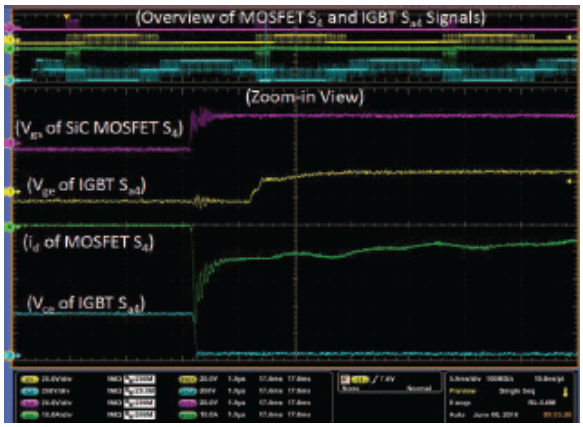

Fig. 10 Measured switching waveforms of SiC MOSFET S_4 and Si IGBT S_{a4} during negative load current.

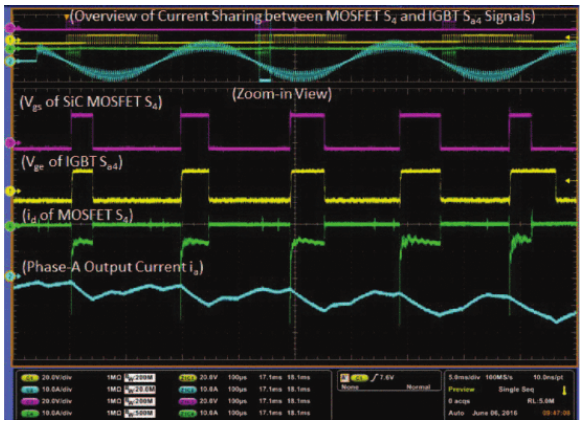

Fig. 11 Measured SiC MOSFET gate voltage and drain current as well as the phase-A output load current waveforms of the proposed fault-tolerant T-type inverter.

SECTION VI. Conclusions

This paper introduced a fault-tolerant high-efficiency three-phase three-level inverter topology based on a conventional T-Type inverter. According to the analysis, simulation and experimental results presented above, a few conclusions can be drawn as follows:

1. The presented fault-tolerant inverter topology provides improved fault-tolerant solutions to device open-circuit and short-circuit faults in the T-Type inverters. During post-fault operation of any of the aforementioned device faults, the inverter is still able to output the same maximum and rated voltage/power as that under normal operation. In other words, no derating is required during fault-tolerant operation. Although the harmonic distortions in the phase currents are slightly increased during some of the fault-tolerant operation mode due to the two-level modulation, the reliability improvement of the T-Type inverter are much more preferred, especially in safety-critical applications.
2. By adopting a quasi-ZVS and ZCS strategy through the utilization of the SiC MOSFETs in the redundant phase leg, the pronounced switching losses in the IGBTs of the original T-Type inverter can be significantly reduced.
3. Under normal healthy condition, the redundant SiC inverter leg helps share the load current with the original T-Type inverter legs, and therefore can enhance the inverter thermal overload capability. Since a normal T-Type inverter exhibits the waveforms of the output voltages as a conventional two-level inverter under low modulation indices ($Ma \leq 0.5$), there is no penalty in harmonic distortion in the output voltages under such scenario. Moreover, the redundant leg can also be utilized for load current sharing at high modulation indices ($Ma \leq 0.5$) to relieve large thermal stress on main switches (S_{x1}/S_{x4}), but the harmonic distortion in the output voltages will be slightly higher compared to these voltage output from a three-level modulation.
4. This three-phase four-leg fault-tolerant T-Type inverter has a very modular structure, and therefore very suitable for power module packaging and manufacturing, which will make the commercialization of such power modules more feasible.

ACKNOWLEDGMENT

The authors would like to express thanks to the U.S. National Science Foundation (NSF) for the partial financial support for

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