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Fabrication of 3D Surface Structures Using Grayscale Lithography

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Abstract

The ability to design and develop 3D microstructures is important for microelectromechanical systems (MEMS) fabrication. Previous techniques used to create 3D devices included tedious steps in direct writing and aligning patterns onto a substrate followed by multiple photolithography steps using expensive, customized equipment. Additionally, these techniques restricted batch processing and placed limits on achievable shapes. Gray-scale lithography enables the fabrication of a variety of shapes using a single photolithography step followed by reactive ion etching (RIE). Micromachining 3D silicon structures for MEMS can be accomplished using gray-scale lithography along with dry anisotropic etching. In this study, we investigated: using MATLAB for mask designs; feasibility of using 1 µm Heidelberg mask maker to direct write patterns onto photoresist; using RIE processing to etch

patterns into a silicon substrate; and the ability to tailor etch selectivity for precise fabrication. To determine etch rates and to obtain desired etch selectivity, parameters such as gas mixture, gas flow, and electrode power were studied. This process successfully demonstrates the ability to use gray-scale lithography and RIE for use in the study of micro-contacts. These results were used to produce a known engineered non-planer surface for testing micro-contacts. Surface structures are between 5 µm and 20 µm wide with varying depths and slopes based on mask design and etch rate selectivity. The engineered surfaces will provide more insight into contact geometries and failure modes of fixed-fixed micro-contacts.

1. INTRODUCTION

The ability to develop 3D micro-structures is of great importance for increasing optical and electro-mechanical device performance. Previous technologies used multiple direct writing and photolithography steps, or customized equipment.[1,2,3] However, these technologies are restricted to a limited range of shapes and do not utilize batch processing cannot be utilized. Gray-scale technology has emerged enabling the development of arbitrary 3D micro-structures in various materials.[3,4,5] Use of gray-scale technology allows 3D shaping of silicon to be performed in a single photolithography step with subsequent dry etching.[6]

Gray-scale lithography utilizes an optical mask patterned with varying intensities of gray pixels and spacing in Matlab. This optical mask combined with laser lithography allows a uniform intensity on the photoresist surface across the pattered region. Changing the size of the pattern and color of the gray, changes the intensity of the laser power; with each distinct power level given a gray level. The height profile in the photoresist after development (composed of photoresist gray levels) will depend upon the incident intensity, time of exposure, and photoresist contrast.

Gray-scale optical masks were designed and developed for a Heidelberg Mask Maker to produce various structures in positive photoresist for characterization of the profile. The gray levels were patterned on the optical mask by varying the size of structures. Due to machine limitations, only 100 of the 255 gray color variations are used to produce 100 unique height levels exist within the chosen method of patterning, yielding a stepped profile in the photoresist.[7]

Also included on the optical masks were features to measure non-uniformity in the photoresist: fully exposed level heights and a conventional opaque region (no exposure). These features will give information on the uniformity of the photoresist spinning, where the gray level features include non-uniformity coming from all steps: photoresist spinning, exposure, and development.[1]

2. IMAGE CREATION

The first attempt at gray-scale lithography utilizing Matlab to create a gray-scale image, the first of the images can be seen in **Figure 1**. However, Matlab saved the image as a color. bmp format that resulted in blue-gray hues at different levels. These blue-gray hues caused an issue in the first test files that led to errors when writing into the photoresist, as shown in **Figure 2**. It was discovered that exporting the image into another program and saving in the correct format, a 24-bit bitmap image, fixed the error. What is also seen in this image is the border which should be fully exposed is not.

Figure 1. Image showing first 2D pyramid pattern attempted, this format of. bmp file, directly from Matlab, created blue-gray hues rather than only a gray-scale image.

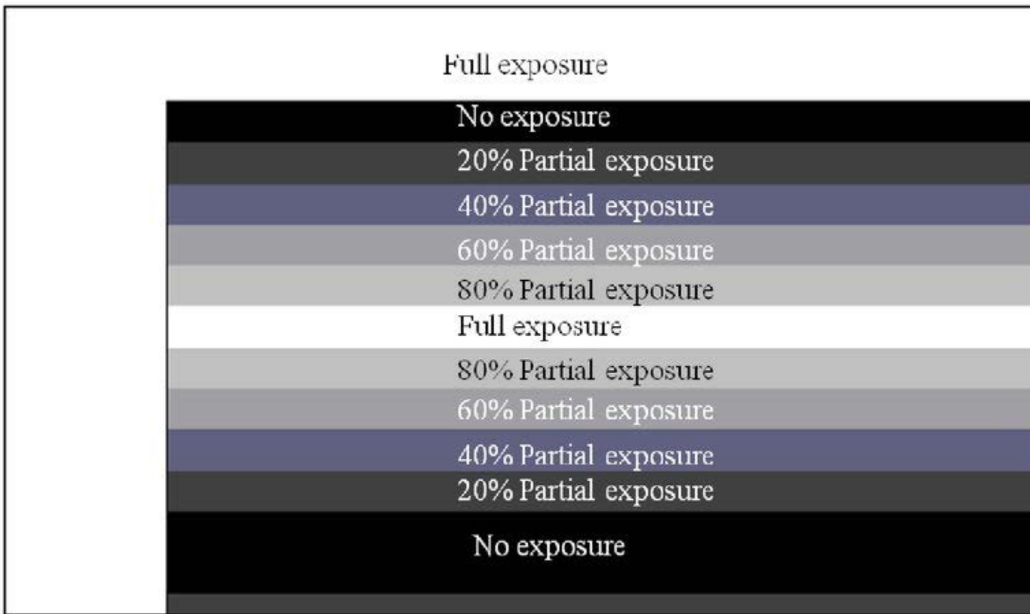
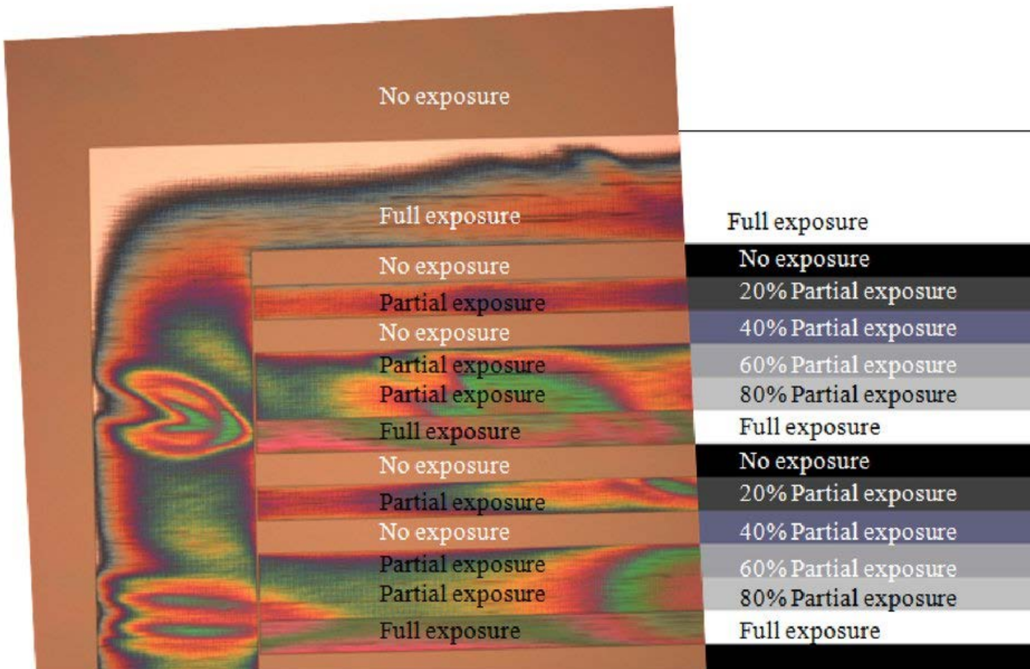


Figure 2. Image showing the caparison of the blue-gray hue with the resulting image in 1818 photoresist, this should be a step down from full height of photoresist down to no photoresist.



3. DIRECT WRITING INTO PHOTORESIST

Test were conducted to find the required power and exposure levels. This study was needed because the incorrect power level could lead to over or under exposure of the photoresist. After some testing it was found that a 14mW power at 10% allowed for exposure of 1.9 µm. Although this exposure power should be enough to fully expose the 1818 photoresist, due to colder than ideal temperatures, it was found that on some samples the power levels were too low to fully expose all of the photoresist.

3.1 Ramp pattern

Ramp design consisted of a ramp up from the substrate to max height, then immediately dropping back down to the substrate to start the ramp up again. This mimicked the layout of stepped ramp, thus the name “ramp”. **Figure 3**(a) shows an example of this type of pattern in Matlab and the result of the direct write and (b) is the expected cross-section of the design. **Figure 4** shows the surface profile measurement of this step function.

Figure 3. Ramp example (a) left is the Matlab image, right is the result of the direct write into 1818 photoresist, (b) is the expected cross-section of the designed along the line b-b.

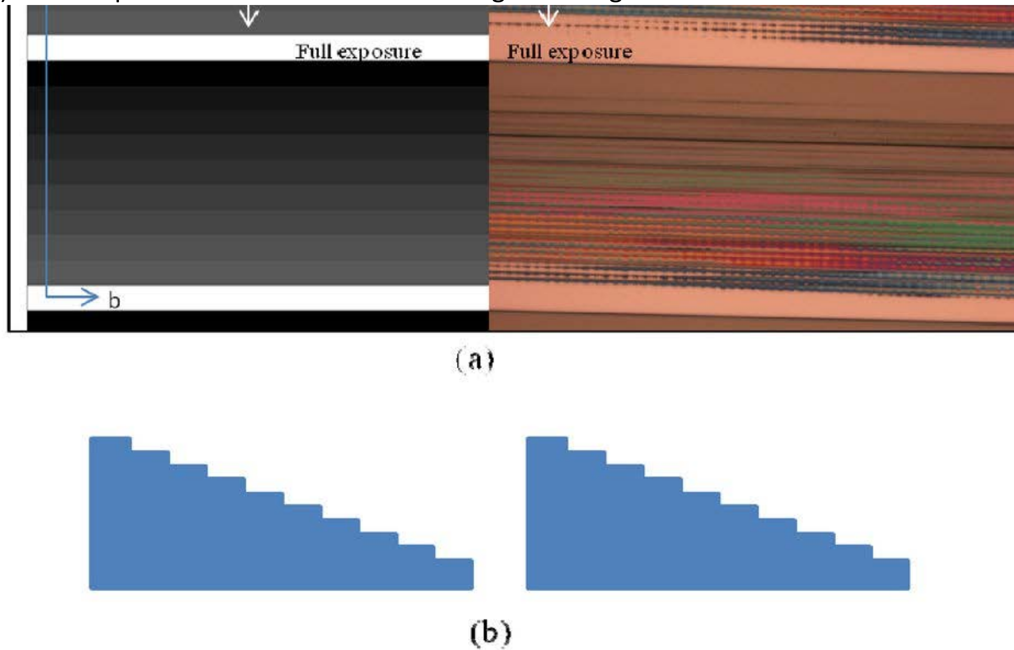
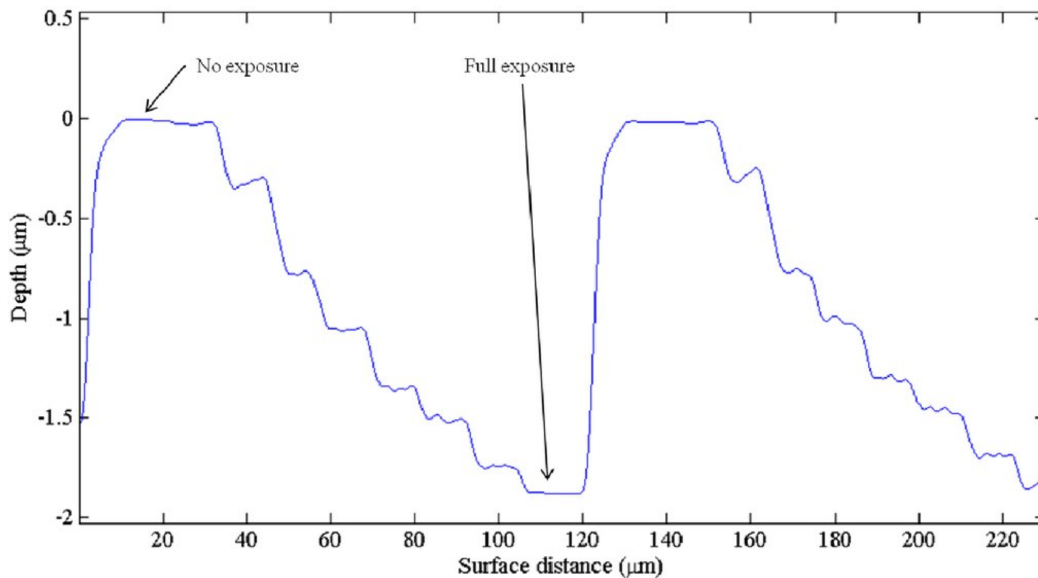


Figure 4. Surface profile plot of the ramp pattern created in **Figure 3** along cross-section b-b.



3.2 2D pyramid pattern

The 2D pyramid is a pattern that ramps up and down from the substrate, which creates a profile structure that looks like 2D pyramid. The profile was developed in Matlab to create a gray-scale image of varying line widths and steps. An example of this can be seen in **Figure 5**.

Figure 5. 2D pyramid example (a) left is the Matlab image, right is the result of the direct write into 1818 photoresist, (b) is the expected cross-section of the designed along the line b-b.

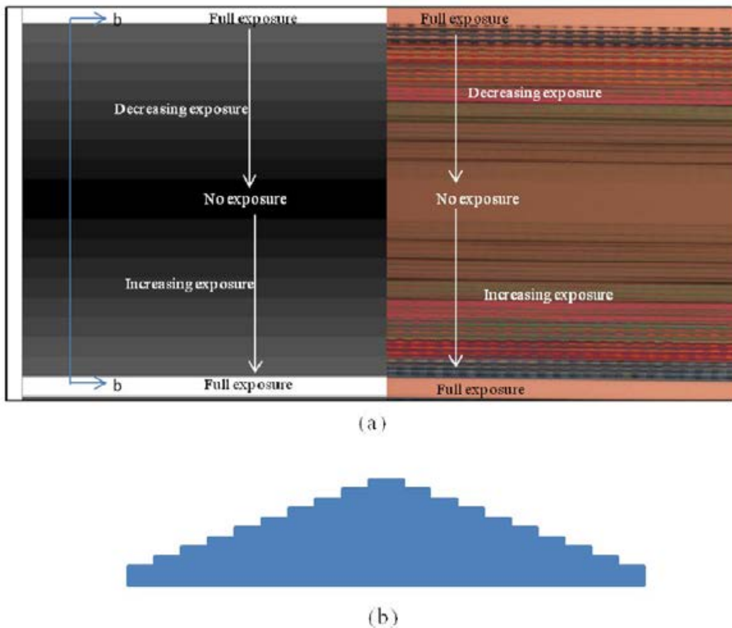
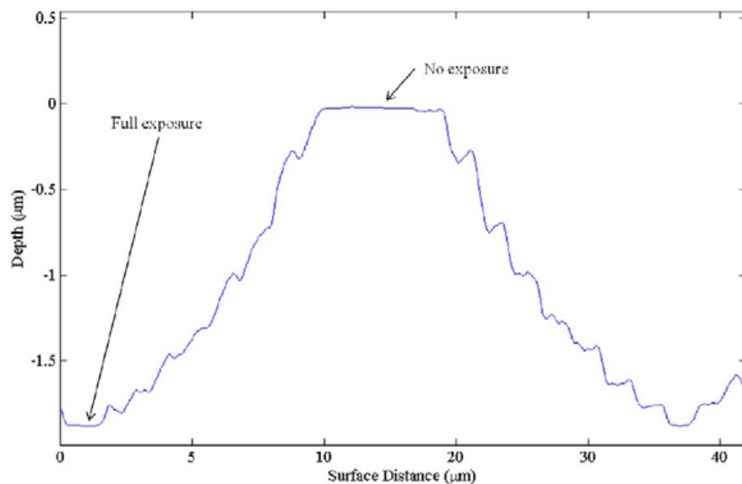


Figure 6. Plot of the 2D pyramid surface profile from the image in **Figure 5** along cross-section b-b.



3.3 3D Pyramid and Dip patterns

Additional variations that were created include a 3D pyramid and a dip pattern. Pyramids were created by ramp ramping from the substrate in the X and Y direction up to the full photoresist height, then ramp back down to the substrate. This pattern could be used to create a lower contact bump or bumps for the lower contact depending on the size and spacing of the pyramids. The dip is the opposite of the 3D pyramid, the structure is a ramp down in the X and Y direction from full photoresist to the substrate or a hole that could capture the upper hemispherical contact.

Figure 7. Example of the 3D pyramid structure created in photoresist. The 3D pyramid is formed by the stepping of fully exposed photoresist up to the top of the pyramid that is unexposed.

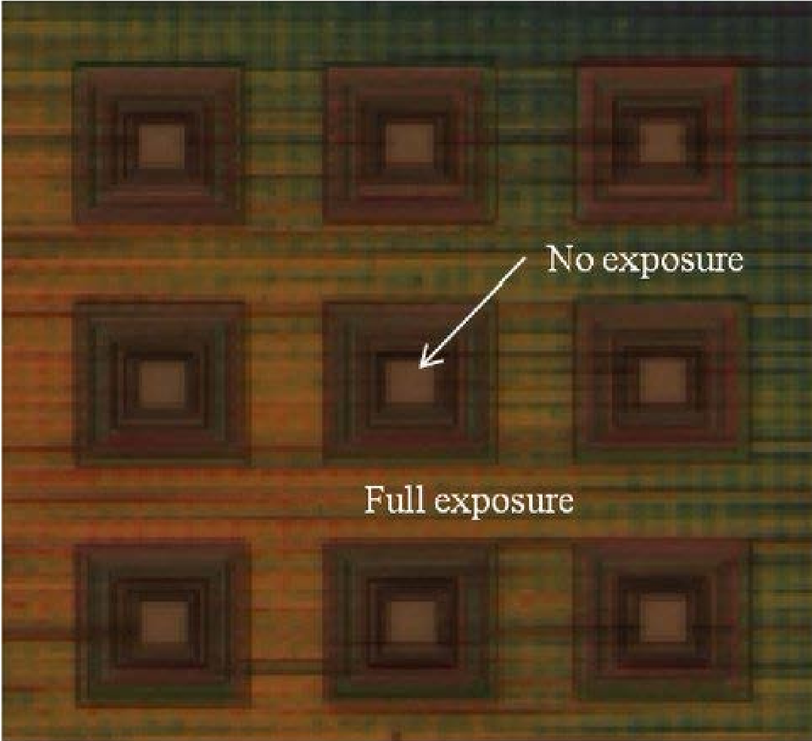
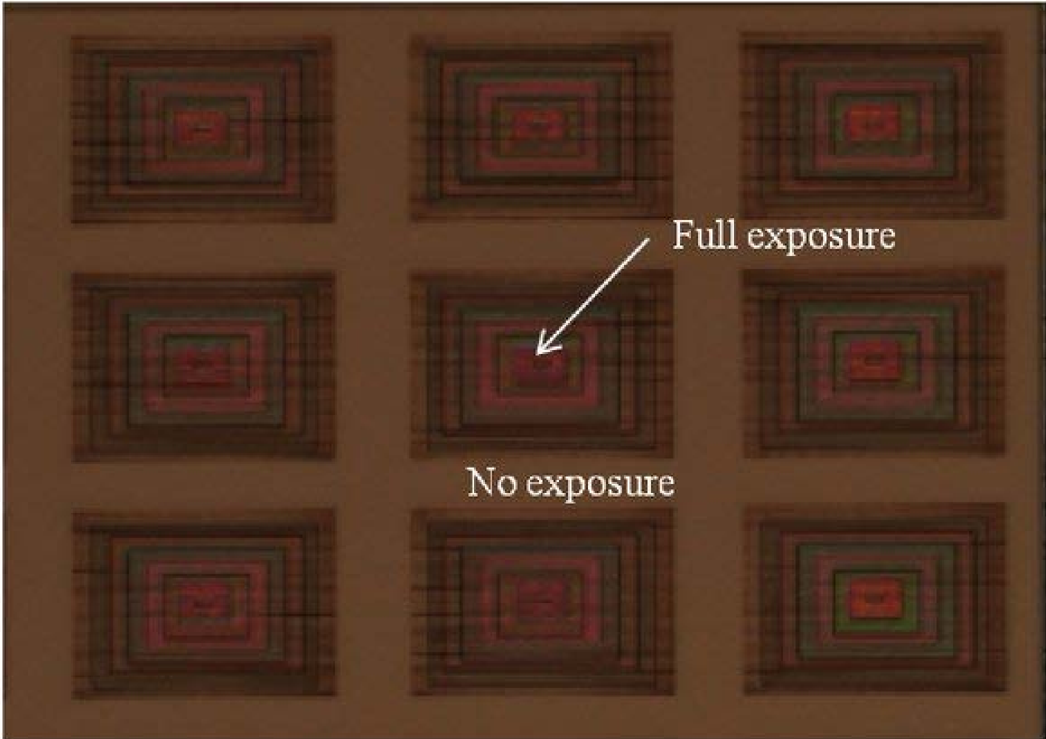


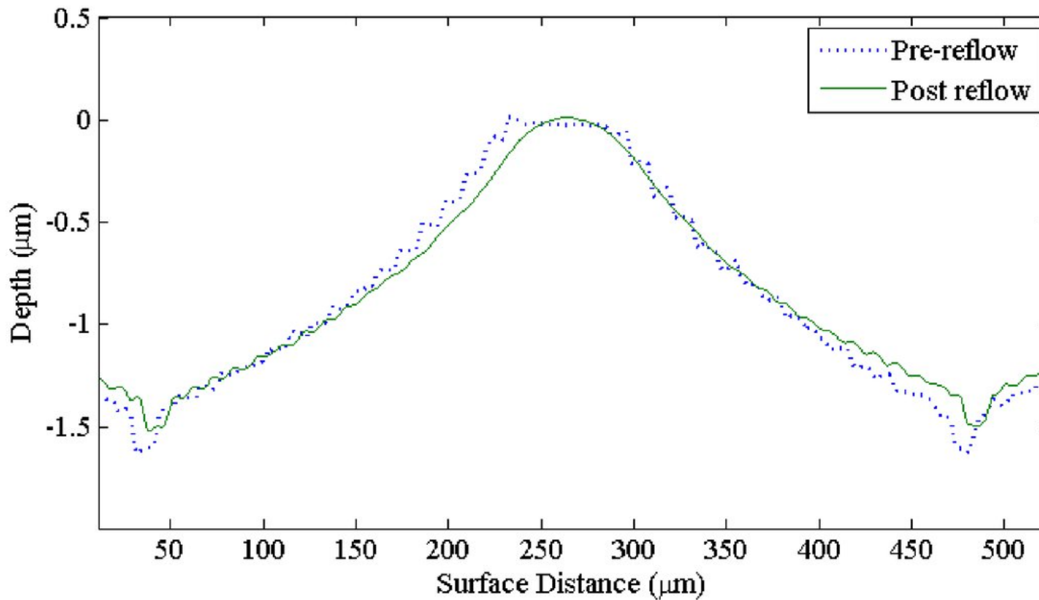
Figure 8. Example of the dip structure created in photoresist. The dip is the opposite of the 3D pyramid, where the center of the dip is fully exposed photoresist and is stepped up to the unexposed photoresist.



3.4 Re-flow of photoresist

As shown in the surface profiles, the stepping of power levels led to steps in the photoresists, but we required a smooth function. One attempt to obtain a smooth surface profile was with re-flowing of the photoresist. This method is used in many different applications, including creating micro-contacts bumps that this project supports. It was found that with 1818 photoresist, full melting of blocks of 1818 photoresist can be done at 150°C at 15 mins.[8] After a few trials, it was determined that an acceptable amount of re-flow happened after 3 mins. Figure 9 plots the before and after re-flow results on the different pattern types.

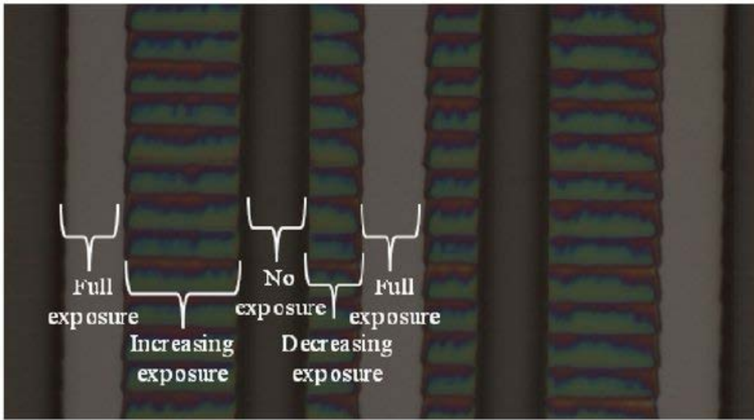
Figure 9. Plot of the 2D pyramid teeth surface profile before and after re-flow, demonstrating the smoothing of the steps on the slope.



3.5 Lower contact 2D pyramid

The ultimate goal was to create a lower contact surface for use in micro-contact testing. The first attempt to design a lower contact structure was to input the design for the lower contact and superimpose the image into the existing design. This would ensure the size and spacing would be correct. Due to a limitation of the design software the images cannot be superimposed into the mask design, so another way to write these lower contacts were required. Two methods were attempted to create these lower pads with the 2D pyramid pattern, the first was an image to represent the entire die, this consisted of 16 beam, and therefore 16 lower contacts in a 5000 µm x 5000 µm area was needed. This was created with one large picture that was scaled to the correct overall size. Figure 10 shows a picture of one of these lower contact pads that worked out to be about 70 µm x 150 µm. The second method was by using the manual alignment of the mask maker to direct where these blocks should be located. This method was more labor intensive, but with the addition of some alignment marks on the wafer this allowed for precise alignment of the lower contact.

Figure 10. 2D pyramid design imposed into the overall die image, due to the laser direction from left to right, created the lines against the grain of the 2D pyramid.



4. ETCH STUDY

An etch study was conducted to determine etching parameters in the Trion RIE system that would allow for the most uniform and least selectivity of etching.

Table 1. Etch rates found by varying parameters in four tests, parameters held constant for each test is grayed, pressure was held at 200 Torr for all tests. Test 1 varied the flow of O2. Test 2 varied the flow of both O2 and SF6. Test 3 varied the power level and test 4 varied the flow of SF6.

Test	O2 flow (SCCM)	SF6 flow (SCCM)	Power level (W)	Delta Photoresist (µm)	Delta Silicon (µm)	Selectivity
1	52	52	100	0.3672	0.5961	1.62
13	52	100	0.1068	2.0094	19.76	
6	52	100	0.1917	4.7848	24.96	
3	52	100	0.0895	10.995	112.79	
2	52	52	100	0.4747	0.8744	1.84
26	26	100	0.3956	0.8897	2.25	
13	13	100	0.3597	1.7137	4.76	
3	52	52	200	0.9282	8.0864	8.71
52	52	150	0.7768	5.5510	7.15	
52	52	100	0.4747	0.8744	1.84	
52	52	50	0.1057	0.0810	0.77	
4	52	52	100	0.5850	1.1840	2.02
52	39	100	0.5495	0.7198	1.30	
52	26	100	0.4789	0.2884	0.60	
52	13	100	0.5817	0.1275	0.21	

As expected, decreasing the oxygen rate increased the effects of the SF_6 reactively etching the silicon. From the results of the 1st test, the lowest selectivity was determined to be when the O_2 and SF_6 percentages were equal. When changing the overall flow of both O_2 and SF_6 caused small changes in the selectivity. It was determined that the best option for selectivity desired is at 52 SCCM of SF_6 and O_2. Power variations also has an effect on the etch selectivity, with higher powers causing the selectivity to increase. From the results of this set of tests a power of 100 Watts was chosen. Finally varying the SF_6 follows the expectation of the flow of the SF6 controlling the etch rate of the silicon.

This provides the key parameter when controlling the etching of the photoresist structures into the silicon wafers.

With the results of the etch study, the final selection of an O_2 and SF_6 Flow 52 SCCM, Pressure 200 Torr, Power 100 W, and an etch time of 1200 sec was the recipe needed to etch the gray-scale structure into the silicon substrate.

The etch parameters were used on a 2D pyramid pattern to check the results of the etching of the pattern into a silicon substrate, the results of this etch is seen in Figure 11. The change in depth of the pattern due to the selectivity of the etch parameters can be seen in Figure 12

Figure 11. The results of etching of a 2D pyramid pattern into the silicon substrate, the image of the direct write pattern is on the right and the resulting etch into the silicon can be seen on the left.

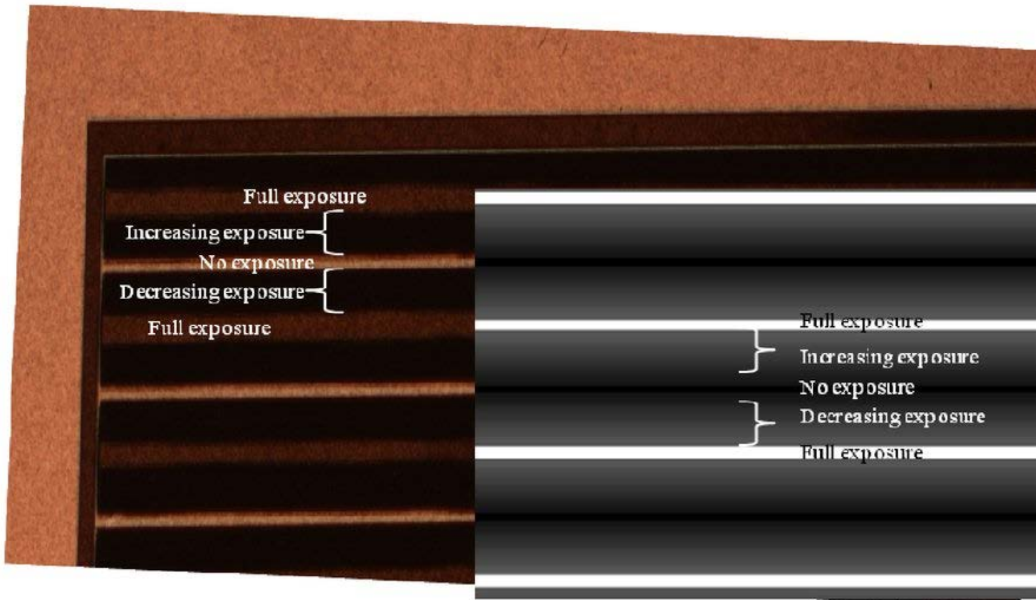
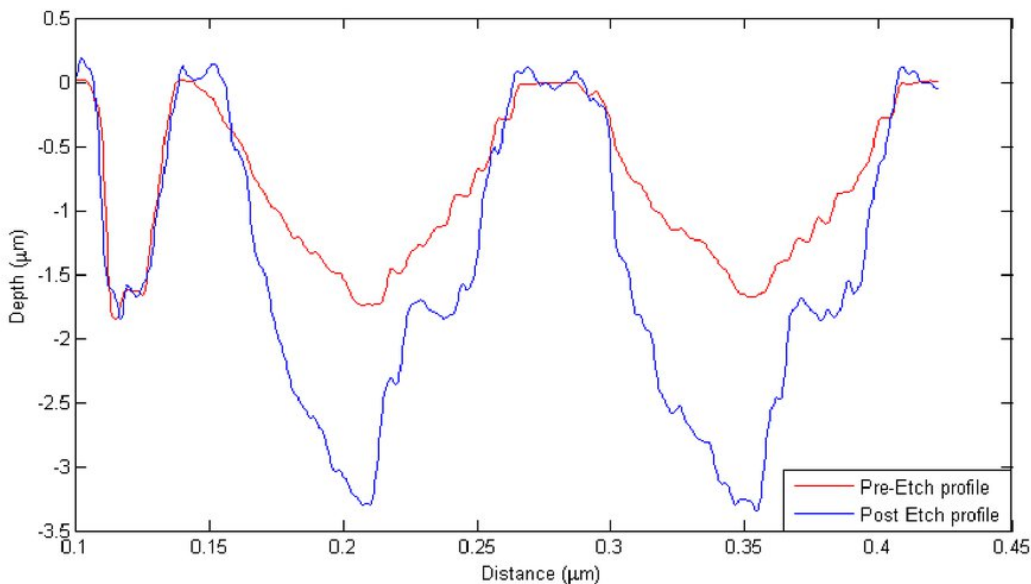


Figure 12. Showing the etch profile of the pattern shown in Figure 11. This demonstrates the close to 2:1 etch selectivity desired with the depth changing from ~1µm in the photoresist to ~3.4µm once etched into the silicon.



5. CONCLUSION

The ability to design and develop 3D microstructures is important for MEMS fabrication. Along with traditional fabrication techniques this paper presents how gray-scale lithography can be used in MEMs fabrication. It was shown that using the Heidelberg mask maker for patterning and RIE for etching, gray-scale lithography is achievable. Using this process, it will be possible to create many different 3D structures. This paper shows how these processes can be used to create profiles to a lower substrate that then can be processed with traditional surface micro-machining processes to create devices on non-planar surfaces.

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