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Novel microelectromechanical systems image reversal fabrication process based on robust SU-8 masking layers

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Abstract. This paper discusses a novel fabrication process that uses a combination of negative and positive photoresists with positive tone photomasks, resulting in masking layers suitable for bulk micromachining high-aspect ratio microelectromechanical systems (MEMS) devices. MicroChem's negative photoresist Nano^{TM} SU-8 and Clariant's image reversal photoresist AZ 5214E are utilized, along with a barrier layer, to effectively convert a positive photomask into a negative image. This technique utilizes standard photolithography chemicals, equipment, and processes, and opens the door for creating complementary MEMS structures without added fabrication delay and cost. Furthermore, the SU-8 masking layer is robust enough to withstand aggressive etch chemistries needed for fabrication research and development, bulk micromachining high-aspect ratio MEMS structures in silicon substrates, etc. This processing technique was successfully demonstrated by translating a positive photomask to an SU-8 layer that was then utilized as an etching mask for a series of trenches that were micromachined into a silicon substrate. In addition, whereas the SU-8 mask would normally be left in place after processing, a technique utilizing Rohm and Haas Microposit^{TM} S1818 as a release layer has been developed so that the SU-8 masking material can be removed post-etching. *© 2011 Society of Photo-Optical Instrumentation Engineers (SPIE).* [DOI: 10.1117/1.3625633]

Subject terms: microelectromechanical systems; bulk micromachining; lithography; image reversal; unexposed SU-8; uncrosslinked SU-8.

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1 Introduction

Photolithography is an iterative process used to transfer patterns from a photomask design onto a photosensitive material or photoresist. Once transferred into the photoresist, the pattern is then developed and "windows" to the underlying material are opened up. The underlying materials are then etched away, leaving behind a permanent pattern in the lower material, or materials are deposited into the windows. When fabricating surface micromachined microelectromechanical systems (MEMS) devices, thin film depositions are interlaced with photolithography, etching, and lift-off processing steps. Typically, positive photomasks and photoresists are used in MEMS fabrication to ensure fine resolution and precise minimum feature sizes. Sometimes, however, reverse field or complementary mechanical structures must be etched into the substrate (e.g., thermal isolation), which necessitates using a combination of surface and bulk micromachining and involving aggressive etch chemistries, negative photoresist, and robust masking materials. When these situations arise, the ability to use a positive photomask with a negative resist is often helpful to avoid fabrication delays and higher costs. In addition, certain negative photoresists (i.e., MicroChem's Nano^{TM} SU-8) are desirable because when they are hard baked they become chemically and thermally resistant. This allows them to stand up very well to the aggressive etching profiles needed for bulk micromaching, such as SF_6, when isotropic silicon etching is required. This paper discusses a novel processing technique that uses a combination of negative and positive photoresists for use with positive masks, resulting in masking layers suitable for bulk micromaching.

The novel process developed here utilizes image reversal (IR) and a positive tone mask to achieve the intended results. Of course, one could purchase a new mask if funding were available. Often times, however, in university-based, sponsor-funded research, funding is simply not available to purchase new masks while device fabrication is on-going. With this novel procedure, the fabrication schedule can be preserved and research dollars saved. For example, a new negative tone mask with 2 μm minimum features can cost approximately $3500 per mask and takes approximately 1 week to write, fabricate, and ship. This unnecessary delay and cost can add up quickly when device fabrication-oriented research is being conducted. The innovative procedure developed here utilizes photolithography chemicals, equipment, and processes that are readily available in most university fabrication facilities. This processing technique is illustrated in Fig. 1, and described in detail in Sec. 3. Specifically, SU-8 and Clariant's image reversal photoresist AZ 5214E are used, along with a barrier layer composed of a protective positive photoresist layer (Rohm and Haas Microposit^{TM} S1818) and an evaporated metal layer, to effectively convert a positive photomask into a negative photomask. The overall process resolution is limited by the SU-8 negative photoresist since

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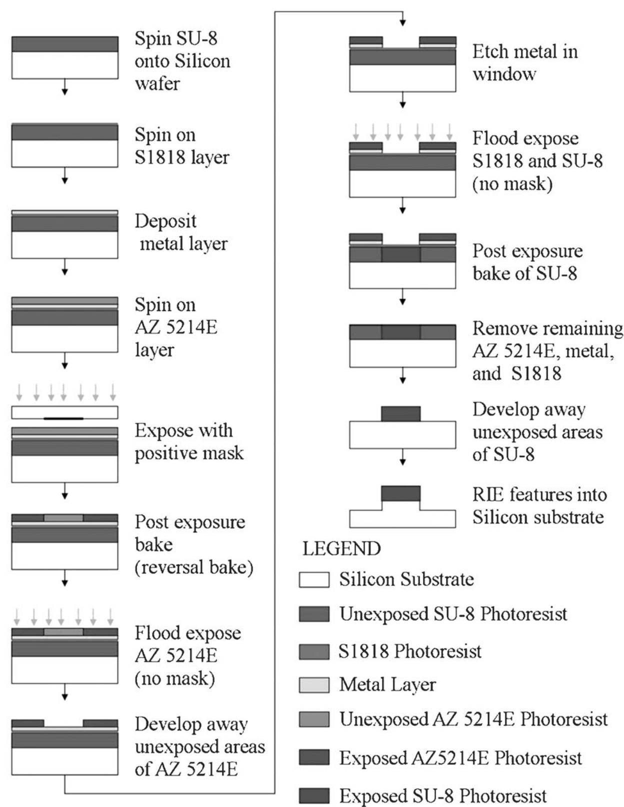

Fig. 1 Process flow for using positive photomasks to pattern SU-8 masking layers for fabricating inverse MEMS structures.

AZ 5214E allows for feature resolutions below 0.5 μm and SU-8's resolution limit is approximately 2 μm. Nevertheless, the novel fabrication process presented here is straightforward and suitable for novice device fabricators making bulk micromachined structures.

2 Background

AZ 5214E is a positive photoresist that also has the ability to be utilized for image reversal, providing the negative pattern of a photomask. It is most commonly utilized in the IR mode for lift-off processes where thin film metals are deposited and selectively patterned using a lift-off technique. Through an initial exposure, post-exposure bake (which acts as an image reversal bake), and flood exposure steps, image reversal is easily obtained. After a layer of AZ 5214E is exposed with a positive photomask, it is baked at a temperature between 115 °C and 125 °C, which initiates an agent in the photoresist that crosslinks the areas that have been exposed. This step is critical, since if it is not baked at the right temperature ($\pm$ 1 °C) the negative pattern of the photomask will not be obtained and the AZ 5214E will just act like a positive photoresist. Therefore, it is important to determine and optimize the reversal bake temperature in the range mentioned above for individual processes. The exposure of a photoactive compound within the photoresist, and the crosslinking in the exposed areas, makes these exposed areas insoluble in the developer. Meanwhile, after a flood exposure, the unexposed areas develop away in a standard positive photoresist developer. Unfortunately, AZ 5214E alone is not robust enough to stand up to the aggressive bulk micromachining etching profiles.[1]

SU-8 is a thick, epoxy-based, high contrast photoresist that is typically used in applications where it will be a permanent layer. Through an exposure and post-exposure bake steps, an SU-8 layer crosslinks and becomes resistant to liquid developers, and a wide range of other removal methods [e.g., O_2 plasma ashing, reactive ion etching (RIE), corrosive etches, etc.], thus making SU-8 an excellent masking material for bulk micromachining. The exposure step creates an acid and the post-exposure bake step follows this up by thermally activating the acid to crosslink the exposed areas.[2] The challenge here is that the SU-8 must remain uncrosslinked, and therefore unexposed, through a majority of the process. If the SU-8 gets exposed at any point it will crosslink and no longer be usable for this process. Various methods have been used to protect an uncrosslinked SU-8 layer during subsequent lithography and/or metal deposition steps, such as a filament evaporated metal layer,[3] using an antireflective coating on top of the SU-8,[4,5] UV exposure dose control,[6] contact printing of a metal layer,[7] and using a positive photoresist as a protection layer.[8] These approaches have been used in applications where SU-8 is utilized as a sacrificial material,[3] in the creation of microfluidic channels and other stacked structures,[6,9–11] and for electroforming.[4,5]

In order to protect the unexposed SU-8 in the processing technique presented here, a protective layer of positive photoresist is utilized on top of the SU-8 to protect it from being exposed and crosslinked during the evaporation of the metal barrier layer. This metal layer then serves to protect the unexposed SU-8 from being inadvertently exposed and crosslinked during subsequent UV photolithography steps performed on the AZ 5214E photoresist layer.

3 Methodology/Procedures

The process developed in this research is illustrated in Fig. 1 above. The process starts with the coating of a clean silicon wafer with SU-8 at the standard spin speeds. A 5-μm thick SU-8 layer was utilized in the development of this novel process. This is followed by a ramped softbake, with a bake at 65 °C for 3 min followed by a bake at 110 °C for 10 min. This is a longer bake time and higher bake temperature than typically prescribed, but it is critical to ensure the integrity of the SU-8 layer and to optimize material compatibility throughout subsequent processing. After a rest of several minutes at ambient temperature to allow for the SU-8 layer to stabilize, the wafer sample is coated with a layer of S1818 positive photoresist, which serves to protect the SU-8 from being exposed and crosslinked during metal deposition. Allowing the SU-8 layer to stabilize creates a solid base for the S1818 layer, and reduces the chances of unwanted interactions between the two photoresists. The SU-8 layer needs to be protected because it is highly sensitive to UV wavelengths, and high energy photon radiation emitted during the deposition process are in this range and above, thus resulting in the exposure and crosslinking of the SU-8 layer.[3] The S1818 layer undergoes a longer softbake than is usually utilized, 110 °C for approximately 12 $\frac{1}{2}$ min rather than the prescribed 75 s at 110 °C. The reason for this longer bake is to create a more stable base for the metal layer. Once again, the softbake times and temperatures were fine-tuned

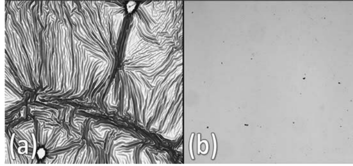

Fig. 2 Qualitative difference in integrity of an aluminum barrier layer based on S1818 softbake time. (a) Standard 75 s, shows deformations in the metal layer as a result of solvents baking out from the S1818 layer below it, (b) 12.5 min, shows a more uniform metal layer since the solvents were completely baked out prior to metal deposition.

to optimize material compatibility and the overall process. When a standard S1818 softbake is used, remaining solvents in the photoresist are baked off in subsequent steps following metal deposition, resulting in defects and nonuniform characteristics in the metal layer, as shown in Fig. 2(a) with an aluminum layer. It was discovered that a 12 $\frac{1}{2}$ min S1818 softbake resulted in a more stable and uniform metal layer through subsequent bakes, as shown in Fig. 2(b), while not having a negative impact on the processing of the SU-8 layer. The sample is then allowed to rest at ambient temperature for several minutes to allow the S1818 layer to stabilize. Next, approximately 500 Å of aluminum, titanium, or gold is evaporated onto the sample to serve as a UV block for the SU-8 layer. Aluminum was initially chosen as a metal barrier layer because it blocks the 365 nm UV wavelength used to expose the sample, plus it can be deposited via e-beam evaporation at a lower power than other available metals, thus reducing the likelihood of unintentional crosslinking during the deposition process. Titanium and gold were also investigated because they also block the 365 nm UV wavelength, plus they were shown to effectively not crosslink the SU-8 layer during deposition.

Once the sample has had adequate time to cool, it is coated with AZ 5214E at the standard spin speed for a 1.4 μm layer and baked at 110 °C for 50 s. The sample is then exposed using a positive photomask for 3 s at an intensity of 11 mJ/cm^2 using a Karl Suss MJB3 Photomask Aligner. This is followed by the most critical step for the AZ 5214E processing, a 115 °C post-exposure bake for 2 min. This post-exposure bake acts as a reversal bake, in which the image reversal characteristic of the AZ 5214E is activated. Following the reversal bake, the sample is subjected to a 14 s flood exposure on a Karl Suss MJB3, which affects the solubility of the AZ 5214E, as described above. The AZ 5214E layer is then developed using 351 Developer. Once the image reversal features are obtained and verified in the AZ 5214E layer, as shown in Fig. 3, the metal in the open windows is etched with buffered oxide etch (BOE) for aluminum or titanium layers, and gold etchant (Transene Company, type TFA) for the gold layers. The exposed areas of photoresist (S1818 on top of SU-8) are then subjected to a 1 min and 45 s exposure on the MJB3, with the remaining metal features on the sample acting as a UV blocking barrier mask, as shown in Fig. 4. The 1 min and 45 s exposure time was obtained through an exposure study to determine the optimum time to expose the photoresist layer, since the SU-8 is being exposed through the S1818. This was important because if the SU-8 layer is not exposed completely, and thus not fully crosslinked, it would not have the structural integrity to act as a masking layer. Figure 5

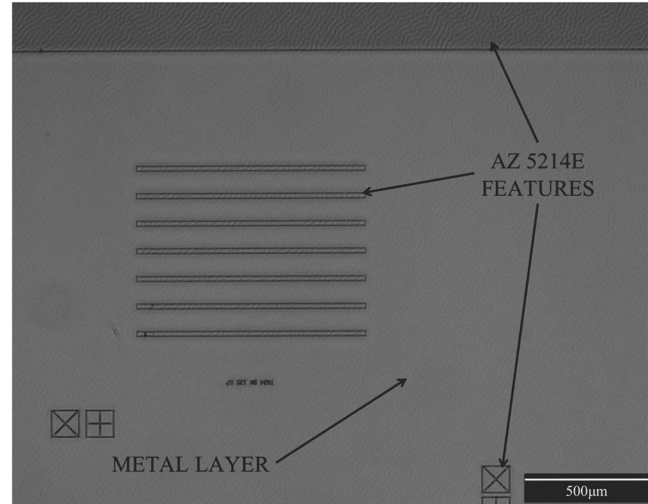

Fig. 3 Developed AZ 5214E features on titanium layer.

highlights some of the results for the exposure study. As can be seen, at an exposure time of 60 s, (a), the integrity of the layer is poor with multiple defects. At 90 s, (b), the integrity of the layer is better, but there are still some apparent defects. At 1 min and 45 s, (c), and 2 min, (d), the integrity of the layer is good enough to process with. There is not much difference in the integrity of the layers between 1 min and 45 s and 2 min, so 1 min and 45 s was chosen in order to avoid any overexposure problems.

The exposure of the photoresist layer is followed by a ramped post-exposure bake, with a bake at 65 °C for 3 min followed by a bake at 110 °C for 3 min. Once again, this longer bake helps ensure the integrity of the SU-8 layer as it proceeds through the process. Next, the remaining AZ 5214E is removed, as well as the remaining metal and S1818 layers. This opens up the unexposed SU-8 areas for the development step. The sample is placed in SU-8 developer and placed in an ultrasonic bath to develop out the unexposed SU-8 areas, and as a result opening up windows to the substrate, as shown in Fig. 6. The exposed SU-8 areas are crosslinked, so they

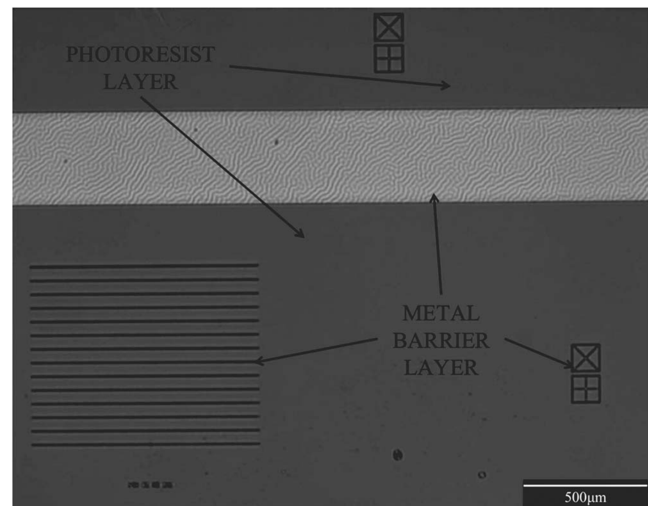

Fig. 4 Titanium barrier layer on photoresist layer.

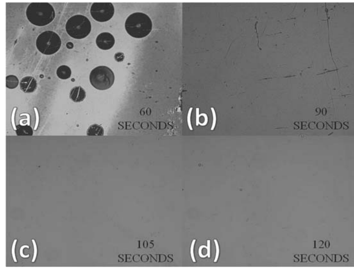

Fig. 5 Qualitative comparison of SU-8 photoresist layer integrity based on exposure time: (a) 60 s, (b) 90 s, (c) 105 s, and (d) 120 s.

do not develop out, and now are able to act as a mask for the etching. Next, the sample is given a quick BOE dip to clear out any native oxides or contaminants that may have formed in the photoresist windows, and then the features are isotropically etched into the silicon substrate using a RIE tool and SF_6.

4 Results and Discussion

Figure 6 shows an optical image of the SU-8 masking layer created utilizing this processing technique with a titanium barrier layer. The positive photomask characteristics and features were successfully translated to the SU-8 layer. Figure 7 shows the features obtained with this SU-8 masking layer, trenches etched into a silicon substrate, thus highlighting the ability to use a combination of negative and positive photoresists with a positive mask, to create masking layers suitable for bulk micromachining silicon substrates. Figure 8 shows an SEM side view of a trench in the silicon substrate, and Fig. 9 shows an end view of the trench. The SU-8 layer step height was measured at approximately 5 μm prior to etching. After etching for 60 min, the total step height was measured at approximately 9.2 μm, resulting in an approximate etch depth into the silicon of 8.2 μm.

While the final process is straightforward, working through the process development showcased some critical

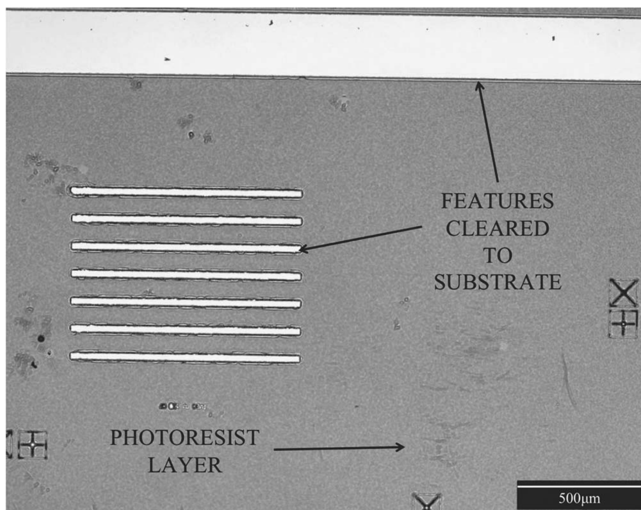

Fig. 6 SU-8 masking layer fabricated using a positive photomask and titanium barrier layer.

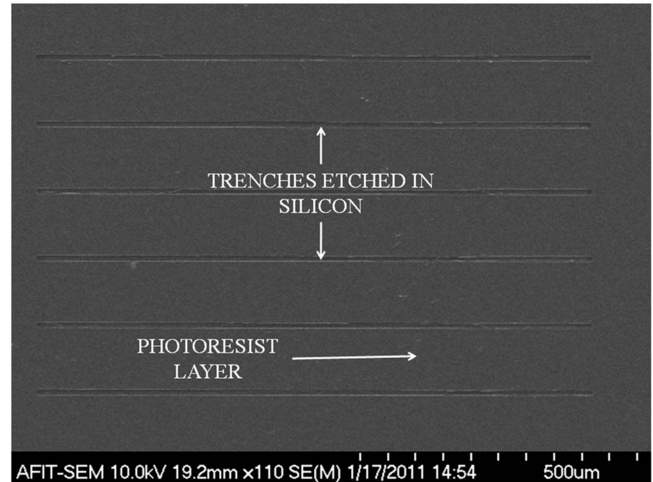

Fig. 7 Top view of features etched into the silicon substrate utilizing an SU-8 masking layer fabricated using a positive photomask and a titanium barrier layer.

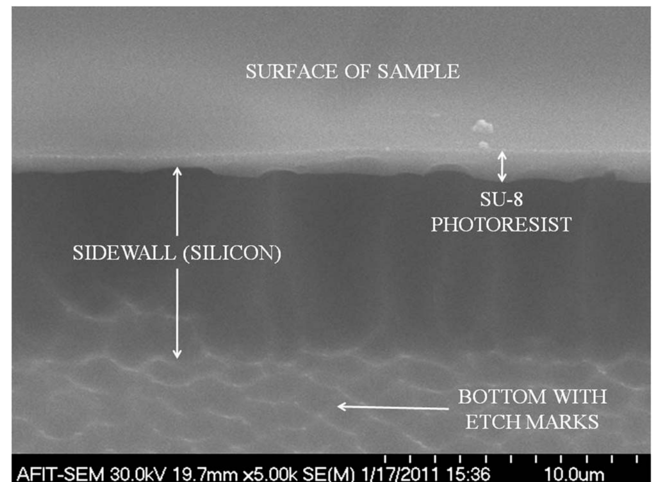

Fig. 8 Side view of a trench etched into a silicon substrate (titanium barrier layer used).

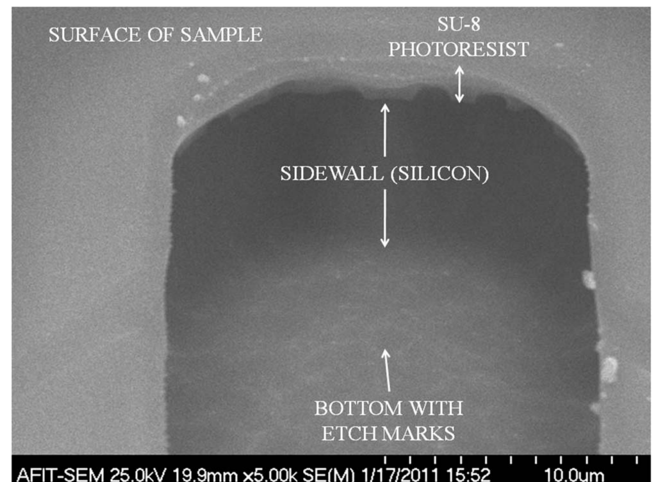

Fig. 9 Endcap of a trench etched into a silicon substrate (titanium barrier layer used).

areas that need to be considered when working with this combination of materials, mostly with how these materials interact with unexposed SU-8. The temperature at which SU-8 was baked, and the temperatures it was subjected to during processing, were important aspects in developing this process. To begin with, when SU-8 was baked at the prescribed times and temperatures, adhesion issues and cracking were observed during the SU-8 post-exposure bakes. A typical solution to these types of issues is a longer post-exposure bake, but since these issues appeared during the 65 °C softbake step, a longer post-exposure bake alone was not a viable option. Through further investigation, it was discovered that extending the softbake and the post-exposure bake times to the steps described above resulted in a consistent and viable SU-8 layer. Another critical area was ensuring that the SU-8 was not inadvertently exposed and crosslinked prematurely. Initially, plans were to use a metal layer directly on top of the unexposed SU-8 as a UV block, therefore only requiring three layers—SU-8, metal, and AZ 5214E. Attempts at sputtering and evaporating various metals directly onto the SU-8 resulted in crosslinking. As detailed in Refs. 3, 7, 8, and 10, the sputtering and evaporating processes, through the creation of plasma in the case of sputtering and radiation/heat transfer in the case of evaporation, created enough UV energy to expose and inadvertently crosslink the SU-8.

Initial attempts at depositing various protective layers on top of the unexposed SU-8 before depositing the metal layer were not successful. Eventually, it was discovered that exposing both the S1818 and SU-8 layers at the same time, followed by the SU-8 post-exposure bake, allowed for the SU-8 layer to be developed out and processed as intended. Furthermore, when applying the S1818 on top of the SU-8, the spin speed of the S1818 was important. When the S1818 was spun at a speed greater than what the SU-8 was spun at, the S1818 tends to diffuse into the SU-8, resulting in erratic thicknesses. When the S1818 was spun at a speed less than what the SU-8 was spun at, this issue was overcome and film thickness was as expected. There is most likely, however, still some material diffusion at the interface of the two photoresists but it does not negatively affect using the SU-8 and S1818 in this process. Therefore, an S1818 layer on top of the SU-8 provided adequate protection to allow for the evaporation of a UV barrier metal without exposing and prematurely crosslinking the SU-8 layer below. A longer S1818 softbake to maximize solvent release and create a more stable base for the metal barrier layer is crucial. A 12 $\frac{1}{2}$ min bake time was found to be a sufficient bake time provided the samples were not unnecessarily left exposed to ambient conditions. Figure 10 shows the AZ 5214E developed on top of an aluminum layer after being inadvertently exposed and not processed for approximately 2 days. As can be seen, the aluminum layer develops "hills and valleys," which translates to poor features in the AZ 5214E. This unevenness is seen through the rest of the process, such as the aluminum mask as shown in Fig. 11 and the SU-8 masking layer as shown in Fig. 12. This unevenness results in lower resolution features when compared to those that were processed without delays. This is highlighted in Fig. 13, which shows trenches etched into a silicon substrate, and Fig. 14, which shows a side view of a trench. Even though features were realized with the

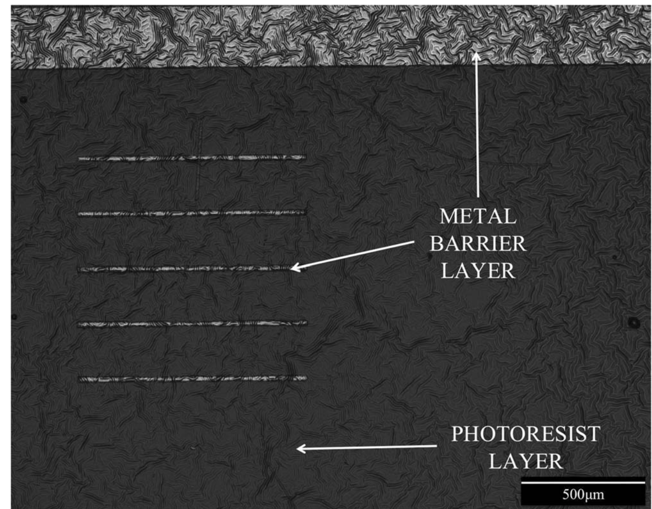

Fig. 11 Aluminum barrier layer on photoresist layer (both uneven).

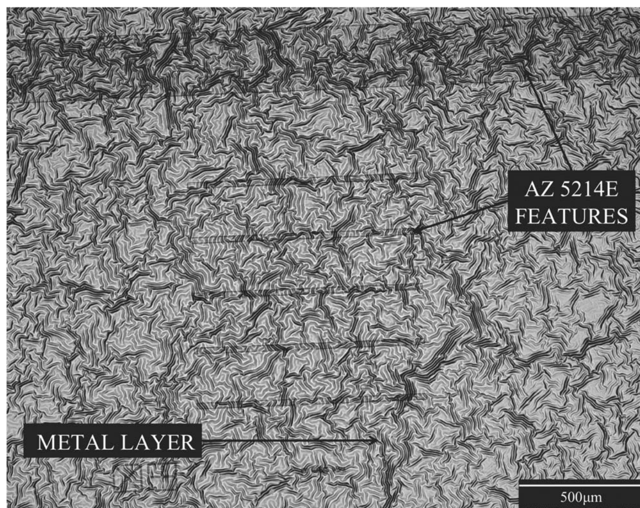

Fig. 10 Developed AZ 5214E features on uneven aluminum layer.

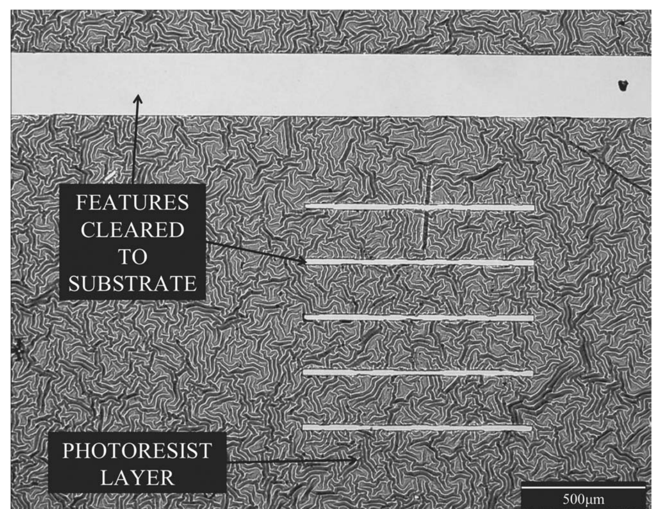

Fig. 12 Uneven SU-8 masking layer fabricated using a positive photomask and aluminum barrier layer.

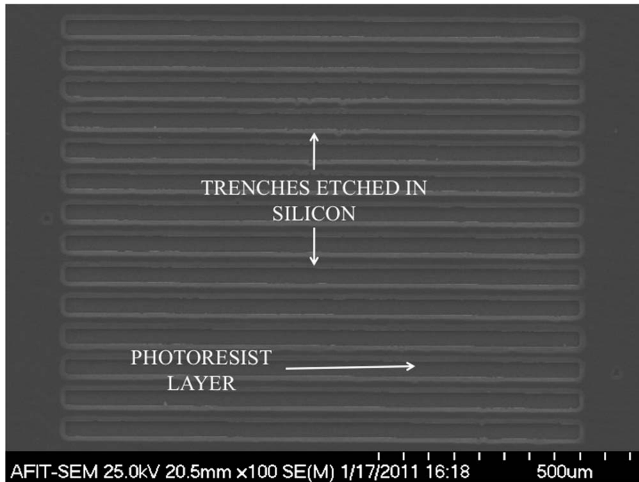

Fig. 13 Features etched into the silicon substrate utilizing an uneven SU-8 masking layer fabricated using a positive photomask and aluminum barrier layer.

processing technique utilizing this sample, the results are less than desirable. In general, samples that are processed the same day provided the best results.

The current processing technique results in a robust SU-8 layer remaining after etching, which in some applications is not desirable. In order to address this, a quick investigation into using S1818 as an SU-8 release layer was initiated, and the initial results look promising. In this initial investigation, S1818 was spun onto a silicon substrate, followed by an extended bake of $12\frac{1}{2}$ min at 110 °C. The extended bake was utilized to provide a solid base for the SU-8 layer that is spun on top of the S1818. After the SU-8 was spun on, the sample was exposed for 10 s, and then developed out as shown in Fig. 15(a). The features were then etched into the substrate using an RIE, as shown in Fig. 15(b). This was followed by placing the sample in acetone and placing it in an ultrasonic bath. In less than 2 min, the S1818 dissolved and the SU-8 layer floated off of the substrate leaving behind a sample with bulk micromachined features without an SU-8 masking layer, as shown in Figs. 15(c) and 15(d). In Fig. 15(d), the

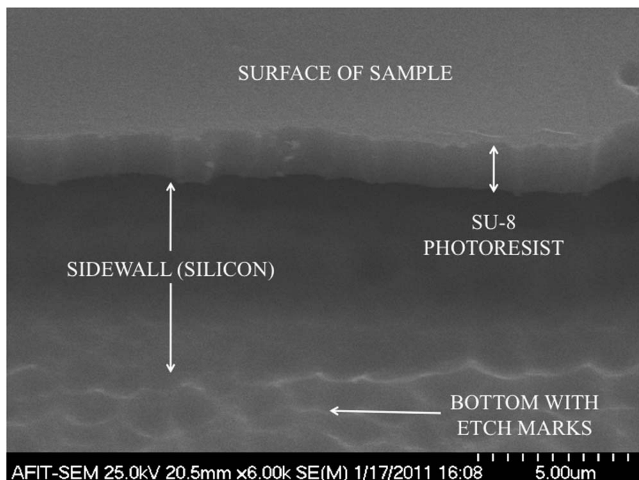

Fig. 14 Side view of a trench etched into a silicon substrate (Al barrier layer used).

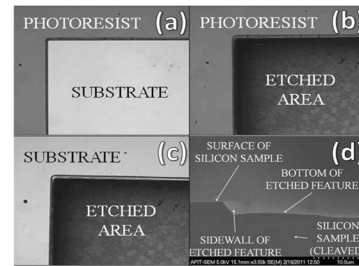

Fig. 15 S1818 release layer for SU-8: (a) developed features in SU-8; (b) features etched into the silicon substrate; (c) SU-8 removed from sample; (d) profile of etched features in silicon.

sample was cleaved in order to provide a profile of the etched features.

5 Conclusions

A novel processing technique that uses a combination of negative and positive photoresists with positive tone masks, resulting in reversed masking layers suitable for bulk micromachining, has been developed. This process has been demonstrated through the fabrication of trenches in a silicon substrate, utilizing a positive photomask along with a combination of AZ 5214E image reversal photoresist, a barrier layer of an S1818 protective layer and evaporated metal layer, and SU-8 negative photoresist. Titanium, aluminum, and gold were shown to be effective UV barrier layer metals. This novel procedure is actually quite simple and suitable for even novice device fabricators. Despite being simple and straightforward in concept, there are critical pitfalls that must be considered and effectively avoided when working through this process. These include, but are not limited to, thermal concerns with the SU-8 layer to ensure it does not hard bake, negative and unforeseen interactions between the SU-8 layer and other material layers, and ensuring that the uncrosslinked SU-8 does not get exposed and crosslinked prematurely. Finally, a simple process for removing unwanted robust layers of SU-8 (post-etch) was developed where S1818 was used as releasable layer deposited underneath the SU-8.

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References

1. AZ 5214E Image Reversal Photoresist Product Data Sheet.
2. Nano SU-8 Negative Tone Photoresist Formulations 2–25, Rev. 2/02. ⟨http://www.microchem.com/products/pdf/SU8_2–25.pdf⟩.
3. C. Chung and M. Allen, "Uncrosslinked SU-8 as a sacrificial material," *J. Micromech. Microeng.* **15**(1), N1–N5 (2005).

4. C. K. Chung, Y. Z. Hong, and W. T. Chang, "Fabrication of the monolithic polymer-metal microstructure by the backside exposure and electroforming technology," *Microsyst. Technol.* **13**(5/6), 531–536 (2007).
5. C. K. Chung, C. J. Lin, L. H. Wu, Y. J. Fang, and Y. Z. Hong, "Selection of mold materials for electroforming of monolithic two-layer microstructure," *Microsyst. Technol.* **10**(6/7), 467–471 (2004).
6. F. G. Tseng, Y. J. Chuang, and W. K. Lin, "A novel fabrication method of embedded micro channels employing simple UV dosage control and antireflection coating," in *The Fifteenth IEEE International Conference on MEMS*, pp. 69–72 (2002).
7. D. Haefliger and A. Boisen, "Three-dimensional microfabrication in negative resist using printed masks," *J. Micromech. Microeng.* **16**(5), 951–957 (2006).
8. V. M. B. Carballo, M. Chefdeville, M. Fransen, H. van der Graaf, J. Melai, C. Salm, J. Schmitz, and J. Timmermans, "A radiation imaging detector made by postprocessing a standard CMOS chip," *IEEE Electron Device Lett.* **29**(6), 585–587 (2008).
9. B. E. J. Alderman, C. M. Mann, D. P. Steenson, and J. M. Chamberlain, "Microfabrication of channels using an embedded mask in negative resist," *J. Micromech. Microeng.* **11**(6), 703–705 (2001).
10. F. Ceyssens and R. Puers, "Creating multi-layered structures with freestanding parts in SU-8," *J. Micromech. Microeng.* **16**(6), S19–S23 (2006).
11. P. Abgrall, C. Lattes, V. Conédéra, X. Dollat, S. Colin, and A. M. Gué, "A novel fabrication method of flexible and monolithic 3D microfluidic structures using lamination of SU-8 films," *J. Micromech. Microeng.* **16**(1), 113–121 (2006).

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