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A Fault-Tolerant T-Type Multilevel Inverter Topology With Increased Overload Capability and Soft-Switching Characteristics

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Abstract:

The performance of a novel three-phase four-leg fault-tolerant T-type inverter topology is introduced in this paper. This inverter topology provides a fault-tolerant solution to any open-circuit and certain short-circuit switching faults in the power devices. During any of the fault-tolerant operation modes for these device faults, there is no derating required in the inverter output voltage or output power. In addition, overload capability is increased in this new T-type

inverter compared to that in the conventional three-level T-type inverter. Such increase in inverter overload capability is due to the utilization of the redundant leg for overload current sharing with other main phase legs under healthy condition. Moreover, if the redundant phase leg is composed of silicon carbide metal-oxide-semiconductor field-effect transistors, quasi-zero-voltage switching, and zero-current switching of the silicon insulated-gate bipolar transistors (IGBTs) in the conventional main phase legs can be achieved at certain switching states, which can significantly relieve the thermal stress on the outer IGBTs and improve the whole inverter efficiency. Simulation and experimental results are given to verify the efficacy and merits of this high-performance fault-tolerant T-type inverter topology.

Keywords

Inverters, Circuit faults, Legged locomotion, Switches, Fault tolerance, Fault tolerant systems, Insulated gate bipolar transistors

SECTION I.

Introduction

A t-type multilevel converter is an attractive breed of high-performance power converters widely applied in industrial applications. This is because of the lower number of switching devices utilized in their circuit topologies and higher efficiency compared with the conventional I-type neutral-point-clamped converters [1]–[3]. However, like other types of multilevel converters, T-type converters are not immune to electrical faults in their semiconductor devices. For instance, switch open-circuit or short-circuit faults could cause catastrophic system failures if no fault-tolerant solutions are provided. Particularly, the availability of fault-tolerant solutions becomes more important when such T-type inverters are applied in safety-critical applications, such as electric vehicles (EVs), uninterruptable power supplies (UPSs), wind and solar energy conversions, and the like. Although T-type converters have certain inherent fault-tolerant capabilities due to their unique topologies, as reported in [4], the output voltage and linear modulation range have to be significantly reduced during the fault-tolerant operation region. Such derating is not preferred in certain applications (e.g., UPSs, EVs, etc.), where rated output voltages and output power are stringent requirements. Therefore, it would be of great significance to improve T-type converters' topology with enhanced fault-tolerant capability, to guarantee full output voltages during postfault operations. The existing solutions for the fault-tolerant operation of T-type converters are mainly achieved by paralleling multiple redundant inverter legs, such as the circuit topologies detailed in [5] and [6], which achieves full output voltages under inverter fault-tolerant conditions, but at much higher system cost with decreased inverter efficiency due to a large number of redundant semiconductor devices involved in the converter circuits. In fact, most of the redundant semiconductor devices in the existing fault-tolerant topology simply idle in the circuits without any contribution to system performance improvement under healthy conditions, resulting in decreased inverter efficiency due to the associated device conduction and/or switching losses.

Unlike these existing solutions proposed in the literature [4]– [6], a novel three-phase four-leg T-type inverter topology will be introduced and evaluated in this paper. This new topology can not only enhance the fault-tolerant capability of the inverter under faulty conditions, but also increase the inverter thermal overload capacity as well as achieve soft switching for the insulated-gate bipolar transistors (IGBTs) in the original T-type inverter. If the redundant phase leg is composed of four widebandgap devices, such as silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs), high inverter efficiency can be achieved due to the soft switching characteristics, although the proposed fault-tolerant inverter topology contains four phase legs.

The remainder content of this paper is organized as follows. In Section II , the fault-tolerant operation characteristics of this proposed T-Type inverter will be presented for different fault scenarios. In Section III, the increased overload capability of this new fault-tolerant T-Type inverter will be analyzed. In Section IV, soft-switching characteristics of this T-type inverter by leveraging the redundant SiC leg will be elaborated. In Sections V and VI, simulation and experimental results will be demonstrated, respectively, to verify the improved fault-tolerant operation, increased overload capability, and the soft-switching characteristics of the presented T-type inverter. Finally, conclusions will be given in Section VII.

SECTION II.

Proposed Fault-Tolerant T-Type Inverter

The conventional three-phase three-leg T-type inverter topology and the proposed four-leg T-type inverter topology are shown in Fig. 1 and Fig. 2, respectively. As it can be seen, there is one redundant leg added between the dc-bus capacitors and the original T-type inverter package in the proposed three-phase four-leg inverter shown in Fig. 2. In this paper, the redundant leg is composed of four SiC MOSFETs, while the original three-leg T-type inverter package consists of Si IGBT modules. Under normal or healthy condition, this redundant leg, marked in the yellow shaded area in Fig. 2, outputs zero voltage by keeping the MOSFETs S_2 and S_3 on constantly. Considering the circuit symmetry of the proposed four-leg T-type inverter, only six cases of switching device faults are analyzed here to represent all the possible switching fault scenarios that could happen and can be tolerated in such a four-leg T-type inverter. These six cases of fault scenarios include the following:

1. open-circuit fault in switch S_{a1};
2. open-circuit fault in switch S_{a2};
3. open-circuit fault in switch S_1/S_2 on the redundant leg;
4. short-circuit fault in switch S_{a2};
5. short-circuit fault in switch S_1 on the redundant leg;
6. short-circuit fault in switch S_2 on the redundant leg.

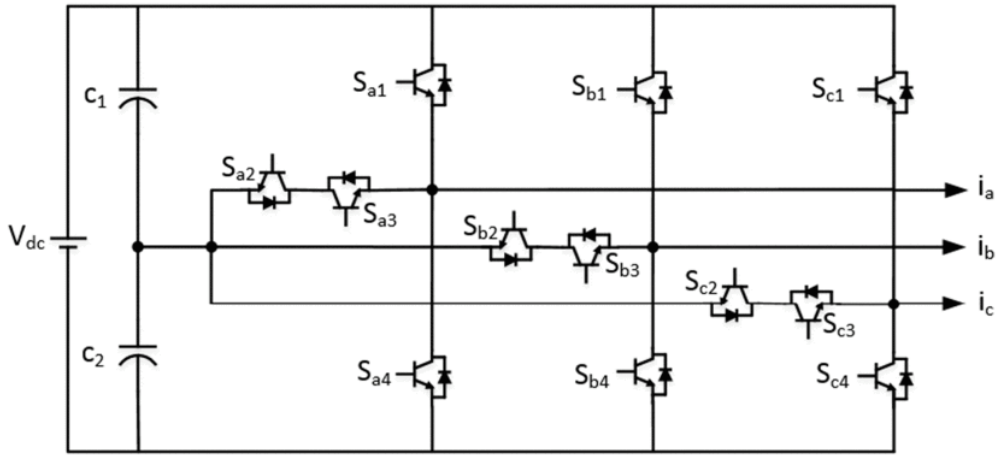


Fig. 1. Conventional three-phase three-level T-type inverter topology.

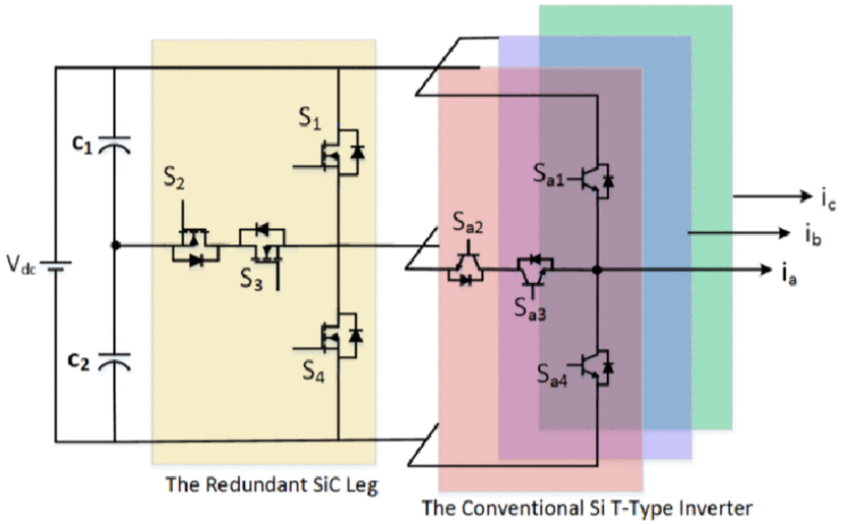


Fig. 2. Proposed fault-tolerant three-level T-type inverter topology.

It should be noted that a short-circuit fault in any of the outer switches (S_{x1} or S_{x4}, $x = a, b,$ or c) of the original T-type inverter is not considered in this proposed T-type inverter topology. Potential fault-tolerant solution to such short-circuit faults in outer switches could be adding ultrafast acting fuses in series connected to the outer switches, in purpose to transform a short-circuit fault into an open-circuit fault, which can be tolerated in this proposed inverter topology. However, such investigation involves the performance verification of the fuses and is beyond the research scope of this paper. Moreover, in this paper, only a single device fault is considered for the inverter, and multiple simultaneous device faults are out of the scope of investigation in this paper. Although the fault scenario analysis and fault-tolerant solutions discussed below only focus on fully controlled active devices in this proposed T-type inverter, they are also applicable to the faults in the related free-wheeling diodes. The fault-tolerant strategy for each of the six aforementioned fault scenarios in the developed T-type inverter will be detailed next.

A. Case I: Open-Circuit Fault in IGBT Sa1

Once an open-circuit fault in the IGBT S_{a1} is identified, Phase-A leg of the T-type inverter will not be able to produce a positive voltage. Under such scenario, IGBT S_{a1} will be replaced by SiC MOSFET S_1 in the redundant phase leg through turning on IGBTs S_{a2} and S_{a3}, while all the other SiC MOSFETs (i.e., S2 , S3, and S4) on the redundant leg are turned off to avoid shorting the dc-bus capacitors, as illustrated in Fig. 3(a). As it can be seen, during such fault-tolerant operation, the three-phase inverter can still output rated voltages, but will have to be modulated as a two-level inverter due to no access to the dc-bus neutral point. Similar fault-tolerant solutions can be applied for open-circuit faults in other outer IGBTs S_{x1} (where $x = b$ or c) and S_{x4} (where $\mathrm{x} = a, b,$and c). There is no derating required for the modulation indices or the output voltages.

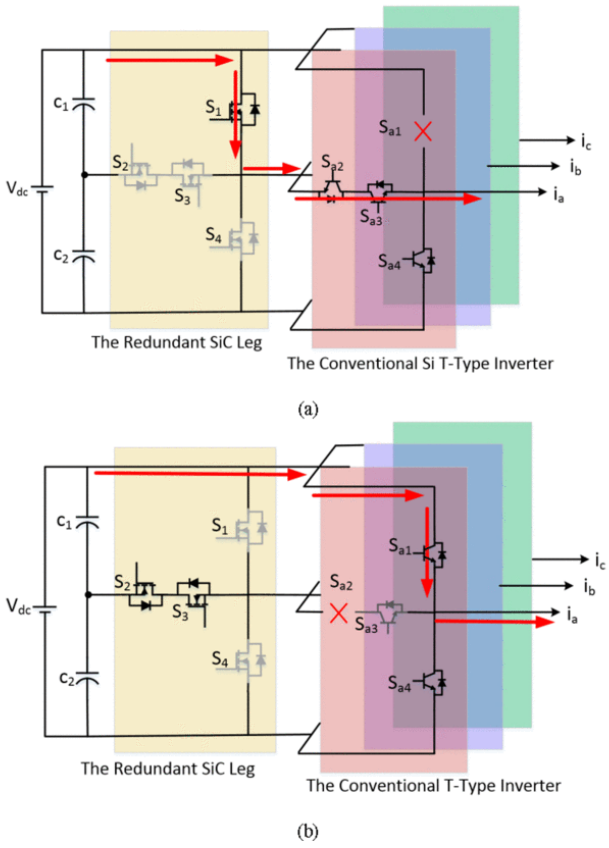


Fig. 3. Current flow during fault-tolerant operation when (a) IGBT S*a*1 has an open-circuit fault and (b) IGBT S*a*2 has an open-circuit fault (the devices in gray color refer to constant-off state).

B. Case II: Open-Circuit Fault in IGBT S_{a2}

If an open-circuit fault happens in the IGBT S_{a2}, the related faulty leg, i.e., Phase-A leg, can only output positive voltage and negative voltage by only using S_{a1} and S_{a4} for fault-tolerant operation (the same as a conventional two-level inverter leg), which is due to the loss of the bidirectional switch (constituted by S_{a2} and S_{a3}) accessing the dc-bus neutral point for the

faulty phase, as shown in Fig. 3(b). Under such a situation, the gate signal of S_{a3} will be turned off; thus, the output of Phase-A leg will be isolated from the dc-bus neutral point. However, the other healthy phase legs, namely, Phase-B and Phase-C legs in this case, can still be operated as normal three-level inverter legs. As a result, the line-to-line voltages of the inverter can still exhibit three-level staircase waveforms. There is no derating required for the modulation index or voltage output during postfault operation in this case. Similar fault-tolerant solutions can be applied for open-circuit faults in other middle IGBTs S_{x2}/S_{x3} in Phase-B and Phase-C legs. It should be clarified that such fault-tolerant capability to open-circuit faults in the middle switches (S_{x2} or S_{x3}, $\mathrm{x} = a, b,$ and c) is an inherent characteristic in the conventional T-type inverters, as reported in [4].

C. Case III: Open-Circuit Switch Fault on the Redundant Leg

It is possible that an open-circuit fault may occur in one of the devices in the redundant SiC phase leg. If the upper/lower SiC MOSFET, i.e., S_1 or S_4, has an open-circuit fault, there is no impact for this redundant leg on providing the dc-bus neutral point access for the normal operation of the T-type inverter. In other words, the original three-phase three-leg T-type can still be operated as a normal three-level inverter. However, if the middle SiC MOSFETs, i.e., S_2 or S_3, have an open-circuit fault, the T-type inverter has to be modulated as a conventional two-level inverter, which is due to the loss of the access to the dc-bus neutral point through S_2 and S_3. Nevertheless, under any of these open-circuit faulty conditions, no deratings are required for the modulation indices or output voltages.

D. Case IV: Short-Circuit Fault in IGBT S_{a2}

If a short-circuit fault in IGBT S_{a2} is determined, its complimentary switch S_{a3} has to be switched off due to the loss of reverse blocking capability. Accordingly, all the switches in the redundant leg should be turned off to avoid shorting the dc-bus capacitors, as shown in Fig. 4(a). Under such a scenario, the three-level T-type inverter will be operated as a conventional two-level inverter by only using S_{x1} and S_{x4} (where, $x = a, b,$ or c) during the postfault operation. A similar fault-tolerant strategy can be applied for short-circuit faults in IGBTs S_{x2} (where, *x*=*b*or *c*) or S_{x3} (where $x = a, b,$ or c). Again, no deratings are required for the modulation indices or output voltages for this type of short-circuit switching faults.

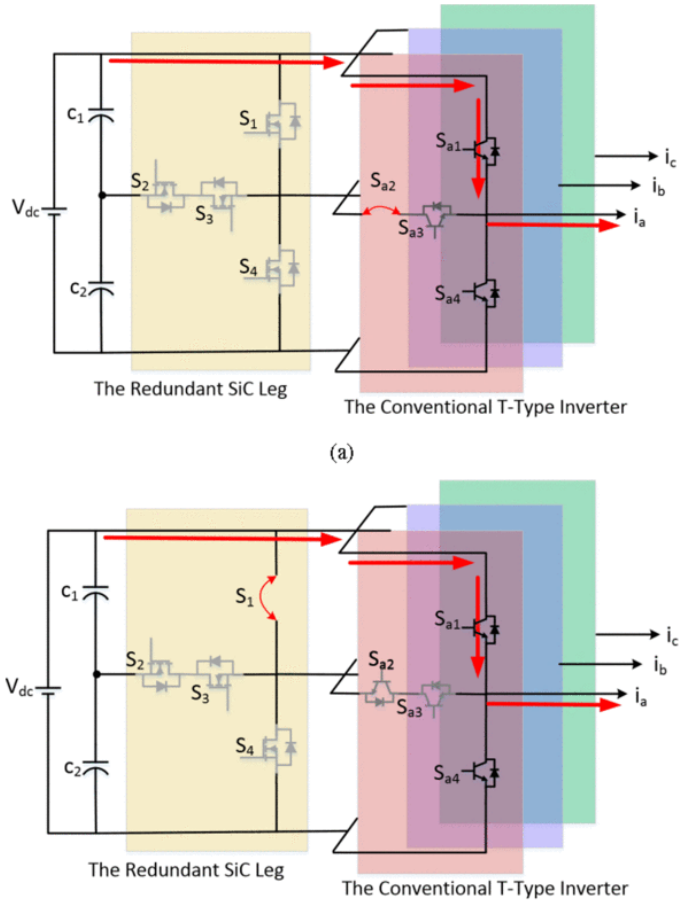


Fig. 4. Current flow during fault-tolerant operation when (a) IGBT S_{a2} has a short-circuit fault and (b) MOSFET S_1 has a short-circuit fault (the devices in gray color refer to constant-off state).

E. Case V: Short-Circuit Fault in S1 on the Redundant Leg.

If there is a short-circuit fault occurring in any of the outer switches (i.e., S_1 or S_4) on the redundant leg, all the middle switches, including S_2 and S_3 on the redundant leg, as well as S_{x2} and S_{x3} ($x = a, b, \text{and } c$), have to be switched off, as shown in Fig. 4(b) . Otherwise, a cascaded dc-bus shoot-through fault may happen. For instance, during normal operation, S_2 and S_3 are constantly on to provide the access to dc-bus neutral point for all the three main legs, and a short-circuit fault in S_1 will simultaneously cause a short circuit of the upper dc-bus capacitor C_1 if S_2 and S_3 are still on. After all the middle switches are turned off, the three-level T-type inverter has to be operated as a two-level inverter during the postfault stage by switching the outer switches S_{x1} and S_{x4} (where $x = a, b, \text{and } c$).

F. Case VI: Short-Circuit Fault in S2 on the Redundant Leg

If a short-circuit fault occurs in any of the middle switches (i.e., S_2 or S_3) of the redundant leg, there is no impact on the normal operation of the original T-type inverter, since the access to the dc-bus neutral point is still available. However, under such a fault situation, the option of

using the redundant leg for sharing the overload current with other phase legs has to be disabled, or else a dc-bus shoot-through fault may occur. Such overload current-sharing characteristics by leveraging the redundant leg under healthy condition of the inverter will be presented in Sections III and IV.

In summary, this proposed T-type inverter can tolerate any open-circuit switching faults, as well as all the short-circuit switching faults except these in outer devices, i.e., S_{x1} and S_{x4}, (*x* = *a*, *b*, and *c*). For any of these aforementioned device faults, there is no derating required for the output voltages during the fault-tolerant operation mode of the inverter. However, such an inverter has to be modulated as a two-level inverter under some of these faulty conditions, which implies a slightly higher harmonic distortion in the output currents and voltages compared to these under three-level normal operation.

SECTION III.

Increased Overload Capability of the Inverter

As is known that the overload capability of a power inverter is mainly determined by the electrical ratings of the power devices, which in essence is the thermal constraint on the devices during operation. When a conventional T-type inverter is operating at a high power factor, the outer devices (S_{x1} or S_{x4}, $x = a, b,$ and c, as shown in Fig. 1) will dissipate larger losses than the middle devices (S_{x2} or S_{x3}, $x = a, b,$ and c) [1]. From the perspective of thermal distribution among all the power devices, the dominant losses in these outer devices constrain the overload capability and highest switching frequency of the T-type inverter at a high power factor. However, in this proposed T-type inverter, the redundant leg provides a promising solution to reduce the conduction and switching losses in the outer devices of the T-type inverter. In this section, the mitigation of conduction losses in the outer devices by using the redundant leg will be elaborated, while the reduction of switching losses in outer devices by using soft-switching techniques will be detailed in Section IV. Here, the mitigation of conduction losses in the outer devices is achieved by leveraging the redundant leg to share overload current with any of the main phase legs (i.e., Phase-A, Phase-B, or Phase-C), at large voltage space vectors during the normal operation of the three-level T-type inverter, as shown in Fig. 5 . For instance, at large voltage vector of (P, N, N), device S1 in the redundant leg will be used to share the load current with the outer switch S*a*1 on the Phase-A leg. Load current sharing at other large vectors is given in Table I. Such load current sharing with the redundant leg will effectively reduce the conduction losses in the outer devices. The current flow directions during the load current sharing between the Phase-A leg and the redundant leg under the normal condition is depicted in Fig. 6(a) and (b). Fig. 6(a) and (b) depicts the positive current sharing and negative current sharing, respectively. Taking Fig. 6(a) as an example, the current-sharing ratio between MOSFET S1 and IGBT S*a*1 at the steady state is determined by the devices' instantaneous on-state resistances between the two parallel conduction paths. If the current through S_1 and S_{a1} are defined as I_{s1} and I_{sa1}, respectively, the current sharing between the two paths at the steady state can be expressed as follows:

$$\frac{I_{s1}}{I_{sa1}} = \frac{R_{\mathrm{on(S}a1)}}{R_{\mathrm{on(S1)}} + R_{\mathrm{on(S}a3)} + R_{\mathrm{on(D}a2)}} \quad (1)$$

where $R_{\mathrm{on}(Sa1)}, R_{\mathrm{on}(S1)}, R_{\mathrm{on}(Sa3)}$, and $R_{\mathrm{on}(Da2)}$ refer to the instantaneous on-state resistance of devices S*a*1 , S1, S*a*3, and D*a*2, respectively. According to (1), the lower the on-state resistance of device S_1, the larger the current will be shared by the redundant leg. As a result, more conduction losses in the outer devices will be reduced.

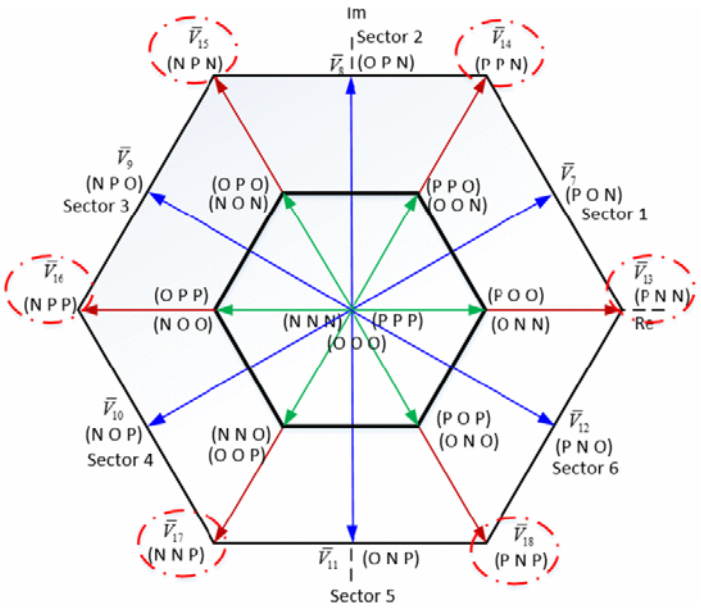


Fig. 5. Voltage space vector diagram of the three-level T-type inverter (the six large vectors that can be implemented with the current-sharing strategy are marked in red-dashed ellipses).

TABLE I Using the Redundant Leg for Load Current Sharing in the Proposed Three-Phase Four-Leg T-Type Inverter

Switching States	Redundant Devices to be Used for Load Current Sharing
(P, N, N)	Use S_1 to share with S_{a1}
(P, P, N)	Use S_4 to share with S_{c4}
(N, P, N)	Use S_1 to share with S_{b1}
(N, P, P)	Use S_4 to share with S_{a4}
(N, N, P)	Use S_1 to share with S_{c1}
(P, N, P)	Use S_4 to share with S_{b4}

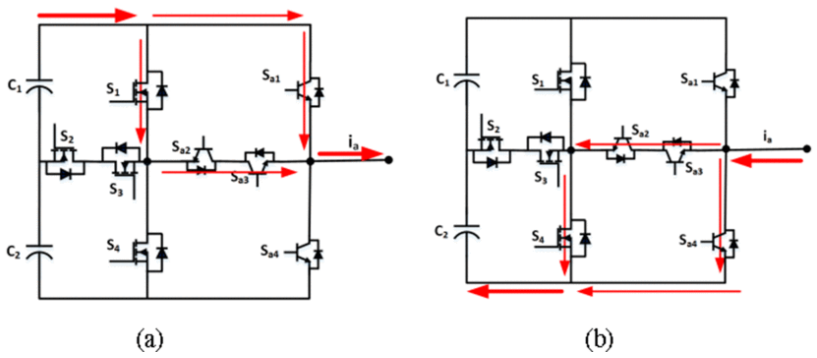


Fig. 6. Current sharing between the redundant leg and the main phase leg (Phase-A) (a) for positive load current (b) for negative load current.

The current sharing discussed above is all based on maintaining the inverter's three-level operation characteristics, in which the redundant leg can only be used at large space vectors. In other words, such load current-sharing mode is discontinuous, which can only be used for transient or short-term overload situation, such as motor drive startup. Another option for the overload operation of the proposed inverter is to operate in a continuous-load current-sharing mode between the redundant leg and the three main legs at any switching state, but the three-level inverter has to be modulated as a two-level inverter. As is known, two-level inverters have eight voltage space vectors in total, which include all the six large voltage space vectors as given in Table I and two zero voltage vectors (P, P, P) and (N, N, N). Obviously, the load current sharing with the redundant leg can be implemented in any of these eight voltage space vectors. The specific improvement of the inverter overload capability is determined by the amount of current shared by the redundant leg, which is related to the output characteristics of the power devices used in the proposed inverter, as illustrated in (1). To obtain a larger overload improvement, these outer devices on the redundant leg, i.e., S_1/S_4, can be selected with lower on-state resistance to share more load current with the IGBTs S_{x1}/S_{x4}. It is known that modulating a three-level T-type inverter as two-level incurs some performance degradation, including deteriorated common-mode voltage, higher harmonic distortion, and increased rate of change of the voltage (dv/dt). However, such two-level inverter operation with improved overload capability is still of great significance for power conversion applications with frequent overload situations, such as servo drives, EVs, and any other motor-drive applications that require frequent startups and accelerations.

SECTION IV.

Quasi-Zero-Voltage Switching and Zero-Current Switching Soft Switching

Most of the existing fault-tolerant converter topologies in the literature achieved the fault-tolerant capability at the cost of much decreased efficiency due to commutation of many redundant switching devices [7]–[10]. However, one unique feature of the fault-tolerant topology presented in this paper is the soft-switching characteristics on the IGBT devices assisted by the SiC devices in the redundant leg. Specifically, for the proposed inverter topology shown in Fig. 2, the presence of the redundant SiC leg provides a quasi-zero-voltage switching (ZVS)

and zero-current switching (ZCS) solution to the IGBTs in the T-type inverter, which will be elaborated next.

It is well known that SiC MOSFETs have much lower switching losses than their counterpart Si IGBTs due to increased switching speed of SiC devices [11]– [13]. This motivates the authors to use SiC MOSFETs in the redundant leg to undertake the switching losses for the IGBTs in the main phase legs under the healthy condition of the inverter. This is particularly beneficial for alleviating the large thermal stress on the outer IGBTs, i.e., S_{x1}/S_{x4} (x = *a* , *b*, and *c*), when the proposed inverter is operated at unity power factor. Specifically, for reducing the switching losses in the outer IGBTs, the parallel conduction path constituted by an outer MOSFET (S_1/S_4) and a middle IGBT (S_2/S_{x3}) provides an opportunity of reducing the switching voltage across S*x*1/S*x*4 to only several volts (i.e., quasi-ZVS). This can be achieved simply by earlier turning on all the devices on the parallel conduction path but turn them off later, compared to the switching timing of IGBTs S_{x1}/S_{x4}. Such a switching sequence is similar to that for Si/SiC parallel-connected hybrid devices, as investigated in [14]–[19]. Furthermore, to eliminate the switching losses in the middle IGBTs S*x*2/S*x*3 during this process, the SiC MOSFETs S_1/S_4 in the redundant leg is turned on later but turned off earlier, compared to the switching timing of the middle IGBTs S_{x2}/S_{x3}. In other words, the SiC MOSFETs, S_1/S_4, are used to interrupt the load current for the switching of the middle IGBTs (i.e., ZCS). Such quasi-ZVS coupled with the ZCS switching strategy is depicted in Figs. 7 and 8 for positive and negative currents of the inverter, respectively.

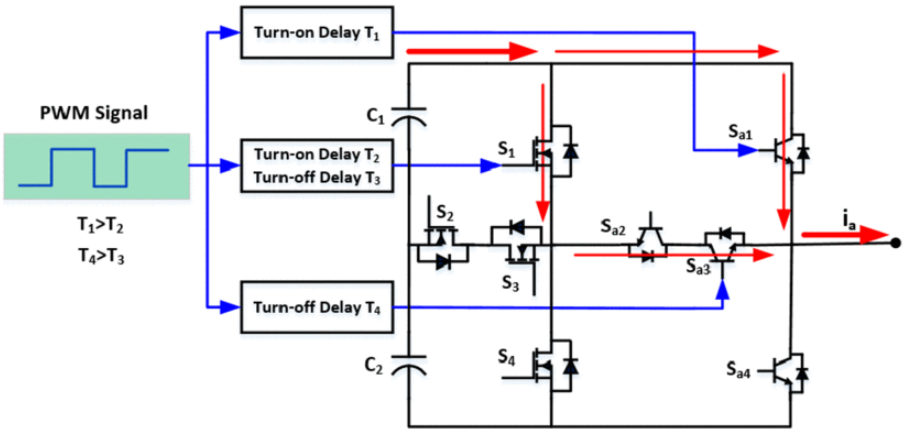


Fig. 7. Quasi-ZVS and ZCS switching strategy during positive output voltage of the Phase-A leg of the T-type inverter at positive output current condition.

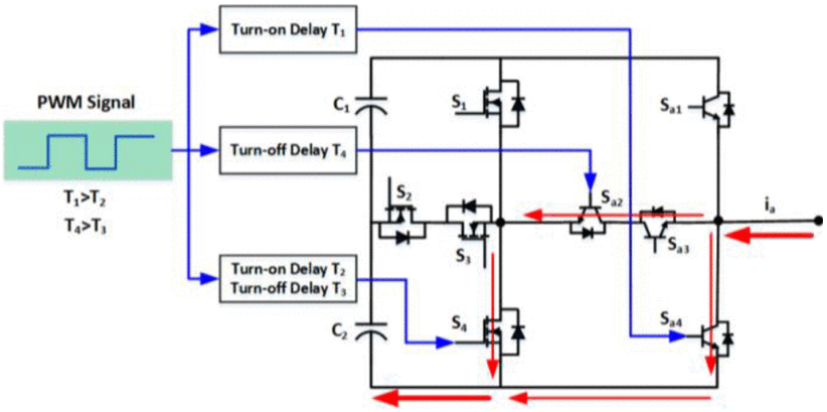


Fig. 8. Quasi-ZVS and ZCS switching strategy during negative output voltage of the Phase-A leg of the T-type inverter at negative output current condition.

It should be noted that this novel soft-switching strategy can only be applied at the six large voltage vectors of the three-level modulation or any voltage vectors of the two-level modulation of the proposed T-type inverter. Otherwise, a dc-bus shoot-through fault may occur due to the simultaneous turn-on of S_1 and S_2, or S_3 and S_4. To further illustrate this ZVS and ZCS switching strategy, detailed procedures are given below based on an example of reducing the switching losses in S_{a1} on the Phase-A leg.

1) Procedures for achieving the ZVS turn-on of S_{a1}

1. First, turn on the middle IGBT S_{a3} at large voltage vectors, which is a zero current turn-on (i.e., ZCS).
2. After a short delay to make sure that S_{a3} is completely turned on (e.g., 1μs), switch on the SiC MOSFET S_1, and the current will flow from dc source to the output terminal of Phase-A leg. This will reduce the voltage across the S_{a1} from the value of a dc-bus voltage to only a few volts. Here, for instance, the switching-on voltage of S_{a1} is determined by the on-state voltages of S_1, S_{a3}, and D_{a2} (antiparallel diode of S_{a2}) on the parallel propagation path as shown in Fig. 7 , which can be expressed as follows:

$$V_{\text{turn-on}(sa1)} = V_{\text{on}(S1)} + V_{\text{on}(Sa3)} + V_{\text{on}(Da2)} \quad (2)$$

where $V_{\text{turn-on}(sa1)}$ refers to the turn-on voltage across S_{a1}. $V_{\text{on}(S1)}$, $V_{\text{on}(Sa3)}$, and $V_{\text{on}(Da2)}$ refer to the on-state voltage of the SiC MOSFET S_1, and IGBT S_{a3}, and the free-wheeling diode D_{a2}, respectively.

3. After another short delay (e.g., 1μs) following the turn-off on of the SiC MOSFET S_1, S_{a1} is turned on at quasi ZVS.

2) Procedures for achieving the ZVS turn-off of $\mathbf{S_{a1}}$

1. First, turn off the IGBT $\mathbf{S_{a1}}$. Since the parallel conduction path constituted by the SiC MOSFET S_1 is still conducted, the voltage across $\mathbf{S_{a1}}$ is very low, which is a quasi ZVS turn-off.
2. After a short delay to make sure that S*a*1 is completely turned off (e.g., 1μs), turn off the SiC MOSFET S_1 to interrupt the load current.
3. After another short delay (e.g., 1μs) following the turn-on of SiC MOSFET S_1, S_{a3} is turned on at zero current (i.e., ZCS).

Similar procedures can be applied on other outer IGBTs in the proposed T-type inverter, which can significantly alleviate the thermal stress on these devices. Meanwhile, the loss reduction in these outer IGBTs will compensate the conduction losses of the SiC MOSFETs S_1/S_4 during normal operation. According to the ZVS and ZCS procedures given above, it can be seen that the soft switching in the outer and middle IGBTs is achieved by leveraging the hard switching of the SiC MOSFETs on the redundant leg. However, as it is known, the switching losses in the SiC MOSFETs are typically much lower than these in the Si IGBTs. Simulation and experimental results to be given in Sections V and VI will verify such soft-switching characteristics of this proposed T-type inverter.

SECTION V.

Simulation Results

To verify the fault-tolerant capability, overload current sharing, as well as ZVS and ZCS soft-switching characteristics of the proposed three-level four-leg T-Type inverter, simulation and thermal modeling are carried out in PLECS software environment. Simulation results will be given in the following subsections to confirm the aforementioned performance of this proposed T-type inverter.

A. Pulse Width Modulation Switching Strategy

In this paper, the PWM strategy used for the proposed fault-tolerant T-type inverter is space vector pulse width modulation (SVPWM), which is implemented by injecting a zero-sequence signal into the sinusoidal reference signals. Assuming that the duty ratio for each phase of the T-type inverter can be written as follows:

$$\begin{cases} d_a = m_a \cos(\theta) \\ d_b = m_a \cos(\theta - 2\pi/3) \\ d_c = m_a \cos(\theta - 4\pi/3) \end{cases} \quad (3)$$

where m_a is the amplitude modulation index, and θ is the initial phase angle. It follows that the instantaneous maximum and minimum duty ratio will be

$$\begin{aligned} d_{max} &= max(d_a, d_b, d_c) \\ d_{min} &= min(d_a, d_b, d_c). \end{aligned} \quad (4)(5)$$

The injected zero-sequence signal is defined as

$$d_0 = -(d_{max} + d_{min})/2. \quad (6)$$

With the injection of such a zero-sequence signal, the duty ratio for each main phase of the T-type inverter under SVPWM can be written as

$$\begin{cases} d_{a,SV} = m_a \cos(\theta) + d_0 \\ d_{b,SV} = m_a \cos(\theta - 2\pi/3) + d_0 \\ d_{c,SV} = m_a \cos(\theta - 4\pi/3) + d_0. \end{cases} \quad (7)$$

Regarding the switching strategy for the redundant leg in the proposed T-type inverter, it depends on the health condition of the original T-type inverter as well as the load condition. A flowchart for the switching strategy of the SiC MOSFETs on the redundant leg is shown in Fig. 9. As it can be seen in this flowchart, there are three operation modes of the proposed T-type inverter, namely, fault-tolerant operation mode, two-level continuous overload operation mode, and three-level discontinuous overload operation mode. The switching patterns are different between these three operation modes, which have been elaborated in Sections II–IV of this paper, respectively.

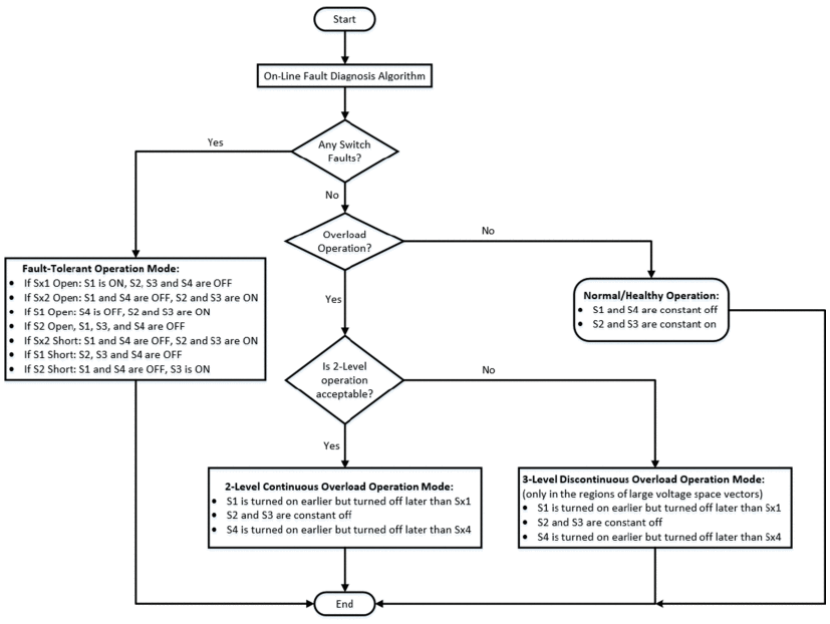


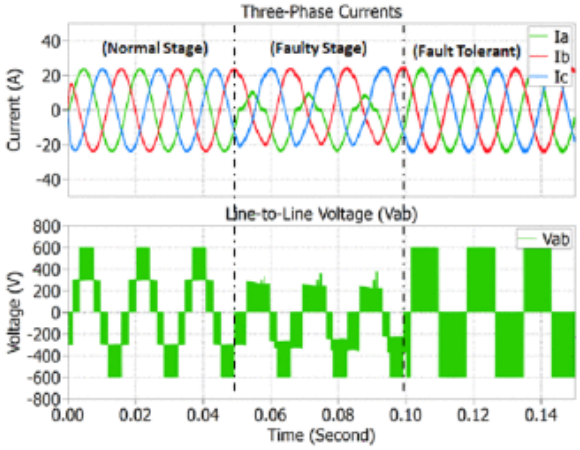
Fig. 9. Flowchart for the switching pattern of the SiC devices on the redundant leg in the proposed three-level fault-tolerant T-type inverter (note: $x = a, b,$ or c, for S_{x1}, S_{x2}, S_{x3}, and S_{x4} mentioned in the flowchart).

B. Fault-Tolerant Operation

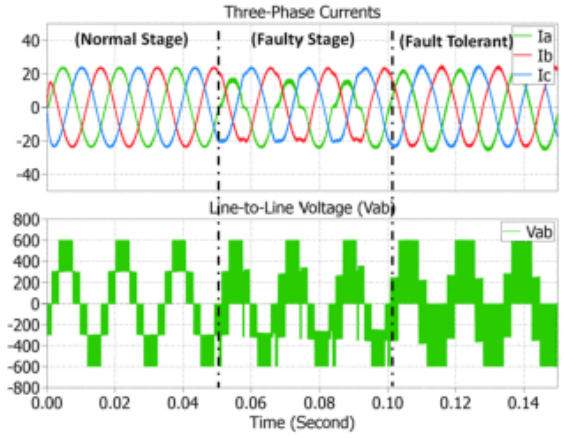
Simulations for different switching fault scenarios and their associated fault-tolerant operations are conducted in PLECS. In the simulation, the dc-bus voltage is set at 600 V, and the switching frequency and output fundamental frequency are 5kHz and 60Hz, respectively. A wye-type three-phase resistive-inductive (*RL*) load is connected to the inverter in the simulation, and the *RL* values and other inverter parameters are given in Table II. The simulation results showing the fault-tolerant operation for three representative open-circuit switching faults in the proposed T-type inverter are given in Fig. 10(a) –(c). In Fig. 10(a), the three-phase currents (i_a, i_b, and i_c) and the line-to-line voltage (V_{ab}) waveforms under the conditions of normal operation, S_{a1} open-circuit faulty condition, and the related fault-tolerant operation are demonstrated, which are consistent with the analysis in Case I of Section II. As can be seen, during the open-circuit faulty operation of the inverter (between $t = 0.05$s and $t = 0.1$s), the line-to-line voltage *Vab* and the Phase-A current *ia* lose part of the positive cycle, which is due to the open-circuit fault occurring in S*a*1, thus resulting in no access to the positive dc bus at positive current for Phase-A leg. However, as mentioned in Case I of Section II, the faulty device S_{a1} can be replaced by the upper device S_1 in the redundant leg to achieve fault-tolerant operation, as shown in the simulation results between $t = 0.1$s and $t = 0.15$s in Fig. 10(a). It can be observed that the harmonic distortion in the phase currents during fault-tolerant operation is slightly higher compared to that in normal stage, which is caused by the two-level voltage modulation of the inverter.

TABLE II System Parameters Used in the Simulation of a 20-kW Inverter Based on the Proposed T-Type Inverter Topology

Parameter	**Value**
DC-bus voltage	600V
Rated power	20 kW
Switching frequency	5 kHz
Output fundamental frequency	60 Hz
Modulation index	0.8
Load resistance per phase	10 Ω
Load inductance per phase	500 μH



(a)



(b)

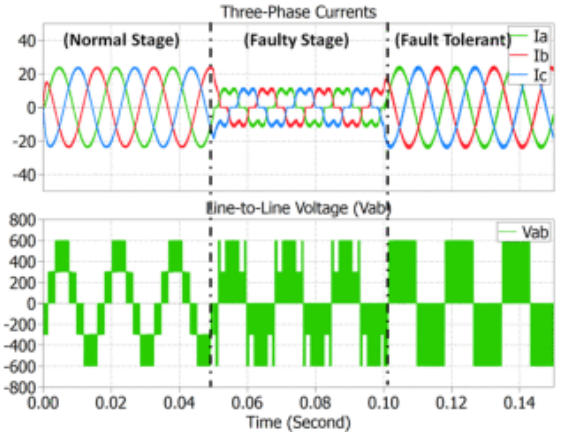


Fig. 10. Simulated three-phase currents (i_a, i_b, and i_c) and line-to-line voltage (V_{ab}) during normal operation, faulty operation, and fault-tolerant operation under the condition of (a) open-circuit fault in S_{a1}, (b) open-circuit fault in S_{a2}, and (c) open-circuit fault in S_2 of the redundant leg.

For the middle IGBT S_{a2} open-circuit faulty condition, the simulated phase currents and line-to-line voltage waveforms are shown in Fig. 10(b). It can be observed that the line voltage (V_{ab})

still exhibits three-level waveform during fault-tolerant operation region (between $t = 0.1$s and $t = 0.15$s), as analyzed in Case II of Section II. Similarly, the simulation results for S_2 open-circuit fault are shown in Fig. 10(c), which is consistent with the analysis presented in Case III of Section II. It can be seen that the proposed fault-tolerant T-type inverter can output full voltage and current during postfault operation for any of the aforementioned open-circuit switching faults.

The simulation results for the fault-tolerant operation of three representative short-circuit switching faults are shown in Fig. 11(a)–(c). As shown in Fig. 11(a) and (b), the three-level inverter has to be modulated as a two-level inverter during the fault-tolerant operation of short-circuit faults in the IGBT S_{a2} and MOSFET S_1. For a short-circuit fault in the MOSFET S_2, it should be noticed that such a fault does not affect the three-level voltage and current waveforms, as shown in Fig. 11(c). In conclusion, the inverter can still output full voltage and current during any of these short-circuit switching faults.

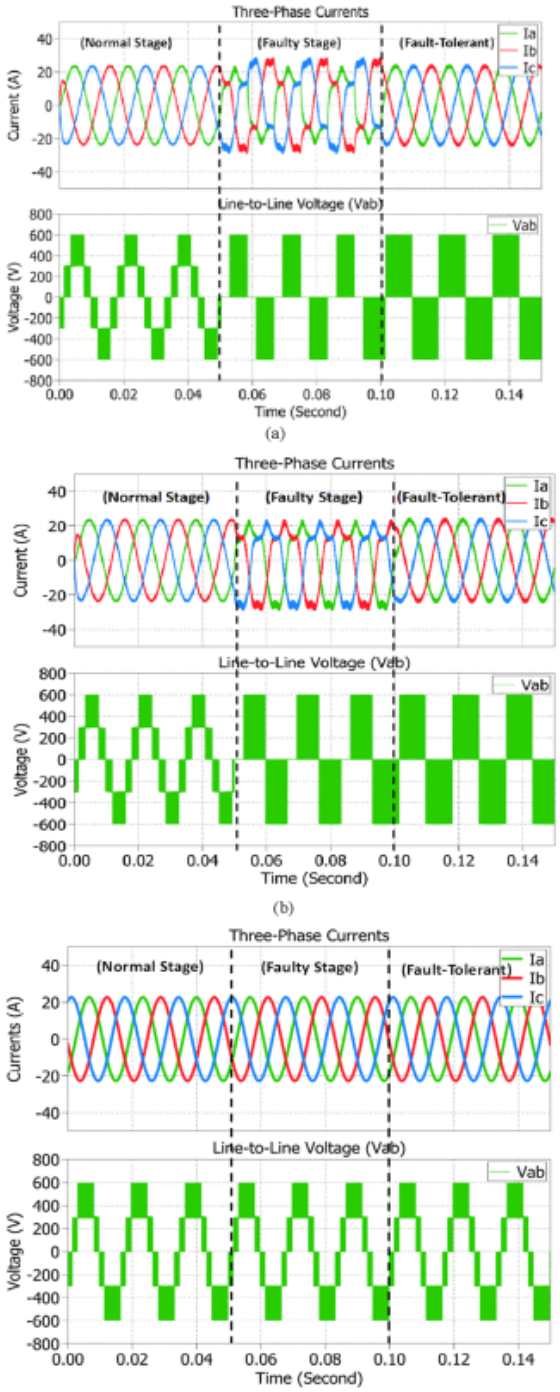


Fig. 11. Simulated three-phase currents (i_a, i_b, and i_c) and line-to-line voltage (V_{ab}) during normal operation, faulty operation, and fault-tolerant operation under the conditions of (a) short-circuit fault in S_{a2}, (b) short-circuit fault in S_1 of the redundant leg, and (c) short-circuit fault in S_2 of the redundant leg.

C. Overload Improvement

As mentioned in Section III, the overload capability of a power inverter is mainly determined by the thermal constraints of the power devices in the inverter. To investigate the thermal performance of the proposed inverter, thermal models of each semiconductor device in the proposed T-type inverter have been developed in PLECS. To keep consistent with the experimental verification to be given in Section VI, a Fuji T-type IGBT module (12-in-one package) 12MBI50VX-120-50 (1200 V/50 A) is used to constitute the conventional T-type inverter [20]. The redundant SiC phase leg is modeled based on using four SiC MOSFETs from Wolfspeed C2M0040120D (1200 V/60 A), with external antiparallel connected SiC Schottky diodes C4D40120D (1200 V/50 A) [21]. All the device thermal models are based on the devices' output characteristics (i.e., $I(V, T_j)$) curves), switching energy curves (i.e., $E_{\text{on}}(i, T_j)$ and $E_{\text{off}}(i, T_j)$), and transient thermal impedance curves ($Z_{\text{th\_jc}}$) given in the datasheets from the device manufacturers [20], [21]. In the thermal models, the ambient temperature is set at 50 °C, and a virtual heatsink is employed to absorb the thermal losses dissipated from all the semiconductor components within its boundaries. Meanwhile, the heatsink provides an isotherm environment and propagates its temperature to the power components it encloses. Again, the switching frequency and output fundamental frequency of the inverter are set at 5 kHz and 60 Hz, respectively. Under an overload percentage of 150% condition, the simulated currents in the redundant leg and Phase-A leg with/without adopting the current-sharing strategy are shown in Fig. 12. It can be seen that the peak current in the outer IGBTs in Phase-A leg is reduced from 60 to 48.8 A by adopting the current strategy, which indicates a 23% improvement of the inverter overload capability in this case. Accordingly, the simulated junction temperature profiles in the IGBT S_{a1} without and with using the redundant leg for overload current sharing are given in Fig. 13. It can be seen that the peak junction temperature in the outer IGBT S_{a1} is reduced from 92.5 to 84 °C.

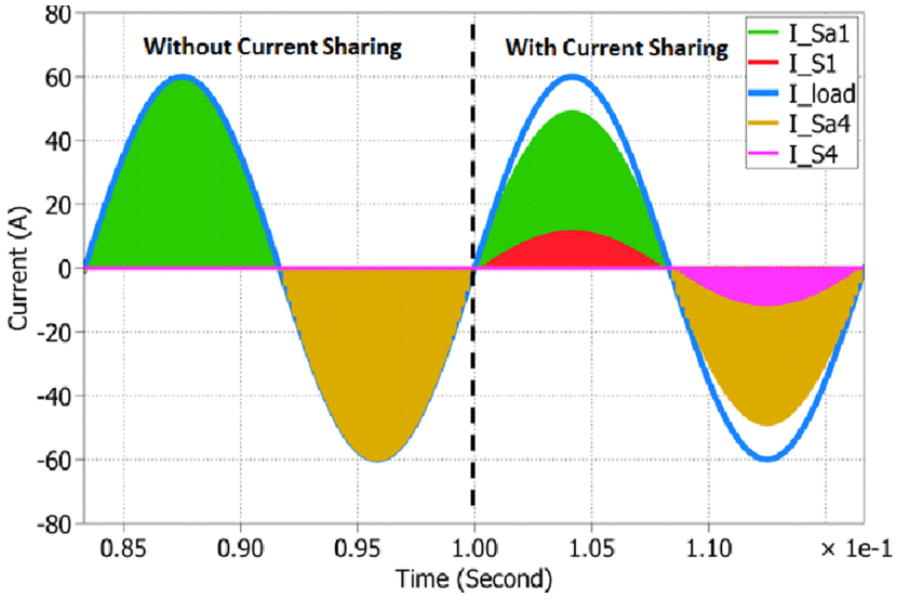


Fig. 12. Currents in the redundant leg and Phase-A leg without/with using the overload current-sharing strategy (150% overload percentage).

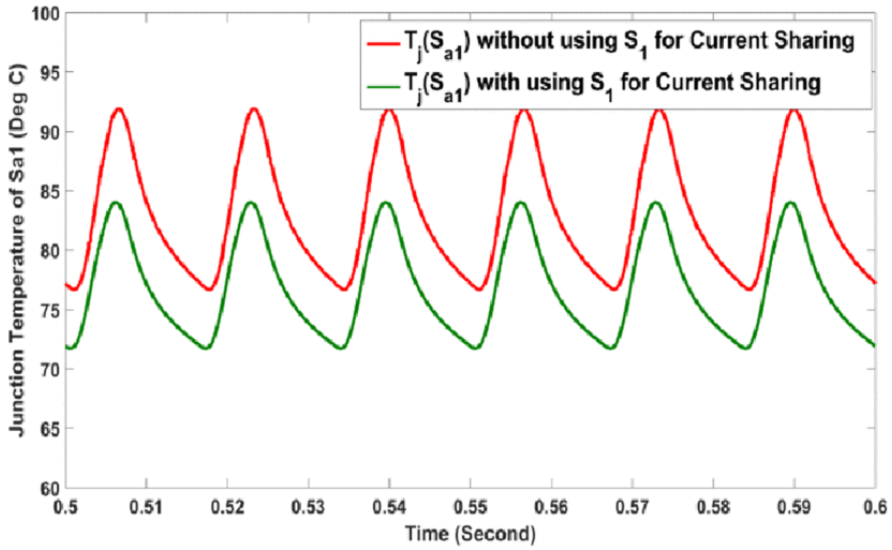


Fig. 13. Simulated junction temperature profiles of IGBT S_{a1} under the condition of without/with using the redundant SiC leg for 150% overload current sharing at large vectors (ambient temperature $T_{\text{amb}} = 50^{\circ}\text{C}$).

D. Soft-Switching Operation

Simulation results that demonstrate the ZVS operation of the IGBT S*a*1 and the ZCS operation of the IGBT S_{a3} in the Phase-A leg of the T-type inverter are given in Fig. 14(a)–(d). Fig. 14(a) shows the time sequence of the PWM or gate signals of MOSFET S_1, IGBT S_{a1}, and IGBT S_{a3}. Fig. 14(b) shows the current sharing between the redundant SiC leg and the Phase-A leg during the conduction mode and the switching mode. Fig. 14(c) illustrates the ZVS operation of the IGBT S_{a1}, and Fig. 14(d) depicts the ZCS operation of the IGBT S_{a3}. It should be noted that the device voltage in Fig. 14(c) and (d) is demonstrated by multiplying a gain of 0.1, in order to match the scale of the device current for better visual effect.

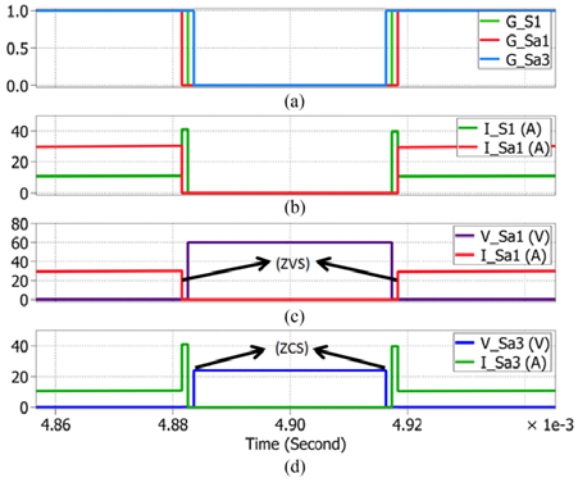


Fig. 14. Simulated switching waveforms showing (a) switching sequence of the MOSFET S_1, IGBT S_{a1}, and IGBT S_{a3} during ZVS and ZCS operations, (b) the current sharing between the SiC redundant leg

and Phase-A leg, (c) ZVS of IGBT S_{a1}, and (d) ZCS of IGBT S_{a3}, under the condition of positive output voltage and positive output current condition of the proposed T-type inverter (note: the device voltage in Fig. 14(c) and (d) is shown by multiplying a gain of 0.1 to match the scale of the device current for better visual effect).

With the ZVS and ZCS soft-switching strategies presented above, the device loss distribution is simulated and compared between the conventional T-type inverter and the proposed fault-tolerant four-leg T-type inverter. The inverter simulation is carried out at unity power factor (i.e., $\cos(\alpha) = 1$) and an ambient temperature of $T_{\text{amb}} = 50^{\circ}\text{C}$. The related simulated device loss data at 100% load condition is given in Table III. As shown in this table, both the conduction losses and switching losses in the outer devices S_{x1}/S_{x4} (*x*=*a*, *b*, or *c*) is reduced in the proposed T-type inverter, which results from the load current-sharing and soft-switching strategy by using the redundant leg. The conduction losses in the middle devices, S_{x2}/S_{x3} (*x*=*a*, *b*, or *c*), are slightly increased due to the additional conduction of S_{x2}/S_{x3} for connecting to the redundant leg for load current sharing and soft switching. It can also be seen that the conduction losses in the middle devices S_2/S_3dominate the losses from the redundant leg, which will slightly decrease the efficiency of the proposed T-type inverter. Accordingly, efficiency comparison between the conventional T-type inverter and the proposed T-type inverter is shown in Fig. 15. As can be seen, only a maximum efficiency drop of 0.4% is shown in the proposed fault-tolerant T-type inverter at 150% overload condition. Such a slight efficiency drop is mainly due to the conduction losses from the middle SiC MOSFETs in the redundant leg.

TABLE III Device Loss Comparison Between the 20-kW Conventional T-Type Inverter and the Proposed T-Type Inverter Topology Under 100% Load condition (Conditions: cos(*α*)= 1, *T*amb=50◦C)

NA	Conventional T-Type Inverter		The Proposed T-Type Inverter	
Device	P_{con} (Watts)	P_{sw} (Watts)	P_{con} (Watts)	P_{sw} (Watts)
S_{a1}	27.13	4.85	22.27	1.24
D_{a1}	0	0	0	0
S_{a2}	8.47	0.94	9.66	0.83
S_1	0	0	2.94	1.57
D_1	0	0	0	0
S_2	0	0	16.2	0
D_2	0	0	14.7	0
P_{total} (Watts)	248.34 (inverter loss)		274.82 (inverter loss)	

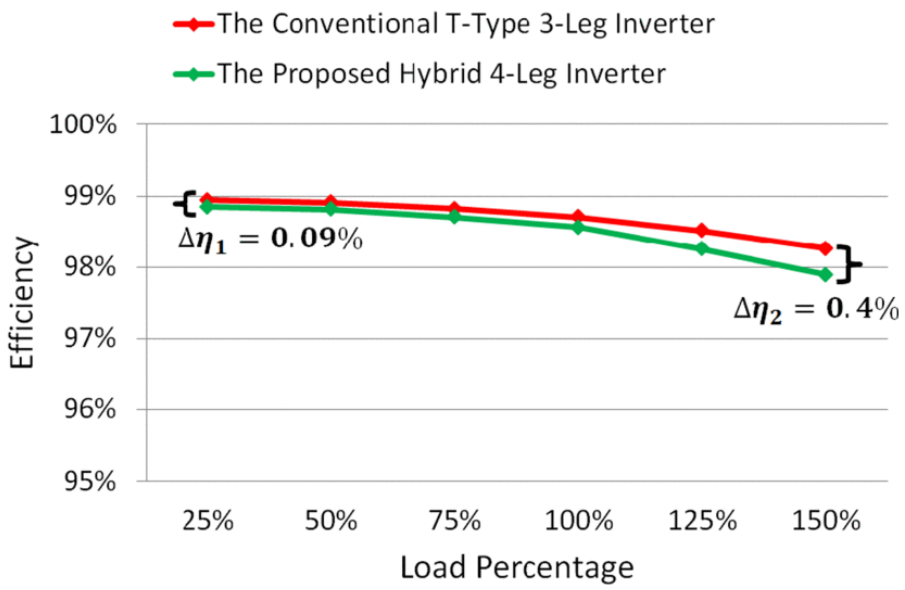


Fig. 15. Simulated efficiency comparison between the conventional T-type inverter and the proposed three-phase four-leg hybrid T-type inverter at various load conditions ($\cos(\alpha) = 1$, $T_{\text{amb}} = 50^{\circ}\text{C}$).

SECTION VI.

Experimental Verifications

In order to experimentally verify the fault-tolerant capability, soft switching, and the load current-sharing characteristics of this proposed three-level four-leg T-Type inverter, a 20-kW three-phase inverter prototype based on this novel fault-tolerant T-type inverter topology has been implemented in the laboratory, as shown in Fig. 16. Again, to keep consistent with the hardware configurations used in the simulation in Section V, a Fuji T-type IGBT module (12-in-one package) 12MBI50VX-120-50 (1200 V/50 A) is used in the prototype to constitute the conventional T-type inverter [20]. The redundant SiC phase leg is built based on using four SiC MOSFETs from Wolfspeed C2M0040120D (1200 V/60 A), with external antiparallel-connected SiC Schottky diodes C4D40120D (1200 V/50 A) [21]. All the other main operating parameters of the inverter prototype are maintained the same as the simulation parameters given in Table II.

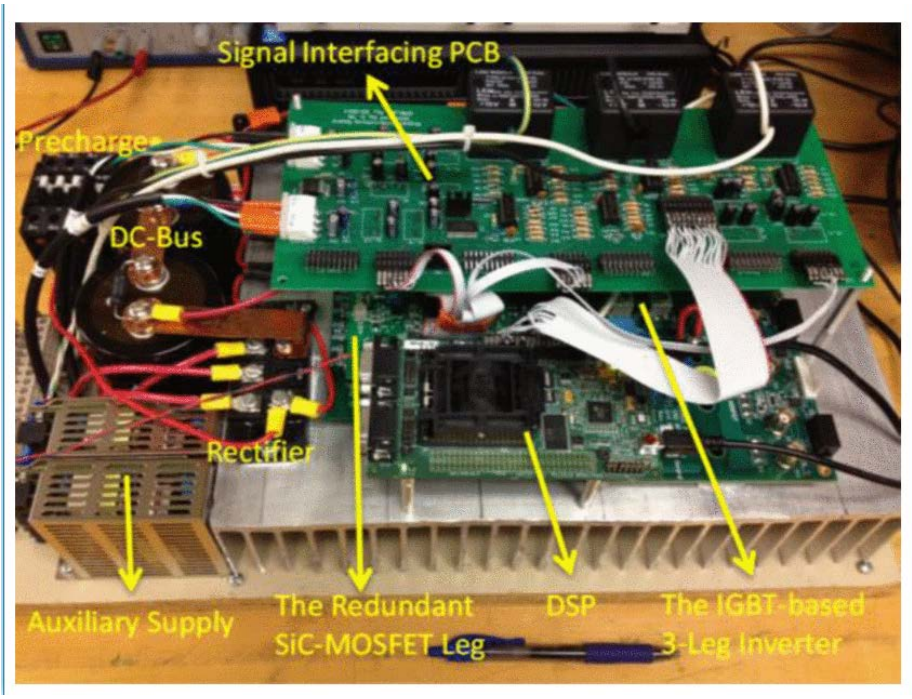


Fig. 16. 20-kW three-phase inverter prototype based on the proposed four-leg T-type inverter topology with Si and SiC hybrid phase legs.

In the experiments, open-circuit faults are emulated by disabling the PWM signals of the switching devices. The experimental results given in Fig. 17(a)–(c) verified the fault-tolerant capability of this three-phase four-leg T-type inverter for the three representative open-circuit fault scenarios, namely, open-circuit fault in S_{a1}, open-circuit fault in S_{a2}, and open-circuit fault in S_2, respectively. These test results show good agreement with the simulation results given in Fig. 10(a)–(c). Thus, the explanation of these results will not be repeated. Likewise, the three representative short-circuit fault scenarios are tested and shown in Fig. 18(a)–(c). In all these test results, the first three cycles refer to the normal/healthy operation, the next three cycles exhibit the open-switch faulty operation with distorted currents and voltages, and the last three cycles demonstrate the fault-tolerant operation under the assistance of the redundant leg. It can be seen that there is no magnitude derating in the output voltages and currents during all these fault-tolerant operation stages. Also, for all the switching faults except the short-circuit fault in S2, it can be observed that the harmonic distortions in the phase currents during fault-tolerant operations are slightly higher than these under healthy conditions, which is due to the two-level voltage output during postfault operations. However, in safety-critical applications of power converters, fault-tolerant operation is superior to harmonic distortions in the output currents.

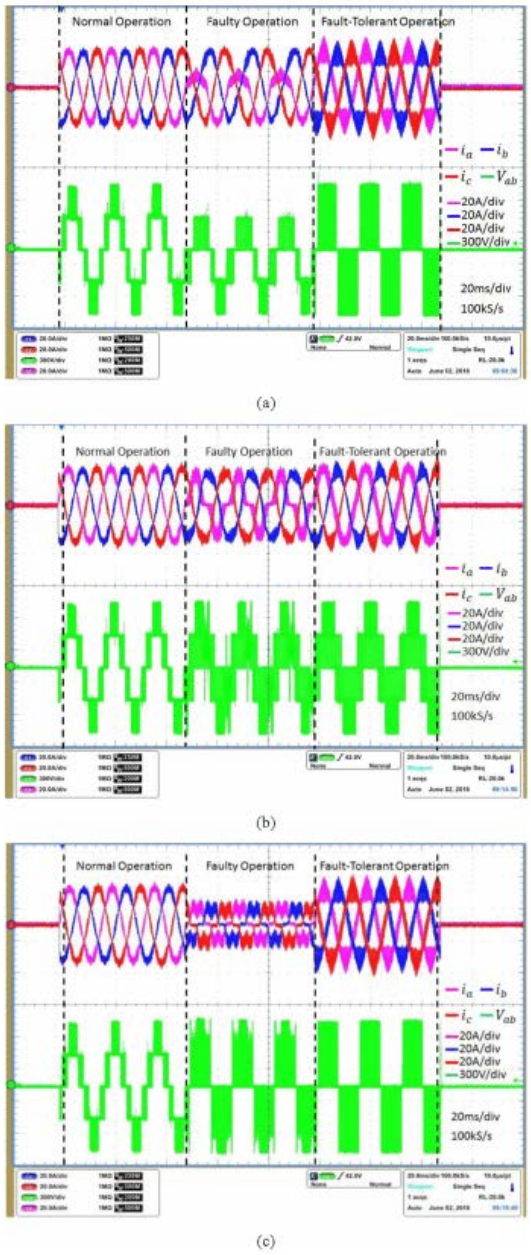


Fig. 17. Measured three-phase currents (i_a, i_b, and i_c) and line-to-line voltage (V_{ab}) during normal operation, faulty operation, and fault-tolerant operation under the conditions of (a) open-circuit fault in

S_{a1}, (b) open-circuit fault in S_{a2}, (c) open-circuit fault in S_2 of the redundant leg.

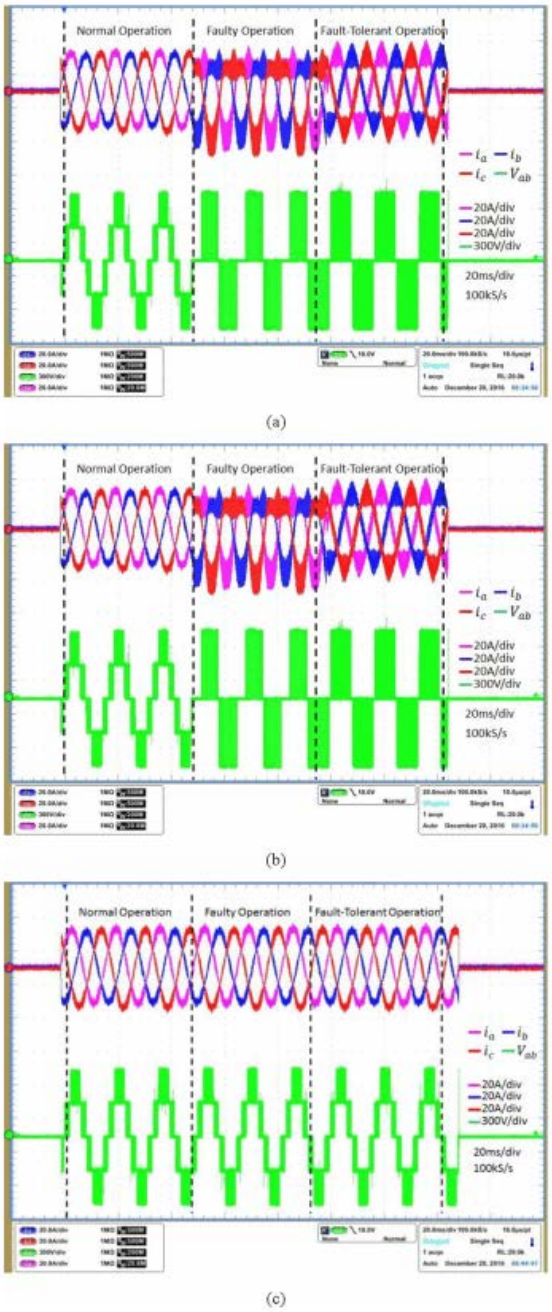


Fig. 18. Measured three-phase currents (i_a, i_b, and i_c) and line-to-line voltage (V_{ab}) during normal operation, faulty operation, and fault-tolerant operation under the conditions of (a) short-circuit fault in S_{a2} (b) short-circuit fault in S_1 of the redundant leg (c) short-circuit fault in S_2 of the redundant leg.

In addition, the ZCS and quasi-ZVS soft-switching characteristics in the IGBTs of the proposed T-type inverter are tested and demonstrated in Fig. 19(a) and (b). Fig. 19(a) shows the turn-on of the IGBT S_{a3} at zero current when the load current is positive, which results from the later turn-on of the SiC MOSFET S1. Fig. 19(b) shows the turn-on of the IGBT S_{a4} at zero voltage when the load current is negative, due to the prior turn-on of the SiC MOSFET S_4, as indicated

by the measured gate signal (V_{gs}) and drain current (i_d) in S_4. Moreover, the load current sharing between the redundant leg and the Phase-A leg under both positive and negative load current conditions is demonstrated in Fig. 20(a) and (b), respectively. Taking Fig. 20(a) as an example, the decrease in the middle of the current waveform of the IGBT S_{a1} (in dark blue) indicates the current shared by the SiC MOSFET S1 [separately shown in purple in Fig. 20(a)]. It should be noticed that the current spikes in the MOSFET drain current in Fig. 20(a) and (b) derives from the rapid turn-on and the undesired dc-bus bar design (high parasitic inductance), which will be optimized in future work.

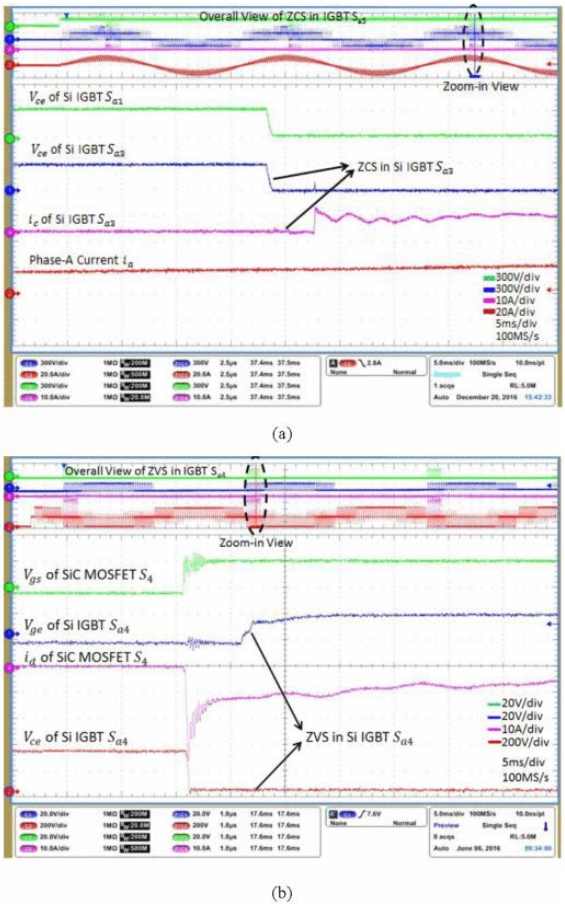


Fig. 19. Measured soft-switching waveforms in Si IGBTs S_{a3} and S_{a4} with the assistance of the SiC redundant leg (a) ZCS in IGBT S_{a3} and (b) quasi-ZVS in IGBT S_{a4}.

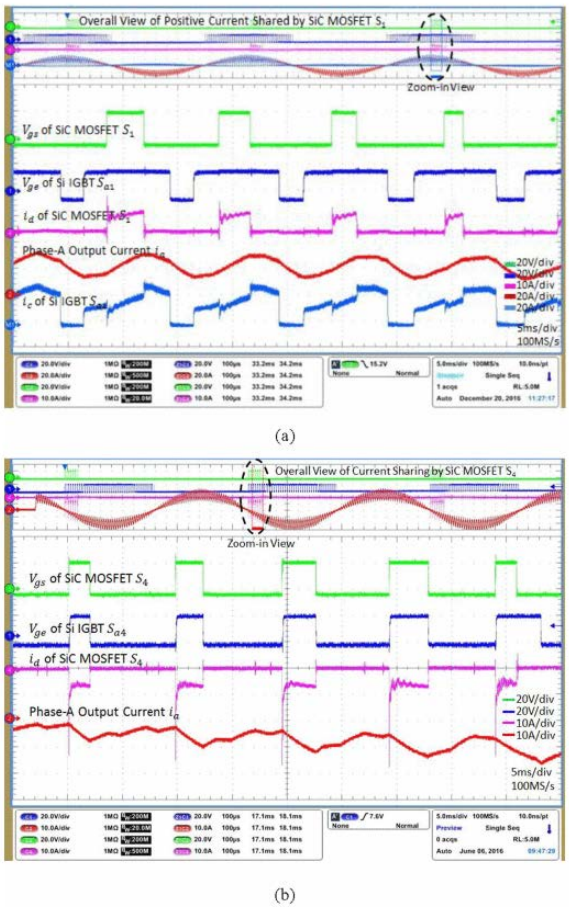


Fig. 20. Measured load current sharing between the SiC redundant leg and Phase-A leg under the condition of (a) positive load current and (b) negative load current.

SECTION VII.

Conclusion

In this paper, a fault-tolerant three-phase three-level inverter topology based on the conventional T-type inverter has been introduced. According to the analysis, simulation, and experimental results presented above, a few conclusions can be drawn as follows.

1. The fault-tolerant inverter topology presented here provides improved fault-tolerant solutions to device open-circuit and short-circuit faults that could occur in T-type inverters. During postfault operation of any of the aforementioned device faults, the inverter is still able to output full voltages/currents as that in normal operation. In other words, no derating is required during fault-tolerant operation. Although the harmonic distortions in the phase currents are slightly increased during some of the fault-tolerant operation mode due to the two-level modulation, the reliability of the inverter has a higher priority than harmonic distortions, especially in safety-critical applications.
2. Under the normal healthy condition, the redundant SiC inverter leg helps share the load current with the main phase legs of the original T-type inverter at large voltage space

vectors. Therefore, it can enhance the inverter overload capability. More importantly, under an unexpected continuous overload conditions, the inverter overload capability can be boosted by 23% in this case, if the T-type inverter is modulated as a two-level inverter and the redundant leg is controlled to share continuous overload current with the main phase legs.

3. By adopting a quasi-ZVS and ZCS strategy through the utilization of the SiC MOSFETs in the redundant phase leg, the losses in the IGBTs of the conventional T-type inverter can be significantly reduced. Particularly, the thermal stress in the outer IGBT devices (S_{x1} and S_{x4}, *x*=*a*,*b*,or *c*) is effectively mitigated at unity power factor condition.

Finally, the circuit topology in this proposed fault-tolerant four-leg T-type inverter has a modular structure and, therefore, will be very suitable for power module packaging and manufacturing, which makes the commercialization of such fault-tolerant power converters more feasible.

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