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A Novel Batch-processing Method for Accurate Crystallographic Axis Alignment

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Abstract

A new method for the accurate alignment of lithographically-defined patterns to the crystallographic axes of substrates is presented. We provide a lower (worst-case) limit of the achievable high aspect ratio using anisotropic wet chemical silicon etch for deep trenches. The method uses the fact that the intensity of light reflected from two sets of gratings, one on the photomask and the other on the substrate, is a sharp function of their relative angular misalignment. By using pre-etched gratings on the substrate formed by wet anisotropic etching, alignment accuracies better than 50 millidegrees with respect to silicon crystallographic axes have been demonstrated. Two types of microstructures—trenches with an aspect ratio >90:1 and silicon nanowires with

widths <50 nm with atomically smooth etched facets—have been fabricated using i-line lithography to illustrate some applications of this alignment method. This all-optical method is readily applicable to industry-standard optical lithography and avoids the need for any individualized process steps, enabling cost-effective micro/nanostructure manufacturing.

1. Introduction

Anisotropic wet chemical etching has been extensively studied and used for the fabrication of silicon micro and nanostructures [1–6], making use of high differences in etch rates between silicon's (1 1 1) family of planes and those with other Miller indices in certain alkaline etchants [7–11]. Two particular advantages of using anisotropic wet etch of silicon are the ability to produce atomically smooth etched surfaces [12] and complex 3D nanoscale shapes [13, 14], as in the case of tips for atomic force microscopy (AFM tips). Of particular interest is the use of (1 1 0)-oriented silicon substrates to produce microstructures with vertical sidewalls, since there exist two sets of (1 1 1) family of planes that are perpendicular to a (1 1 0) plane [15], giving the ability to fabricate dense, high aspect ratio structures in silicon. Such structures can be useful in many different applications. Some areas of current interest are devices that require a high surface area with minimal damage to the silicon crystalline structure such as semiconductor PN or PiN sensor arrays [16, 17] or secondary battery electrodes [18]. Other applications such as optical to x-ray diffraction gratings [19, 20] as well as some biosensors [21] can be designed to exploit vertical, atomically smooth sidewalls. In these applications, the use of deep reactive ion etch (DRIE) is not always attractive due to high levels of sidewall roughness and crystal damage generated by the process, in spite of its ability to produce structures of aspect ratios of 50:1 or better [22]. One approach to reduce the etch damage is to use anisotropic wet etchants to smoothen out rough sidewalls. Such methods offer only limited improvement unless the etch faces are exactly along (1 1 1) planes, as any other planes would result in significant undercut and/or distortion due to the anisotropy of the etch process.

2. General principles for aligning with respect to substrate crystallographic axes

The main limitation for the accurate angular alignment (henceforth simply referred to as alignment) of a designed pattern to the substrate's crystallographic axes is that major flats in the substrates that specify the crystal orientation are typically accurate to only ±0.5° [15, 23]. Such a misalignment can change the etch rate of the crystal planes and cause significant facet undercuts, resulting in the distortion of the etched structures compared to the desired structures [7]. The general method for accurate alignment to the substrate's crystallographic axes consists of first etching a set of marks using coarse alignment (e.g. using the substrate's major flat) to the substrates axes. The marks are designed to exploit the considerably lower etch rates of (1 1 1) planes compared to non-(1 1 1) planes, typically with etch rate ratios of 1:100 or lower. Examples of such patterns are wagon-wheel-shaped, wedge-shaped and fan-out gratings that are etched using anisotropic wet chemical etchants of silicon substrates, revealing silicon crystal planes [7, 24, 25]. By inspecting the relative sizes of the patterns (typically using a scanning electron microscope (SEM)) that are misaligned to the substrate's crystallographic axes by different angles, it is possible to determine which of the angles in the design coincides with the substrate's axes the closest. Using such methods, crystal alignment accuracies of 50 to 100 millidegrees (mdeg) have been demonstrated. However, the need for several sets of marks corresponding to different levels of misalignment significantly reduces the process throughput, since each substrate requires the identification and marking of the set of marks corresponding to the closest alignment.

3. A novel all-optical crystal alignment method

In this paper, a new all-optical method is presented where gratings on a photomask are aligned to pre-etched gratings on the substrate. The intensity of reflected microscope light is a strong function of the angular misalignment between the two gratings. By integrating a photodetector at the end of the eyepiece lens of a contact mask-aligner to monitor the reflected light intensity, accurate alignment to the substrate crystallographic axes is achieved without the need for individualized wafer marking or processing. We demonstrate two types of structures that were designed to exploit the high anisotropy of certain wet etchants in silicon, showing alignment accuracy of 50 mdeg or better. First is a periodic dense array of high aspect ratio trenches that are 90 μm deep, 2 μm wide and with 4 μm pitch on (1 1 0)-oriented silicon substrates. The second are 50–100 nm wide suspended silicon nanowires with atomically smooth etch facets fabricated on (1 0 0)-oriented silicon-on-insulator (SOI) substrates.

Two periodic grating patterns, one on the substrate and the other on the optical photomask, are used to align to the substrate's crystallographic axes. The gratings on the substrate are initially defined near the substrate periphery and with an orientation coarsely aligned to the substrate's major flat. The gratings are then etched using an anisotropic wet etchant. For both (1 0 0) and (1 1 0)-oriented substrates, the gratings will be bounded by (1 1 1) planes. The coarse alignment using the major flat of the substrate can easily result in ±0.5° misalignment with respect to the substrate's crystallographic axes. This misalignment can cause the (1 1 1) planes to show 'steps' along the grating sidewall [7]. A long anisotropic etch is therefore typically used to reduce the steps and to reveal the true crystal planes of the substrate. For e.g., due to the high etch rate ratio of higher Miller index planes to (1 1 1) plane, a 12 h long etch with a 30% wt/vol potassium hydroxide solution (30% KOH) at 70 °C has resulted in smooth (1 1 1) planes as shown in figure 1. This long etch is necessary to ensure that the (1 1 1) plane is a single plane along the crystal direction with minimal steps, which will be used as a reference for the device alignment.

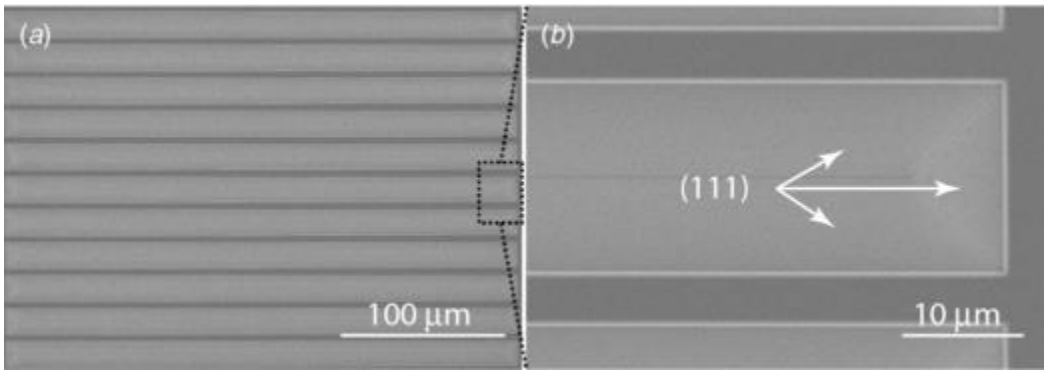

Figure 1. Rectangular gratings on the (1 0 0) silicon substrate after anisotropic wet etch. (*a*) A 12 h long etch using 30%-KOH at 70 °C. (*b*) Close-up view of the area defined by box in (*a*) showing smooth (1 1 1) crystal planes.

The gratings on the optical photomask are then aligned to the gratings on the substrate. When the gratings on the wafer and optical mask are overlapped, the location of gratings on the substrate is aligned to be parallel and alternated with respect to the gratings on the optical mask, as shown in figure 2. In this configuration, microscope light, such as one used in a mask-aligner is shone on the overlapped gratings. The intensity of the light that is normally reflected back is measured using a photodetector mounted on an eyepiece of the contact mask-aligner. When light is shone on the overlapped gratings, the light is normally reflected only by the areas between the (1 1 1) planes on the substrate and gratings on the optical mask (chromium). The etched areas on the substrate either scatter or reflect the incident light off-normally as they are non-parallel to the substrate and hence appear dark under the optical microscope. When the gratings on the substrate and the optical mask are

misaligned, the normally reflecting areas overlap each other, resulting in the reduction in the total reflected light at the photodetector, as shown in figure 2(*a*). The maximum normally reflected light intensity from the overlapped gratings is obtained when the gratings on the substrate are perfectly aligned parallel to the grating in the optical mask, as shown in figure 2(*b*). The normally reflected light intensity from the overlapped gratings is thus a strong function of the alignment of the gratings on the mask and the substrate. Crystal direction alignments of 50 mdeg have been demonstrated using this method.

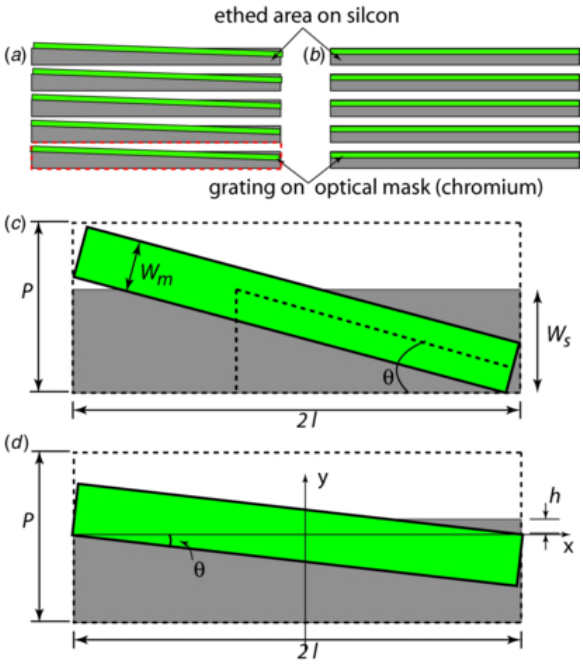

Figure 2. Schematic of alignment of gratings on wafer and optical mask: (*a*) misaligned, (*b*) aligned to the crystal direction. (*c*) Single (grating) cell illustrating the parameters of the gratings. (*d*) Close-up view of the overlapped area for calculation of fine alignment.

3.1. Initial coarse alignment

Figure 2(*a*) shows the general case where the gratings on the optical mask are slightly misaligned (θ < 0.5°) and rotated with respect to the centre of the pre-etched gratings on the wafer. The relative vertical displacement of the two gratings is such that the maximum amount of the normally reflecting portion of the gratings on the photomask overlaps the etched gratings on the wafer, thus reflecting the maximum amount of light for this angular misalignment. One cell of the grating that is periodically repeated with pitch, *P*, is shown in figure 2(*c*). The total area per cell that reflects light normally is $2Pl - 2W_s l + A_{overlap}$, where $A_{overlap}$ is the area of the etched groove that is covered by one grating in the mask. Here, W_s and W_m are the widths of each grating on the substrate and photomask, respectively, and *l* is the half-length of the gratings (on the mask and the substrate). For small angles of misalignment (i.e. θ < 0.5°), $A_{overlap}$ can be calculated as $W_m \cdot (W_s - W_m/2)/\theta$. Thus, the light intensity at the photodetector is proportional to

(1)

$$I(\theta) \propto 1 - \frac{W_s}{P} + \frac{W_m \cdot (W_s - W_m/2)}{2Pl} \cdot \frac{1}{\theta}.$$

This expression is valid until the gratings on the mask can be entirely enclosed by the gratings on the wafer, i.e. for all $\theta > \theta_{min\text{-}coarse} = (W_s - W_m)/2l$. It can be shown that this $\theta_{min\text{-}coarse}$ represents the angular misalignment of the gratings on the wafer with respect to the crystallographic axes of the substrate. Hence, the initial coarse

alignment guarantees an angular alignment better than alignment schemes only using wafer major flat ground by the manufacturer.

3.2. Fine alignment

Once the photomask and the substrate are aligned to be within $\theta_{min\text{-}coarse}$, the gratings on the optical mask are aligned to the substrate, as illustrated by the general case in figure 2(*d*). The approximate overlapped area during coarse alignment can be calculated as a function of the angular misalignment, θ. If *h* is the height of the portion of optical mask outside of the pre-etched silicon groove, then $h = l\tan\theta$. The overlapped area is $A_{overlap} = (l/2)h \approx (1/2)l^2\theta$. Therefore, the normalized light intensity can be obtained by total reflecting areas on the optical mask and wafer less the overlapped area,

(2)

$$I(\theta) \propto 1 - \frac{l}{2m} \cdot \theta,$$

where *m* is the distance between gratings on the optical mask and those on the wafer. The overlapped area is proportional to the misaligned angle and the length of the gratings. As can be seen from figure 2(*b*), the maximum reflected light will be registered on the photodetector when the gratings on the optical mask are parallel to and aligned inside the pre-etched gratings on the wafer. To maximize the signal at the photodetector, the grating length should be larger than the field of view of the microscope. The accuracy of angular alignment during fine alignment would typically be limited by the signal-to-noise ratio at the photodetector and/or the resolution of the rotation stage on the contact mask-aligner.

4. Device fabrication

Two types of nanostructure devices were fabricated to illustrate the use of this alignment method, usable for both (1 1 0) and (1 1 0)-oriented silicon substrates. Figure 3 shows the masks relative to the substrate surface type and the crystallographic axes, as coarsely defined by the major flat of the substrate.

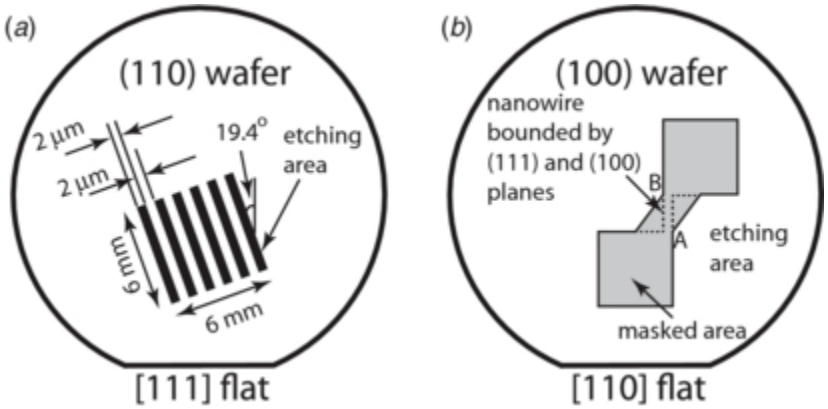

Figure 3. Device patterns. (*a*) Patterns for deep trenches on a (1 1 0) wafer with [1 1 1] major flat. (*b*) Patterns for nanowire on a (1 0 0) SOI wafer with [1 1 0] major flat.

In both cases, the fabrication process starts with low-pressure chemical vapor deposition of 300 nm of silicon-rich silicon nitride (SiN*x*). The SiN*x* film served as the etch mask to define the set of gratings on the substrate to be used for the crystallographic alignment. Substrate gratings that were 300 μm long, 10 μm wide with a 20 μm pitch were defined using a Karl–Suss MA-6 contact mask-aligner on both the (1 0 0) and (1 1 0)-oriented substrates, using the substrate major flats for coarse alignment. The grating patterns were transferred to the SiN*x* thin film using reactive ion etching (RIE). Then, the grating patterns were etched in 30% KOH at 70 °C for

12 h. Since the alignment of the substrate gratings is only approximate, the width of etched areas is typically wider than the designed value, as shown in figure 1. After the KOH etch, the SiN*x* thin film is selectively removed using hot phosphoric acid etch. The alignment method described in section 3 is then performed where the same photomask used to define the substrate gratings is aligned with respect to the pre-etched gratings on the two substrates until the light intensity at the photodetector is maximum, representing that the mask is aligned to the substrates axes with maximum possible accuracy. Two alignment marks on the photomask are lithographically transferred to the substrate. In our case, we transferred alignment keys for a GCA i-line optical stepper to the left and right of the wafer. At this stage, the silicon substrates have alignment marks that are accurately aligned to the substrate's crystallographic axes.

4.1. High aspect ratio trenches

Figure 3(*a*) shows a periodic array of a rectangular 'trench' (dark regions) structures with a width of 2 µm and a pitch of 4 µm. The trenches are 6 mm long. The pattern is designed such that the trenches are aligned to a set of (1 1 1) planes that are vertical to the (1 1 0) substrate. After the crystallographic axis alignment, a 300 nm low-stress SiN*x* is deposited on the (1 1 0) silicon substrates to serve as the etch mask during deep trench etch using KOH. The above-described pattern was transferred to the SiN*x* using RIE, and the trenches etched using a 30% KOH etch at 70 °C. The high aspect ratio trenches on the (1 1 0) wafer are shown in figure 4. Figure 4(*a*) shows the top view of the 6 mm long, 2 µm wide and 50 µm deep trenches. The total number of trenches is 1500 along the 6 mm die size. Figure 4(*b*) shows a close-up image of figure 4(*a*). Figures 4(*c*) and (*d*) show the cross-section views of the trench. Using high-magnification SEM, we estimated the maximum variation in etch depth of <1 µm. This represents a depth non-uniformity of less than 2%.

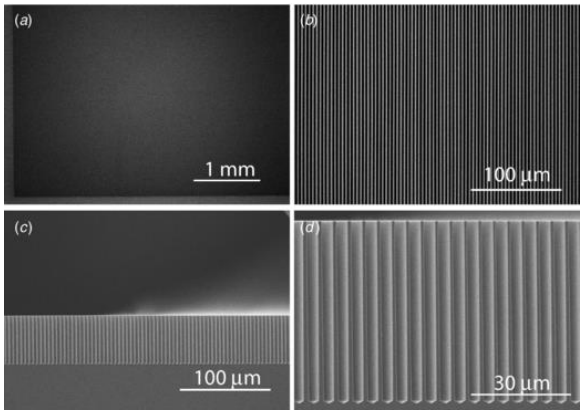

Figure 4. Deep trenches on a (1 1 0) wafer. (*a*) Top view of the 1500 trenches. (*b*) Close-up view of the (*a*). (*c*) Overview of the cross-section of the trenches. (*d*) Close-up view of (*c*).

4.2. Silicon nanowires with sub-lithography resolution widths

Figure 5(*a*) shows the designed pattern on a (1 0 0)-oriented device layer on an SOI substrate, where the grey regions represent the masked areas. The dotted lines represent the (1 1 1) planes on the substrate with respect to the [1 1 0] major flat. The etch of high Miller index planes results in a rapid undercut of the masked device layer until the (1 1 1) planes are exposed. The width of the resulting structure under the etch mask is then defined only by the offset of the masked areas (the distance between the dotted lines), which can be designed to be much smaller than optical resolution limits. By aligning to the crystal axis of the (1 0 0)-oriented device layer accurately, silicon nanowires of approximately 50 nm width and with atomically smooth sidewalls are presented below.

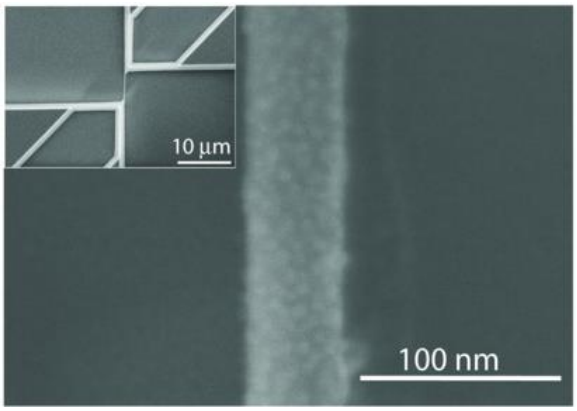

Figure 5. A fabricated suspended silicon nanowire (5 µm long, 50 nm wide and 50 nm thick). Inset is the overview of the nanowire. Due to the metal evaporation (5 nm thick) for SEM imaging, the surface and edge of the nanowire looks rough.

After accurate crystal alignment described in the previous section, a silicon dioxide (SiO_2) film was thermally grown on the (1 0 0) SOI substrates. The initial device layer thickness was 270 nm thick, which was thinned down to ~50 nm by controlled thermal oxidation. The thermally grown oxide was used as a KOH etch mask for the nanowire patterning. The corners A and B are offset with respect to the [1 1 0] direction as shown in figure 3(*b*). The offset between the A and B is the designed nanowire width bounded by (1 1 1) planes [6]. The initial offset (in mask layout) between A and B in figure 3(*b*) is 250 nm. This offset is reduced further by using a timed isotropic etch of the masking SiO_2 layer using a 6:1 solution of buffered oxide etchant (BOE 6:1). The device layer is then etched using a 30% KOH solution at 70 °C. The device layer undercuts under the SiO_2 mask until the (1 1 1) planes shown as dotted lines become exposed. Thus, silicon device layers that were 5 µm long, 50 nm wide and 50 nm thick were defined. Finally, the silicon device layer was released from the buried oxide layer using a 49% hydrofluoric acid etch to form 50 nm wide suspended silicon nanowires with atomically smooth sidewalls as shown in figure 5.

5. Discussion

Although anisotropic wet chemical silicon etches have been extensively used for micromachining and the processes well developed, the etch rates and etch profiles are typically dependent on a wide range of parameters such as doping concentration in silicon, chemical bath concentration, temperature and additives [26]. For high aspect ratio structures, the etch rate ratios of high Miller index planes to that of a (1 1 1) plane and the alignment are critical. To determine the maximum achievable aspect ratio for a given etch condition, a series of gratings were designed as shown in figure 6. Each grating set was rotated 50 mdeg successively with respect to the central grating set, up to ±1° in both directions. The grating in the centre series is designed to be aligned with the designated crystal plane direction, [1 1 1] direction in the trench array microstructure case. Using this method, the maximum possible etch depth as a function misaligned angle was experimentally obtained. The gratings most misaligned with the [1 1 1] crystal direction suffered the most severe undercut, as easily visualized by an optical microscope. Using the method described in this paper, we achieved the least amount of undercut for the grating set in the middle, indicating an alignment accuracy better than 50 mdeg.

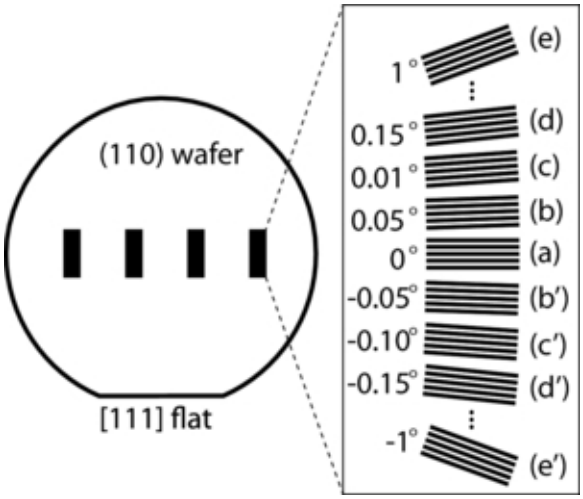

Figure 6. Printed series of gratings aligned along the pre-etched [1 1 1] direction on (1 1 0)-oriented wafer. Each grating is 0.05° rotated successively up to ±1°.

In the following, we calculate the relation between the alignment accuracy and the achievable aspect ratio of deep trenches using wet anisotropic etching. The upper bound of the allowable misalignment to fabricate the deep trenches is shown in figure 7(*a*). The distance '*b*' is determined by the misalignment angle (θ) with respect to the [1 1 1] direction and the gap between trenches, '*a*'. Then, the distance between the undercut etch front due to the misalignment can be written as

(3)

$$b = a/\sin\ \theta.$$

The etch rate of the undercut etch front (high Miller index planes) depends on the misalignment angle [7, 15]. Let α be the etch rate of (1 1 0) planes and β be the aggregate etch rate of high Miller index planes (*h k l*) for a given KOH concentration and temperature. Then, β can be expressed as β = *c* × α , where *c* is a proportionality constant that can be found experimentally by fitting the measured etch depth. The constant *c* is measured to be 1.6 in 30% KOH at 80 °C as shown in figure 7(*b*), which is close to previously reported values [27]. Then, the etch depth *d* can be expressed as

(4)

$$d = \frac{t_{hkl} \cdot \alpha}{2},$$

where t_{hkl} = *b*/β is the etch time of the high Miller index planes.

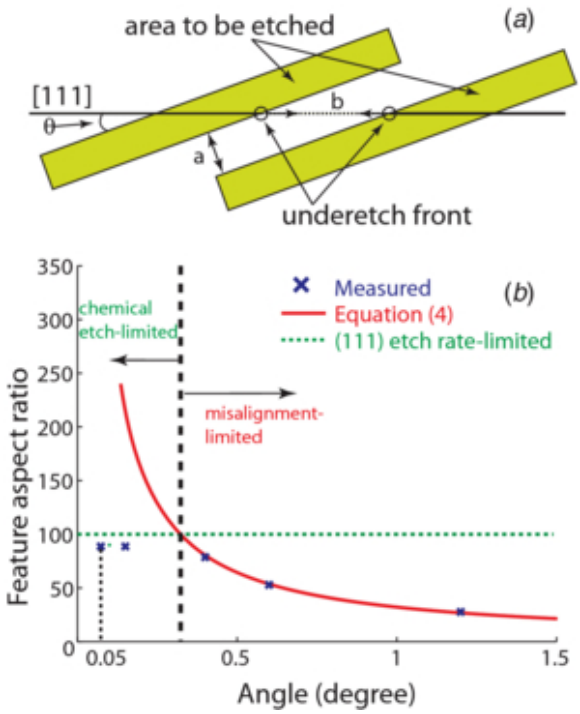

Figure 7. Limit of achievable trench depth for the case of 2 µm trench width and 4 µm pitch gratings by misalignment and (1 1 1) etch rate. (*a*) Schematic description of (*h k l*) underetch front along the [1 1 0] direction with misaligned gratings. (*b*) Etch depth as a function of misalignment angle and non-zero (1 1 1) etch rate.

Figure 7(*b*) shows the maximum trench depth as a function of the misalignment angle. Since the typical etch rate ratios of (1 1 0) and (1 0 0) planes to that of (1 1 1) are greater than 100, the undercut of high Miller index planes between the (1 1 1) plane steps (undercut front) determines the maximum etch depth before the walls etch away (laterally). The measured aspect ratio as a function of the crystal misaligned angle is shown in figure 7(*b*). For an initial spacing of 2 µm between the trench walls ('*a*'), a misalignment angle of the trench wall to the silicon (1 1 1) planes must be less than approximately 150 mdeg to etch trenches of 90 µm deep, representing an aspect ratio of ~100. This represents a point where the contribution of aspect ratio limitation due to misalignment is <10%.

In this work, an SiN*x* etch mask was designed to have 2 µm openings for the gratings and was printed using a 5× reduction i-line stepper. From figure 8(*a*), the undercut is approximately 230 nm over a 50 µm trench depth etched into the substrate using 30% KOH at 70 °C. The KOH etch selectivity we obtained between (1 1 0) and (1 1 1) planes at 70 °C was approximately 100, which is close to a previously reported value of approximately 130 [12]. Higher selectivities can be achieved using a 50% KOH solution concentration at 60 °C, resulting in even higher aspect ratios.

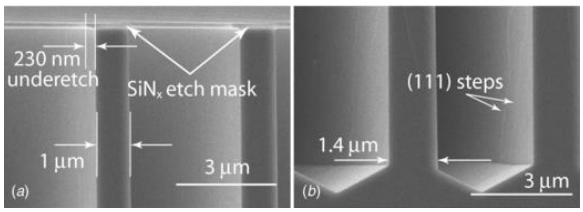

Figure 8. Close-up view of the trenches, figure 4(*d*), for misalignment analysis: (*a*) top of the wall, (*b*) bottom of the wall.

Figure 8(*b*) shows the bottom of the fabricated trenches. As indicated in the figure, (1 1 1) steps are visible in the SEM images. The (1 1 1) steps are the result of a non-zero misalignment of the trench patterns to the crystal

direction [7]. Although, the step height is difficult to measure, it is expected to be very small (of the order of a few nanometers) because of the small misalignment. The thicknesses of the walls at the top (figure 8(*a*)) and the bottom (figure 8(*b*)) are 1 and 1.4 μm, respectively. The results thus indicate that the undercut is primarily due to the finite etch rate ratio between (1 1 1) and (1 1 0) planes, approximately 100 in our case. This is also illustrated in figure 7, where an alignment to the left of the cross-over point results in microstructures limited only by the finite etch rate ratios of (1 1 1) and (1 1 0) planes in wet anisotropic etchants. As discussed above, a further increase in this ratio can result in higher aspect ratio trench structures, resulting in a misalignment-limited aspect ratio. In such cases, the practical limit of achievable alignment would be limited by the resolution of the rotation stage of the contact mask-aligner. We estimate this limit to be approximately 50 mdeg for most commercially available contact mask-aligners.

6. Conclusions

Single crystal silicon micro/nano structures are fabricated using wet chemical anisotropic etching using an all-optical method to accurately align designed patterns to the substrate's crystal directions. This method has been used to fabricate high aspect ratio trenches for dense integration and single crystal silicon nanowires using a top–down approach. Alignment accuracies better than 0.05° have been achieved using grating alignment marks and an integrated photodetector using conventional optical lithography. We provide a method to estimate the maximum depth of trenches for gratings or arrays on (1 1 0)-oriented silicon substrates. The etched facets of the structures by KOH etch result in atomically smooth (1 1 1) planes, which can be particularly useful in optical and semiconductor PN detector applications. The optical crystal alignment method introduced in this paper can expand the wet chemical anisotropic etching technique for the fabrication of various micro/nano structures.

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