Health Condition Monitoring and Fault-Tolerant Operation of Adjustable Speed Drives

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HEALTH CONDITION MONITORING AND FAULT-TOLERANT OPERATION OF ADJUSTABLE SPEED DRIVES

by

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PREFACE

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Under the supervision of Professor Nabeel A.O. Demerdash

Marquette University, 2015

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To My Family, Colleagues, and Friends

ABSTRACT

HEALTH CONDITION MONITORING AND FAULT-TOLERANT OPERATION OF ADJUSTABLE SPEED DRIVES

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Adjustable speed drives (ASDs) have been extensively used in industrial applications over the past few decades because of their benefits of energy saving and control flexibilities. However, the wider penetration of ASD systems into industrial applications is hindered by the lack of health monitoring and fault-tolerant operation techniques, especially in safety-critical applications. In this dissertation, a comprehensive portfolio of health condition monitoring and fault-tolerant operation strategies is developed and implemented for multilevel neutral-point-clamped (NPC) power converters in ASDs. Simulations and experiments show that these techniques can improve power cycling lifetime of power transistors, on-line diagnosis of switch faults, and fault-tolerant capabilities.

The first contribution of this dissertation is the development of a lifetime improvement Pulse Width Modulation (PWM) method which can significantly extend the power cycling lifetime of Insulated Gate Bipolar Transistors (IGBTs) in NPC inverters operating at low frequencies. This PWM method is achieved by injecting a zero-sequence signal with a frequency higher than that of the IGBT junction-to-case thermal time constants. This, in turn, lowers IGBT junction temperatures at low output frequencies. Thermal models, simulation and experimental verifications are carried out to confirm the effectiveness of this PWM method.

As a second contribution of this dissertation, a novel on-line diagnostic method is developed for electronic switch faults in power converters. Targeted at three-level NPC converters, this diagnostic method can diagnose any IGBT faults by utilizing the information on the dc-bus neutral-point current and switching states. This diagnostic method only requires one additional current sensor for sensing the neutral-point current. Simulation and experimental results verified the efficacy of this diagnostic method.

The third contribution consists of the development and implementation of a fault-tolerant topology for T-Type NPC power converters. In this fault-tolerant topology, one additional phase leg is added to the original T-Type NPC converter. In addition to providing a fault-tolerant solution to certain switch faults in the converter, this fault-tolerant topology can share the overload current with the original phase legs, thus increasing the overload capabilities of the power converters. A lab-scale 30-kVA ASD based on this proposed topology is implemented and the experimental results verified its benefits.

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ACRONYMS AND TERMINOLOGY

ADC	Analog-to-digital conversion
ASD	Adjustable speed drive
ANPC	Active neutral point clamped
Al	Aluminum
CPSR	Constant power speed ratio
CTE	Coefficient of thermal expansion
CPLD	Complex programmable logic device
Cu	Copper
di/dt	Instantaneous change in current per unit time
DPWM	Discontinuous pulse width modulation
DSP	Digital signal processor
dv/dt	Instantaneous change in voltage per unit time
EV	Electric vehicle
FPGA	Field programmable gate array
GaN	Gallium nitride
HEV	Hybrid electric vehicle
HMI	Human machine interface
HRG	High resistance grounded
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate commutated thyristor
I-V	Current-voltage
kVA	Kilovolt Ampere

MOSFET	Metal-oxide semiconductor field-effect transistor
MTTF	Mean time to failure
NDPWM	Novel discontinuous pulse width modulation
NPC	Neutral point clamped
NTC	Negative temperature coefficient
PD-PWM	Phase disposition pulse width modulation
PI	Proportional-integral
PMSM	Permanent magnet synchronous machine
PWM	Pulse width modulation
QEP	Quadrature encoder position feedback
RMS	Root-mean-square
RUL	Remaining useful lifetime
SCWT	Short-circuit withstand time
Si	Silicon
SiC	Silicon carbide
SMPS	Switched mode power supply
SPWM	Sinusoidal pulse width modulation
SV-PWM	Space vector pulse width modulation
THD	Total harmonic distortion
TRIAC	Triode for alternating current
UPS	Uninterruptable power supply
V/Hz	Volt per hertz
WTHD	Weighted total harmonic distortion
ZVS	Zero voltage switching

CHAPTER 1

INTRODUCTION

1.1 Background

Electric adjustable speed drives (ASDs) have been increasingly utilized in various industrial applications due to the benefits stemming from their use in energy savings and control flexibilities. Emerging applications, such as electric/hybrid vehicles (EVs/HEVs), renewable energy direct-drive wind turbine generators, high-efficiency heating and air-conditioning equipment, as well as other industrial applications, have made ample use of ASDs for their powertrain systems. However, the wide penetration of such drive systems into numerous industrial applications is partially hindered by the lack of health condition monitoring techniques and fault-tolerant operation solutions. Especially, when ASDs are used in safety-critical applications, for instance, EVs/HEVs, electric aircraft systems, medical devices and instruments, and renewable energy generation systems, integrating health condition monitoring and fault-tolerant techniques would be of paramount importance to help avoid catastrophic failures or even disastrous consequences.

A standard industrial ASD system is composed of several major functional units, which include input/output filters, power converters, dc bus, control unit, and human-machine interface (HMI), as shown in Fig. 1.1. Among these functional units, the power converter unit is at the heart of such a system. However, this unit constitutes a vulnerable part in such an ASD system. One of the main reasons

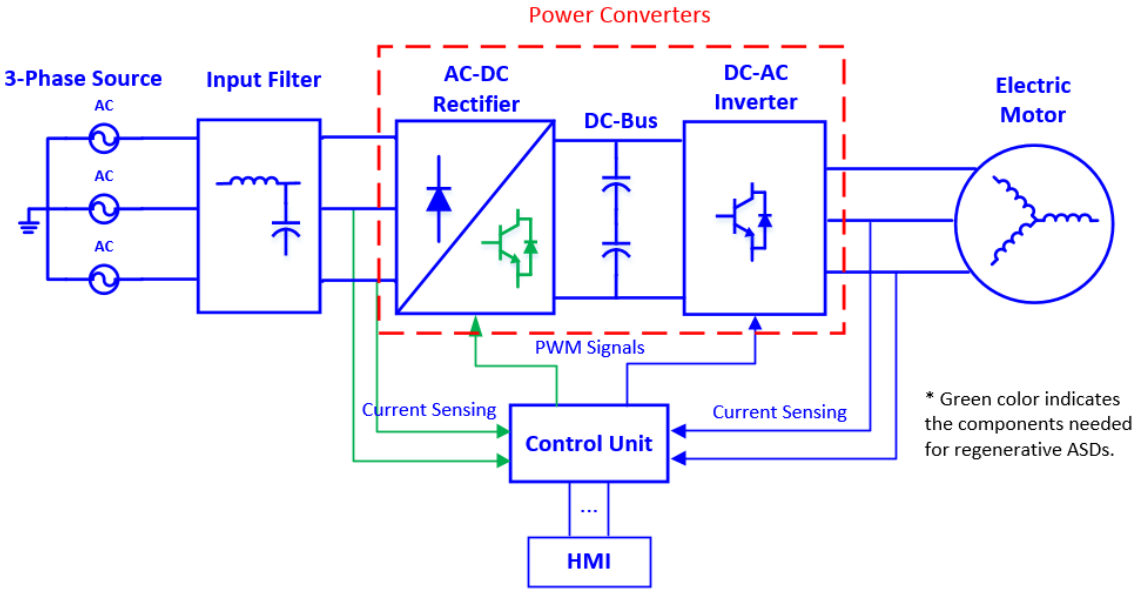


Figure 1.1: Basic functional structure of a standard industrial ASD system.

accounting for such power converter vulnerability is that it contains many power electronic devices, which may experience open-circuit or short-circuit device faults during switching operations. An industry-based survey on the reliability of power electronic converters shows that semiconductor power devices are regarded as the most fragile components by power electronic industrial respondents, as shown in Fig. 1.2 [1]. This is particularly the case, when some types of power converters containing a great many switching devices are utilized to meet the increasing power capacity requirements arising from market, such as multilevel power converters. Multilevel converters are well-known to be very suitable for medium-voltage high-power applications, in addition to other performance benefits such as their low harmonic distortion in outputs, low change rate of the voltages (dv/dt), and low switching frequencies [2]. Such power converters generally employ a large number of switching devices, which are either connected in series to withstand high voltage, or connected in parallel to meet high current

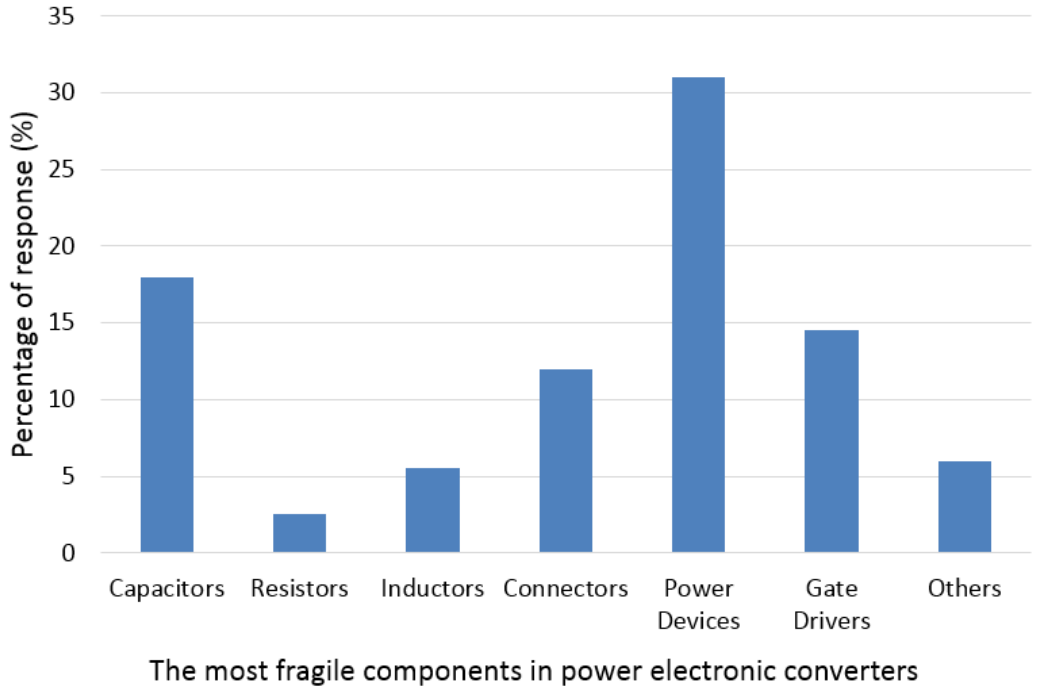


Figure 1.2: An industry-based survey on reliability of power electronics converters: the most fragile components in power converters.

demand. However, one major drawback with multilevel power converters is the degraded system reliability caused by the utilization of a large number of switching devices and their associated gate drivers in the converter topologies. The complexity of the hardware circuit increases the device failure probability. As a matter of fact, the system reliability of a multilevel converter is generally determined by the most vulnerable device in its circuit topology. In other words, if one critical switching device in a multilevel converter has a fault, the function of the whole converter may collapse.

Faults in switching devices of power converters can be classified into two categories. One category refers to acute failures, which are typically caused by sudden overvoltage, overcurrent, or overheating in the power circuit, and such faults are very difficult to predict. Another category represents drift failures, which

are caused by an accumulating effect of decreasing life cycles. Drift failures materialize through a slow process of deterioration in the devices. This category of drift failures is predictable. In this dissertation, it is assumed that a device failure in the multilevel power converter starts with a power cycling lifetime degradation, in which the device would deteriorate into an open-circuit or short-circuit fault if there is no remedial action available. Such a single device fault generally facilitates the drift failures of other adjacent devices in the circuits, and eventually may bring, in a cascading manner, the crumbling of the whole power converter. However, if a hierarchical and progressive fault-diagnostic and fault-tolerant strategy can be developed for multilevel inverters, the reliability of these associated multilevel-inverter-based ASDs would be significantly improved. For instance, one promising three-stage health monitoring and fault-tolerant solution having been conceived may relieve such concerns and will be described next. At the first stage, the power cycling lifetime of switching devices in multilevel inverters will be predicted. Furthermore, the power cycling lifetime of the most vulnerable device in the inverters will be improved through control strategies. Through this approach, drift-type device failures in the power inverters can be predicted and avoided. At the second stage, on-line diagnosis of switch faults in such inverters can be conducted, with the knowledge that some of the faults cannot be accurately predicted and can still occur in power converters, such as the aforementioned acute device failures. At the final stage, once a device fault is diagnosed in the converter, a corresponding fault-tolerant operation strategy will be triggered during a post-fault stage, which aims to output satisfactory voltages and currents for the related load. This comprehensive portfolio of health monitoring and fault-tolerant

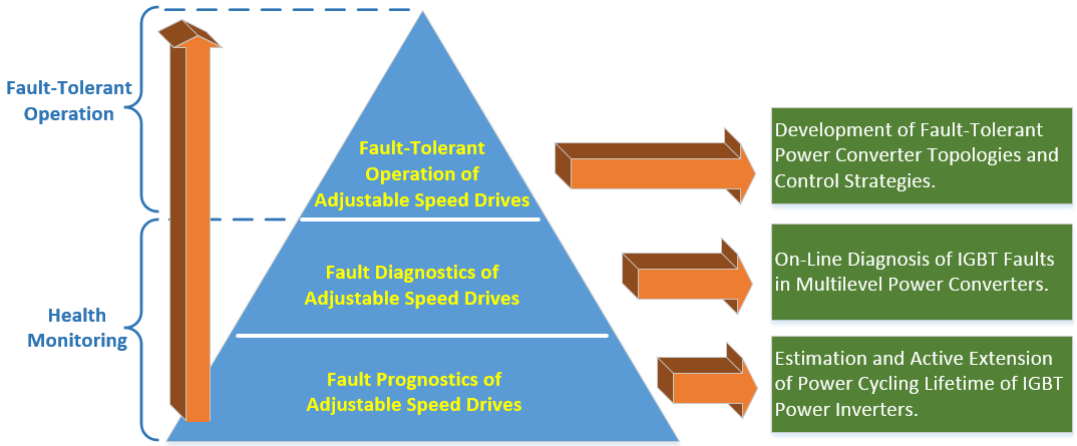


Figure 1.3: Hierarchical functional diagram of the proposed fault-tolerant adjustable speed drives.

solutions is shown in Fig. 1.3. It can be seen in this figure that these hierarchical and progressive solutions actually cover fault prognosis, diagnosis, and fault-tolerant operation of the power converters used in an ASD system. Therefore, the reliability of the associated ASDs should be dramatically enhanced, if all these hierarchical health monitoring and fault-tolerant solutions can be developed and implemented. These motivations will constitute the research objectives of this dissertation, which will be elaborated in the next section.

1.2 Research Objectives

In this dissertation, health condition monitoring techniques and fault-tolerant operation solutions for multilevel inverters will be thoroughly investigated. Among various types of multilevel inverter topologies, three-level neutral-point-clamped (NPC) inverters possess a few advantages over other types of topologies and have been widely used in medium-voltage high-power industrial ASDs [3]. Therefore, they are chosen as the subject inverter topologies under investigation in this work. Regarding the switching devices used in NPC inverters,

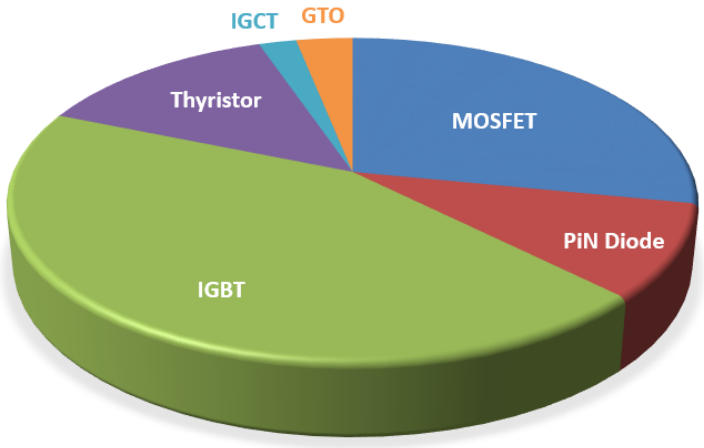


Figure 1.4: An industry-based survey on the percentage of semiconductor power devices used in power electronic industries.

they can be either Insulated Gate Bipolar Transistors (IGBTs) or Integrated Gate Commutated Thyristors (IGCTs) [4]. According to an industry-based survey on the utilization percentage distribution of semiconductor power devices, IGBTs are the most common devices used in power electronic industries [1], as depicted in Fig. 1.4. Therefore, IGBT switches are selected as the subject devices here for the investigations in this dissertation.

The first objective of this dissertation is to extend the power cycling lifetime of three-level NPC inverters in ASDs through innovative PWM methods. Given the fact that power inverters in ASDs may suffer severe lifetime degradation at low-frequency operations [5-7], especially in multilevel NPC inverters where the thermal distribution among the devices is significantly uneven at low frequencies [8-10], a novel pulse width modulation (PWM) method will be developed to improve the power cycling lifetime of the most thermally stressed power devices of the NPC inverters in the associated ASDs.

The second objective is to develop an on-line fault diagnostic method for

common device faults in ASDs. Common device faults include open-circuit and short-circuit faults. Detection of short-circuit switch faults have received much attention in the past decades and several solutions have become technically mature and have been integrated into most commercial IGBT gate drivers [11-14]. Therefore, only the diagnosis of open-circuit switch faults will be investigated under this research objective. A novel on-line diagnostic method with low computational effort and low increase of system cost will be developed, which is supposed to accurately and promptly detect any open-switch faults in an NPC inverter.

The third objective is to develop a novel fault-tolerant topology as well as the corresponding fault-tolerant control strategy for three-level NPC inverters. In other words, with this innovative fault-tolerant inverter topology used in ASDs, a "limp-home" post-fault operation can be achieved through adjustment of the microcontroller output, and consequently its impact on the switching sequence in the drives. Unlike the conventional fault-tolerant power converter topologies which use a redundant phase leg or more back-up devices [15-18], the innovative fault-tolerant topology to be developed in this dissertation is expected to possess five critical functional features which are listed as follows:

- The fault-tolerant inverter topology should be able to mitigate most of the potential device faults, including both open-circuit and short-circuit device faults.
- The fault-tolerant inverter topology should have very low number of redundant power devices. Otherwise, too many additional devices will boost the cost of the inverter, which may prevent its

commercialization or market acceptance.

- The fault-tolerant inverter topology should possess a modular circuit structure, which is for the convenience of manufacturing and commercialization of this new fault-tolerant topology.
- The fault-tolerant inverter topology is expected to improve the performance of the original NPC inverter under healthy conditions. It is well known that a fault-tolerant power converter topology generally requires the addition of redundant/back-up phase legs or switching devices to the original NPC inverter topology. Mostly, these redundant devices idle in the circuit under healthy conditions and degrade the inverter efficiency as well as bring about a cost increase. However, for the novel fault-tolerant inverter topology to be developed in this dissertation, it is expected that these redundant phase legs or devices can contribute to the performance improvement of the original NPC converters under healthy conditions. For instance, it is expected that such a redundant phase leg would lead to increasing the overload capability, reducing the fluctuation of the dc-bus neutral-point potential or common-mode voltage, or even improving the inverter efficiency.
- The fault-tolerant inverter topology should be able to output rated voltages and currents during post-fault operation. In other words, no derating in voltages and currents is required during a post-fault stage. This functional feature is very critical for certain applications, for instance, uninterruptible power supplies (UPS), EVs/HEVs, and

renewable energy generations, where rated voltages and currents have to be guaranteed all the time to provide the required performance.

1.3 Dissertation Organization

The remainder content of this dissertation is organized as follows:

In Chapter 2, existing health condition monitoring techniques and fault-tolerant operation solutions to power converters in ASDs documented in the literature are thoroughly reviewed. This literature review includes methods for extending the power cycling lifetime of IGBT power converters, diagnosis of open-circuit and short-circuit IGBT switch faults, as well as several existing fault-tolerant topologies for NPC power converters.

In Chapter 3, an improved discontinuous pulse width modulation (DPWM) method is developed to improve the power cycling lifetime of NPC inverters, especially for such inverters operating at low-frequency conditions. In addition to extending the lifetime of power inverters, this newly conceived DPWM method is also optimized to reduce the fluctuation of dc-bus neutral-point voltages in NPC inverters. Both simulation and experimental results are presented to confirm the efficacy of this improved DPWM method.

In Chapter 4, negative impacts of switch faults in multilevel power converters are discussed. A novel on-line diagnostic method for diagnosing open-circuit switch faults in NPC converters is presented. The principle and characteristics of this novel diagnostic method are explained in detail. The effectiveness of such a diagnostic method is validated by both simulation and

experimental results.

In Chapter 5, an innovative fault-tolerant circuit topology for three-level T-Type NPC power converters is introduced. This new fault-tolerant topology not only can provide a satisfactory fault mitigation solution to most device faults that could occur in T-Type converters, but also can increase such converters' overload capabilities. Moreover, a zero-voltage switching (ZVS) control strategy is introduced to improve the efficiency of this fault-tolerant four-leg T-Type NPC inverter. Simulation and experimental results are presented to confirm the advantages of this proposed fault-tolerant converter topology.

In Chapter 6, a few conclusions and contributions of this dissertation are summarized. Future research opportunities related to the work presented in this dissertation are recommended.

CHAPTER 2

REVIEW OF LITERATURE

2.1 Lifetime Improvement of Power Converters

2.1.1 Introduction

IGBT modules, which typically integrate IGBT chips and free-wheeling diode chips, are used in most power electronic ASD systems. However, such IGBT modules are one of the most unreliable devices after capacitors causing failures in power converters, according to an industry-based survey presented in [1]. A cross section schematic of the internal structure of a wire bonding IGBT module with a baseplate is shown in Fig. 2.1 [19]. As can be seen in this schematic figure, the IGBT module is composed of bond wires, IGBT and diode chips, soldering, substrate, and baseplate, each of which is usually made of different materials, as listed in Table 2.1. During the switching operations of IGBT modules, the IGBT/diode chips will experience cyclic temperature profiles due to the conduction and switching losses in the chips. Accordingly, these various materials in IGBT modules expand with a rising temperature and contract with a decreasing temperature. Such a property can be described by coefficients of thermal expansion (CTE), which is a material-dependent parameter. The comparison between the CTEs of various materials in an IGBT module is depicted in Fig. 2.2, which demonstrates a variety of magnitude mismatching among the CTEs of the different materials in such IGBT modules. For instance, the CTE of aluminum bond wires is almost one order of magnitude higher than that of IGBT/diode chips. During

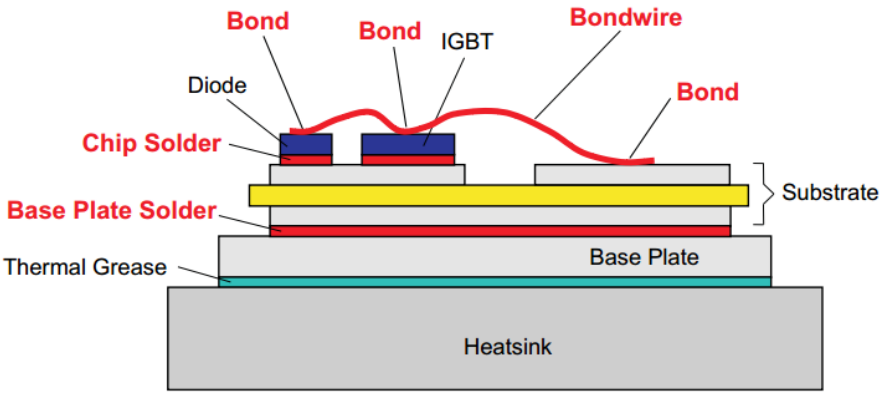


Figure 2.1: Cross section schematic of the internal structure of a wire bonding IGBT module (interfaces that are releveant to module lifetime are marked in red).

Table 2.1: CTEs of the materials in different parts of IGBT modules [20, 21]

Name of the Part	Material	CTE (ppm/K)
Bond wires	Aluminum (Al)	23
	Copper (Cu)	16
Soldering layer	Stannum Lead ($Sn_{63}Pb_{37}$)	25
	Stannum Silver (96.5%Sn/3.5%Ag)	30
IGBT/Diode chips	Silicon (Si)	2.5
	Silicon Carbide (SiC)	4
Ceramic substrate	Aluminum Oxide (Al_2O_3)	6
	Aluminum Nitride (AlN)	4.5
Baseplate	Aluminum Silicon Carbide ($Al_{37}SiC_{63}$)	7.9
	Copper Carbon ($Cu_{60}C_{40}$)	8.5

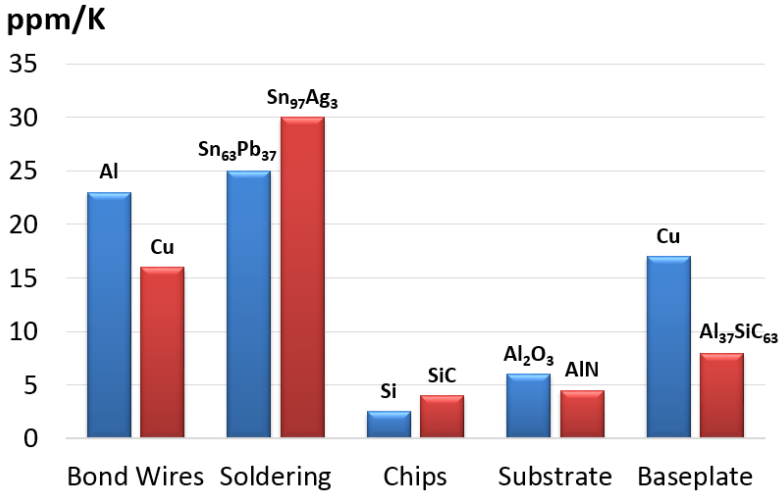


Figure 2.2: Comparison of CTE values of different materials in IGBT modules.

switching operations of IGBT modules, the junction temperatures of each chip may increase or decrease quickly, which results in a differential elongation of the bond wires with respect to the substrate. This will cause a plastic flow of the wire material, especially at the periphery of the bonding interface where the shear stress reaches its maximum limit [22]. Eventually, a bond wire lift-off will occur if such thermal-mechanical stress is larger than the maximum bond strength. Fig. 2.3 shows the bond wire lift-off in an IGBT module [23]. Once one of the bond wires lifts off, the current sharing in the remaining of the parallel bond wires will become larger than the normal current rating, which will facilitate more bond wires to experience lift-off until an IGBT open-circuit fault happens. According to [22], bond wire lift-off has been regarded as one of the leading reliability concerns in IGBT modules. To predict such failures, active power cycling tests are generally conducted to estimate the remaining lifetime of IGBT modules [24].

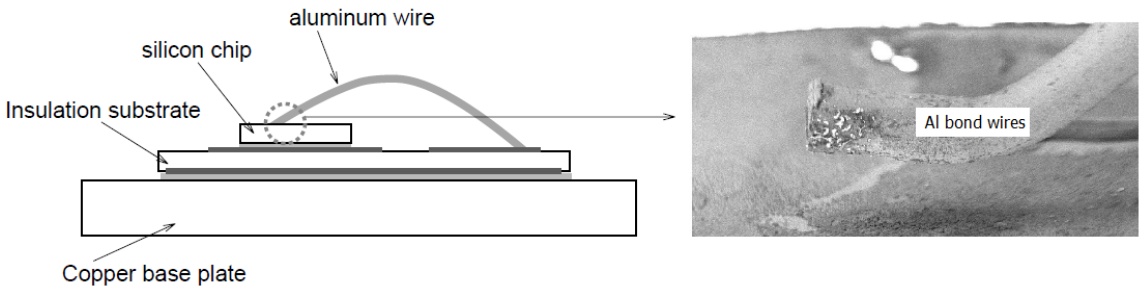


Figure 2.3: Aluminum bond wire lift-off in an IGBT module.

On the other hand, it can be seen in Fig. 2.2 that there is also dramatic mismatch in the CTE values between the substrate and the baseplate, which produces thermal stress and subsequent mechanical strain on the soldering layer. Consequently, soldering fatigue appears and accumulates between the ceramic

substrate and the baseplate in the form of creep [25], voids [26], cracks or delamination [27]. These increase the heat flux density in the remaining soldering layer and retard the heat dissipation. If left untreated, such soldering fatigue can rapidly accelerate and eventually result in a soldering cracking failure in the IGBT module, as shown in Fig. 2.4 [29]. During this process, the thermal impedance through the heat transfer path in the IGBT module will increase. The increased thermal impedance will cause higher temperature rise in the IGBT/diode chips, which will further accelerate the cracking of the soldering. Such soldering fatigue is mainly caused by slow thermal cycles [28]. The lifetime of the solder between the substrate and baseplate can be predicted by conducting passive thermal cycling tests, which have been reported in [28] and this aspect is beyond the scope of this dissertation.

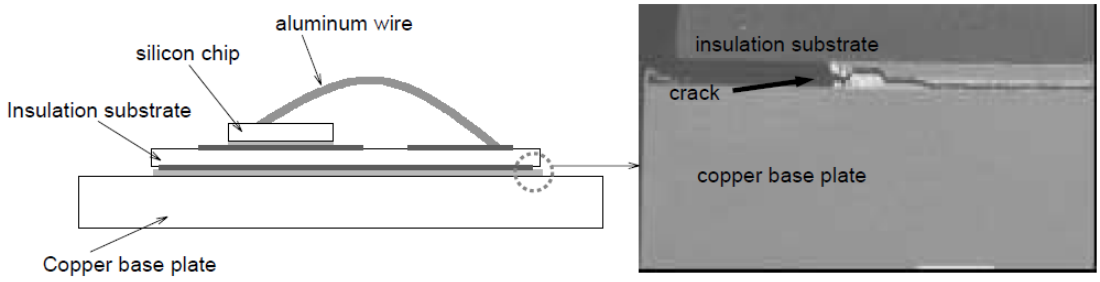


Figure 2.4: Substrate soldering cracking failure in an IGBT module.

To extend the lifetime of IGBT modules, generally there are two categories of methods to be adopted. One is to select the materials with better thermal and mechanical matching/compatibility during the packaging and manufacturing process of the IGBTs. For instance, replacing the copper baseplate of IGBTs with AlSiC alloy material to reduce the differences between the CTEs. In particular, the difference in CTEs between a ceramic substrate and a baseplate. As given in Table

2.1, a copper (Cu) baseplate has a CTE value of 16 ppm/K, which exhibits large mismatch with the CTE of a ceramic substrate that typically ranges around 4.5-6 ppm/K. If an IGBT baseplate can be packaged based on $Al_{37}SiC_{63}$ material, the CTE value of such a baseplate will be reduced to 7.9 ppm/K, closer to the CTE value of the ceramic substrate. As a result, the lifetime of the soldering layer between the IGBT baseplate and substrate could be significantly extended. Similar lifetime extension effects can be achieved upon replacing the silicon (Si) chips with silicon carbide (SiC) material [30], replacing aluminum (Al) bond wire with copper (Cu) material [31], or replacing the "Al+AlN" substrate material with "Cu+Si_3N_4" [32], and so forth. However, the adoption of these proposed material substitutes such as SiC, Cu and "Cu+ Si_3N_4" in the IGBT packaging generally involves a few factors to be concurrently considered, such as thermal conductivity, convenience of processing, and material cost, which is quite challenging to make a compromise in practice.

Another category of methods for improving IGBT lifetime is to modify the PWM and control strategies that are used to regulate the switching of IGBT modules. Basically, the purpose of such methods is to reduce the switching and conduction losses generated in the IGBT/diode chips, and/or attenuate the swing magnitude of the chip junction temperatures. As a result, the lifetime of the IGBTs and the related PWM inverters can be improved. These methods do not require the changes of IGBT internal structure or materials, thus are more practical and more convenient to be adopted by industries. One of the objectives of this dissertation is to develop a novel PWM strategy to reduce the IGBT junction temperatures and temperature swings. Therefore, existing methods in the literature that aim at

reducing the IGBT/diode thermal losses or mitigating junction temperature swings through PWM control strategies will be reviewed first, which will be given in the following section.

2.1.2 Existing Solutions to Improve IGBT Lifetime

Lifetime of IGBT power converters has been investigated and extended by a few PWM or control methods presented in the literature [33-39]. Among these existing methods, either the switching frequencies, or load currents of the power inverters are regulated to reduce the dissipated device losses and subsequently obtain longer lifetime of such IGBT power converters. Each of these methods will be reviewed in detail in the following.

In [33], a PWM frequency hysteresis control approach was proposed, in which the PWM switching frequency was reduced to its lowest level when the swing magnitudes of the IGBT junction temperatures are higher than their preset upper limit. In other words, under normal operation, if the swing magnitudes of the IGBT junction temperatures are lower than the preset upper limit, all the control and PWM strategies will remain in the normal mode, which is unchanged. As a result, the overall lifetime of the IGBT inverter was significantly improved. The functional block diagram of this method is given in Fig. 2.5 [33], and the improvement of the inverter lifetime, namely, mean-time-to-failure (MTTF), based on this method is shown in Fig. 2.6 [33]. As can be seen in Fig. 2.6, the MTTF of the IGBT inverter is effectively improved after halving the switching frequency. However, one drawback of this method is the dramatic increase of the harmonic distortion in the output when the PWM switching frequency is reduced.

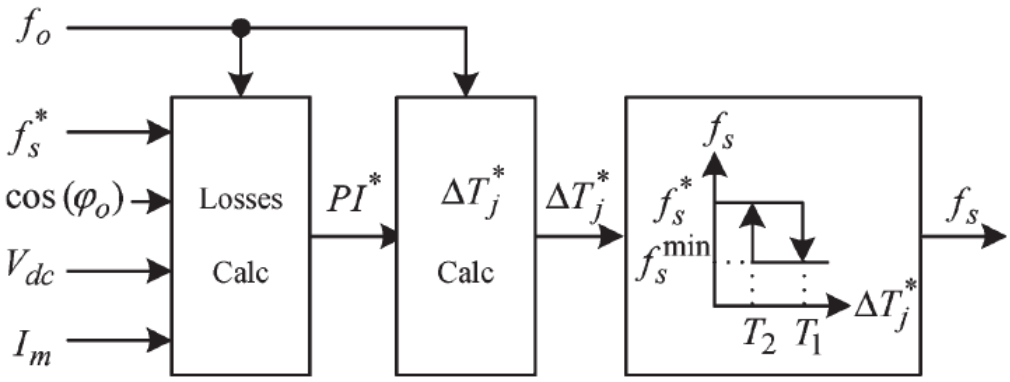


Figure 2.5: PWM Switching frequency hystersis control.

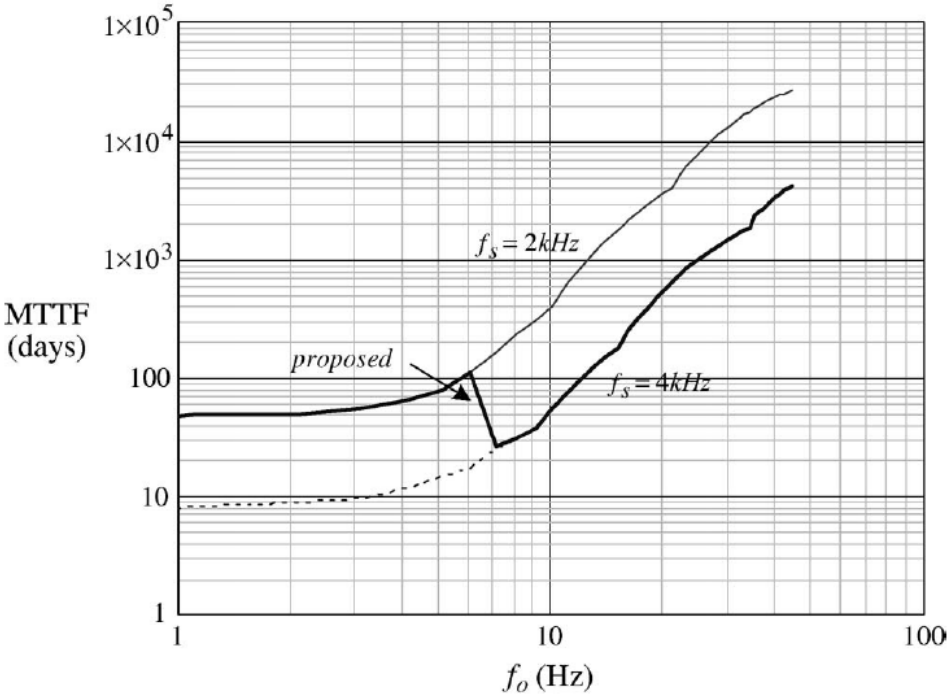


Figure 2.6: MTTF of the IGBT inverter under various output frequencies.

Such deterioration in harmonic distortions may not be acceptable in certain applications requiring high-precision motion control and low acoustic noise, unless the output filter of the inverter is overdesigned.

Similarly, another method based on the manipulation of switching frequencies and load currents to adjust the IGBT losses was introduced in [34].

Two proportional-integral (PI) regulators were utilized to reduce the switching frequencies and load currents, respectively, when the IGBT junction temperature was approaching its upper limit of 110℃ [34]. The inputs for these PI regulators are the actual switching frequencies or load currents, and the output is the estimated IGBT junction temperatures, which serve as the feedback variables for the PI regulators. The block diagram of this control method is shown in Fig. 2.7 [34].

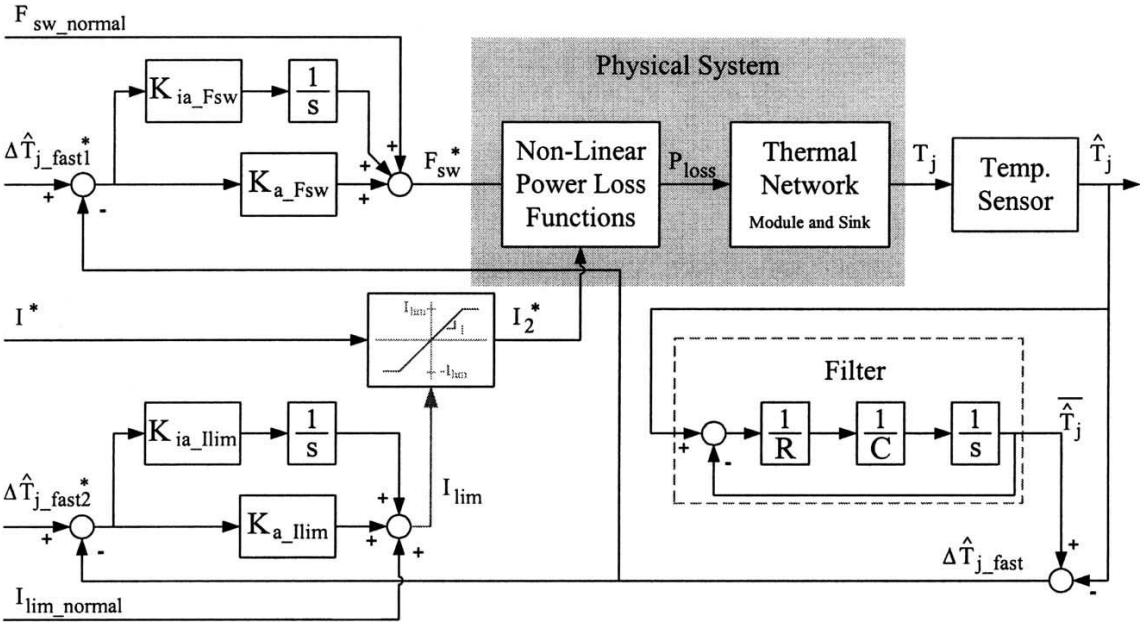


Figure 2.7: Block diagram of the PI regulators for improving IGBT power cycling lifetime.

In addition, novel PWM methods were investigated in the literature to reduce the conduction or switching losses in the IGBT modules. Once the device losses are reduced, this results in lower IGBT junction temperatures, and subsequently the IGBT lifetime would be extended. In [35], a DPWM method and a space vector PWM (SVPWM) method were selectively utilized during the

converter modulation, namely, the so-called “hybrid modulation method”. Such a modulation method was developed for improving the lifetime of the generator-side converter in a wind turbine generation system [35]. Specifically, when the wind speed is below certain threshold value, the conventional SVPWM method will be employed. Once the wind speed is higher than the threshold reference value, the DPWM method will be utilized to mitigate the thermal stress on the associated IGBTs. This DPWM method has been well-known for the reduction of IGBT switching losses, although the harmonic distortions generated under certain modulation indices are generally much higher than those yielded under the SVPWM method. More details on the DPWM method were reported in [36]. The IGBT lifetime improvement through using this hybrid modulation method in [35] is demonstrated in Fig. 2.8, and the harmonic distortions generated from the generator-side converter by using such a method is shown in Fig. 2.9. It can be seen from these figures, by selectively using the DPWM and SVPWM methods, a longer IGBT lifetime can be achieved, although the harmonic distortion in the converter outputs will be inevitably increased.

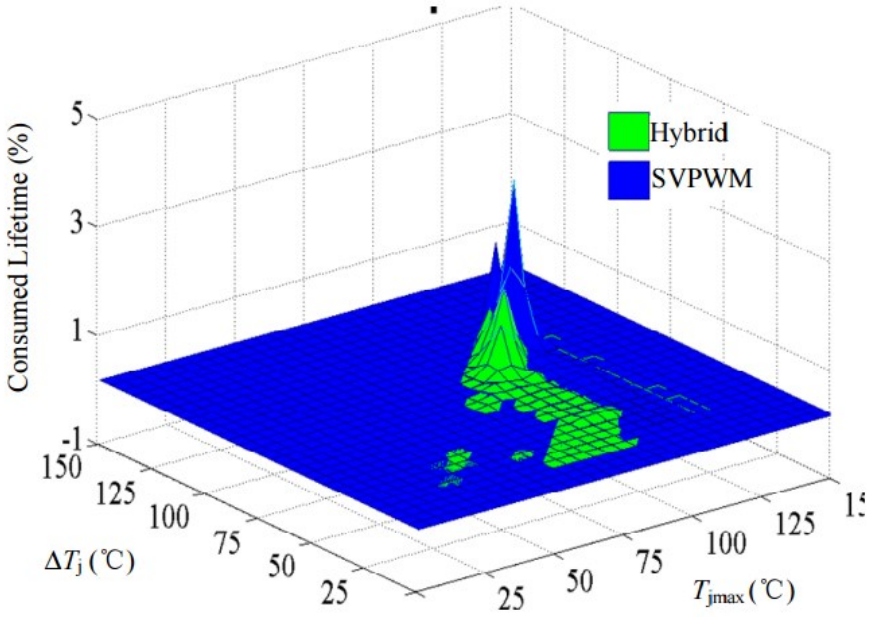


Figure 2.8: Reduction of the consumed IGBT lifetime by using a hybrid modulation method for the generator side converter in a wind turbine generation system.

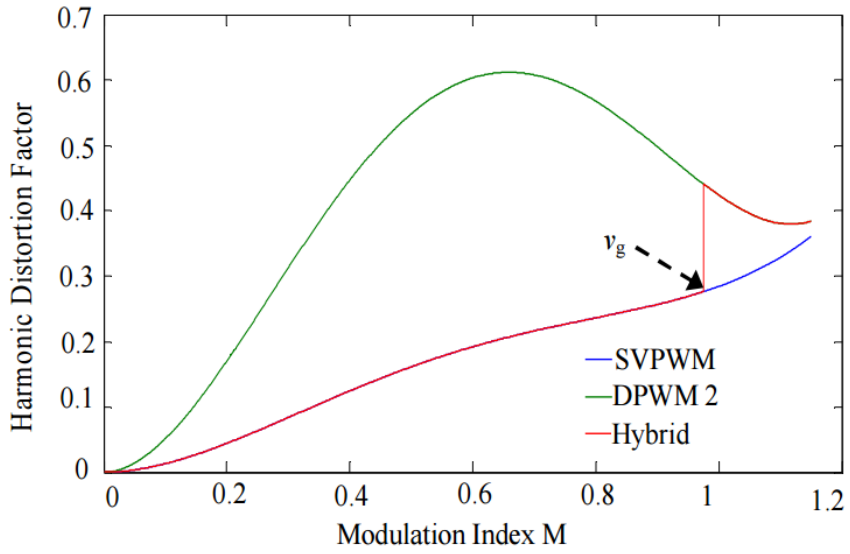


Figure 2.9: Harmonic distortion factor for SVPWM, DPWM, and the hybrid modulation method at a constant switching frequency.

Another DPWM method was proposed to improve the IGBT lifetime in a two-level voltage source inverter under low output frequency conditions [37]. In this new DPWM method, a zero-sequence signal with frequency much higher than

the time constants of IGBT junction-to-case thermal impedance was injected into the voltage reference signals. As a result, lower IGBT junction temperatures were achieved and correspondingly and the lifetime of the IGBT inverter was extended. According to the simulation and experimental results given in [37], a reduction of 15% of the IGBT junction temperatures were achieved for a 480V/65A ASD system, while the harmonic distortions in the output voltages and currents almost stay the same, compared to the results obtained under the conventional SVPWM modulation.

As for multilevel NPC inverters which are being investigated in this dissertation, existing solutions in the literature to improve their IGBT lifetime mainly focused on the utilization of redundant voltage space vectors to actively redistribute the losses from the overloaded devices to other cooler devices [38, 39]. In [38, 39], redistribution of the semiconductor losses in a three-level NPC inverter by taking advantage of the redundant zero voltage vectors and small voltage vectors were carried out for both low and high modulation indices, respectively. A trade-off between the loss redistribution and the neutral-point voltage control freedom was considered in these investigations for purposes of ensuring the proper operation of the control system for such NPC inverters.

In summary, the fundamental motivation of improving the lifetime of IGBT inverters through PWM or control strategies is to reduce the losses in the related IGBT devices. Such an objective can be achieved by two approaches, namely, directly reducing the PWM switching frequencies or load currents under thermal overload conditions, or improving the PWM strategies to alleviate the thermal stress on the related IGBTs.

2.2 On-line Diagnosis of Switch Faults in Power Converters

2.2.1 Introduction

As discussed in Section 2.1.1, the mismatch of the thermal expansion coefficients among different materials in IGBT modules, in conjunction with the large swings in IGBT junction temperatures, can lead to IGBT failures such as bond wire lift-off or soldering cracking, which generally exhibits itself as an IGBT open-circuit failure mode. Actually, there are a few other causes that may lead to IGBT open-circuit faults as well, namely, gate driver malfunctions, insufficient cooling for the IGBT modules, large gate resistors, very high switching frequencies, and overload/overcurrent operations. All these causes will be briefly explained here. First, malfunction in the gate driver may cause a constant turn-off gate signal in the output for IGBTs, which makes the IGBT behave as if encountering an open-circuit fault. Second, insufficient cooling, large gate resistors, too high switching frequencies, and overload/overcurrent operations, causing IGBT open-circuit faults, essentially occur because of the excessive thermal losses in such semiconductor devices under these operating conditions. This may eventually result in the lift-off of bond wires, or cracking of the soldering layers in the IGBTs. All these failure mechanisms are listed in the block diagram of Fig. 2.10. Once an open-circuit fault occurs in a power inverter, dc components will be present in the profiles of load currents and voltages. If the load is an electric motor, such dc components will bring about magnetic saturation and induce an oscillating/pulsating airgap torque at the fundamental frequency [40].

As a matter of fact, in addition to the open-circuit failure mode, there is

another common failure mode for IGBT devices, namely, short-circuit fault. During a short-circuit fault, the IGBT will be in a constant-on mode, like a conductor with very small resistance. More severely, dc-bus shoot-through may occur when the complimentary IGBT on the same phase bridge is turned on. The large dc-bus shoot-through current will damage the related power devices and dc-bus capacitors. Causes for IGBT short-circuit faults mainly include static/dynamic latch-up, gate driver malfunction, and high-voltage breakdown, as again shown in Fig. 2.10. Each of these failure mechanisms will be briefly analyzed in the following discussion:

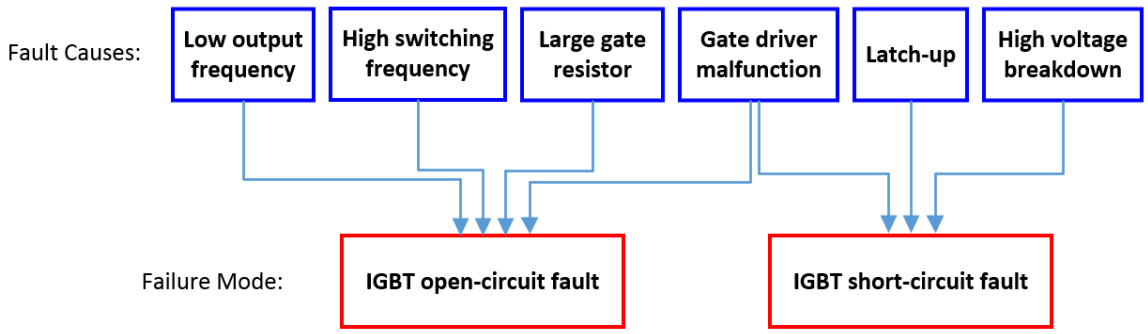


Figure 2.10: Main failure mechanisms in an IGBT module.

An IGBT device generally has a parasitic P-N-P-N sandwich structure between the collector and emitter terminals, as depicted in Fig. 2.11. The presence of this parasitic four-layer thyristor structure in the IGBT creates the possibility of the device latching up by regenerative actions. This mode of operation is highly undesirable because it leads to loss of control of the collector current by the applied gate voltage. Once the device has latched up, it can only be turned off by either externally interrupting the collector voltage or reversing its polarity [41]. Latch-up usually produces catastrophic failures in the devices as a results of excessive heat

dissipation in the dc circuits. The latch-up modes of IGBT can be generally classified as static and dynamic modes. In a static mode, the collector voltage is low and the latch-up occurs when the steady-state current densities exceed a critical value. The dynamic mode of latch-up mainly occurs during turn-off switching operations. This mode involves both high collector current and voltage. The current densities at which latch-up occurs in the dynamic mode is lower than that for the static mode. It should be mentioned that the later-generation IGBTs with trench-gate structure and heavily doped P-base region under N-emitter, have been proved to have good latch-up immunity, which may render the occurrence of latch-up rare failure event for IGBT devices [42, 43].

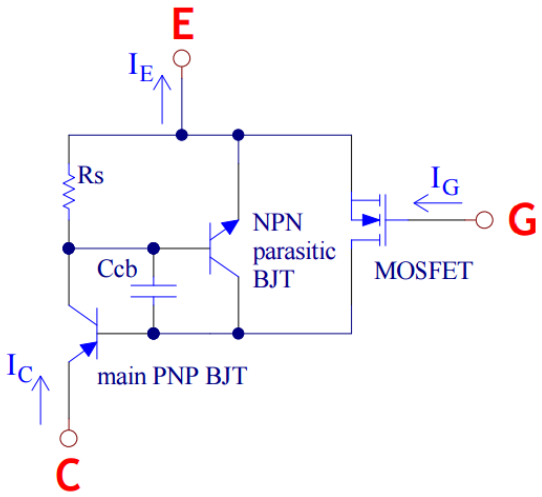


Figure 2.11: Equivalent circuit schematic of an IGBT device.

Gate driver malfunction can also cause short-circuit faults in IGBTs. Any damage of the IC components in power stages of gate drivers may disable their output of turn-off gate signals, which will make the IGBT stay in a constant-on mode, until the resulting large short-circuit current damages the device if no protection solutions are available.

High voltage breakdown: high voltage spikes induced by high change rate of collector current (di/dt) and stray inductance can damage IGBTs during their turn-off, especially under repetitive voltage spikes [44]. Due to the high turn-off voltage spikes, electric field may reach the critical field which can break down one or more the IGBT cells. Such phenomenon can lead to high leakage current as well as high local temperature.

In summary, a short-circuit IGBT fault can be caused by several factors, including gate driver malfunction, high voltage break down, and static/dynamic latch-up. Large short-circuit current will be caused during such failure mode in an IGBT power converter, which may damage the dc bus, power devices, or bring about other catastrophic failures. The diagnosis of such short-circuit faults requires fast detection speed to ensure that the protection actions can be applied in time before an irremediable failure occurs. Specifically, the standard short-circuit withstanding time (SCWT) for modern silicon IGBTs is mostly less than $10\mu s$ [45]. A few well-established detection/protection solutions for IGBT short-circuit faults will be reviewed next in Section 2.2.2.

2.2.2 Existing Diagnostic Methods for IGBT Faults

In this section, diagnostic methods presented in the literature for IGBT short-circuit and open-circuit faults in multilevel NPC converters will be reviewed and critically examined.

Regarding the diagnosis of IGBT short-circuit faults, the most well-established method is the well-known desaturation detection technique, as reported in [46]. In this technique, a high-voltage fast recovering diode (D_1) is usually

connected to the IGBT's collector terminal to monitor the IGBT collector-emitter on-state voltage, as shown in Fig. 2.12. Once there is a short-circuit fault occurring in an IGBT, the IGBT on-state voltage will increase dramatically. If this on-state voltage is larger than a predetermined threshold value for a certain duration of time (i.e., t_{trip} shown in Fig. 2.12), a short-circuit fault will be identified. Such a desaturation detection technique has been commercialized and integrated into most of the off-the-shelf gate drivers in the market. It should be noted that, the requirement of this time delay (generally around 1μs to 5μs) is for avoiding any false diagnosis/protection. However, the fault current could surge to a very high value during the blanking time, thus resulting in damage of the IGBT due to excessive local heating. Thus, new generations of the commercial gate drivers employ a two-stage soft turn-off technique for solving the overcurrent issue during the time delay associated with the desaturation detection method [47, 48].

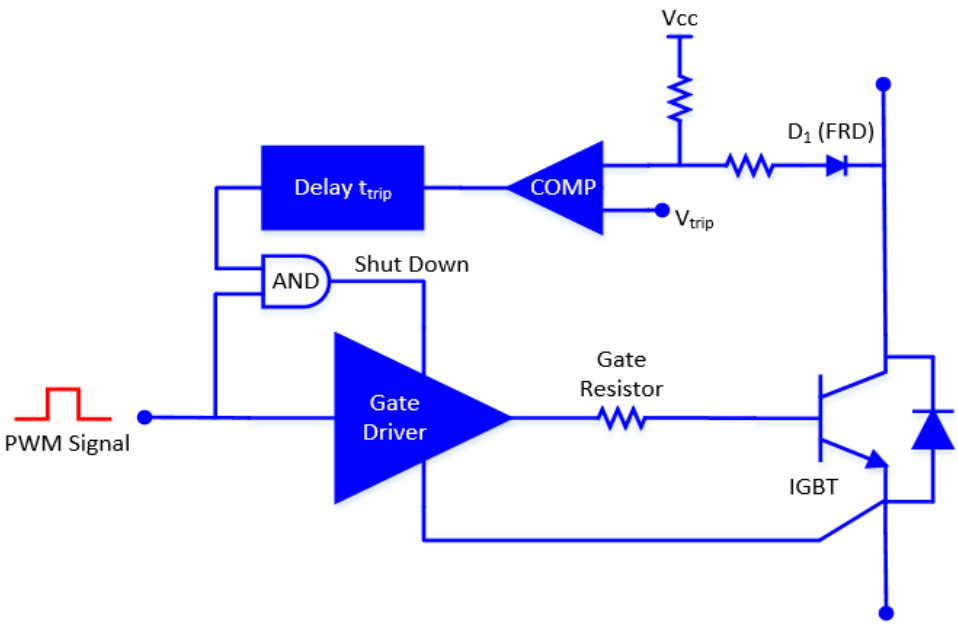


Figure 2.12: Schematic of IGBT desaturation detection circuit.

In addition, variations in the gate voltage and current rate (di/dt) have been analyzed to identify a fault condition in IGBT devices [49, 50]. Recently, a new promising short-circuit detection method was introduced in [51] for IGBT devices based on the evaluation of fault current level by measuring the induced voltage across the stray inductance between the Kelvin emitter and power emitter of the IGBT modules. Compared with the commonly used desaturation detection method, this new method provides a fast and reliable detection of short-circuit faults.

It can be seen from the above that mature diagnostic methods for IGBT short-circuit faults have been well established and some of them have been widely commercialized and applied in industry. Accordingly, the remaining content of this section will focus on the review and analysis of existing methods proposed in the literature for the diagnosis of IGBT open-circuit faults.

First of all, an open-switch fault diagnostic method was developed in [52] based on detecting the dimensions and orientation angle of the so-called "Concordia current patterns". Such current pattern is determined by plotting the instantaneous ac current components in the two-axis orthogonal reference frame, i_α versus i_β, which are defined as follows:

$$i_\alpha = \frac{2}{3} i_a - \frac{1}{3} i_b - \frac{1}{3} i_c \tag{2.1}$$

$$i_\beta = \frac{1}{\sqrt{3}} (i_b - i_c) \tag{2.2}$$

where, i_a, i_b, and i_c are the three-phase instantaneous currents in the stationary reference frame. i_α and i_β are the ac current components in the two-axis

orthogonal stationary reference frame.

Under any healthy condition, the Concordia current pattern should be a circle ideally, which is distorted into a semicircle or other geometrical patterns once there is an open-circuit switch fault in the inverter. In this method, it was assumed that the distortion of the current pattern for each IGBT open-circuit fault is unique, and therefore can be detected by pattern recognition techniques. This method could be effective under most of the normal conditions. However, the drawback with this method is that, such "Concordia current patterns" change with the value of the amplitude modulation indices of the PWM strategy, which may cause misdiagnosis of such open-circuit switch faults.

Similarly, one more diagnostic method, the so-called "the average current park's vector approach", was introduced in [53], for detecting open-circuit switch faults in a three-level NPC inverter. The fault detection in this method relies on the analysis of the Park's vectors [54] of the mean value of each inverter output ac current over one fundamental period. Specifically, there are two steps for the implementation of this method, which are detailed as follows:

First, the average value of each inverter output current (i_{av}, i_{bv}, i_{cv}) is calculated from current samplings by the following equation:

$$I_{j_{av}} = \frac{1}{N}\sum_{k=1}^{N} i_{j,k},\ \text{j=a, b, c} \tag{2.3}$$

where, N is the amount of samples, k is the current sample number and a, b and c are the indices of each phase, and $I_{j_{av}}$ is the resulting average current.

Second, the Park's vector transformation [54] is applied to these average values, in order to obtain the magnitude ($\bar{I}_{s_{av}}$) and phase angle ($\theta_{s_{av}}$) of a vector in the complex plane, which is calculated as follows:

$$\begin{cases} I_{d_{av}} = \sqrt{\frac{2}{3}} I_{a_{av}} - \frac{1}{\sqrt{6}} I_{b_{av}} - \frac{1}{\sqrt{6}} I_{c_{av}} \\ I_{q_{av}} = \frac{1}{\sqrt{2}} I_{b_{av}} - \frac{1}{\sqrt{2}} I_{c_{av}} \\ \bar{I}_{s_{av}} = I_{d_{av}} + jI_{q_{av}} = |\bar{I}_{s_{av}}| \angle \theta_{s_{av}} \end{cases} \tag{2.4}$$

Under normal operation, the magnitude of the average current Park's vector, namely, $|\bar{I}_{s_{av}}|$, is zero in theory (in practice, there would be some variations around zero due to the inherent PWM switching characteristics). However, if an open-circuit fault occurs in the NPC inverter, this magnitude will increase to a value higher than the predetermined threshold value. By using this approach, the faulty switch can be identified.

The effectiveness of this method is based on one assumption that the sum of the average values of the instantaneous three-phase currents is zero under any healthy condition, which holds true for the NPC converter fed by three-phase ac source with a floating neutral point. However, such an assumption may be incorrect for the power source with the neutral point solidly grounded or high-resistance-grounded (HRG), where the sum of the three-phase currents may not be zero, especially when there is a line-to-ground fault occurring in the system. In other words, this diagnostic method would not work properly for NPC converters fed by three-phase sources with a solidly grounded or HRG neutral point.

Recently, an open-switch fault detection method for a back-to-back NPC converter used in wind turbine systems was introduced in [55]. The circuit schematic of this converter is shown in Fig. 2.13. In this method, variations of the phase current directions and the time duration during which the phase current remains in the zero range are used as the indicators for open-circuit faults in the

back-to-back NPC converters. This method only requires the information on input and output phase currents, which are generally available in the associated microcontroller. Therefore, no external components or devices are demanded for the implementation of this method. However, as clarified in this reference [55], for any open-circuit switch faults in an NPC inverter, this diagnostic method can only distinguish the faults between the upper branch and lower branch in one phase leg, but incapable of identifying a specific faulty switch. Obviously, such ambiguous diagnostic effect will pose challenges in the post-fault maintenance or fault-tolerant operations. Another potential drawback is that, the required ac current information on the input of the NPC rectifier typically contains rich harmonics/ripples due to the high-frequency switching of the rectifier. Such harmonics/ripples may mask the fault signatures for diagnosing any open-switch faults in the NPC rectifier.

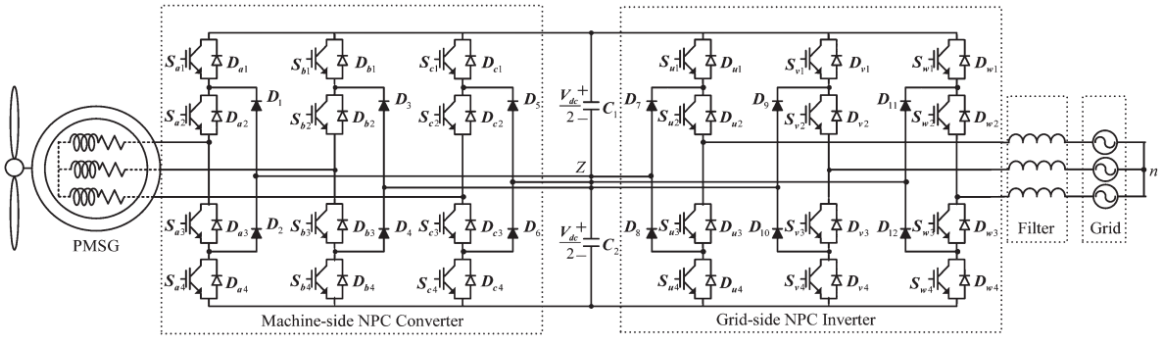


Figure 2.13: A back-to-back NPC converter for the wind turbine system.

All these three diagnostic methods discussed above are based on monitoring the fault signatures from the phase currents of the NPC inverter. There are several other diagnostic methods [56-58] proposed in the literature using the pole voltage information for detecting open-circuit switch faults in NPC inverters, which will

be reviewed next.

In [56], an on-line diagnostic method for IGBT open-circuit faults in a three-phase three-level active NPC (ANPC) inverter was developed. In this method, three types of real-time information are needed, namely, instantaneous three-phase pole voltages, the predetermined inverter PWM switching strategies, and the polarities of the three-phase currents. All these three types of information are utilized together to form a look-up table. During each specific switching state, the pole voltage of each phase is measured and compared to the supposed value under a healthy condition. The outcome of the comparison will be the indicator for identifying the faulty switch. It should be pointed out that the information on the switching states and three-phase currents is typically available in an industrial ASD system. Hence, only three voltage sensors are demanded for the implementation of this method. In addition, it is well known that the dc-bus neutral point is always accessible for measuring the pole voltages in multilevel NPC inverters due to the necessity of controlling the dc-bus neutral point voltage. Such a characteristic is different from that in two-level power converters, where the dc-bus neutral point may not be accessible in practical ASD systems. Another benefit of this diagnostic method is the fast detection speed. According to the analysis in [56], an open-circuit fault can be diagnosed within one fundamental period of the load currents.

Another diagnostic method based on the analysis of inverter pole voltages was proposed in [57]. This method is based on the well-known fact that the magnitude of the pole voltages of the NPC inverter is distorted or disappears whenever there is an open-circuit switch fault, in comparison to these under normal conditions. Therefore, in this diagnostic method, a direct comparison between the

measured pole voltages to the fault reference signals was conducted, the functional block diagram of which is shown in Fig. 2.14 [57].

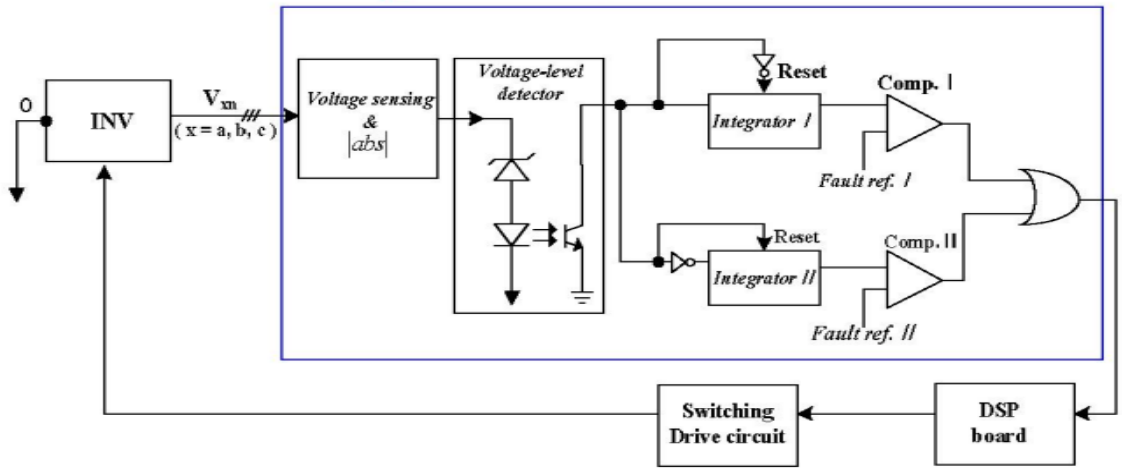


Figure 2.14: Equivalent circuit of a fault detection system.

Different from these methods discussed above utilizing the information of phase currents or pole voltages for the diagnosis, a new method based on monitoring the clamp branch currents was introduced in [58] for detecting IGBT faults in a three-phase three-level ANPC inverter. The main principle of this method lies in the fact that the clamp branch current under healthy condition of the converter is completely different from that under faulty conditions for a given switching state. The implementation of this diagnostic method requires two Rogowski coils [59] to be installed on the upper and lower locations of each clamp branch, respectively, see "Ⓐ" in Fig. 2.15, which implies that there will be six Rogowski coils needed for the implementation of this method in a three-phase ANPC converter, as shown in Fig. 2.13. According to the analysis in [58], this diagnostic method can effectively detect both IGBT open and short-circuit faults in ANPC inverters. However, such a benefit is achieved at the price of the

increased system cost, hardware complexity and physical volume, which significantly increase due to the requirement of the six Rogowski coils and six channels of related current sensing circuits.

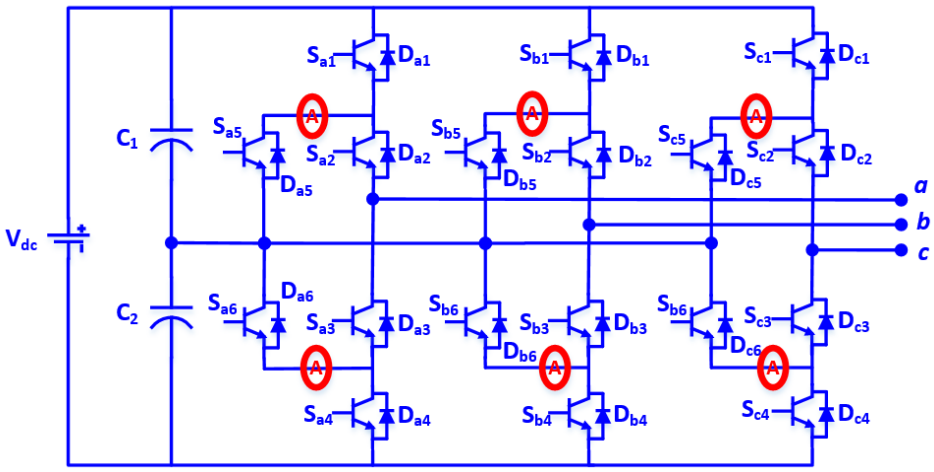


Figure 2.15: Using Rogowski coils (marked in red) for the diagnosis of IGBT faults in a three-level ANPC inverter.

A comprehensive comparison between all these existing diagnostic methods for detecting IGBT faults in multilevel NPC inverters is shown in Table 2.2. In this table, four critical criteria, namely, diagnostic capabilities, cost increase, computational burden imposed on the microcontroller, and fault detection speed (assessed by the period, T_0, of the fundamental frequency of the load current), are utilized for the evaluation and comparison of these existing diagnostic methods. According to this comparison, it can be observed that, among these diagnostic methods, some of them have a high cost for implementation, some have a lower fault detection speed, and some of them have ambiguities in the diagnostic outcome. Such drawbacks stimulate the motivation to develop a more efficient and cost-effective diagnostic method for the NPC-inverter-based ASD

systems, which will be elaborated in detail in Chapter 4.

Table 2.2: Comparison of various diagnostic methods in the literature for multilevel NPC inverter.

Diagnostic method	Diagnostic capabilities	Cost increase	Computation complexity	Detection speed
Concordia current pattern method [52]	Open-circuit switch faults	No	Medium	$\leq 2T_0$
Average current park's vector approach [53]	Open-circuit Switch faults	No	Medium	$\leq 2T_0$
Current distortion method [55]	Part of the open-circuit faults	No	Medium	$\leq T_0$
Inverter pole voltage method [56, 57]	All the IGBT open-circuit faults	High	Low	$\leq T_0$
Neutral-point branch current method [58]	Both open and short-circuit faults	High	Low	$\leq T_0$

2.3 Fault-Tolerant Power Converter Topologies

2.3.1 Introduction

Fault-tolerant operation plays a crucial role for the reliability of power converters during the post-fault stage, especially when a switch fault has been detected. A fault-tolerant power converter should be able to tolerate any device faults, including both open-circuit and short-circuit faults. Such fault-tolerant capability could be achieved by either software-based fault-tolerant control strategies, or hardware-based redundant design concepts, or can be a solution combining both software and hardware modifications. Software-based fault-

tolerant operation of power converters is generally only suitable for certain types of multilevel converters, in which there are more redundant switching states to be utilized during post-fault stage to synthesize satisfied output voltages. Hardware-based redundant design is a universal solution for almost all the power converters. A simple fault-tolerant power converter can be designed merely based on adding one or more redundant inverter legs, or even parallel connecting one additional converter, to provide back-up solutions to any faulty switches or inverter legs. However, the acceptance of such redundant design methodologies by industries is mostly constrained by the dramatic cost increase, expansion of physical volume, and the increased complexity of hardware circuits. Hence, regarding the multilevel NPC converters being investigated in this dissertation, a more attractive solution to achieve fault-tolerant operation is to fully utilize the redundant switching states while adding a minimum number of redundant power devices.

In addition to these concerns on cost and physical volume increase for fault-tolerant power converters, another concern is the output performance degradation during post-fault operation, such as deratings in output voltages and currents, harmonic distortions, decreased efficiency, and the like. Ideally, these output performance of the power converters should be at kept the same as these during normal operation. However, it is very challenging to meet this objective in practice, due to the absence of certain switching states related with the faulty switch and the switching/conduction of redundant devices/phase legs. Almost all of the existing fault-tolerant solutions in the literature either require derated operation, or have degraded converter efficiency or harmonic distortion during post-fault operations. The literature review below will further illustrate such perspectives.

2.3.2 Existing Fault-Tolerant Topologies for NPC Converters

In this section, all the existing fault-tolerant topologies in the literature for NPC converters will be reviewed. It should be clarified that the NPC inverters being examined here include both I-Type and T-Type NPC inverters, and both of them have been widely used in industries. The operating principle and characteristic comparisons between these two types of NPC inverters were analyzed in [60] and thus will not be repeated here. The following literature review will be first focused on the fault-tolerant operations of I-type NPC inverters, and then followed by the related literature review of the T-Type NPC inverters.

Fault-tolerant capability of the I-Type NPC inverter was early investigated in [61]. In this work, the fault-tolerant strategies of a three-phase three-level NPC inverter under singular short-circuit faulty condition of IGBTs and clamping diodes were discussed. Considering the circuit symmetry of NPC inverters, three cases of short-circuit conditions were analyzed. Taking the Phase-A leg of the NPC inverter topology shown in Fig. 2.16 as an example, these three short-circuit fault cases are as follows:

- Case I: Short-circuit fault in an outer switch S_{a1} or S_{a4}.
- Case II: Short-circuit fault in an inner switch S_{a2} or S_{a3}.
- Case III: Short-circuit fault in an antiparallel diode D_{a1} or D_{a2}.

Once there is a short-circuit switch fault in the inverter, the switching states that require the turn-off of this associated switch will be lost. Therefore, the switching strategies for the whole inverter will have to be modified, otherwise dc-

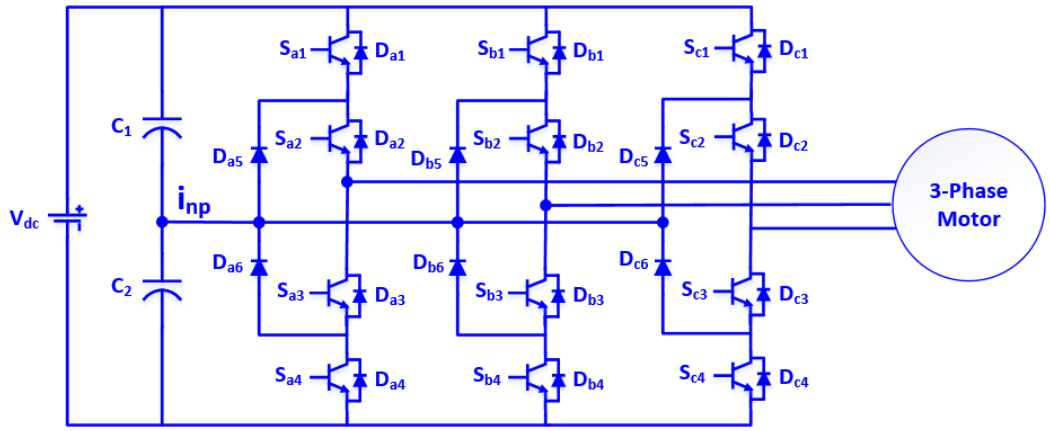


Figure 2.16: Circuit topology of a three-phase three-level I-Type NPC inverter.

bus shoot-through or capacitor short-circuit failures may occur. The unavailable switching states due to the short-circuit faults in S_{a1}, S_{a2} and D_{a1} are shown in the red shadowed parts in the voltage space vector diagram in Figs. 2.17 through 2.19, respectively. As can be seen that a few large voltage space vectors are lost for each of the fault cases, which indicates the necessity of derated operation of the NPC inverter during the post-fault stage. Specifically, the NPC inverter cannot operate at a modulation index higher than 0.577 (i.e., $1/\sqrt{3}$) [61].

This reference [61] also discussed the fault-tolerant operation of NPC inverters in presence of any open-circuit switch faults. The proposed fault-tolerant control strategy is to connect the output terminal of the Phase-A to the dc-bus neutral point and accordingly modify the PWM strategy to output a derated three-phase balanced currents, if there is an open-circuit fault occurring in Phase-A leg. No further details were given in [61] regarding the implementation of such a fault-tolerant strategy. However, it is obvious that additional switches are needed to connect the phase-A leg to the dc-bus middle point if any of the inner switches (i.e., S_{x2} or S_{x3}, x=a, b, or c, see Fig. 2.16) encounters an open-circuit failure.

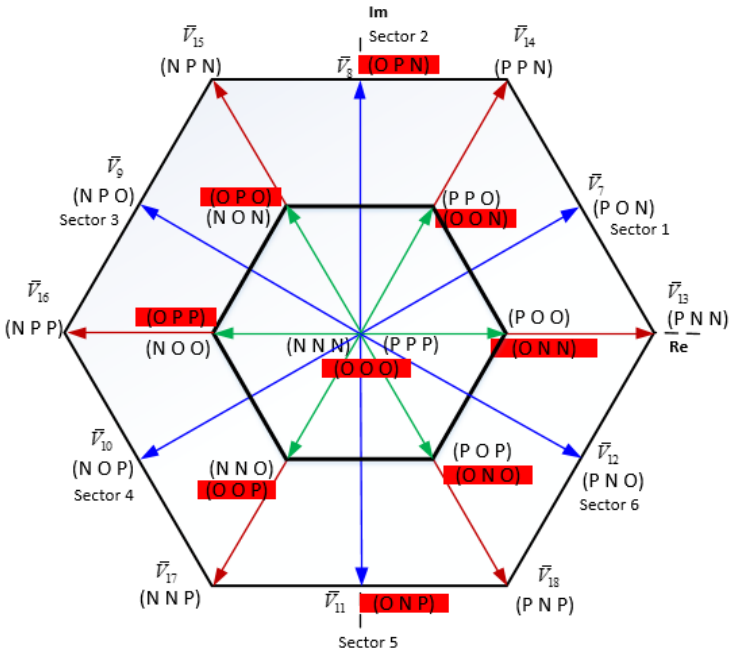


Figure 2.17: Unavailable (filled in red color) and available voltage space vectors due to the short-circuit fault in the switch S_{a1}.

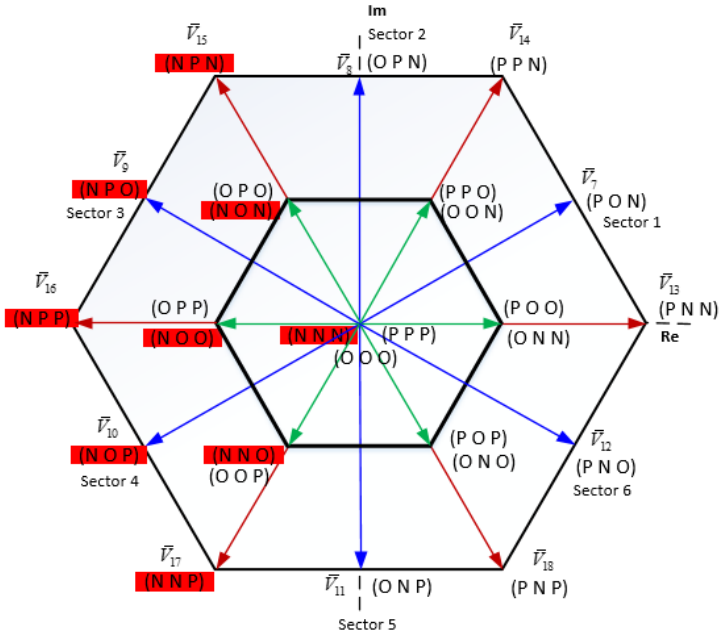


Figure 2.18: Unavailable (filled in red color) and available voltage space vectors due to the short-circuit fault in the switch S_{a2}.

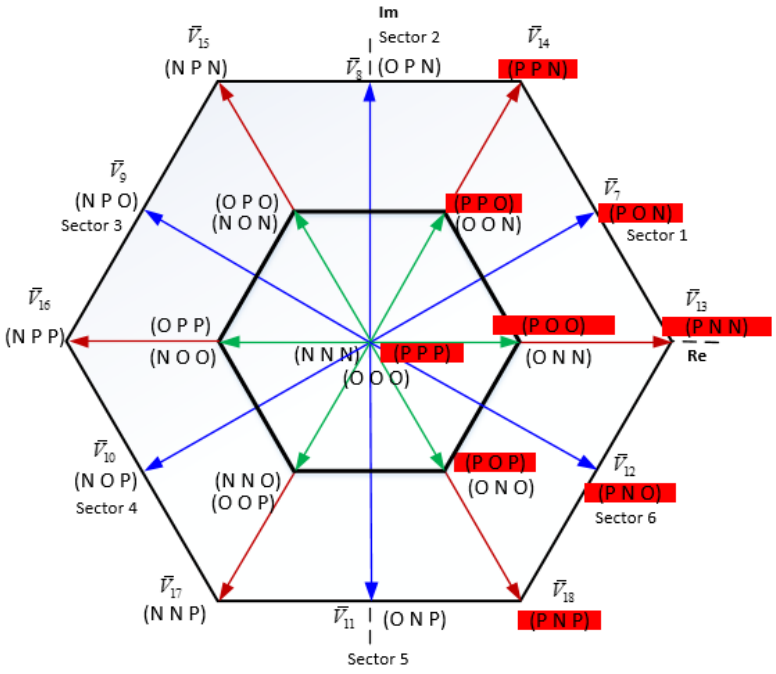


Figure 2.19: Unavailable (filled in red color) and available voltage space vectors due to the short-circuit fault in the switch D_{a1}.

Another fault-tolerant solution to NPC inverters was introduced in [62]. In this solution, three pairs of thyristors and fuses have been added to the NPC inverter circuit topology to improve its fault-tolerant capability, as shown in Fig. 2.20. The purpose of adding these thyristors is to avoid the short circuit of dc-bus capacitors when one of the switches has a short-circuit fault. For instance, when the switch S_{a1} (see Fig. 2.21) has a short-circuit fault, the upper dc-bus capacitor will be short circuited when the Phase-A leg of this NPC inverter is outputting a zero voltage state by turning on the inner switches S_{a2} and S_{a3}, as depicted in Fig. 2.21. Thanks to the addition of the thyristor T_{a1}, the upper clamp branch can be interrupted by turning on the thyristor T_{a1} and subsequently the blowing out of the fuse F_{a1}. The similar fault protection mechanism can be applied to the switch faults in other mechanisms, such as S_{x2} and S_{x3} (where x=a, b and c).

One advantage of this fault-tolerant solution is that no derating is required during fault-tolerant operation. However, there are three issues/drawbacks with this method. The first issue is that the fuses used in the fault-tolerant circuit topology typically have lower i^2t characteristic than that of the IGBTs, which indicates that the related IGBT may fail prior to the blow-out of the fuse. The second issue is that some of the IGBTs will encounter large voltage stress if there is a short-circuit fault in the series-connected adjacent switch on the same inverter leg. For instance, if the switch S_{a1} has a short-circuit fault, the switch S_{a2} has to withstand half of the dc-bus voltage, which may impose excessive thermal stress or cause a high-voltage breakdown on S_{a2}. The third issue or drawback of this fault-tolerant solution in [62] is the more complicated hardware circuits caused by these thyristors and the related gate driving circuits. Also, the addition of these six fuses may result in higher ohmic losses in the inverter, which will decrease the inverter efficiency.

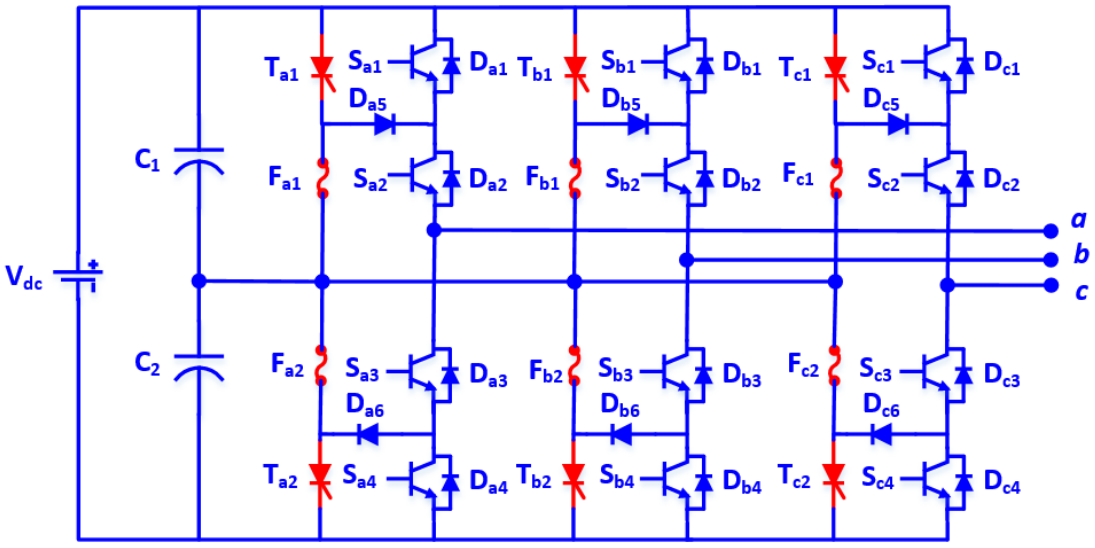


Figure 2.20: Modified NPC inverter topology for fault-tolerant operation (the redundant power devices are marked in red color).

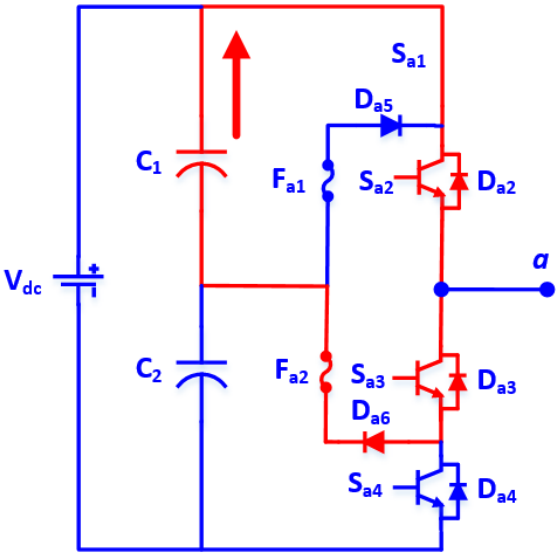


Figure 2.21: Current flow direction when the upper dc-bus capacitor is short-circuited by the short-circuit fault in the switch S_{a1} of the NPC inverter.

One attractive solution for the fault-tolerant operation of NPC inverters was introduced in [63]. Basically, an active switch, for instance, an IGBT device, is added to each of the clamping diode in the NPC inverter. As a result, the NPC inverter is upgraded to be an ANPC inverter, as shown in Fig. 2.22. The active switches added to the NPC inverter are shown in red color in Fig. 2.22. The fault-tolerant operation of this ANPC inverter is summarized as follows:

- **Case I: open-circuit fault in S_{a1}/D_{a1}.**

  When there is an open-circuit fault occurring in the IGBT module S_{a1}/D_{a1} (see Fig. 2.22), the output terminal of the Phase-A leg will be connected to the dc-bus neutral point by turning on switches S_{a2} and S_{a5}, or S_{a3} and S_{a6}. In other words, the voltage output of the Phase-A leg in the ANPC inverter will be zero. Accordingly, in order to output three-phase balanced currents,

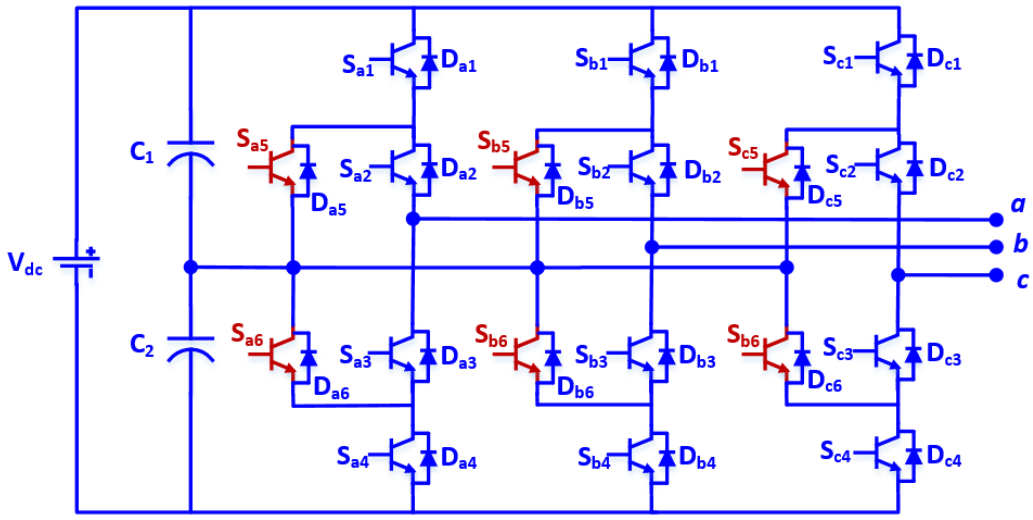


Figure 2.22: Circuit topology of a three-phase three-level ANPC inverter.

the PWM switching strategy needs to be changed from Equation (2.5) to Equation (2.6), which are shown as follows [63]:

$$\begin{cases} V_a = msin(2\pi ft) \\ V_b = msin(2\pi ft - \frac{2\pi}{3}) \\ V_c = msin(2\pi ft - \frac{4\pi}{3}) \end{cases} \tag{2.5}$$

$$\begin{cases} V_a' = 0 \\ V_b' = \sqrt{3}msin\left(2\pi ft + \pi + \frac{\pi}{6}\right) \\ V_c' = \sqrt{3}msin\left(2\pi ft + \frac{2\pi}{3} + \frac{\pi}{6}\right) \end{cases} \tag{2.6}$$

where, V_a, V_b, and V_c are the PWM reference signals under normal operation. V_a', V_b', and V_c' are the PWM reference signals under faulty conditions. m is amplitude the modulation index under normal operations. f is the fundamental output frequency of the NPC inverter.

It can be seen from Equations (2.5) and (2.6) that the PWM amplitude modulation index is derated by $1/\sqrt{3}$ during post-fault operations, which indicates that the output voltages of the ANPC inverter during a post-fault stage cannot meet

the rated voltage requirements in certain applications (e.g., UPS, EVs/HEVs, etc). For instance, the EVs/HEVs require rated or higher ac voltages from the inverters for the field weakening operation of the permanent magnet synchronous machines (PMSMs), which is generally evaluated by an important operating characteristic, namely, constant power speed ratio (CPSR). Assuming that such NPC/ANPC inverters in [63] are utilized in the powertrain systems of the EVs/HEVs, the derated operations during the post-fault stage will prevent the vehicles from operating at high-power high-speed region, which is not allowed for such practical applications. For more details about the field weakening operations of EVs/HEVs, please see the references [64, 65].

- **Case II: open-circuit fault in S_{a2}/D_{a2}.**

  If there is an open-circuit fault in S_{a2}/D_{a2}, the associated fault-tolerant operation can be achieved by connecting the output terminal of the Phase-A leg to the dc-bus neutral point through the turn-on of the switches S_{a3} and S_{a6} for commutating bi-directional current. As a result, the voltage output of the Phase-A leg will be zero, and the PWM strategy of the three-phase ANPC inverter will be modified accordingly to output derated three-phase voltages, which is the same as the fault-tolerant operating principle discussed for Case I.

- **Case III: short-circuit fault in S_{a1}/D_{a1}.**

  Regarding the short-circuit faults in S_{a1}/D_{a1}, the fault-tolerant solution is the same as the one presented in [61]. Thus, it will not be repeated here.

- **Case IV: short-circuit fault in S_{a2}/D_{a2}.**

  As for any short-circuit faults in S_{a2}/D_{a2}, the related fault-tolerant operation

can be realized by turning on the switch S_{a5} to connect the output terminal of the Phase-A leg to the dc-bus neutral point. The subsequent fault-tolerant operation is the same as these presented in Case I and Case II.

According to the review and discussion above, it can be seen that the ANPC inverter provides a very promising fault-tolerant solution for the NPC inverter, although the output voltages during some of the post-fault operation have to be derated. Also, it should be mentioned that the ANPC inverter can distribute the device losses more evenly among the switching devices, compared to that in NPC inverter, as reported in [10][66-68]. Therefore, the maximum allowable switching frequency and output power in the ANPC inverters will be higher than these for the conventional NPC inverters.

A four-leg fault-tolerant solution for NPC inverters was introduced in [17], and the circuit topology was given in Fig. 2.23. The purpose of adding this fourth phase leg is to provide a back-up to the NPC inverter in case of any switch faults occurring in one of the three main legs, while this fourth leg can also be used to provide a stiff neutral-point voltage under healthy conditions. Consequently, the low-frequency voltage oscillation that usually appears at the dc-bus neutral point is eliminated, and the PWM voltage space vectors can be more intensively utilized to optimize the inverter efficiency and harmonic distortions, instead of being considered for controlling the dc-bus neutral point voltage. However, all these benefits are achieved at the cost of many more redundant hardware devices used in this fault-tolerant inverter topology, which specifically include one capacitor, four fast-acting fuses, six IGBT modules, three TRIACs (triode for alternating

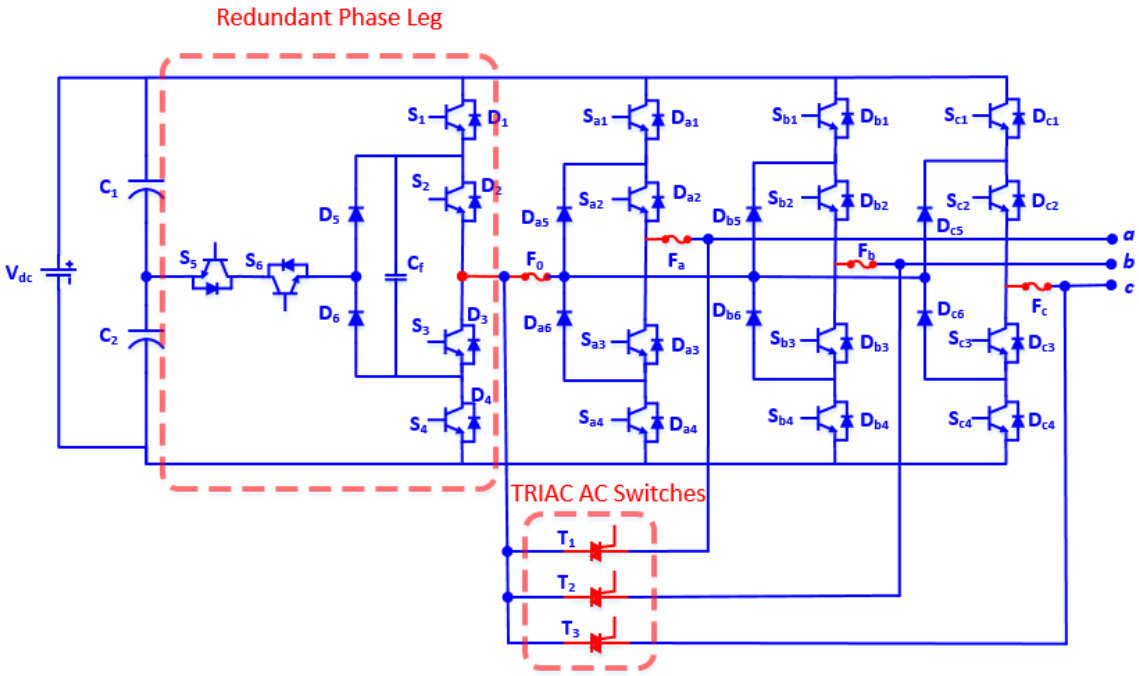


Figure 2.23: A four-leg fault-tolerant topology for three-level NPC inverters (the redundant power devices for fault-tolerant operations are circled/marked in red color).

current), as well as their associated gate driving circuits, as shown in Fig. 2.23.

Based on the review and discussion of these existing fault-tolerant solutions for multilevel NPC inverters in the literature, a comprehensive comparison between these fault-tolerant solutions is shown in Table 2.3.

Table 2.3: Comparison of existing fault-tolerant operation solutions for multilevel NPC inverters.

Fault-Tolerant Solution	Fault-Tolerant Capability	Cost Increase	Derating	Efficiency
Inherent fault-tolerant characteristic of NPC inverters [61]	Tolerate short-circuit and part of the open-circuit switch faults	No	Yes	Unchanged
Thyristor-assisted method [62]	Tolerate both short-circuit and open-circuit switch faults*	High	Yes	Decrease
ANPC converter method [63]	Tolerate short-circuit and open-circuit switch faults	Medium	Yes	Decrease
Four-leg NPC inverter method [17]	Tolerate both short-circuit and open-circuit switch faults	Very High	No	Decrease

* This is based on the assumption that the fuses have a lower i^2t than the related IGBTs.

In addition to investigating the fault-tolerant solutions for the I-Type NPC inverters as discussed above, there also have been investigations on the fault-tolerant operations of three-level T-Type NPC inverters. As a matter of fact, T-Type inverters possess certain inherent fault-tolerant capabilities. Taking the Phase-A leg of the T-Type inverter shown in Fig. 2. 24 as an example, when the switch S_{a1} has an open-circuit fault, the output terminal of the Phase-A leg can be connected to the dc-bus neutral point through the conduction of S_{a3} and S_{a4} for commutating the bidirectional current, while the switch S_{a2} is kept in an OFF state. As a result, the output voltage of the Phase-A will be zero. Accordingly, the PWM switching pattern needs to be modified as given in Equations (2.5) and (2.6), so that the T-Type inverter can still output three-phase balanced but derated currents.

On the other hand, if the switch S_{x2} or S_{x3} (x=a, b, or c) has an open-circuit fault, this associated inverter leg will lose the access to the dc-bus neutral point. Under such scenario, this faulty leg have to be operated as a conventional two-level converter. No deratings are required for the output voltages and currents, but the harmonic distortions in these outputs will be somewhat higher compared to that under three-level operation. Moreover, the T-Type inverter shown in Fig. 2.24 can also tolerate short-circuit faults in its switch S_{x2} or S_{x3}, due to the available access to the dc-bus neutral point for Phase-A leg. More details on such inherent fault-tolerant capability of the T-Type inverter was reported in [69, 70].

It should be noticed that the original T-Type inverter does not have fault-tolerant capability for short-circuit faults in S_{x1} or S_{x4} (x=a, b, or c). Once such faults are diagnosed to be present in the inverter, the whole T-Type inverter has to be shut down before any more severe damages occur.

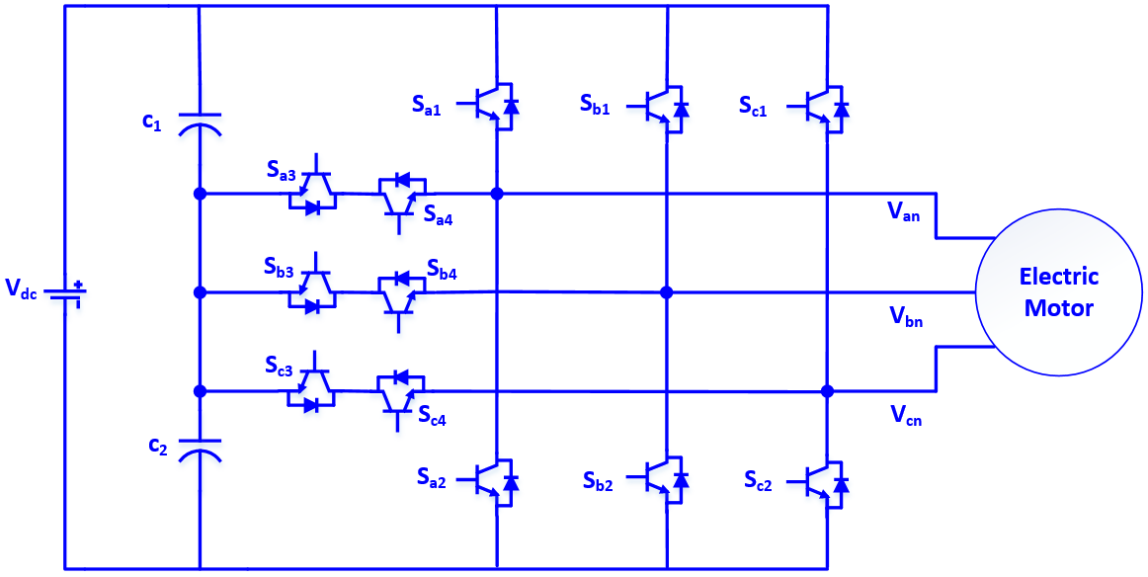


Figure 2.24: Circuit topology of a three-phase three-level T-Type NPC inverter.

In [15], a fault-tolerant topology was introduced for three-phase three-level T-Type inverters. The circuit topology of this fault-tolerant T-Type inverter is shown in Fig. 2.25. Unlike the fault-tolerant solution introduced in [69, 70], the fault-tolerant topology shown in Fig. 2.25 can tolerate both open-circuit and short-circuit switch faults, as well as guarantee the output of rated voltages during fault-tolerant operation. For instance, when the switch S_{a1} in the Phase-A leg of the T-Type inverter encounters an open-circuit fault, the fault-tolerant operation will be realized by the following two steps:

- Turning off the redundant switches T_{a1} and T_{a2} to disconnect the output terminal of Phase-A leg to the load, and disable all the PWM signals for the switches on Phase-A leg, including S_{a1}, S_{a2}, S_{a3}, and S_{a4}.
- Turning on the switch T_{a3}, so that the faulty Phase-A leg can be replaced by the redundant phase leg constituted by the switches S_{d1} and S_{d2}.
- Modulate the fourth leg with two-level PWM modulation, and modulate the Phase-B and Phase-C legs by three-level or two-level PWM strategies.

The fault-tolerant operations for any other fault cases were reported in [15]. It can be seen that such desired fault-tolerant capability with this proposed fault-tolerant topology for T-Type inverters is attributed to the addition of a complete redundant inverter leg to the original T-Type inverter topology, as circled in red dashed lines in Fig. 2.25. The penalty of this fault-tolerant solution is that too many redundant switching devices are employed, and some of these redundant devices, namely, T_{x1} and T_{x2} (x=a, b, or c), have to be kept in ON state during normal operations, which will cause much device losses and dramatically decrease the inverter efficiency.

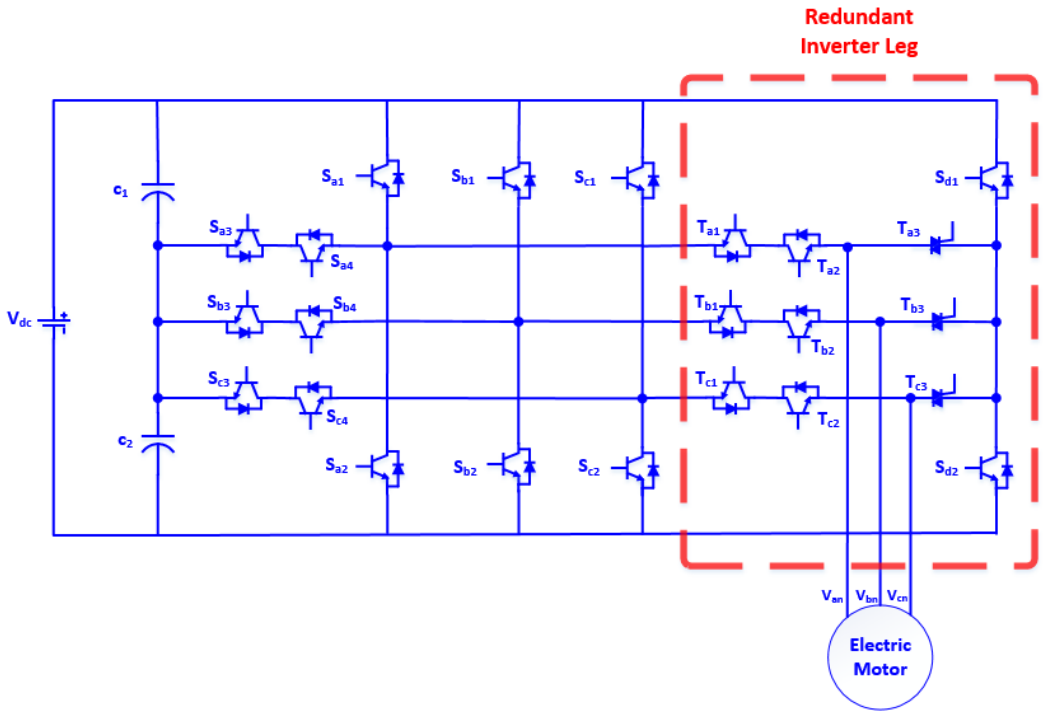


Figure 2.25: A fault-tolerant T-Type NPC inverter based on a redundant phase leg (the redundant leg is circled in red dashed lines).

2.4 Summary

This chapter reviewed the existing health monitoring and fault-tolerant operation solutions for multilevel NPC converters. Specifically, this literature review includes three following topics:

- Power cycling lifetime improvement methods for IGBTs in the NPC inverters.
- On-line diagnostic methods for switch faults in NPC inverters.
- Fault-tolerant operation solutions for I-Type and T-Type NPC inverters.

Among these methods for IGBT lifetime improvement in the literature [33-39], they either focus on upgrading the materials for bond wires, soldering, or baseplate in the IGBT internal structure to reduce the mismatch of CTEs, or

concentrate on reducing the switching frequencies and load currents in the converter control strategies with the ultimate objective to attenuate the thermal losses and junction temperatures in the devices. As discussed in Section 2.1, the former methods are typically at a higher cost, while the latter methods sometimes will cause more harmonic distortions in the output voltages and currents, which is not desirable in certain applications where there are stringent requirements on the power qualities. However, such drawbacks provide the stimulations and possibilities to develop a more promising method in this dissertation, to flexibly adjust the IGBT junction temperature and extend the IGBT lifetime under thermal overload conditions, while maintaining satisfactory power inverter performance.

Regarding the on-line diagnostic methods for open-circuit and short-circuit switch faults in multilevel NPC converters, all of these methods are capable to diagnose some of the IGBT faults in NPC converters. However, some of them [56-58] can accurately and promptly diagnose the switch faults, but the implementation of these methods requires higher system cost. Other methods [52, 53] do not demand any additional sensors or hardware devices, but the detection speed is slower than expected. Nevertheless, it should be noticed that some critical information on NPC inverters that are typically available in the related microcontrollers have not been fully utilized in any of these existing diagnostic methods [52, 53], [55-58]. Such information includes the instantaneous switching states and dc-bus voltages. If they can be utilized in combination with the phase current information, another more promising diagnostic method can be probably developed with a lower cost and faster detection speed. This will motivate the investigations to be presented in Chapter 4 of this dissertation.

As for the existing methods for the fault-tolerant operations of NPC converters, I-Type NPC inverters have received extensive attention and interest in the past years, and some of these fault-tolerant operation techniques [54, 59] have been well established and accepted. However, the present fault-tolerant solutions to T-Type NPC inverters still leave much to be desired, due to either the high cost in implementation or the derated output during post-fault stages. Hence, in Chapter 5 of this dissertation, the author will focus on the development of a novel fault-tolerant solution for T-Type NPC inverters, to meet the objectives of lower cost increase, performance improvement during healthy conditions, and rated voltage output during fault-tolerant operations.

CHAPTER 3

LIFETIME EXTENSION OF NPC INVERTERS WITH AN IMPROVED PWM METHOD

3.1 Introduction

As discussed in Chapter 2, the lifetime of IGBT modules degrades dramatically when there is large swing in the chip junction temperatures. For an IGBT-based power converter in an ASD, large swings of IGBT junction temperatures typically happen when the ASD is operated at low output frequencies, as reported in [5-7]. This is because the thermal time constant of a power converter under low-frequency operation would be higher than the time constant of the IGBT thermal impedance, thus a much more considerable temperature variation/swing will occur in the IGBT modules. Obviously, such phenomenon mainly occurs in dc-ac PWM inverters in ASDs rather than ac-dc PWM rectifiers, since ac-dc PWM rectifiers in ASDs generally interface with grid frequencies (e.g., 50Hz/60Hz).

In this Chapter, the lifetime of a three-level NPC inverter at low output frequencies will be investigated. First, analytical models for lifetime prediction of IGBT modules will be reviewed. Second, procedures for lifetime prediction of such IGBTs will be introduced, which include the conduction and switching losses calculation in such an NPC inverter as well as its thermal modelling. Third, a DPWM method will be introduced to extend the lifetime of an NPC inverter at low output frequencies. Finally, simulation and experimental results will be given to verify the effectiveness of this proposed PWM method.

3.2 Analytical Models for IGBT Lifetime Estimation

It is well known that wear-out of IGBT modules by the thermal-mechanical stress in internal bond wires and soldering joints cannot be promptly detected by conventional thermal sensors or current sensors due to the slow response of these sensors [71]. The most common way to predict the lifetime of IGBT modules is through using the analytical lifetime models due to their fast on-line calculation and simplicity. Therefore, selecting a proper analytical model is a fundamental step in lifetime prediction of IGBT power converters.

Over the past few years, extensive research in this area has led to various lifetime prediction models [24][72-74]. In [72-73], a Coffin-Manson law was used to model the power cycling capability of power devices. In this law, the number of cycles to failure is assumed to be inversely proportional to the swing of device junction temperatures per power cycle. The mathematical model of this Coffin-Manson law is expressed as follows:

$$N_f = A \cdot \Delta T_j^{-\alpha} \tag{3.1}$$

where, N_f is the number of cycles to failure. A and α are module-dependent positive constants. ΔT_j is the swing magnitude of device junction temperatures in one power cycle.

A more detailed analytical model was introduced in [74], namely, Bayerer's model, which considered multiple variables, including junction temperature swings (ΔT_j), absolute junction temperatures (T_j), power-on-time (t_{on}), chip thickness, bonding technology, diameter of bonding wires (D), applied dc current

per wire bond (I), and blocking voltage (V). The mathematical equation of this Bayerer's model is given here:

$$N_f = K \cdot \Delta T_j^{\beta_1} \cdot e^{\frac{\beta_2}{T_j+273}} \cdot {t_{on}}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \tag{3.2}$$

where, K, β_1, β_2, β_3, β_4, β_5, and β_6 are all module-based constants.

It can be seen that this Bayerer's model requires more variables to calculate the remaining device lifetime. Some of the constants and variables have to be obtained through experimental testing, and therefore not convenient to be used in IGBT lifetime evaluation. As pointed out in [74], the Bayerer's model is not a universal or generalized model, and the consultation with the device manufacturer is recommended before the utilization of this model for device lifetime investigation.

Another well-known lifetime prediction empirical model was proposed in [24], in which the mean value of device junction temperatures were considered by adding an Arrhenius factor to the Coffin-Manson law. Such a model is called "Coffin-Manson-Arrhenius" model, and its mathematical expression is given as follows [24]:

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot \exp[Q/R \cdot T_m] \tag{3.3}$$

where, Q and R are also module-dependent constants; T_m is the mean value of device junction temperatures in one power cycle. Most semiconductor device manufactures follow the Coffin-Manson-Arrhenius model for predicting the remaining lifetime of power converters and hence the corresponding constants are readily available. In this dissertation, the Coffin-Manson-Arrhenius model is used

for predicting the remaining lifetime of power converters.

As can be seen from (3.3), the lifetime of an IGBT module can be predicted as long as the junction temperature data is available. Also, the value of ΔT_j of semiconductor devices is the most important factor influencing the lifetime of IGBT modules, which indicates that the lifetime of an IGBT module could be extended if the swing magnitude of the IGBT junction temperatures, ΔT_j, can be attenuated by improving the PWM strategies.

3.3 Lifetime Prediction Process of Power Converters

As introduced in Session 3.2, evaluation of the number of cycles to failure, N_f, of an IGBT module, requires the junction temperature data to be obtained through the dissipated power losses of the IGBT and the corresponding thermal network. A basic flowchart of lifetime prediction of IGBT power converters is shown in Fig. 3.1. It should be noted that the lifetime of the whole power converter is determined by the shortest lifetime among its power devices. The details of calculating device power losses and modelling the related thermal RC network are explained in the following sub-sessions.

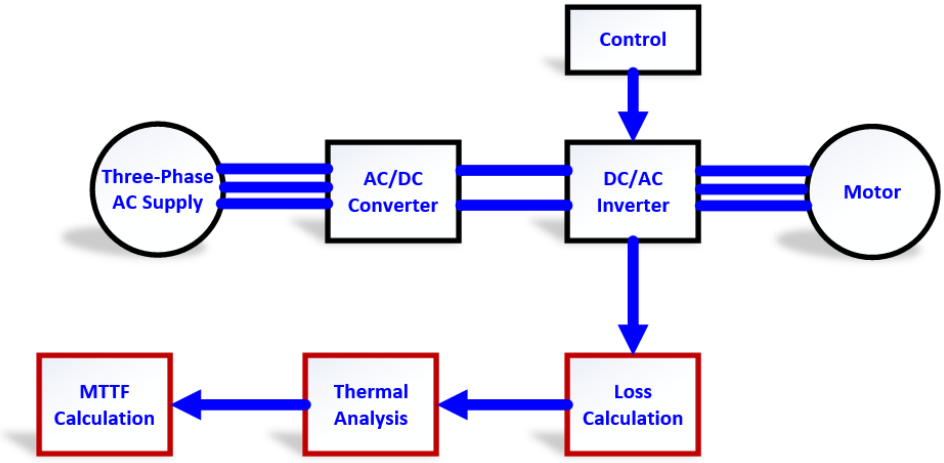


Figure 3.1: Lifetime prediction process of PWM power inverters.

3.3.1 Calculation of Device Conduction Losses

It is well known that conduction losses of semiconductor devices depend on the instantaneous on-state voltage and conducting current. Here, in this work, the instantaneous value of the IGBT conduction losses is calculated based on the following equations [75]:

$$u_{ce}(t) = u_{ce0} + r_{on} \cdot i_c(t) \tag{3.4}$$

$$p_{con}(t) = u_{ce}(t) \cdot i_c(t) = u_{ce0} \cdot i_c(t) + r_{on} \cdot i_c^2(t) \tag{3.5}$$

where, u_{ce0} is the voltage drop of the IGBT chip at near-zero forward current; r_{on} is the on-state resistance; $i_c(t)$ is the instantaneous IGBT collector current; $p_{con}(t)$ is the instantaneous conduction losses of the IGBT.

If the average IGBT current value is I_{av}, and the RMS value of the IGBT current is I_{rms}, then the average IGBT conduction losses can be expresses as:

$$P_{av\_con} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{con}(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (u_{ce0} \cdot i_c(t) + r_{on} \cdot i_c^2(t))dt \tag{3.6}$$

$$P_{av\_con} = u_{ce0} \cdot I_{av} + r_{on} \cdot I_{rms}^2 \tag{3.7}$$

where, P_{av_con} is the average IGBT conduction losses, and T_{sw} represents the switching period.

Similarly, the conduction losses of the antiparallel diodes are calculated based on the following equations:

$$u_d(t) = u_{d0} + r_d \cdot i_d(t) \tag{3.8}$$

$$p_{d\_con}(t) = u_d(t) \cdot i_d(t) = u_{d0} \cdot i_d(t) + r_d \cdot i_d^2(t) \tag{3.9}$$

$$P_{d\_av\_con} = \frac{1}{T_{sw}} \int_0^{T_{sw}} P_{d\_con}(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (u_{d0} \cdot i_d(t) + r_d \cdot i_d^2(t))dt \tag{3.10}$$

$$P_{d\_av\_con} = u_{d0} \cdot I_{d\_av}(t) + r_d \cdot I_{d\_rms}^2 \tag{3.11}$$

where, u_d is the voltage drop across the diode at certain dc current, and u_{d0} refers to the approximated voltage drop of the diode at near-zero forwarding current. r_d is the slop resistance of the diode chip, and i_d is the current flowing through the diode. Also, p_{d_con} and $P_{d\_av\_con}$ represents the instantaneous and average conduction losses in the diode, respectively. I_{d_av} and I_{d_rms} refer to the average diode current and RMS value of the diode current, respectively.

It can be seen that the calculation of IGBT and diode conduction losses depends on the current-voltage (I-V) curves of the devices under various junction temperatures. The device loss calculation in this work is conducted in PLECS simulation software, where an integrated visual editor provides the access to input the I-V curve of each device to model the conduction loss of IGBTs and diodes based on a manufacturer's datasheet. For operating points beyond the given data from the datasheet, PLECS will conduct an estimation based on linear interpolation

[76]. For the IGBT module (Infineon F3L200R07PE4) adopted in this work, the I-V data of IGBTs and their free-wheeling diodes (FWDs) was input into the model via thermal editors in PLECS software, as shown in Figs. 3.2-3.3.

It should be noted that, the clamping diodes in the NPC inverters have the same ratings and characteristics as the IGBT free-wheeling diodes (FWD), according to the manufacture datasheet [77]. Thus, the modeling of conduction and switching losses of clamping diodes will not be repeated, since it is the same as the modeling for the IGBT free-wheeling diodes in an NPC inverter.

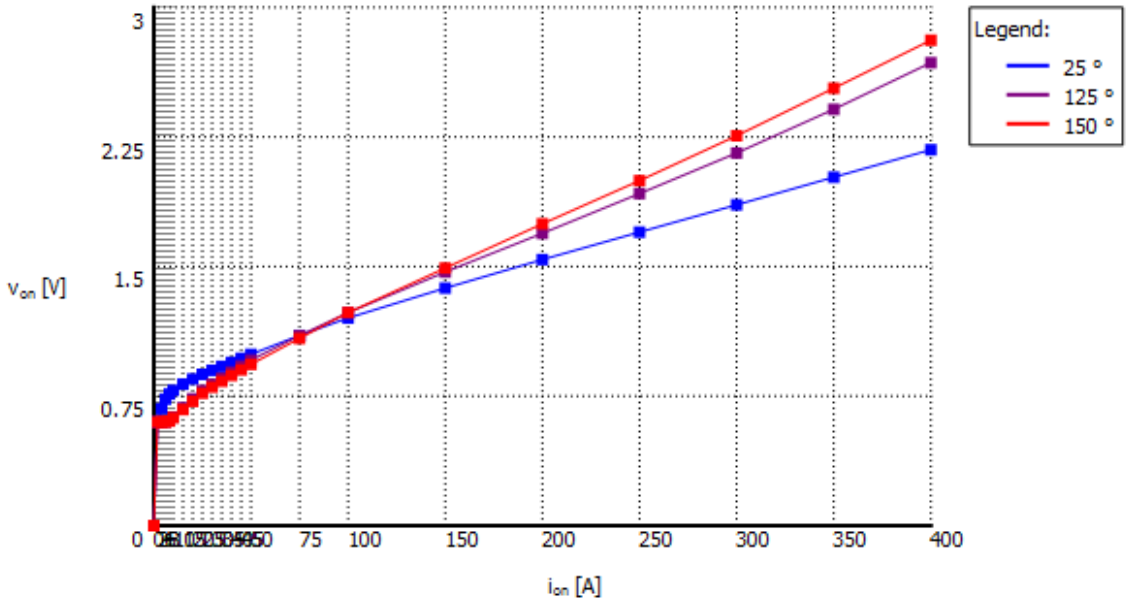


Figure 3.2: Modeling of the conduction losses (I-V curves) of the IGBTs in the three-level NPC inverter.

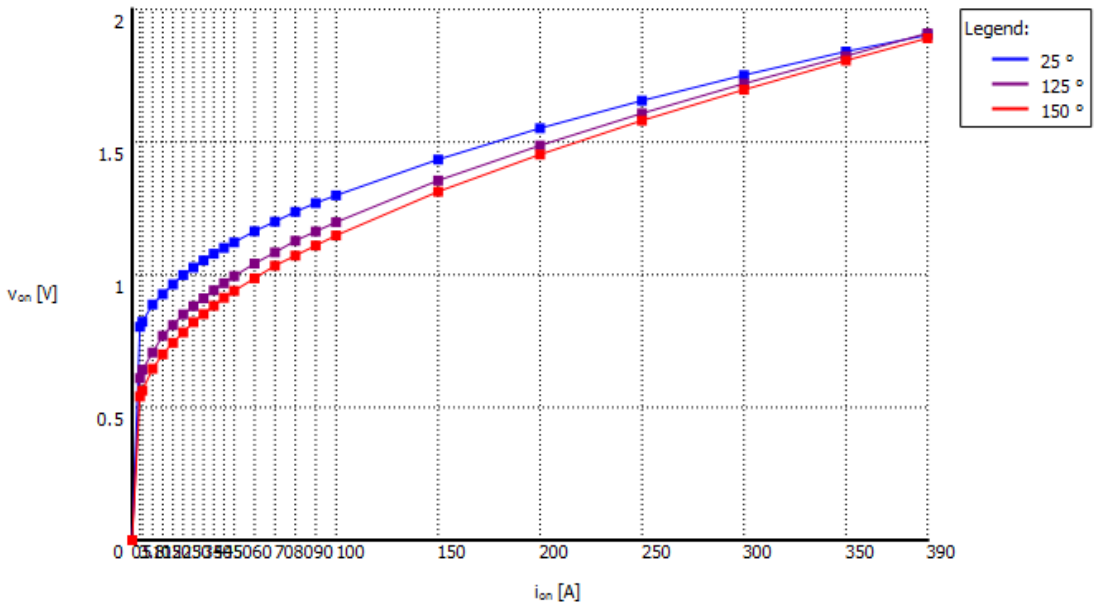


Figure 3.3: Modeling of the conduction losses (I-V curves) of the free-wheeling diodes used in the three-level NPC inverter.

3.3.2 Calculation of Device Switching Losses

Switching loss of semiconductor devices depends on the turn-on and turn-off energy at specific operating points (current, blocking voltage, and junction temperature). The mathematical model for calculating IGBT instantaneous switching loss, $P_{sw}(t)$, is given as follows [75]:

$$P_{sw}(t) = \left(E_{on}\left(i_c, v_{ce}, T_j\right) + E_{off}\left(i_c, v_{ce}, T_j\right)\right) \cdot f_{sw} \tag{3.12}$$

where, $E_{on}\left(i_c, v_{ce}, T_j\right)$ and $E_{off}\left(i_c, v_{ce}, T_j\right)$ refer to the switching-on energy and switching-off energy at the specific levels of the currents, voltages and junction temperatures, respectively, while f_{sw} is the switching frequency.

The calculation of diode reverse recovery losses is carried out in a similar manner to that for IGBTs as given in (3.12), and therefore will not be elaborated

further here. In order to model the switching losses of IGBTs and diodes in PLECS software, the turn-on and turn-off energy curves of each device are input into component thermal descriptions of the NPC inverters, as depicted in Figs. 3.4 through 3.6.

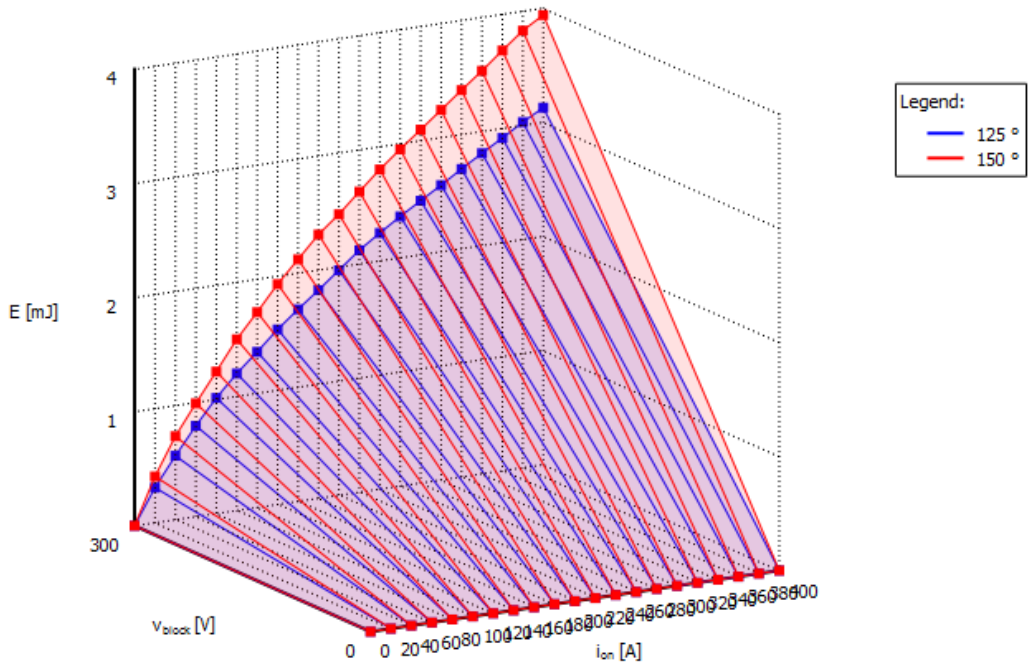


Figure 3.4: Modeling of the switching-on losses (E_{on}) of the IGBTs used in the three-level NPC inverter.

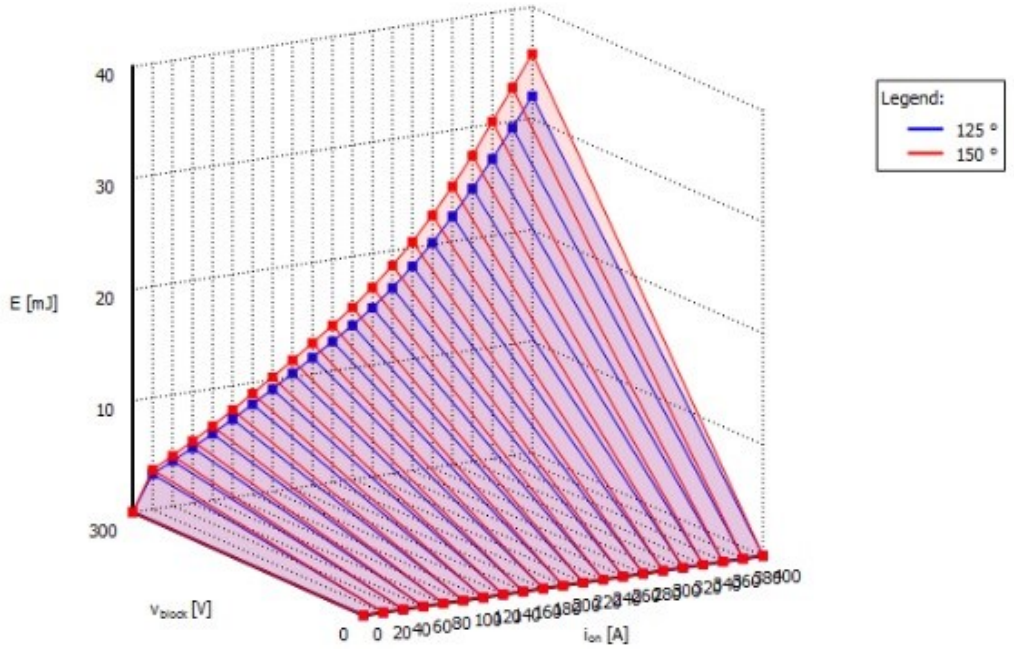


Figure 3.5: Modeling of the switching-off losses (E_{off}) of the IGBTs used in the three-level NPC inverter.

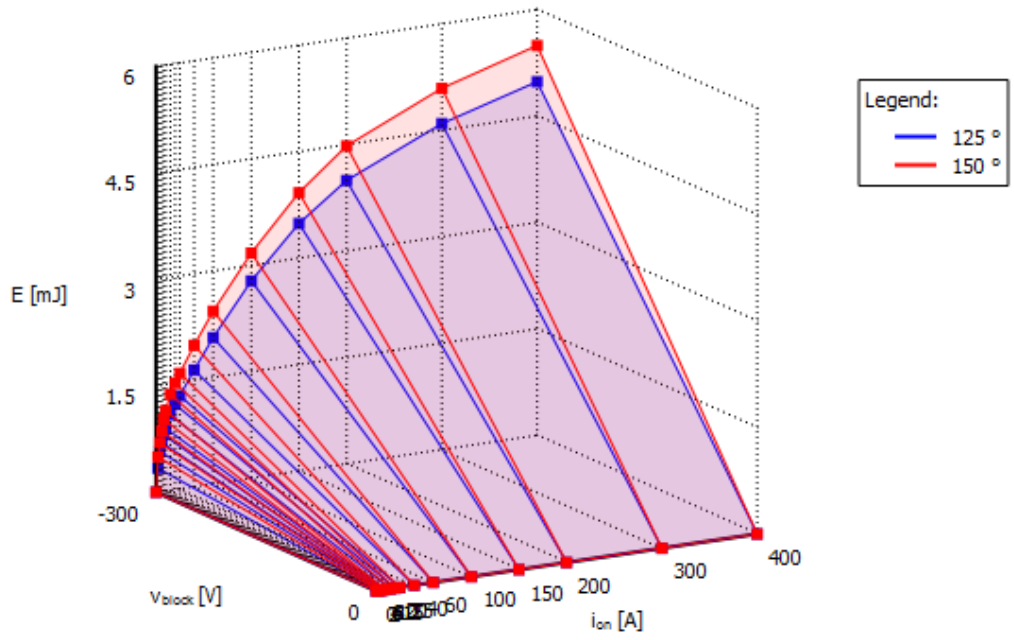


Figure 3.6: Modeling of the reverse recovery losses of the free-wheeling diodes used in the three-level NPC inverter.

3.3.3 Thermal Modeling of NPC Inverters

To analyze the thermal performance of the NPC inverter, thermal equivalent RC network from device junction to module case, from case to heatsink, and from heatsink to the ambient needs to be modelled. A fourth-order Foster model [78] describing the junction to case of IGBT modules is adopted in this work, which is shown in Fig. 3.7. The thermal impedance from device case to heatsink as well as from heatsink to ambient are also considered here, as illustrated in Fig. 3.8. It should be mentioned that the parameters of the fourth-order Foster model describing the junction to case thermal conduction of IGBTs and diodes are extracted from their transient thermal impedance curves given by the manufacture datasheet [77].

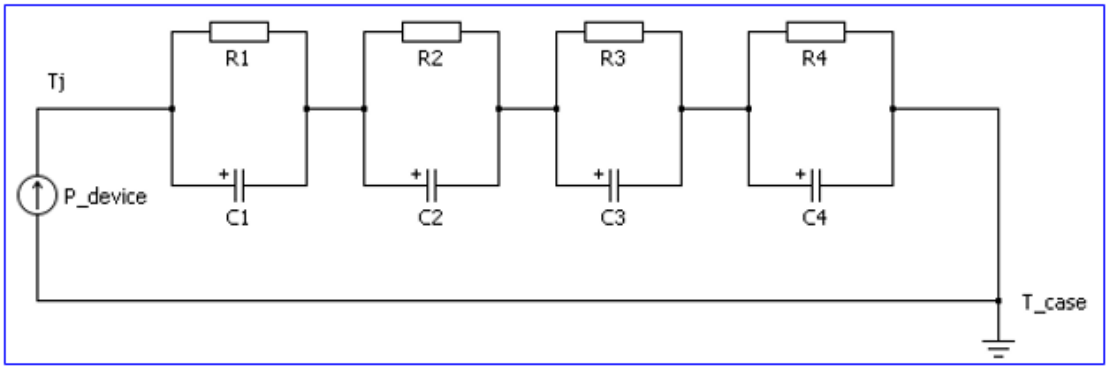


Figure 3.7: Junction-to-case fourth-order Foster thermal network for each power device (IGBTs/diodes).

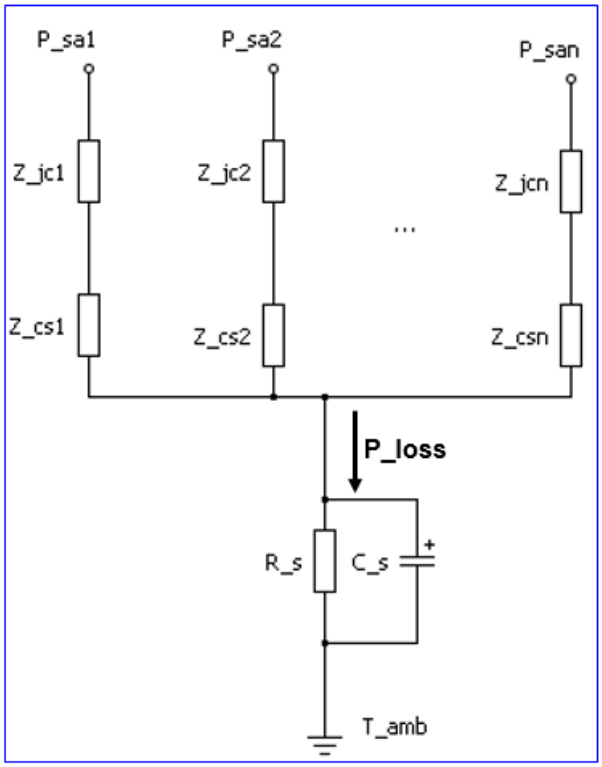


Figure 3.8: Thermal RC network of the whole three-level NPC inverter.

With the modeling of device conduction losses, switching losses, and the thermal modeling introduced above, the dissipated power of each device in the NPC inverter will be absorbed by the heatsink in the PLECS simulation software, which will in turn provide a dynamic isotherm environment to the components it enclosed. Through this way, the thermal modeling of the NPC inverter is developed, and furthermore the variation of IGBT and diode junction temperatures and the related lifetime of the NPC inverter can be predicted.

3.4 The Proposed Novel DPWM Method

One important factor contributing to the short lifetime of power inverters at low output frequency lies in the fact that the time constant of semiconductor device thermal systems is much lower than the fundamental period of the inverter output.

Thus, the lifetime of NPC inverters could be improved upon by injecting a zero sequence signal with higher frequency than the thermal time constant of the semiconductor devices. Based on an exhaustive investigation of various PWM methods on the influence of the IGBT thermal performance, a novel discontinuous PWM (NDPWM) method will be introduced to extend the lifetime of IGBT-based NPC inverters, especially for low-frequency operations. Details of this novel PWM scheme and its relationship to the conventional SVPWM are given next.

Assuming that the duty ratio for each phase of an NPC inverter under carrier-based SPWM can be written as follows:

$$\begin{cases} d_u = m_a \cos(\theta) \\ d_v = m_a \cos(\theta - 2\pi/3) \\ d_w = m_a \cos(\theta - 4\pi/3) \end{cases} \tag{3.13}$$

where, m_a, is the amplitude modulation index, and θ is the initial phase angle, it follows that the instantaneous maximum and minimum duty ratio will be:

$$d_{max} = \max(d_u, d_v, d_w), \;\; d_{min} = \min(d_u, d_v, d_w) \tag{3.14}$$

In conventional SVPWM, the injected zero-sequence signal was defined as:

$$d_0 = -(d_{max} + d_{min})/2 \tag{3.15}$$

With the injection of such a zero-sequence signal, the duty ratio for each phase of an NPC inverter under SVPWM can be written as:

$$\begin{cases} d_{u,SV} = m_a \cos(\theta) + d_0 \\ d_{v,SV} = m_a \cos(\theta - 2\pi/3) + d_0 \\ d_{w,SV} = m_a \cos(\theta - 4\pi/3) + d_0 \end{cases} \tag{3.16}$$

However, to reduce the time constant of the IGBT thermal systems, a zero-

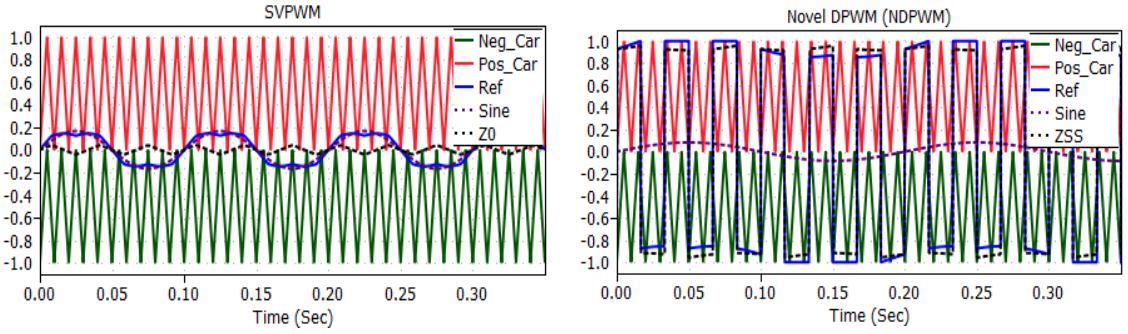
sequence signal with a fundamental frequency higher than that of the IGBT junction-to-case time constants is defined as follows:

$$d_{zss} = \begin{cases} 1 - d_{max}, & \sin(2\pi f_{cm} t) > 0 \\ -1 - d_{min}, & \sin(2\pi f_{cm} t) < 0 \end{cases} \tag{3.17}$$

where, f_{cm} is the fundamental frequency of the injected zero-sequence signal. Therefore, the duty ratio for each phase under this novel discontinuous PWM method, namely, NDPWM, will be:

$$\begin{cases} d_{u,NDPWM} = m_a \cos(\theta) + d_{zss} \\ d_{v,NDPWM} = m_a \cos(\theta - 2\pi/3) + d_{zss} \\ d_{w,NDPWM} = m_a \cos(\theta - 4\pi/3) + d_{zss} \end{cases} \tag{3.18}$$

A graphical illustration of the SVPWM method and the proposed NDPWM method is shown in Figs. 3.9 (a) and (b), respectively, in which the red and green triangular signals are the upper and lower carrier signals, respectively. The purple sinusoidal signal is the reference signal used in conventional SPWM, and the blue signals in both figures are the duty ratios for one of the three phase legs in the NPC inverter.



(a) (b)

Figure 3.9: Illustration of the PWM methods for the three-level NPC inverter (a) SVPWM (b) NDPWM.

3.5 Simulation Results

In the PLECS simulation software, both the SVPWM and NDPWM methods for a 50 kVA NPC-inverter-based ASD are implemented. In all the simulations, the input power supply is a three-phase 480V/60Hz source. The switching frequency in both the SVPWM and NDPWM methods is set at 4 kHz. The initial ambient temperature for all device thermal models is assumed to be 40°C. The output frequency of the ASD is regulated ranging from 2 Hz to 60 Hz under open-loop constant volts/Hertz (V/Hz) scalar control. All the parameters for the subject ASD investigated in the simulation are given in Table 3.1.

Table 3.1: Specifications of the ASD based on an NPC inverter.

Control mode	Open-loop scalar control (V/Hz)		
Input	Line-to-line voltage	480	V_{RMS}, three phase
	Frequency	60	Hz
	Switching frequency	4	kHz
	DC bus voltage	650	V_{dc}, max
	Initial ambient temp.	40	^{o}C
Output	Rated power	20	kVA
	Overload Current	180	A_{RMS}, max
	Line-to-line Voltage	480	V_{RMS}, three phase

For every output frequency, the device losses and the related swing magnitudes of the junction temperatures of each device are correspondingly obtained from the simulation. The junction temperature profiles of each device in the NPC inverter under the NDPWM method are compared to these under the SVPWM method at low frequencies. These profiles are given in Figs. 3.10 through 3.12. It should be noted that, considering the symmetries of the NPC inverter

topology, only half of the semiconductor devices in one phase leg are investigated (S_{x1}, S_{x2}, D_{x1}, D_{x2}, and D_{x5}, x≡a, b, or c, as shown in Fig. 2.16), and the other half of the complimentary devices have the identical thermal performance.

Since the lifetime of the NPC inverter is mainly determined by the most thermally-stressed component, which in this case happens to be the clamping diodes at low output frequency operation. Accordingly, the number of cycles to failure, N_f, can be computed based on substituting the ΔT_j and $\overline{T_j}$ of the clamping diodes into the Coffin-Manson-Arrhenius model given in (3.1). According to the power cycling data provided by the manufacturer, the IGBT module constants in (3.3) are obtained through curve fitting techniques. In this work, the values of these constants used in this model are listed as follows: A=$3.3125*10^6$, $\alpha = -5.039$, Q=$9.89*10^{-20}$, and R=$1.38066*10^{-23}$. Thus, the values of N_f for the NPC inverter can be calculated at various frequencies, which are depicted in Fig. 3.13. As can be seen in Fig. 3.13, the number of cycles to failure, N_f, decreases dramatically at low output frequencies under the SVPWM method. For instance, the value of N_f is reduced to 200,000 cycles at 2 Hz, which may result in a remaining useful lifetime (RUL) of just a few days if one is to keep operating the NPC inverter at such a lower frequency or near dc condition. However, with the implementation of the NDPWM method, the number of cycles to failure, N_f, is significantly improved at both the low and the high output frequency operations, as again demonstrated in Fig. 3.13. Once more, as can be seen, the value of N_f is improved to up to 1,130,200 cycles by using NDPWM at the 2 Hz of low-frequency operation of this NPC inverter. This is almost 5.7 times higher than the value of N_f of the NPC inverter modulated by the 3-level SVPWM method.

Moreover, at low frequencies, the thermal stress is most severe in the clamping diodes of the NPC inverter modulated by the 3-level SVPWM method. Such thermal stress is significantly mitigated through the use of this proposed NDPWM method, as can be seen from Figs. 3.10-3.12. Taking the comparison between the two modulation methods at 2 Hz as an example, the average junction temperatures of IGBTs S_{a1} and S_{a2} are 40.4℃ and 64.3℃, respectively, under the use of the SVPWM method, which become 55.4℃ and 55.5℃, respectively, under the use of the proposed DPWM method.

Based on all the analysis and simulation results above, a conclusion can be drawn that the NDPWM method can effectively increase the number of cycles to failure for the most stressed power devices of this NPC inverter, and the thermal distribution balancing among their power devices is further improved, which will in turn extend the reliability of the whole ASD systems.

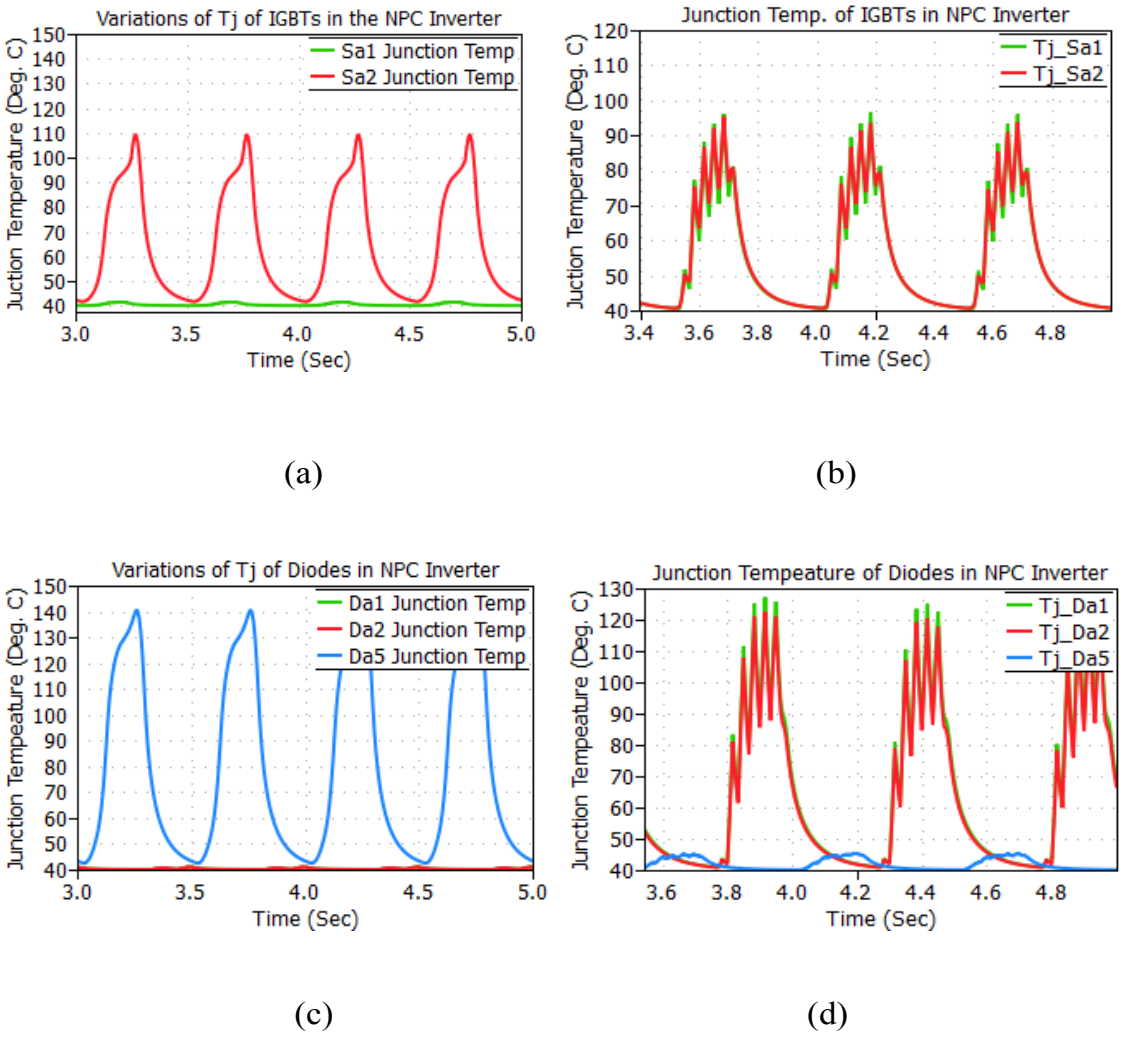


Figure 3.10: Comparison of the device junction temperature profiles between the conventional SVPWM method and the proposed NDPWM method at the output frequency of 2 Hz (a) T_j of IGBTs under SVPWM (b) T_j of IGBTs under the NDPWM (c) T_j of the free-wheeling diodes under the SVPWM (d) T_j of the free-wheeling diodes under the NDPWM.

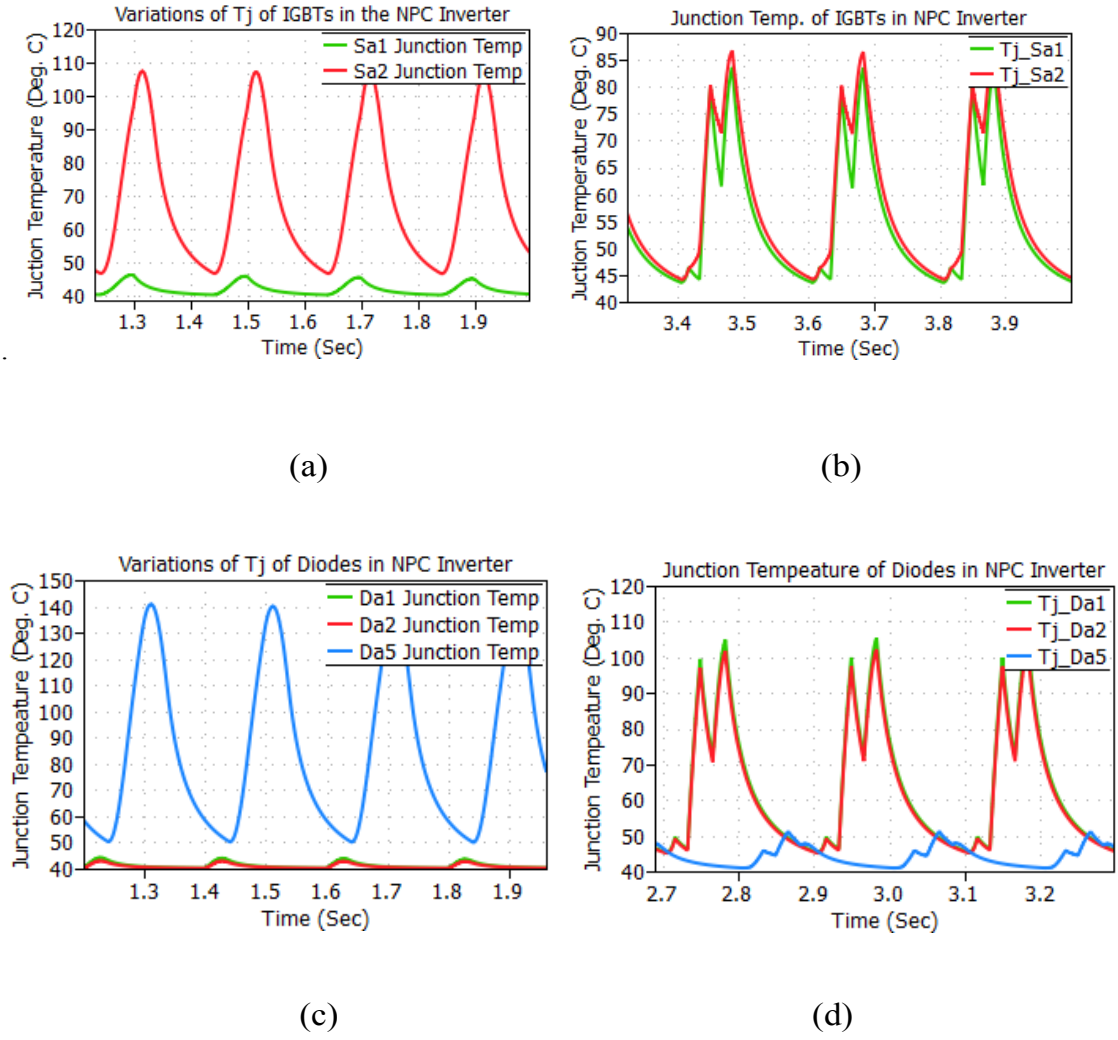


Figure 3.11: Comparison of the device junction temperature profiles between the conventional SVPWM method and the proposed NDPWM method at the output frequency of 5 Hz (a) T_j of IGBTs under SVPWM (b) T_j of IGBTs under the NDPWM (c) T_j of the free-wheeling diodes under the SVPWM (d) T_j of the free-wheeling diodes under the NDPWM.

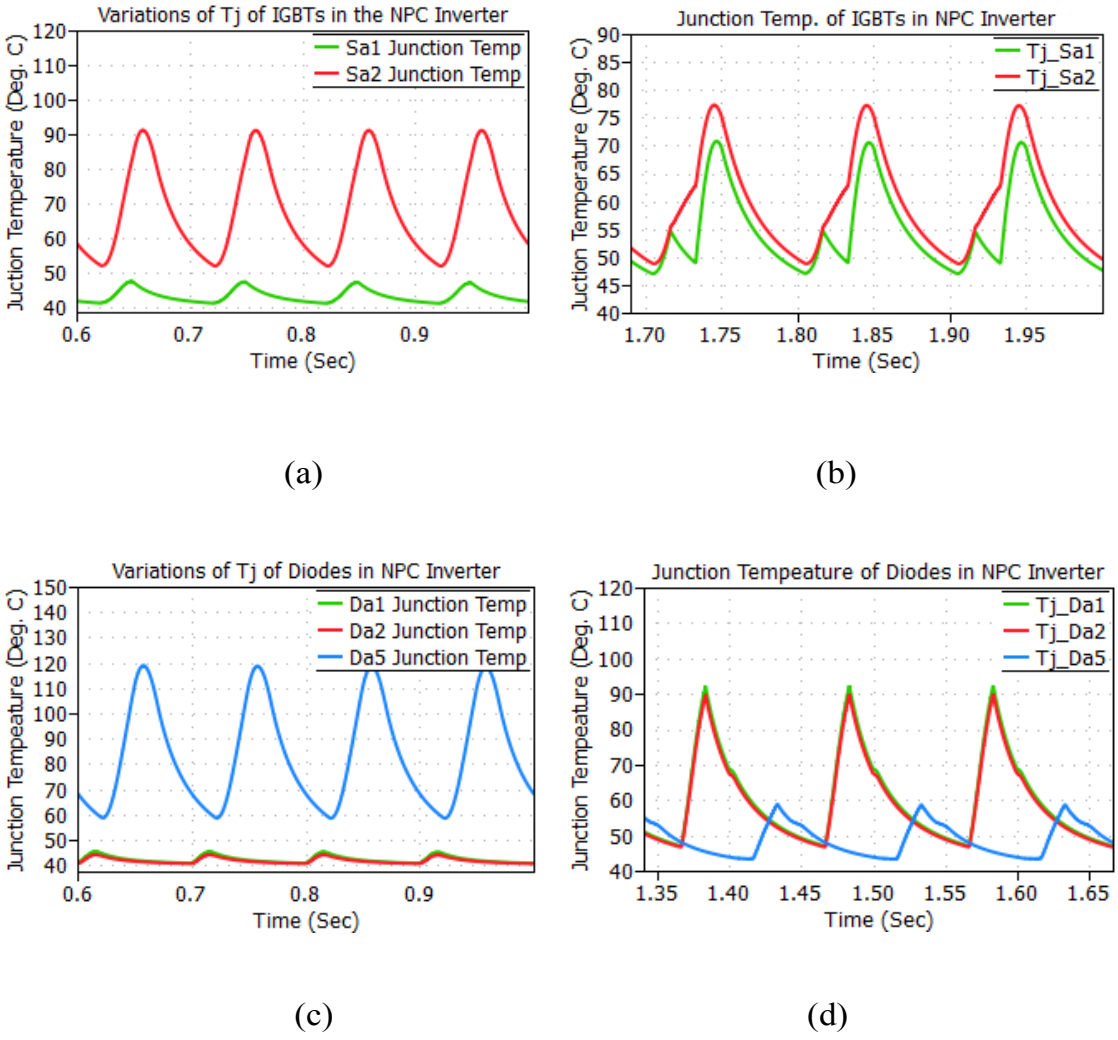


Figure 3.12: Comparison of the device junction temperature profiles between the conventional SVPWM method and the proposed NDPWM method at the output frequency of 10 Hz (a) T_j of IGBTs under SVPWM (b) T_j of IGBTs under the NDPWM (c) T_j of the free-wheeling diodes under the SVPWM (d) T_j of the free-wheeling diodes under the NDPWM.

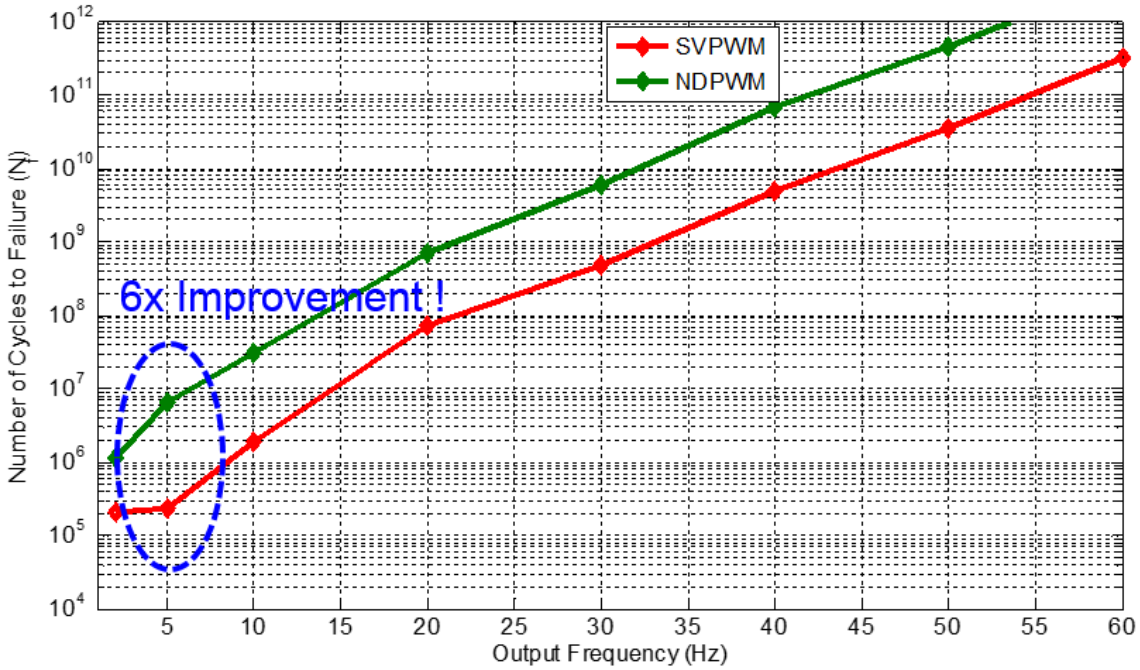


Figure 3.13: Comparison of the power cycling lifetime of the three-level NPC inverter between using the SVPWM and the proposed DPWM method.

3.6 Experimental Results

Experimental verifications have been carried out to evaluate the performance of this proposed PWM method, mainly including the harmonic distortion in the output voltages and currents, as well as the influence on the balancing of the dc-bus capacitor voltages of the NPC inverter. The necessity to investigate the balancing of dc-bus capacitor voltages is due to the fact that any unbalance between the upper dc-bus capacitor voltage and the lower dc-bus capacitor voltages in the NPC inverters will directly degrade the output current/voltage waveform quality and the lifetime of dc-bus capacitors. The mitigation of the IGBT junction temperatures cannot be directly measured, thus cannot be demonstrated here through experimental results. A 50-kVA NPC-inverter-based ASD prototype and a dynamometer setup are shown in the

photographs of Figs. 3.14 and 3.15, respectively. As is shown in Fig. 3.14, two three-phase 5-hp induction machines are utilized as the motor and generator, and an ABB adjustable speed drive, namely, ACS800, is used to apply torque to the inductor machine. Other parameters and circuit schematics of the NPC-inverter-based ASD prototype are given in the Appendices A.1 through A.3 of this dissertation.

Oscillograms of three-phase currents and voltages under normal operation with the SVPWM method are shown in Fig. 3.16, in which the satisfactory quality of the three-phase current and the staircase waveforms of the line-to-neutral voltages are demonstrated. By embedding the NDPWM method into the DSP microcontroller, three-phase currents and dc-bus capacitor voltages were captured at very low output frequencies of 2 Hz and 5 Hz and are shown in Fig. 3.17 and Fig. 3.18, respectively. To make a comparison with the conventional SVPWM method, three-phase load currents and dc-bus capacitor voltages were also captured under the SVPWM method at the same load conditions, which are shown in Fig. 3.19 and Fig. 3.20. It should be mentioned that all these experimental waveforms were captured without any LC filter connected at the output of the ASD system. It can be seen that the harmonic distortions in the output currents between using the NDPWM method and the SVPWM method are close to each other. At 2 Hz of output frequencies, the dc-bus balancing under the NDPWM method is slightly better than that under the SVPWM method. The maximum unbalance voltage between the upper and the lower dc-bus capacitors is around 50 V, which accounts for 7.7% of the rated dc-bus voltage of 650V. Such unbalance extent is negaligble in general industrial drive systems.

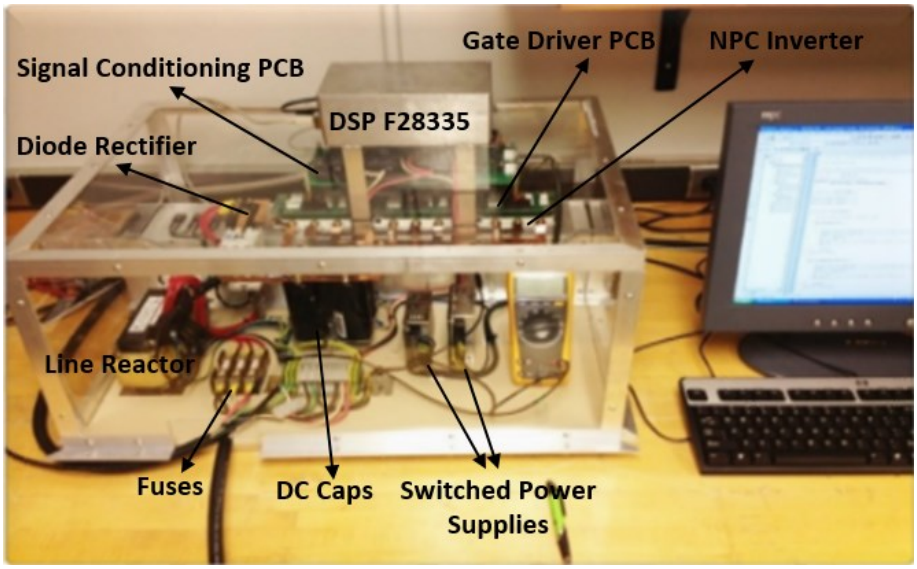


Figure 3.14: Customized 50-kVA ASD prototype based on a three-level NPC inverter used for the evaluation of this novel DPWM method.

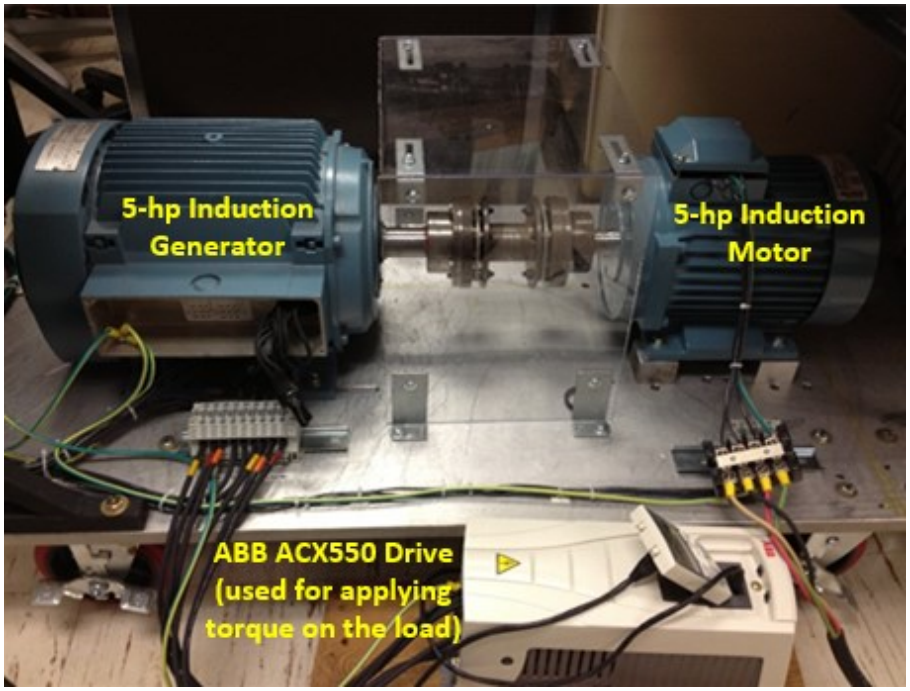
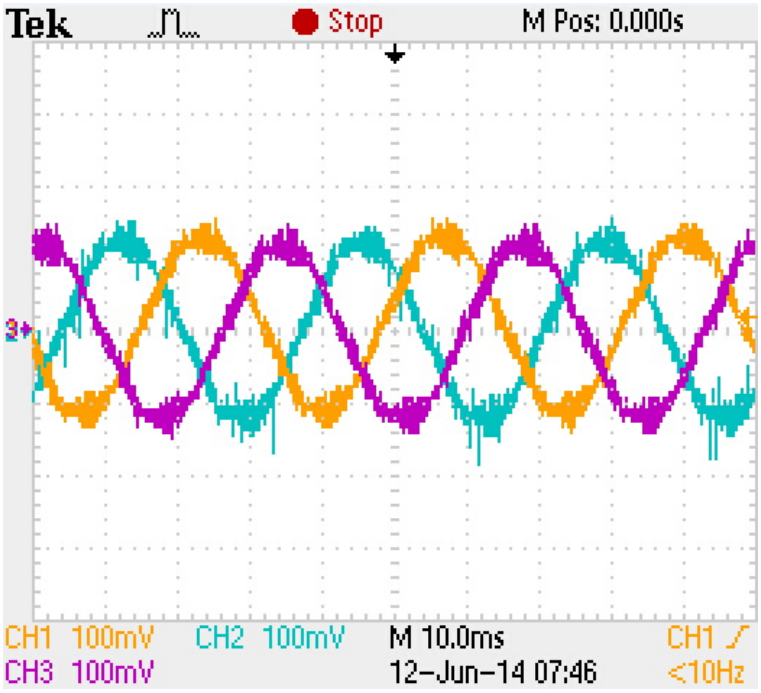
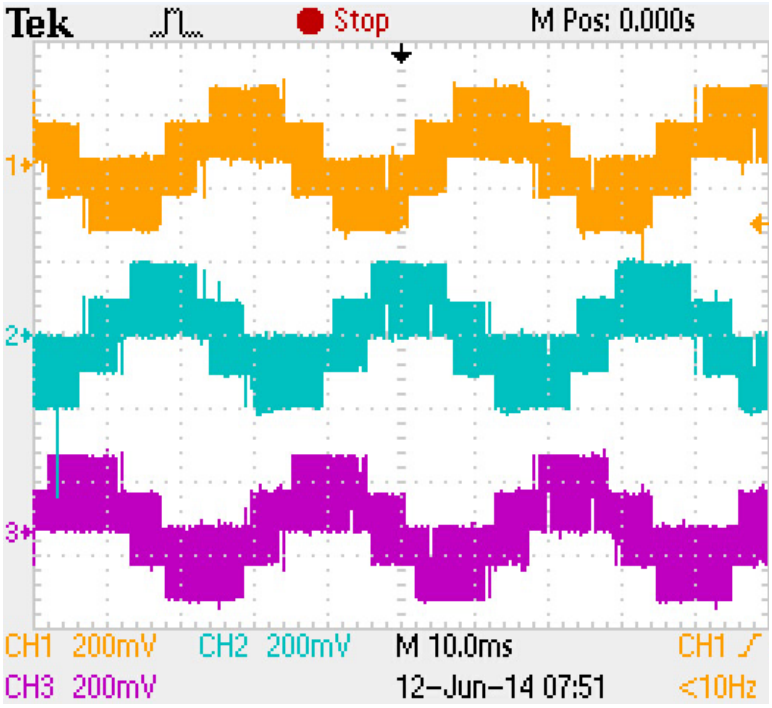


Figure 3.15: The dynamometer setup used in the experiments.

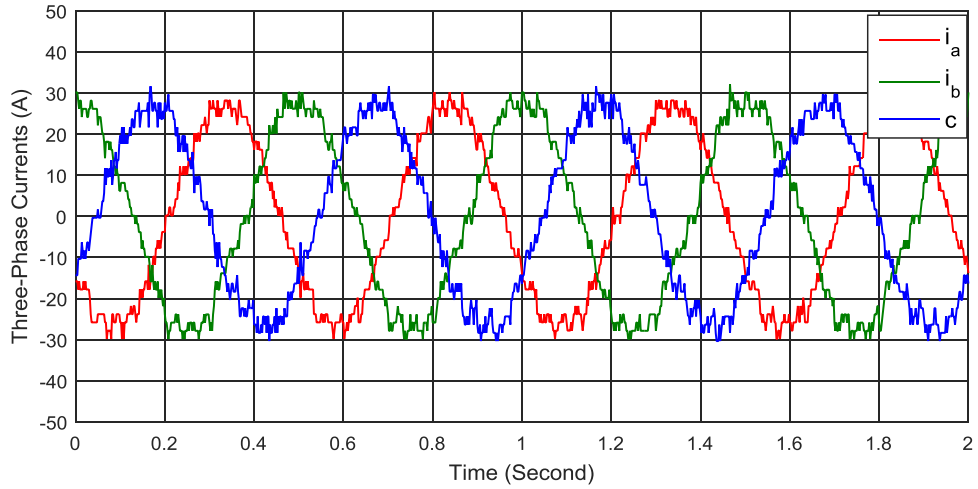


(a)

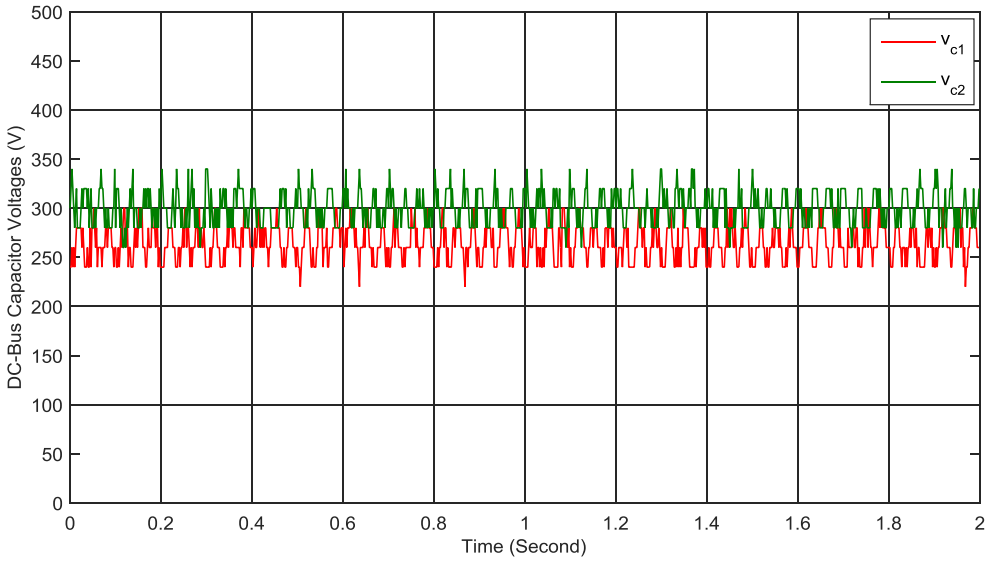


(b)

Figure 3.16: Measured phase currents and voltages from the custom-designed 50kVA ASD under healthy condition with the SVPWM method when driving a three-phase induction motor (a) measured three-phase currents (b) measured three-phase line-to-neutral voltages.

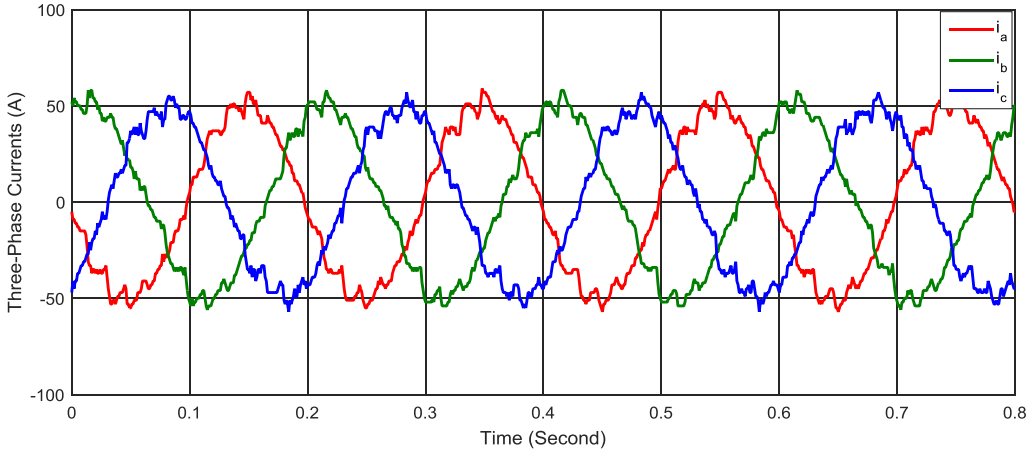


(a)

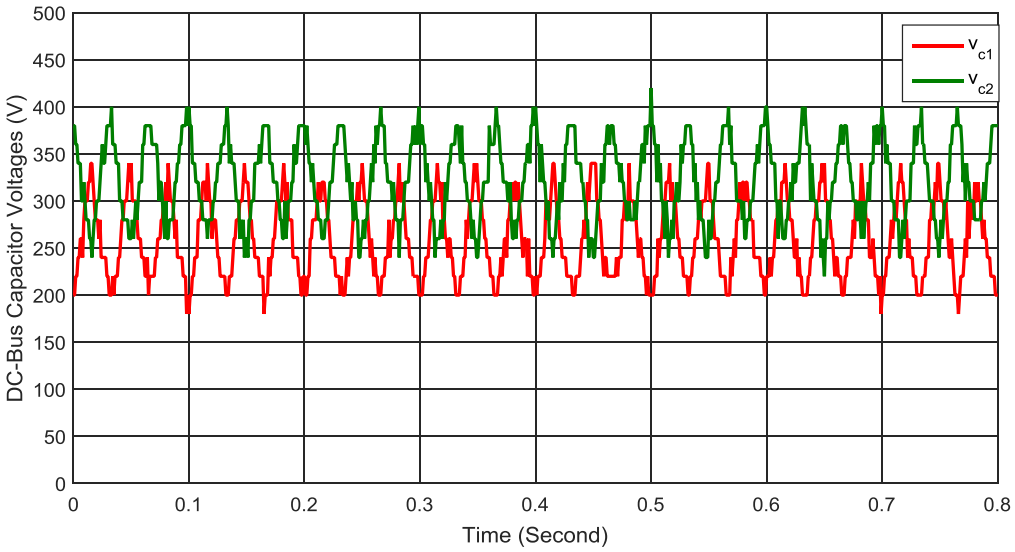


(b)

Figure 3.17: Measured three-phase currents and dc-bus capacitor voltages from the 50kVA ASD under the NDPWM method at 2 Hz of output frequencies (a) measured three-phase currents (b) measured dc-bus capacitor voltages.

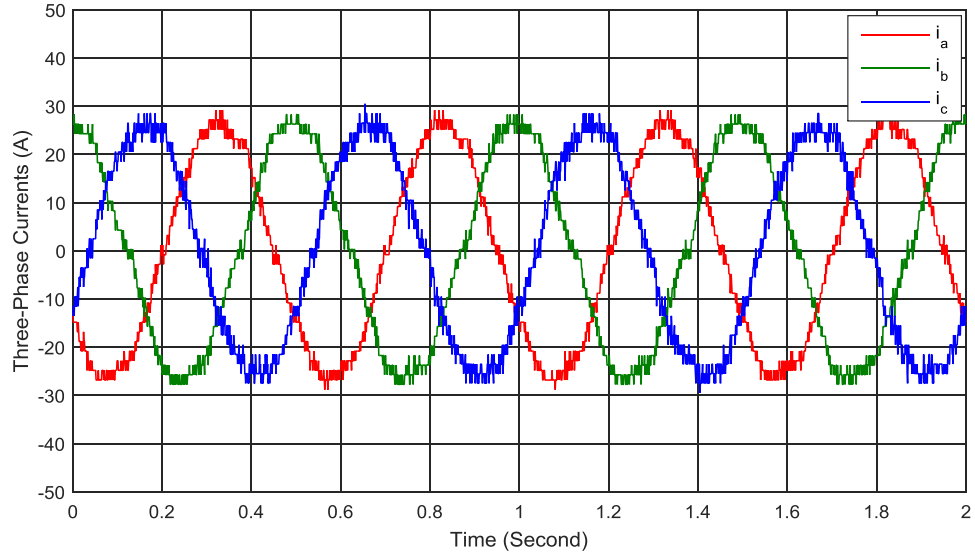


(a)

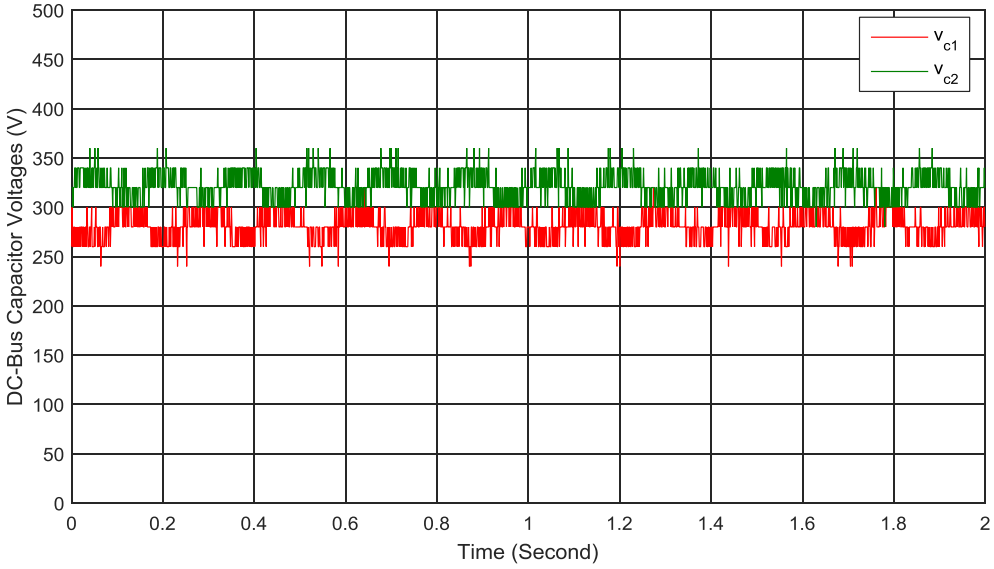


(b)

Figure 3.18: Measured three-phase currents and dc-bus capacitor voltages from the 50kVA ASD under the NDPWM method at 5 Hz of output frequencies (a) measured three-phase currents (b) measured dc-bus capacitor voltages.

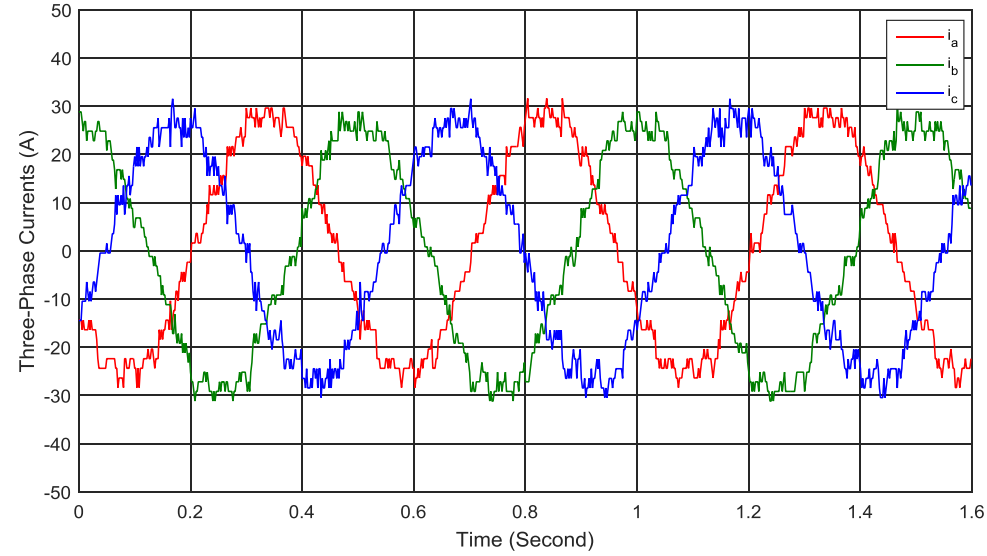


(a)

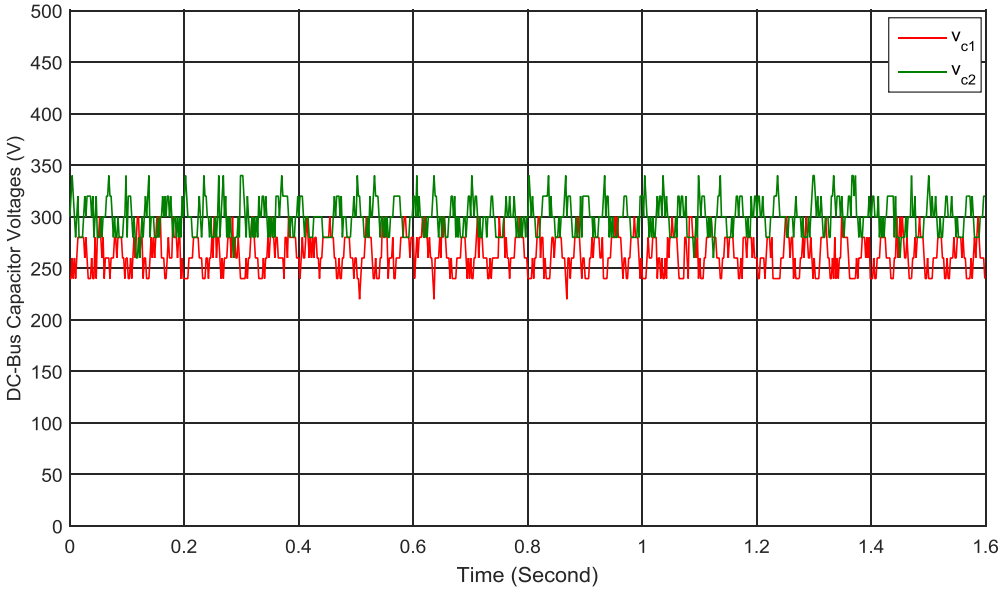


(b)

Figure 3.19: Measured three-phase currents and dc-bus capacitor voltages from the 50kVA ASD under the SVPWM method at 2 Hz of output frequencies (a) measured three-phase currents (b) measured dc-bus capacitor voltages.



(a)



(b)

Figure 3.20: Measured three-phase currents and dc-bus capacitor voltages from the 50kVA ASD under the SVPWM method at 5 Hz of output frequencies (a) measured three-phase currents (b) measured dc-bus capacitor voltages.

3.7 Summary

In this chapter, prediction of the remaining power cycling lifetime to failure of a power converter was reviewed. A novel DPWM method was introduced to extend the lifetime of a three-level NPC inverter during low-frequency operations. This proposed DPWM method indirectly reduces the time constant of the IGBTs' thermal impedance based on injecting a zero-sequence signal with higher fundamental frequency into the reference signals of the DPWM. In addition, the thermal distribution (i.e., junction temperatures) among all the power devices in the NPC inverter was found to be better balanced, and correspondingly the lifetime of the NPC inverter would be accordingly extended. Simulation results obtained from thermal modeling in the PLECS simulation software have verified the effectiveness of this DPWM method. Experimental results demonstrate that the harmonic distortions in the output voltages and currents as well as the balance of the dc-bus capacitor voltages meet the requirements if using this NDPWM modulation method.

CHAPTER 4

ON-LINE DIAGNOSIS OF IGBT FAULTS IN NPC INVERTERS

4.1 Introduction

Safety and reliability have been two important factors in evaluating the competiveness of ASDs in the market place, especially regarding their use in safety-critical applications such as machine tools, vehicular power train systems, medical instruments, and so forth. With the increase of power capacities and the decrease of price of semiconductor devices, multilevel converters have been increasingly applied in ASDs, especially for high-power (above 0.75 MVA) or medium-voltage (2.3-13.8kV) applications [79]. One concern raised by the utilization of multilevel converters is the potentially degraded reliability due to the use of large number of switching devices and the associated gate driver circuits in such ASDs. Thus, there is a need to more frequently detect and diagnose common electrical faults, such as device short-circuit faults and open-circuit faults, in multilevel-converter-based ASDs. Solutions to detect short-circuit faults in the switching devices in power electronic systems have received much attention over the past decades [46-51]. However, open-circuit fault detection in switching devices has not received adequate attention. As a matter of fact, open-circuit faults in power converters can be encountered more often in some applications where the ASDs are operating for prolonged periods at low output frequencies and heavy loads, such as in elevators, EVs or HEVs, and the like. In such low-frequency and heavy-load operating modes, generally there will be high fluctuations of junction

temperatures in switching devices, as was discussed in Section 3.2 of Chapter 3. Such phenomena will cause open-circuit faults due to "bond wire lift-off" or "solder joint cracking" in such switching devices, as reported in [5-7]. Therefore, the need for an efficient, low-cost diagnostic method for detecting open-circuit faults in power converters is of high necessity and significance.

In this Chapter, a novel diagnostic method will be introduced for detecting IGBT open-circuit faults in an NPC inverter. This method is based on monitoring the variations of dc-bus neutral point current in combination with the switching patterns and phase current information that are generally available in ASDs. Before introducing this novel diagnostic method, open-circuit IGBT faults in an NPC inverter and their corresponding negative impacts on the output currents and voltage balancing of the dc-link capacitors are analyzed, which is followed by the introduction of the principle of the proposed diagnostic method for detecting IGBT open-circuit faults in NPC inverters. Finally, simulation and experimental results based on a lab-scale 50-kVA NPC inverter-based ASD experimental setup will be given to verify the validity of this proposed diagnostic method.

4.2 Negative Impacts of Switch Faults

The topology of the NPC inverter is given in Fig. 2.16 in Chapter 2. The working principle of the NPC inverter is detailed in [80], and therefore will not be repeated in this dissertation. The switching state vectors of the NPC inverter are given in Fig. 4.1, in which the output voltage of each phase leg is designated as "P", "O", and "N," to represent positive ($V_{dc}/2$), zero, or negative ($-V_{dc}/2$) output pole voltages. For example, the switching state, (P, O, N), in Section 1 of Fig. 1(b),

implies that the output pole voltages of Phase-A, Phase-B, and Phase-C are ($+V_{dc}/2$), 0, and ($-V_{dc}/2$), respectively. The definitions of such designations for each switching state of the NPC inverter will be very convenient for the analysis of the negative effects of IGBT open-circuit faults.

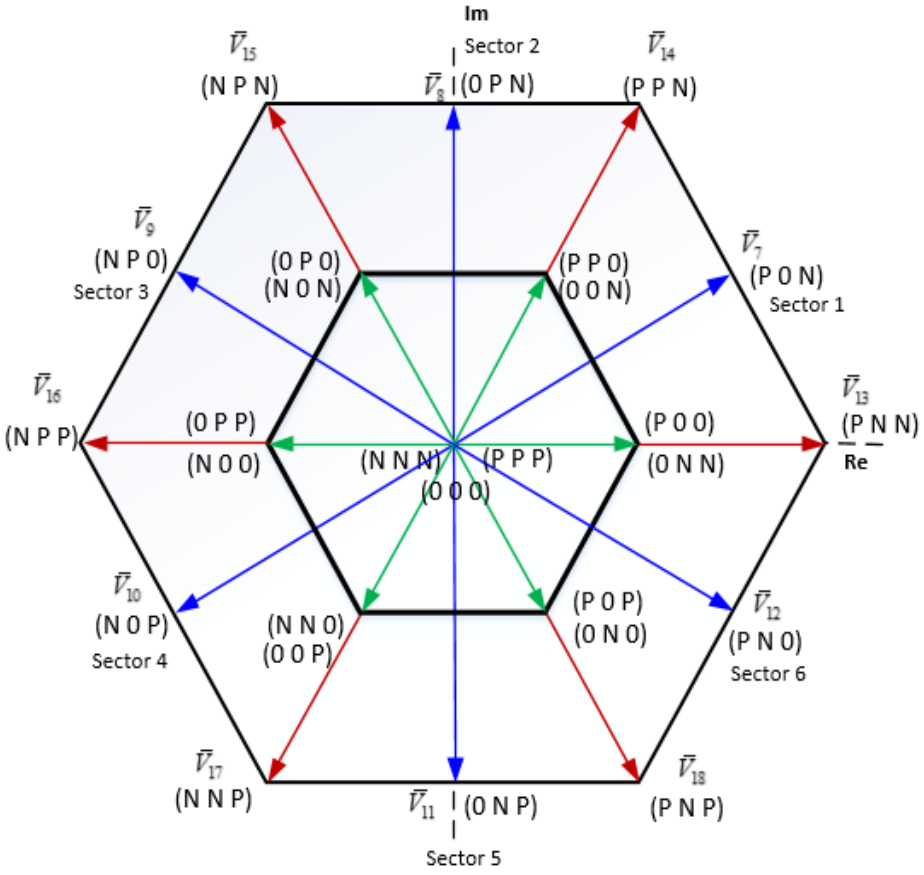
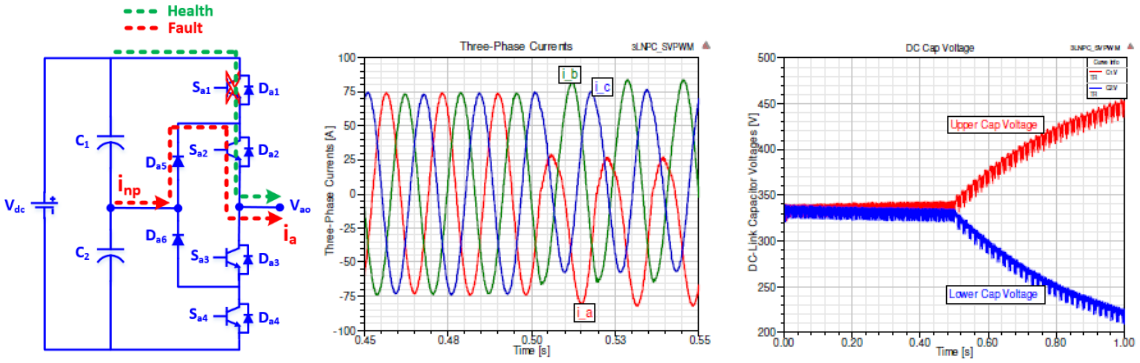


Figure 4.1: Switching state vectors of NPC inverters (small voltage vectors in green, medium voltage vectors in blue, and large voltage vectors in red).

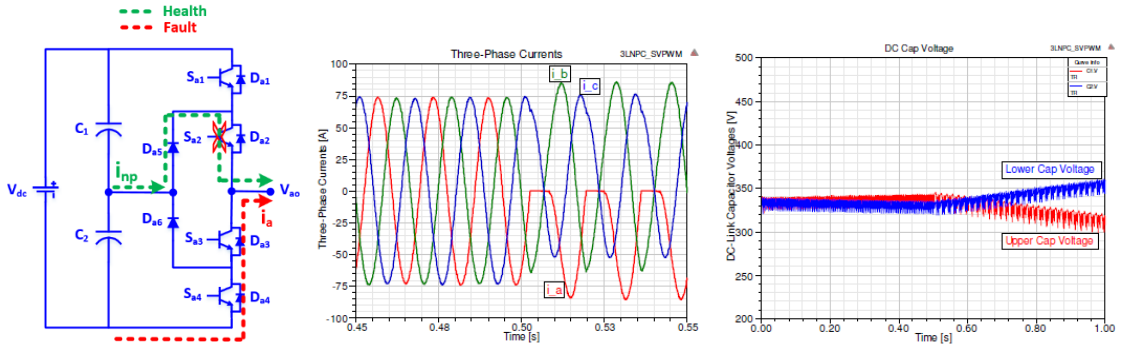
Considering the symmetrical topology of the NPC inverter, only the open-circuit faults in IGBTs S_{a1} and S_{a2} in Phase-A are analyzed here. As shown in Fig. 4.2 (a), when IGBT S_{a1} encounters an open-circuit fault, the output terminal cannot be connected to the positive dc-bus during the "P" state, when the Phase-A current, i_a, is positive (current flowing from the dc source to the load), as shown in the

green current path in Fig. 4.2(a). Instead, the output terminal of Phase-A leg will be connected to the dc-bus neutral point through the clamping diode D_{a2} and inner switch IGBT S_{a2}, as shown in the red current path of Fig. 4.2(a). As a result, there will be a large negative dc component in the Phase-A current, i_a, as shown in Fig. 4.2 (b). Additionally, it can be seen that the upper dc-link capacitor will be more charged than the lower capacitor due to the open-circuit fault in IGBT S_{a1}, which will results in a much larger voltage in the upper capacitor C_1 than that in the lower capacitor C_2, as shown in Fig. 4.2(c). Similarly, when the IGBT S_{a2} in Phase-A leg has an open-circuit fault, the output terminal will not be connected to the dc-link neutral point during the "N" state if the phase-A current is positive, as depicted in the green path shown in Fig. 4.3 (a). Instead, the output terminal will be connected to the negative dc-link through the freewheeling diodes D_{a3} and D_{a4}, as shown in the red current path in Fig. 4.3 (a). Since the open-circuit fault in S_{a2} interrupts all the current paths in Phase-A flowing from source to the load, the Phase-A current will consist of negative half cycles, as shown in Fig. 4.3 (b). Moreover, the lower dc-link capacitor C_2 will be more charged than the upper capacitor C_1, which results in a higher capacitor voltage in C_2 than that in C_1. If no measures are taken to balance the dc-link voltages, then C_2 may fail because of the potential overheating caused by the large voltage. In summary, IGBT open-circuit faults in NPC inverters can severely degrade the performance of the related ASDs and may cause cascaded failures in the dc-link capacitors. Therefore, an effective on-line diagnostic method is of great necessity for enhancing the system reliability in such ASDs.



(a) (b) (c)

Figure 4.2: Current path, variations of phase currents and dc-bus capacitor voltages under health and open-circuit faulty condition of IGBT S_{a1} when $i_a>0$ (the open-circuit fault is triggered at t=0.5 second) (a) current paths (b) variation of three-phase currents.



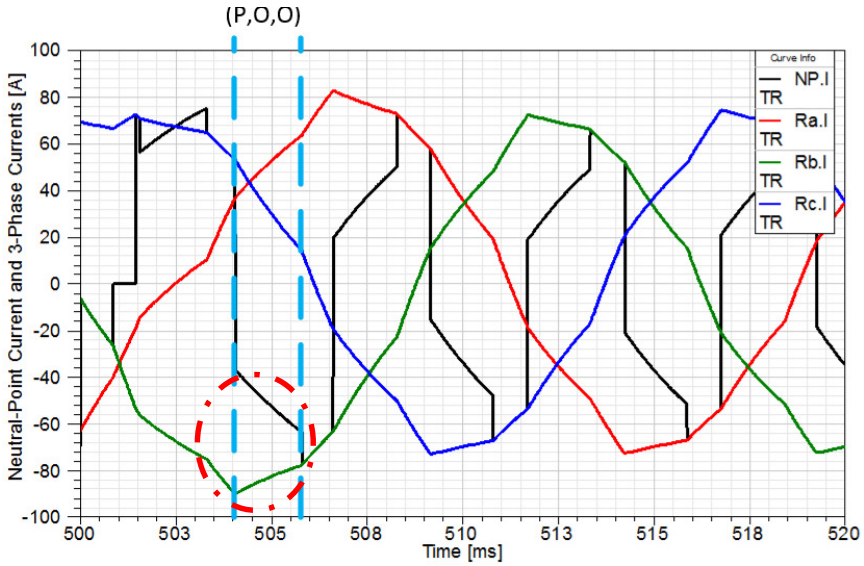
(a) (b) (c)

Figure 4.3: Current path, variations of phase currents and dc-bus capacitor voltages under health and open-circuit faulty condition of IGBT S_{a4} when $i_a>0$ (the open-circuit fault is triggered at t=0.5 second) (a) current paths (b) variation of three-phase currents.

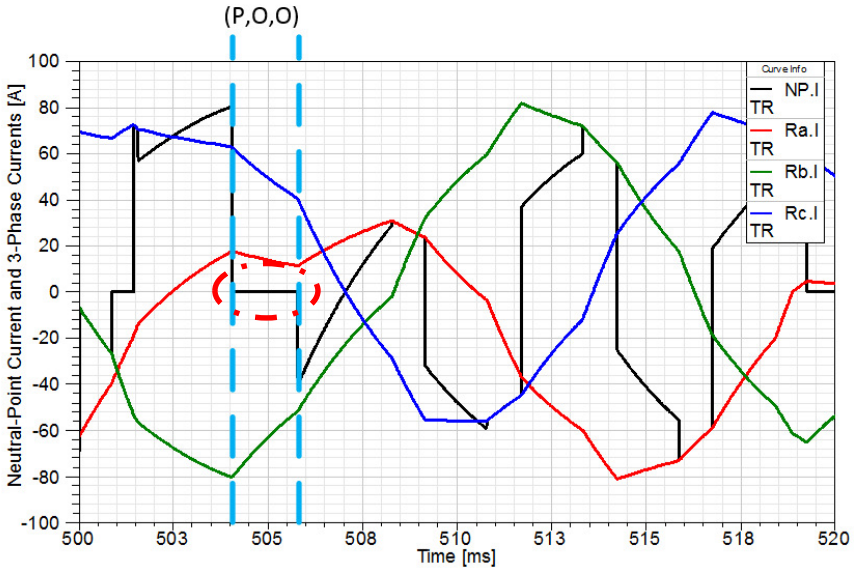
4.3 The Proposed On-Line Diagnostic Method

An ideal fault diagnostic method should be accurate, robust, and low-cost. To be specific, for the diagnosis of switch faults in multilevel converters, an optimal fault diagnostic method is supposed to have accurate detection, short

microcontroller execution time, easy implementation, as well as the need for minimum number of additional sensors to limit the cost increase. The diagnostic method to be introduced in this Chapter is based on monitoring the dc-bus neutral-point current, i_{np}, of the NPC inverter. This is because such information on this current, in combination with the switching states, and phase currents, can indicate the health condition all the IGBTs. In other words, if the information on the instantaneous switching states and phase currents is known to the system microcontroller, a faulty IGBT in an NPC inverter can be identified by comparing the actual value of the neutral-point current under a faulty condition to the supposed value at otherwise healthy condition. For instance, when the IGBT S_{a1} in Phase-A, see Fig. 4.3 (a), experiences an open-circuit fault, it follows that such a fault can be identified at the switching state of (P, O, O) by comparing the average value of i_{np} with zero, as depicted in Figs. 4.4 (a) and (b). If the average value of i_{np} during the state (P, O, O) is zero, as shown in Fig. 4.4 (b), it follows that an open-circuit fault in S_{a1} can be diagnosed and logically assumed to have occurred, because the open-circuit fault in S_{a1} will cause the switching state (P, O, O) to operate as (O, O, O), see the current path which is shown in Fig. 4.2 (a), in which the neutral-point current, i_{np}, will be ideally zero. However, in practice, a proper hysteresis band around zero should be considered in the diagnostic algorithm due to the undesired resulting common-mode voltages occurring during the switching. Similarly, faults in other IGBTs of the NPC inverter can also be detected and identified by using the same logic methodology. The diagnostic strategies for diagnosing all the other IGBT faults in an NPC inverter are listed in Table 4.1. A functional flow chart of this proposed diagnostic method is given in Fig. 4.5, in



(a)



(b)

Figure 4.4: Neutral-point current and three-phase currents of the NPC inverter under healthy and faulty conditions (a) healthy condition (b) faulty condition.

which it can be seen that the information on the neutral-point current, i_{np}, instantaneous switching states, as well as the polarities of the three phase currents, i_a, i_b, and i_c, are the inputs to the diagnostic algorithm, and the output will be the

flag signal on the identified faulty switch. Simulation and experimental results which will be given in the following sections can further illustrate the operating principle of this novel diagnostic method.

Here, it should be mentioned that this proposed diagnostic method only requires one addition current sensor to measure the dc-link neutral-point current, i_{np}. Thus, this implies very slight cost increase is necessary, if one is to implement this method in commercial multilevel ASDs or power electronic systems. In this diagnostic method, the required information on the switching states and polarities of the load currents of such an NPC inverter is generally available in the system microcontroller of these inverters. Therefore, no additional hardware components are required.

Table 4.1: Diagnostic look-up table for IGBT faults in the NPC inverters.

IGBT	**Switching States**	**Diagnostic Index**
S_{a1}	(P, O, O)	If $i_{np} = 0$, then S_{a1} is "Open"
S_{a2}	(O, P, N), (O, N, P) (O, N, N), (O, P, P)	If $i_{np} = 0$, then S_{a2} is "Open"
S_{a3}	(O, P, N), (O, N, P) (O, N, N), (O, P, P)	If $i_{np} = 0$, then S_{a3} is "Open"
S_{a4}	(N, O, O)	If $i_{np} = 0$, then S_{a4} is "Open"
S_{b1}	(O, P, O)	If $i_{np} = 0$, then S_{b1} is "Open"
S_{b2}	(P, O, N), (N, O, P) (N, O, N), (P, O, P)	If $i_{np} = 0$, then S_{b2} is "Open"
S_{b3}	(P, O, N), (N, O, P) (N, O, N), (P, O, P)	If $i_{np} = 0$, then S_{b3} is "Open"
S_{b4}	(O, N, O)	If $i_{np} = 0$, then S_{b4} is "Open"
S_{c1}	(O, O, P)	If $i_{np} = 0$, then S_{c1} is "Open"
S_{c2}	(P, N, O), (N, P, O) (N, N, O), (P, O, P)	If $i_{np} = 0$, then S_{c2} is "Open"
S_{c3}	(P, N, O), (N, P, O) (N, N, O), (P, O, P)	If $i_{np} = 0$, then S_{c3} is "Open"
S_{c4}	(O, O, N)	If $i_{np} = 0$, then S_{c4} is "Open"

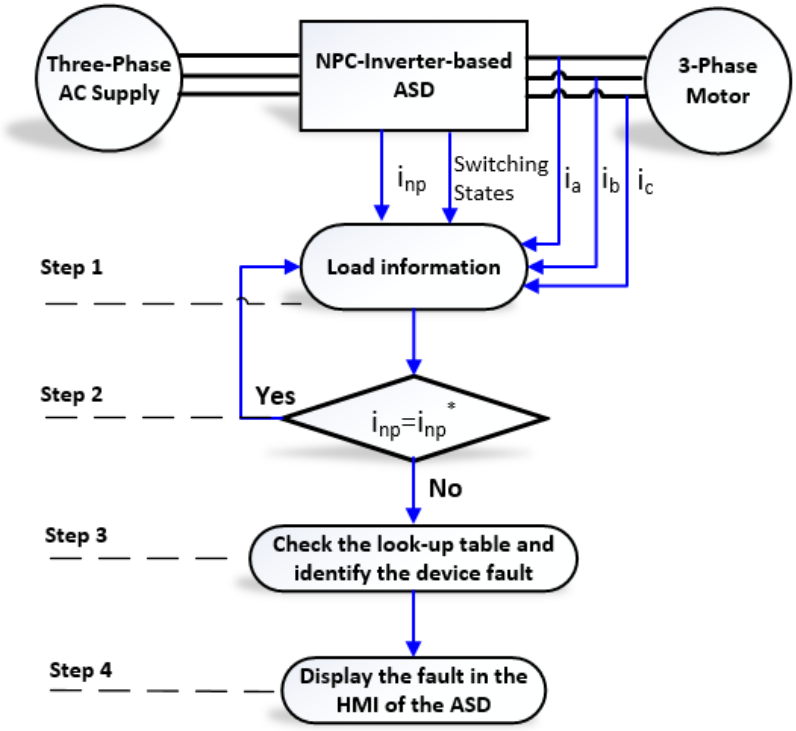


Figure 4.5: Flow chart of the proposed diagnostic method for IGBT faults in the NPC inverters.

4.4 Simulation Results

To verify the efficacy of the proposed diagnostic method, simulations of an ASD based on a three-level NPC inverter have been carried out in ANSYS Simplorer simulation software environment. The parameters of the ASD used in the simulation are listed in Table 4.2. As introduced in Section 4.3 of this chapter, the fault signatures under investigation here are the variations of the dc-bus neutral-point current under certain switching states of the NPC inverter. To graphically illustrate the fault signatures under various switching states, carrier-based Phase Disposition PWM (PD-PWM) method was adopted to modulate the three-level NPC inverter. As is well known, the definition of various switching states for a three-level NPC inverter is based on the caparison of the amplitudes of

the triangular carrier signals and the sinusoidal reference signals, which is detailed in Table 4.3.

Table 4.2: Main parameters of an NPC-inverter-based ASD used in the simulation analysis.

Control mode PWM method	Scalar control (V/Hz) PD-PWM		
Input	Line-to-line voltage	480	V_{RMS}, three phase
	Frequency	60	Hz
	Switching frequency	1	kHz
	DC bus voltage	650	V_{dc}, max
Load	Resistor	0.8	Ω
	Inductor	6	mH
	Output frequency	60	Hz

Table 4.3: Definition of switching states for a three-level NPC inverter modulated by the PD-PWM method.

Switching State of One Inverter Phase	**Definition**
Positive voltage "P"	When the magnitude of the positive portion of the sinusoidal reference signal is larger than the magnitude of the upper carrier triangular signal.
Negative voltage "N"	When the magnitude of the negative portion of the sinusoidal reference signal is larger than the magnitude of the lower carrier triangular signal.
Zero voltage "O"	For all the other cases.

First, an open-circuit fault in IGBT, S_{a1}, was simulated and investigated. As is shown in Fig. 4.6, during the switching state (P, O, O), the dc-bus neutral-point current, i_{np}, represented by the black rectangular trace, increases in magnitude

from $-7A$ to $-20A$, which drops to zero when the IGBT, $S_{a1,}$ has an open-circuit fault, as shown in Fig. 4.7. As explained earlier in this Chapter, such a variation results from the fact that the switching state (P, O, O) is forced to become (O, O, O) under the open-circuit faulty condition of IGBT S_{a1}, and the value of i_{np} at the switching state of (O, O, O) is zero due to the zero voltage potential for each phase output of the NPC inverter. Through monitoring the value of i_{np}, the open-circuit fault in the IGBT S_{a1} can be promptly and accurately diagnosed.

Similarly, another type of fault in the NPC inverter, namely, an open-circuit fault in the IGBT, S_{a2}, was simulated and examined. At the switching state of (O, N, N), the dc-bus neutral-point current, i_{np}, again represented by the black rectangular trace, is a positive current under healthy condition as shown in Fig. 3.8, which decreases to zero under the condition of an open-circuit fault in this IGBT, as shown in Fig. 4.9. Such dramatic change in the dc-bus neutral-point current derives from the fact that the switching state (O, N, N) becomes (N, N, N) under the open-circuit faulty condition of this IGBT, S_{a2}. It should be noted that, the variations of the neutral-point current under three other switching states, namely, (O, P, P), (O, N, P), and (O, P, N), can also be used to identify the open-circuit fault in S_{a2}. The nature of these fault signatures is very similar to the fault signature discussed above, and thus will not be repeated here.

From all these simulation results, it can be concluded that the open-circuit switch faults in a three-level NPC inverter can be effectively diagnosed by monitoring the dc-bus neutral-point current under certain switching states. The experimental results given in the following section will further confirm such efficacy of this diagnostic method.

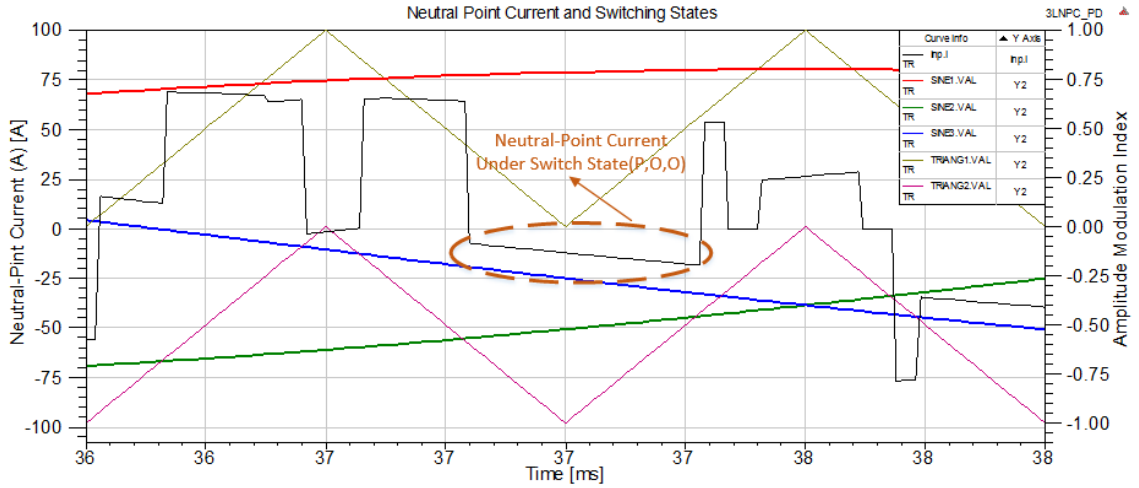


Figure 4.6: Fault signature (i.e., variation of the neutral-point current at the switching state (P, O, O), circled in yellow dashed line) under healthy condition of the three-level NPC inverter.

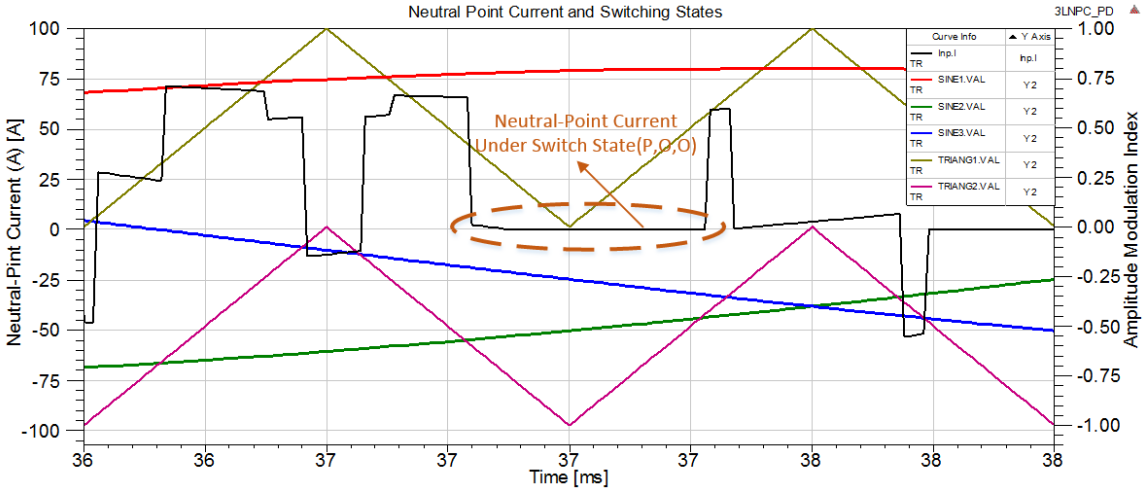


Figure 4.7: Fault signature (i.e., the abnormal variation of the neutral-point current at the switching state (P, O, O), circled in yellow dashed line) under open-circuit faulty condition in switch S_{a1} of the NPC inverter.

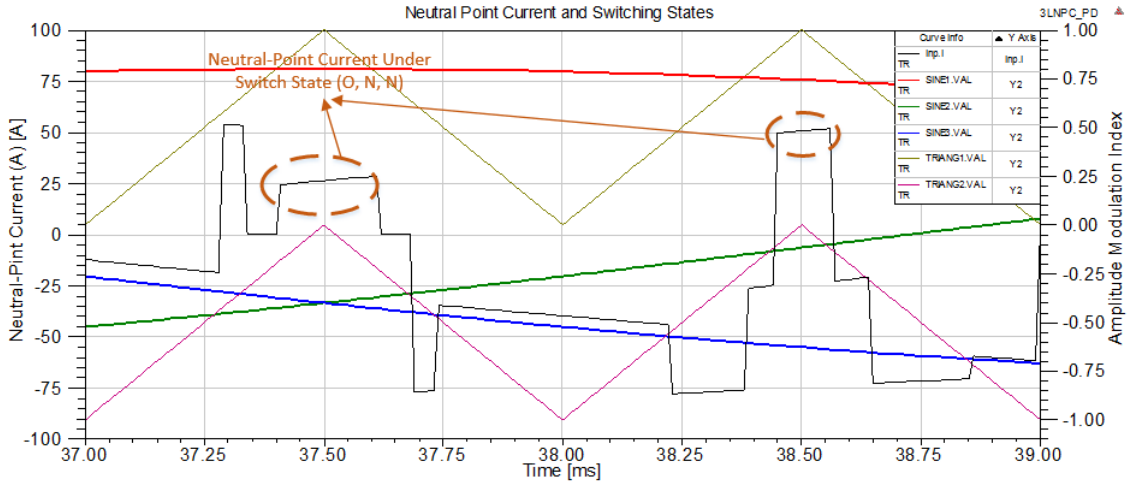


Figure 4.8: Fault signature (i.e., the variation of the neutral-point current at the switching state (O, N, N), circled in yellow dashed line) under healthy condition of the three-level NPC inverter.

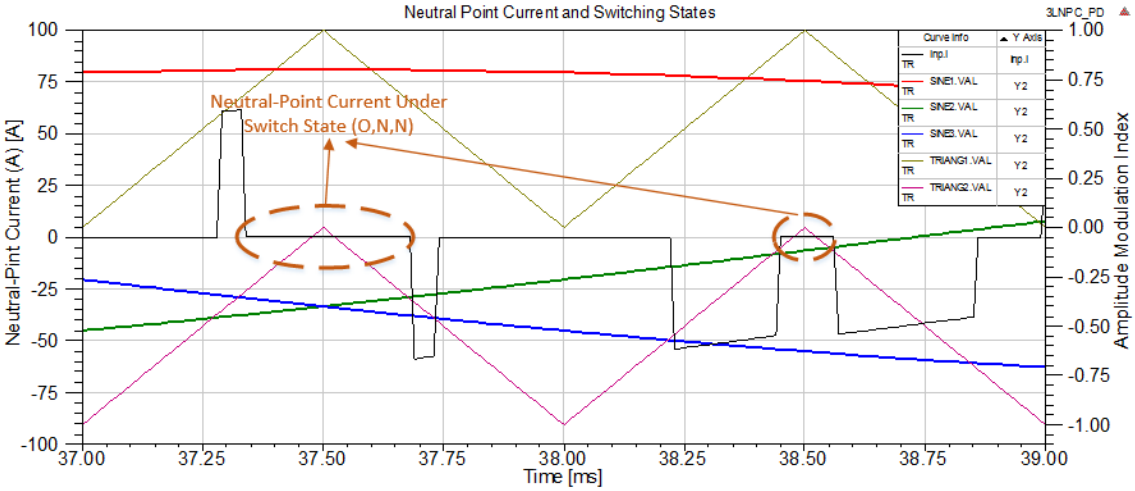


Figure 4.9: Fault signature (i.e., the abnormal variation of the neutral-point current at the switching state (O, N, N), circled in yellow dashed line) under open-circuit faulty condition in switch S_{a2} of the NPC inverter.

4.5 Experimental Results

Regarding the experimental verifications of this proposed fault diagnostic method discussed above, the same experimental setup, namely, the 50-kVA customized ASD system, introduced in Section 3.6 of Chapter 3 will be used here. The open-circuit faults in the IGBTs of the NPC inverter were emulated by disabling the related PWM signals. For instance, when the PWM signal for IGBT, S_{a1}, is disabled, as shown in the oscillogram of Fig. 4.10, this IGBT will be kept in an open state, which exhibits the same phenomenon as an open-circuit fault occurring in such a device. The fault signatures, namely, the variations of the dc-bus neutral point current, i_{np}, at certain switching states, were investigated when an open-circuit fault occurred in one of the IGBT devices in the NPC inverter. Here, to be consistent with the simulation results shown in Section 4.4, only the open-circuit faults in IGBTs, S_{a1} and S_{a2}, were investigated, and the open-circuit faults in other switching devices are very similar to these two types of faults due to the symmetries of the inverter circuit topology. To provide baseline results for the comparison of phase currents and dc-bus neutral-point currents, the measured three-phase currents and the dc-bus neutral-point current under healthy conditions are shown in Fig. 4.11 through Fig. 4.12, respectively. Meanwhile, these results under faulty condition, i.e., an open-circuit switch fault occurring in the IGBT S_{a1}(see the circuit schematic in Fig. 2.16), are shown in Fig. 4.13 and Fig. 4.14. As can be seen in Fig. 4.13, when an open-circuit fault occurred in the IGBT, S_{a1}, of the NPC inverter, there will be a loss of most of the positive current in Phase-A, which is due to the lack of access to the positive dc-bus for positive load current.

Accordingly, the distorted dc-bus neutral-point current, under the condition of an open-circuit fault occurring in the IGBT, S_{a1}, is shown in Fig. 4.14. By comparing Fig. 4.12 and Fig. 4.14, one can find that the neutral-point current in Fig. 4.14 has an abnormal profile during the state of positive current output from the Phase-A leg, which leads to the fault signatures examined next.

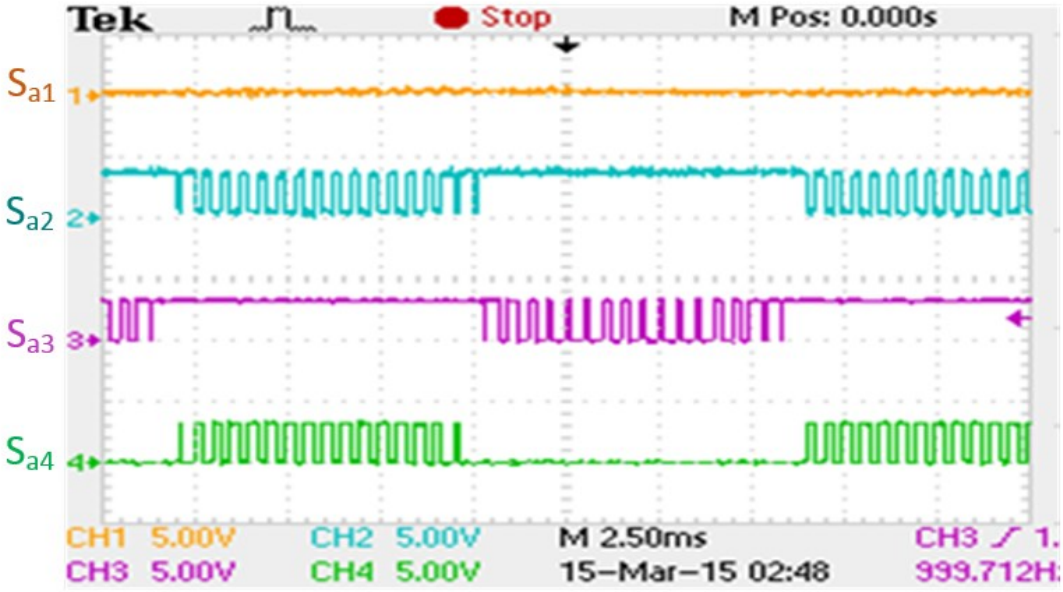


Figure 4.10: Measured PWM signals for the Phase-A leg of the three-phase three-level NPC inverter.

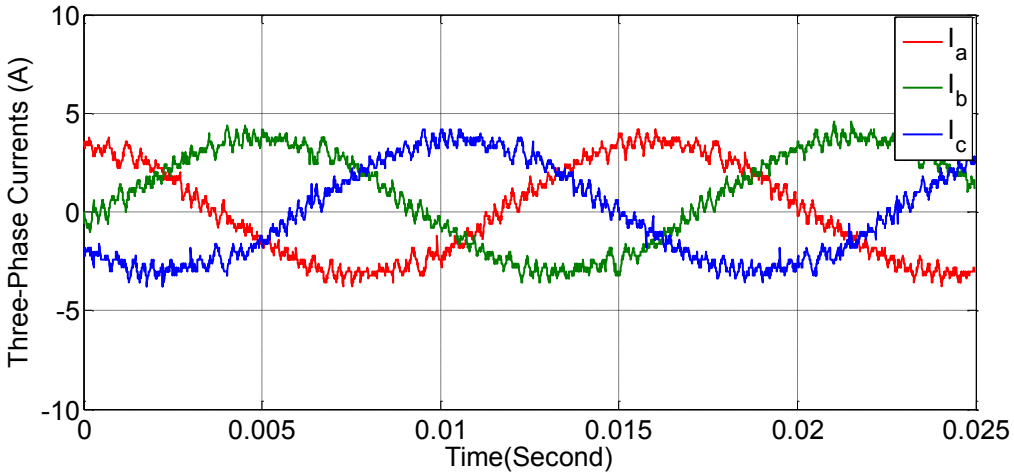


Figure 4.11: Measured three-phase load currents under healthy condition of the NPC inverter.

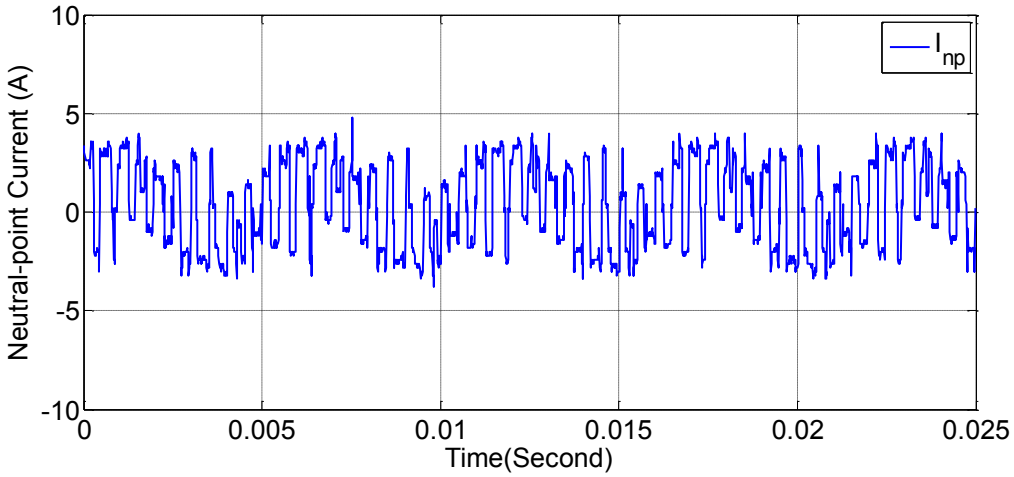


Figure 4.12: Measured dc-bus neutral-point current under healthy condition of the NPC inverter.

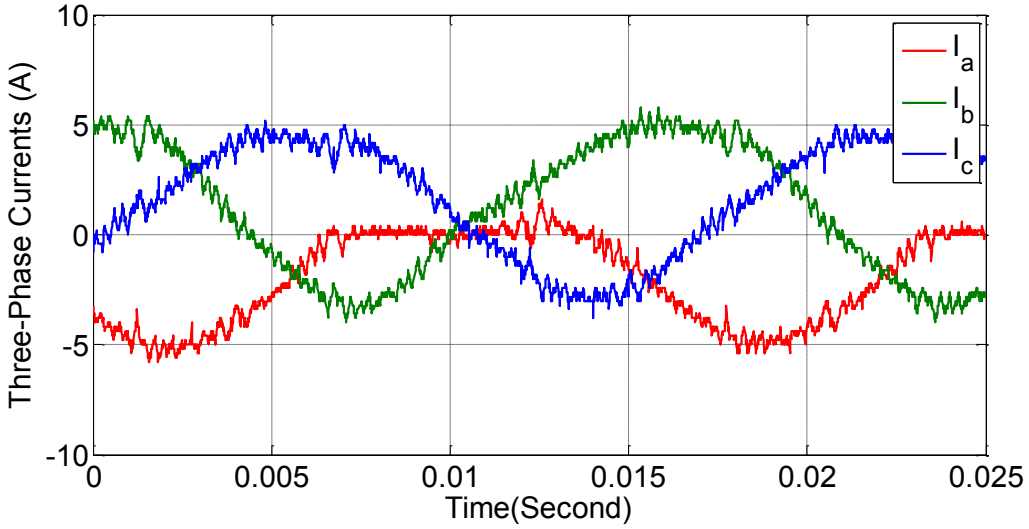


Figure 4.13: Measured three-phase load currents when an open-circuit switch fault occurred in the IGBT S_{a1} of the NPC inverter.

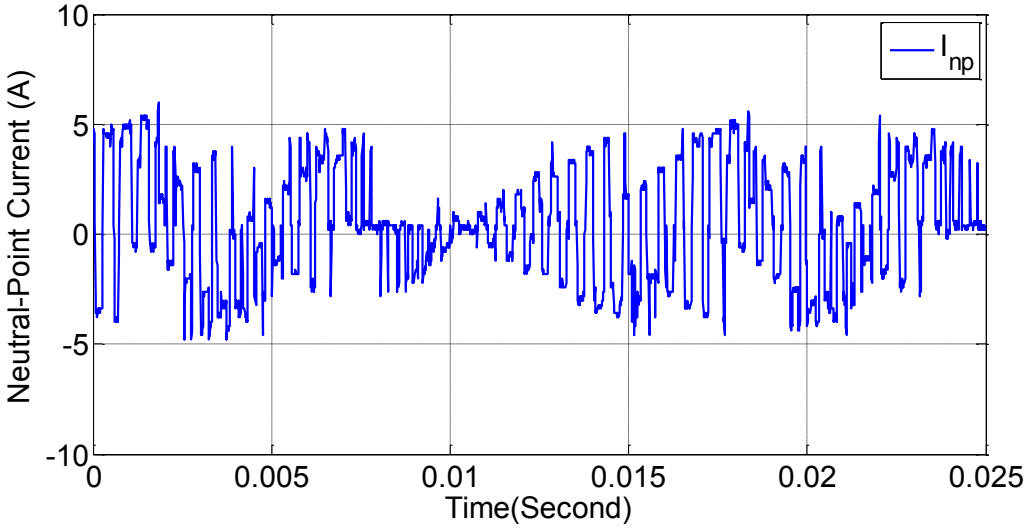


Figure 4.14: Measured dc-bus neutral-point current when an open-circuit switch fault occurred in the IGBT S_{a1} of the NPC inverter.

As is shown in Fig. 4.15, the measured dc-bus neutral-point current is around -3A at the switching state of (P, O, O), which decreases to almost zero at the same switching state when an open-circuit fault happens in the IGBT, S_{a1}, as shown in Fig. 4.16. As mentioned in the previous sections in this chapter, such abnormal variation is due to the fact that the original positive switching state, “P”,

of the Phase-A leg is forced to turn into a zero switching state, "O", when an open-circuit fault occurs in the IGBT, S_{a2}. Obviously, the dc-bus neutral-point current becomes zero under the switching state of (O, O, O) of the NPC inverter. In other words, once the measured neutral-point current in an NPC inverter is detected to be zero under the predetermined switching state of (P, O, O), an open-circuit fault can be diagnosed in the IGBT, S_{a1}.

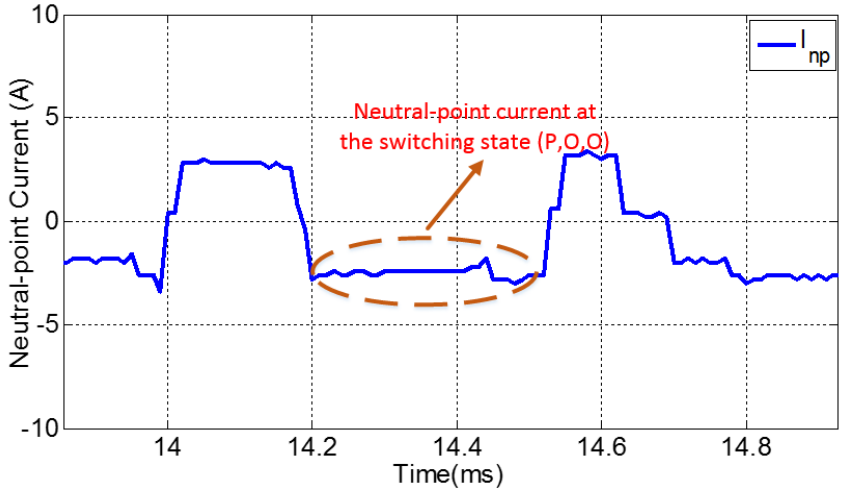


Figure 4.15: Zoom-in view of the measured dc-bus neutral-point current at the switching state of (P, O, O) under healthy condition of the NPC inverter.

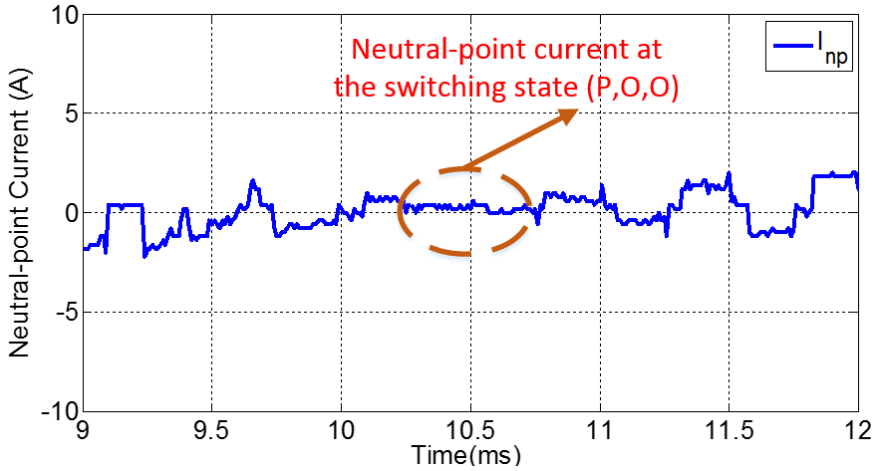


Figure 4.16: Zoom-in view of the measured dc-bus neutral-point current at the switching state of (P, O, O) when an open-circuit switch fault occurred in the IGBT S_{a1} of the NPC inverter.

In the same manner, an open-circuit fault in the IGBT, S_{a2}, was investigated in the customized ASD experimental setup. The measured three-phase load currents and the dc-bus neutral-point current are shown in Fig. 4.17 and Fig. 4.18, respectively. The fault signatures associated with the open-circuit fault in IGBT S_{a2}, namely, the changes in the profiles of the neutral-point current under the switching state of (O, N, N), are demonstrated in Figs. 4.19 and 4.20. It can be seen in these figures that the dc-bus neutral-point current at the switching state of (O, N, N) is around 7A under healthy condition, which drops to zero for the same switching state when S_{a2} experiences an open-circuit fault. The time duration of the zero value of this current representing this fault signature is 0.5 ms, as shown in Fig. 4.20. Such duration can be easily detected by general hall-effect current sensors or shunt resistive sensors in industrial ASD systems.

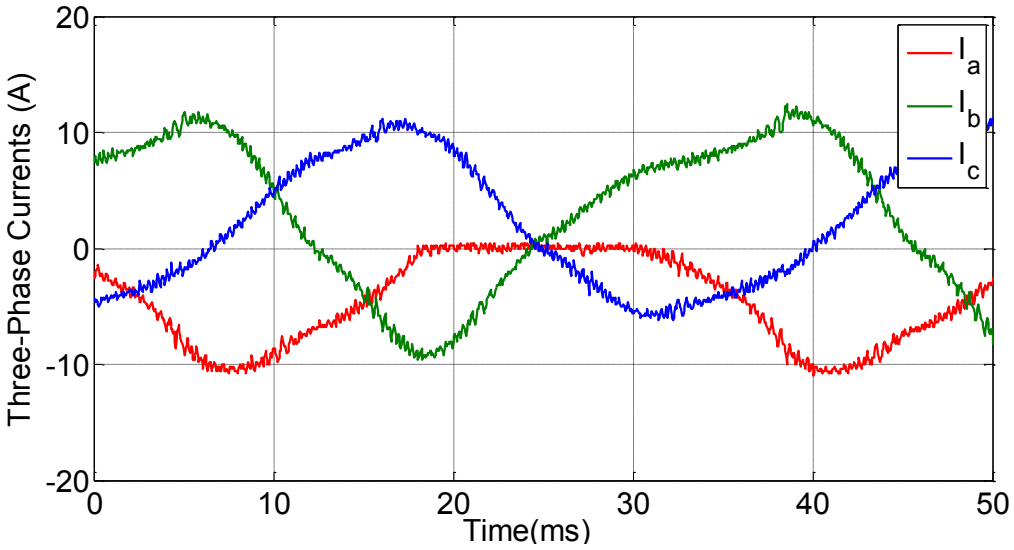


Figure 4.17: Measured three-phase load currents when an open-circuit switch fault occurred in the IGBT S_{a2} of the NPC inverter.

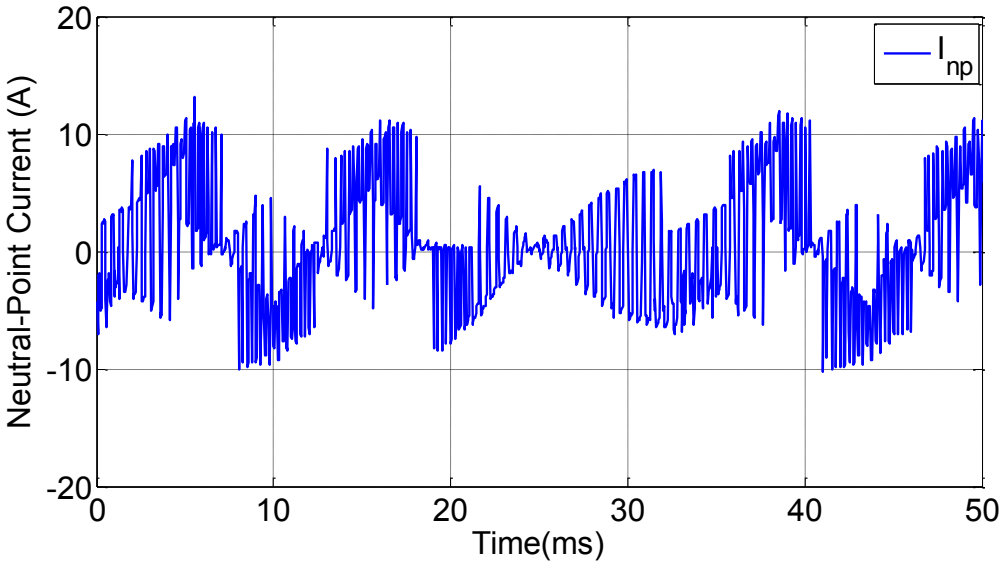


Figure 4.18: Measured dc-bus neutral-point current when an open-circuit switch fault occurred in the IGBT S_{a2} of the NPC inverter.

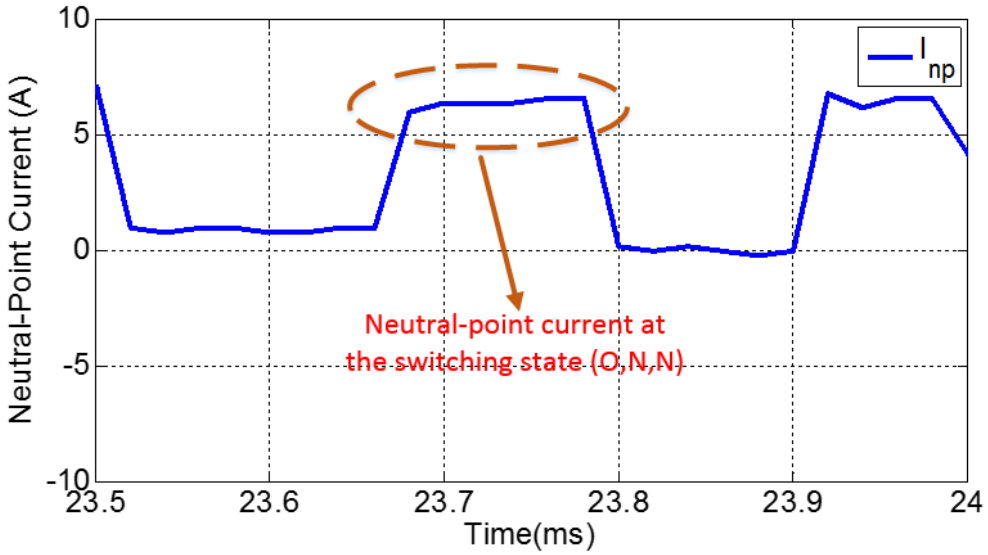


Figure 4.19: Zoom-in view of the measured dc-bus neutral-point current at the switching state of (O, N, N) under healthy condition of the NPC inverter.

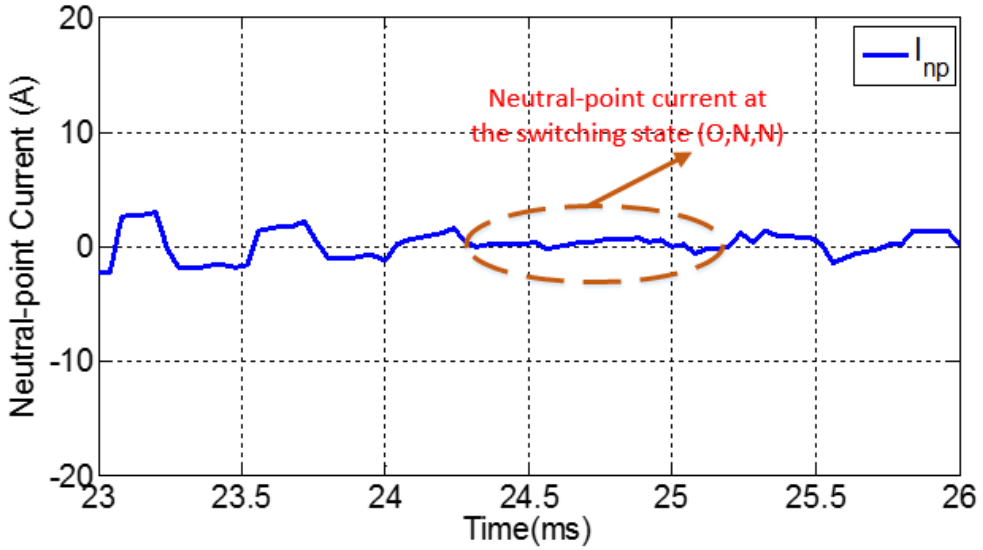


Figure 4.20: Zoom-in view of the measured dc-bus neutral-point current at the switching state of (O, N, N) when an open-circuit switch fault occurred in the IGBT S_{a2} of the NPC inverter.

In conclusion, the measured experimental results given in this section verified the effectiveness of the proposed diagnostic method for IGBT open-circuit faults in a three-level NPC inverter, which are also consistent with the simulation results presented in Section 4.5 in this chapter. It should be mentioned that this diagnostic method is mainly introduced for improving the reliability of medium-voltage high-power ASDs, which are generally operated at low switching frequencies (e.g., below 5 kHz) [81]. For the NPC inverters used in low-power high-frequency industrial applications, such as solar power conversion, which requires higher switching frequencies for the NPC inverters, such a novel diagnostic method may not detect IGBT switch faults accurately due to the short duration of the switching states for the inverter and the limited frequency bandwidth of the general current sensors. Under such scenario, a high frequency bandwidth dc current sensing solution is recommended to implement the proposed diagnostic method for IGBT faults.

4.6 Summary

In this Chapter, diagnosis of IGBT faults in NPC inverters was introduced. Negative impacts of switch faults on the performance of such inverters were analyzed, and both simulation and experimental results were given to confirm the analysis. A novel on-line diagnostic method has been presented to diagnose IGBT faults in an NPC-inverter-based ASD. The operating principle of this method is based on monitoring the variations in the dc-link neutral-point current. Such neutral-point current under faulty switch conditions is very different from that under healthy conditions. By leveraging the information of the switching states and load currents of the NPC inverter, a faulty switching device can be identified through monitoring of the dc-link neutral-point current. The advantages of this diagnostic method include the fast detection speeds (within one period of the fundamental frequency) and a very slight increase in system cost (only one additional current sensor needed to be added for sensing the dc-link neutral-point current). This method is easy to implement, and no complex computational efforts are required. Therefore, it is totally feasible to integrate such diagnostic method into the microcontrollers of the related ASDs or power electronic systems for enhancing such system reliability.

CHAPTER 5

A FAULT-TOLERANT TOPOLOGY OF T-TYPE NPC INVERTERS

5.1 Introduction

T-Type NPC inverters have been regarded as constituting a very promising topology of high-performance multilevel inverters in industrial applications. This is because of the relatively lower number of switching devices utilized in this topology, and its higher efficiency compared with the conventional I-Type NPC inverters [60]. However, like other types of multilevel inverters, T-Type NPC inverters are not immune to switching device faults. For instance, when such inverters are applied in safety-critical applications, such as EVs/HEVs and UPSs, any IGBT open-circuit or short-circuit faults in these inverters would cause catastrophic system failures if no fault-tolerant solution is provided. Although T-Type NPC inverters have certain inherent fault-tolerant capability due to their unique topology, as reported in [69, 70], the output voltage and linear operating range will be derated significantly during fault-tolerant operation. This derating is not allowed in some applications such as these mentioned above, namely, UPSs, EV/HEVs, etc., where rated output voltages are always a stringent requirement. Therefore, it would be of great necessity to improve the inverter topologies with satisfactory fault-tolerant characteristics, to guarantee rated output voltages not only under healthy but also under faulty conditions.

However, the existing solutions for the fault-tolerant operation of T-Type NPC inverters are mainly achieved by paralleling one or three redundant inverter

legs, as discussed in Section 2.3 of Chapter 2. Some of the redundant design solutions do ensure a rated voltage output under inverter faulty conditions, but at a much higher system cost with decreased efficiency due to the considerable additional semiconductor devices employed. As a matter of fact, most of the redundant semiconductor devices in the existing fault-tolerant topologies just idle most of the time in the circuits without any contributions to improving system performance under healthy conditions, while degrading system efficiencies due to the additional device switching and conduction losses.

5.2 The Proposed Fault-Tolerant Topology

In this chapter, a novel fault-tolerant solution is introduced for conventional T-Type NPC inverters. The fault-tolerant topology proposed here is shown in Fig. 5.1. In this topology, a redundant inverter leg is added to help improve the inverter thermal overload capability under healthy condition. This is by sharing part of the load current. Meanwhile, this extra leg can also be used to mitigate other device faults while maintaining rated output voltages under faulty conditions. The following sections will elaborate on the operating principle and advantages of this proposed fault-tolerant inverter topology including simulation and experimental results.

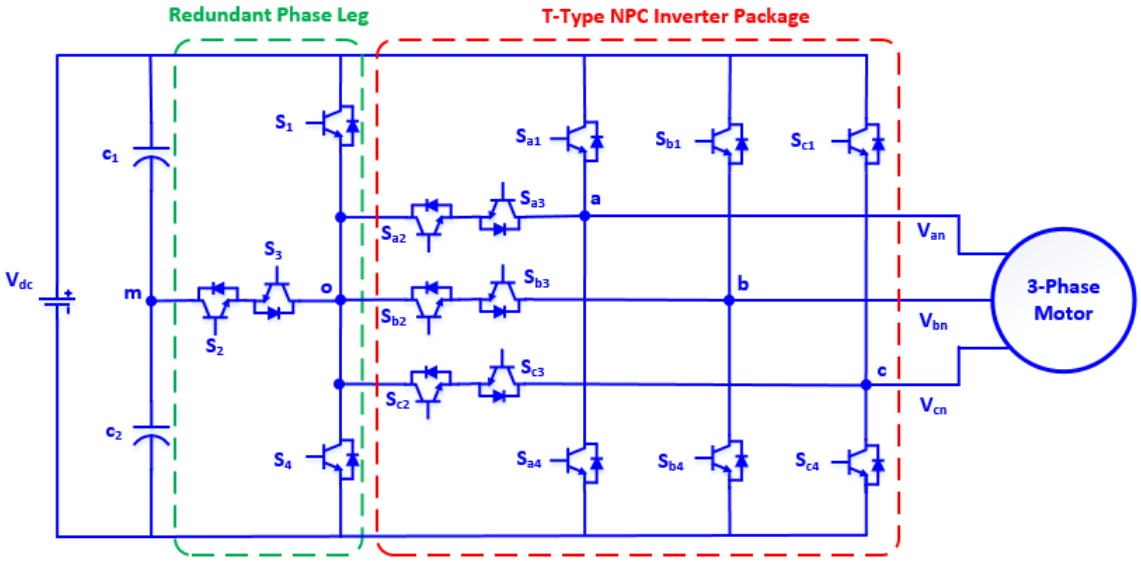


Figure 5.1: The proposed fault-tolerant topology for the T-Type NPC inverter.

5.3 Fault-Tolerant Operation of the Proposed Topology

Considering the circuit symmetries of this T-Type NPC inverter, only four cases of switch faults are analyzed in the following sections to represent all the possible switch fault scenarios that could happen in such an inverter. Here, it is assumed that only single type of device fault happens in the inverter. It should be noted that the fault scenario analysis and fault-tolerant solutions discussed below only focus on IGBT devices in the T-Type inverters, although these concepts also applicable to mitigating the faults in the related free-wheeling diodes.

Case I: Open-Circuit fault in IGBT S_{a1}

Once an open-circuit fault in IGBT S_{a1}, see Fig. 5.2, is identified, the Phase-A leg of the T-Type inverter will not be able to produce a positive voltage. Under such a scenario, the IGBT S_{a1} will be replaced by the switch S_1 on the redundant phase leg through the switching-on of the IGBT S_{a2}, while all other IGBTs on the redundant leg are kept in the "off" state, as depicted in Fig. 5.2. As can be seen in

this figure, during such fault-tolerant operation, the three-phase inverter can still output the rated voltages. However, the inverter will have to be operated as a two-level one. Similar fault-tolerant solutions can be applied for open-circuit faults in other IGBTs S_{x1} (where x=b or c) and S_{x4} (where x=a, b, or c).

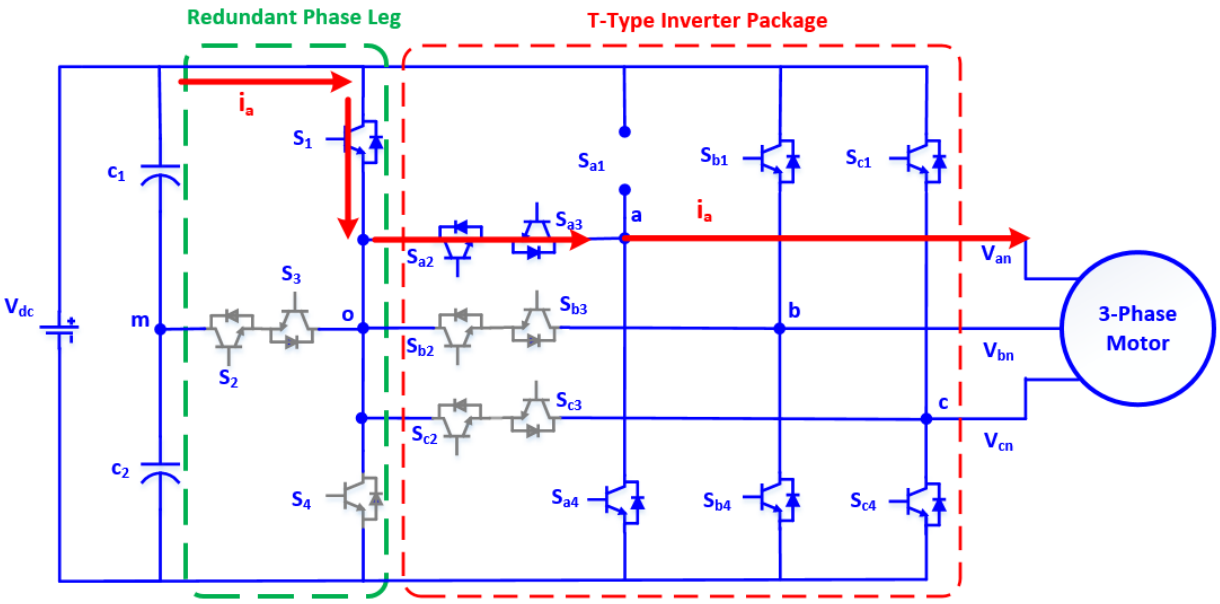


Figure 5.2: Current flow illustration during fault-tolerant operation when the IGBT S_{a1} has an open-circuit fault.

Case II: Short-circuit fault in IGBT S_{a1}

Generally, a short-circuit failure mode in IGBT modules concludes with an open-circuit mode due to the large short-circuit current and rapidly accumulated heat dissipation in the IGBT bond wires or soldering joints if no fast protection actions are available (typically, protection should be triggered for such faults within 10 μs [45]). When a short-circuit fault occurs in the IGBT S_{a1}, assuming that the large short-circuit current will change the short-circuit failure mode into an open-circuit failure mode by melting the internal bond wires in the IGBT package, it follows that the fault-tolerant solution to such a fault scenario will be

the same as that for an open-circuit fault which was explained in Case I above.

Case III: Open-Circuit fault in IGBT S_{a2}

If an open-circuit fault happens in the IGBT S_{a2}, the three-level T-Type NPC inverter will have to be operated as a two-level one, only by using S_{a1} and S_{a4} (see Fig. 5.3) for fault-tolerant operation (the same as the conventional two-level inverter operation), which is due to the loss of the bi-directional switch (constituted by the reverse series connection of S_{a2} and S_{a3}) accessing the dc-bus middle point for the faulty phase. Under such a situation, all the switches on the redundant leg and all the bi-directional switches (S_{x2} and S_{x3}, x=a, b, or c) will be switched off, as shown in Fig. 5.3. There is no derating for the rated and maximum voltage outputs during the post-fault operation. However, the harmonic distortion will be higher under two-level modulation compared with that under three-level modulation. Similar fault-tolerant solutions can be applied to the open-circuit faults in all other IGBTs S_{x2}/S_{x3} (x=a, b, or c).

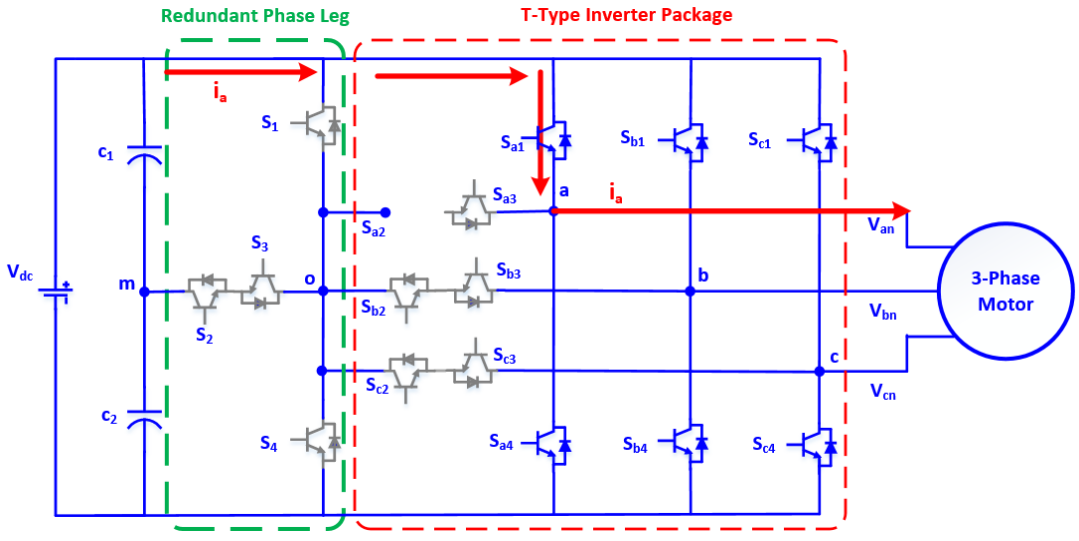


Figure 5.3: Current flow illustration during fault-tolerant operation when IGBT S_{a3} has an open-circuit fault (grey color refers to the switching-off state).

Case IV: Short-circuit fault in IGBT S_{a2}

If a short-circuit fault in IGBT, S_{a2}, is identified, its complimentary switch, S_{a3}, has to be switched off due to the loss of reverse blocking capability in the Phase-A leg. Consequently, the three-level inverter will have to be operated as a conventional two-level inverter by only using S_{a1} and S_{a4} for post-fault operation. This procedure is similar to Case III, which was discussed above. A similar fault-tolerant strategy can be applied for short-circuit faults in IGBTs S_{x2} (x=b, or c) and S_{x3} (x=a, b, or c).

In summary, as can be seen here that when any of the IGBTs in the T-Type inverter has a fault, there is no derating required during the fault-tolerant operating mode of the inverter. However, such an inverter has to be modulated as a two-level type under these faulty conditions, which implies a slightly higher harmonic distortion in the output currents and voltages compared to these under three-level healthy operation. Meanwhile, it should be noted that reliability of these inverters has a much higher priority than the slight increase of harmonic distortion, particularly for these inverters used in safety-critical applications.

5.4 Thermal Overload Improvement

It is known that three-level NPC inverters exhibit output voltage waveforms similar to two-level inverters at low amplitude modulation indices (i.e., $Ma \leq 0.5$) [82]. Under such condition, as depicted in Fig. 5.4, the bi-directional switches (S_{x2} and S_{x3} x=a, b, or c), instead of being used to output any zero voltage states, can be used to interconnect/conduct the redundant phase leg to any of the original three legs of the T-Type inverter for purposes of sharing any overload current.

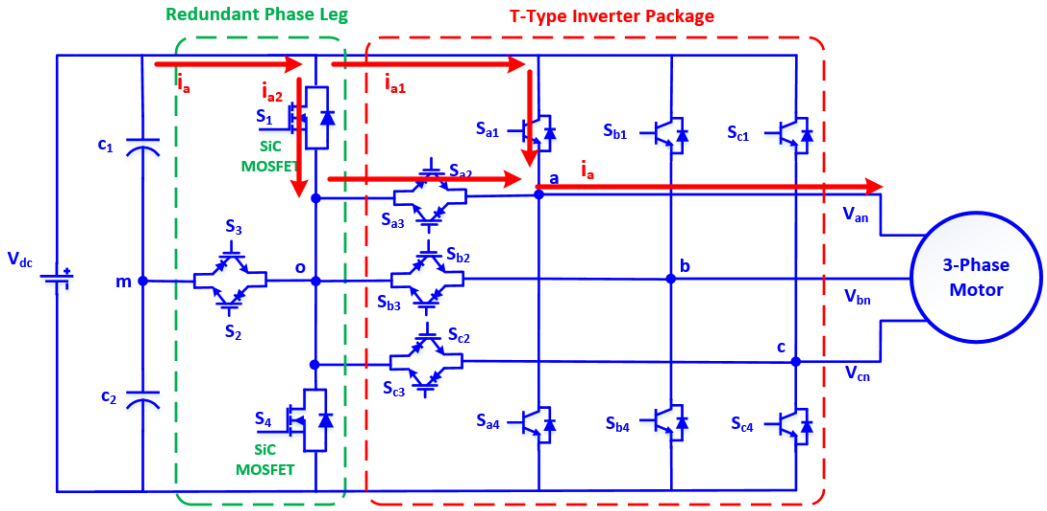


Figure 5.4: Current flow directions of a SiC redundant phase leg sharing the overload current with the Phase-A leg of the original T-Type inverter.

To increase the load current sharing ratio and restrict additional device losses in the redundant phase leg, SiC MOSFETs are used here for switches S_1 and S_2 in the redundant leg, and a commercial modular three-level T-Type inverter package is employed where the RB-IGBTs are utilized as the bi-directional switches in such a package due to their low on-state voltage drops [83]. To illustrate the load current sharing between the redundant leg and one of the original inverter legs in the T-Type inverter, the I-V curve comparison between the IGBT S_{a1} and the other commutation path formed by switches S_1 and S_{a2} is shown in Fig. 5.5. As can be seen in this figure, if the T-Type NPC inverter under normal operation is rated to drive a continuous load current of 40A (RMS), it follows that the redundant leg can share an additional load current of 10A (RMS) considering the same resultant on-state voltage across the two parallel paths that are depicted in Fig. 5.4. This indicates that the total load current can be increased from 40A to 50A (RMS) by using this redundant leg, which is an improvement of 25% overload capability compared to the original overload rating. Moreover, such load current sharing

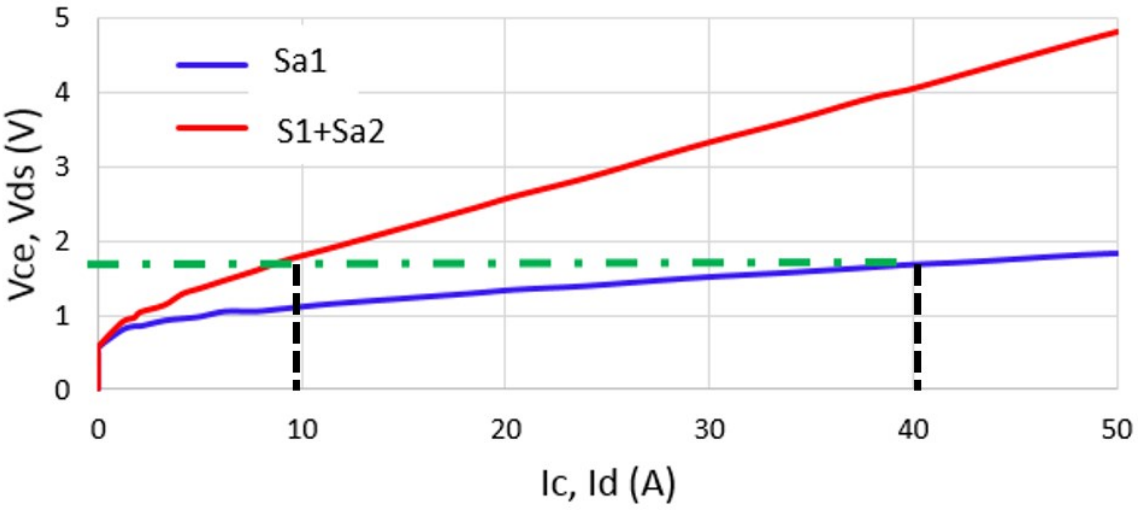
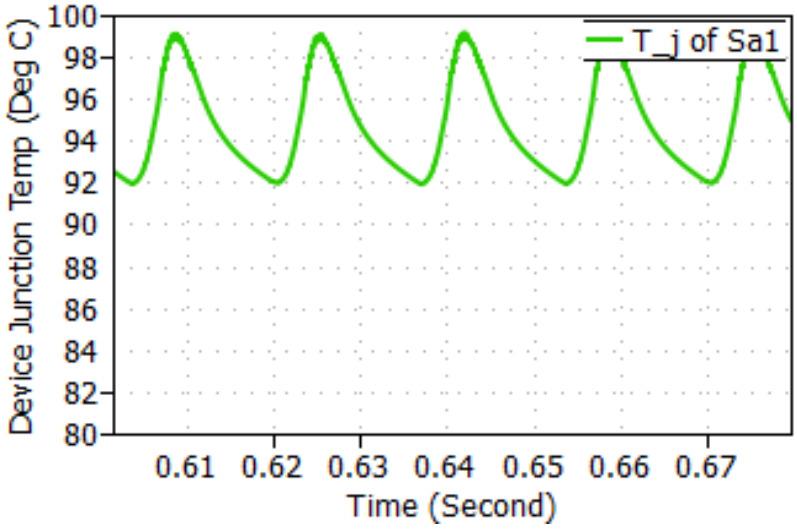


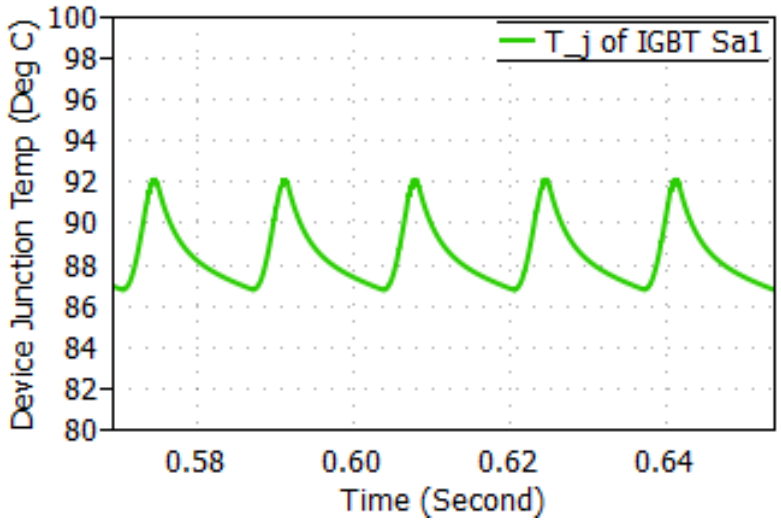
Figure 5.5: Comparison of output characteristics (I-V curves) between S_{a1} and the redundant half-bridge constituted by the series connection of switches S_1 and S_{a2}.

achieved by the redundant leg in this proposed inverter topology yields lower junction temperatures in the switching devices of the original T-Type inverter. According to the simulations carried out in PLECS software, the junction temperature profiles of the IGBT S_{a1} with/without the current sharing from the redundant phase leg under the same thermal overload conditions are shown in Figs. 5.6 (a) and (b). Examining this figure, a significant mitigation of the junction temperatures in the switch S_{a1}, see Fig. 5.4, can be realized through the use of the redundant phase leg for load current sharing. Specifically, the average value of the junction temperature in S_{a1} is reduced from 95.5℃ to 89.8℃ by leveraging the load current sharing capability of this redundant leg, as shown in Figs. 5.6 (a) and (b). Furthermore, it can be observed that the swing magnitude of the junction temperature in S_{a1} is reduced from 7℃ to 5℃ by taking advantage of this redundant leg, which will improve the power cycling lifetime of the related power device, as previously presented in Chapter 3. In conclusion, such improvement in the thermal

overload capability is of great significance for some industrial applications such as EVs (e.g., hill climbing), servo motor drives, etc., where overload or high torque is one of the most common functional requirements [84, 85].



(a)



(b)

Figure 5.6: Comparison of the junction temperature profiles of IGBT S_{a1} under heavy load conditions with/without using the redundant phase leg for load current sharing (a) without using the redundant leg (b) with using the redundant leg.

5.5 Efficiency Improvement with the Proposed Topology

Most of the fault-tolerant power converter topologies have a lower efficiency than the original topologies for normal operations, which is due to the addition of redundant power devices. A good case in point is the fault-tolerant solution proposed in [15], see Fig. 2.25, which significantly reduces the converter efficiency due to the constant conduction of six redundant IGBTs added to the conventional T-Type three-level inverter topology. However, the fault-tolerant power converter topology introduced in this Chapter has the potential of improving converter efficiency, if one adopts a zero-voltage-switching (ZVS) pattern. The following subsections will introduce this ZVS switching pattern for this proposed fault-tolerant T-Type inverter topology introduced here in this dissertation. Simulation results are given to confirm the efficacy of this concept.

5.5.1 A ZVS Switching Pattern for "SiC+Si" Hybrid Devices

It is well known that wide bandgap semiconductor devices (SiC, GaN, diamond, etc.) have much lower switching losses than their Si counterparts due to the material properties [86-87]. Also, one should be aware that whenever SiC/GaN devices are parallel connected with the Si devices, as shown in Fig. 5.7, it is feasible to reduce the total device losses by having the SiC/GaN devices undertake the majority of the switching losses of the parallel devices through adopting a ZVS switching pattern. Such a ZVS switching pattern is depicted in Fig. 5.8. As shown in this figure, the SiC MOSFET is turned on prior to the switching-on of the Si IGBT in the parallel-connected hybrid devices. After the turn-on of the SiC

MOSFET, the voltage across the hybrid devices will be reduced from the high blocking voltage to a very low on-state voltage, which provides a quasi ZVS for the later switching-on of the Si IGBT. Similarly, for the switching-off of the hybrid devices, the Si IGBT is switched off prior to the switching-off of the SiC MOSFET, in order to achieve the quasi ZVS on the Si IGBT. Therefore, it can be seen that the switching losses only come from SiC MOSFET. However, these switching losses are very low due to the property of the wide bandgap material constituting such devices. The turn-on delay and turn-off delay between the gate signals for SiC MOSFET and Si IGBTs are generally several microseconds, which can be easily achieved through programming in the microprocessor. More details about this switching pattern are presented in references [88-90].

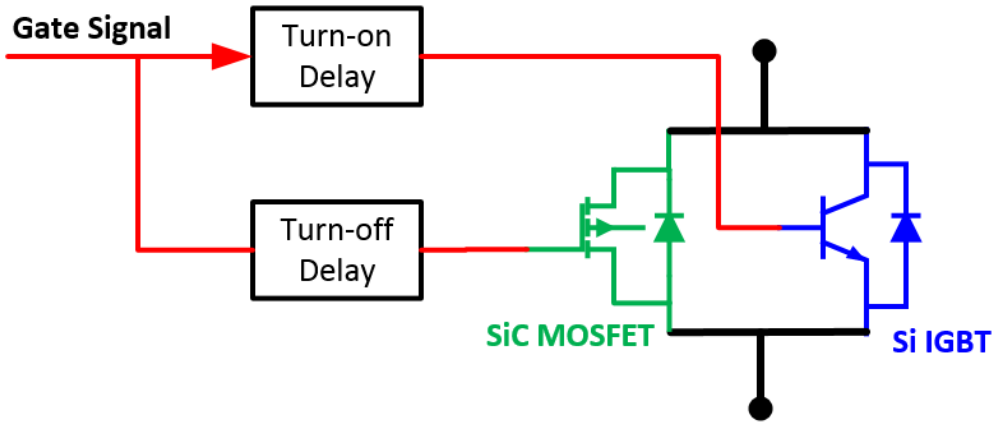


Figure 5.7: ZVS switching strategy for "SiC+Si" hybrid devices.

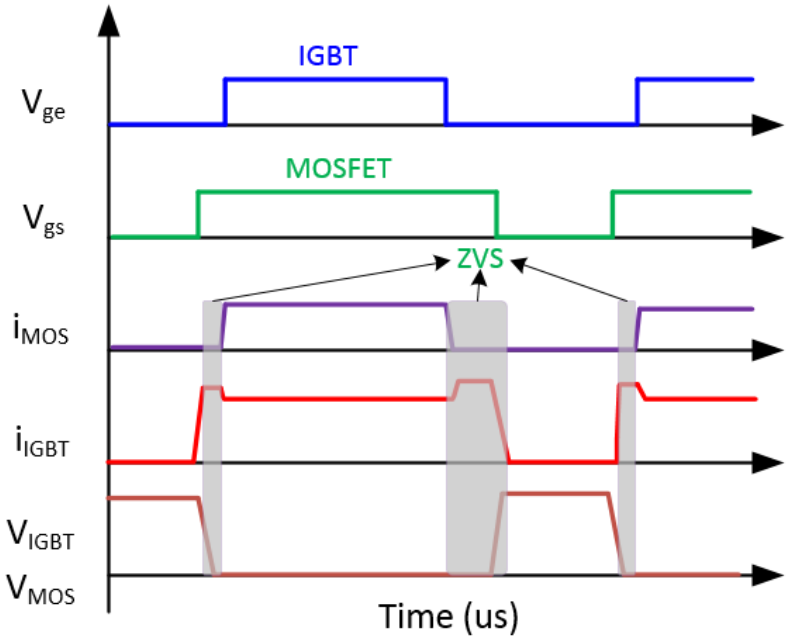


Figure 5.8: Switching sequence of the fault-tolerant T-Type inverter.

5.5.2 A Novel PWM Switching Pattern for the Proposed Fault-Tolerant Inverter Topology

Meanwhile, the fault-tolerant T-Type power converter topology introduced earlier in this Chapter provides a promising opportunity to implement such ZVS switching pattern explained in the above section. As shown in Fig. 5.9, whenever the redundant leg is used to share the positive overload current with the original inverter phase legs, S_1 and S_{x2} (x=a, b, or c) can be switched on prior to the switching-on of S_{x1}(x=a, b, or c), which indicates that the voltage across the switch S_{x1} will be very low when this device is switched on. A similar switching mechanism can be applied whenever a negative overload current needs to be shared between S_4 and S_{x3} (x=a, b, or c). Assuming that, these switches, namely, S_1, S_4, S_{x2} and S_{x3} are SiC/GaN devices, and S_{x1} and S_{x4} (x=a, b, or c) are conventional Si devices such as IGBTs, it follows that the efficiency of the

proposed fault-Tolerant T-Type inverter will be significantly improved if the ZVS switching pattern is applied to the proposed fault-tolerant T-Type inverter.

With the application of this ZVS switching pattern, the switching sequence for all the controllable power devices of the proposed fault-tolerant T-Type inverter is shown in Fig. 5.9. By implementing such switching pattern in the PLECS software, the load current sharing between the redundant SiC MOSFET, namely, S_1 and the Si IGBT, namely, S_{a1} is shown in Fig. 5.10. This figure shows the current sharing at the turn-on instant, turn-off instant, as well as the current sharing under parallel conduction mode. It should be noted that not for all the switching states can the redundant leg be utilized for the overload current sharing, which is the reason accounting for the discontinuous current sharing between switches S_1 and S_{a1}, as depicted in Fig. 5.10. As mentioned in Section 5.4, the utilization of the redundant leg only happens when the T-Type inverter is operated at low modulation indices ($M_a<0.5$). Under such scenario, there is no degradation of the harmonic distortions in the inverter output currents/voltages, compared to these during normal operation. At high modulation indices ($M_a \geq 0.5$), the utilization of the redundant leg will prevent the access to the dc-bus middle point for obtaining zero voltages, which will render the three-level change into two-level modulation. As a result, the harmonic distortions in the inverter output voltages or currents will be slightly higher. The simulation results to be given in the following section will further explain this perspective.

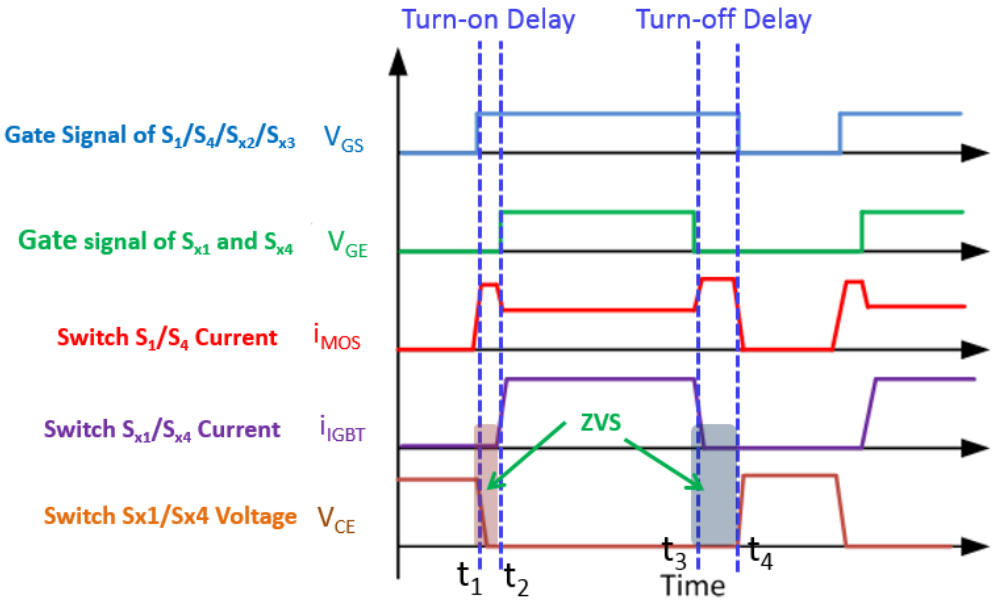


Figure 5.9: Switching sequence of the fault-tolerant T-Type inverter.

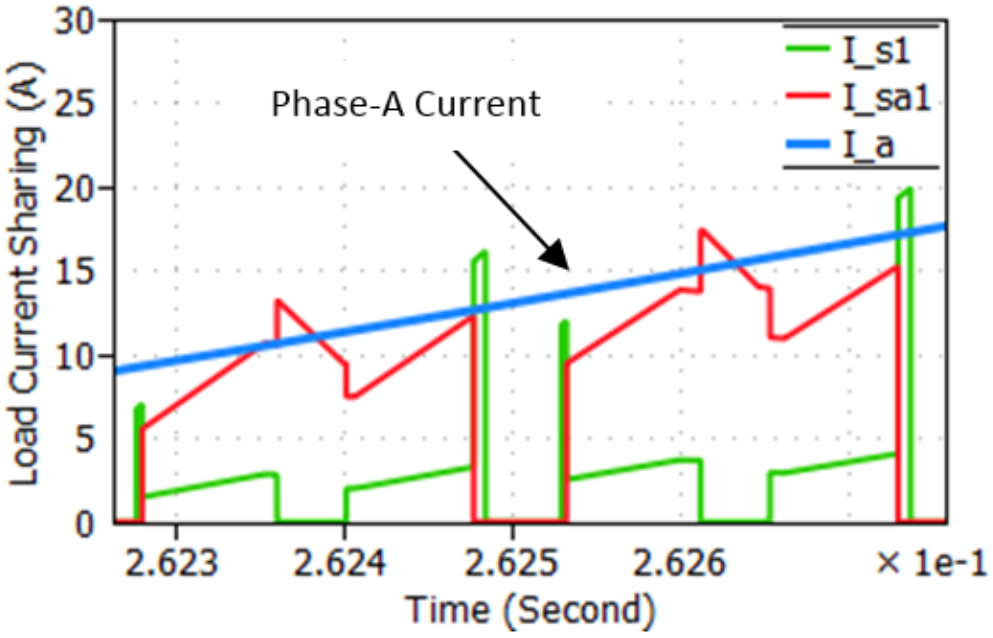


Figure 5.10: Load current sharing between switches S_1 and S_{a1}.

5.6 Experimental Results

A lab-scale 30 kVA ASD prototype based on the proposed fault-tolerant T-Type inverter topology has been designed. This ASD prototype is composed of several important functional units, including a diode rectifier, dc-bus capacitors, contactor-based precharge mechanism, three-phase four-leg T-Type inverter, DSP controller, signal conditioning PCB, and switched mode power supplies (SMPS), as shown in Fig. 5.11. The fourth redundant leg is constituted by four SiC MOSFETs and external SiC Schottky diodes, and the related circuit schematics as well as the basic parameters are given in the Attachment B of this dissertation. Open-circuit faults in the IGBT S_{a1} and S_{a2} (as shown in Fig. 5.4) and the corresponding fault-tolerant operation control strategies were examined, which represents all fault scenarios for IGBT open-circuit switch faults considering the circuit symmetry of the T-Type inverter. The three-phase line-to-neutral voltages were measured under the fault-tolerant operation of the T-Type inverter with an open-circuit switch fault in the switches S_{a1} and S_{a2}, the oscillograms of which are shown in Fig. 5.12 and Fig. 5.13, respectively. It can be seen from these figures that the three-phase line-to-natural voltages are balanced during fault-tolerant operations and there is no derating in the output voltages. Under these fault-tolerant operations, the three-level output will become a two-level output–due to the unavailability of using the RB-IGBTs (S_{x2} and S_{x3}, where x=a, b, or c) to access the dc-bus midpoint. This accounts for the slightly higher harmonic distortion in the output voltages as shown in Fig. 12 and Fig. 13. However, as discussed in Section 5.3, under such faulty conditions, fault-tolerant operation has a higher

priority than the degradation of output waveform quality, especially in safety-critical applications.

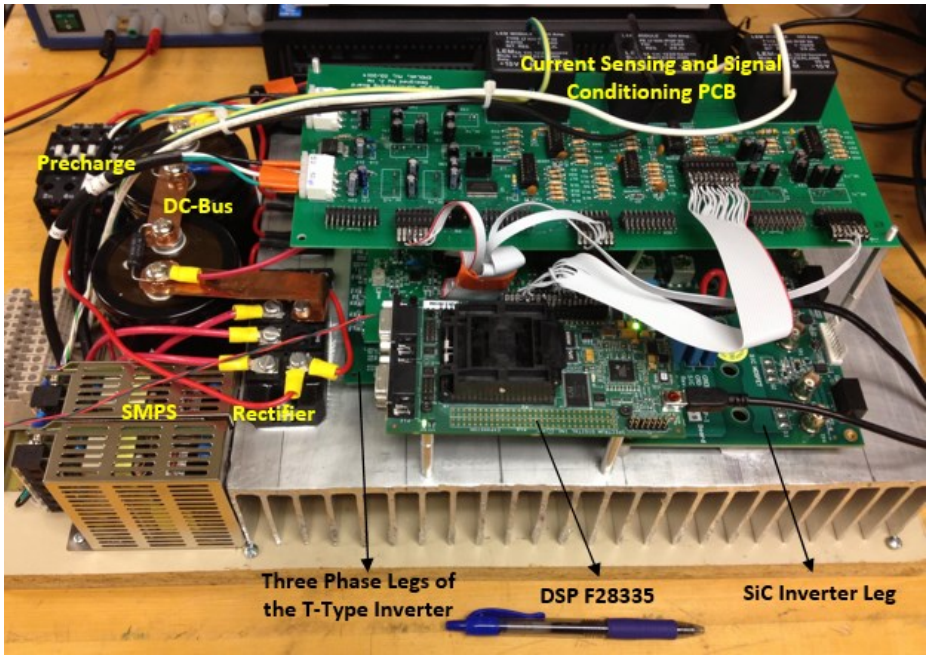


Figure 5.11: Customized 30-kVA fault-tolerant ASD based on the proposed fault-tolerant three-level four-leg T-Type inverter topology.

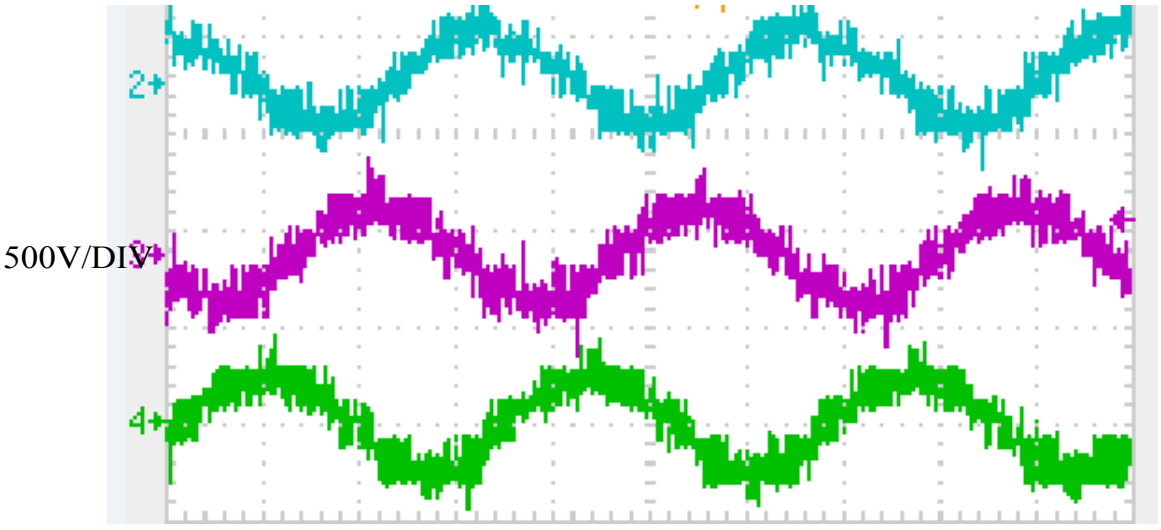


Figure 5.12: Measured three-phase line-to-neutral voltages during the fault-tolerant operation of the proposed four-leg T-Type NPC inverter with an open-circuit fault in the IGBT S_{a1}.

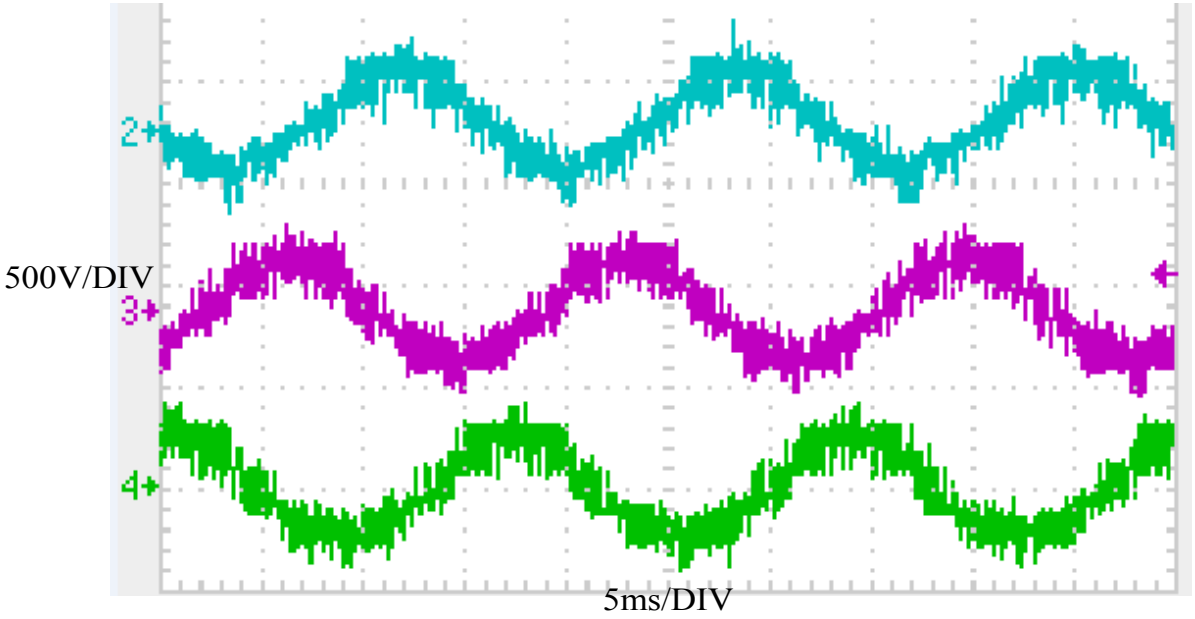


Figure 5.13: Measured three-phase line-to-neutral voltages during the fault-tolerant operation of the proposed T-Type NPC inverter with an open-circuit fault in the IGBT S_{a2}.

5.7 Summary

This chapter introduced an improved fault-tolerant inverter topology based on the conventional T-Type NPC inverter. According to the simulation and experimental results presented above, a few conclusions can be drawn as follows:

1) The proposed fault-tolerant inverter topology provides desired fault-tolerant solutions to device open-circuit and short-circuit faults in the T-Type inverters. During post-fault operation of any of the device faults, the inverter is still able to output the same maximum and rated voltage/power as that under normal operation. In other words, no derating is required during fault-tolerant operation, although the inverter has to be controlled as a two-level one.

2) Under normal healthy condition, the redundant inverter leg helps to share the overload current with the inherent three inverter legs, and therefore can

significantly improve the inverter thermal overload capability. Since a normal T-Type inverter exhibits the waveforms of the output voltages as a conventional two-level inverter under low modulation indices ($Ma \leq 0.5$), there is no penalty in harmonic distortion in the output voltages under such scenario. Moreover, the redundant leg can also be utilized for load current sharing at high modulation indices ($Ma > 0.5$) to relieve large thermal stress on main switches (S_{x1}/S_{x4}), but the harmonic distortion in the output voltages will be slightly higher compared to these output voltages from a three-level modulation.

CHAPTER 6

CONCLUSIONS, CONTRIBUTIONS AND FUTURE WORK

6.1 Conclusions

Power electronic converters play a critical role in industrial ASDs and other power conversion systems. However, the reliability of power electronic converters has aroused many concerns in recent years. Especially, such concerns are becoming a more challenging technical bottleneck in the development and application of medium-voltage high-power multilevel converters, corresponding to the increasing market demands on the power converter capacities and ever-increasing demand of higher operating frequencies. In this dissertation, the health condition monitoring techniques and fault-tolerant operation strategies for NPC-inverter-based ASD systems have been investigated. Throughout the content of this dissertation, these investigations started from the estimation and active extension of power cycling lifetime of NPC inverters, which were followed by the explorations of on-line diagnostic methods for IGBT faults in such inverters, and finally concluded with a novel fault-tolerant T-Type NPC inverter topology. All these investigations aim at providing a more comprehensive portfolio of progressive and hierarchical fault prognostics, diagnostics, and fault-tolerant solutions for NPC-inverter-based ASDs.

First of all, the mechanism of lifetime degradation in bond wires and soldering layers in IGBT modules were reviewed. It was concluded that the mismatch of the thermal expansion coefficients of different materials in an IGBT

module is the leading factor for the aging/degradation of the IGBT lifetime. Such degradation is significantly accelerated when there are large junction temperature swings occurring in the IGBT chips. This indicates that if the swings of the IGBT junction temperatures can be mitigated through the modification of PWM switching patterns, the IGBT on-line lifetime could be extended. Based on this motivation, an improved DPWM modulation method was conceived to reduce the junction temperature swings in the most vulnerable IGBT devices in a three-level NPC inverter. In this DPWM method, a zero-sequence signal with a frequency higher than the output frequency of the inverter is injected into the three-phase voltage reference signals in the modulation. The injection of such zero-sequence signals is to reduce the time duration for the rising of the IGBT junction temperatures, and consequently lower swing magnitudes of the junction temperatures can be achieved. According to the thermal modelling and simulation results, the lifetime of an NPC inverter under low-frequency operating conditions can be improved by as much as six times compared to that under the well-known SVPWM modulation. Other performance characteristics of this new DPWM method, including influences on inverter efficiency, harmonic distortions, and oscillation of the dc-bus neutral-point voltage, were all evaluated through simulation and experiments, all with beneficial positive outcomes.

Second, on-line diagnosis of IGBT faults in NPC inverters were investigated in this dissertation. Considering the fact that IGBT short-circuit detection/protection has received much more attention over the past years, and there have been several solutions widely commercialized [46-51], this dissertation is therefore focused on the development of a novel diagnostic method for IGBT

open-circuit faults. Most existing diagnostic methods for IGBT open-circuit faults either use several additional voltage/current sensors [56-58] or have a lower diagnostic speed [52, 53] during the implementation and application. This will boost the system cost and increase the execution burdens on the microprocessors, respectively. However, the diagnostic method introduced in this dissertation only requires the combined information on instantaneous dc-bus neutral-point current and switching states as the fault indicator for IGBT open-circuit faults. The implementation of this novel diagnostic method only demands one addition current sensor for acquiring the variations of the dc-bus neutral-point current, and no complex computations are involved.

Finally, fault-tolerant power inverter topologies were explored in this dissertation. In this new inverter topology, one more addition phase leg is introduced between the dc-bus and the original T-Type inverter. This redundant inverter leg, not only provides a fault-tolerant back-up solution, but also can increase the overload capability and the inverter efficiency if a special switching and control strategy is utilized.

6.2 Contributions

In this dissertation, a thorough investigation on the health condition monitoring techniques and fault-tolerant operation strategies of IGBT faults in multilevel-inverter-based ASDs was conducted. The main contributions in this dissertation are briefly summarized as follows:

1) A novel DPWM method was developed for three-level NPC inverters, which can significantly improve the power cycling lifetime of IGBT

devices during low-frequency operations of such inverters. The essence of this DPWM method is the injection of a zero-sequence signal with higher frequency than the inverter fundamental output frequencies into the voltage reference signals. Through this approach, the swing value of the IGBT junction temperatures can be reduced, which will result in a longer power cycling lifetime. Moreover, the fluctuation of the dc-bus middle point voltage is attenuated by flipping/inversing the zero-sequence signal in every switching cycle. Both simulation and experimental results confirmed the efficacy of this novel approach.

2) An innovative on-line fault diagnostic method was conceived for IGBT open-circuit faults that could occur in three-level NPC inverters. The diagnostic method can identify any faulty switches based on the instantaneous switching states and dc-bus neutral-point current. Since the information of switching states is always available in system microcontrollers, only one additional current sensor is required during the implementation of this diagnostic method, which brings about very low cost increase and hence possible acceptance for commercialization.
3) A novel fault-tolerant topology was developed for three-level T-Type inverters. In this novel fault-tolerant topology, one redundant inverter leg is added to the conventional T-Type inverter. Under healthy conditions, this redundant leg helps to share any overload current with the original phase legs, therefore increasing the converter overload capabilities. Under the condition of a device fault occurring in the T-Type inverter, this redundant leg can be utilized to replace any faulty leg

to output rated voltage and current. Other advantages of this fault-tolerant topology includes the symmetrical circuit structure, very low number of redundant devices, as well as improving the converter efficiency by employing a ZVS switching pattern. Simulation and experimental results have verified these functional advantages of this fault-tolerant inverter.

6.3 Recommendations for Future Work

Several research ideas have materialized as a result of this work presented in this dissertation, which are listed in the following.

First, regarding the novel DPWM method introduced in Chapter 3 for improving the power cycling lifetime of three-level NPC inverters, it can be further extended to five-level or higher voltage levels of NPC inverters. Also, this modulation method can be further optimized to reduce the inverter common-mode voltage by utilizing the redundant zero switching vectors. In other words, if lifetime extension, mitigation of dc-bus neutral-point voltage oscillations, as well as reducing common-mode voltages can all be well considered in this novel DPWM method, the performance of NPC inverters will be significantly enhanced and consequently the applications of such inverters will be made more desirable and further expanded.

Second, the fault diagnostic method for detecting IGBT open-circuit faults, as presented in Chapter 4, can be investigated for detecting IGBT short-circuit faults and diode faults. It should be mentioned that the information on the dc-bus neutral-point current of NPC inverters is like the hub linking the commutation of

each component, which can directly/indirectly indicate the health condition of all the devices in the NPC inverters. Moreover, as pointed out in Chapter 4, this diagnostic method may not be suitable for NPC inverters operated with high switching frequencies. However, if high-bandwidth current sensors and microprocessors (such as FPGA, CPLD, etc.) can be used, this diagnostic method may be also effective for diagnosing device faults in NPC inverters that are operated at higher switching frequencies. All these potential performance benefits accruing from this diagnostic method are worth further investigation through simulations and experiments.

Third, regarding the fault-tolerant T-Type inverter introduced in Chapter 5, the efficiency improvement of this inverter by adopting the ZVS switching strategy needs to be experimentally verified. The implementation of the turn-on and turn-off time delays required in this ZVS strategy should be investigated. In addition, considering the emerging commercialization of SiC/GaN devices, it will be of great significance to implement a purely SiC/GaN device-based fault-tolerant T-Type inverter. The current sharing capabilities and efficiency improvement in such SiC/GaN-type inverter would be quite different from the "Si+SiC" hybrid fault-tolerant inverter described in Chapter 5. Last but not the least, the feasibility of extending this three-level fault-tolerant T-Type inverter to higher voltage level topologies is worth an investigation as well.

In conclusion, health condition monitoring and fault-tolerant operation of power converters for ASDs should be investigated for specific applications, since different applications have different fault-tolerant requirements. In some applications, for example, in industry dealing with national defense, if cost

constraint is not a priority, health condition monitoring and fault-tolerant operation can be achieved by more sensors and redundant hardware devices. On the contrary, in some highly competitive consumer industries, where cost constraints are of paramount priority, then the health monitoring and fault-tolerant operation have to be achieved by taking full advantage of the information that is already available in related ASD systems. However, in general, the most essential purpose is to guarantee the accuracy of the health monitoring and fault-tolerant operation of ASD systems.

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APPENDIX

A. Specifications of the Customized Lab-Scale 50-kVA ASD based on an I-Type NPC Inverter

A.1 Main Features of the ASD

- Texas Instruments Digital Signal Processor (TMS320F28335 DSP) technology integrated with Spectrum Digital EZ-DSP F28335 evaluation board with USB programming port.
- Infineon EconoPACK 4 technology integrated three-level IGBT power modules with attached gate driver/adapter boards with SC and undervoltage lockout protection and junction temperature measurements.
- Signal conditioning systems for IGBT gate driver circuits with isolated dc power supplies current measurement sensors (LEM sensors), incremental optical encoder position feedback, and IGBT junction temperature measurement.
- On-board dc power supplies for EZ-DSP F28335 evaluation board and signal conditioning system.
- Pre-charge circuitry to protect the dc bus from current transients at system turn-on.
- Input reactor for power line quality and high frequency rejection and output LC network for common- and differential-mode filtering.
- Rugged open frame hardware layout for ease of measurements, testing, modifications, and enhancements in addition to a transparent safety enclosure.
- Robust aluminum enclosure to shield the DSP system with short but manageable shielded cables to protect sensitive signals/circuits from EMI.
- Large heat sink and two ventilation fans for maximum heat transfer during high-power drive operation.
- A power switch for the 120 V control circuits.
- Ability to increase drive rating up to 50 kVA through modification of the pre-charge circuitry and bleed resistors.

A.2 Specifications of the ASD System

Table A.2.1: Three-level NPC ASD specifications.

Drive Type	Three-Level IGBT-Based NPC Inverter		
Input	Drive line voltage	200-240	V_{RMS}, Three phase
	Current	18	A_{RMS}, Max
	Power	50	kVA @ 240V_{RMS}
	Frequency	50/60	Hz
	Control voltage	120	V_{RMS}, Single phase
	Control current	5	A_{RMS}, Max
	Reactor	7.3	% Reactance, 60 Hz
	Input fuse size	20	A
	Fuse type		Class CC (KTMR)
	DC bus voltage	325	V_{dc}, Max
Output	Power	50	kVA
	Current	160	A_{RMS}, Max
	Line Voltage	240	V_{RMS}, Three phase
	Filter type		LC
	Filter inductance	2.5	mH
	Filter capacitance	10	μF
DC Supplies	Input voltage	120	V_{RMS}, Single phase
	Supply #1	+5, +12	V_{dc}
		30	W
	Supply #2	±15	V_{dc}
		35	W
EZ-DSP F28335	Input voltage	5	V_{dc}
	Input current	2	A_{dc}, Max
	Operating voltage	3.3	V_{dc}
Signal Conditioning	Input voltage	+5, +12, ±15	V_{dc}
	Input current	2	A_{dc}, @ +5V_{dc}
		1	A_{dc}, @ +12V_{dc}
		500	mA_{dc}, @ -15V_{dc}
		500	mA_{dc}, @ +15V_{dc}
	PWM inputs (18)	+3.3 .. 5	V_{dc}
	PWM outputs (18)	+3.3	V_{dc}, 24 mA_{dc}/ch.
	Encoder QEP inputs (3)	+3.3 .. 5	V_{dc}
	Encoder QEP outputs (3)	+3.3	V_{dc}, 24 mA_{dc}/ch.
	Current sens. Inputs (3)	0 .. 100	A, 1000:1 conv.ratio
	Current sens. Outputs (3)	0 .. 2.5	V_{dc}, 25 mA_{dc}/ch.
	Temperature input range	-50 .. +150	°C
	Temperature outputs (3)	0 .. 2.5	V_{dc}, 25 mA_{dc}/ch.
	Gate driver supplies (10)	+15, -8	V_{dc}, +100/-80 mA_{dc}, isolated
Cooling	Ventilation fans (2)	120	V_{RMS}

A.3 Control Hardware Architecture

A.3.1 Functional Features

- TMS320F28335 DSP programming with Texas Instruments Code Composer Studio (CCStudio) version 3.3 or higher as part of TI's eXpressDSP software and development tools [91, 92].
- Texas Instruments Flash APIs for TMSF28335 support.
- Header files and example code for TMSF28335 DSP controller.
- The Spectrum Digital EZ-DSP F28335 Evaluation Board include the following features:
    - 150 MHz CPU with an integrated Floating Point Unit (FPU).
    - 30 MHz crystal input clock.
    - 512 kB of on-chip flash memory.
    - 68 kB of on-chip single-access RAM (SARAM).
    - 256 kB of off-chip static RAM (SRAM).
    - 88 shared general purpose I/O pins (GPIO).
    - Up to 12 channels of PWM with a dedicated six channels of high-resolution PWM (HRPWM).
    - An additional six auxiliary channels of PWM can be utilized with proper configuration of the six 32-bit capture (eCAP) inputs.
    - Two quadrature encoder position feedback channels (QEP), with each channel consisting of four signals.
    - 16 analog to digital converters (AD) with 12-bit resolution and 80 ns conversion time.
    - Three 32-bit CPU timers
    - A broad range of communications interfaces are onboard: RS-232 connector with line driver, CAN 2.0 interface with line driver, embedded USB JTAG controller, and an IEEE 1149.1 JTAG emulation connector.

A.3.2 Hardware Description

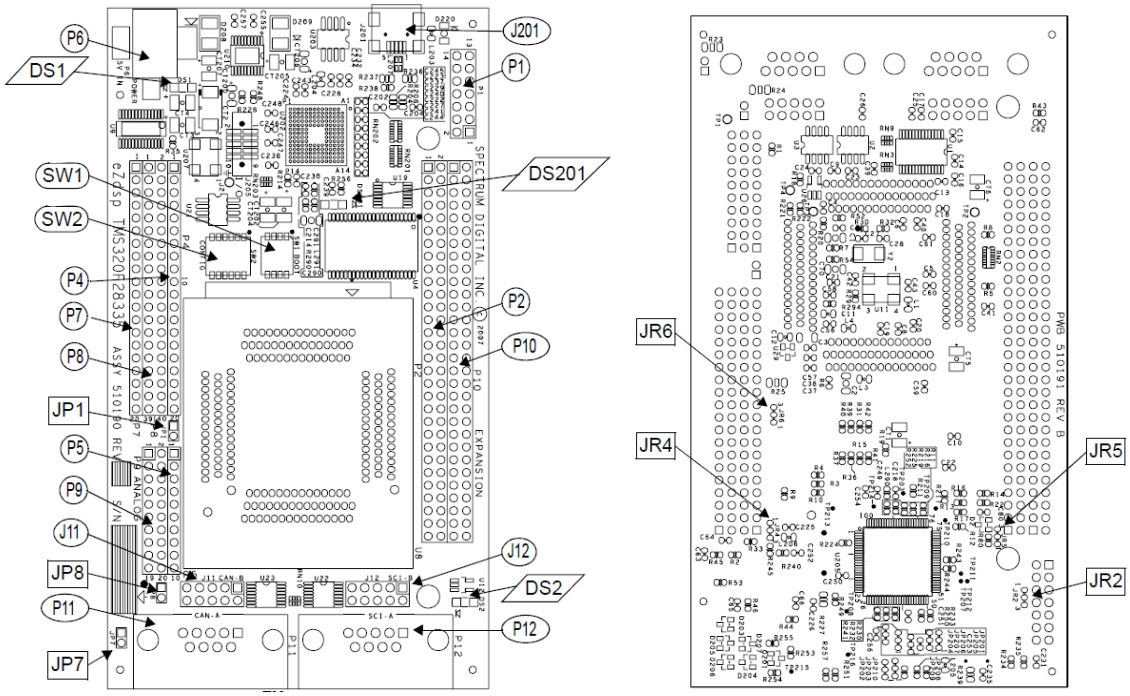

Figure A.3.2.1: EZ-DSP F28335 DSP board layout and component identification. (a) top view, (b) bottom view [91].

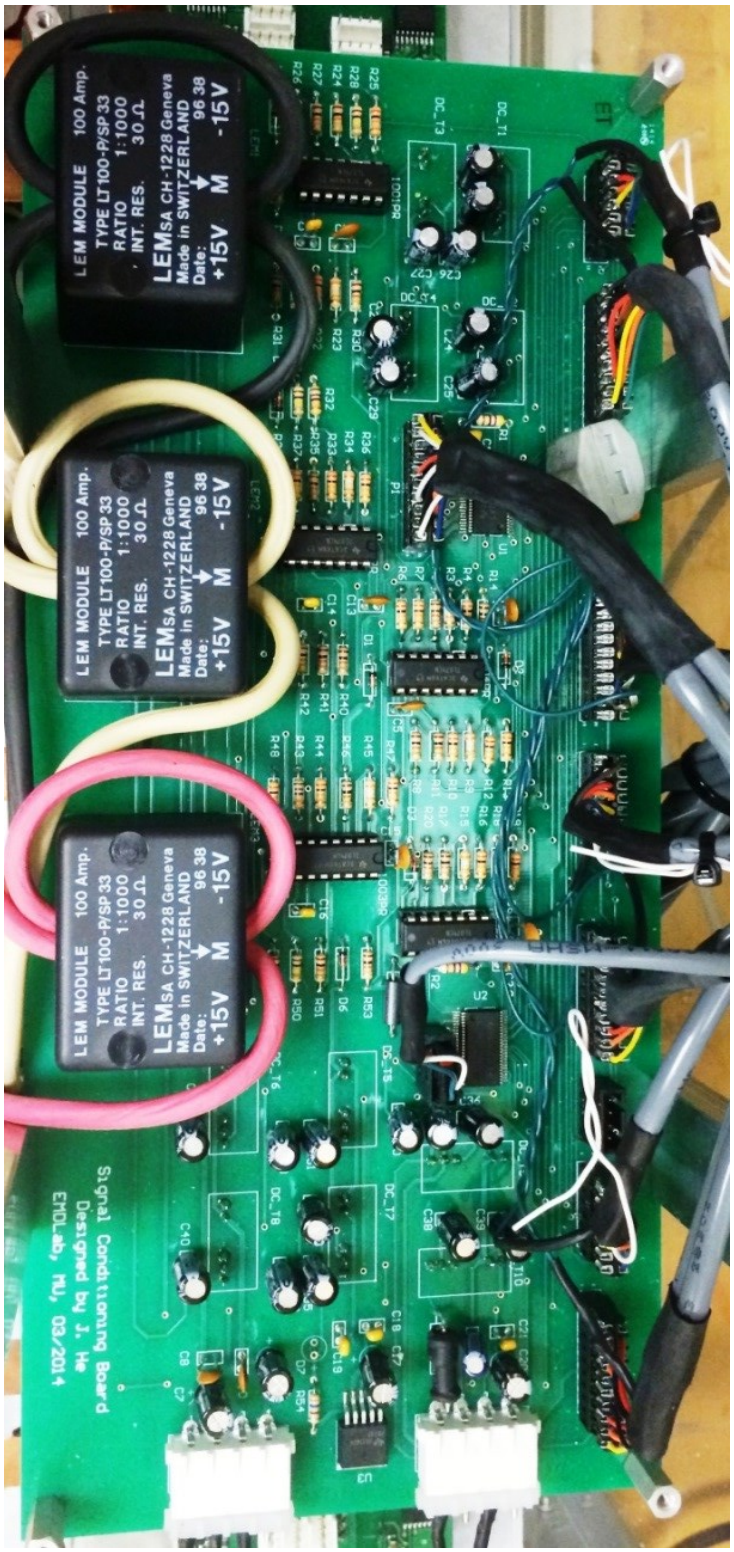

Figure A.3.2.2: Customized universal signal condition circuit board for general ASD systems.

Table A.3.2.1: EZ-DSP F28335 component/device description and settings.

Identifier	Settings/Connections	Description
DS1	Green LED	+5 V_{dc} active
DS2	Green LED	GPIO32 status
DS201	Green LED	Embedded emulation link status
J11	No connection	CANB header connection (2 x 5)
J12	No connection	SCIB header connection (2 x 5)
J201	USB Programming Port	Embedded USB JTAG interface
JP1	Shorted	+2.048 V_{dc} connected to ADCREFIN
JP7	Shorted	CANA termination resistor installed
JP8	Shorted	CANB termination resistor installed
JR2	+3.3 V_{dc}	+3.3/5 V_{dc} supply selection to XTPD
JR4	+3.3 V_{dc}	+3.3/5 V_{dc} supply selection to P4 & P8
JR5	+3.3 V_{dc}	+3.3/5 V_{dc} supply selection to P2 & P10
JR6	GPIO22 Selected	MUX GPIO22/GPIO24 selection
P1	No connection	JTAG interface header connection (2 x 7)
P2	No connection	Expansion interface header connection (2 x 30)
P4	No connection	I/O interface header (1 x 20)
P5	No connection	Analog inputs B0-B7, ADCREFM, ADCREFP
P6	+5 V_{dc}	Power connector
P7	No connection	I/O interface header (1 x 20)
P8	PWM outputs (16)	I/O interface header (2 x 20)
P9	Analog inputs (6) Current/temperature	Analog inputs A0-A7, ADCLO
P10	QEP inputs (3) PWM outputs (2)	Expansion interface header connection (2 x 30)
P11	No connection	CANA DB9 female connector
P12	No connection	RS-232 DB9 female connector
SW1	{1 2 3 4}=[0 0 1 0]	Boot load option switch (set to SPI-A boot)
SW2	{1 2 3 4}=[1 1 0 1] {5 6 7}=[1 1 1]	Processor configuration

A.4 Circuit Schematics

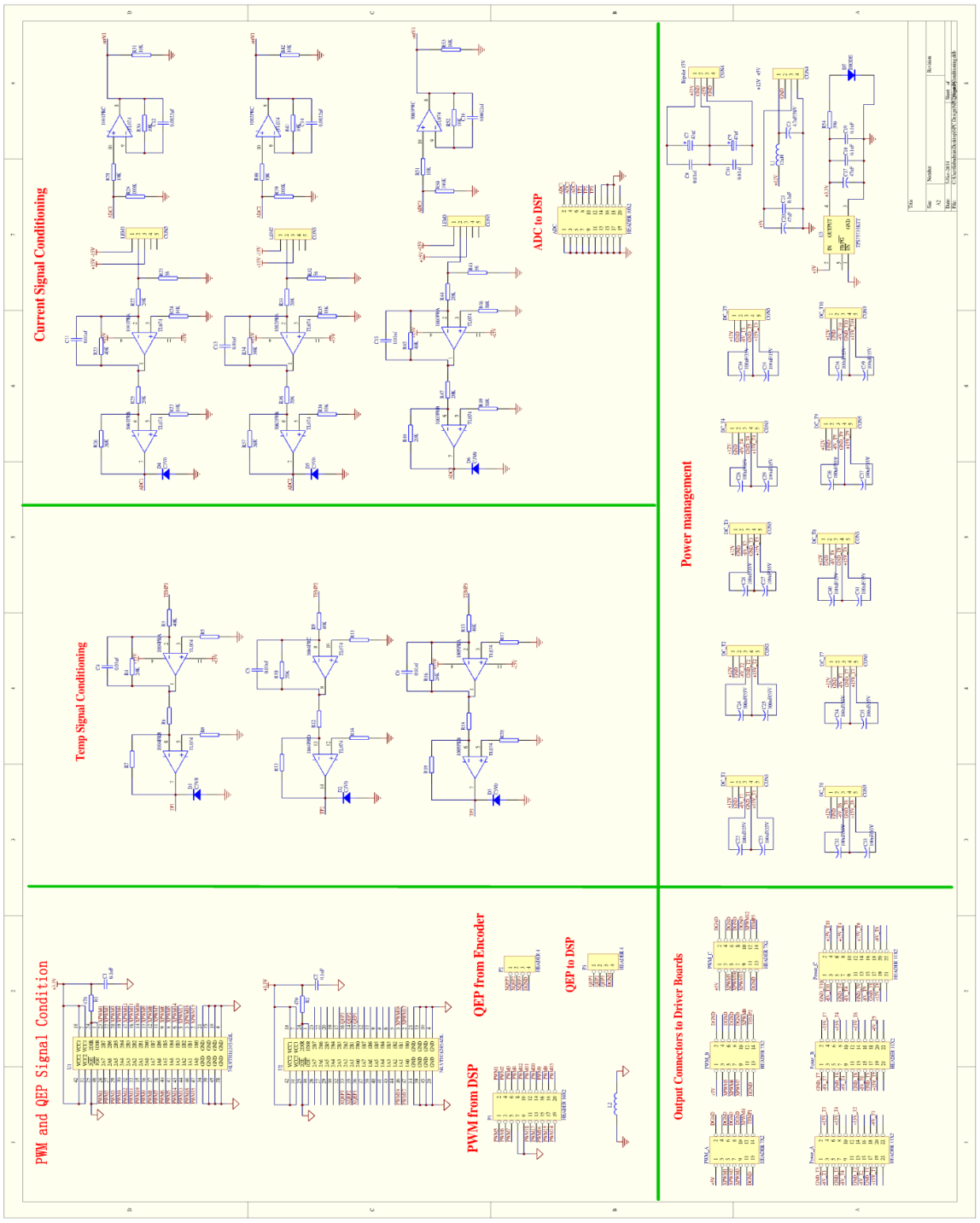

Figure A.4.6.1: Three-level NPC ASD signal conditioning schematic diagram.

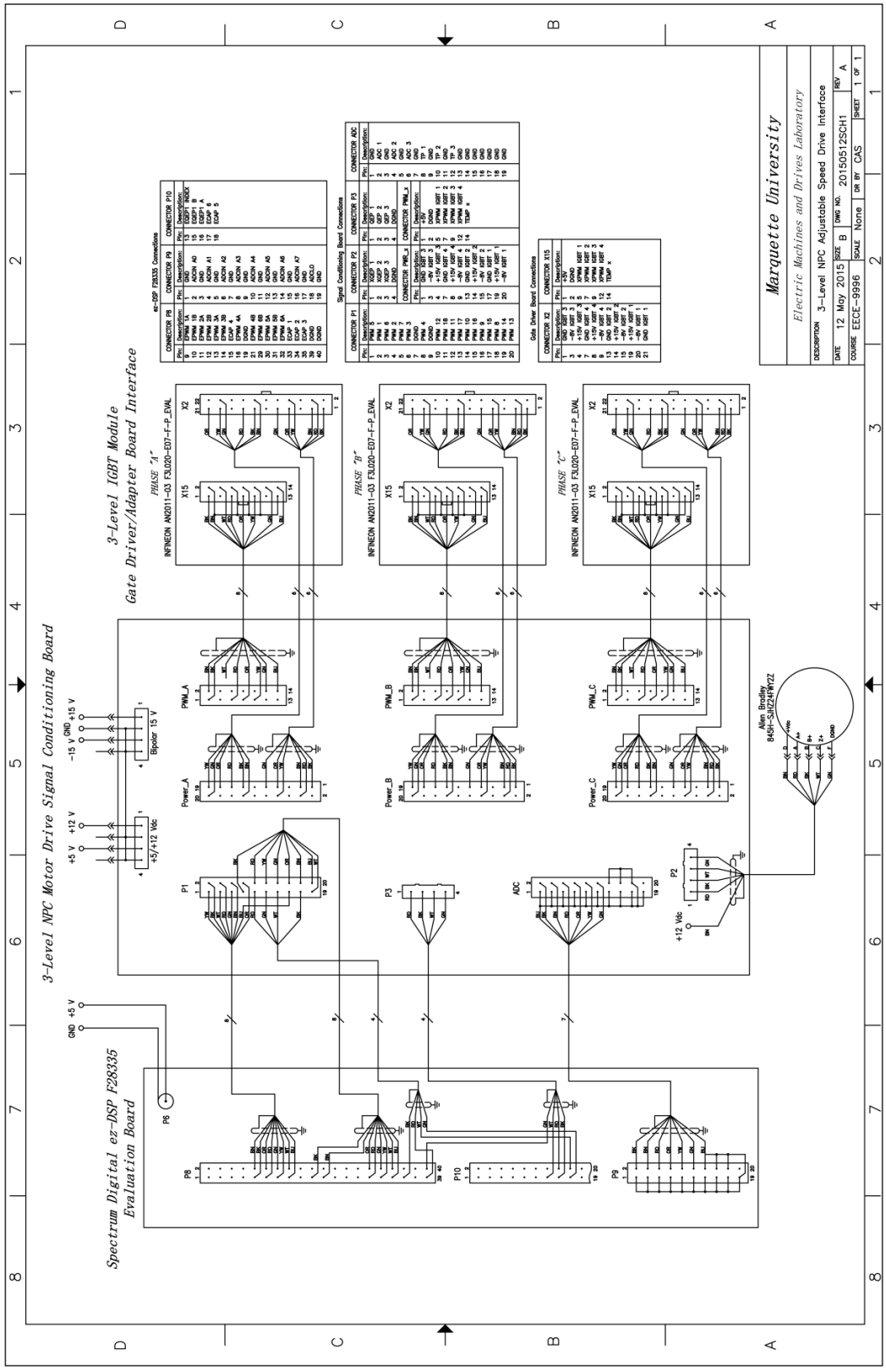

Figure A.4.6.2: Three-level NPC ASD low voltage interface schematic diagram.

B. Circuit Schematic of the Customized Lab-Scale 30-kVA ASD based on the Fault-Tolerant T-Type NPC Inverter

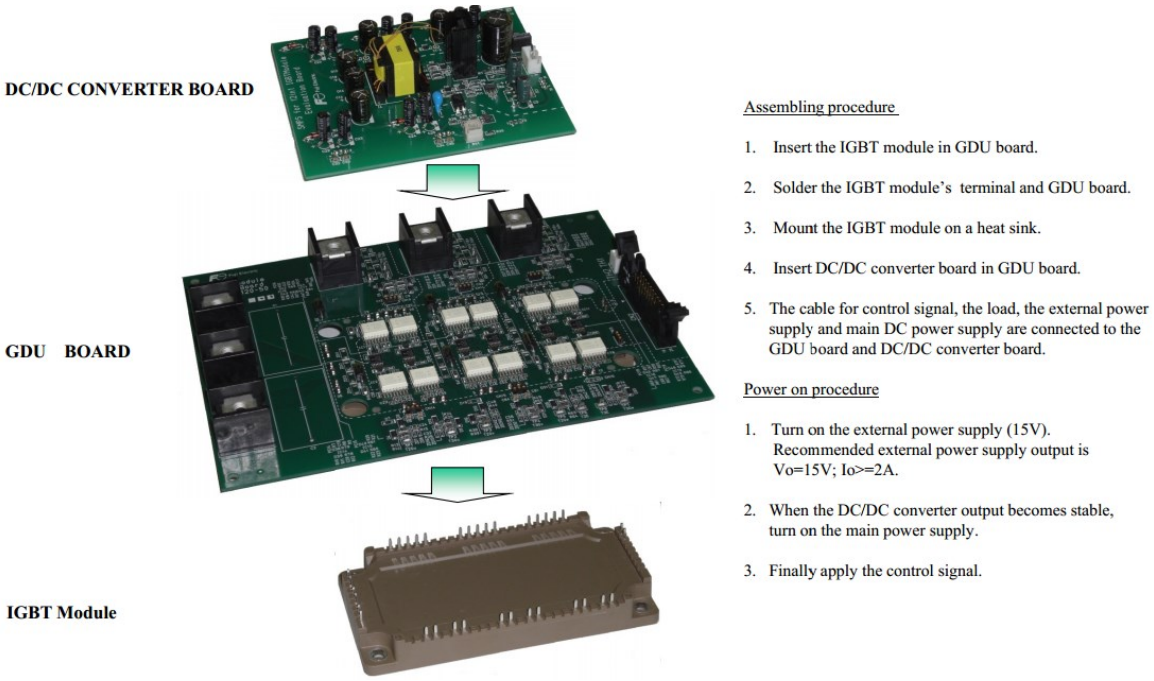

Figure B.1: Power structure of the three-level fault-tolerant ASD.

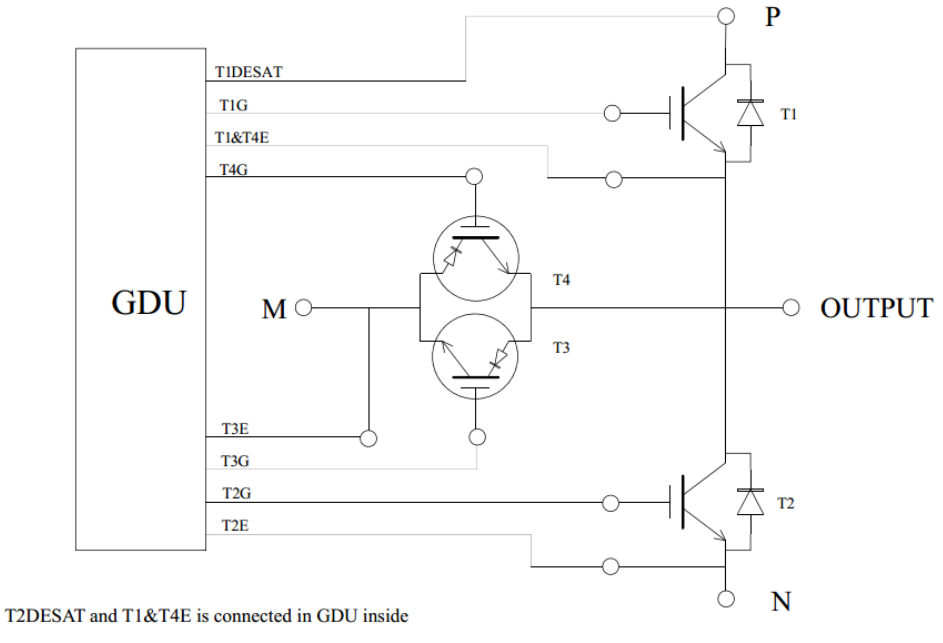

Figure B.2: Power circuit schematic of the three-level T-Type inverter (one leg).

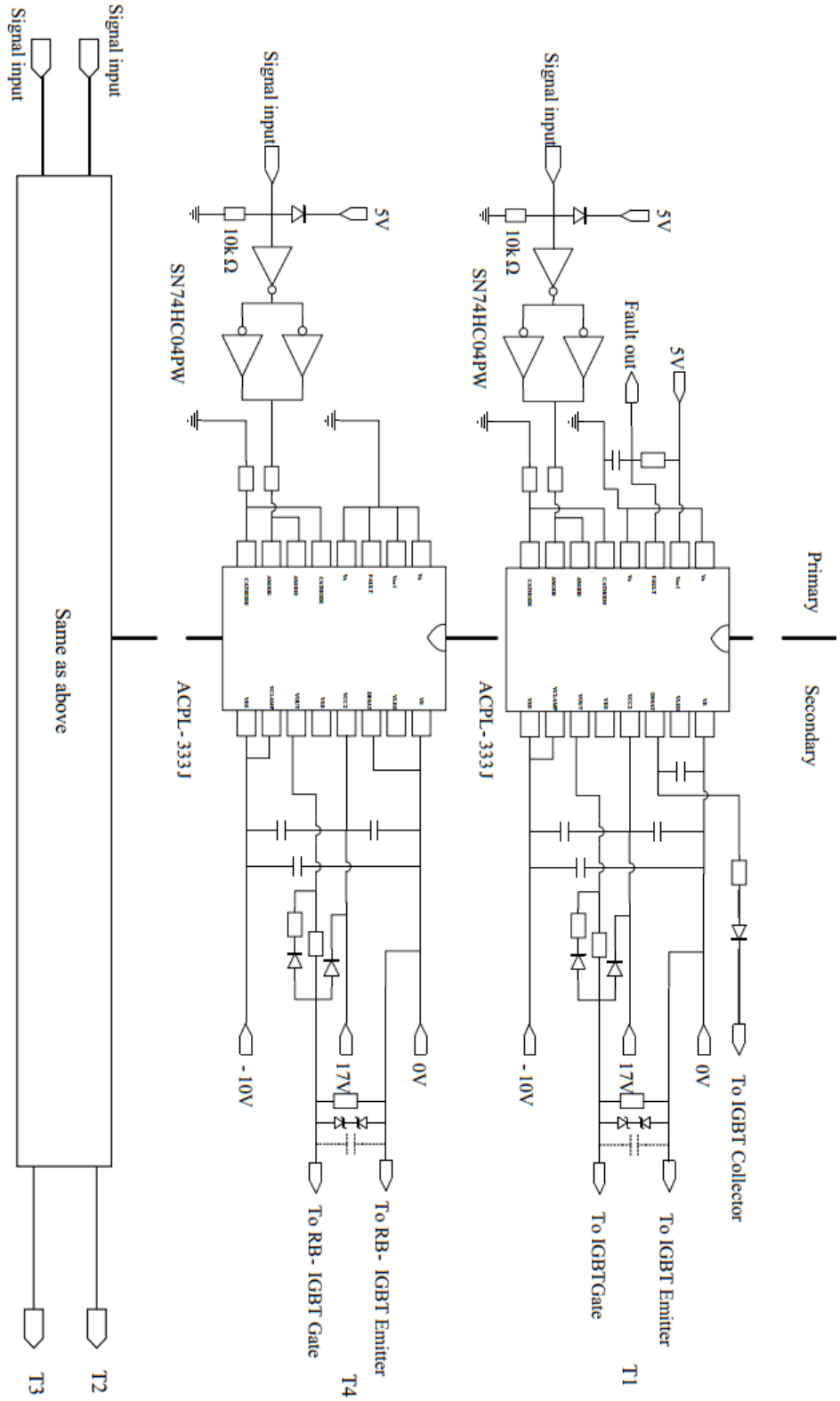

Figure B.3: Schematic of the signal conditioning circuit for the input/output signals for the gate driver board.

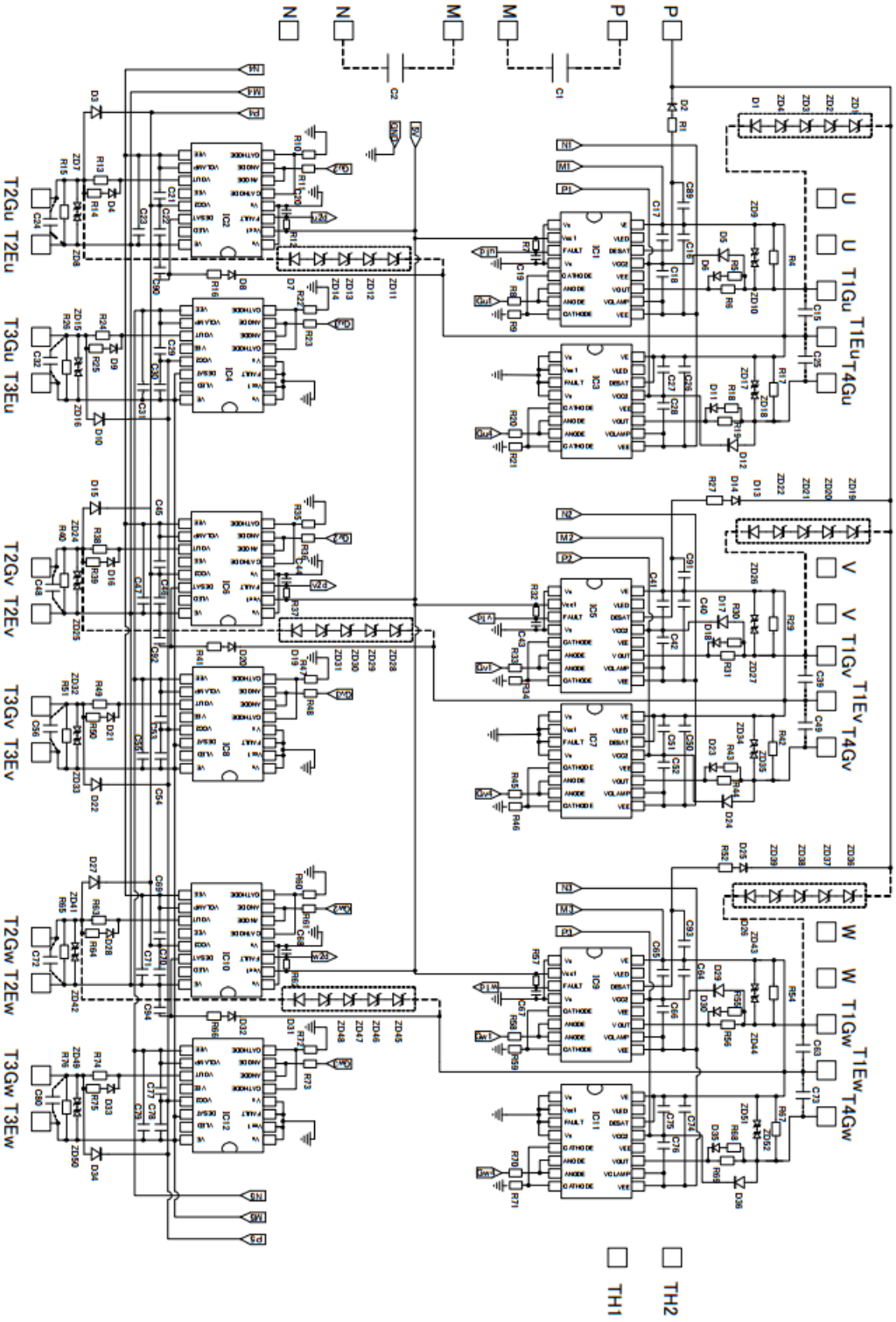

Figure B.4: Circuit schematic of the IGBT gate driver board.

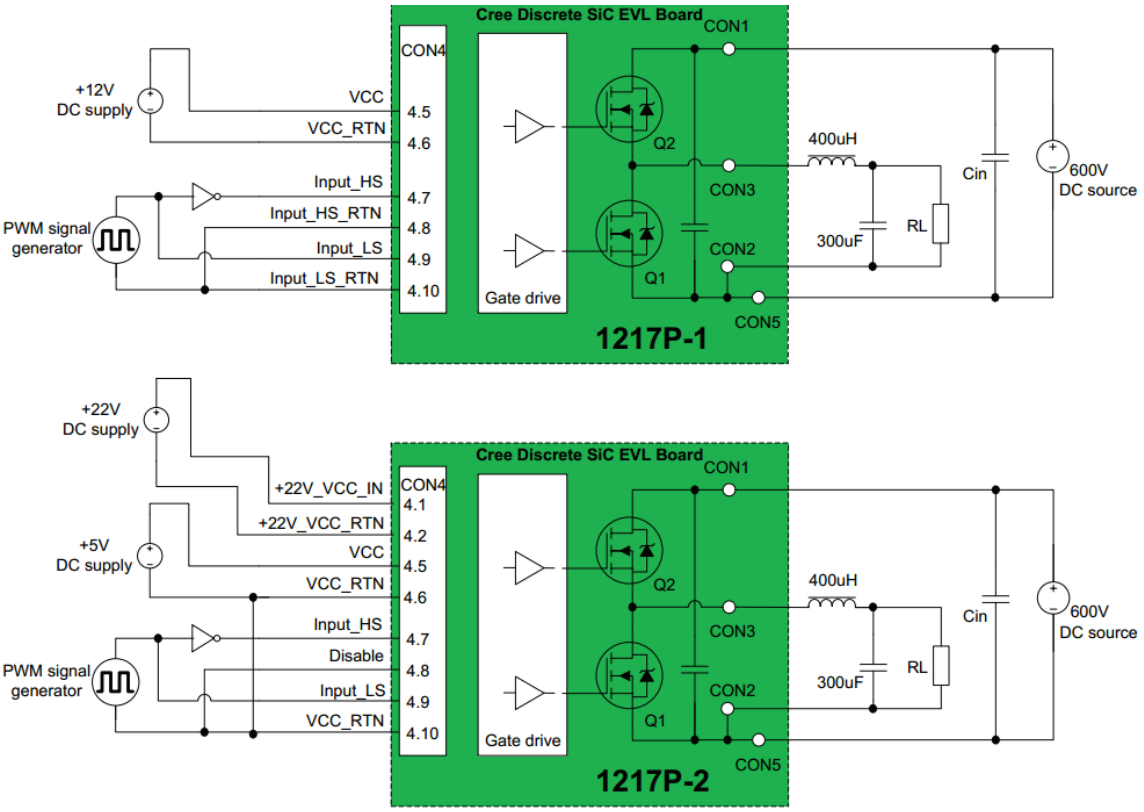

Figure B.5: Circuit schematic of the fourth inverter leg based on SiC MOSFETs in the proposed fault-tolerant T-Type inverter topology.

C. DSP C-Code Programming Used in the Experiments

```
//*****************************************************************
// The following code is for the evaluation of the NDPWM method for the NPC
   inverter operating at low output frequencies.
// Date: September 20, 2015
//*****************************************************************
#include      <math.h>
#include      "PS_bios.h"
typedef float DefaultType;
#define       GetCurTime() PS_GetSysTimer()
interrupt void Task();
DefaultType  fGblV_ref1 = 0;
DefaultType  fGblV_ref2 = 0;
DefaultType  fGblV_ref3 = 0;
DefaultType  fGblCMSignal = 0;
DefaultType  fGblSin = 0;
interrupt void Task()
{
      DefaultType  fSUMP3, fSUMP1, fSUMP4, fMUX21, fCOMP1, fConst1,
fSin4, fSUMP5;
      DefaultType  fMAX_MIN3, f1, fSUMP6, fMAX_MIN4, fSin2, fSin1,
fConst, fSin3;
```

```
        PS_EnableIntr();
{
        static DefaultType wt = 3.14159265 * ((240) / 180.);
        const static DefaultType dwt = (3.14159265 * 2 * (2) / 2000);
        fSin3 = sin(wt);
        wt += dwt;
        if (wt >= 2 * 3.14159265) wt -= 2 * 3.14159265;
        fSin3 *= 0.2;
}
fConst = 1;
{
        static DefaultType wt = 3.14159265 * ((0) / 180.);
        const static DefaultType dwt = (3.14159265 * 2 * (2) / 2000);
        fSin1 = sin(wt);
        wt += dwt;
        if (wt >= 2 * 3.14159265) wt -= 2 * 3.14159265;
        fSin1 *= 0.2;
}
{
        static DefaultType wt = 3.14159265 * ((120) / 180.);
        const static DefaultType dwt = (3.14159265 * 2 * (2) / 2000);
        fSin2 = sin(wt);
        wt += dwt;
        if (wt >= 2 * 3.14159265) wt -= 2 * 3.14159265;
```

```
        fSin2 *= 0.2;
}
fMAX_MIN4 = (fSin1 > fSin2) ? fSin2 : fSin1;
fMAX_MIN4 = (fMAX_MIN4 > fSin3) ? fSin3 : fMAX_MIN4;
fSUMP6 = fConst * (-(1.0)) + fMAX_MIN4 * (-(1.0));
f1 = 1;
fMAX_MIN3 = (fSin1 < fSin2) ? fSin2 : fSin1;
fMAX_MIN3 = (fMAX_MIN3 < fSin3) ? fSin3 : fMAX_MIN3;
fSUMP5 = f1 - fMAX_MIN3;
{
        static DefaultType wt = 3.14159265 * ((0) / 180.);
        const static DefaultType dwt = (3.14159265 * 2 * (30) / 2000);
        fSin4 = sin(wt);
        wt += dwt;
        if (wt >= 2 * 3.14159265) wt -= 2 * 3.14159265;
}
fConst1 = 0;
fCOMP1 = (fSin4 > fConst1) ? 1 : 0;
fMUX21 = (fCOMP1 > 0.5) ? fSUMP5 : fSUMP6;
fSUMP4 = fSin3 + fMUX21;
PS_SetPwm5RateSL(fSUMP4);
fSUMP1 = fSin1 + fMUX21;
PS_SetPwm1RateSL(fSUMP1);
PS_SetPwm2RateSL(fSUMP1);
```

```
        fSUMP3 = fSin2 + fMUX21;
        PS_SetPwm3RateSL(fSUMP3);
        PS_SetPwm4RateSL(fSUMP3);
        PS_SetPwm6RateSL(fSUMP4);
#ifdef _DEBUG
        fGblV_ref1 = fSUMP1;
#endif
#ifdef _DEBUG
        fGblV_ref2 = fSUMP3;
#endif
#ifdef _DEBUG
        fGblV_ref3 = fSUMP4;
#endif
#ifdef _DEBUG
        fGblCMSignal = fMUX21;
#endif
#ifdef _DEBUG
        fGblSin = fCOMP1;
#endif
                PS_ExitPwm5General();
}
void Initialize(void)
{
        PS_SysInit(30, 10);
```

```
        PS_StartStopPwmClock(0);
        PS_InitTimer(0, 0xffffffff);
        PS_InitPwm(5, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 61197);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(5, 1, 0, 1.0/1);
        PS_SetPwmIntrType(5, ePwmNoAdc, 1, 0);
        PS_SetPwmVector(5, ePwmNoAdc, Task);
        PS_SetPwmTzAct(5, eTZHighImpedance);
        PS_SetPwm5RateSL(0);
        PS_StartPwm(5);
        PS_InitPwm(1, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 61197);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(1, 1, 0, 1.0/1);
        PS_SetPwmIntrType(1, ePwmNoAdc, 1, 0);
        PS_SetPwmTzAct(1, eTZHighImpedance);
        PS_SetPwm1RateSL(0);
        PS_StartPwm(1);
        PS_InitPwm(2, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 61197);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(2, 1, (-(1.0)), 1.0/1);
        PS_SetPwmIntrType(2, ePwmNoAdc, 1, 0);
        PS_SetPwmTzAct(2, eTZHighImpedance);
        PS_SetPwm2RateSL((-(1.0)));
        PS_StartPwm(2);
```

```
        PS_InitPwm(3, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 61197);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(3, 1, 0, 1.0/1);
        PS_SetPwmIntrType(3, ePwmNoAdc, 1, 0);
        PS_SetPwmTzAct(3, eTZHighImpedance);
        PS_SetPwm3RateSL(0);
        PS_StartPwm(3);
        PS_InitPwm(4, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 61197);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(4, 1, (-(1.0)), 1.0/1);
        PS_SetPwmIntrType(4, ePwmNoAdc, 1, 0);
        PS_SetPwmTzAct(4, eTZHighImpedance);
        PS_SetPwm4RateSL((-(1.0)));
        PS_StartPwm(4);
        PS_InitPwm(6, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 61197);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(6, 1, (-(1.0)), 1.0/1);
        PS_SetPwmIntrType(6, ePwmNoAdc, 1, 0);
        PS_SetPwmTzAct(6, eTZHighImpedance);
        PS_SetPwm6RateSL((-(1.0)));
        PS_StartPwm(6);
        PS_StartStopPwmClock(1);
}
```

```
void main()
{
        Initialize();
        PS_EnableIntr();   // Enable Global interrupt INTM
        PS_EnableDbgm();
        for (;;) {
        }
}


//*************************************************************
// The following code is for the evaluation of the SVPWM method for the NPC
   inverter operating at low output frequencies.
// Date: June 15, 2015
//*************************************************************
#include      <math.h>
#include      "PS_bios.h"
typedef float DefaultType;
#define       GetCurTime() PS_GetSysTimer()
interrupt void Task();
DefaultType  fGblV_ref1 = 0;
DefaultType  fGblV_ref2 = 0;
DefaultType  fGblV_ref3 = 0;
DefaultType  fGblCMSignal = 0;
```

```
interrupt void Task()
{
    DefaultType  fSUMP3, fSUMP1, fSUMP4, fP2, fSUMP7, fMAX_MIN4,
fMAX_MIN3, fSin2;
    DefaultType  fSin1, fSin3;
        PS_EnableIntr();

    {
        static DefaultType wt = 3.14159265 * ((240) / 180.);
        const static DefaultType dwt = (3.14159265 * 2 * (2) / 2000);
        fSin3 = sin(wt);
        wt += dwt;
        if (wt >= 2 * 3.14159265) wt -= 2 * 3.14159265;
        fSin3 *= 0.2;
    }
    {
        static DefaultType wt = 3.14159265 * ((0) / 180.);
        const static DefaultType dwt = (3.14159265 * 2 * (2) / 2000);
        fSin1 = sin(wt);
        wt += dwt;
        if (wt >= 2 * 3.14159265) wt -= 2 * 3.14159265;
        fSin1 *= 0.2;
    }
    {
```

```
            static DefaultType wt = 3.14159265 * ((120) / 180.);
            const static DefaultType dwt = (3.14159265 * 2 * (2) / 2000);
            fSin2 = sin(wt);
            wt += dwt;
            if (wt >= 2 * 3.14159265) wt -= 2 * 3.14159265;
            fSin2 *= 0.2;
        }
        fMAX_MIN3 = (fSin1 < fSin2) ? fSin2 : fSin1;
        fMAX_MIN3 = (fMAX_MIN3 < fSin3) ? fSin3 : fMAX_MIN3;
        fMAX_MIN4 = (fSin1 > fSin2) ? fSin2 : fSin1;
        fMAX_MIN4 = (fMAX_MIN4 > fSin3) ? fSin3 : fMAX_MIN4;
        fSUMP7 = fMAX_MIN3 + fMAX_MIN4;
        fP2 = fSUMP7 * (-(0.5));
        fSUMP4 = fSin3 + fP2;
        PS_SetPwm5RateSL(fSUMP4);
        fSUMP1 = fSin1 + fP2;
        PS_SetPwm1RateSL(fSUMP1);
        PS_SetPwm2RateSL(fSUMP1);
        fSUMP3 = fSin2 + fP2;
        PS_SetPwm3RateSL(fSUMP3);
        PS_SetPwm4RateSL(fSUMP3);
        PS_SetPwm6RateSL(fSUMP4);
#ifdef _DEBUG
        fGblV_ref1 = fSUMP1;
```

```
#endif
#ifdef _DEBUG
        fGblV_ref2 = fSUMP3;
#endif
#ifdef _DEBUG
        fGblV_ref3 = fSUMP4;
#endif
#ifdef _DEBUG
        fGblCMSignal = fP2;
#endif
                PS_ExitPwm5General();
}

void Initialize(void)
{
        PS_SysInit(30, 10);
        PS_StartStopPwmClock(0);
        PS_InitTimer(0, 0xffffffff);
        PS_InitPwm(5, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 60745);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(5, 1, 0, 1.0/1);
        PS_SetPwmIntrType(5, ePwmNoAdc, 1, 0);
        PS_SetPwmVector(5, ePwmNoAdc, Task);
        PS_SetPwmTzAct(5, eTZHighImpedance);
```

```
        PS_SetPwm5RateSL(0);
        PS_StartPwm(5);

        PS_InitPwm(1, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 60745);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(1, 1, 0, 1.0/1);
        PS_SetPwmIntrType(1, ePwmNoAdc, 1, 0);
        PS_SetPwmTzAct(1, eTZHighImpedance);
        PS_SetPwm1RateSL(0);
        PS_StartPwm(1);

        PS_InitPwm(2, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 60745);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(2, 1, (-(1.0)), 1.0/1);
        PS_SetPwmIntrType(2, ePwmNoAdc, 1, 0);
        PS_SetPwmTzAct(2, eTZHighImpedance);
        PS_SetPwm2RateSL((-(1.0)));
        PS_StartPwm(2);

        PS_InitPwm(3, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 60745);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(3, 1, 0, 1.0/1);
        PS_SetPwmIntrType(3, ePwmNoAdc, 1, 0);
        PS_SetPwmTzAct(3, eTZHighImpedance);
```

```
        PS_SetPwm3RateSL(0);
        PS_StartPwm(3);

        PS_InitPwm(4, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 60745);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(4, 1, (-(1.0)), 1.0/1);
        PS_SetPwmIntrType(4, ePwmNoAdc, 1, 0);
        PS_SetPwmTzAct(4, eTZHighImpedance);
        PS_SetPwm4RateSL((-(1.0)));
        PS_StartPwm(4);

        PS_InitPwm(6, 3, 2000*1, (6E-6)*1e6, PWM_TWO_OUT, 60745);//
pwnNo, waveType, frequency, deadtime, outtype
        PS_SetPwmPeakOffset(6, 1, (-(1.0)), 1.0/1);
        PS_SetPwmIntrType(6, ePwmNoAdc, 1, 0);
        PS_SetPwmTzAct(6, eTZHighImpedance);
        PS_SetPwm6RateSL((-(1.0)));
        PS_StartPwm(6);

        PS_StartStopPwmClock(1);
}
void main()
{
        Initialize();
```

```
        PS_EnableIntr();   // Enable Global interrupt INTM
        PS_EnableDbgm();
        for (;;) {
        }
}
```