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Novel Design of a Wideband Ribcage-Dipole Array and its Feeding Network

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NOVEL DESIGN OF A WIDEBAND RIBCAGE-DIPOLE ARRAY AND ITS FEEDING NETWORK

by

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Abstract

In this thesis the focus was on the design, fabrication, and tests of the feeding networks individually and within an array system. The array feeding network is a corporate-fed type utilizing equal-split, stepped-multiple sections of the conventional Wilkinson power divider in microstrip form with a unique topology. The feeding network was specifically designed for a broadside relatively small linearly-polarized wideband UHF non-scanning array for directed power applications that uses an array radiator with a new volumetric ribcage dipole configuration. The array has a large impedance bandwidth and consistent front lobe gain over the wide frequency band. Theoretical and experimental results describing the performance of the array feeding network and the array are presented and discussed.

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1. Introduction

The use of three-port power dividers is especially important for antenna array systems that utilize a power-splitting network, such a corporate or parallel feed system. The corporate feed is simply a device that splits power between *n* output ports with a certain distribution while maintaining equal path lengths from input to output ports. It can be implemented with n-way power splitters where three-port power dividers are commonly used. The flexibility of the two-way divider's feed structure allows use of multiple stepped-sections to achieve power division with the capability of wideband operation. The bandwidth is primarily limited by the match of the radiating elements, although using high-isolation power dividers reduces the dependence on the match of the loads.

The history of the three-port power divider began in 1960 when Wilkinson [1] described a device that separated one signal into *n* equal signals of equal phase and amplitude. Theoretically perfect isolation between all output ports was achieved at one center frequency. In 1965, hybrid with arbitrary amplitude difference of the output signals was presented by Parad and Moynihan [2]. A perfect three-port hybrid property was again achieved at one frequency. In 1968, Cohn [3] presented a class of equal-power dividers with isolation and matching at any number of frequencies. Further, in 1971 Ekinge [4] described three-port hybrids made up of *n* sections in cascade, where each section is composed of two coupled lossless transmission lines of electrical length Φ and an intermediate isolation resistor. The analysis of both Ekinge and Cohn were similar. However the difference was that Cohn considered the equal power-split three-port hybrid, while Ekinge discussed the three-port hybrid of an arbitrary number of splits. Since that time, research on three-port hybrids has continued.

One limitation of the corporately fed array is space usage that the feeding network requires. The designer is often faced with challenge of choosing a topology for the 2-way divider that reduces the total size of the feeding network layout and also avoids the coupling between the two impedance transformers. Therefore, careful optimization of the individual 2-way power divider topology needs be included in the design of the feeding network.

The main objective of this thesis is to design, investigate, and analyze a corporate feeding network of custom Wilkinson power dividers that can be used with any arbitrary radiator in an antenna array. Although the corporate-fed network can be used for any type of radiator, a new type of volumetric radiator [5] is investigated that provides improved gain and bandwidth.

Part 1:

Wilkinson divider design of an array corporate fed-network

2. Problem statement

2.1. Goal

The goal of Part 1 of this thesis is to analyze and design an equal-split Wilkinson power divider using stepped multiple sections of the conventional Wilkinson divider to achieve 2:1, 4:1, and 8:1 power division. The microstrip design was optimized for operation over the UHF band, specifically 0.5-1 GHz, and utilized in a corporate-feeding network for an antenna array. Further, the designs were fabricated from low-cost materials but have the capability for use in high power applications using enhanced components.

2.2. Approach

The design approach builds from three-port network theory and derivation of scattering parameters of the Wilkinson divider, and then investigates different microstrip topologies using Agilent ADS and Ansoft HFSS simulation software for design optimization. Microstrip design considerations are also discussed especially in relation to the choice of an appropriate substrate for fabrication. The experimental results for the design prototype are also shown and discussed.

2.3. Expected results

The return loss, insertion loss, coupling, and isolation between ports were evaluated to determine the optimized final design. A minimal return loss of -10 dB or better over the band and isolation between output ports is a critical design requirement. Also, approximately -3 dB coupling (half of the power) between input and output ports for each stage is anticipated. The frequency response of the 4:1 and 8:1 dividers is expected to have a wider bandwidth than seen in the 2:1 Wilkinson resulting from the use of additional cascaded 0.25λ sections.

3. Introduction and background

3.1. Three-port networks

Three-port network power dividers with one input and two outputs have a scattering matrix with the following nine independent elements:

$$[S]=\begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \quad (1)$$

For reciprocal networks the [S] matrix is symmetric and $(S_{ij} = S_{ji})$. Ideally, to avoid any loss of power, the network would be lossless and matched at all ports. When all ports are matched $(S_{ii} = 0)$ and the reciprocal matrix reduces to [6]

$$[S]=\begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{21} & 0 & S_{23} \\ S_{31} & S_{32} & 0 \end{bmatrix} \quad (2)$$

3.2. Ideal network assumption

Following the analysis in [7], for the lossless network the scattering matrix is unitary and leads to

$$
\begin{aligned}
&S_{12}S_{12}^{*}+S_{13}S_{13}^{*}=|S_{12}|^{2}+|S_{13}|^{2}=1\\
&S_{21}S_{21}^{*}+S_{23}S_{23}^{*}=|S_{21}|^{2}+|S_{23}|^{2}=1\\
&S_{31}S_{31}^{*}+S_{32}S_{32}^{*}=|S_{31}|^{2}+|S_{32}|^{2}=1
\end{aligned}
\tag{3}
$$

$$
\begin{aligned}
&S_{13}^{*}S_{23}=0\\
&S_{23}^{*}S_{12}=0\\
&S_{12}^{*}S_{13}=0
\end{aligned}
\tag{4}
$$

Which results in

$$
\begin{aligned}
&S_{12}\neq 0\\
&\rightarrow S_{13}S_{12}^{*}=0\rightarrow S_{13}=0\\
&\rightarrow S_{23}^{*}S_{12}=0\rightarrow S_{23}=0
\end{aligned}
\tag{5}
$$

This asserts that $|S_{13}|^{2}+|S_{23}|^{2}=0$ and therefore contradicts $|S_{31}|^{2}+|S_{32}|^{2}=1$. If the three-port network is allowed to be lossy it can be reciprocal and matched at all ports.

3.3. Passive three-port power dividers (advantages and disadvantages)

Three commonly used passive three-port power dividers are the T-junction divider, the resistive divider, and the Wilkinson divider. The advantages and disadvantages of these three dividers are summarized in Table 3 below [7].

Table 1: Comparison of passive power dividers.

Passive power divider	Advantage	Disadvantage
T-junction	• Lossless	• Not matched at all ports • No isolation between output ports
Resistive	• Can be matched at all ports	• No isolation between output ports • Poor power handling, limited by resistor tolerances • Lossy
Wilkinson	• Lossless (if matched at all ports) • High isolation	• Reflected power is dissipated through isolation resistor if mismatched

The Wilkinson divider can meet the ideal three-port network conditions (if it is matched at all ports) being lossless, reciprocal, matched. Therefore, the Wilkinson divider is the best choice in the above comparison and will be used in the optimized design of the corporate-fed network for the array.

4. Wilkinson divider theory

4.1. Transmission line circuit

The Wilkinson power divider is a three-port network that is lossless when the output ports are matched; where only reflected power is dissipated. Input power can be split into two or more in-phase signals with the same amplitude. For a two-way Wilkinson divider using $\lambda/4$ impedance transformers having a characteristic impedance of $\sqrt{2}Z_0$ and a lumped isolation resistor of $2Z_0$ with all three ports matched, high isolation between the output ports is obtained [1]. The design of an equal-split (3 dB) Wilkinson is often made in stripline or microstrip form; all designs considered in this thesis are microstrip, as shown below in Fig. 1(a). The equivalent transmission line circuit is shown in Fig. 1(b).

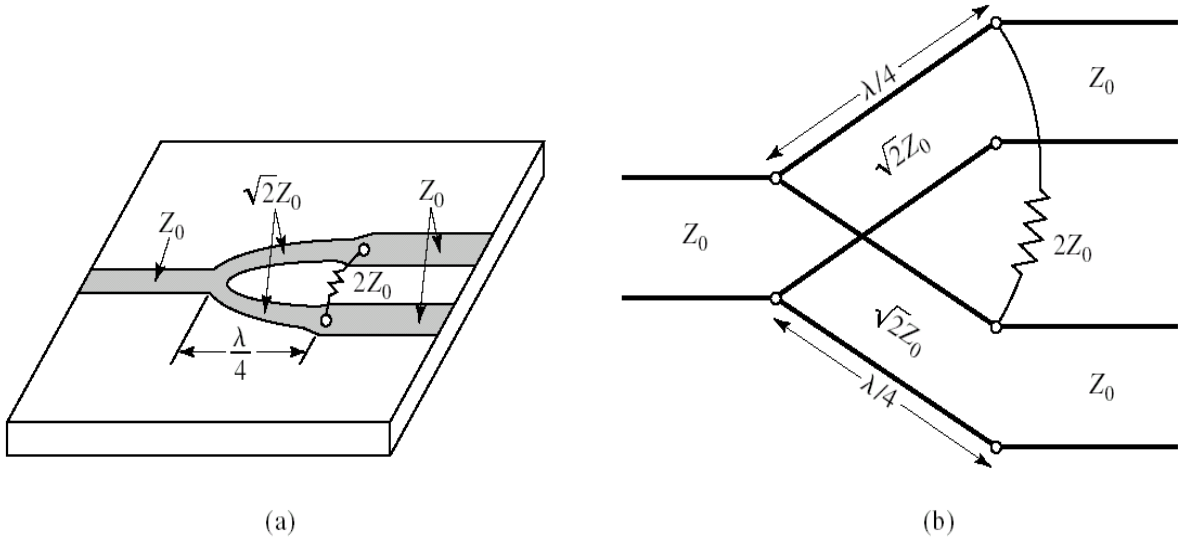

Fig. 1: The Wilkinson power divider taken from [7]. (a) An equal-split Wilkinson power divider in microstrip form. (b) Equivalent transmission line circuit.

Design for center frequency of 0.75 GHz and $Z_0 = 50\Omega$ requires the isolation resistor to be $2Z_0 = 100\Omega$ and the impedance of the quarter-lambda transmission line split section to be $\sqrt{2}Z_0 = 70.7\Omega$.

4.2. Derivation of scattering parameters

The S-parameter matrix for the Wilkinson power divider can be found using even-odd mode analysis which uses circuit symmetry and superposition [7]. As a first step the circuit in Fig. 1(b) is redrawn with all impedances normalized to the character impedance Z_0 and redrawn as shown in Fig.2.

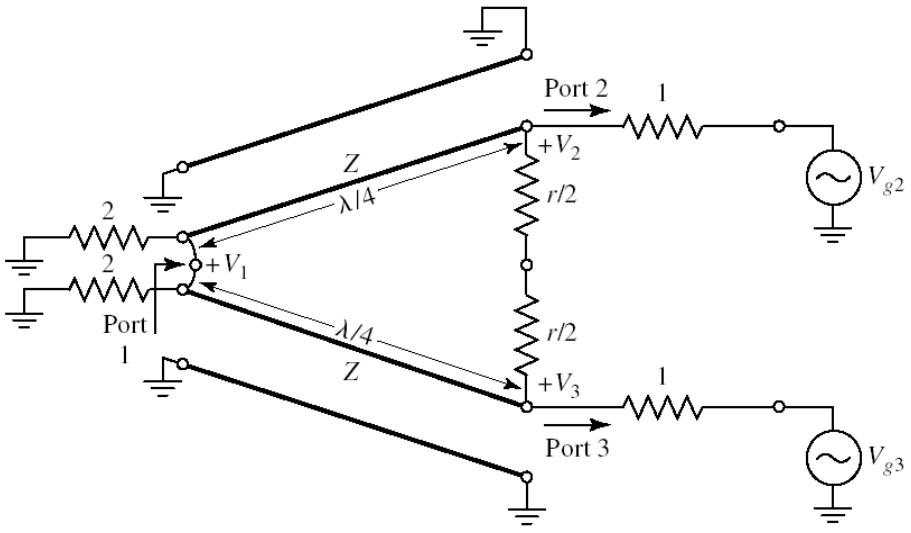

Fig. 2: The Wilkinson power divider circuit taken from [7] in normalized and symmetric form.

There is no current flow between the *r*/2 resistors or the short circuit between the inputs of the two transmission lines at port 1. Therefore the circuit above can be bisected and separated into two systems, even and odd (Fig. 3 (a) and (b) respectively). Each system can be then analyzed separately.

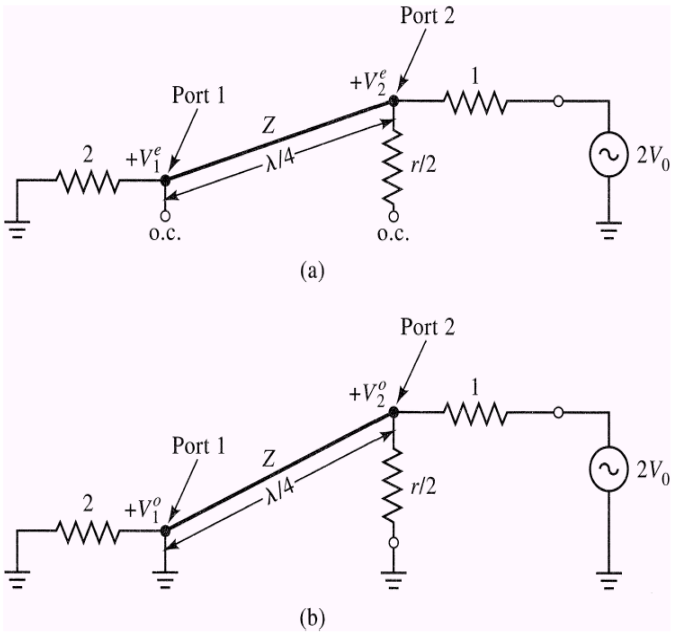

Fig. 3: Bisection of the circuit of Fig. 2 taken from [7]. (a) Even-mode excitation. (b) Odd-mode excitation.

4.2.1. Even-mode analysis

First the input impedance at Port 2 of the circuit in Fig. 3 (a) is checked where $Z = \sqrt{2}$

$$Z_{in}^{e} = \frac{\sqrt{2}^{2}}{2} = 1\,(matched) \tag{6}$$

Then voltages at port 2 and port 1 are found

$$V_2^e = jV^+(1-\Gamma) = V_0$$
$$V_1^e = V^+(1+\Gamma) = jV_0\frac{\Gamma+1}{\Gamma-1} \quad (7)$$

$$\Gamma = \frac{2-\sqrt{2}}{2+\sqrt{2}} \quad (8)$$
$$V_1^e = -jV_0\sqrt{2}$$

4.2.2. Odd-mode analysis

The input impedance at port 2 of Fig. 3 (b) is found again as

$$Z_{in}^o = \frac{\sqrt{2}^2}{2} = 1\,(matched) \quad (9)$$

Voltages at port 2 and port 1 are

$$V_2^o = V_0$$
$$V_1^0 = 0\,(virtual\ ground) \quad (10)$$

The S11 in the circuit shown below in Fig. 4 (a) and its bisection (b) are used.

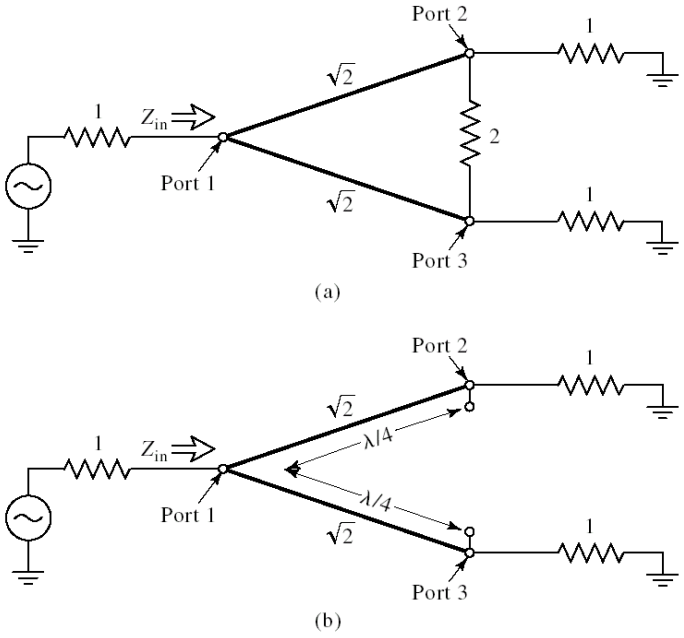

Fig. 4: Analysis of the Wilkinson divider (from [7]) to find S11. (a) Terminated Wilkinson divider. (b) Bisection of the circuit in (a).

When ports 2 and 3 are terminated with matched loads, there is no current flow through the normalized isolation resistor and it can be removed. The input impedance at port 1 is then

$$Z = \frac{\sqrt{2}^2}{2} = 1 \tag{11}$$

4.2.3. Summary of scattering parameters

The S-parameters are thus:

$$S_{11} = 0 \qquad Z_{in} = 0 \text{ at port 1} \quad (12)$$

$$S_{22} = S_{33} = 0 \qquad \text{Output matched for even/odd modes} \quad (13)$$

$$S_{12} = S_{21} = \frac{V_1^e + V_1^o}{V_2^e + V_2^o} = -j/\sqrt{2} \qquad \text{symmetry due to reciprocity} \quad (14)$$

$$S_{13} = S_{31} = -j/\sqrt{2} \qquad \text{symmetry of ports 2 and 3} \quad (15)$$

$$S_{23} = S_{32} = 0 \qquad \text{due to short or open at bisection} \quad (16)$$

Therefore, the S-matrix can be written as:

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & j \\ j & 0 & 0 \\ j & 0 & 0 \end{bmatrix} \quad (17)$$

4.3. Figures of merit

The performance of the Wilkinson divider/coupler is commonly evaluated by the following figures of merit [8]:

$$RL_1[dB] = -20\log|S_{11}| \; and \; RL_2[dB] = -20\log|S_{22}| \quad \text{return loss at ports 1 and 2} \quad (18)$$

$$CP_{12}[dB] = -20\log|S_{12}| \quad \text{coupling between ports 1 and 2} \quad (19)$$

$$IL_{23}[dB] = -20\log|S_{23}| \quad \text{isolation between ports 2 and 3} \quad (20)$$

4.4. Frequency response of an equal-split divider

The frequency response of the equal-split Wilkinson divider is shown in Fig. 5 below. The figures of merit discussed in the previous section are shown over the band from 0.5 to 1 GHz, return loss, isolation, and coupling.

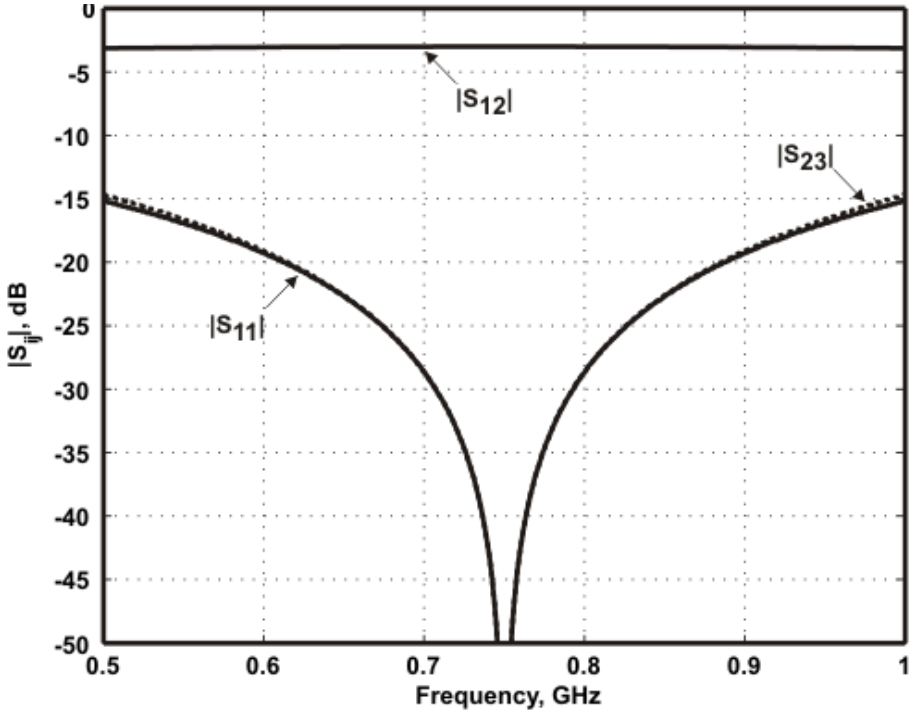

Fig. 5: Frequency response of an equal-split Wilkinson power divider.

The above plot was generated in Agilent ADS using ideal transmission line components to model the Wilkinson divider. The frequency response over the band 0.5-1 GHz has -3dB coupling and return loss and isolation approaching negative infinity at center frequency which coincides with the Wilkinson S-matrix previously derived.

5. Microstrip design considerations

There are some important design considerations when choosing an appropriate material for the microstrip substrate. The important factors are size, higher-order modes, surface wave effects, dielectric loss, and power handling (such as dielectric strength and thermal conductivity).

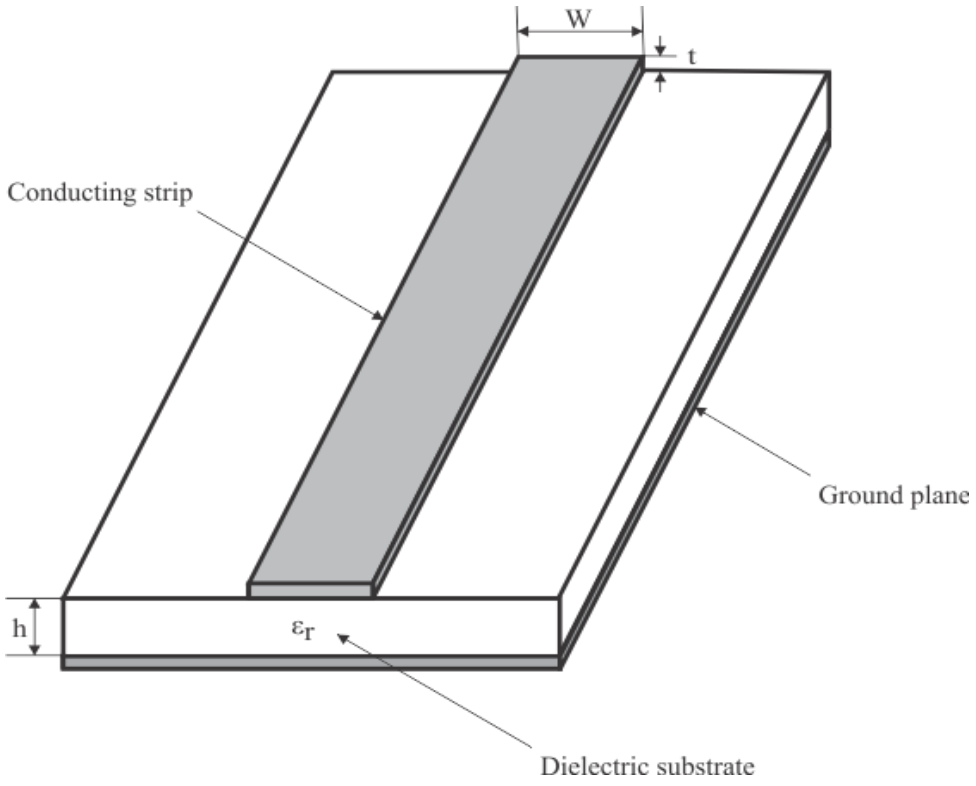

Fig. 6: Diagram of a microstrip line.

5.1. Topology

At lower frequencies such as L-band and below, size can become significant as lambda becomes large. Therefore, a topology that reduces the substrate area is beneficial. In the design of the Wilkinson divider, three topologies for the quarter-lambda split transmission line section were considered: the conventional straight split section, a circular split section, and an elliptical split section. The elliptical split transmission line design reduces the size the most but requires close spacing between transmission lines in the quarter lambda section. Because the close spacing of the lines did not allow them to be sufficiently decoupled from each other, this topology was rejected, though the use of coupled lines in the design of Wilkinson dividers by calculation of even and odd mode impedances has been investigated by [9]. The circular and straight line quarter lambda split sections are shown in Fig. 7 below. These two topologies will be compared in simulation.

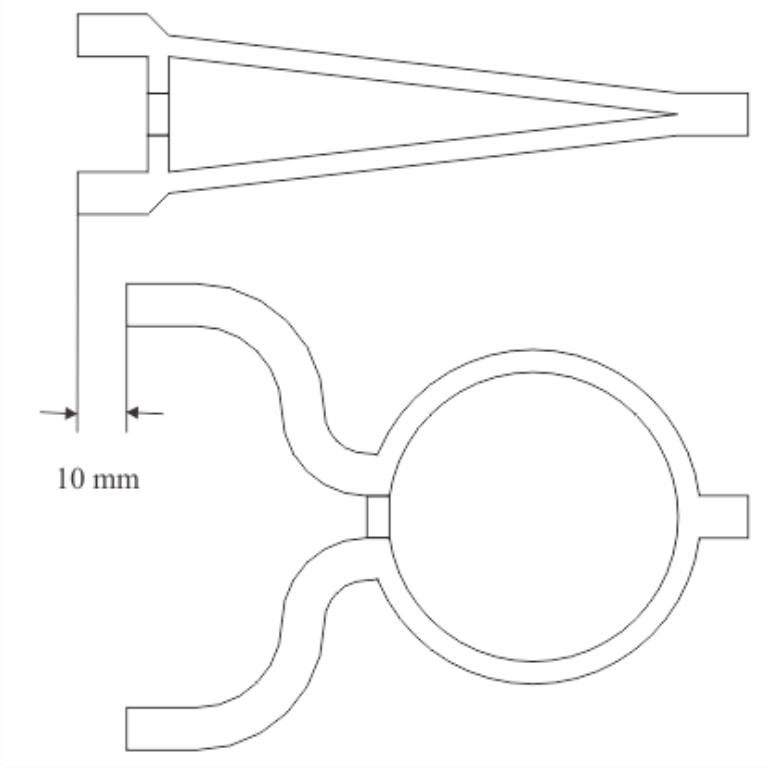

Fig. 7: Straight split design vs. circular split the circular design reduces size by 10 mm in length and width of substrate.

At a design center frequency of 0.75 GHz, the size of the substrate is approximately 90 mm x 90 mm when using the circular split design. In comparison to the 100 mm x 100 mm straight split design, this is a size reduction of 10 mm in the length and width of the substrate. This size reduction can be improved by further optimization.

5.2. Higher-order modes

To avoid excitation of higher-order modes in a microstrip the operating frequency used in design should be kept below the cutoff frequency for the first higher-order mode. The expression for cutoff frequency in a microstrip line is given as [10]

$$f_c = \frac{c}{\sqrt{\varepsilon_r}\left(2W + 0.8h\right)} \tag{21}$$

The following plot of Fig. 8 shows the curves of cutoff frequency versus microstrip substrate thickness for three common substrates, Teflon, Rogers Duroid 6002 , and FR-4. Microstrip trace widths of 1 mm, 3 mm and 6 mm were chosen, 6 mm being the widest trace used in the Wilkinson divider design corresponding to the 50Ω impedance strip.

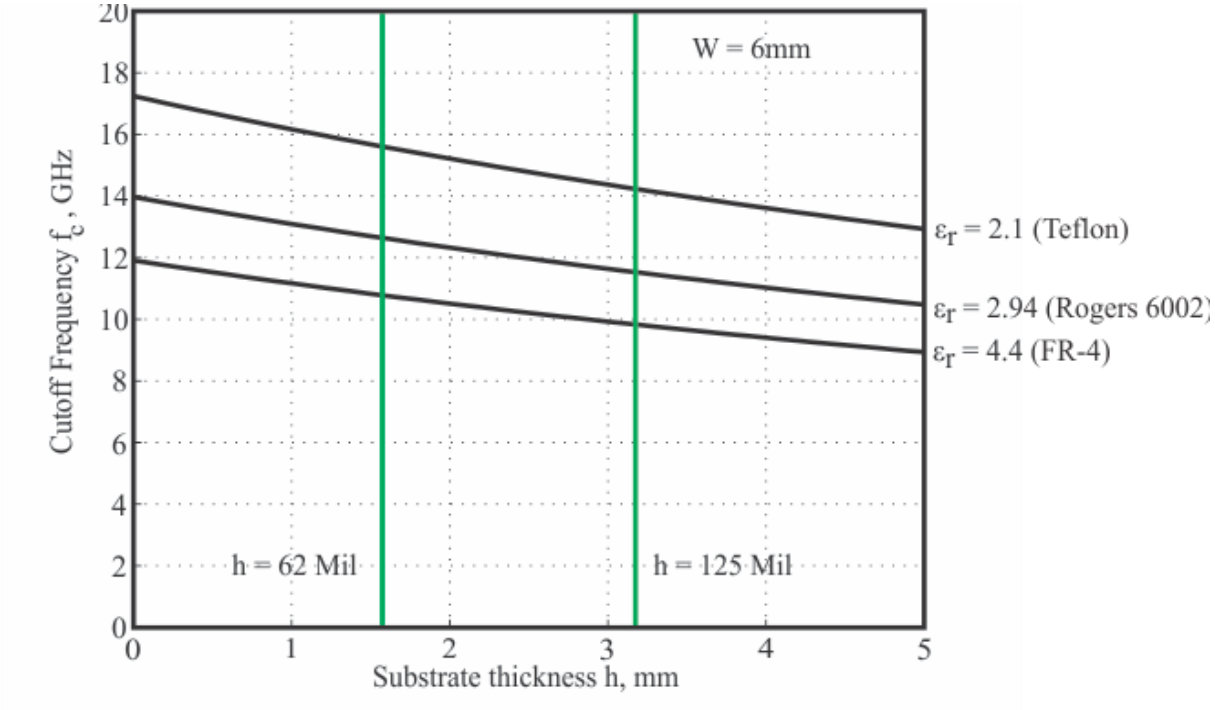

Fig. 8: Cutoff frequency versus substrate thickness for three substrate materials, Teflon, Rogers Duriod 6002, and FR-4. The microstrip trace width is 6 mm (50Ω impedance).

The cutoff frequency of the first higher-order mode does not appear until 10 GHz and above for a 125 mil thickness substrate of any of the three materials shown. The highest frequency used in the Wilkinson design is 1 GHz, which is far below the limitation of 10 GHz. FR-4 could be chosen since it is commonly used in printed circuit board fabrication and is a low cost substrate. The figure below shows the cutoff frequency of the first higher-order mode for the microstrip trace widths of 1 mm, 3 mm, and 6 mm of FR-4.

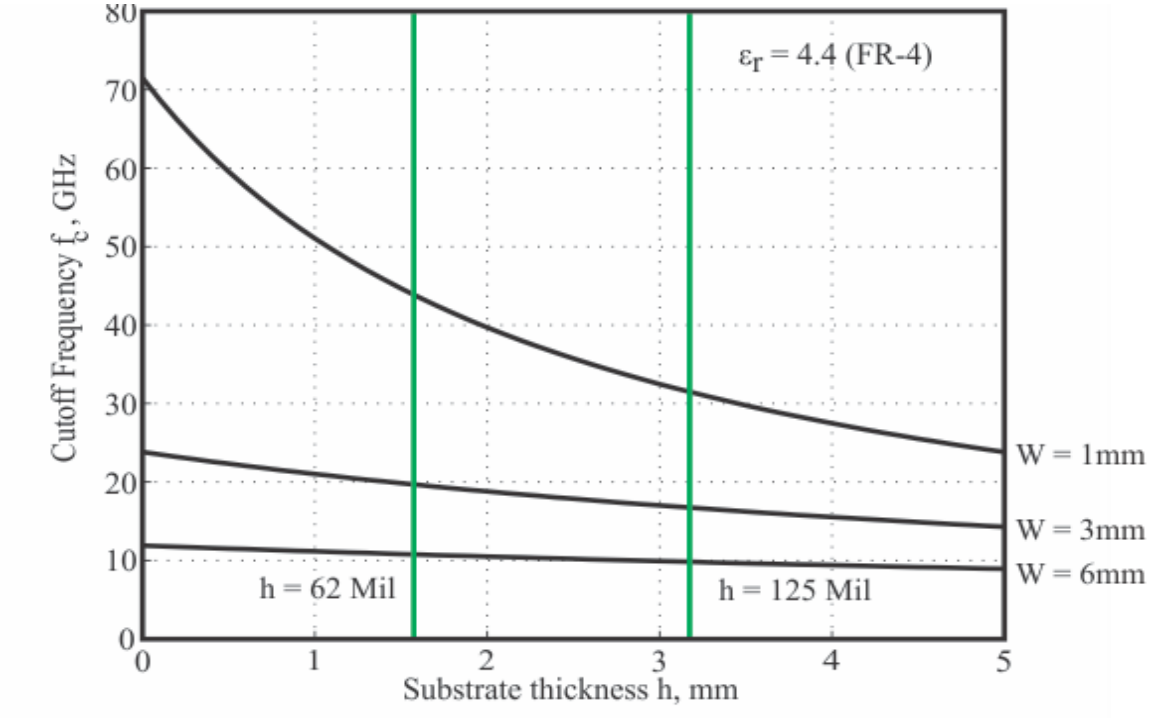

Fig. 9: Cutoff frequency versus substrate thickness for three microstrip trace widths, 1 mm 2 mm, and 3 mm of FR-4, microstrip trace width of 6 mm (50Ω impedance).

5.3. Surface waves

The next microstrip design consideration is the lowest surface wave mode coupling to the quasi-TEM mode of the microstrip, which becomes significant at the threat frequency given by [10]:

$$f_s = \frac{c \tan^{-1} \varepsilon_r}{\sqrt{2}\pi h \sqrt{\varepsilon_r - 1}} \tag{22}$$

At this frequency the phase velocities of the two modes are close. The threat frequency versus substrate thickness for the same three materials considered in the previous section, Teflon, Rogers Duriod 6002, and FR-4, is shown in Fig. 10. The widest microstrip trace width (50Ω impedance) is again used.

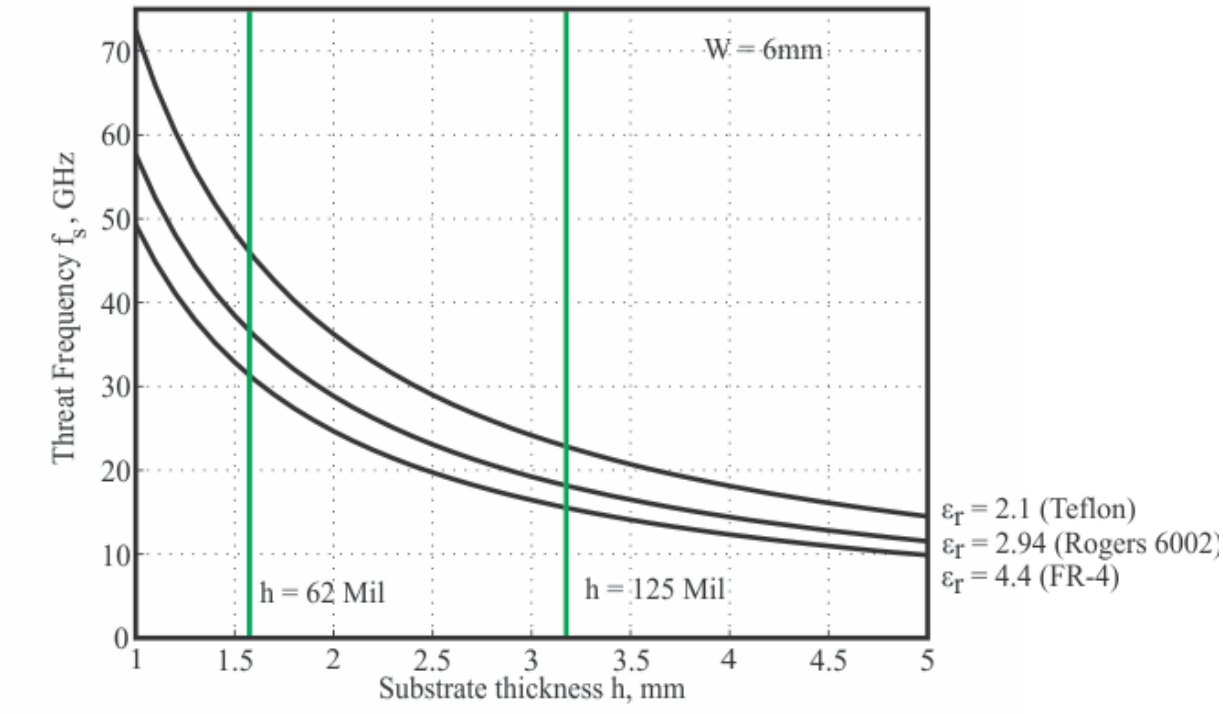

Fig. 10: Threat frequency versus substrate thickness for the lowest surface wave mode coupling to the quasi-TEM mode for the three materials, Teflon, Rogers Duroid 6002, and FR-4. The

maximum microstrip trace width in the Wilkinson design of 6 mm was used (50Ω trace impedance).

Threat frequency at 125 mils thick substrate is above 15 GHz. As before when considering excitement of higher-order modes the design frequency of 1 GHz, it is well below the threat frequency. As a rule of thumb, the lower bound between the cutoff frequency of the first higher-order mode and the threat frequency for surface wave coupling to the quasi-TEM mode is selected for the maximum allowable operating frequency of design. All three of the substrate materials are acceptable for design. Although lossy, FR-4 is the most common and readily available material for printed circuit board fabrication and also low cost. Therefore, it has been chosen as the microstrip substrate material for this Wilkinson power divider design. The MATLAB script computing the effects of higher order modes and surface wave affects is included in Appendix I.

5.4. Losses

There are three types of losses that are considered when designing a microstrip line: conductor loss, dielectric loss, and radiation loss. Magnetic losses play a role in magnetic substrates such as ferrites and are not presented. The following expressions are used to approximate the conductor loss and dielectric loss [11].

$$Q_C \propto \pi\left(\frac{h}{\lambda}\right)\cdot\left(\frac{377\,\Omega}{R_s}\right) \tag{23}$$

$$Q_d \propto \frac{1}{\tan\delta} \tag{24}$$

The total Q-factor can be expressed as a sum of the component Q factors and are inversely proportional to resistance. The total loss is the inverse total Q:

$$\frac{1}{Q_t} = \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_r} \tag{25}$$

In the Wilkinson divider design, the most significant loss will be the dielectric-induced loss of FR-4, which is inversely proportional to the loss tangent. The loss tangent of FR-4 is approximately 0.02 much higher than low loss substrates such as Teflon which has a loss tangent of 0.001. FR-4 is commonly used due to its low cost, that makes it a good choice for use in a prototype corporate feeding network.

5.5. Power handling

High-power capability in microstrip design depends on both peak power handling capacity and average power handling capacity of the microstrip line. The peak power is proportional to the breakdown voltage of the substrate (dielectric breakdown). The peak power handling capacity is given as [12]:

$$P_{PEAK} \propto \frac{V_0^2}{2Z_c} \tag{26}$$

which is proportional to the square of the dielectric breakdown voltage and inverse of twice the characteristic impedance of the line. FR-4 has a dielectric breakdown voltage of approximately 75 kV for 125 mil thickness (Appendix II: Data sheets). Given that the highest impedance in the Wilkinson design is 70.7Ω for the quarter-lambda split section, the peak power handling is quite sufficient for design specifications. A 64-element antenna array is powered by delayed pulses so the average power to the feeding network is within the average power handling capability of the microstrip. A detailed coverage of average power handling capacity is shown in [13] and MATLAB script following the methodology described there is used to calculate the average power handling capacity for FR-4 for different temperatures (Appendix I: Microstrip average power handling). The limiting factor is not be the microstrip, but the N-type connectors: most available connectors are rated at 10 kW peak power and 0.6 kW average power.

6. Numerical simulation

Ansoft HFSS version 12 and Agilent ADS 2009 were used to simulate the 2:1, 4:1, and 8:1 Wilkinson power dividers. Comparison of simulation results between numerical solvers allowed for verification of design performance. All simulations in Ansoft HFSS were run on a 48-processor server which aided the optimization of design topology. Two design topologies were simulated for the 2:1 divider, the straight quarter-lambda split section and the circular quarter-lambda split section.

6.1. 2:1 divider simulation results (straight design)

The straight quarter-lambda split section 2:1 divider is being the conventional Wilkinson divider design was modeled first. Figures 11 and 12 show the 2:1 model in ADS and HFSS.

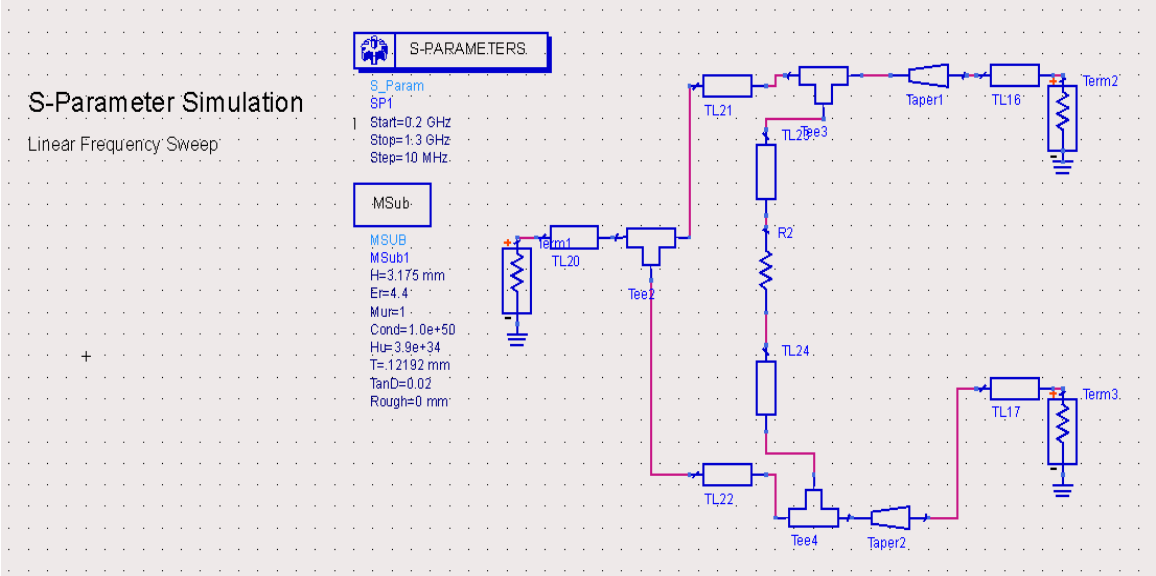

Fig. 11: ADS transmission line model of 2:1 Wilkinson divider (straight quarter-lambda split section).

The ADS model shown in Fig. 11 is matched terminated to 50Ω at all ports. The microstrip transmission line segments are chosen to match the HFSS 3D model as closely as possible using microstrip T-junctions , tapered lines, and straight transmission lines. The microstrip substrate characteristics for FR-4 were included in the model as well.

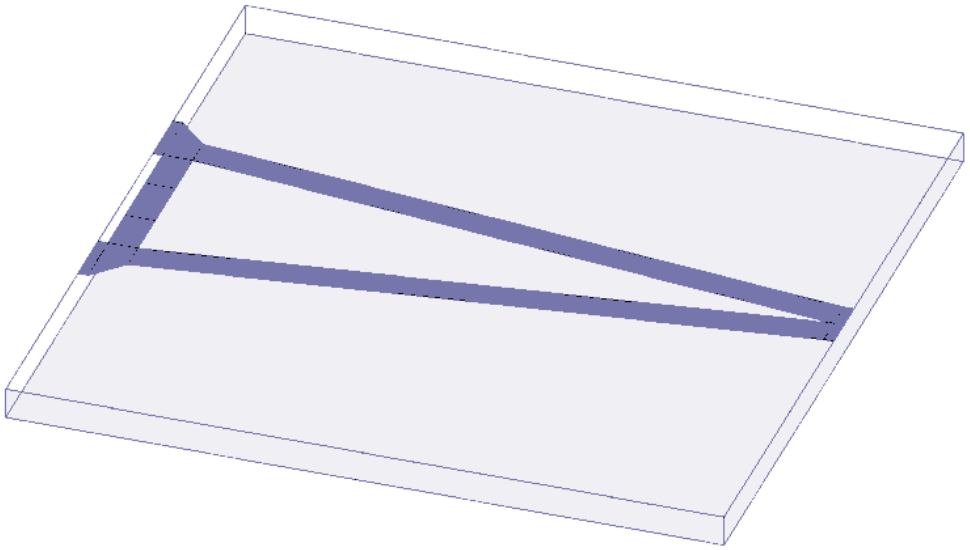

Fig. 12: HFSS model of 2:1 Wilkinson divider (straight quarter-lambda split section).

Shown in Fig. 12 is the conventional Wilkinson design for 2:1 equal-split power division using straight quarter-lambda microstrip lines. This 3D model was constructed in Ansoft HFSS and the topology was optimized by running parametric sweeps for the best frequency response.

Table 2: Ansoft HFSS simulation profile, 2:1 straight design.

Solution frequency	0.75 GHz
Iterative convergence	Good: 10-12 passes
Final meshes, tetrahedral	20328
Memory used by FEM solver	665 MB
Total solution time	1m 18s

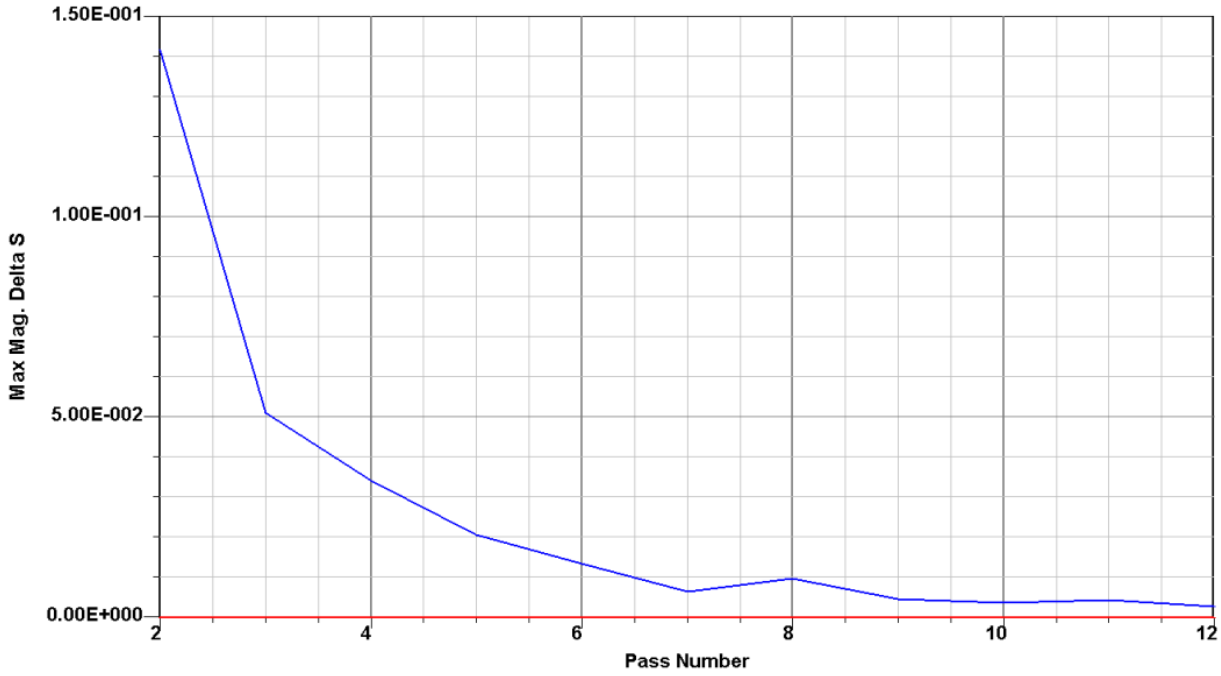

Fig. 13: Convergence plot of iterative steps for 2:1 straight design Wilkinson.

The simulation profile of the straight design 2:1 Wilkinson divider is given in Table 2. For the solution frequency of 0.75 GHz and 12 adaptive passes the final mesh had 20,328 tetrahedra, using 665 MB peak RAM. The total solution time was 1 minute and 18 seconds. The iterative

convergence of the adaptive meshing in Fig 13 shows good convergence at the 10^{th} - 12^{th} iteration.

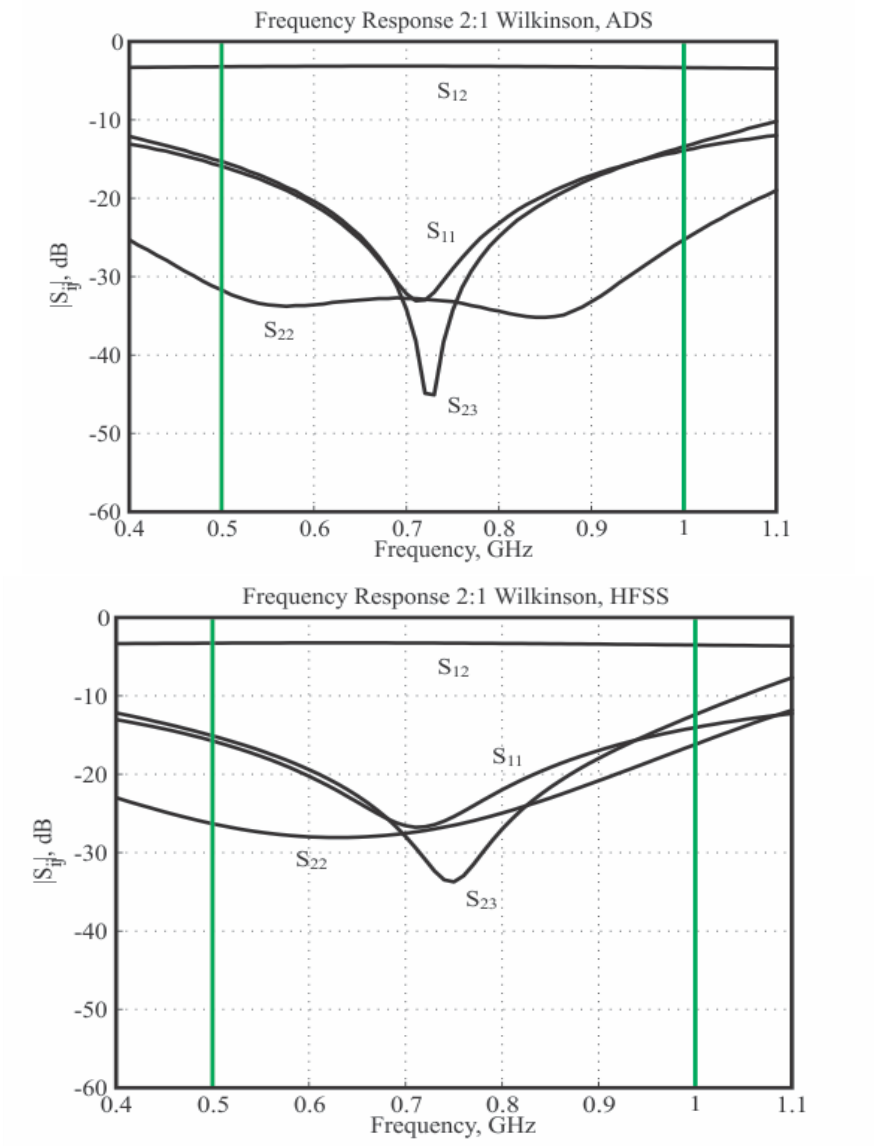

Fig. 14: Frequency response of 2:1 Wilkinson divider, ADS (top) and HFSS (bottom).

The frequency response for return loss, isolation, and coupling are shown in Fig. 14, comparing the ADS simulation results with HFSS. Both plots are similar showing good agreement between models. There is some difference in S_{22}, the reflection coefficient at the output port. This is

most likely caused by the tapered line and junction at the isolation resistor to the output port which is better modeled in HFSS or using a 2D planar EM solver like Agilent's Momentum. The Ansoft HFSS model results are more accurate than the ADS model in this case, though both model results show agreement with the ideal frequency response for an equal-split Wilkinson divider.

6.2. 2:1 divider simulation results (circular design)

The circular topology design was simulated in ADS using microstrip curve segments to model the circular quarter-lambda split section and also for the S-shape terminating microstrip traces at the output ports that follow the isolation resistor (Fig. 15). The microstrip characteristics of the FR-4 substrate were included in the simulation model parameters. Other than the addition of microstrip curve segments, the tapered line segments were removed.

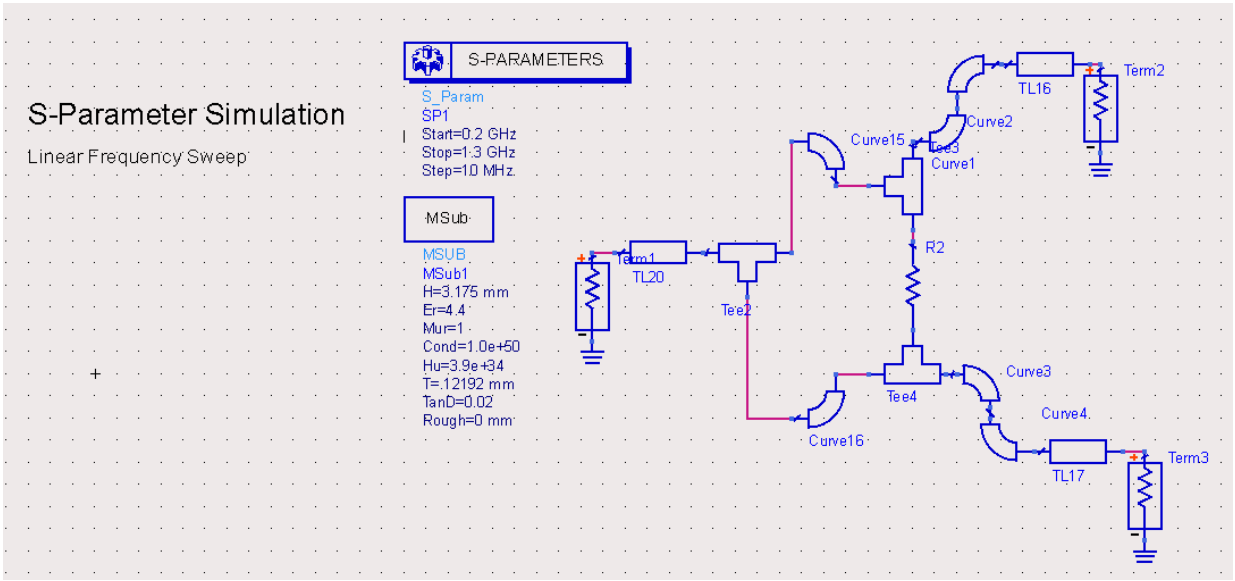

Fig. 15: ADS transmission line model of 2:1 Wilkinson divider (circular quarter-lambda split section).

The HFSS model in Fig. 16 shows the optimized circular design. The size of this design was acceptable for the 2:1 divider contribution to the total array feeding network size and further optimization of size was not necessary, though reduction of the lengths of the output port traces was done to decrease the substrate area.

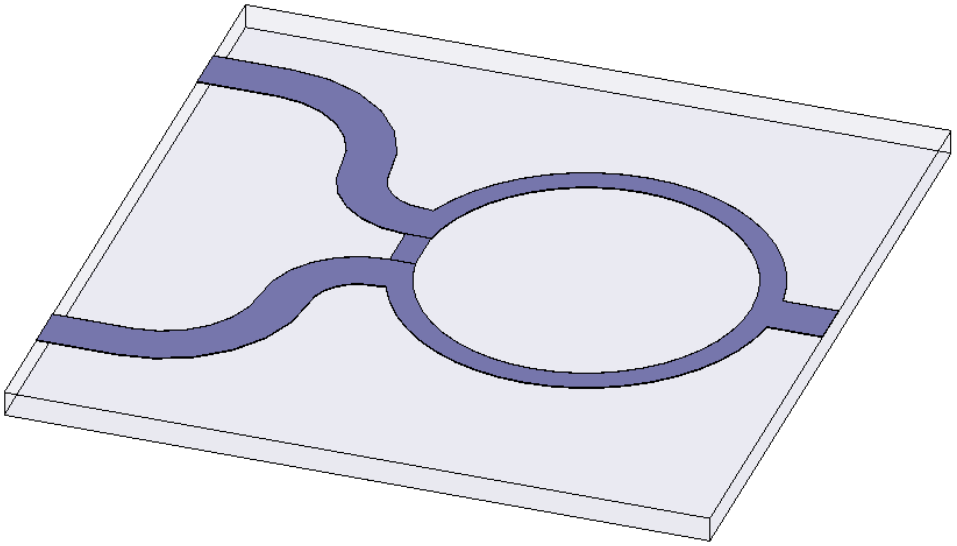

Fig. 16: HFSS model of 2:1 Wilkinson divider (circular quarter-lambda split section).

Table 3: Ansoft HFSS simulation profile, 2:1 circular design.

Solution frequency	0.75 GHz
Iterative convergence	Good, 9-12 passes
Final meshes, tetrahedral	39187
Memory used by FEM solver	1.3 GB
Total solution time	1m 36s

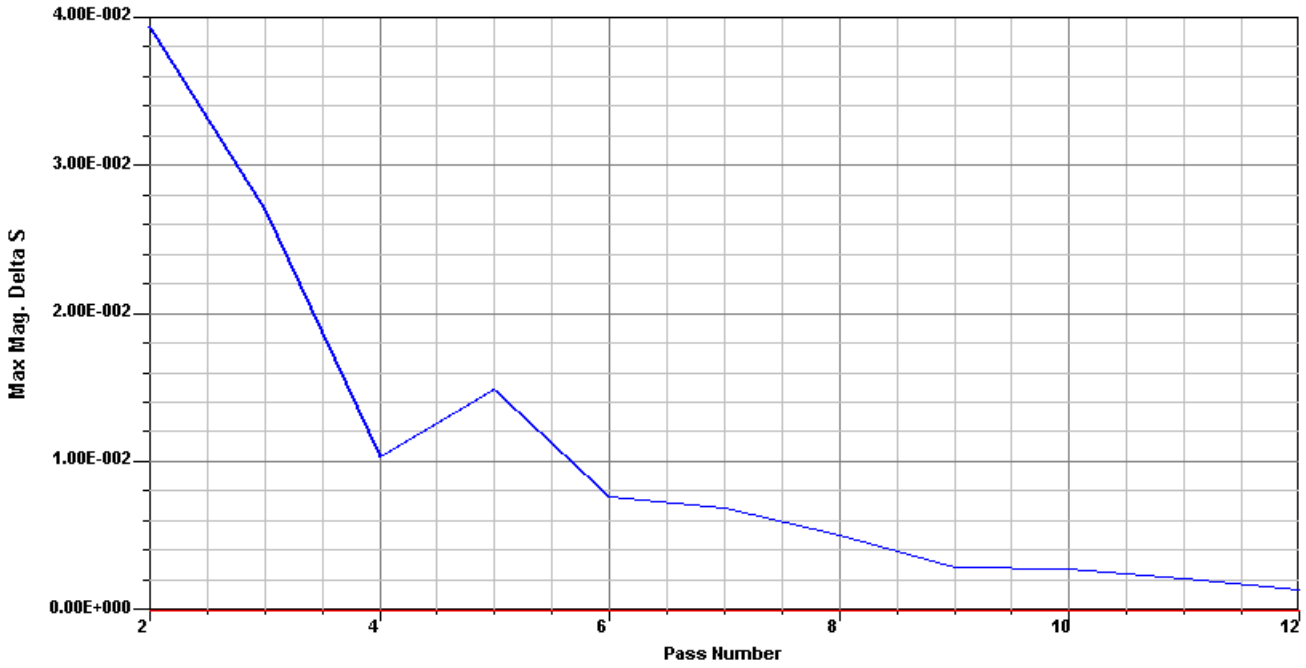

Fig. 17: Convergence plot of iterative steps for 2:1 circular design Wilkinson.

The simulation profile of the circular design 2:1 Wilkinson divider is given in Table 3. For the solution frequency of 0.75 GHz and shows good convergence with 9-12 adaptive passes the final mesh had 39187 tetrahedra, using 1.3 GB memory. The total solution time was 1 minutes and 36 seconds. The iterative convergence of the adaptive meshing in Fig. 17 shows acceptable convergence at the 9^{th} iteration. For better convergence the iterative steps can be increased beyond 12, although the error between S-parameters is reduced slightly with additional passes, the solution with only 12 passes is sufficient for analysis and is used.

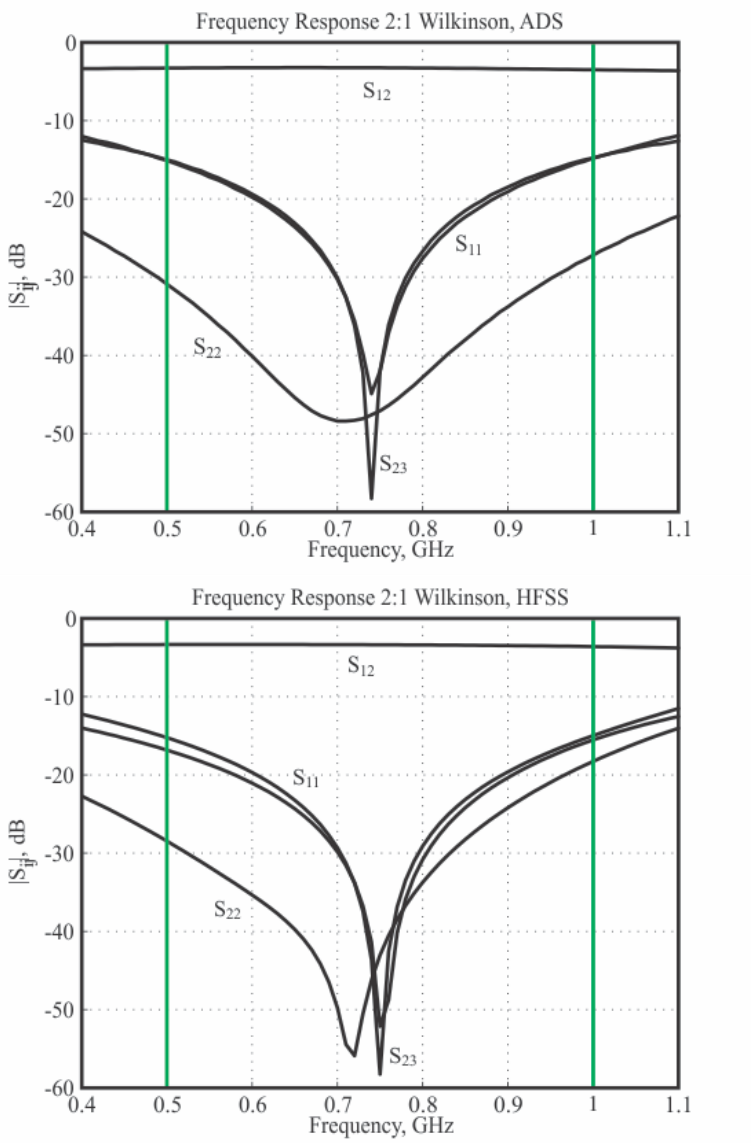

Fig. 18: Frequency response of 2:1 Wilkinson divider, ADS (top) and HFSS (bottom).

Both HFSS and ADS plots of Fig. 18 show excellent agreement with each other and with theoretical curves. The same difference in the reflection coefficient at output ports between ADS and HFSS is seen, which is attributed to the tapering at the output port microstrip lines. The frequency response of the circular design is quite similar to the theoretical one, and an additional advantage is the reduction of substrate size compared to the straight design.

6.3. Advantages of the circular topology 0.25λ TL section

In the microstrip design consideration section, the three topologies for the quarter-lambda split section were introduced and their respective advantages and disadvantages were discussed. While the elliptical design was rejected earlier, the straight and circular designs were simulated for the 2:1 Wilkinson and compared in the previous sections. Here a summary of the advantages and disadvantages is shown for the three microstrip design topologies considered. The final decision to proceed with the circular topology was a result of the necessity to reduce the size of the substrate and the good simulation results achieved for this design.

Table 4: Summary of topology advantages and disadvantages.

Wilkinson microstrip topology	Advantage	Disadvantage
Straight	• Simplest topology • Easy design • Low tetrahedra in final mesh • Faster simulation time	• Uses maximum amount of space
Elliptical	• Maximum substrate size reduction	• Lines are not sufficiently decoupled • Requires calculation of coupled line impedances
Circular	• Sufficiently decoupled lines, reduced size substrate	• More tetrahedral in the final mesh • More iterative steps for convergence • Longer simulation time

6.4. 4:1 divider simulation results

The same procedure used in the simulation of the 2:1 dividers was used for the 4:1. The models were made by cascading two stages of 2:1 dividers to form a 4:1 divider. The ADS and HFSS 4:1 Wilkinson divider models and simulation results are shown in Fig. 19, 20, 21, and Table 5.

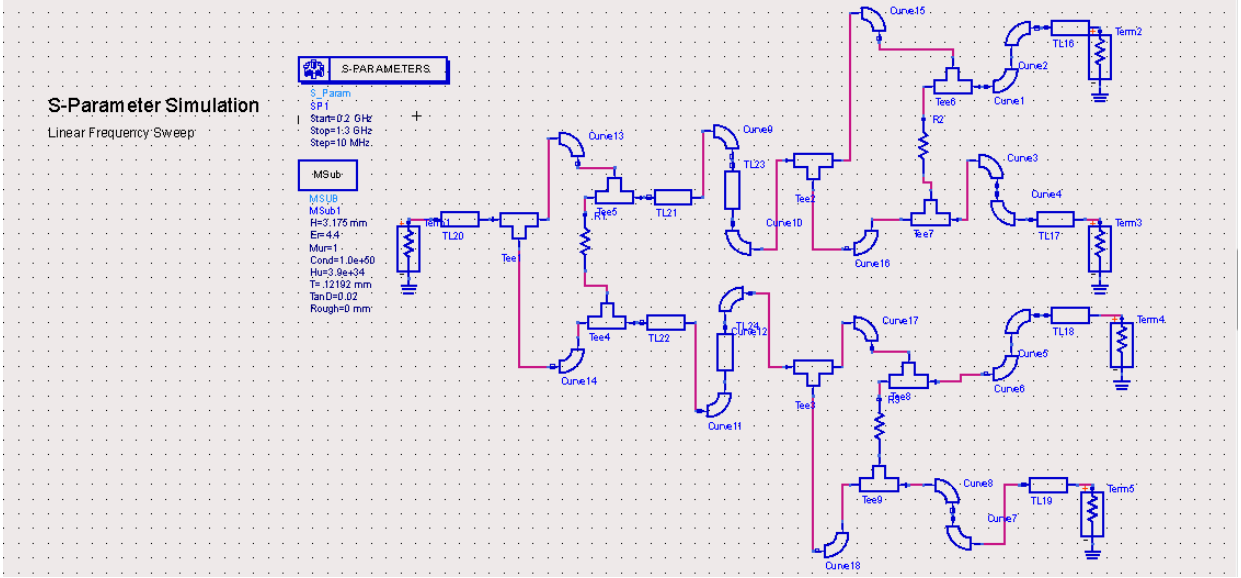

Fig. 19: ADS transmission line model of 4:1 Wilkinson divider (circular quarter-lambda split section).

The optimized 4:1 HFSS design of cascaded 2:1 dividers, are shown in Fig. 20.

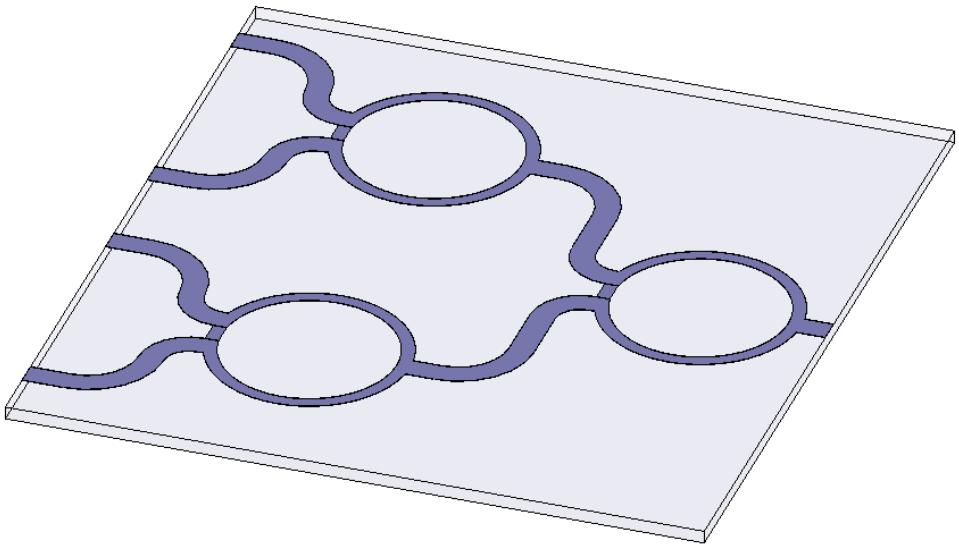

Fig. 20: HFSS model of 4:1 Wilkinson divider (circular quarter-lambda split section).

Table 5: Ansoft HFSS simulation profile, 4:1 circular design.

Solution frequency	0.75 GHz
Iterative convergence	Good, 8-12 passes
Final meshes, tetrahedral	111760
Memory used by FEM solver	3.7 GB
Total solution time	22m 55s

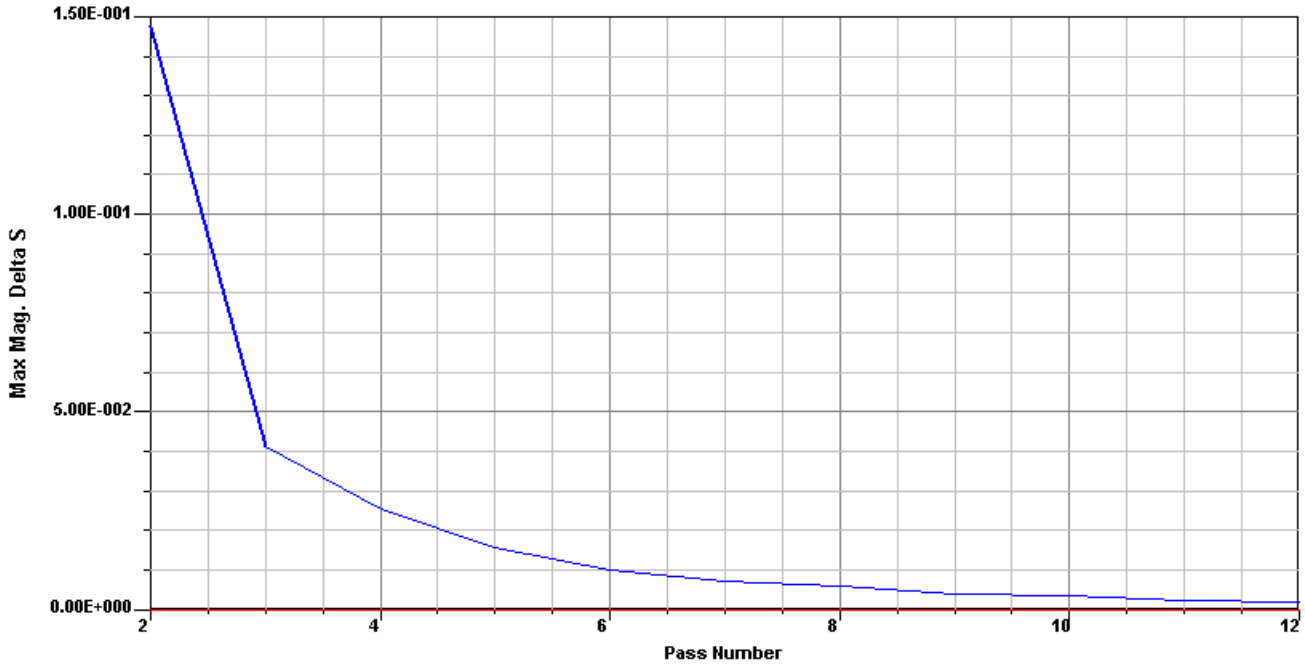

Fig. 21: Convergence plot of iterative steps for 4:1 circular design Wilkinson.

The HFSS simulation profile for the 4:1 divider shows good convergence in 8-12 passes, 111760 tetrahedra, 3.7 GB memory required, and a total simulation time of 22 minutes and 55 seconds.

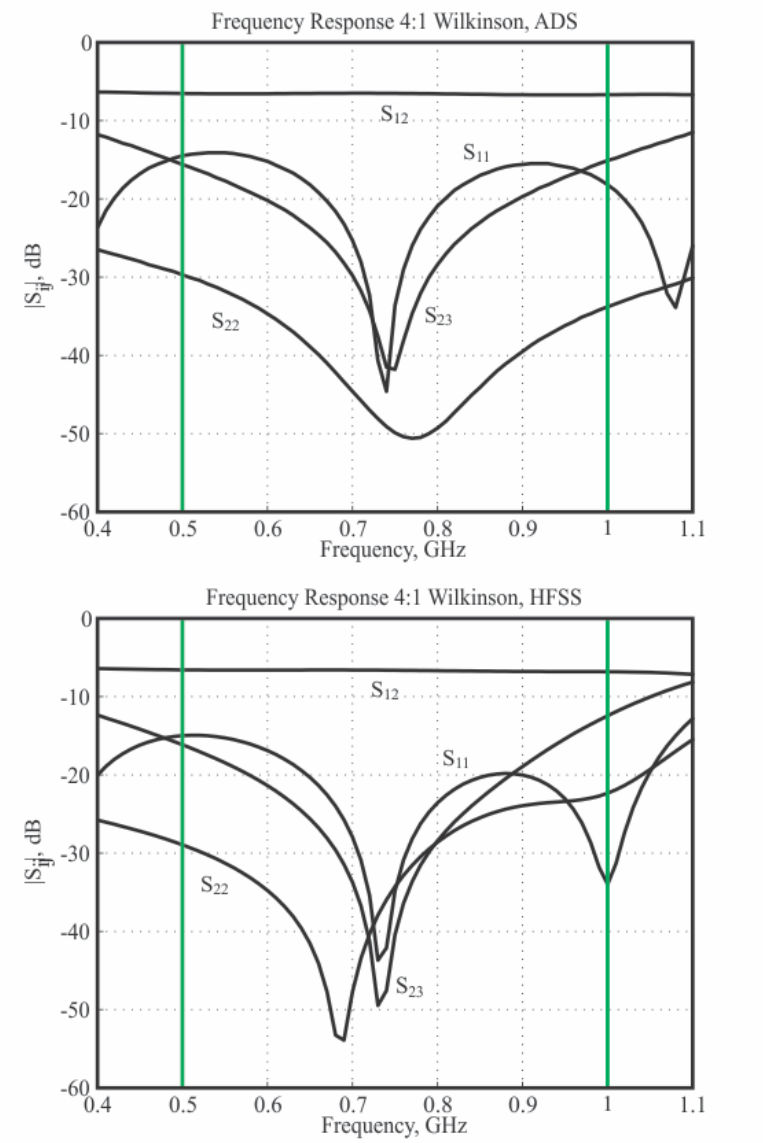

Fig. 22: Frequency response of 4:1 Wilkinson divider, ADS (top) and HFSS (bottom).

HFSS and ADS plots of Fig. 22 show excellent agreement with each other and with theoretical curves.

6.5. 8:1 divider simulation results

The ADS and HFSS 8:1 Wilkinson divider models and simulation results are shown in Fig. 23, 24, 25, and Table 6.

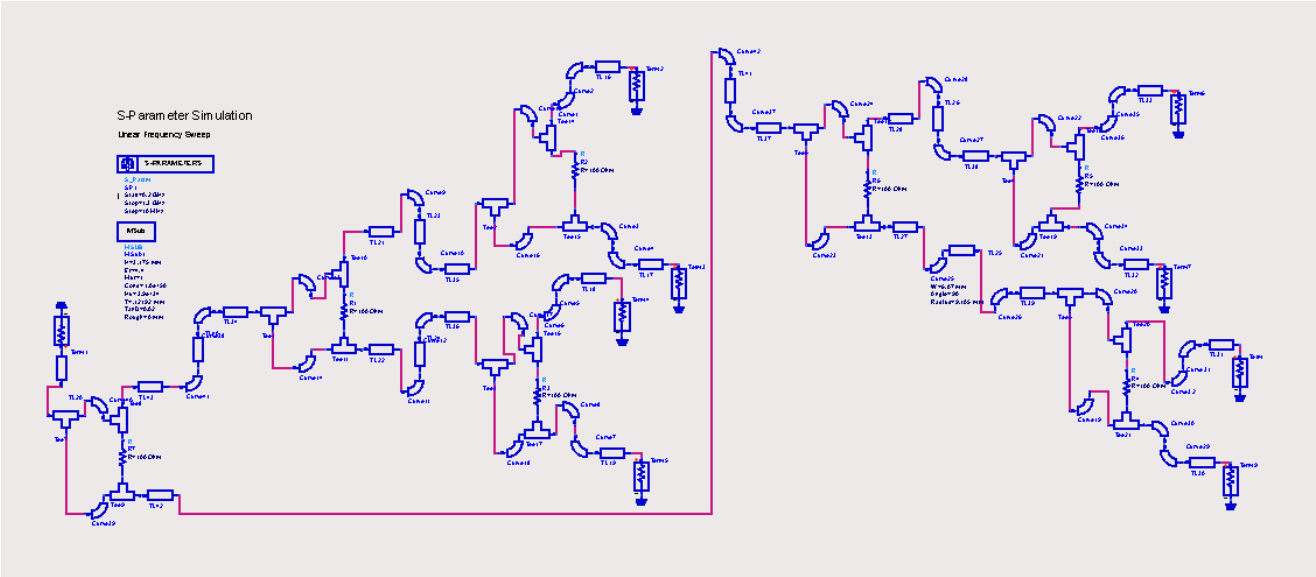

Fig. 23: ADS transmission line model of 8:1 Wilkinson divider (circular quarter-lambda split section).

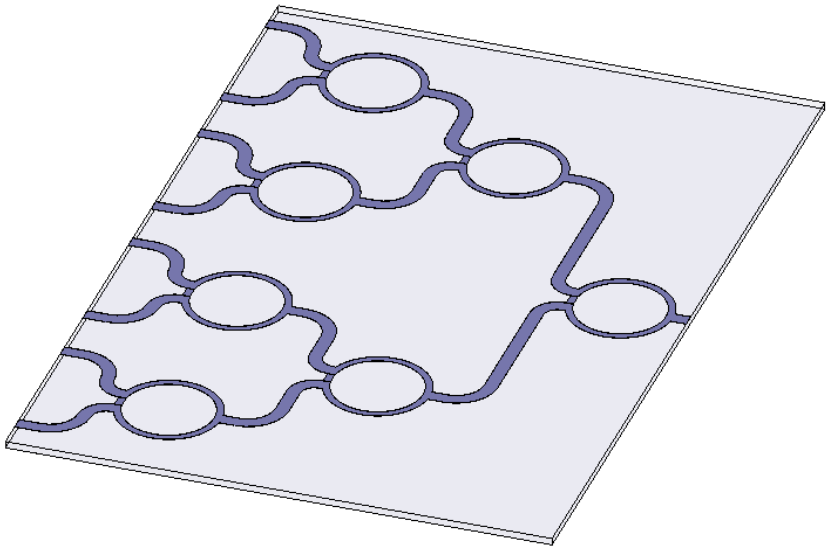

Fig. 24: HFSS model of 8:1 Wilkinson divider (circular quarter-lambda split section

Table 6: Ansoft HFSS simulation profile, 8:1 circular design.

Solution frequency	0.75 GHz
Iterative convergence	Good, 8-12 passes
Final meshes, tetrahedral	238397
Memory used by FEM solver	8.14 GB
Total solution time	51m 35s

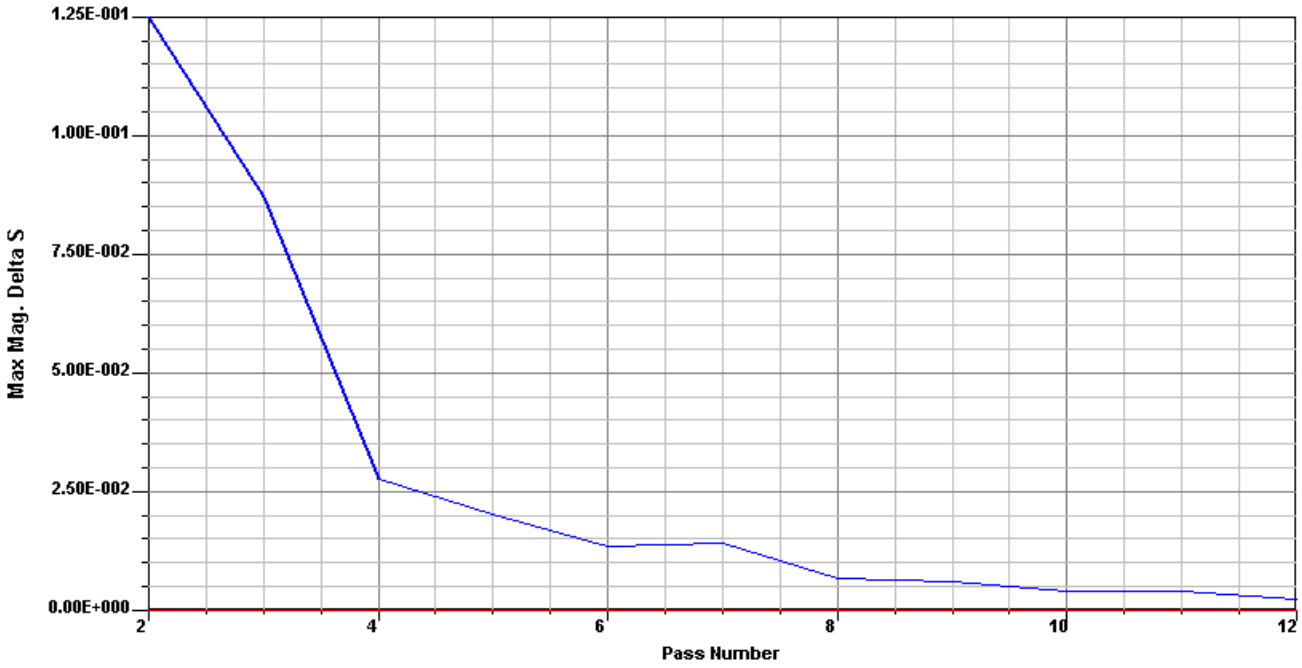

Fig. 25: Convergence plot of iterative steps for 8:1 circular design Wilkinson.

The HFSS simulation profile for the 4:1 divider shows good convergence in 8-12 passes, 238397 tetrahedra, 8.14 GB memory required, and a total simulation time of 51 minutes and 35 seconds.

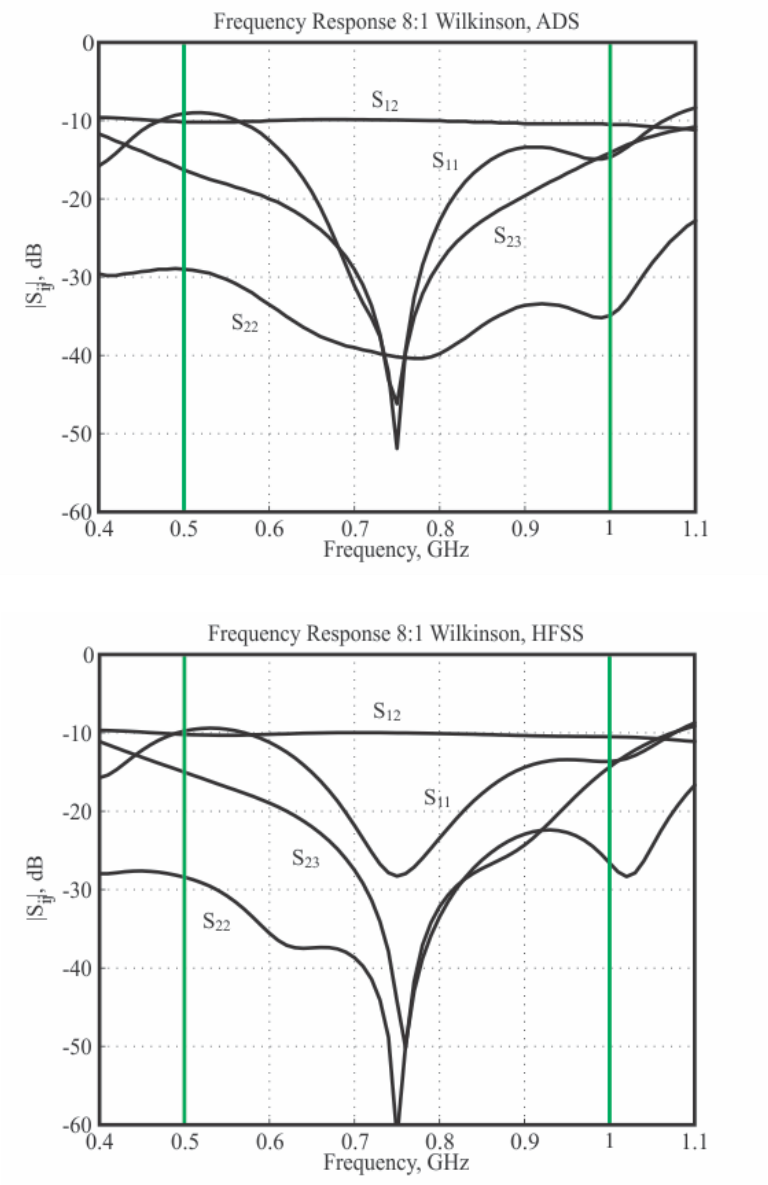

Fig. 26: Frequency response of 8:1 Wilkinson divider, ADS (top) and HFSS (bottom).

The HFSS and ADS plots of Fig. 26 show good agreement.

6.6. Simulation result summary

The ADS and HFSS simulation results agree well and follow the theoretical curves. As expected, the output power for each divider split section is half the input power, S_{12} = -3dB for the 2:1, S_{12} = -6dB for the 4:1, S_{12} = -9dB for the 8:1, with good accuracy using lossy FR-4. The dielectric induced loss for each divider at the 1 GHz (highest frequency in design) was approximately 0.1-0.2 dB for the 2:1, 0.25 dB for the 4:1, and 0.5 dB for the 8:1. This result is quite good, since FR-4 is common and easily available from any PCB fabricator, and also lower cost than other substrates. The 4:1 and 8:1 dividers had an increased bandwidth compared to the 2:1 dividers, which was a predicted result from using cascaded multiple-stepped sections. Overall, the frequency response showed low return loss, low coupling, and high isolation. The following plots of Fig. 27 show the simulated behavior of the three series Wilkinson dividers used in the hardware prototype.

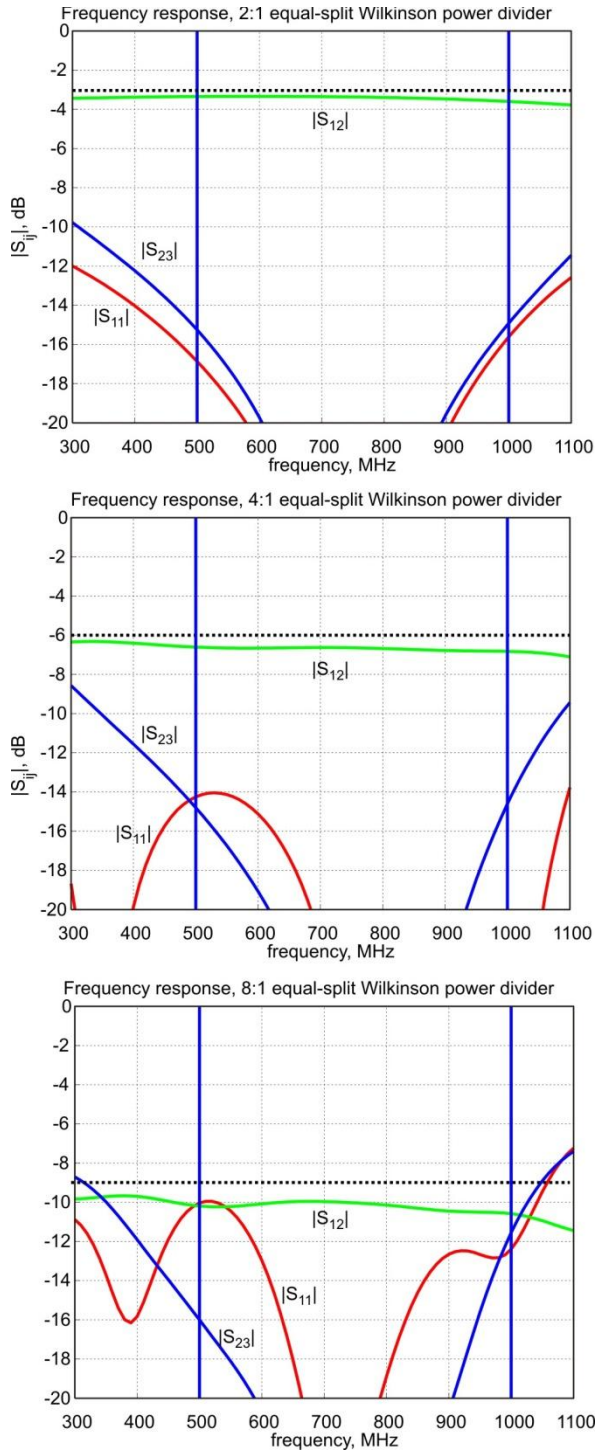

Fig. 27: Simulated behavior of three series Wilkinson dividers used in hardware prototype. The loss is given by the deviation of S_{12} from the theoretical dashed line.

7. Divider hardware fabrication

The 4:1 divider was designated to be the master divider of the corporate feeding network and receiving the most power. Therefore, it was planned to be custom-built using a thicker substrate and copper traces with different type of connector at the input design for high power. The 2:1 and 8:1 power dividers were fabricated using 125-mil thick, FR-4 substrate and 2 ounce copper traces. These were all manufactured by Advance Circuits located in Aurora, CO. A 125W power RF isolation chip resistor of 100Ω impedance was used for all dividers, ordered from Florida RF. The connectors used for each port were N-type female to PCB mount, these were rated for 10 kW peak power and 0.6 kW average power and made by Amphenol Connex (see Appendix II: Data sheets for all hardware specifications). The dimensions and pictures of the final prototype of the 2:1 and 8:1 dividers are shown below [14].

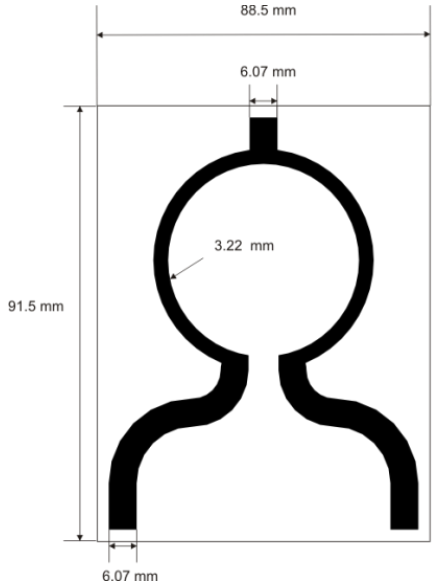

Fig. 28: 2:1 Wilkinson divider drawing with dimensions.

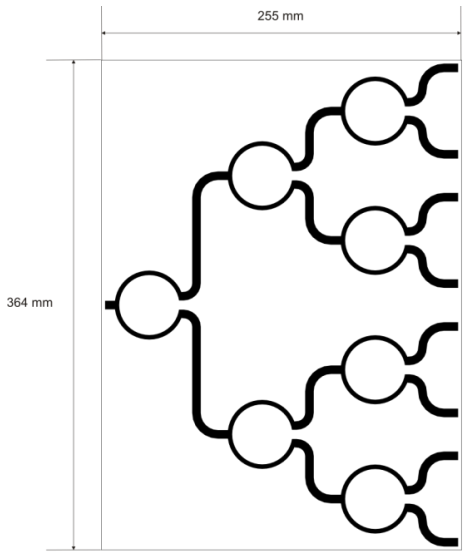

Fig. 29: 8:1 Wilkinson divider drawing with dimensions.

For timing reasons, the 4:1 divider was built in the same manner as the 2:1 and 8:1. This was acceptable since it allowed the array to be completed and tested at low power while the high-power 4:1 master divider could be built later. The completed 2:1, 4:1, and 8:1 microstrips are shown in Figs. 30-32.

Fig. 30: 2:1 power divider, without connectors and chip resistors soldered.

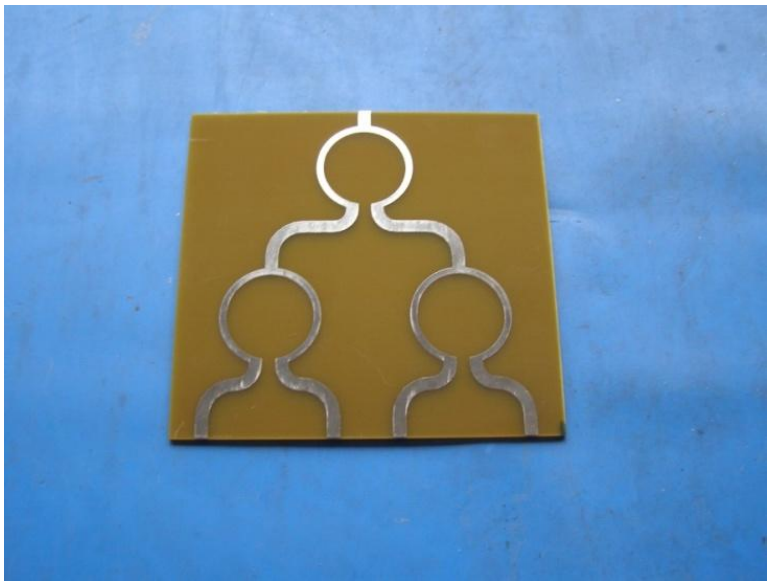

Fig. 31: 4:1 power divider, without connectors and chip resistors soldered.

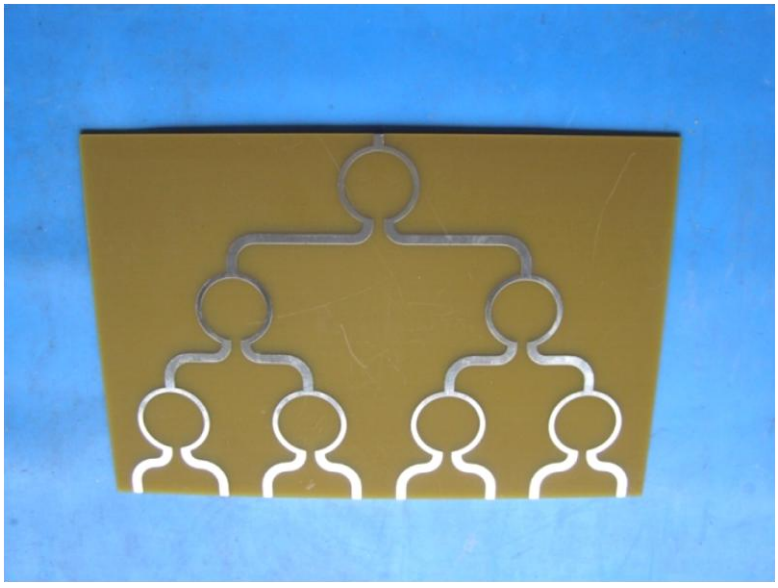

Fig. 32: 8:1 power divider, without connectors and chip resistors soldered.

8. S11 measurement of 2:1 divider

Return loss of the 2:1 divider was measured with an Agilent network analyzer using 50Ω terminations at the output ports. The losses in the cable connected between the 2:1 divider and the network analyzer were calibrated. The setup is shown in the Fig. 33. The return loss for the 8:1 and 4:1 dividers were not measured because of the time constraint on construction of the 64-element array which was being constructed in parallel with the Wilkinson dividers.

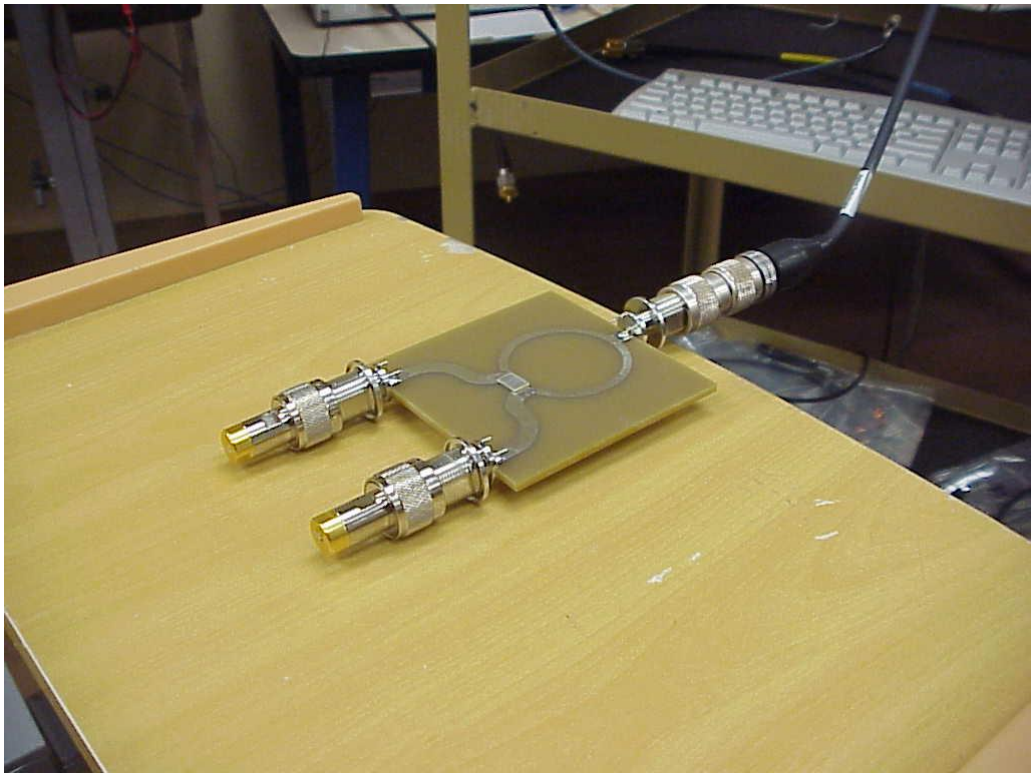

Fig. 33: Return loss measurement setup for the 2:1 divider: 50Ω terminations at output ports; input port connected to an Agilent network analyzer.

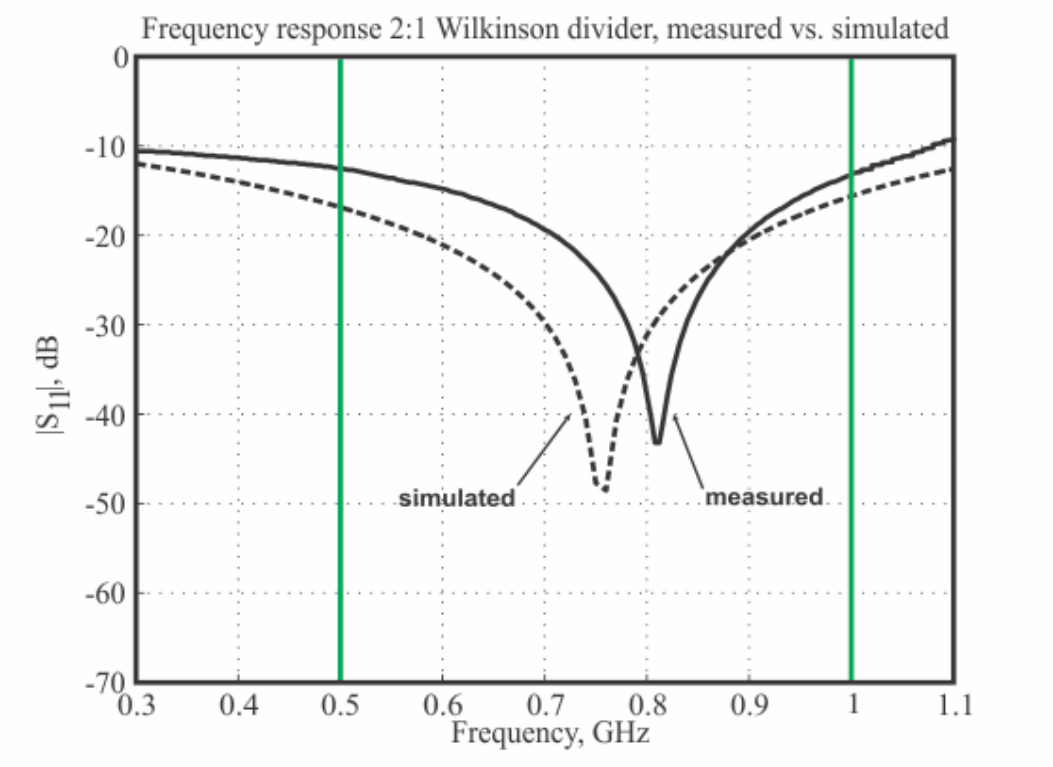

Fig. 34: Return loss plot of the 2:1 divider, simulated vs. measured.

Measured and simulated return losses are shown in Fig. 34. The measured return loss has a shift upward of approximately 500 MHz from the simulated result. The cause of the shift in resonance frequency was the larger isolation chip resistor used in place of the one originally designed for. The original 2:1 divider design was optimized for a 3 x 5 mm isolation chip resistor, but the cost of this size resistor was significantly higher than a 6 x 10 mm one. So, the larger isolation resistor was used for the prototype design.

8.1. Effect of increased isolation resistor size on S11

The effect of the larger isolation resistor on the resonance of S_{11} is shown in the plot below. When the isolation resistor length is increased from 5 mm to 10 mm in the HFSS divider model, the 0.25λ split transmission line segment (100 mm at 750 MHz) is indirectly reduced to approximately 90 mm. The reduced λ causes a center frequency shift to 800 MHz.

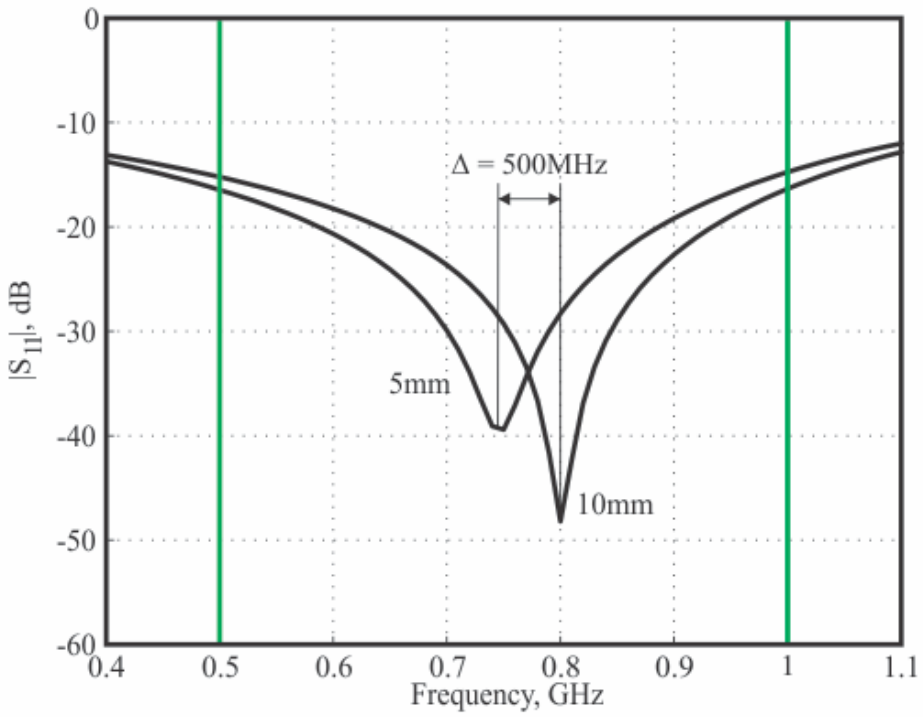

Fig. 35: Simulated return loss plot showing shift in resonance in HFSS model from 5 mm length isolation resistor to 10 mm length isolation resistor.

9. Application of Wilkinson dividers for an array corporate-fed network

Corporate-fed networks are used to provide power splits of 2^n, such as n = 2, 4, 6… and so on, and are commonly used in arrays of dipoles [15]. For an antenna array, this type of feed is more general and versatile because it provides the designer more control over the amplitude and phase of each element [16]. The feeding network that was constructed using the 2:1, 4:1, and 8:1 Wilkinson dividers designed earlier for the 64-element antenna array corporate feed is shown in Fig. 36. The array is divided into 4 sub-arrays having 16 elements in each 4x4 module. Within each module, each individual element is fed by two 8:1 power dividers, which in turn are fed by one 2:1 divider. Each module is fed by a master 4:1 power divider. In total the feed network is composed of one 4:1 master divider, four 2:1 dividers, and eight 8:1 dividers.

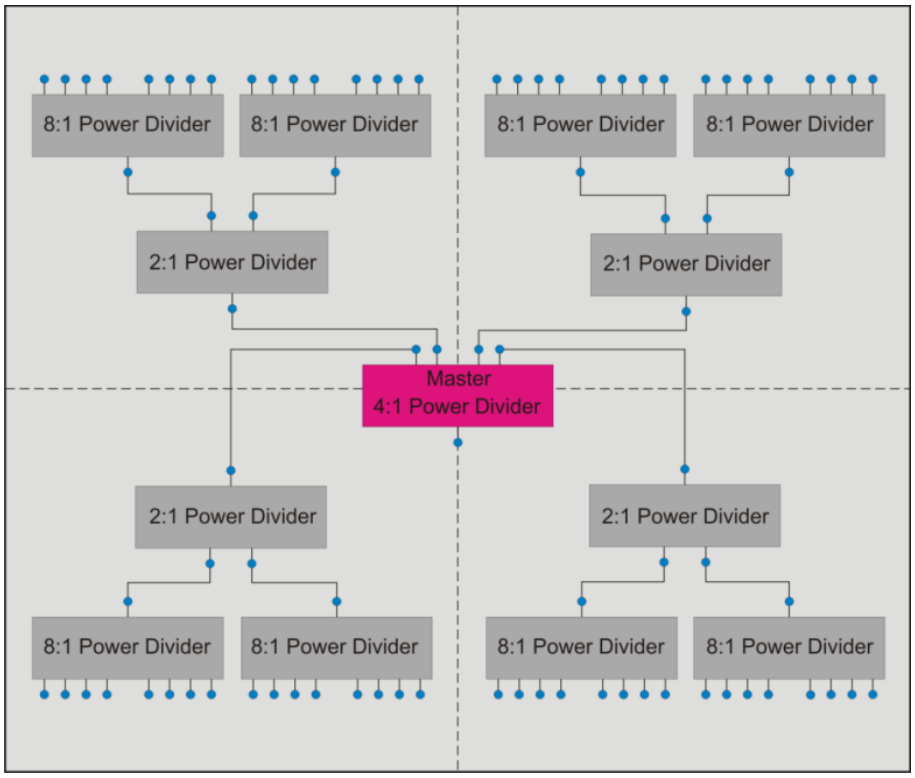

Fig. 36: Corporate feeding network for the 64-element array with 2:1, 8:1, and 4:1 Wilkinson power dividers.

The rear side of one quadrant of the array shows the feeding network for 16 elements (Fig. 37). Two 8:1 dividers fed by one 2:1 divider which will connect to the master 4:1 divider when the remaining three quadrants are attached.

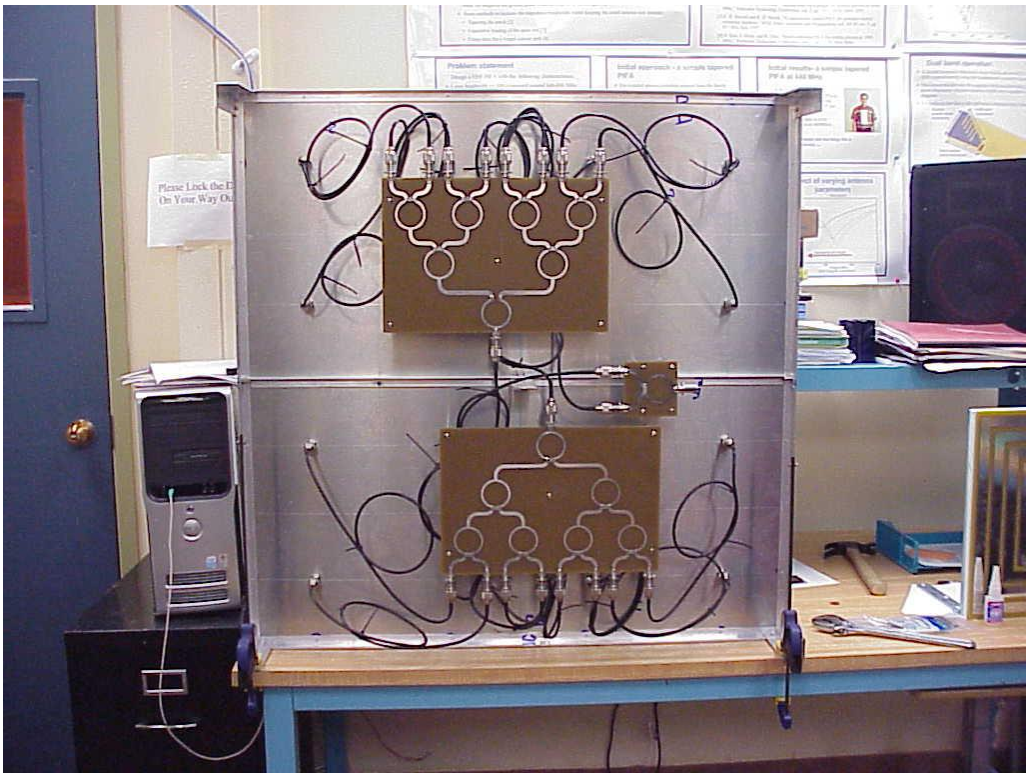

Fig. 37: One 16-element quadrant of the array showing two 8:1 Wilkinson dividers fed by one 2:1 Wilkinson divider.

The entire 64-element array feeding network is shown in the Fig. 47. All four 16-element quadrants are held together within a frame and mounted on a stand that allowed azimuth and elevation directional scanning.

10. Summary

Analysis and design of an equal-split Wilkinson power divider using stepped multiple sections of the conventional Wilkinson divider for 2:1, 4:1, and 8:1 power division was investigated. Important microstrip design considerations were taken when selecting the appropriate substrate. Although lossier than other choices (Teflon and Rogers), FR- 4 material was ultimately used: FR-4 is commonly used, readily available, and low cost. Comparison between ADS and HFSS simulation models allowed for an optimized circular Wilkinson power divider design to be realized. Hardware fabrication and S11 measurement results were discussed. Lastly, the application of the Wilkinson divider as a corporate-feed network for antenna arrays was shown.

11. Future work

The monolithic microwave integrated circuit (MMIC) technique has motivated the size reduction of circuits, which three-port power dividers are important components. The move towards smaller size dividers presents design issues where the coupling between the two impedance transformers becomes significant. Design topologies that employ coupled lines can be used to reduce the size of the dividers [9] and additional quarter-lambda impedance transformer stages (multi -section inline hybrids) can be added to increase the bandwidth of the divider [17]. Further, power dividers and their conventional structures have traditionally been symmetric with matched conditions assumed in the design, which brings the need of matching networks when these symmetric components are integrated with other elements in microwave integrated circuits. Asymmetric structures with arbitrary termination impedances are beneficial since they allow elimination of these matching networks. Design equations for asymmetric three-port power dividers with arbitrary impedance terminations have been derived for equal and unequal power division by Ahn [18]. The design of asymmetric three-port power dividers is a current area of development.

Part 2:

Design of an 8x8 wideband ribcage-dipole array for directed power applications

12. Theoretical gain pattern of a finite 2D array

12.1. Gain of the main beam

The directive gain of a large finite mutually-coupled 2D phased array with *M* by *N* regularly-spaced elements is determined by the expression first suggested by Hannan and repeatedly cited by Hansen and others. Namely, with reference to Fig.38,

$$D(\theta,\varphi) = MN\,\frac{4\pi A}{\lambda^2}\cos\theta, \quad A = d_x d_y \tag{27}$$

Here, λ is the wavelength, θ is the *scan* elevation angle. This equation was suggested based on the "natural guess" that the directivity of the large array is exactly equal to the directivity of the large (compared to the wavelength) aperture. The directivity of the uniform-distribution aperture with the impingent electric field in the free space exactly coincides with Eq. (27). Furthermore, since the effective area of an element should be proportional to its projected area in the direction of interest, the element gain should have a cosine variation with the angle in Eq. (27). Based on this intuitive reasoning, Eq. (27) has been stated.

Despite the lack of initial theoretical justification it was shown by Oliner and Malech (and also mentioned by Hansen) that Eq. (27) can be proved for slots and dipoles. For the case of a non-scanning array pointing at zenith, $\theta = 0$, so that Eq. (27) can be used to predict the gain in dB at zenith (at broadside) in the form

$$D_0 = 10\log_{10}\left[MN \frac{4\pi d_x d_y}{\lambda^2} \right] \quad \text{dB} \tag{28}$$

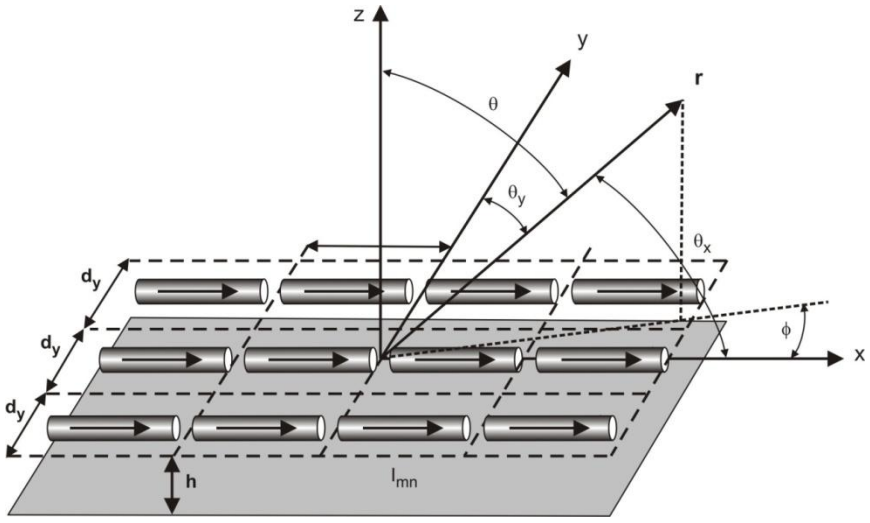

Fig. 38: Array geometry and unit cell dimensions.

12.2. Array factor and directivity

The amplitude pattern (array factor for isotropic radiators) of the scanning array in Fig. 38 is conveniently expressed in terms of direction cosines in Fig. 38. It is given by

$$AF(\theta,\varphi)=\left|\sum_{m=1}^{M}\sum_{n=1}^{N}I_{mn}\exp\left(j(md_{rx}\tau_x+nd_{ry}\tau_y)\right)\right|,\quad d_{rx}=\frac{2\pi d_x}{\lambda},\quad d_{ry}=\frac{2\pi d_y}{\lambda}$$
$$\tau_x=\cos\theta_x-\cos\theta_{xs},\quad \tau_y=\cos\theta_y-\cos\theta_{ys}$$
$$\cos\theta_{xs}=\frac{\psi_x}{d_{rx}},\quad \cos\theta_{ys}=\frac{\psi_y}{d_{ry}} \tag{29}$$

where,

I_{mn} are (real) excitation weights; $I_{mn}=1$ with no taper;

θ_x and θ_y are the polar angles from the array axis (direction cosines) shown in Fig. 38;

ψ_x and ψ_y are the progressive phase shifts between elements.

When scanning at zenith, the direction cosines of the radius vector specifying scan direction (beam maximum) $\cos\theta_{xs}$ and $\cos\theta_{ys}$ are both equal to zero.

After some manipulations, the result from Eq. (29) is reduced to the form,

$$AF(\theta,\varphi)=\frac{\sin x}{x}\frac{\sin y}{y},\quad x=\frac{1}{2}Md_{rx}\tau_x,\quad y=\frac{1}{2}Nd_{ry}\tau_y \tag{30}$$

which is the Fraunhofer scalar diffraction pattern of the corresponding rectangular aperture.

12.3. Gain of the individual element

For vector fields or the array fields, Eq. (30) has to be further augmented with the pattern of an individual element. This step is omitted though since the dipole pattern close to zenith is very uniform, and since only the main beam of the large 8×8 array is of interest.

12.4. Total directive gain

The array scanning at zenith is considered. Combining the results of subsections 12.1 to 12.3 the directive gain of the array is obtained in the form

$$D_0 = 10\log_{10}\left[NM\,\frac{4\pi d_x d_y}{\lambda^2}\left(\frac{\sin x}{x}\frac{\sin y}{y}\right)^2\right] \quad \text{dB}, \qquad x = \frac{1}{2}Md_{rx}\cos\theta_x \quad y = \frac{1}{2}Nd_{ry}\cos\theta_y \quad (31)$$

For the *E*-plane scan (*xz*-plane in Fig. 1) $\theta_x + \theta = 90\,\text{deg}$, $\theta_y = 90\,\text{deg}$, and Eq. (31) simplifies to

$$D_0 = 10\log_{10}\left[NM\,\frac{4\pi d_x d_y}{\lambda^2}\left(\frac{\sin x}{x}\right)^2\right] \quad \text{dB}, \qquad x = \frac{1}{2}Md_{rx}\sin\theta \quad (32)$$

For the *H*-plane scan (*yz*-plane in Fig. 38) $\theta_y + \theta = 90\,\text{deg}$, $\theta_x = 90\,\text{deg}$, and Eq. (31) simplifies to

$$D_0 = 10\log_{10}\left[NM\,\frac{4\pi d_x d_y}{\lambda^2}\left(\frac{\sin y}{y}\right)^2\right] \quad \text{dB}, \qquad y = \frac{1}{2}Nd_{ry}\sin\theta \quad (33)$$

12.5. Application

The geometry of the unit cell in the array under study is shown in Fig. 39. The radiator is a ribcage dipole with a conical matching network close to the antenna feed to be connected to a balun. The overall size of the radiator is slightly less than the size of the unit cell.

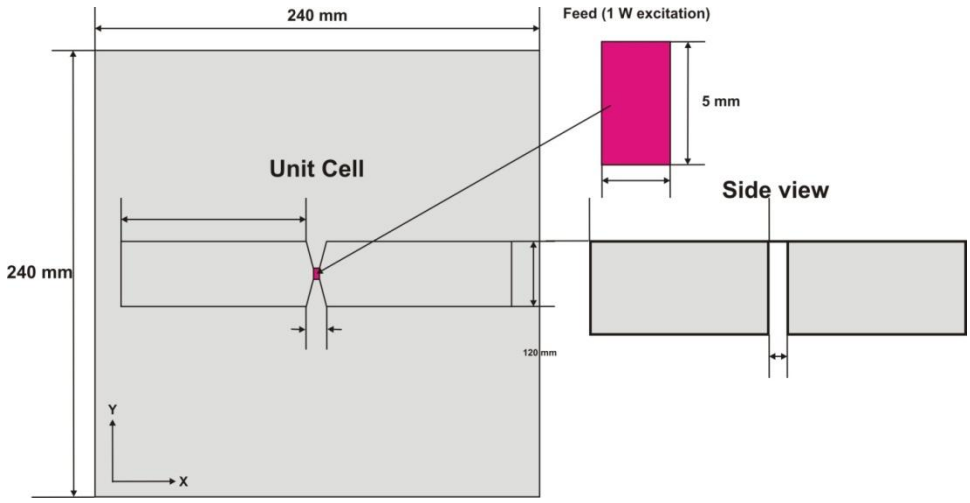

Fig. 39: The array unit cell on the size of 240 mm by 240 mm.

In the particular case of the 8×8 array, with reference to Fig. 38, the following parameters in Eqs. (32) and (33) are used:

$$N = 64, d_{rx} = d_{ry} = 240\text{mm}, \\ k = 2\pi / \lambda, \quad \lambda = c_0 / f \tag{34}$$

Fig. 41 shows the theoretical gain pattern for the array described by Eq. (33) at 500 MHz and 1 GHz, respectively.

12.6. Comparison between theory and numerical simulations

The numerical simulations have been carried out for the array of center-fed ribcage dipoles (see the next section) with Ansoft HFSS v. 12. The spacing from the ground plane was 150mm. Fig. 40 shows the array structure. The solution was obtained with the PML box and used about 100,000 tetrahedra. Fig. 41 shows numerical directive gain (dashed curve) versus theoretical gain (Eq. (33) – solid curve) in the H-plane at two frequencies of interests.

The theoretical and numerical data agree quite well. This confirms the estimates used to predict the behavior of the hardware prototype considered in the following text.

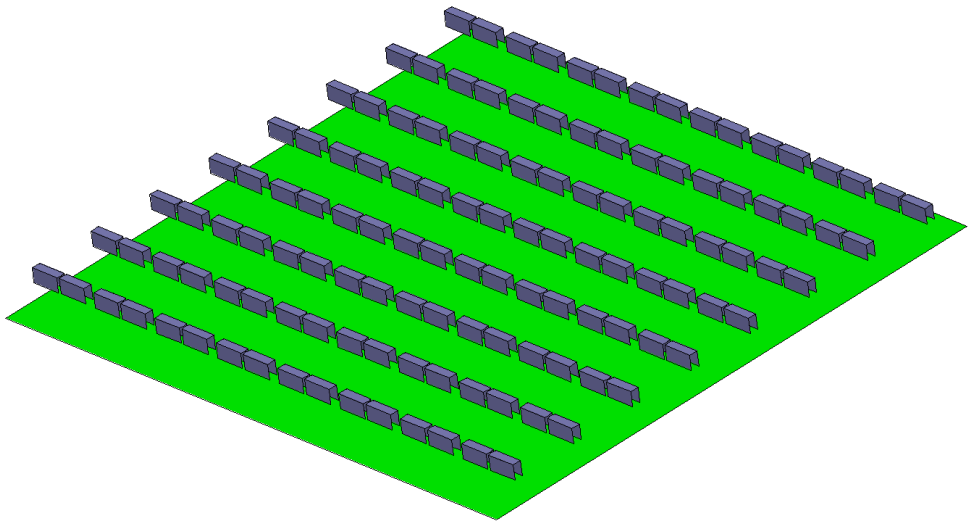

Fig. 40: Modeling of an 8×8 array of dipoles on the total size of 1.96×1.96 m.

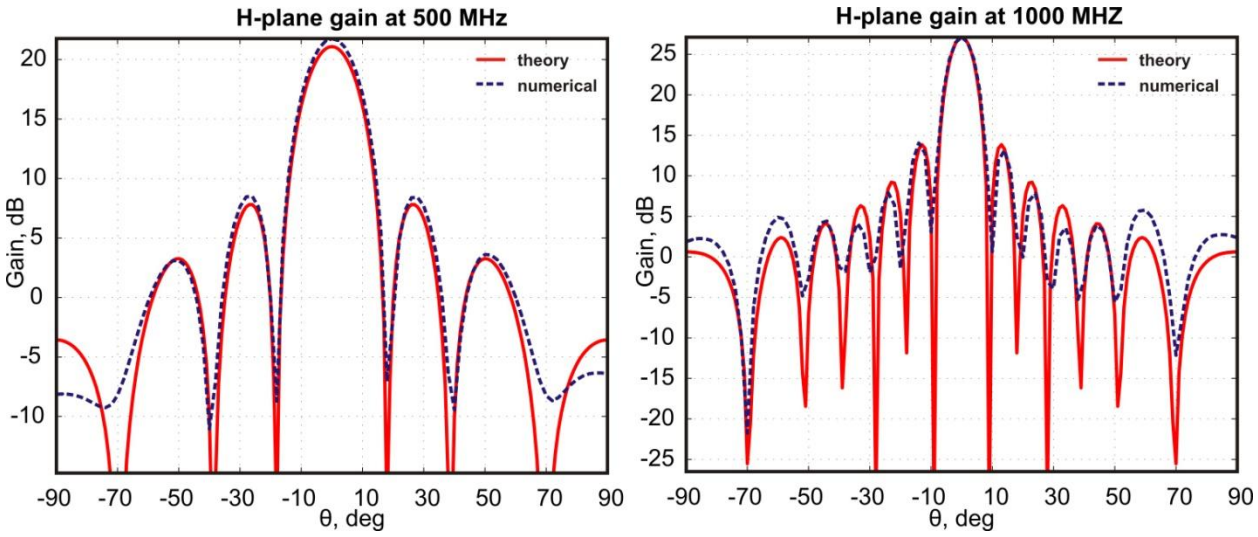

Fig. 41: Theory versus numerical simulations of a 64-element array of dipoles shown in Fig. 40.

13. Array hardware

13.1. Radiator

As a single radiator the ribcage dipole shown in Fig. 42a has been chosen. Compared to other equivalent designs – the blade dipole in Fig. 42b and the droopy dipole in Fig. 42c - the ribcage dipole is more versatile. It has been shown that, among other possible dipole configurations it combines the advantages of both the blade dipole and the droopy dipole – the wider impedance bandwidth typical for the blade dipole and the better pattern uniformity over the frequency band typical for the droopy dipole.

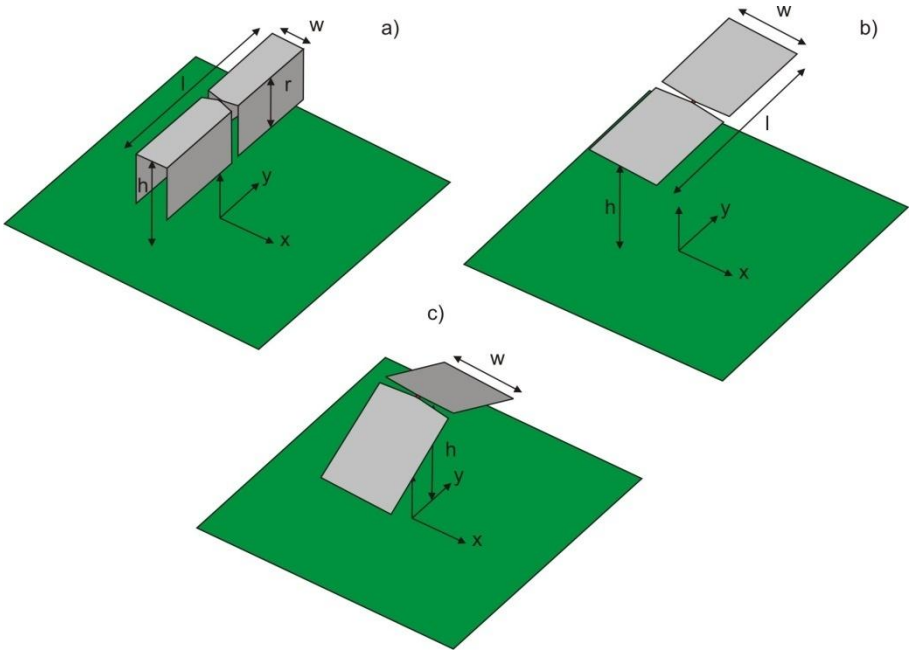

Fig. 42: Ribcage dipole versus its competitors: b) - the planar blade dipole; and c) - the droopy dipole (from reference [5]).

13.2. Balun

A tapered microstrip balun shown in Fig. 43 has been employed. The use of this type of balun is common for broadband linearly-polarized dipoles over a ground plane. The balun is printed on a 125 mil thick FR4 (using thick copper traces) and is soldered to a N-type male connector in the ground plane. The microstrip trace itself is either tapered or not. The typical trace width is 5-6mm.

Different tapering profiles including triangular, exponential, and Chebyshev's profiles have been investigated, but a significant improvement in the impedance bandwidth compared to the simple triangular profile was not found.

Compared to the center-fed ribcage dipole, the isolated ribcage radiator with the balun may be optimized for a slightly lower or a similar impedance bandwidth.

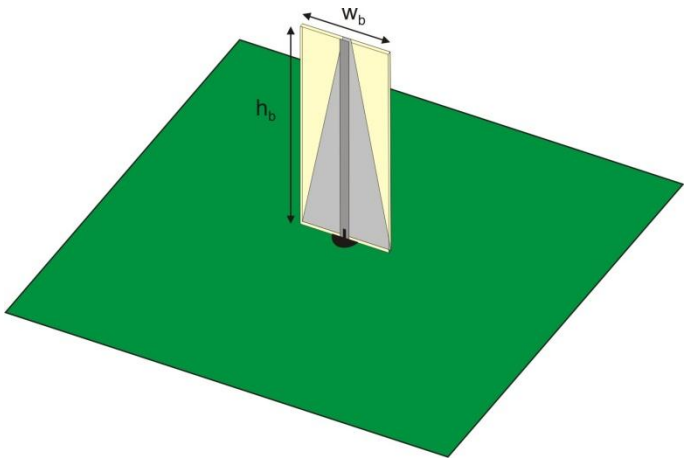

Fig. 43: Microstrip tapered balun and its dimensions (from reference [5]).

13.3. Radiator with balun

Two isolated radiators including the printed balun shown in Fig. 44 have been tested prior to arrays assembly. Fig. 44 shows a comparison between simulations and experiments - the return loss measurements (calibrated 8722ETR Agilent network analyzer). The agreement is satisfactory, but not perfect. The difference in the middle of the band can be partially explained as a detuning effect of two Teflon posts seen in Fig. 44. These posts have not been considered in the simulations. When the posts are removed, a better agreement is obtained.

13.4. Feeding network with Wilkinson dividers

Corporate-fed networks are used to provide power splits of 2^n, such as n = 2, 4, 8… and so on. For an antenna array, this type of feed is more general and versatile because it provides the designer more control over the amplitude and phase of each element. For the 64-element antenna array a corporate feed network is constructed using 2:1, 4:1, and 8:1 Wilkinson dividers, shown in Fig.45. The array is divided into 4 sub-arrays having 16 elements in each 4x4 module. Within each module, each individual element is fed by two 8:1 power dividers, which in turn are fed by one 2:1 divider. Then, each module is fed by a master 4:1 divider. In total the feed network is composed of one 4:1 master divider, four 2:1 dividers, and eight 8:1 dividers.

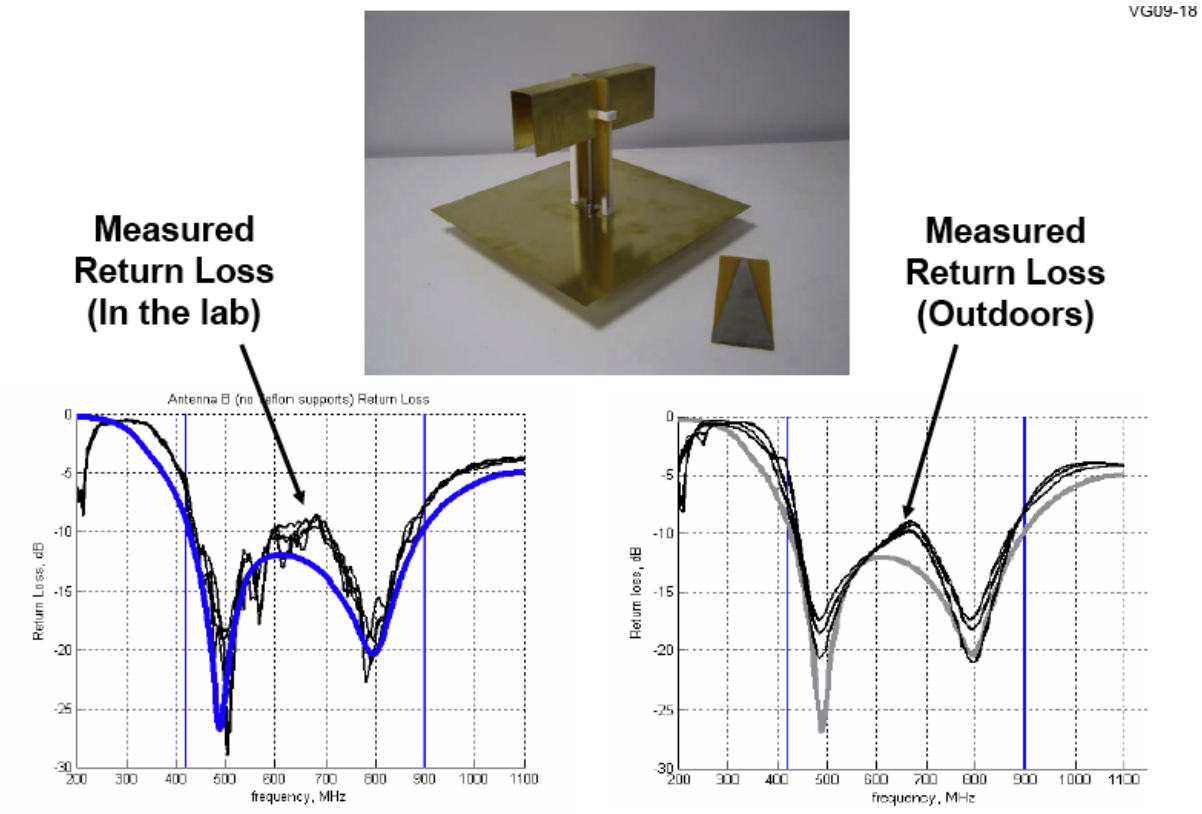

Fig. 44: Top – a ribcage dipole antenna. Bottom left - comparison between simulations and experiment (indoor measurement). Bottom right - comparison between simulations and experiment (outdoor measurement) - showing return loss of the isolated ribcage above 300×300mm ground plane. The thick curves indicate simulations; thin curves – experiment (Courtesy of Physical Sciences Inc.).

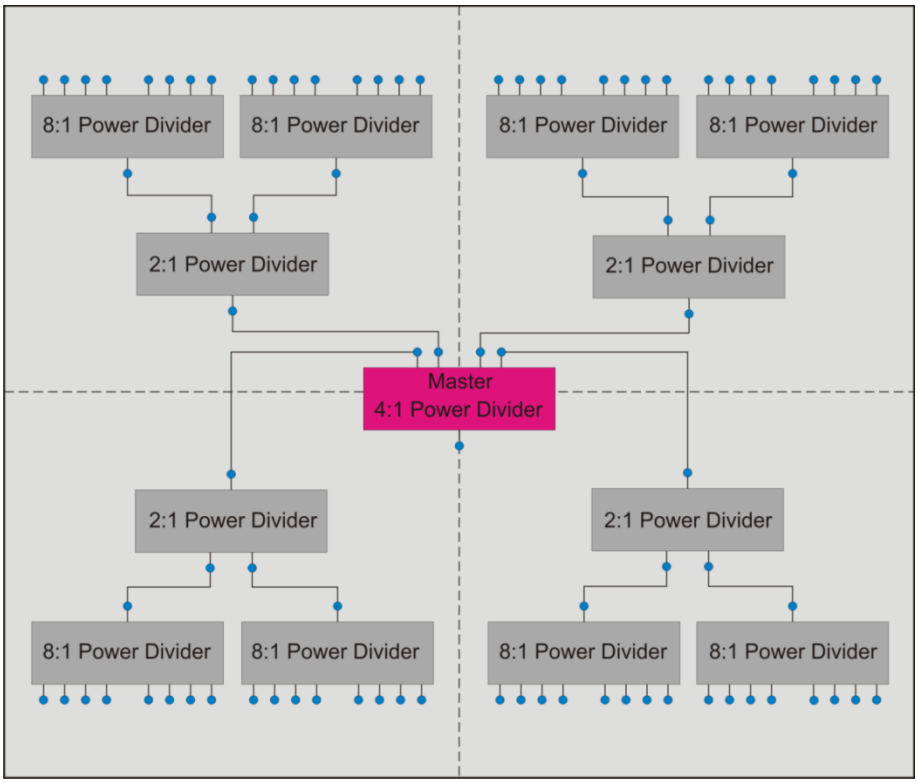

Fig. 45: Corporate-feeding network used for the 64-element antenna array.

13.5. Array assembly

The array is mounted on a 2D controlled mast shown in Fig. 46. The digitized motor controller allows for mechanical scanning in both azimuth and elevation plane, to within ±45 degrees. The array itself was built as a combination of four 4×4 individual blocks as shown in Fig. 45 and then tuned for the maximum impedance bandwidth.

Fig. 46: Front view of the 64-element array (Courtesy of Physical Sciences Inc.).

Fig. 47: Array assembly. Back view with the feeding network (Courtesy of Physical Sciences Inc.).

14. Array measurements

14.1. Return loss of the array

The return loss of the array measured at the output of the 4:1 power divider is shown in Fig. 48 that follows. The array has a slightly better impedance bandwidth than initially simulated (Ansoft HFSS v. 12). This may be explained by extra loss in the feeding network, which become especially important at higher frequencies.

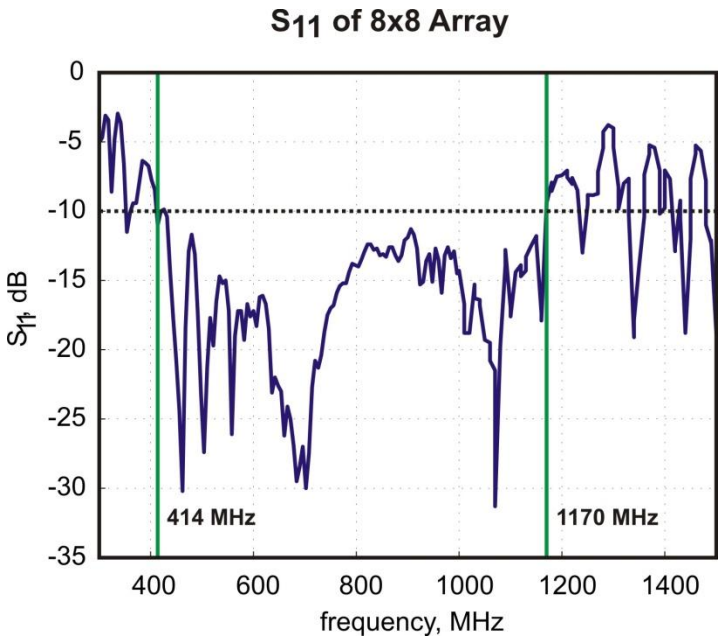

Fig. 48: Return loss of the array measured at the output of the 4:1 power divider.

14.2. Measurement calibration: Path loss estimates

Horn-to-horn measurements were taken at 500 MHz and 1 GHz outside of the Physical Sciences Inc. (PSI) building in North Andover, Massachusetts to calibrate the path and investigate the effects of ground reflections on the antenna gain.

The measurements of the directive gain have been performed in house, using a setup with two, A.H. Systems Inc. wideband ridged horns (AHS-570), shown in Fig. 49 for calibration purposes.

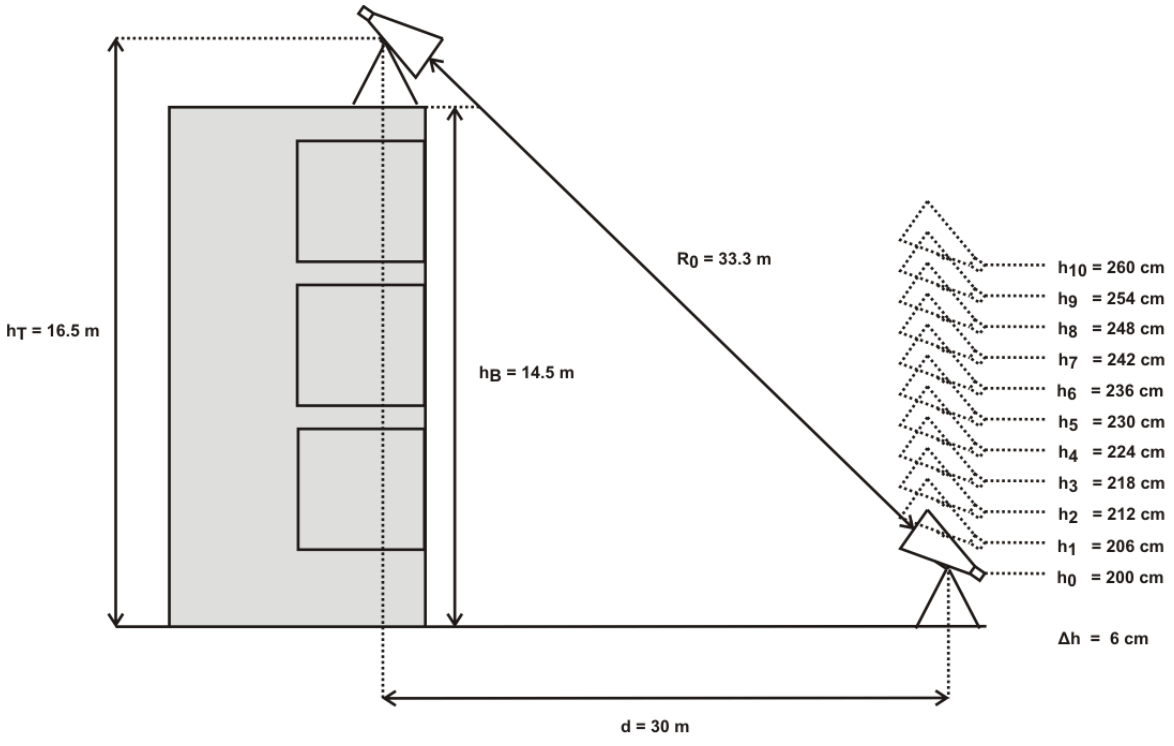

Fig. 49: Horn measurement setup at Physical Sciences Inc. (Courtesy of Physical Sciences Inc.)

The transmitting horn was set on the building's roof and the receiving horn was set in the parking lot in the arrangement shown above. Both horns stand 2 meters high when supported by tripod.

The height of the receiving horn was varied by 6 cm increments and the received power was measured using an Agilent spectrum analyzer (E4402B ESA-E). Minimum and maximum values were taken because of the rapidly changing values shown on the spectrum analyzer. The minimum, maximum, and mean values are shown in Tables 7 and 8 that follow.

The results given in Tables 7 and 8 indicate that the gain remains nearly constant at 500 MHz and 1 GHz when the height is varying, MATLAB code in Appendix I: Path loss estimation received power. The height of the receiving horn was varied sufficiently for one cycle of interference pattern at 500 MHz and two cycles at 1 GHz, so the effect of reflections appears to be minimal (on the order of ±1dB or less in pattern distortion) because of the stable gain values recorded.

Table 7: Received power at 500 MHz for increments of R.

ΔR **(m)**	**Max (dBm)**	**Min (dBm)**	**Mean (dBm)**
$R_0 = 33.32\ m$	-53.46	-57.02	-55.24
$R_1 = 33.34\ m$	-53.23	-56.94	-55.09
$R_2 = 33.37\ m$	-53.42	-56.72	-55.07
$R_3 = 33.40\ m$	-52.24	-56.91	-54.58
$R_4 = 33.43\ m$	-52.92	-56.03	-54.48
$R_5 = 33.45\ m$	-52.73	-56.18	-54.46
$R_6 = 33.48\ m$	-53.21	-56.13	-54.67
$R_7 = 33.51\ m$	-53.42	-56.11	-54.77

$R_8 = 33.53\ m$	-53.33	-56.82	-55.08
$R_9 = 33.56\ m$	-53.03	-56.72	-54.88
$R_{10} = 33.59\ m$	-53.01	-56.84	-54.93

Table 8: Received power at 1 GHz for increments of R.

ΔR **(m)**	**Max (dBm)**	**Min (dBm)**	**Mean (dBm)**
$R_0 = 33.32\ m$	-48.75	-52.36	-50.56
$R_1 = 33.34\ m$	-48.92	-52.38	-50.65
$R_2 = 33.37\ m$	-48.75	-52.46	-50.61
$R_3 = 33.40\ m$	-48.76	-52.38	-50.57
$R_4 = 33.43\ m$	-46.87	-52.12	-49.50
$R_5 = 33.45\ m$	-47.98	-51.20	-49.59
$R_6 = 33.48\ m$	-47.65	-51.38	-49.52
$R_7 = 33.51\ m$	-48.72	-52.22	-50.47
$R_8 = 33.53\ m$	-48.79	-52.06	-50.43
$R_9 = 33.56\ m$	-48.88	-52.43	-50.66
$R_{10} = 33.59\ m$	-48.93	-52.56	-50.75

14.3. Gain calibration with two horns

To calculate the absolute antenna gain from the received power measurements, measurements with two horns first were performed first, and then used the following expression:

$$G_{\text{Array}} = G_{\text{Hom}} + \{P_{\text{Array/dBm}} - P_{\text{hom/dBm}}\} \quad (35)$$

where

G_{Array} - sought array directive gain at a given frequency (dB)

G_{Hom} - calibrated second horn gain at a given frequency from datasheet (dB)

$P_{\text{Array/dBm}}$ - measured array received power (dBm)

$P_{\text{Hom/dBm}}$ - measured second horn received power (dBm)

This estimate does not depend on the input power to the measurement setup.

14.4. Gain measurement results

The received power of the antenna array was measured after the horn-to-horn calibration. The array was mounted and positioned such that the face of the array was directed toward the roof of the PSI building. The phase center of the array was approximately 2 meters above the ground. The horn on the roof facing the array was excited with 20 dBm power. The array was then connected to the spectrum analyzer and rotated horizontally by 5 degree steps and scanned a total of 45 degrees. At each 5 degree step, the received power of the array was recorded.

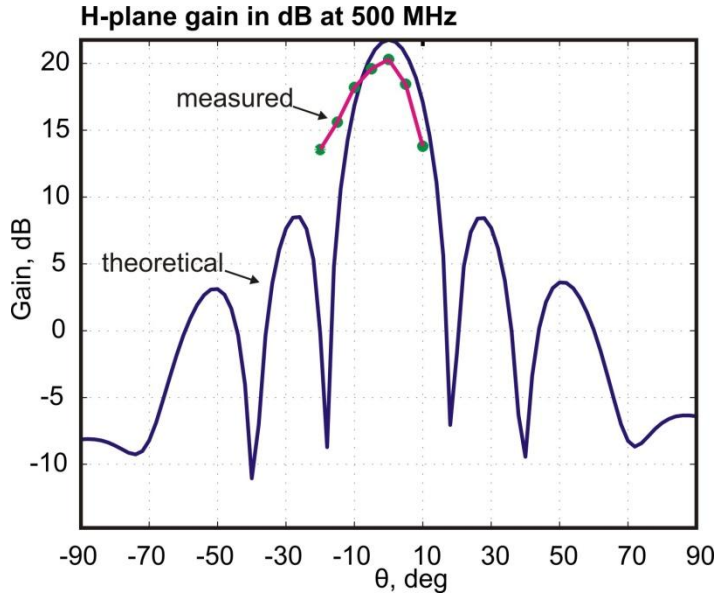

Fig. 50: Measured vs. numerical simulation - H-plane directive gain at 500 MHz.

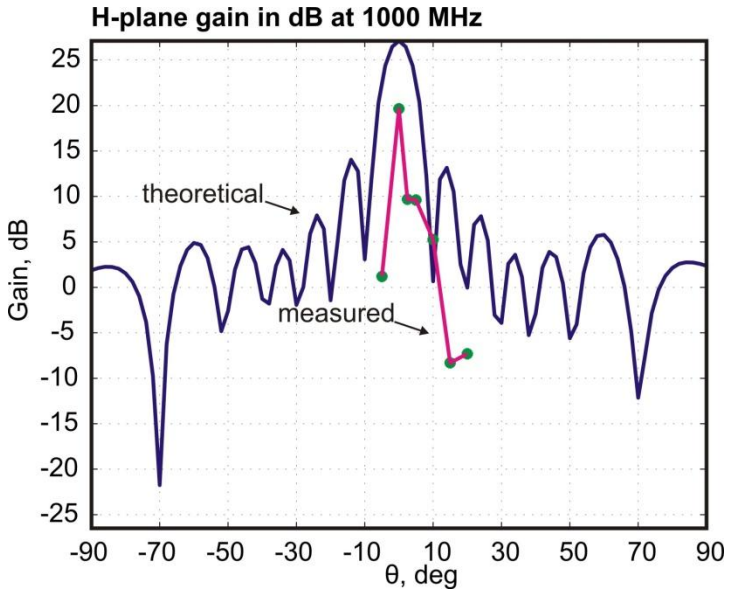

Fig. 51: Measured vs. numerical simulation - H-plane directive gain at 1000 MHz.

15. Discussion and conclusions

The array performance follows well theoretical prediction and assures that the array realized gain is at least 20 dB over the frequency band of interest (MATLAB code in Appendix I: Theoretical and measured array gain pattern) . The gain degradation compared to the theory in Fig. 50 at 1 GHz is due to feeding network losses, which become especially important at the upper band edge. The corresponding losses include the losses of the 4:1, 2:1, and 8:1 Wilkinson dividers in Figs. 30-32. Their performance was simulated in Ansoft HFSS; it is shown in Fig. 27 that follows. The estimated divider loss at 1 GHz is 0.7+1+2=3.7dB. Another 1.5 dB is coming from cable adapters; the sum of those two numbers convincingly explains the deviation between theory and experiment in Fig. 50. Using a low loss substrate instead of the 130 mil FR4 would allow one to reduce the realized gain loss by about 3 dB.

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Appendix I MATLAB Script

Theoretical and measured array gain pattern

```
%Theoretical and measured array gain pattern

clc;clear all;

FullData1           = csvread('HFSS_Gain_Hplane_500MHz.CSV');
FullData2           = csvread('HFSS_Gain_Hplane_1000MHz.CSV');

Theta_500           = FullData1(:,1);
Theta_1000          = FullData2(:,1);
Gain_dB_500         = FullData1(:,2);
Gain_dB_1000        = FullData2(:,2);
X1 = vertcat(Theta_500(91:180,1)-360,Theta_500(1:91,1));
Y1 = vertcat(Gain_dB_500(91:180,1),Gain_dB_500(1:91,1));
X2 = vertcat(Theta_1000(91:180,1)-360,Theta_1000(1:91,1));
Y2 = vertcat(Gain_dB_1000(91:180,1),Gain_dB_1000(1:91,1));

%   finite array directive gain  pattern
f1   = 0.5e9;
f2   = 1.0e9;
M   = 8;
N   = 8;
dx  = 0.24;
dy  = 0.24;
%   dimensionless parameters and angle theta
lambda1 = 3e8/f1;
lambda2 = 3e8/f2;
drx1 = 2*pi*dx/lambda1;
dry1 = 2*pi*dy/lambda1;
drx2 = 2*pi*dx/lambda2;
dry2 = 2*pi*dy/lambda2;
theta0 = [-90:1:90];            % deg
theta  = theta0*pi/180 + eps;   % rad
%   directive gain
y1 = 0.5*N*dry1*sin(theta);
D1 = 10*log10(N*M*4*pi*dx*dy/lambda1^2*(sin(y1)./y1).^2);
y2 = 0.5*N*dry2*sin(theta);
D2 = 10*log10(N*M*4*pi*dx*dy/lambda2^2*(sin(y2)./y2).^2);
%   plot

figure
plot(theta0, D1, 'r', 'LineWidth', 2); grid on; hold on;
plot(X1,Y1, 'b', 'LineWidth', 2)
title('H-plane gain at 500 MHz, theory (red) vs. numerical (blue)');
xlabel('\theta, \circ')
ylabel('Gain, dB')
axis([-90 90 min(Gain_dB_500) max(Gain_dB_500)])
set(gca,'XTick',-90:20:90)
```

```
grid on

figure
plot(theta0, D2, 'r', 'LineWidth', 2); grid on; hold on;
plot(X2,Y2, 'b', 'LineWidth', 2)
title('H-plane gain at 1000 MHz, theory (red) vs. numerical (blue)');
xlabel('\theta, \circ')
ylabel('Gain, dB')
axis([-90 90 min(Gain_dB_1000) max(Gain_dB_1000)])
set(gca,'XTick',-90:20:90)
grid on
```

Path loss estimation received power

```
%Path loss estimation received Power

clear all; clc;
PT = (10^(15/10))/1000 %    ok
GT = 10^(7.5/10)
GR = 10^(7.5/10)
f0 = 0.5e9;
c0 = 3e8;
lambda = c0/f0;
R = [ 33.3204,   33.3466,   33.3728,   33.3991,   33.4256,   33.4521,
33.4786,   33.5053,   33.5321,   33.5589,   33.5859 ];
PR = (GT*GR*PT*(lambda^2))./(4.*pi.*R).^2
PR_dBm = 10*log10(1000*PR)
```

Microstrip average power handling

```
% AVERAGE AND PEAK POWER-HANDLING CAPABILITY OF MICROSTRIP LINE
% Analysis taken from :Bahl, I.J. and K.C. Gupta, " Average Power Handling
Capability of
% Microstrip Lines," IEE Jour. on Microwaves, Optics and Acoustics, January,
1979
% Adapted for MATLAB by Daniel Harty, November, 06, 2009
% FR4 substrate with characteristic impedances of Z01 = 50 Ohm (input/output
ports), Z02 = 70.71 Ohm (quarter-wave line)
clear all;clc;
format long;
pc = 1.724e-8;
% Resistivity of copper strip conductor, Ohm-m
e0 = 1/(36*pi*1e9);
% electric permittivity of free space
u0 = 4*pi*1e-7;
% magnetic permeability of free space
c0 = 299792458;
% speed of light in a vacuum
f = 0:1e6:2e9;
% Operational frequency range
LOSS_TAN = 0.015;
% Loss tangent of substrate (FR4)
LAMBDA_0 = c0./f;
% Free space wavelength
D_B = 1000;
% Dielectric breakdown voltage (FR4), V/mil
Kd = 0.36;
% Thermal conductivity of substrate (FR4), W/mC
Ka = 0.0240;
% Thermal conductivity on air, W/mC
Tmax = 140;
% FR4 maximum substrate operating, deg C
Tamb = 25;
% Ambient temperature, deg C
SIGMA_c = 5.813e7;
% Conductivity of copper strip conductor, S/m @ 20 deg C
MIL_d = 125;
% Height of substrate, mil
MIL_c = 2.4;
% Thickness of microstrip line, mil
V0 = D_B*MIL_d;
% Maximum voltage the line can withstand
Z01 = 50;
% Characteristic impedance Z01 of microstrip line, Ohms
Z02 = 70.17;
% Characteristic impedance Z02 of microstrip line, Ohms
t = 0.0254*MIL_c*1e-3;
% Thickness of microstrip line, m
h = 0.0254*MIL_d*1e-3;
% Substrate height, m
eps_r = 4.4;
% Static relative dielectric constant of FR4
```

```
A1 = (Z01./60).*(sqrt((eps_r+1)./2))+((eps_r-
1)./(eps_r+1)).*(0.23+0.11./eps_r);
W1 = h.*(8.*exp(A1)./(exp(2.*A1)-2));
% Width of microstrip line, m
A2 = (Z02./60).*(sqrt((eps_r+1)./2))+((eps_r-
1)./(eps_r+1)).*(0.23+0.11./eps_r);
W2 = h.*(8.*exp(A2)./(exp(2.*A2)-2));
eps_r_ = Kd./Ka;
% Ratio of thermal conductivity of the dielectric to that of air
C1_ = ((eps_r_-1)./(4.6)).*((t./h)./(sqrt(W1./h)));
C2_ = ((eps_r_-1)./(4.6)).*((t/h)./(sqrt(W2./h)));
eps_re1_ = (eps_r_+1)./2 + ((eps_r_-1)./2).*((1+12./(W1./h)).^(-1/2)) - C1_ ;
% Effective relative permittivity, eps_r_ = Kd/Ka
eps_re2_ = (eps_r_+1)./2 + ((eps_r_-1)./2).*((1+12./(W2./h)).^(-1/2)) - C2_ ;
We1_h = W1./h + (1.25./pi).*(t./h).*(1 + log((2.*h)./t));
% (W/h)>(1/2*pi)
We2_h = W2./h + (1.25./pi).*(t./h).*(1 + log((2.*h)./t));
Z01_ = ((120.*pi)./(sqrt(eps_re1_))).*((We1_h) + 1.393 + 0.667.*log(We1_h
+1.444)).^(-1);   % Characteristic impedance of microstrip in Ohms, eps_r_ =
Kd/Ka
Z02_ = ((120.*pi)./(sqrt(eps_re2_))).*((We2_h) + 1.393 + 0.667.*log(We2_h
+1.444)).^(-1);
Za01 = (Z01_.*sqrt(eps_re1_));
Za02 = (Z02_.*sqrt(eps_re2_));
We1 = (120.*pi.*h)./Za01;
% Equivalent width of the strip
We2 = (120.*pi.*h)./Za02;
C1 = ((eps_r-1)./(4.6)).*((t./h)./(sqrt(W1./h)));
C2 = ((eps_r-1)./(4.6)).*((t./h)./(sqrt(W2./h)));
eps_re1 = (eps_r+1)./2 + ((eps_r-1)./2).*((1+12./(W1./h)).^(-1/2)) - C1;
% Effective relative permittivity, eps_r = 4.4
eps_re2 = (eps_r+1)./2 + ((eps_r-1)./2).*((1+12./(W2./h)).^(-1/2)) - C2;
Rs = sqrt(pi*f*u0*pc);
B = h;
W1_ = W1 + ((1.25.*t)./pi).*(1 + log((2.*B)./t));
W2_ = W2 + ((1.25.*t)./pi).*(1 + log((2.*B)./t));
Y1 = (1 +(h./W1_).*(1 + ((1.25.*t)./(pi.*W1)) +
(1.25./pi).*log((4.*pi.*W1)./t)));
Y2 = (1 +(h./W2_).*(1 + ((1.25.*t)./(pi.*W2)) +
(1.25./pi).*log((4.*pi.*W2)./t)));
alpha_c1 = (6.1e-5).*((Rs.*Z01.*eps_re1)./h).*((W1_./h) +
((0.667.*(W1_./h))./((W1_./h) + 1.444))).*Y1;% Conductor attenuation
constant, dB/unit length
alpha_c2 = (6.1e-5).*((Rs.*Z02.*eps_re2)./h).*((W2_./h) +
((0.667.*(W2_./h))./((W2_./h) + 1.444))).*Y2;
alpha_d1 = 27.3.*(eps_r./(eps_re1)).*((eps_re1-1)./(eps_r-
1)).*(LOSS_TAN./LAMBDA_0);             % Dielectric attenuation constant,
dB/unit length
alpha_d2 = 27.3.*(eps_r./(eps_re2)).*((eps_re2-1)./(eps_r-
1)).*(LOSS_TAN./LAMBDA_0);
DELTA_Pc1 = 1-exp(-0.2303*alpha_c1);
% Conductor loss in the line when 1 W of power is incident, W/m
DELTA_Pc2 = 1-exp(-0.2303*alpha_c2);
DELTA_Pd1 = 1-exp(-0.2303*alpha_d1);
% Dielectric loss in the substrate when 1 W of power is incident, W/m
DELTA_Pd2 = 1-exp(-0.2303*alpha_d2);
Weff_01 = (377*h)/(Z01*sqrt(eps_re1));
```

```
Weff_02 = (377*h)/(Z02*sqrt(eps_re2));
fp1 = Z01/(2*u0*h);
fp2 = Z02/(2*u0*h);
Weff_f1 = W1 + (Weff_01 - W1)./(1 +(f./fp1).^2);
Weff_f2 = W2 + (Weff_02 - W2)./(1 +(f./fp2).^2);
DELTA_T1 = (h/Kd)*((DELTA_Pc1/We1)+DELTA_Pd1./(2*Weff_f1));
% Rise in temperature per Watt, deg C/W
DELTA_T2 = (h/Kd)*((DELTA_Pc2/We2)+DELTA_Pd2./(2*Weff_f2));
Pavg1 = (Tmax-Tamb)./DELTA_T1;
% Maximum average power for microstrip line, <W>
Pavg2 = (Tmax-Tamb)./DELTA_T2;
Pp1 = (V0^2)/(2*Z01_)
Pp2 = (V0^2)/(2*Z02_)
figure
semilogy(f./1e6,Pavg1,'k','LineWidth', 3)
hold on
semilogy(f./1e6,Pavg2,'k','LineWidth', 3)
title(['Maximum average power-handling capability for Z_0_1 and Z_0_2
microstrip lines'],'FontSize',18 )
xlabel(['Frequency, MHz'],'FontSize',18 )
ylabel(['Maximum Average Power, W'],'FontSize',18 )
grid on

figure
semilogy (f./1e6,DELTA_T1,'k','LineWidth',3)
hold on
semilogy(f./1e6,DELTA_T2,'k','LineWidth',3)
title(['Strip conductor temperature rise per unit power flow, Z_0_1 and Z_0_2
microstrip lines'],'FontSize',18)
xlabel(['Frequency, MHz'],'FontSize',18)
ylabel(['\DeltaT, deg C/W'],'FontSize',18 )
grid on
```

Surface wave effects and higher order modes in microstrips

```
% Calculation of surface wave effects and higher order modes in microstrip
% substrates
clear all; clc;
W = 6e-3;
h = 0e-3:1e-4:5e-3;
c = 299792458;
eps_r = [2.1 3.2 4.4]
figure
hold on
grid on
for i=1:3
fc = c./(sqrt(eps_r(i)).*(2*W+0.8.*h));
if i == 1
    plot(h/1e-3,fc/1e9,'b','LineWidth',2)
elseif i == 2
    plot(h/1e-3,fc/1e9,'g','LineWidth',2)
else
    plot(h/1e-3,fc/1e9,'r','LineWidth',2)
end
end
line([1.5748 1.5748],[0 20],'LineWidth', 2);
line([3.175 3.175],[0 20],'LineWidth', 2);
title('Cutoff frequency vs. substrate thickness (1st higher order mode)')
xlabel('Substrate thickness h, mm')
ylabel('Cutoff Frequency f_c, GHz')

h = 1e-3:1e-4:5e-3;
figure
hold on
grid on
for i=1:3
fc = c*atan(eps_r(i))./(sqrt(2).*pi.*h.*sqrt(eps_r(i)-1));
if i == 1
    plot(h/1e-3,fc/1e9,'b','LineWidth',2)
elseif i == 2
    plot(h/1e-3,fc/1e9,'g','LineWidth',2)
else
    plot(h/1e-3,fc/1e9,'r','LineWidth',2)
end
end
line([1.5748 1.5748],[0 75],'LineWidth', 2);
line([3.175 3.175],[0 75],'LineWidth', 2);
axis([1 5 0 75])
title('Threat frequency vs. substrate thickness (lowest surface wave mode)')
xlabel('Substrate thickness h, mm')
ylabel('Threat Frequency f_s, GHz')

h = 0e-3:1e-4:5e-3;
figure
grid on
hold on
eps_r = 4.4;
```

```
W = [1e-3 3e-3 6e-3];
for i=1:3
fc = c./(sqrt(eps_r).*(2*W(i)+0.8.*h));
if i == 1
    plot(h/1e-3,fc/1e9,'b','LineWidth',2)
elseif i == 2
    plot(h/1e-3,fc/1e9,'g','LineWidth',2)
else
    plot(h/1e-3,fc/1e9,'r','LineWidth',2)
end
end
line([1.5748 1.5748],[0 80],'LineWidth', 2);
line([3.175 3.175],[0 80],'LineWidth', 2);
title('Cutoff frequency vs. substrate thickness (1st higher order mode)')
xlabel('Substrate thickness h, mm')
ylabel('Cutoff Frequency f_c, GHz')
```

Appendix II Data Sheets

Type N connectors

Named after Paul Neill of Bell Labs after being developed in the 1940's, the Type N offered the first true microwave performance. The Type N connector was developed to satisfy the need for a durable, weatherproof, medium-size RF connector with consistent performance through 11 GHz.

There are two families of Type N connectors: Standard N (coaxial cable) and Corrugated N (helical and annular cable). Their primary applications are the termination of medium to miniature size coaxial cable, including RG-8, RG-58, RG-141, and RG-225. RF coaxial connectors are the most important element in the cable system. Corrugated copper coaxial cables have the potential to deliver all the performance your system requires, but they are often limited by the performance of the connectors.

Intermodulation distortion, a major concern in today's communications systems, is consistently low with corrugated cable connectors. Typical performance is -125 dBm (-168 dBdc). In-house IMD measurement capability gives Amphenol the unique ability to understand the effects of connector design elements on IMD generation and to design the best performing connectors in the industry. Self-flaring designs are easily attached with standard hand tools in the field, and are highly resistant to pull off and twist off. All corrugated cable connectors are optimally matched to their cables for low VSWR and insertion loss.

Features & Benefits

- Accommodates a wide range of medium to miniature-sized RG coaxial cables in a rugged medium-sized design
- Broad line of Military (M39012), Industrial (UG) and Commercial (RFX) grade products available, giving customers choices in weighing cost versus performance benefits
- Meets many customer application demands with plug styles available in straight and right angle and jack styles available in panel mount, bulkhead mount, and receptacle

Applications

- Antennas
- Base stations
- Broadcast
- Cable assemblies
- Cellular
- Components
- Instrumentation
- Microwave Radio
- Mil-Aero
- PCS
- Radar
- Radios
- Satcom
- Surge Protection
- WLAN

Type N Standard Specifications

Electrical	
Impedance	50 Ω
Frequency Range	0 - 11 GHz
Voltage Rating	1,500 volts peak
VSWR	MIL-C-39012 straight connectors: 1.3 max 0-11 GHz MIL-C-39012 right angle connectors: 1.35 max 0-11 GHz
Dielectric Withstanding Voltage	2,500 volts rms
Insulation Resistance	5,000 MΩ minimum
Center Contact Resistance	1.0 mΩ
Outer Contact Resistance	0.2 mΩ
RF Leakage	-90 dB minimum at 3 GHz
Insertion Loss	.15 dB maximum at 10 GHz
Mechanical	
Mating	5/8-24 threaded coupling
Braid or Jacket Cable Affixment	All crimps: hex braid crimp Clamps: screw-thread nut and braid clamp
Center Conductor Cable Affixment	Crimp: crimp or solder All others: solder only
Captivated Contact	All crimps unless specified otherwise
Cable Retention	Crimps: 60-120 lbs Clamps: 30-70 lbs
Material	
Male Contacts	Brass, silver or gold plated
Female Contacts	Phosphorous bronze or beryllium copper, silver or gold plated
Other Metal Parts	Brass with ASTROplate® finish; M39012 has silver finish
Insulators	TFE, copolymer of styrene or glass-TFE (hermetic seal)
Weatherproof Gaskets	Silicone rubber of synthetic rubber
Crimp Ferrule	Copper
Environmental	
Temperature Range	TFE: -65°C to +165°C

Weatherproof	All series N with gaskets are weatherproof
Hermetic Seals	Pass helium leak test of 2x10-8 cc/sec
Pressurized Shock	Compression seal MIL-STD-202, method 213
Vibration	MIL-STD-202, method 204, test condition B
Moisture Resistance	MIL-STD-202, method 106
Corrosion	MIL-STD-202, method 101, test condition B
Temperature Cycling	MIL-STD-202, method 102, test condition C
Altitude	MIL-STD-202, method 105, test condition C
Millitary	
MIL-C-39012 MIL-A-55339	Where applicable

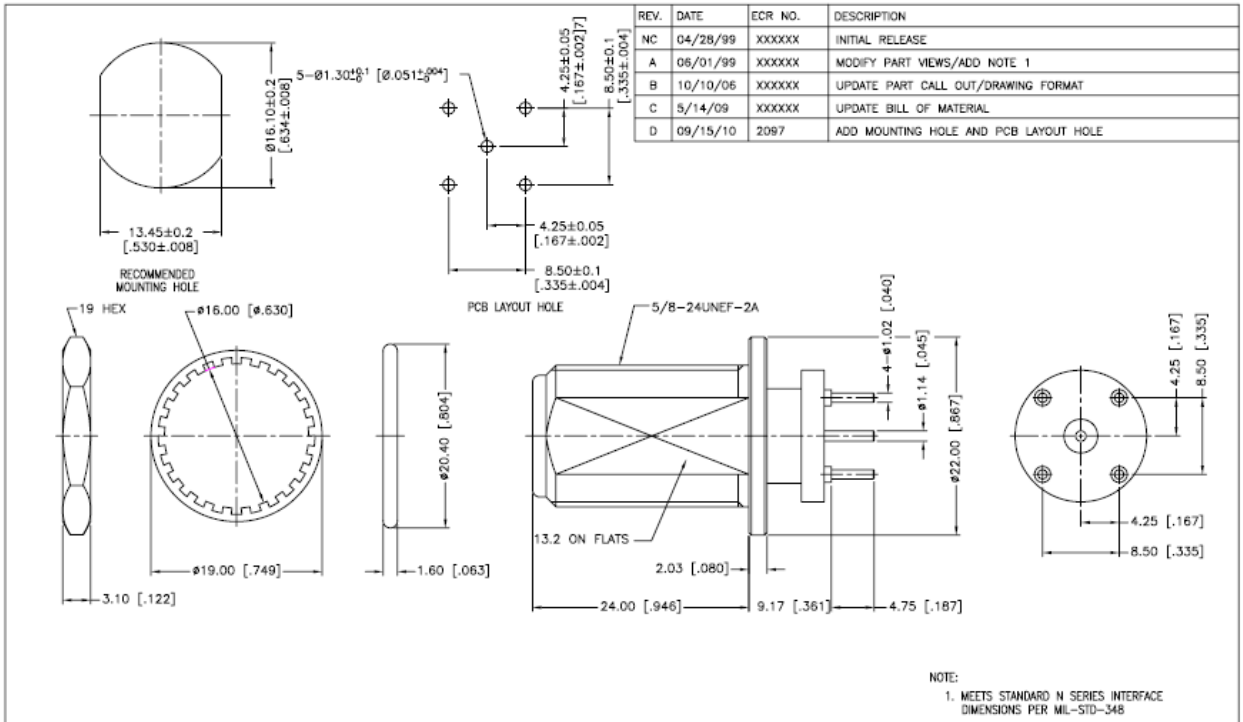
Note: These characteristics are typical but may not apply to all connectors.

Corrugated Type N Specifications

Electrical	
Impedance	50 Ω
Frequency Range	11.0 GHz
Return Loss	33 dB (1-2 GHz) 28 dB (2-3 GHz)
Operating Voltage	Maximum 707 rms
Dielectric Withstanding Voltage	2,000 vdc
Insulation Resistance	5,000 MΩ minimum
Insertion Loss	.05 frequency GHz
Shielding Effectiveness	Minimum 125 dB
Peak Power	Maximum 10 kW
Average Power	Maximum .60 kW
3rd Order IM Product	Typical -125 dBm (-168 dBc)
Mechanical	
Mating	MIL-STD-348
Inner Attachment Method	Solder or captivated
Outer Attachment Method	Compression
Assembly Torque	18/22 lb-ft (25/30 N-m)
Coupling Torque	15.00 lb-in (1.70 N-m)
Coupling Nut Retention Force	100.00 lbs (444.80 N)
Connector Durability	500 cycles, 12 cycles/minute

Material	
Body	Brass, silver plated
Outer Contacts	Brass, silver plated
Inner Contacts	Beryllium copper, gold plated
Other Metal Parts	Brass, silver plated
Insulators	TFE
Gaskets	Silicone rubber
Environmental	
Temperature Range	Operating: -40°C to +150°C Storage: -70°C to +100°C
Thermal Shock	MIL-STD-202, method 107, test condition A-1
Immersion	IEC 529, IP68
Vibration	MIL-STD-202, method 204, test condition B
Corrosion	MIL-STD-202, method 101, test condition B
Mechanical Shock	MIL-STD-202, method 213, test condition I

Note: These characteristics are typical but may not apply to all connectors.



REV.	DATE	ECR NO.	DESCRIPTION
NC	04/28/99	XXXXXX	INITIAL RELEASE
A	06/01/99	XXXXXX	MODIFY PART VIEWS/ADD NOTE 1
B	10/10/06	XXXXXX	UPDATE PART CALL OUT/DRAWING FORMAT
C	5/14/09	XXXXXX	UPDATE BILL OF MATERIAL
D	09/15/10	2097	ADD MOUNTING HOLE AND PCB LAYOUT HOLE

NOTE:
1. MEETS STANDARD N SERIES INTERFACE DIMENSIONS PER MIL-STD-348

	DESCRIPTION	MATERIAL	FINISH	QTY
8	HEX NUT	BRASS	NEXCOTE	1
7	LOCK WASHER	BRASS	NEXCOTE	1
6	GASKET	SILICONE	RED	1
5	PIN	BRASS	BRIGHT TIN	1
4	INNER BODY	BRASS	NEXCOTE	1
3	CONTACT PIN	BER. COPPER	GOLD	1
2	INSULATOR	PTFE	NATURAL	1
1	BODY	BRASS	NEXCOTE	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN [ ] ARE IN INCHES AND FOR CUSTOMER REFERANCE ONLY.

UNLESS OTHERWISE SPECIFIED TOLERANCES FOR MILLIMETERS ARE:
0.5 – 6mm ± 0.20mm
6 – 30mm ± 0.40mm
30 – 120mm ± 0.50mm

UNLESS OTHERWISE SPECIFIED TOLERANCES FOR INCHES ARE:
.020 – .315 = ± 0.007"
.315 – 1.180 = ± 0.015"
1.180 – 4.724 = ± 0.020"

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN M.ZHANG	09/15/10
CHECKED	
ISSUED	
SHEET 1 OF 1	

CAD FILE C:/CONNEX/172243.DWG

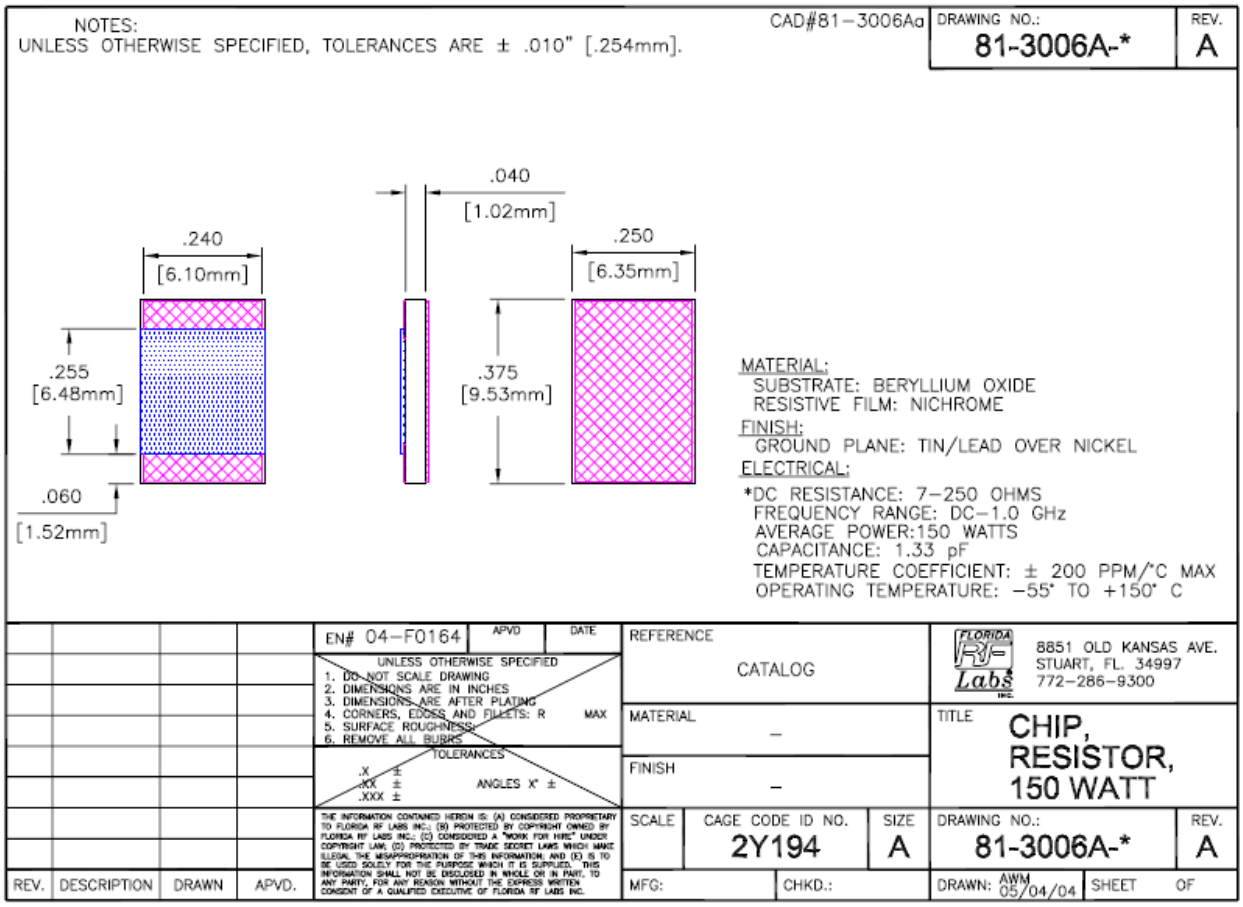
Amphenol Connex

PART DESCRIPTION: N BULKHEAD PCB MOUNT RECEPT. JACK

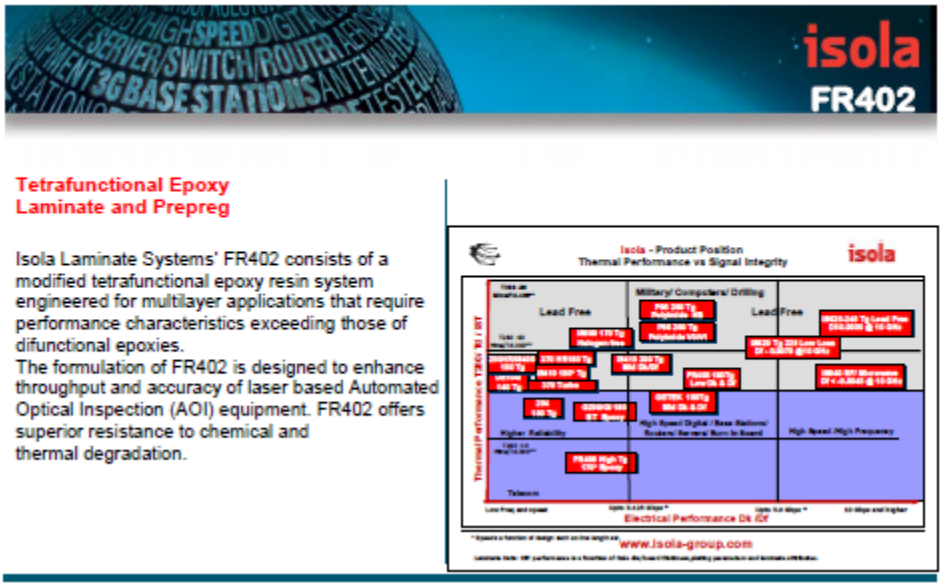
PART NO. 172243

DWG. NO. 172243.DWG | REV. D | SIZE A | SCALE NA

Power divider isolation chip resistor



FR-4 substrate



Performance and Processing Advantages

- **High Tg — 140 °C**
  Superior performance through multiple thermal Excursions Resistance to measling
  Extended capabilities
- **UV Blocking and AOI Compatible**
  Increased throughput and accuracy
  Compatible with all AOI equipment
- **FR-4 System**
  Processes as a standard FR-4

Purchasing Information

- **Industry Approvals**
  IPC-4101B /21
  UL Recognized – FR-4, File Number E41625
  (Part of Isola's FR-4 Family)
- **Availability**
  Thickness: 0.002" [.05 mm] to 0.125" [3.2 mm]
  Available in sheet or panel form

Copper Foil Cladding: Grade 3 (HTE), ½, 1 and 2 oz.

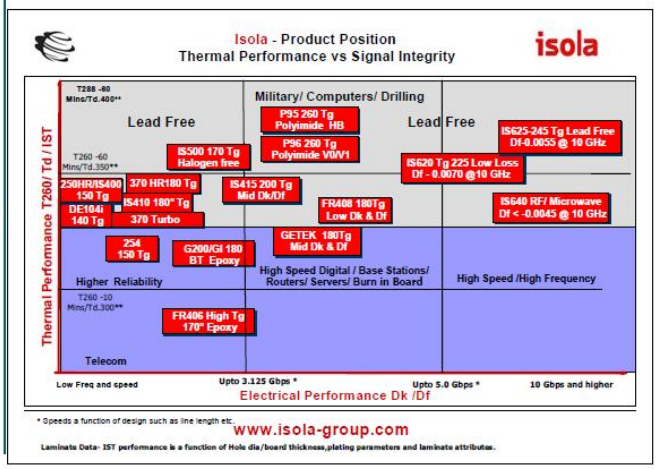
Foil Options: Double treat, reverse treat

Prepregs: Available in roll or panel form

Glass Styles: available on standard styles

Tetrafunctional Epoxy Laminate and Prepreg

Isola Laminate Systems' FR402 consists of a modified tetrafunctional epoxy resin system engineered for multilayer applications that require performance characteristics exceeding those of difunctional epoxies.
The formulation of FR402 is designed to enhance throughput and accuracy of laser based Automated Optical Inspection (AOI) equipment. FR402 offers superior resistance to chemical and thermal degradation.



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  IPC-4101B /21
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- **Availability**
  Thickness: 0.002" [.05 mm] to 0.125" [3.2 mm]
  Available in sheet or panel form

Copper Foil Cladding: Grade 3 (HTE), ½, 1 and 2 oz.

Foil Options: Double treat, reverse treat

Prepregs: Available in roll or panel form

Glass Styles: available on standard styles

FR402 Typical Laminate Properties

		English			Metric			Test Method
		Value	Specification	Units	Value	Specification	Units	IPC-TM-650 (or as noted)
Glass Transition Temperature (Tg) by DSC, spec minimum		140	110-150	°C	140	110-150	°C	2.4.25
Decomposition Temperature (Td) by TGA	@ 5% weight loss	320	—	°C	320	—	°C	ASTM D3850
T260 T288	Minutes	30 >5		min min	30 >5		min min	2.4.25
CTE, Z-axis	Pre-Tg	50	AABUS	ppm/°C	50	AABUS	ppm/°C	2.4.24
	Post-Tg	250	—		250	—		
CTE, X-, Y-axes	Pre-Tg	15	AABUS	ppm/°C	15	AABUS	ppm/°C	2.4.24
	Post-Tg	17	—		17	—		
Z-Axis Expansion (50 – 260C) %		4.2	AABUS	%	4.2	AABUS	%	2.4.24
Thermal Stress 10 Sec @ 288°C (550.4°F), spec minimum	Unetched	Pass	Pass Visual	Rating	Pass	Pass Visual	Rating	2.4.13.1
	Etched	Pass	Pass Visual		Pass	Pass Visual		
Dk (Permittivity, Laminate & prepeg as laminated) 1 Mhz (Fluid cell) 500Mhz and 1Ghz (HP4291)	1 Mhz	4.60	5.4	—	4.60	5.4	—	2.5.5.9
	500 Mhz	4.27	—		4.27	—		2.5.5.9
	1 Ghz	4.25	—		4.25	—		2.5.5.5
Df (Loss Tangent, Laminate & prepeg as laminated) 1 Mhz (Fluid cell) 500Mhz and 1Ghz (HP4291)	1 Mhz	0.016	0.035	—	0.016	0.035	—	2.5.5.3
	500 Mhz	0.015	—		0.015	—		2.5.5.9
	1 Ghz	0.015	—		0.015	—		2.5.5.5
Volume Resistivity, spec minimum	96/35/90	$4.0X10^5$	$1X10^4$	M° -cm	$4.0X10^5$	$1X10^4$	M° -cm	2.5.17.1
	After moisture resistance							
	At elevated temperature	$7.0X10^7$	$1X10^3$		$7.0X10^7$	$1X10^3$		
Surface Resistivity, spec minimum	96/35/90	$3.0X10^6$	$1X10^4$	M°	$3.0X10^6$	$1X10^4$	M°	2.5.17.1
	After moisture resistance							
	At elevated temperature	$6.0X10^6$	$1X10^5$		$6.0X10^5$	$1X10^5$		
Thermal Conductivity		0.36	—	W/mK	0.36	—	W/mK	ASTM D5930
Dielectric Breakdown, spec minimum		>50	40	kV	>50	40	kV	2.5.6
Arc Resistance, spec minimum		120	60	Seconds	120	60	Seconds	2.5.1
Electric Strength, spec minimum (Laminate & prepreg as laminated)		1100	736	V/mil	48000	29000	V/mm	2.5.6.2
Peel Strength, spec minimum	profile – all copper weights >17 microns	8	4	(lb/inch)	105	70	N/mm	2.4.8
	Standard profile copper							2.4.8.2
	-----1. After thermal stress	9	6		145	105		2.4.8.3
	2. At 125°C (257°F)	8	4		125	70		
	3. After process sssolutions	9	4.5		145	80		
Moisture Absorption, spec maximum		0.3	0.8	%	0.3	0.8	%	2.6.2.1
CTI			3	175-249 volts				
HWI			0					
HAI			3					
Max Operating Temp			130					
DSR			yes					