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Parameter Estimation of a High Frequency Cascode Low Noise Amplifier Model

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Parameter Estimation of a High Frequency Cascode Low Noise Amplifier Model

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Abstract

A Low Noise Amplifier (LNA) is an important building block in the RF receiver chain. Typically the LNA should provide acceptable gain and high linearity while maintaining low noise and power consumption. To optimize these conflicting goals the so-called Cascode topology is widely used in industry. Here the gain cell is comprised of two transistors, one in common-source and the other in common gate configuration. Cascode has a number of competitive advantages over other topologies such as high output impedance that shields the input device from voltage variations at the output, good reverse isolation resulting in improved stability, and acceptable input matching. Moreover, the topology features excellent frequency characteristics .

Unfortunately, a Cascode design is expensive to deploy in RF systems and it requires more careful tuning and matching. Since the design relies on many circuit components, optimization methods are generally difficult to implement and often inaccurate in their predictions. To overcome these problems, this thesis proposes a modeling environment within the Advanced Design Systems (ADS) simulator that utilized DC and RF measurements in an effort to characterize each transistor separately. The model creates an easy-to-apply design approach capable of predicting the most important circuit components of the Cascode topology. The validity of the method is tested in ADS with a realistic p-HEMT library device. The comparison between model prediction and the realistic device involves both standard transistor parameters and high-frequency parasitic effects.

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1. Background

An RF transceiver typically includes a Low Noise Amplifier (LNA), mixer, filter, power amplifier and more. The LNA is one of the most important building blocks in this RF receive chain. The LNA amplifies the weak signal from the antenna and duplex filter without adding too much noise to the overall system. Since the LNA is the first stage in the receive path, its noise figure influences significantly to the system performance. Aside from providing gain, while adding as little noise as possible, the LNA should also have high linearity. To meet the RF front end requirement, the LNA should have enough gain to amplify the received signal with little distortion, add low inherent noise, and match the input and output ports with unconditional stability [1].

Most LNAs use so-called Cascode topologies [2]. In a typical Cascode topology, a single-stage is comprised of two transistors, one having a common-source and the other having a common gate configuration. The Cascode LNA has high output impedance and can shield the input device from voltage variations at the output. Furthermore, it consumes low power because it has only one path from the supply voltage to ground. Also, the topology is the best in terms of linearity, a feature attributed to the common gate transistor. Moreover, It has superior frequency characteristics, since it has smaller Miller capacitance.

Unfortunately, Cascode designs are more expensive and require more careful tuning and matching. Also, building a Cascode LNA model requires many components; thus optimization methods for Cascode are generally difficult and often inaccurate.

Tsironis and Meierer [3] have proposed an accurate modeling method which utilizes DC and microwave measurements to characterize each FET separately under different bias conditions. With 28 circuit elements, it is fairly complex. They report results for the GaAs dual-gate MESFETs at microwave frequencies between 2 and 11 GHz.

Scott and Minasian [4] presented a new simple and efficient modeling procedure. Their Cascode model relies on 14 elements, and efficient analytical techniques for parameter evaluation were developed. Previous work by Minasian has shown that the conventional single-

gate FET model can be reduced to the simplified form with little loss of accuracy for frequencies up to 12 GHz. This simplified circuit has the advantage that all the element values may be determined directly from microwave measurements. Their methods have been used to model a dual-gate MESFET where both FET transistors are in saturation, and good agreement between measured and calculated S-parameters were achieved over a multi-octave frequency range (2-11 GHz) without using numerical optimization.

Deng and Chu [5] use a similar method to construct a Cascode LNA model. They deploy RF and DC measurements to initially extract the element values. These values were manually optimized to get more accurate results. The elements for the extrinsic series resistance were determined by considering the distributed channel resistance under the two gate regions. The "end resistance measurement" method [6] was utilized to estimate the components. For the extrinsic capacitance and inductance, they used three-port Y-matrix and Z-matrix calculations from cold measurements, which require the drain source voltage to be zero. The intrinsic elements of the Cascode MESFETs, which is biased properly to be two decoupled single-gate MESFETs, are extracted from hot measurement. The hot measurement means the drain source voltage is not zero.

Umoh and Kazmierski [7] have presented the first VHDL-AMS model for a grapheme field effect transistor using a System Vision simulator by Mentor Graphics. The model does not require numerical analysis and iterations thereby making it computationally efficient. Also, the model has been verified with experimental data and showed a good agreement [8].

2. Objective

This thesis proposes a circuit parameter estimation approach for an RF LNA in Cascode configuration. To have an accurate and rapid to apply model can help analyze the gain, linearity and noise performance of the circuit. Usually the way of building a Cascode low noise amplifier model is very complex and straightforward optimization may not work.

Thus, the overall objective of the thesis is to create an easy to apply inverse model that predicts the most important circuit components of the Cascode LNA model within the industry standard Advanced Design System (ADS) simulation environment.

3. Cascode low noise amplifier

3.1. LNA characteristics

Low noise amplifiers are widely used in many applications including cellular handsets, satellite communications and GPS receivers. A LNA is in the first stage in a receiver and dominates the noise performance of the overall system. It is required to provide adequate gain, input and output matching, and low noise figure (NF). Moreover, in many applications, low power consumption needs to be considered.

3.1.1. Single stage low noise amplifier (LNA)

A generic single-stage amplifier configuration embedded between input and output matching networks is shown in Fig.1.

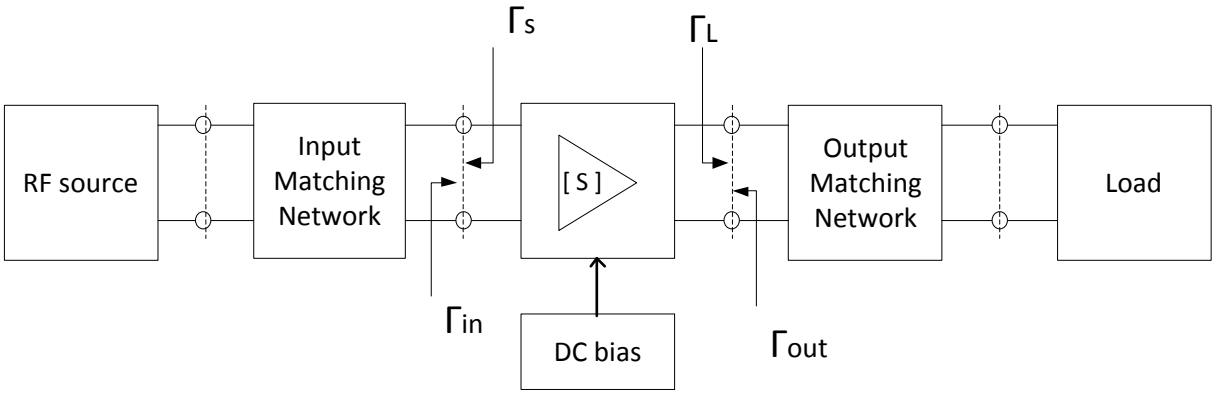


Figure 1: Generic LNA system.

In Fig.1, the amplifier is characterized through its S-parameter matrix at a particular DC bias point. The most useful gain definition for LNAs is the transducer power gain which accounts for both source and load mismatch.

$$G_T = \frac{(1-|\Gamma_L|^2)|S_{21}|^2(1-|\Gamma_s|^2)}{|1-\Gamma_s\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2} \qquad (1)$$

where Γ_{in}, Γ_s and Γ_L are input, source and load reflection coefficient, respectively.

3.1.2. Stability Consideration

One of the first requirements that a LNA must meet is stable performance. This is a particular concern when dealing with RF circuits, which tend to oscillate depending on operating frequency and termination. The criteria for unconditional stability [9] can be derived from S-parameters

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1 \quad (2)$$

$$|\Delta| < 1 \quad (3)$$

Where $\Delta = S_{11}S_{22} - S_{12}S_{21}$.

3.1.3. Noise Figure

In many LNAs, the need for signal amplification at low noise level becomes an essential system requirement. The generated noise of a two-port network can be quantified by investigating the decrease in the signal-to-noise (SNR) from the input to the output. The noise figure F is defined as the ratio of the input SNR to the output SNR. For a two-port amplifier, the noise figure can be stated in the admittance form:

$$F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2 \quad (4)$$

where F_{min} is the minimum noise figure, R_n is the equivalent noise resistance of the device, Y_{opt} is the optimum source admittance, G_s is the source conductance and Y_s is the source admittance.

3.2 Cascode Low noise amplifier (LNA) topologies

Cascode topologies are widely used in low noise amplifiers design, since they have very competitive features over other configurations. There are four broad types as depicted in Fig. 2.

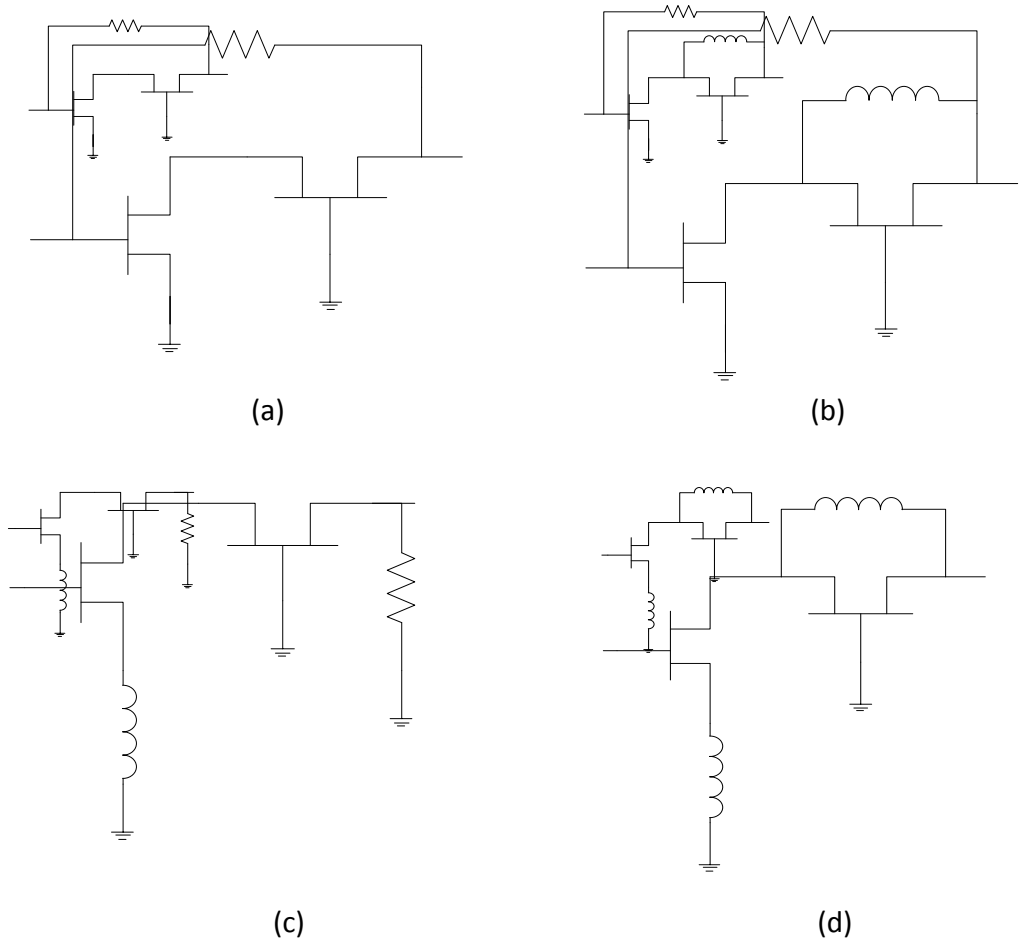


Figure 2: (a) Resistive parallel feedback. (b) Resistive parallel feedback with common gate inductive feedback. (c) Series inductive and series resistive feedback. (d) Inductive series feedback with common gate inductive feedback [2].

The first one is the Cascode resistive parallel feedback, which is shown in Fig.2. (a). This schematic utilizes the inherent advantages of the Cascode configuration such as high gain, wide bandwidth, and gain-controllability via a resistive parallel feedback, which allows for

better linearity, better stability, and insensitivity against parameter variation. The second one is a resistive parallel feedback with common gate inductive feedback as in Fig.2. (b). This configuration becomes very useful at higher frequencies because the common gate parallel feedback can reduce the noise contribution from the common gate stage. The third one is the Cascode inductive series feedback in Fig.2 (c). The simultaneous matching of Γ_{opt} and ${S_{11}}^*$ can be obtained with inductive series feedback and proper loading using a common source topology [2]. However, the gain becomes considerably lower due to the series feedback and small loading impedance, and poor output VSWR is inevitable. Fig. 2.(d) is the combination of the common source inductive series feedback and the common gate inductive parallel feedback. This configuration utilizes the merits of both inductive series feedback and common gate inductive parallel feedback. In other words, the simultaneous noise and input power matching is obtained by inductive series feedback, and both the minimization of noise added from the common gate stage and good stability are obtained by inductive parallel feedback.

Cascode series inductive feedback Fig. 2.(c), and Cascode series inductive feedback with common gate inductive feedback Fig. 2.(d) both show good return loss. Considering the bandwidth, stability, and insensitivity against parameter variation, Cascode resistive feedback Fig. 2.(a) and resistive parallel feedback with common gate inductive feedback Fig. 2.(b) are also good configurations. Overall, Fig. 2.(c) and Fig. 2.(d) are regarded as the best choices for Cascode LNAs at 2 GHz [2].

3.3 Transistor Models

3.3.1. RF Field Effect Transistors

Field effect transistors (FETs) are monopolar devices, meaning that only one carrier type, either holes or electrons, contributes to the current flow through the channel. If the hole contributions are involved we speak of p-channel, otherwise of n-channel FETs. Moreover, the FET is a voltage-controlled device. A variable electric field controls the current flow from the source to the drain by changing the applied voltage on the gate. Usually, FETs are classified into four types:

1. Metal Insulator Semiconductor FET (MISFET). The gate is separated from the channel through an insulation layer. The Metal Oxide Semiconductor FET (MOSFET) belongs to this class.
2. Metal Semiconductor FET (MESFET). If the reverse biased pn-junction is replaced by a Schottky contact, the channel can be controlled as in the Junction FET case.
3. Junction FET (JFET). This type relies on a reverse biased pn-junction that isolates the gate from the channel.
4. Hetero FET. Hetero structures utilize abrupt transitions between layers of different semiconductor materials. The High Electron Mobility Transistor (HEMT) belongs to this class [9].

MISFETs and JFETs have a relatively low cutoff frequency and are usually operated in low and medium frequency ranges of typically up to 1 GHz. GaAs MESFETs find applications up to 60-70 GHz, and HEMT can operate beyond 100 GHz. Because of the importance in RF and MW amplifier, mixer, and oscillator circuits, we focus our analysis on the MESFET shown in Fig.3-1.

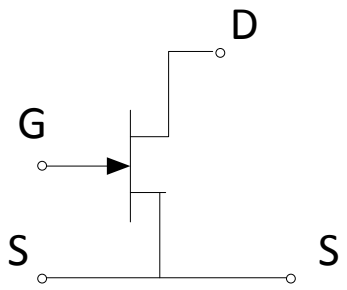


Figure 3: N-channel MESFET circuit symbol.

The saturation drain current I_{Dsat} is often approximately by the relation [9]

$$I_{Dsat} = I_{DSS}(1 - \frac{V_{GS}}{V_{T0}})^2 \qquad (5)$$

where I_{DSS} is the maximum drain current, V_{T0} is the threshold voltage and V_{GS} is the gate source voltage.

Figure 4 shows the typical transfer characteristic for MESFETs.

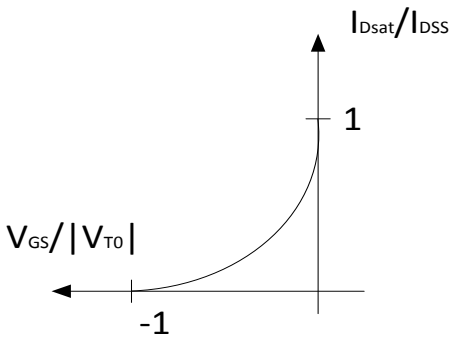


Figure 4: Transfer characteristic

The maximum saturation current is obtained when V_{GS} = 0, which we define as $I_{Dsat}(V_{GS}=0) = I_{DSS}$. In Fig.5, the typical input-output transfer as well as the output characteristic behavior is shown.

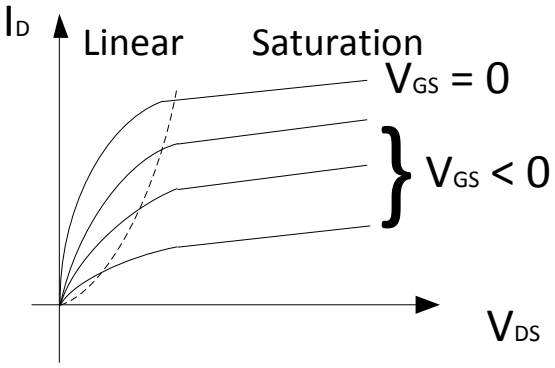


Figure 5: FET output characteristic.

FETs offer many advantages, but also have a number of disadvantages over BJTs. FETs usually exhibit a better temperature behavior, superior noise performance and low power consumption. The drain current of a FET shows a quadratic functional behavior compared with the exponential collector current curve of a BJT. But FETs generally possess lower gain. Because of the high input impedance, it is more difficult to construct matching networks. The power handling capabilities tend to be inferior compared with BJTs.

3.3.2 Large-Signal FET models

Our modeling purposes focus on the noninsulated gate FET. To this group, we count MESFET which are often identified as GaAs FET and the HEMT. In Fig. 6, the n-channel depletion mode MESFET model is shown.

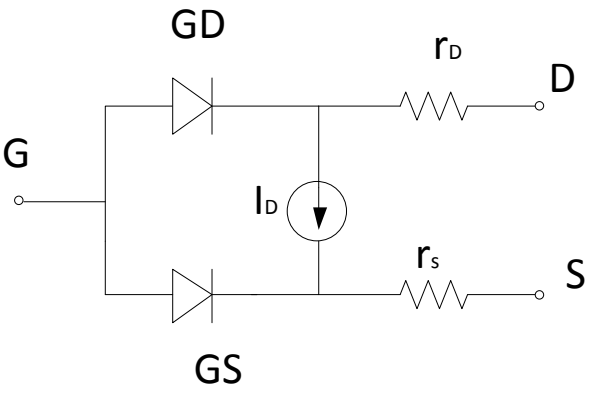


Figure 6: Static n-channel MESFET model.

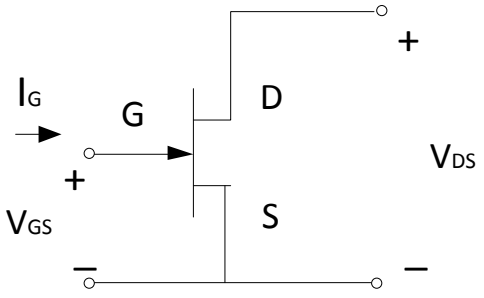


Figure 7: N-channel MESFET symbol.

Depending on the value of V_{DS}, The FET works in four regions which are saturation region, linear region, reverse saturation region and reverse linear region.

(1) Saturation region ($V_{DS} \geq V_{GS} - V_{T0} > 0$)

The saturation drain current equation is a function of V_d and is shown in eq.(6).

$$I_{Dsat} = G_0 \frac{V_P}{3} \left(\frac{3}{4}\right) \left(\frac{V_{GS} - V_{T0}}{V_p}\right)^2 \qquad (6)$$

where G_0 is the gain, V_p is the pinch-off voltage.

The constant factors in front of the square term in (6) are combined to form the conduction parameter β_n

$$\beta_n = \frac{1}{4}\left(\frac{G_0}{V_p}\right) = \frac{\mu_n \varepsilon Z}{2Ld} \tag{7}$$

If the channel modulation effect is included, we arrive at

$$I_D = \beta_n (V_{GS} - V_{T0})^2 (1 + \lambda V_{DS}) \tag{8}$$

(2) Linear region ($0 < V_{DS} < V_{GS} - V_{T0}$)

The channel modulation is considered to achieve a smooth transition from the linear into the saturation region.

$$I_D = \beta_n [2(V_{GS} - V_{T0})V_{DS} - {V_{DS}}^2](1 + \lambda V_{DS}) \tag{9}$$

(3) Reverse saturation region ($-V_{DS} \geq V_{GD} - V_{T0} > 0$)

$$I_D = -\beta_n (V_{GD} - V_{T0})^2 (1 - \lambda V_{DS}) \tag{10}$$

(4) Reverse linear region ($0 < -V_{DS} < V_{GD} - V_{T0}$)

$$I_D = \beta_n [2(V_{GD} - V_{T0})V_{DS} - {V_{DS}}^2](1 + \lambda V_{DS}) \tag{11}$$

The dynamic FET model usually includes the gate-drain and gate-source capacitances. Also shown in the model are source and drain resistors associated with source-gate and drain-gate channel resistances. A gate resistor is not included because the metallic gate connection represents a low resistance.

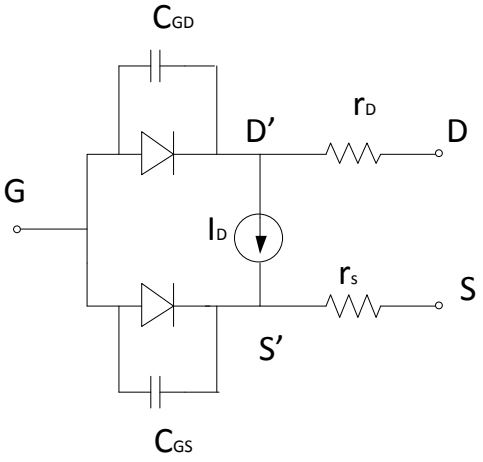


Figure 8: Dynamic FET model.

3.3.3 Small-Signal FET models

A small-signal FET model can be derived from the large-signal FET model by replacing the gate-drain and the gate-source diodes with their small-signal representations. Moreover, the voltage-controlled current source is modeled via a transconductance g_m and a shunt conductance $g_0 = 1/r_{ds}$. The small signal model is shown in Fig.9.

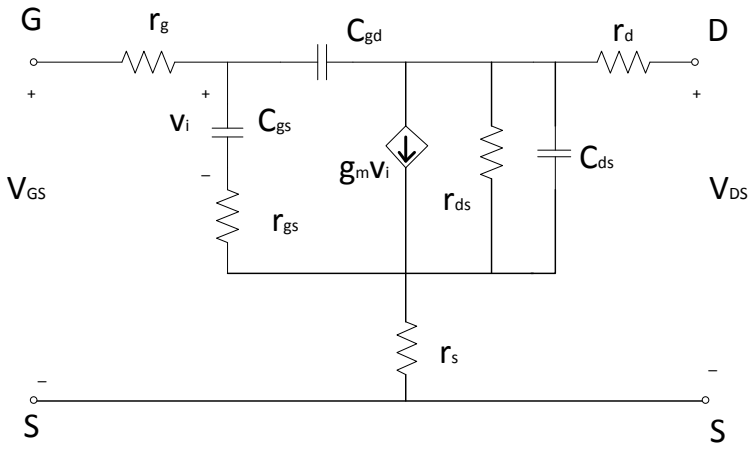


Figure 9: Small signal MESFET model

This model can be described by a two-port Y parameter network in the form

$$i_g = y_{11}v_{gs} + y_{12}v_{ds} \tag{12}$$

$$i_d = y_{21}v_{gs} + y_{22}v_{ds} \tag{13}$$

Under low frequency conditions, the input conductance of y_{11} and the feedback conductance of y_{12} are very small and thus can be neglected. However, for high frequency operation, the capacitance are typically included. For DC and low-frequency operation, the model in Fig.3-7 simplifies to the condition where the input is completely decoupled from the output. Transconductance g_m and output conductance g_0 can be computed for the forward saturation region from the drain current equation.

$$y_{21} = g_m = \frac{dI_D}{dV_{GS}}\bigg|_Q = 2\beta_n(V_{GS}^Q - V_{T0})\,(1 + \lambda V_{DS}^Q) \tag{14}$$

$$y_{22} = \frac{1}{r_{ds}} = \frac{dI_D}{dV_{DS}}\Big|_Q = \beta_n \lambda (V_{GS}^Q - V_{T0})^{\,2} \qquad (15)$$

where V_{GS}^Q and V_{DS}^Q denote the operating points.

The gate-source and gate-drain capacitances play an important role in determining the frequency performance. The transition frequency is given by

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \qquad (16)$$

One of the first MESFET models implemented in the simulator tools was the Curtice FET model. The model is very simple, but includes all important transistor parameters, such as pinch off voltage, transconductance parameter *β,* etc. The model describes well the transconductance and gain with the parameter *β*, output conductance via parameter *λ* etc. Due to its simplicity and easy to use and extract, the model shown in Fig.10 is widely deployed.

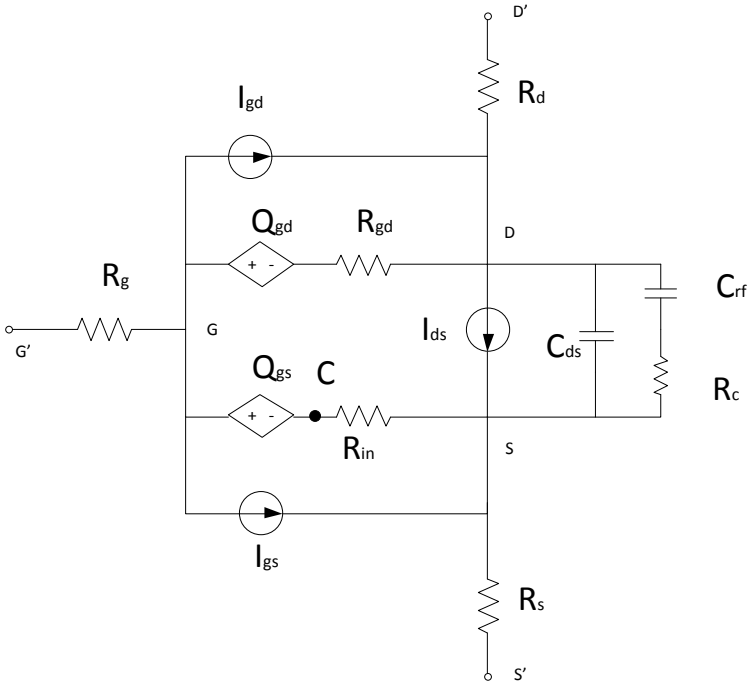


Figure 10: The Curtice 2 model schematic [18].

$$I_{ds} = \beta(V_{gs} - V_{t0})^2 \tanh(\alpha V_{ds})(1 + \lambda V_{ds}) \qquad (17)$$

Parameter β is the transconductance parameter, α define the slope of I_{ds} vs. V_{ds} in the linear region ($V_{ds} < V_{kn}$). λ is the slope in the saturated region ($V_{ds} > V_{kn}$). V_{t0} is the pinch-off voltage.

3.3.4. Cascode LNA models

The equivalent circuit of a Cascode MESFET is essential in the design of microwave circuits. In general, the Cascode MESFET is modeled as a cascaded circuit of two single –gate MESFETs. It is shown in Fig.11.

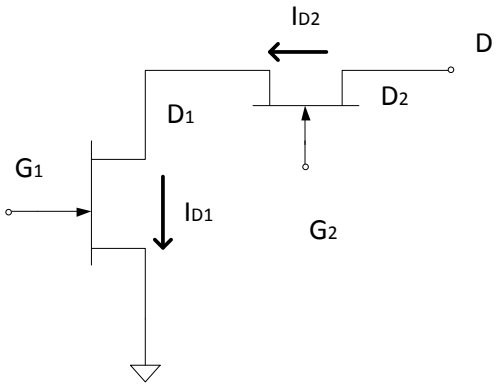


Figure 11: The schematic representation of the Cascode LNA

3.3.4.1 Physical modeling of the Cascode MESFET

Physical models are based on the device physics and usually describe the carrier transport mechanisms. They have the inherent ability to describe the operation of the device under any condition. It is this feature that makes a physical model particularly attractive for the modeling of the Cascode MESFET.

In order to understand the fundamental operation of the dual-gate FET, it is helpful to break down the device into simpler units. A dual-gate FET can be separated at the midpoint

between the first and the second gates into two series connected single-gate FETs. The characteristics of the composite (dual-gate) FET can therefore be calculated if the static and small-signal behavior of the single-gate FET is known. A carrier drift velocity v varying with the electric field *E* is assumed together with the gradual-channel approximation.

$$v = \frac{\mu E}{1 + \frac{\mu E}{v_{sat}}} \tag{18}$$

Here, μ is the low-field mobility and v_{sat} is the saturation velocity. This model provides all the important small-signal parameters of the FET as well as the *I-V* characteristics. Since, under normal operating conditions, the gate currents are negligible, the drain current of FET 1 must be equal to that of FET 2.

$$I_{D1} = I_{D2} \tag{19}$$

If the effect of series resistances is ignored, the drain currents are given by

$$I_{Di} = I_{pi} \frac{3\left(u_i^2 - t_i^2\right) - 2(u_i^3 - t_t^3)}{1 + z_i(u_i^2 - t_i^2)} \qquad (i = 1,2) \tag{20}$$

Where u_i^2 and t_i^2 are the drain and gate biases of FET i normalized by the pinch-off voltage. The factor z_i is a measure of the effect of the drift-velocity saturation, and is defined by

$$z_i = \frac{\mu_i V_{pi}}{v_{sat} L_{Gi}} \tag{21}$$

where L_{Gi} is the gate length.

The normalized biases u_i^2 and t_i^2 in explicit forms are given by [10].

$$u_i^2 = \frac{V_{Di} + V_{si} - V_{Gi} - V_{BIi}}{V_{pi}} \tag{22a}$$

$$t_i^2 = \frac{V_{si} - V_{Gi} - V_{BIi}}{V_{pi}} \tag{22b}$$

where V_{Di}, V_{Gi} and V_{si} are drain, gate and source potentials, V_{BIi} is the built-in voltages and V_{pi} is the pinch-off voltage.

For a given set of externally applied voltages, i.e., V_D, $V_{G1}$and V_{G2}, (18) and (22) are solved simultaneously to yield the drain current $I_D = I_{D1} = I_{D2}$, together with the drain voltages of the individual FET's, V_{D1} and $V_{D2} = V_D - V_{D1}$. It should be noted that the second gate is biased lower than the externally applied (plus built-in) voltage $V_{G2} + V_{BI2}$by the self-bias $V_{D1} = V_{s2}$ due to FET1.

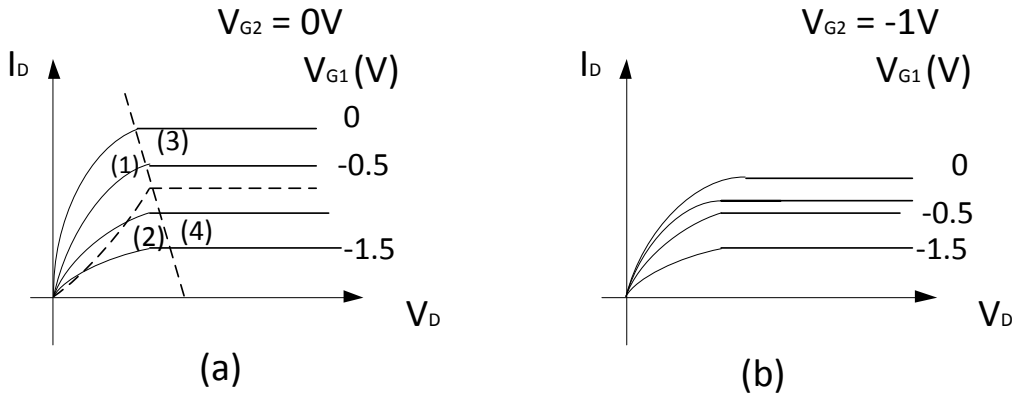


Figure 12: (a) I-V characteristics of a Cascode device when V_{G2} = 0 V.
(b) I-V characteristics of a Cascode device when V_{G2} = -1 V.

The following four different regions arise depending on the bias.

1) Both FET's 1 and 2 are unsaturated.
2) FET 1 is saturated while FET 2 is unsaturated.
3) FET 1 is unsaturated while FET 2 is saturated.
4) Both FET's 1 and 2 are saturated.

In Fig.12, the static I-V characteristics of a Cascode FET are shown for two different second-gate biases. As seen in Fig. 12 (b) and compared with (a), a deeper second-gate bias suppresses the I-V curves. The four regions are shown in Fig. 12 (a), The boundaries between

these regions are marked with broken lines and labeled. As can be seen, only gate 1 (or 2) effectively modulated the drain current in region 2 (or 3). The dual-gate FET is most active in region 4, since both FET's 1 and 2 are working with saturated current. The versatile functions of the dual-gate FET are attributable to this variety in modes of operation which are determined by the biasing conditions.

3.3.4.2 Equivalent network and small signal characteristics

An equivalent circuit of a Cascode FET is constructed on the basis of the model described in the preceding section. The most commonly employed configuration is schematically depicted in Fig. 11. G_1 is the signal input and *D* is the output. In this case, a Cascode FET is regarded as a cascaded amplifier composed of a common source FET (FET 1) and a common-gate FET (FET 2). A more complete equivalent network is seen in Fig. 13, with parasitic resistances and bond wire inductances L_{g1}, L_{g2}, L_d and L_s taken into account. The capacitances C_{pg1}, C_{pg2} and C_{pd} simulate the package parasitics [5].

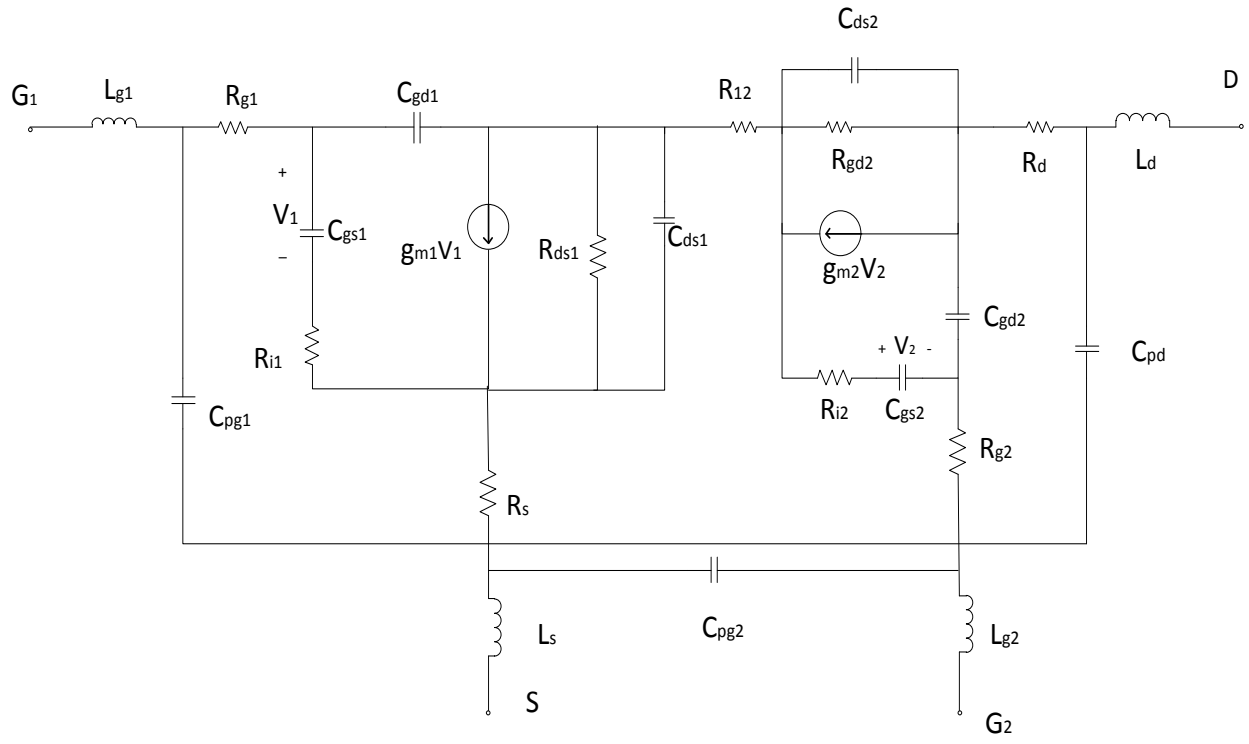


Figure 13: Complete small signal model of a Cascode LNA.

The proposed model consists of two nonlinear, intrinsic MESEET-models embedded in a network of passive components that models bondwires, bondpads and parasitic coupling. The parasitic, bias-independent components are:

L_{g1}, L_{g2}, L_d and L_s (bond wire inductances).

C_{pg1}, C_{pg2} and C_{pd} (bonding pads and interconnect metal to the FET fingers).

R_{g1}, R_{g2}, R_d and R_s (resistivity and contact resistances between the active area and the ports of the FET).

R_{12} (bulk resistance between the two FETs).

The small signal parameters can be computed under given bias conditions. The transconductance g_m is defined by

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D} \tag{23}$$

The gate input capacitance C_{gs} is calculated as

$$C_{gs} = \left.\frac{\partial Q}{\partial V_G}\right|_{V_D} \tag{24}$$

where Q is the depletion layer charge. The gate drain feedback capacitance $C_{gd}$is given by

$$C_{gd} = \left.\frac{\partial Q}{\partial V_D}\right|_{V_G} + \varepsilon W \tag{25}$$

where the last term approximates the fringing capacitance at the drain end of the gate.

Parasitic source and drain series resistances R_s and R_d are determined by the inter electrode separations and the contact resistance. The contact resistance is limited by the current-crowding effect. Gate series resistances R_{g1} and R_{g2} are essentially distributed elements and are determined by the sheet resistance of the gate metal.

3.3 Measurement of FET Parameters

Because the GaAs MESFET has gained such prominence in RF circuits, it is important to look at its parameter extraction. The fundamental equation for the drain current in the linear region is

$$I_D = \beta(V_{GS} - V_{T0})V_{DS} \tag{26}$$

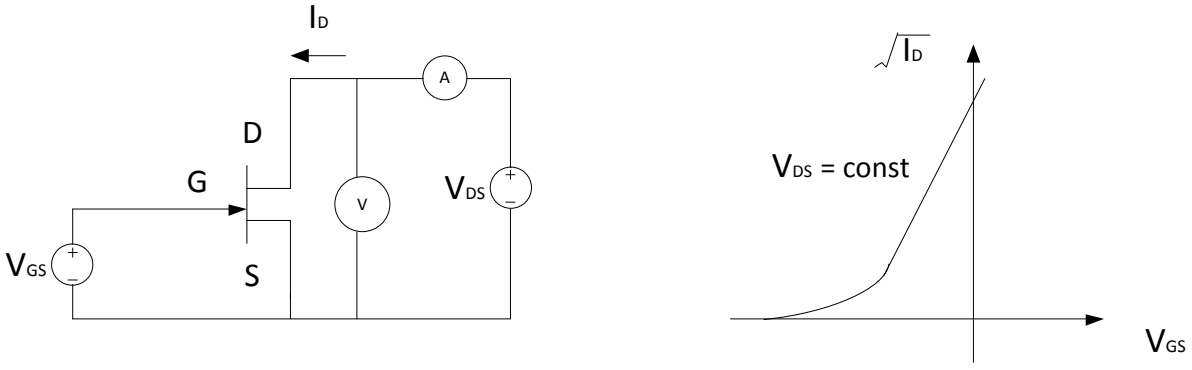
The only difference between MESFET and HEMT lies in the definition of the threshold voltage V_{T0}. Specifically, with the Schottky barrier voltage V_d , and pinch-off voltage V_p, we obtain the following expression:

$$V_{T0} = V_d - V_p \tag{27}$$

In the saturation region, when $V_{ds} \geq V_{GS} - V_{T0}$, the drain current becomes

$$I_D = I_{Dsat} = \beta(V_{GS} - V_{T0})^2 \tag{28}$$

We can extract values for the conduction parameter β and the threshold voltage V_{T0} by plotting the square root of the drain current versus the gate source voltage V_{GS} [9]. A measurement arrangement of a MESFET for obtaining V_{T0} and β is shown in Fig. 14.



(a) Measurement arrangement (b) I_D versus V_{GS} transfer characteristic

Figure 14: Generic measurement arrangement and transfer characteristics in saturation region.

The threshold voltage is determined by setting two different gate-source voltages V_{GS1} and V_{GS2}, where maintaining a constant drain-source V_{DS} = const ≥ $V_{GS} - V_{T0}$, such that the transistor is operated in the saturation region. Using eq.(28), we can get

$$\sqrt{I_{D1}} = \sqrt{\beta}(V_{GS1} - V_{T0}) \tag{29}$$

$$\sqrt{I_{D2}} = \sqrt{\beta}(V_{GS2} - V_{T0}) \tag{30}$$

Here, we assume the channel length modulation effect is negligible. Therefore, the measured current is close to the saturation drain current. Taking the ratio of (29) and (30) and solving for V_{T0}, we obtain

$$V_{T0} = \frac{V_{GS1} - (\sqrt{I_{D1}}/\sqrt{I_{D2}})V_{GS2}}{1 - \sqrt{I_{D1}}/\sqrt{I_{D2}}} \tag{31}$$

We can then substitute (31) into (30) and solve for β.

4. Multiport Networks Analysis

4.1 Impedance and Admittance Matrices

The Cascode low noise amplifier is usually a three-port network, thus a multiport network analysis becomes necessary. Figure 15 shows the basic current and voltage definitions for a multiport network.

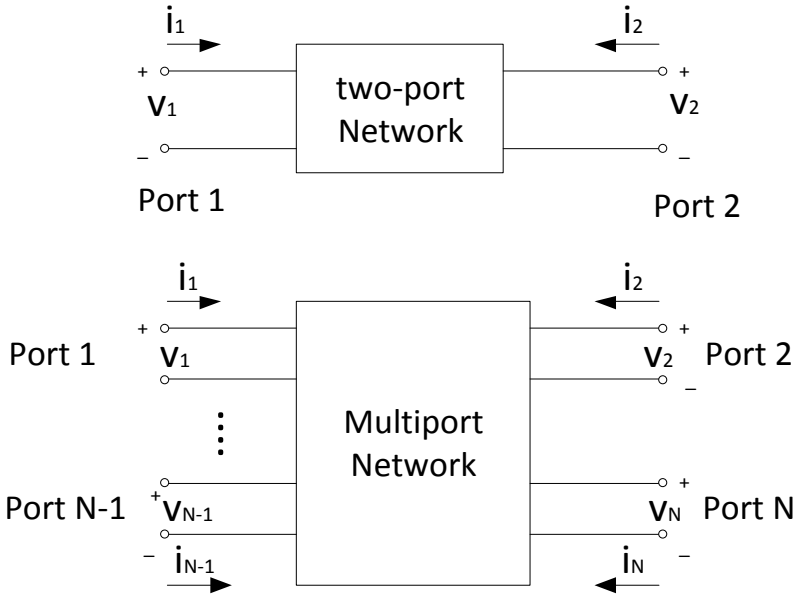


Figure 15: Basic voltage and current definitions for multiport network.

In establishing the various parameter conventions, we begin with the voltage-current relations through double-indexed impedance coefficients Z_{nm}, where indices n and m range between 1 and N. The voltage at each port is given by

$$v_1 = Z_{11}i_1 + Z_{12}i_2 + \cdots + Z_{1N}i_N \quad (32a)$$

$$v_2 = Z_{21}i_1 + Z_{22}i_2 + \cdots + Z_{2N}i_N \quad (32b)$$

$$v_N = Z_{N1}i_1 + Z_{N2}i_2 + \cdots + Z_{NN}i_N \quad (32c)$$

In a more concise notation, (32) can be converted into an impedance or Z-matrix form:

$$\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1N} \\ Z_{21} & Z_{22} & \cdots & Z_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{N1} & Z_{N2} & \cdots & Z_{NN} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix} \tag{33}$$

Each impedance element in (33) can be determined via the following protocol

$$Z_{nm} = \left. \frac{v_n}{i_m} \right|_{i_k=0 \text{ (for k}\neq\text{m)}} \tag{34}$$

This means that the voltage v_n is recorded at port n, while port m is driven by current i_m and the rest of the ports are maintained under open circuit conditions.

Instead of using voltages as the dependent variable, the admittance or Y-matrix can be defined such that

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & \cdots & Y_{1N} \\ Y_{21} & Y_{22} & \cdots & Y_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{N1} & Y_{N2} & \cdots & Y_{NN} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} \tag{35}$$

Here we define the individual element of the Y-matrix as

$$Y_{nm} = \left. \frac{i_n}{v_m} \right|_{v_k=0 \text{ (for k}\neq\text{m)}} \tag{36}$$

It is apparent that impedance and admittance matrices are inverses of each other:

$$[Z] = [Y]^{-1} \tag{37}$$

4.2 Scattering Parameters

When building the small signal model for a Cascode LNA, the scattering or S-parameter representation plays a key role. The importance is derived from the fact that practical system characterization can no longer be accomplished through simple open- or short-circuit measurements, as is customarily done in low frequency applications. For example, the open circuit leads to capacitive loading at the terminal. Consequently, open/short-circuit conditions needed to determine Z-, Y-, h-, and ABCD-parameters can no longer be guaranteed. Moreover, when dealing with wave propagation phenomena, it is not desirable to introduce a reflection coefficient whose magnitude approaches unity. With S-parameters, engineers can characterize the two-port network description of practically all RF devices without requiring unachievable terminal conditions. The S-parameters denote the fraction of incident power reflected at a port and transmitted to other ports. Like the impedance or admittance matrix for an N-port network, the scattering matrix provides a complete linear description of the network as seen at its N ports. While the impedance and admittance matrices relate the total voltages and currents at the ports, the scattering matrix relates the voltage wave incident on the ports to those reflected from the ports. For some components and circuits, the S-parameters can be calculated using network analysis techniques. Once the S-parameters of the network are known, conversion to other matrix parameters can be performed.

S-parameters are power wave descriptors that permit us to define the input-output relations of a network in terms of incident and reflected power waves. In Fig.16, a_n represents an incident normalized power wave and b_n is a reflected normalized power wave at port n. Written in terms of total voltage and current representation of port n, we get [11]

$$a_n = \frac{1}{2\sqrt{Z_0}}(V_n + Z_0 I_n) \tag{38a}$$

$$b_n = \frac{1}{2\sqrt{Z_0}}(V_n - Z_0 I_n) \tag{38b}$$

where the index n refers to either port 1 or 2. The impedance Z_0 is the characteristic impedance of the connecting lines on the input and output side of the network. However, the characteristic line impedance on the output side can differ from the line impedance on the input side.

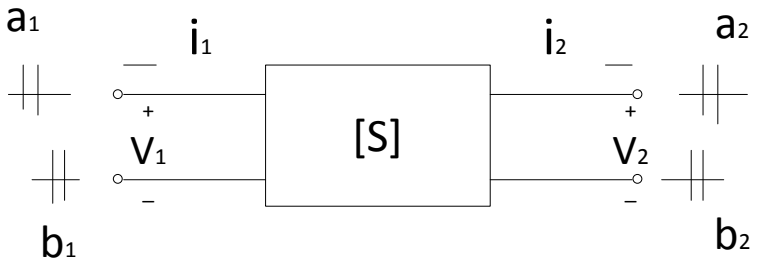


Figure 16: S-parameters for a two port network.

Inserting (38) results in the voltage and current expressions:

$$V_n = \sqrt{Z_0}(a_n + b_n) \tag{39a}$$

$$I_n = \frac{1}{\sqrt{Z_0}}(a_n - b_n) \tag{39b}$$

The power equation for the network is

$$P_n = \frac{1}{2} Re\{V_n {I_n}^*\} = \frac{1}{2}(|a_n|^2 - |b_n|^2) \tag{40}$$

Isolating forward and backward traveling wave components, we see

$$a_n = \frac{V_n^+}{\sqrt{Z_0}} = \sqrt{Z_0} I_n^+ \tag{41a}$$

$$b_n = \frac{V_n^-}{\sqrt{Z_0}} = -\sqrt{Z_0} I_n^- \tag{41b}$$

Based on the directional convention shown in Fig.16, we can define the S-parameters:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{42}$$

Here the terms are

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \equiv \frac{\text{reflected power wave at port 1}}{\text{incident power wave at port 1}} \tag{43a}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \equiv \frac{\text{transmitted power wave at port 1}}{\text{incident power wave at port 2}} \tag{43b}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \equiv \frac{\text{transmitted power wave at port 2}}{\text{incident power wave at port 1}} \tag{43c}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} = \frac{\text{reflected power wave at port 2}}{\text{incident power wave at port 2}} \tag{43d}$$

The reflection coefficient at the input side is expressed in terms of S_{11} under matched output.

$$\Gamma_{in} = \frac{V_1^-}{V_1^+} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = S_{11} \tag{44}$$

The S-parameters can be determined under conditions of perfect matching on the input or output side. In order to record S_{11} and S_{22} , we have to ensure that on the output side that the line impedance Z_0 is matched. This allows us to compute S_{11} by finding the input reflection coefficient:

$$S_{11} = \Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{45a}$$

$$S_{21} = \frac{b_2}{a_1}\Big|_{a_2=0} = \frac{V_2^-/\sqrt{Z_0}}{(V_1 + Z_0 I_1)/(2\sqrt{Z_0})}\Big|_{I_2^+=0, V_2^+=0} \tag{45b}$$

To compute S_{22} and S_{12}, we need to the output reflection coefficient in a similar way.

$$S_{22} = \Gamma_{out} = \frac{Z_{out} - Z_0}{Z_{out} + Z_0} \tag{45c}$$

$$S_{12} = \frac{b_1}{a_2}\Big|_{a_1=0} = \frac{V_1^-/\sqrt{Z_0}}{(V_2 + Z_0 I_2)/(2\sqrt{Z_0})}\Big|_{I_1^+=0, V_1^+=0} \tag{45d}$$

Consider the N-port network shown in Fig. 4-2, where V_n^+ is the amplitude of the voltage wave incident on port n, and V_n^- is the amplitude of the voltage wave reflected from port n. The scattering matrix is defined in relation to these incident and reflected voltage waves.

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1N} \\ \vdots & \ddots & \vdots \\ S_{N1} & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{bmatrix} \tag{46}$$

An element of the $[S]$ matrix can be determined by

$$S_{ij} = \frac{V_i^-}{V_j^+}\Big|_{V_k^+=0 \text{ for } k\neq j} \tag{47}$$

In words, S_{ij} is found by driving port j with an incident wave of voltage V_j^+, and measuring the reflected wave amplitude V_j^+, coming out of port i . The incident waves on all ports except the jth port are set to zero, which means that all ports should be terminated in matched loads to avoid reflection. Thus, S_{ii} is the reflection coefficient seen looking into port i when all other

ports are terminated in matched loads. And S_{ij} is the transmission coefficient from port j to port i when all other ports are terminated in matched loads.

4.3 Parameters Conversion

When doing calculation for the small signal model, sometimes we need to do the conversion between the S-parameters and Z-parameters. To find the conversion between the Z- and S-parameters, we need to define S-parameter relation in matrix notation.

$$[b] = [S][a] \tag{48}$$

Multiplying by $\sqrt{Z_0}$ gives

$$\sqrt{Z_0}[b] = [V^-] = \sqrt{Z_0}[S][a] = [S][V^+] \tag{49}$$

Adding $[V^+] = \sqrt{Z_0}[a]$ to both sides results in

$$[V] = [S][V^+] + [V^+] = ([S] + [E])[V^+] \tag{50}$$

where $[E]$ is the identity matrix. To compute this form with the impedance expression $[V] = [Z][I]$, we have to express $[V^+]$ in terms of $[I]$. This is accomplished by the following equation:

$$[V^+] - [S][V^+] = \sqrt{Z_0}([a] - [b]) = Z_0[I] \tag{51}$$

By isolating $[V^+]$, it is seen that

$$[V^+] = Z_0([E] - [S])^{-1}[I] \tag{52}$$

Then finally we get the desired result

$$[Z] = Z_0([S] + [E])([E] - [S])^{-1} \tag{53}$$

4.4 Network Interconnection

4.4.1. Series connection of networks

A series connection consisting of two two-port networks is shown in Fig. 17.

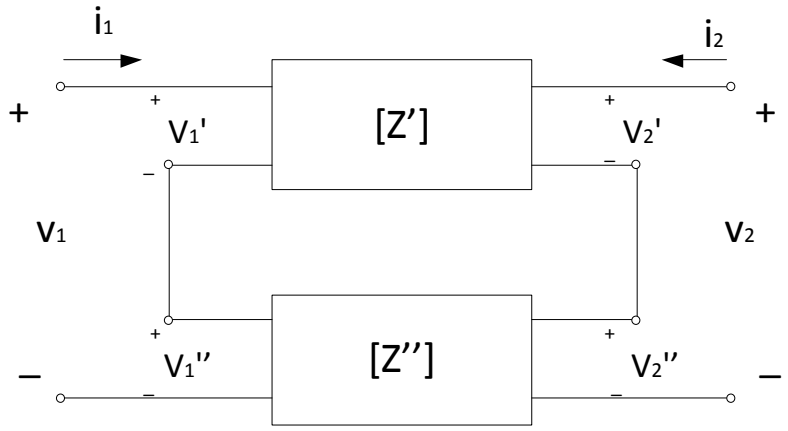


Figure 17: Series connection of two two-port networks.

In this case, the individual voltages are additive while the currents remain the same. This results in

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} V_1' + V_1'' \\ V_2' + V_2'' \end{bmatrix} = [Z] \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{54}$$

where the new composite network $[Z]$ takes the form

$$[Z] = [Z'] + [Z''] = \begin{bmatrix} Z_{11}' + Z_{11}'' & Z_{12}' + Z_{12}'' \\ Z_{21}' + Z_{21}'' & Z_{22}' + Z_{22}'' \end{bmatrix} \tag{55}$$

4.4.2. Parallel Connection of Networks

A parallel connection of two dual-port networks is shown in Fig. 18.

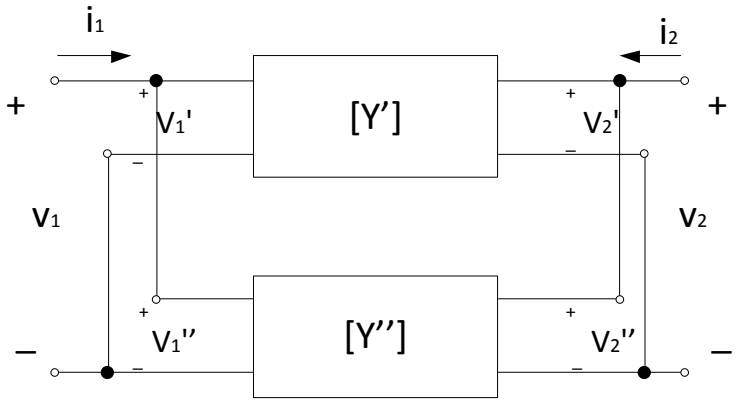


Figure 18: Parallel connection of two-port networks.

The new admittance matrix is defined as the sum of the individual admittances.

$$[Y] = [Y'] + [Y''] = \begin{bmatrix} Y'_{11} + Y''_{11} & Y'_{12} + Y''_{12} \\ Y'_{21} + Y''_{21} & Y'_{22} + Y''_{22} \end{bmatrix} \tag{56}$$

4.4.3. Cascaded Connection of Networks

If FET1 and FET2 are represented by their two-port Z-parameters $[Z^I]$ and $[Z^{II}]$ respectively, the Cascode MESFETs may be represented as a cascaded connection of two two-port networks as shown in Fig. 19.

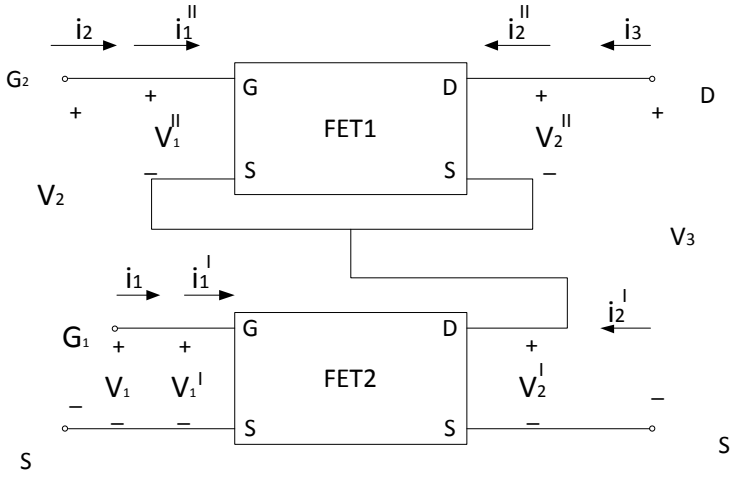


Figure 19: Cascode connection of two dual-port networks.

Taking port 1 as being between gate 1 and the source, port 2 as being between gate 2 and the source, and port 3 as being between the drain and the source, the Cascode connection forces the following relationship:

$$V_1 = V_1^I \tag{57a}$$

$$V_2 = V_2^I + V_1^{II} \tag{57b}$$

$$V_3 = V_2^I + V_2^{II} \tag{57c}$$

$$i_1 = i_1^I \tag{57d}$$

$$i_2 = i_1^{II} \tag{57e}$$

$$i_3 = i_2^{II} \tag{57f}$$

Using (57), the following simple relationships may be found between the three-port Z-parameters of the Cascode MESFETs and the individual dual-port Z-parameters of the two single-gate FET, which is shown in Appendix A:

$$\begin{aligned} Z_{11} &= Z_{11}^I & Z_{12} &= Z_{12}^I & Z_{13} &= Z_{12}^I \\ Z_{21} &= Z_{21}^I & Z_{22} &= (Z_{22}^I + Z_{11}^{II}) & Z_{23} &= (Z_{22}^I + Z_{12}^{II}) \\ Z_{31} &= Z_{21}^I & Z_{32} &= (Z_{22}^I + Z_{21}^{II}) & Z_{33} &= (Z_{22}^I + Z_{22}^{II}) \end{aligned} \tag{58}$$

5. Modeling Approach

5.1 General idea for modeling

The Cascode LNA is a three-port circuit, which is comprised of two FETs: one in common source and the other in common gate. When building a Cascode LNA model, a direct optimization by means of a computer makes no sense, since the number of elements is of the order of 25 or more and the error function can have several local minima with physically nonacceptable values of the elements. Thus precise starting values for the optimization must be found.

For Cascode LNAs, an equivalent circuit is composed of two single gate FET. Here we assume the two single gate FET parts to be equal. The proposed method consists of characterizing each FET part separately in its actual bias conditions. Consequently, we need to reduce the three-port circuit to two dual-port circuits, which is shown in Figure 20.

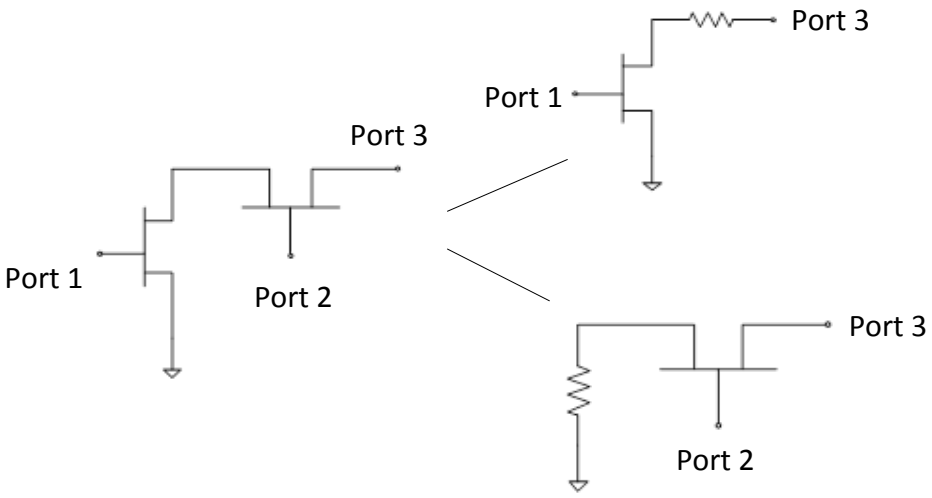


Figure 20: The three-port circuit reduces to two dual-port circuits.

Then we can build a small signal equivalent circuit for each dual-port circuit, and the intrinsic elements of the two-port circuit can be estimated. After the elements of the intrinsic device are estimated, external parasitic components can be determined.

5.2 DC analysis for Cascode LNA

This thesis proposed a modeling environment in the Advanced Design System (ADS) simulator. An N-channel FET device is picked up from ADS, which is based on the Advanced Curtice 2 model. The Advanced Curtice 2 model has 56 elements, which is shown in Fig. 21. The parameters of the Agilent ATF551M4 MESFET were entered into this model, which is designed for LNA applications in the 450MHz-10GHz range..

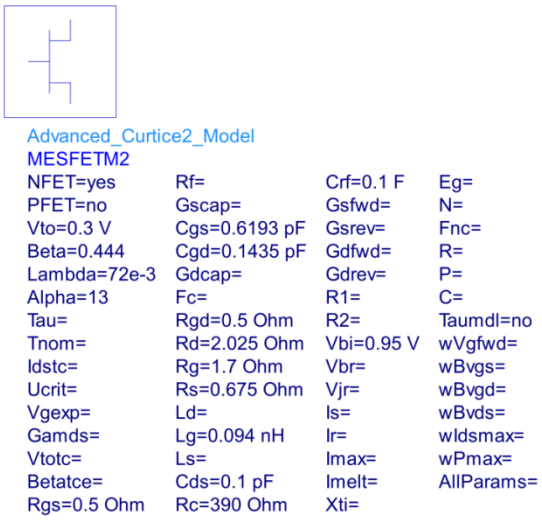


Figure 21: Advanced Curtice 2 model for ATF551M4 MESFET.

The circuit schematic for Advanced Curtice 2 model is shown in Fig. 22.

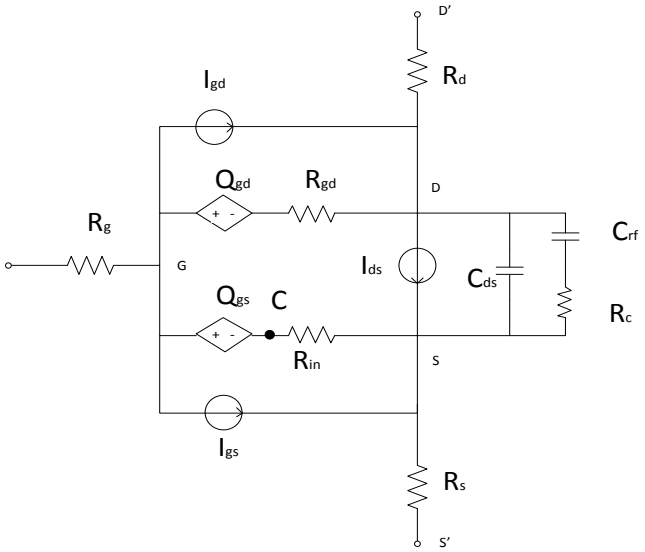


Figure 22: Circuit schematic for Advanced Curtice 2 model.

In Fig.22, Q_{gd} is the gate-drain junction charge, and Q_{gs} is the gate-source junction charge.

$$Q_{gs} = 2V_{bi}C_{gs}\left[1 - \sqrt{1 - \frac{V_{gc}}{V_{bi}}}\right] \tag{59a}$$

$$C_{gs} = \frac{\partial Q_{gs}}{\partial V_{gc}} = \frac{C'_{gs}}{\sqrt{1 - \frac{V_{gc}}{V_{bi}}}} \tag{59b}$$

where C'_{gs} is the zero bias gate-source junction capacitance, and V_{bi} is the built-in gate potential.

$$Q_{gd} = 2V_{bi}C_{gd}\left[1 - \sqrt{1 - \frac{V_{gd}}{V_{bi}}}\right] \tag{60a}$$

$$C_{gd} = \frac{\partial Q_{gd}}{\partial V_{gd}} = \frac{C'_{gd}}{\sqrt{1 - \frac{V_{gd}}{V_{bi}}}} \tag{60b}$$

Where C'_{gd} is the zero bias gate-drain junction capacitance.

The Drain current in the Advanced Curtice quadratic model is based on the modification of the drain current equation in the Curtice quadratic model. The quadratic dependence of the drain current with respect to the gate voltage is calculated with the following expression in the region V_{ds} ≥ 0.0V.

$$I_{ds} = \beta\left(V_{gs} - V_{t0}\right)^2(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \tag{61}$$

Assuming symmetry, in the reverse region, the drain and source swap roles and the expression becomes:

$$I_{ds} = \beta\left(V_{gd} - V_{t0}\right)^2(1 - \lambda V_{ds})\tanh(\alpha V_{ds}) \tag{62}$$

The drain current is set to zero in either case if the junction voltage drops below the threshold voltage V_{t0}.

Since the Cascode LNA has two single-gate FETs, its bidirectional DC transfer characteristics $I_D(V_{G1S}, V_{G2S})|_{V_{DS}}$ can be derived using

$$V_{DS} = V_{D1S} + V_{DD1} \tag{63}$$

$$V_{G2D1} = V_{G2S} - V_{D1S} \tag{64}$$

Two MESFETs are cascaded together to form the Cascode low noise amplifier, which is shown in Fig. 23. To obtain the DC transfer characteristics, we apply V_{dc}= 10 V to the drain of the LNA, then use the parameter sweep option in ADS to sweep V_{g1} and $V_{g2}$from 0 to 1.5 V. The results of DC transfer characteristics of the Cascode LNA is shown in Fig. 24.

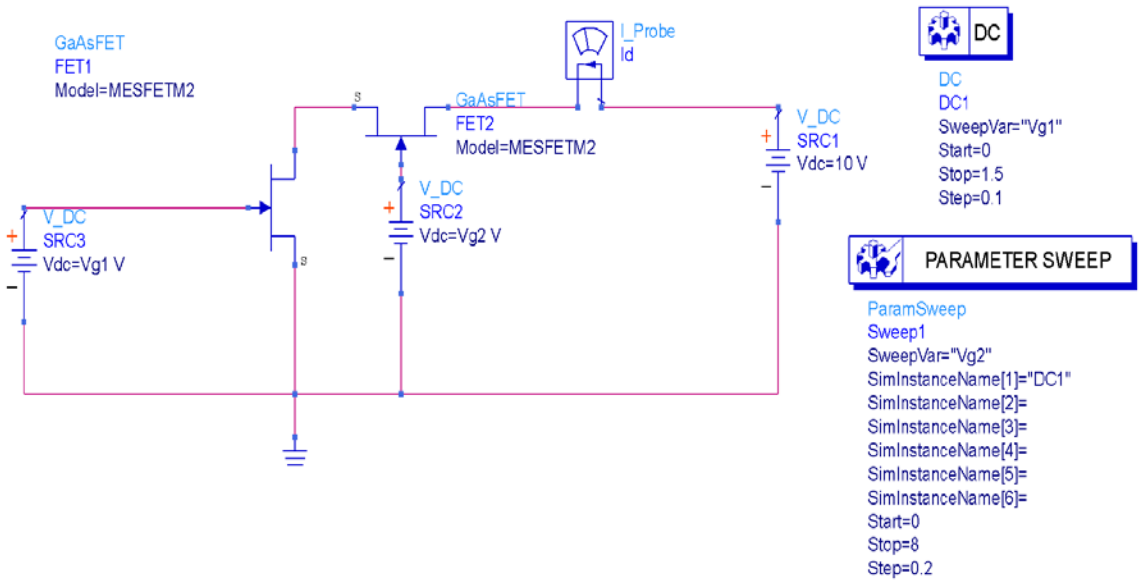


Figure 23: DC simulation for the Cascode LNA in ADS.

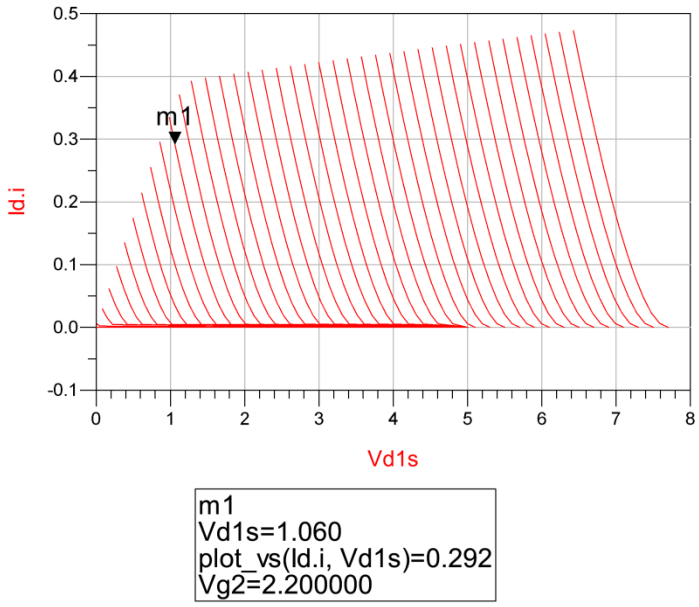


Figure 24: I_d versus V_{d1s} with different V_{g2} values.

After carrying out the DC analysis for the Cascode LNA, we needed to know each FET's DC characteristics. Thus V_{ds} is swept from 0 to 10 V and V_{gs} from -1 to 1.5 V. The DC simulation for one FET is shown in Fig. 25.

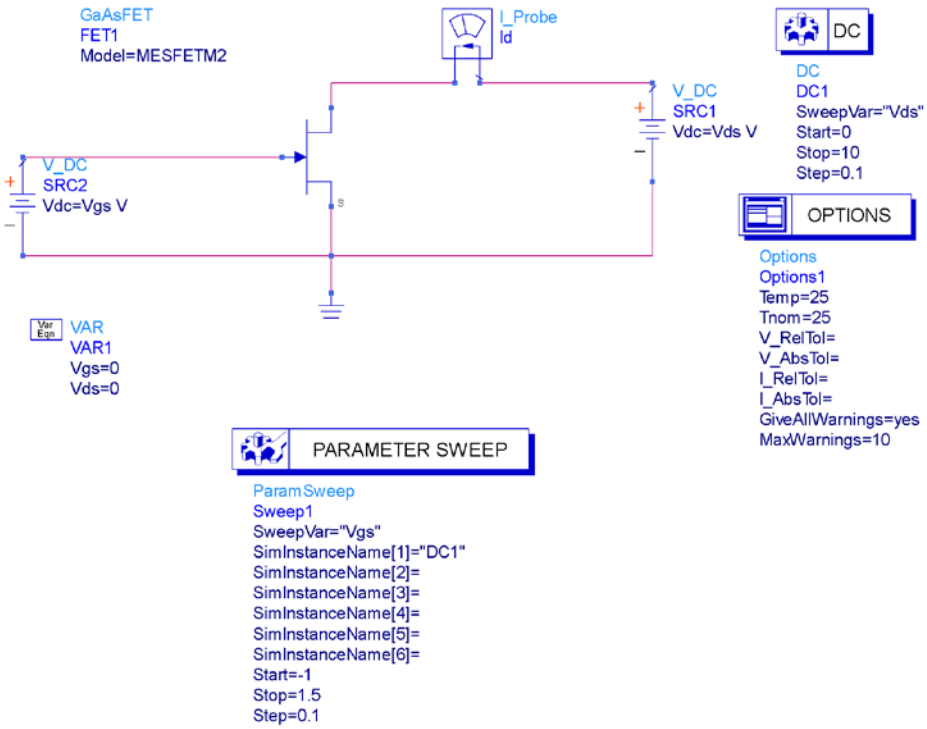


Figure 25: DC simulation for the single-gate FET.

Figure 24 and 26 can be combined together to decide DC bias conditions for the Cascode LNA. In Fig. 5-5, as m_1 is the bias point of the Cascode LNA with V_{ds} = 10 V, V_{G2S} = 2.2 V and I_d = 292 mA, it corresponds to V_{G1S} = 1.3 V, V_{D1S} = 1.06 V, V_{G2D1} = 1.14 V and V_{DD1} = 8.94 V. In this case, FET1 works in the linear region, and FET2 works in saturation.

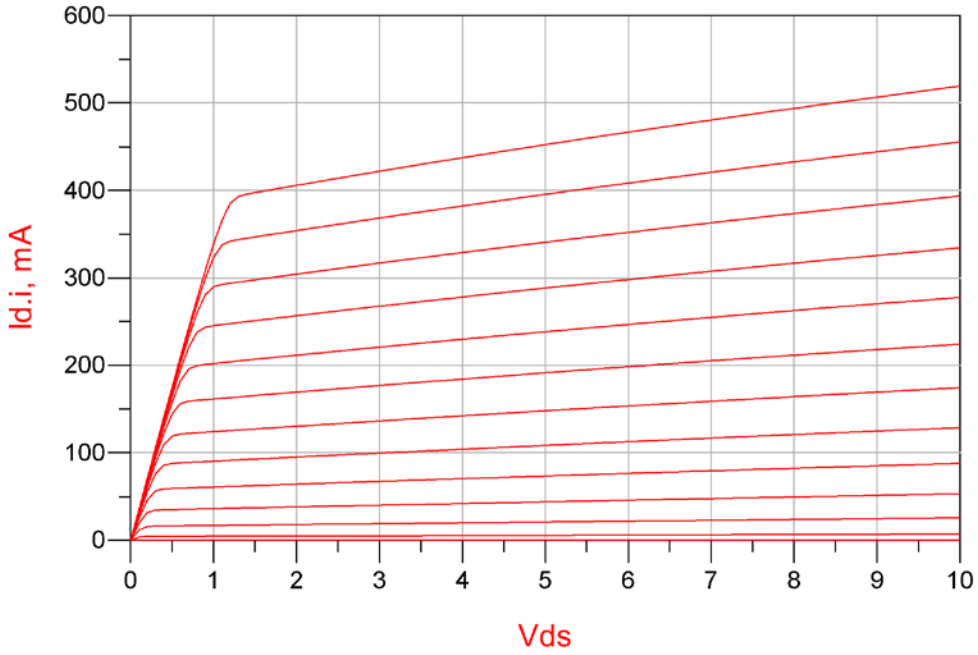


Figure 26: Simulated I-V curve for ATF551M4 MESFET

In the normal operation, the two transistors should both work in the saturation region. The values I chose to make them work in the saturation region are the following: V_{g2} = 5 V, V_{g1} = 1.1V and V_{ds} = 10 V. The following table lists the bias condition for the Cascode transistors.

Table 1: DC bias for both transistors working in saturation

freq	Id.i	Vd1s	Vd2s	Vg1	Vg2	Vg2s2
0.0000 Hz	229.1 mA	3.937 V	6.063	1.100 V	5.000 V	1.063

When adjusting DC bias condition for the Cascode LNA properly, FET1 is operated in the linear region and FET2 is biased in the active region, which is shown in Table 2. This gives the operation of the Cascode LNA to be two decoupled single-gate MESFET with FET2 bias condition unchanged and FET1 as a series resistor. Moreover, one can adjust the DC bias condition to make FET2 operated in the linear region and FET1 biased in the active region.

Table 2: DC bias for FET1 working in linear region and FET2 in saturation

freq	Id.i	Vd1s	Vd2s	Vg1	Vg2s2	Vg2
0.0000 Hz	219.8 mA	657.0 mV	6.143	1.300 V	1.043	1.700 V

5.3 Small Signal Analysis for Cascode LNAs

The small signal equivalent circuit for the Cascode LNA is shown in Fig.13. It is comprised of two intrinsic devices cascaded together with external parasitic components. If we first ignore the parasitic components, the equivalent circuit is reduced to the following model.

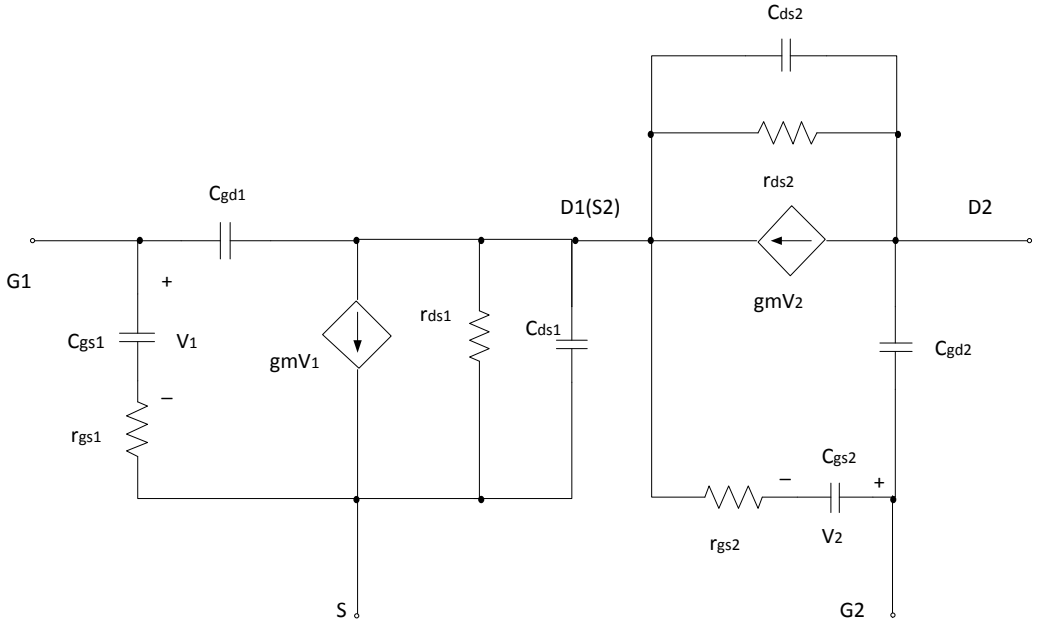


Figure 27: Simplified Cascode LNA model.

The C_{gs} is the gate source junction capacitance, R_{gs} is the gate source resistance, C_{gd} is the gate drain junction capacitance, R_{ds} is the drain source resistance, and C_{ds} is the drain source junction capacitance.

As described above, the DC transfer characteristics of the Cascode LNA can be decomposed into two cases. In each case, there is one FET operating as a resistor and the other FET is operating in saturation. As the bias changes to m_1 , FET1 can be modeled by series resistance $R_s + R_{c1} + R_{12}$. Since the bias of FET2 is unchanged in the same active region as that in the normal operation, the three-port circuit is reduced into a dual-port circuit as shown in Fig. 28.

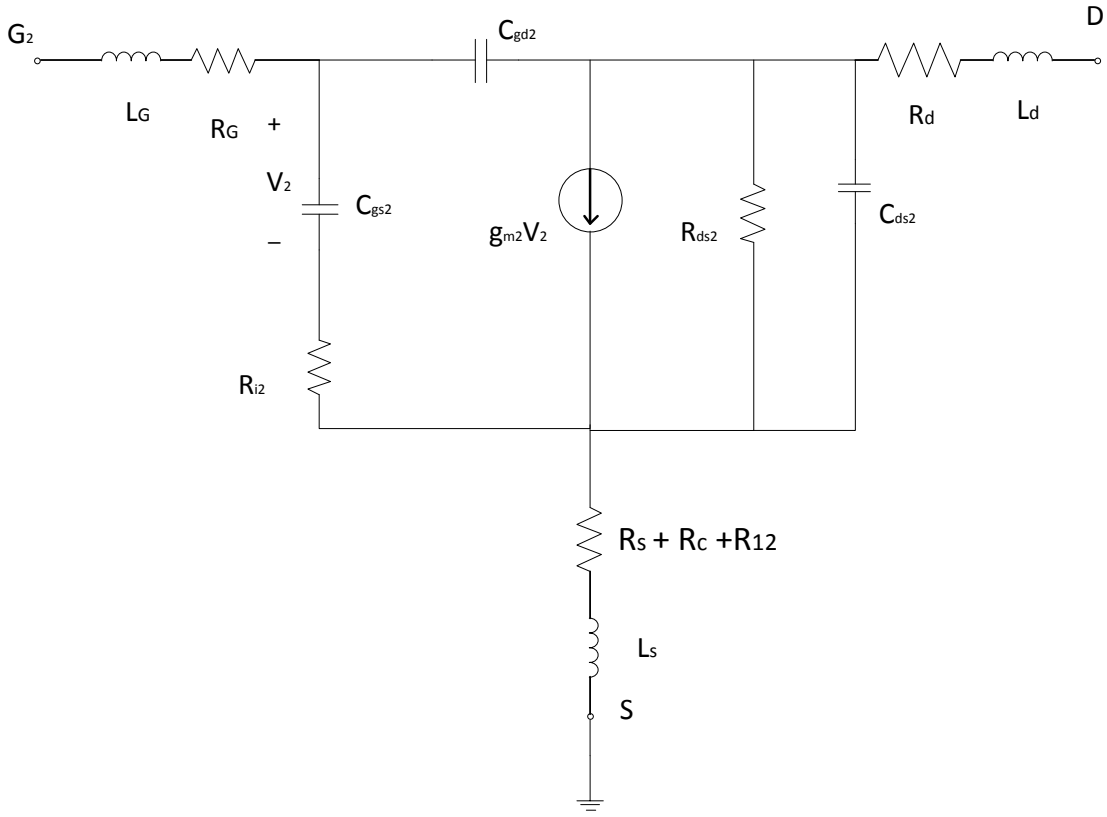


Figure 28: Small signal model of the Cascode LNA when FET1 in linear region and FET2 in saturation.

Similarly, as the bias condition changed to make FET2 work in the linear region, and FET1 in saturation, FET2 is modeled by series resistance $R_d + R_{c2} + R_{12}$, where R_{12} is the inter gate resistance and R_{c2} is the channel resistance for FET2. FET1 is then in the active region with the resulting two-port small signal model as shown in Fig. 29.

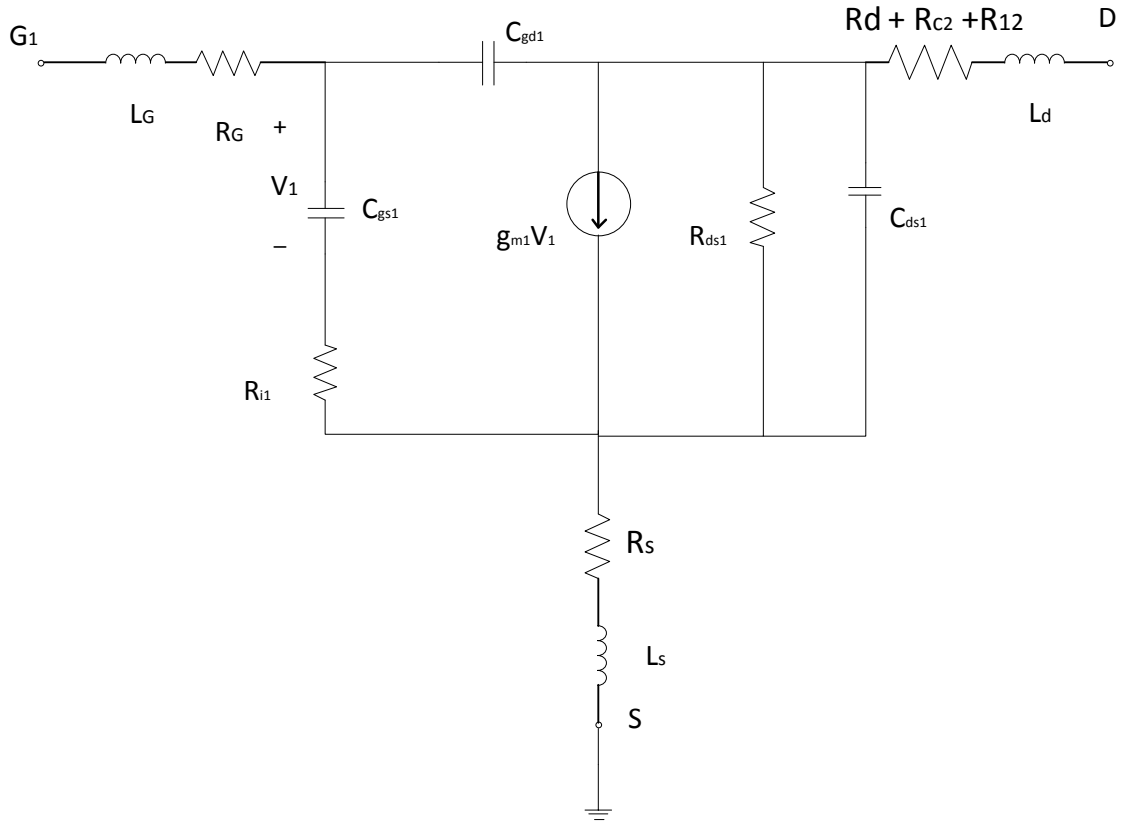


Figure 29: Small signal model of the Cascode LNA when FET2 in linear region and FET1 in saturation

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5.4 Algorithm to estimate model component values

After the three-port LNA circuit is reduced to two dual-port circuits, a two-port network analysis can be applied. To analyze the two-port circuit, a high frequency single-gate MESFET model is needed; it is depicted in Fig. 30.

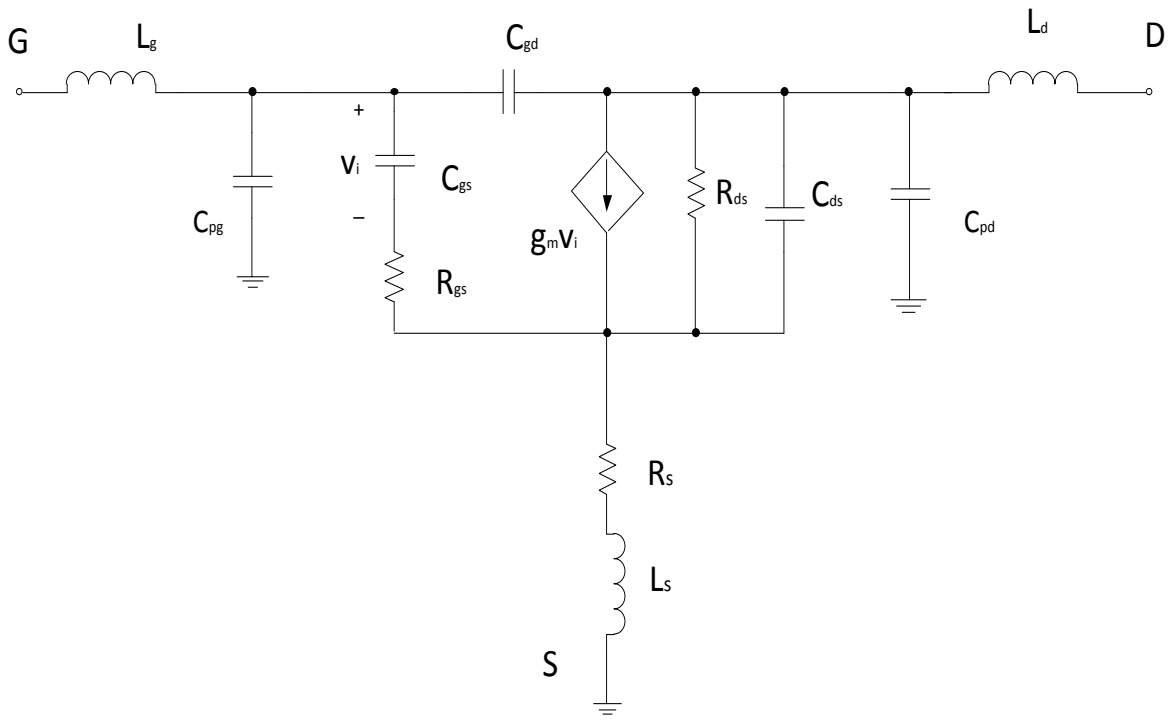


Figure 30: High frequency MESFET model.

This equivalent circuit can be divided into two parts:

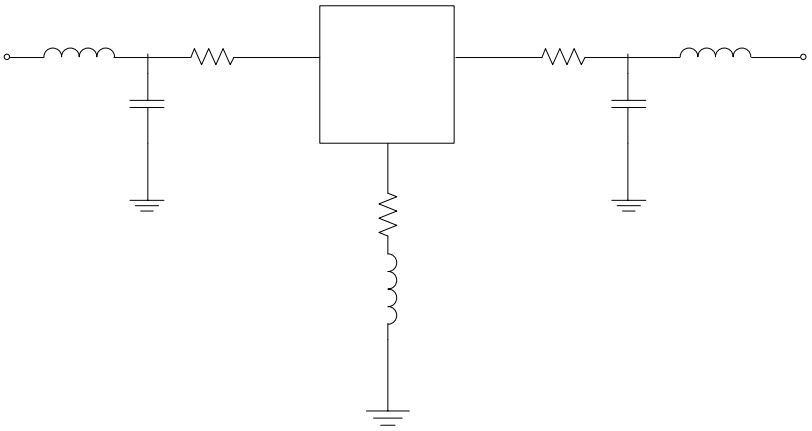
(i) the intrinsic elements g_m , g_d , C_{gs} , C_{gd} (which includes, in fact, the drain-gate parasitic), C_{ds} , R_{gs}, which are functions of the biasing conditions;

(ii) the extrinsic elements L_g, R_g, C_{pg}, L_s, R_s, R_d, C_{pd}, and L_d, which are independent of the biasing conditions.

Since the intrinsic device exhibits a "pi" topology, it is convenient to use the admittance (Y) parameters to characterize its electrical behavior. Assuming that all the extrinsic elements are known, the Y-matrix can be carried out using the following procedure:

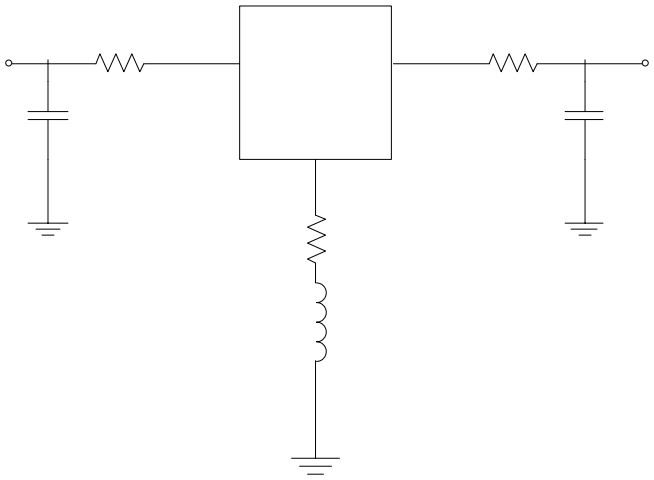
a) measurement of the S-parameters of the extrinsic device;
b) transformation of the S-parameters to impedance Z-parameters and subtraction of L_g and L_d that are series elements;
c) transformation of Z to Y parameters and subtraction of C_{pg} and C_{pd} that are in parallel;
d) transformation of Y to Z parameters and subtraction of R_g, R_s, L_s, R_d that are in series;
e) transformation of Z to Y parameters that correspond to the desired matrix.

The following figure shows the method to extract the intrinsic device elements.



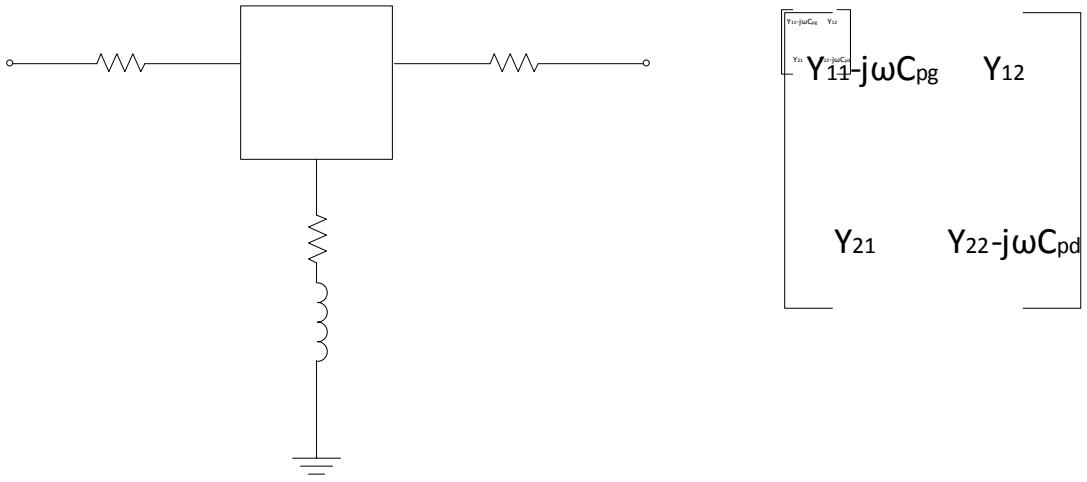
$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

(a)

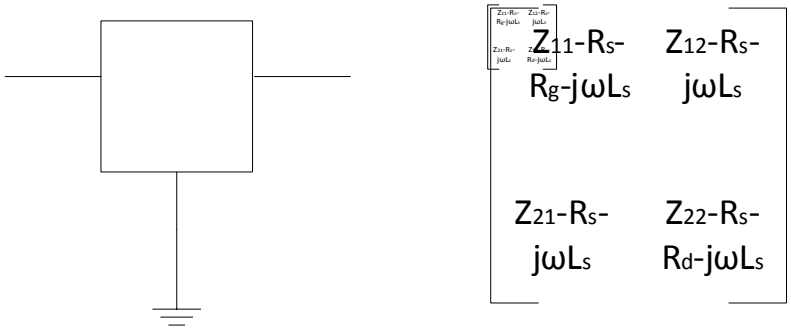


$$\begin{bmatrix} Z_{11}-j\omega L_g & Z_{12} \\ Z_{21} & Z_{22}-j\omega L_d \end{bmatrix}$$

(b)



(c)



(d)

Figure 31: Method for extracting the device intrinsic Y matrix.

After we get the Y matrix for the intrinsic device, the Y parameter description for the small signal MESFET model is the following:

$$Y_{11} = \frac{j\omega C_{gs} + \omega^2 {C_{gs}}^2 R_{gs}}{1 + \omega^2 {C_{gs}}^2 {R_{gs}}^2} + j\omega C_{gd} \tag{65a}$$

$$Y_{12} = -j\omega C_{gd} \tag{65b}$$

$$Y_{21} = \frac{g_m}{1 + j\omega C_{gs} R_{gs}} - j\omega C_{gd} \tag{65c}$$

$$Y_{22} = j\omega\left(C_{gd} + C_{ds}\right) + \frac{1}{R_{ds}} \quad (65d)$$

For a typical low noise device, the term $\omega^2 {C_{gs}}^2 {R_{gs}}^2$ is less than 0.01 at low frequency. Assuming $1 + \omega^2 {C_{gs}}^2 {R_{gs}}^2 \approx 1$, we can obtain simplified equations as shown below.

$$Y_{11} = \omega^2 {C_{gs}}^2 R_{gs} + j\omega(C_{gs} + C_{gd}) \quad (66a)$$

$$Y_{12} = -j\omega C_{gd} \quad (66b)$$

$$Y_{21} = g_m - j\omega(g_m R_{gs} C_{gs} + C_{gd}) \quad (66c)$$

$$Y_{22} = \frac{1}{R_{ds}} + j\omega(C_{gd} + C_{ds}) \quad (66d)$$

Expressions (66a)-(66d) show that the intrinsic small-signal elements can be deduced from the Y-parameters as follows: C_{gd} from Y_{12}, C_{gs} and R_{gs} from Y_{11}, g_m from Y_{21}, and lastly R_{ds} and C_{ds} from Y_{22}.

Therefore, the determination of the intrinsic admittance matrix can be carried out using some simple matrix manipulations if the different extrinsic elements are known.

5.5 Parasitic Components Estimation

The parasitic components need to be known in order to get accurate results. As Diamant and Laviron have suggested, the S-parameter measurements at zero drain bias voltage can be used for the evaluation of device parasitics, because the equivalent circuit is much simpler**.** Curtice and Camisa have used this biasing condition to optimize the device parasitics using the program SUPER-COMPACT. This thesis proposed a measurement method performed at V_{ds} = 0. The parasitic components include lead inductance, lead resistance and the package capacitance, which is shown in Fig. 32.

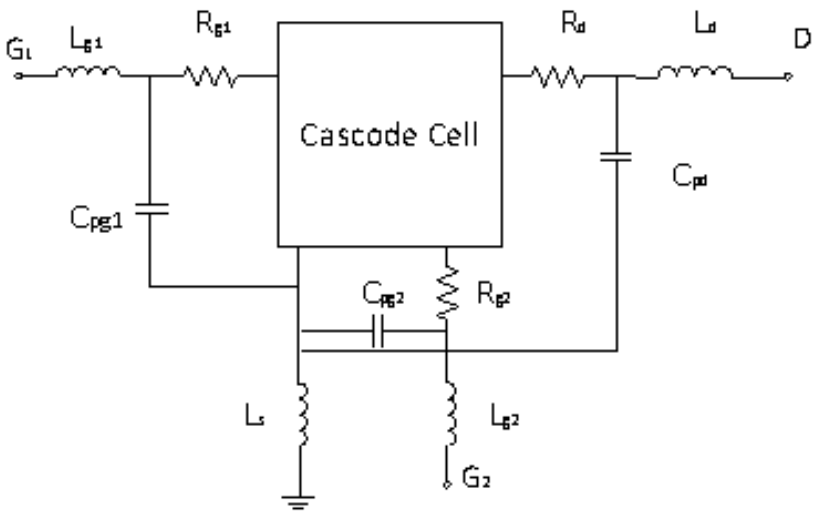


Figure 32: The Cascode cell with parasitic components.

A realistic device is picked from the ADS library, which is shown in Fig. 33. It is an NEC N-channel MESFET (V_{th} = -1.5 V, V_{ds}(typical) = 3 V, I_{dss}= 69.93 mA).

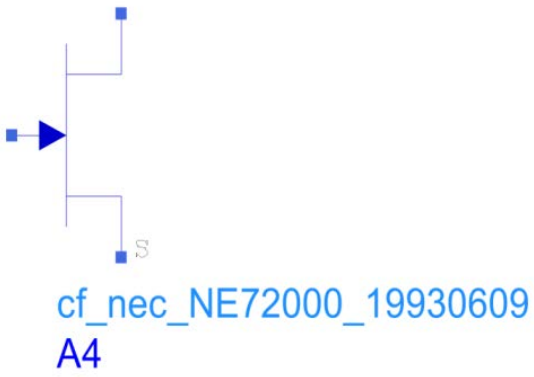


Figure 33: The NEC N-channel realistic library device from ADS.

5.5.1 Parasitic Capacitance Estimation

The equivalent circuit for the Cascode LNA is simplified to the model in Figure 34 when the circuit has the following bias condition: V_{ds} = 0 V, FET1 reverse biased and FET2 forward biased in the linear region.

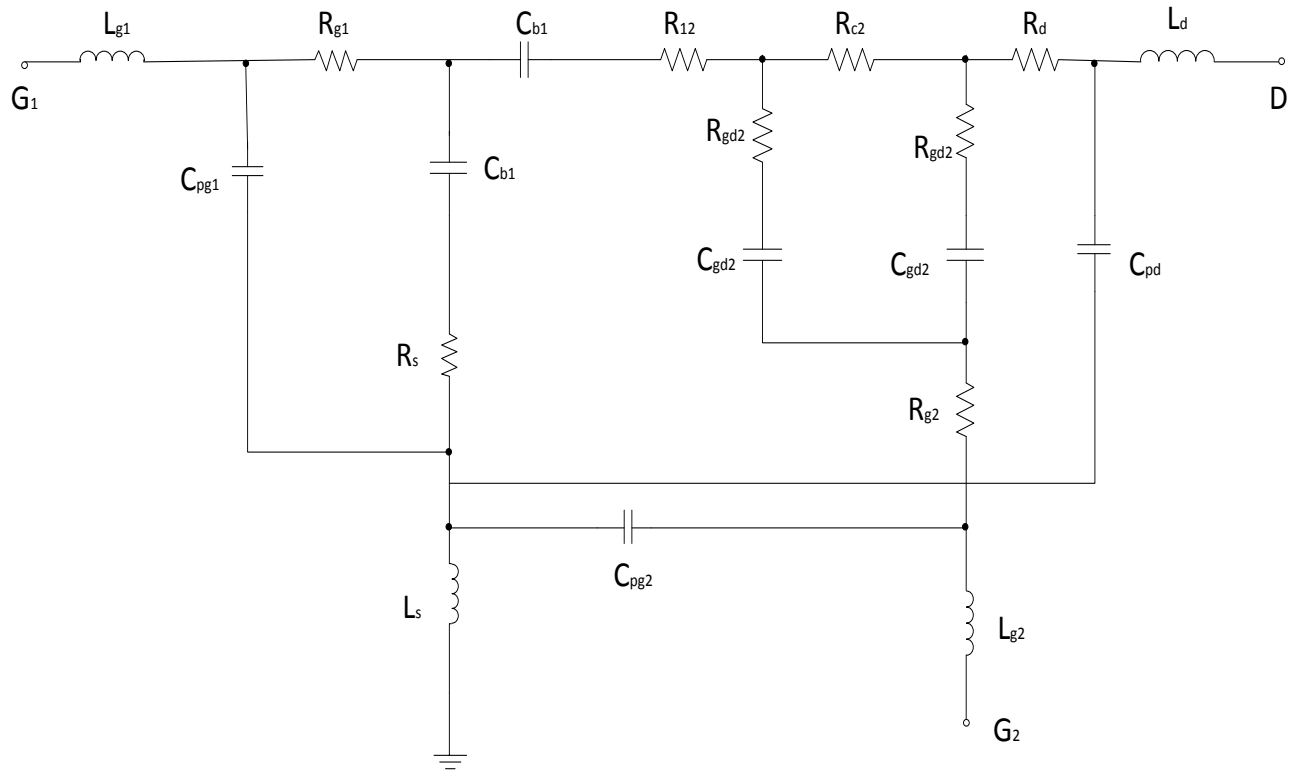


Figure 34: Equivalent circuit of a cold Cascode LNA with FET1 reverse biased and FET2 forward biased.

The Y matrix can be used to describe this small signal model. The imaginary part of its three-port Y-matrix, with frequency below a few gigahertz, can be written as

$$Im(Y_{11}) = \omega(C_{pg1} + 2C_{b1}) \quad (67a)$$

$$Im(Y_{13}) = -\omega C_{b1} \quad (67b)$$

$$Im(Y_{22}) = \omega(2C_{gd2} + 2C_{pg2}) \quad (67c)$$

$$Im(Y_{23}) = -\omega 2C_{gd2} \quad (67d)$$

$$Im(Y_{33}) = \omega(C_{pd} + 2C_{gd2} + C_{b1}) \quad (67e)$$

In Figure 35, the S-parameters are simulated in ADS to estimate the parasitic capacitance. The frequency response of the imaginary part of Y-parameters is almost linear, which is shown in Fig. 36. Based on eq. (67) and Fig.5-17, parasitic capacitance is estimated as follows: C_{pd} = 0.16 pF, C_{pg1} = 0.08 pF, C_{pg2} = 0.04 pF.

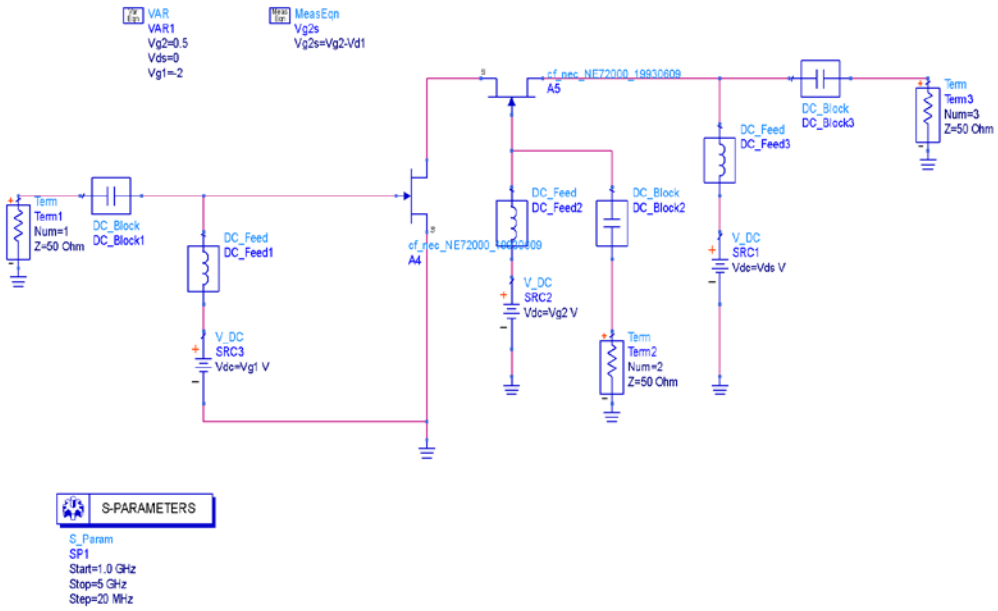


Figure 35: S-parameters simulation with FET1 reverse biased and FET2 forward biased

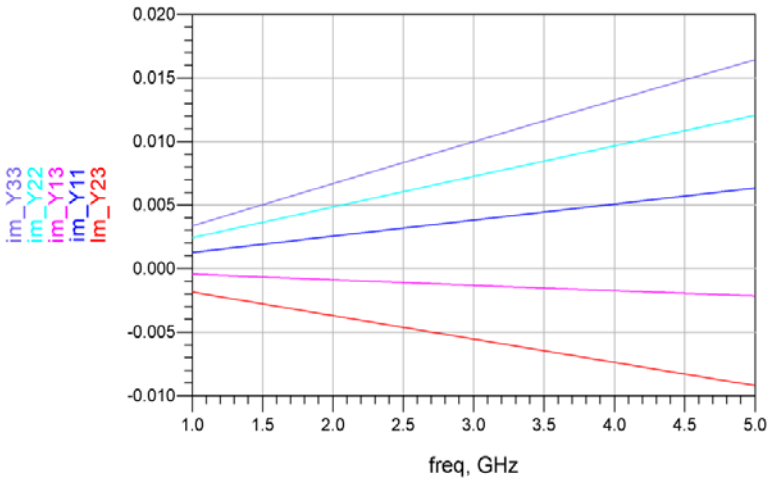


Figure 36: Frequency response of the imaginary part of the three-port Y matrix at V_{ds} = 0V, V_{g1} = -2V and V_{g2} = 0.5V.

5.5.2 Parasitic Resistance Estimation

5.5.2.1 Parasitic source resistance

The parasitic resistances includes the drain resistance R_d, the source resistance R_s, and the inter gate resistance R_{12}. The resistances are due to the contact resistance at the metallization and in part to the bulk resistance of the semiconductor. Figure 37 shows the parasitic resistances.

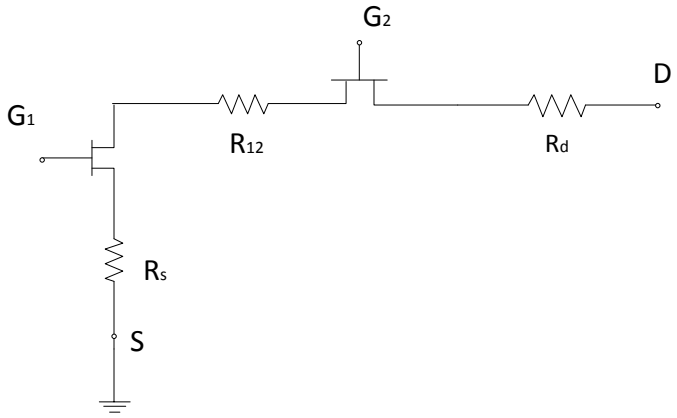


Figure 37: Parasitic resistances for the Cascode LNA.

The "end" resistance measurement technique can be used to measure the parasitic resistances, which is shown in Fig. 38. In this scheme the flowing gate current creates a voltage drop across the series resistance and the drain contact is floating so that the drain section of the device acts as a "probe." Hence, the series source resistance has been estimated as

$$R_s \approx \frac{V_D}{I_g} \tag{68}$$

where V_D is the floating drain potential. The potential V_D however also includes a contribution from the voltage drop across a part of the channel. But I just ignore it here.

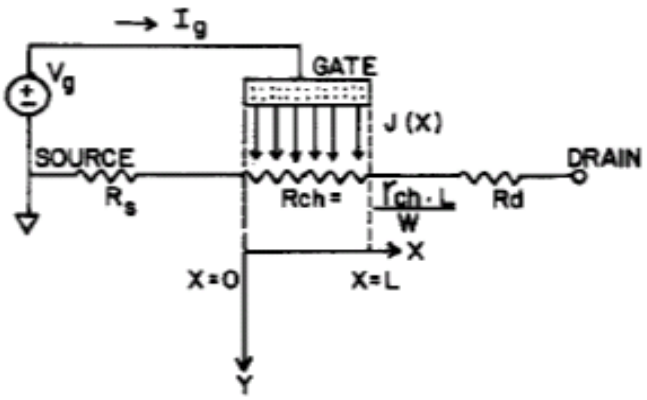


Figure 38: "End" resistance measurement technique [6].

The "end" resistance measurement technique is used for the Cascode LNA, which is shown in Fig. 39. The drain and gate 2 are both floating so that the drain serves as a voltage "probe". And the source resistance R_s is calculated as:

$$R_s = \frac{\Delta V_{DS}}{\Delta I_{G1S}} \tag{69}$$

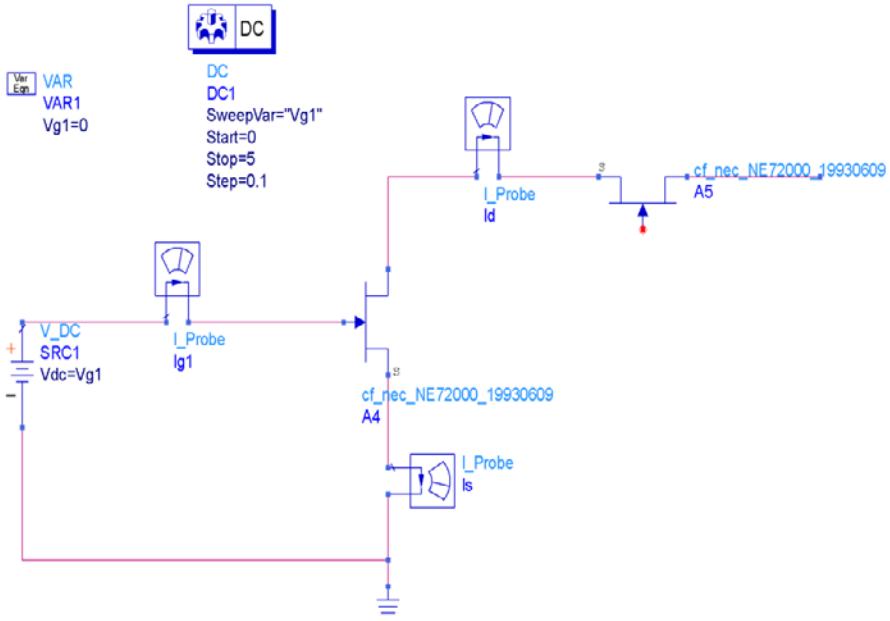


Figure 39: DC simulation for parasitic source resistance R_s in ADS.

Based on eq. (69) and Fig. 40, the parasitic source resistance R_s is equal to 0.375 Ω.

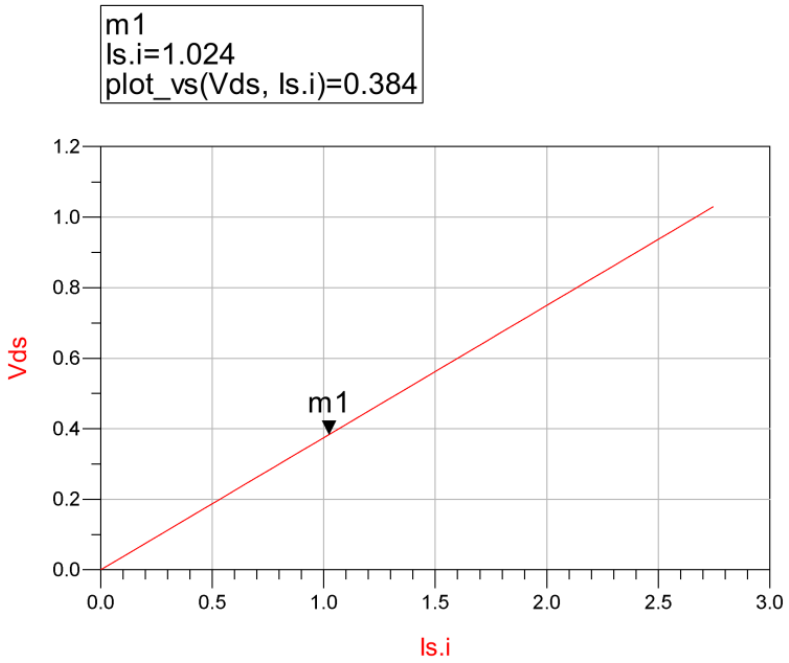


Figure 40: V_{ds} versus I_s when the drain and gate 2 are floating.

5.5.2.2 Parasitic drain resistance

To estimate the parasitic drain resistance, the similar technique is deployed. Instead of the drain and gate 2 floating, the source and gate 1 are floating now, and a voltage source is applied on the gate 2, which is shown in Fig. 41. The drain resistance is estimated as:

$$R_d = \frac{\Delta V_{SD}}{\Delta I_{G2S}}\Big|_{S,G_1\text{float}} \tag{70}$$

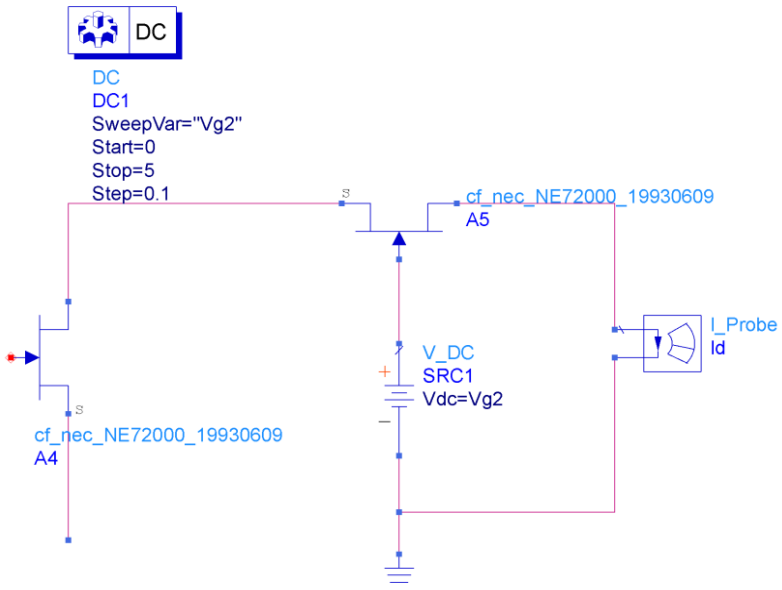


Figure 41: DC simulation for parasitic drain resistance R_d in ADS.

The V_{sd} versus I_d curve is almost linear, which is shown in Fig. 42. Using eq. (70), R_d is estimated to be 7.8 Ω.

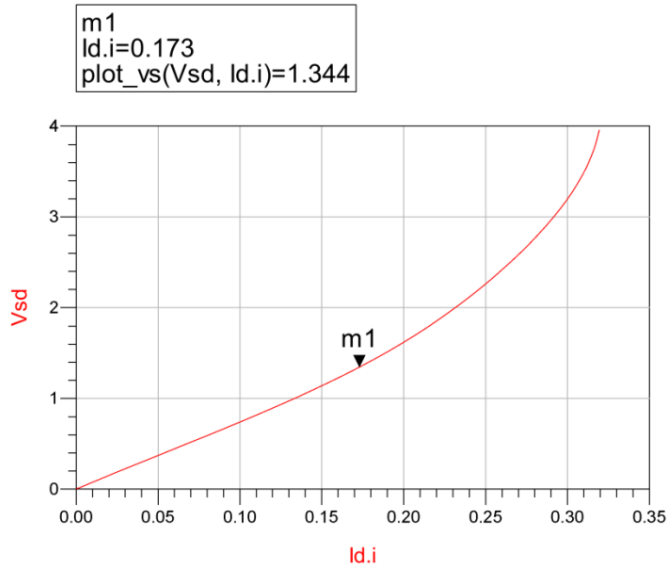


Figure 42: V_{sd} versus I_d when the source and gate 1 are floating.

5.5.2.3 Parasitic inter gate resistance

The inter gate resistance R_{12} follows from:

$$R_{12} = \frac{\Delta V_{DS}}{\Delta I_{G2S}} - R_s\Big|_{D,G_1 \text{ float}} \tag{71}$$

The drain and gate 1 are floating, and a voltage source is applied at gate 2. Thus the current flows through the inter gate resistance and source resistance. The simulated V_{ds} versus I_d curve is shown in Fig. 44.

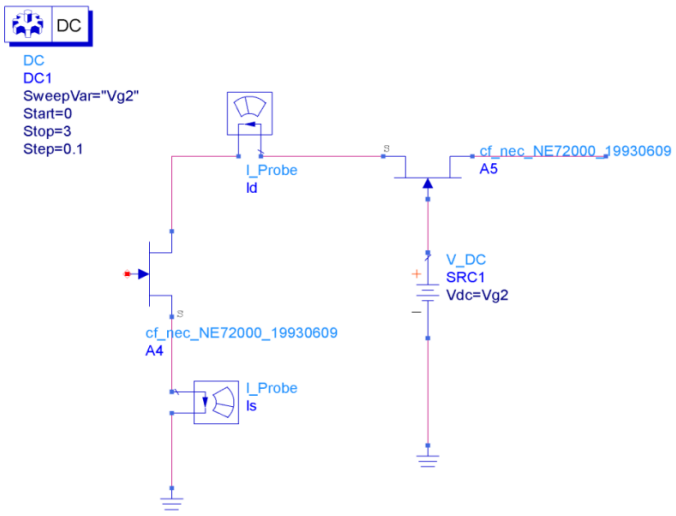


Figure 43: DC simulation for parasitic inter gate resistance R_{12} in ADS.

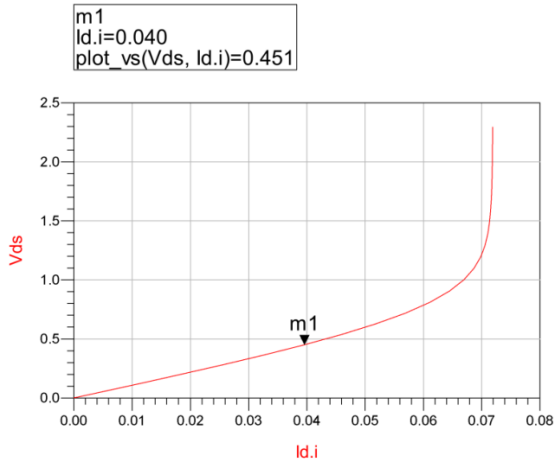


Figure 44: V_{ds} versus I_d when the drain and gate 1 are floating.

From Fig. 44 and eq. (71), the inter gate resistance R_{12} is estimated to be 10.9 Ω.

6. Construction of a Test Bench

6.1 S-parameters from Agilent ATF551M4 Cascode LNA

The Advanced Curtice 2 model is used to build the test bench for the Cascode LNA. And its parameters are based on the Agilent ATF551M4 MESFET, which is shown in Fig. 45.

Figure 45: The Advanced Curtice 2 model based on the ATF551M4 MESFET.

Two ATF551M4 MESFETs are cascaded together with the proper bias condition in ADS, which is shown in Fig. 46. The DC bias condition shown in Table 3 makes FET 1 operate in the linear region and FET 2 in the active region.

Table 3: DC bias condition for FET1 in linear region and FET2 in saturation

V_{g1}(V)	V_{g2}(V)	V_{ds}(V)	I_d(mA)
1.2	1.1	5	301

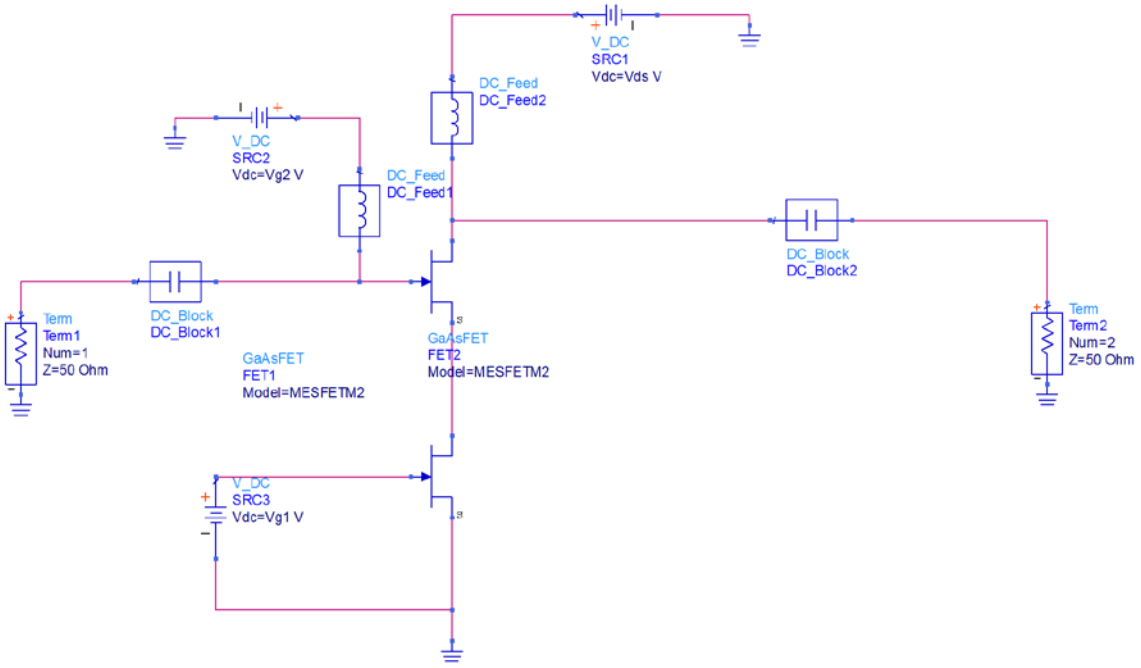


Figure 46: S-parameters simulation when FET 1 is in the linear region and FET 2 in saturation.

The S-parameter results, shown in Table 4, are then converted to Z parameters. Using eq. (66), the intrinsic device elements can be estimated. First, the parasitic effects are ignored. Thus the Z-matrix only subtracts the FET 1 series resistance and then is converted to Y-parameters.

Table 4: S-parameters from 1GHz to 5GHz

freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)
1.000 GHz	0.963 / -87.371	0.042 / 44.999	23.944 / 134.707	0.587 / -116.272
1.500 GHz	0.948 / -110.147	0.049 / 33.587	18.805 / 123.151	0.673 / -133.471
2.000 GHz	0.940 / -124.697	0.053 / 26.353	15.171 / 115.771	0.716 / -143.648
2.500 GHz	0.935 / -134.503	0.055 / 21.482	12.603 / 110.754	0.740 / -150.261
3.000 GHz	0.932 / -141.464	0.056 / 18.013	10.733 / 107.139	0.754 / -154.858
3.500 GHz	0.930 / -146.627	0.057 / 15.423	9.325 / 104.403	0.763 / -158.220
4.000 GHz	0.929 / -150.592	0.057 / 13.416	8.233 / 102.251	0.769 / -160.776
4.500 GHz	0.928 / -153.726	0.058 / 11.812	7.364 / 100.502	0.774 / -162.779
5.000 GHz	0.927 / -156.261	0.058 / 10.499	6.657 / 99.043	0.777 / -164.386

6.2 Comparison between the estimated model and the actual one without parasitic estimation

Based on the steps in section 5.4, the intrinsic device element values for the ATF551M4 MESFET are estimated. Table 5 shows the comparison between the estimated component values and the actual values.

Table 5: Comparison between the estimated values and the actual values

ATF551M4 FET component	g_m(A/V^2)	R_{gs}(Ω)	C_{gs}(pF)	C_{gd}(pF)	C_{ds}(pF)	R_{ds}(Ω)
Actual values	0.444	0.5	0.6193	0.1435	0.1	390
Estimated values	0.6472	0	0.477	0.143	0.08	70.9

We pick frequencies f = 1GHz, 1.2GHz, 1.4GHz, 1.6GHz, 1.8GHz and 2GHz. For each frequency, we can then use the Y-parameter data to estimate C_{gd}, C_{gs}, C_{ds}, g_m, R_{gs}, R_{ds} . The average values for each components are shown in Table 5. There are some difference between the actual values and the estimated values. The reason may be the neglection of the parasitic capacitance and inductance and external resistances.

The following smith charts show the comparison between the model prediction and the actual ones. The blue line represents the model prediction, and the red line shows the results for ATF551M4 MESFET. For S_{11} and S_{22}, the comparison shows good agreement. And for S_{12}, there is some discrepancy, and it may due to the feedback capacitance and resistance.

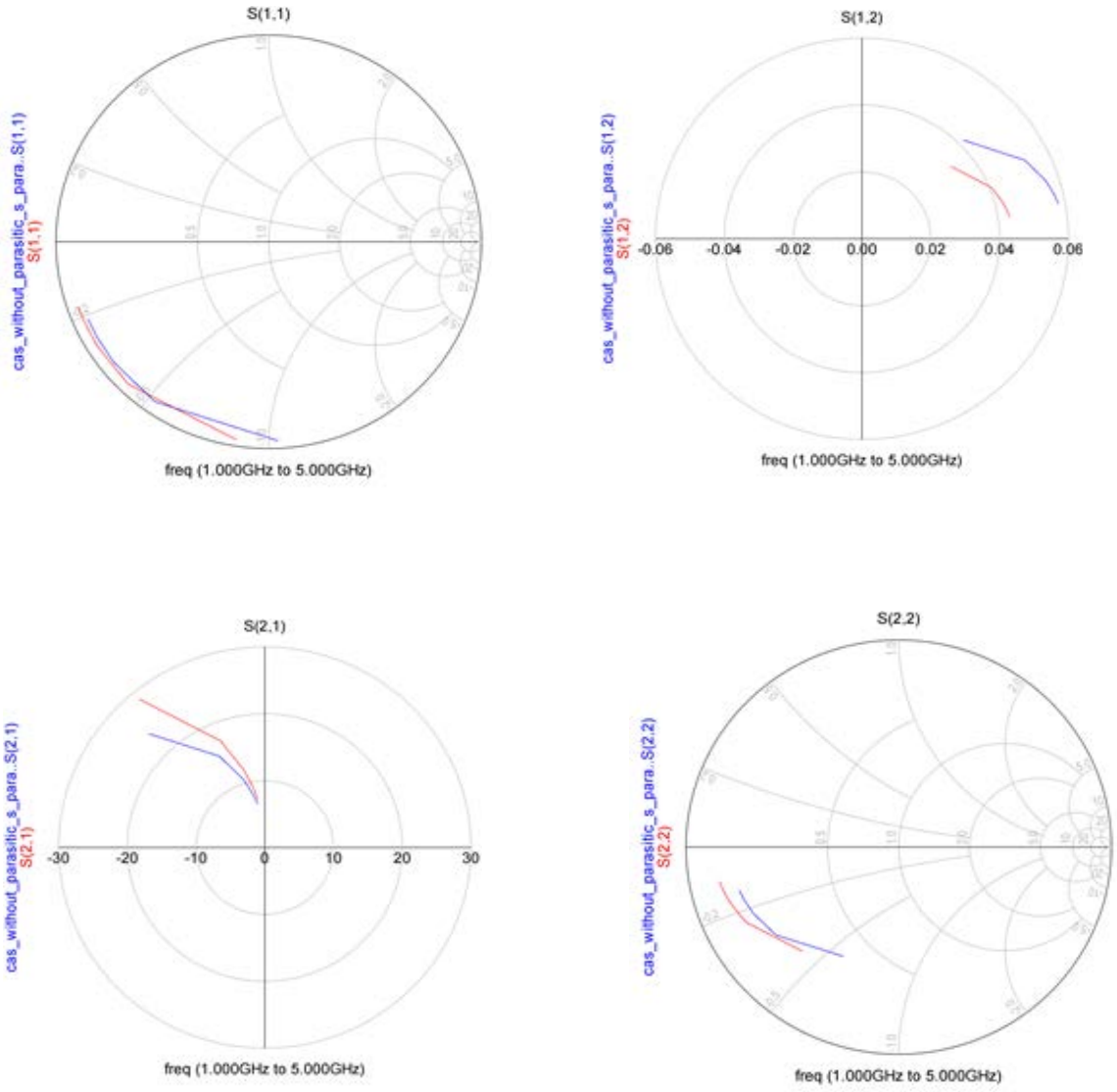


Figure 47: Smith Chart comparison between the model prediction and the ATF551M4 behavioral model.

We can also compare them from a different view. In Fig. 48, it shows the input impedance, the gain and the output impedance comparison, where the blue line represents the model prediction, and the red line shows the results for ATF551M4 MESFET. From the comparison, there is small difference at higher frequencies.

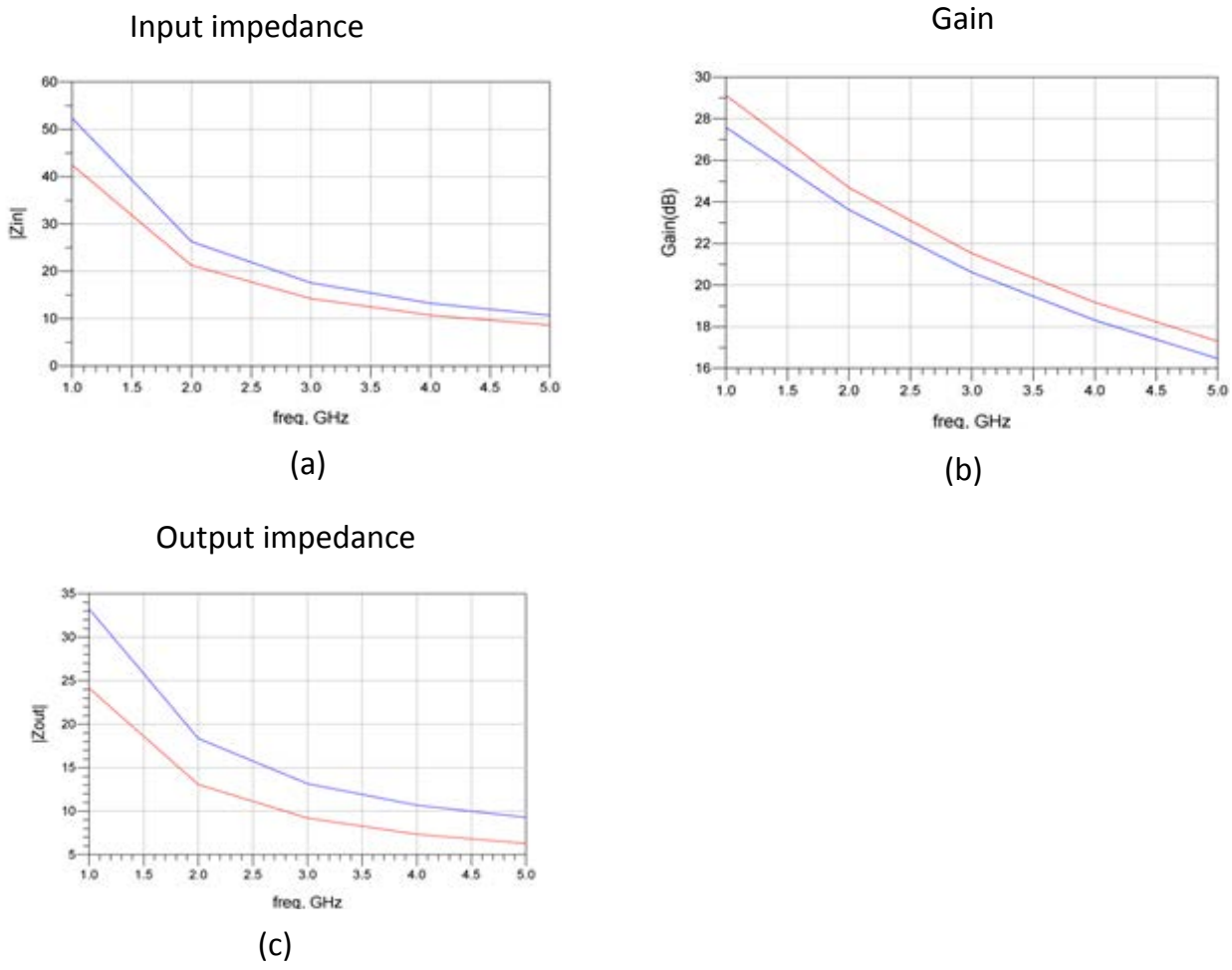


Figure 48: The comparison of (a) the input impedance, (b) the gain and (c) the output impedance.

6.3 Parasitic effects

The above results do not include parasitic parameters in the Advanced Curtice 2 model, which makes the device become ideal. However, If we need to model a realistic device, the parasitic effects have to be considered. Parasitic component values are entered into the Advanced Curtice 2 model, which is shown in Fig. 49. The parasitic components are the following:

R_d = 2.205 Ω, R_g = 1.7 Ω, R_s = 0.675 Ω and L_g = 0.094 nH.

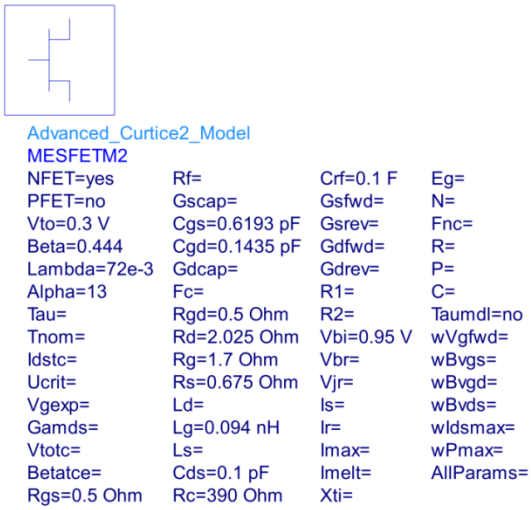


Figure 49: The Advanced Curtice 2 model with parasitic parameters included.

Using the steps mentioned in section 5.4, the intrinsic device element values are calculated and summarized in Table 6.

Table 6: Comparison between the estimated values and the actual ones with parasitic effects

ATF551M4 FET component	g_m(A/V^2)	R_{gs}(Ω)	C_{gs}(pF)	C_{gd}(pF)	C_{ds}(pF)	R_{ds}(Ω)
Actual values	0.444	0.5	0.6193	0.1435	0.1	390
Estimated values	0.424	5.07	0.5	0.143	0.17	145

After the intrinsic device element values are estimated, we run the S-parameters simulation for the Cascode LNA model and compare them with ATF551M4 MESFET.

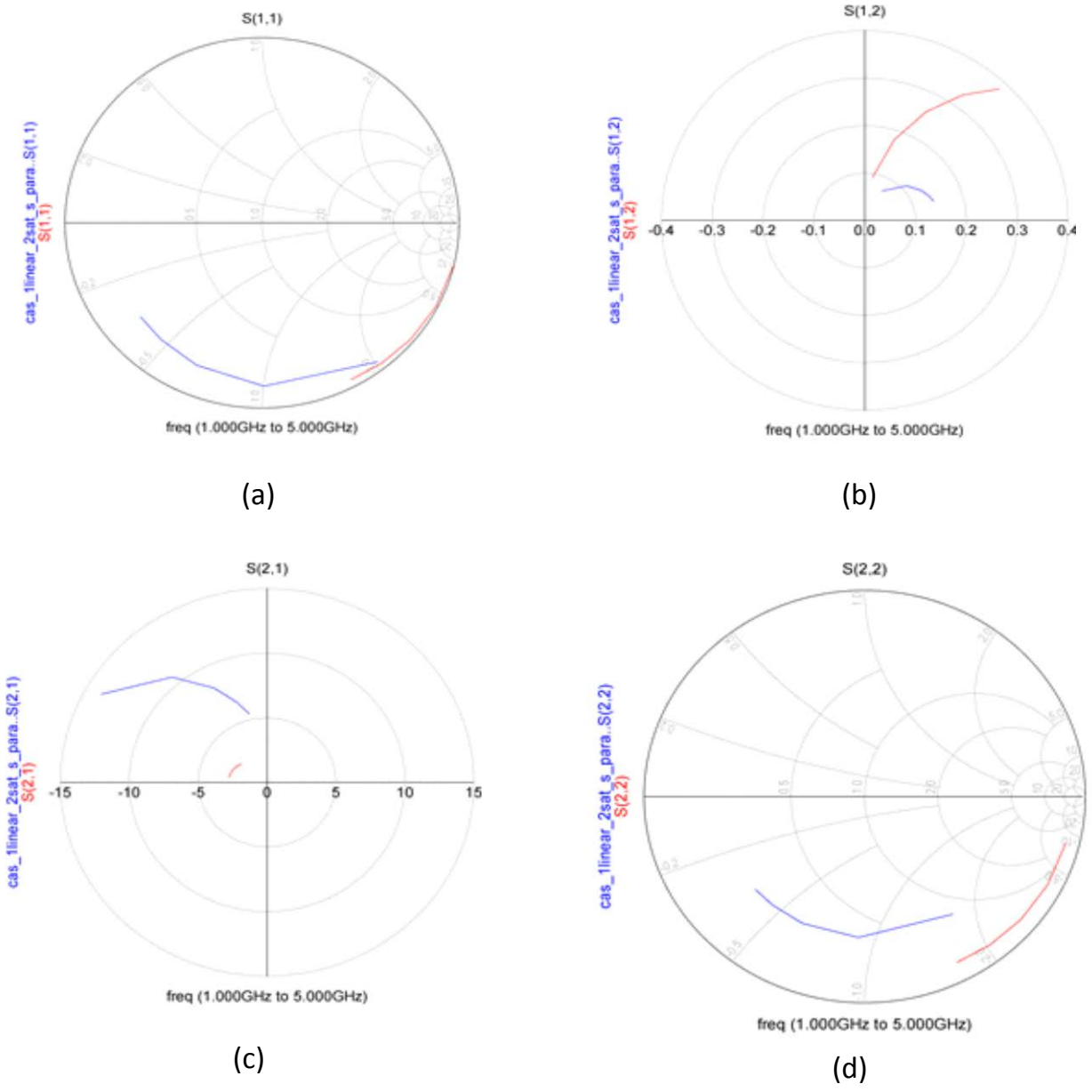


Figure 50: S-parameters comparison between the model prediction and ATF551M4 with parasitic effects. (a) S(1,1), (b) S(1,2), (c) S(2,1), (d) S(2,2).

The red curve is the model prediction and the blue one shows the actual S- parameters. The discrepancy indicates that the parasitic effects have a big influence for the estimated model, even though the parasitic component values are very small.

6.3 Realistic device verification

Two NEC N-channel devices are cascaded to build a Cascode LNA, which is shown in Fig. 51. Also, appropriate DC bias conditons are applied to this circuit to make both FETs work in saturation region.

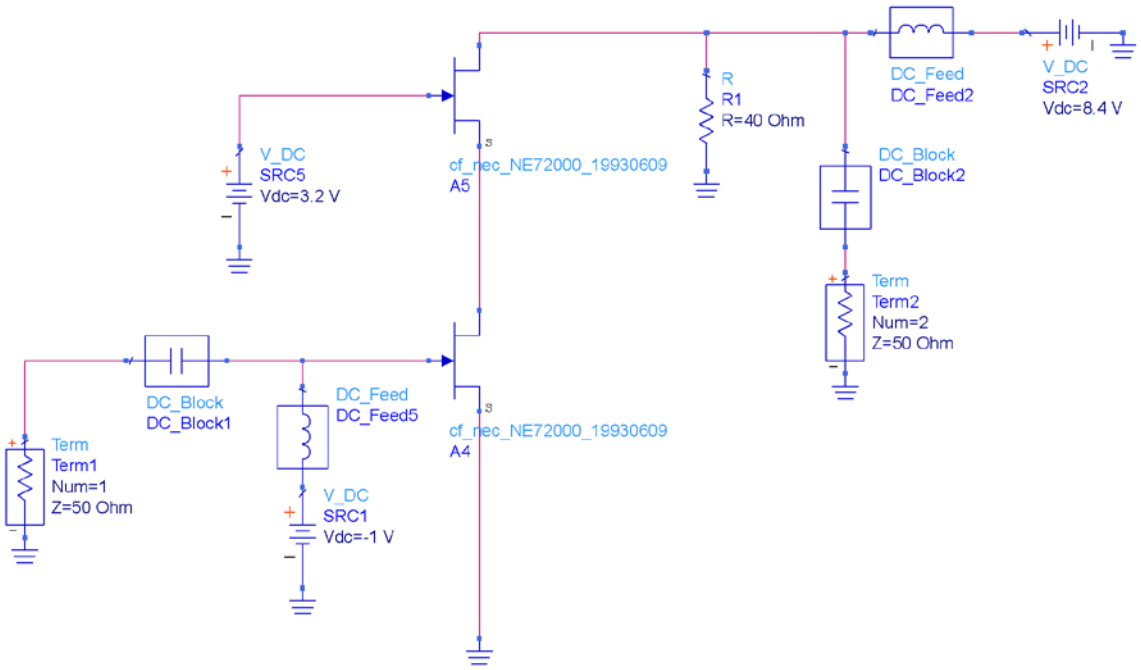


Figure 51: The Cascode LNA using NEC realistic devices.

Table 7: DC bias condition for the NEC Cascode LNA working in saturation

V_{g1}(V)	V_{g2}(V)	V_{ds}(V)	I_d(mA)
-1	3.2	8.4	10.1

Based on the estimated parasitic component values in 5.5.2 and the algorithm is 5.2, the intrinsic device component values and parasitic component values for the NEC Cascode LNA are estimated, which is shown in Tables 8 and 9.

Table 8: Estimated values of the intrinsic devices for the NEC Cascode LNA

	g_m(A/V^2)	R_{gs}(Ω)	C_{gs}(pF)	C_{gd}(pF)	C_{ds}(pF)	R_{ds}(Ω)
Estimated values	0.0045	603	0.279	0.103	0.096	1000

Table 9: Estimated values of the parasitic components for the NEC Cascode LNA

	R_s(Ω)	R_d(Ω)	R_{12}(Ω)	C_{pg1}(pF)	C_{pg2}(pF)	C_{pd}(pF)
Estimated values	0.375	7.8	10.9	0.08	0.04	0.16

With these values, a Cascode LNA model for the NEC Cascode LNA (from 1GHz to 5GHz) can be built. It is shown in Fig. 52.

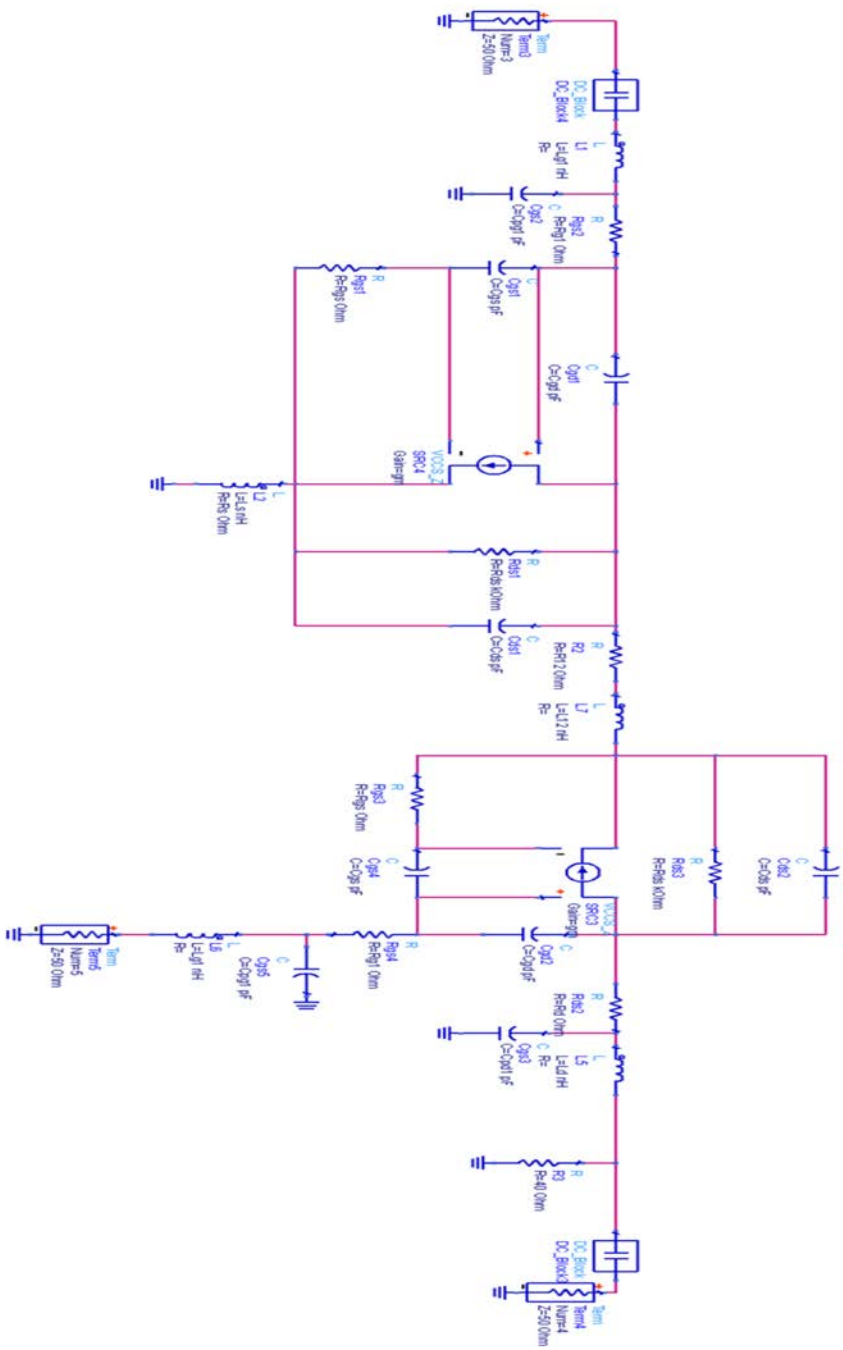


Figure 52: A Cascode LNA model for the NEC Cascode LNA.

Once we obtain the model component values, the S-parameter simulation is run on the estimated model. Also, the S-parameters comparison between the model prediction and the NEC Cascode LNA is conducted, as shown in Fig. 52. In Fig. 53, the blue lines are the model predictions and the red ones are the actual device response.

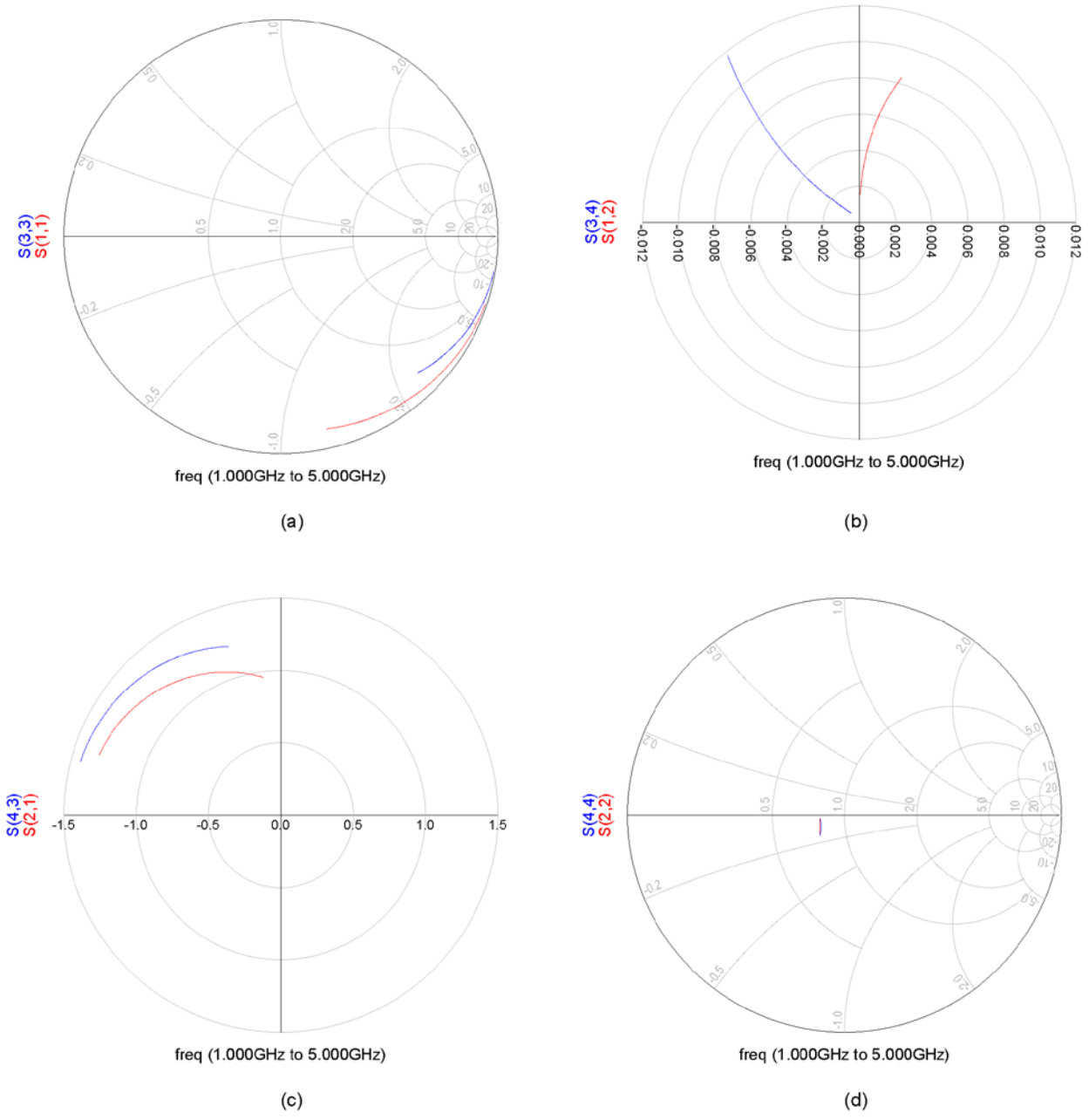


Figure 53: S-parameters comparison between the NEC Cascode LNA and the model prediction. (a) S(1,1) and S(3,3), (b) S(1,2) and S(3,4), (c) S(2,1) and S(4,3), (d) S(2,2) and S(4,4).

From this comparison, there is some difference between the S-parameters. This may be due to the estimation method for the parasitic components, which is not highly accurate. But, the results generated from the model is acceptable in general, since it gives reasonable starting point for the optimization.

6.4 Optimization Results

As in the previous section, the intrinsic device component values and the parasitic component values are both estimated using the algorithm in 5.2. Also, a Cascode LNA model within the frequency range from 1GHz to 5GHz for the NEC Cascode LNA is built. Besides, the comparison results between the model prediction and the actual device show good agreement. These component values are given as the initial values for the optimization tool in ADS. Since the starting values are reasonable, the gradient search method is used in optimization. The least square error function is used in Gradient optimizer, as is shown in eq.(71). In Fig.54, the least square error ε is 0.3 based on the performance measurement.

$$\varepsilon = \sum_{i=1}^{4} W_i |simulation_i - goal_i|^2 \qquad (71)$$

where W_i are constant weighting factors and i denotes the four goals of optimization.

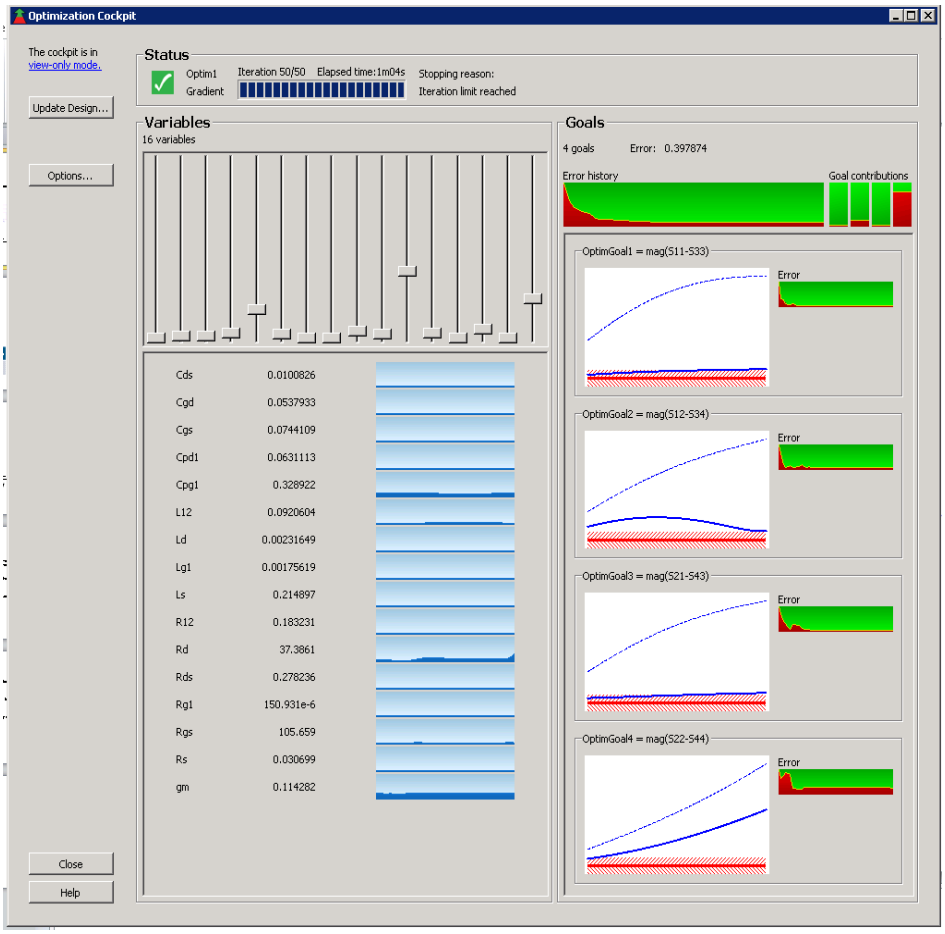


Figure 54: Optimization in ADS for the Cascode LNA model.

After the Cascode LNA model is optimised, the final values for the model are shown in the Tables 10 to 12.

Table 10: Intrinsic device component values after optimization

	g_m(A/V^2)	R_{gs}(Ω)	C_{gs}(pF)	C_{gd}(pF)	C_{ds}(pF)	R_{ds}(Ω)
Estimated values	0.114	105	0.279	0.053	0.01	278

Table 11: Parasitic resistance and capacitance values after optimization

	R_s(Ω)	R_d(Ω)	R_{12}(Ω)	C_{pg1}(pF)	C_{pg2}(pF)	C_{pd}(pF)
Estimated values	0.03	37.4	0.12	0.33	0.33	0.063

Table 12: Parasitic inductance values after optimization

	L_s(nH)	L_d(nH)	L_{g1}(Ω)	L_{g2}(pF)
Estimated values	0.03	37.4	0.12	0.33

After the Cascode LNA model is optimized in ADS; it shows good agreement with the actual device. In Fig. 55, the blue line represents the model prediction for the S-parameters, and the red line represents the results from the actual device.

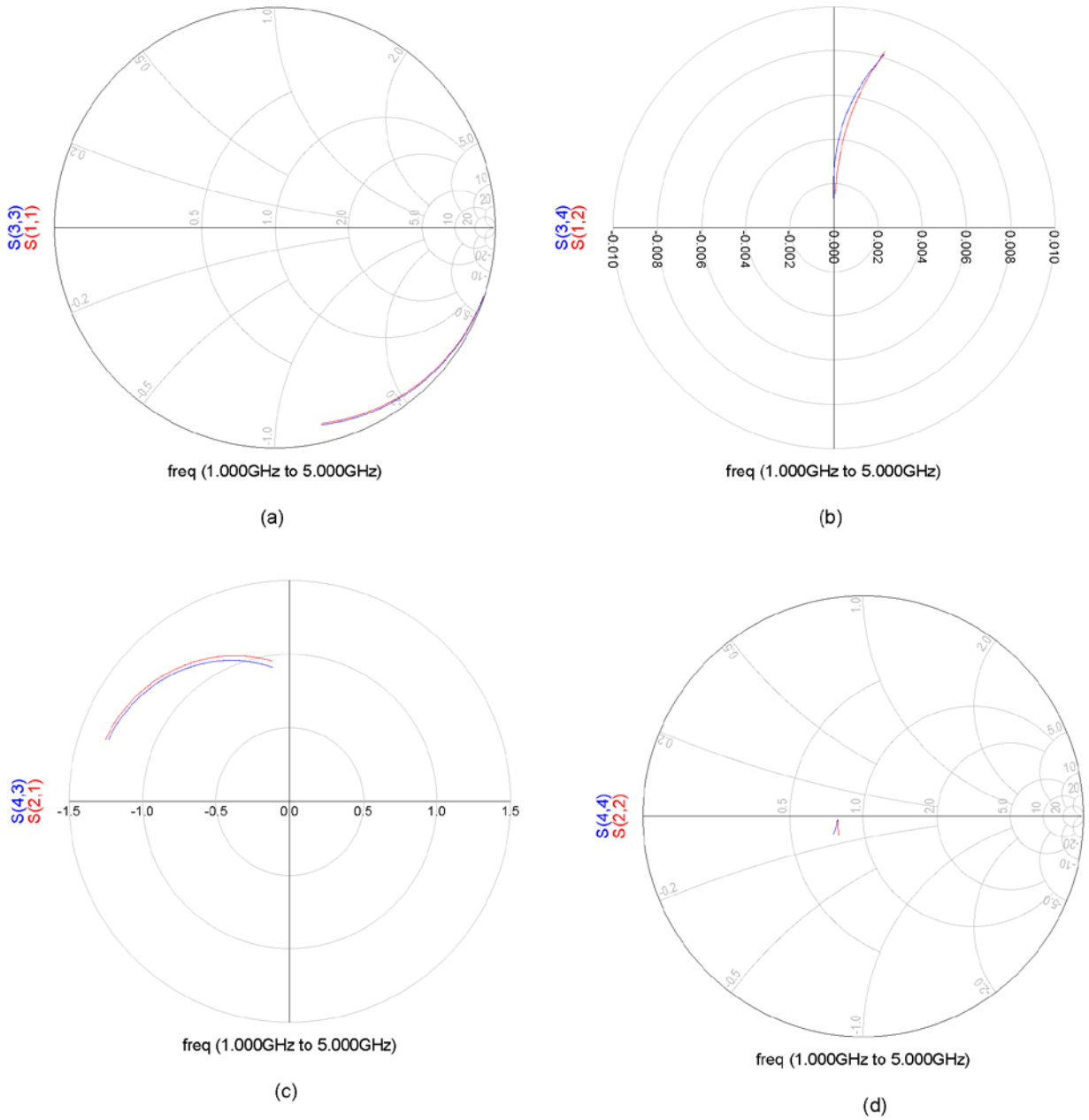


Figure 55: S-parameters comparison between the NEC LNA and the CascodeLNA model optimization in ADS. (a) S(1,1) and S(3,3),(b) S(1,2) and S(3,4),
(c) S(2,1) and S(4,3), (d) S(2,2) and S(4,4).

7. Conclusions

A procedure for extracting the small signal equivalent circuit elements of the Cascode LNA has been described. All the intrinsic device component values and parasitic element values are directly estimated from DC and RF measurements using analytical formulas. The values of the extrinsic series resistance are estimated from physical modeling. In this thesis, a circuit model of a cold Cascode LNA ($V_{DS} = 0$) is proposed to consider the distributed channel resistance. The element values of extrinsic series resistance are then extracted by using the "end resistance measurement" method. The extrinsic elements of capacitance and inductance are extracted using three-port Y-matrix and Z-matrix calculations with gate 1 or 2 of the Cascode LNA at forward bias or reverse bias. In this thesis, it is shown that the extrinsic parasitic effects have significant influence on the model prediction. For the intrinsic elements, the bidirectional DC transfer characteristics are used to find the proper bias voltages, which makes one FET work in the linear region and the other FET in saturation. Then, the intrinsic small-signal elements are deduced from Y-parameters. These values show good agreement with the actual LNA, and are reasonable starting values for optimization. Moreover, the optimization method is deployed for the estimated model, which helps obtain accurate component values for the Cascode LNA model. At the end of optimization using gradient search, the least error function gives 0.39 with respect to the goals.

Due to its relative simplicity and ease of parameter estimation (while maintaining acceptable accuracy) the method provides the RF engineers with a design template that enables rapid prototyping and customization. The small signal model will also be of benefit to manufacturers of semiconductor devices, since it enables the investigation of linearity, noise performance, gain, and power consumption.

8. Future work

This modeling method for Cascode LNAs is conducted within the ADS simulator environment. In order to obtain better verification of the modeling method, a realistic Cascode LNA device has to be used for the test. Since the operation frequency range for the Cascode LNA model is from 1GHz to 5GHz, we need to expand the bandwidth of operation so that the model can be used in this wideband application. The model proposed in the thesis only considers the S-parameter performance; it needs to be expanded to conduct noise performance and shows the noise figure comparison between the model prediction and the actual device response. Although the estimation values for the Cascode LNA model provide accpectable starting values for optimization, there are still errors between the model and the actual device. Thus, the model still needs to be modified to reduce the initial errors, and we also need to find a more accurate way to estimate the parasitic components. Moreover, we need to test the modeling method for other non-FET devices that do not rely on the Curtice 2 model.

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Appendix A – Relationships between three-port Z-parameters of the Cascode MESFETS

In order to get the equations in eq.(58), we should notice the following equations based on Figure 19.

$$V_1 = V_1^I \tag{A.1}$$

$$V_2 = V_2^I + V_1^{II} \tag{A.2}$$

$$V_3 = V_2^I + V_2^{II} \tag{A.3}$$

$$i_1 = i_1^I \tag{A.4}$$

$$i_2 = i_1^{II} \tag{A.5}$$

$$i_3 = i_2^{II} \tag{A.6}$$

The three-port Z-paramters are

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{A.7}$$

From (A.7), we can get

$$Z_{22} = \left. \frac{V_2}{I_2} \right|_{i_1=0, i_3=0} \tag{A.8}$$

For port 1 and port 2 in Figure 19, the two-port Z-parameters are

$$\begin{bmatrix} V_1^I \\ V_2^I \end{bmatrix} = \begin{bmatrix} Z_{11}^I & Z_{12}^I \\ Z_{21}^I & Z_{22}^I \end{bmatrix} \begin{bmatrix} i_1^I \\ i_2^I \end{bmatrix} \tag{A.9}$$

$$\begin{bmatrix} V_1^{II} \\ V_2^{II} \end{bmatrix} = \begin{bmatrix} Z_{11}^{II} & Z_{12}^{II} \\ Z_{21}^{II} & Z_{22}^{II} \end{bmatrix} \begin{bmatrix} i_1^{II} \\ i_2^{II} \end{bmatrix} \tag{A.10}$$

Since i_1 = 0 and i_3 = 0, V_2^I and V_1^{II} can be represented by

$$V_2^I = Z_{22}^I i_2^I = Z_{22}^I i_2 \tag{A.11}$$

$$V_1^{II} = Z_{11}^{II} i_1^{II} = Z_{11}^{II} i_2 \quad \text{(A.12)}$$

Based on (A.2), we get

$$Z_{22} = (Z_{22}^{I} + Z_{11}^{II}) \quad \text{(A.11)}$$

Using a similar method, we can get the rest of the equations in eq.(58).

Appendix B – Matrix Conversion

The following transfromations accomplish the conversion between Z-, Y-, and S-parameters.

$$Z = Z_0(I+S)(I-S)^{-1} \tag{B.1}$$

$$S = (Z - Z_0 I)(Z + Z_0 I)^{-1} \tag{B.2}$$

$$Y = \frac{1}{Z_0}(I-S)(I+S)^{-1} \tag{B.3}$$

$$S = (I - Z_0 Y)(I + Z_0 Y)^{-1} \tag{B.4}$$

where

S network S-parameters,

I identity matrix,

Z network Z-parameters,

Y network Y-parameters,

Z_0 characteristic impedance.