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Noise Analysis and Simulation of a Sub-Pixel Analog to Digital Voltage-To-Frequency Converter for use with IR Focal Plane Arrays

Curtis Benson Colonero
Worcester Polytechnic Institute

WORCESTER POLYTECHNIC INSTITUTE

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NOISE ANALYSIS AND SIMULATION OF A SUB-PIXEL ANALOG TO DIGITAL VOLTAGE-TO-FREQUENCY CONVERTER FOR USE WITH IR FOCAL PLANE ARRAYS

BY

CURTIS BENSON COLONERO

B.S., Pennsylvania State University, 1998

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Approved by

First Reader _____

Brian M. King
Thesis Advisor, Assistant Professor
of Electrical and Computer Engineering

Second Reader _____

John A. McNeill
Associate Professor
of Electrical and Computer Engineering

Third Reader _____

Fred J. Looft
Professor and Department Head
of Electrical and Computer Engineering

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Abstract

The performance of a dedicated A/D converter located beneath each pixel is explored in this thesis. Specifically, a voltage to frequency converter coupled with a direct injection amplifier designed for use with an IR focal plane array is analyzed. This versatile implementation of a Readout Integrated Circuit can be found applicable to a wide variety of imaging technologies.

Noise performance of the conversion system is theoretically calculated, and is supported by SPICE simulations using valid CMOS SPICE models. It is shown that a 10 transistor sub-pixel voltage to frequency analog to digital converter will produce noise that is less than the input shot noise. Design considerations will be addressed to ensure continued performance as the scale of the imagers increase to large format arrays.

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List of Symbols

A_{Cint}	Area of integration capacitance
C_{dep}	Depletion capacitance
C_g	Combined input gate capacitance of inverter
C_{int}	Integration capacitance
C_{ox}	Gate oxide capacitance per unit area
C_{xx}	Capacitance between node x and node x
g_m	Transconductance
I_d	Drain current
I_{dark}	Dark current
I_{DC}	DC current
I_{int}	Integrated current
I_{ph}	Photocurrent
I_{sat}	Drain current in saturation
k	Boltzmann's constant
L	Transistor length
mFR	Minimum allowable frame rate
N	Number of bits in counting circuitry
n	MOSFET ideality factor
n_i	Carrier concentration in silicon channel region
N_{dep}	Doping concentration in the depletion region
P	Period length
q_e	Electron charge

q_x	Charge at node x
R_{ph}	Photodiode shunt resistance
T	Temperature
t_d	Propagation delay
t_{int}	Integration period
t_{ox}	Oxide thickness
$V_{cathode}$	Photodiode cathode voltage
V_{di_bias}	Direction Injection amplifier bias
V_{gs}	Gate to source voltage
V_{ith}	Inverter threshold voltage
V_{ph_bias}	Photodiode bias
V_{sat}	Peak to peak saturation voltage of an A/D converter
V_{thp}	PMOS transistor threshold voltage
V_{thn}	NMOS transistor threshold voltage
W	Transistor width
ε_o	Permittivity in a vacuum
ε_{ox}	Permittivity of gate oxide
ε_{si}	Permittivity of silicon
φ_s	Surface potential
ΔT	Measurement interval
μ_n	Mobility ratio

List of abbreviations and acronyms

CMOS	Complementary Metal Oxide Semiconductor
CMOS9SF	IBM CMOS 90nm Standard Process
COTS	Commercial off the Shelf
DBFS	Decibels Below Full Scale
EMI	Electromagnetic Interference
ENOB	Effective Number of Bits
HgCdTe	Mercury-Cadmium-Telluride
IC	Integrate Circuit
IP	Intellectual Property
IR	Infrared
K	Kelvin
LSB	Least Significant Bit
MSB	Most Significant Bit
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
ROIC	Readout Integrated Circuit
SPICE	Simulation Program with Integrated Circuit Emphasis
SNR	Signal to Noise Ratio
SRAM	Static Random Access Memory
VTOF	Voltage to Frequency Converter

1 Introduction

This thesis is divided into five main chapters. Applications, design and operation of a Voltage-To-Frequency converter will be covered in section 1. Theoretical development of the noise in the Voltage to Frequency Converter (VTOF) and the experimental simulation of these individual noise sources covered in sections 2 and 3. Techniques for reducing the total system noise in scalable designs will be discussed in section 4. Section 5 concludes by summarizing the results of the thesis.

This thesis intends to answer this question of performance. Can a FPA using a VTOF beneath each pixel perform as well or better than the conventional shot noise limited architecture which is failing to meet the aggressive requirements of the future? If the desired noise performance can be reached, the possible advantages in area consumption, speed and power consumption will be addressed.

1.1 Applications

The principal benefit of using a sub-pixel readout integrated circuit (ROIC) is its scalability. Designs meeting performance, area, and power requirements can be easily arrayed to accommodate large format imagers. A full conversion system built within a 15 micron footprint will be applicable to the majority of Long-Wave Infrared (LWIR) applications that typically use pixels sizes between 15 and 60 microns.

Sub-pixel digital ROIC technologies can be made available through intellectual property (IP) distributors. Similar to IP offered for scalable static random access memories (SRAM), designers can use the available ROIC IP to quickly design an efficient imaging system suiting their specific needs. The massive task of laying out an ROIC from scratch can now be started at the pixel block level. Together with IP

structures containing high speed digital output technology, full image capture and processing systems can be implemented on a single die.

1.2 Transistor Process Information

All calculations and simulations are based on the standard IBM CMOS 90 nanometer process flow (CMOS9SF). Simulations were done using the supplied IBM SPICE models. Temperature for all measurements was chosen to be 218K (*T*) due to the fact that the supplied SPICE models are only valid down to -55C.

Ideally the calculations and simulations would be done at 77K, the cryogenic temperature where many of the applicable focal plane arrays will operate. Unfortunately, cryogenic simulation models for this process are unavailable. IBM has only hardware verified the models down to -55º Celsius. In order to have a tested simulation comparison for the theoretical analysis, this lower temperature bound is used. It is assumed that imagers operating at cryogenic temperatures will experience noise that is less than or equal what is modeled at -55º Celsius.

1.3 Operational Characteristics

Figure 1-1 diagrams the schematic of a voltage to frequency converter. Appendix F contains an enlarged version of Figure 1-1 for increased readability. The converter consists of 9 transistors, 8 of which are in the configuration of 4 static CMOS inverters.[i] A current at the input node *int* charges the gate, drain, and parasitic capacitances seen by this node. Appendix C details the calculation of this capacitance value for use in the theoretical noise calculations.

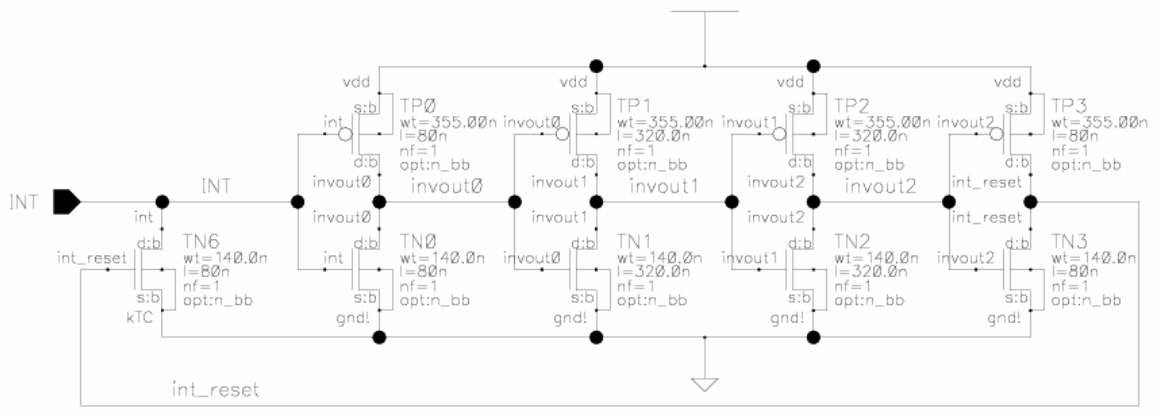

Figure 1-1 Voltage-To-Frequency Converter

Once the threshold of 0.4504 (V_{ith}) volts for the first inverter is reached, the output of the first inverter is pulled to ground. In result, the remaining three inverters trigger and the pulse propagates to the output of the final inverter. This active-high output pulse triggers the reset NMOS transistor *(TN6)* as well as clocks any circuitry designed for counting the number of pulses This reset transistor discharges the integrated voltage to ground, or alternatively to an applied voltage. During this discharge time, the output of the first inverter is pulled high and the remaining three inverters change state leaving the *int_reset* node once again at ground. The VTOF is now in its initial state and the preceding process repeats. Appendix C details the inverter's threshold calculation.

The middle two inverters have gate lengths that are four times the minimum for the 90 nm process. This increased gate length limits the current traveling through these two inverters resulting in longer rise and fall times. This also results in a wider output pulse period allowing the integration capacitance to fully discharge before the pulse is deactivated. Without this wider reset pulse, the integration capacitance is left with residual voltage after each reset period hindering the performance of the converter.

Increasing the amplitude of the input current increases the rate of change for the voltage. Continuously reaching this threshold quicker results in a higher frequency output pulse rate. For any given period of time, the number of output pulses counted corresponds to the current input intensity over that time period. When connected to a photodiode, the output frequency is directly proportional to the amount of photons within the detectors sensitivity range absorbed in its active region. This ratio is also dependent on the injection efficiency of the system which defines the percentage of photocurrent lost during any integration period.

Basic transient operation of the converter is shown in Figure 1-2.[i] Both the voltage at the integration capacitance and pulse output for an ideal DC current input are shown. The discharge or reset time has a varying effect on the converter based on the input rate. This individual integration time to reset time ratio can be characterized as a non-linearity in this ADC system and does not qualify as a noise.[i] However, the jitter seen in the 4 stage ring oscillator which will be discussed later can be modeled as an additive noise to the system.

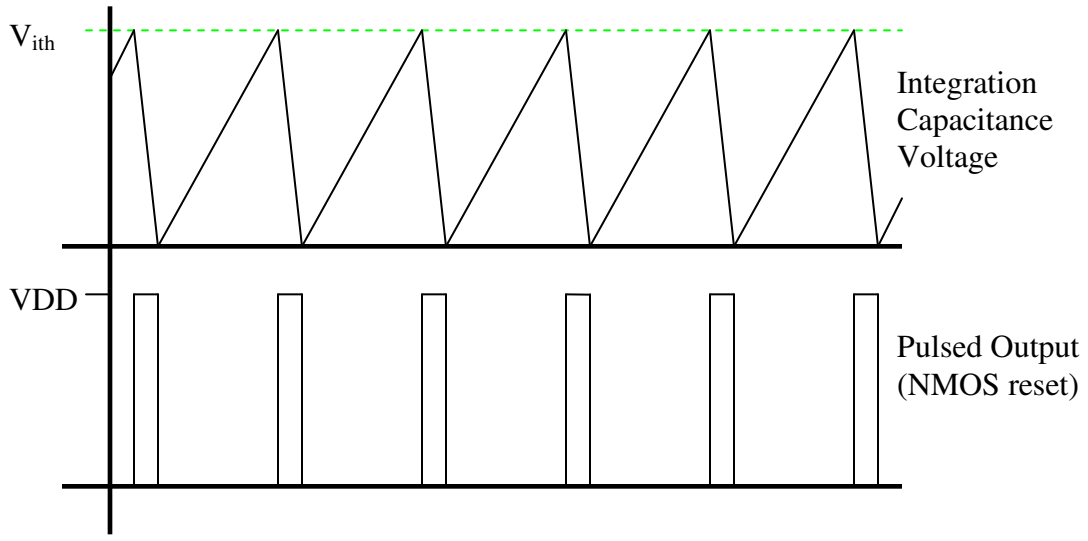

Figure 1-2 Voltage-To-Frequency Transient Operation

1.3.1 Photodiode and Direct Injection Amplifier Characteristics

Before modeling the noise of the system, decisions must be made regarding the operational characteristics of the photodiode. The photodiode will be reverse biased with approximately -30 mV which will place it in a comfortable range away from the higher noise forward-bias region.[iii] Considering submicron process variations which will vary the designed bias level, the 30 mV buffer is chosen to ensure that no single diode is forward-biased throughout our entire array. This bias across the photodiode (V_{ph_bias}) is set by the Equation (1-1) where V_{di_bias} is the voltage at the gate of direct injection (DI) amplifier, V_{thp} is the threshold of the PMOS transistor, and $V_{cathode}$ is the voltage at the cathode of the photodiode.

$$V_{ph\_bias} = V_{di\_bias} - V_{thp} - V_{cathode} \quad \textbf{(1-1)}$$

The photodiode's shunt resistance can be modeled as a 150 MΩ (R_{ph}) resistor for 30 micron longwave infrared (LWIR) Mercury-Cadmium-Telluride (HgCdTe) detectors like the ones contemplated in this work. The photodiode cathode voltage (detector common) is modeled as an ideal source.

For simulation purposes, the photodiode will be modeled using a piece-wise linear current source and resistor in parallel. HgCdTe photodiodes also have a shunt capacitance that is typically less than or equal to 1 pF. Any shunt capacitance will improve the noise performance of the diode, therefore it will be absent from the model to represent the worst case scenario. Figure 1-3 shows a modeled photodiode that outputs a current through a direct injection amplifier which consists of a single PMOS transistor. Output node *int* is connected to the input of VTOF converter which will digitize the intensity of apparent photocurrent.

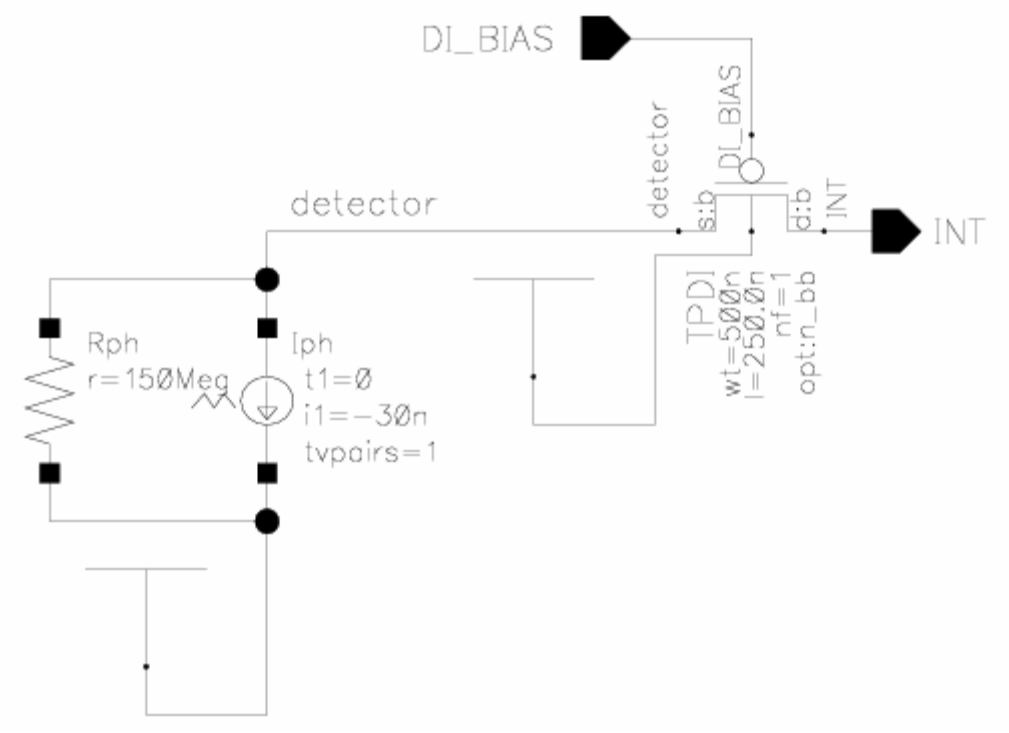

Figure 1-3 Modeled Photodiode and Direct Injection Amplifier

Unlike the transistors in the VTOF circuitry, the DI amplifier PMOS transistor has been sized up to greater than 3 times the minimum width and length. Transistor mismatch is a large problem when using the minimum size devices available for a given submicron process. This PMOS has been sized up to put us outside the peak mismatch zone. Appendix E details the steps taken to determine the 3σ mismatch parameters for a given transistor size.

When this system is implemented with large photodiode arrays, transistor mismatch would result in varying threshold voltages for the DI transistor. This is turn would randomly vary the individual photodiodes bias voltage throughout the array affecting the injection efficiencies. Varying pixel sensitivities across a large array could render the system useless in certain applications.

1.3.2 Conversion Rate

The conversion rate *CR* or output pulse rate is determined by Equation (1-2) where I_{ph} is the photocurrent, I_{dark} is the dark current, and *C* is the integration capacitance. For example, with the threshold voltage equal to 0.4504V, integration capacitance equal to 5 fF, and input photocurrent equal to 30nA, the conversion rate is equal to 13.3214 MHz.

$$CR = \frac{I_{ph} + I_{dark}}{CV_{ith}} \tag{1-2}$$

For any given period, circuitry will count the number of output pulses. The limitation of this period length is set by the saturation of the *N*-bit counter used. The saturation of an *N*-bit system can be defined using the minimum allowable frame rate *mFR* shown in Equation (1-3). Systems reading out the array at a frame rate greater than or equal to the *mFR* will not experience pixel saturation issues.

$$mFR = \frac{CR}{2^N} \tag{1-3}$$

In a 12 bit system with a conversion rate equal to 13.3214 MHz, the *mFR* equals 3.252 kHz. Increasing the integration capacitance (increasing circuit area) will decrease the system's *mFR* but will also decrease other performance characteristics of the system to be discussed later.

Looking at the case where photocurrent is at a minimum, it is possible that a count will never be triggered during a short frame period. Counteracting this case is the dark current seen in active arrays. Even with no input photocurrent, the dark current alone will eventually result in an output pulse.

1.4 Relation of time domain output to system noise

The VTOF maps a DC current input to a corresponding output pulse frequency. In an ideal system, the pulse period would remain constant for a constant current input. The introduction of noise into the system correlates to variations in the individual pulse periods. Given an extended output pulse stream we can plot the pulse to pulse period lengths. The histogram of this data will directly give us the mean (Equation (1-4)) and standard deviation (Equation (1-5)) of the period lengths *P*.

$$\overline{P} = \frac{1}{N}\sum_{i=1}^{N} P_i \qquad \textbf{(1-4)}$$

$$\sigma_{sim} = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(P_i - \overline{P})^2} \qquad \textbf{(1-5)}$$

The standard deviation of the period lengths directly corresponds to the simulated RMS noise of the VTOF. Using this technique, the simulation results can be easily compared to the theoretical calculations.

1.5 Motivation and Goals

The next generation IR imaging applications will demand a wide area of coverage, high spatial resolution, and high SNR. A new design approach is needed to meet the demand of these large high speed imagers. Conventional technologies often can not simultaneously meet all the desired requirements for a specific application. Design tradeoffs must be made in order to satisfy only the most crucial requirements.

The following section will detail the operation of analog Focal Plane Arrays (FPA) and the reasons why current ROICs are failing to meet the new demands of coverage, spatial resolution, and dynamic range. Specific to each problem presented, the advantages of moving to an all digital architecture are explained.

Conventional analog Focal Plane Arrays (FPA) integrate photocurrent which is the result of photons absorbed in the active regions of a photodiode detector. This photocurrent charges a large capacitor connected underneath each pixel. During readout this analog voltage is shifted vertically or horizontally to an analog X-to-1 multiplexer at the edge of the array. The voltage which corresponds to the light intensity incident on any given pixel is then amplified by an output amplifier and communicated to an analog-to-digital converter (A/D), located off-chip, for quantization. The analog signal must be appropriately conditioned prior to sampling and quantization to minimize noise and maximize system performance. This conditioning includes filtering, level shifting, and gain stages.

Throughout this repetitive output process, noise has the opportunity to affect the quality of the signal at multiple points. On chip the analog multiplexer and output driver can both introduce noise to the traveling signal. Off chip, the signal conditioning circuitry and sampling circuitry of the A/D can both add noise reducing the overall SNR. Typically, analog output taps are limited to less than approximately 5-10 million pixels per second readout rate for 12–14 bit dynamic range applications. Figure 1-4 diagrams the noise entry points. Once the signal has been digitized, it is no longer affected by noise sources.

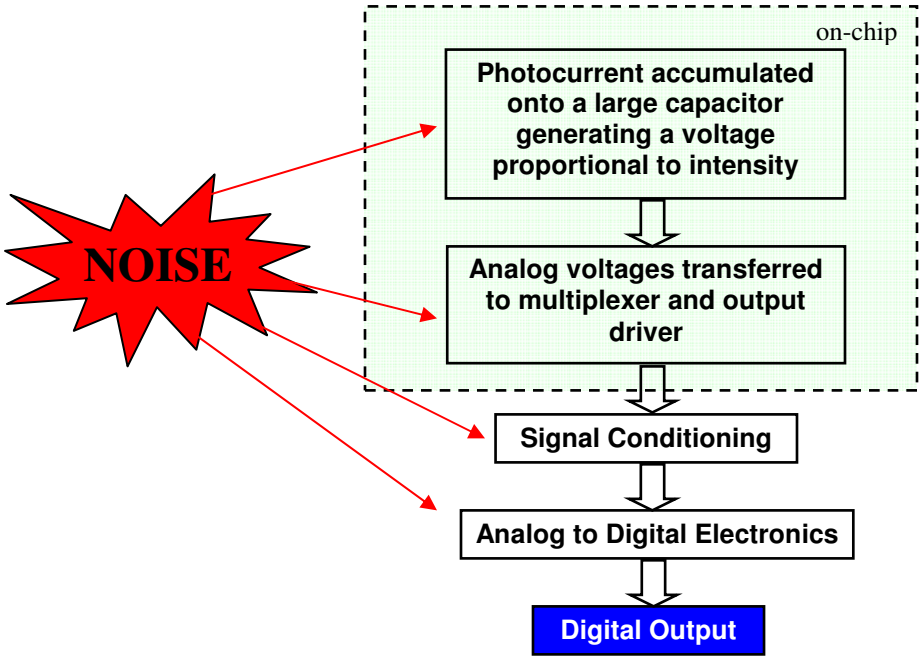

Figure 1-4 Conventional FPA

The simplest way to eliminate these additive noise points is to quantize the intensity of the photocurrent at the earliest possible point. This is of course immediately below the active photodiode detector. As seen in Figure 1-5, using a VTOF reduces the design to one noise entry point. Shifting the digital count value now provides full immunity to all other exterior noise sources given the noise is not powerful enough to flip a digital bit.

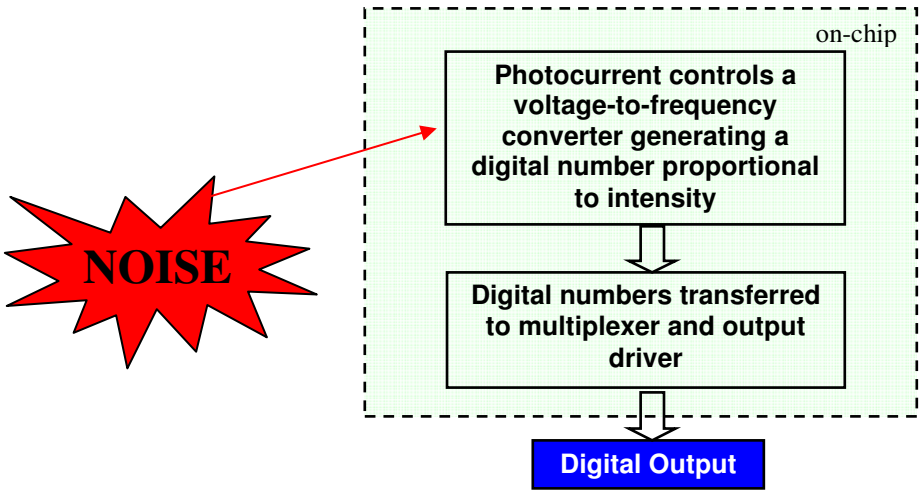

Figure 1-5 FPA using Voltage-To-Frequency Converter

Current FPA technologies use pixel pitches approaching 15 μm and below leaving only 15^2 μm of design space to accommodate the A/D and digital counter technologies. The proposed VTOF is only a 9 transistor design allowing it to be fit into a fraction of this available space using a 90nm process leaving ample area for the remaining digital processing electronics including counting and shifting digital circuitry. Advancing foundry technology's decreasing feature sizes render design area concerns insignificant leaving only the question of performance.

1.5.1 Limitations of Conventional Technologies

The capacitor size you can fit below a pixel defines your well depth or the most significant bit (MSB) of your system. Capacitors consume large amounts of silicon area in comparison to single transistor devices. Using the *mFR* of 3.252 KHz calculated in Section 1.3.2, the needed integration capacitance C_{int} size can be determined using Equation (1-6) where V_{sat} is the peak to peak saturation voltage of the A/D converter. For a typical V_{sat} of 5 volts and photocurrent of 30 nA, a C_{int} of 1.845 pF is needed to avoid saturation during each integration period.

$$C_{\text{int}} = \frac{I_{ph} \times mFR^{-1}}{V_{sat}} \qquad \textbf{(1-6)}$$

The amount of silicon area needed to implement this size capacitor will now be determined. For a simple MOSFET gate capacitor, the gate oxide capacitance per unit area C_{ox} is calculated using Equation (1-7) where ε_{ox} is the permittivity of the gate oxide and t_{ox} is the thickness of the oxide.[ii] Using the given CMOS9SF values, the calculated C_{ox} can be used to determine the area of the capacitor A_{Cint} by Equation (1-8).[ii] For a required C_{int} of 1.845 pF, an A_{Cint} of approximately 128 um^2 is required. In a 15 by 15 μm pixel this accounts for almost 57% of the area below each pixel leaving only 97 square microns for the remaining circuitry, which includes reset logic and analog multiplexers.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times \varepsilon_0}{2.38 \times 10^{-7}} = 1.4509 \times 10^{-6} \quad F/cm^2 \qquad \textbf{(1-7)}$$

$$A_{C\text{int}} = WL = \frac{C_{\text{int}}}{C_{ox}} \times \frac{1 \times 10^8 \quad um^2}{1 \quad cm^2} \quad [um^2] \qquad \textbf{(1-8)}$$

The industry's constantly reducing pixel pitch fundamentally limits the capacitor size that will fit, thus limiting your spatial resolution. Maintaining the needed dynamic range with a larger capacitor prohibits the use of smaller pixels. The signal level at each pixel scales directly with the detector optical area. During this size reduction, the area needed for the control circuitry of the pixel remains constant. Therefore, the ratio of that total available area left for the capacitor decreases and eventually becomes too small for applicable use. Smaller feature sizes are not an option because these large capacitors

need the allowable higher voltages of older process technologies. The 3.3 and 5 volt capacitors are needed to maintain the dynamic range needed for the imager. With digital pixel technology, capacitor size is no longer a limiting factor and the maximum spatial resolution can now be defined solely by the optical system.

The VTOF uses a small capacitance and a digital well that counts how many times this capacitor has been filled as shown in Figure 1-6. Therefore, our MSB is now only limited by the size of our digital well counter and the Least Significant Bit (LSB) is defined by the size of our tiny integration capacitance. The LSB of analog FPAs are defined by its sampling electronics.

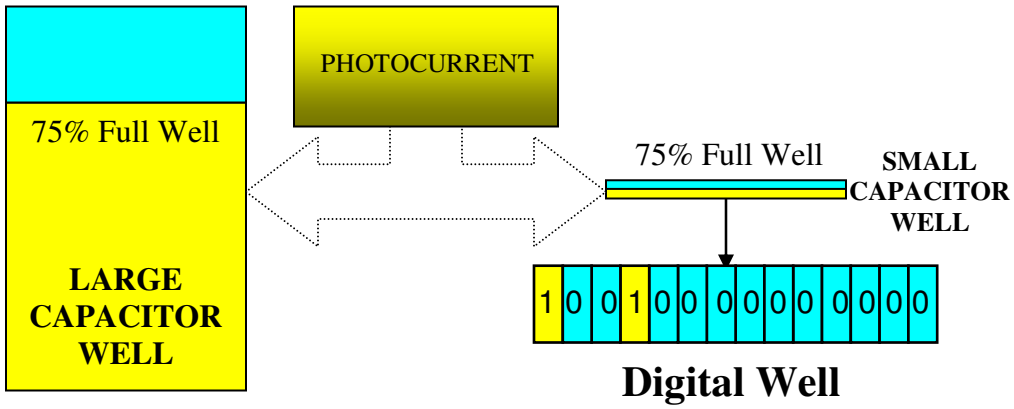

Figure 1-6 Integration Capacitor Comparison

In conventional technologies, readouts must be done quickly to avoid saturation of the integration capacitor. Reading out quickly means numerous output taps reading pixels at 5–10 MHz. Noise limits the speed at which data can be transmitted on a single output in order to maintain a required SNR. When building large arrays you need to compromise with an increasing number of output taps, or a reduction in the dynamic range of the system. If dynamic range is maintained, an unusually high number of output

taps must be actively used increasing design cost, complexity, and overall power consumption.

Digital output rates in the gigabits per second range can be easily maintained allowing digital imagers to operate at frame rates higher than conventional technology allows. Without a well depth limitation and the ability to accommodate large arrays with high frame rates using high speed digital output technology, large power conservative arrays can be constructed and effectively used.

This use of high speed digital outputs greatly improves the data collection capability. Increased pixel output rates increases the field of view for a constant frame rate and spatial resolution. Figure 1-7 shows an image captured with a one megapixel array. Using one digital output running at 10Gbps with 12 bit converters beneath each pixel, a frame rate of 833 Hz can be sustained. If analog technology was used with one output tap operating at a sample rate of 10 millions pixels per second, maintaining a frame rate of 833Hz would only allow a 12,000 pixel area to be read out. In Figure 1-7, the comparative field of view for digital technology is shown in blue while the analog is in red. The improvement obtained using digital technology is clear.

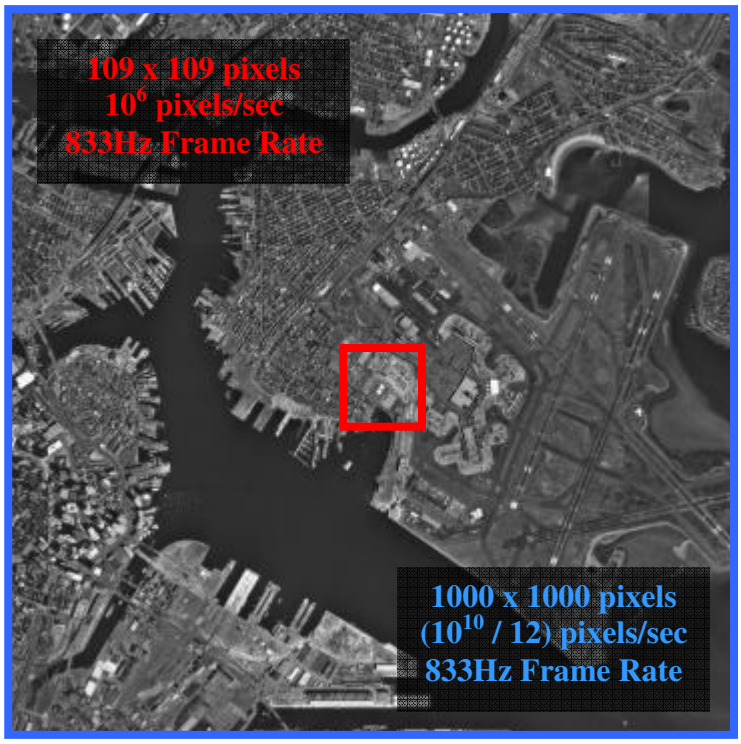

Figure 1-7 Field of View Improvement

It has been shown that moving to an all digital architecture will eliminate the design tradeoffs seen with analog ROICs. Dynamic range can be easily increased with the addition of a digital counting bit. Large integration capacitors no longer limit the ability to use the tightest pixel pitches available. Extremely high readout rates can be maintained allowing for fast full frame operation of large imagers. If matched noise performance can be obtained, scalable digital imagers meeting all design requirements can be easily constructed given the available advantages.

2 Analysis of Noise in Voltage to Frequency Converters

The noise analysis has been subdivided into two categories, first and second order noise sources. First order noise sources are devices internal to the VTOF circuitry generating noise affecting the output. Second order noise sources are devices external to the VTOF that also directly affect the performance of the A/D conversion.

2.1 First Order Noise Sources

We will first explore the quantitative calculations of shot, kTC, mosfet, 1/f, jitter, and quantization noise. These are the fundamental noise sources of the system. Each noise source will be computed individually to be later combined in root sum square (RSS) fashion to obtain full system noise numbers.

2.1.1 Photodiode Shot Noise

Although different types of current sources may be used to drive this system, this design is geared towards operation with an IR focal plane array. The use of any current source introduces shot noise; in this case a photodiode is modeled. The goal of any image sampling system using photodiodes is to be background limited in performance or BLIP. This means the performance of the system is limited by the shot noise of the photocurrent which is the combination of the current generated from the signal and the background. BLIP does not include dark current. A system's performance can not be increased when the shot noise from the photocurrent is the dominant noise source of the system.

Other noise sources within the detector include 1/f and Johnson noise.[iii] LWIR detectors are cryogenically cooled making Johnson noise negligible in this case. In a cooled and correctly biased detector, shot nose will dominate the other noise sources.

Hence, the analysis will only focus on the detector's shot noise. A conversion system designed with a noise level lower than this input noise results in the maximum noise performance possible.

Over each integration period t_{int} calculated in Equation (2-1), the capacitor will see the shot noise generated by the photodiode. This noise along with the photocurrent is integrated on C_{int}.

$$t_{\text{int}} = dt = \frac{C_{\text{int}} dV}{I_{DC}} = \frac{C_{\text{int}} V_{ith}}{I_{DC}} \tag{2-1}$$

Photocurrent can be represented in terms of signal electrons $SIGNAL_e$. The number of signal electrons per integration period can be calculated using Equation (1-2). Integrated white noise is classified as a random walk, and the equivalent noise electrons represented in Equation (1-3) are equal to the square root of the system's signal electrons.

$$SIGNAL_e = \frac{C_{\text{int}} V_{ith}}{q_e} \tag{2-2}$$

$$NOISE_e = \sqrt{SIGNAL_e} \tag{2-3}$$

The noise voltage at the integration capacitor due to shot noise is shown in Equation (2-4) where I_{DC} equals the DC photocurrent, q_e equals the electron charge, and C_{int} equals integration capacitance. Using the process mobility ratio of approximately 2.0875 (Appendix A), the first inverter is minimally sized accordingly to this ratio which gives a first stage input capacitance of 5 fF (Appendix C). To keep the physical size and LSB size of the circuit at a minimum, this input capacitance is used as the integration capacitance C.

$$\sigma_{shot} = \frac{\sqrt{t_{\text{int}} I_{DC} q_e}}{C_{\text{int}}} \qquad \textbf{(2-4)}$$

Figure 2-1 shows the signal-to-noise Ratio (SNR) in dB and the effective number of bits (ENOB) for any given input photocurrent amplitude. ENOB is discussed in more detail later in Section 2.3.2. The units on the x-axis represent decibels relative to the full scale input which is 2^{12} counts or 4,096. At full scale input, the ENOB equals 11.1 bits.

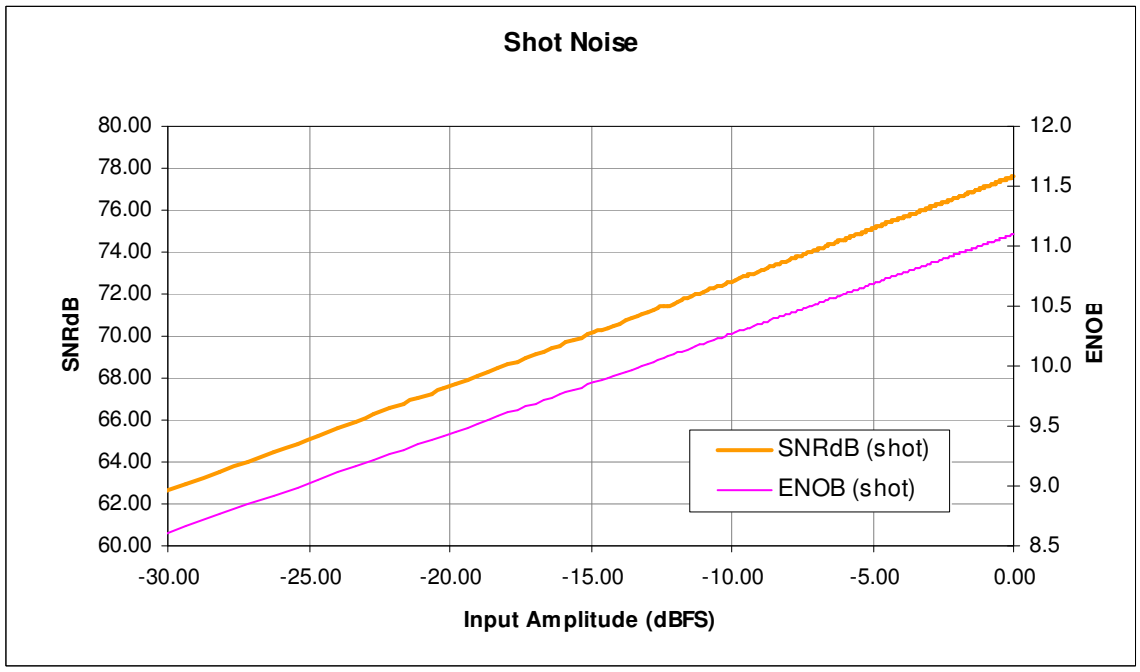

Figure 2-1 Photodiode Shot Noise

Figure 2-1 considers an ideal VTOF with only shot noise at its input. Equation (2-4) shows the total electronic noise for one count (one integration period). Treating each individual integration period as a separate sample we can calculate the total electronic noise in *N* counts by multiplying the total electronic noise in one count by the square root of *N*. The noise is assumed to be randomly distributed Gaussian noise with zero mean and *N* is large under normal operation. The total signal is equal to *N* times the signal level for one count which is equal to V_{ith}. Equation (2-5) gives us the SNR ratio

which defines the plotted data in Figure 2-1. The number of counts translates to decibels relative to the full scale using Equation (2-6).

$$SNR_{shot} = \frac{N(V_{ith})}{\sqrt{N(\sigma^2_{shot})}} \quad \textbf{(2-5)}$$

$$dbFS = 20\log 10\left(\frac{N}{2^{12}}\right) \quad \textbf{(2-6)}$$

2.1.2 Integration Capacitance kTC Noise

kTC Noise is the varying charge stored on the capacitance at the instance the reset NMOS is disabled.[iii] Varying initial voltages result in different individual integration periods using a constant DC input current. The resulting noise at the end of each integration period can be written as the following equation where *k* equals Boltzmann's constant and *T* is the operating temperature.

$$\sigma_{kTC} = \sqrt{\frac{kT}{C_{\text{int}}}} \quad \textbf{(2-7)}$$

The fact that the majority of IR focal plane arrays are run at cryogenic temperatures helps decrease the effect that kTC will have on the overall system. Using 218 degrees Kelvin as our temperature reference, the full scale ENOB equals 13.4 bits as shown in Figure 2-2. Again this is assuming all other components ideal and kTC noise being the only circuit disturbing quantity.

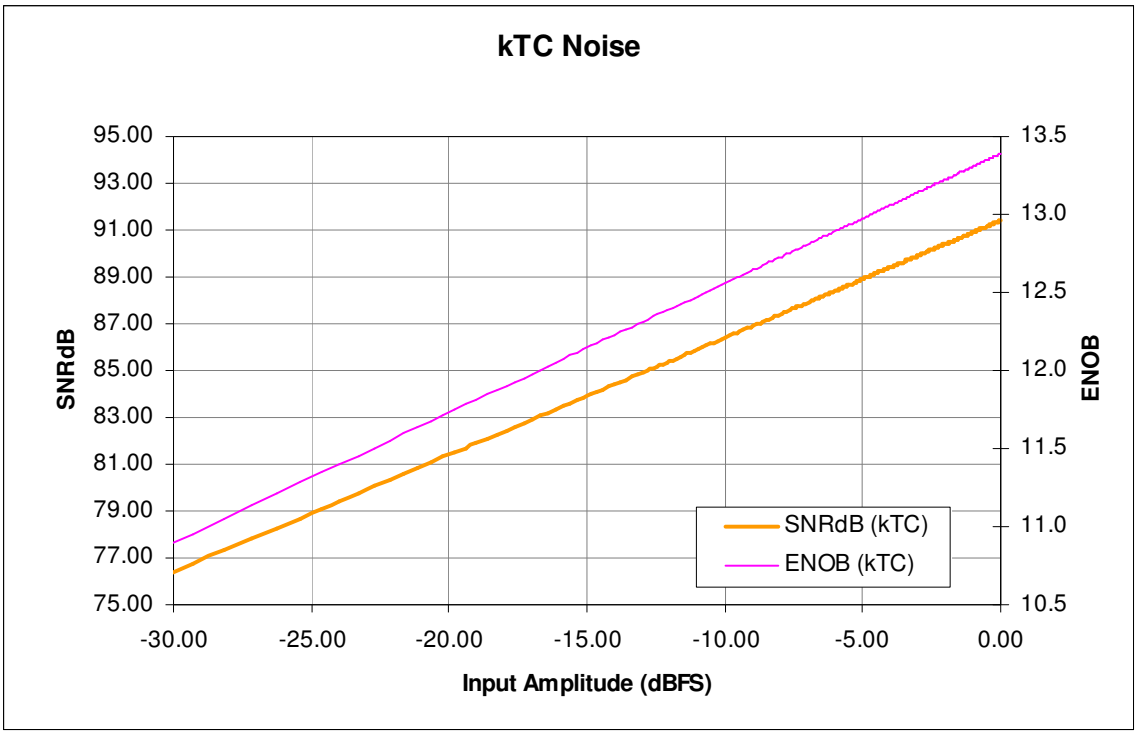

Figure 2-2 kTC Noise

$$SNR_{kTC} = \frac{N(V_{th})}{\sqrt{N(\sigma_{kTC}^2)}} \tag{2-8}$$

2.1.3 MOSFET Noise

The MOSFET channel thermal noise is defined in Equation (2-9).

$$e_{n-mosfet} = \sqrt{\frac{8}{3}\frac{kT}{g_m}} \tag{2-9}$$

In the subthreshold region, transconductance g_m is given by the Equation (2-10) where n equals the sub-threshold slope parameter.[iii] In the IBM CMOS9SF 90nm process models I found n equal to 1.5204 for the PMOS transistor.

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{I_d q_e}{nkT} \tag{2-10}$$

$$n = \frac{C_{ox} + C_{dep}}{C_{ox}} = 1.5204 \qquad \textbf{(2-11)}$$

The subthreshold slope factor n shown in Equation (2-11) is defined as 1 plus the ratio of the depletion capacitance per unit area (C_{dep}) over the oxide capacitance per unit area (C_{ox}).[ii] The inversion layer capacitance (C_{inv}) is much lower than C_{ox} + C_{dep} in the subthreshold region and does not factor into the slope equation.[iv] C_{ox} and C_{dep} are defined in Equations (2-12) and (2-13).

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times \varepsilon_0}{2.38 \times 10^{-7}} = 1.4509 \times 10^{-6} \quad F/cm^2 \qquad \textbf{(2-12)}$$

$$C_{dep} = \frac{\varepsilon_{si}}{w_{dep}} = \sqrt{\frac{(11.8 \times \varepsilon_0) q_e N_{dep}}{2\phi_s}} = 2.788 \times 10^{-6} \quad F/cm^2 \qquad \textbf{(2-13)}$$

The doping concentration of the depletion region N_{dep} is 6.79e17 cm^{-3}. The carrier concentration of the silicon channel region n_i is 1.08e10 cm^{-3} and the permittivity of silicon is equal to 11.8 times the permittivity in a vacuum ε_o. Using these values, the surface potential φ_s is calculated to be 0.73733 V in Equation (2-14).[ii]

$$\phi_s = 0.4 + \frac{kT}{q_e} \ln\left(\frac{N_{dep}}{n_i}\right) = 0.4 + 0.01878 \ln\left(\frac{6.79 \times 10^{17}}{1.08 \times 10^{10}}\right) = 0.73733 \qquad \textbf{(2-14)}$$

The injection efficiency or ratio of integrated photon current to actual photon current will be assumed ideal. MOSFET noise e_n can be referred to the output as a noise current i_n via the transfer function in Equation (2-15).[iii] After multiplication by the noise

bandwidth, noise current can converted to noise voltage using Equation (2-16). The noise bandwidth for a pulse of duration t_{int} is equivalent to $(2t_{int})^{-1}$.[v]

$$i_{n-mosfet} \approx \frac{e_{n-mosfet}}{R_{ph}} \tag{2-15}$$

$$\sigma_{mosfet} = \frac{e_{n-mosfet}}{R_{ph}} \sqrt{\frac{1}{2t_{\text{int}}}} \frac{t_{\text{int}}}{C} = \frac{e_{n-mosfet}}{R_{ph}C} \sqrt{\frac{t_{\text{int}}}{2}} \tag{2-16}$$

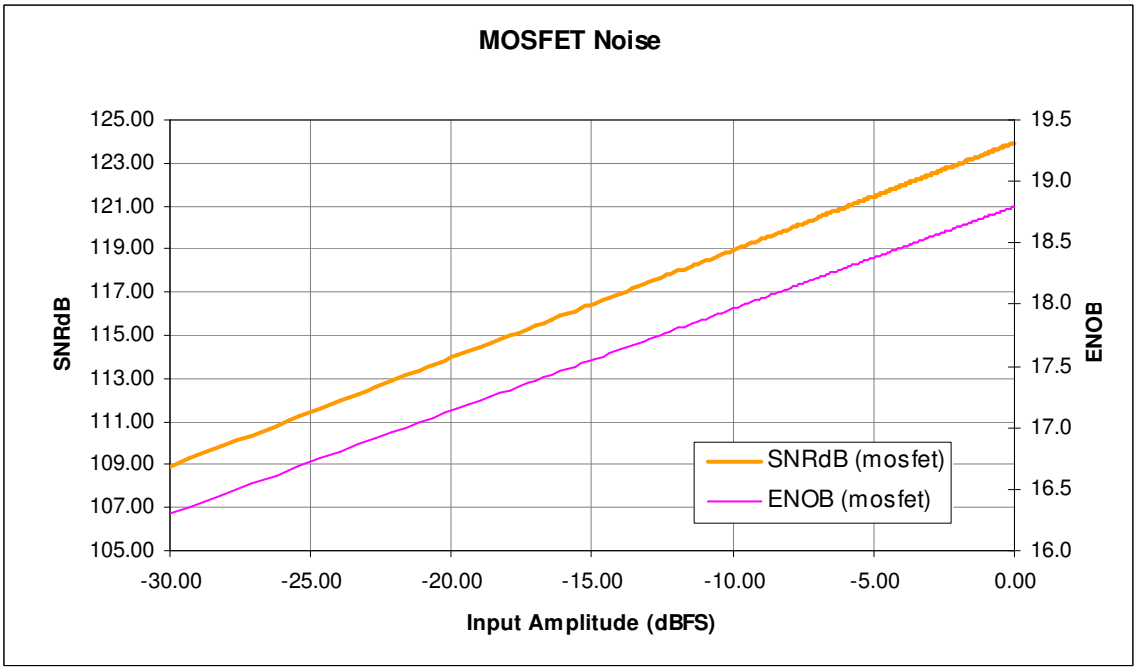

Figure 2-3 MOSFET Noise

$$SNR_{mosfet} = \frac{N(V_{th})}{\sqrt{N(\sigma^2_{mosfet})}} \tag{2-17}$$

2.1.4 1/F Noise

The primary cause of 1/f or flicker noise is the movement of the inversion layer carriers in and out of the oxide traps causing variations in the current output.[iv] This noise

will dominate the MOSFET until the switching frequency has reached the tens of kilohertz range. 1/f noise is also a significant noise in LWIR detectors but it is neglected here because we are focusing only on the dominant shot noise of the source. Equation (2-18) shows a basic SPICE 1/f noise model which will be used to calculate the 1/f current noise density.[vi]

$$i_{n-1/f}(f) = \sqrt{\frac{KF \cdot I_{DC}^{AF}}{f^{EF} C_{ox} W L_{eff}}} \qquad \textbf{(2-18)}$$

Using the 1/f noise parameters given for the CMOS9SF process outlined in Figure 2-4, the rms noise can be calculated from Equation (2-19). L_{eff} is the effective length of the transistor and is equal to 233 nm for a 500 nm by 250 nm drawn transistor.

KF	Flicker Noise Coefficient	1.10E-21
EF	Flicker Noise Frequency Exponent	1.062
AF	Flicker Noise Exponent	2

Figure 2-4 Flicker Noise Parameters

$$\sigma_{1/f} = i_{n-1/f} \sqrt{\frac{1}{2t_{\text{int}}}} \frac{t_{\text{int}}}{C} = 154.165 \quad uV \qquad \textbf{(2-19)}$$

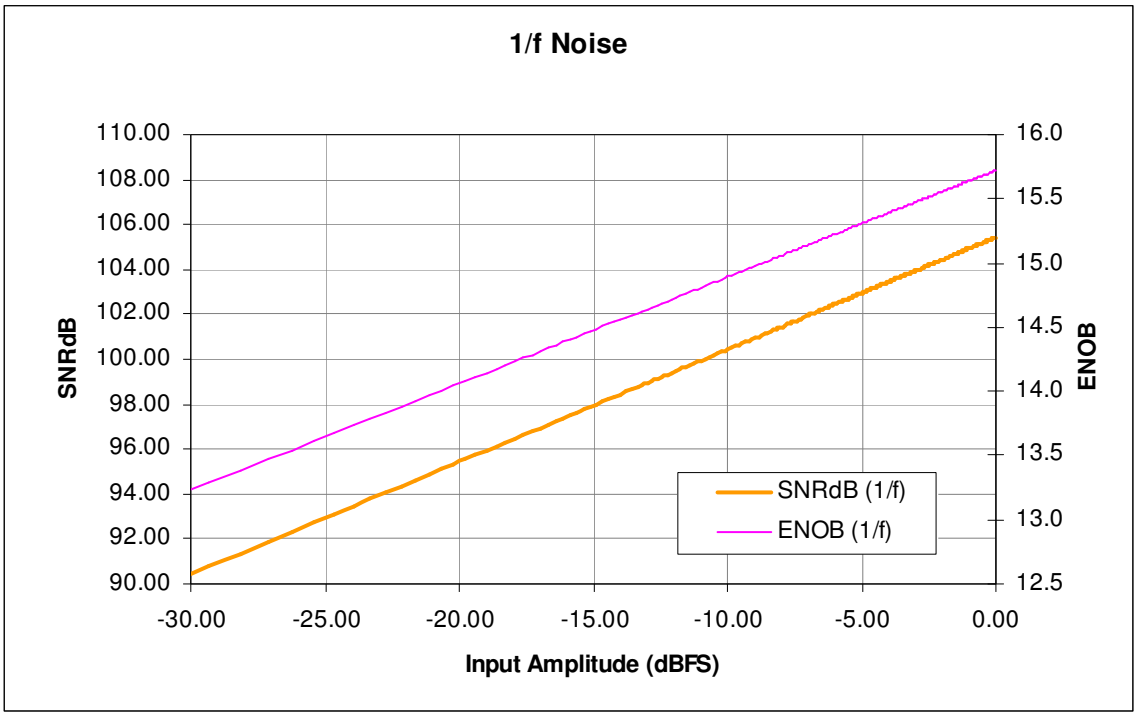

Figure 2-5 1/f Noise

$$SNR_{1/f} = \frac{N(V_{th})}{\sqrt{N(\sigma_{1/f}^2)}} \tag{2-20}$$

2.1.5 Jitter Noise

Timing jitter is proportional to the measurement interval ΔT.[vii] This is due to the cumulative property of phase noise.

$$\sigma_{\Delta T} = \kappa\sqrt{\Delta T} \quad \text{[vii]} \tag{2-21}$$

In this case the chain of inverters, which would classify as a single-ended CMOS ring oscillator if the output was fed back into the input, is not continuously running. Therefore, our measurement interval in this case is only the time it takes for the pulse to travel through the four inverters. Using a simple capacitive charge model, the propagation delay t_d of each stage is defined by Equation (2-22) where C_g is the combined gate capacitance.

$$t_d = \frac{C_g V_{th}}{I_{sat}} \tag{2-22}$$

The drain current in saturation (I_{sat}) will be defined using the simple square law model shown in Equation (2-23).[ii]

$$I_{sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{thn})^2 \tag{2-23}$$

As discussed previously the middle two inverters have gate lengths that are 4 times that of the surrounding outside inverters. Therefore, the saturation current will be 4 times less in these inverters, resulting in a propagation delay that is 4 times as long. Using this relationship the t_d of the first inverter can be multiplied by 10 to get the full propagation period through the 4 inverters, which in this case is also our measurement interval, ΔT.

$$\Delta T = 10 t_d \tag{2-24}$$

The last step to calculating jitter noise is to define κ which is a figure-of-merit used to describe the quality of the oscillator. For single ended CMOS ring oscillators, κ is defined by Equation (2-25).[viii]

$$\kappa = \sqrt{\frac{8}{3}kT}\sqrt{\frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{thn})^3}} \tag{2-25}$$

During a reset period, a pulse propagates twice through the chain of inverters. Once when the threshold is reached to activate the discharge of the integration capacitance, and a second time to release the discharge NMOS and begin a new integration period. The total jitter noise encountered in each integration period is defined by Equation (2-26).

$$\sigma_{jitter} = \sqrt{2}\sigma_{\Delta T} \quad \textbf{(2-26)}$$

Using the variables given in Figure 2-6, the calculated transient jitter noise is equal to 45.6 fS.

C_g	5.00E-16
t_d	1.3969E-12
ΔT	1.3969E-11
μ_n	0.02035
C_{ox}	0.020229234
W	1.40E-07
L	8.00E-08
V_{thn}	0.331
I_{sat}	0.000161215
κ	8.63E-09
$\sigma_{\Delta T}$	3.22E-14
σ_{jitter}	4.55971E-14

Figure 2-6 Jitter Noise Variables

For a constant 30nA input current giving us an integration period of 75 nS, the resulting SNR ratio is equal to 160.5 dB at full scale. This SNR as shown in Figure 2-7 is substantially largely than that of the system with input shot noise. Clearly jitter noise will have little to no effect on the system's total noise with all the individual noise contributions. It is safe to say jitter noise is negligible in this system.

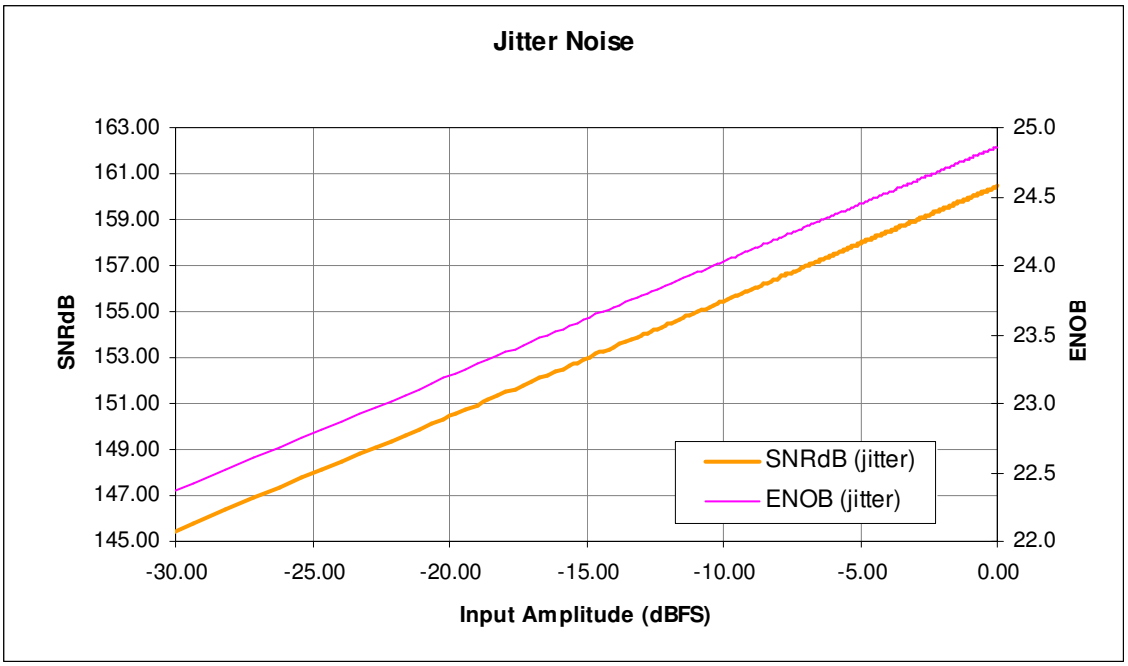

Figure 2-7 Jitter Noise

$$SNR_{jitter} = \frac{N(V_{th})}{\sqrt{N(\sigma^2_{jitter})}} \tag{2-27}$$

2.1.6 Quantization Noise

The voltage to frequency converter, similarly to any other A/D, introduces a noise error at the end of an integration period due to left over charge on the integration capacitance. This magnitude of this quantization noise is between zero and one half of a LSB. When input signal amplitudes are higher than a single LSB, the system's quantization noise is uniform and uncorrelated. The RMS value of this noise is given by Equation (2-28).

$$\sigma_{quant} = \frac{V_{ith}}{\sqrt{12}} \tag{2-28}$$

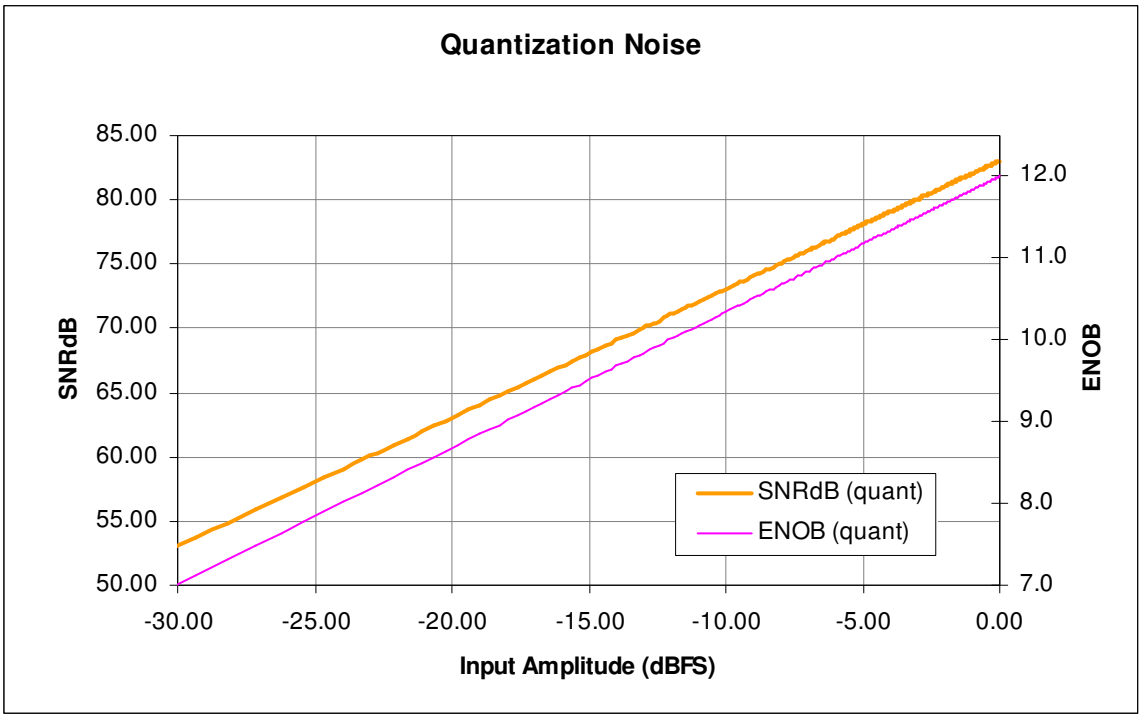

Figure 2-8 Quantization Noise

$$SNR_{quant} = \frac{N(V_{th})}{\sigma_{quant}} \tag{2-29}$$

2.2 Second Order Noise Sources

This section will explore the quantitative calculations of power supply noise, and direct injection bias noise. Other noise sources may apply, but are beyond the scope of this paper. For example, ground bounce could become an issue if the power supply and ground networks are not properly designed. The use of multiple thick traces will help ensure low resistance paths for current returns. Another issue could arise with electromagnetic interference (EMI) from fast switching devices in close proximity. This effect is highly dependent on the layout and guard structures implemented in the design

2.2.1 Power Supply Noise (Inverter Threshold Noise)

In the case of kTC noise, varying initial voltages results in different individual integration periods. Power supply noise now varies the end of integration switching point for individual integration periods. The combination of these noise models now allows us to predict the variance at both endpoints of our integration periods.

In a perfectly matched static inverter the threshold or switching point is ideally defined as half of the power supply voltage. The nominal operating voltage of CMOS9SF is 1V, therefore making our ideal inverter threshold equal to 500 mV with matched transistors (Appendix B). Noise at the power supply can be referenced to the input of the first inverter. In the worst case scenario, the inverter threshold noise will be equal to half of the power supply noise.

$$\sigma_{ITN} = \frac{\sigma_{PSN}}{2} \qquad \textbf{(2-30)}$$

The designer can now put a hard limit on the allowable power supply noise in the system. Constructing supplies with noise levels safely below the dominant shot noise will ensure maximum system performance. Typical high current Linear Dropout Regulators (LDO) have output noise voltages equal to Vout multiplied by 25 μVrms. These commercial off the shelf (COTS) LDOs are available today that more than fit the noise requirements of our system. The nominal CMOS9SF VDD of 1 volt results in a 25 uVrms noise voltage. To push the results to a worst case scenario we will use 100 uVrms as the power supply noise figure. Figure 2-9 graphs the corresponding SNR and ENOB for this given power supply noise.

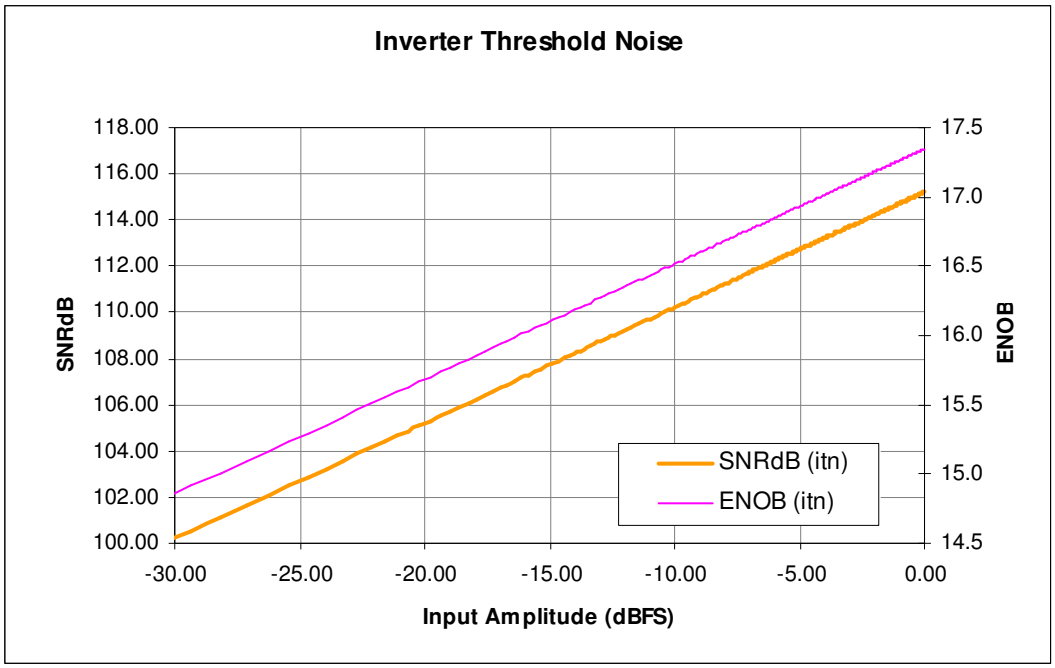

Figure 2-9 Power Supply Noise

$$SNR_{ITN} = \frac{N(V_{th})}{\sqrt{N(\sigma^2_{ITN})}} \tag{2-31}$$

2.2.2 Direct Injection Bias Noise

The DI bias is a voltage that is generated outside of the image array via a regulator on chip or it is supplied from a source off chip. The DI bias noise can be approached in a similar manner to that of the MOSFET noise. The noise voltage at the gate input of the DI transistor can be output referred as a current which is integrated on the capacitance using the transfer function in Equation (2-32).[iii]

$$i_{n-bias} \approx \frac{e_{n-bias}}{R_{ph}} \tag{2-32}$$

For a voltage biasing circuit built with COTS parts, an output noise density of less than 100 nV/√Hz is easily obtainable. To model the worst case scenario, 1 μV/√Hz will

be used as the input noise density at the PMOS. The RMS voltage noise for each integration period is then calculated using Equation (2-33).

$$\sigma_{bias} = i_{n-bias}\sqrt{\frac{1}{2t_{\text{int}}}}\frac{t_{\text{int}}}{C} = \frac{e_{n-bias}}{R_{ph}C}\sqrt{\frac{t_{\text{int}}}{2}} \qquad \textbf{(2-33)}$$

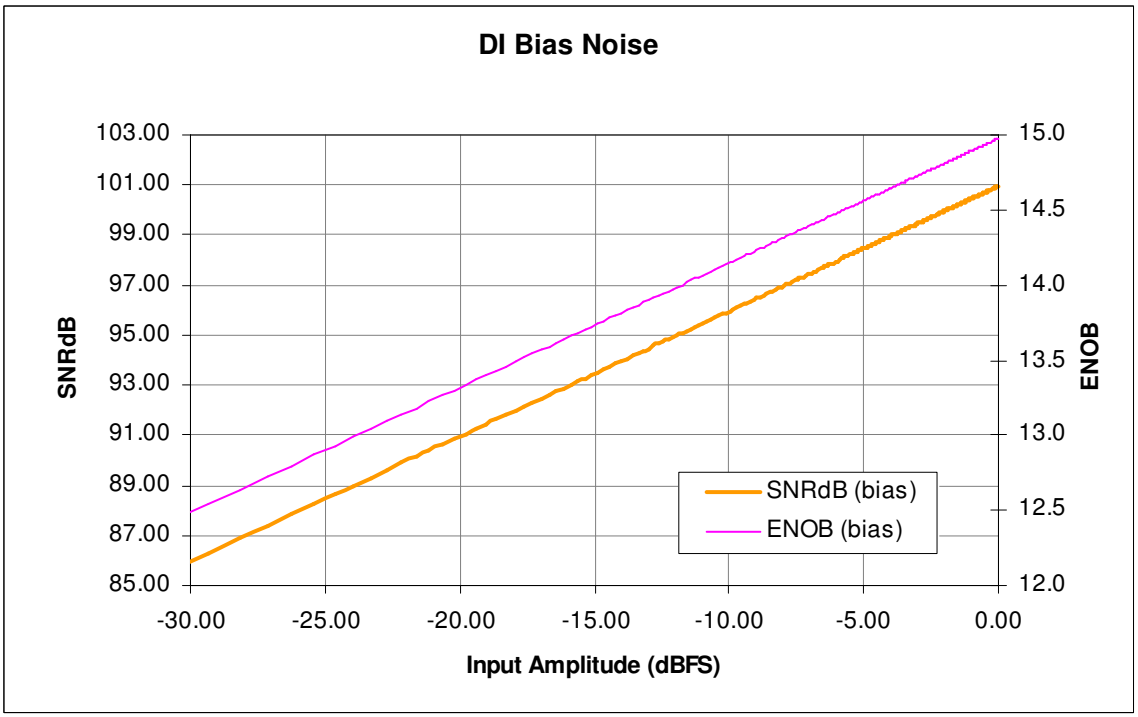

Figure 2-10 DI Bias Noise

$$SNR_{bias} = \frac{N(V_{th})}{\sqrt{N(\sigma_{bias}^2)}} \qquad \textbf{(2-34)}$$

2.3 Total Noise

The total voltage noise seen at the capacitor for each integration period is the RSS of the individual contributions because the sources are uncorrelated.

$$\sigma_{TOTAL} = \sqrt{\sigma_{shot}^2 + \sigma_{kTC}^2 + \sigma_{mosfet}^2 + \sigma_{1/f}^2 + \sigma_{jitter}^2 + \sigma_{psn}^2 + \sigma_{bias}^2} \qquad \textbf{(2-35)}$$

σ_{shot}	0.00379900163
σ_{kTC}	0.00077586525
σ_{mosfet}	0.00001831478
$\sigma_{1/f}$	0.00015416629
σ_{jitter}	0.00000070711
σ_{psn}	0.00005000000
σ_{bias}	0.00025831362

Figure 2-11 Individual Noise Contributions

Equation (2-35) shows the total electronic noise for one count. Treating each individual integration period as a separate sample we can calculate the total electronic noise in *N* counts by multiplying the total electronic noise in one count by the square root of *N* (Equation (2-36)).

$$\sigma_{TOTAL*N} = \sqrt{N(\sigma_{shot}^2 + \sigma_{kTC}^2 + \sigma_{mosfet}^2 + \sigma_{1/f}^2 + \sigma_{jitter}^2 + \sigma_{psn}^2 + \sigma_{bias}^2)} \quad \textbf{(2-36)}$$

Incorporating quantization noise error into the system we end up with a total system noise in Equation (2-37).

$$\sigma_{TOTAL*N+QUANT} = \sqrt{\sigma_{quant}^2 + N(\sigma_{shot}^2 + \sigma_{kTC}^2 + \sigma_{mosfet}^2 + \sigma_{1/f}^2 + \sigma_{jitter}^2 + \sigma_{psn}^2 + \sigma_{bias}^2)} \quad \textbf{(2-37)}$$

2.3.1 Signal to Noise Ratio

The total system noise has been determined allowing the calculation of the signal to noise ratio to quantify the expected performance of the system. Each integration period sees a signal level of V_{th}, therefore *N* integration periods see a signal level of $N(V_{th})$. Comparing this to the noise level in *N* counts gives the SNR shown in Equation (2-38).

$$SNR = \frac{N(V_{ith})}{\sqrt{\sigma_{quant}^2 + N(\sigma_{shot}^2 + \sigma_{kTC}^2 + \sigma_{mosfet}^2 + \sigma_{1/f}^2 + \sigma_{jitter}^2 + \sigma_{itn}^2 + \sigma_{bn}^2)}} \quad \textbf{(2-38)}$$

At full scale input or N equal to 2^{12} counts, this system achieves a SNR ratio of 76.3 dB.

Figure 2-12 compares the individual noise contributions to each other and the system's total noise. It can be seen that the system is predicted to be limited by the shot noise of the input photodiode. At approximately -12.5 dBFS, the shot noise of the system overcomes the quantization noise of the converter.

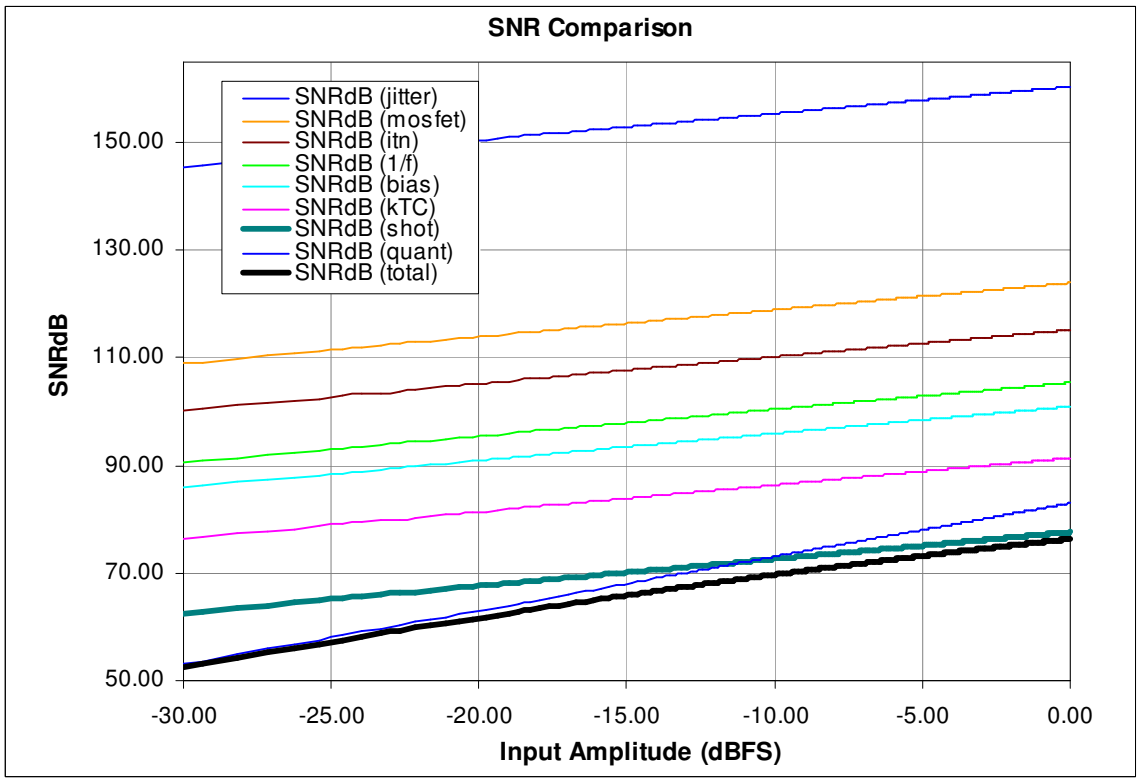

Figure 2-12 SNR Comparison

2.3.2 Effective Number of Bits

It is often easier to think of a system in regards to the effective number of bits (ENOB) it is capable of producing. Once the SNR of the system has been established, ENOB can be easily determined using Equation (2-39).

$$ENOB = \log_2(SNR) - 1.79 \quad \textbf{(2-39)}$$

At full scale input, this system achieves an ENOB of 10.9 bits. Figure 2-13 compares the ENOB for the individual and total noise contributions.

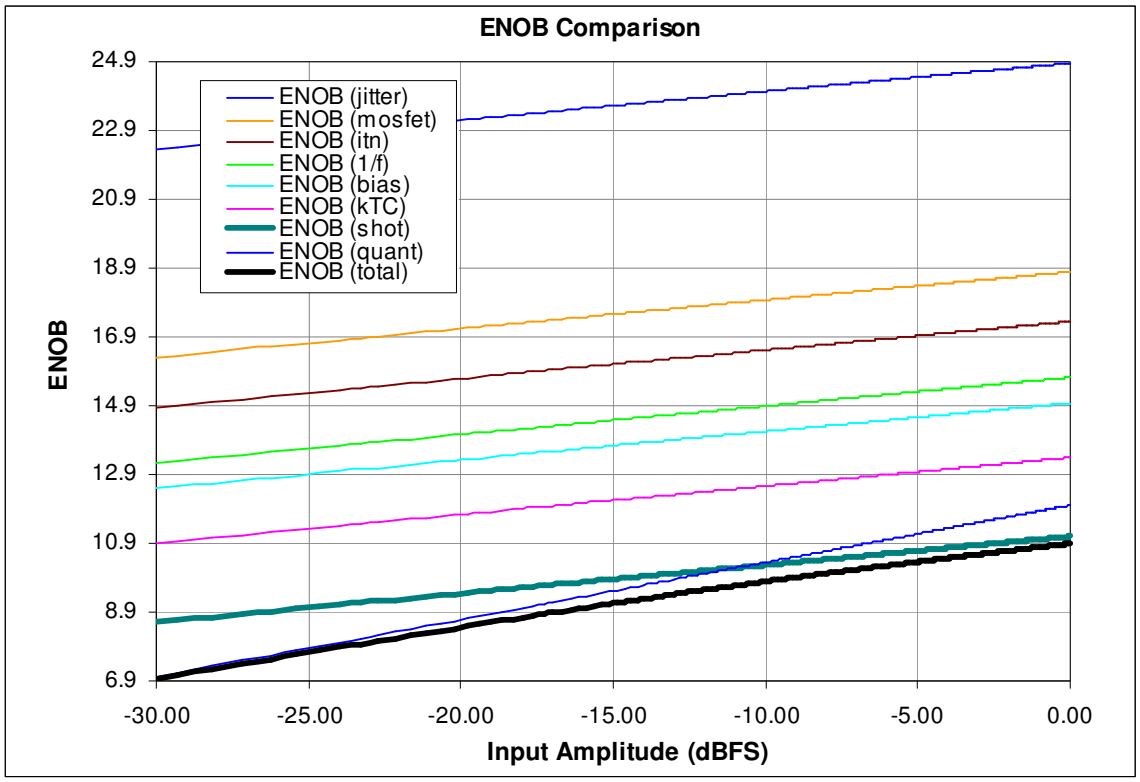

Figure 2-13 ENOB Comparison

3 Transient Noise Simulations

The circuit was first built using Cadence Virtuoso Schematic. The circuit's netlist was then exported and simulated in Synopsys' HSPICE environment due to the availability of more advanced simulation viewers. Mentor Graphics EZWave viewer allows for easy transient calculations of varying pulse periods.

Transient noise sources were simulated using piece-wise linear functions driven via a file input.[ix] This input file was generated using Matlab's normally distributed random number generator function (Appendix D) and exported to a file in SPICE input format.

3.1 First Order Noise Source Simulations

We will first simulate the individual noise contributions of shot, kTC, mosfet, and jitter noise. As a reference, noiseless simulations were also run using ideal voltages and current sources. Figure 3-1 plots the varying output period length for an ideal current input of 30 nA. The transient plot on top shows the voltage on the integration capacitance node and the output of the final inverter in the VTOF controlling the reset of the integration capacitance. The lower plot shows the period lengths of these individual pulses.

The simulated ideal ENOB was over 27+ bits for a full scale 12 bit input. This limit is set by the precision obtainable with the SPICE simulators. For example, a simulation step size set to 10 fS will only result in pulse to pulse variations above 10 fS. This must be considered when performing the following simulation of the individual additive noise sources. If the noise performance is going to be above this ceiling, then the output results will be meaningless. It is safe to say that any noise sources producing results above this ceiling will have little to no affect on the performance of the system.

In order to speed simulation time, the step sizes for individual noise simulations will be set so that the lack of transient resolution doesn't dominate the effects of the noise sources.

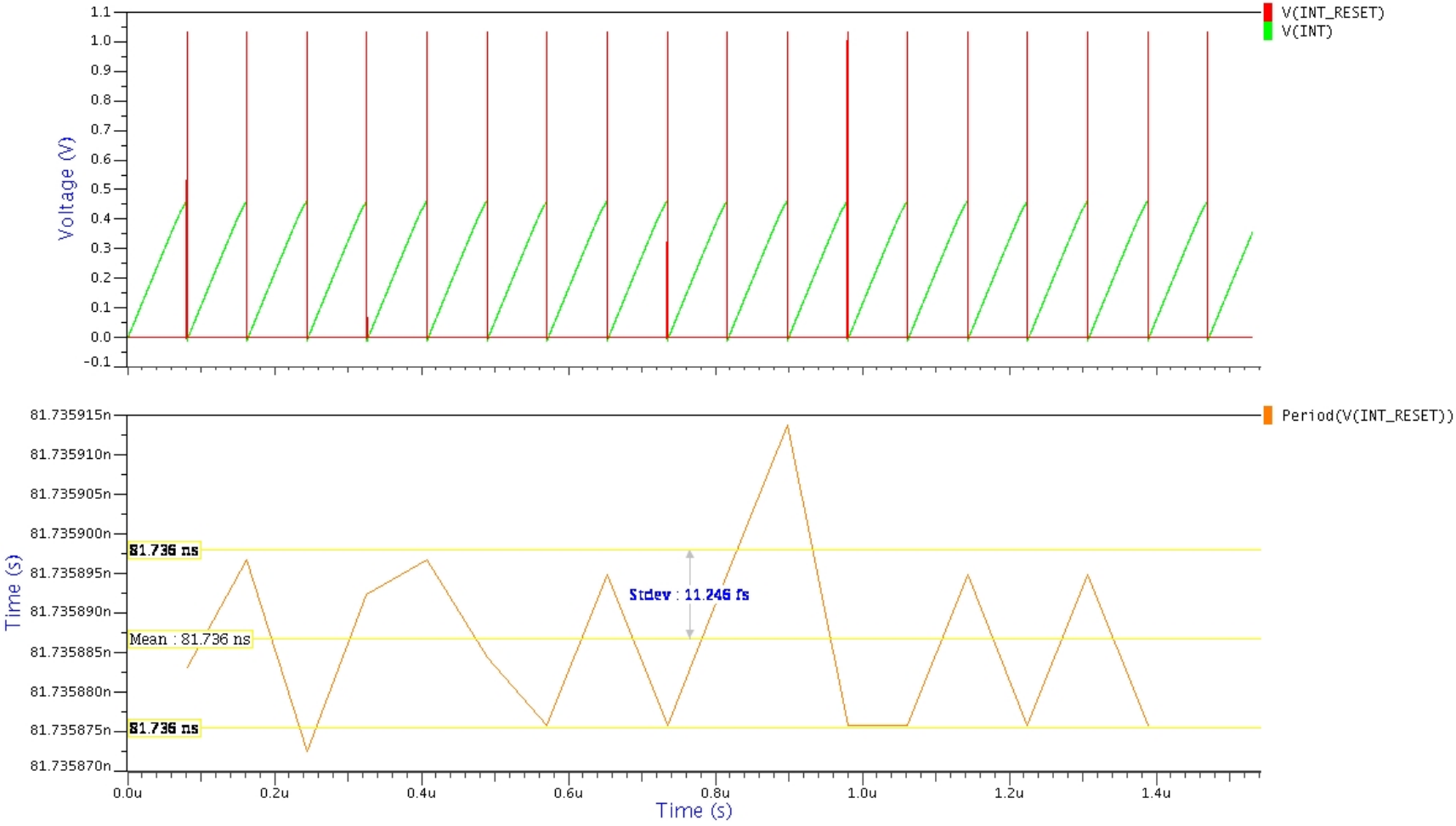

Figure 3-1 Simulated Noiseless VTOF

3.1.1 Shot Noise Simulation

The input shot noise for the transient source was calculated using the following equation where T_s is the pulse width. T_s is chosen so $1/T_s$ is much greater than the highest frequency of interest.

$$i_n = \sqrt{2q_e I_{DC}} \quad \textbf{(3-1)}$$

$$T_s = \frac{t_{\text{int}}}{100} \quad \textbf{3-2)}$$

$$\sigma_{shot} = \frac{i_n}{\sqrt{2T_s}} \quad \text{iv} \quad \textbf{(3-3)}$$

Using an I_{DC} of 30 nA, the input shot noise σ_{shot} was calculated to be 2.5304 nA/√Hz. Referring to Figure 1-3, the I_{ph} constant current source is replaced with a PWL source whose output is generated in MATLAB according to the shot noise calculations in Equation (3-3).

Figure 3-3 plots the pulsed output on top and the individual pulse period lengths on the bottom. The varying period lengths are due to the current source with simulated shot noise at the input. Output noise can now be calculated using the mean and standard deviation of these changing output period lengths.

The standard deviation must first be scaled up by the ratio of the source and drain currents (η) before comparing it to the theoretical calculations. The theoretical calculations assume shot noise and photocurrent are ideally apparent on the integration node. This is not the case when leakage currents in the DI PMOS transistor play a role in decreasing these currents. These leakage currents include gate leakage due to the thin oxide, and body currents due to band-to-band tunneling.[x] Equation (3-4) defines the

inverse ratio of the current integrated to the current input from the detector or the current source in this case.

$$\eta = \left(\frac{I_{\text{int}}}{I_{DC}} \right)^{-1} \tag{3-4}$$

Simulations show that this ratio is equal to approximately 1.1.

Figure 3-2 compares the calculated results from Section 2.1.1 to the simulation results obtained. The simulated ENOB with input shot noise VTOF overlaps what was predicted. Calculated and simulated results show the system is capable of achieving an ENOB of 11.1 with the integration capacitance of 5 fF.

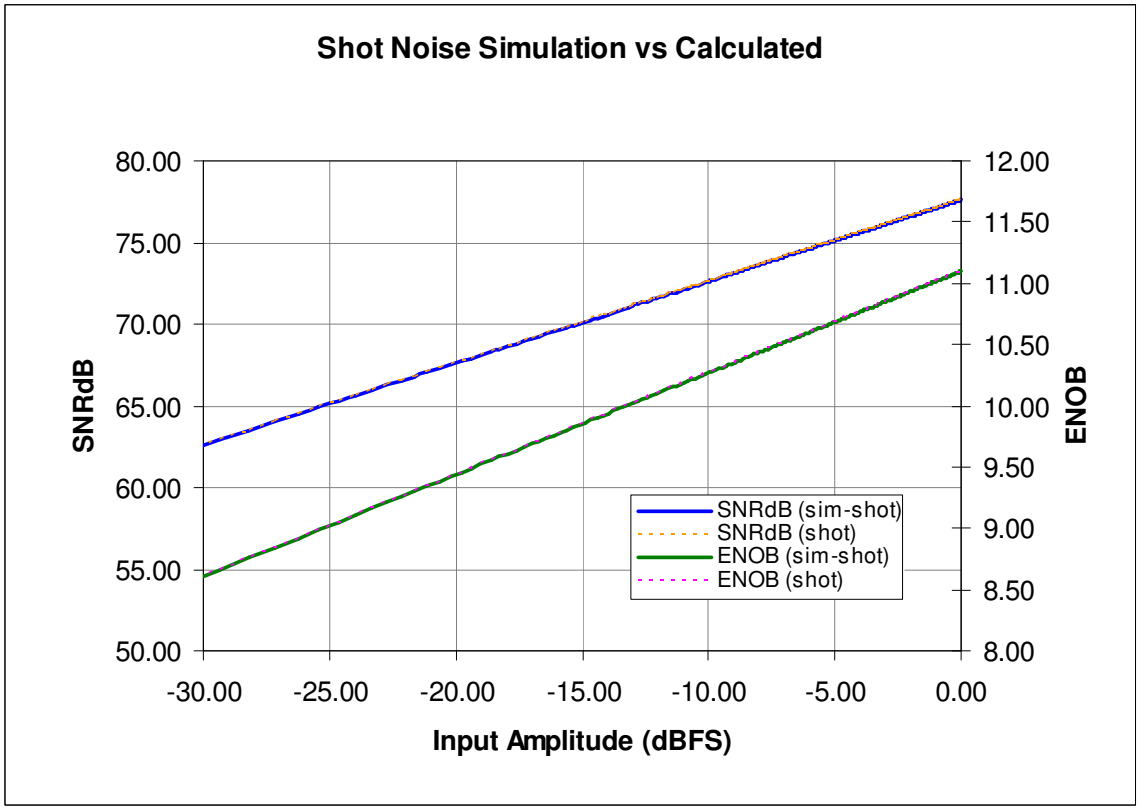

Figure 3-2 Shot Noise Simulated vs Calculated

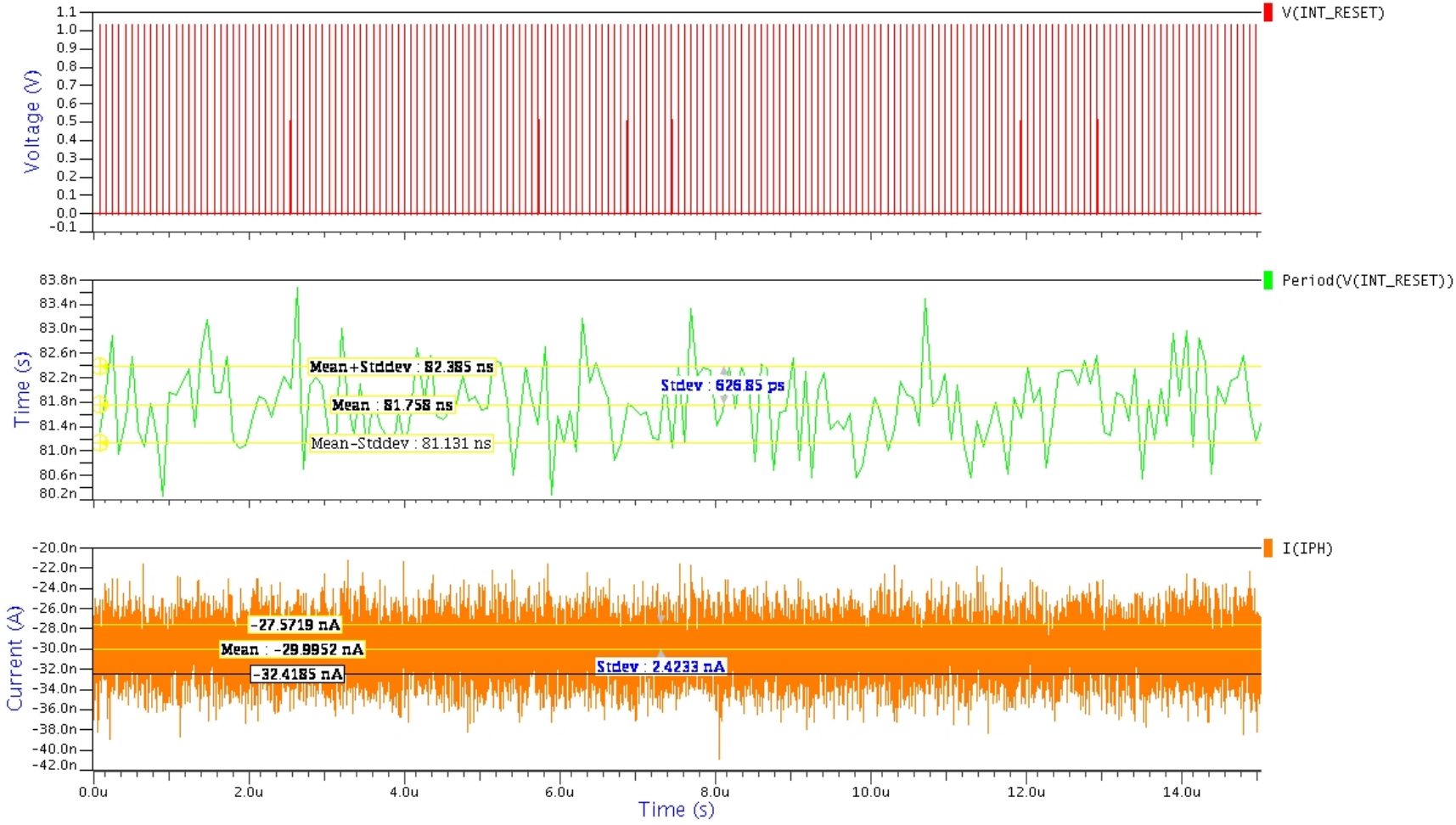

Figure 3-3 Transient Shot Noise Simulation

3.1.2 kTC Noise Simulation

To simulate the effects of the kTC noise, the reset NMOS tying the integration capacitance to ground was disconnected from ground and tied to a transient noise source. Visually referring to Figure 1-1, the source of transistor *TN6* connected to node *kTC* is cut from ground and connected to transient voltage PWL source *V(KTC)*. The noise source was generated in Matlab using the output of Equation (2-7) as the input standard deviation. After this circuit modification, the integration node is pulled to a random voltage opposed to ground with each output pulse.

Each integration period now begins with a varying voltage. The difference between this voltage and V_{th} will result in pulse period variations or noise at the output of the system. The resulting SNR of the simulation is calculated in Equation (3-5) and plotted in Figure 3-4.

$$SNR_{sim-kTC} = \frac{N(\overline{t_{\text{int}-sim-kTC}})}{\sqrt{N(\sigma^2_{t\,\text{int}-sim-kTC})}} \qquad \textbf{(3-5)}$$

Figure 3-5 plots the varying voltage at *V(KTC)* which is varying the reset integration reset voltage. The varying period length and calculated standard deviation are also shown for the kTC noise simulation.

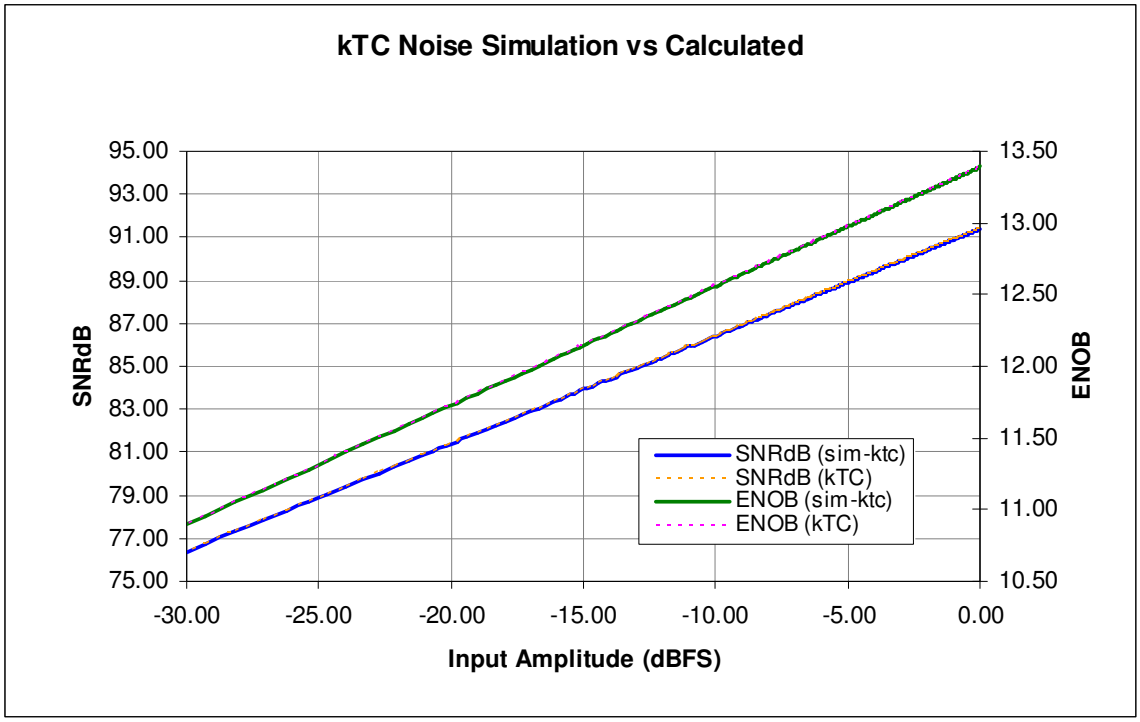

Figure 3-4 kTC Noise Simulated vs Calculated

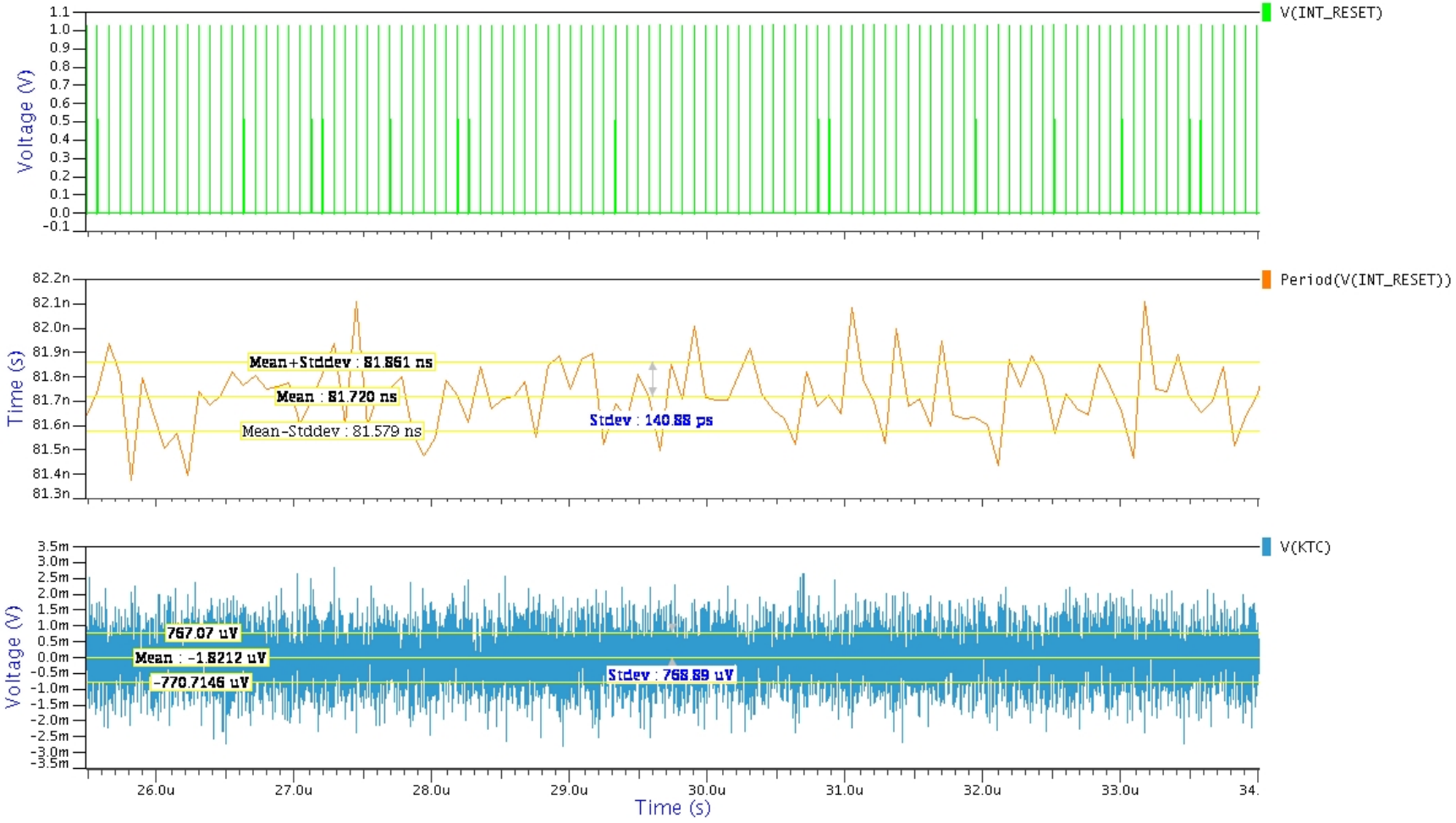

Figure 3-5 kTC Transient Noise Simulation

3.1.3 MOSFET Noise Simulation

Noise will be injected into the converter by referring the voltage noise density to a current noise density using Equation (2-32). A transient current source can then be placed in parallel with the simulated photodiode which is producing a constant DC current for this simulation.

The current noise density at the output of the PMOS is calculated using Equation (2-15). The corresponding piece-wise linear file controlling this transient source has a standard deviation calculated by using Equation (3-6). Given an $e_{n\text{-}mosfet}$ of 70.9 nV/√Hz, the σ_{pwl_mosfet} is equal to 11.68 pA. Figure 3-7 shows the output current of the transient source representing this MOSFET noise and its waveform calculated standard deviation equal to 11.65 pA.

$$\sigma_{pwl\_mosfet} = \frac{i_{n-mosfet}}{\sqrt{2T_s}} \tag{3-6}$$

The resulting SNR ratio of the simulation is determined with Equation (3-7) by using the mean of the individual integration period lengths $t_{int\text{-}sim\text{-}mosfet}$ and the standard deviation of these period lengths $\sigma_{tint\text{-}sim\text{-}mosfet}$. Figure 3-6 compares the simulated results with those calculated in the theoretical noise section.

$$SNR_{sim-mosfet} = \frac{N(\overline{t_{\text{int}-sim-mosfet}})}{\sqrt{N(\sigma^2_{t\,\text{int}-sim-mosfet})}} \tag{3-7}$$

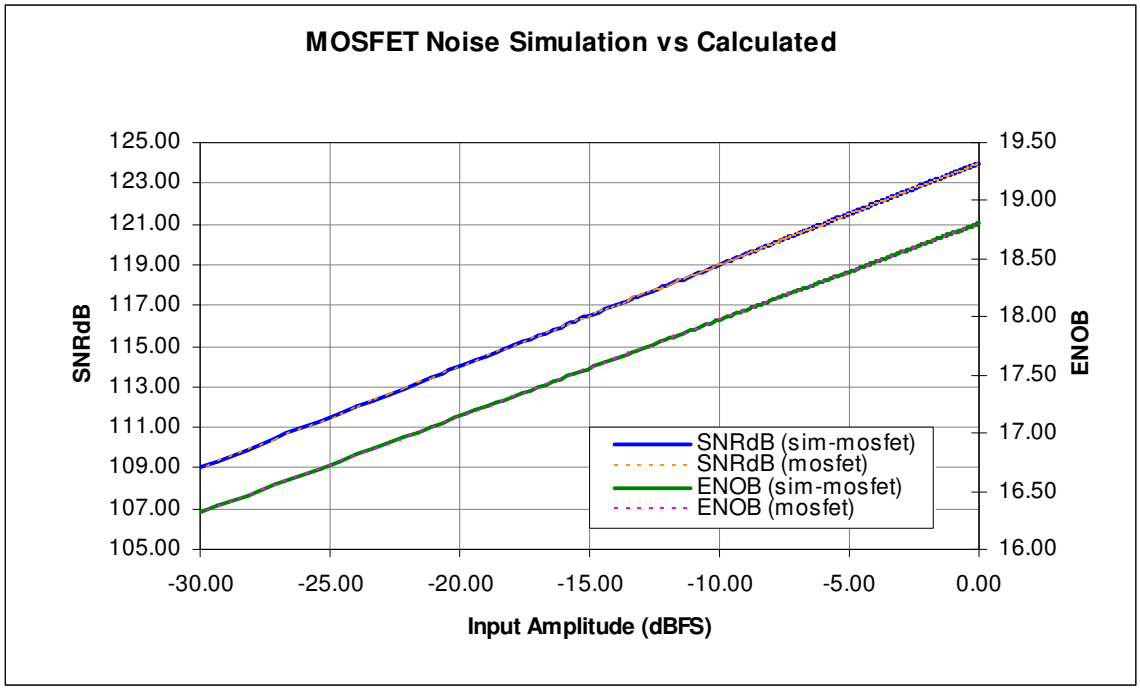

Figure 3-6 MOSFET Noise Simulated vs Calculated

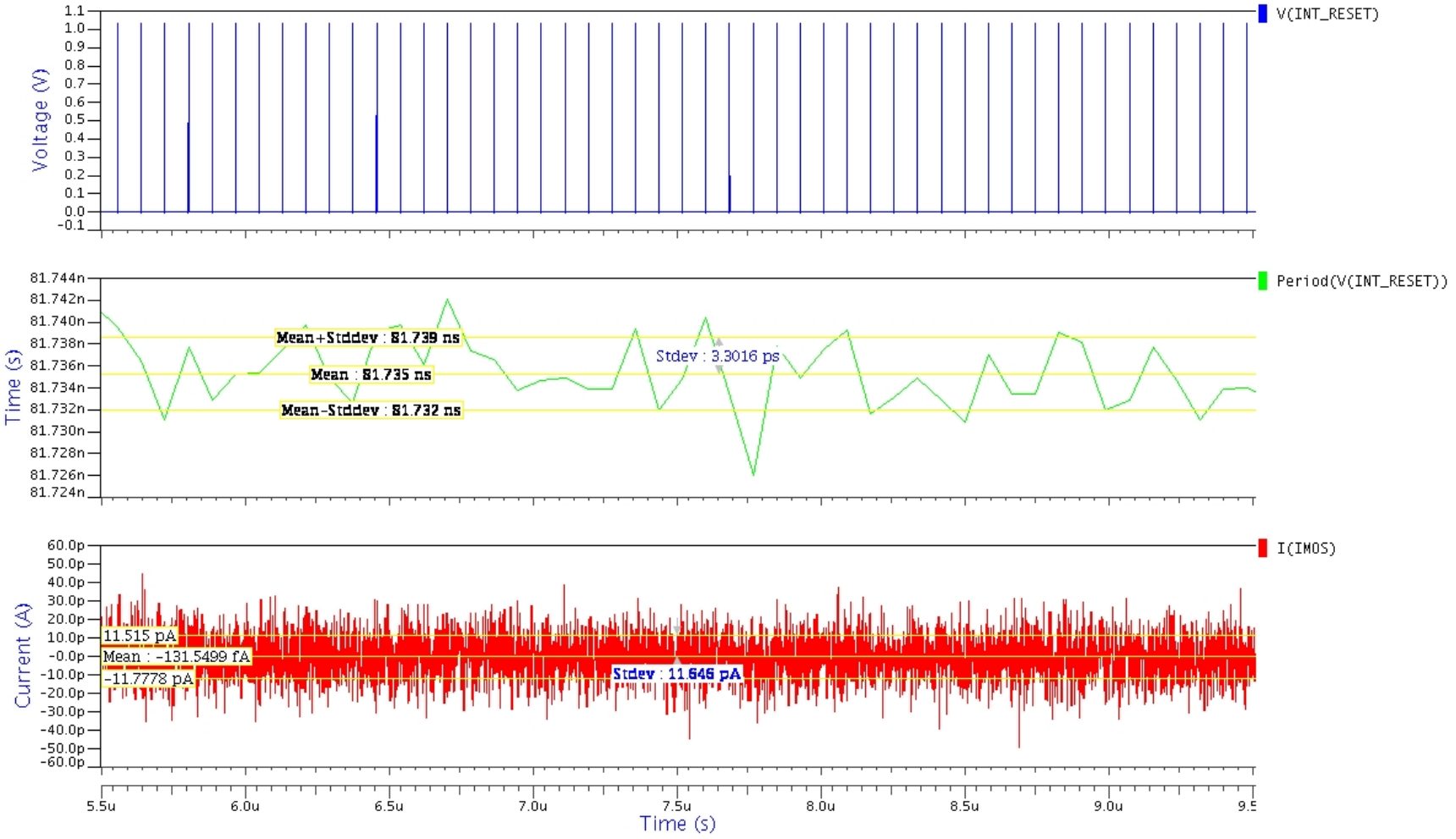

Figure 3-7 MOSFET Transient Noise Simulation

3.1.4 1/f Noise Simulation

Equation (2-18) provides an output referred current noise density. A transient current source can then be placed in parallel with the simulated photodiode that has a standard deviation given by Equation (3-8).

$$\sigma_{pwl\_1/f} = \frac{i_{n-1/f}}{\sqrt{2T_s}} \quad \textbf{(3-8)}$$

The resulting SNR ratio of the simulation is determined with Equation (3-7) by using the mean of the individual integration period lengths $t_{int\text{-}sim\text{-}1/ft}$ and the standard deviation of these period lengths $\sigma_{tint\text{-}sim\text{-}1/f}$. Figure 3-6 compares the simulated results with those calculated in the theoretical noise section.

$$SNR_{sim-1/f} = \frac{N(\overline{t_{\text{int}-sim-1/f}})}{\sqrt{N(\sigma^2_{t\,\text{int}-sim-1/f})}} \quad \textbf{(3-9)}$$

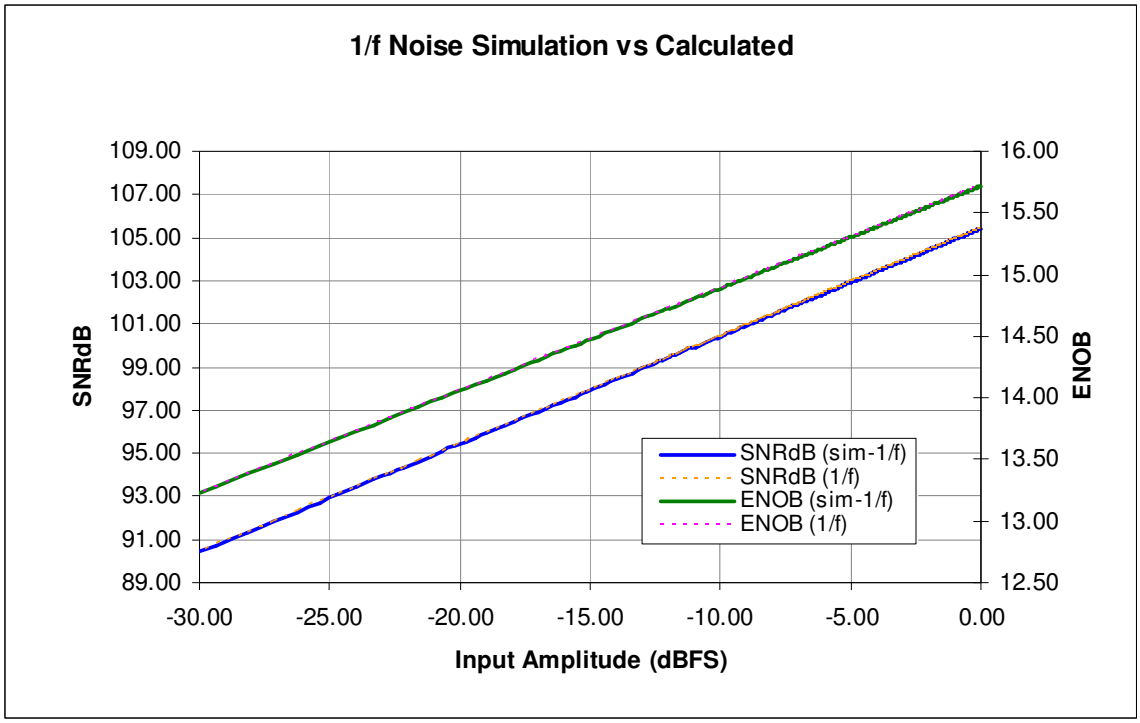

Figure 3-8 1/f Noise Simulated vs Calculated

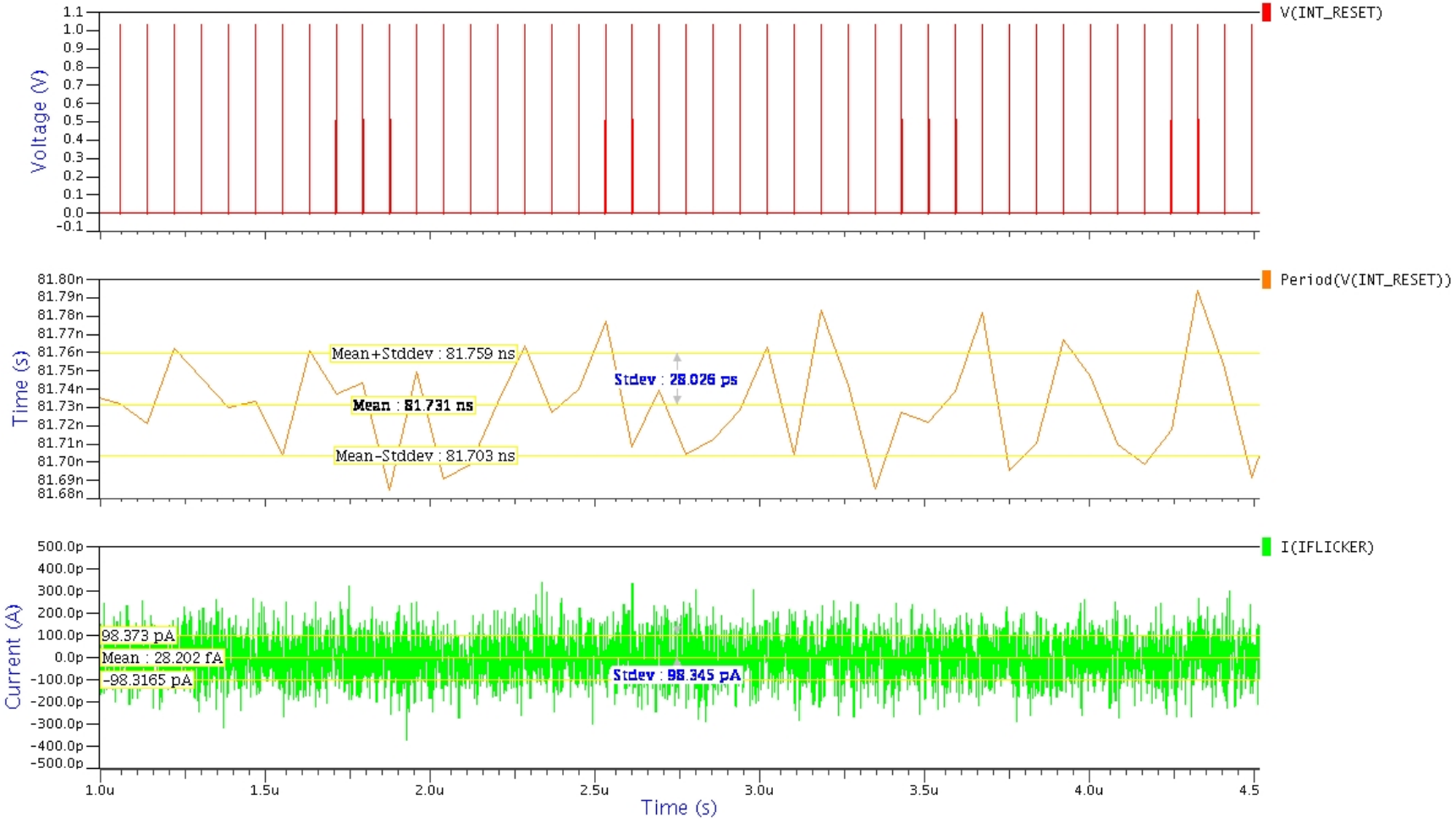

Figure 3-9 1/f Transient Noise Simulation

3.1.5 Jitter Noise Simulation

Simulations need not be run due to the fact that the effect of jitter noise is negligible. In a simulation period averaging 82 nS, a variation caused by Jitter Noise of under 50 fS results in a SNR ratio of 135 dB and above. It is unreasonable to collect microseconds of data using a step size of 50fS or less to resolve the effect of this noise. Therefore, the total noise simulation performed later will not contain the negligible effects of jitter noise.

3.1.6 Quantization Noise Simulation

Quantization noise can not be injected into this system and simulated. It is simply the loss of data caused by the digitizing of an analog signal level. Any conversion system having a bit resolution less than infinity will suffer from quantization noise. A later comparison will evaluate simulated noise numbers versus calculated noise results excluding the effect of quantization noise.

3.2 Second Order Noise Source Simulation

This section will discuss the simulation results of the individual contributions of power supply noise, and direct injection bias noise.

3.2.1 Power Supply Noise (Inverter Threshold Noise) Simulation

For the inverter threshold noise simulation, the ideal 1 volt VDD power supply will be replaced with a transient noise source with a standard deviation of 100 μVrms. In the ideal case, the first inverter's threshold will be linearly dependent on its power supply. This produces the worst case scenario for variation on the inverter's threshold.

The transistor's internal capacitances, modeled in the SPICE files will bandlimit the noise seen at the source of the PMOS transistors in the inverter chain. Expected simulation results will show a lessened affect of the power supply noise on this system then what was previously calculated. Figure 3-11 shows a power supply input with 100 uVrms noise and the given output pulse periods.

As expected, the reduced effect of this noise is illustrated in Figure 3-10. A full scale input produces an ENOB at the output of 17.3 in the worst case. Bandlimiting the noise at the power supply offers improvement over this number to more than 18.5 bits.

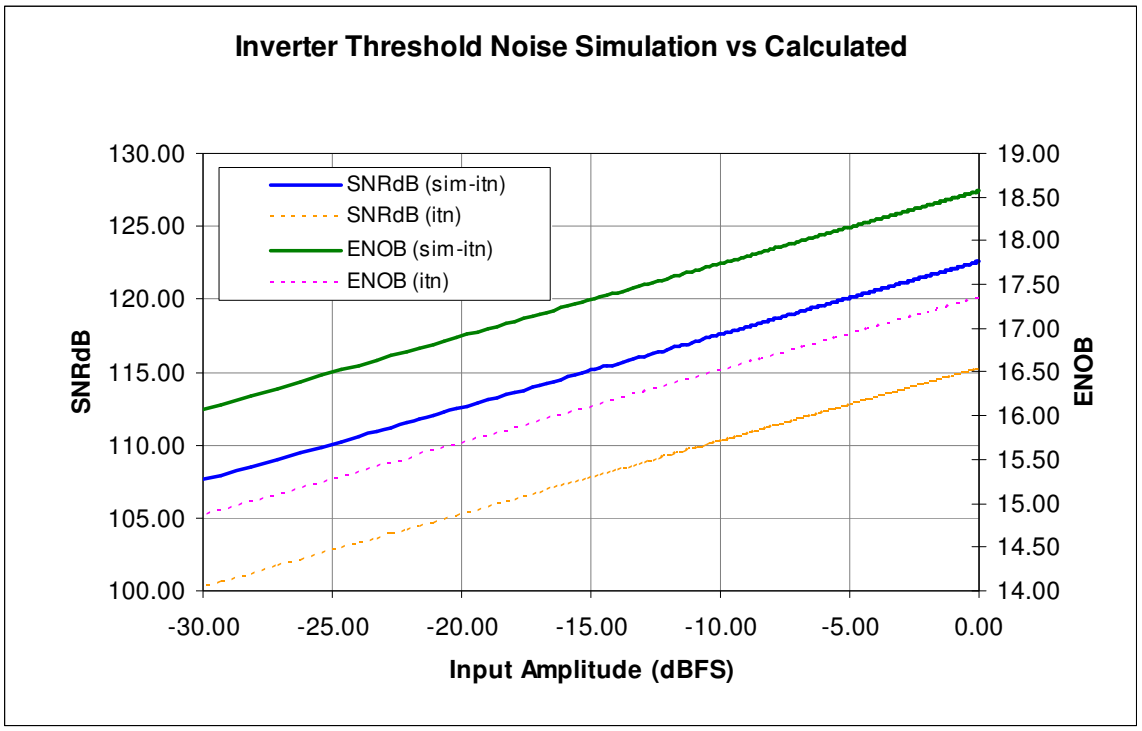

Figure 3-10 Power Supply Noise Simulated vs Calculated

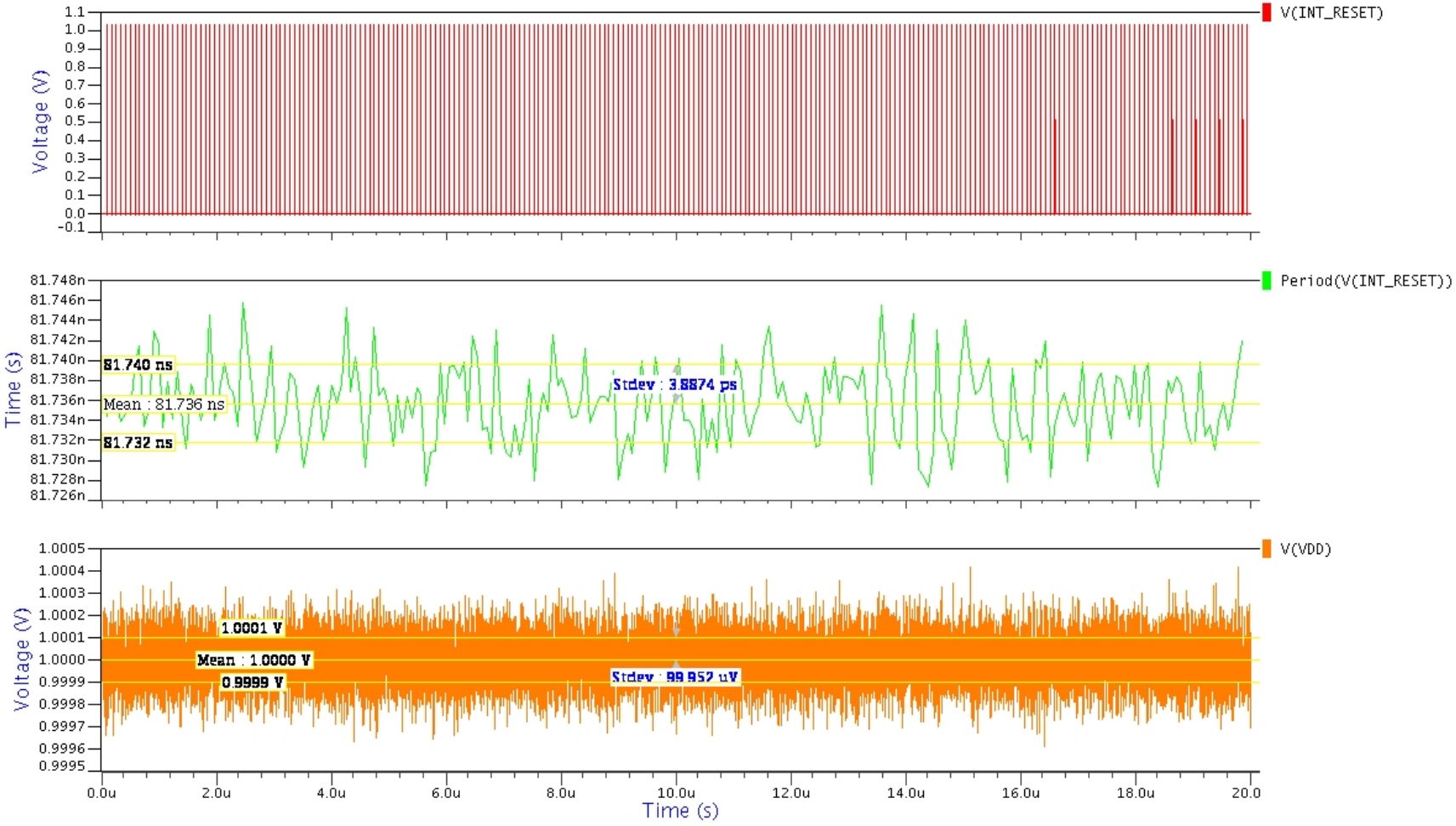

Figure 3-11 Transient Power Supply Noise Simulation

3.2.2 Direct Injection Bias Noise Simulation

Using the same simulation technique as the MOSFET noise simulation, DI Bias noise will be injected into the converter by referring the voltage noise density to a current noise density using Equation (2-32). Once again, a transient current source can then be placed in parallel with the simulated photodiode

The piece-wise linear file controlling this transient source has a standard deviation calculated by using Equation (3-10). A voltage noise density of 1 uV/√Hz at the gate of the DI results in a σ_{bias} of 164.82 pS. Figure 3-12 shows the output current of the transient source representing this DI bias noise and its waveform calculated standard deviation.

$$\sigma_{pwl\_bias} = \frac{i_{n-bias}}{\sqrt{2T_s}} \qquad \textbf{(3-10)}$$

The resulting SNR ratio of the simulation is determined with Equation (3-11) by using the mean of the individual integration period lengths $t_{sim\text{-}int}$ and the standard deviation of these period lengths $\sigma_{tsim\text{-}int}$. Figure 3-13 compares the simulated results with those calculated in the theoretical noise section. The SNR results are within 5% of each other verifying the previous calculations.

$$SNR_{sim-bias} = \frac{N(\overline{t_{sim-\text{int}}})}{\sqrt{N(\sigma^2_{tsim-\text{int}})}} \qquad \textbf{(3-11)}$$

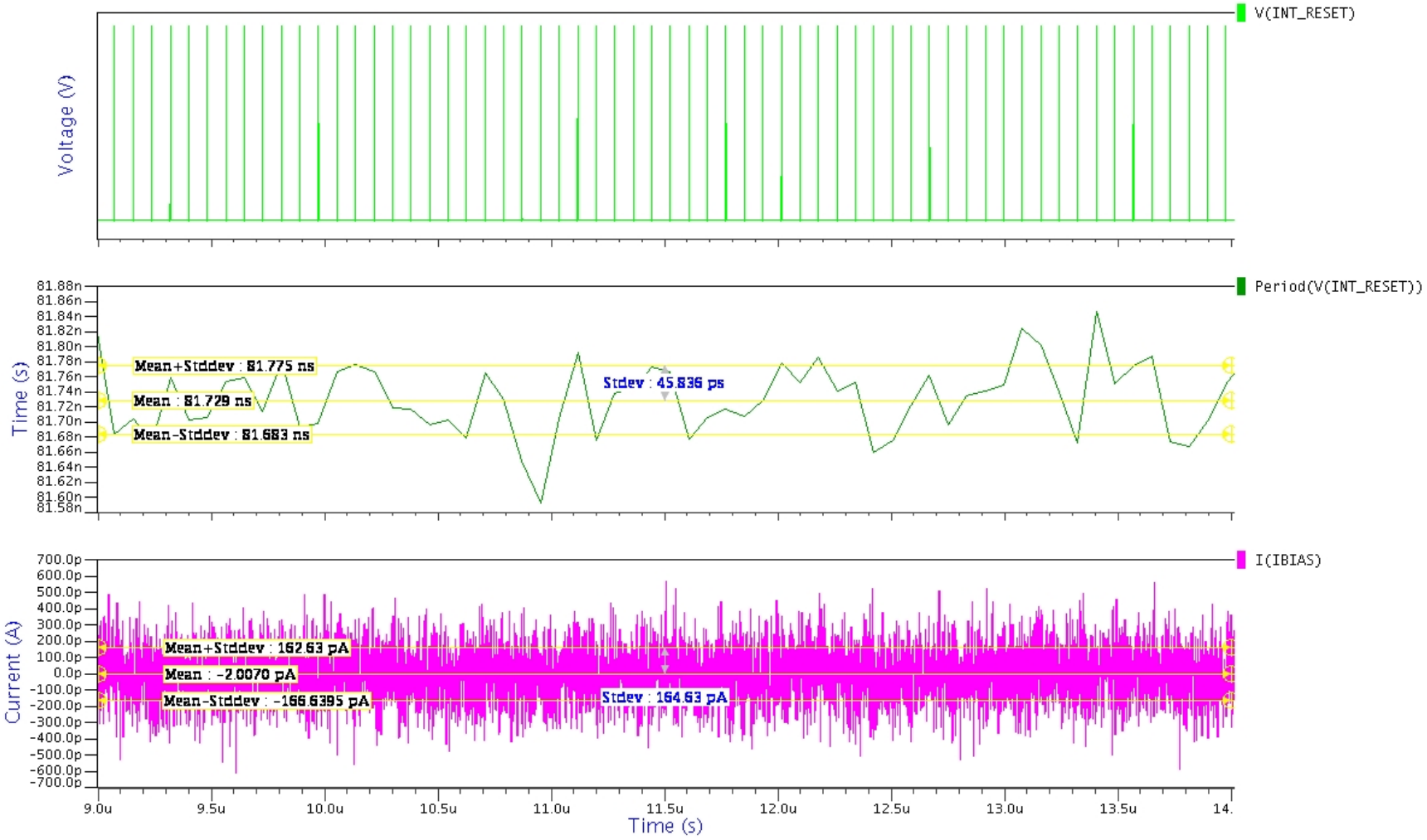

Figure 3-12 DI Bias Noise Simulation

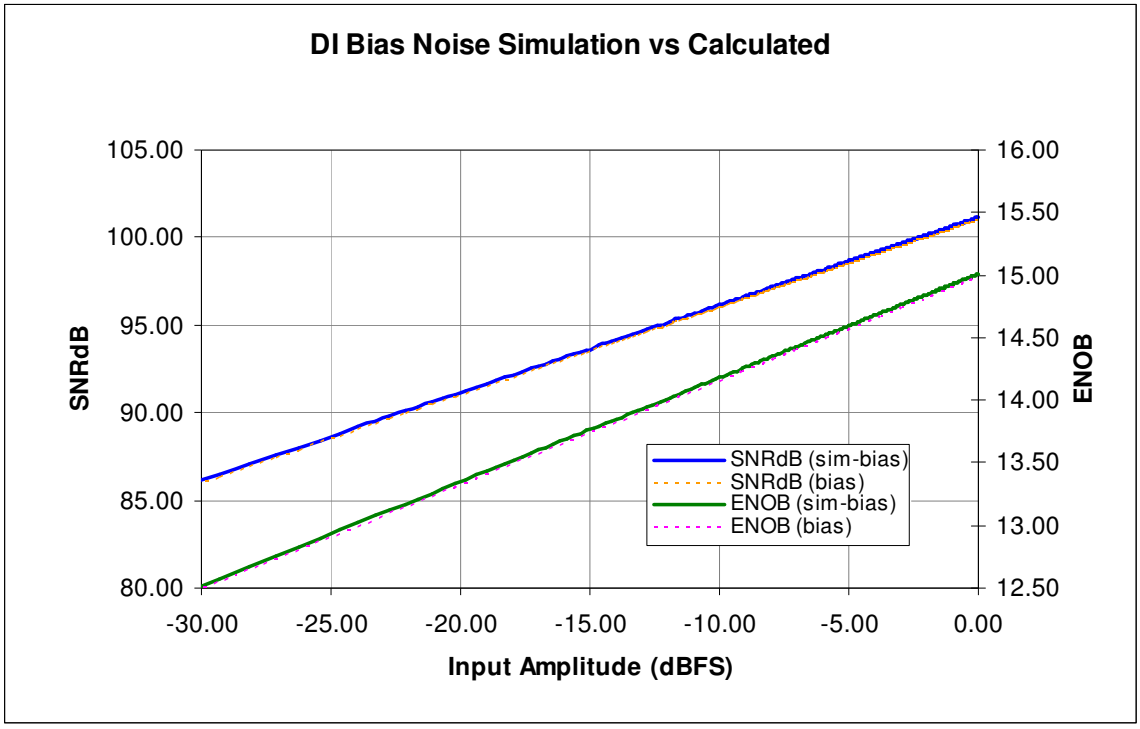

Figure 3-13 DI Bias Noise Simulated vs Calculated

3.3 Total Noise Simulation

For the final simulation, all noise sources were generated and implemented in the netlist. For comparison purposes, quantization noise is not included in the total calculated comparison shown in Figure 3-14. Calculated shot noise was also scaled by η to account for loss due to leakage currents. At full scale input or N equal to 2^{12} counts this system achieves a simulated SNR ratio of 78.01 dB and an ENOB of 11.17 bits.

The calculated total noise results from Section 312.3 are supported by the simulation shown in Figure 3-15.

$$SNR_{sim-total} = \frac{N(\overline{t_{\text{int}-sim-total}})}{\sqrt{N(\sigma^2_{t\,\text{int}-sim-total})}} \qquad \textbf{(3-12)}$$

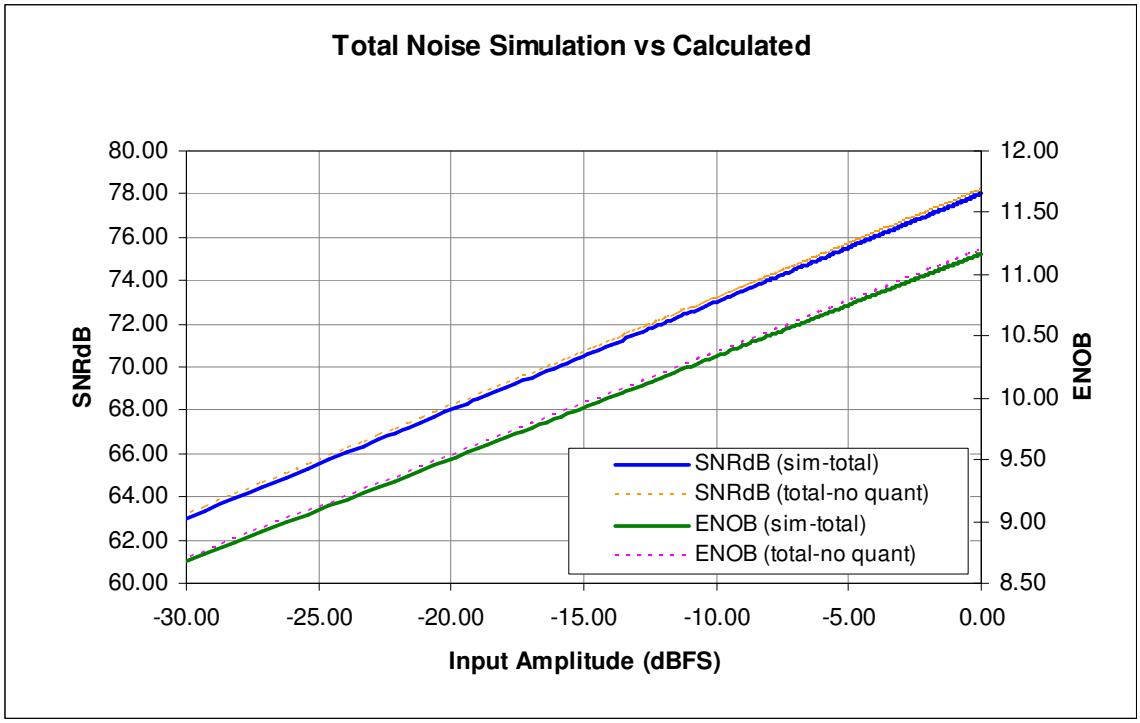

Figure 3-14 Total Noise Simulated vs Calculated

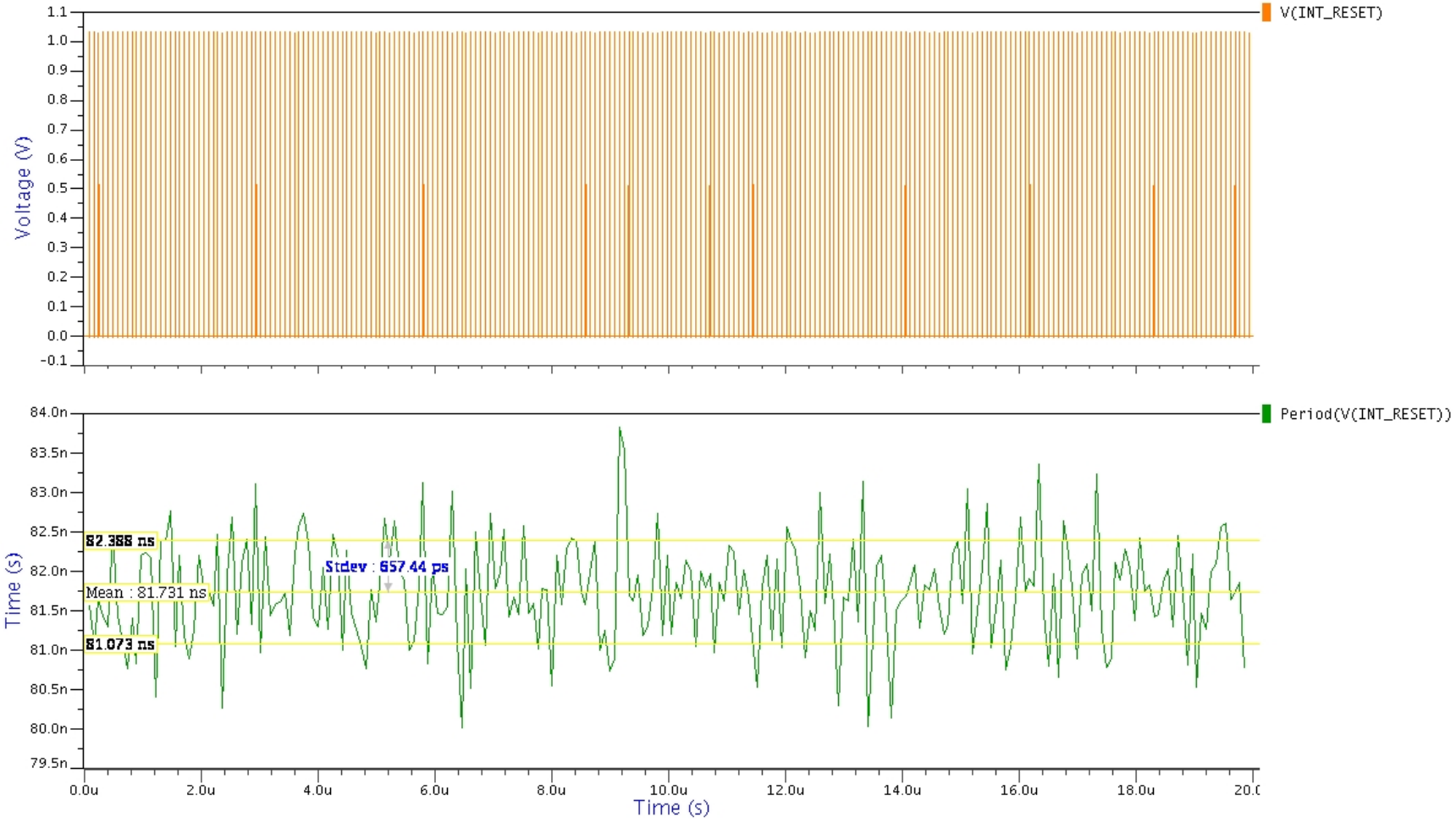

Figure 3-15 Total Noise Simulation

4 Design Considerations for Voltage to Frequency Converters

The following section will discuss aspects that an engineer must consider when designing a system using sub-pixel A/D VTOF converters.

4.1 Bypassing Power Supplies

Similar to other large integrated circuits (IC), power droop can be apparent at the internal structures if the power network is not properly designed. Thick traces will provide a low resistance path for current supplying the asynchronously switching inverters beneath each pixel. Along these traces, bypass capacitors must be generously placed to supply the needed power in the case of an intense scene or high speed digital shifts to move the captured data to the edge of the array.

4.2 Cascode Transistor

Each output pulse triggers an NMOS transistor responsible for resetting the integration node to a predefined voltage, usually ground. This continuous resetting is repeatedly turning off the Direct Injection (DI) amplifier which is responsible for setting the photodiode's bias voltage. Before the PMOS shuts off, the bias voltage at the source node is pulled down slightly. As a result, the bias voltage varies slightly over the sample period. The amount of noise that this translates to in the system's output is dependent on how sensitive the photodiode is to bias variations. Better isolation can be obtained by inserting a cascade transistor in between the DI amplifier and the integration capacitance node.

This cascade PMOS transistor will be biased using a lower voltage. Ensuring this transistor is operating in a region between the DI amplifier's subthreshold operation and saturation will allow full passage of the photocurrent to the integration node minus the

leakage seen inside the transistor. During a reset, the primary voltage variation will occur between the DI and cascade transistor. If a stricter photodiode bias voltage is needed, isolation can be greatly increased via use of this cascade PMOS at the expense of slight photocurrent loss due to leakage.

4.3 Loading

To ensure a quick and constant pulse width at the output of the converter, the final inverter must see a minimal load. In addition to resetting the integration capacitance via the reset NMOS, the output pulse must also clock a counting circuit. When this output pulse is properly buffered, a variety of counter types and sizes may be chosen which will be transparent to the VTOF. In the best case scenario, the final inverter will be driving the gate capacitance of the minimally sized NMOS reset transistor and a minimally sized buffer. This minimum size allowed is of course dependant on the process technology used.

If the output of the VTOF sees varying loads throughout a large format array, the resulting unbalanced reset times will cause diverse individual pixel sensitivities. These imperfections can be corrected via signal processing to some extent, but will require more circuitry area, power, and time. Designing for matched loads initially, will eliminate later post processing efforts.

5 Summary

It has been shown that a simple Voltage to Frequency A/D conversion system that is shot noise limited can be built using only 10 CMOS transistors. Due to its simplicity and size, this system can be used as a sub-pixel converter. Unlike conventional analog

sampling systems with a larger capacitance (well) that is sampled only once per sample period, this systems samples its well up to 2^N times for a N bit sample period.

The conversion of the input photocurrent at the sub-pixel level limits the system's noise vulnerability to one point. All design efforts can be focused on a single pixel conversion structure and later arrayed to make large format imagers. Incorporating good layout practices and the scalability of this sub-pixel converter allow for the rapid development of efficient ROICs.

As with any system there are design tradeoffs including area, speed, and power. For example, the designer could use a more advanced preamplifier at a greater cost of area and power. This specific DI amplifier design was analyzed because of its minute area requirements applicable to a sub-pixel system.

Shot noise limited noise performance has been proven. In order to realize the full benefits of digital pixel architecture, the designs aspects of area, speed, and power consumption must be visited. Figure 5-1 outlines the advantages of a full digital pixel compared to an analog pixel.

Transitioning to a digital well ROIC architecture eliminates the need for large area consuming higher voltage integration capacitors. Spatial resolution is no longer limited by the ROIC due to these capacitors, and can be defined by the active array's pixel pitch. The latest submicron process technologies using lower transistor voltages can also be used to decrease the size of the LSB and reduce the total circuit area, and power consumption.

A single high speed 10Gbps digital output can read out more than 80 times the numbers of pixels per second than a 10 million pixels per second analog output in a 12 bit

imager. Digital outputs eliminate the need for multiple analog signal conditioning and sampling structures increasing design cost and power consumption.

As the size of imagers increase, high speed digital outputs offer the needed bandwidth to keep up with desired pixel rates. Increased readout rate allows for an increased field of view at a constant frame rate and spatial resolution.

	Analog Technology	Digital Technology
Noise	Shot Noise Limited	Shot Noise Limited
Area	Large Integration Capacitance Required	Digital Well requires minimal area
Process Technology	Older higher voltage process technologies must be used to maintain dynamic range	Current submicron process technologies can be used decreasing area and power consumption
Readout Rate	Noise limits readout rates of individual taps to approximately 10 million pixels per second	Digital readout rates allow for 500 million+ pixels per second per tap
Scalability	ROICs must be individually designed with area, power, and speed design tradeoffs in mind	Digital pixels can be arrayed to accommodate large high speed imagers with high spatial resolution

Figure 5-1 Digital Pixel Advantages

This system has the ability to accommodate many varying requirements. The input capacitance can be easily adjusted to vary the system's full frame rate and sensitivity to a given input current. Due to its versatility of application and small area, this shot noise limited A/D conversion system is an effective and scalable sampling solution for current and future advanced imaging systems.

6 Appendix A: Mobility Ratio Calculation

The easiest way to calculate the mobility ratio of the NMOS and PMOS transistors is to perform a DC analysis on a static inverter with its output fed back into its input. The width of the NMOS is fixed and a sweep is performed on the width of the PMOS. When the voltage on the output net equals half the supply voltage, the transistors are matched. The width of the PMOS divided by the width of the NMOS is the mobility ratio for the process. Figure 5-2 illustrates the schematic used in the DC analysis.

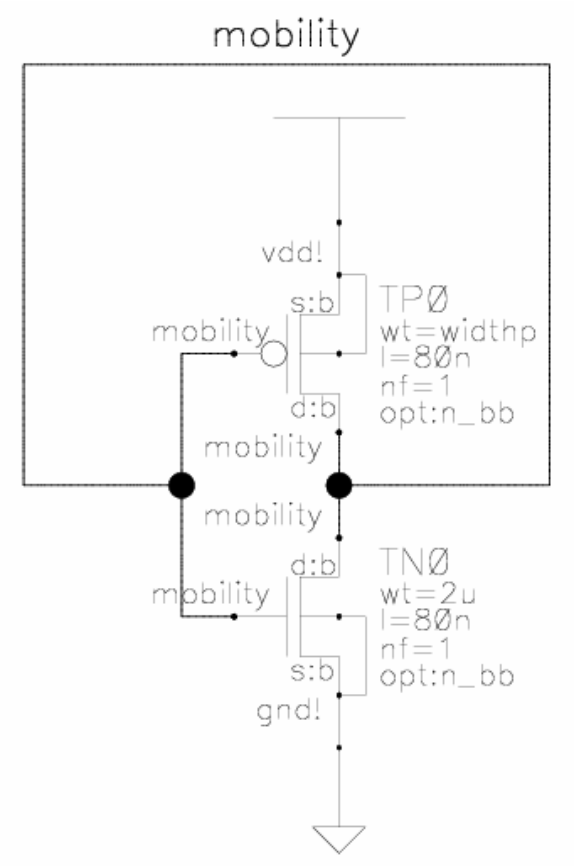

Figure 5-2 Mobility Ratio Test Schematic

Figure 5-3 shows the DC voltage at the feedback node of the inverter for different PMOS widths. When the voltage axis is equal to 500 mV, the width axis is equal to 5.0628 um. This width divided by the fixed 2 um width of the NMOS results in a mobility ratio of 2.5314.

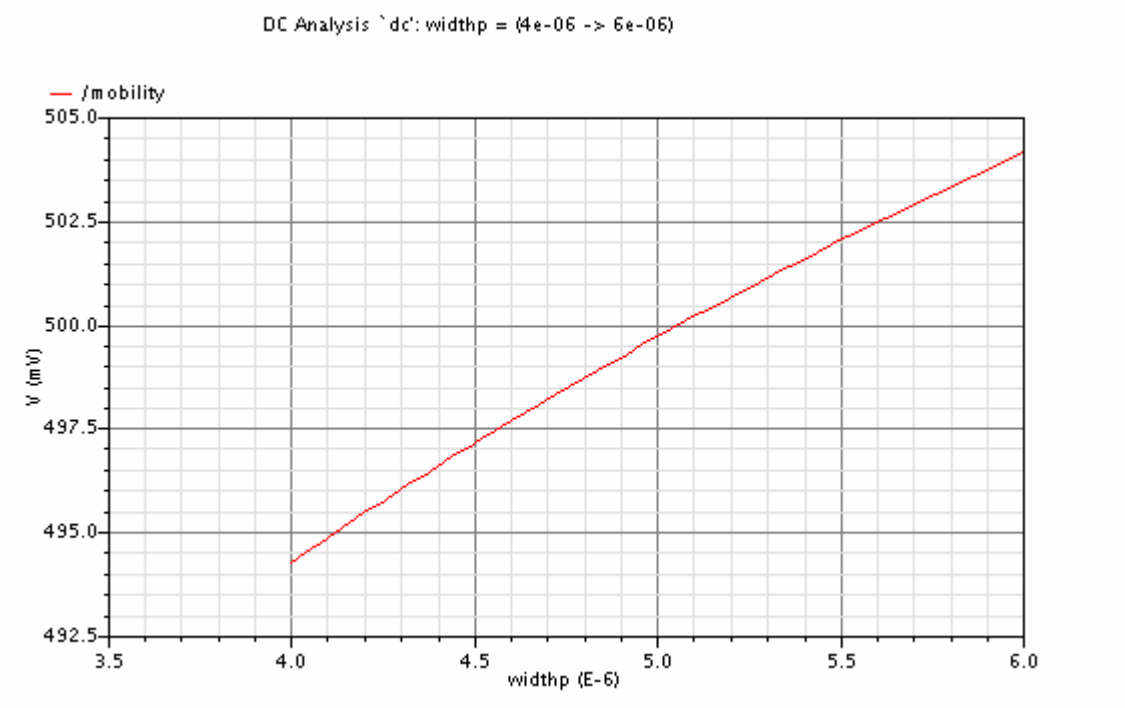

Figure 5-3 DC Sweep of PMOS width

7 Appendix B: Minimum Size Inverter Threshold

The four inverters used in the VTOF circuitry for the entire analysis were sized according to the calculated mobility ratio of 2.5314 (Appendix A). The minimum width of the NMOS transistor in the process is 140 nm thus resulting in a matched PMOS width of 355 nm. A DC analysis performed on the schematic in Figure 5-4 resulted in an inverter threshold of 450.4 mV.

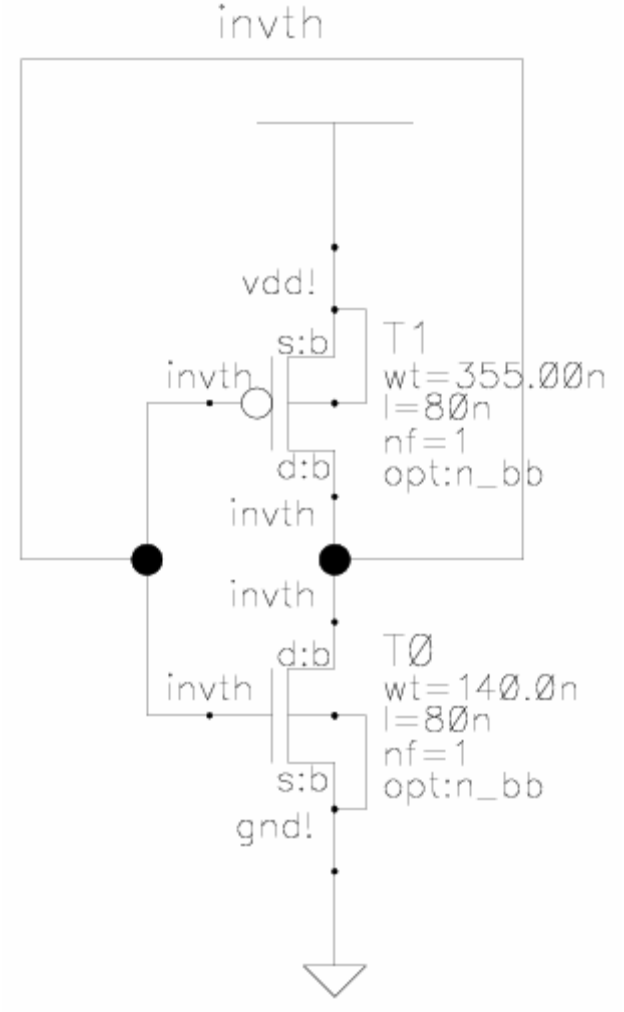

Figure 5-4 Inverter Threshold Test Schematic

8 Appendix C: Integration Node Capacitance

The capacitance at any given node can be defined using Equation (5-1) where charge q_x and voltage v_x are at the same node. The integration capacitance of the VTOF is made up of the gate capacitances seen at the first inverter and the drain capacitances of the DI amplifier PMOS and reset NMOS. In order to begin analysis on the VTOF, the integration capacitance must be known.

$$C_{xx} = \frac{\partial q_x}{\partial v_x} \tag{5-1}$$

Figure 5-5 highlights the node named *int*, the integration capacitance node of the VTOF. A SPICE simulation performed on this node using Equation (5-1) results in a capacitance value of 1.06 fF. This value is only taking into account the device capacitances seen at the endpoints. Post-layout parasitic capacitances will be the majority of the total capacitance.

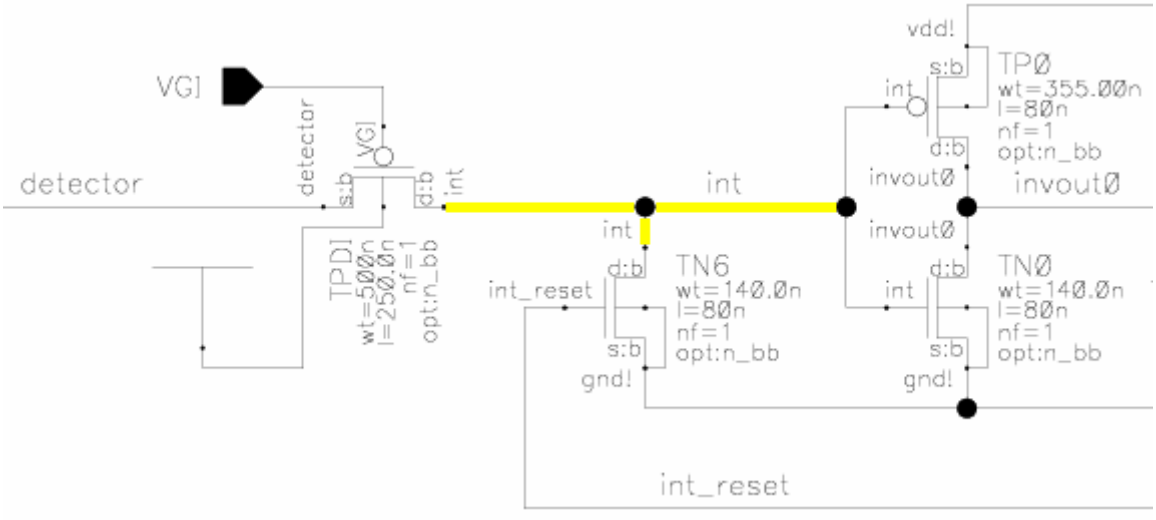

Figure 5-5 Integration Capacitance Node

An optimized layout of the VTOF results in an extracted parasitic capacitance of 3.96 fF on the integration node. Parasitic extraction was performed with Mentor Graphics Calibre xRC toolset. The total calculated integration capacitance equals 5.02 fF. 5 fF will be used throughout this thesis to simplify the calculations.

9 Appendix D: Transient Noise Source MATLAB M-File

```
clear all;
%length = 26650;      %# PWL pairs
Cap = 5e-15;          %Integration Capacitance
Temp = 218;           %-55 Celcius
k = 1.380658E-23;     %Boltzman's Constant
Vth = 0.4504;         %Inverter Threshold
Idc = 30e-9;          %DC Current
Tint=Cap*Vth/Idc;     %Integration Time
Tint=81.8e-9;         %Simulation Mean Int Time
Ts = Tint/100;        %Sample Time
q = 1.60217733e-19;   %Electron Charge
en = sqrt(8*k*Temp/3/(Idc*q/1.0002/k/Temp));
in_flicker = 3.97879E-15;
Rph = 150e6;
length = ceil(20.1e-6/Ts);
SIMTIME = Ts * length

stddevVDD = 100e-6;
for match = 1:2000
   VDD = 1 + stddevVDD*randn(length,1);
   if (abs(stddevVDD - std(VDD)) <= 1e-9)
      disp('VDD STD MATCHED')
      std(VDD)
      break;
   end
end

stddevVGI = 25e-6;
for match = 1:10
   VGI = 0.65 + 0*stddevVGI*randn(length,1);
   if (abs(stddevVGI - std(VGI)) <= 1e-8)
      disp('VGI STD MATCHED')
      std(VGI)
      break;
   end
end

stddevVKTC = sqrt(k*Temp/Cap);
for match = 1:2000
   VKTC = 0 + stddevVKTC*randn(length,1);
   if (((stddevVKTC - std(VKTC)) >= -1e-8) & ((stddevVKTC - std(VKTC)) <= 0))
      disp('VKTC STD MATCHED')
      std(VKTC)
      break;
   end
end

stddevIPH = sqrt(2*q*Idc)/(sqrt(2*Ts))
for match = 1:2000
   IPH = -Idc + stddevIPH*randn(length,1);
   if (((stddevIPH - std(IPH)) >= -1e-13) & ((stddevIPH - std(IPH)) <= 0))
```

```
        disp('IPH STD MATCHED')
        std(IPH)
        break;
    end
end

stddevIMOS = (en/Rph)/(sqrt(2*Ts))
for match = 1:2000
    IMOS = 0 + stddevIMOS*randn(length,1);
    if (((stddevIMOS - std(IMOS)) >= -1e-15) & ((stddevIMOS - std(IMOS)) <= 0))
        disp('IMOS STD MATCHED')
        std(IMOS)
        break;
    end
end

stddevIBIAS = (1e-6/Rph)/(sqrt(2*Ts))
for match = 1:2000
    IBIAS = 0 + stddevIBIAS*randn(length,1);
    if (((stddevIBIAS - std(IBIAS)) >= -1e-14) & ((stddevIBIAS - std(IBIAS)) <= 0))
        disp('IBIAS STD MATCHED')
        std(IBIAS)
        break;
    end
end

stddevIFLICKER = (in_flicker)/(sqrt(2*Ts))
for match = 1:2000
    IFLICKER = 0 + stddevIFLICKER*randn(length,1);
    if (((stddevIFLICKER - std(IFLICKER)) >= -1e-16) & ((stddevIFLICKER - std(IFLICKER)) <= 0))
        disp('IFLICKER STD MATCHED')
        std(IFLICKER)
        break;
    end
end

for m = 1:length
    TIME(m,1) = ((m-1)*Ts);
end

fid = fopen('datapwl.txt', 'w');
fprintf(fid, 'VVGI (vgi 0) PWL\n');
for m = 1:2
%for m = 1:length-1
    fprintf(fid,'+%10e %10e\n',TIME(m,1),VGI(m,1));
    fprintf(fid,'+%11.10e %11.10e\n',TIME(m+1,1)-1e-12,VGI(m,1));
end

fprintf(fid, 'VVDD (vdd 0) PWL\n');
%for m = 1:2
for m = 1:length-1
    fprintf(fid,'+%11.10e %11.10e\n',TIME(m,1),VDD(m,1));
    fprintf(fid,'+%11.10e %11.10e\n',TIME(m+1,1)-1e-12,VDD(m,1));
end
```

```
fprintf(fid, 'VKTC (0 ktc) PWL\n');
%for m = 1:2
for m = 1:length-1
   fprintf(fid,'+%11.10e %11.10e\n',TIME(m,1),VKTC(m,1));
   fprintf(fid,'+%11.10e %11.10e\n',TIME(m+1,1)-1e-12,VKTC(m,1));
end

fprintf(fid, 'IPH (net28 vcom) PWL\n');
%for m = 1:2
for m = 1:length-1
   fprintf(fid,'+%11.10e %11.10e\n',TIME(m,1),IPH(m,1));
   fprintf(fid,'+%11.10e %11.10e\n',TIME(m+1,1)-1e-12,IPH(m,1));
end

fprintf(fid, 'IMOS (int 0) PWL\n');
%for m = 1:2
for m = 1:length-1
   fprintf(fid,'+%11.10e %11.10e\n',TIME(m,1),IMOS(m,1));
   fprintf(fid,'+%11.10e %11.10e\n',TIME(m+1,1)-1e-12,IMOS(m,1));
end

fprintf(fid, 'IBIAS (int 0) PWL\n');
%for m = 1:2
for m = 1:length-1
   fprintf(fid,'+%11.10e %11.10e\n',TIME(m,1),IBIAS(m,1));
   fprintf(fid,'+%11.10e %11.10e\n',TIME(m+1,1)-1e-12,IBIAS(m,1));
end

fprintf(fid, 'IFLICKER (int 0) PWL\n');
%for m = 1:2
for m = 1:length-1
   fprintf(fid,'+%11.10e %11.10e\n',TIME(m,1),IFLICKER(m,1));
   fprintf(fid,'+%11.10e %11.10e\n',TIME(m+1,1)-1e-12,IFLICKER(m,1));
end
fclose(fid);
```

10 Appendix E: Transistor 3σ Mismatch Calculations

In submicron process technologies, transistor mismatch can be detrimental to one's design if not careful. Random variations in transistor sizing across a chip can result in varying transistor threshold voltages. This variation is inversely proportional to device area.

In the case of the DI amplifier, the threshold voltage of this PMOS ultimately sets the bias for the photodiode. In an imager situation, mismatched DI amplifiers will result in varying pixel sensitivities across the array. This effect could render captured data useless if the system is not designed to limit mismatch.

A design tradeoff must be reached regarding the size of the DI transistor. Increasing the area of the DI transistor will decrease threshold mismatch across an imager array, but it will increase the capacitance seen on the integration node.

IBM supplies transistor mismatch models allowing Monte Carlo simulations to be run measuring across chip transistor variations. A DC sweep analysis was run 1000 times on a PMOS transistor to determine the threshold voltage variation for a given area. The threshold voltage of a PMOS will be defined as the point when the drain current is equal to 70nA*(W/L). A number of iterations were run varying the area of the transistor.

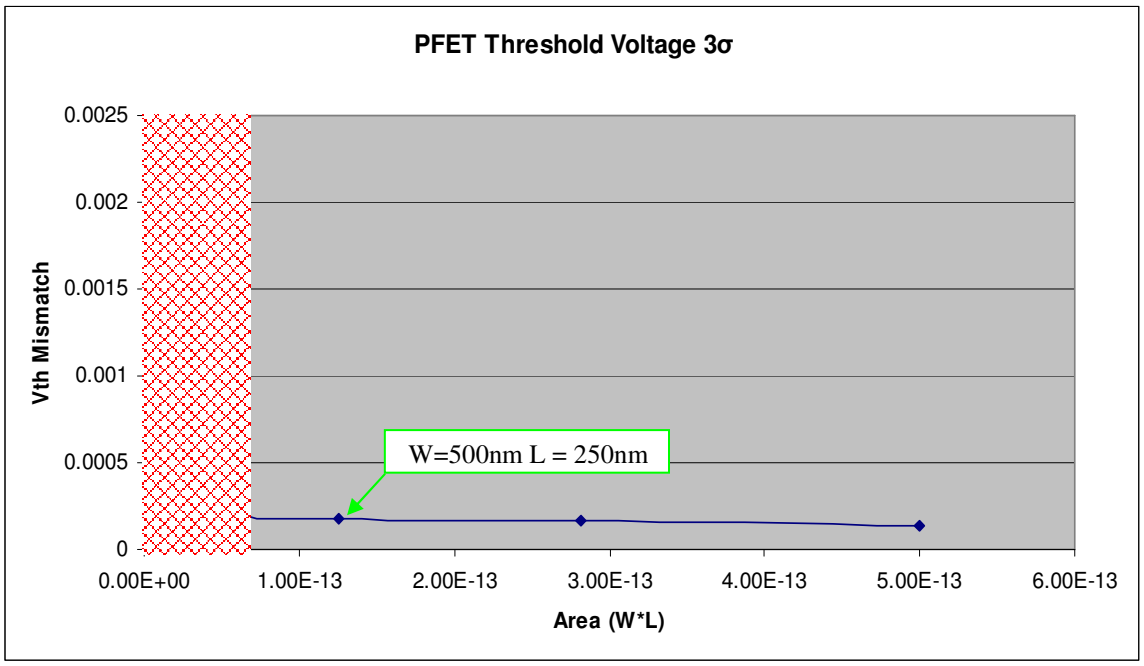

Figure 5-6 PFET 3σ Threshold Mismatch vs Area

Figure 5-6 show the 3σ threshold voltage mismatch for transistors with areas increasing from left to right. The size of the DI PMOS transistor was chosen to have a width of 500 nm and a length of 250 nm giving us an area of 125 sq. fm. This size keeps the increased integration capacitance at a minimum while also putting the transistor out of the higher mismatch range represented by red crosshatch in the plot.

11 Appendix F: Voltage-To-Frequency Converter Schematic

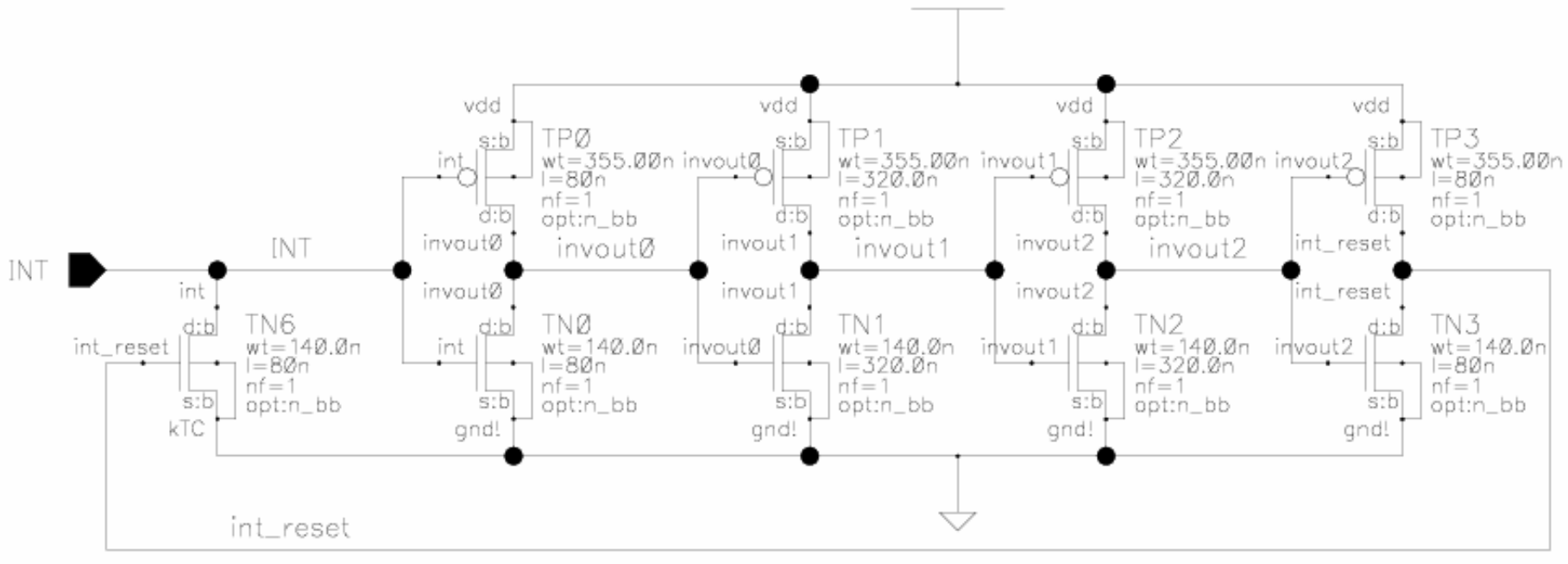

Figure 5-7 Voltage-To-Frequency Converter (Enlarged)

[i] Shahram Tadayyon, "A Pixel-Level A/D Converter For the Imaging Array of an Advanced Interferometer," MIT, Cambridge, MA, 1999.
[ii] Betty Lise Anderson, Richard L. Anderson, "Fundamentals of Semiconductor Devices" McGraw-Hill, New York, NY, 2005.
[iii] John L. Vampola, "Readout Electronics for Infrared Sensors," *SPIE - Electro-Optical Components*, vol. 3, pp. 285-342, Jan. 1993.
[iv] Yail Nemirovksy, Igor Brouk, Claudio G. Jakobson, "1/f Noise in CMOS Transistors for Analog Applications," *IEEE Transactions on Electron Devices*, vol. 48, no. 5, pp 921-927, May, 2001.
[v] E. L. Dereniak and G.D. Boreman, "Infrared Detectors and Systems," Wiley-Interscience, New York, NY, 1996
[vi] SPICE – Electronics Research Laboratory – University of California, Berkley
[vii] John McNeill, "Jitter in Ring Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, pp 870-879, June, 1997.
[viii] Toh Yuping, "The Effect of Channel Width on Jitter in CMOS Ring Oscillators" WPI, Worcester, MA, 2002.
[ix] John McNeill, "Jitter in Ring Oscillators," Appendix I, Boston University, Boston, MA, 1994.
[x] Saibal Mukhopadhyay, Arijit Raychowdhury, Kaushik Roy, "Accurate Estimation of Total Leakage in Nanometer-Scale Bulk CMOS Circuits Based on Device Geometry and Doping Profile," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 3, March, 2005.