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Design of Tunable Low-Noise Amplifier in 0.13um CMOS Technology for Multistandard RF Transceivers

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by

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Abstract

The global market of mobile and wireless communications is witnessing explosive growth in size as well as radical changes. Third generation (3G) wireless systems have recently been deployed and some are still in the process. 3G wireless systems promise integration of voice and data communications with higher data rates and a superior quality of service compared to second generation systems. Unfortunately, more and more communication standards continue to be developed which ultimately requires specific RF/MW and baseband communication integrated circuits that are designed for functionality and compatibility with a specific type of network. Although communication devices such as cellular phones integrate different services such as voice, Bluetooth, GPS, and WLAN, each service requires its own dedicated radio transceiver which results in high power consumption and larger PCB area usage. With the rapid advances in silicon CMOS integrated circuit technology combined with extensive research, a global solution which aims at introducing a global communication system that encompasses all communication standards appears to be emerging. State of the art CMOS technology not only has the capability of operation in the GHz range, but it also provides the advantage of low cost and high level of integration. These features propel CMOS technology as the ideal candidate for current trends, which currently aim to integrate more RF/MW circuits on the same chip. Armed

with such technology ideas such as software radio look more attainable than they ever were in the past. Unfortunately, realizing true software radio for mobile applications still remains a tremendous challenge since it requires a high sampling rate and a wide-bandwidth Analog-to-Digital converter which is extremely power hungry and not suitable for battery operated mobile devices. Another approach to realize a flexible and reconfigurable RF/MW transceiver that could operate in a diverse mobile environment and provides a multiband and multistandard solution. The work presented in this thesis focuses on the design of an integrated and tunable low-noise amplifier as part of software defined radio (SDR).

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Chapter 1

Introduction

1.1 Cellular Phones: Past, Present, and Future

Very few technological advances have had such a profound impact on our daily lives as the cellular phone. It was more than twenty years ago when the first analog cellular network was introduced to the public in the United States. After decades of research and development based on an idea that originated in the late 1940s. This analog cellular network, also known as the Advanced Mobile Phone System (AMPS), was later labeled as the first generation, or 1G, wireless cellular network. While deploying such a network was a major achievement, the first generation of mobile telephones had very little popularity among the general public, mainly due to the high costs of handsets and subscriptions. In spite the financial burden, analog cellular networks soon became overcrowded and eventually services were deemed

unreliable. The solution was digital transmission techniques in order to improve quality of service, increase network capacity, and reduce operating costs. This marked the birth of the second generation (2G) cellular networks with the introduction of new standards such as Global System for Mobile Communications (GSM) and IS-95. Although these new standards all relied on the advantages digital transmission techniques, they used different air interfaces. GSM uses Time Division Multiple Access (TDMA), while IS-95 uses Code Division Multiple Access (CDMA). The rise of the 2G cellular networks around the world was the turning point for the cellular telephone industry. In the United States, the number of subscribers increased from a few hundred thousands in the late 1980s to tens of millions by the in the mid 90s. Nowadays it is estimated that there are more than 1 billion cellular phone subscribers around the world.

Second generation cellular systems were mainly designed to handle voice communication. In addition, they were also designed to support low data rate transfers at 14.4 kbps [50]. The long-term vision, however, was to create a global cellular network that supports voice, data, and even video services, essentially turning the cellular phone into a multi-media global communication device that could serve as a pocket PC. Indeed, with the explosive growth and popularity of the Internet, demand rose for higher data rates over the air waves. This market demand was one of the major forces behind establishing new wireless systems that could support higher data rates such as General Packet Radio Service (GPRS), Enhanced Data Rates for GSM Evolution

(EDGE), High Performance Radio LAN (HIPERLAN), International Mobile Telecommunications-2000 (IMT-2000), Wireless Local Area Networks (WLAN), Bluetooth, and many more [52]. The integration of these standards with the existing 2G standards was viewed as an evolution to the next generation of cellular networks, or 3G.

The migration to pure 3G cellular networks was a very gradual and slow progression. At first, systems such as GPRS and EDGE were developed and deployed merely as an extension to the 2G networks; they did not offer the full capabilities and services that were initially promised by 3G cellular networks. In fact, true deployment of 3G networks has just been initiated by major cellular service providers such as Verizon and Nextel, who are currently in the process of deploying 3G networks that offer average data rates between 400 and 700 kbps [53]. The essence of 3G networks is to merge voice and high-speed data services as well as to provide access to the Internet and encompass a wide range of multi-media services.

3G networks present a major and significant leap forward from the 2G networks, especially in regards to the inclusion of IP-based services. Unfortunately, with the evolution of 3G networks, many different wireless standards have been developed targeting different kinds of applications such as voice, data, images, broadcast and online gaming [52]. Some of these standards have been designed to support communications over a long distance such as Wideband CDMA (W-CDMA) while others have been developed for short range applications such as Bluetooth. The existence of all these different

standards makes it difficult for users to roam across diverse networks that provide different types of services. In many cases consumers are compelled to purchase more than one handset in order to have concurrent cellular service in the United States and Europe.

It appears clear that the telecommunication industry is moving towards a global solution. Researchers are exploring a more expanded network which may ultimately span the entire globe, and the development of a single architecture that will encompass all the different platforms that exist today. The long term vision is to have networks which are completely IP-based and allow the consumer access to any kind of service, anytime and anywhere [54]. This is the essence of the next generation of mobile systems, the 4G networks. Research into fourth generation standards has just been initiated, and according to many authorities in this field, 4G systems could become a reality as early as 2010. Although such a forecast could be considered optimistic, it is never too early to start looking into the major areas which require considerable amount of research in order for such a network to exist one day. And one of these issues is the underlying technology that is required to realize such a system.

1.2 Motivation

The push towards a global system requires the development of flexible, reconfigurable, and multistandard radio transceivers. In other words, there is

an emerging need for radio transceivers that can support multiple wireless standards. For example, a flexible hand-held mobile device would enable a user to access the Internet through a WLAN as well as place a phone call on a GSM network. For hand-held devices to reach such flexibility requires major modifications applied to traditional RF/MW transceivers such as the one shown in Figure 1.1.

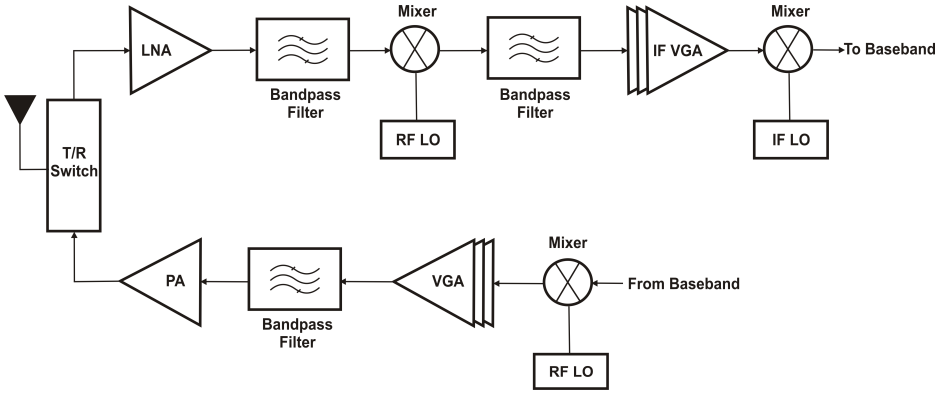

Figure 1.1: Simplified heterodyne RF front end.

The simplified architecture in shown in Figure 1.1 uses the commonly known heterodyne design introduced by E.H. Armstrong in 1918 for short wave reception [8]. It is necessary in modern digital communication circuits to use numerous types of data and channel encoding before converting the signal to higher frequency for transmission. The main point of interest here is the RF front end, hence, baseband encoding/decoding is not shown in Figure 1.1. The encoded data is upconverted by the mixer to a higher frequency which is suitable for radio transmission. An ideal mixer produces signals centered at frequencies which are the sum and differences of the data

signal's center frequency and the carrier sine wave frequency generated by the RF local oscillator. The variable-gain amplifier (VGA) provides variable and controllable gain to the upconverted signal, which serves many purposes such as supplying adequate signal power at the antenna and ensuring transmitter power efficiency. In practical circuitry, mixers and amplifiers produce distortion and unwanted signals in a broad range of frequencies which can cause interference to neighboring users and other wireless systems. For this reason a bandpass filter is used to attenuate undesired frequency components and to ensure proper selection of the desired signal to be transmitted. After filtering, a power amplifier is used to boost the signal power level in order to deliver sufficient amount of power to the antenna while achieving maximum attainable power efficiency.

The receiver part of the RF front-end essentially reverses the process undergone in the transmitter. A signal in the form of an electromagnetic wave is received by the receiver antenna, in Figure 1.1 the same antenna is used for both transmission and reception. A low-noise amplifier (LNA) is used to provide power gain while adding the minimum noise power to the RF signal. The bandpass filter is used to suppress undesirable frequency components, particularly at the image frequency, produced after amplification from the LNA. A mixer downconverts the signal to a desired intermediate frequency (IF) with the aid of the local RF oscillator. Bandpass filtering is used again after the mixer to ensure selection of the desired signals while attenuating all other unwanted frequency components. The final stage consists of another

amplification-mixing stage comprised of the IF VGA and the IF mixer which eventually produces a baseband signals ready to be digitized and decoded. The transceiver illustrated in Figure 1.1 operates in a half duplex mode which means that transmit and receive operations do not occur at the same time. It is for this reason that a T/R switch is needed.

The demand for multistandard handheld devices raises the need for flexible and reconfigurable RF front-ends that are controlled by means of software. The Software Radio (SWR) concept is not a novel one [20], and over the years it has grown in scope to encompass many evolving ideas. In fact, it is somewhat difficult to present a comprehensive definition of SWR. However, in the context of realizing transceivers for the next generation of mobile networks, SWR can be defined as an emerging technology which aims at designing multiband, multistandard, reconfigurable RF front-ends that are programmed by software [20]. It is also important to mention that the SWR concept extends beyond the realm of realizing multistandard and multiband transceivers; the ideal SWR is sometimes perceived as a radio device that operates totally in the digital domain, i.e., a radio device with no analog components. This simply implies the idea of migrating the digital signal processing part of the transceiver more and more towards the antenna side. In other words, an ideal SWR would convert the RF signal received from the antenna as early as possible, see Figure 1.2.

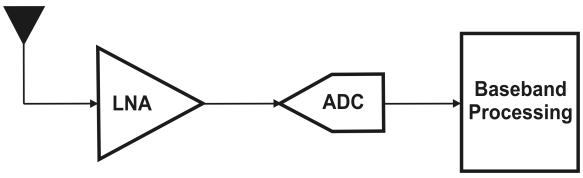

Figure 1.2: Ideal software radio featuring RF amplification, analog to digital conversion, and digital baseband processing.

The main reason for such an approach is that the RF and analog circuitry in transceivers are most of the time the bottleneck in the design process and consume almost 70% of the total power. Nevertheless, the notion of creating a complete digital radio is beyond reach at present due to technological limitations, such as issues pertaining to the required dynamic range and bandwidth of the Analog to Digital converters (ADCs). Simply put, even with state of the art technology, ADCs which can sample a GSM or UMTS signal in the upper MHz and lower GHz range are not realizable with reasonable power consumption in battery operated mobile devices. On the other hand, advances in microelectronic fabrication has made innovative architectures possible and within reach such as single chip phones. The migration to deep sub-micron technologies has enabled the use of standard CMOS technology for RF applications. With transistor gate lengths being scaled down to 0.13-μm and lower, the unity gain frequency of MOS transistors has exceeded the 100 GHz mark, making them very suitable for RF/MW circuit design. Unfortunately, integrated passive components such as inductors and capacitors remain one of the drawbacks of today's IC technologies due to their low quality factors [10].

On-chip inductors have been by far the most prominent challenges of conventional IC technologies. The most commonly used inductor structure is the hallow spiral, which is simply constructed by using metal traces to form a spiral shape. As the size of the metal spiral increases so does the series resistance of the structure due to the skin effect, and thus degrading the quality factor [69]. Another major issue associated with on-chip spiral inductors is the capacitive coupling to the substrate. This capacitance reduces the self resonance frequency of the inductor, and combined with a fairly conductive substrate, limits the frequency range in which the inductor can be used effectively.

Modern IC technologies offer the advantage of having several metal layers. Using spirals of identical structures constructed from different layers and connecting them in a parallel configuration helps reduce the series resistance, since the thickness of the inductor is effectively the sum of all the layers [69]. Using higher layer metals also help reduce the capacitive coupling to the substrate. Moreover, highly doped substrates featured in many modern CMOS technologies contribute to lower eddy current losses and effectively improved inductor quality factors. The combination of all these factors has boosted quality factor numbers from 5 to 20 and higher at frequencies as high as high as 5 GHz [69].

The use of on-chip inductors still remains a matter of a trade-off analysis on the part of the circuit designer. Modern technology and improved layout techniques offer significant improvements, but in many cases designers will

opt to use off-chip inductors due to their superior performance and in the interest of saving space on the silicon wafer. An alternative approach is the use of bond-wire inductors which have lower resistive losses and higher self-resonance frequencies [7]. The use of these types of inductors will be discussed in more detail in later chapters.

In light of the previous discussion we realize the critical need for developing flexible, reconfigurable transceivers which can operate in a diverse environment, and CMOS technology has presented itself as the perfect candidate for such a challenge. As expected, developing multistandard RF front ends implies a considerable amount of new design challenges in transceiver building blocks such as RF filters, low-noise amplifiers, mixers, VCOs, etc. The low-noise amplifier (LNA) is an important building block of modern day transceivers since it has a major role in determining overall receiver sensitivity and noise performance. LNAs intended for cellular applications present a considerable design challenge since they are required to provide sufficient amount of power gain, add minimal noise to the received signal, maintain linear transfer characteristics over a wide dynamic range, and consume a minimal amount of power. This thesis will address the design of a multistandard LNA in a standard CMOS process. Specifically, the proposed LNA will be programmed to operate in four different operational bands for four different standards, namely GSM, IS-95, UMTS, and IEEE 802.11g.

1.3 Objective

This thesis will focus on designing a multistandard and multiband programmable low-noise amplifier in a standard CMOS technology. This programmable LNA will target functionality and performance specifications of devices that are needed in next generation, multistandard software defined transceivers on a single RF CMOS chip. A top level block diagram of the LNA structure is shown in Figure 1.3. The design will comply with four different bands of operation and will incorporate mixed signal design techniques in order to enable band selection by reading a digital code. Embedded in the design process will be the understanding of major RF CMOS integrated circuit design implications and limitation, including analysis of noise behavior in MOSFET devices, the use of bond-wires in tuning/matching, linearity analysis of short channel MOSFETs, and reconfigurable matching networks.

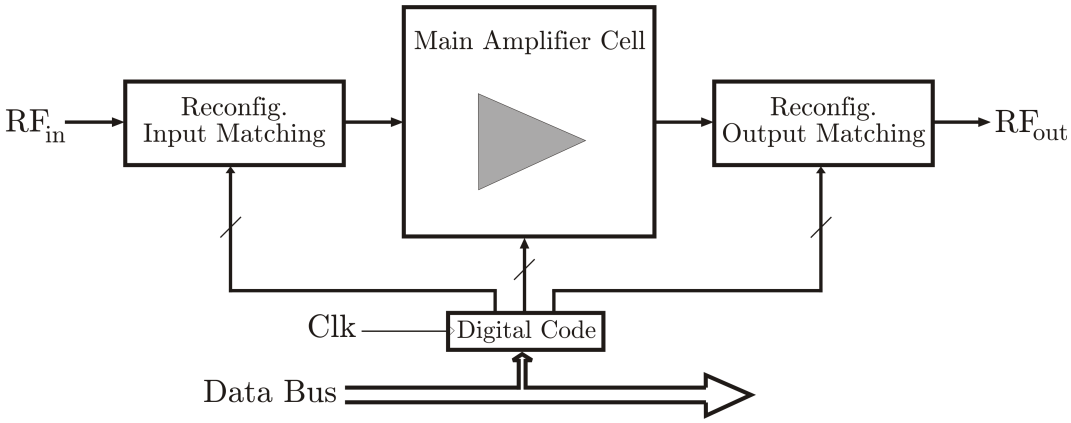

Figure 1.3: Programmable LNA block diagram.

Reconfigurable input matching is used to provide the LNA with flexible

input impedance matching, which should provide suitable power and noise match over the entire frequency band of operation. The main amplifier cell consists of the active devices which provide the small signal gain and buffering operations. Reconfigurable output matching is implemented to provide optimum power transfer over the entire frequency band of operation to the following stage in the receiver chain. The LNA design that will be presented in thesis will target a voltage gain of no less than 20 dB, an input return loss no higher than -10 dB, and a noise figure no higher than 2 dB.

Chapter 2

Background Research

2.1 Introduction

The boom in wireless and mobile communications in the past two decades has spurred an enormous demand for higher performance RF products. From a designer's point of view, this translates into achieving higher performance at lowest cost, which naturally leads to the idea of more and more integration of electronic components on a single die. This is one of the major reasons why RF IC design is a very exciting and growing field of interest nowadays. The push towards integration with the aid of advances in IC technology has revolutionized RF front end design. With the growing complexity of today's mobile communication protocols and standards, the RF transceiver becomes more and more of a design challenge, especially with the growing demand for multimode, software-defined transceivers.

Radio communication can simply be described as a process in which a signal is transmitted and received through the air while maintaining acceptable signal quality. In case of a receiver, for example, the RF circuitry connected to a transducer (usually an antenna) must be able to detect the desired signal, while blocking out all other interfering signals and introducing as little distortion as possible at minimal cost. In many cases, such as cellular networks, desired signal power might be lower than -100 dBm, requiring the receiver to have high sensitivity and also provide very high power gain, anywhere between 120 and 140 dB in order to detect such weak signals [7]. In a wireless environment, especially in urban areas, many interfering and blocking signals coexist alongside a weak desirable signal; this puts stringent selectivity demands on a radio receiver. In many cases receivers have to deal with large signals as well, such a case may occur when a mobile station is operating very near a base station. A receiver is still expected to accurately detect such strong signals without being driven into saturation.

Transmitters have stringent requirements, especially for power amplifiers driving the antenna. Most modern cellular handsets require a transmit power of several hundred milliwatts. This requires the power amplifier to provide 30 dB of power gain or more depending on the cellular phone standard. A power amplifier must achieve such a gain while introducing minimal distortion and keep out-of-band radiation emission as low as possible in order to comply with FCC regulations. Meeting these requirements usually involves high power consumption and/or using very high quality off-chip bandpass filters

prior to the antenna, which also contribute to more power consumption and use of die or PCB space [18].

From this discussion we can see that there are many issues in RF IC design that need to be carefully addressed. This chapter will introduce some of the issues involved in designing reliable and efficient RF ICs such as noise and linearity.

2.2 Noise

Noise can be defined in many different ways depending on context and application. However, generally the term noise refers to anything that is undesired or interfering. In electrical engineering, noise refers to everything besides the desired signal. Noise essentially puts an upper limit on electronic system performance. In the specific case of a radio communication system, noise puts an upper limit on receiver sensitivity and complicates signal detection. Noise can be man-made such as a 60 Hz hum from power lines, or it could be intrinsic in the system itself. Such noise is random in nature and requires statistical characterization [7].

The source of noise in electronic systems was unknown in the beginning and remained a mystery until J.B. Johnson published a paper in 1927 describing noise behavior in conductive materials [31]. This noise is commonly known as thermal noise and is the fundamental source of noise in electronic devices. Other noise mechanisms in electronic devices include so-called shot

noise and *1/f* noise. The following sections will be a brief discussion of several types of noise mechanism in electronics devices and more specifically in MOSFETs.

2.2.1 Thermal Noise

As the name implies, thermal noise is directly related to the thermal properties of materials. J. B. Johnson found that charged particles in a resistor exhibit random motion defined as Brownian motion or random walk at temperatures above 0 K. Thermal noise has a direct dependence on absolute temperature T since the random motion of charged particles is a function of temperature itself. A random current can be directly associated with random movement of charged particles and by Ohm's law we expect to observe a random voltage or noise voltage across open circuit resistors in thermal equilibrium. Indeed, Johnson found that this random voltage depends on temperature, bandwidth, and the resistance of the conducting material as follows [7]

$$\overline{v_n^2} = 4kTR\Delta f \tag{2.1}$$

where k is Boltzmann's constant, T is the absolute temperature in Kelvins, R is the resistor value in Ω, and Δf is the noise bandwidth in Hz. $\overline{v_n}$ is defined as the root mean square (rms) noise voltage. Hence, $\overline{v_n^2}$ by definition would be the total noise power over a given bandwidth Δf. In the context of

low frequency analog engineering, noise is usually measured in units of $\frac{V}{\sqrt{Hz}}$ in which case (2.1) is averaged over the measurement noise bandwidth Δf yielding what is usually referred to as noise spectral density. As an example, a 1 KΩ resistor would have an rms noise spectral density of $\frac{4nV}{\sqrt{Hz}}$ at room temperature. A noisy resistor is modeled as a noiseless resistor R in series with a noise voltage source as shown in Figure 2.1.

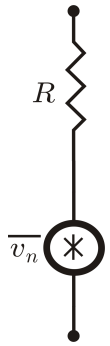

Figure 2.1: Resistor noise model.

In RF engineering, units of power are recorded in decibels. They are typically used since constant reference impedances are deployed throughout the circuit interfaces such as 50 Ω or 75 Ω. Hence, a term known as available noise power is more commonly used when expressing noise in RF/MW systems. The available noise power concept arises from a very common situation in RF/MW engineering where it is important to find the power that is delivered to a certain load by a generator. In the specific case of a noisy resistor, it is simple, yet very essential, to find the noise power delivered to a load, or the available noise power at the load. This situation is depicted in Figure 2.2 where the model of a noisy resistor is loaded with a noiseless

resistor R_{load}.

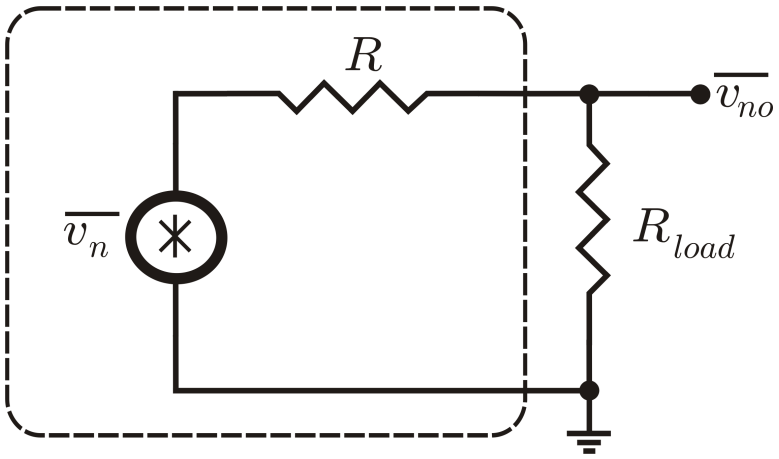

Figure 2.2: Noisy resistor attached to a noiseless load resistor R_{load}.

For simplicity we assumed that the load resistor does not contribute any noise, although in a practical case the load resistor would add noise as well. If we attempt to find the available noise power at the load, we have to realize that this is a simple voltage divider circuit in which case $\overline{v_{no}} = \frac{R_{load}}{R_{load}+R}\overline{v_n}$. For maximum power delivery, a perfect power match is required and this implies $R_{load} = R$. The expression for $\overline{v_{no}}$ simplifies to $\overline{v_{no}} = \frac{1}{2}\overline{v_n}$, and the output noise power is found by

$$P_o = \frac{\left(\frac{1}{2}\overline{v_n}\right)^2}{R} = \frac{\overline{v_n}^2}{4R} = \frac{4kTR\Delta f}{4R} = kT\Delta f \tag{2.2}$$

The previous result proves important in modeling many types of noisy circuits. The most relevant example in our case would be the amount of noise delivered by an antenna to a matched load. Using the same model as the

one shown in Figure 2.2, here the noisy resistor models the antenna and the load resistor models a second component in the RF link such as a filter or an amplifier. If we choose a narrow-band signal, let us say 200 kHz, this means that the amount of noise power in dBm available at the load at T = 290 K is found as follows

$$P_{no} = 1.38\times10^{-23}(J/K)\times290(K)\times200(kHz) = 8.004\times10^{-16}W \approx -121dBm \tag{2.3}$$

which is defined as the noise floor. The noise floor simply indicates the minimum power a 200 kHz signal can have in order to be detected in a perfect, noiseless receiver circuit. This is directly related to the concept of signal to noise ratio (SNR) which is the most prominent means of analyzing communication circuits, and is defined in dB as

$$SNR_{dB} \equiv 10\log_{10}[\frac{SignalPower(W)}{NoisePower(W)}] \tag{2.4}$$

From the previous analysis we can see that the minimum SNR is 0 dB in the case of an ideal noiseless receiver. Modern day digital communication systems require a specific SNR for reliable bit detection. Accuracy of bit detection is expressed using bit error rates (BER) in digital communication theory. BER varies depending on the type of signal (voice or data) and on the type of standard used. For example, a DECT system requires a minimum SNR of about 10 dB for a BER of 10^{-3} for a 700 KHz signal [4]. Using (2.2)

and adding the required SNR we obtain the following noise floor for a DECT system assuming noiseless circuitry

$$Noise\ Floor = 10\log_{10}\frac{1.38\times10^{-23}(J/K)\times290(K)\times700(kHz)}{1mW}+10\approx -106\,dBm \tag{2.5}$$

This indicates that the minimum detectable signal should be at a level no lower than -106 dBm in a noiseless receiver. Unfortunately, noiseless circuits do not exist in practice. This means that the noise performance of a receiver must be analyzed and quantified in order to determine the minimum detectable signal in a communication system. In Section 2.2.4 we analyze the effect of cascading noisy two-port networks on the system's overall noise performance.

2.2.2 Shot Noise

Shot noise was discovered by Walter Schottky in 1918 while conducting experiments on vacuum tubes [71]. Shot noise has similar statistical characteristics as thermal noise since they are both described using a Gaussian distribution (white noise). However, shot noise is generated by a different mechanism. As Schottky discovered, shot noise occurs only when there is a constant (DC) current flow and a potential or energy barrier over which charged particles leap [7]. A good example of where such noise would occur would be a $p-n$

junction. DC current is a continuous flow of charge, so on a microscopic level these charges are described as discrete particles. When these discrete particles reach a boundary where an energy barrier exists (depletion region) they will overcome the energy barrier and thus give rise to a small pulse of current. The total current measured at terminals of the device is a collection of a large number of current pulses. However, charge exhibits random motion as well. Therefore, the time of arrival of each charge to the energy barrier is random and is independent of the time of arrival of any other charged particle [27]. This is what gives rise to the random nature of shot noise. Shot noise cannot exist in linear devices such as resistors since no potential barrier exists. Shot noise current has a mean square value which was formulated by Schottky as [7]

$$\overline{i_n^2} = 2qI\Delta f \tag{2.6}$$

where q denotes the electron charge in C, I is the DC current in A, and Δf is the noise bandwidth in Hz.

2.2.3 Flicker Noise

This type of noise is a phenomenon present in all active devices as well as some passive devices. Flicker noise is a mysterious source of noise since its origin remains a topic of debate and scrutiny among researchers. One explanation for flicker noise is the capturing and releasing of charged particles by traps in

contaminated or defected crystals in integrated circuits [3]. A time constant can be associated with this trap and release process; it has been shown from measurements that a noise signal rising from such mechanism has a density concentrated at low frequencies, and hence the term 1/f noise which indicates that the noise density rises as frequency decreases. As mentioned previously, flicker noise still remains a mystery and for this reason efforts to characterize this type of noise are based on observations and measurements. Consequently, many empirical forms have been introduced which sometimes include several fitting parameters that are deduced by statistical means. In the interest of simplicity, flicker noise can be modeled using the following equation [7]

$$\overline{v_{1/f}} = \frac{K}{f^n}\Delta f \tag{2.7}$$

where $\overline{v_{1/f}}$ is the rms voltage, K is a fitting parameter which is process and device dependent, n is a constant exponent usually close to unity, and Δf is the noise bandwidth. The parameter K has also been shown to depend on bias conditions, i.e., DC current flowing in the device. For this reason, another form that incorporates this is shown in (2.8) [3]

$$\overline{i_{1/f}} = K_1\frac{I^a}{f^b}\Delta f \tag{2.8}$$

where I denotes the DC current, K_1 is a fitting parameter, Δf is the noise bandwidth, and a and b are constant exponents. In some cases flicker noise

can be referred to as excess noise in resistors since this appears to be in excess of thermal noise. Therefore, depending on operating frequency we expect to see certain noise mechanisms dominate more than others. Taking the example of a linear resistor, we expect flicker noise to dominate at low frequency and thermal noise to dominate at higher frequencies. This is illustrated in Figure 2.3 as noise voltage root spectral density of a certain component such as a resistor or a MOSFET.

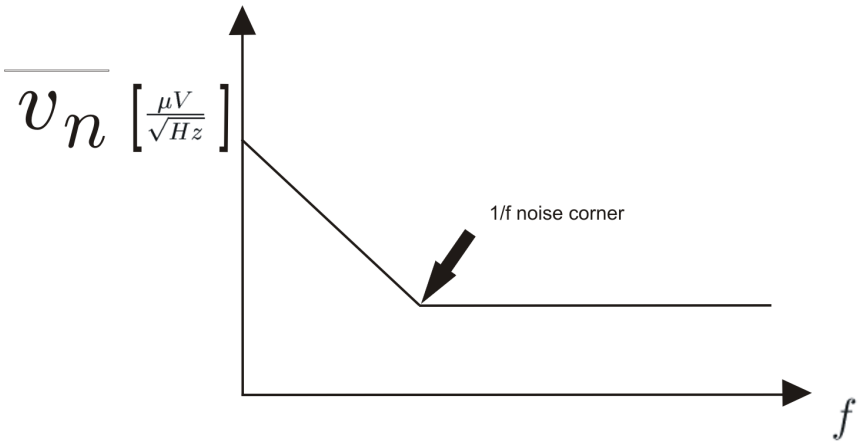

Figure 2.3: Noise spectral density of a device having both thermal and flicker noise.

A common term associated with such a measurement is flicker ($\frac{1}{f}$) noise corner which simply refers to the intersection of the $\frac{1}{f}$ curve and the thermal noise curve. It indicates the point along the frequency scale where the $\frac{1}{f}$ noise starts to dominate. Given the $\frac{1}{f}$ dependence of flicker noise, its amplitude distribution is not Gaussian and cannot be described as white noise; in fact flicker noise is sometimes referred to as pink noise since it has a large low

frequency content [5].

2.2.4 Noise Factor of Cascaded Networks

The goal of this analysis is to quantify the effect of the noise power from a generator's source resistance on the overall noise power at the output of an RF transceiver system. We first start by analyzing a single two-port network as the one shown in Figure 2.4. From this we express the total noise factor of the network as

$$F_j = \frac{N_{out}}{N_{in}} = \frac{G_j N_{in} + N_j}{G_j N_{in}} = 1 + \frac{N_j}{G_j N_{in}} \tag{2.9}$$

where N_j is the internally generated noise power by the network j and G_j is the network gain. We can relate the noise factor to N_j as

$$F_j - 1 = \frac{N_j}{G_j N_{in}} \tag{2.10}$$

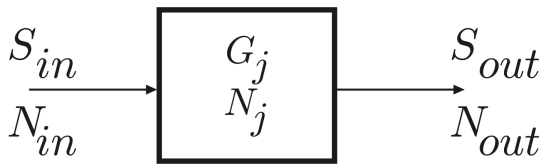

Figure 2.4: Single noisy two-port network j with gain G_j and internally generated noise power N_j.

We next consider a system of multiple cascaded networks, say three, as shown in Figure 2.5. Without loss of generality, the noise factor in this case

is expressed as the ratio of overall output noise power to the output noise power due to the source resistance as follows

$$F_{total} = \frac{N_{out3}}{N_{out3(source)}} \tag{2.11}$$

We can write the overall noise power, N_{out3}, at the output for the three-block configuration as

$$\begin{aligned} N_{out3} &= G_3(G_2(G_1N_{in} + N_1) + N_2) + N_3 \\ &G_3G_2G_1N_{in} + G_3G_2N_1 + G_3N_2 + N_3 \end{aligned} \tag{2.12}$$

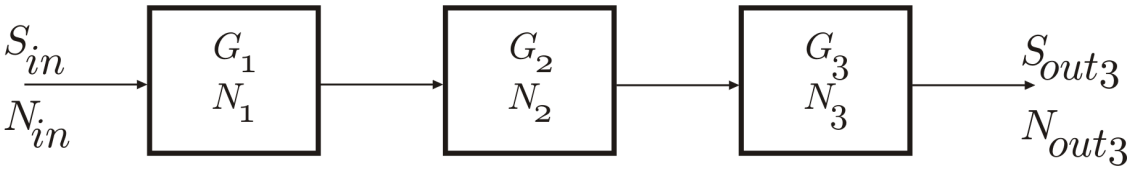

Figure 2.5: Cascade of three noisy two-port networks.

The noise power at the output due to the source resistance is: $N_{out3(source)} = G_1G_2G_3N_{in}$. Inserting this expression along with (2.12) in (2.11), we obtain

$$F_{total} = 1 + \frac{N_1}{G_1N_{in}} + \frac{N_2}{G_1G_2N_{in}} + \frac{N_3}{G_1G_2G_3} \tag{2.13}$$

Using the result in (2.10), we can rewrite (2.13) as

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} \tag{2.14}$$

This result can be generalized for k networks by writing the total noise power at the output, and the total noise power at the output due to the source resistance of the kth stage is given by

$$N_{out(total_k)} = (G_1...G_k)N_{in} + (G_2...G_k)N_1 + (G_3...G_k)N_2 + ... + G_kN_{k-1} + N_k \tag{2.15}$$

$$N_{out(source_k)} = G_1...G_kN_{in} \tag{2.16}$$

Using (2.11) and (2.10) we can write the generalized noise factor for k networks as

$$F_{total(k)} = 1 + \frac{F_1 - 1}{G_1} + \frac{F_2 - 1}{G_1G_2} + ... + \frac{F_{k-1}}{G_1...G_{k-2}} + \frac{F_k}{G_1...G_{k-1}} \tag{2.17}$$

From the previous analysis we can see the importance of having a first stage which provides sufficient gain and, more importantly, has a relatively low noise factor. This is the reason why LNAs are most of the time used as the first component in a receiver chain. The expression in (2.17) was obtained assuming all stages have the same input and output resistance. The result can be extended for cases where this is not a valid assumption [26]

2.2.5 Noise in MOSFETs

Analysis of noise in MOSFETs is essential, especially in the context of designing low noise CMOS circuits. Noise mechanisms in MOS transistors are similar in nature to other active devices such as bipolar transistors. Since FETs are essentially voltage controlled resistors, we expect thermal noise to exist in the observed drain current. Van der Ziel was the first to analytically formulate drain thermal noise current in MOSFETs and his work resulted in a simple expression for drain noise current spectral density as follows [31]

$$\overline{i_{nd}^2} = \gamma 4kTg_{d0} \triangle f \tag{2.18}$$

where γ is a bias dependent parameter and g_{d0} is the drain-source conductance at zero V_{DS}. Based on the fact that the gate terminal of a MOSFET is coupled to the channel via the oxide capacitance and at high frequencies the gate impedance becomes small, drain noise current induces a gate noise current given by the following [32]

$$\overline{i_{ng}^2} = \delta 4kTR_{gs}\omega^2 C_{gs}^2 \Delta f \tag{2.19}$$

where δ is another bias dependent parameter, similar to γ used in (2.18), R_{gs} is the gate series resistance, and C_{gs} is the gate-source capacitance. More simplified forms of the gate noise are usually presented where the term $(R_{gs}\omega^2 C_{gs}^2)$ is lumped into a single parameter g_g. Hence, (2.19) becomes

$$\overline{i_{ng}^2} = \delta 4kTg_g\Delta f \tag{2.20}$$

It is important to note that both drain and gate noise currents described in equations (2.18) and (2.20) arise from the same source, which is the random thermal charge motion in the channel [12]. In a statistical sense this implies that the gate and drain noise currents are correlated with a correlation factor usually denoted by C; it is defined as

$$C \equiv \frac{\overline{i_{ng}i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}.\overline{i_{nd}^2}}} \tag{2.21}$$

where $(*)$ denotes the complex conjugate operation.

The equations presented above model the thermal noise behavior in MOS transistors. Other noise mechanisms exist in MOS devices such as flicker noise and shot noise. As described in Section 2.2.3, flicker noise is a dominant source of overall device noise at low frequencies, and thus will not be considered here since we are only interested in the high frequency noise behavior of the MOS transistor (it has been shown that thermal noise is dominant at such frequencies). Also shot noise will not be considered since MOS transistors do not exhibit such kind of a noise mechanism when biased in saturation, which is the bias condition commonly used for MOS transistors in RF amplifier design.

The bias dependent parameters, γ and δ, have been well documented for long channel devices. Van der Ziel found that γ is unity at $V_{DS} = 0$ and

decreases to about 2/3 in saturation. The parameter δ has a value of approximately twice that of γ (4/3) for long channel devices [7]. As technology has advanced and device size has continued to scale down into the submicron regime, early research efforts, such as [58] and [59], reported significant enhancement of drain thermal noise and induced gate noise in submicron MOSFETs. The enhancement factors of drain and gate noise in submicron devices are usually related to long channel devices via the γ and δ parameters. In the case of drain noise current, γ was found to be 12 times larger than the classical long channel value for an n-channel device of 0.7-μm of gate length in [58]. An enhancement factor of 30 was reported for induced gate noise in devices with 0.25-μm gate length [17]. Numerous models were developed to explain the dramatic increase in channel thermal noise and induced gate noise, most of which invoke the effect of hot electrons in the device's conducting channel and non-quasi static effects. Other research efforts [13] have shown that the main contributor to the increase in channel thermal noise in short channel devices is the velocity saturation and mobility degradation of charge carriers in the channel due to the effect of high electric fields in short channel devices. The noise enhancement factors reported in [12] were no more than 3 or 4 times the classical long channel values; this shows significant contrast to earlier values as reported in [58] and [17]. A combined approach was taken in [11] where the device noise model included both velocity saturation and hot electron effects, and results also show moderate enhancement of channel thermal noise and induced gate noise.

In general, noise modeling of short channel devices shows several inconsistencies which could be attributed to many factors, but it is mainly due to the inconsistencies that arise from numerous and somewhat contrasting mobility and channel conductivity models, which include the effects of high electric fields on charge carriers in the conducting channel of a FET device. The notion of hot electrons and electron temperature has been a source of confusion as well. In an effort to shed more light on this matter, in the following section we will describe three different techniques that are widely used in noise modeling in semiconductor devices in general, and MOSFETs in particular. We will briefly discuss the major differences between all three.

2.2.6 Noise Modeling Methodologies

The study and characterization of noise from a circuit designer's point of view mainly involves the description of certain devices such as a transistor by means of classical two-port noise theory. Here devices and circuits are characterized by equivalent noise sources such as voltages and currents. Using the classical two-port noise theory and the equivalent noise sources, a designer can then analyze a device or circuit and predict the noise performance between the input and output ports of the network. The treatment of this topic will be handled later in this chapter. In this section we provide a brief treatment of noise at the microscopic level where its characteristics are related to device-intrinsic parameters. Studying and modeling a device's noise behavior at such a scale is essential for designing efficient low-noise high

frequency circuits.

Noise analysis techniques can be divided into two categories: a) an equivalent circuit approach and b) a physics based approach. An equivalent circuit based approach simply models the device's noise behavior by using lumped two port elements such as resistors, capacitors, and inductors which connect the input and output ports of the device [30]. Of course, in the case of an active device, nonlinear and bias dependent elements need to be added to the model in order to accurately describe the small signal characteristics between input and output. A physics based approach to noise modeling is deeply involved in describing the device behavior at the microscopic level. Using such an approach produces either microscopic variables like electron transport, carrier velocity, charge distributions, or external variables such as voltages and currents [29]. The latter is more relevant and more beneficial since it facilitates the extraction of compact noise modeling parameters used circuit simulators. Physical modeling relies on the evaluation of Boltzmann's equation describing charge distribution in a non-equilibrium state in conjunction with Poisson's equation relating charge to the electric field [29]. Details of the evaluation of Boltzmann's equation is beyond the scope of this thesis and can can found in several references, including [29]. Several methods have been developed for compact noise modeling in solid state devices, and for MOSFETs we can identify the following [14]

1. Klaassen-Prins method

2. Equivalent circuit method, and

3. Impedance field method

The following is a brief discussion of each method.

2.2.6.1 Klaassen-Prins Model

The Klaassen-Prins approach is utilized by many to describe noise in semiconductor devices, including Van der Ziel [31]. The procedure of obtaining the general Klaassen-Prins equation for drain thermal noise current for long channel FETs will be briefly described here based on derivation steps developed in [31] and [13].

The current in a semiconductor device can be described using the the nonquasi-static one-dimensional as follows

$$I = g\frac{dV}{dx} \tag{2.22}$$

where g is the conductivity and $V(x)$ is the voltage or potential at a certain point x along the channel. The reader is referred to [3, App. J] for the details on the derivation of (2.22). Equation (2.22) can be used to model the drain current in an n-channel MOSFET. In the presence of thermal agitation, charges will undergo random motion as they travel across the channel; this is seen at the terminals of the device as minor fluctuations around the drain DC current level. We can model the drain current with a DC component I_D and a small signal component i_d representing fluctuations due to thermal

noise. The noise current source in a FET channel must also be modeled, which is usually done by using a Langevin equation with current source $i_n(x)$, having a zero ensemble average [13]. The Langevin equation is a stochastic differential equation describing Brownian motion of particles [72]. It is essential to remember that random motion of charges will perturb the channel potential, this is expressed by a small signal noise voltage term, $v_n(x)$, added to the DC channel potential $V(x)$ and the channel conductance term (g) in (2.21), since it is a function of the channel potential. Adding the small signal component $v_n(x)$ and the Langevin noise component to (2.22) results in

$$I_D + i_d = g(V(x) + v_n(x))\frac{d(V(x) + v_n(x))}{dx} + i_n(x) \tag{2.23}$$

Since we are interested in the noise component of the drain current, only small signal components of equation (2.23) are kept, and the resulting expression for i_d is integrated over the length of the channel, i.e. L. Using the boundary conditions: $v(0) = v(L) = 0$, we obtain

$$i_d = \frac{1}{L}\int_0^L i_n(x)dx \tag{2.24}$$

By definition, the spectral density of a random process with zero time or ensemble average is given by $S_{id} \equiv \frac{\overline{i_d i_d^*}}{\Delta f}$. Using this definition for S_{id} and (2.24) the drain noise current spectral density is

$$S_{id} = \frac{1}{L^2} \int_0^L \int_0^L \overline{i_n(x) i_n^*(x')} dx dx' \tag{2.25}$$

At this point an assumption can be made regarding the nature of the noise source $i_n(x)$. The classical Klaassen-Prins equation was derived using a thermal noise source where the noise density of a section Δx of the FET's channel; it is given by [31]

$$S_n = \frac{4kTg(x)}{\Delta x} \tag{2.26}$$

As $\Delta x \to 0$ in (2.26) we can approximate the discontinuity by a Dirac delta function in the form

$$S_n = 4kTg(x)\delta(x - x') \tag{2.27}$$

Consequently

$$\overline{i_n(x) i_n^*(x')} = 4kTg(x)\Delta f \delta(x - x') \tag{2.28}$$

where δ is the Dirac delta function, not to be confused with the bias dependent parameter of gate noise current in (2.19). Substituting (2.28) into (2.25) and using (2.22) to switch the variable to V instead of x results in the classical Klaassen-Prins equation [12]

$$S_{id} = \frac{4kT}{I_D L^2} \int_{V_0}^{V_L} g^2(V) dV \tag{2.29}$$

If (2.22) is solved for the current term, I, or I_D in the case of drain current of a FET, the general expression for DC drain current is obtained

$$I_D = \frac{1}{L}\int_{V_0}^{V_d} g(V)dV \tag{2.30}$$

Substituting (2.30) into (2.29) and introducing the term g_0, defined as the conductance per unit length at the source, the drain current spectral density becomes [60]

$$S_{id} = \frac{4kTg_0}{L}\frac{\int_{V_0}^{V_D}(\frac{g(V)}{g_0})^2 dV}{\int_{V_0}^{Vd}(\frac{g(V)}{g_0})dV} = \gamma 4kTg_{d0} \tag{2.31}$$

where g_{d0} has already been introduced in (2.18) and is defined as [31]

$$g_{d0} = \frac{g_0}{L} \tag{2.32}$$

From the previous derivation we can see how the Klaassen-Prins equation was simplified by Van der Ziel in order to obtain an analytical, closed form equation for drain noise current formulated in (2.20) and (2.18).

The Klaassen-Prins equation is a simple, but powerful, equation which is used widely in compact MOSFET noise modeling today. The original form of (2.29) has undergone several modifications in an effort to extend its use to submicron devices, for which channel length modulation and the dependence of charge mobility and channel conductivity on the electric field must be included for accurate modeling. Inclusion of channel length modulation

effect (CLM) is adopted in [61] using the channel segmentation model, which divides the conducting channel into two parts: the gradual channel region and the pinch-off region, as shown in Figure 2.6 where L_{eff} is the effective length of the channel, L_{elec} is the electric length of the channel (which is also the length of the gradual channel region), and $\triangle L$ is the length of the pinch-off region.

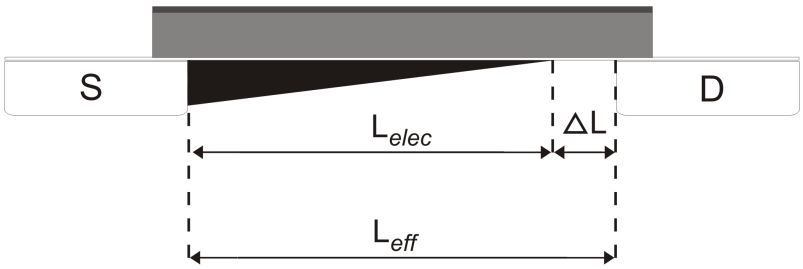

Figure 2.6: NMOS cross sectional view.

It has been shown that the noise contribution from the pinch-off region of the channel is negligible [61]. This assumption is widely accepted and used in [12], [16], and [14]. Building on this, velocity saturation of charge carriers in the presence of strong electric fields is incorporated into the formulation of channel conductivity by [13]. This results in a new DC current differential equation similar to (2.22) in the form

$$I_D = \frac{g_0(V)}{[1 + (\frac{\mu_0}{v_{sat}} \frac{d\psi}{dx})^p]^{-\frac{1}{p}}} \frac{dV}{dx} \tag{2.33}$$

where $g_0(V)$ is the conductivity neglecting velocity saturation, μ_0 is the zero-field mobility, p is a power value of 2 for NMOS devices, v_{sat} is the saturation

velocity, and ψ is the electrostatic potential at the surface (consequently $\frac{d\psi}{dx}$ denotes the electric field). In [13] proper steps are taken from this point in order to obtain the modified Klassen-Prins equation where the final result for drain noise current spectral density is given by

$$S_{I_D} = \frac{4kT}{I_D L_{vsat}^2} \int_{V_0}^{V_L} g_c^2 dV \tag{2.34}$$

where g_c denotes the corrected channel conductivity taking into account velocity saturation, and L_{vsat} is the length corresponding to corrections on the position x due to velocity saturation as well. Finding an expression for the induced gate noise follows the same steps which were taken in [29] in order to obtain (2.19). The key step in this process is to model the MOSFET as a distributed RC network in which the distributed resistance models the conducting channel and the distributed capacitance models the gate oxide coupling to the gate. A general expression used to calculate gate noise current is given by [13]

$$i_G = -j\omega W \int_0^L C_{gc}(x) v(x) dx \tag{2.35}$$

where $v(x)$ is the distributed voltage across the channel, C_{gc} is the local gate to channel capacitance, and W is the channel width. The final expression for gate noise current and the correlation coefficient defined in (2.21) can be found in [13].

The result obtained in (2.34) is a generalization to the classical Klaassen-

Prins equation in (2.29), in which the channel conductivity was corrected to include dependencies on voltage as well as position along the channel, and finally velocity saturation and CLM effects were included. In the next section the impedance field method will be briefly introduced and discussed.

2.2.6.2 Impedance Field Method

The impedance field method is similar to the Klaassen-Prins approach where the MOSFET is also regarded as a distributed RC network and Langevin stochastic sources are used in order to model the local noise sources in small channel segments. The Langevin noise sources, δi_n, are slightly modified and are modeled as one component injecting current in a noiseless channel segment between x and $x + \Delta x$, and another component drawing current from the noiseless channel segment as shown in Figure 2.7. Currents i_g and i_d denote the short circuit gate and drain currents resulting from the local microscopic noise source δi_n [62].

The noise transfer from the microscopic level, δi_n, to the device terminals, $i_{d(g)}$, is calculated using the vector impedance field term denoted as $\Delta A_{d(g)} \equiv [A_{d(g)}(x) - A_{d(g)}(x + \Delta x)] = dA_{d(g)}(x)/dx$ and the resulting terminal noise current for gate or channel can be found by [14]

$$i_{d(g)}(t) = \int_0^L \frac{dA_{d(g)}(x)}{dx} \delta i_n(x,t) dx \tag{2.36}$$

This shows that the terminal noise current is found by simply adding the

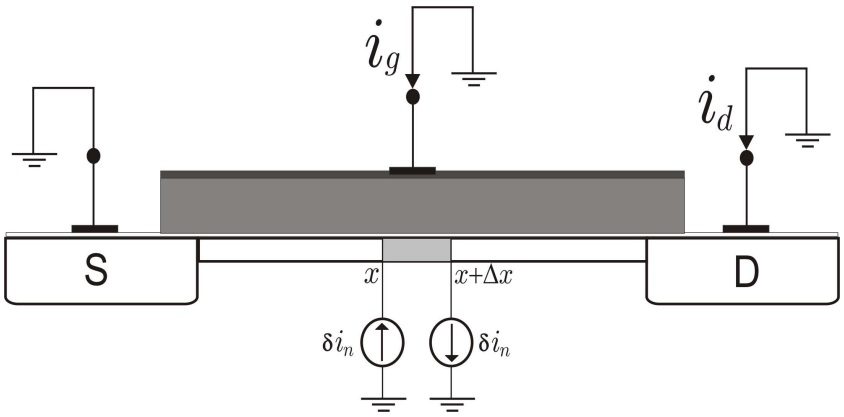

Figure 2.7: Illustration of impedance field method applied to an N-channel device.

noise contributions of all the small segments as shown in Figure 2.7. The general equation in (2.36) requires some modifications in order to account for velocity saturation and CLM effects. Similar to the generalized Klaassen-Prins method described in the previous section, the noise from the pinch-off region of the channel is assumed to be negligible. Therefore, (2.36) is integrated over the electric length of the channel, L_{elec}. The microscopic noise source used in this case is given by the diffusion noise [31]

$$\delta i_n^2 = 4q^2 D_n n(x) \frac{W}{\Delta x} \Delta f \tag{2.37}$$

where q is the charge carrier, $n(x)$ is the electron concentration , and D_n is the electron diffusion coefficient given by the Einstein relation in thermal equilibrium as

$$D_n = \frac{kT}{q}\mu_n \tag{2.38}$$

where μ_n is the electron mobility. Einstein's relation holds only in situations where thermal equilibrium exists. If this is the case, then inserting (2.38) into (2.37) simply produces the thermal noise current equation for a resistor. This implies that thermal noise in semiconductors is a special case of diffusion noise in which thermal equilibrium conditions are assumed. Following the derivation steps outlined in [11], the differential DC drain current equation is used, including mobility degradation effect as

$$I_D = g_0(V)\frac{\frac{dV}{dx}}{1+\frac{\frac{dV}{dx}}{E_c}} \tag{2.39}$$

where E_c is the critical electric field at which carrier velocity saturates, $g_0(V) = \mu_{eff}WC_{ox}(V_{od} - \alpha V)$, α accounts for bulk charge effects, V_{od} is the gate overdrive voltage, C_{ox} is the gate oxide capacitance per unit area, and μ_{eff} is the effective mobility of charge carriers. Using (2.39) the impedance field is formulated with the aid of circuit analysis on the small channel segment between x and Δx as shown in Figure 2.7. Using the formulated impedance field, the noise contribution of all the segments are summed to find the total drain noise current as described mathematically in (2.36), with the assumption that the noise contributions of all the small segments are uncorrelated. A key assumption made in [11] is that the diffusion coefficient D_n is constant along the gradual channel, the justification being that the

decrease of carrier mobility due to high electric fields is compensated by the increase in electron temperature. The diffusivity equation is only modified to incorporate mobility degradation effects where the term μ_n is replaced by μ_{eff}. The final equation for drain noise current spectral density is found as [11]

$$S_{id} = \frac{4kT}{I_D L_{elec}^2 (1 + \frac{V_{DS}}{L_{elec} E_c})^2} \int_0^{V_{DS}} g_0^2(V)(1 + \frac{E}{E_c}) dV \tag{2.40}$$

which shows similarities to the classical and modified Klaasen-Prins equations in (2.29) and (2.34), respectively. The procedure of finding the induced gate noise current follows directly from (2.35).

2.2.6.3 Equivalent Circuit Method

A circuit based approach models the distributed channel using lumped components: a differential resistance Δr, and two channel conductances g_s and g_d looking toward the source and drain terminals as shown in Figure 2.8.

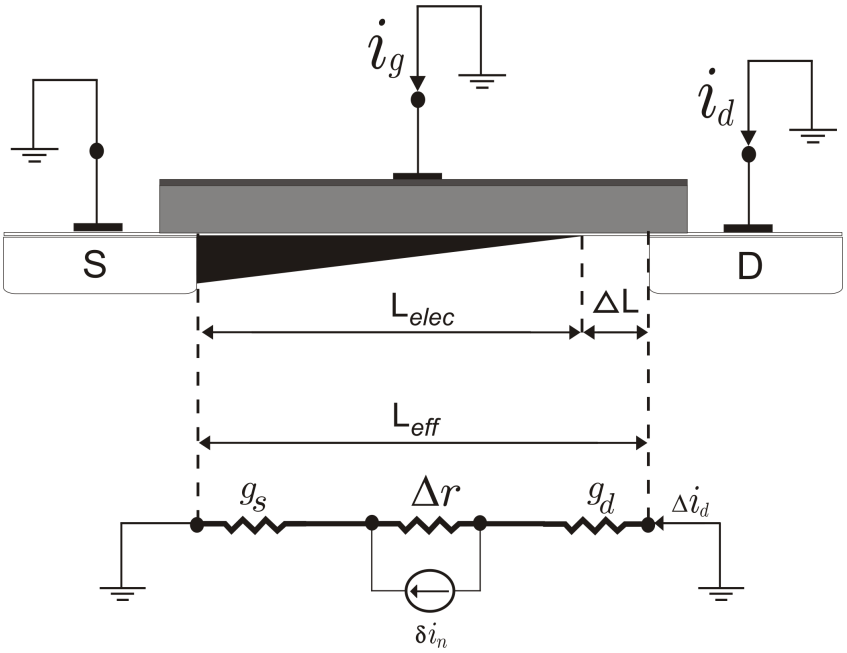

Figure 2.8: Equivalent circuit approach.

Based on this type of model, the terminal response to the fundamental noise source δi_n in spectral density form is [15]

$$S_{\Delta i_d^2} = S_{\delta i_n^2} \Delta r^2 g_{eq}^2 \tag{2.41}$$

where

$$\frac{1}{g_{eq}} \equiv \frac{1}{g_s} + \frac{1}{g_d} \tag{2.42}$$

Obtaining $S_{\Delta i_d^2}$ requires the calculation of all three terms in (2.41). The procedure is found in [14]. What is most significant is the formulation of the $S_{\delta i_n^2}$ term. The channel segment between x and $x + \Delta x$ is not assumed to be

in equilibrium due to the presence of the electric field. Therefore, Einstein's relation cannot be used. Similar to the impedance field method adopted by [11] in the previous section, Einstein's relation is modified so that it can be used for non-equilibrium conditions as follows

$$D_n = \frac{kT_n}{q}\mu_{diff} \tag{2.43}$$

where μ_{diff} denotes the differential mobility which is defined as $\mu_{diff} = \frac{dv}{dE}$, v is the electron velocity, and T_n is the noise temperature which is eventually shown to be equal to the carrier temperature, T_c, in situations specific to MOSFET device operations. Also, the carrier temperature is different from the lattice temperature, T_L. Since it is more convenient to use lattice temperature, an approximate closed form relation between carrier and lattice temperature is used, which is consistent with the field dependent carrier mobility. Under these assumptions the power spectral density of the microscopic noise source is found as [15]

$$S_{\delta i_n^2} = 4kT_L\Delta g(\frac{\mu_0}{\mu_{eff}})^2 \tag{2.44}$$

With the assumption that the microscopic noise sources are uncorrelated, the total drain noise current power spectral density, denoted as $S_{I_d^2}$ in [15], is found by integrating over the effective channel length. The gate induced noise current is found using the same approach as employed by the other two noise modeling methods. It is important to realize that the carrier heating

effect is taken into account. This is in contrast to [11] where increase in carrier temperature was considered to be balanced by the decrease in carrier mobility. Carrier heating effects were not considered in the formulation of the generalized Klaassen-Prins equation by [13]. The definition of diffusivity and its relation to the carrier mobility in the channel is similar in all three methods presented, the difference occurs in the modeling of mobility and conductance and their dependence on the electric field. This in turn translates into differences in the fundamental or microscopic noise models.

The three methods calculate drain noise current by applying different techniques to model the distributed MOSFET channel. In principle, the Klaassen-Prins derivation utilizes the Langevin method in which a macroscopic differential equation describing the transfer characteristics of the system is used and a random source function is added to describe the random fluctuations of the noise sources [31]. Boundary conditions are then used to obtain drain and gate noise currents. The impedance field method breaks down the distributed channel into small noiseless segments with two microscopic noise current sources drawing from and injecting current into the channel segment. A channel segment between x_1 and $x_1 + \Delta x$ is unaffected by the presence of a noise source in an adjacent channel segment between x_2 and $x_2 + \Delta x$. This assumption allows the use of superposition in order to find the total drain noise current.

The equivalent circuit approach lumps the entire channel into one resistance, including a microscopic noise source, and a drain and source conduc-

tance. The noise transfer to the device terminals is found using linear circuit techniques [15]. These noise modeling methods described seem to have a great degree of similarity. Indeed, a generalization of all three methods was performed in [14] where it was shown that all three methods eventually produce the same integral equations for drain noise current and induced gate noise current. The generality of these forms proves to be very useful since they were derived assuming an arbitrary mobility and microscopic noise source models.

As mentioned previously, these noise modeling methodologies have been developed for use in compact transistor modeling for use in circuit simulators. Several MOSFET models have been developed and are used as an industry standard, such as the Berkeley Short-Channel IGFET Model (BSIM), developed by the BSIM Research Group at UC Berkeley. The BSIM3 has been widely adopted and used by many corporations since its release in 1995. The third version of the BSIM3, namely the BSIM3v3 model, is the model that will be used throughout all circuit simulations that will be presented in this work.

Later extension of the BSIM3v3 model, such as the BSIM3v3.2.4, model the drain thermal noise current as follows [65]

$$S_{id} = \frac{4kT\mu_{eff}}{L_{eff}^2 + \mu_{eff}|Q_{inv}|R_{ds}}|Q_{inv}| \tag{2.45}$$

where Q_{inv} is the inversion layer charge and R_{ds} is the drain to source resis-

tance. In [16], a similar expression for the drain noise current was found by simplifying the drain noise current expression in (2.40) as

$$S_{id} = 4kT\frac{\mu_{eff}}{L_{elec}^2}Q_{inv} \tag{2.46}$$

which is similar to (2.45). It was shown in [11] that (2.46), albeit originally developed for long channel devices, is still valid in the submicron regime. The BSIM3v3 model incorporates the effects of the drain to source resistance, R_{ds}, whereas (2.46) uses the electric length of the channel instead of the effective length. The effective mobility, μ_{eff}, in (2.45) and (2.46) does not take into account the degradation due to the lateral electric field [11]. Nevertheless, the simple expression in (2.46) was shown in [11] to be practically accurate even in short channel devices, with deviations from (2.40) of less than 5% for channel lengths down to 0.18 μm.

Induced gate noise is not modeled in the BSIM3v3.2.4 model. Many publications, such as [39], have addressed this issue by introducing lumped component extensions, namely a gate resistance which is used to model the induced gate thermal noise and the non-quasi-static effects of the distributed channel. Induced gate noise tends to dominate the overall measured noise at high frequencies [62]. Flicker noise dominates the observed noise at low frequencies, whereas observed noise at mid-range frequencies is dominated by the channel thermal noise. The mid-range to high frequency break-point is usually assumed to be around one tenth of f_t [17], [62]. With a 0.13 μm

CMOS process, which will be assumed throughout this work, f_t exceeds 100 GHz. Assuming a long-channel device operating in the saturation region, f_t is approximated as [7]

$$f_t \approx \frac{3}{2}\frac{\mu_n(V_{gs} - V_t)}{L^2} \tag{2.47}$$

From (2.47) we can see that $f_t \propto \frac{1}{L^2}$, indicating that technology scaling has the effect of increasing f_t. The highest frequency targeted in this work will be below 3 GHz. Hence, it is fair to assume that the lack of an induced gate noise formulation in the BSIM3v3.2.4 model will not have a significant effect on the accuracy of noise figure simulations.

From this discussion, we can conclude that the noise model provided by BSIM3v3.2.4 is sufficient in describing the overall noise behavior for the purpose of designing RF CMOS LNAs in the frequency range between 800 MHz and 3 GHz.

2.2.7 Noise Theory in Two-Port Networks

Noise in circuits is usually represented by an input noise voltage, v_n, and an input noise current, i_n, as shown in Figure 2.9. For convenience, the noisy signal source is drawn in a Norton equivalent form using a current, i_s, and an admittance Y_s. The goals of this analysis is to show how the noisy two-port network affects the input SNR by finding an expression for the noise factor, and to show what effect the source admittance has on the overall noise

performance of the network.

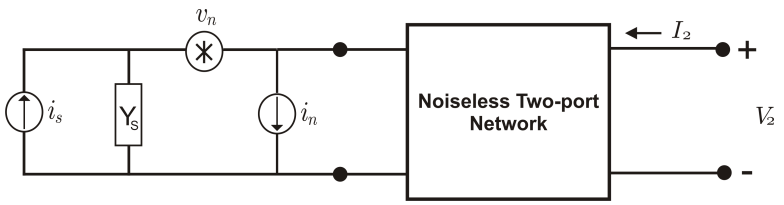

Figure 2.9: Representation of noise in two-port networks.

The short circuit rms current, i_{sc}, at the input ports of the network is given by [66]

$$\overline{i_{sc}^2} = \overline{i_s^2} + \overline{|i_n + Y_s v_n|^2} \tag{2.48}$$

The noise factor is found by taking the ratio of total noise power at the output to the noise power available from the signal source which yields the following

$$F = \frac{\overline{i_s^2} + \overline{|i_n + Y_s v_n|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{|i_n + Y_s v_n|^2}}{\overline{i_s^2}} \tag{2.49}$$

It is important to realize that the input noise current and input noise voltage are very likely to be correlated since they both arise from the same noise mechanisms in the network. We can therefore express i_n as the sum of two current components, one that is correlated with the noise voltage and one that is uncorrelated. Thus, we can write i_n as $i_c + i_u$ denoting the correlated (i_c) and uncorrelated (i_u) currents, respectively. The correlated current can be related to v_n by a correlation admittance Y_c where $i_c = Y_c v_n$. Inserting

this into (2.49) along with i_n and i_u and rearranging the expression yields

$$F = 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \overline{v_n^2}}{\overline{i_s^2}} \tag{2.50}$$

The independent noise sources in (2.50) can be expressed as thermal noise sources produced by an equivalent noise resistance or conductance. We can thus write

$$\overline{i_u^2} = 4kT\Delta f G_U \tag{2.51}$$

$$\overline{v_n^2} = 4kT\Delta f R_n \tag{2.52}$$

$$\overline{i_s^2} = 4kT\Delta f G_S \tag{2.53}$$

where G_U is an equivalent noise conductance, R_n is the equivalent noise resistance, and G_s is the real part of the source admittance. Using these expressions and representing the admittances as $G_c + jB_c$ and $G_s + jB_s$, respectively, (2.50) can be rewritten as follows

$$F = 1 + \frac{G_U}{G_S} + \frac{R_n}{G_S}[(G_C + G_S)^2 + (B_C + B_S)^2] \tag{2.54}$$

The noise factor expressed in (2.54) contains terms which are not of practical use to a circuit designer. However it does provide insight into the optimum noise performance of a particular two port network in terms of source and

correlation admittances. In order to find the minimum noise factor we first eliminate the imaginary part by setting $B_S = -B_C$. Minimizing F with respect to G_S we obtain the expression for the optimal source conductance

$$G_{Sopt} = \sqrt{\frac{G_U}{R_n} + G_C^2} \tag{2.55}$$

As a result, an expression for the minimum noise factor, F_{min}, can be given by

$$F_{min} = 1 + \frac{G_U}{G_{Sopt}} + \frac{R_n}{G_{Sopt}}(G_C + G_{Sopt})^2 \tag{2.56}$$

Solving (2.55) for G_U yields: $G_U = R_n(G_{Sopt}^2 - G_C^2)$. Inserting this expression for G_U in (2.56) results in

$$F_{min} = 1 + 2R_n(G_C + G_{Sopt}) \tag{2.57}$$

It is of practical importance to obtain a noise factor expression which describes the noise performance of the circuit in relation to measurable circuit parameters, such as device dimensions, transcondutance, and gate oxide capacitance. To obtain this, the expression for G_U and (2.57) can be used in (2.54). We will assume that the optimum noise match is obtained, $(B_C = -B_{Sopt})$, which results in the following

$$F = F_{min} + \frac{R_n}{G_S}[(G_S - G_{Sopt})^2 + (B_S - B_{Sopt})^2] \tag{2.58}$$

To obtain more practical use of (2.58), the expression is further manipulated to obtain a circle equation. This procedure can be found in [2]. The resulting equation describes a collection of circles which can be plotted on the Smith Chart. This enables the circuit designer to choose the source reflection coefficient, Γ_s, to affect the noise factor. These circles uniquely target a single frequency and a certain bias condition in the case of an active device such as a transistor. In general, the noise figure is used more often since it is measured in dB.

The expression in (2.58) provides the basis for noise analysis of a specific device in terms of the so-called four noise parameters: F_{min}, R_n, G_{Sopt}, and B_{Sopt}. Since these noise parameters have been derived for any two-port network, it is essential to obtain analytical expressions for each noise parameter. In the case of a MOSFET, this process starts by finding the equivalent input referred noise voltage and current in order to use the classical two-port noise theory summarized above. The goal is to find simple analytical expressions for the four noise parameters in terms of intrinsic MOSFET device parameters. The complete derivation of these parameters is rigorous and beyond the scope of this background section, details can be found in [62] and [7] where the noise parameters are listed as

$$NF_{min} \approx 1 + \frac{\omega}{\omega_T}\sqrt{\gamma\delta\zeta(1-|C|^2)} \tag{2.59}$$

$$R_n \approx \frac{\gamma g_{d0}}{g_m^2} \tag{2.60}$$

$$G_{Sopt} \approx \frac{g_m \omega C_{gs}}{g_{d0}} \sqrt{\frac{\delta\zeta(1-|C|^2)}{\gamma}} \tag{2.61}$$

$$B_{Sopt} \approx -\omega C_{gs}(1+|C|\frac{g_m}{g_{d0}}\sqrt{\frac{\delta\zeta}{\gamma}}) \tag{2.62}$$

Here ω_T is the unity gain angular frequency, g_m is the small signal transconductance, γ and δ are bias dependent parameters defined in (2.18) and (2.19), respectively, ζ is a constant, C is the drain and gate noise current correlation coefficient, and g_{d0} is the drain conductance at $V_{DS} = 0$. These equations can be used in the design process for obtaining optimum noise performance in the case of an LNA. A certain input matching network is generally chosen by the circuit designer in order to transform the generator impedance, for example 50Ω, into the impedance (admittance) required for minimum noise factor. As mentioned previously, LNA's are required to provide power gain as well, and we can easily deduce from our noise analysis that the input impedances required for minimum noise figure and maximum gain are generally not the same. In this case the designer is required to make a trade-off between noise figure and power gain. Also, power consumption plays an important role in this trade-off since mobile devices need to maximize battery life time. This puts a stringent power budget on all types of circuitry, including LNAs. Amplifier linearity adds an extra dimension to the trade-off analysis. The next

section will provide a brief analysis of linearity and how it is measured in RF/MW circuits.

2.3 Gain Compression and Intermodulation Distortion

Nonlinear effects are inherit in any realistic circuit component, especially in active devices such as transistors. Nonlinear transfer characteristics in amplifiers for example result in undesired distortion that is present in the output signal as well as gain compression when the input drive increases. In the frequency domain, distortion creates spurious frequency components which may lie in the desired signal band. Unwanted frequency components behave like added noise, thus, nonlinear effects ultimately degrade the signal SNR. As mentioned previously, receivers operating in a wireless mobile environment are very likely to receive a weak desired signal in the presence of a strong interfering one such as narrowband jammers. The LNA is required to maintain linear operation even in the presence of strong interferers. Failure to do so results in what is usually referred as blocking where the desired weak signal is swamped by intermodulation products of the interfering signal [7]. Generally, characterization of linearity in RF/MW amplifiers is given by the *1-dB compression point* and the input referred third order intercept point (IIP_3). These terms will be explained below, but we first introduce various types of nonlinearities that are of major importance in RF/MW amplifiers.

2.3.1 Gain Compression

The transfer characteristics of a nonlinear and memoryless circuit or network from input to output are commonly modeled using a Taylor series expansion [35] and [34] . In terms of input and output voltages, the Taylor series expansion can be written as

$$v_{out} = c_0 + c_1 v_{in} + c_2 v_{in}^2 + c_3 v_{in}^3 + ... \tag{2.63}$$

where c_0, c_1, c_3 are the first three coefficients of the Taylor series and v_{in} is an arbitrary input voltage. For practical considerations, we limited the expression to the third order term since this is generally sufficient to model the network input-output characteristics to a reasonable degree of accuracy. We can analyze the gain of the network using a single tone input denoted as $a_0 cos\omega_0 t$, with a_0 being the tone's amplitude and $\omega_0$its angular frequency. Inserting this input in (2.63) yields

$$v_{out} = c_0 + c_1 a_0 \cos\omega_0 t + c_2 a_0^2 \cos^2 \omega_0 t + c_3 a_0^3 \cos^3 \omega_0 t + ... \tag{2.64}$$

Using the trigonometric identity $\cos^2 x = \frac{1}{2} + \frac{1}{2}\cos 2x$, $\cos x \cos y = \frac{1}{2}[\cos(x - y) + \cos(x + y)]$, (2.64) becomes

$$v_{out} = c_0 + \frac{1}{2}c_2a_0^2 + c_1a_0\cos\omega_0t + \frac{1}{2}c_3a_0^3\cos\omega_0t + \frac{1}{4}c_3a_0^3\cos\omega_0t + \frac{1}{2}c_2a_0^2\cos 2\omega_0t + \frac{1}{4}c_3a_0^2\cos 3\omega_0t \quad (2.65)$$

To identify the small signal gain we take the ratio of the coefficients of the fundamental term to the input. This results in

$$A_{\omega_0} = \frac{c_1a_0 + \frac{3}{4}c_3a_0^3}{a_0} = c_1 + \frac{3}{4}c_3a_0^2 \quad (2.66)$$

From (2.66) we can see that the small signal gain is affected by the coefficient of the third order term, c_3. In devices such as MOSFETs c_3 is negative when the device is operating in strong inversion. In this case the gain, A_{ω_0}, experiences compression as the fundamental input power increases. The 1-dB compression point is defined as the input or output referred power point at which the power gain of the network is 1 dB below its ideal value. This is shown in Figure 2.10 where IP_{1dB} and OP_{1dB} are the input and output referred 1-dB compression points, respectively. From the definition of the 1-dB compression point, we can write

$$OP_{1dB} - P_{o(ideal)} = -1dB \quad (2.67)$$

where $P_{o(ideal)}$ is the ideal output power. Hence, at the 1-dB compression point we can define the amplitude of the input voltage as a_{1dB} . From this

we can denote the ideal output voltage at the 1-dB compression point as

$$v_{out(ideal)} = c_1 a_{1dB} \tag{2.68}$$

It follows that the non-deal output voltage can be written as

$$v_{out} = c_1 a_{1dB} + \frac{3}{4} c_3 a_{1dB}^3 \tag{2.69}$$

Rewriting (2.67) in terms voltages yields

$$20\log(\frac{v_{out}}{v_{out(ideal)}}) = -1dB \tag{2.70}$$

Substituting the expressions for $v_{out(ideal)}$ and v_{out} from (2.68) and (2.69), respectively, into (2.70) yields

$$20\log[\frac{c_1 a_{1dB} + \frac{3}{4} c_3 a_{1dB}^3}{c_1 a_{1dB}}] = -1 \tag{2.71}$$

As mentioned previously, the c_3 coefficient associated with a device operating in saturation is negative. With this in hand we can solve (2.71) for a_{1dB} to obtain in V as

$$a_{1dB} = 0.38\sqrt{\frac{c_1}{c_3}}\,[V] \tag{2.72}$$

As mentioned previously, wireless receivers are also characterized by the minimum detectable signal or noise floor. The output power range in which the amplifier maintains linear gain above the noise floor is referred to as

dynamic range. In practice this would be obtained by taking the difference between the 1-dB compression point and the noise floor level.

In addition to gain compression, amplifier nonlinearities also create harmonic distortion in which multiple frequencies of the fundamental frequency appear at the output. In the case of narrowband RF amplifiers, harmonic distortion is not of direct importance since multiples of the fundamental frequency will lie far outside the amplifier's band of operation. On the other hand, intermodulation distortion is a key nonlinear effect which needs to be carefully characterized and minimized.

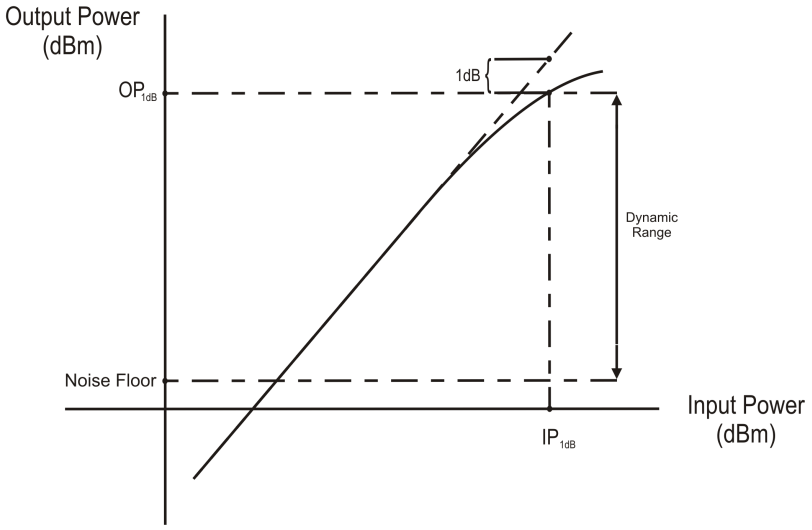

Figure 2.10: Illustration of 1-dB compression point.

2.3.2 Intermodulation Distortion

Intermodulation distortion results from applying a two-tone signal with a specific center frequency and frequency spacing between the two tones. In other words we can write the input mathematically as

$$v_{in} = a[\cos(\omega_1 t) + \cos(\omega_2 t)] \tag{2.73}$$

where ω_1, ω_2 are the angular frequencies, and a is the amplitude of both tones. In general, the amplitudes of both tones are not the same. However, we will assume that both tones have the same amplitude in the interest of simplicity. Applying this input to (2.64) one can obtain an expression for the different frequency components expected at the output as

$$\begin{aligned} v_{out} = {} & c_0 + c_1 a[\cos(\omega_1 t) + \cos(\omega_2 t)] + c_2 a^2[\cos(\omega_1 t) + \cos(\omega_2 t)]^2 \\ & + c_3 a^3[\cos(\omega_1 t) + \cos(\omega_2 t)]^3 + ... \end{aligned} \tag{2.74}$$

The expansion of (2.74) results in harmonic terms as well as in intermodulation terms. As mentioned before the harmonic terms are sufficiently attenuated in a narrowband amplifier. The quantity of interest in this case is the third order term, and more specifically the difference frequency components of the third order term which can be written as [7]

$$IM_3 = (\frac{3}{4}c_3a^3)[\cos(2\omega_1 - \omega_2) + \cos(2\omega_2 - \omega_1)] \tag{2.75}$$

We can see from (2.75) that the third order terms could represent a major source of distortion since they can easily lie in the amplifiers band of operation if $\omega_1$and ω_2 are close to each other, and the amplitude of these terms grows as the cube of input amplitude. The third order intercept point is used as a measure of intermodulation distortion using a two-tone input signal, where the linear region of the fundamental and third order frequency terms are extrapolated until they meet. The point of intersection is called the third order intercept point, or IP_3 as illustrated in Figure 2.11. The higher this point is the more linear the device is. In general, every communication standard has its specifications for overall receiver input-referred IP_3 or (IIP_3). Typically, microelectronic implementation of LNAs are required to have IIP_3 values of -10 dBm or higher, mixers are usually expected to attain an IIP_3 value higher than $+5$ dBm.

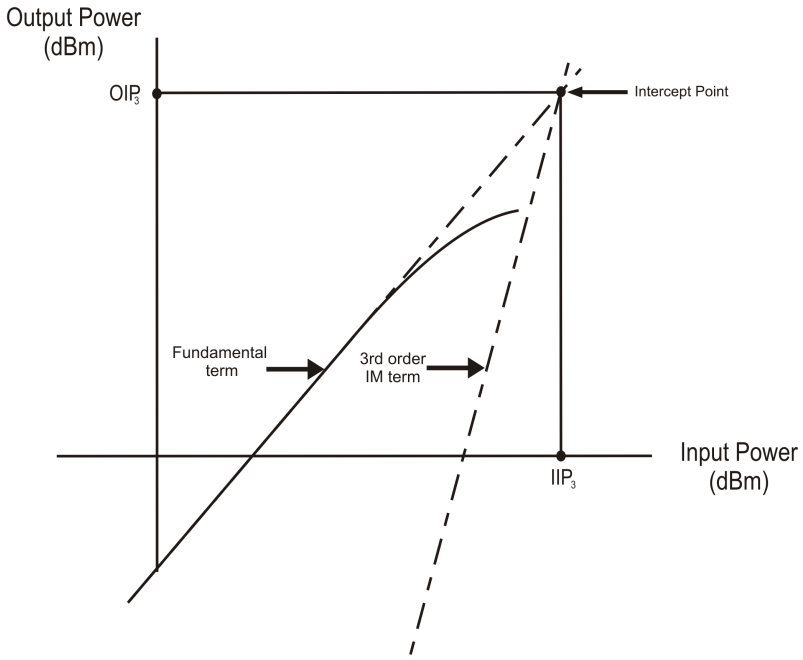

Figure 2.11: Definition of third order intercept point.

From this analysis we realize the importance of minimizing the third order coefficient $c_3$in order to maximize the linearity of the operating device. There are several ways to achieve this goal depending on the type of device and its ease of implementation in an IC environment. A technique specific to FETs and suitable for LNA operational requirements will be used in order to obtain the required IP_3 depending on standard and band of operation. This will be one of the design considerations which will be discussed in the upcoming chapters.

Chapter 3

Low-Noise Amplifier Design

3.1 General Considerations

Low-noise amplifiers (LNAs) are usually the first active block in a receiver chain and play a major role in determining a receiver's overall noise performance. Thus, an LNA is required to provide maximum amount of gain while adding the minimum amount of noise power to the receiver signal. In today's modern integrated transceivers, LNAs are usually preceded by off-chip duplexers or band-selection filters, which requires the LNA to have a 50 Ω input impedance, since the transfer characteristics of duplexers and filters are usually sensitive to terminating load impedances. Furthermore, LNAs are required to achieve high degree of linearity in order to maintain a wide dynamic range of operation.

The push toward more integration and single-chip transceivers has ul-

timately altered the design procedure of high frequency circuits such as RF/MW amplifiers. Until the early nineties, radio design engineers relied on the S-parameter method for designing discrete radio frequency circuits, treating each circuit element as a distributed component, analyzed using transmission line theory. Using this method, designing a high frequency amplifier is usually divided into three stages as shown in Figure 3.1.

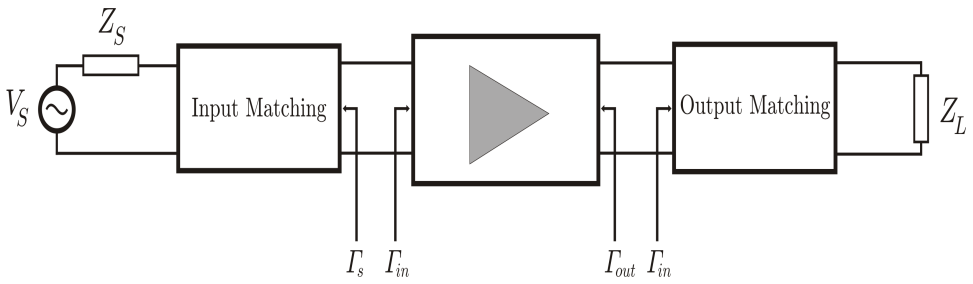

Figure 3.1: General high frequency transistor amplifier.

As transistor feature sizes keep shrinking into the deep sub-micron regime and beyond, circuit dimensions become so small compared to the wavelength that lumped element design techniques can be employed in the design of integrated circuits in the GHz range without loss of accuracy. The general rule of thumb is that transmission line effects can be ignored if the ratio of average circuit dimension (l) to the associated wavelength (λ) is smaller than 0.01 [22]. In the case of a 130 nm CMOS technology and at a frequency of 50 GHz, as an example, the ratio $\frac{l}{\lambda}$ is approximately 0.007, allowing for lumped element representation to be used in circuit analysis and design. Nevertheless, S-parameter representation still remains essential in the design process, especially in characterizing the circuit interface with off-chip components such

as filters.

Designing an LNA for multiband operation can be accomplished using two different approaches: a) a wideband approach, and b) a tunable narrowband approach. A wideband LNA is an attractive approach since it consists of designing a general amplifier operating over a broad bandwidth. The band selection must be done using a bandpass filter following the amplifier. A wideband LNA requires broadband matching networks at the input and output and possibly interstage matching if more than one stage is used. This translates into more off-chip components or more lossy on-chip components which also consume more die area. Demand for a wideband response generally requires more complex circuitry and more power consumption, while noise performance generally remains unsatisfactory over the entire band [4]. On the other hand, a narrowband LNA uses tuned circuits to achieve matching at the input and output of the amplifier for each frequency of interest. Thus, gain, matching, and noise performance can be optimized for each band with considerably less power consumption and smaller chip area compared to a wideband topology. Simple LC resonators are used for output matching in order to peak the amplifier gain, and simple two or three-element matching is used to achieve optimum power transfer at the input. The major disadvantage of using a narrowband technique is the component value variation in large scale IC manufacturing process. This can be effectively mitigated using on-chip tuning for input matching and output LC tank circuits. In general wideband LNAs are more complex in nature and inferior in performance

measures pertaining to gain, noise figure, matching, and DC power consumption. Also, receivers based on a wideband solution are more susceptible to out of band interfering signals which degrade overall receiver sensitivity. For these reasons a tunable narrowband approach will be used in this work for the purpose of designing a multiband LNA.

3.2 The Narrowband CMOS LNA

The cascode LNA, consisting of a common source followed by a common gate device, with inductive degeneration is the most widely used architecture due to its simple design and the potential of achieving the best noise performance. As illustrated in Figure 3.2, the common source LNA generally uses two inductors in order to achieve noise and power match at the input. The common gate device (M2) in Figure 3.2 will be referred to as the cascode device for simplicity. Achieving an input match is dependent on the proper choice of device width, bias condition, and L_s and L_g values. In the following we will analyze this LNA architecture in terms of input match, output match, and noise performance.

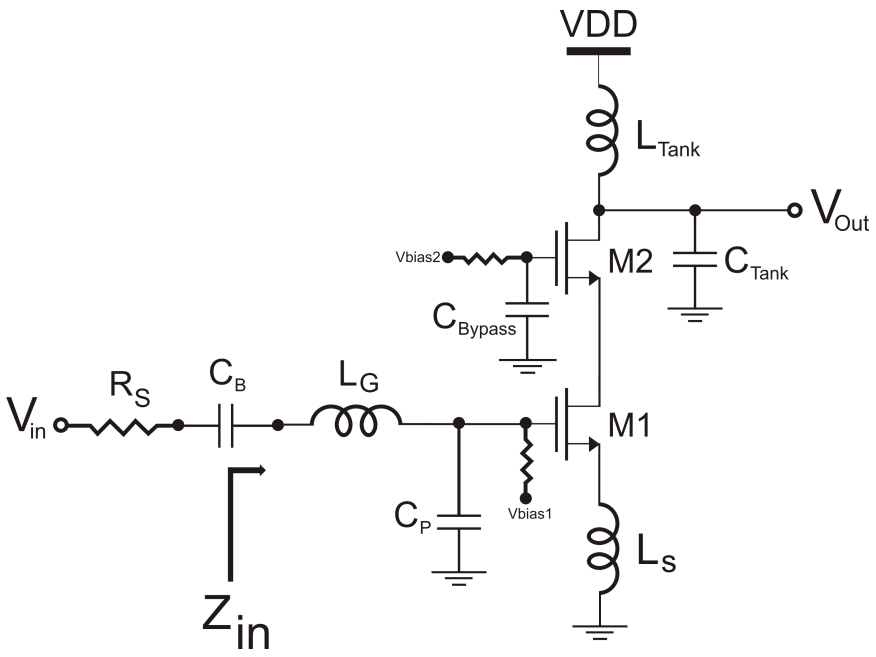

Figure 3.2: Narrowband common-source LNA architecture using two element input matching network and a cascode stage.

3.2.1 Input Match

Achieving maximum power transfer to the LNA requires a conjugate match at the input device (M1). Since the input impedance of a FET is inherently capacitive, and we need a match at a single frequency, we can use inductors to achieve an LC resonating circuit to reach this goal. The first design step is to choose a device width and a gate bias voltage which will provide desired transconductance, current consumption, noise performance, and gate to source capacitance. In some cases the scaling of device widths to obtain a certain gate to source capacitance might result in unacceptable current

consumption, for this reason an on-chip capacitor (C_p) is used. The second step is to use the source degenerating inductance (L_S) to match the real part of the device input impedance to 50 Ω. Finally, the reactive part of the device input impedance is tuned out using the gate inductance (L_G). This process is more clearly illustrated using the device model depicted in Figure 3.3.

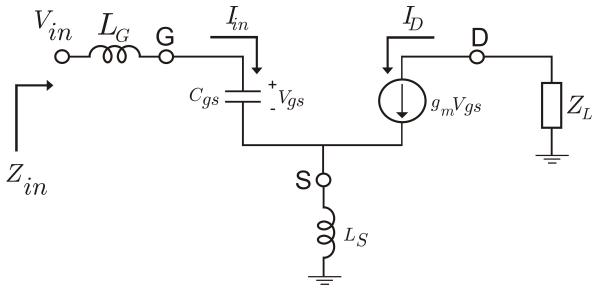

Figure 3.3: NMOS small-signal model employing source degeneration and gate inductances

In order to obtain an intuitive and simple design procedure, the NMOS device is modeled using a controlled current source and a gate to source capacitance. Writing a KVL at the input loop and ignoring (C_p) we obtain

$$V_{in} = I_{in} j\omega L_G + I_{in}(\frac{1}{j\omega C_{gs}}) + I_{in}(j\omega L_S) + I_D(j\omega L_S) \tag{3.1}$$

Substituting $I_D = g_m I_{in}(\frac{1}{j\omega C_{gs}})$ into (3.1) and solving for $\frac{V_{in}}{I_{in}}$ we obtain an expression for Z_{in} as follows

$$Z_{in} = \frac{V_{in}}{I_{in}} = j\omega(L_S + L_G) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_S}{C_{gs}} \tag{3.2}$$

The third term of (3.2) represents the real part of the input impedance, which implies that with the proper choice of source inductance and device dimensions one can match the real part of Z_{in} to 50 Ω. At first glance, it might seem that the source degenerating inductance would be enough to compensate for the capacitive term. The source degenerating inductance is usually realized using a bondwire which cannot provide an inductance of more than 5 nH in a 130 nm CMOS process. On the other hand, it has been shown that a smaller source inductance improves noise performance, although a complete understanding of this relation has not been obtained yet . For these aforementioned reasons a gate inductance (L_G) is used.

3.2.2 Output Matching and Gain

In the world of discrete RF circuit design, LNAs are required to have a 50 Ω output match in order to deliver power efficiently to a subsequent stage. This is not the case when dealing with an integrated LNA, which usually drives a capacitive load such as the input to a down-converting mixer. Power reflections at the input of the mixer are not of major concern either since circuit dimensions are much smaller than the wavelength. For these reasons the load circuit of an integrated LNA is designed to maximize voltage gain using an LC tank as shown in Figure 3.2.

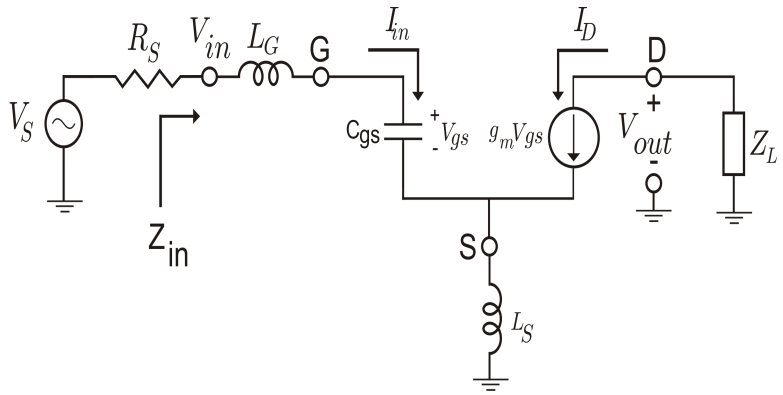

Figure 3.4: NMOS small-signal model with load impedance and voltage source

Using the small-signal model and the configuration shown in Figure 3.4 we can derive an analytical expression for the voltage gain of the degenerated common source FET. First, we note that the load impedance attached to the drain of the common source device represents the impedances of the cascode device and the LC tank combined. Second, we assume that the cascode device provides unity gain so that the overall transconductance of the LNA can be equated to the transconductance of the common-source FET. With these underlying assumptions the expression for V_{out} can be written as

$$V_{out} = -g_m V_{gs} Z_L \tag{3.3}$$

We can express V_{gs} as

$$V_{gs} = I_{in} Z_{gs} \tag{3.4}$$

Inserting (3.4) into (3.3) we obtain and solving for $\frac{V_{out}}{V_{in}}$

$$\frac{V_{out}}{V_{in}} = -g_m I_{in} Z_{gs} Z_L \tag{3.5}$$

Substituting $I_{in} = \frac{V_{in}}{R_S}$ and the capacitor impedance expression for Z_{gs} in (3.5), and solving for the voltage gain we obtain

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{g_m Z_L}{\omega_o C_{gs} R_S} \tag{3.6}$$

Using the expression $\omega_T = \frac{g_m}{C_{gs}}$ in (3.6) we find the voltage gain expression as

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{\omega_T Z_L}{\omega_o R_S} \tag{3.7}$$

This simplified expression for the voltage gain provides first order insight into the design procedure. In order to maximize voltage gain the impedance at the source must be minimized, and the parallel LC load circuit must resonate and provide high impedance at the center frequency of the operating band. Moreover, we observe how the gain will tend to roll-off as the operation frequency increases compared to the unity gain frequency of the FET.

3.2.3 Noise Performance

The study of noise performance of the LNA topology shown in Figure 3.2 must take into consideration the various types of noise sources. In general, the overall noise in the circuit originates from the active devices, FET's in this

case, and from losses in passive components such as inductors and capacitors. In order to obtain a intuitive analytical expression for the noise figure of the LNA, certain simplifications have to be made. First, we can ignore the losses in the passive components, their contribution to the noise performance will be characterized later on using computer simulations. Second, we can assume that the major contributor to the overall noise is the common-source FET. The cascode device does contribute drain noise current, but since it provides unity gain and is preceded by a gain stage which is the common-source FET, we can ignore its noise contribution for a first order approximation.

Based on our analysis of the BSIM3v3.2.4 MOSFET noise model in the previous chapter, we will assume that the MOSFET noise is dominated by the channel thermal noise. Gate induced noise will be neglected since we are interested in operating frequencies well below the $f_T/10$ point, which allows us to make such an approximation as stated in section 2.2.6.3.

With these assumptions, we can rewrite (2.11) for the noise factor as follows

$$F = \frac{N_{out(Total)}}{N_{out(Source)}} = \frac{N_{out(Source)} + N_{out(Added)}}{N_{out(Source)}} = 1 + \frac{N_{out(Added)}}{N_{out(Source)}} \tag{3.8}$$

where $N_{out(Total)}$ is the total noise power measured at the output, $N_{out(Source)}$ is the total noise power measured at the output due to the source resistance, and $N_{out(Added)}$ is the noise power at the output added by the noisy network.

In order to use (3.8) we need to represent the noisy FET with an equivalent input voltage noise source. This is done by reflecting the short-circuit drain noise current, given by (2.18), to the input of the device [7]. To do this we use the fact that the short circuit drain current is related to an input voltage, say v_i , by the device transconductance (g_m) as follows [3]

$$i_d = g_m v_i \tag{3.9}$$

Using this same definition for short circuit drain noise current, we can find the input voltage noise generator using (2.18) as

$$\overline{v^2_{n(FET)}} = \frac{\gamma 4kTg_{d0} \triangle f}{g^2_m} \tag{3.10}$$

where the noise voltage generated by the source resistance is given by (2.1). The transconductance in (3.10) corresponds to the transconductance of the FET only. Since we have a degeneration and a gate inductance we need to take into consideration the overall stage transconductance. This can be written as [4]

$$G_m = g_m Q_{in} \tag{3.11}$$

where Q_{in} refers to the input matching network's nodal quality factor which is defined as [7]

$$Q_{in} = \frac{1}{\omega_o C_{gs} R} \tag{3.12}$$

where R is the real part of the input impedance of the common source FET, which can be equated to R_S in matched conditions, and ω_o is the center frequency of interest. Inserting the expression for G_m instead of g_m in (3.10) we obtain

$$\overline{v^2_{n(FET)}} = \frac{\gamma 4kT g_{d0} \triangle f}{g_m^2 Q_{in}^2} \tag{3.13}$$

To use (3.13) in (3.8) we substitute $\frac{\overline{v^2_{n(FET)}}}{\Delta f}$ instead of $N_{out(Added)}$, express the noise added by the source resistance by $4kTR_S$ instead of $N_{out(Source)}$, and performing the necessary algebraic manipulation we obtain an expression for the noise factor as follows

$$F = 1 + \frac{\gamma g_{d0}}{g_m^2 Q_{in}^2 R_s} \tag{3.14}$$

Consequently, the noise figure expression is

$$NF = 10Log(1 + \frac{\gamma g_{d0}}{g_m^2 Q_{in}^2 R_S}) \tag{3.15}$$

Substituting the expression for Q_{in} from (3.12) in (3.15) we obtain

$$NF = 10Log(1 + \frac{\gamma g_{d0}}{\frac{g_m^2}{\omega_o^2 C_{gs}^2 R_s}}) \tag{3.16}$$

The intrinsic transistor unity gain frequency is given by $\omega_T = \frac{g_m}{C_{gs}}$, resulting in a noise figure expression as follows

$$NF = 10Log(1 + \frac{\gamma g_{d0}}{(\frac{\omega_T}{\omega_o})^2 \frac{1}{R_S}}) \tag{3.17}$$

Finally, using the matching condition ($R_S = g_m \frac{L_S}{C_{gs}}$) in (3.17) and the simplification ($g_{d0} = g_m$) [3] we obtain

$$NF = 10Log(1 + \frac{\gamma g_m^2 L_S}{C_{gs}(\frac{\omega_T}{\omega_o})^2}) \tag{3.18}$$

Analyzing (3.18) we can obtain some insight into the parameters influencing the noise performance of the common source FET. First, we recall that reduction in device length results in increase in the transistor unity gain frequency (ω_T), which in turn reduces the noise figure as we hold the operating frequency (ω_o) constant. However, increasing operational frequency will result in increase in noise figure. Second, we observe that having the minimum source degenerating inductance helps in optimizing the noise figure performance and also improves the overall voltage gain as depicted in (3.18). From a mathematical point of view, we can obtain the optimum noise performance if we set Q_{in} to ∞ which in turn implies that R in (3.12) should be 0. In Section 3.2.1 we saw that R is designed such that it matches the source resistance (R_S) for good power transfer. This shows that the optimum power and noise performance cannot be simultaneously obtained.

With this theoretical formulation in hand, we can now proceed to the

practical implementation of a tuned multiband and multistandard LNA, this will be discussed in detail in the next chapter.

Chapter 4

Multistandard CMOS LNA Implementation

4.1 Design Specifications

Implementation of a CMOS multiband and multistandard LNA requires a great degree of flexibility from the three amplifier building blocks presented in Figure 1.3. Operation in more than one frequency band stresses the need for simple but effective methods of reconfiguring input match, output match, transistor size, and power consumption in order to meet all the specifications of each mode of operation. Armed with state of the art CMOS technology, we can take advantage of several mixed-signal design concepts and techniques in order to transform a static narrow-band LNA, operating in one frequency band, to a dynamic and flexible LNA that can operate across a wide range

of frequencies. In order to obtain a table of performance specifications for a multiband LNA, we need to look into the radio specifications of all four target standards. Unfortunately, this task is not completely generic to all wireless communication standards, especially when considering more than one standard at a time. Moreover, the type of receiver architecture used influences the performance specifications required of each receiver building block. Several receiver architectures have been explored in the literature, from the classical superheterodyne architecture to the direct conversion or "Zero-IF" receiver. Each architectures has its own advantages and drawbacks. Nonetheless, "Zero-IF" receivers have gained significant attention over the past decade since it is far more suitable for multistandard applications, and, more importantly, it eliminates several off-chip components such as filters, therefore improving the degree of integration. Comprehensive treatment of different receiver architectures is beyond the scope of this work. More detail can be found in [21], for example.

In spite of the complications arising from deriving LNA performance parameters, we can set our goal on implementing a multistandard LNA suitable for direct conversion receivers. Taking all four targeted standards, namely IS-95, GSM900, UMTS, and IEEE802.11g, a generic set of performance parameters can be found that satisfy all standards. Table 4.1 summarizes the LNA specifications which we will attempt to meet.

	IS-95	GSM	UMTS	IEEE802.11g
Band (MHz)	869-894	925-960	1930-1960	2400-2483.5
Gain (dBV)	18	14	18	15
NF (dB)	2	3	2	4.5
S11 (dB)	-14	-14	-14	-14
S12 (dB)	-20	-20	-20	-20
IIP3 (dBm)	-10	-10	-10	-10

Table 4.1: IS-95/GSM900/UMTS/IEEE 802.11g LNA performance specifications.

In the following sections, we will introduce the circuit topologies and techniques used to implement a multistandard LNA which will meet the performance specifications presented in Table 4.1.

4.2 Detailed LNA Architecture

Figure 4.1 shows a detailed block diagram of the proposed LNA architecture. The dotted line represents the chip boundaries. The core of the LNA structure is composed of the common source (CS) and the cascode stage as described in detail by Figure 3.2. Two switching capacitor networks are used for input and output matching. The input switched capacitor network works in conjunction with the RF switching block and the off-chip inductors in providing a 50 Ω input match. The top of Figure 4.1 depicts an LC resonating tank and a switched capacitor circuit both used to peak the voltage gain at any of the target operating bands. On the DC biasing side, a programmable bias network provides the desired gate voltages for the common source and

the cascode transistors. A shift register converts incoming serial data to parallel which is used to digitally program the reconfigurable blocks. Detailed description of each block is carried in the subsequent sections.

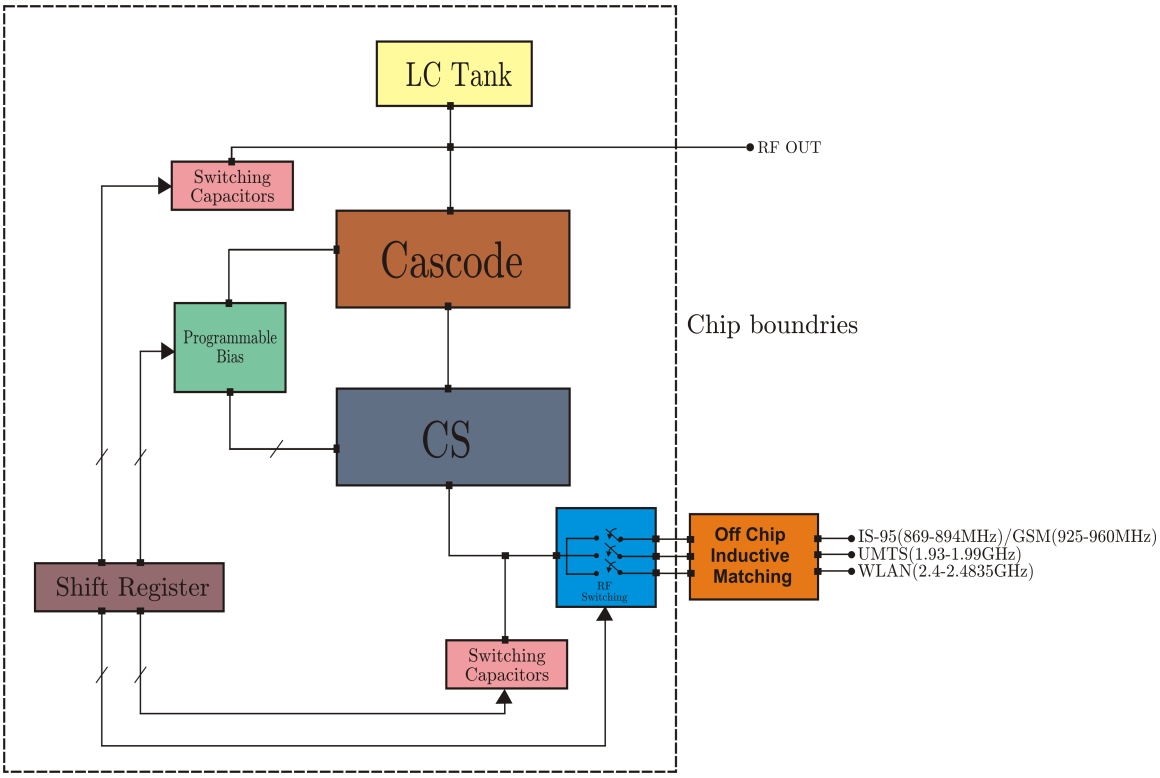

Figure 4.1: Detailed programmable LNA block diagram.

4.2.1 Common Source Stage

From Section 3.2.1 we saw that the transistor width, in a common source configuration, has significant contribution to the overall capacitance present in the input series LC network. Sizing transistor width will size the gate to source capacitance proportionally and thus altering the capacitive reactance

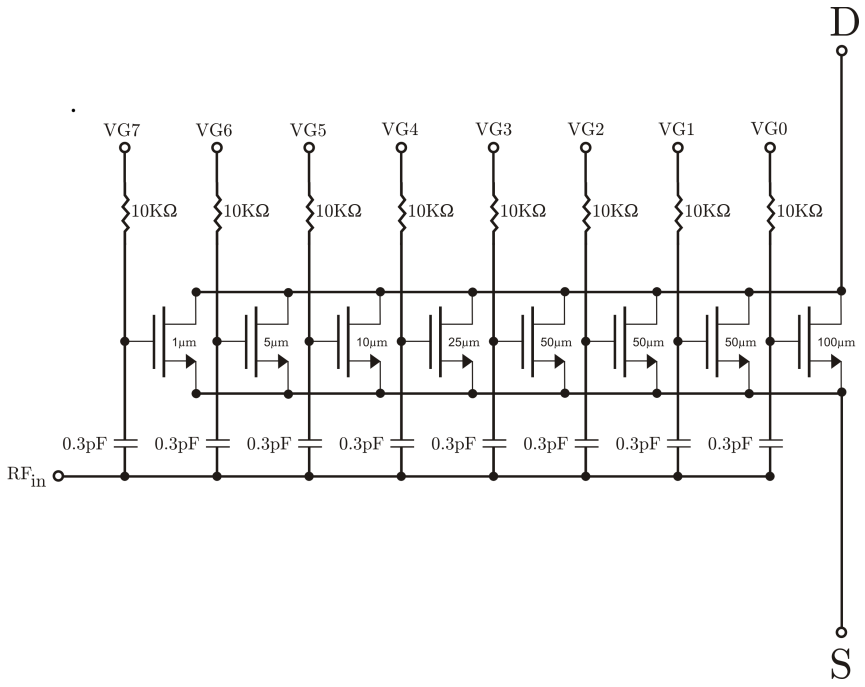

Figure 4.2: Input common source device consisting of a parallel connection of eight NMOS transistors.

at a specific frequency. For this reason we need a common source network that basically implements a single common source transistor but with the added feature of a tunable transistor size. Figure 4.2 shows the implementation of such a common source stage.

The network consists of a bank of transistors, sized to provide a wide range of effective widths according to operating frequency, desired current consumption, etc. Using the programmable DC bias network, one can choose which transistor to turn on/off by changing the voltage at the gate of the device, labeled VG for each transistor as shown in Figure 4.2. Since we have eight transistors, we can use a binary word consisting of eight bits to obtain

a desired transistor width. All transistors have a common RF input, thus necessitating the need for DC blocking capacitors. The capacitors are realized by on-chip metal-insulator-metal (MIM) capacitors. These capacitors are chosen to be small enough so that their reactance does not significantly affect the resonance frequency of the series LC tank composed of the device itself, the degenerating inductance, the switched capacitor network, and the off-chip gate inductance. All transistor source and drain terminals are connected together, respectively. This effectively implements a single common source transistor with a tunable channel width. The width of each device was chosen such that the network can provide the required device width for each frequency of operation. More specifically, initial analytical analysis and simulations in ADS showed that a device with a width of 200 μm is required for operation in 800 MHz band, while a device as narrow as 50 μm can be used at 2.4 GHz. The resistors through which the gate voltage is provided are not modeled in this design, but as far as layout is concerned a diffusion resistor will be used since its structure is very similar to a MOSFET.

4.2.2 Cascode Stage

The cascode stage is realized by a single $300\mu m$ NMOS transistor. Although this size seems somewhat arbitrary, the specific width was chosen in order to allow maximum current sinking that the common source stage requires when all transistors are on, and operating in saturation. Also, a large casocode transistor provides a greater degree of isolation between the output and input

ports of the amplifier. Having good isolation is critical especially in direct conversion receivers since the frequency of the local oscillator (LO) is identical to the RF frequency. This results in LO leakage into the reverse path of the receiver, towards the output port of the LNA. On the other hand, a cascode transistor chosen to be too wide will increase the overall capacitance that the common source stage sees at its output as well as its noise contribution. This makes it difficult to peak the voltage gain and maintain low noise figure at high frequencies. In most cases, the cascode device is chosen to be the same width as the common source device in a single band LNA. Since we have a tunable common source structure that can have a transistor as large as 295 μm when all transistors are on, we chose the cascode device to be $300\mu m$ for all cases in order to keep the design simple.

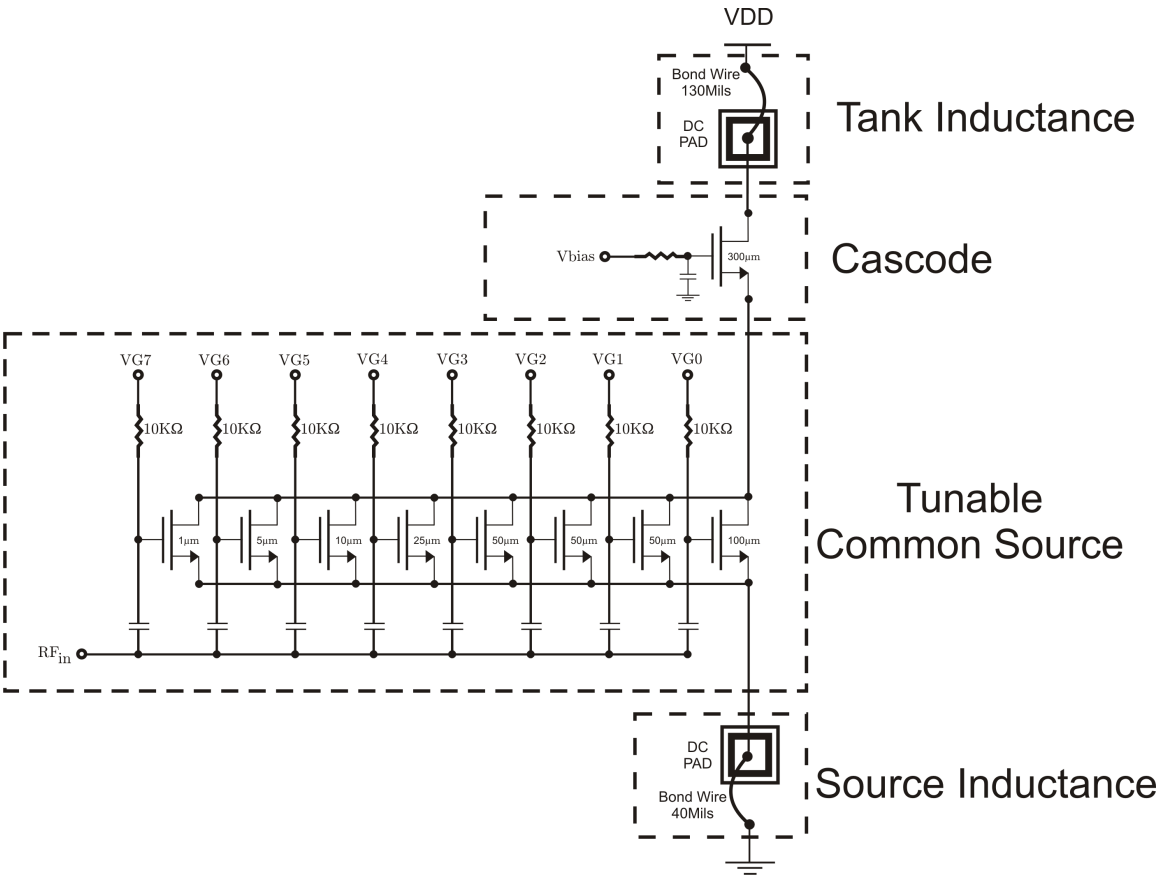

Figure 4.3: Tunable common source transistor configuration with cascode device and bondwire inductors.

Figure 4.3 illustrates the common source stage and the cascode stage. The source inductance is realized by a bondwire with the minimum length of 40 Mils. This minimum bondwire length is typical of UMC's CMOS process for the purpose of RF and mixed signal design. In this case, the bondwire provides an inductance of approximately $1nH$. The tank inductance is also realized using a bondwire of130 Mils in length. This length was chosen in order to provide good voltage gain across the targeted frequency bands in

conjunction with a switched capacitor network, this will be explained in more detail in Section 4.2.4.

4.2.3 Switched Capacitor Networks

Switched capacitor networks will be used in two instances in this design. At the gate of the common source device, a switched capacitor network will provide an additional capacitive component which will allow us to increase the effective gate to source capacitance the RF signal "sees" when viewing into the input of the amplifier. Also, this will assist in compensating for the variations in bondwire length which occurs during fabrication, this variation can be as high as 40%. Having a tunable common source stage helps in mitigating the effect of bondwire variations. Another switched capacitor network will be used in conjunction with the bondwire at the drain of the cascode device to form a tunable LC tank. This capacitor network will provide a tuning range over which the voltage gain of the amplifier can be peaked. Figure 4.4 shows a circuit schematic of the switched capacitor network used at the gate of the common source device. The logic levels (0/1) correspond to 1.2V and 0V, respectively.

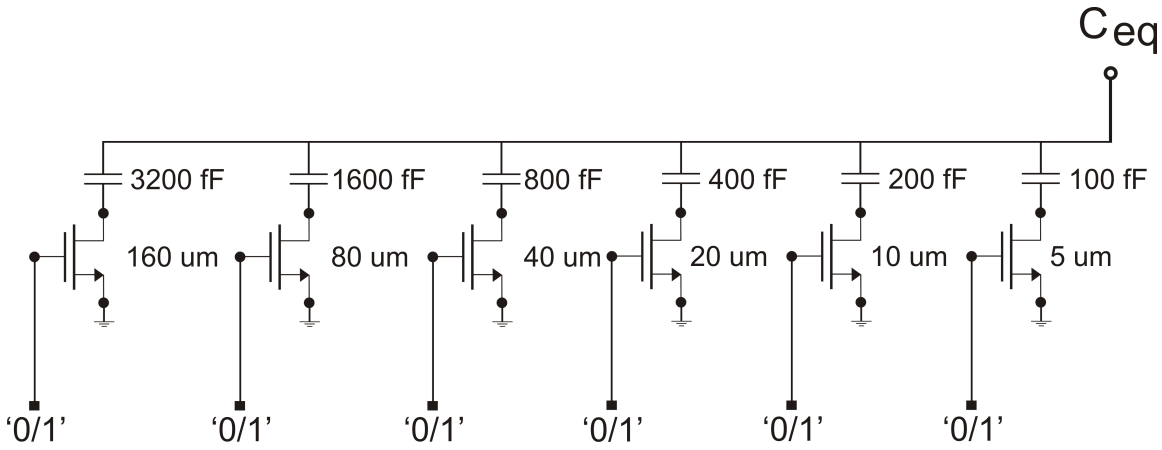

Figure 4.4: Input switching capacitor circuit.

Capacitors are realized using on-chip MIM structures provided by UMC's CMOS technology. A typical MIM structure has an effective capacitance of $1fF/\mu m^2$ [67]. Depending on process technologies, these MIM capacitors have a finite quality factor: according to UMC, a 1fF MIM capacitor has a Q of more than 30 at 2.4GHz [67]. Since the overall quality factor of the input matching network affects the overall noise performance of the LNA, we start by characterizing the quality factor of the input switched capacitor network shown in Figure 4.4. The quality factor of the switched capacitor network will be a function of the number of switches that are in an "on" state. This is due to the FET's "on" resistance, R_{FETon}, as well as the finite quality factor of the MIM capacitor itself, see Figure 4.5. The model used for MIM capacitors in this design is a simple ADS "capacitor with Q" model which models the Q of the capacitor as a function of frequency. A detailed model description can be found in [73].

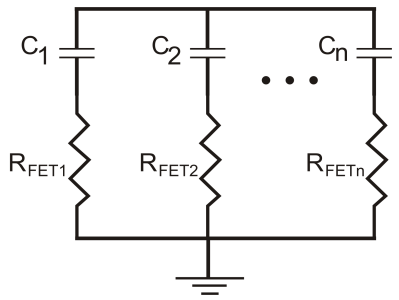

Figure 4.5: Switched capacitor network equivalent circuit when all switches are turned on.

The switched capacitor circuit illustrated in Figure 4.4 uses binary weighted capacitor values as well as FET sizes. Using binary weighted capacitor values gives a wide range of capacitor values and allows fine tuning using an 8-bit word. The FETs are binary sized in order to scale each FET's "on" resistance by a binary weight. This maintains an overall constant nodal Q independent of the number of branches that are on [68]. From this we can write a general expression for the FET channel size as follows

$$W_{FET_n} = 2^{n-1}W \tag{4.1}$$

where n is the number of switch/capacitor pairs and W is the channel width of the smallest FET. A similar formula applies for the capacitor values. In the case of a MOSFET, using a first order approximation, we can assume that the channel "on" resistance scales proportionally with the device width. Thus, we can write

$$R_{FET_n} = \frac{R_{FET_1}}{2^{n-1}} \tag{4.2}$$

where R_{FET_1} is the channel "on" resistance of the smallest device. For each switch/capacitor pair, we can analytically determine the quality factor by taking the ratio of total reactance to the total resistance. This can written as

$$Q_{branch_n} = \frac{|X_{C_n}|}{R_{FET_n}} = \frac{1}{\omega_o R_{FET_n} C_n} \tag{4.3}$$

where C_n is the capacitance value of branch n, and ω_o is the angular frequency. With the scaling relationship of device size, channel resistance, and capacitor values we expect the quality factor to remain constant irrespective to how many switches are turned on. So depending on how many branches are switched on, we can write an expression for the total quality factor as

$$Q_{Total} = \frac{1}{\omega_o R_{Total} C_{Total}} \tag{4.4}$$

Performing an S-parameter simulation we can characterize the quality factor of the switched capacitor network shown in Figure 4.4 as a function of the programming bits. Figure 4.6 shows the quality factor versus the serial word that is written to the programming ports of the device.

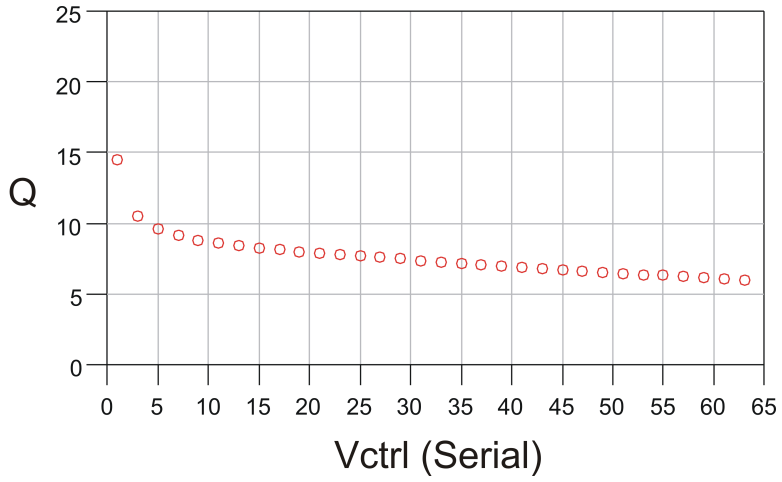

Figure 4.6: Input switched capacitor network quality factor (Q) versus Vctrl.

From Figure 4.6, the first observation we can make is that the quality factor is not held constant with respect to the serial input labeled $Vctrl$, which represents the integer equivalent of the serial bits written to the network. In (4.2) and (4.3) we assumed that channel resistance will scale proportionally with the device width according to the simple MOSFET drain current square law relationship with the overdrive voltage $(V_{GS} - V_t)$ when operating in saturation

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_t)^2 \tag{4.5}$$

Using (4.5) the transistor "on" resistance can be derived as

$$R_{FET} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)} \tag{4.6}$$

In the case of advanced CMOS silicon technology and short channel

regimes, the observed channel-on resistance will differ significantly from what (4.6) suggests, and will not have the direct proportionality relationship with device width. This is the major reason why the quality factor in Figure 4.6 does not remain constant as $Vctrl$ is swept. We also realize from Figure 4.6 that having the minimum number of branches on helps maintain the quality factor since more active branches results in larger total series resistance. Figure 4.7 shows the effective capacitance as a function of $Vctrl$ for the switched capacitor circuit in Figure 4.4.

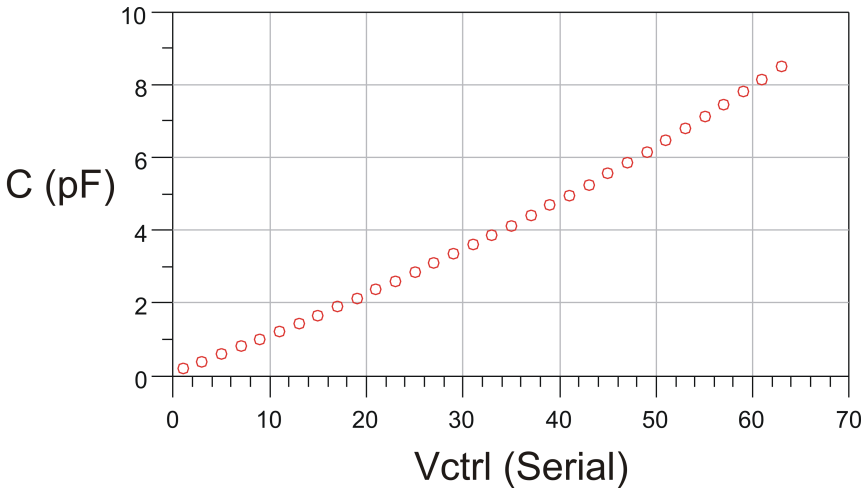

Figure 4.7: Effective capacitance as a function of serial control voltage for the input switched capacitor circuit.

In order to minimize the channel on resistance, capacitors and MOSFETs are realized using a parallel structure of small unit cells consisting of a $5\mu m$ MOSFET and a $100fF$ MIM capacitor. As a result, for the first branch in the switched capacitor circuit shown in Figure 4.4, a unit cell is used. Larger cells contain multiple cells in a parallel configuration according to the binary

weighting explained above.

4.2.4 Input/Output Matching

As discussed in Section 3.2.1, the input match is achieved using the degenerating source inductance (L_S), the variable gate capacitance (C_P), and the off-chip gate inductor (L_G) in order to achieve a 50 Ω match. Using the programmable common source stage, the fixed source inductance, and the programmable gate capacitance, we can run simulations in ADS in which we sweep any of the two variable quantities mentioned above and find the conditions that will provide the best matching at a given center frequency. Considerations of power consumptions and common source gate bias are taken into account as well. Thus, the design process starts by making an intuitive choice of the common source device width for a specific center frequency. The selection of gate bias will be explained in Section 4.4 where we discuss linearity performance. The next step is to find the optimal C_P that will provide a 50 Ω real impedance. This is done by sweeping the programming bits sent to the switched capacitor network at the gate of the common source FET. Several iterations can be made by adjusting the width of the common source device and running the simulation again until the desired real part is obtained. The final step is to find a suitable chip inductor which will provide a pure real impedance at the LNA's input port.

Figure 4.8 shows a family of $Re[Z_{in}]$ curves obtained by running the simulation described above in the frequency range between 0.7 and 1.2GHz.

Each curve corresponds to a specific bit sequence, where the top most curve corresponds to the lowest bit sequence (000000) and the bottom most curve corresponds to the highest bit sequence used in the this simulation (000111). With three bits being swept, the effective capacitance provided by this network will range from ideally 0pF to 0.7pF with 0.1 increments since we are only using the first three branches shown in Figure 4.4. Hence, the top most and bottom most curves in Figure 4.8 corresponds to a C_P of 0pF and 0.7pF, respectively.

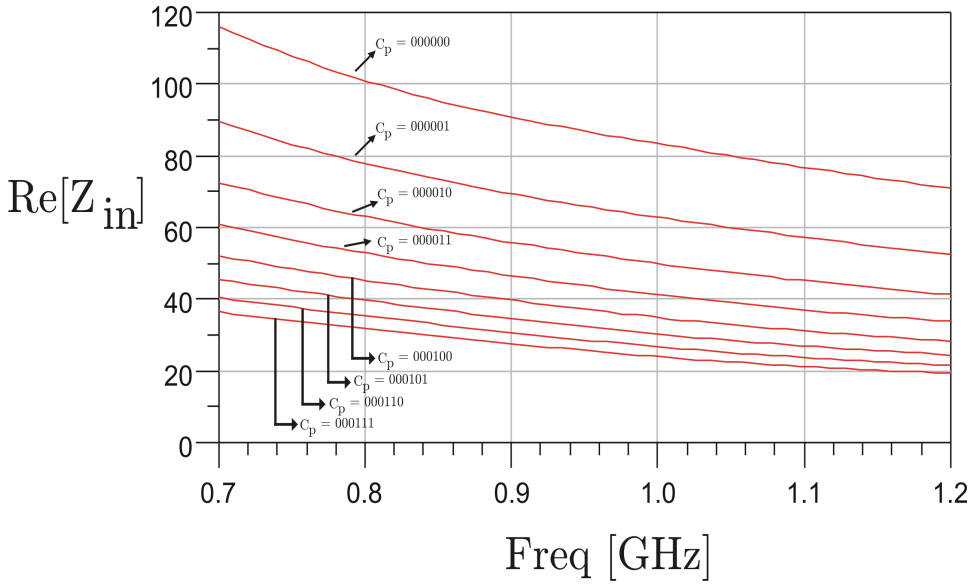

Figure 4.8: Real part of input impedance vs. frequency and C_P for common source with W = 185 μm and L = 0.13μm.

Once the desired settings for the common source transistor width and C_P have been obtained for the desired center frequency, the off-chip series gate inductance is chosen. The inductors are chosen from a list of available 0402

chip inductors provided by Coilcraft [70]. For the purpose of simulations, we use the lumped element models for inductors provided by Coilcraft as well. Details of inductor models are listed in [70].

Finally, the output match is as described in Section 3.2.2 where a parallel resonating circuit is used to peak the voltage gain at a specific center frequency. The inductance used for this purpose is a 130 mil long bondwire. Since the inductance of the LC tank is fixed, and the tuning range is wide ($0.88GHz - 2.44GHz$), the capacitance is realized using a large on-chip MIM capacitor on the order of $6.5pF$ and a switched capacitor network that provides small tuning steps as shown in Figure 4.9.

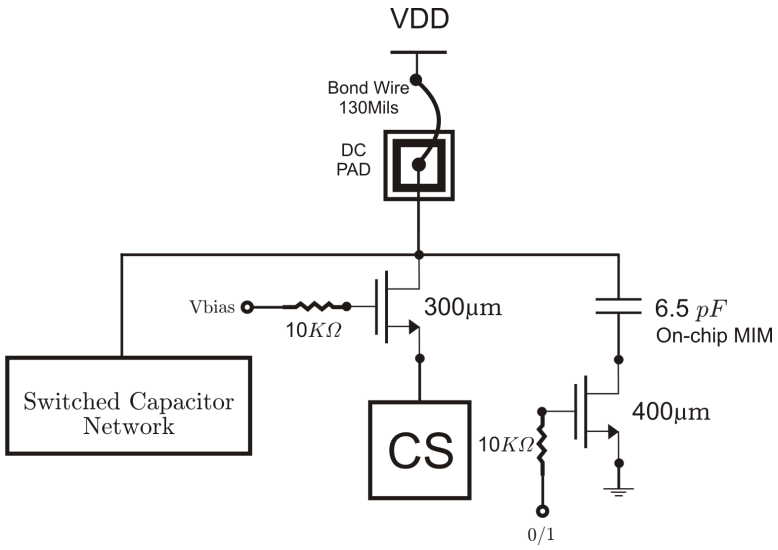

Figure 4.9: Block diagram of load LC tank circuit using a switched capacitor network as well as a switchable 6.5pF MIM capacitor.

It is possible to use only the switched capacitor network to obtain the needed capacitance across the entire bandwidth, which eliminated the need

for an extra large capacitance. The drawback of this approach is the low quality factor of the switched capacitor network when most or all the branches are turned on. For this reason a $6.5pF$ MIM capacitor is switched into the LC tank when the voltage gain needs to be peaked at the low frequency bands (IS-95 and GSM). Peaking the voltage gain at higher frequencies only requires the use of the switched capacitor network.

4.2.5 Programmable Bias

Two separate, but similar, bias networks are used to bias the common source stage and the cascode stage of the LNA. Each bias network utilizes a binary weighted current mirror configuration comprised of PMOS devices. The building block of the bias network consists of a configuration widely used in CMOS technology for the purpose of generating a reference current, independent of temperature variations.

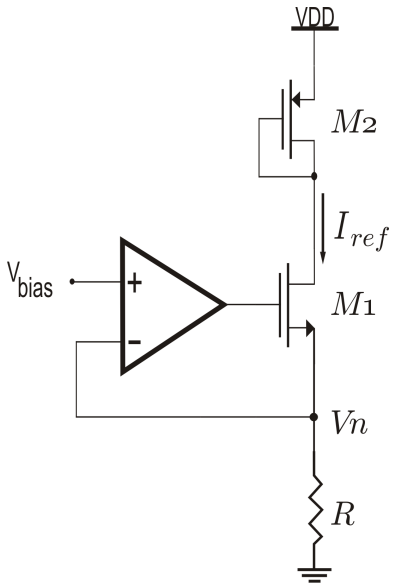

Figure 4.10: Circuit topology used as a current reference for transistor DC biasing.

We first note the use of an operational amplifier whose output voltage regulates the gate voltage of the NMOS device M1. M2 is a diode connected PMOS device used to provide a constant current. If we assume that the gain of the operation amplifier is very large, the reference current denoted as I_{ref} in Figure 4.10 can be found by

$$I_{ref} = \frac{V_{bias}}{R} \tag{4.7}$$

where R is the resistor shown in Figure 4.10 and V_{bias} is assumed to be a temperature independent reference voltage provided by a voltage reference circuit. With this assumption and equation (4.7) we can see that I_{ref} should remain constant with changing temperatures. In order to use this reference

current to bias the gate of a transistor, another PMOS device (M3) is used to implement a current mirror with M2. As shown in Figure 4.11, M3 sinks the mirrored current into a diode connected NMOS device (M4) providing the desired bias voltage V_G.

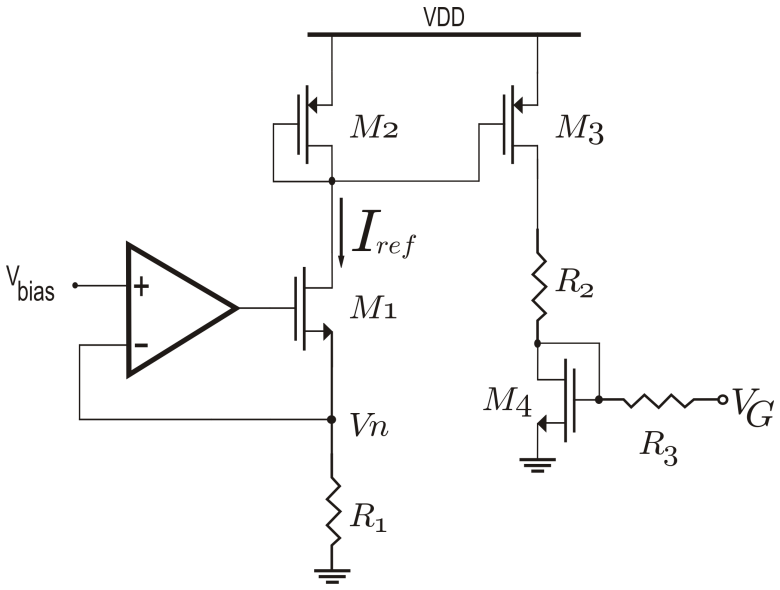

Figure 4.11: Current reference circuit including current mirror PMOS and NMOS devices for providing a gate bias voltage.

The goal of the bias circuitry is to provide a variable or programmable bias voltage. With variable bias voltages the LNA can operate in different gain modes and different IIP3 modes. The latter will be discussed in more detail in Section 4.3.1. The different gain modes can be achieved by varying the gate voltage on the cascode device as well as the common source device. The latter is avoided since drastic changes in the gate bias on the common source device will alter the matching conditions.

The complete bias circuitry is shown in Figure 4.12 where binary weighted PMOS devices forming current mirrors similar to M3 are used. To vary the current that these devices sink into M4, PMOS switches are used in order to turn on/off any given branch. The binary voltage levels, high/low, used for the PMOS switches are 1.2V and 0V, respectively. Transmission gate type switch, which uses a binary signal, is used to either provide the bias voltage ($Vcascode$) to the gate of the cascode device or shunt it to ground. In the case of common source biasing, eight transmission gates are used for the eight different transistors that compose the common source stage as depicted in Figure 4.2.

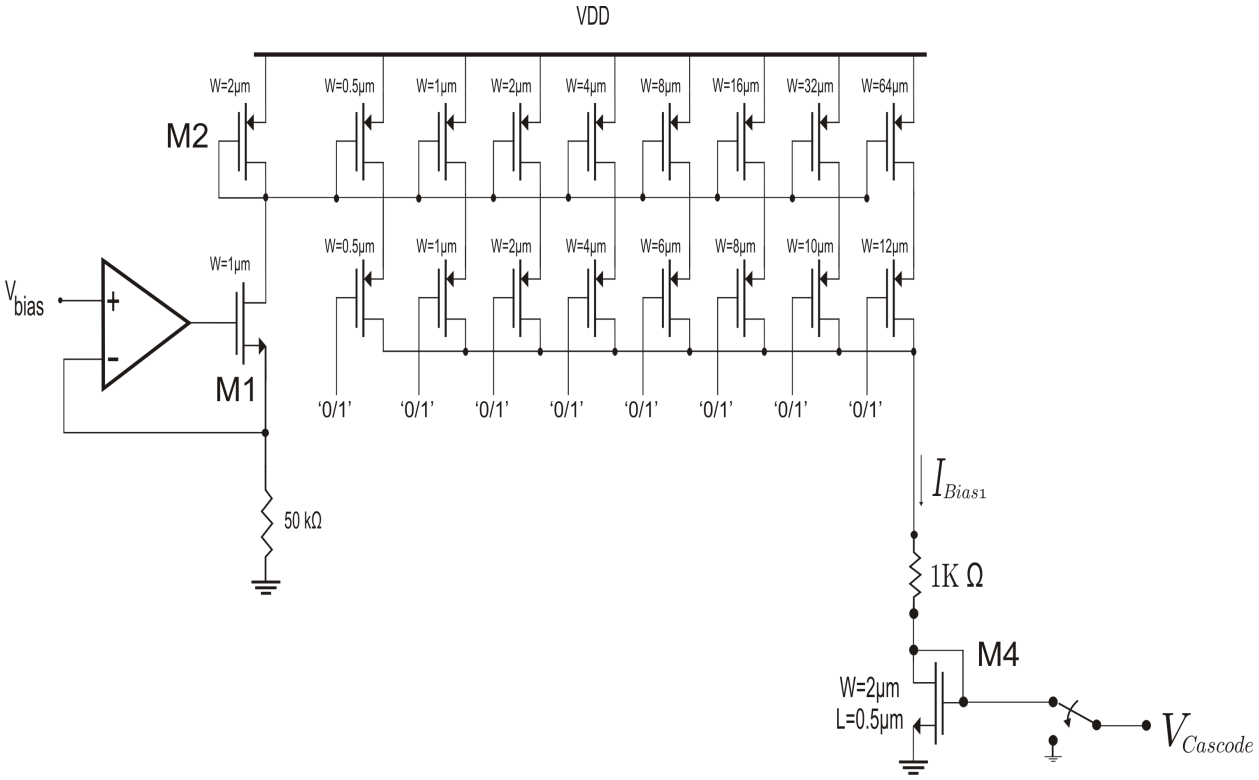

Figure 4.12: Complete cascode bias circuitry employing binary weighted PMOS devices and on/off switches.

Figure 4.13 shows the change in $V_{Cascode}$ as the 8-bit word written to the PMOS switches is swept from its maximum value to its minimum value. For ease of presentation, the 8-bit word is coded into an integer value, these values form the x-axis in Figure 4.13. Note the use of inverse logic in this case since the switches are PMOS devices.

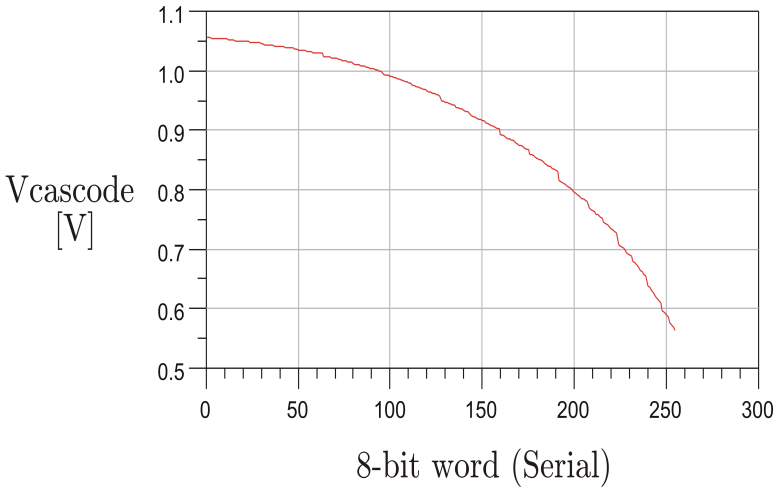

Figure 4.13: Casocde bias voltage vs. serial programming bits. The X-axis represents the serial integer representation of the 8-bit word.

4.2.6 Input RF Switching

Input RF switches perform a multiplexing operation where one signal path is turned on and the others are off. As shown in Figure 4.1, the switches take in a programming binary word, which designates the band of operation, and provides a signal path accordingly. The proposed architecture uses three signal paths for the targeted four standards. The two low frequency standards (IS-95 and GSM) use one path, and consequently use the same off-chip matching inductor. It was observed during the design and simulation process results that a single off-chip matching inductor is sufficient in providing the required matching for both bands.

The RF switches are implemented using an NMOS device in a common-gate configuration as shown in Figure 4.14. A DC bias voltage is applied

to the drain and source in order to keep the Drain/Bulk and Source/Bulk junctions reverse biased all all time, especially in the presence of strong RF signals.

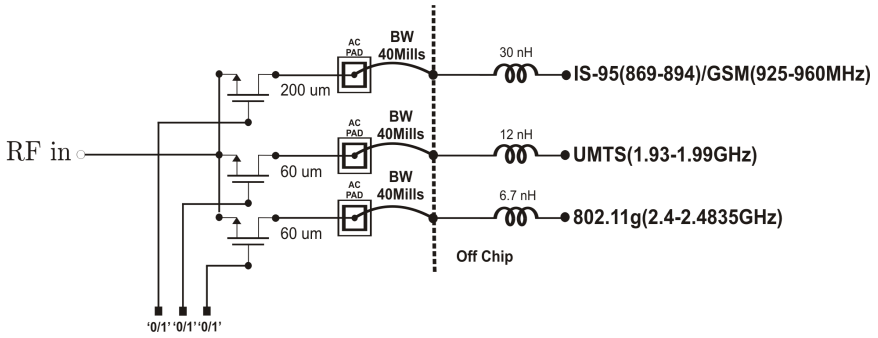

Figure 4.14: NMOS RF input switches (biasing not shown) and off chip inductors.

4.3 Linearity Performance

The linearity performance of an LNA is crucial to the overall performance of RF receivers . Today's wireless and mobile devices operate in the presence of many different, but coexisting, wireless standards which tends to complicate the task of selective and accurate reception of a narrowband signal. A good example would be a CDMA device receiving a signal in the presence of a GSM narrowband jammer. These jammers can be very close to, if not in, the receiving band of a CDMA receiver. CDMA systems operate in a full-duplex mode allowing the transceiver to receive and transmit at the same time. This requires the use of duplexers which have finite isolation between transmit (TX) and receive (RX) sides; thus, TX leakage into the receiving

path introduces another undesirable signal injected into the input port of the LNA. The sensitivity of receivers is directly coupled to the amount of thermal noise present in the receive path. This total thermal noise is the noise generated by the TX side of the transceiver and the noise generated by the RX itself. TX noise level in the receive band is typically around -135 dBm/Hz and duplexer isolation in the RX band is typically 40dB, which translates approximately to -114 dBm of added noise power from the TX in the RX band

The presence of such undesired signals coupled with the non-constant envelope nature of CDMA signals and the non-linear transfer characteristics of an LNA distort the desired signal and produce intermodulation components, which could ultimately prevent accurate data reception. Figure 4.15 depicts the situation described in the front end of a CDMA RF transceiver working in full-duplex mode.

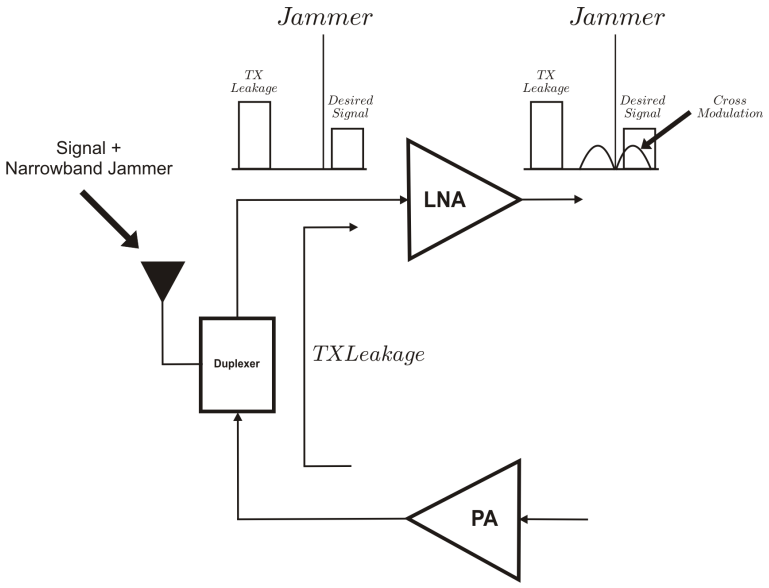

Figure 4.15: Illustration of cross modulation distortion in a CDMA transceiver [63] .

The measure of linearity performance in small signal amplifiers such as LNA's is the IP_3 as discussed in Section 2.3.2. Several techniques have been developed for the purpose of peaking the IP_3 in high frequency small signal amplifiers. Some techniques are more suitable than others depending on the application and the design constraints. Examples of common linearization techniques include linear feedback, analog/digital predistortion, postdistortion, optimum biasing, and non-linear feedback. The optimum biasing, technique is the most suitable and cost effective technique since it does not depend on adding additional hardware components to the existing circuit. Theoretically, this method depends on exploiting a biasing "sweet spot" developed by Aparin *et al.* in [24] in the FET's small signal transfer char-

acteristics. The following is a detailed analysis of distortion in FET devices and the optimum biasing method.

4.3.1 Distortion in RF CMOS Devices and the Optimum Biasing Technique

Distortion in short-channel CMOS transistors mainly arises from the nonlinear behavior of the device's transconductance. Assuming the common-source NMOS transistor is operated in the saturated mode, we can neglect the drain current's dependence on drain to source voltage, allowing us to write the simple form of the power series relating the small signal drain current i_d to the small signal gate to source voltage as follows [63]

$$i_d(v_{gs}) = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + ..., \tag{4.8}$$

where g_1, g_2, and g_3 represent the first, second, and third order transconductance terms, respectively. Hence, g_1 is the small signal device transconductance and $g_2$and $g_3$define the strength of the second and third order components as discussed in Section 2.3. As mentioned in Section 4.3, the optimum gate biasing technique exploits a biasing "sweet spot" in order to achieve maximum linearity performance. This can be seen by analyzing the behavior of the transconductance terms as a function of DC bias. The three transconductance terms can be derived by differentiating the I_D vs. V_{GS} curve as shown in the following equations [63]

$$g_1 = \frac{\partial I_D}{\partial V_{GS}}, \tag{4.9}$$

$$g_2 = \frac{\partial^2 I_D}{\partial V_{GS}^2}, \tag{4.10}$$

$$g_3 = \frac{\partial^3 I_D}{\partial V_{GS}^3}. \tag{4.11}$$

It is worth noting that only the first three terms are considered since the device will be operated under small signal conditions, which are typical for RF LNAs. Hence, higher order terms can be neglected. To view the characteristics of these transconductance terms as a function of gate bias, a common source NMOS FET is used with no source degeneration, V_{DS} is set to approximately 0.7V, and V_{GS} is swept from 0V to 1V. As described in [63], the extraction of these transconductance terms from the discrete data will result in unacceptable errors, hence a continuous semi-imperical model of I_D vs. V_{GS} is first fitted to the discrete data. Details about this model can be found in [24] and [23]. Using the fitted curves, the transconductance terms can be found using equations (4.9), (4.10), and (4.11). The results are shown in Figure 4.16

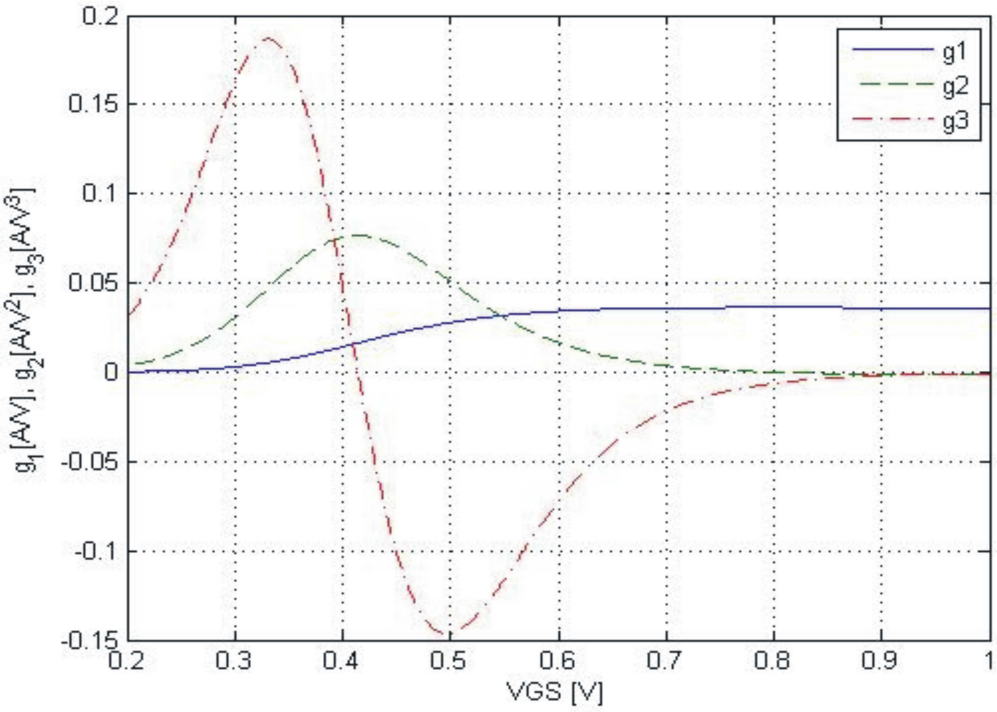

Figure 4.16: First, second, and third order transconductance terms extracted from I_D *vs* V_{GS}curve for a FET with dimensions of: $W = 50\mu m$ and $L = 0.13\mu m$. $V_{DS} = 0.7V$.

A theoretical figure for tone amplitude at the intercept point in V can found as [7]

$$AIP_3(V) = \sqrt{(\frac{4}{3}|\frac{g_1}{g_3}|)} \tag{4.12}$$

Using (4.12) we can plot the theoretical AIP_3 in (dBV) as shown in Figure 4.17.

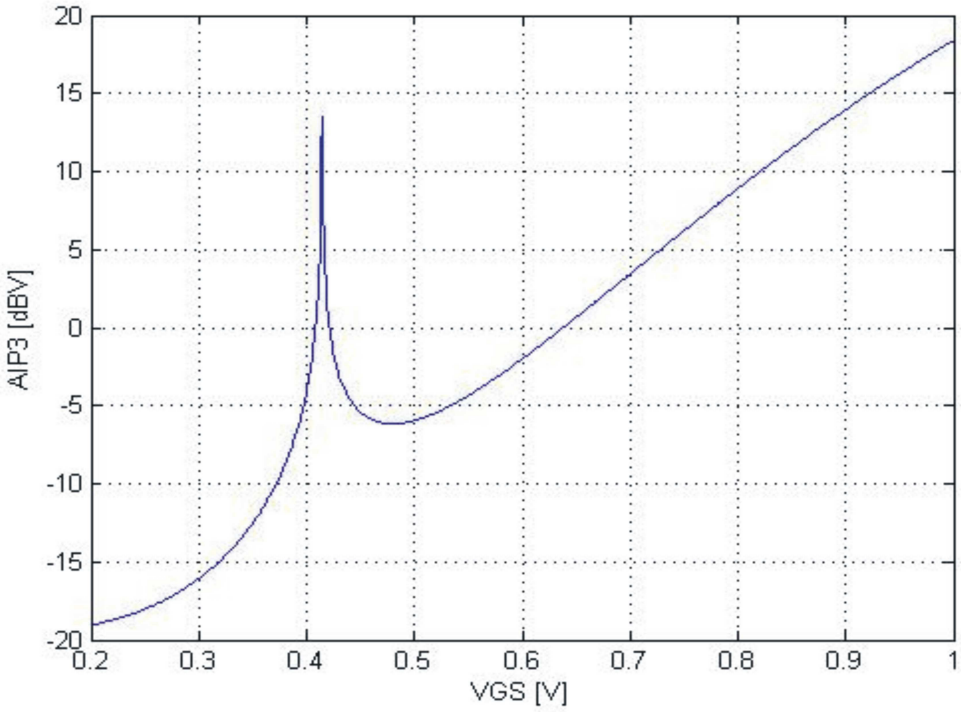

Figure 4.17: Theoretical IIP_3 curve in dBV at DC as a function of V_{GS} for a width of $50\mu m$ and length of $0.13\mu m$

The analysis in DC shows that a very high IIP_3 can be obtained by tuning the gate voltage of the common source device to a value that nulls the third order transconductance term g_3 and provide infinite IIP_3. As might be expected, deviating behavior occurs when operation frequencies rise. The source degenerating inductance L_S , used for input matching in the common source LNA, provides a feedback path from the source terminal to the gate. This feedback path allows second order components of the drain current, generated by $g_2 v_{gs}^2$, to mix with the fundamental v_{gs} component at the gate

of the device, consequently adding to second and third order components of the drain current [63]. Therefore, simply tuning the gate voltage to the point where the g_3 component of the drain current is nulled does not significantly improve the IIP_3 performance of the FET.

Intuitively, reducing second order harmonics components that are fed back into the gate of the common source FET would entail a reduction in the amount of source degeneration, which translates into minimizing the inductance at the source ($L \rightarrow 0$). However, inductances smaller than $0.5nH$ are not feasible using bondwires. On the other hand, due to the tunability requirements of the design, such a small inductance would not provide proper matching over the entire frequency band, especially at the low end of the band. The theoretical IIP_3 that can be achieved as a function of L_S can be seen in Figure 4.18. It is clear from such an analysis how the peak IIP_3 is reduced and also shifted due to increasing source degeneration.

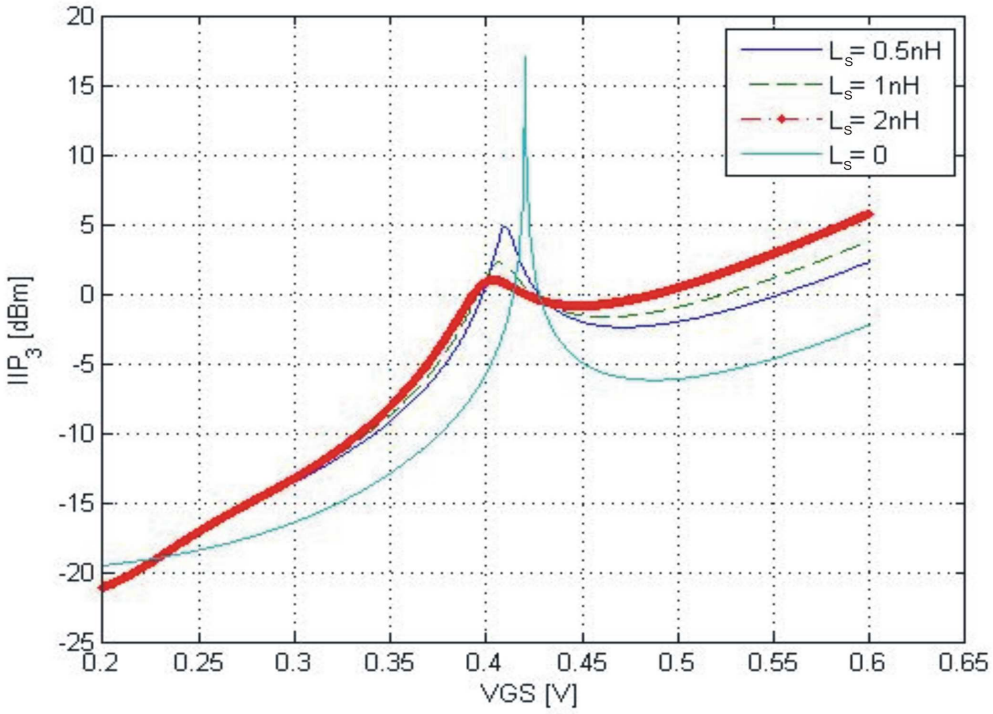

Figure 4.18: Theoretical IIP_3 curves as a function of FET source degeneration at $f = 900MHz$.

Since the IIP_3 performance at high frequencies is degraded by the second order harmonics in the drain current, it is possible to tune the common source FET's terminal impedances at the second harmonic frequencies in order to zero out the second order harmonics. In the case of cascode LNA, the impedance presented to the device at the drain is the impedance seen looking into the cascode device $Z_3(\omega)$. The impedance presented to the gate of the device is what the common source device sees after the input matching network, and this will be labeled $Z_1(\omega)$. The effect of varying $Z_1(2\omega)$ on the

theoretical IIP_3 can be see in Figure 4.19.

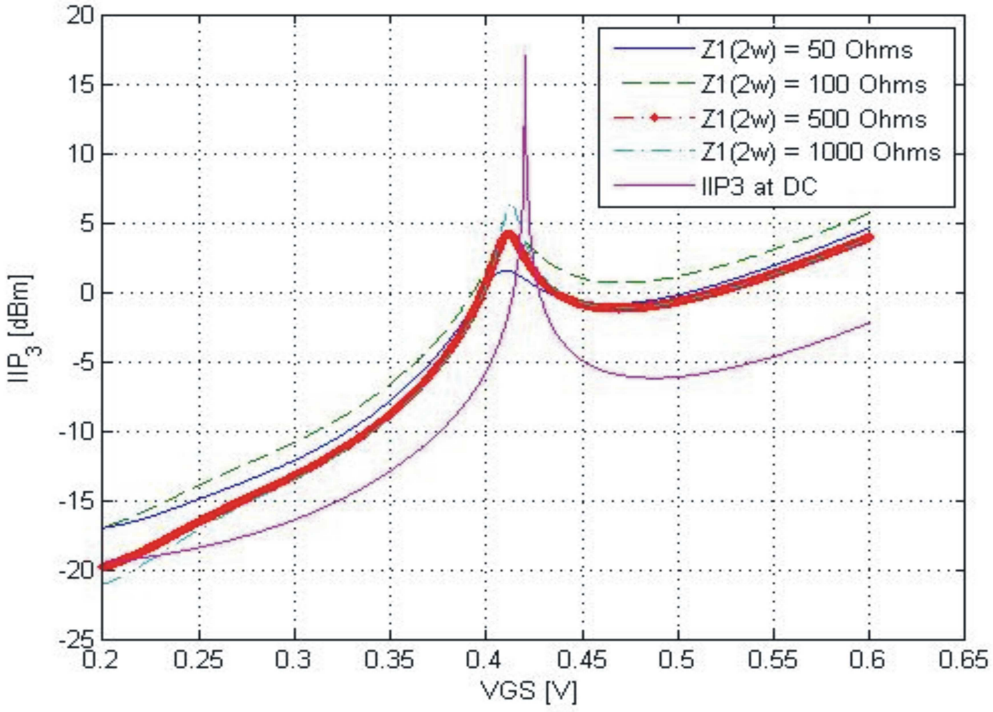

Figure 4.19: Theoretical IIP_3 curves as a function of $Z_1(2\omega)$ for $L_S = 1nH$

Reducing the effect of the second order harmonics requires the use of the Voltera series to characterize the transfer characteristics of the FET. This detailed analysis, along with all the underlying assumptions, can be obtained from [63] or [25] where analytical expressions for IIP_3 are derived in terms of device parameters and terminal impedances for the common source FET. From a designer's point of view, the presence of C_{gd} provides another feedback path for the second order drain current to the gate terminal of the FET. As a result, even zeroing the source degeneration does not completely limit

this feedback mechanism. Also, there is little flexibility in tuning $Z_1(2\omega)$ since this terminal impedance is mainly designed to optimize the noise figure performance and power transfer to the device. Hence, $Z_3(2\omega)$ is the most practical terminal impedance that can be tuned to cancel the contribution of the second order terms of the drain current contribution to the third order distortion terms. In [63], this is done by using a bypassing capacitance at the gate of the cascode device. The fact that the LNA designed in this work operates in different frequency bands makes the choice of an optimum fixed gate capacitance almost impossible. The idea of using a switched capacitor network to provide a variable capacitance in this case is avoided mainly due to the quality factor of such a network, which would prove to be unsatisfactory for such an application. The quality factor also is degraded due to the small value of capacitance required, usually smaller than 0.1 pF in some bands. A MIM implementation of such a capacitance tends to have poor quality factors. Using several iteration in the simulation process allows us to find a practical capacitance value that will tune the cascode device impedance at the second harmonic frequencies as close as possible to the desired value. A 0.1 pF on-chip MIM capacitor is used at the gate of the cascode device for this purpose. Simulation results for the IIP_3 will be presented in Chapter 5.

Chapter 5

Simulation Results

5.1 Baseline Simulation Results

Figure 5.1 shows simulations results in ADS for the voltage gain and S11 behavior for each mode of operation. The simulation results for noise figure are shown in Figures 5.2 and 5.3. Specifically, Figure 5.2 shows the noise figure plots for the IS-95 and GSM mode of operation, while Figure 5.3 shows the noise figure plots for UMTS and WLAN modes of operation.

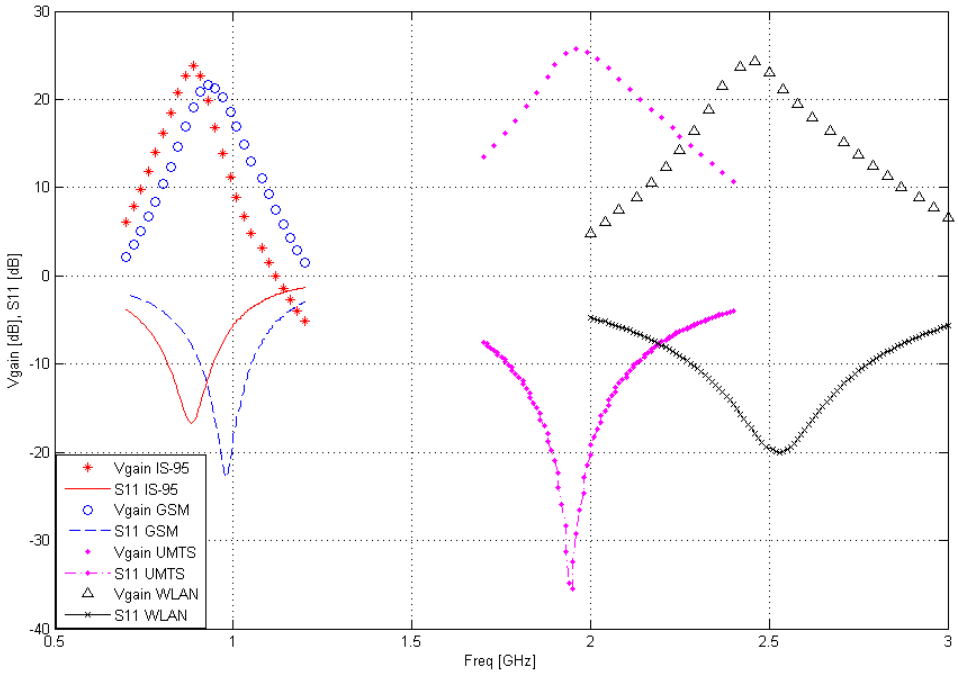

Figure 5.1: LNA baseline simulation results: voltage gain and S11 for IS-95, GSM, UMTS, and WLAN.

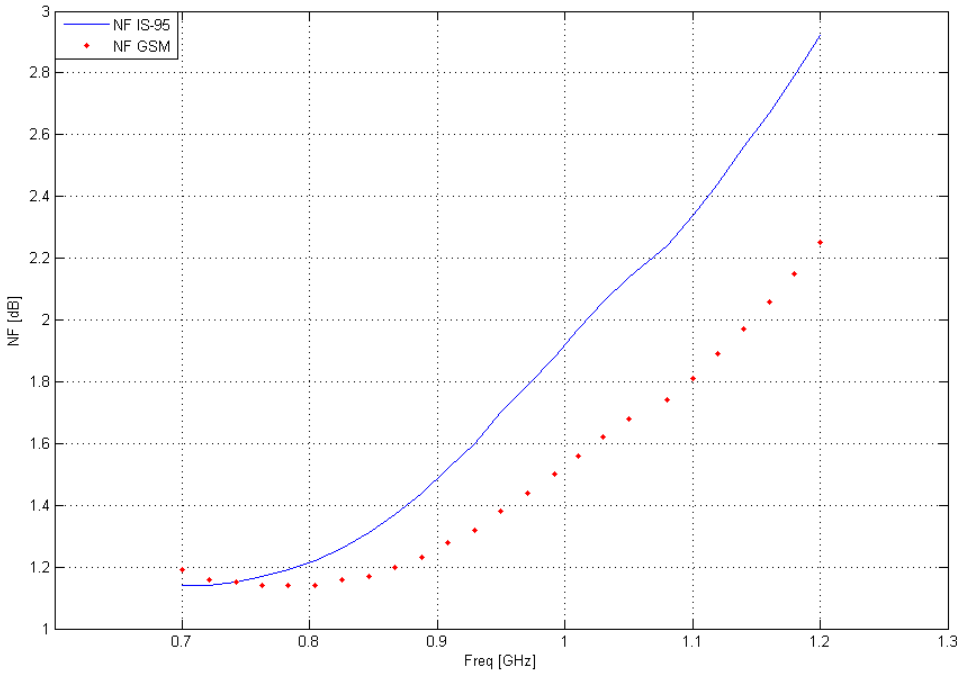

Figure 5.2: LNA baseline simulation results: noise figure (NF) for IS-95 and GSM bands.

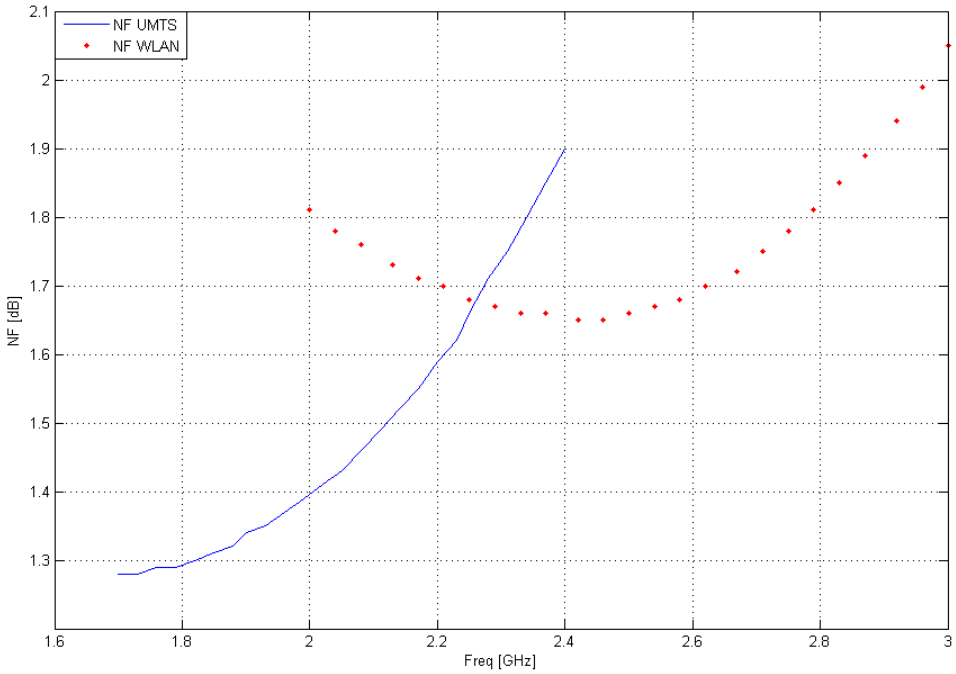

Figure 5.3: LNA baseline simulation results: noise figure (NF) for UMTS and WLAN bands.

The following figures show the simulation results for the third order intercept point for each mode of operation.

We can see from the results illustrated above that the LNA meets the general requirements listed in Table 4.1 in terms of voltage gain, noise figure, and input return loss in all of the four bands that were designated as design targets. The LNA provides sufficient voltage gain, more than 20 dB, across the operational bandwidth and exhibits a noise figure under 2 dB while consuming no more than 4mW of power. Third order intercept points fall well

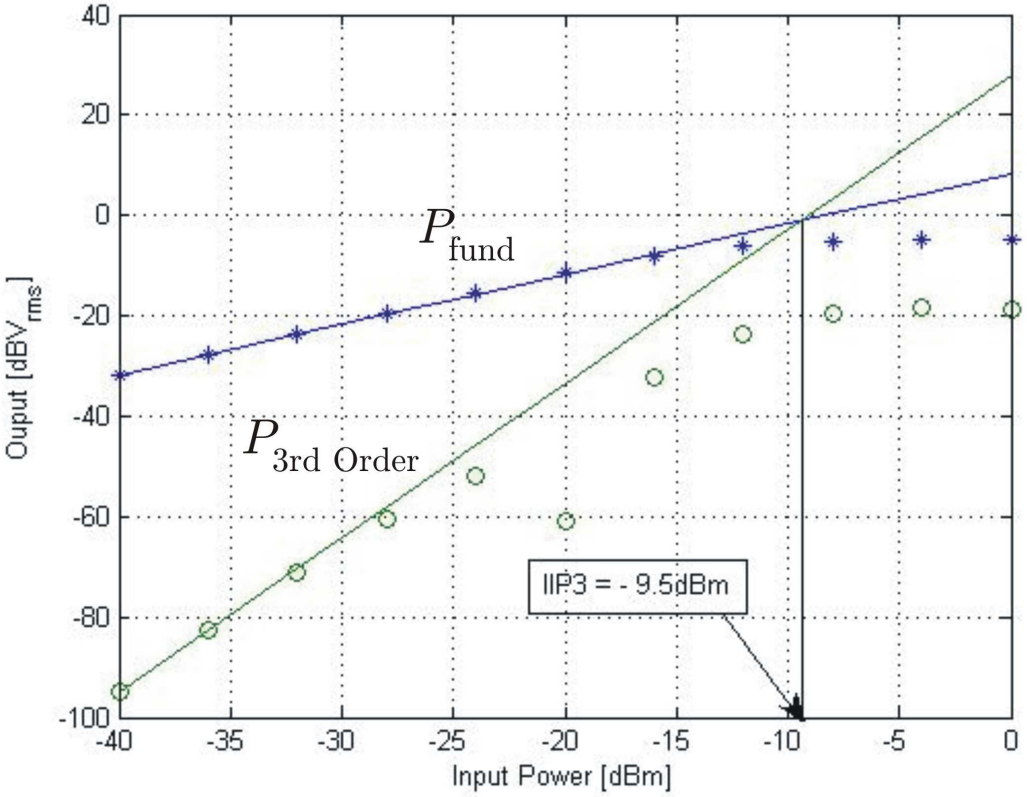

Figure 5.4: Simulated IIP3 point at 880MHz.

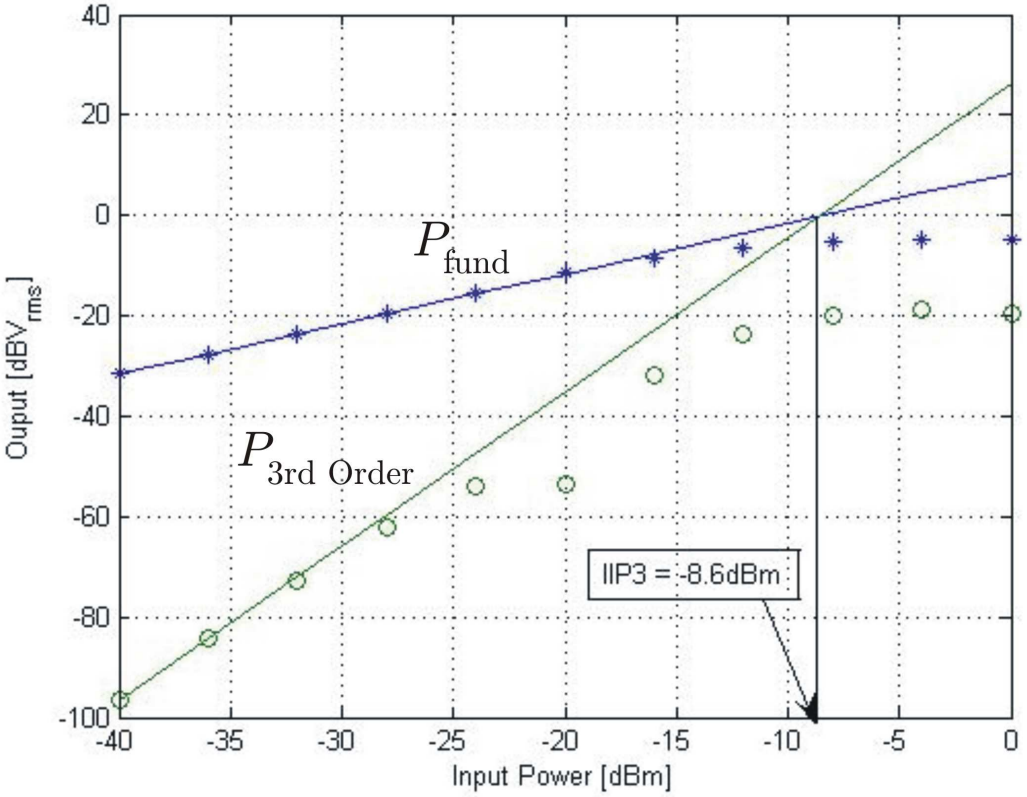

Figure 5.5: Simulated IIP3 point at 930MHz.

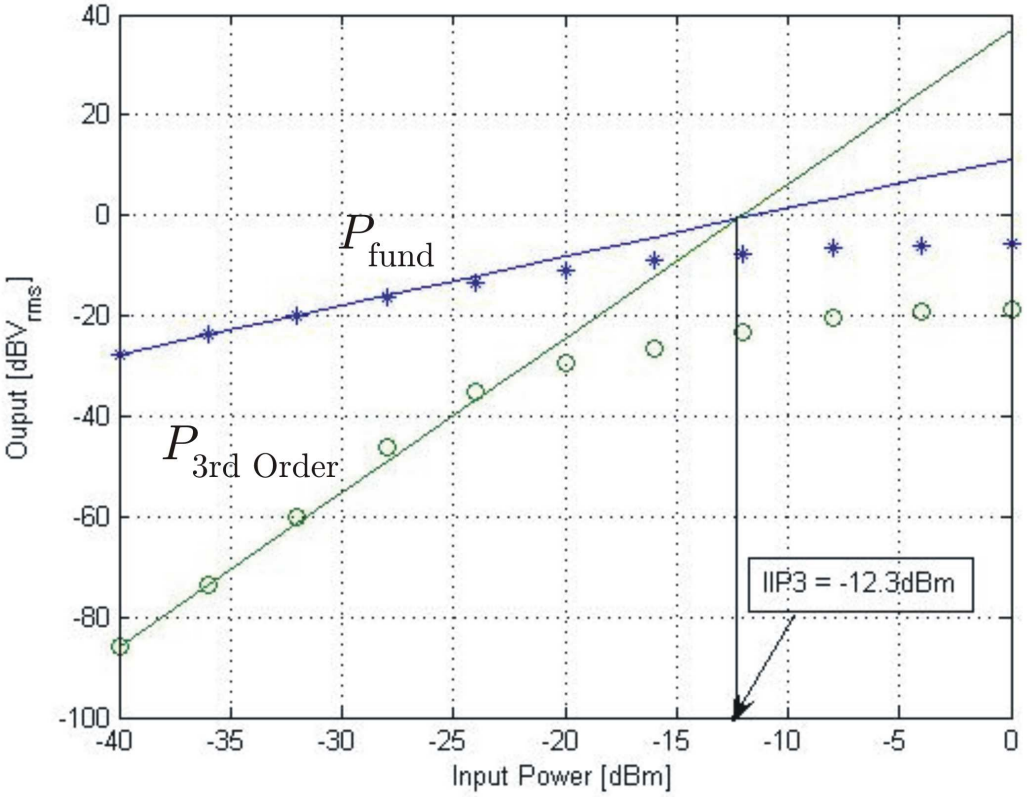

Figure 5.6: Simulated IIP3 point at 1960MHz.

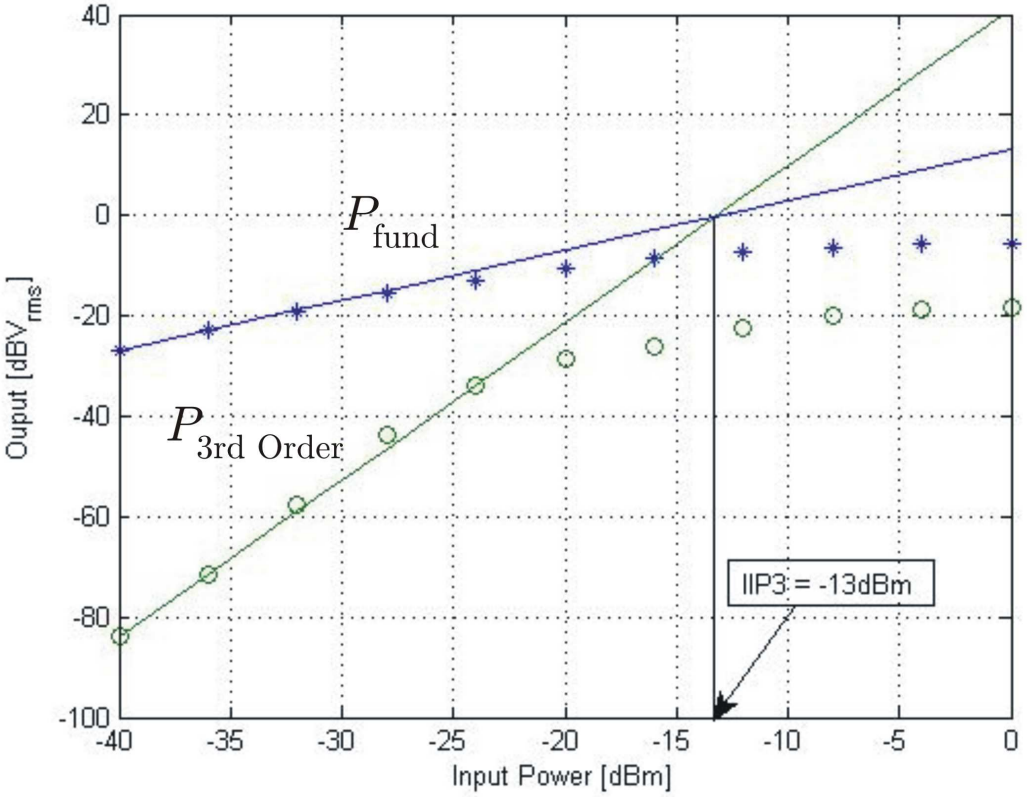

Figure 5.7: Simulated IIP3 point at 2440MHz.

around the specification set in Table 4.1, although these intercept points fall 2 or 3 dB short in the UMTS and WLAN bands. In the UMTS band, the IIP_3 point can be improved by raising the power consumption of the LNA by increasing the common source device's gate voltage and reducing the device width. This approach is followed in [25]. An IIP_3 point of -12.3 dBm was obtained while consuming 2.6 mW of power, which gives plenty of room to increase the drain current of the common source device to improve IIP_3 performance. An IIP_3 of -13 dBm is quite respectable for a cellular standard, and it is sufficient for WLAN applications since such standards put more emphasis on bandwidth than linearity.

5.2 Tuning

Results of tuning the programmable LNA are presented in Figures 5.8, 5.9, 5.10, and 5.11. In the UMTS and WLAN modes of operation, tuning was performed using the switched capacitor networks at the input and of the LNA. Capacitor switching at the input works primarily to alter the input match of the LNA. For each value of capacitance that the input switched capacitor network produces (C_p), the output LC tank is tuned using the switched capacitor network at the drain of the cascode NMOS device as described in Section 4.2.4. For IS-95 and GSM standards, C_p was tuned to give an equivalent capacitance between 0.1 pF and 1.3 pF. Tuning C_p in the UMTS and WLAN modes of operation swept the equivalent capacitance between 0

pF and 0.7 pF. The result of sweeping C_p and the output tank capacitance yields a family of voltage gain curves as well noise figure curves along with S11 curves. Figure 5.8 and 5.10 show the voltage gain curves and S11 curves as a result of the tuning for UMTS and WLAN modes, respectively. The effect of tuning on the noise figure performance is shown in Figures 5.9 and 5.11 for the UMTS and WLAN modes of operation, respectively. These results clearly illustrate the tunability of the LNA which serves, several purposes. From Figure 5.8 we can see how the LNA can be tuned to operate in lower frequencies while it is in the WLAN mode of operation. This allows the LNA to support communication standards operating at a frequency as low as 1.8 GHz. This proves to be very useful especially since many mobile and wireless communication standards, not accounted for in the initial design of the LNA, can now be included as other modes of operation, such as DCS1800. Tunability also proves crucial when dealing with process variations, which can easily alter the nominal center frequencies which the LNA had been designed for. Results of tuning in the IS-95 and GSM modes of operation are presented in Appendix A.

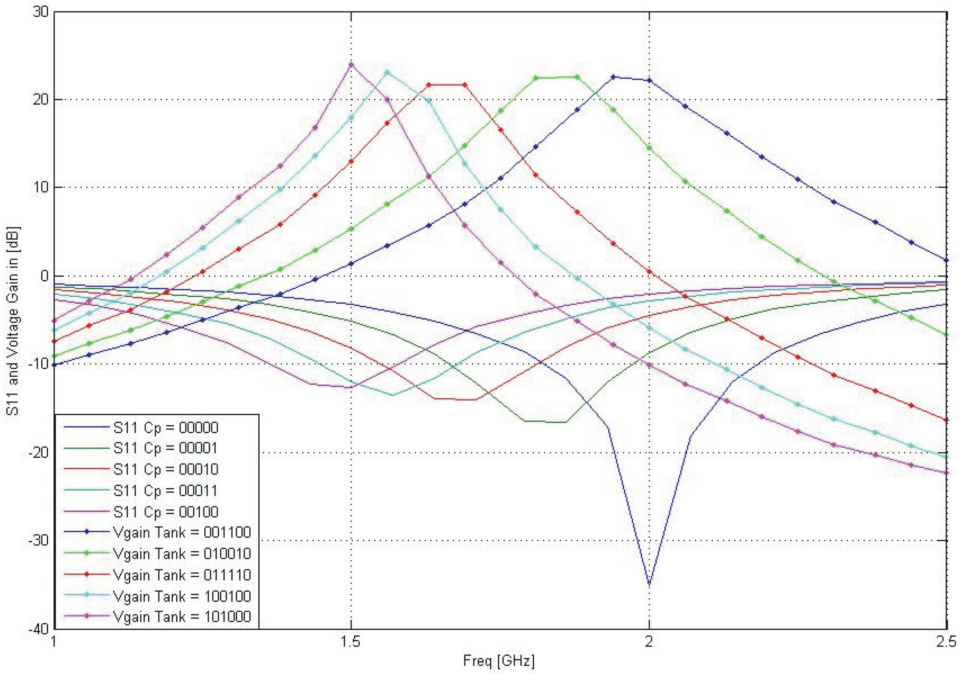

Figure 5.8: Simulation results for voltage gain and input match tuning in the UMTS mode of operation.

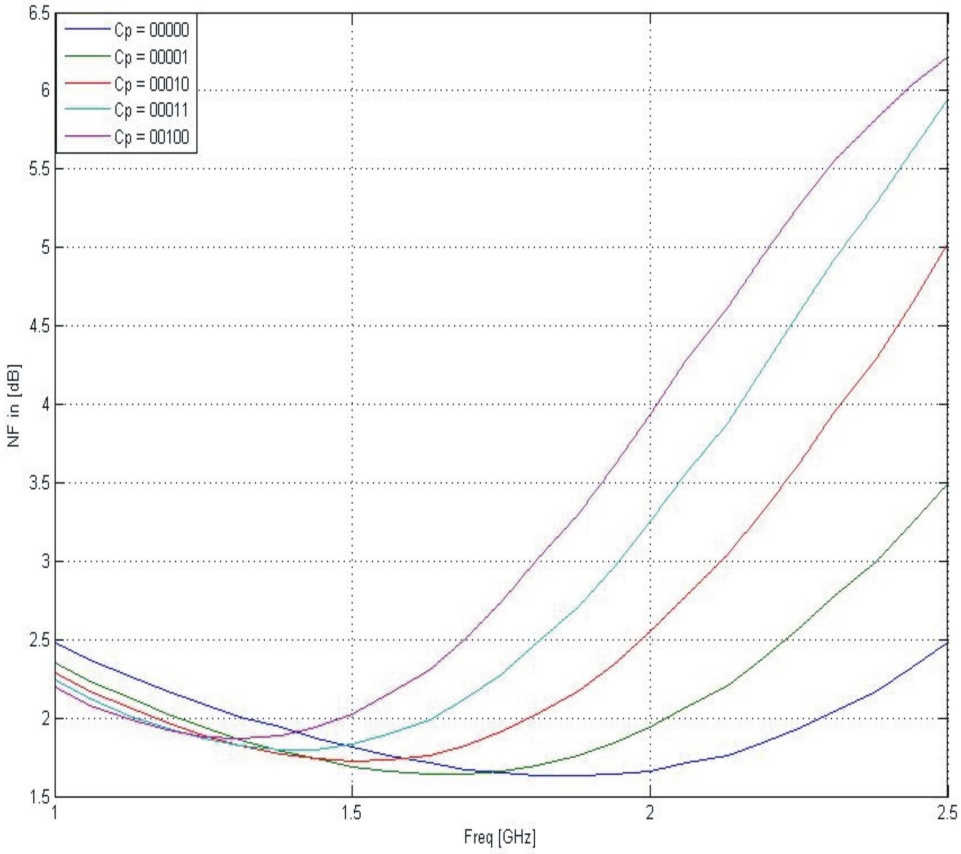

Figure 5.9: Simulation results for noise figure (NF) as C_p is varied in the UMTS mode of operation

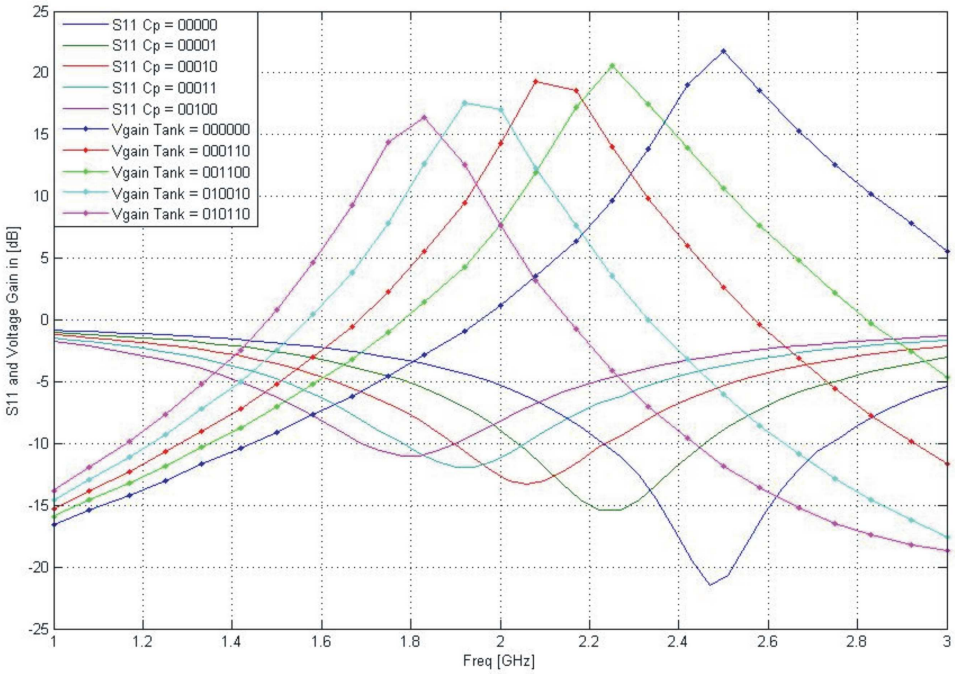

Figure 5.10: Simulation results for voltage gain and input match tuning in the WLAN mode of operation.

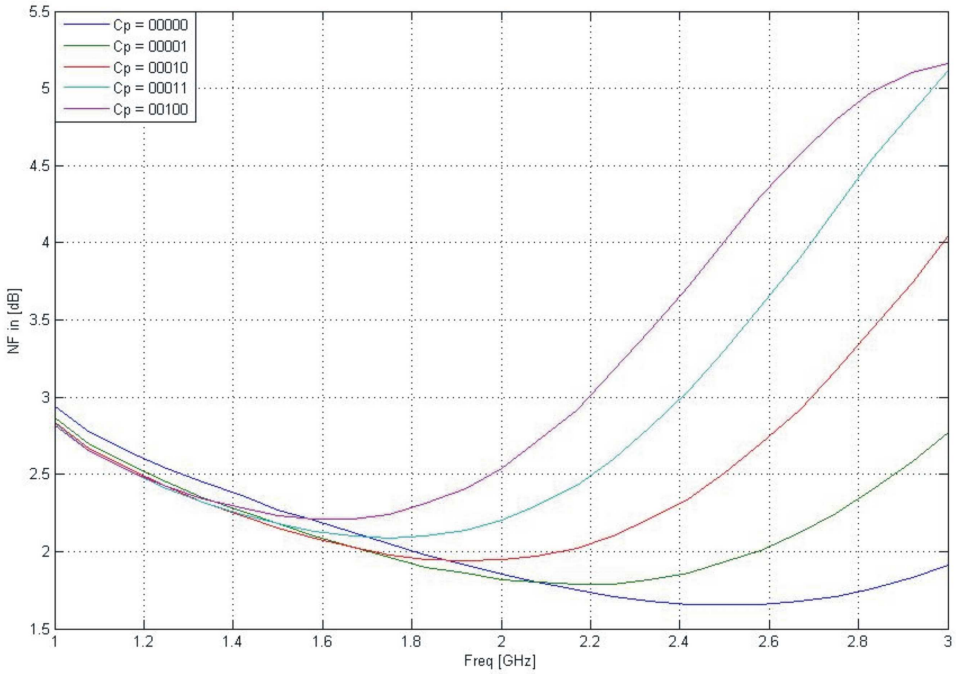

Figure 5.11: Simulation results for noise figure (NF) as C_p is varied in the WLAN mode of operation.

Table 5.1 summarizes the overall performance of the programmable LNA.

	IS-95	GSM	UMTS	WLAN
Voltage Gain (dB)	23	22	25	24
Noise Figure (dB)	1.4	1.35	1.37	1.65
S11 (dB)	-16	-22	-35	-20
IIP3 (dBm)	-9.5	-8.6	-12.3	-13
Power (mW)	3.9	3.7	2.6	1.96

Table 5.1: Summary of programmable LNA performance specifications.

Chapter 6

Conclusions

RF/MW transceiver ICs are currently being designed for multiband and multistandard operations in order to support more and more communication standards and protocols. Low-noise amplifiers are a crucial component in today's communication circuits. Traditionally, RF/MW transceiver ICs supporting multiband and multistandard operations have relied on a parallel structure of narrowband transceivers, each dedicated to a single band of operation. This approach proves to be rather space consuming and not cost effective especially with mobile devices. The idea of software defined radio (SDR) [57] shows great potential as a radical and extremely efficient approach to tackling the multiband and multistandard transceivers IC challenge. Realizing a true SDR in real time represents a tremendous challenge in itself, since RF/MW circuits are required to operate in a very wide frequency band, while maintaining proper functionality which complies with the designated

standard of communication.

Low-noise amplifiers are key components in any communication circuit. This thesis work presents a tunable LNA in 0.13 μm CMOS technology designed as an integral part of an SDR intended for mobile communication between 0.7 GHz and 2.5 GHz. The developed design builds on the traditional inductively degenerated common-source cascode structure, and introduces key mixed-signal design techniques in order to perform tuning over a wide range of frequencies. Simulations performed in ADS show the functionality of the programmable LNA in the four targeted bands of operation. Further simulations have also shown the wide range of tunability that this LNA can achieve in each mode of operation.

Overall, the programmable LNA presented in this thesis showcases a balance in overall performance. All major specifications have been met, and at power consumptions that are well within the typical budgets that are assigned for such applications. The LNA almost covers the entire frequency band between 0.7 GHz and 2.5 GHz, with the exception of the band located between 1.1 GHz and 1.5 GHz. Covering this band requires no more than a simple extension by adding another off-chip inductor that would provide the impedance matching at this band; in this case the LNA would have four inputs instead of three. Expanding operations to frequencies higher than 2.5 GHz is also a simple extension requiring more off-chip inductors. Using the design and configurations presented in this work, the LNA can easily support operations up to 5 GHz. Future work and other consideration can include

the following

1. Design the cascode (common-gate) gate device of the LNA similar to the common source device in an effort to allow more flexibility in terms of DC biasing as well as reducing the loading effects on the common source device.

2. Explore matching networks with multiple resonances, this reduces the amount of off-chip components and allows for concurrent modes of operations [55].

3. Employ other techniques for the purpose of linearizing the cascode LNA, since further distortion analysis on the cascode LNA at frequencies higher than 3 GHz shows that the optimum gate biasing technique provides little if no advantage at all over other linearization techniques. An example of other techniques include the one outlined in [26] in which the cascode LNA is linearized by choosing the smallest common source device width possible that can provide the required transconductance, and using the highest gate overdrive voltage possible.

4. Extend the flexibility and the fine tuning capabilities of matching networks and resonating tanks via the use of on-chip varactors.

5. Explore the folded-cascode architecture in which a PMOS FET is used as the common base device. This architecture is an attractive alternative due to the ongoing reduction of the core voltages used in today's

advanced CMOS technologies. For a classical cascode LNA, this translates to lower overhead voltage and thus less signal swing range, which ultimately reduces the linearity of the LNA. The folded-cascode architecture is well suited to handle to handle this situation.

Appendix A

Tuning Simulation Results

A.1 IS-95 and GSM

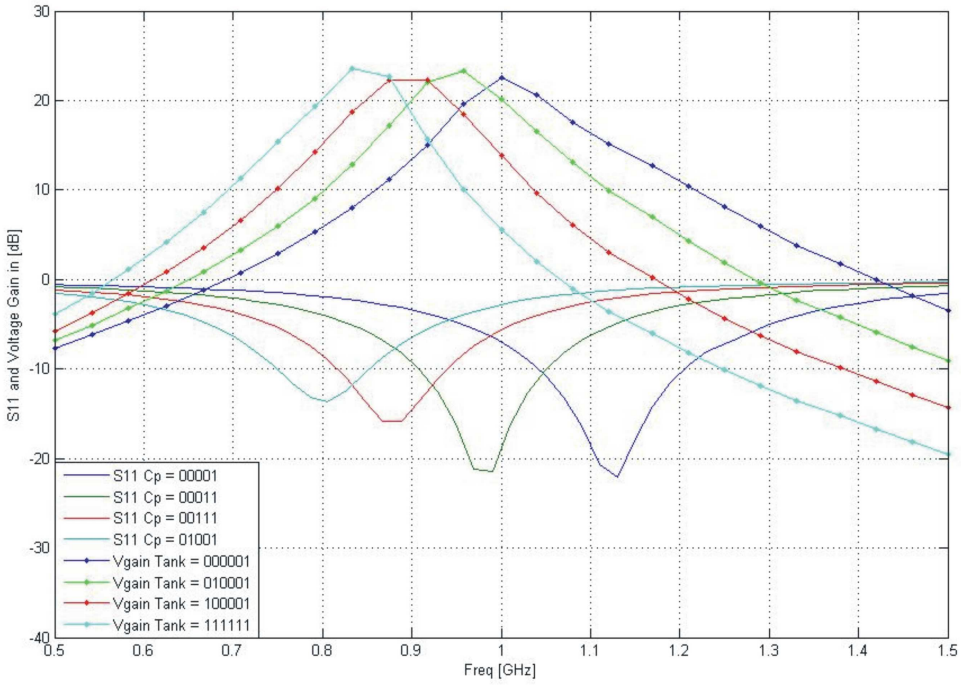

Figure A.1: Simulation results for voltage gain and input match tuning in the IS-95 and GSM modes of operation.

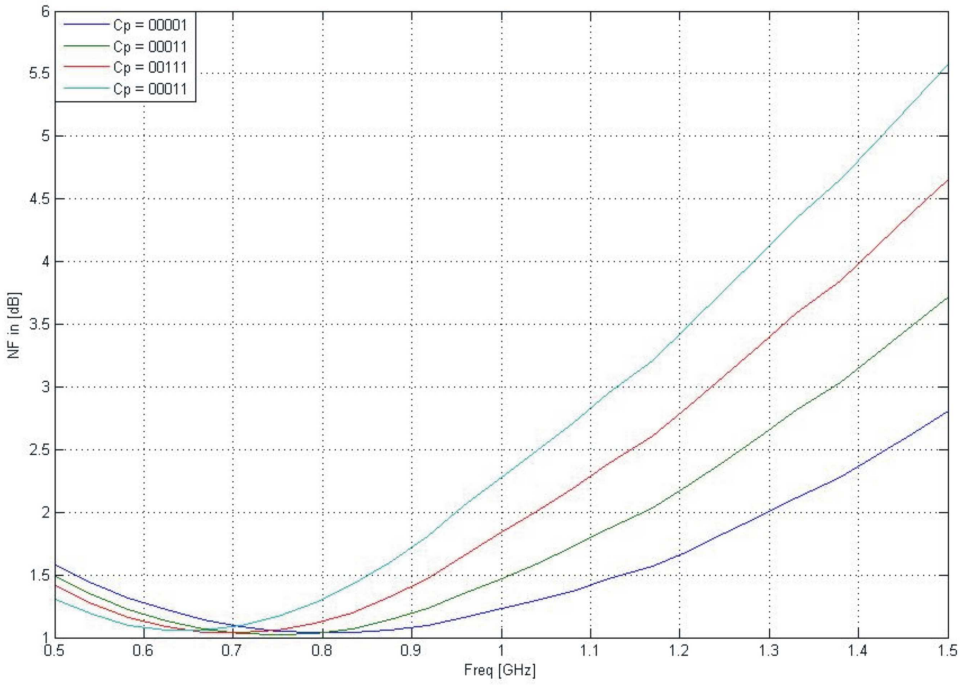

Figure A.2: Simulation results for noise figure (NF) as C_p is varied in the IS-95 and GSM modes of operation.

Appendix B

Circuit Component Models

B.1 AC Pad with Shielding

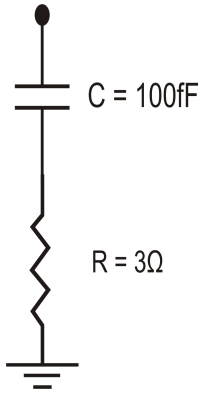

Figure B.1: AC Pad with Shielding model

B.2 DC Pad

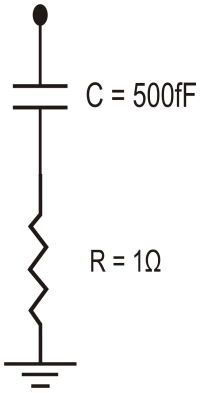

Figure B.2: DC pad model

B.3 Bondwires

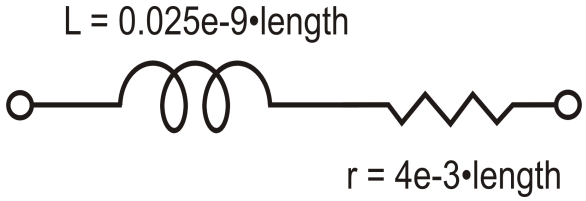

Figure B.3: Bondwire model

B.4 BSIM3v3.24 ADS Model Parameters

B.4.1 NMOS Parameter File

; Translated with ADS Netlist Translator (*) 270.500 Sep 21 2004

;

```
model n_12_hsl130e MOSFET Version=3.24 Mobmod=1 Capmod=3
Nqsmod=0 Binunit=2 Tnom=25 Xl=0 \

Xw=0 Llc=1.4e-015 Lwc=0 Lwlc=0 Wlc=0 Wwc=0 Wwlc=0
Tox=2.73e-009 Toxm=2.73e-009 Wint=3.5e-008 \

Lint=1.41e-008 Dlc=1.4e-008 Dwc=4e-015 Hdif=1.25e-007 Ldif=9e-008
Ll=-7.592e-016 Wl=0 \

Lln=1 Wln=1 Lw=0 Ww=-5.4e-015 Lwn=1 Wwn=1 Lwl=0 Wwl=0
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Xpart=1 Vth0=0.2365 K1=0.3339 K2=-0.0407 K3=18 K3b=10.8
Nlx=1.4812e-007 Dvt0=6 Dvt1=2 \

Dvt2=0 Dvt0w=0.01 Dvt1w=1e+008 Dvt2w=0 Nch=1.7e+017 Voff=-0.12
Nfactor=0.7371 Cdsc=0.00024 \

Cdscb=0 Cdscd=0.00024 Cit=0 U0=0.03621 Ua=1e-010 Ub=1.0248e-018
Uc=9e-011 Ngate=1e+021 \

Xj=1.05e-007 W0=2.5e-006 Prwg=0 Prwb=0 Wr=1 Rdsw=100 A0=1.175
Ags=0.7 A1=0 A2=1 B0=1e-005 \

B1=0.0001 Vsat=105000 Keta=-0.015 Dwg=0 Dwb=3e-008 Pclm=1.325
Pdiblc1=1.1548e-007 Pdiblc2=0.045 \

Pdiblcb=-0.32 Drout=1 Pvag=0 Pscbe1=4.24e+008 Pscbe2=1e-005
Delta=0.0113 Eta0=1 Etab=-0.3 \
```

Dsub=1.5 Elm=5 Vfb=-0.93677 Clc=1e-007 Cle=0.6 Cf=0 Ckappa=0.6
Cgdl=0 Cgsl=0 Vfbcv=-1.5 \

Acde=0.3 Moin=10.65 Noff=1 Voffcv=-0.03285 Kt1=-0.3235 Kt1l=5e-009
Kt2=-0.036 Ute=-1 \

Ua1=4.7e-009 Ub1=-5.1e-018 Uc1=-5.9e-011 Prt=-76 At=43000 Noimod=2
Noia=1.58e+019 Noib=113720 \

Noic=-1.73e-014 Em=26036000 Ef=0.9701 Rsh=7 Js=6.73e-006
Jsw=7e-012 Cj=0.000722 Mj=0.264 \

Cjsw=9.93e-011 Mjsw=0.105 Pb=0.62 Rdc=0.3 Rsc=0.3 Xti=3 Nj=1.2
NMOS=1 PMOS=0 Idsmod=8 \

Vbm=-3.0 Lvth0=-1.3e-009 Wvth0=4.55e-010 Pvth0=6.7e-017
Lk2=-9e-010 Wk2=-2e-009 Lk3=1.8e-006 \

Wk3=-9.6e-006 Lk3b=-3e-006 Wk3b=1e-006 Lnfactor=4.5e-007
Wnfactor=-6.545e-008 Pnfactor=-4e-014 \

Lu0=5.0325e-010 Wu0=3.1e-010 Pu0=8e-017 Wuc=5.5e-017
Lvsat=-0.00054375 Wvsat=0.008 \

Pvsat=-3.185e-010 Wketa=-8e-009 Pketa=-7e-015 Petab=8e-015
Wkt1=7e-009 Wkt1l=-7e-016 \

Wkt2=4e-009 Wute=5e-008 Wuc1=4e-017 Wat=-0.001

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; GENERAL MODEL PARAMETERS
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; EXPERT PARAMETERS
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; CAPACITANCE PARAMETERS
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; TEMPERATURE PARAMETERS
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; DIODE PARAMETERS
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B.4.2 PMOS Parameter File

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; Translated with ADS Netlist Translator (*) 270.500 Sep 21 2004
;
;Copyright (C) 1993-2004 Cadence Design Systems, Inc.
; All rights reserved.
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```
model p_12_hsl130e MOSFET Version=3.24 Mobmod=1 Capmod=3
Nqsmod=0 Binunit=2 Tnom=25 Xl=0 \

Xw=0 Llc=1.0815e-015 Lwc=0 Lwlc=0 Wlc=0 Wwc=0 Wwlc=0
Tox=2.86e-009 Toxm=2.86e-009 Wint=3.807e-008 \

Lint=1.944e-009 Dlc=1.4e-008 Dwc=0 Hdif=1.25e-007 Ldif=9e-008
Ll=1.172e-015 Wl=0 Lln=1 \

Wln=1 Lw=0 Ww=-7.8e-015 Lwn=1 Wwn=1 Lwl=-9e-023 Wwl=5.6e-023
Cgbo=0 Cgso=3.1e-010 Cgdo=3.1e-010 \

Xpart=1 Vth0=-0.2608 K1=0.4218 K2=-0.0214 K3=-2.725 K3b=2.3
Nlx=4.5e-008 Dvt0=58.5 Dvt1=2.928 \

Dvt2=0.1031 Dvt0w=0 Dvt1w=100000 Dvt2w=0 Nch=1.7e+017
Voff=-0.12 Nfactor=1.5 Cdsc=0 \

Cdscb=0 Cdscd=0.00024 Cit=0 U0=0.013376 Ua=1.53e-009 Ub=2.2e-019
Uc=-7e-011 Ngate=1e+021 \

Xj=1.55e-007 W0=5e-007 Prwg=0.15 Prwb=-0.5 Wr=1 Rdsw=130.38
A0=2 Ags=0.30253 A1=0 A2=1 \

B0=8e-008 B1=0 Vsat=95940 Keta=0 Dwg=-2.47e-008 Dwb=-4.8e-009
Pclm=1.08 Pdiblc1=1.15e-007 \

Pdiblc2=0.1 Pdiblcb=0 Drout=0.56 Pvag=1.1 Pscbe1=4.24e+008
Pscbe2=1e-005 Delta=0.00835 \

Eta0=0.0568 Etab=-0.0169 Dsub=0.4726 Elm=5 Vfb=-0.9826 Clc=1e-007
Cle=0.6 Cf=0 Ckappa=0.6 \

Cgdl=0 Cgsl=0 Vfbcv=-1.001 Acde=0.6037 Moin=10.125 Noff=1
Voffcv=2.24e-008 Kt1=-0.2722 \
```

Kt1l=-1.53e-009 Kt2=-0.056 Ute=-1.5764 Ua1=5.95e-010 Ub1=-3.4e-018
Uc1=-1e-010 Prt=-100 \

At=0 Noimod=2 Noia=9.7813e+019 Noib=30815 Noic=3.0136e-011
Em=46143000 Ef=1.1919 Rsh=7 \

Js=1.42e-007 Jsw=1e-012 Cj=0.000953 Mj=0.295 Cjsw=1.05e-010
Mjsw=0.135 Pb=0.684 Xti=3 \

Nj=1.007 PMOS=1 NMOS=0 Idsmod=8 Vbm=-3.0 Lvth0=9e-010
Wvth0=-1e-009 Pvth0=8e-017 Pk1=6.3e-016 \

Lk2=-1.1224e-009 Pk2=-1e-016 Lk3=1.54e-006 Wk3=-3e-007
Wk3b=1.04e-006 Lnlx=1.5e-015 \

Pnlx=-2.8892e-022 Lnfactor=2.4e-007 Pnfactor=-2.1e-014 Lu0=-1e-010
Wu0=7e-011 Pu0=-1e-017 \

Lags=6.25e-007 Pvsat=-7.25e-010 Wketa=1e-020 Ldelta=1.27e-009
Peta0=-4.8e-016 Petab=1e-016 \

Wkt1=5e-009 Wute=-1.42e-008 Pute=-2e-015 Wua1=-1.9152e-016
Wub1=5.25e-025 Wuc1=1.248e-017 \

Puc1=1e-023 Pat=-8.73e-010

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