2003-04-24

A 2.5 GHz Optoelectronic Amplifier in 0.18 m CMOS

Carlos Roberto Calvo
Worcester Polytechnic Institute

A 2.5 GHz Optoelectronic Amplifier in 0.18 μm CMOS

by

Carlos Roberto Calvo

A Thesis

Submitted to the Faculty

of the

Worcester Polytechnic Institute

in partial fulfillment of the requirements for the

Degree of Master of Science

in

Electrical Engineering

May 2003

Approved:

_____

Professor John A. McNeill

Thesis Advisor

_____ _____

Professor Stephen J. Bitar

Thesis Committee

Professor Demetrios Papageorgiou

Thesis Committee

Abstract

The ever-growing need for high speed data transmission is driven by multimedia and telecommunication demands. Traditional metallic media, such as copper coaxial cable, prove to be a limiting factor for high speed communications. Fiber optic methods provide a feasible solution that lacks the limitations of metallic mediums, including low bandwidth, cross talk caused by magnetic induction, and susceptibility to static and RF interferences.

The first scientists to work with fibers optics started in 1970. One of the early challenges they faced was to produce glass fiber that was pure enough to be equal in performance with copper based media. Since then, the technology has advanced tremendously in terms of performance, quality, and consistency. The advancement of fiber optic communication has met its limits, not in the purity of its fiber media used to guide the data-modulated light wave, but in the conversion back and forth between electric signals to light. A high speed optic receiver must be used to convert the incident light into electrical signals.

This thesis describes the design of a 2.5 GHz Optoelectronic Amplifier, the front end of an optic receiver. The discussion includes a survey of feasible topologies and an assessment of circuit techniques to enhance performance. The amplifier was designed and realized in a TSMC 0.18 μm CMOS process.

Acknowledgements

I would like to thank the following for making this thesis possible:

Professor John McNeill for technical advice, funding, the opportunity to work in his laboratory, and his patience.

Professor Stephen Bitar and Professor Demetrios Papageorgiou for serving on my thesis committee.

Chengxin, Tony, Pavan, Ping, and Renato for the fond memories in the VLSI Lab and at ISSCC.

Brian, Jennifer, Mara, and Matt for their help along the way.

My family for their love and support.

Table of Contents

List of Figures

List of Tables

Chapter 1: Introduction

The advancement of the communications industry has placed increasing importance on high-speed data transfer with the development of multimedia technologies. Several impediments pertaining to high-speed electronic data communications exist, including low bandwidth of metallic mediums, cross talk caused by magnetic induction, and susceptibility to static and RF interferences. An alternative to conventional metallic or coaxial cable facilities is the transmission of data via glass and plastic fiber optic cables. Fiber optics offer a high bandwidth medium with none of the aforementioned restrictions of electronic data transmission [25].

In March of 2003, a group of scientists broke the internet transmission speed record. The Cable News Network, CNN, reported:

> Scientists at the Stanford Linear Accelerator Center used fiber-optic cables to transfer 6.7 gigabytes of data -- the equivalent of two DVD movies -- across 6,800 miles in less than a minute. The center is a national laboratory operated by Stanford University for the U.S. Department of Energy…. The team was able to transfer uncompressed data at 923 megabits per second for 58 seconds from Sunnyvale, California, to Amsterdam, Netherlands. That's about 3,500 times faster than a typical Internet broadband connection…. "You have this inversion where the limitations on advances will not be the speed of the Internet but rather the speed of your computer," [Les Cottrell, assistant director of the Stanford Linear Accelerator Center] said. [15]

Optoelectronic, or optic-to-electric, communications is a rapidly developing field with many new applications that deal with the transmission of serial data through fiber optic links at extremely high speeds between electronic components. As noted by [15] and

[23], despite advances in materials allowing for faster communication mediums, the interface to electronic devices is still one of the greatest challenges.

The conversion of data between electrical signals and light is accomplished with a photonic system, as illustrated by Figure 1. The modulation of the data to light takes place at the optic transmitter. The data, in the form of an electrical signal, is converted to current by the laser driver. Light is produced with the current responding laser diode. The data-modulated light is channeled to the receiver via a fiber guide. The receiver uses a photodiode to convert the incoming light to current. The data is recovered by two amplification stages which convert the current to an electrical signal.

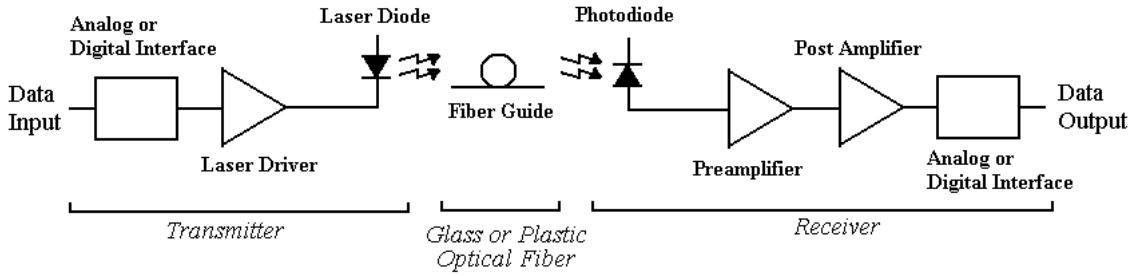

Figure 1: Photonic Communication Link

The project detailed by this document is an endeavor to design an Optoelectronic Amplifier, the front-end electronics of an optic receiver.

This thesis is organized into 8 chapters. Chapter 2 introduces the general layout of an optic receiver and defines its four basic components. Each of the functional blocks is discussed to better understand the role the Optoelectronic Amplifier plays in an optic receiver. At the end of the chapter, the specifications for the endeavor are outlined. Chapter 3 conducts a survey of the possible topologies for the first functional block of the Optoelectronic Amplifier, the Transimpedance Amplifier (TIA). Chapter 4 examines the Limiting Amplifier (LA), the second stage of the endeavor. The chapter also considers the feasibility of active inductors and other circuit techniques to enhance the performance of the LA. Chapter 5 examines different methods to interface the single-ended TIA to

the differential LA. An Offset Feedback method is introduced as a possible solution. Chapter 6 describes the silicon implementation of the Optoelectronic Amplifier system and 9 independent TIA circuits and examines the results of the test chip. The 1/f characteristics of the CMOS process are also discussed. Chapter 7 presents the conclusions of the thesis with suggestions for future design considerations.

Chapter 2: System Overview

Typical optoelectronic receiver topologies consist of four major components: photo-detector, preamplifier, limiting amplifier, and clock and data recovery [14]. Figure 2 illustrates the generic block diagram of the system. In addition to these, miscellaneous circuitry may be included in a design for biasing and compensation.

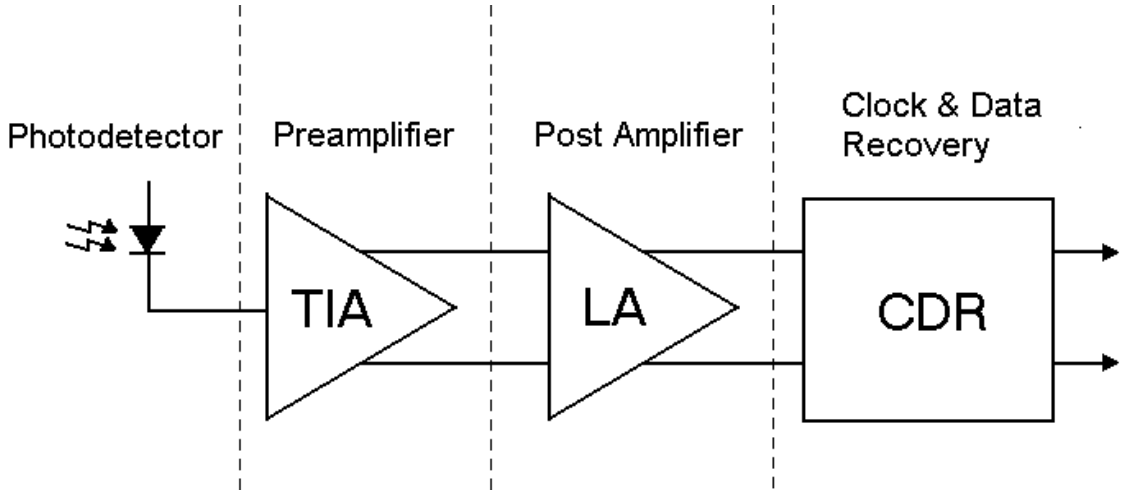

Figure 2: Typical Optoelectronic Amplifier Block Diagram

The objective of this thesis is to design an Optoelectronic Amplifier which consists of the preamplifier and post amplifier. The following sections will detail the four components of an optic receiver to better understand the concerns and motivations involved with the design.

2.1 Photo-detector

When a reverse biased *p-n* junction is illuminated by incident light, the photons impacting the junctions cause covalent bonds to break. The disruption causes the generation of holes and carriers in the depletion region. The electric field in the depletion region allows the freed electrons to move across to the *n* side and the holes to the *p* side, giving rise to current flow across the junction [26].

Two-terminal devices designed to respond to photon absorption are called photodiodes. When the photodiode is operated in the reverse-biased region of its I-V characteristic, the current is independent of voltage but is proportional to the incident light. Such a device serves as a very useful means of measuring illumination levels or of converting time-varying optical signals into electrical signals [24].

In most optical detection applications the response speed of the detector is critical. The photodiode has to respond to a series of light pulses of very short duration. Thus, the photo generated minority carriers must diffuse to the junction and be swept quickly across to the other side. The carrier diffusion time determines the response time of the detector. Since the carrier diffusion takes longer compared to the carrier drift, the width of the depletion is made very wide so that most of the photons are absorbed within it rather than in the neutral *p* and *n* regions. In operation these detectors, which are reverse biased, absorb the incident radiation. This process generates electron-hole pairs which drift to the detector electrodes, generating a current in the external circuit. The most commonly used photo-detectors are the PIN diode and the Avalanche photodiode [26], [30].

P-type-Intrinsic-N-type Diodes

PIN diodes are the leading candidates for optical receiver applications due in large part to their capacity to exceed speeds of hundreds of gigahertz [25]. The basic construction of a PIN diode is shown in Figure 3.

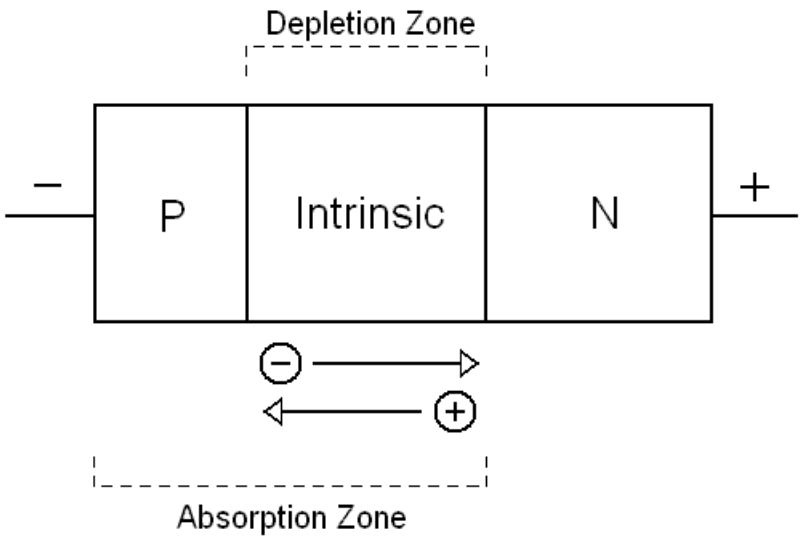

Figure 3: PIN Photodiode Construction

An intrinsic layer of *n*-type semiconductor material is placed between the junction of two heavily doped contact areas, one of *n*-type and the other of *p*-type. Light falls on the carrier-void intrinsic material, which is built thick enough to absorb nearly all of the photons. The absorption of the majority of the photons is achieved by the electrons in the valence band of the atoms in the intrinsic material. The absorption of photons provides the electrons with sufficient energy to move from the valence band into the conduction band, as illustrated in Figure 4. The shift in bands provides carriers in the depletion region allowing current to flow through the device. The increase in the number of electrons that move into the higher conductive band is matched by an increase in the number of holes in the valence band [25], [26].

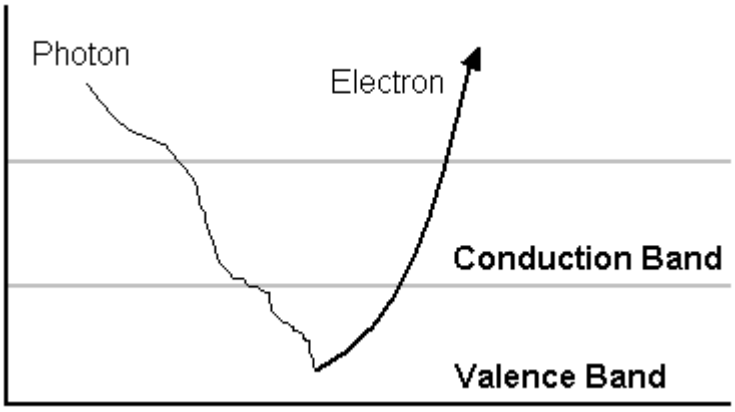

Figure 4: Photoelectric Effect

To cause current to flow in a photodiode, the light energy must be sufficient enough to impart the required amount of energy for electrons to jump the energy gap between bands. The energy gap for silicon is 1.12 eV at room temperature (in electron Volts), which corresponds to

$$E_g = (1.12eV)\left(1.6 \cdot 10^{-19} \frac{J}{eV}\right) = 1.792 \cdot 10^{-19} J \quad (1)$$

The energy of a photon is the product of Planck's constant, h = 6.65256·10-34 J/Hz, and its frequency, ν.

$$E = h \cdot \nu \quad (2)$$

Thus, the frequency of the photon necessary for the energy gap jump in a silicon photodiode is

$$\nu = \frac{E}{h} = \frac{1.792 \cdot 10^{-19} J}{6.6256 \cdot 10^{-34} \frac{J}{Hz}} = 2.705 \cdot 10^{14} Hz \quad (3)$$

Converting the frequency to wavelength yields

$$\lambda = \frac{c}{\nu} = \frac{3 \cdot 10^{-8} \frac{m}{s}}{2.705 \cdot 10^{14} Hz} = 1109nm \quad (4)$$

where the *c* denotes the speed of light. Consequently, light waves of 1109 nm or shorter are required to cause electrons to jump the energy gap of a silicon photodiode [25].

Avalanche Photodiodes

An Avalanche photodiode (APD) is a p^+ipn^- structure, shown in Figure 5.

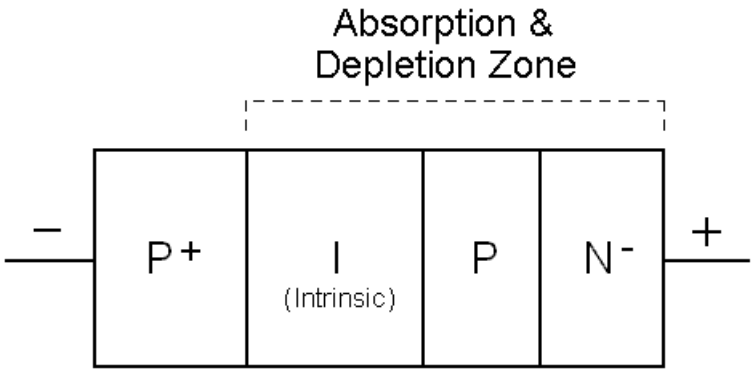

Figure 5: Avalanche Photodiode Construction

Light enters the diode and is absorbed by a thin, heavily doped *n*-layer. Impact ionization is caused by a high electric field intensity developed across the *i*-*p*-*n* junction, supplied by an external bias voltage. Impact ionization allows the carrier to gain adequate energy in order to ionize bound electrons. The newly ionized electrons, in turn, will cause more ionization to occur. The process continues in a manner similar to an avalanche, thus its name. The progression of the "avalanche" is equivalent to an internal gain or carrier multiplication specific to the device. It is for this reason that APDs are more sensitive than PIN diodes and require less amplification. The major disadvantages of the APD are the relatively long transit times, in comparison to the fast PIN diode, and the additional internally generated noise due to the avalanche multiplication factor [24], [25].

The trade-offs of each photo diode are listed in Table 1 [28].

Table 1: Comparison of Photodiodes

PIN Photodiode	Avalanche Photodiode
▪ No Internal Gain ▪ High Bandwidth ▪ Low Noise	▪ Internal Gain (≈100) ▪ Small Bandwidth ▪ Excessive Noise

Photodiode Model

The model for a generic photodiode is illustrated in Figure 6. All diodes consist of two major current players - photocurrent, i_p, and dark current, i_d. Photocurrent is the medium through which the data is transferred from light to current. Dark current, produced by thermally generated carriers in the diode, is the leakage current that flows through a photodiode with no light input. The photodiode is also susceptible to thermal and shot noise, i_{ns} and i_{nt}, respectively [28].

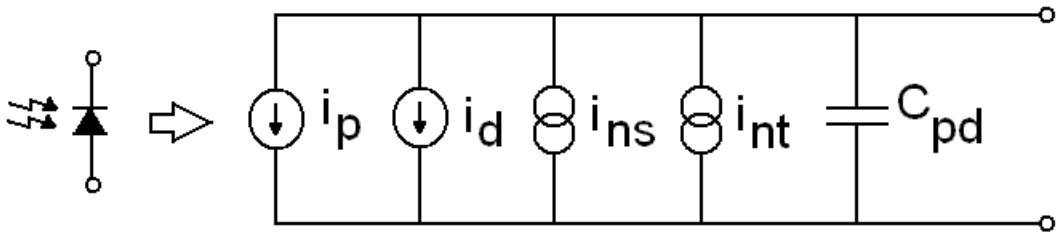

Figure 6: Photodiode Model

The most significant portion of the model, second only to the photocurrent, is that of the large photodiode capacitance. This is especially true when considering the transmission

speed demands placed on the subsequent amplification stage of an external photodiode, where packaging and interconnection have to be considered.

To simplify the discussion, only the major contributors, i_p and C_{pd}, will be considered throughout the document. The rest of the pieces will be omitted as they are negligible within the scope of this project.

2.2 Preamplifier

The photocurrent generated by the detector must be converted to a usable signal for further processing with a minimum amount of added noise. The preamplifier is the first stage in the amplification of the photocurrent and, therefore, will be the dominant source of noise added to the signal. Due to this fact, the preamplifier design will be the principal factor in determining the sensitivity of the entire receiver system.

There are three options for the optical receiver front-ends: low-impedance preamplifier, high-impedance preamplifier, or transimpedance amplifier. These three options are depicted in Figure 7. All of the optical to electrical conversion configurations would interface with the photodetector (either a PIN or an Avalanche photodiode).

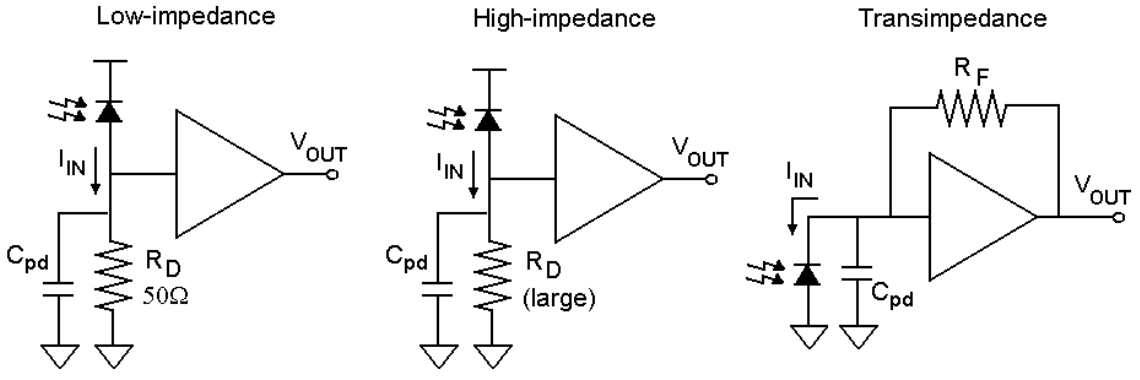

Figure 7: Preamplifier Configurations

The low-impedance receiver has the advantage of being able to use a very wide variety of commercially available amplifiers. Because of the low signal levels at the input of the

preamplifier, this configuration has the widest dynamic range and can easily achieve the widest bandwidths. Unfortunately, its wide input range is at the expense of its poor noise performance due to the small R_D.

Photodiodes act as current sources and are able to interface with high resistance. The added resistance of a high-impedance receiver can be used to increase the signal voltage from the input photocurrent. To improve the noise performance, higher values of terminating resistance, $R_{d,}$ are used. While the higher input impedance levels improve the sensitivity, they limit the bandwidth and lead to early saturation of the amplifier. Large amplitudes at the input of the amplifier will limit the dynamic range of the configuration. In practice, high-impedance front ends require equalization to compensate for their lack of bandwidth.

Transimpedance amplifiers typically have wider input current ranges than the high-impedance preamplifiers and have better sensitivity than low-impedance preamplifiers. These advantages are due in large part to the negative feedback used in the configuration [28].

Table 2 summarizes the trade-offs of the preamplifier configurations. Due to the transimpedance amplifier's adaptability to this application, it was selected as the best option for this endeavor.

Table 2: Comparison of Preamplifier Topologies

Low-impedance	High-impedance	Transimpedance
▪ High Bandwidth	▪ Small Bandwidth	▪ High Bandwidth
▪ Low Sensitivity	▪ High Sensitivity	▪ High Sensitivity (dependent on R_F)
▪ High Noise	▪ Low Noise	▪ Medium Noise

More detail of the transimpedance amplifier is discussed in the following chapter. Throughout this document, any unspecified mention of preamplifiers will be inferring the Transimpedance Amplifier (TIA).

2.3 Post Amplifier

The post amplifier provides the remaining amplification of the signal so that the output signal swings rail-to-rail. Due to the rail-to-rail saturation of the post amplifier, it is also referred to as a limiting amplifier. The post amplifier does not contribute significant input referred noise in the system because the dominant noise source is the preamplifier due to its gain. In some applications, the post amplifier contains features such as automatic level control to keep the signal level constant, as well as clamping circuitry to reference the signal to particular voltage levels.

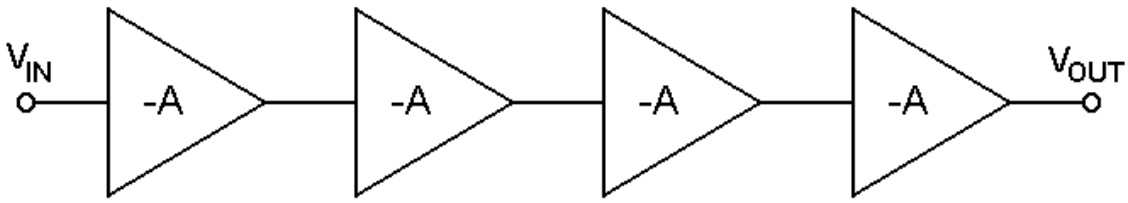

Figure 8: Inverter Chain Post Amplifier

The post amplifier is typically an open-loop voltage amplifier. A chain of properly biased inverters can be used to provide the necessary gain, shown in Figure 8. However, this option is not viable because it is susceptible to common-mode noise, including the power supply noise [1]. An alternative is the differential voltage amplifier which can be used to suppress the common-mode noise. The differential voltage amplifier is illustrated in Figure 9 [22].

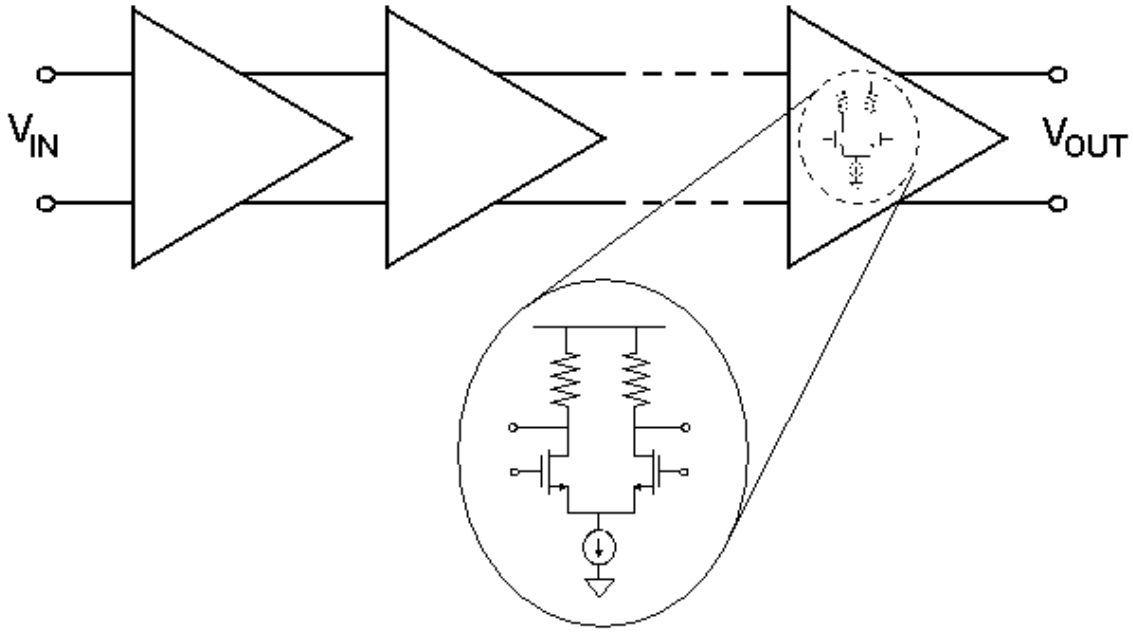

Figure 9: Differential Amplifier Post Amplifier

The challenges of various amplifier realizations are explored in Chapter 4. Future mention of post amplifiers will be in reference to the differential Limiting Amplifier (LA).

2.4 Clock and Data Recovery

Connected to the LA is the Clock and Data Recovery (CDR) circuitry. The purpose of the CDR block is to extract the clock timing from the incoming data, while also retiming the data and reducing its jitter. The extracted clock signal must have small timing jitter to prevent the system from having increased bit error rate (BER) [17]. Optical networking standards mandate that data be transmitted in synchronized format, as in the case of the Synchronous Optical Network (SONET) standard. Synchronized networks are generally prone to phase differences due to jitter and propagation delay. It is for this reason that SONET has very strict jitter tolerance, jitter transfer, and jitter generation specifications to avoid poor data quality [4], [17].

A generic clock and data recovery circuit is illustrated in Figure 10. The data enters the CDR where it is compared to an internally generated clock signal by the phase detector. The clock signal comes from the voltage-controlled oscillator (VCO). Any difference in the phase will result in an error signal, which controls the charge pump. Together, the charge pump and a low-pass filter generate the VCO control voltage. The VCO will then increase or decrease its frequency to match the incoming data phase. The settled VCO output signal represents the extracted clock. The newly generated clock is fed back to the phase detector and the process repeats. The clock signal also drives the decision circuit which will retime the data and reduce the jitter [23].

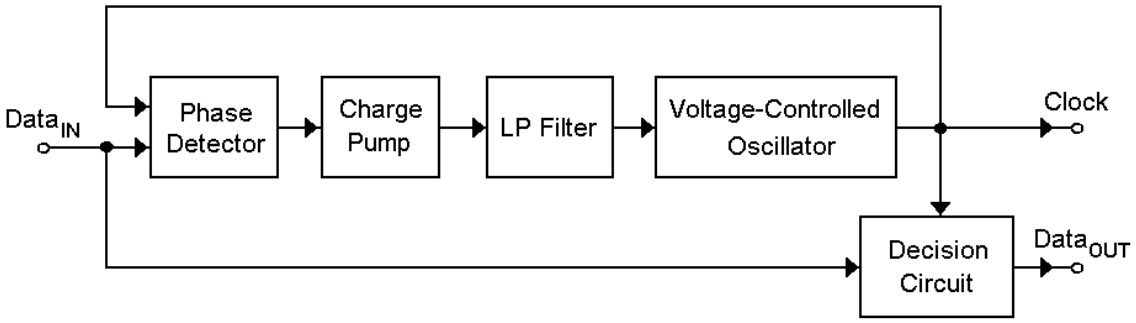

Figure 10: Generic Clock and Data Recover Architecture

For the purpose of this endeavor, the output of the Optoelectronic Amplifier to the Clock and Data Recovery will require a differential signal with a peak-to-peak voltage of 250 mV, the commonly used input range of a CDR [22], [29].

2.5 Definition of Specifications

Once again, the project detailed by this document is an endeavor to design an Optoelectronic Amplifier, the front-end electronics of an optic receiver, as illustrated in with the shaded region of Figure 11. The Optoelectronic Amplifier consists of the TIA and LA in a monolithic semiconductor.

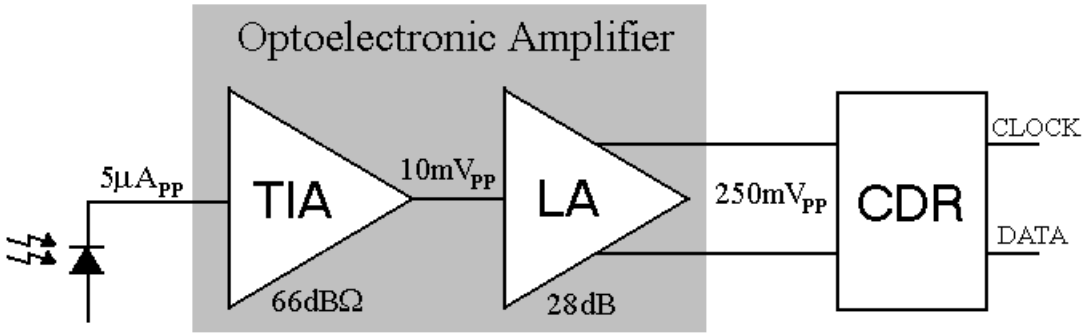

Figure 11: Optoelectronic Amplifier Block Diagram

The Optoelectronic Amplifier must be sensitive to various levels of optical power that are directly related to the length of the fiber link. A photodiode is expected to produce a 5 $\mu A_{p\text{-}p}$ current signal under the worst optical attenuation conditions as defined by SONET-48 [22]. The two most important parameters of the transimpedance amplifier are its sensitivity and the maximum bit rate [8]. The sensitivity of the TIA is a result of the transimpedance [9]. The TIA amplifies the current signal to a gain of near 66 dBΩ. High gain is desired for a TIA to produce high system performance. However, the large transimpedance leaves the TIA as the dominant noise contribution to the system. In an effort to reduce the input noise contribution of the TIA to 400 nA_{rms}, the bandwidth should be limited [22]. The maximum bit rate is a consequence of the TIA bandwidth, therefore, binding the bandwidth must be done carefully to avoid Intersymbol Interference (ISI). For an NRZ data format, the bandwidth should be between 0.6 and 0.7 of the data rate [14]. The determined bandwidth for the TIA is 1.65 GHz, which is a good balance between ISI and noise for a 2.5 GHz bit rate.

$$f_{3dB} = 0.65 \cdot Bitrate \approx 1.65GHz \tag{5}$$

The TIA feeds a voltage signal of 10 mV_{pp} to the input of the Limiting Amplifier (LA). The task of the LA is to amplify the incoming voltage signal to a sufficient voltage level of 250 mV_{pp} for the reliable operation of a clock and data recovery (CDR) circuit [22], [29]. The LA must have a small-signal gain of 28 dB to allow the minimum allowable

input signals to reach the full voltage swing. If the input current to the TIA is greater than the minimum, the large gain of the LA will cause the output into saturation, thereby cutting off or 'limiting' the output voltage level [22].

Throughout the following documentation, it will be verified that an Optoelectronic Amplifier with the subsequent specifications, listed in Table 3, can be built in TSMC 0.18 μm CMOS technology.

Table 3: Proposed Optoelectronic Amplifier Specifications

Parameter	***Value***
CMOS Technology	3.3V, 0.18 μm
Maximum Bit Rate	2.5 Gb/s
Bandwidth (-3dB)	1.65 GHz
Transimpedance	66 dBΩ
LA DC Gain	28 dB
I_{min}	5μA
I_{max}	500μA
TIA Input Noise, i_n	400nA_{rms}
Diode Capacitance, C_D	1pF

Throughout this document, the project will be referred to as the Optoelectronic Amplifier (to distinguish it from the optic receiver).

2.6 Conclusion

In this chapter, the major blocks of an optoelectronic receiver were presented. Some of the various component details were presented and some options were eliminated in order to focus the design to a smaller assortment of suitable solutions. The project scope was declared along with the definition of the specifications to be met by the design. In the next chapter, the Transimpedance Amplifier configurations will be dissected to provide the best possible solution. Subsequent chapters will discuss the remaining blocks.

Chapter 3: Transimpedance Amplifier

The most vital component of an Optoelectronic Amplifier is that of the Transimpedance Amplifier (TIA). That being the case, its design becomes the most challenging of all of the system modules [9].

The demands on the TIA stage require a balance of tradeoffs of transimpedance gain, bandwidth, and input noise. The TIA must be sensitive enough to detect small current levels produced by the photodiode and yet possess an input range wide enough to handle signals that are one hundred times larger than the minimum required input. High gain addresses the sensitivity issue by allowing the TIA to respond to smaller input currents. However, greater gain serves as an obstruction to achieving a suitable bandwidth [8], [11]. The TIA is the first stage of amplification and will be injecting the dominant noise contribution to the system. The undesirable consequence of the large bandwidth is the inability to eliminate high frequency noise. The goals set to balance the TIA tradeoffs are listed below:

High Bandwidth – 1.65 GHz

High Transimpedance Gain – 2 kΩ

Low Input Referred Current Noise – 400 nA_{rms}

Large Input Current Range – 5 to 500 μA_{p-p}

3.1 Transimpedance Amplifier System

The highest priority of the design of the TIA was placed on bandwidth and the transimpedance gain. Two limiting factors of the design of the TIA are the input capacitance introduced by the photodiode and the resistor closing the negative feedback

link around the TIA. Figure 12 shows a generalized schematic of a TIA used in an optic system.

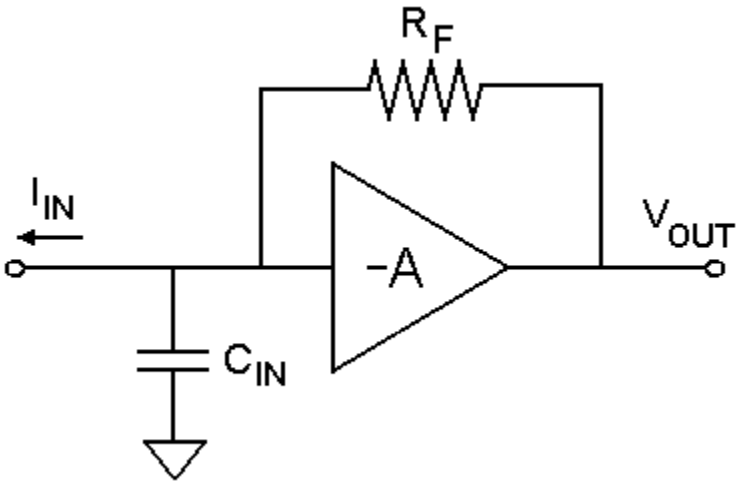

Figure 12: Typical Transimpedance Amplifier Configuration

For an ideal voltage gain, A, for the inverting gain stage, the closed-loop transimpedance gain of the TIA is given by

$$\frac{V_{out}}{I_{in}} = R_f \cdot \frac{A}{(1+A)+sR_fC_{in}} \tag{6}$$

$$\approx R_f \cdot \frac{1}{1+s\left(\frac{R_fC_{in}}{1+A}\right)} \tag{7}$$

The bandwidth of the TIA is specified by the pole of the system described in the equation above. The bandwidth is given by

$$f_{3dB} \approx \frac{1+A}{2\pi R_fC_{in}} \tag{8}$$

[8], [9], [12]. The desired bandwidth of 1.65 GHz and the transimpedance gain of 2 kΩ require the open-loop gain of the inverting gain stage to be approximately 20, or 26 dB.

The former was corroborated by work done by [9]; however, it is important to note that the bandwidth required by [9] was in the magnitude of hundreds of MHz, not GHz. The equation developed above must be used with the caveat that the necessary A must be achieved at the desired f_{3dB}. The inverter has a transfer function of

$$A(s) = \frac{A_o}{1 + s\tau} \tag{9}$$

where A_o is the DC gain of the inverting stage and τ is its corner frequency. Thus, the new model for the TIA is

$$\frac{V_{out}}{I_{in}} = R_f \cdot \frac{\frac{A_o}{1 + s\tau}}{\left(1 + \frac{A_o}{1 + s\tau}\right) + sR_f C_{in}} \tag{10}$$

A simplified equation for the open-loop gain is given by

$$A(f_{3dB}) \approx 2\pi R_f C_{in} f_{3dB} - 1 \tag{11}$$

where $A(f_{3dB})$ is at the desired bandwidth of the TIA. The design of the inverting gain stage block must achieve the gain of at least 20, or 26 dB, at the high frequency of 1.65 GHz.

The input capacitance and transimpedance are set by the specifications, leaving the open-loop gain of the inverting gain stage as the sole parameter for TIA optimization. In the following sections several configurations for the inverting gain stage, or inverter, will be examined.

3.2 Inverter Configurations

There are many variations of inverters regularly available. Figure 13, Figure 14, and Figure 15 illustrate some of the different inverter configurations.

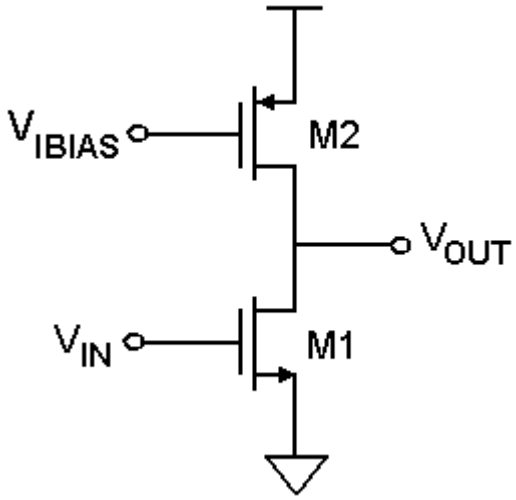

Figure 13: Current Load Inverter

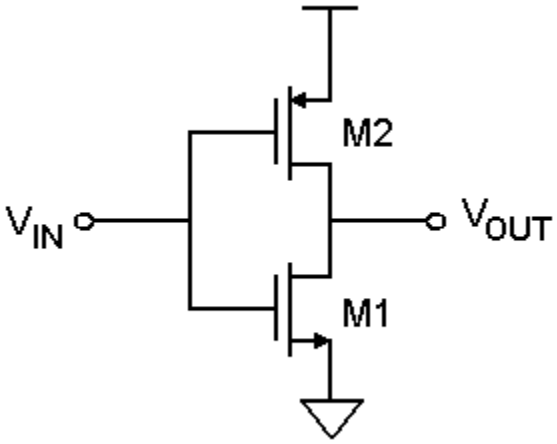

Figure 14: Push-Pull Inverter

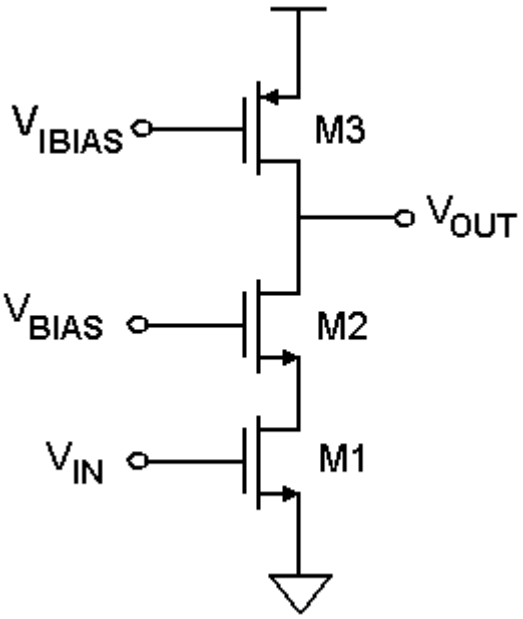

Figure 15: Cascode Inverter

The following sections will examine the inverter configurations and outline the strengths and weaknesses of each.

3.2.1 Current Load

The current load inverter has two variables with which the necessary open-loop gain can be achieved: the transistor dimensions and the bias current. The small-signal performance can be analyzed with the aid of Figure 16 [1].

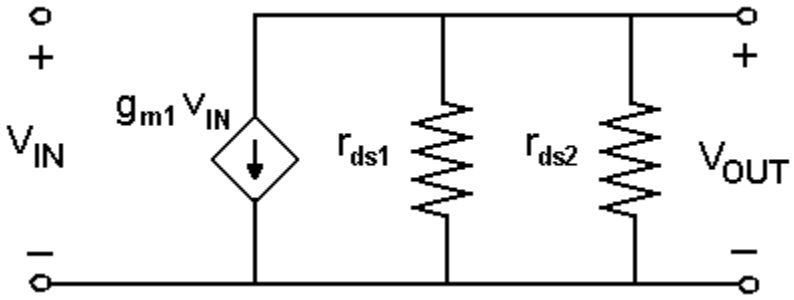

Figure 16: Small-signal Model for the Current Load Inverter

The small-signal voltage gain for the current load inverter is

$$-A = \frac{g_{m1}}{g_{ds1} + g_{ds2}} \tag{12}$$

The equivalent TIA thermal input noise is

$$\bar{i}_{eq}^2 = \frac{\bar{i}_{n-ds1}^2}{\left(g_{ds1} + g_{ds2}\right)^2 R_F^2} + \frac{\bar{i}_{n-ds2}^2}{\left(g_{ds1} + g_{ds2}\right)^2 R_F^2} + \frac{\bar{e}_{n-Rf}^2}{R_F^2} \tag{13}$$

which yields

$$\bar{i}_{eq}^2 = \frac{8}{3} \cdot \frac{k \cdot T \cdot g_{m1}}{\left(g_{ds1} + g_{ds2}\right)^2 R_F^2} + \frac{8}{3} \cdot \frac{k \cdot T \cdot g_{m1}}{\left(g_{ds1} + g_{ds2}\right)^2 R_F^2} + 4 \cdot \frac{kT}{R_F} \tag{14}$$

The first two terms are the noise generated by the drain currents of the transistors; the third term represents the noise generated by the feedback resistor. It is important to note that the noise added by the feedback resistor is inversely proportional to the resistor size, i.e. a larger feedback resistor results in lower current noise at the input of the TIA [27].

Unfortunately, the optimized current source inverter can only produce an open-loop gain of 10 at the TIA bandwidth frequency, as can be seen in Figure 17.

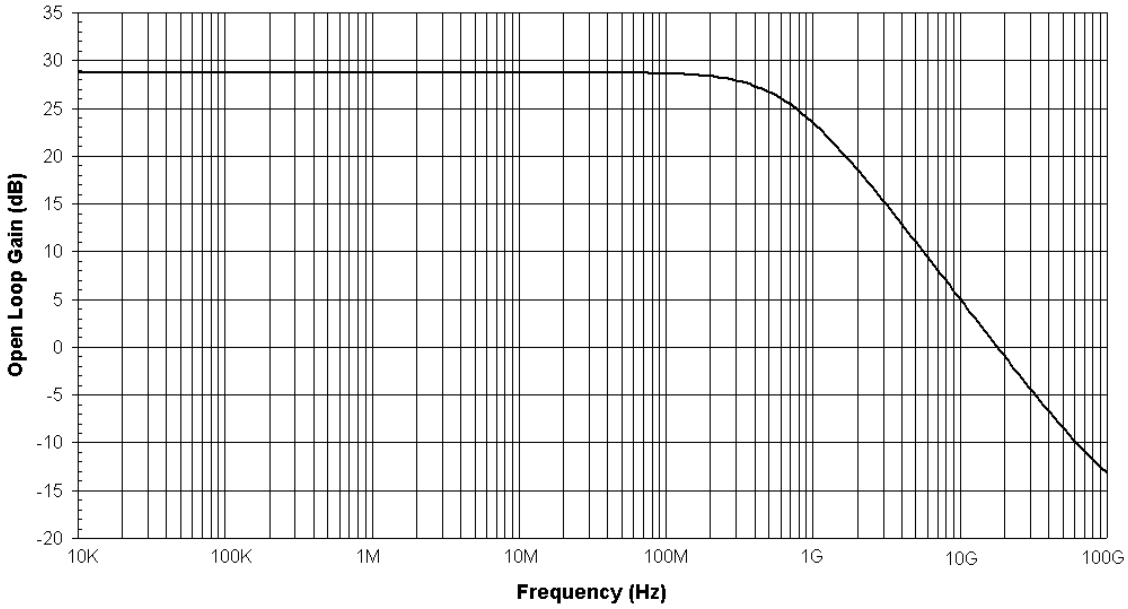

Figure 17: Open-loop AC Response of Current Load Inverter

The failure to meet the necessary open-loop gain is also evident in the closed-loop response, shown in Figure 18. The bandwidth of the TIA is limited to 1.12 GHz. The simulated input referred noise figure is 315 nA_{rms}; a seemingly promising measure due to the low bandwidth.

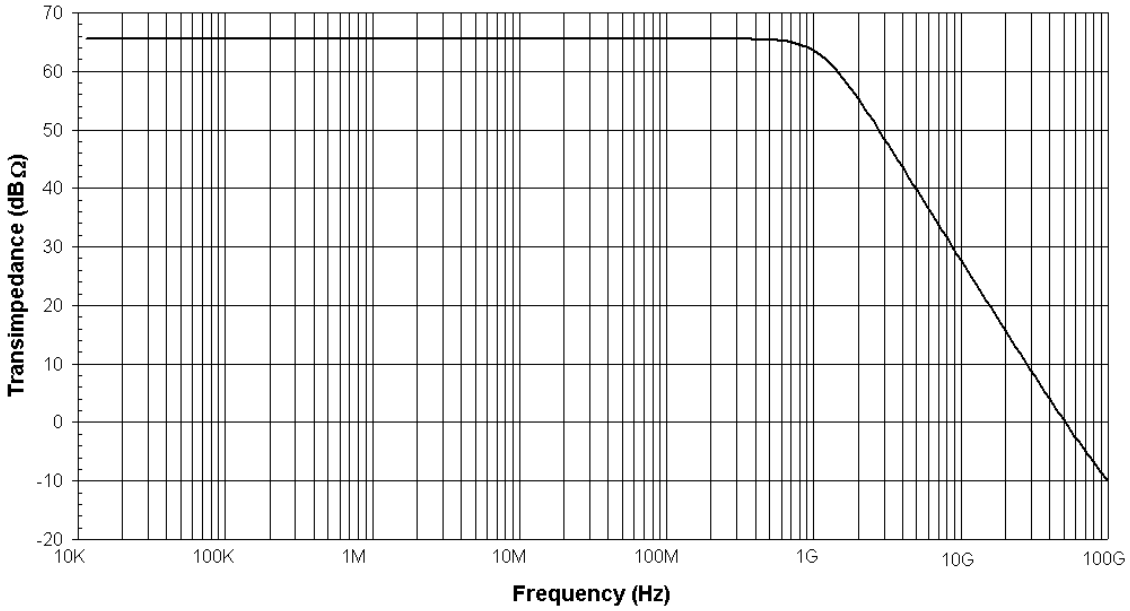

Figure 18: Closed-Loop AC Response of Current Load TIA

The total performance of the current load TIA is summarized in Table 4. The open-loop gain of the inverter is 14, or 23 dB, at the bandwidth of 1.12 GHz which agrees with the relationship of equation 11.

Table 4: Summary of Current Load Inverter Performance

Parameter	***Value***
M1 Dimensions, W/L	3.30 μm/0.18 μm
M2 Dimensions, W/L	62.64 μm/0.18 μm
Current Bias, I_{BIAS}	2.544 mA
Transimpedance, R_F	2 kΩ
Open-loop Gain @ 1.65 GHz	20.0 dB
Bandwidth, f_{3dB}	1.12 GHz
Input Referred Noise, i_n	315 nA_{rms}

3.2.2 Push-Pull

The push-pull inverter is another two-transistor amplifier solution. The small-signal model is illustrated in Figure 19.

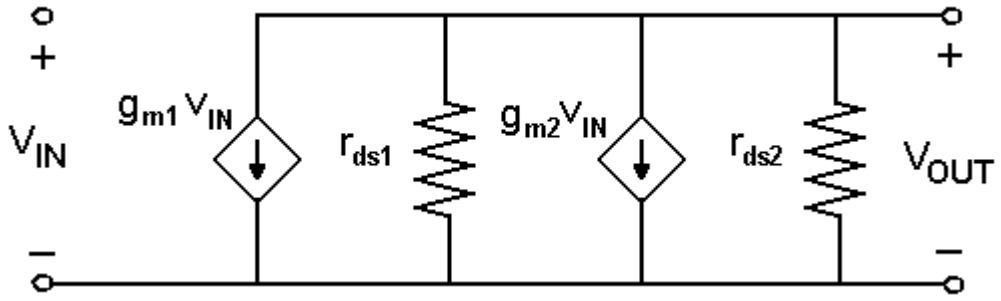

Figure 19: Small-signal Model of the Push-pull Inverter

The small-signal gain of the inverter is

$$-A = \frac{g_{m1} \cdot g_{m2}}{g_{ds1} + g_{ds2}} \tag{15}$$

which can only be modified with the dimensions of the two transistors [1]. For a homogenous voltage swing, the nMOS and pMOS transistors are traditionally sized to have close transconductances. The open-loop gain of the push-pull configuration can achieve higher gains than the current load inverter. It is for this reason that this topology has a better possibility of reaching the necessary bandwidth than the current load inverter.

The noise injected by this configuration is composed predominately of drain currents. The TIA equivalent thermal input noise is

$$\bar{i}_{eq}^2 = \frac{\bar{i}_{n-ds1}^2}{\left(g_{ds1} + g_{ds2}\right)^2 R_F^2} + \frac{\bar{i}_{n-ds2}^2}{\left(g_{ds1} + g_{ds2}\right)^2 R_F^2} + \frac{\bar{e}_{n-Rf}^2}{R_F^2} \tag{16}$$

which yields

$$\bar{i}_{eq}^2 = \frac{8}{3} \cdot \frac{k \cdot T \cdot g_{m1}}{\left(g_{ds1} + g_{ds2}\right)^2 R_F^2} + \frac{8}{3} \cdot \frac{k \cdot T \cdot g_{m1}}{\left(g_{ds1} + g_{ds2}\right)^2 R_F^2} + 4 \cdot \frac{kT}{R_F} \tag{17}$$

where the first term is the noise model of the nMOS transistor and the second term corresponds to the pMOS transistor [1]. The third term represents the feedback resistor. Note that the noise model is the same as the current load configuration.

As expected, the push-pull configuration can achieve a higher open-loop gain; however, the gain at the needed TIA bandwidth is merely 5, as shown in Figure 20.

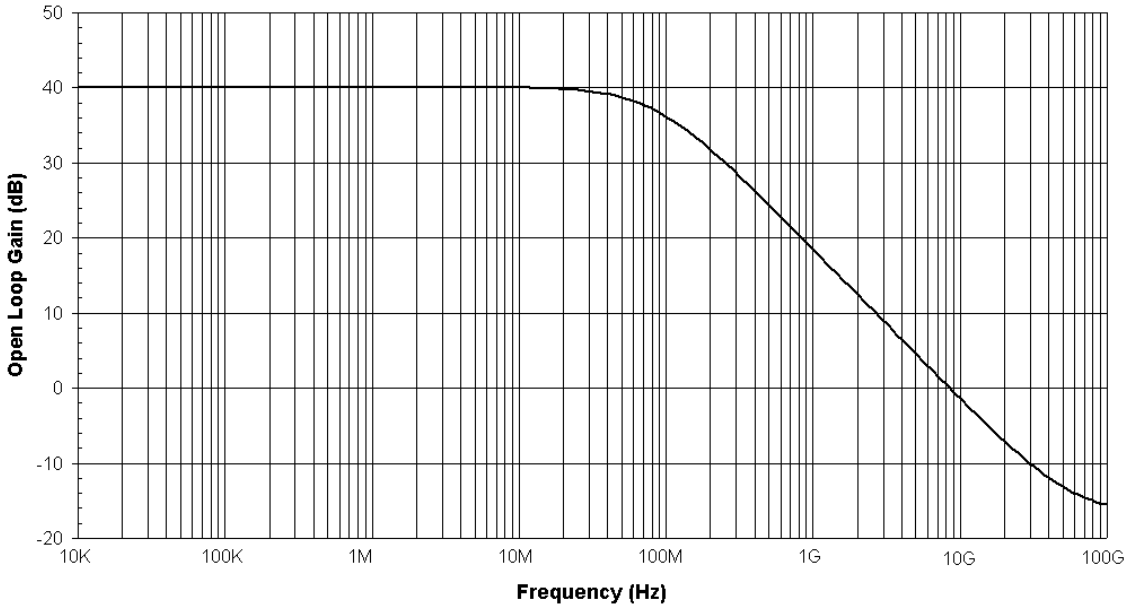

Figure 20: Open-loop AC Response of Push-Pull Inverter

The closed-loop response of the system is affected by the low open-loop gain of the inverter. The push-pull TIA can only boast of a bandwidth of 1 GHz, illustrated in Figure 21. The simulated input referred noise figure is 289 nA_{rms}. This value is apparently a good figure. However, it is significantly reduced because the bandwidth is only 2/3 of the specification.

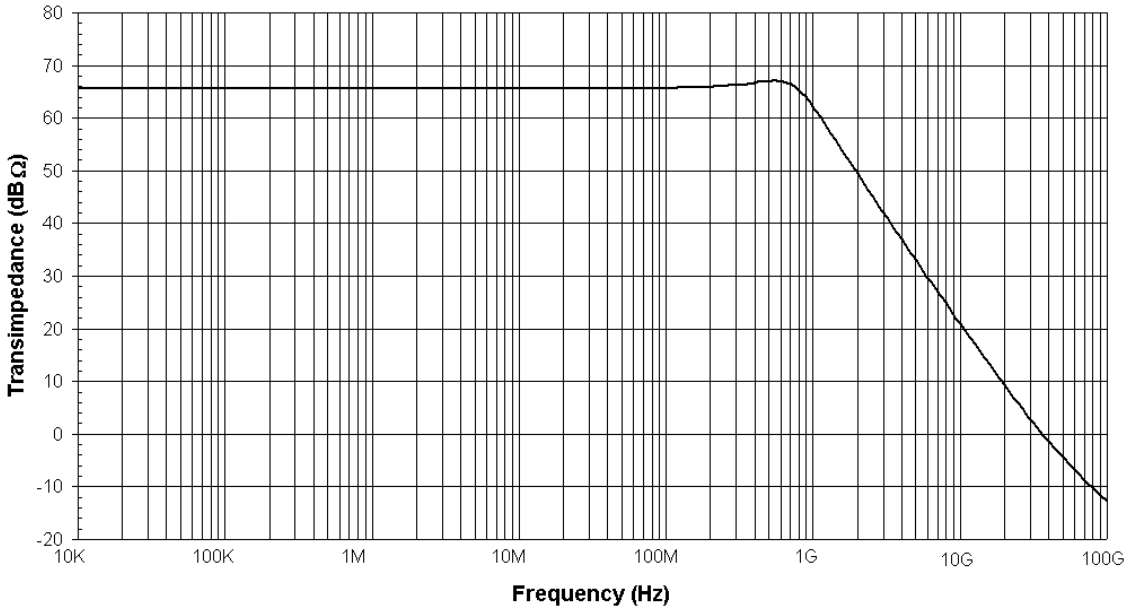

Figure 21: Closed-Loop AC Response of Push-Pull TIA

It is important to note that due to the higher gain of the TIA, some peaking is evident in the AC behavior. This topic will be covered in the following section, with reference to the Cascode TIA.

The total performance of the push-pull TIA is summarized in Table 5.

Table 5: Summary of Push-pull Inverter Performance

Parameter	***Value***
M1 Dimensions, W/L	30.15 μm/0.35 μm
M2 Dimensions, W/L	60.21 μm/0.35 μm
Transimpedance, R_F	2 KΩ
Open-Loop Gain @ 1.65 GHz	14.1 dB
Bandwidth, f_{3dB}	1.0 GHz
Input Referred Noise, i_n	289 nA_{rms}

3.2.3 Cascode

The cascode inverter is a three-transistor amplifier. This configuration is very similar to the current load inverter with variables including the bias current and the dimensions of the transistors. Recall that the current load inverter suffered from small gain, yet it had a wider bandwidth than the push-pull inverter. With the added transistor, M2, of Figure 15, the configuration is less susceptible to the Miller capacitance on the input of the amplifier. The small-signal performance can be analyzed with the aid of Figure 22.

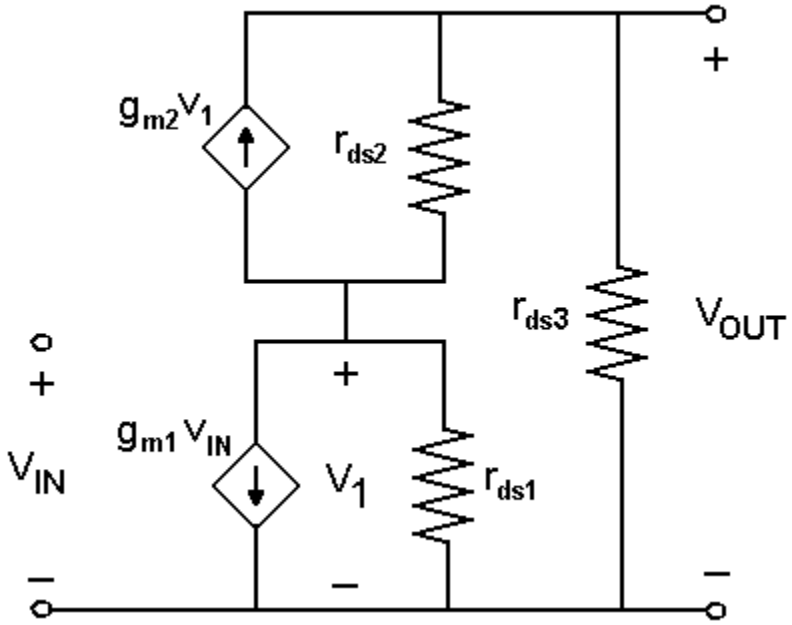

Figure 22: Small-signal Model for the Cascode Inverter

The small-signal voltage gain for the cascode inverter is

$$-A = \frac{g_{m1}(g_{ds2} + g_{ds3})}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}} \tag{18}$$

[1]. The equivalent TIA thermal input noise is

$$\bar{i}_{eq}^{2} = \frac{\bar{i}_{n-ds1}^{2} \cdot \left(g_{ds2} + g_{ds3}\right)}{\left(g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}\right)^{2} R_F^2} + \frac{\bar{i}_{n-ds2}^{2} \cdot g_{ds1}^{2}}{\left(g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}\right)^{2} R_F^2} + \frac{\bar{i}_{n-ds3}^{2} \cdot \left(g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}\right)^{2}}{\left(g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}\right)^{2} R_F^2} + \frac{\bar{e}_{n-Rf}^{2}}{R_F^2} \tag{19}$$

which yields the noise contributions

$$\bar{i}_{eq}^{2} = \frac{8}{3} \cdot \frac{kTg_{m1} \cdot \left(g_{ds2} + g_{ds3}\right)^{2}}{\left(g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}\right)^{2} R_F^2} + \frac{8}{3} \cdot \frac{kTg_{m2} \cdot g_{ds1}^{2}}{\left(g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}\right)^{2} R_F^2} + \frac{8}{3} \cdot \frac{kTg_{m3} \cdot \left(g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}\right)^{2}}{\left(g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}\right)^{2} R_F^2} + 4 \cdot \frac{kT}{R_F} \tag{20}$$

where the first two terms represent the two transistors, M1 and M2, respectively [12]. As in the case of the other inverter configurations, the feedback resistor is the last term in the noise model.

With the improved open-loop bandwidth performance and higher gain, the optimized cascode inverter is able to meet the required gain of 20 at a specified TIA bandwidth frequency of 1.65 GHz. Figure 23 shows the cascode inverter meeting the open-loop gain at a frequency approaching 2 GHz.

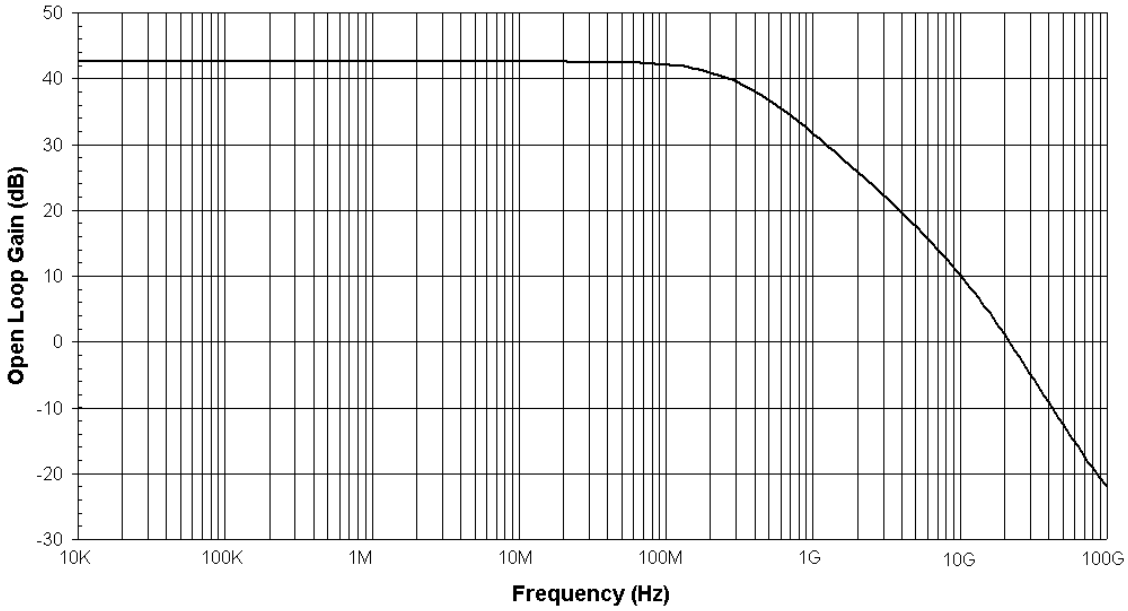

Figure 23: Open-loop AC Response of Cascode Inverter

The closed-loop performance of the TIA, is shown in Figure 24. The Cascode Transimpedance Amplifier meets the required bandwidth. The closed-loop response was simulated using a 2 KΩ feedback resistor. The simulated input referred noise figure is 363 nA_{rms}, well below the required specification.

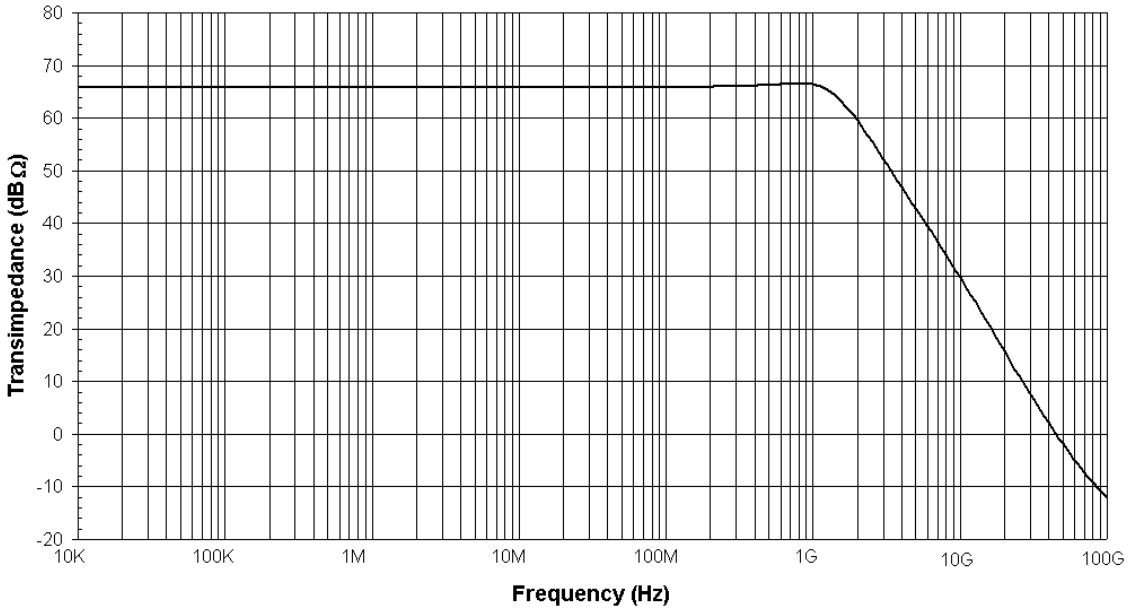

Figure 24: Closed-Loop AC Response of Cascode TIA

As mentioned in the previous section, the high open-loop gain of the inverter, in conjunction with the large input capacitance, leads to some instability with the evidence of peaking at high frequencies [19]. This is a common effect of transimpedance amplifiers. [13] and [19] offer the solution of using a capacitor in parallel with the feedback resistor to reduce the amount of ringing at high frequencies, as shown in Figure 25.

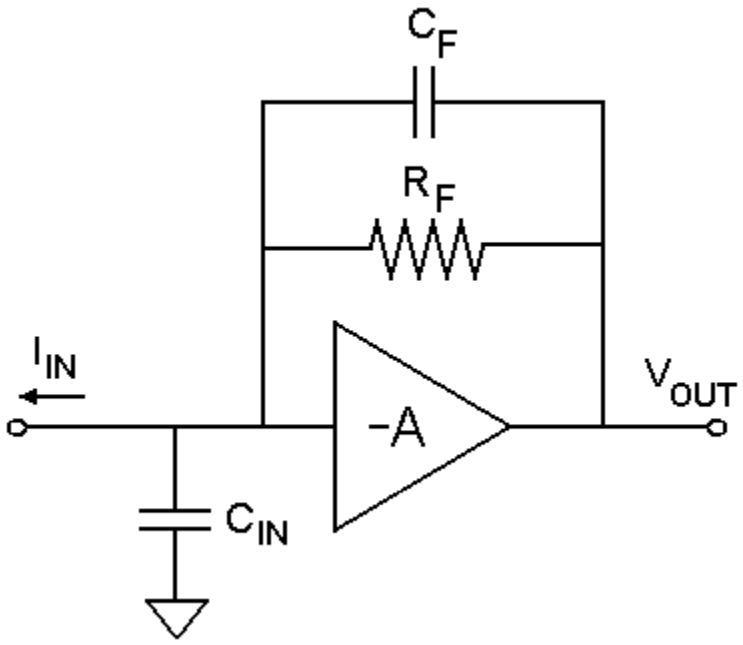

Figure 25: Transimpedance Amplifier with Capacitive Feedback

The optimum value of the capacitor can be found using the relationship

$$C_f = \sqrt{\frac{C_{in}}{2\pi R_F f_u}} \tag{21}$$

where the unit frequency of the inverter is represented by f_u. The feedback capacitor used in the above simulation for the Cascode TIA was 37 fF in order to achieve a 45° phase margin [13].

The total performance of the current load TIA is summarized in Table 6. The cascode performed within specifications and was thus chosen as the inverting gain stage for the Optoelectronic Amplifier.

Table 6: Summary of Push-pull Inverter Performance

Parameter	***Value***
M1 Dimensions, W/L	12.00 μm/0.18 μm
M2 Dimensions, W/L	77.70 μm/0.18 μm
M3 Dimensions, W/L	278.25 μm/0.18 μm
Voltage Bias, V_{BIAS}	1.04 V
Current Bias, I_{BIAS}	4.775 mA
Transimpedance, R_F	2 KΩ
Feedback Capacitor, C_F	37 fF
Open-Loop Gain @ 1.65 GHz	27.4 dB
Bandwidth, f_{3dB}	1.7 GHz
Input Referred Noise, i_n	363 nA_{rms}

3.3 Conclusion

The theory and design of three different Transimpedance Amplifier configurations were discussed in this chapter. The current load and push-pull inverters provide satisfactory noise performance while providing the specified transimpedance gain. Nevertheless, the two inverter topologies were unable to meet the bandwidth required to transmit 2.5 GB/s. The cascode inverter was able to surpass the needed bandwidth and achieve the other provisions. At the end, the high gain, high bandwidth Cascode Transimpedance Amplifier was chosen as the preamplifier stage in the Optoelectronic Amplifiers design. The following chapter will discuss the design of the Limiting Amplifier, the second amplification stage of the Optoelectronic Amplifier.

Chapter 4: Limiting Amplifier

Up to this point it is assumed that the Transimpedance Amplifier converts the photodiode current to a minimum peak-to-peak voltage of 10 mV. The voltage signal at the output of the preamplifier must be further amplified by the Limiting Amplifier to reach the proper voltage swing necessary for data and clock recovery. The design of the LA must demonstrate high gain to achieve the 250 mV_{pp} necessary for clock and data recovery while still conserving the bandwidth at the output of the TIA [22], [29]. Noise considerations are not a major concern of the LA because the TIA is the dominant noise source. Nevertheless, it is desirable to minimize the noise contributions of the post amplifier stage so that the complete input referred noise contributions of the system are no worse than 10 % of the original TIA noise figure (after root-mean-square addition).

The interface used to compensate for the single-ended TIA to the differential LA is addressed in the next chapter. For now, the discussion will continue with the design of the LA with the assumption of a differential input.

As mentioned in the prior discussion on Optoelectronic Amplifier specifications, the LA must achieve a gain of 30 dB. A conventional Limiting Amplifier is shown in Figure 26. The total gain can be achieved with several stages of smaller differential amplifiers cascaded for improved bandwidth performance.

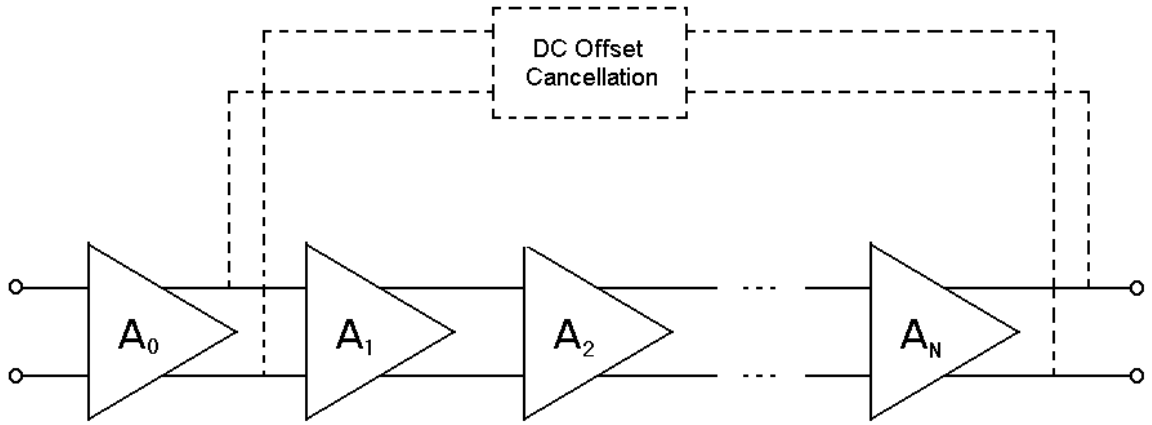

Figure 26: Limiting Amplifier Block Diagram

[22] suggests that the issue of maintaining high bandwidth in an LA can be corrected by gradually decreasing the size of the internal amplifiers by a factor of two, for example, a system of 4 amplifying stages with gains of 8x, 4x, 2x, and 1x. The steady decrease of sizes also lowers the load capacitance seen by the previous stage thus causing bandwidth extension. The limits to this method lay in the demands of the last stage's output drive capabilities and the maximum allowable LA input capacitance.

An alternative is to have matched amplifier blocks for equal input capacitance and drive capabilities. This method is advantageous in its simplicity of layout. As long as the load capacitance of blocks is small enough, the bandwidth can be achieved with this configuration. In this case, the total gain of the LA is given by

$$A_{Total} = \left(A_n\right)^{n+1} \tag{22}$$

where A_n is the differential gain of each stage and $n+1$ denotes the number of cascaded stages.

The matched differential amplifier topology was chosen given the aforementioned advantages. There are several possible architectures for a matched LA. The simplest solution is a cascade of resistive load differential amplifiers.

4.1 Resistive Load differential amplifier

The basic model for a LA block is that of a resistive load differential amplifier, depicting in Figure 27. The output voltage swing will be placed in the upper portion of the supply voltage of 3.3 V, i.e. a differential swing centered at 3.0 V with rails of plus or minus 300 mV.

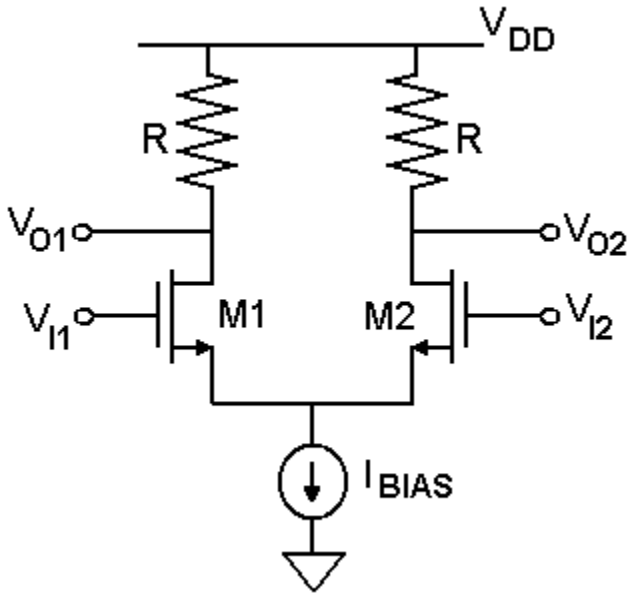

Figure 27: Resistive Load Differential Amplifier Schematic

The gain of the symmetric differential amplifier is set by the transconductance of the matched differential transistors, M1 and M2. Due to the symmetry of the design, the small-signal performance can be analyzed with the aid of half-circuit model in Figure 28 [24].

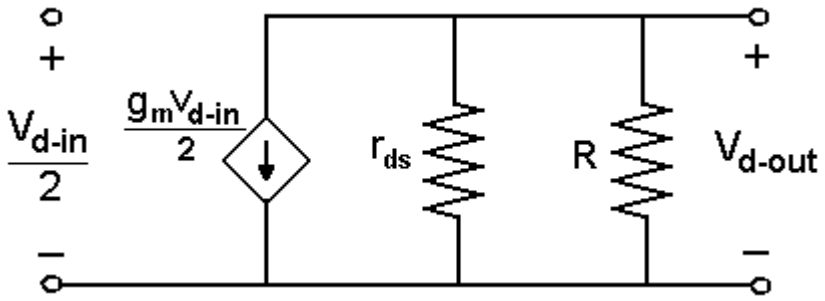

Figure 28: Small-signal Model of Differential Half-circuit

The gain expression is

$$\frac{V_{d-out}}{V_{d-in}} = 2 \cdot g_m \cdot \left(r_{ds} \,//\, R\right) \tag{23}$$

The common mode of the output voltage is determined by the resistor value and half of the bias current, I_{bias}, which is demonstrated by the relationship

$$V_{CM} = V_{DD} - \frac{I_{bias}}{2} \cdot R \tag{24}$$

With parameters I_{bias} and R_L set appropriately for DC operating points, the transconductance of the transistors can be changed to meet the appropriate gain requirements.

Figure 2 shows the AC response of a single stage of the LA. Note that the individual bandwidth of the device is seemingly sufficient to preserve the TIA bandwidth. The corner frequency of the differential stage is 2.5 GHz.

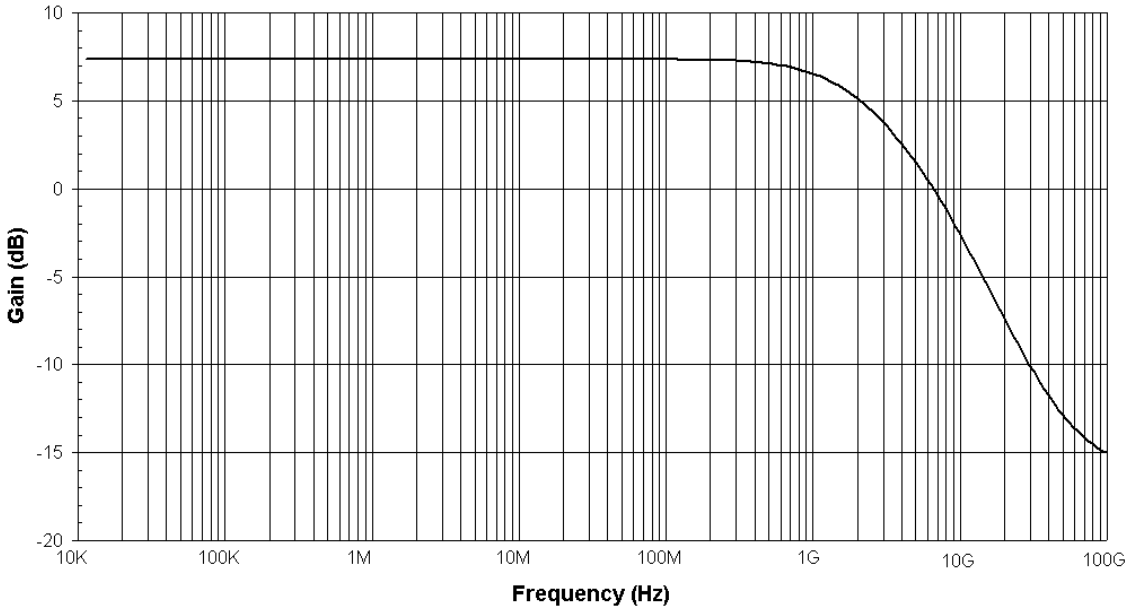

Figure 29: AC Response of Single Stage Resistive Load LA

Unfortunately, the bandwidth of a single stage must be greater to provide the LA, consisting of four cascaded stages, with sufficient bandwidth. A more complex design is required to achieve the desired bandwidth. Figure 30 shows the AC response of the four-stage resistive load LA with a bandwidth of 1.1 GHz

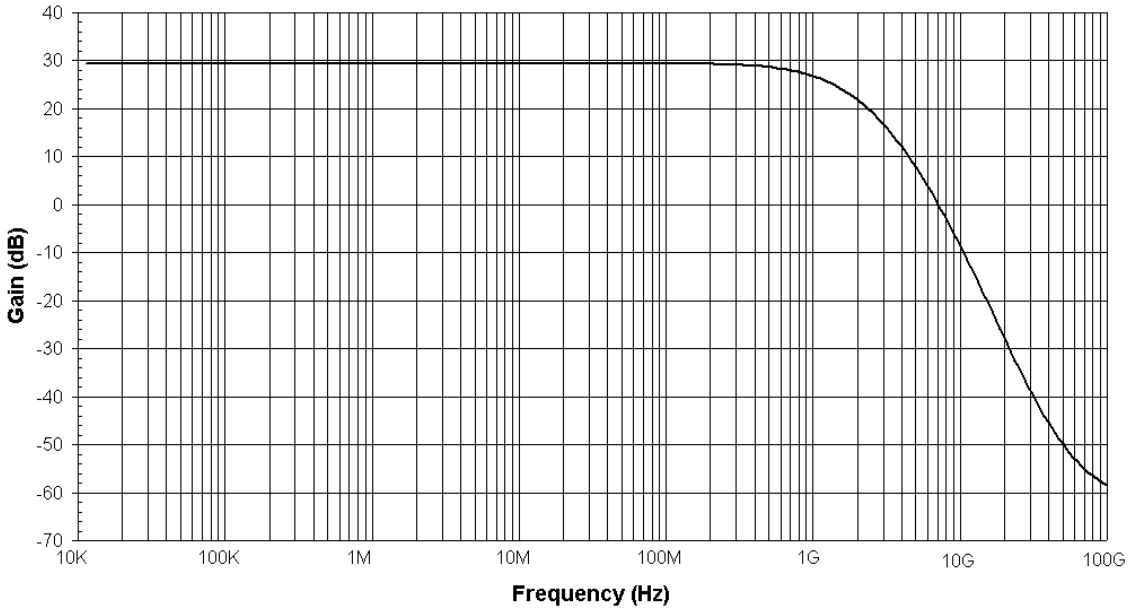

Figure 30: AC Response of Cascaded Resistive Load LA

The total performance of the resistive load LA is summarized in Table 7.

Table 7: Summary of Resistive Load LA Performance

Parameter	***Value***
Resistive Load, R	170 Ω
M1 & M2 Dimensions, W/L	159.94 μm/0.35 μm
Current Bias, I_{BIAS}	3.0 mA
Single Stage LA	
DC Gain	7.3 dB
Bandwidth, f_{3dB}	2.5 GHz
Input Referred Noise, e_n	273 μV_{rms}
Cascaded LA	
DC Gain	29.4 dB
Bandwidth, f_{3dB}	1.1 GHz

4.2 Inductive Load Differential Pair

A well known technique called “shunt peaking” is a possible solution used to extend the bandwidth. Shunt peaking allows for bandwidth extension with the addition of an inductor to the circuit, as shown in Figure 31. With the addition of the inductor, the

improved bandwidth for each differential stage will allow for sufficient improvement to meet the desired performance of the overall LA system [18].

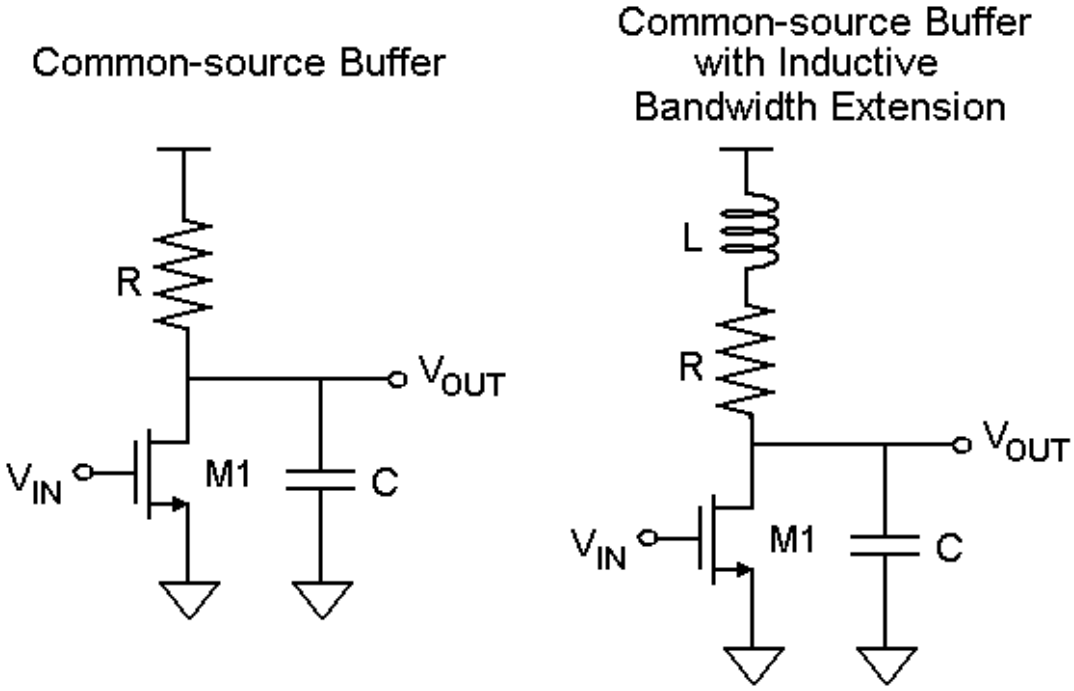

Figure 31: Shunt Peaking Configuration

With the addition of an inductive load to the resistive load already in place, the bandwidth can be further enhanced by moving the pole to a higher frequency. The small-signal performance of the simple common-mode buffer and the buffer with the added shunt peaking inductor can be analyzed with the aid of Figure 32 and Figure 33.

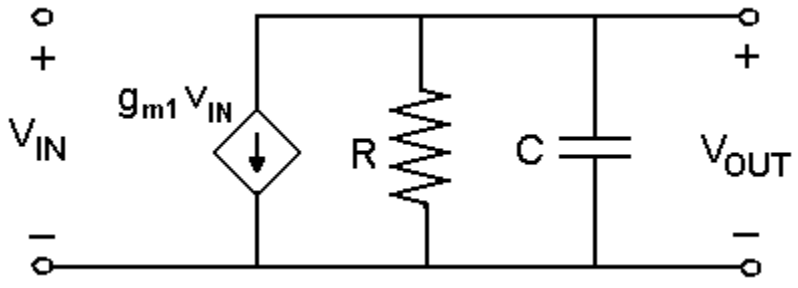

Figure 32: Small-signal of Common-source Buffer

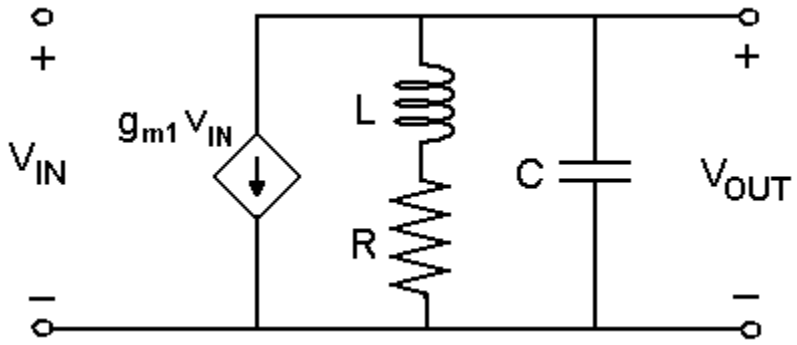

Figure 33: Small-signal of Common-source Buffer with Shunt Peaking

The transfer function of the simple common-source buffer in Figure 32 is

$$\frac{V_{out}}{V_{in}} = g_{m1} \cdot \frac{R}{1 + sCR} \tag{25}$$

The added inductor in Figure 33 alters the transfer function as shown by

$$\frac{V_{out}}{V_{in}} = g_{m1} \cdot \frac{R + sL}{1 + sCR + s^2CL} \tag{26}$$

The introduction of an inductor adds a zero to the LA stage transfer function in addition to a second pole. A properly sized inductor can strategically place a zero to partially tune-out the capacitive load, thereby extending the bandwidth. The second pole pushes the 3dB corner to a higher frequency [18]. [22] suggests that the optimal inductance can be found using the values of the load resistance and capacitance with the relationship

$$L_{opt} = 0.4 \cdot R^2 \cdot C \tag{27}$$

for a bandwidth extension of nearly 70%. Figure 34 shows the effects of a differential amplifier using the shunt peaking technique. The bandwidth was increased from 3.98 GHz to over 5 GHz with minimum peaking.

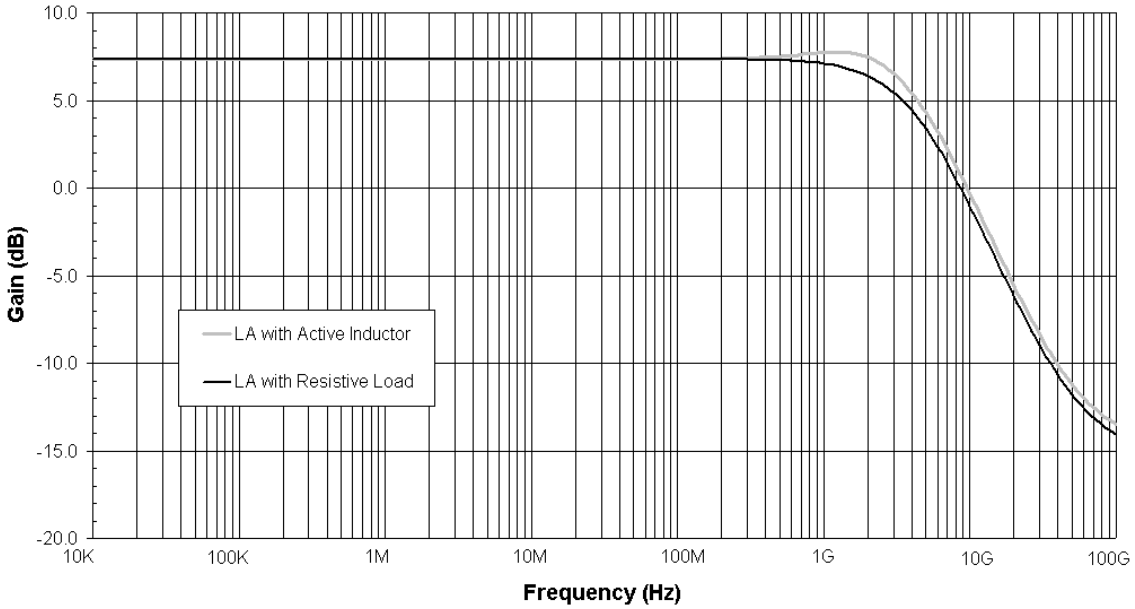

Figure 34: Bandwidth Extension Using Shunt Peaking in a Differential Amplifier

Unfortunately, a spiral inductor with high inductance, of magnitude greater than 20 nH, can be very cumbersome to design as well as expensive in silicon real estate [18]. Active inductors can be implemented to greatly reduce the area.

4.3 Differential Pair with Active Inductors

An active inductor can be created with the use of a FET and a resistor. As shown in Figure 35, the resistor connects the gate to the drain, putting the transistor in the active region.

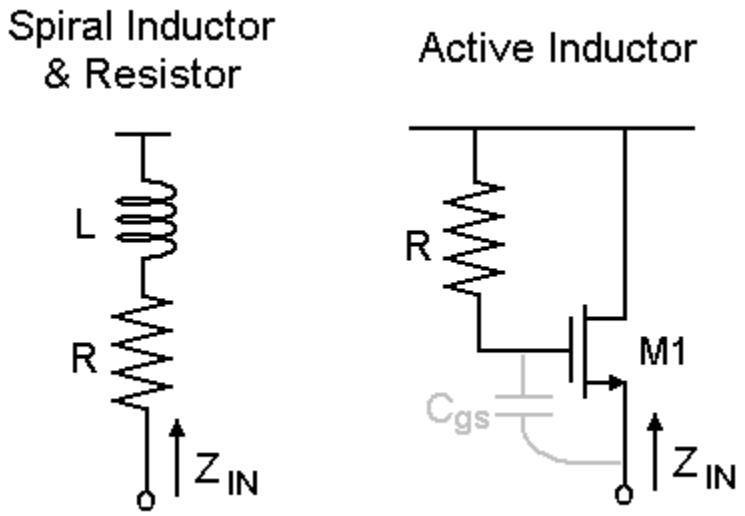

Figure 35: Active Inductor Schematic

Figure 36 shows the small-signal model of the active inductor.

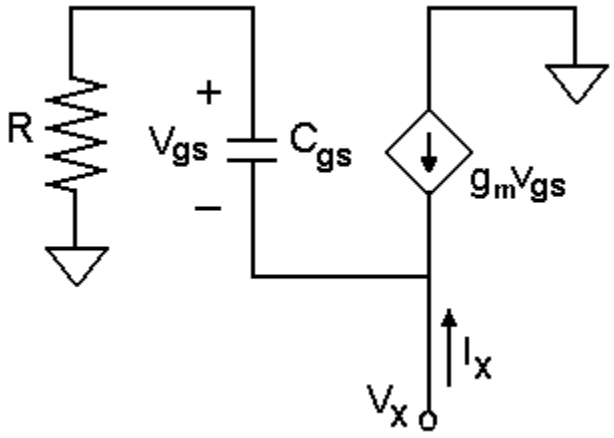

Figure 36: Small-signal Model for Active Inductor

The approximate small-signal impedance looking into the source of the active inductor is

$$Z_X = \frac{V_X}{I_X} \approx \frac{1 + sRC_{gs}}{gm} = \frac{1}{g_m} + s \cdot \frac{RC_{gs}}{g_m} \tag{28}$$

The impedance of the configuration consists of the resistive and inductive components. The resistive component is composed purely of the transistor parameters. Once the desired resistance of the transistor is achieved, the resistor between the gate and drain of the transistor can be sized for inductance.

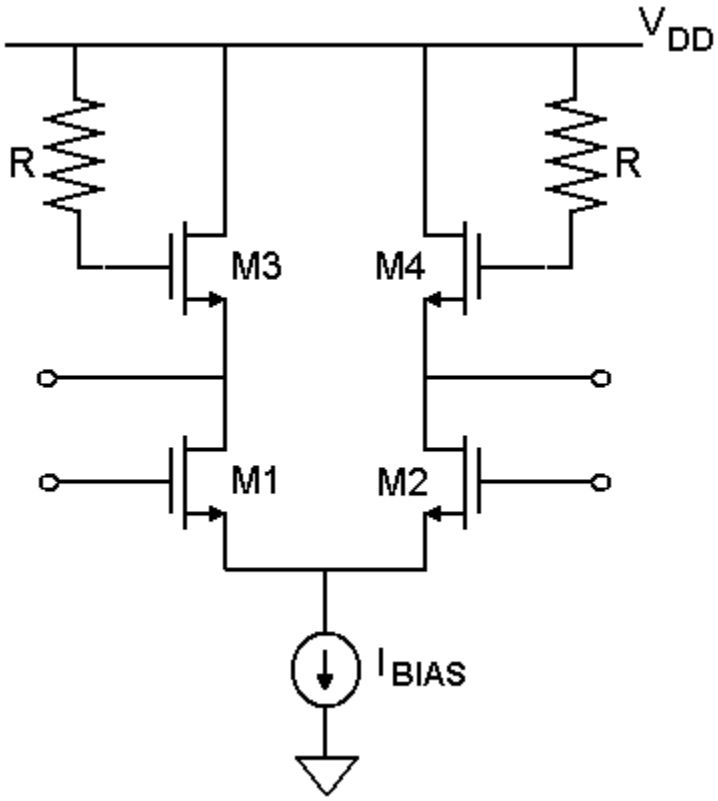

Figure 37: Schematic of Differential Amplifier with Active Inductors

The drawbacks of active inductors are the added noise and the voltage drop caused by the nMOS threshold voltage, which is worsened by the body effect [22]. The differential amplifier configuration with active inductors, depicted in Figure 37, puts a severe strain on the voltage range of the differential transistors. The nMOS threshold voltage demands a large voltage drop and leaves a very low ceiling in which the differential transistors must operate. Raising the voltage ceiling can be accomplished by biasing the gate of the active inductor above the VDD level, as shown in Figure 38.

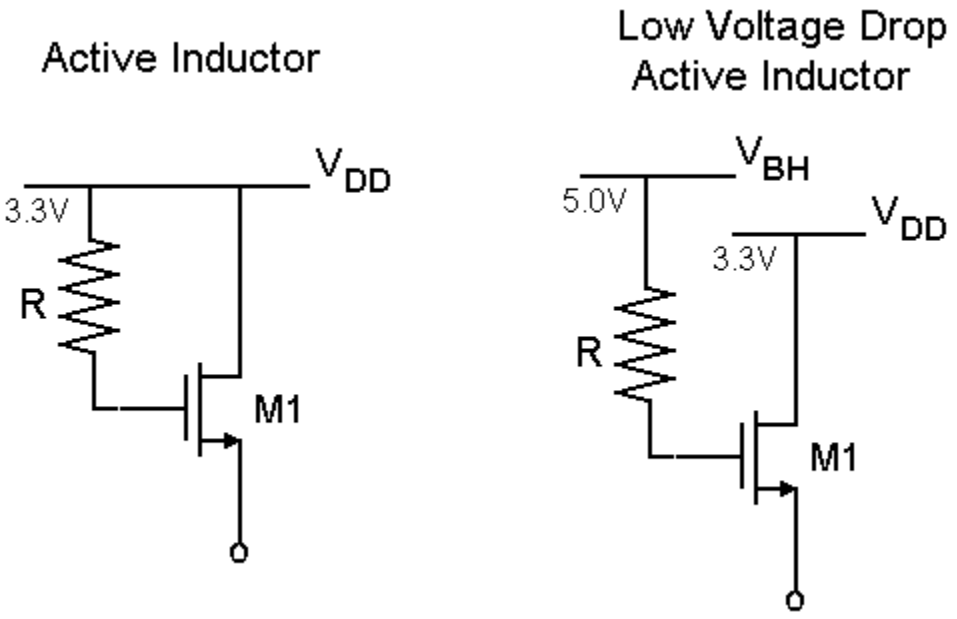

Figure 38: Active Inductor with a High Bias

With the low voltage drop active inductor in place of the load resistor from Figure 27, the voltage swing can be centered at 3.0 V with a bandwidth exceeding the BW of the TIA. Figure 39 illustrates one of the four identical differential amplifier stages used to create the LA.

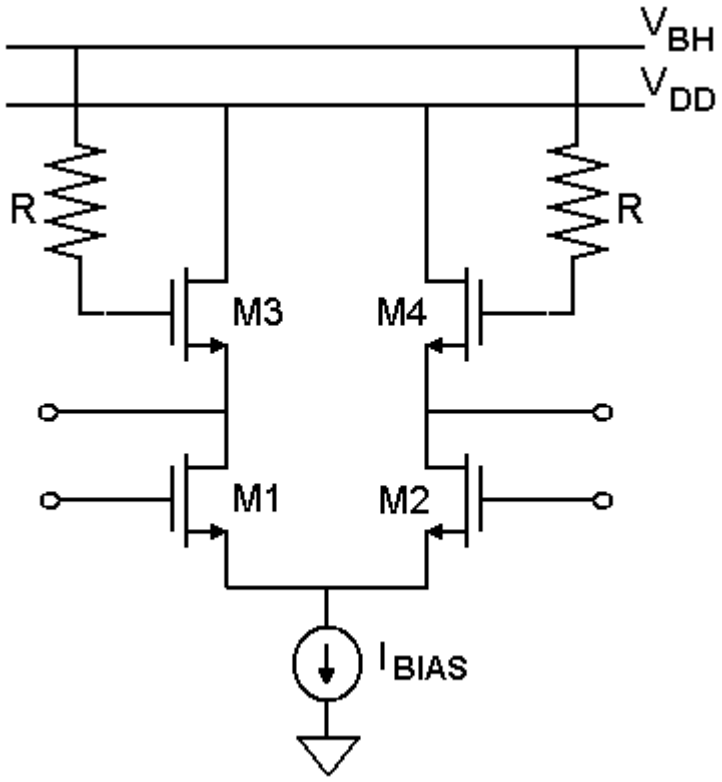

Figure 39: Schematic of Differential Amplifier with Low Voltage Drop Active Inductor

The bandwidth of the single stage low voltage active inductor is above 3 GHz, as demonstrated by Figure 40. The AC response of the cascaded Limiting amplifier is shown in Figure 41 with a bandwidth of 1.75 GHz.

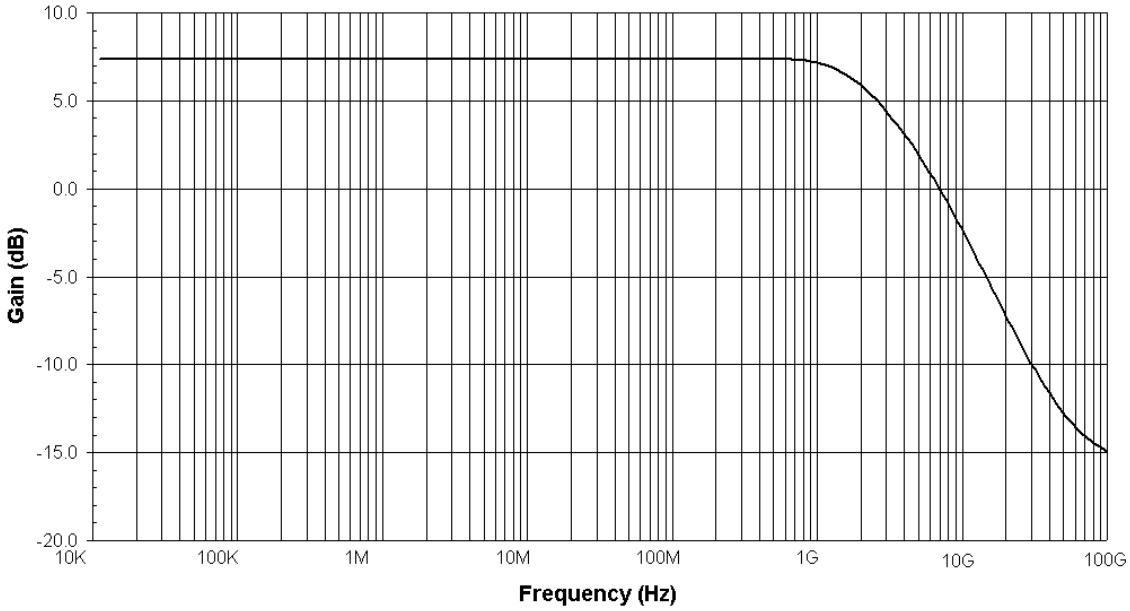

Figure 40: AC Response of Single Stage LA with Low Voltage Active Inductors

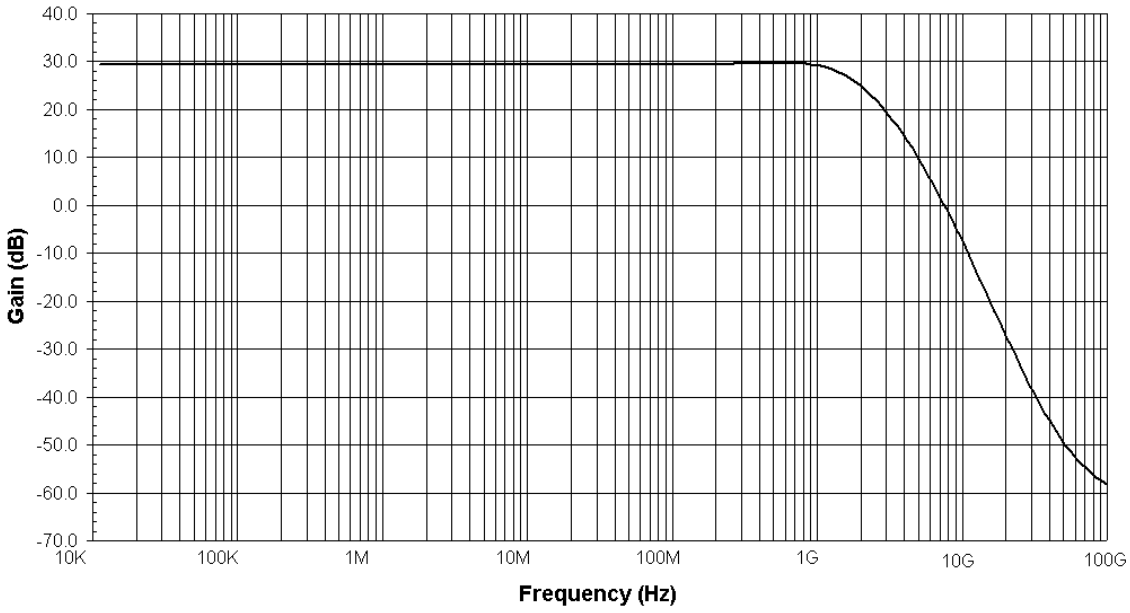

Figure 41: AC Response of Cascaded LA with Low Voltage Active Inductors

Figure 42 illustrates the noise model for the cascaded Limiting Amplifier. Due to the root-square method of noise addition, the input noise of each stage, e_n, can be referred back to the input of the first LA stage by the relationship

$$0.21 \cdot \bar{i}_{n-TIA} \cdot R_F = \bar{e}_n^{\,2} \cdot \frac{A_{LA}^8 + A_{LA}^6 + A_{LA}^4 + A_{LA}^2}{A_{LA}^8} \tag{29}$$

which yields

$$\bar{e}_n = \sqrt{\frac{0.21 \cdot \bar{i}_{n-TIA}^{\,2} \cdot R_F^2}{A_{LA}^8 + A_{LA}^6 + A_{LA}^4 + A_{LA}^2}} = 330 \mu V_{rms} \tag{30}$$

where $i_{n\text{-}TIA}$ is the input referred noise of the Transimpedance Amplifier.

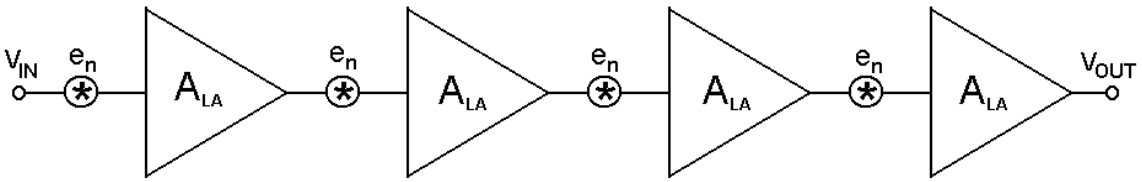

Figure 42: Noise Model of Limiting Amplifier

The simulated noise of the cascaded Limiting Amplifier resulted in an LA input referred noise figure of 270 μV_{rms}, which corresponds to a Optoelectronic Amplifier input referred current of 135 nA_{rms}. This LA input noise figure is well below the desired specification of 330 μV_{rms}. The total performance of the LA with Low Voltage Active Inductors is summarized in Table 8.

Table 8: Performance Summary of LA with Low Voltage Active Inductors

Parameter	***Value***
Active Load Resistors, R	≈10 KΩ
M1 & M2 Dimensions, W/L	159.94 μm/0.35 μm
M3 & M4 Dimensions, W/L	159.94 μm/0.35 μm
Current Bias, I_{BIAS}	3.0 mA
Single Stage LA	
DC Gain	7.3 dB
Bandwidth, f_{3dB}	3.7 GHz
Input Referred Noise, e_n	281 μV_{rms}
Cascaded LA	
DC Gain	29.4 dB
Bandwidth, f_{3dB}	1.8 GHz

4.4 Conclusion

The theory and design of a Limiting Amplifier was discussed in this chapter. At the end, a high gain, high bandwidth LA was described. The benefits of shunt-peaking were exploited with the use of active inductors to extend the bandwidth of the LA. The next chapter will discuss the offset correction scheme used to interface the single-ended TIA to the differential LA.

Chapter 5: Offset Correction

As previously mentioned, there is an interface conflict between the output of the Transimpedance Amplifier and the input of the Limiting Amplifier. The output of the TIA is single-ended and must interface with the differential LA. There are several possible solutions to this problem.

In an ideal differential system, an amplified differential signal would be produced from a differential input, as illustrated in left side of Figure 43. It is also possible to produce a favorable differential output when introducing a single-ended source. If the input amplitude to a differential amplifier is small enough, the differential input can be imitated with the original single-ended signal and its common mode bias (or DC offset), as illustrated in the right side of Figure 43.

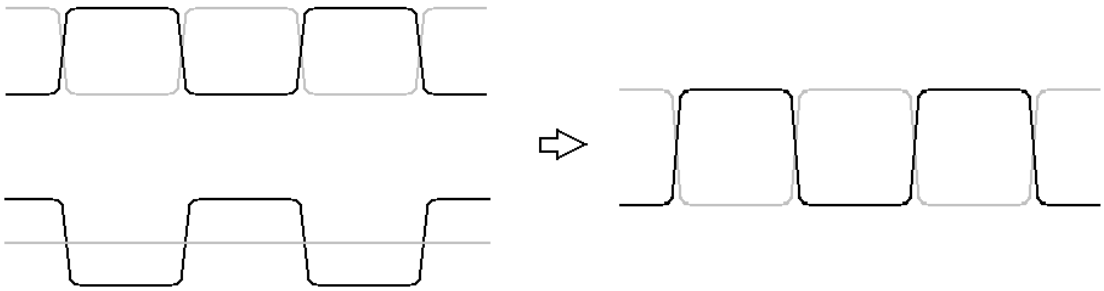

Figure 43: Effects of Pure Differential versus Common Mode Biased Single-ended Input

Performing DC offset correction by finding the proper bias point must be precise. Two examples of biasing are shown in Figure 44. The first example is that of a poorly biased differential input. If the DC offset of the signals was to increase, the output differential signals of the amplifier would begin to drift away from each other. The same holds true for a decreased DC offset. The second example in Figure 44 shows the effects of proper biasing. The output waveform is generated as a result of the common mode voltages of both signals being equal.

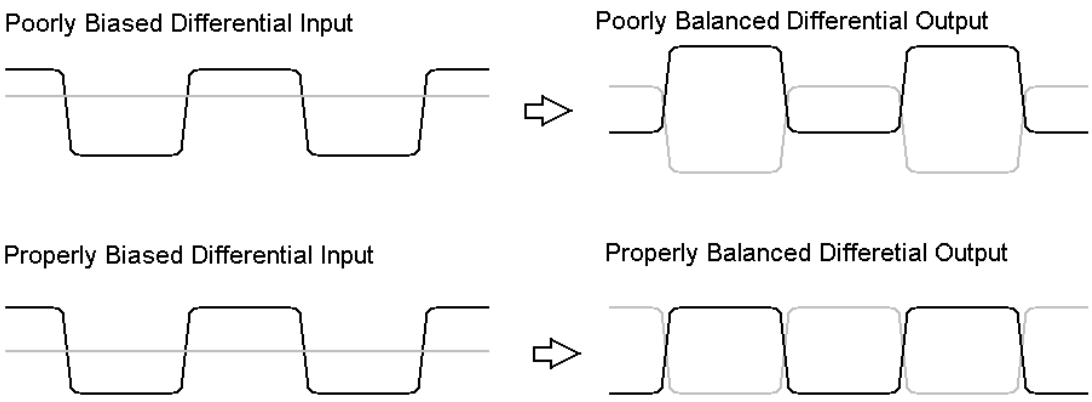

Figure 44: Effect of Poor Biases in Differential Signals

5.1 Low Pass Filter and AC Coupling

In order to find the proper dc bias point, there are two fundamental options: low pass filtering or AC coupling the single-ended output of the TIA at the input of the LA. The common mode of a signal can be found with a low pass filter. This simple method is illustrated in Figure 45. The original signal is fed to one of the inputs of the differential LA. The second LA input is biased with the result of a low pass filter, which centers the differential signal at the proper common-mode voltage.

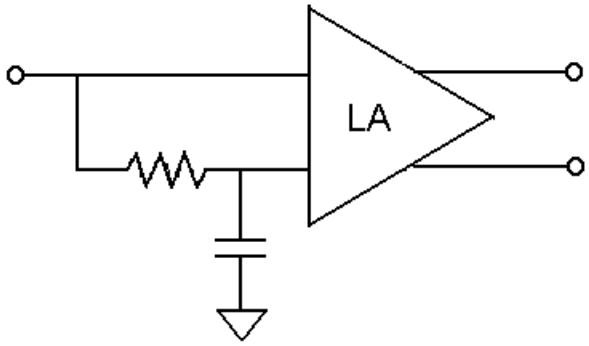

Figure 45: Low Pass Filter Offset Correction Method

The low-pass filter has the response shown in Figure 46. Simulations provided satisfactory high frequency attenuation with a corner frequency of 16 MHz, which can be achieved with resistor and capacitor values of 1 kΩ and 10 pF, respectively.

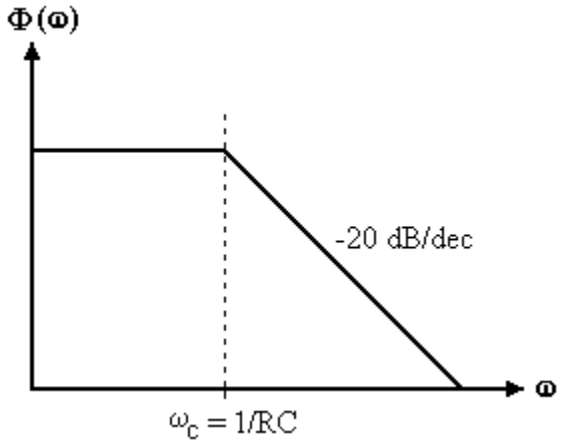

Figure 46: Low-Pass Filter Response

An alternative consisting of the same fundamentals is the AC Coupling method. This configuration, depicted in Figure 47, uses a high pass filter to center the single-ended signal to a predetermined bias voltage, V_b. Essentially, the bias of the incoming signal is forced to the desired voltage [21].

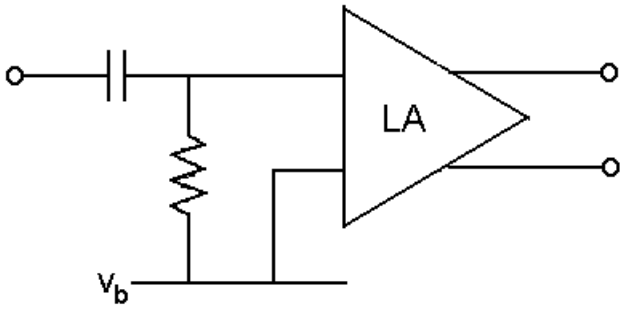

Figure 47: Offset Correction with AC Coupling

The AC Coupling method has a response as shown in Figure 46. The DC offset is completely removed with AC coupling, regardless of the corner frequency; however, the high frequency components of the signal must be conserved for signal integrity. The corner frequency should be as small as possible. Simulations with corner frequency of 16 MHz provided adequate signal propagation in terms of frequency components.

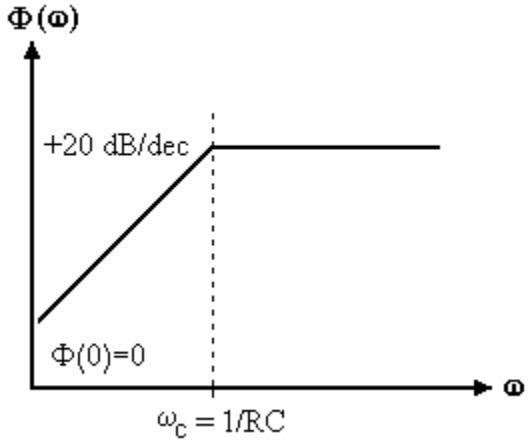

Figure 48: AC Coupling Response

Although the AC coupling and low-pass filter offset correction methods are effective solutions, their major drawback is the dependence on the DC signal component. The best results are achieved only when a 50% duty cycle is assured. As the duty cycles vary to either extreme, the DC offset also strays. The duty cycle dependency can be addressed with a properly tuned transmission encoding scheme. However, a more robust, duty cycle independent solution is more desirable.

5.2 Offset Feedback

The feedback method is much more complex in nature than the AC coupling and low-pass solutions. The goal of the loop is to constantly compare the bias levels of the output signals and adjust the input bias accordingly. Figure 49 illustrates the Offset Feedback method.

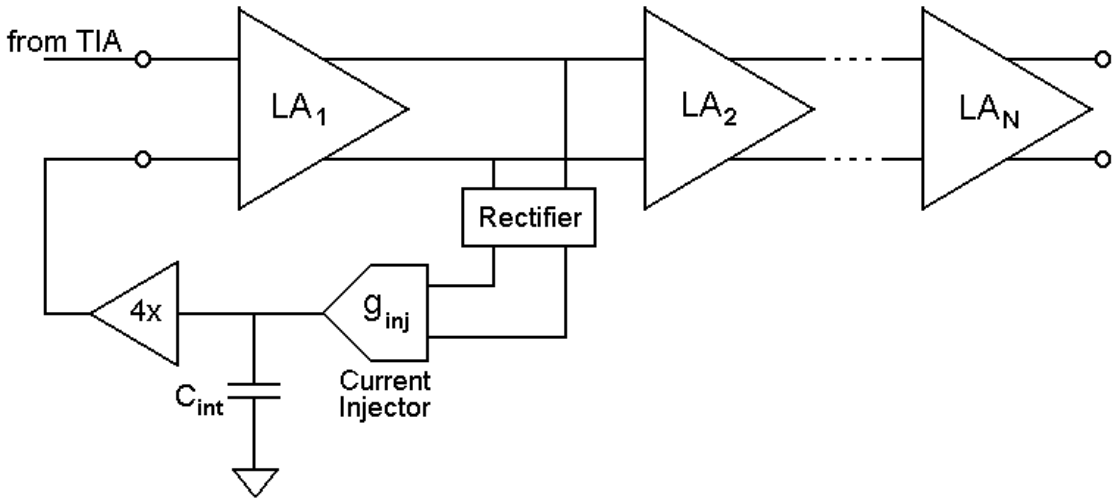

Figure 49: Offset Control with Feedback

The outputs of the first differential amplifier are monitored to insure that their maximum swings share the same offset. The rectifier generates DC bias voltages that are proportional to the peaks of differential voltage swings. A difference in the bias voltages indicates misbalanced differential signals caused by an erroneous offset at the input of LA_1. The error correction behavior of the current injector and capacitor is similar to an integrator. The bias voltages are monitored by the current injector, which will sink or source current to the capacitor to remove the error. The voltage across the capacitor is then buffered with a gain of 4 and fed back to the input of LA_1. At steady state, the capacitor will maintain a scaled-down version of the offset voltage necessary for proper DC biasing of the LA.

As with any feedback system, stability is an issue. Figure 50 illustrates the stability analysis model for the offset feedback.

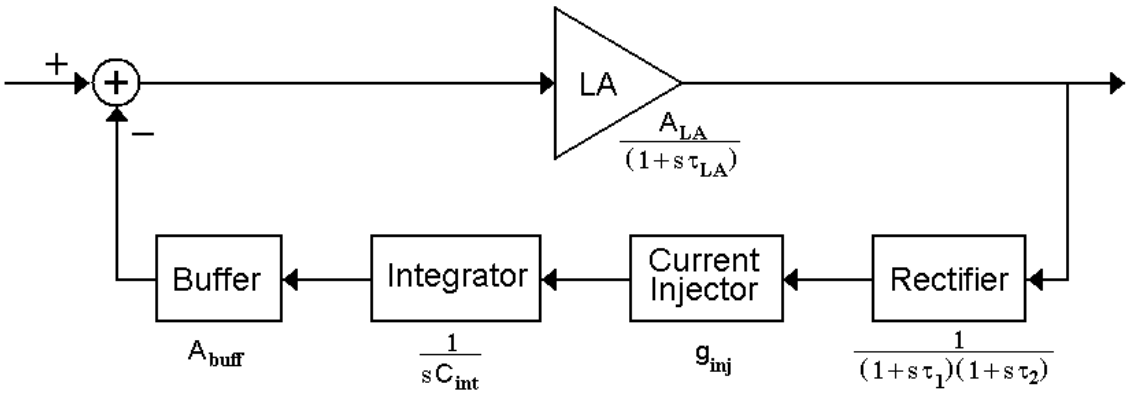

Figure 50: Model of Offset Feedback Method

The transfer function of the loop can be represented by the standard form equation

$$H(s) = \frac{forward}{1 + forward \cdot feedback} = \frac{\frac{A_{LA}}{1 + s \cdot \tau_{LA}}}{1 + \frac{A_{LA}}{1 + s \cdot \tau_{LA}} \cdot A_{buff} \cdot g_{inj} \cdot \frac{1}{C_{\text{int}}} \cdot \frac{1}{(1 + s \cdot \tau_1) \cdot (1 + s \cdot \tau_2)}} \tag{31}$$

The LA parameters, A_{LA} and τ_{LA}, were already predetermined from the design in the previous chapter. The rectifier poles, τ_1 and τ_2, are essentially set in order to produce clean control voltages and do not offer much flexibility. Thus, optimization to ensure stability must be performed with the use of the remaining model variables: C_{int}, A_{buff}, g_{inj}.

In a stable system, all pole locations are in the open left half-plane of the *s*-Plane. The closed-loop function will become unstable only when its denominator equals zero. The Routh-Hurwitz Stability Criterion states that for a fourth order polynomial, with a denominator of

$$P(s) = a_4 \cdot s^4 + a_3 \cdot s^3 + a_2 \cdot s^2 + a_1 \cdot s + a_0 = 0 \tag{32}$$

is guaranteed to have all of its roots in the left half-plane if all of the coefficients, a_n, are strictly positive and

$$a_3 \cdot a_2 > a_4 \cdot a_1 \tag{33}$$

$$a_3 \cdot a_2 \cdot a_1 > a_4 \cdot a_2^2 + a_3^2 \cdot a_0 \tag{34}$$

The expanded coefficients of *H(s)* correspond to

$$a_4 = C_{\text{int}} \cdot \tau_{LA} \cdot \tau_1 \cdot \tau_2 \tag{35}$$

$$a_3 = C_{\text{int}} \cdot \left(\tau_{LA} \cdot \tau_1 + \tau_{LA} \cdot \tau_2 + \tau_1 \cdot \tau_2 \right) \tag{36}$$

$$a_2 = C_{\text{int}} \cdot \left(\tau_{LA} + \tau_1 + \tau_2 \right) \tag{37}$$

$$a_1 = C_{\text{int}} \tag{38}$$

$$a_0 = G \cdot A_{buffer} \cdot g_{injector} \tag{39}$$

After assuring that the system was stable with the Routh-Hurwitz Stability Criterion, the values were then further massaged to achieve satisfactory performance [31]. The transient response of the Offset Feedback method is shown in Figure 51. The figure shows the output of the first stage LA as the Offset Feedback circuit converges to the proper DC offset.

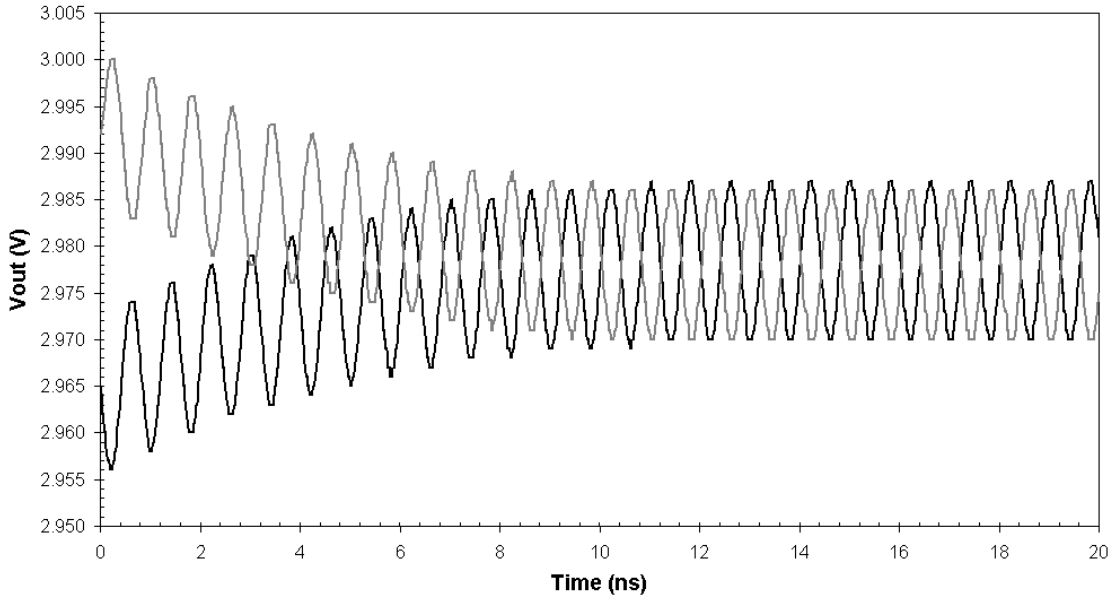

Figure 51: Transient Response of the Offset Feedback Method

Table 9 summarizes the parameters of the Offset Feedback configuration.

Table 9: Summary of Offset Feedback Parameters

Parameter	***Value***
LA Gain, A_{LA}	29.5
LA Bandwidth, τ_{LA}	1.8 GHz
Buffer Gain, A_{buff}	4
Integrator Capacitance, C_{int}	1 pF
Injector Transconductance, g_{inj}	5 μA/V
Rectifier Pole, τ_1	500 ps
Rectifier Pole, τ_2	250 ps

5.3 Conclusion

The theory and design of an Offset Feedback scheme used to interface the single-ended Transimpedance Amplifier to the differential Limiting Amplifier was discussed in this chapter. The following chapter will discuss the layout of the test chip with the details of each functional block.

Chapter 6: Verification, Testing and Results

The goal of the test chip was to corroborate the performance results of the simulations. All schematic entry, simulation, and layout were developed with the use of the Cadence suite of design and layout tools. The process used to fabricate the test chip was a TSMC 0.18 μm 6-metal 1-poly CMOS process via the IC fabrication service of MOSIS.

The test chip included ten separate circuits for simulation correlation: one full Optoelectronic Amplifier, three independent cascode Transimpedance Amplifiers, three independent current load TIAs, and three independent push-pull TIAs.

6.1 Transimpedance Amplifier

As mentioned earlier, the TIA serves an extremely important role in the Optoelectronic Amplifier. It is the first gain stage of the system and defines the system level sensitivity. The TIA's position as the first amplification stage also makes it the key contributor of noise in the system.

Nine TIAs were added to the test chip to allow for analysis of the vital first stage of the Optoelectronic Amplifier. The three topologies of TIAs were included on the chip, current load, push-pull, and cascode. Each TIA configuration was created with three different transimpedance gains, 500 Ω, 1 kΩ, 2 kΩ, to further study the effects of the transimpedance gain on the bandwidth of the TIA.

The output drive capabilities of the TIAs were developed for the interface with the LA. In order to allow the TIA output to be tangible off-chip, an output driver was required. The current drive necessary for off-chip TIA output signals is generated with a drive transistor. The output of the TIA is connected to an open-drain P-type transistor. The drain of the drive transistor is connected directly to the pad for the package pin. An external resistor connected from ground to the pin will serve to create the current to voltage conversion off-chip. Figure 2 illustrates the TIA on the test chip with the use of

the P-type driving transistor. The bias voltages represented are generic and are not necessary of each TIA topology.

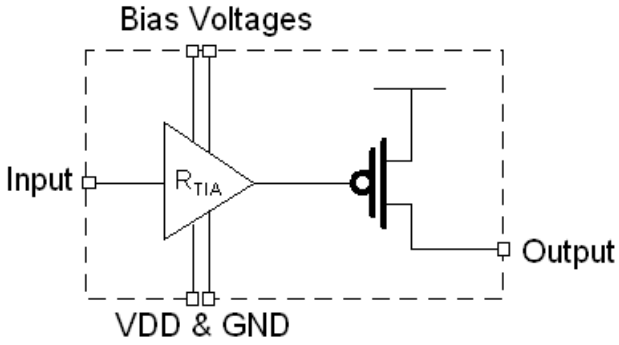

Figure 52: Block Diagram of TIA on Test Chip

6.2 Optoelectronic Amplifier System

The Optoelectronic Amplifier built on the test chip included the TIA, LA, and Offset Feedback circuitry, as shown in the block diagram in Figure 53.

There is an added buffer between the TIA and the LA. The buffer serves to level shift the output of the TIA to the required input levels of the LA. The LA expects an input centered at 3 V with a 300 mV amplitude. The output of the TIA starts at approximately 600 mV and must be raised to the satisfactory LA input voltage level. The buffer also adds the small amount of gain that is lost due to the single-ended to differential conversion.

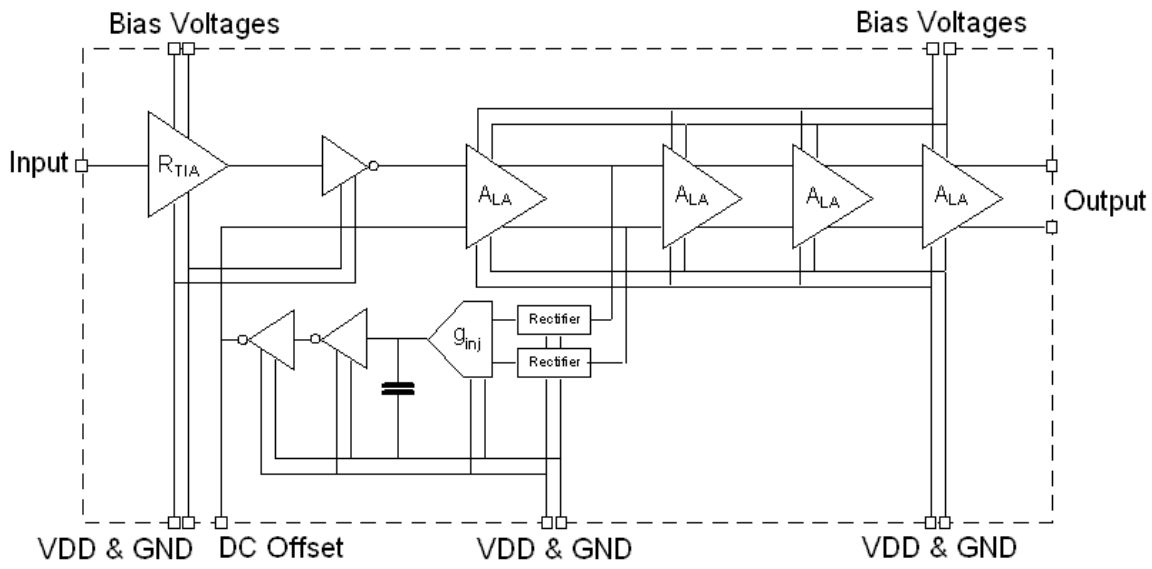

Figure 53: Block Diagram of Optoelectronic Amplifier System on Test Chip

The issue of transmitting the output signals off-chip was addressed by increasing the drive capabilities of the last LA stage. Three LA stages in parallel where used to drive the test chip pin.

6.3 Test Chip

A photograph of the test chip is shown in Figure 54. The silicon real estate was shared between two projects: this MS thesis to create the Optoelectronic Amplifier and PhD thesis for another student on the relationship between kappa, the time domain noise figure of merit, frequency, channel width, and channel length.

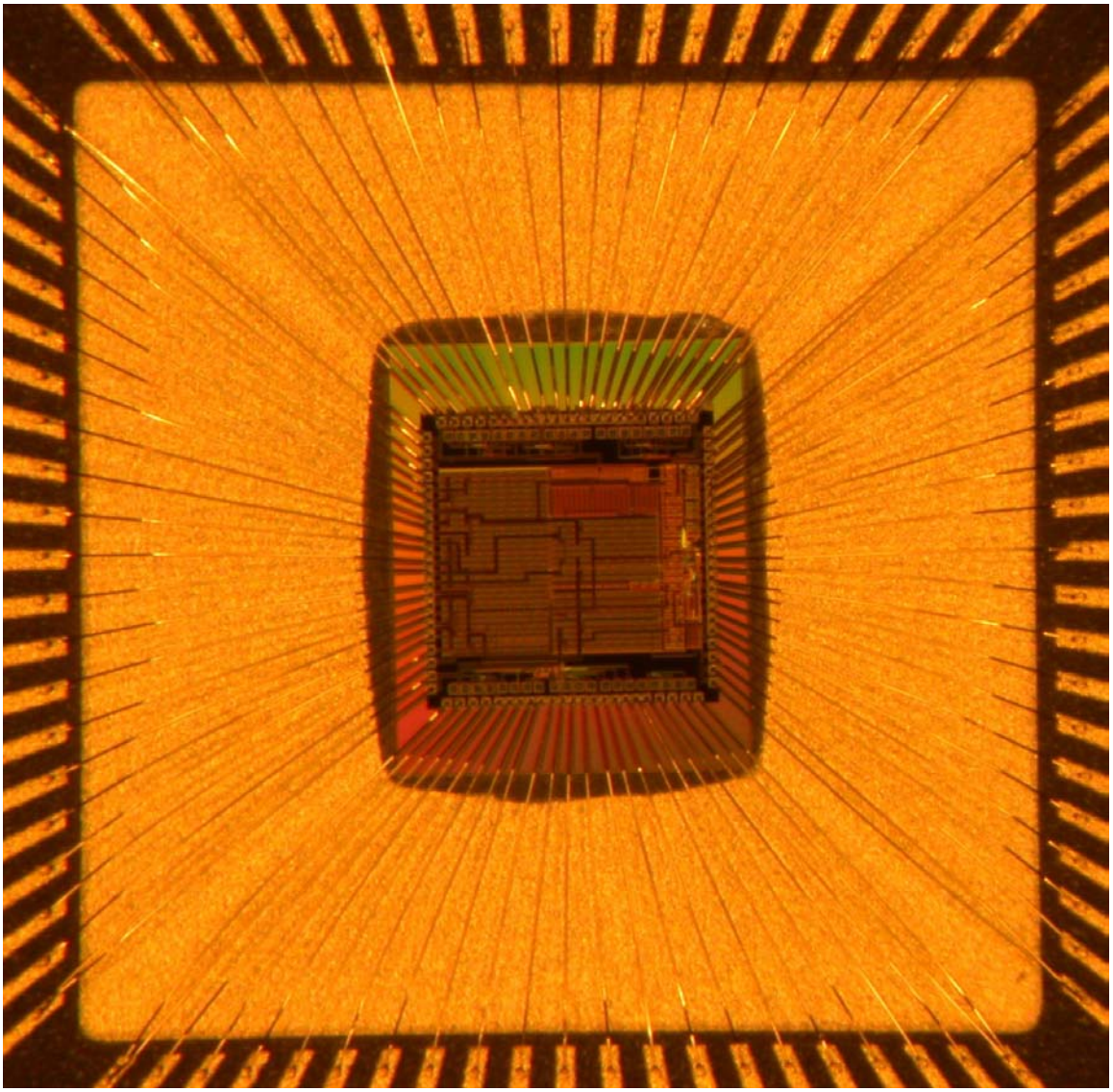

Figure 54: Photograph of Whole Test Chip

The Optoelectronic Amplifier and the various TIAs used the minority of the silicon die space, as illustrated in Figure 55. The die size is 2.4 mm x 2.4 mm. The Optoelectronic Amplifier uses 360 μm x 125 μm of die area. Each TIA instance consumes 90 μm x 45 μm.

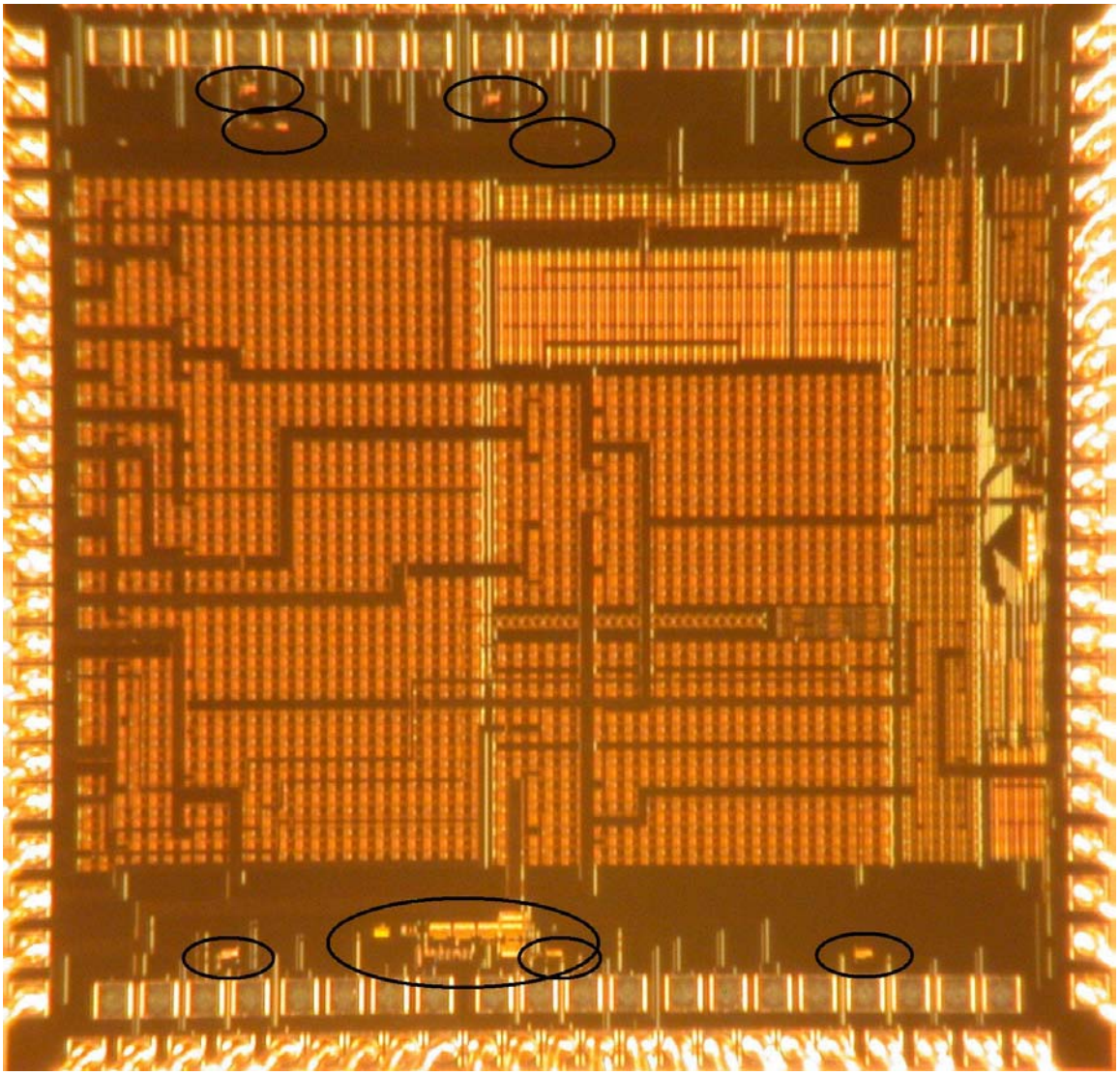

Figure 55: Test Chip with Highlighted TIAs and Optoelectronic Amplifier

Note the 10 independent circuits line the top and bottom pins. The circuits required more pins than where available: the Optoelectronic Amplifier uses 15 pins and the assortment of TIAs consumes a total of 45 pins. Two rows of bond pads where used to increase the number of pins available for the project. Two iterations of the test chips where created, each bonded to a different row of pads.

6.4 Evaluation Board

The evaluation board interface to the TIA has to supply the bias voltages and currents, as well as the power supply, as illustrated in Figure 56. The RF input to the TIA is generated with a voltage signal converter to a current via a resistor. The output of the TIA, corresponding to the driving transistor drain, was connected to a resistor for current to voltage conversion.

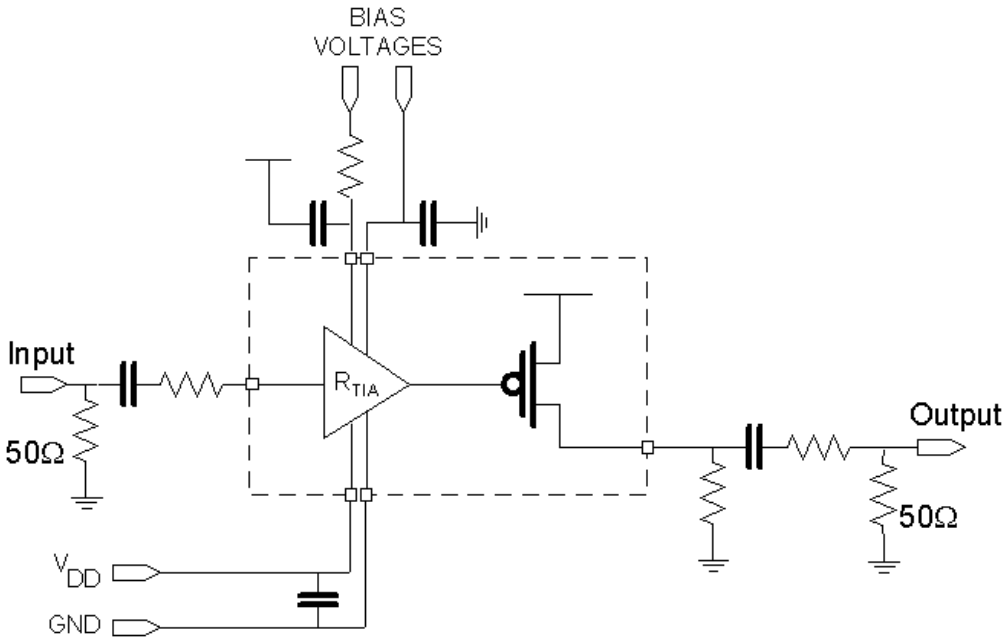

Figure 56: TIA Evaluation Board Interface

The interface to the Optoelectronic Amplifier was similar, as shown in Figure 57. Note that the output of the Optoelectronic Amplifier does not require the current to voltage conversion.

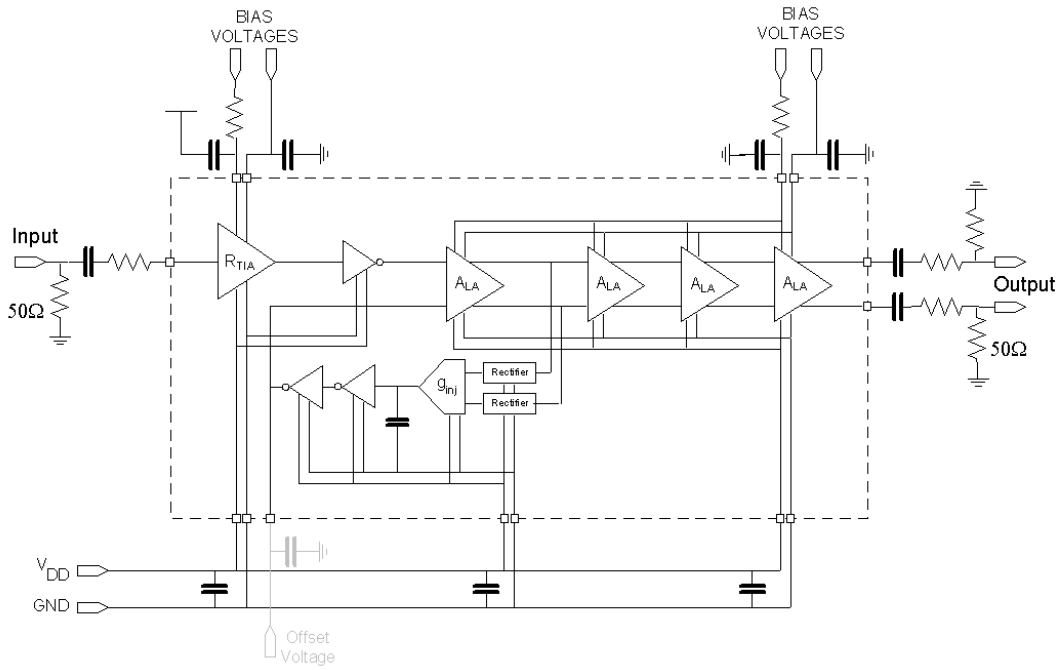

Figure 57: Optoelectronic Amplifier Evaluation Board Interface

Both the TIA and Optoelectronic Amplifiers required some network matching, to convert the output impedance to a 50 Ω environment for connectivity with laboratory equipment.

Figure 58 shows the picture the evaluation board. Recall that two rows of bond pads where used to increase the number of pins available for the project. Two iterations of the test chips were manufactured, each bonded to a different row of pads. The evaluation board was laid out with dual footprints, corresponding with both bonding iterations. The iteration with the bonded inner row of pads is placed in the device mount with no rotation. The iteration with the bonded outer row of pads is placed in the device mount with a 90° rotation (counter clockwise).

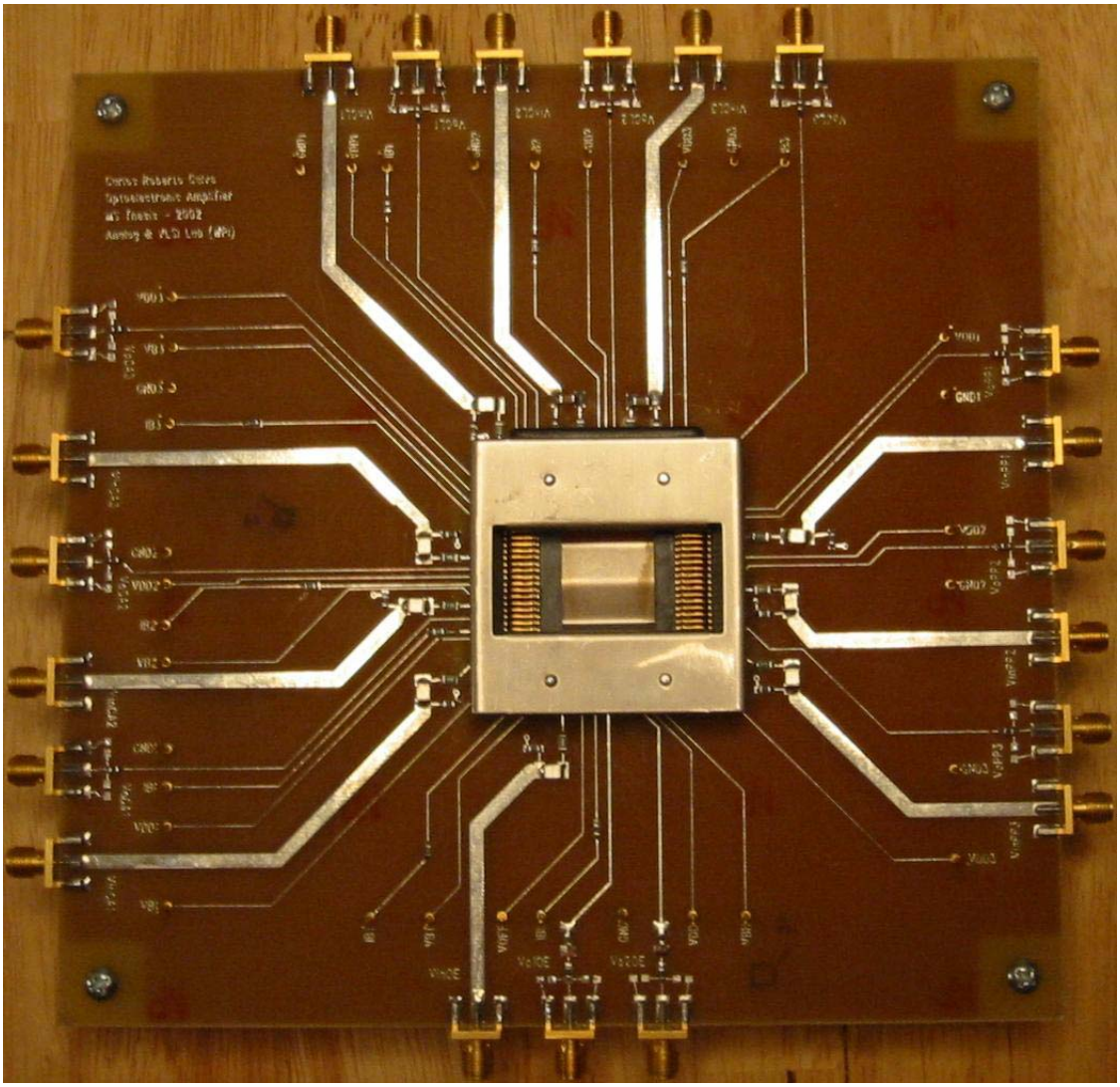

Figure 58: Picture of the Evaluation Board

6.5 Amplifier Measurements

The goal of the test chip was to corroborate the results of the simulations of the TIAs and the Optoelectronic Amplifier. Because the test chip required more than 70 pins, there was a limited choice for chip packages. The package used for the test chip was an 84-pin ceramic leadless chip carrier from Kyocera America, Inc.. The expected bandwidth of

the package is in the order of 500 - 800 MHz, well below the bandwidth of the Optoelectronic Amplifier. Nevertheless, simulation of the design with the estimated package parameters showed that the high-speed signals could propagate off chip, albeit with significantly attenuated signals.

Initial high-speeds testing of the TIAs on the test chip provided unfavorable results. The speed of the device was brought down well below the expected bandwidth of the package to verify basic functionality of the amplifiers. The experiment was conducted by monitoring the input signal at the closest point to the package and the output of the TIAs. The input was a sinusoid of 30 mV_{rms} with frequencies spanning the frequency range of the signal generator, from 300 KHz to 3 GHz. The gain was calculated at each frequency interval to determine the bandwidth of the TIA. Figure 1 shows the results of the gain calculations.

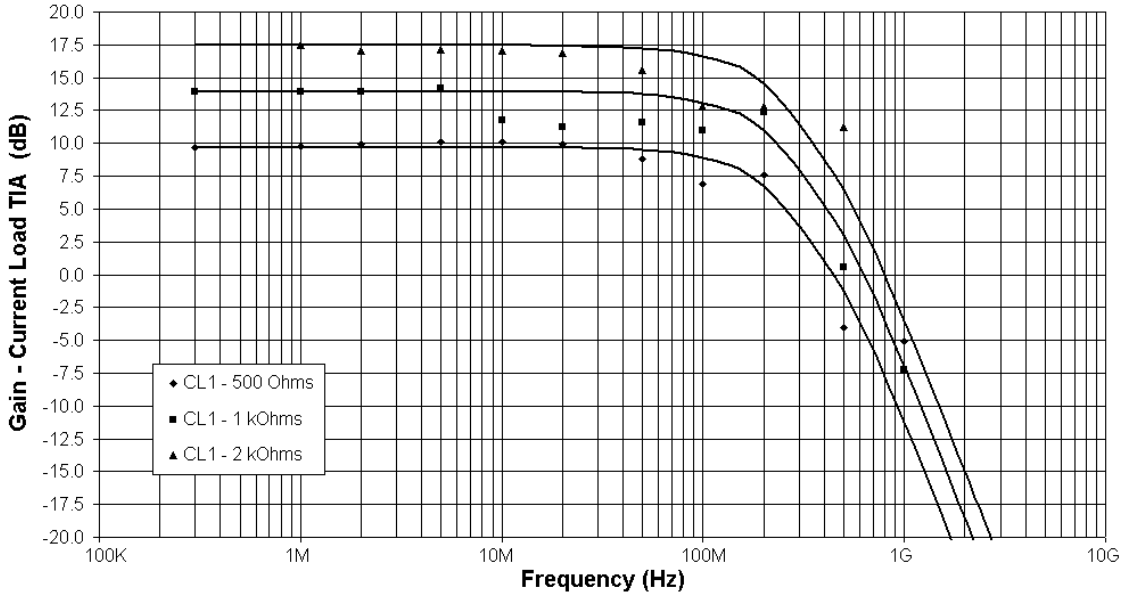

Figure 59: Measured Bandwidth of the Current Load TIA

The measured response was modeled with the two pole representation

$$A(s) = \frac{A_o}{(1 + s\tau_c)^2} \tag{40}$$

where A_o is the low frequency gain and τ_c is the 3 dB bandwidth. The bandwidth was found to be between 450 to 500 MHz.

The package bandwidth of 500 to 800 MHz was expected. Thus, it would seem that the ceramic package is filtering out the high frequencies. The test board also provides some filtering. Figure 60 shows the response of the test board. The measurement was made by monitoring the input of the package socket while sweeping the frequency.

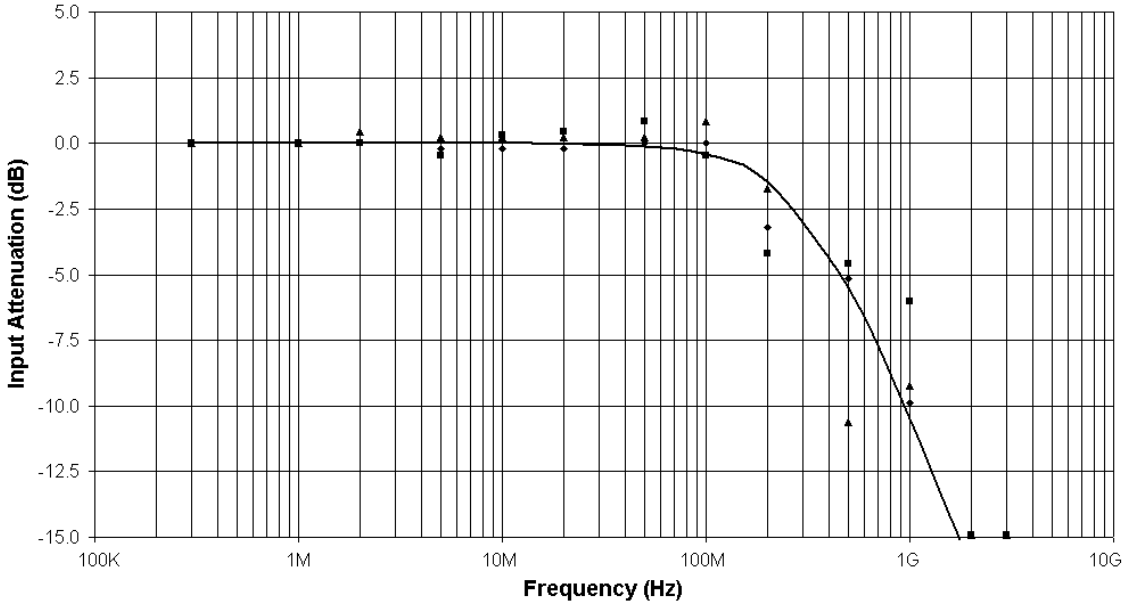

Figure 60: Measured Bandwidth of Test Board

The response of the board was modeled with the single pole representation

$$A(s) = \frac{1}{1 + s\tau_b} \tag{41}$$

where τ_b is the 3 dB bandwidth. The test board bandwidth also corresponds to 500 MHz.

The cascode and push-pull TIA configurations demonstrated bandwidth limitations similar to those of the current load TIA. It was expected that the Optoelectronic Amplifier would be affected by the same bandwidth restrictions as the TIAs. However, due to time limitations the performance of the system was not confirmed. Since most of the vital signals of the Optoelectronic Amplifier are not accessible off chip, only a limited number of options exist for debugging. The only accessible signal to the LA, aside from the output, is the offset bias to the first LA stage. In spite of this, the offset voltage was changed with nominal change resulting in unconfirmed system functionality.

6.6 1/f Noise

1/f, also known as flicker noise, is one of the major concerns in IC design in CMOS. The source of the noise is the carrier traps in semiconductors which capture and release carriers randomly [1]. The spectral density of *1/f* noise is approximated by

$$\overline{V}_n^2(f) = \frac{k_v^2}{f} \tag{42}$$

where k_v is a constant. As denoted by its name, the noise is inversely proportional to frequency, f. The root spectral density of flicker noise is given by

$$\overline{V}_n(f) = \frac{k_v}{\sqrt{f}} \tag{43}$$

It is important to note that the noise falls off at a rate of -10 dB/decade because it is inversely proportion to $\sqrt{f}$, as shown in Figure 61 [12]. The *1/f* noise energy is concentrated at the low frequencies due to the inverse relationship with frequency, yet maintains equal power in every decade.

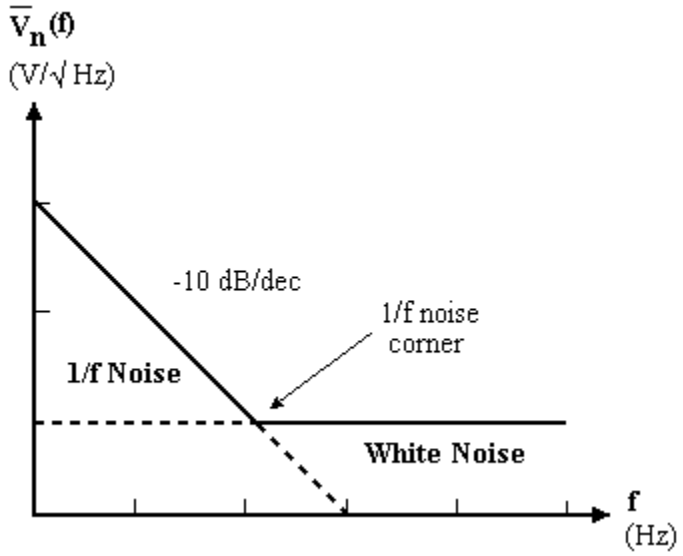

Figure 61: Noise Signal with 1/f and White Noise

As previously mentioned, the test chip silicon was shared between the Optoelectronic Amplifier design and another student's study on jitter in CMOS single-ended ring oscillators and the relationship between kappa - the time domain noise figure of merit, frequency, channel width, and channel length.

Jitter in Deep Submicron CMOS Single-Ended Ring Oscillators

Single-ended ring oscillators (SROs) are appealing for applications requiring high speed and moderate jitter. As a guide to design, the time domain figure-of-merit κ is measured as a function of channel width, length, and inverter stage delay. Although use of a deep submicron process allows the possibility of higher VCO frequency, it also introduces the problem of a higher 1/f noise corner. In previous work [33] [34] the VCO design process is simplified by assuming the 1/f noise corner to lie below the PLL loop bandwidth; in deep submicron this assumption is no longer valid [32].

For a VCO dominated by white noise sources, the standard deviation of jitter after time delay ΔT is [3]

$$\sigma_{\Delta T} = \kappa\sqrt{\Delta T} \tag{44}$$

where κ is the time domain figure of merit.

In the frequency domain, a phase noise plot for a VCO dominated by white noise will have the form

$$S_{\phi}(f) = \frac{N_1}{f^2} \tag{45}$$

where N_1 is a frequency domain figure of merit. In this case the plot of phase noise will have a slope of -20dB/decade [32].

In the presence of 1/f noise, the slope of the phase noise plot is -30dB/decade and the model of (42) no longer applies. However, when the PLL loop is closed around the VCO, the 1/f noise contribution becomes negligible if the PLL loop bandwidth f_L exceeds the 1/f noise corner. Given the condition of negligible 1/f noise, a simple technique was given in [34] to relate time domain and frequency domain figures of merit by

$$\kappa = \frac{\sqrt{N_1}}{f_o} \tag{46}$$

and to predict the closed-loop jitter with respect to the PLL reference clock

$$\sigma_x = \kappa\sqrt{\frac{1}{4\pi f_L}} \tag{47}$$

Thus only κ and PLL loop bandwidth are needed to predict the jitter performance in an oscillator dominated by white noise [32].

Measured 1/f Corner

1/f noise is caused by carrier traps in semiconductors which capture and release carriers randomly. To measure the noise, the input to the system is removed. In the case of a TIA, the input of the circuit is left open to ensure there is no current flow to the amplifier. The device is powered and the noise density is measured with a spectrum analyzer. Figure 62 shows the measured results of 36 TIAs.

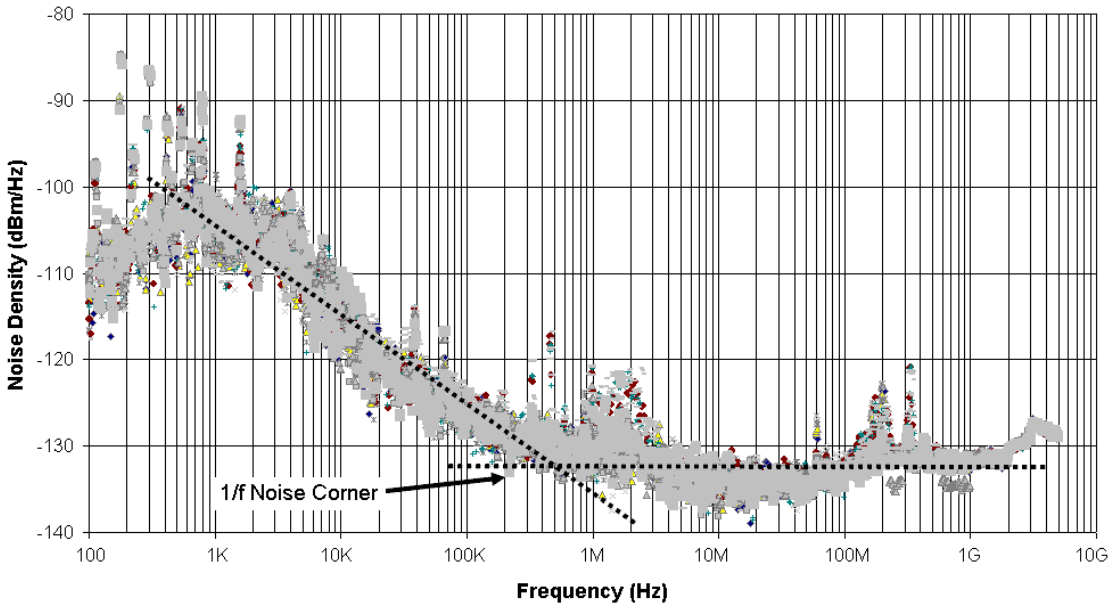

Figure 62: 1/f Noise Measurement of TIAs

The dashed line to the left represents the 1/f fall off rate of -10 dB/decade. The horizontal dashed line represents the noise floor of the analyzer. Although the noise floor of the analyzer prevents the true noise corner to be measured, it is evident that the corner frequency is beyond 500 kHz.

Chapter 7: Conclusions

The design of an Optoelectronic Amplifier has been investigated in this thesis. The front end of the receiver, consisting of the TIA and LA blocks, was designed and simulated to specification.

The Transimpedance Amplifier was designed with a bandwidth of 1.65 GHz in order to maintain a 2.5 Gb/s data rate. Three inverting gain stage topologies were examined as options for the core of the TIA. Only the cascode inverter was able to meet the bandwidth specifications while achieving a transimpedance of 2 kΩ and input referred current noise less than 400 nA_{rms}.

The primary challenge in the design of the Limiting Amplifier was to preserve the high bandwidth at the output of the TIA. The process began with a simple resistive load differential amplifier chain; however, the bandwidth was not achievable with the resistive load LA configuration. The technique of shunt peaking was introduced in the LA design to enhance the bandwidth to 1.8 GHz. Due to the fact that passive inductors are expensive in silicon real-estate, active inductors where used to make the shunt peaking technique feasible.

Offset Feedback, a novel approach of to interface the single-ended output of the TIA with the differential LA inputs, was introduced. The Offset Feedback method allows for the Optoelectronic Amplifier to dynamically change the DC offset of the LA to match the incoming common-mode of the TIA output.

A test chip with the Optoelectronic Amplifier and nine TIA configurations was fabricated. The TIAs varied with three transimpedance gains and the three inverting gain topologies discussed in Chapter 3. Although the operation of the Optoelectronic Amplifier was achieved in simulation, the functionality of the system on the test chip was unconfirmed. The TIA functionality was demonstrated only at low frequencies.

Parasitics related to the ceramic package and the test board layout limited the bandwidth of the chip to 500 MHz.

The test chip was shared between the Optoelectronic Amplifier design and another student's study on jitter in CMOS single-ended ring oscillators and the relationships of the time domain noise figure of merit, kappa, and the major jitter contributors. The relationship requires only κ and the PLL loop bandwidth to predict jitter performance. 1/f noise can be ignored because the 1/f noise corner is assumed to be inside the loop bandwidth frequency. With results measured from the same deep submicron CMOS process, it is evident that the 1/f corner can exceed the PLL loop bandwidth. The added noise causes more jitter than predicted using κ. Although the noise floor of the analyzer prevents the true noise corner to be measured, it is evident that the corner frequency is beyond 500 MHz.

Future Design Considerations

High-speed data transmission requires very wide bandwidths. In the case of this thesis, the required bandwidth was 1.65 GHz. Ceramic leadless chip carriers provide a feasible packaging solution for RF signals with frequencies of 500 MHz or less. RF signals exceeding in the GHz range should designed into smaller packages, such as chip scaled packages (CSP). Unfortunately, CSPs tend to be more expensive. Alternatively, measurements with die probing can be conducted to minimize the effects evident from package parasitics.

Appendix A: Cadence Schematics

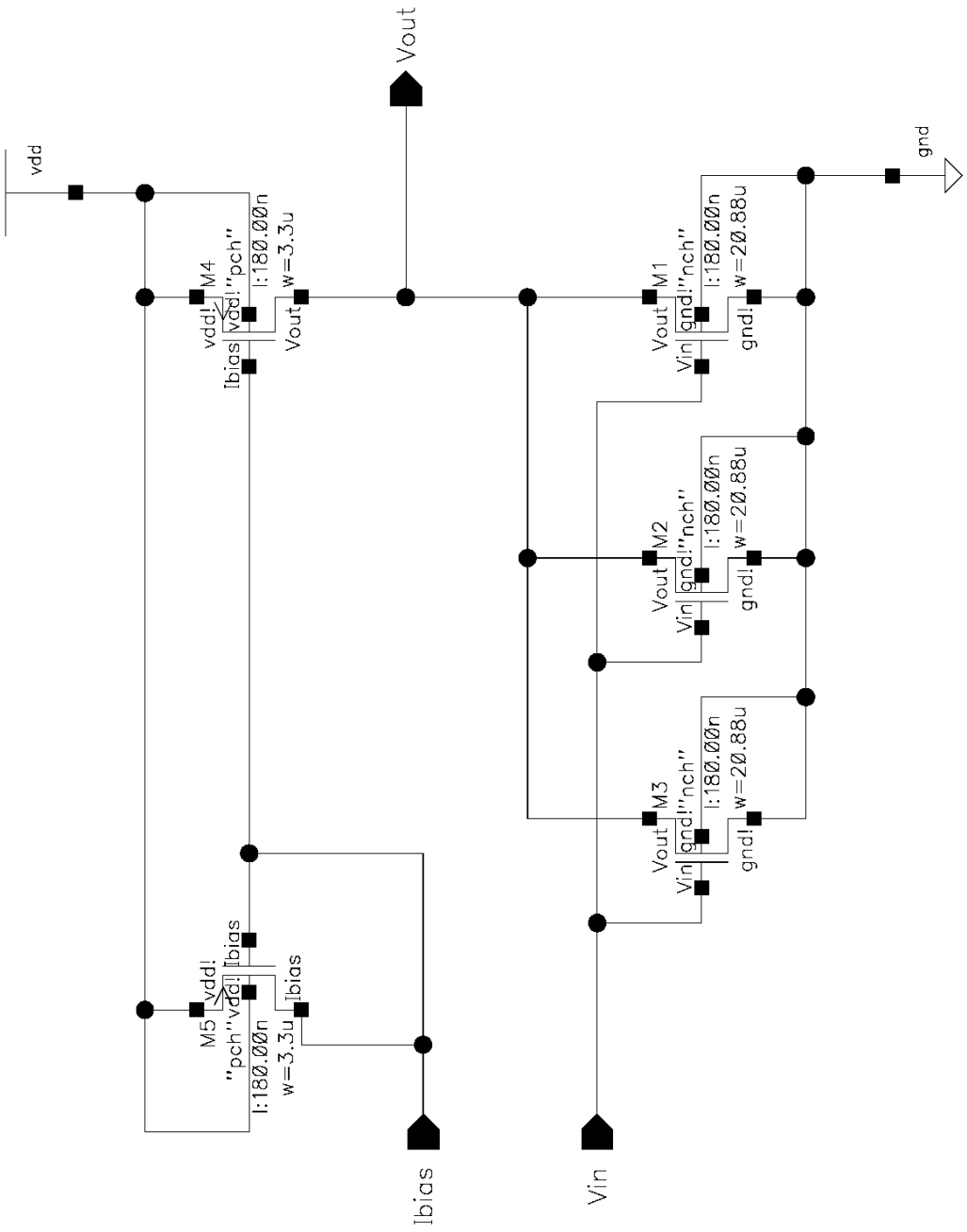

Figure 63: Current Load Inverter Schematic

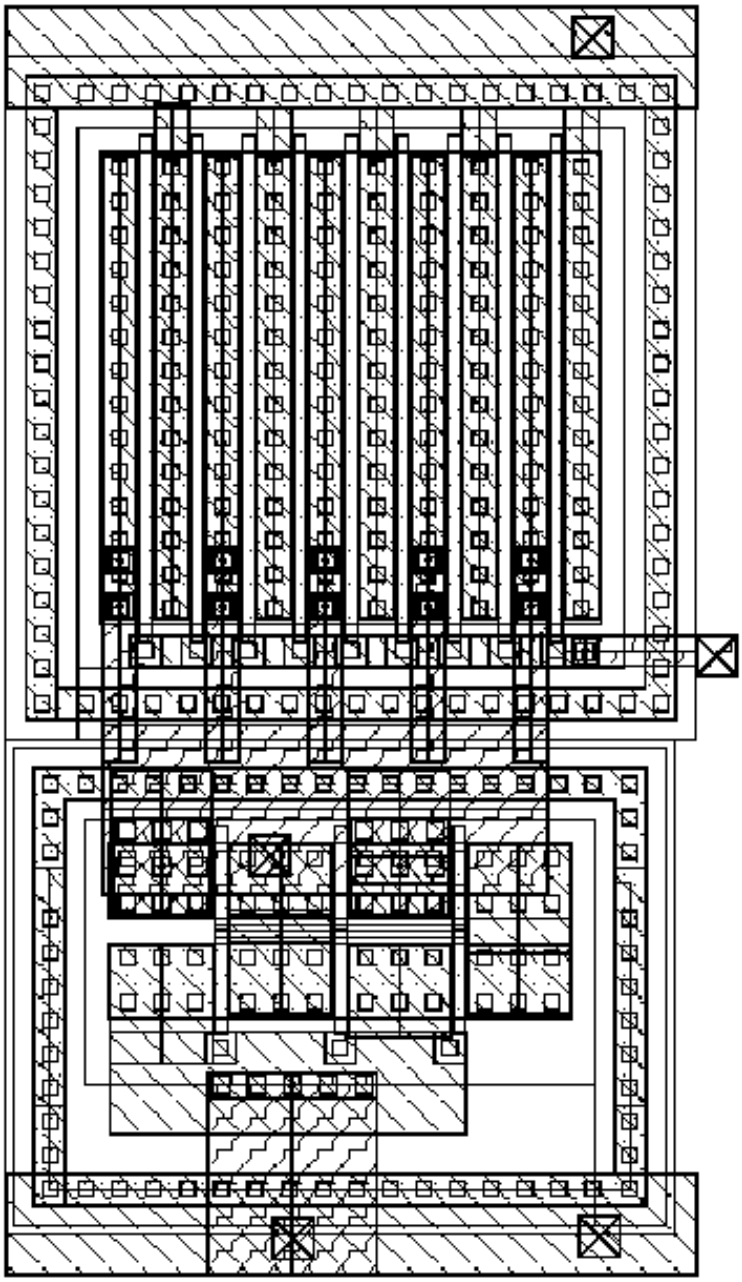

Figure 64: Current Load Inverter Layout

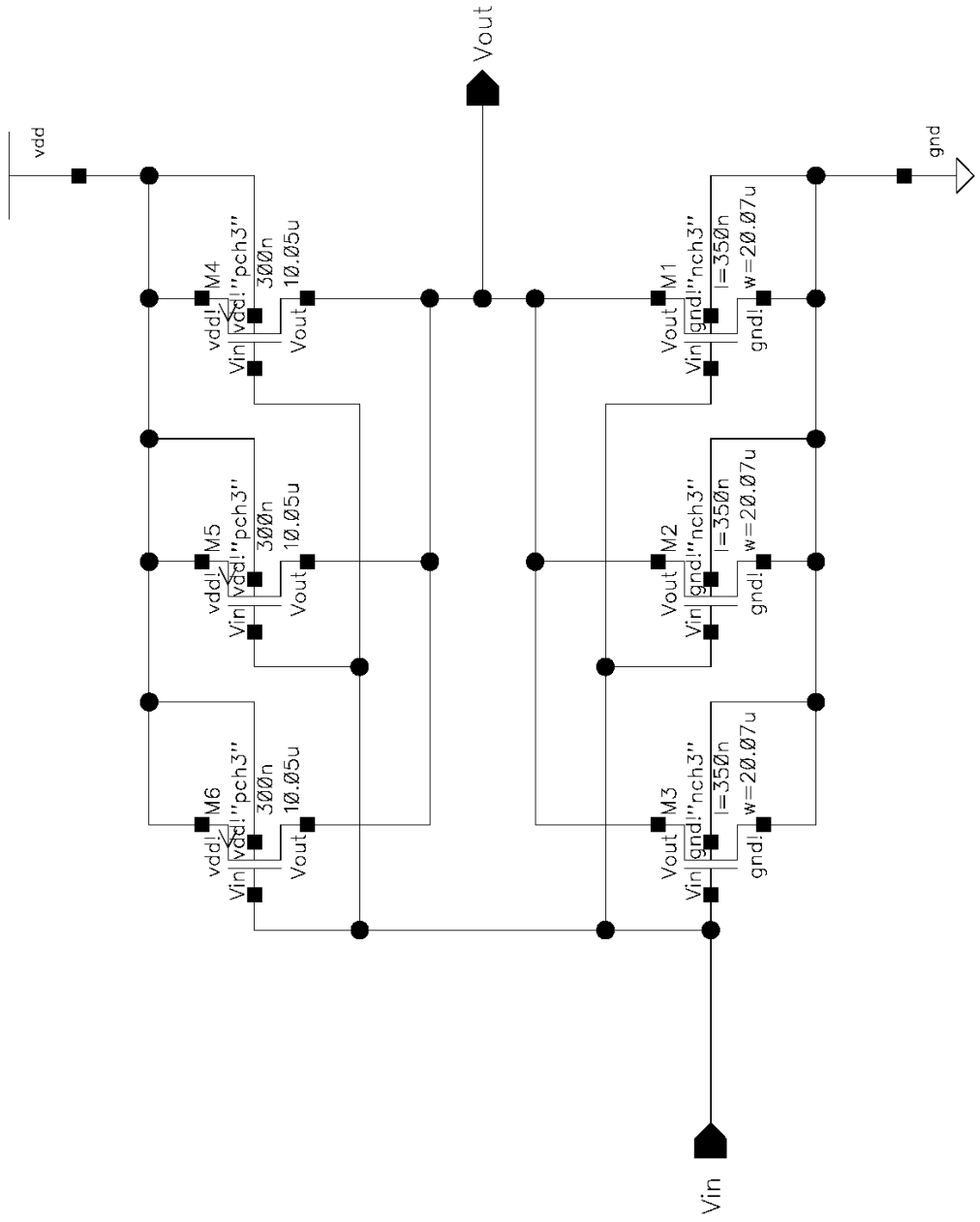

Figure 65: Push-pull Inverter Schematic

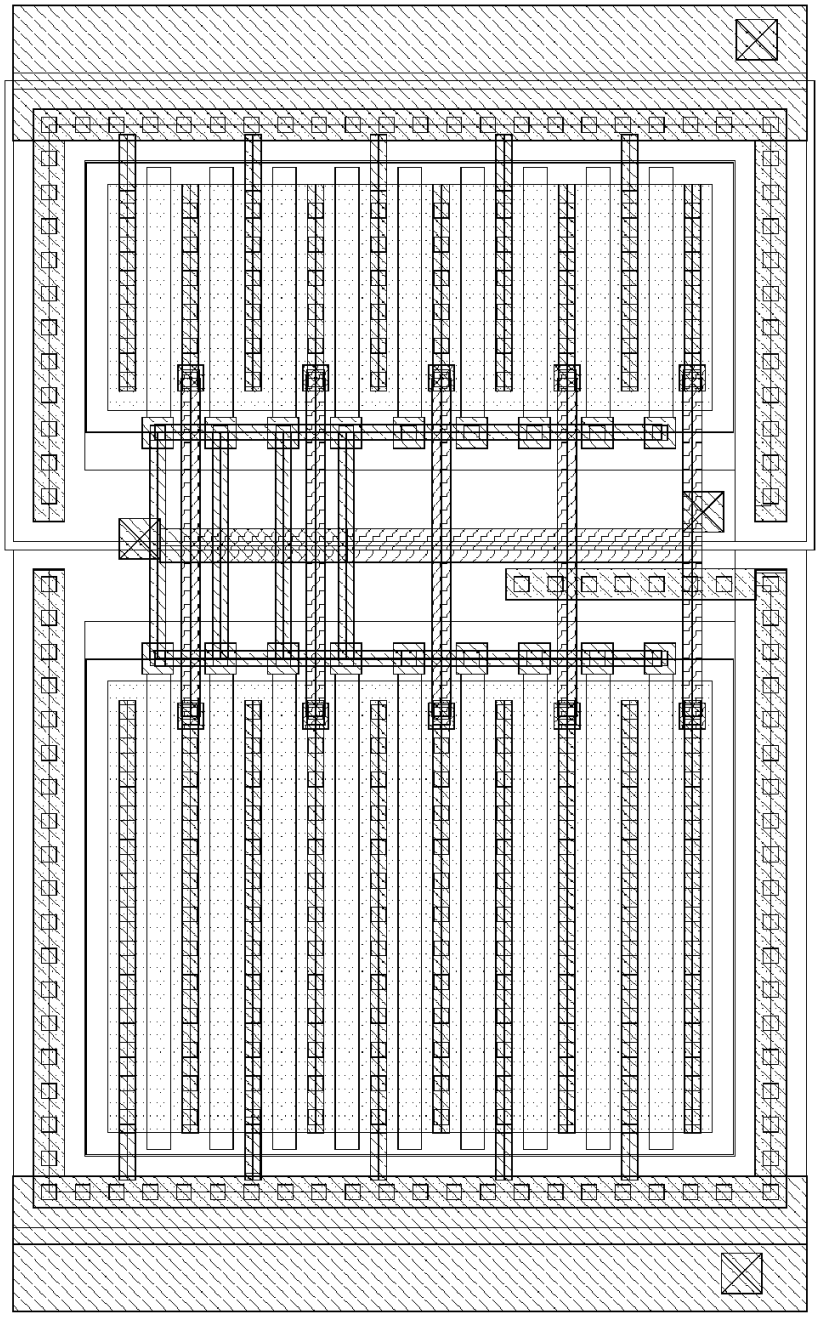

Figure 66: Push-pull Inverter Layout

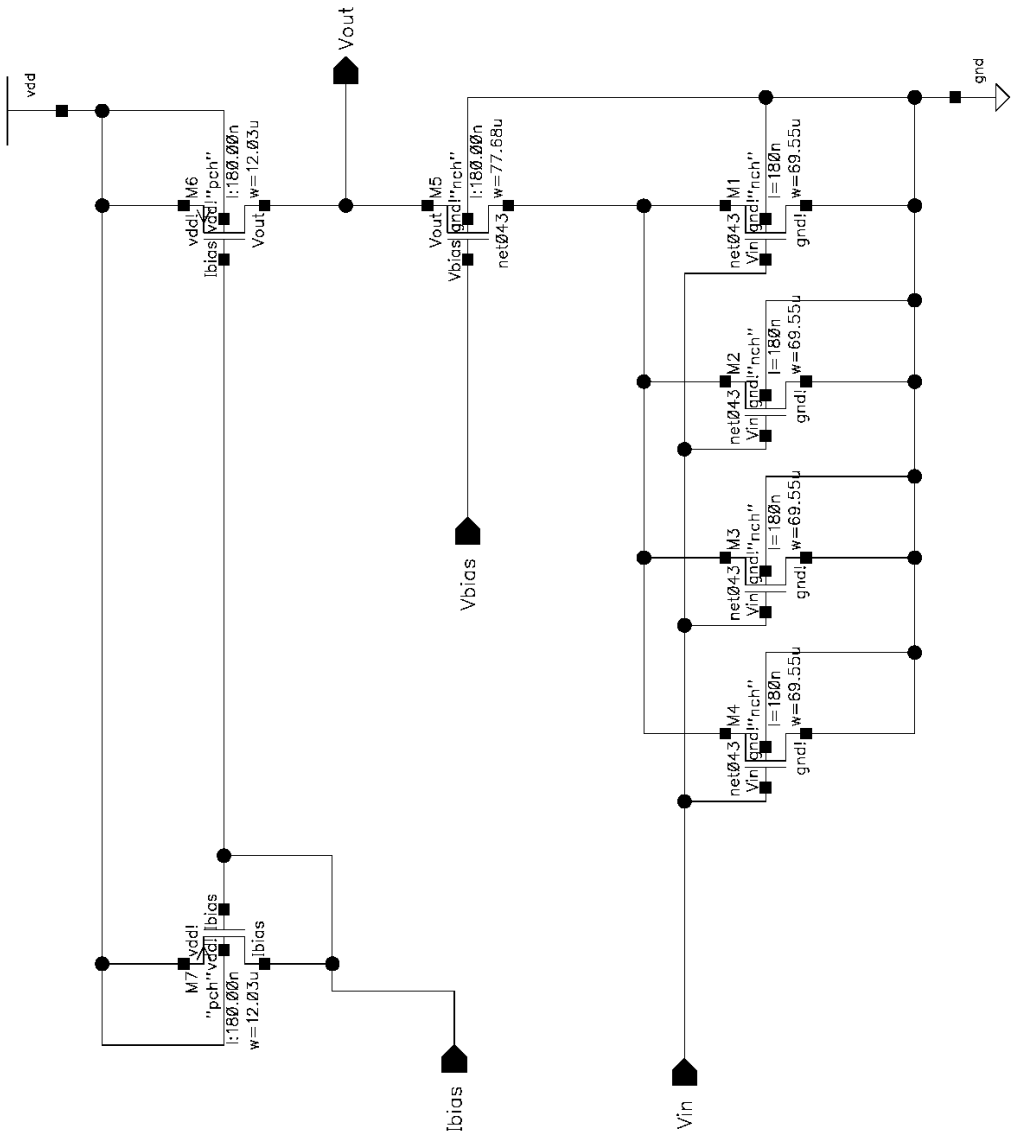

Figure 67: Cascode Inverter Schematic

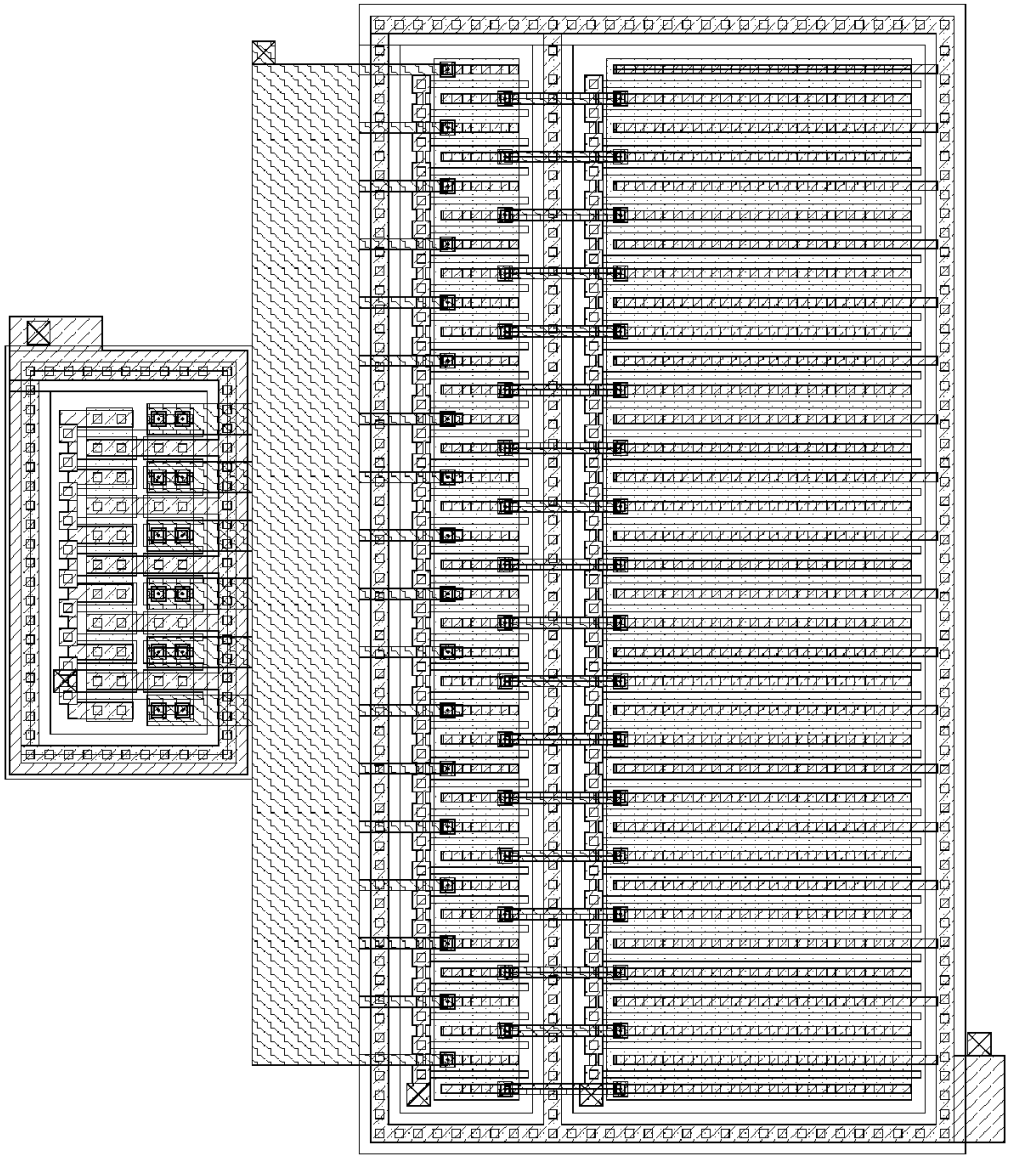

Figure 68: Cascode Inverter Layout

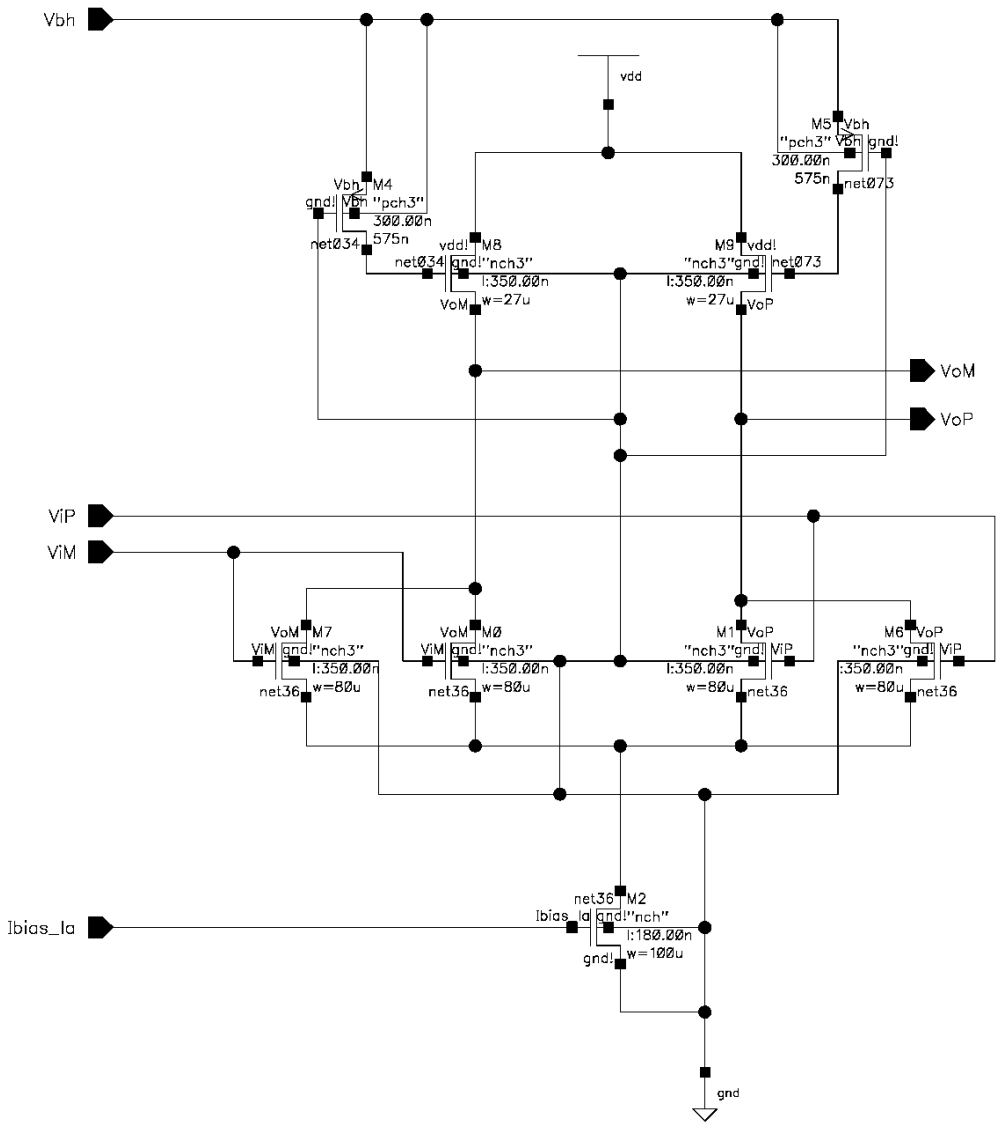

Figure 69: Active Inductor LA Stage Schematic

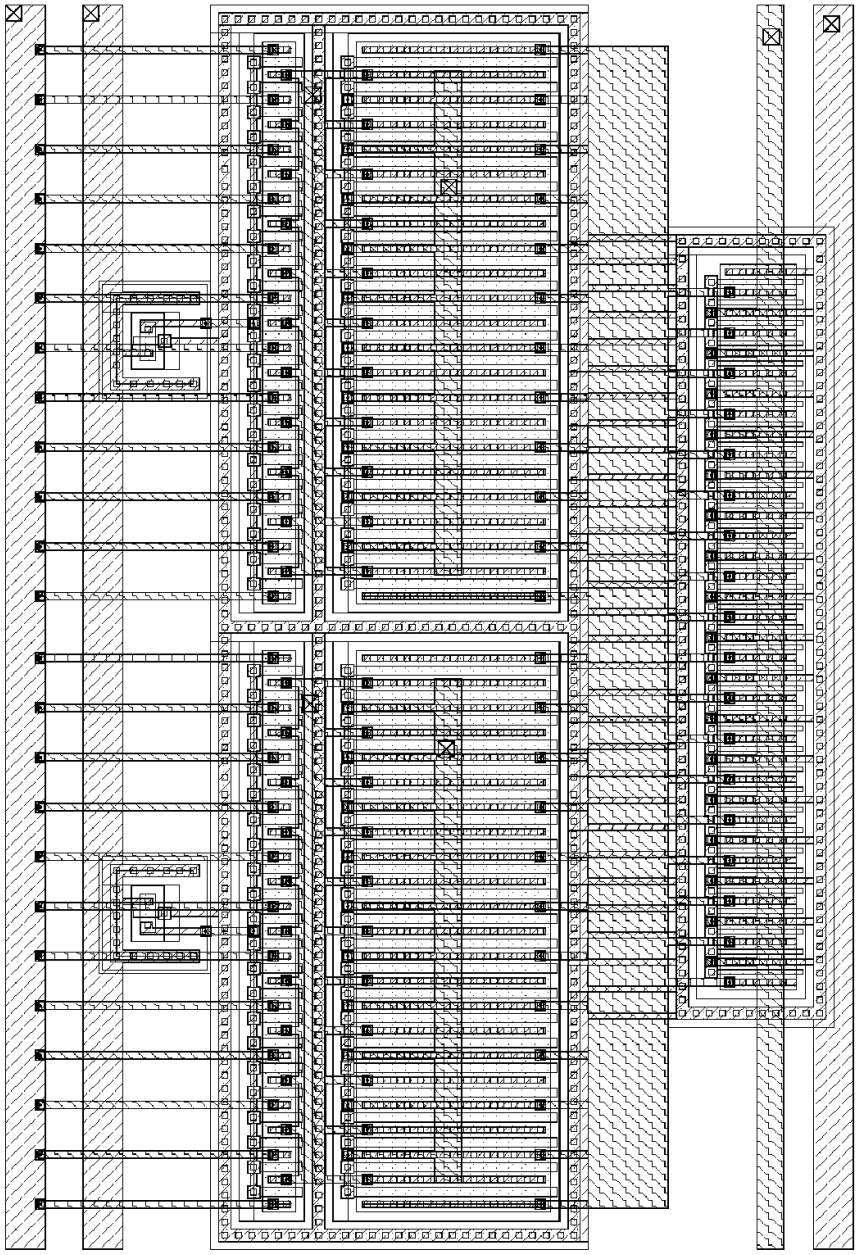

Figure 70: Active Inductor LA Stage Layout

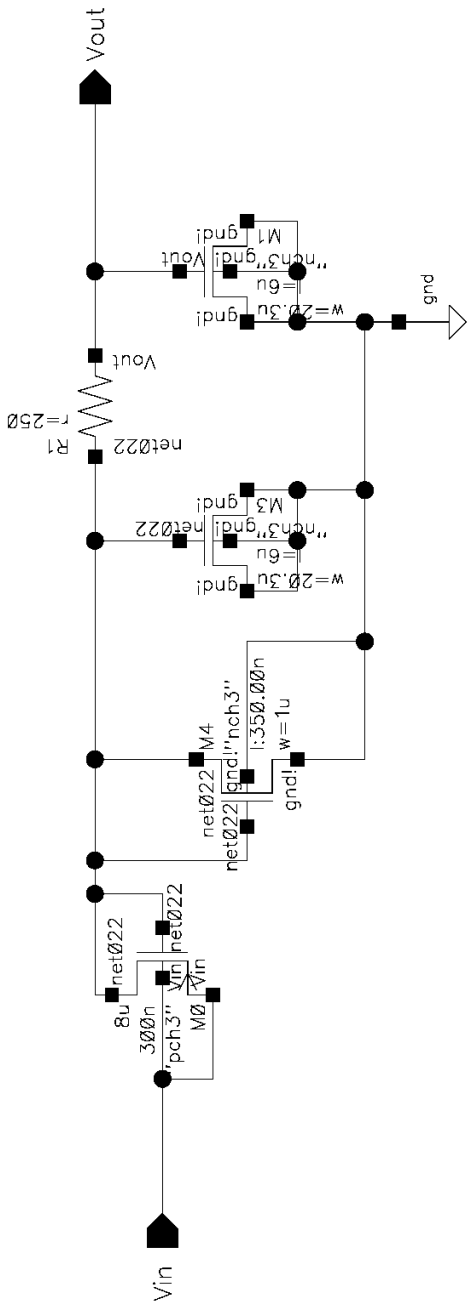

Figure 71: Rectifier Schematic

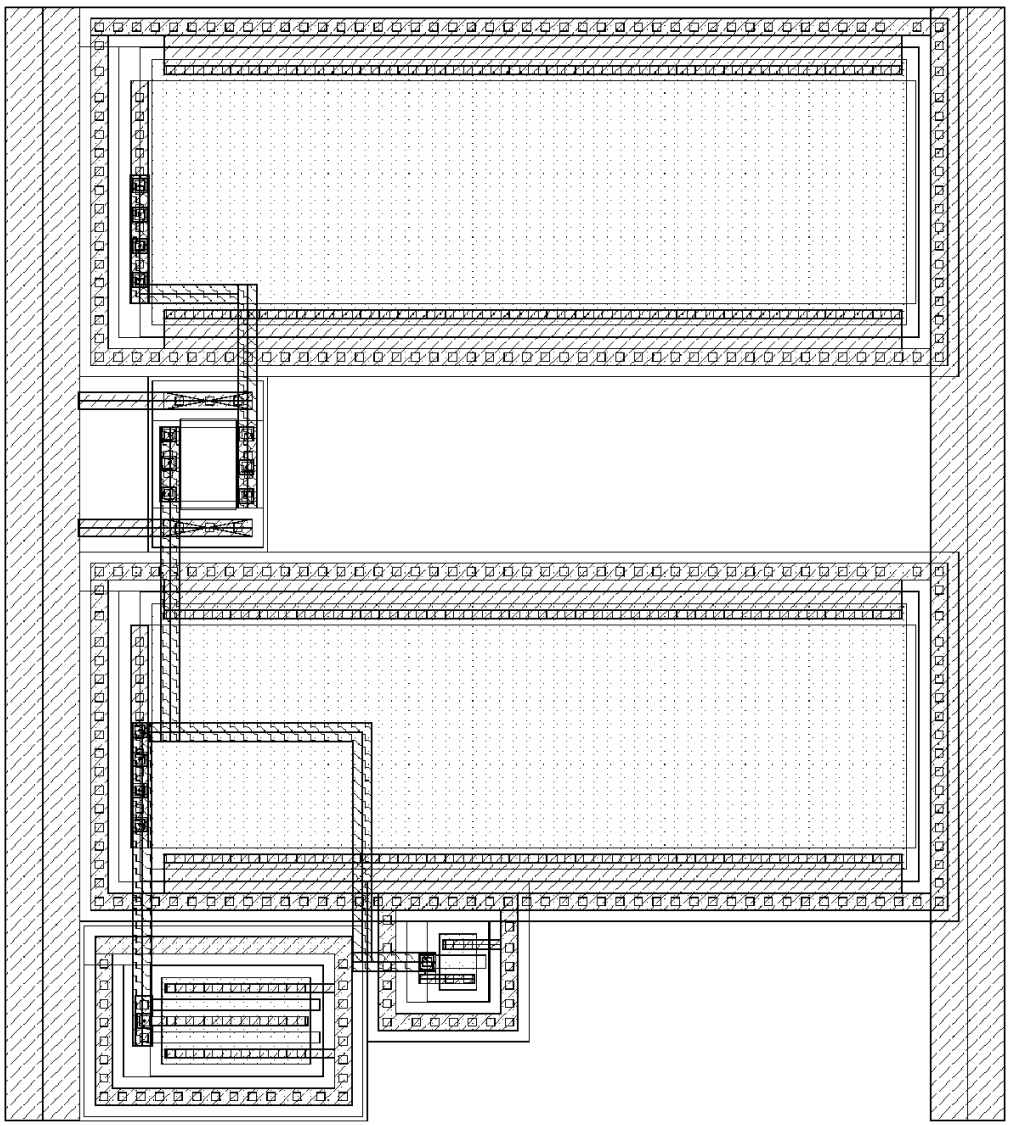

Figure 72: Rectifier Layout

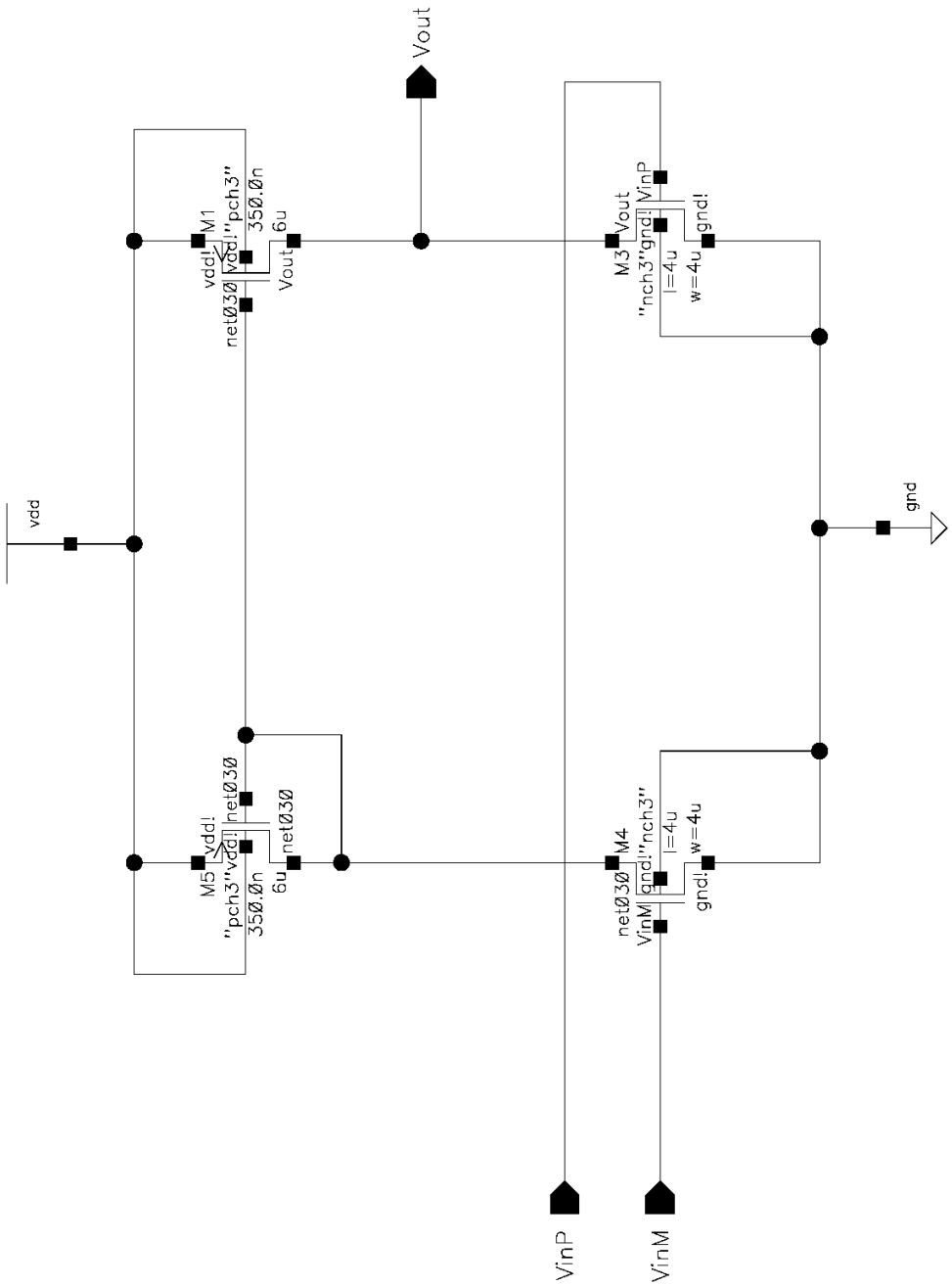

Figure 73: Current Injector Schematic

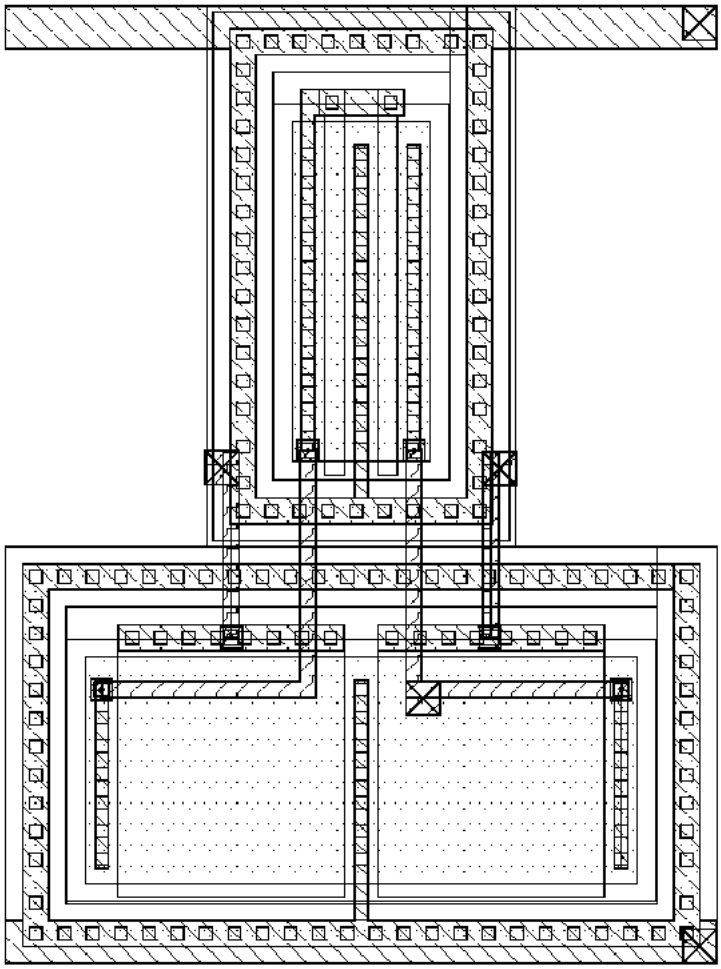

Figure 74: Current Injector Layout

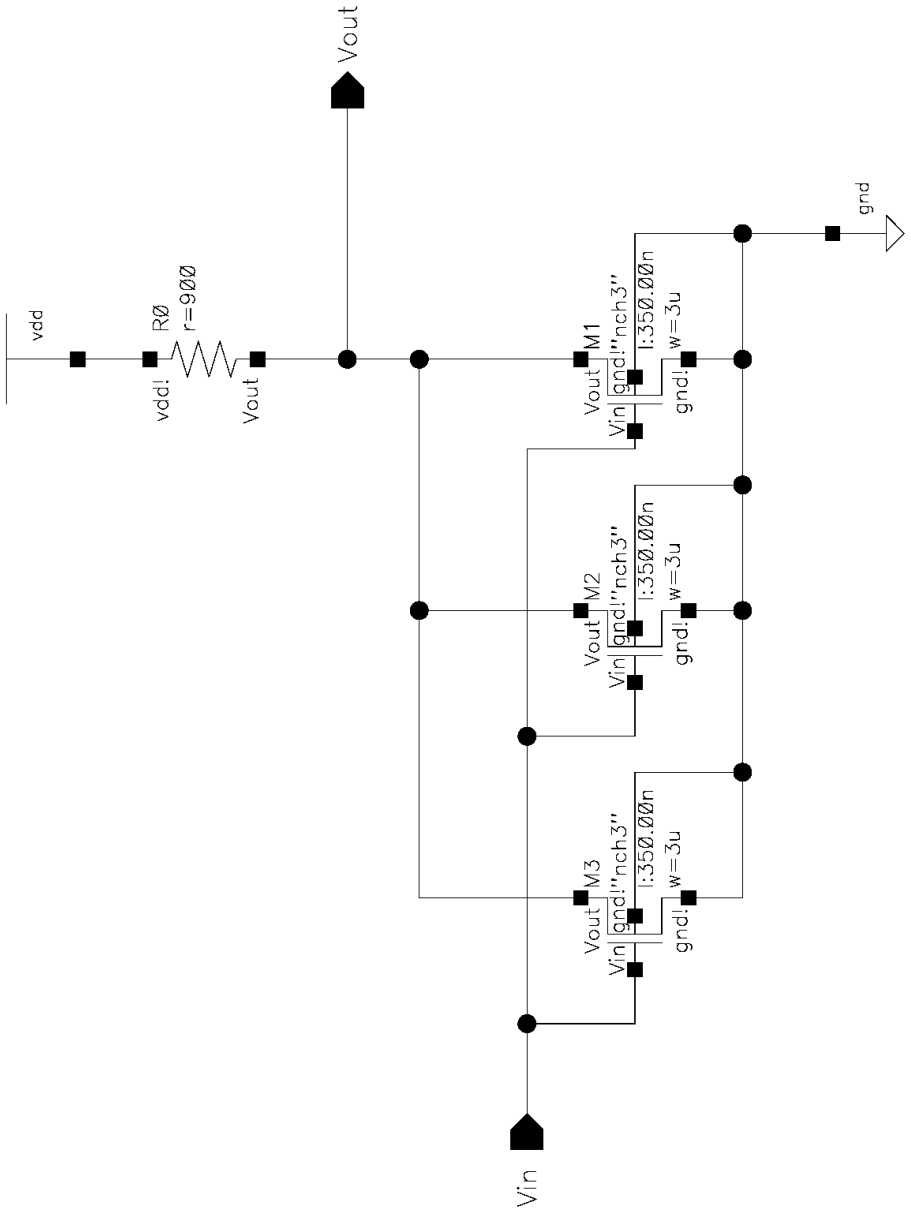

Figure 75: Offset Feedback Buffer Schematic

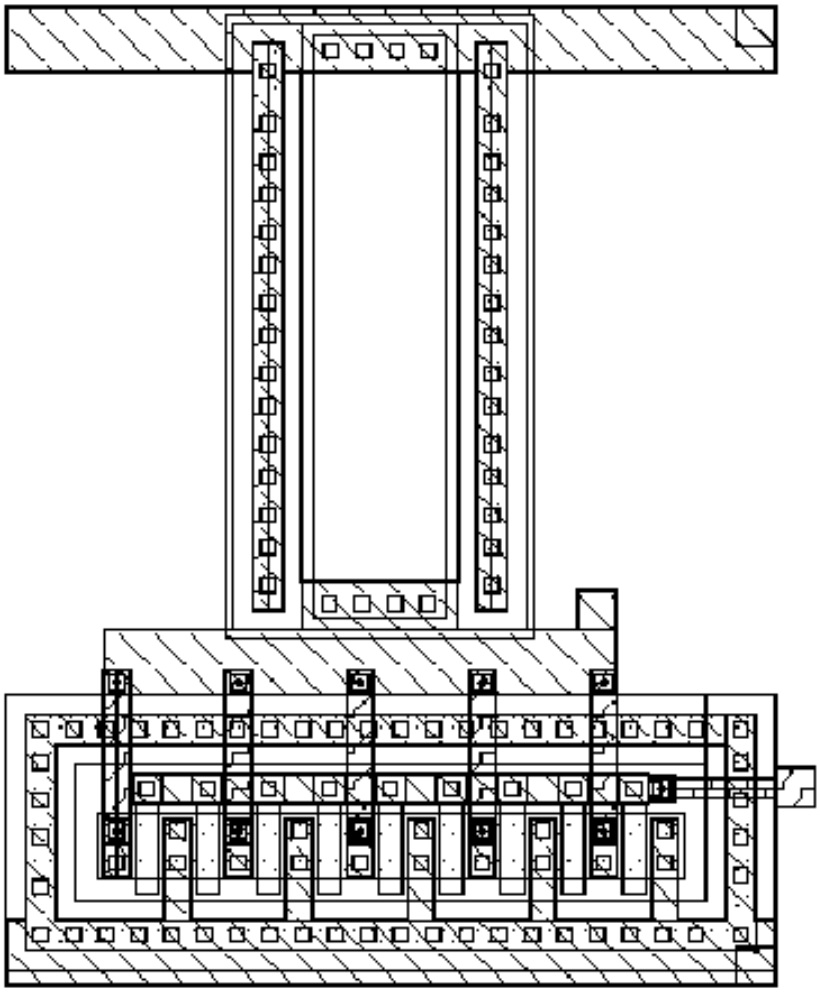

Figure 76: Offset Feedback Buffer Layout

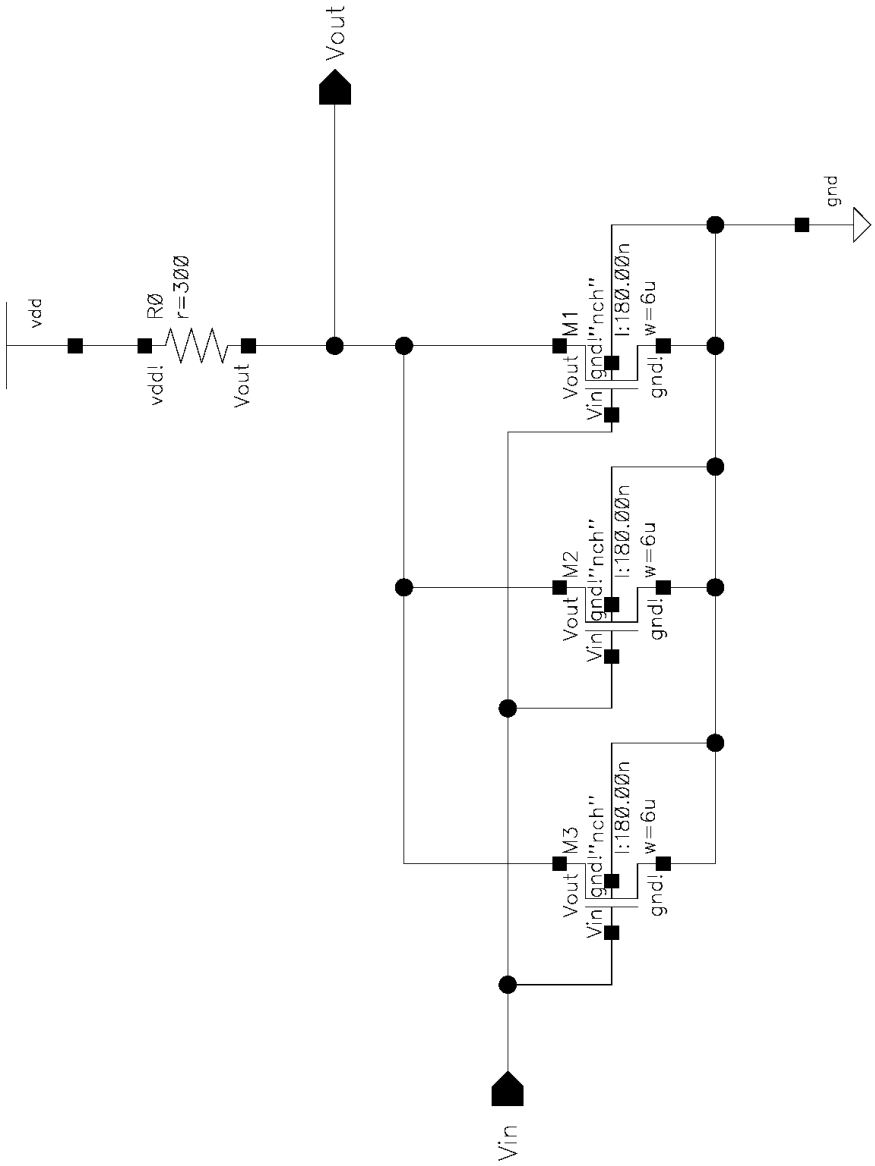

Figure 77: TIA Buffer Schematic

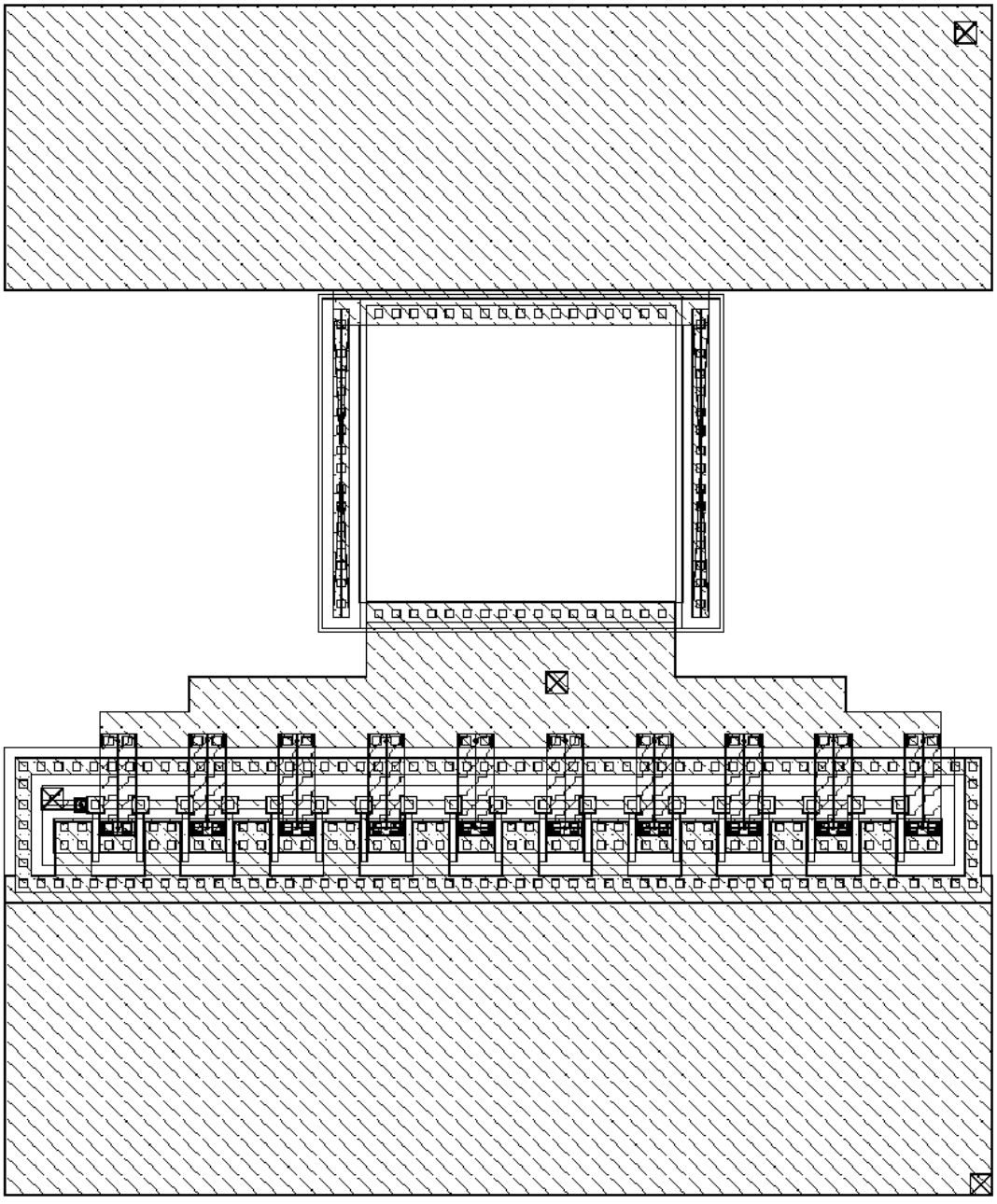

Figure 78: TIA Buffer Layout

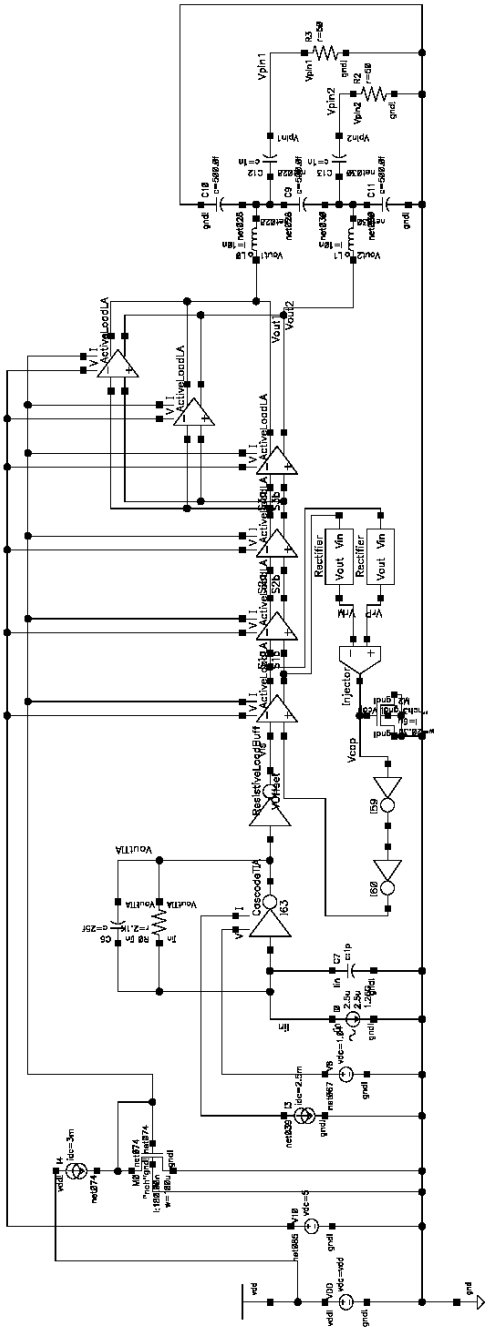

Figure 79: Optoelectronic Amplifier Schematic

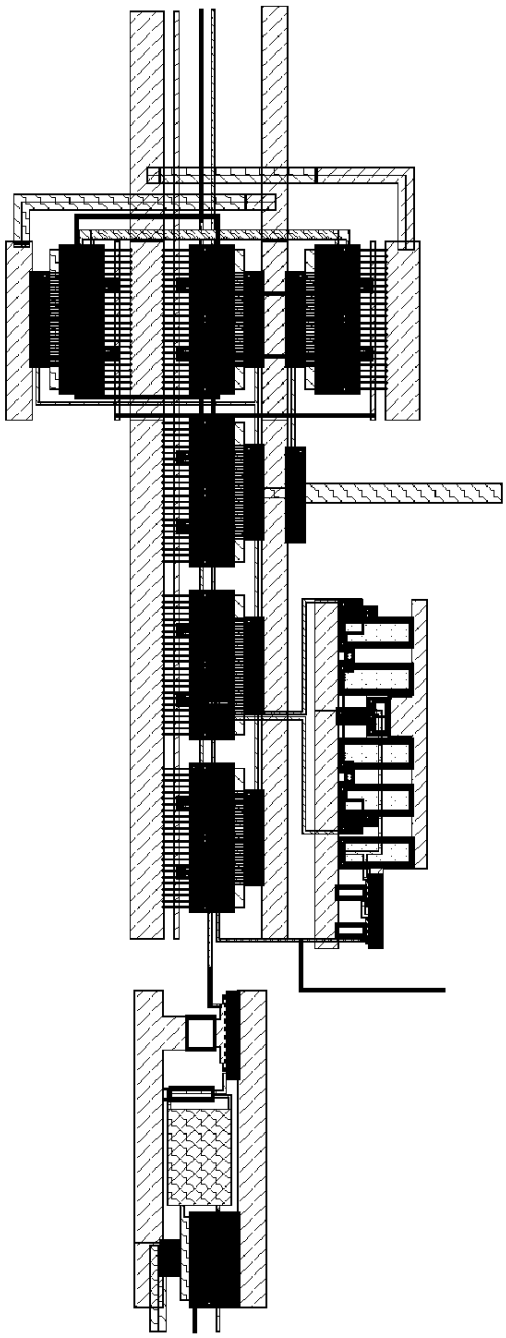

Figure 80: Optoelectronic Amplifier Layout

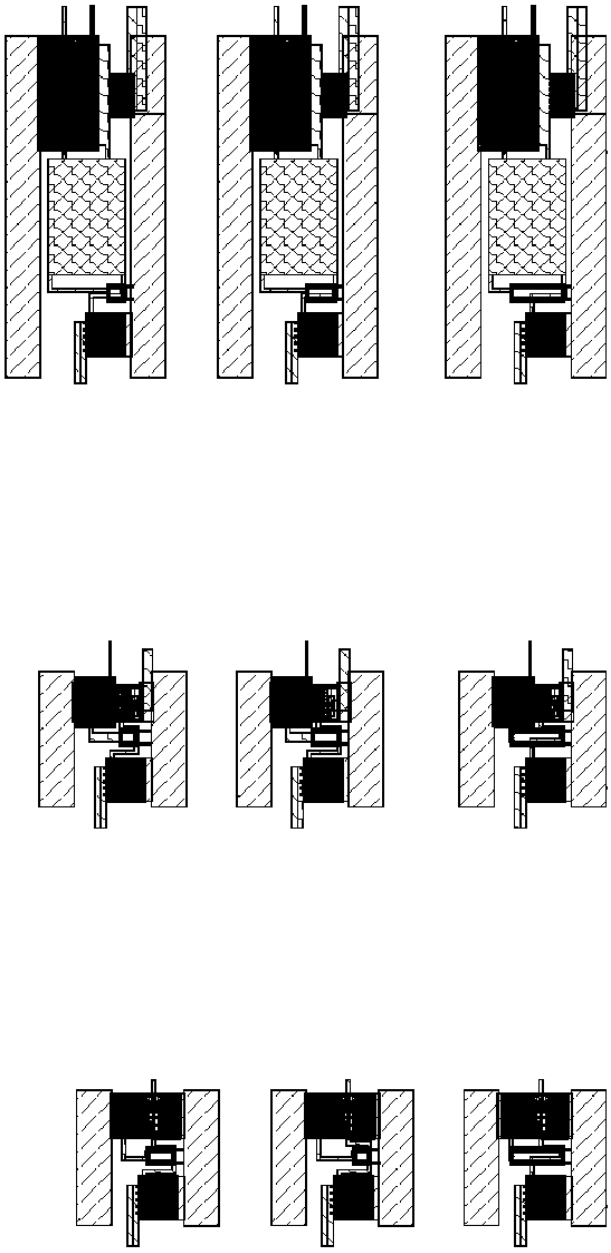

Figure 81: TIA Layouts

Appendix B: Bonding Diagrams

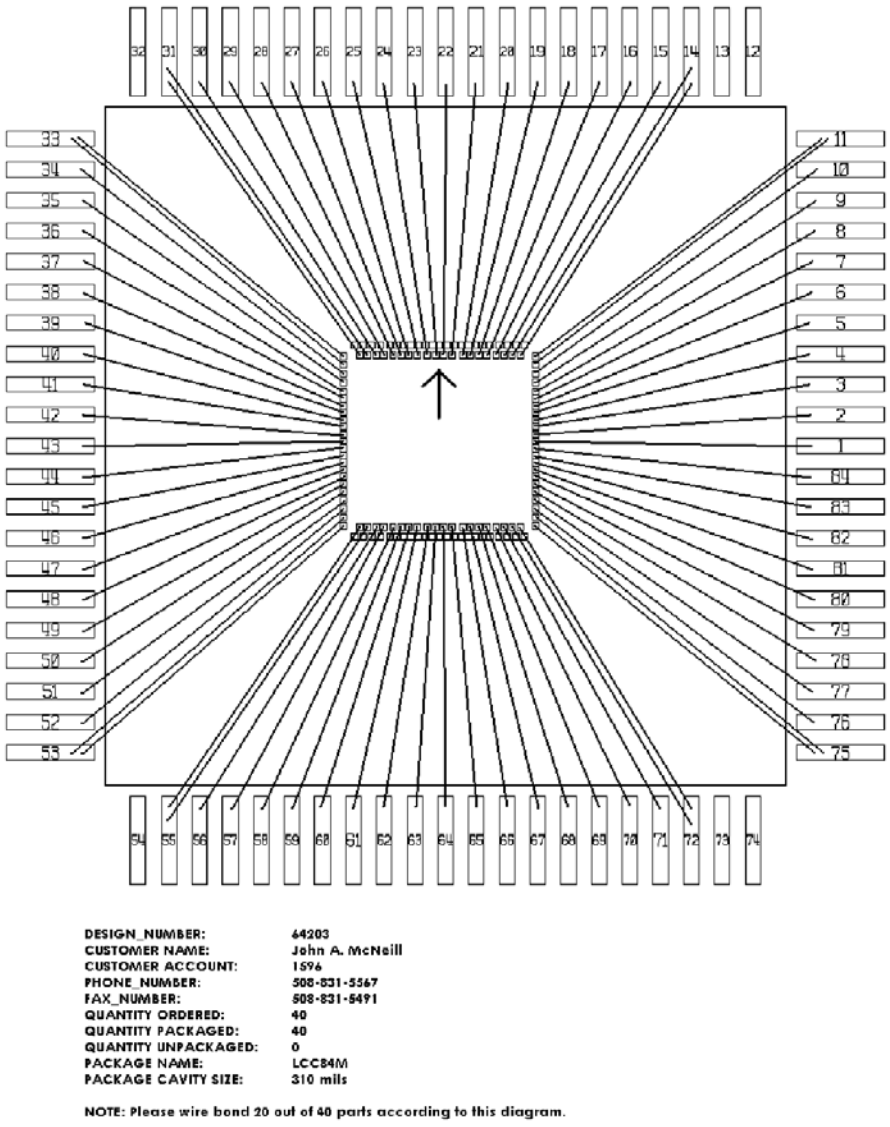

Figure 82: Bonding Diagram of Inner Pad Ring

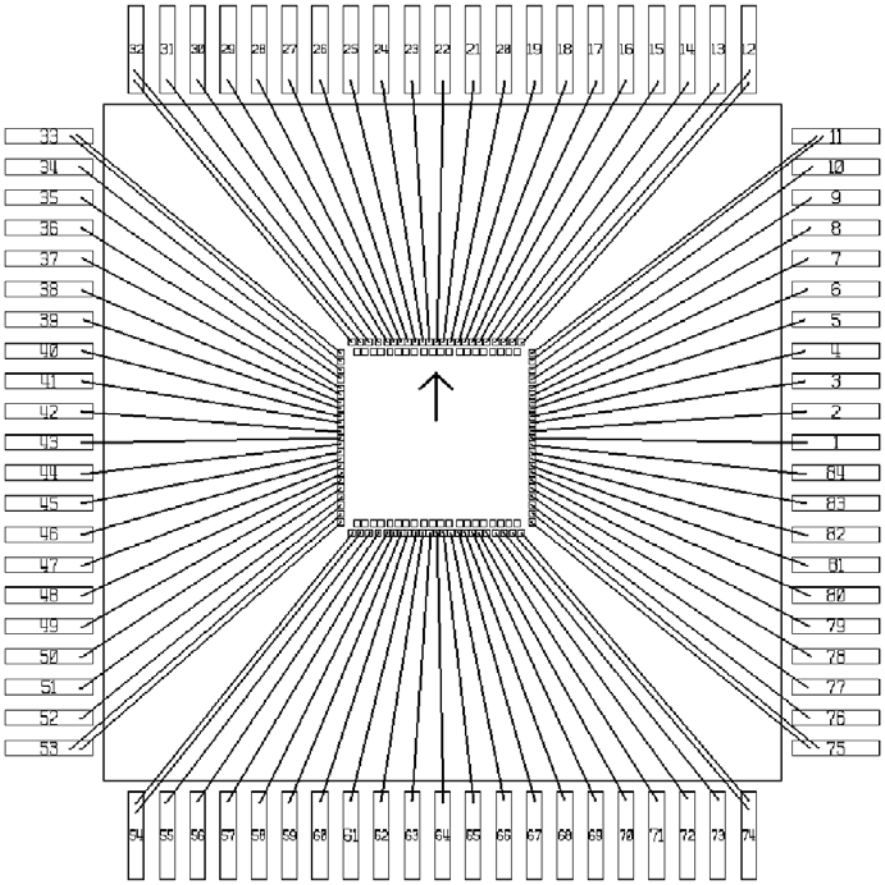

Figure 83: Bonding Diagram of Outer Pad Ring

References

[1] P.E. Allen, D.R. Holberg, CMOS Analog Circuit Design. Orlando, FL: Harcourt Brace Jovanovich College Publishers, 1987.

[2] A. Birbas, D. Triantis, S. Plevridis, E. Tsakas, “Input Capacitance Scaling Related to Short-Channel Noise Phenomena in MOSFET’s,” IEEE Transactions on electronic Devices, vol. 31, “pp. 1091-1099, August 1996.

[3] J. Blyler, "Understanding Optics In A Wireless World," Wireless Systems Design, April 2001.

[4] M. Bollesen, "Industry Insights: Understanding SONET Jitter Specifications," Nikkei Electronics Asia, June 2002.

[5] T.M Frederiksen, Intuitive IC Op Amps. Santa Clara, CA: National Semiconductor Corporation, 1984.

[6] P. Gray, R. Meyer, Analysis and Design of Analog Integrated Circuits, Second Edition: John Wiley & Sons, 1984.

[7] P. Horowitz, W. Hill, The Art of Electronics. Cambridge: Cambridge University Press, 1980.

[8] M. Ingels, G. Van der Plas, J. Crols, M. Steyaert, “A CMOS 18 THzΩ 240 Mb/s Transimpedance Amplifier and 155 Mb/s LED-Driver for Low Cost Optical Fiber Links,” IEEE J. Solid-State Circuits, vol. 29, pp. 1552-1559, Dec. 1994.

[9] M. Ingels, M.S.J. Steyaert, "A 1-Gb/s 0.7μm CMOS Optical Receiver with Full Rail-to-Rail Output Swing," IEEE J. Solid-State Circuits, vol. 34, pp. 971-977, Jul. 1999.

[10] M. Ismail, T. Fiez, "Analog VLSI Signal and Information Processing," McGraw-Hill, Inc., 1994.

[11] A. Jayakumar, M. Bustos, D. Cheskis, S. Pietrucha, M. Bonelli, S. Al-Kuran, N. Scheinberg, " 3-V MSM-TIA for Gigabit Ethernet," IEEE J. Solid-State Circuits, vol. 35, "pp. 1271-1275, September 2000.

[12] D. Johns, K. Martin, "Analog Integrated Circuit Design," John Wiley & Sons, 1997.

[13] W. Kester, S. Wurcer, C. Kitchen, "High Impedance Sensors, Section 5," Analog Devices, 2000.

[14] H. Kim, S. Chandrasekhar, C.A. Burrus, Jr., J. Bauman, "A Si BiCMOS Transimpedance Amplifier for 10Gb/s SONET Receiver," IEEE J. Solid-State Circuits, vol. 36, pp. 769-776, May 2001.

[15] J. Legon, "Scientists: Internet speed record smashed," March 7 2003, CNN.com/Technology, March 2003, http://www.cnn.com/2003/TECH/internet/03/07/speed.record/index.html.

[16] R.G. Meyer, W.D. Mack, "A Wideband Low-Noise Variable-Gain BiCMOS Transimpedance Amplifier," IEEE J. Solid-State Circuits, vol. 29, pp. 701-706, Jun. 1994.

[17] M. Nakamura, Y. Imai, S, Yamahata, Y. Umeda, “Over-30-GHz Limiting Amplifier IC’s with Small Phase Deviation for Optical Communication Systems, IEEE J. Solid-State Circuits, vol. 31, “pp. 1091-1099, August 1996.

[18] Y. Oh, S. Lee, H. Park, "A 2.5Gb/s CMOS Transimpedance Amplifier Using a Novel Active Inductor Load," RF Micro-Electronics Lab, Information and Communications University.

[19] B. Pease, “What’s all this Transimpedance Stuff, Anyhow? (Part 1),” Electronic design, pp. 139-144, January 2001.

[20] D.M. Pietrusynski, J.M Steininger, E.J. Swanson, “A 50-Mbit/s CMOS Monolithic Optical Receiver,” IEEE J. Solid-State Circuits, vol. 23, pp. 1426-1433, Dec. 1988.

[21] B. Razavi, “A 5.2-GHz CMOS Receiver with 62dB Image rejection,” IEEE J. Solid-State Circuits, vol. 36, “pp. 810-815, May 2001.

[22] E. Säckinger, W. Fisher, “A 3-GHz 32-dB CMOS Limiting Amplifier for SONET OC-48 Receivers,” IEEE J. Solid-State Circuits, vol. 35, pp. 1884-1888, Dec. 2000.

[23] J. Savoj, B. Razavi, “A 10-Gb/s CMOS Clock and DATA Recovery Circuit with a Half-Rate Linear Phase Detector,” IEEE J. Solid-State Circuits, vol. 36, “pp. 761-767, May 2001.

[24] A. Sedra, K. Smith, Microelectronic Circuits, Fourth Edition: Oxford University Press, 1988.

[25] W. Tomasi, Advanced Electronic Communication Systems. Upper Saddle River, NJ: Prentice-Hall, 1998.

[26] S. Unlu, “Resonant Cavity Enhanced (RCE) Photonic Devices,” October 7 1995, Boston University, March 2003, http://photon.bu.edu/selim/papers/apr-95/review.html.

[27] T. Vanisri, C.Toumazou, “Integrated High Frequency Low-Noise Current-Mode Optical Transimpedance Preamplifiers: Theory and Practice,” IEEE J. Solid-State Circuits, vol. 30, pp. 677-685, Jun. 1995.

[28] J. Vinogradov, O. Ziemann, E. Bluoss, "Receivers for POF - Solution for Low Noise,” University of Applied Sciences Nuernberg, Slides, San Jose, May 2001.

[29] Vitesse Semiconductor Corp., VSC8122 Multi-Rate SONET/SDH Clock and Data Recovery IC Data Sheet, January 2001.

[30] “Photodiode Basics,” Silicon Sensors, Inc., March 2003 , http://www.siliconsensors.com/PB.html.

[31] K. Lundberg, “Feedback Control Systems for Analog Circuit Design, Version 2.2.2,” Analog Devices and Massachusetts Institute of Technology, Class Notes, February 2003.

[32] C. Liu, J. McNeill, “Jitter in Deep Submicron CMOS Single-Ended Ring Oscillators.”

[33] J. McNeill, “Jitter in ring oscillators”, *IEEE J. Solid-State Circuits*, vol. 32, pp. 870-879, June 1997.

[34] J. McNeill, “A simple method for relating time- and frequency-domain measures of oscillator performance”, 2001 Southwest Symposium on Mixed-Signal Design, pp. 7 -12, 2001.