April 2016

# Nonlinear Load Compensation

Joseph Harry Keogh
*Worcester Polytechnic Institute*

# Nonlinear Load Compensation

---

*Project #:  AAZC*

*Author: Joseph Harry Eisenberg Keogh*

*Advisor: Professor Alexander Emanuel*
*Co-Advisor: Professor Alexander Wyglinski*

---

# Abstract

Nonlinear loads pose significant problems to power engineers, and have proliferated in occurrence over the past few decades. This project seeks to design and simulate a process by which one might mitigate the harmful consequences that result from their usage, employing signals processing techniques, logical decision-making processes, and currently available power electronics hardware.

# Table of Contents

# List of Figures

# List of Tables

## Executive Summary

This project strives to improve power quality in a power distribution network, one user at a time. One measure of the quality of power is the degree to which harmonics are present. As harmonic currents may propagate throughout a network and cause harmful effects at neighboring nodes. [1]

The target behavior of the process designed in this project is to eliminate nonlinear current by superimposing the inverse waveforms of each harmonic into the current being returned to the network from the load. Instead of a physical device, the process was modelled in Simulink. This enabled more-idealized development of the device while maintaining certain physical behaviors modelled to be realistic.

The process proposed within, and implemented in Simulink, involves sampling of the current in, and voltage applied to the load. An H-Bridge configuration of four IGBTs was provided to be used as a power delivery mechanism, switching in different configurations, or states, left to the designer to find and implement, along with a model for a power distribution network paired with a model for a nonlinear load, constructed of ideal current sources. Around these two mechanisms and the provided model for the device's environment, instructions were provided to create a mixed-signal system to counteract all harmonics produced by the load to counteract, or deliver the inverse or 180°-shifted copy of those harmonics (all are equivalent), to prevent their propagation and protect other nodes in the network from absorbing them.

The proposed design has not yet been proven as effective as it should be, but highlights a relatively novel approach due to its foundation in mixed-signal processing. While it likely requires adjustment in the parameters of the physical systems comprising the device, is expected to enjoy the advantages of near-agnosticism relative to the nonlinear load, and its produced harmonics, over many other active processes currently existing. With relation to passive equivalents, such as RLC filters, power-loss is less

extreme, and the as impedance is variable with respect to voltage, is less vulnerable to issues of resonance.

# 1 Introduction

In recent decades, new nonlinear loads in power delivery networks have proliferated at a rapid rate, where they used to be primarily found in heavy requirement and industrial settings. Nonlinear loads are those whose power requirements or characteristics vary with time, or those that exhibit impedances that are non-constant with regard to applied voltage. They have become ubiquitous within modern life, and the average user of power networks likely has numerous devices that, in various contexts, serve as nonlinear loads.

Linear components include, primarily, resistances, capacitances, and inductances. But the defining circuit elements of electronics, in both consumer devices, and others, are now semiconducting components such as diodes and transistors which enable digital technology. As this report is being written, in addition to many other relevant devices, the author has both a laptop computer and a smart-phone charging on this very desk, which make extensive use of semiconductor switching technology. With the direct-current charging requirements for these devices, power must be supplied by a rectifier circuit, which also exhibits nonlinear voltage-current characteristics.

The trend towards semiconductor switching and digital technologies shares the responsibility for increase in harmonic generation in power networks with other phenomena such as the move to clean energy sources, which can also introduce a need for harmonic compensation. Connection of photovoltaic power production often requires DC-AC inverters. Harmonic currents generated by nonlinear loads can cause losses in devices that utilize ferromagnetic cores or electromagnetic induction to store or transfer energy, such as inductors, transformers and generators [2] [3].

Magnetic-core devices and impedance of conductors, due to the skin effect[1] suffer greater consequences of harmonic power, the primary culprits are rectifier loads whose leads are crossed with smoothing pulse. AC-to-DC charging devices now frequently include power electronic elements drawing directly from the network, like the common SMPS[2], like that in Figure 1. [4] [5]

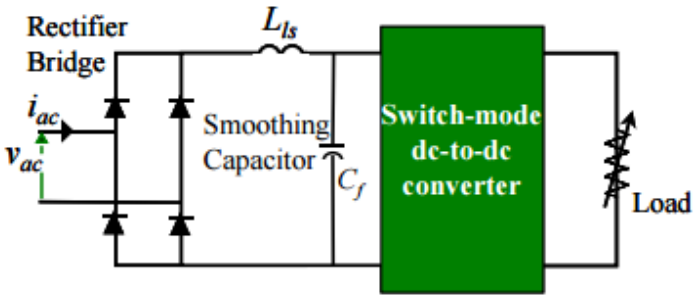


*Figure 1: SMPS Nonlinear Load [4]*

The smoothing capacitor exacerbates the situation. It stores energy to smooth the transition between half-waves, usually meaning at least two charge-discharge cycles per period of the fundamental frequency. During the charging portion of the cycle, the SMPS absorbs some current to charge the capacitor for shorter an interval than the period of the waveform. This misshapes the waveform, imposing current dips when the capacitor charges. As these dips occur periodically, and at a frequency exceeding that of the network, they may be represented as a higher frequency waveform superimposed on the pure alternating current signal. [4] [6]

[1] The phenomenon of increased current density towards the outer boundaries of the conductor, packing greater like-charge density into a narrower cross-section, increasing power losses and thus impedance.
[2] Switch-Mode Power Supply

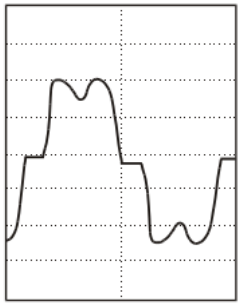

*Figure 2: Example Current Waveform for a 6-Pulse Rectifier [7]*

This work is intended to provide a method by which the harmful effects of nonlinear loads in such a network may be corrected on the user-side. This is beneficial, not to just the power companies who might suffer efficiency problems as a result, and not just to neighboring users who may suffer issues rooted in the concept of resonance at certain current frequencies, but the users themselves, who might responsibly compensate for their own nonlinear loads or reintroduction of power back into the grid.

Other models attempting active-compensation in single-phase power distribution networks do exist, but for the most part appear to differ from the proposed implementation in a few key details. These details vary from system-to-system, they are not static industry-wide, suggesting a dynamic area of the field, still being explored, and with much room for experimentation with new approaches.

Instead of compensation at the load's connections, one model targets a centralized-node. The bridge-converter, operated in a "Sliding-Mode" control pattern, similar to that used in the design produced by this project. Applicable transistor gate impulses are given as the result of a logical determination, which follows the sensed current and voltage signals, presented in Table 1 far more eloquently than was achieved within this document, but presented in a manner stipulated on exclusion of certain circuit states not occurring naturally within the network. Further key differences include a

pulse-width modulation pattern driving the active gates. The duty-cycle is the result of a calculation involving attributes of physical components, namely a supply capacitor (implemented as a DC voltage supply in this design) and a lowpass RL filter, or rather just an inductor, to smooth sharp transitions and extend their transition times. [8]

| | $i_s < kv_s$ | $i_s > kv_s$ |
|---|---|---|
| $u_1$ | 0 | 1 |
| $u_2$ | 1 | 0 |

| | $v_s < 0$ | $v_s > 0$ |
|---|---|---|
| $u_3$ | 1 | 0 |
| $u_4$ | 0 | 1 |

*Table 1 : Sliding Rules for Active Gate Impulse Dependency on Network Power States [8]*

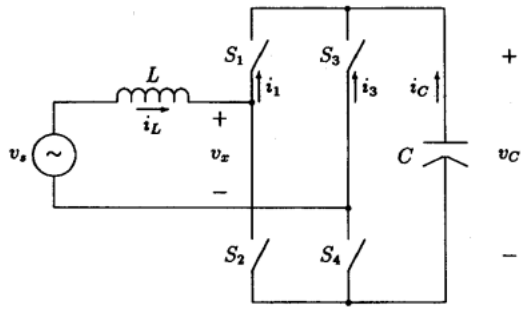


*Figure 3: Single-Phase Inverter Implementation of Compensator, Applied at a Central Node [8]*

Another model, using a single-phase IGBT bridge converter, prefers a more signals theory based approach, and successfully implements an approach towards nonlinear current separation once attempted in this project due to the utter-lack of phase effects involved. By reconstructing a waveform representation of the fundamental frequency component of the signal, this waveform might be subtracted from the network's electrical current signal, and effective isolate the nonlinearities with zero phase-shift and unity gain at other frequencies. This well-obtained current is however also delivered with a PWM pattern, with a duty cycle determined by a PI controller. [9]

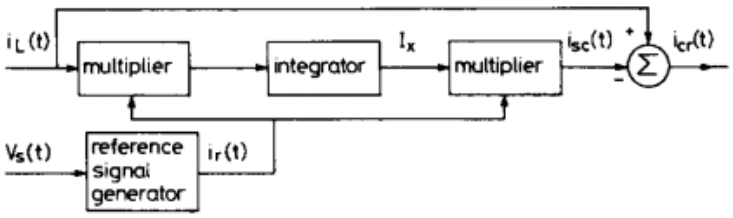


*Figure 4: Compensator's Fundamental Frequency Reconstruction Diagram Using Power Calculations and Energy Detection [9]*

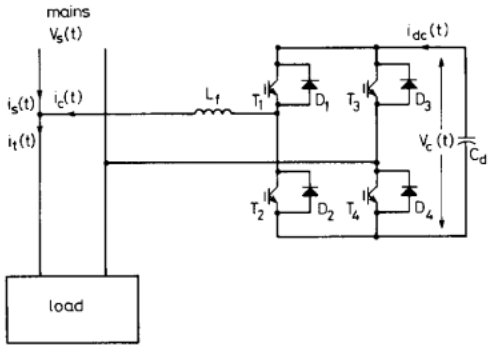


*Figure 5:Power Circuit Shown with Waveform Reconstruction Compensator [9]*

## 1.1 Proposed Solutions

The proposed solution may be broken down into three major components: Analog Pre-Processing, the Digital Processing and Controls Unit, and the Power Delivery System. The Analog Pre-Processing Unit exists to provide the Digital Processing and Controls with information on the relevant information regarding the network's operation at a given moment. The Digital Processing and Controls Unit is included to take the information from Analog Pre-Processing, separate desired behaviors from undesired behaviors, and turn these into the controlling impulses for operation of the Power Delivery Unit. The Power Delivery Unit takes these firing impulses, and from them delivers the power necessary to correct network behaviors.

### 1.1.1 Analog Pre-Processing

Given that the yield of this project is intended as a supporting simulation, this unit has been paid the least attention. Simulation software provides the means with which to work around this unit's necessity, and the absence of physical reality in this instance has very limited consequence to the process as a whole.

If simplified, more abstract, means for this functionality exists in simulation, full-advantage was to be taken until the process itself could be refined. With use of the Simscape Power Systems library, which possesses its own current measurement block, design of these components proved unnecessary.

Refined, more realistic implementation, is intended to have two primary processes involved. First, some indication of the current being fed between the greater network and the load must be obtained. This is done, first, through a current transformer. Current transformers obtain the current metric through electromagnetic induction, with a strong inverse-gain. As they are not connected in-line, they are essentially lossless. [1011]

As the output of the current transformer which encapsulates the desired information is a current and not a voltage, yet information may only be captured for digital processing purposes as a voltage, a component is required to transform this current into a voltage. This component is a current-sense amplifier. If the first stage of Analog Pre-Processing exhibits behaviors of a current-source, the voltage across a conductor of known resistance is going to be proportional to the currents produced by the network and nonlinear load. Thus a difference amplifier connected across a known resistance helps accurately and safely transform this current signal into a voltage that may be sampled by an Analog-to-Digital Converter.

Sampling Theory mandates that amplitude is not the only variable important in moving a waveform into the digital domain. Frequency is critical to the process as well, and for accurate control,

the signal must be effectively band-limited to half of the sampling rate. In other terms, the largest frequency to be sampled must be half of the frequency at which the ADC captures samples. If, at installation, one cannot ensure that the highest persistent frequency present does not meet these constraints, a lowpass filter must be installed. It is recommended that such a filter be active, as opposed to passive, to mitigate loss in a low-power environment. It is critical that the phase-response of this filter be easily modelled or approximated, and that the group delay of the filter be small for precise, accurate, and rapidly responding compensation. To this end, a low-order Bessel filter is recommended due to its maximally flat phase-response.

### 1.1.2 Digital Processing and Control

This is the most complicated and sensitive unit in the design. Requirements for its operation dictate that the firing impulse outputs accurately reflect the relevant information in the input waveform, with limited delay. As a result, preservation and protection of phase information are an enormous concern, as the potential exists for the waveform to be significantly reshaped in the midst of phase-affective processes.

The first stage in any digital unit that makes decisions based on real-world continuous information must always be sampling, the collection of this data. Done via an Analog-to-Digital Converter (ADC), this captures values of the waveform at fixed-interval time instances at a pace called the *sampling rate*. It is theoretically possible to sample a waveform, under certain conditions, so that it can be perfectly reconstructed. These conditions, outlined in the Sampling Theory section, dictate that the sampling rate must be at least twice the maximum-supported frequency, and that no higher frequencies should exist, in significant quantities, above this.

The next step in solving this problem is waveform isolation, achieved by isolating the nonlinear current. This can be done subtractively, if the amplitude and phase of the network's nominal-frequency

current are expected to be constant, where a fixed sinusoidal waveform is used as a reference to be subtracted from the read current. If variations are expected, and very narrow bandpass filter with equalization for the group delay can be implemented. This has the benefit of a narrow phase distortion at frequencies intended for elimination anyways, and a less generalized phase-correction technique. Alternatively, if a sufficiently narrow phase response can be achieved in a notch filter, this can be exploited to remove the nominal frequency, and isolate the elements introduced by the nonlinear load, although one must pay careful attention to the phase response to be sure that phase-distortion is not reshaping the wave to any significant degree.

As filters exhibit transient responses, one must be careful to ensure that one is not injecting transient information into the feedback loop. Testing has shown that memory of the 60Hz signal can be retained in the filter and feedback loop, when operating in transience, in such a manner that the device never ceases to attempt to compensate not just for nonlinear patterns, but for the nominal-frequency as well. Proposed solutions for this include a “flush-state” break in the loop, where compensation is idled while the transient information is flushed out of the system. This would be implemented as an energy detector, placed after waveform isolation, that would assess the presence of the nominal frequency in the output signal, and disconnect compensation until this presence is reduced to tolerably low levels.

The second to last block is the “decision engine” where all determinations regarding the state of the Power Delivery apparatus are performed. Numerous such states must exist in order to achieve practically lossless compensation to a high degree of precision. Such a block must make such decisions off of a number of indicators including voltage in the grid (if it is in the wrong direction, current may be delivered in the wrong direction as well), and the current it intends to deliver. Furthermore, due to the highly sensitive and transient nature of the Power Delivery apparatus, to be seen, requires a greater

real-time determination to determine if the bounds have been surpassed, upon which it must idle the compensator.

Finally, once the decisions have been determined, the final block is the “gate-firing unit”, which from each state-decision, generates a series of firing impulses that will control the physical Power Delivery unit.

### 1.1.3 Power Delivery

As the ability to drive negative and positive current to the grid are essential for the application, an H-Bridge configuration seems an obvious choice. This portion of the document cannot effectively address the operation of this solution sufficiently considering the uncommon states with which the H-bridge is to be driven, these methods are addressed in the Background Information chapter.

Several useful states have been identified, including one that connects a power supply in the same direction as the grid’s reference polarity “push +”, in the opposite direction “push –“, and one in which no power is delivered or sunk, “idle”. The novel implementation in this design are the identification of two bridge configurations each, for two rarely seen actions. Each action is a polarity-sensitive short-circuit, where direct passage of current from the power rail of the network, to ground, are enabled. The states in which the bridge allows passage from the rail to ground are “pull –“, and the states allowing passage of current from ground to the rail are “pull +”.

Given the high-power nature of this environment, implementation of this grid is too taxing on most semiconductor devices. Thus, the H-bridge configuration uses IGBT/Diode pairs.

# 2 Background Information

## 2.1 Signal-Processing Theory

### 2.1.1 Waveform Parameters

The basic waveforms of signals theory, and the basic units of analysis in this project, are composed of the periodic sine and cosine functions. For a proper understanding of the concepts active in this work, one must understand the non-atomic variables used in the analysis of the controlled variable. For the purposes of this work, we describe the fundamental units of the controlled variable to each exist as parameters of "cosine" functions. The parameters which all periodic functions have in common, each entirely independent of the others, are thus: amplitude, frequency, and phase. These parameters' fit into a waveform are represented in the following mathematical model:

$$y(t) = A \times \cos(2\pi \times f \times t + \phi)\,. \tag{1}$$

In this model, amplitude is represented as $A$, frequency as $f$ (often represented as angular frequency, $\omega$), and phase as $\phi$. Each affects the specifications of the wave, but to fully realize how, one must first know the base specification of the waveform in question, modelled as the cosine periodic function.

The most basic form of the cosine function, stripped of all parameters to their unit equivalents, is represented in the following mathematical model:

$$y_{basic}(t) = \cos(t)\,. \tag{2}$$

These parameters evaluate, for reference, to amplitude $A = 1$, angular frequency $\omega = 1$, and phase $\phi = 0$.

As might be observed, the range of this function is from 1 to its negative. One cycle, or *period* is measured from peak to same-peak, i.e. from $y(t_0) = 1$, to $y(t_1) = 1$, where $t_0 < t_1$. As the wave is *periodic* (repeats), the waveform over one period $T = t_1 - t_0$ will be identical to that over any other period, measured at the same *phase* (details to follow), in the cycle. The period of the basic cosine form is $T = 2\pi$.

The first parameter examined here is *amplitude*. The amplitude parameter is represented as $A$ in the generalized cosine function representation.

One observes that adjusting the amplitude parameter scales the value of the waveform, at all time instances, proportionally to the magnitude of the parameter's change. As previously mentioned, the amplitude of the most basic cosine function, $\cos(t)$, is 1. Thus in-phase cosines of the same frequency, with amplitude values $A = 2$ and $A = 0.5$ respectively double and halve each value of the waveform.

As seen subsequently in the section on superposition and the Fourier Transforms, amplitude is valuable to signal analysis as this is the parameter responsible for the energy or the prominence of a signal component, and ultimately informs the shape of more complex waveforms for which certain analyses are desired within the scope of this project.

More complex signals are commonly analyzed and manipulated in the frequency domain, rather than the time-domain format, more common in most other applications. The *frequency* parameter, denoted as $f$ in the basic cosine function, denotes how many periods of the cosine exist per unit time.

Frequency adjustment is akin to a time-scaling operation. For a single cosine waveform, the two operations are synonymous. The period of a waveform, as mentioned earlier where the period of the basic cosine function was given as $T = 2\pi$, is related to waveform frequency by $f = \frac{1}{T}$. If one cycle occurs per second, the period is one second. If two occur, the period is half a second. Continued exploration of behavior reveals that the inverse-proportional behavior holds, and no other information exists in the relation.

Frequency information may be expressed in either Hertz (Hz, inverse seconds) or in radians per second, as an angular velocity, $\omega = 2\pi f$. Multiples of a given frequency of interest are referred to as *harmonics*. In the above frequency demonstration plot, the double-frequency wave is the 2nd harmonic, which is in turn such to the half-frequency wave.

There exist two special cases of the cosine function that are exhibited with frequency, at those points where either $f$ and $\omega$, or their limits, converge. The first occurs at $f = \omega = 0$, where no oscillation occurs. We derive the formula for this case from that of the generalized cosine function, yielding: $y_0 = A \times \cos(\phi)$, a constant dependent upon the other two parameters, also known as the DC (from electrical engineering's "direct current") case. The second exists at $\lim_{f \to \infty} \omega = \infty$. This case is physically impossible to achieve (at least in the context of this project) as the waveform value, unlike a mathematical function, does not possess a singular value for every instance in time, yet persistently exhibits two constant values.

The third parameter, *phase*, is often considered rather more of a nuisance than the other two which provide solid means of analysis and manipulation. In much of signals processing, phase exists as a non-ideal reality, more to be matched or corrected for than to be used to one's advantage.

Subtractive phase-shifting makes a wave occur earlier in time, and additive shifting delays its occurrence, respectively called *lag* and *lead*. Phase can be expressed in angular degrees, radians, an in

rare occasions may even be represented in units of time. Phase-shift is also the relational operator between the sine function, cosine, and each of their negative, where cosine is a copy of sine with a lag of 90 degrees, or $\frac{\pi}{2}\ rad$. Finally, the negative of any periodic function, with a bias (average value) of zero, is a copy of itself, either lead or lagged (equivalent in this case and the identity case) by 180 degrees, or $\pi\ rad$.

### 2.1.2 Waveform Superposition

The principle of *superposition* states that the result of the presence of two independent sources in a linear system results in the algebraic sum of those sources. Sinusoidal waveforms are, mathematically, linear functions, and thus the effects sinusoidal sources superimpose to define the behavior of the system.

In the time domain, this is perhaps most visible using two waveforms with a high order of magnitude difference in frequency, with the lower frequency waveform possessing a far greater amplitude. We might think of this as a noise-interference introduced to a desired signal.

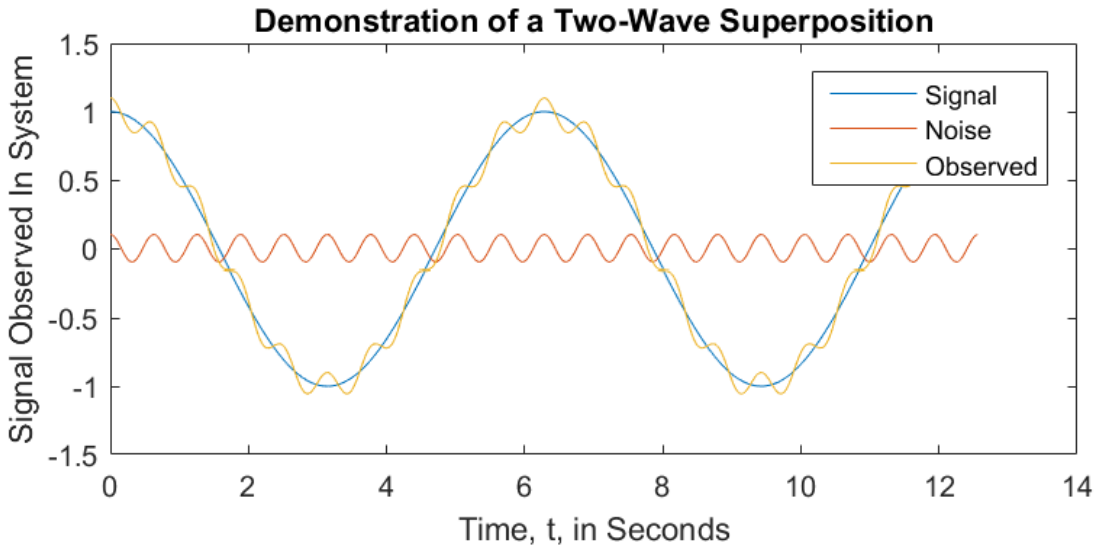


*Figure 6:Illustration of the Superposition Principle*

A copy of the noise waveform oscillates around the signal as if it were using the signal as its own private time axis (which it is). Some variation on the wave "Observed" will result in any linear system in which multiple waves of different frequencies are present.

### 2.1.3 Continuous-Time, Discrete-Time, and Digital Signals

A continuous-time signal is represented as a mathematical function defined for every real-valued time instance. A discrete-time signal may exist for any full-continuum range of values, but is only defined for fixed-integer discrete-time values in the domain. A digital signal, like a discrete signal, is only defined for a number of fixed-integer indices, but may only have a finite set of values.

Suppose a signal $x$ is to be sampled over fixed length intervals to yield the sampled signal $x_s$. There exists a difference in how these two signals are annotated. The continuous-time original is written as $x(t)$, whereas the sampled copy is $x_s[n]$. The index, $n$, may only possess integer values. For instance, $x_s[1.3]$ is, by definition, undefined.

The unit-impulse function, $\delta(t)$ (continuous time) or $\delta[n]$ is used to model significant events, which occur over very short periods of time. For both continuous or discrete-time models of the function, non-zero value only occurs when its parameter is zero.

The impulse function can be easily delayed and scaled in a manner shown in the following equation, and can be seen for $c = 5$ and $n_0 = 2$ in the subsequent demonstration plot.

$$c \times \delta[n - n_0] = \begin{cases} c, & n = n_0 \\ 0, & t \neq 0 \end{cases} \tag{3}$$

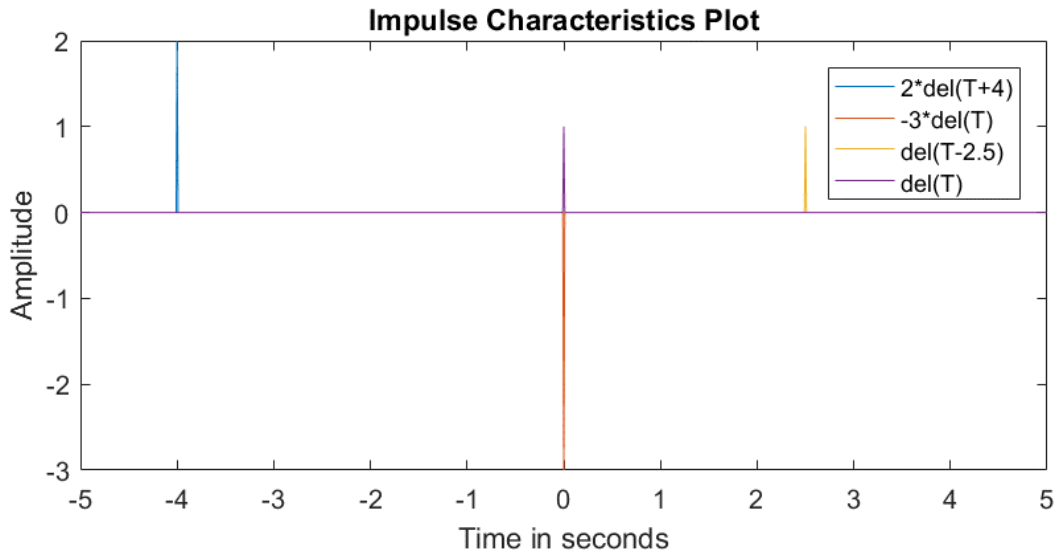


*Figure 7:Behaviors of the Impulse Function*

The unit step function models a square-step transition:

$$u(t) = \begin{cases} 1, & t > 0 \\ 1/2, & t = 0 \\ 0, & t < 0 \end{cases}. \tag{4}$$

It scales and time-shifts just as the unit-impulse function and is used to model the introduction of new information to a system. By multiplying another function by the unit-step, and shifting both function appropriately in time, one can dictate when the function appears.

### 2.1.4 Complex Magnitude and Phase, and Euler's Identity

*Complex numbers* are those numbers of the form:

$$c = a + j \cdot b \tag{5}$$

This relation is labelled complex as it contains the *imaginary number*:

$$j = \sqrt{-1} \tag{6}$$

Such a value is said to exist in the *complex plane*, in which the vertical axis is the real-part of the value $a$, and the horizontal is the scale of the imaginary part $b$. The representation above is a

rectangular coordinate, but like any value on a two-dimensional plane, it has a polar representation as well, containing the value's magnitude, $\|c\| = r$, and phase $\angle c = \theta$, (length of vector from the origin to the value, and the angle between the vector and the positive x-axis.)

$$c = r(\sin\theta + j\sin\theta) \tag{7}$$

By introducing *Euler's Formula*, one allows for an even simpler representation of complex numbers. Euler's formula and its application to the task at hand are as follows:

$$e^{j\theta} = \cos\theta + j\sin\theta \tag{8}$$

$$c = re^{j\theta} \tag{9}$$

This representation of complex numbers informs the ability to be able to transform a set of time-domain information into the complex-plane in a manner reflecting any periodicities present. For each value in the range of the function, there is an associated magnitude and phase. As the periodicities are accounted for, this concept enables a view of mathematical functions as super-positions of sinusoids, and the parameters each carries.

### 2.1.5 Complex-Frequency Domain

Building on the principle of superposition, one posits that, as a continuum of frequency values exist, that any mathematical function may be expressed as a superposition with varying parameters. The mathematical concept resulting from this line of research is the *Fourier Transform* of a mathematical function, and happens to lead the user through the complex plane. As a representation for complex numbers exists, with a dependency upon the magnitude and phase of its Euler's representation, a single-frequency waveform's magnitude and phase are encoded as a complex number and each waveform in a superposition is represented as a continuum of such numbers, each assigned to the corresponding point on the frequency continuum.

## 2.2 Circuit Theory

As the motivation for this project is to design a process able to compensate, in physical circuits, in physical currents. Given the high-power demands at output, digital control of a DAC will not suffice. The process must be able to measure large-analog currents, and prepare it to be sampled by an ADC. At output, a configuration of eight semiconductors must be supplied with power, which is to be delivered to the network through proper control of this bridge converter.

### 2.2.1 Loads

If an electrical system is not intended for information and signal processing and analysis, be it either sensory or manipulative, then this system has a *load*. The load is the system's raison d'être. It is the intended target for electrical energy or power in the system, where the remainder of the system exists to cater its power delivery to the specifications required by the load, at a given moment in time, to match the most practical level of efficiency and operational requirements. A prime example is the battery in a mobile phone, for which there are AC-DC conversion systems to turn the available power into that most useful to charge the battery. Other common examples include lights, motors, and heating elements.

Introductory circuit theory largely focuses on linear components, such as resistors, capacitors, and inductors. The shared attribute of these components that makes them linear, is a constant impedance regardless of the supply characteristics.

In electrical engineering, a *linear load* is defined[3] as an electrical load exhibiting an impedance independent of applied voltage [10]. As impedance is frequency dependent, this implies that the

[3] Defined inversely from the definition of non-linear load in the cited MIRUS International, Inc. document

current passed by a circuit branch consisting of a linear load will contain only frequency elements present in the voltage applied.

Inversely, a *nonlinear load* is defined as an electrical load for which “impedance changes with applied voltage” [10]. As such, these loads cannot, in theory, be accurately represented by impedance phasors, or any series-parallel configuration of such mathematical models that would otherwise enable introductory AC circuit analysis techniques.

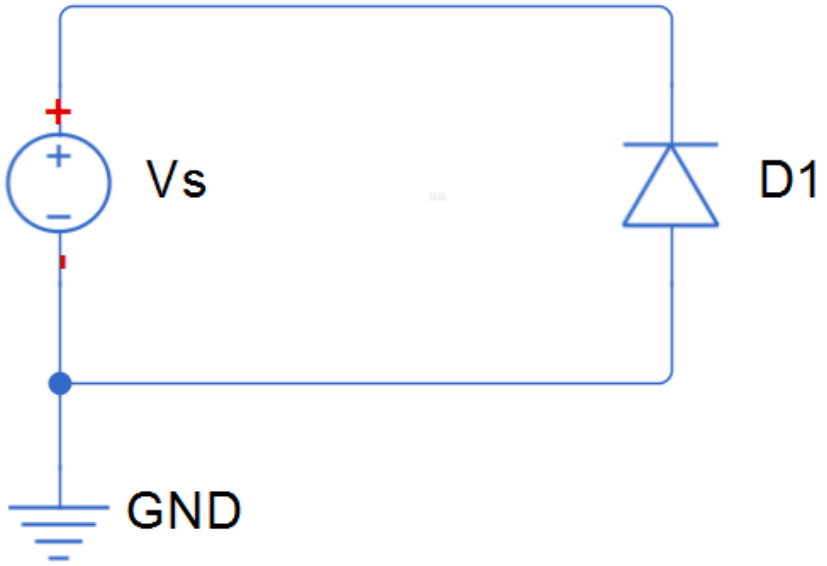


*Figure 8: Circuit Diagram for Nonlinear Load Demo*

There exist wide varieties of nonlinear loads, with wild variation between their behaviors, or characteristics. An early-taught nonlinear element, the diode, makes an acceptable and accessible example. Tutorial information for this device is provided in a closely subsequent section devoted to their behaviors, within their own passages in the Simple Semiconductors tutorial segment. The load’s current and voltage are related in manners that are not expressible as fading or phase-shifting of existing frequency components.

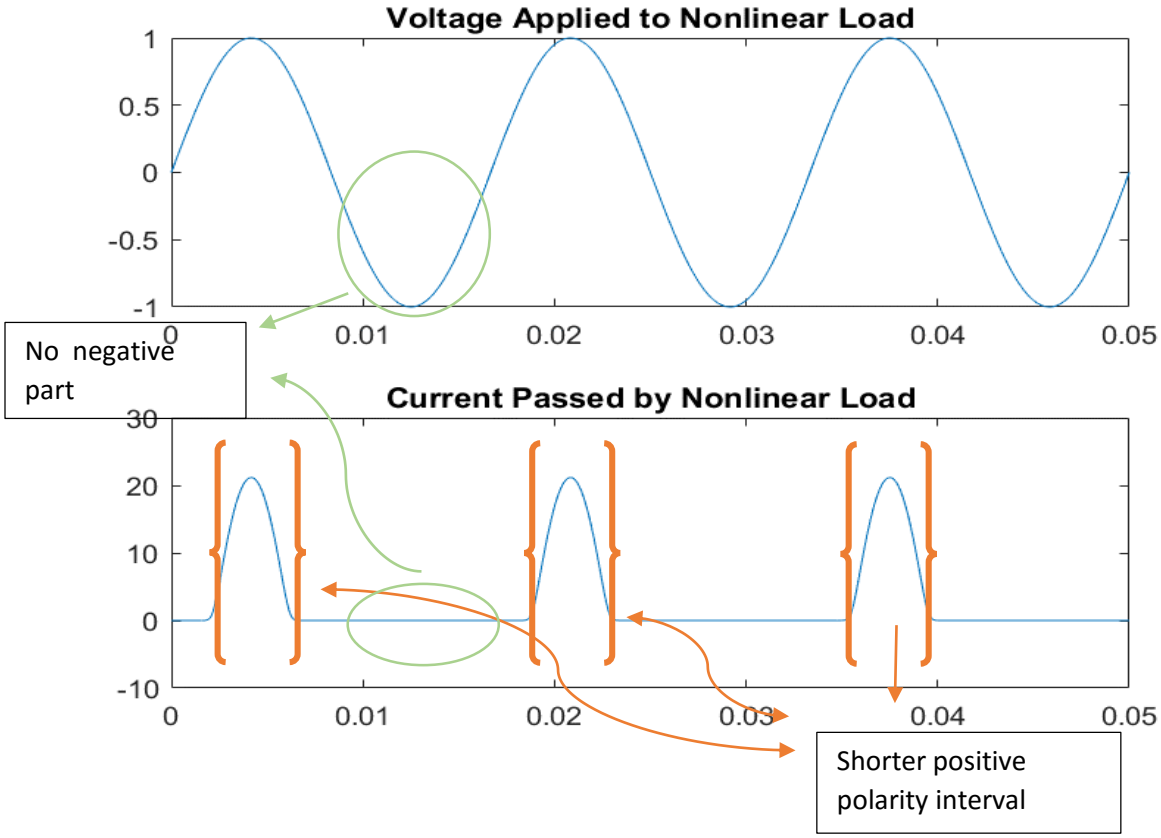


*Figure 9: Simulated Voltage Drop and Current of an Exponential Diode Load*

The example simulation results provide intuitive ability to directly tie the concepts of nonlinear loads and *linearity* (whether scaled and time-shifted inputs yield proportionally scaled and identically time-shifted outputs). If this were a linear load at the simulated steady-state, a purely sinusoidal 60Hz load would produce a purely 60Hz sinusoidal load current with affected magnitude and phase.

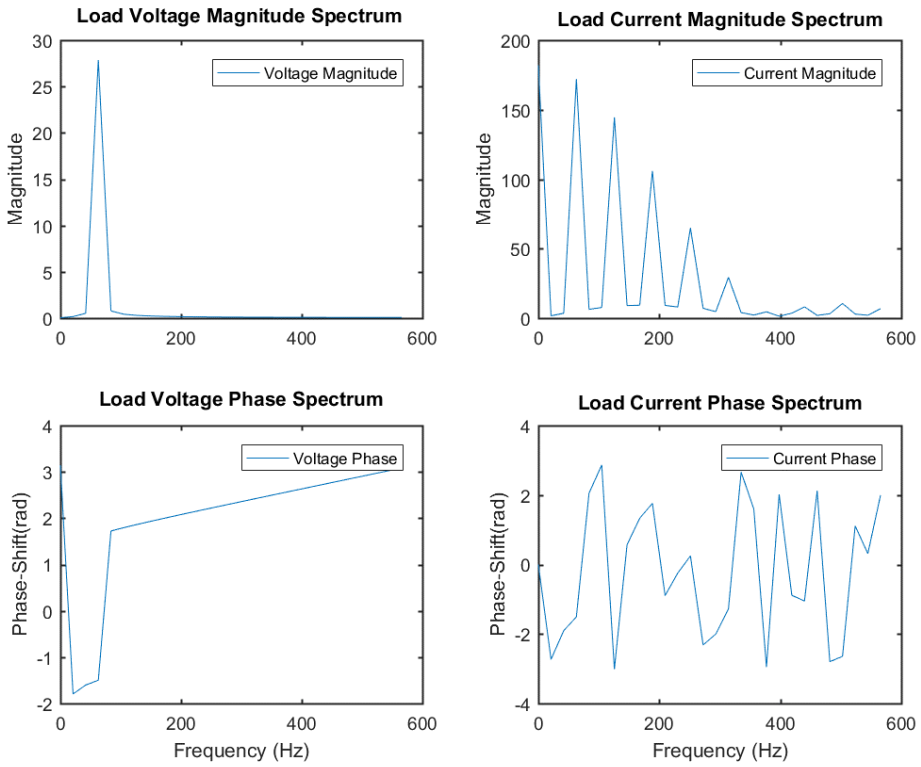


*Figure 10: Nonlinear Load Demo Frequency Domain*

Linearity implies that frequency components in the current could only exist where there were frequency components in the load voltage. One can observe from Figure 10 that the load current contains five prominent frequency components at, not just 60Hz, but at 0, 120, 240Hz, 360Hz, and 420Hz. Given the 60Hz applied voltage, this translates to the $0^{th}$, $1^{st}$, $2^{nd}$, $4^{th}$, and $6^{th}$ harmonic incident in the load current. This document often refers to *nonlinear current*, which is, in the scope of this document, to current signal of all components excluding the $1^{st}$ harmonic.

### 2.2.2 Simple Semiconductors

Diodes exhibit a couple of useful behaviors relevant to the scope of this project. These two-terminal devices are composed of doped semi-conductors that grant it a monopolar electrical operation. The two terminals are referred to as the “anode” and the “cathode”. The anode is connected to a chip composed of a semiconducting material, such as silicon, chemically altered, or “doped”, to be of the “p-

type". The semiconducting chip at the cathode is doped to be "n-type", and these chips are directly joined in series.

Because of the electrical properties introduced through the chemical doping process, electrical current may only flow in one direction through the diode's ""pn-junction", from the anode to the cathode. This gives the diode a very useful application as a sort of one-way valve. It is useful in rectification processes, where current may only be allowed to flow in one direction. AC-DC converters commonly found in laptop, phone, or other battery charging devices make use of a configuration of two diodes to project the negative half of an alternating-current waveform into positive current, so as to effectively output the absolute value of the electrical current and voltage waveforms.

Due to the electrical properties of the junction, there is some distortion in this rectification process that is relevant to operation. There is a voltage threshold in the positive region that must be met for the diode to become active. This pattern is more continuous than suggested, with a more complex exponential mathematical model where any "forward-bias" voltage does increase current flow, significant current flow only occurs one the forward-bias voltage inhabits the neighborhood of 700mV. Due to exponential dependency the current displays with relation to the biasing voltage, even very large currents correspond to a bias-voltage of little over this 700mV threshold, making them an effective voltage-limiter even in forward bias.

Where diodes act as directional valves for current and set a stable voltage drop when correctly biased, devices called *transistors* build upon this behavior, combining doped junctions to exhibit certain circuit behaviors. Like diodes, current may only pass in one direction through a transistor's *channel*, the path between the two pins (called the *drain* and *source* in FETs, and emitter and base in others.

Unlike diodes, transistors possess a third pin used for control of the device. Electrical signals at this pin control how much current may pass through this channel. Different transistors use different

mechanisms to implement this pin. For some, transistor operation is more dependent upon the current at this pin (usually called the *base* in such cases). For others, such as those relying on more capacitive behavior at this pin (called the *gate* for these devices), voltage is more determinant.

One of the primary applications of transistors is *switching*, or allowing and restricting the passage of larger current with a low-powered signal. Gated transistors are commonly used for switching applications due to desirable switching speeds. For this demo, an *insulated-gate bipolar transitor*, or IGBT, is used to demonstrate switching. The Specialized Technology in SimPowerSystems is used, and instead of being fed a real voltage at its gate, is activated by a Simulink signal of '1', and turned off at a Simulink signal of '0'.

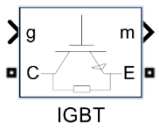


*Figure 11: Simscape Power Systems "Specialized Technology" IGBT*

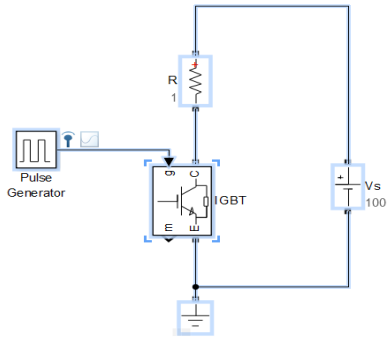


*Figure 12: IGBT Switching Demo Circuit Diagram*

The IGBT's three terminals are the gate, the collector, and the emitter, labeled "g", "C", and "E", respectively[4]. The collector and emitter are the terminals to this device's channel. For the n-type transistor shown above, significant current may only flow from the collector to emitter. For this block,

[4] The fourth terminal, "m", shown is simply a carrier of monitoring and logging data. This has no bearing on its electrical behavior, but provides an easy read-only handle on the voltage drop across- and current through the channel.

current is permitted easy passage if, and only if, a "1" is sent to the gate. By this method, electrical voltage may be restricted or given a path by a controller signal as seen in the demo.

This enables a system to control the average power delivered to a load, in this case the resistance. Lower power analog and digital systems alike commonly take advantage of this with the *pulse-width modulation* (PWM) technique. Pulse-width modulation entails a periodic square-wave pulse where the pulse-width, the time for which the transistor's channel enables the passage of current, is handled as a percentage of the square wave's period.

$$duty\ cycle = \frac{t_{on}}{t_{on} + t_{off}} \times 100\% = \frac{t_{on}}{T} \times 100\% \tag{10}$$

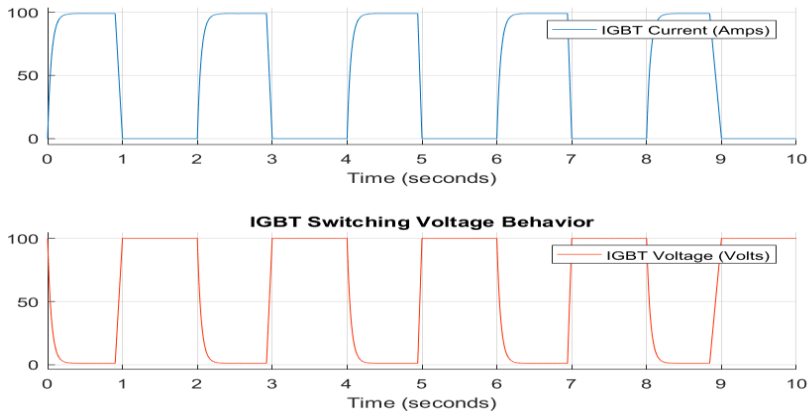


*Figure 13:IGBT Switching Current and Voltage Behaviors*

The demo shows a 50% duty cycle with a period of two seconds. When the channel is closed, a high voltage drop is exhibited across the collector and emitter of the device. As it opens, its effective resistance decreases rapidly and the voltage across the channel drops sharply as an electrical current rushes through what is now effectively a small resistor. The parameters of the IGBT used in the demo have been altered to exaggerate a behavior of interest to this project. Notice the transition times, for

both current and voltage, are finite and non-zero. The capacitive gate takes some time to charge. Thus the channel sweeps through varying degrees of "open" after the moment of switching.

This behavior allows, if a sufficiently fast mechanism can be achieved for current monitoring purposes, the capacity for control to keep it within a determined range. The demo can be altered to never allow the passage of more than a certain threshold. By measuring the current, determining if it is less than or equal to 10A, and performing a logical and with a constant 1 for reference, one achieves the current waveform in Figure 14.

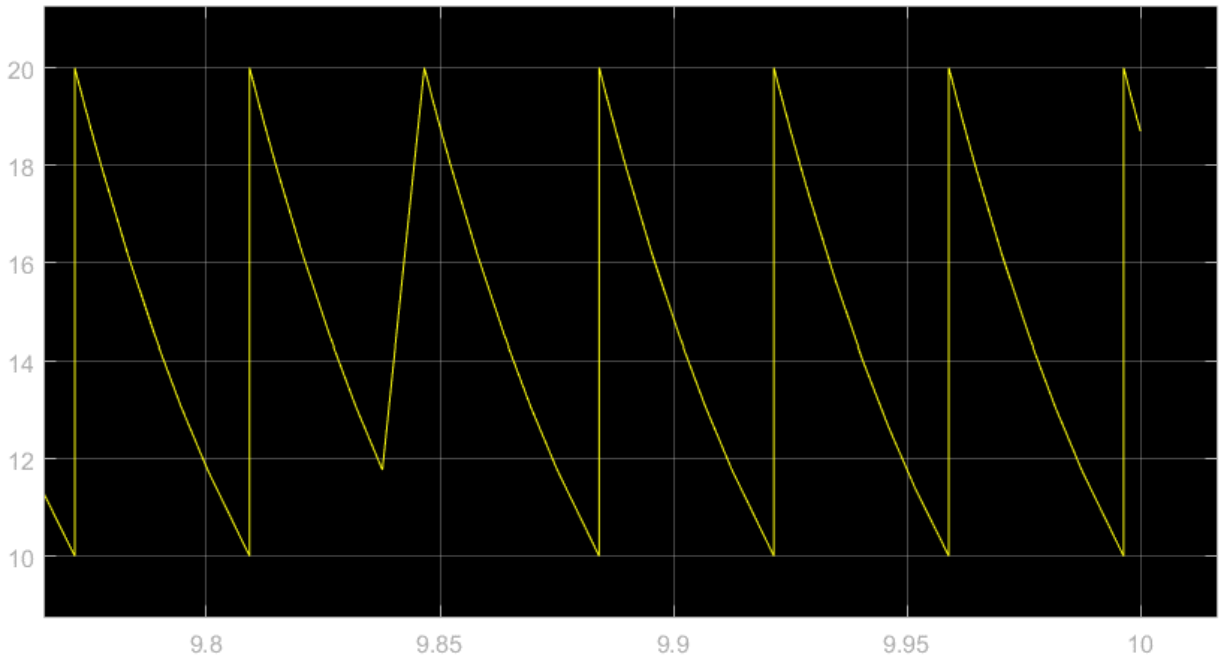


*Figure 14: Current-Amplitude Controlled Switching Demo, Current Waveform*

Use of the Simscape Power Systems → Specialized Technology IGBT is highly recommended if Simulink is to be used further, as these are the only IGBT models that have been observed to allow this behavior in simulation, as a number do not.

This block also allows for some simplification not provided in others, as operation perfectly corresponds to gate input "1" for the active state, and "0" for the off state. This does not reflect gated-

transistor realities. Physical gated transistors, and all Simulink IGBT blocks excluding the one used here, activate if the gate voltage, the emitter or collector voltage (emitter for the n-types used here), and the device's threshold voltage meet the condition: $v_g - v_e \geq V_{Th}$.

In an AC environment this can cause issues if the gating signals are, themselves, absolute with reference to ground, supposing the emitter voltages are not, as was the case in the project. This case caused substantial issues for the project, as its effects were being observed without the root-cause being realized. The compensator was passing substantial current when all transistors were thought to be closed, and checking each transistor's pins voltage and current was a sufficiently daunting task that either debugging was implemented through other means, misattributed, or forewent altogether in early test environments as it was assumed the behavior would not follow to actual implementations.

The gate control signals must follow the emitter's voltage, this is an easy enough task if the emitter is grounded, or for a p-type transistor if its collector is tied to a steady, lower magnitude, DC voltage. But at large or highly variable n-type emitter or p-type collector voltages, generation of these control signals may not be a trivial task. To make matters more difficult, the only viable IGBT or IGBT/Diode block candidates in Simulink are n-type. Thus the gates must be tied to and biased from the transistor. The solution was implemented by, instead of offsetting the transistor gate voltages from ground, tying them to the devices' emitters through more current sensitive relays, themselves tied to ground, allowing for a grounded digital device to switch signals in an environment offset significantly.

The exact circuit natures are yet undetermined, but Simulink and Multisim schematics and their application to the IGBTs may be seen below, for simulation purposes only. More design work is required to provide further realization.

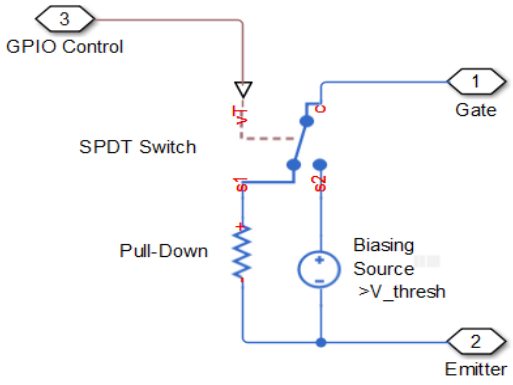


*Figure 16:Simulink Emitter-Following Gating Circuit*

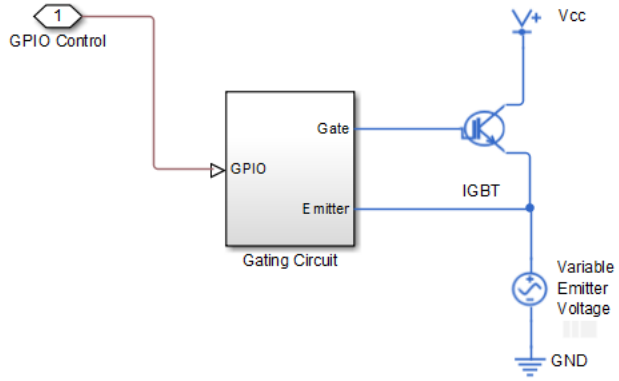


*Figure 15: Simulink Emitter-Following Gating Circuit IGBT Configuration*

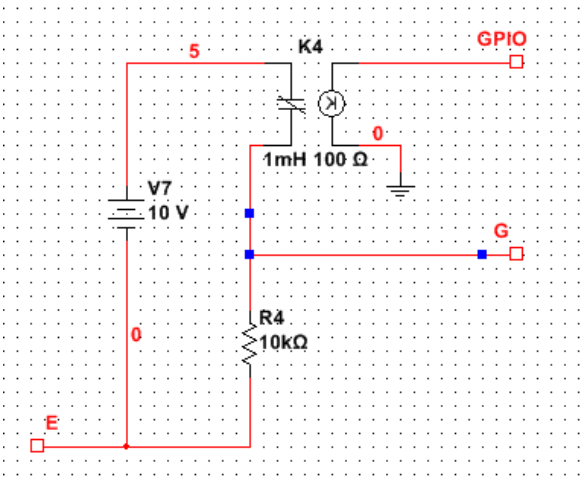


*Figure 17: Gate Emitter-Following Circuit Using Relays*

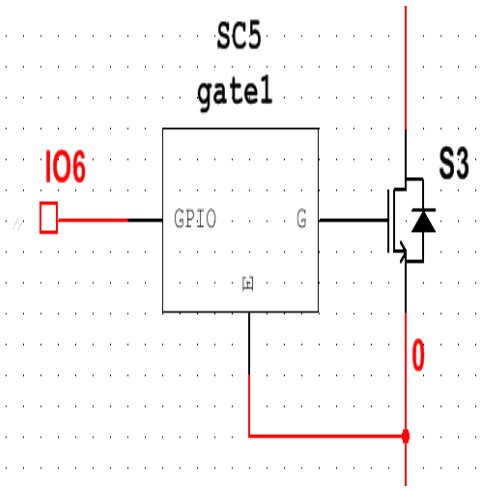


*Figure 18: Multisim Application of Gate Circuit*

The Simulink gating-circuit possesses a nontrivial abstraction. The single-pole double-throw switch is not a physical reality. With limited experience working with the relevant replacements, relays, the following circuits were designed as possible more realistic equivalents.

### 2.2.3 The H-Bridge

The H-Bridge is a configuration of four switching transistors, each coupled with a flyback diode to mitigate the consequences a transistor experience when switching power to an inductive load. The

bridge converters and h-bridges are most famous for their applications in electromechanical controls, where they are used to control motors that require the ability to rotate in both forward and reverse directions, and current moving in opposite directions for each state.

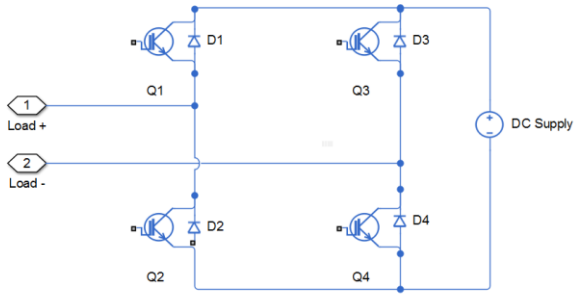


*Figure 19: Project H-Bridge IGBT Configuration*

This configuration essentially allows, when a controller or equivalent circuit is applied to the gates, for the DC supply to be inserted into a circuit, in either polarity, without manual reconfiguration. The convenience, and greater switching speeds than are available with manual reconfiguration, come at the light cost of a small increase in the internal resistance of the supply equivalent to the H-bridge circuit.

Given the very common bi-directional motor application, two states are typically used for this device (forward, reverse, and off), and two are usually avoided. The undesirable “shoot-through” states, are those for which the bridge effectively allows a short-circuit across the terminals of the DC supply. The transistors are not intended to be active at the same time as those with which they are paired vertically. Gated transistors typically exhibit very low resistances in their active states. In any given moment, one transistor is supposed to pass current, and the other to block it so that it may be

redirected to the load, shown by the connection ports for the circuit in Figure 19. If transistors Q1 and Q2, or Q3 and Q4 are in any degree of active simultaneously, these two states, in which nothing is achieved but senseless power loss, are the current operating condition of the device.

The three standard operating states are equivalent to the voltage across “Load +” and “Load –" having positive polarity, having negative polarity, and exhibiting an effective open circuit. For the open-circuit, “off”, “inactive”, or “idle” state, no transistors are on, and the load no power should be delivered unless the transistor gates are incorrectly biased, or a diode is active. Voltages should be thoroughly examined should such problems occur.

The positive polarity case is achieved by setting active control signal to transistors Q1 and Q4. The current path, from connection port “Load -“ flows through transistor Q4 into the negative lead of the supply. It exits the positive terminal and leaves the sub-circuit through “Load +” via Q1. For the opposite polarity, Q2 and Q3 are set to active. Current is drawn through Q2 via “Load +” through the supply, and is ejected via Q3 when presented with an inactive Q4.

# 3 Proposed Approach

## 3.1 Solution Concept

The proposed approach has five top-level units of which the operation is composed. These stages are referred to as the “Analog Current Preprocessing”, “Analog Voltage Preprocessing”, “Digital Processing and Controls”, “Output Monitor Triggering”, and “Power Delivery” units.

The Analog Preprocessing blocks monitor the voltage and current present in the grid, and operate on them in a manner to increase their compatibility with digital processing. The Digital Processing and Controls stage collects this data at fixed-interval time instances, generates a target current to be delivered, and determines the state of operation for the Power Delivery system for any given interval.

The Power Delivery circuitry takes the control signals from the Digital Processing and Controls unit and operates to deliver thusly controlled current into the device's environment, and the Output Monitor Triggering block monitors the output current and sends an alert to the Digital Processing and Controls Unit should the output current drift from an acceptable tolerance in the boundaries, upon which the receiving unit will make appropriate corrections.

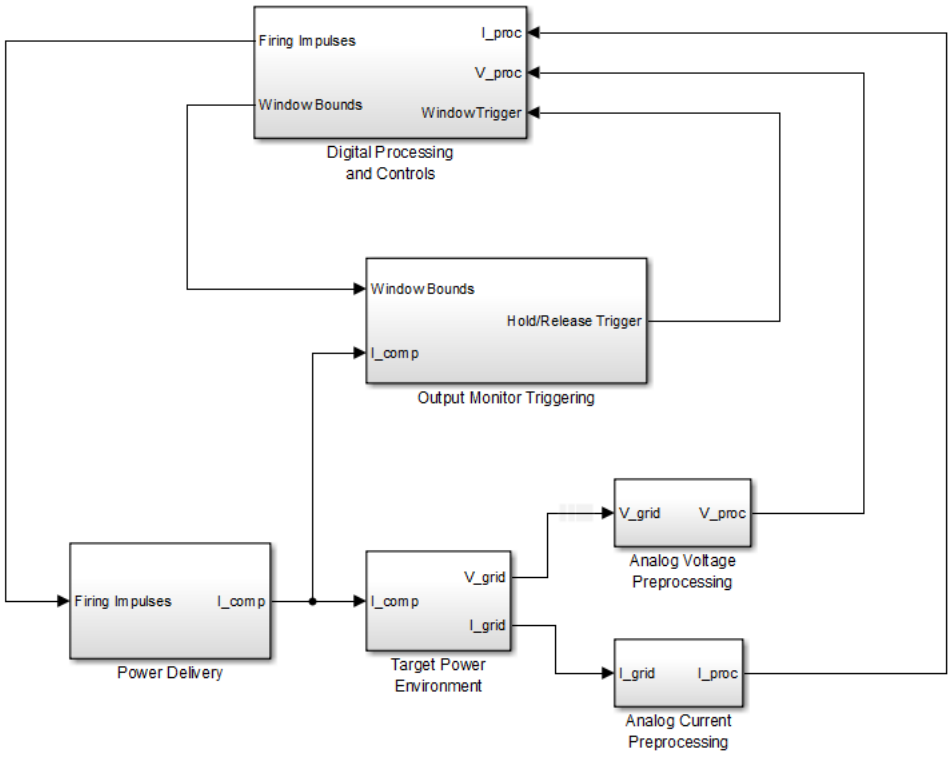


*Figure 20: Top-Level Block Diagram of Proposed Solution*

Here one can see the anatomy of the system. One block, the "Target Power Environment", has not yet been discussed under this handle due to the fact that it is external to the device. It is the environment which the device is intended to control. From this power network, we attain two necessary measurements, grid voltage "V_grid" and grid current "I_grid", which are fed to the inputs of Analog Voltage Preprocessing and Analog Current Preprocessing, respectively.

These blocks turn these indicators into forms the Digital Processing and Controls block can handle, the preprocessed currents and voltages. These are respectively denoted as “I_proc” and “V_proc”.

The Digital Processing and Controls unit produces the gate “Firing Impulses” signals which run to the gates of the IGBT/Diode pairs in the H-Bridge that constitutes the Power Delivery system. It also produces a window of acceptable instantaneous delivery current, calculated to be a fixed tolerance above and below that sample interval’s target compensator current.

The power delivery apparatus makes no internal decisions of its own, nor does it perform any processing, but simply enters the state intended to supply the desired current. Passive lowpass filtering is applied to prevent undesirably swift current transitions, mitigating high-power spikes.

To further mitigate the high-power current spikes, analog circuitry is included to monitor the compensator current “I_comp” in real-time. A scaled version of the compensator current is compared to the window boundaries supplied by a DAC in the Digital Processing and Controls block. If it drifts past the outer-bound of the window, the block sends an asynchronous “hold” trigger, to be received as a hardware interrupt by the digital block, which dictates that the Power Delivery exit all operation. This condition remains true until the compensator current drifts closer to the origin than the floor of the window, at which point the unit sends a “release” trigger, also to be received as a hardware interrupt, that allows the digital unit to resume regular operation of the bridge.

### 3.1.1 Analog Voltage Preprocessing

Each Power Delivery state, with the exception of the “idle” state, is intended for use at a particular bias, refined by further determinations. Thus, the device must have some level of awareness of the grid voltage, one of the conditions under which the bridge operates. This is the justification for generating a digital handle on the grid’s voltage.

This proposed solution implements no predictive functions for further refining of targeted power delivery, thus needs no phase-locked-loop with regards to the voltage, nor any memory of past grid voltages. As instantaneous sampled voltage is all that is used, there are no aliasing concerns. Aliasing concerns would likely be unnecessary in any case, as in power applications, voltage oscillation is restricted to low frequencies, such as 60Hz in most US applications, and 50Hz in most European.

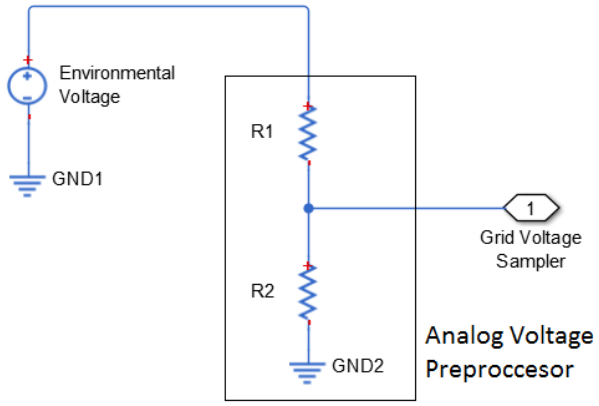


*Figure 21: Analog Voltage Preprocessor Circuit Diagram*

Thus, the only necessary function for this block to perform is a linear scaling of the voltage. Analog Voltage Preprocessing is accordingly simplified to a basic voltage divider circuit. 3.3V is a ubiquitous supported voltage scale for ADCs so the voltage is scaled appropriately. Instantaneous high-voltages are made safe by scaling to use only 60% of the ADCs range, splitting the 20% on either end to allow for unexpected voltages, considered damaging to the device.

The nominal voltage of a given target environment is unknown in the scope of this project, whose purview is the design of the process. Yet the objective is to scale the maximum expected voltage amplitude to 30% of 3.3V, producing an expected maximum voltage of just under 2V, close enough to make this the new metric.

The voltage divider equations, under this requirement produce a relationship between the shown variables $R_1$, $R_2$, and the expected environmental peak voltage $V_g$:

$$\frac{V_g}{2V} = \frac{R_1}{R_2} + 1 \tag{11}$$

For the simulated power grid used in this project, with a 1kV amplitude voltage, this would give the relation:

$$R_1 = 499R_2 \tag{12}$$

This block should also behave with near-zero loss, given the environment, 100µW of power loss is deemed acceptable. Thus, for the purposes of this project, this block tolerates 100nA of current draw. To achieve this, the series resistance should be at least 10GΩ, giving resistor values of:

$$R_1 = 9.98G\Omega, \qquad R_2 = 20M\Omega \tag{13}$$

#### *3.1.1.1 In Abstract Simulation*

As attention was primarily focused on other units for the scope of this project, this has yet to be fully implemented. Rather, both the SimPowerSystems and SimElectronics libraries of Simulink provide "Voltage Measurement" or "Voltage Sensor" blocks that may be used in-stead, without voltage scaling. These were leaned on heavily throughout the project as this particular aspect was deemed a detail of the larger task, in which the true technical difficulties lay elsewhere.

### 3.1.2 Analog Current Preprocessing

The Analog Preprocessing Unit exists to measure the grid's current in the analog continuous-time domain, and process it in a manner where it may be effectively analyzed by the Digital Processing and Controls Unit.

Three stages are used in this process, and while variations in their functionalities may exist, these three functionalities cannot, in general real applications, be removed, mitigated, or replaced, while maintaining an expectation of a functioning device. The three stages are current sensing, current-voltage transformation, and antialiasing filtration.

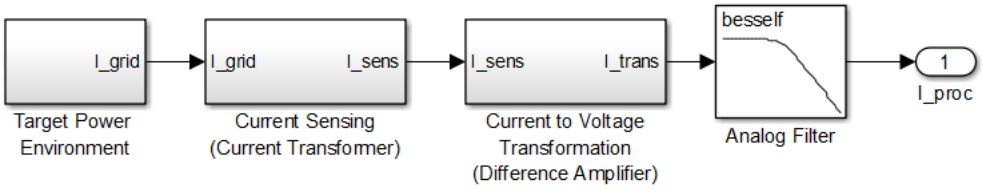


*Figure 22: Top-Level Diagram of Analog Current Preprocessing*

To this end, for general applicability of the process, three variables must be left unspecified, and all three must be accounted for, primarily, in this stage of the process. All three stages can affect the target parameters, *gain* and *cutoff frequency*.

The first of such variables are the maximum expected in the environment or portion of the power network in which the device is applied. This is critical to device operation, as if this value is exceeded significantly, irreversible and function-prohibitive damage can and will be done to the device. This is best illustrated when examining the *gain* variable of the Analog Preprocessing unit.

The second unspecified variable is the maximum supported frequency for which the device is intended to accurately compensate. Beyond the often band-limited nature of semiconductors, sampling theory dictates that accurate processing may only occur for a range of frequencies wholly dependent upon the sampling rate utilized. Thus, the Analog Preprocessing Unit must be tailored to sufficiently suppress information at frequencies existing beyond this range. This is relevant to determinations of the *cutoff frequency* of the Analog Preprocessing Unit's filtration-type sub-processes.

The third is the frequency response of the grid current, itself. This variable is strongly tied to determination of an effective cutoff frequency, but is distinct, in its own right, from the concept of maximum supported frequency. It is possible for certain high-magnitude components to survive a filter's nominal *break frequency* to a degree that could result in aliasing when the Analog Preprocessing unit's output is sampled. In designing the filters used, it is important to ensure that no such case exists persistently in standard operation.

As suggested above, the two targeted design parameters for this unit are *gain* and *cutoff frequency*. Design requirements for this block include minimal *operational delay*, and *phase-distortion characteristics*. Operational delay refers to the real-time delay between the existence of a current measurement in the grid, and the moment at which that information appears at the output of this unit. Phase-distortion characteristics apply primarily to the filter's phase response, but also to any frequency domain responses of any nonlinear semiconductor devices, such as the operational-amplifiers that must necessarily appear in this process.

This is a simpler process than its current-focused counterpart, but no less crucial to providing accurate output. Given the high-power target environments and the requirement of minimal loss, only one device can effectively perform this job: the current transformer.

A very low winding current transformer, installed around the line of interest (not in-line), will provide, to the Analog Current Preprocessing Circuit, a down-stepped current proportional to current present in the grid. This contributes to the targeted gain parameter.

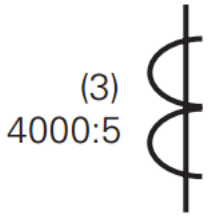


*Figure 23: Symbol for Current Transformer [8]*

As the sampling process commonly reads voltage, and not current, it is necessary to set change the independent variable of the circuit from current to voltage. The enabling principle behind this block is, that as the independent variable of a series loop at the secondary winding of the current transformer

is current, the voltage across a resistance in this loop will vary proportionally to the secondary winding's current, and thus to the grid current. Measuring this voltage difference across a known, constant resistance in the series loop gives a current indicator, in volts, calibrated to the resistance across which it is measured.

A very simple version of the common methods for performing such a conversion in a low-power environment, such as the one this section is describing for the purpose of transitioning from the high-power grid to the low-power, sensitive interface with the digital unit, is a differential amplifier.

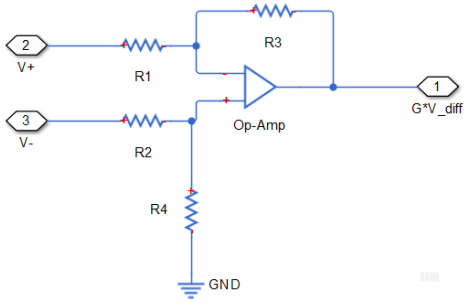


*Figure 24: Difference-Amplifier Schematic [11]*

This is a viable solution for simplicity's sake, where $V_{diff} = V_- - V_+$ (this configuration is inverting), and G is this block's gain parameter. Resistances should be set such that $R_1 = R_3$, and $R_2 = R_4$. Following this the voltage gain parameter is the result of $G = \frac{R_2}{R_1}$. For purposes of isolating the sensitive semiconductor circuitry, the operational amplifier, it may be advantageous to connect the reference node to the digital unit's ground port, rather than that of the high-power target environment.

The difference amplifier is installed with the "V-" input lead on the positive-reference side of the resistance in the loop of the secondary current transformer winding, and with "V+" on the other side. As the current transformer will attempt to fix the current in the loop, and vary voltage, minimal losses occur with the lowest possible sense resistance, if an actual component must be wired in to serve this purpose.

This circuit, in such a configuration, will output the voltage drop across the resistor, multiplied by the gain. With the sense-resistance known, the output voltage of the difference amplifier might be divided by this current in the digital unit to obtain a current value.

The compensation process must depend upon past states regarding the grid current. Nonlinearities are most easily recognized in the frequency domain. As frequency is the inverse of time, time-varying data is necessary to manipulating the signal in the frequency domain. Thus the information delivered to the Digital Processing and Controls unit must be conducive to conversion into discrete time-samples that allow some precision in analysis.

Calling back to the sampling theory, the signal presented at the output of Analog Preprocessing must be bandlimited to the highest supported frequency of the compensator, *at most* half of the sampling frequency. To ensure this, an analog lowpass filter must precede sampling, in-order to condition the signal to be sampling friendly.

Total elimination of certain frequency components is usually not possible, but sufficient mitigation will be close enough to prevent prohibitive aliasing. An active filter (using operational amplifiers) is recommended, instead of passive (relying on resistors, inductors, and capacitors), as this unit's low power environment permits their use, and they usually enjoy significant power-loss advantages over passive filters.

The circuit diagram for this stage of the process is pictured below, attached to a copy of this project's simulated test grid assembled in the SimElectronics and Simscape Foundation Libraries.

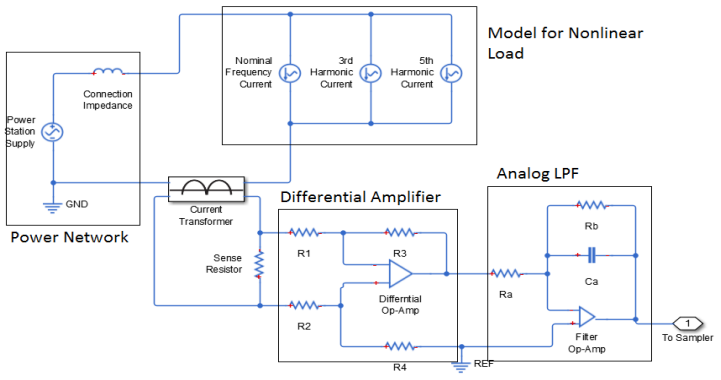


*Figure 25:Proposed Circuit Schematic for Analog Preprocessing*

The differential amplifier is connected in such a manner to output a voltage proportional to the current through the Sense Resistor, at the same polarity as the grid current it is involved in sensing. The lowpass filter, however, inverts the signal. This is acceptable as ultimately it is the inverse signal that must be delivered, and the inversion would need to be performed, if not here, then at some later stage of the compensation process.

#### *3.1.2.1 Within the Project Scope*

This is all essentially moot in the context of the work done for this project. This system was conceptualized in the early days of the project, but never fully designed for a duality of reasons. First, it is more application-specific than any other unit in the project, which seeks to design a process to achieve its goal in a more generalized range of applications. Secondly, it proved entirely unnecessary in the simulation environment.

The functional simulation equivalent can be designed with one or two blocks depending on the libraries used, and the continuous-time signal format one hopes to see at the Analog Preprocessing block's output. Functional equivalents in the Simscape electrical environment is shown below.

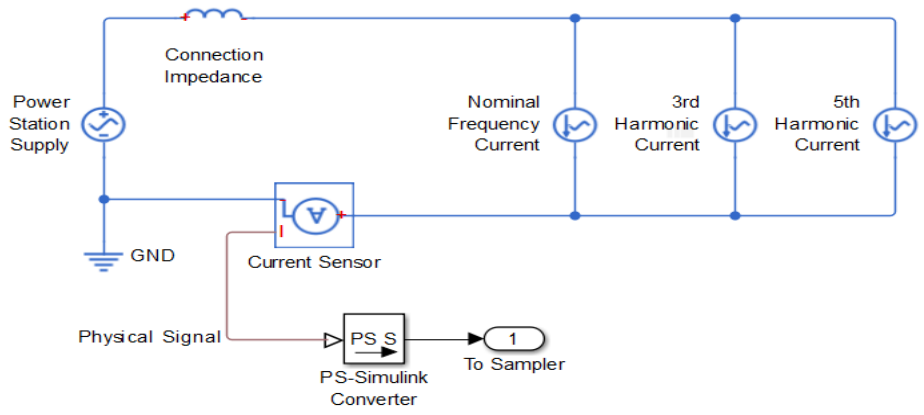


*Figure 26: Reading Grid Current in SimElectronics Environment*

The current sensor outputs the current as a “Physical Signal” type, which is then converted into a more standard Simulink continuous-time signal.

Another environment frequently used in this project is one only used in Simulink’s “SimPowerSystems” → “Specialized Technology” sub-library.

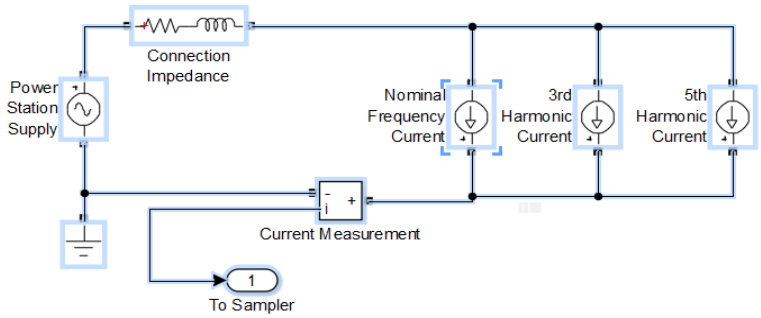


*Figure 27: Reading Grid Current in "SimPowerSystems" --> "Specialized Technology" Environment*

The only action detailed in the realization, but skipped in simulation, is filtering. As the nonlinear load used here only displays current at three relatively low frequencies, aliasing was no issue provided that sampling was performed at a rate of 700Hz or faster.

### 3.1.3 Digital Processing and Controls

This is the block that performs any cognitive digital processes needed to achieve precise compensation. The tasks required from this unit are:

- Sampling processed grid current and voltage
- Accurate isolation of current behaviors resulting from load nonlinearities
- Calculating integrity indicators for resulting waveform
- Making integrity-based determinations
- Determining state at which to operate the Power Delivery block

- Generating operating signals for Power Delivery block
- Interacting with Output Monitor Triggering

Only two real design question are present in sampling. The first, which system values to sample, is a parameter of the process used in compensation. The second, how often new samples should be obtained for each indicator, or each signal's sampling frequency, is a question more relevant to the environment it is intended to operate.

For the project, the utility of digitally attaining each of three variables was closely considered. The three variables were the current in the grid, the voltage in the grid, and the current delivered by the compensator. The determination regarding which to sample was based on where they were needed in the system, the benefit different system blocks might receive by their inclusion, and the time-sensitivity of the system component functions that would operate on these variables.

Grid current, the target variable, is non-negotiable. Digital operations were required on the basis of this metric, and thus sampling was of the utmost importance.

Grid voltage seemed too low-frequency to attain for digital determinations. It was later realized that the decision engine would ultimately need a digital representation of this variable for H-Bridge state determinations.

Compensator current was more complicated, as the Output Monitor Triggering relied on this variable. As is later to be seen, an even partially implementation of this variable involves sampling of either this particular variable, or some derivative thereof. An analog implementation, however, requires only an interrupt-enabled port or digital logic circuitry. As interrupts typically arrive along general-purpose input, or GPIO, ports, sampling would be ultimately unnecessary in this case, and the time-sensitivity involved in control of the transient states used would be better addressed if an analog

representation of this variable were available for processing, regardless of whether or not it were sampled in addition.

The question of sampling frequency is, as has been mentioned, directly application and hardware specific. Tradeoffs are involved in both lower and higher sampling frequencies.

Benefits of higher sampling rates include:

- Greater supported frequency range.
- Higher sampling rate mitigates impact of group and sample delays.
- As much of such a system could be forced to wait for samples at run-time, a higher sampling rate could improve response-time.

Benefits of lower sampling time include:

- Greater isolation filter complexity or consequences.
    - The critical filters employed in most designs have incredibly narrow selective or distortive bands.
    - Higher sampling frequency requires either higher-order filters, or far greater floating-point support, to capture such narrow responses.
        - Higher floating-point requirements jeopardize stability on less powerful computing platforms.
- More-fitted sampling frequencies place very manageable strain on any embedded system, while those high enough to be considered ubiquitous for any load encounter filtration difficulties and place very unnecessary strain on Digital Processes and Controls Units
- FFT buffers must be far greater (increasing response-times) for all buffering algorithms involved or considered.

In the sampling frequency decision, it is important to calibrate to consider not just the frequencies generated by the nonlinear load in isolation, but also other factors in the physical network. The switching times on the bridges effect how steep transitions might be in delivered current, introducing the frequency information of bridge state transitions of various magnitudes and shapes. The switching intervals also control an effective switching frequency. Given rapid transition intervals, current spikes occur over less time, and the Output Monitor Triggering responds with greater immediacy, in turn leading to a more imminent repetition of this cycle. Thus frequency information is inserted into the continuous-time frequency spectrum at a location inversely proportional to the unfixed periods of this cycle.

There are several ways to approach frequency selective models for wave isolation, the most simplistic method is a base-elimination, consisting of a single notch-filter, a particularly targeted implementation of a bandstop filter.

As this block utilizes a digital filter, important design parameters include sample rate (which should be consistent with that of the preceding and subsequent blocks), some filter-type dependent combination of passband or stopband, the gains of each band, and the filter's order and type. Design targets and consequences include the filter's magnitude response, group delay, and transient characteristics, as well as stability and floating point demand.

### 3.1.4 Controls Units

These are the blocks that perform any cognitive digital processes needed to achieve precise compensation. It must take preprocessed analog signals, representing physical quantities present within the physical network, determine what current should be delivered to the circuit, determine the method of control as well as implement such control for an analog device delivering this power.

Important design targets and consequences for this process are accuracy, signal propagation delay, and response time, and signal-shape retention at output. Accounting for lagging signal and group-delay effects was a significant focus in this project.

Too significant of a time-domain offset could lead to only partial cancellation of the current marked for elimination, or in extreme cases, the doubling of such undesirable currents. Group delays, the time it takes the amplitude envelope of a signal's frequency components to propagate through a system, could significantly reshape the wave being used for control of the compensator if it is too harshly varied in the system's response spectrum.

Furthermore, if a system is too slow to stabilize when presented with unexpected information, it could provide output that has failed to adjust, and feed that into the system causing further physically damaging effects, in addition to entering an operational state, where the device is compensating for what it intends to keep present, and ultimately fail to isolate the nonlinear currents from the nominal frequency of the network.

Individual tasks required to accomplish the process's desired functionality remain constant, yet their implementations may differ. The three primary objectives of the processing and controls block are:

- Target generation
- State determination and gate-firing
- Output monitoring and control

Target generation is the process of calculating a numerical representation, in real-time, of the current to be delivered by the compensator. The result must suffer from limited time delay, and maintain the shape of the wave as accurately as possible. Thus it follows that this function must

produce phase-shifting and time delay effects, and passband gain of a negligible order. If base process effects do not meet these requirements, these side-effects must be corrected.

State determination, or the decision engine, must produce the identity of a scheme, within a set of those supported, to be applied to the power delivery unit, accounting for both the target and relevant environmental states. The gate firing component of this process converts these states to the physical outputs required by the delivery unit to deliver the target.

Output monitoring and control structures are included for the purposes of safety and highly-responsive and effective operation. A necessity exists for the delivery unit's supply to possess a far higher voltage than that applied to the load. This, coupled with the rapid switching intervals of IGBTs, create highly-volatile potential to drastically overshoot the target current if delivery is ignored for too long of a period. Thus, more sensitive monitoring of compensator current is mandatory if one desires to create an accurate compensation process.

One such example unit, utilizing a base-elimination technique, a transience controller, and for monitoring purposes, a PWM controller, can be seen below.

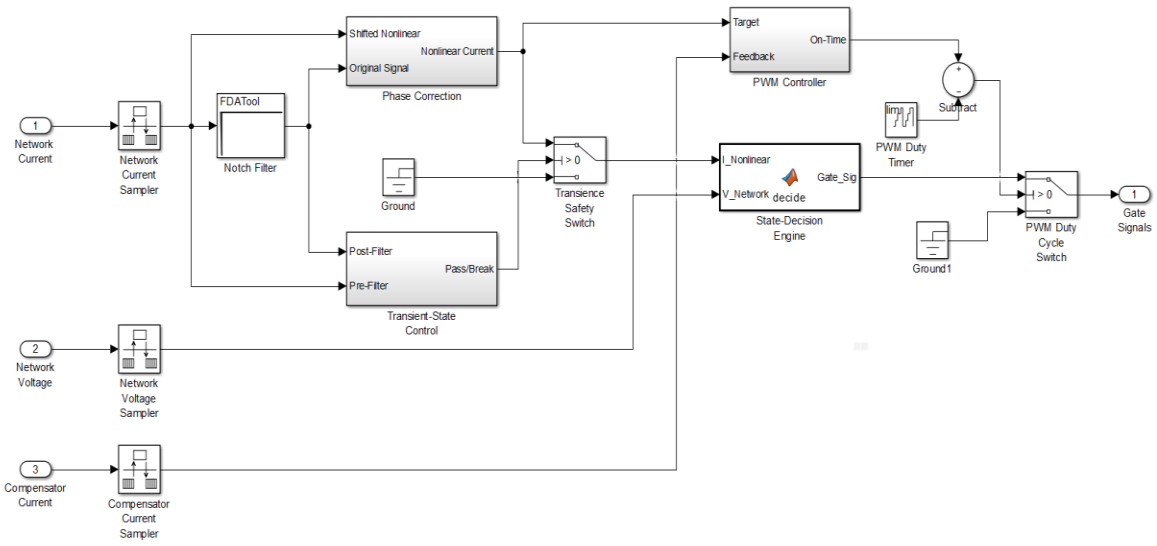


*Figure 28: Processing and Controls Example, Uses Notch-Filter Base-Elimination, Preemptive Transience Measurement, and Pulse-Width Control System*

### 3.1.5 Power Delivery

The only devices able to serve as the anchor, around which this block might be built, are H-bridge configurations of IGBT/Diode pairs.

Design decisions considered for this block were:

- What bridge operating states are to be supported?
- Is there benefit derived from use of multiple bridges?
- How should one or more bridges be configured?
- How should bridges be powered?
- Charging of bridge supply.

### 3.1.6 Output Monitor Triggering

This block provides increased real-time control of bridge operation. It ensures that compensation fits the target within a tolerance.

Design decisions included:

- Analog vs. Digital
- Two boundary (window) comparison vs. precise target matching.

## 3.2 Finalists

### 3.2.1 Analog Preprocessing and Analog-to-Digital Conversion

Analog preprocessing was deemed to be largely outside the scope of this project, undertaken by a single engineer with limited analog engineering ability. As work for this project was done entirely in Simulink, simple sensing blocks, shown in Figure 26 and Figure 27. For realization of the finalist model, refer to Section 1.1.1, and the system shown in Figure 25. The general scheme has been developed, but much calculation to realize a practical design remains to be done.

### 3.2.2 Power Delivery

It turns out, that for a bridge converter in an AC environment, several more operating states exist, supposing that the converter is supplied by a floating (ungrounded) voltage greater than the load's voltage amplitude. The new states introduced for this control scheme are referred to here as "short-states". With these four gate-control signal configurations, it is possible to provide a low-resistance path to ground from the AC power line. Each are polarity dependent, and use only a single active transistor. For each polarity, one is confirmed as operational, and the other is theorized but unconfirmed options within the scope of this project.

Not many configuration options truly exist for this block aside from which IGBTs and diodes to use, either in implementation, or in simulation[5], and the parameters of the devices. The final design simulation uses separate IGBT and diode blocks from the Simscape Power Systems Library. Due to performance difficulties at adequate sample step-sizes in Simulink, the design gives takes advantage of the opportunity to pass unrealistic parameters to the IGBT block in an attempt to prevent transitions too sharp to be detected given a lowered time-resolution.

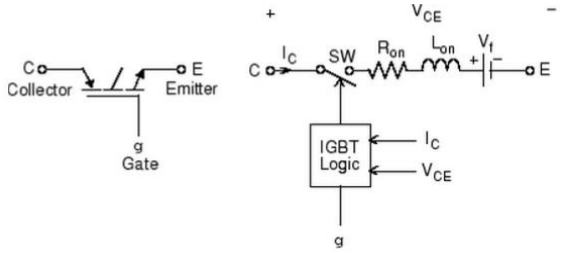


*Figure 29: IGBT Block Reference and Equivalent Circuit*

The resistance, $R_{on}$ has been set to a level unreasonably high (for an IGBT), contrary to the objective of minimal power loss, to mitigate the consequences of overshooting the target delivery current in switching transitions. The same has been done with the inductance, $L_{on}$, compromising the same objective (for simulation purposes) to prolong the turn-on transition interval, and therefore reduce the potential for overshoot.

Numerous options were considered for the bridges supply. These included the rudimentary DC supply, a pre-charged capacitor, and an inductor. The capacitor would have been ideal, considering no reliance on easily spent or over-cycled chemical energy storage techniques existing in a battery, and as such, potential for more frequent manual replacement. As the final design is simply a simulation in which such considerations need not be considered to show concept, and insufficient time was available

[5] Simulink has four IGBT and IGBT Diode blocks, as well as H-bridge, full-bridge, and half-bridge (one vertical pair of a full-bridge.) One has been shown unequivocally to shown to not be suited to simulation of this application. Almost all others are suspect. Only one has proven validity for proof of concept simulation.

to provide a truly functional design, determination of the necessary states to keep the capacitor sufficiently charged, and their integration into the design's decision-making process, was not attempted.

The DC voltage supply, however, does have associated requirements. If it is too small, it will not be effective in a large-amplitude environment, not only because of its inability to actively deliver current if the voltage at output is higher than what it might, itself, supply, but because stronger voltage at the rail will enable the following states, the first for excessive positive power-line voltage, and the other for negative. The active paths for current are traced with red arrows, and the semiconductors passing current are underlined in red.

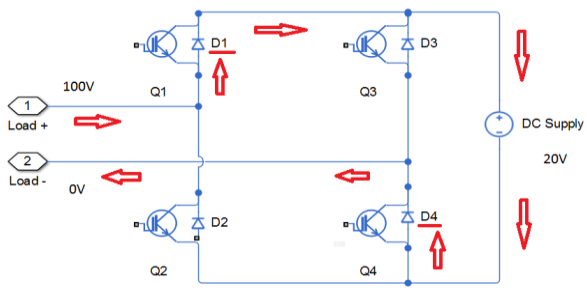


*Figure 31: Current Path Through Bridge Diodes for Insufficient Supply, Positive Network Case*

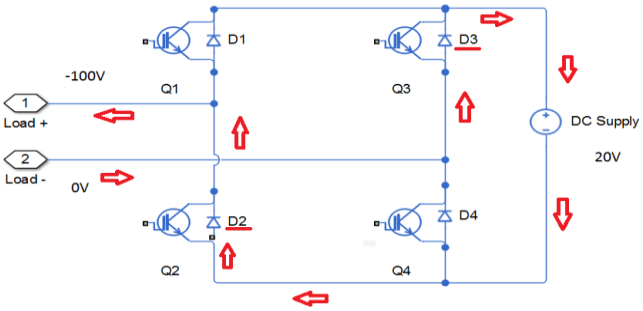


*Figure 30: Current Path Through Bridge Diodes for Insufficient Supply, Negative Network Case*

Thus the supply must be sufficiently large to deliver the necessary current to the grid for the largest expected voltage value given the internal resistance of the bridge. This value must certainly larger than the amplitude of the grid voltage. However, it must not be so large that the switching transitions in the delivered current scale too quickly to be detected and addressed before they exceed tolerable levels and do damage, if not to the device, then to the controls state, introducing numbers of scale that it cannot return quickly, or at all, to acceptable amplitudes. In such cases, the excess current

perceived by processing will be drawn from the supply to match what the controller is demanding for delivery

The final piece of configuration has been partially encompassed by the IGBT model. This component is a series inductance, and possibly a very large parallel resistance. The inductor, and possibly the resistor, serve to reduce the extremity of the current spike at switching-time. The functional model is a lowpass inductor, resisting the higher frequency components involved in the very high-frequency transitions. This component, and the magnitude of the supply voltage, however, remain one of the most unresolved of the final design, with many simulations having been run towards the end of the project to determine what values provide any amount of accurate, smooth, and reliable compensation.

For the Specialized Technology IGBT blocks, gating signal is a simple 0 for off, and 1 for active. Other IGBT simulation blocks, and actual IGBTs, require the emitter-following gating circuits if they are to be controlled digitally, or by other low-power signals.

#### *3.2.2.1 The Short-Circuit States*

There are four short-circuit state. Each polarity of the power-line voltage has two, a high-side and a low-side, each using a different set of semiconductors, and taking advantage of the floating nature supply. Ideally each short-circuit state operation for a given polarity would switch usage between the two, thus distributing the power dissipation between the two separate semiconductor sets in an effort to avoid overheating.

The final design's implementation solely in simulation, however, meant that the thermal characteristics of physical devices were essentially irrelevant to establishing proof of concept. Validity concerns regarding the high-side states were present, due to the current being directed from power-line to ground, or vice-versa, through a node shared by the positive lead of a battery exceeding the

amplitude of the voltage. These theoretical and supported but untested current paths may be seen below.

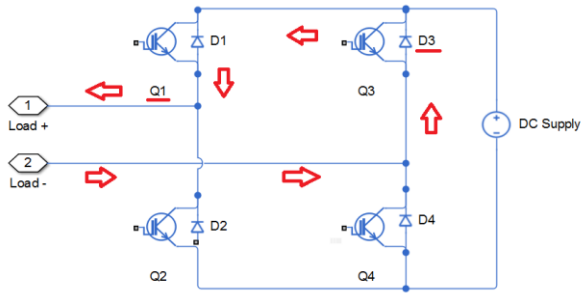


*Figure 32: High-Side, Ground to Power-Line Current Path*

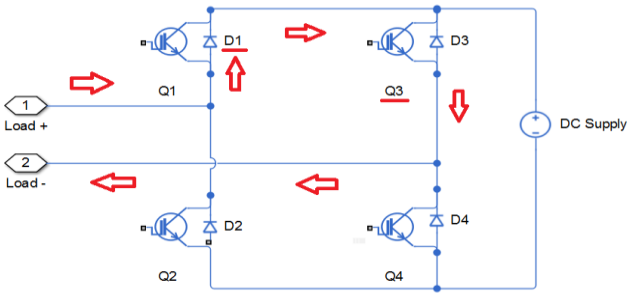


*Figure 33: High-Side, Power-Line to Ground Current Path*

Those actually implemented also direct current from ground to the power-line, and from the power-line to ground, and share a node with the battery's negative lead.

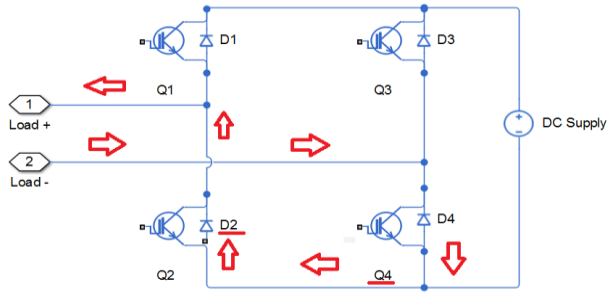


*Figure 35: Low-Side Short-Circuit State, Ground to Power-Line Current Path*

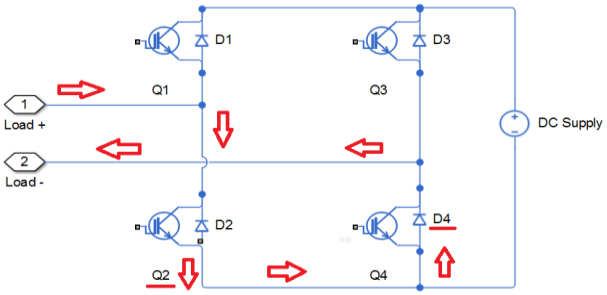


*Figure 34:Low-Side Short-Circuit State, Power-Line to Ground Current Path*

Due to the nature of the abrupt switching transitions, the delivered current must be monitored, and means should be implemented to disable it when it leaves a target window (see Figure 14.)

#### *3.2.2.2 Simulation Implementation of Power Delivery*

This simulation uses the IGBT block found in the "Specialized Technology" library of the *Simscape Power Systems* library. It was selected on the suspicion that it may be the only IGBT block matching the requirement of (indirectly) adjustable and/or calculable turn-on times, which might be switched-off while the transistor transitions to its full conductivity. This was observed to not be taken for granted, as the documentation for the *Simscape Electronics* library's N-Channel IGBT model

(depicted as blue in example diagrams in this document) states that "A minimum pulse width is applied when turning on or off; at the point where the gate-collector voltage rises above the threshold, any subsequent gate voltage changes are ignored for a time equal to the sum of the turn-on delay and current rise time." [11] It is coupled with a diode from the same set. The IGBT in use's gate takes an input "1" to open the channel and "0" to set it inactive. The "Q_logs" and "D_logs" ports do not affect control but provide a handle by-which to record transistor and diode voltage and current information.

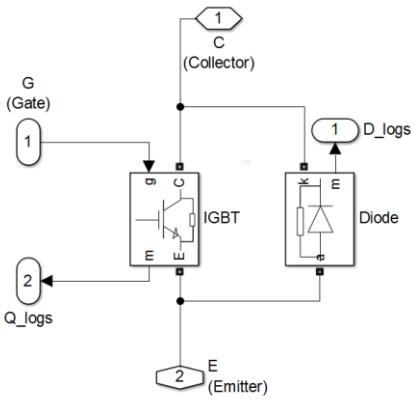


*Figure 36: IGBT/Diode Subcircuit in Power Delivery Bridge Converter*

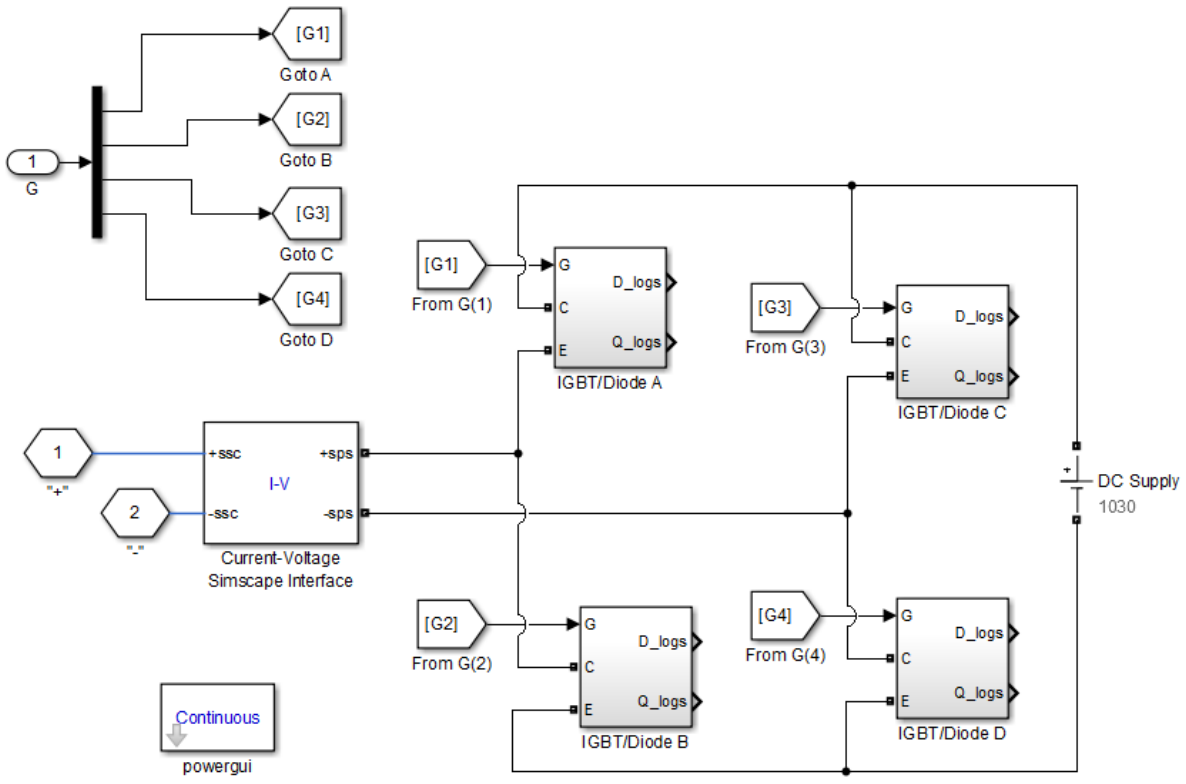


*Figure 37: The Bridge-Converter Simulation Configuration*

Four of the sub-circuits in Figure 36: IGBT/Diode Subcircuit in Power Delivery Bridge Converter are used to construct the needed bridge converter in Figure 37. The supply voltage at time of authorship was 1030V, but this has been subject to change as it is one of several variable being altered for the sake of stable compensation.

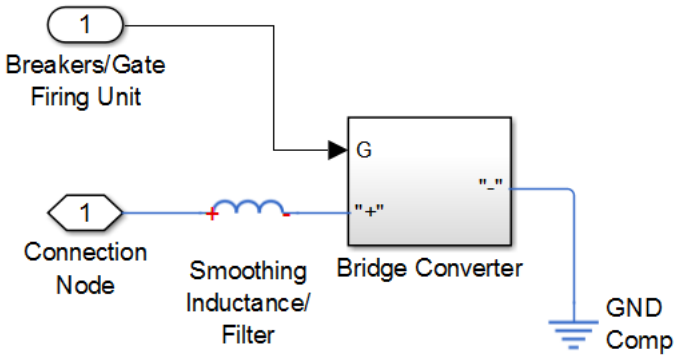


*Figure 38: Simulation Diagram of Bridge Converter's Connection to System and Environment*

### 3.2.3 Logical State-Decisions: The Decision Engine and Gating Codes

The logical decision-making in the final design is quite simple. It determines what state the H-Bridge may occupy to move current in the desired direction for a short-circuit or active-delivery target. It then encodes the state into a four-bit gating signal.

The required inputs for state determinations are simply the voltage at the load and the current which it is drawing. To minimize power loss, it makes sense to preserve the energy stored in the supply. This is achieved by maximizing utilization of the Power Delivery short-circuit states, in which power is not drawn from the supply.

The desire for frequent short-circuit is not always realistic however. The polarities of the voltage at the connection to the load and the polarity of the delivery current dictate whether or not this

is possible. Each must be opposite the other, as it is impractical to draw current from this connection to ground if connection node possesses negative voltage with reference to ground. Any short-circuit states which could produce a path for current, excluding the supply, in such a case would deliver current to this connection node, from ground, as current flows from the greater voltage to the lesser. The same holds true for the case where current must be delivered to the node with positive voltage polarity. Any active short-circuit paths would draw current from the node and bring it to ground.

Thus, in the cases where the sign of the current, with a reference direction leaving the compensator, and the sign of the voltage at the connection node are the same, current must be delivered from the supply. If the signs are opposite, short-circuit is possible.

In the implementation, five integer state-handles were defined, one for the "idle" state, or open circuit across the compensator, one for active positive delivery, one for negative active-delivery, one for a node-to-ground short-circuit, and the last for a ground-to-node short-circuit. The state-descriptions, ID integers, variable handles (MATLAB doesn't provide easily accessible use of macros) used in the decision code are listed in Table 2. The equivalent logic diagram using these handles and IDs, is provided in Figure 39, with the states depicted in green.

| Description | Handle | ID Value |
|---|---|---|
| No current delivered or drawn from grid, Compensator Current ≈ 0 | IDLE | 0 |
| An active delivery path to deliver positive current. | PUSH_POS | 1 |
| An active delivery path to deliver negative current. | PUSH_NEG | 2 |
| A passive delivery path to short current from ground to the node | PULL_GND | 3 |
| A passive delivery path to short current from the node to ground | PULL_NODE | 4 |

*Table 2: Decision State Integer Handles and Descriptions*

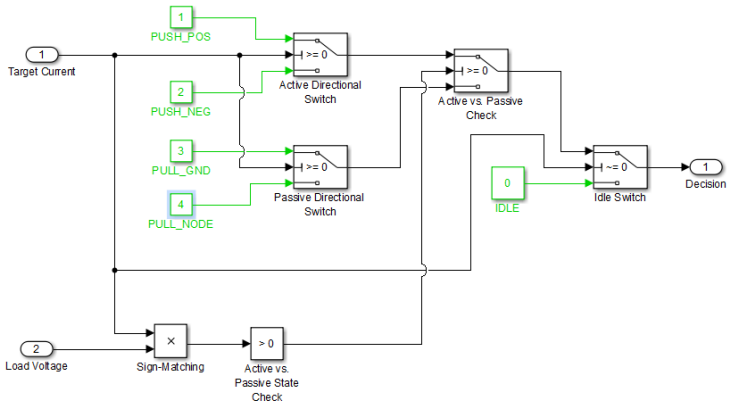


*Figure 39: Logical Structure of Decision Engine*

This is the gate signal block is that which directly deals with the gates of the transistors. In the final simulated design, it exists as a MATLAB function. Recommended implementation, however, includes digitally executed code, transistor logic, and analog circuitry.

The first and foremost task delegated to this functionality is to take the state determination and translate it into four binary signals. The four binary signals are represented in vector form, corresponding to which of the four transistors they signal. The format for representing these signals is [Q1, Q2, Q3, Q4], where, if a transistor is active, its $Q_x$ is replaced with "1", and "0" if the transistor is to be inactive.

| Decision Engine Handle | Gate Encoder Handle | Target Polarity | Voltage Polarity | Gating Signal |
|---|---|---|---|---|
| IDLE | gOPEN | 0 | x | [0, 0, 0, 0] |
| PUSH_POS | gFWRD | 1 | 1 | [1, 0, 1, 0] |
| PUSH_NEG | gRVRS | -1 | -1 | [0, 1, 0, 1] |
| PULL_GND | gSC_G2RL | 1 | -1 | [0, 0, 0, 1] |
| PULL_NODE | gSC_R2GL | -1 | 1 | [0, 1, 0, 0] |

*Table 3 Gate Encoding for Each Implemented Decision:*

The second purpose of this function is to respond to outputs from certain blocks involved in monitoring the operations of other units. Certain such blocks, to prevent entrance into difficult-to-

escape states that may hamper the function of the device, often signal this block to idle the compensator, passing only zeros. In the final design produced by this project, this operation is performed by a block of MATLAB code. In physical implementation, for purposes of speed, particularly concerning independence from digital clock cycles, it is recommended that this portion of Gate-Signal Control be performed by transistor logic circuits with negligible band limitations, due to the high-rate of indicator switching output by one such monitor.

The final design takes two such signals. One indicates whether or not the isolating filter can be trusted, signaling a "1" if it cannot. The other indicates whether or not the output of the Power Delivery unit exceeds a tolerable range, signaling a "1" if it cannot. This implementation can be achieved with a single, three-input AND gate before each emitter-following gating circuit or simulation IGBT.

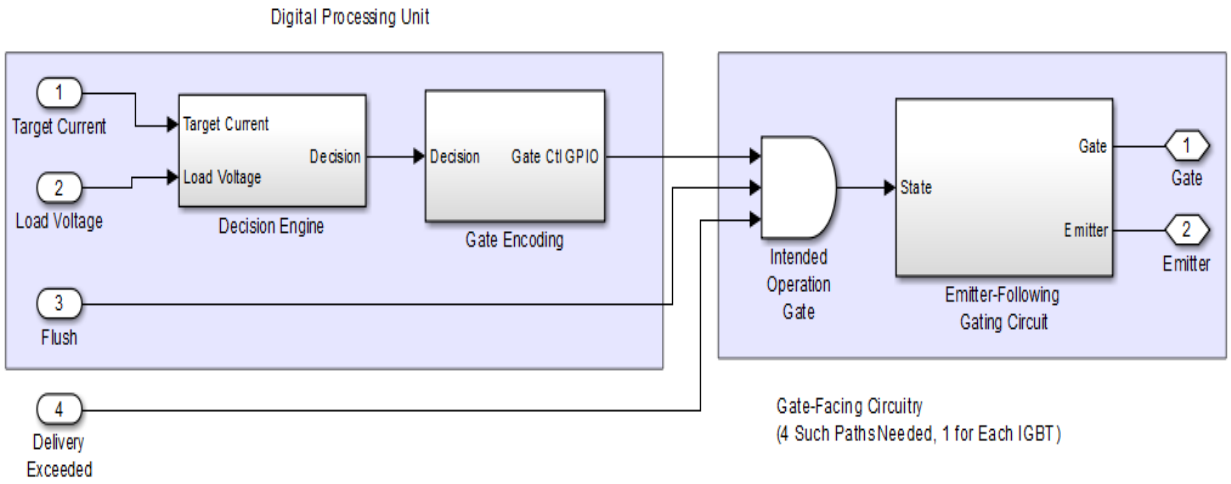


*Figure 40: Proposed Physical Implementation of Logical Decision Making and Gate-Signal Generation and Control*

The block's implementation is presented in Figure 41.

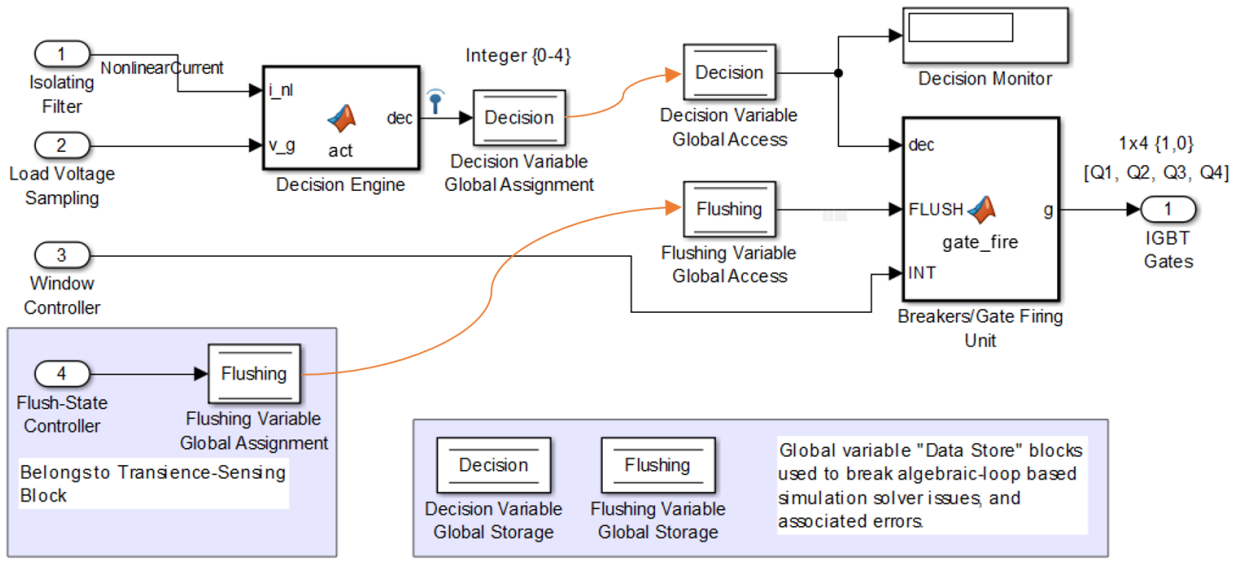


*Figure 41: Simulation Implementation of Decision-Making and Gate-Signal Generation and Control Units*

As the gating circuits are unnecessary with the IGBT blocks in-use, and the minimal detail removed by implementing the AND gate in MATLAB code, all aspects of the Gate-Signal Generation and Control unit have been absorbed into either the IGBT or the Breakers/Gate Firing Unit MATLAB function block.

With direct connections of different implied or set sample-times, and when minimal-delay feedback loops connected, Simulink can encounter algebraic loop errors. Intense computation already a near-prohibitive factor in speed of simulation and data-collection, sometimes Simulink must be aided in not taking the most difficult solution by requiring it to explicitly store to global data existing outside the control flow that the reader can access whenever it executes. This is the purpose of the data store read, write, and memory blocks.

The code for these blocks is detailed below:

```
function dec = act(i_nl, v_g)

%% Decision Commands
IDLE = 0;           % Breakline Equivalent
```

```
PUSH_POS = 1;        % Ground -> Supply -> Rail
PUSH_NEG = 2;        % Rail -> Supply -> Ground
PULL_GND = 3;        % Ground -> Rail
PULL_NODE = 4;       % Rail -> Ground

%% Decision Logic
if(i_nl > 0)
    if(v_g >= 0)
        dec = PUSH_POS;
    else
        dec = PULL_GND;
    end
elseif (i_nl < 0)
    if(v_g >= 0)
        dec = PULL_NODE;
    else
        dec = PUSH_NEG;
    end
else             % Target Current, i_nl = 0
    dec = IDLE;
end
```

```
function g = gate_fire(dec, FLUSH, INT)

%% Decision Commands
IDLE = 0;            % Breakline Equivalent
PUSH_P = 1;          % Ground -> Supply -> Rail
PUSH_N = 2;          % Rail -> Supply -> Ground
PULL_GND = 3;        % Ground -> Rail
PULL_RAIL = 4;       % Rail -> Ground

%% Gate Signal Handles
gOPEN = [0 0 0 0];
gFWRD = [1 0 0 1];
gRVRS = [0 1 1 0];
gSC_R2GH = [0 0 1 0];
gSC_R2GL = [0 1 0 0];
gSC_G2RH = [1 0 0 0];
gSC_G2RL = [0 0 0 1];

%% Interrupt States
CATCH = 1;
RELEASE = 0;

cmd = dec;  % Starting Assumption

if (FLUSH==1) || (INT==1)  % Break Command Evaluation
    cmd = IDLE;
```

```
end

% Convert to Gate Signal
switch cmd
    case PUSH_P
        g = gFWRD;
    case PUSH_N
        g = gRVRS;
    case PULL_GND
        g = gSC_G2RL;
    case PULL_RAIL
        g = gSC_R2GL;
    otherwise
        g = gOPEN;
end
```

### 3.2.4 Nominal Frequency Separation

If the goal of this project is to correct current at all but a single frequency, then perhaps the most important task to be performed by the design involves obtaining an informational handle separating the two. The task should, ideally, be performed adaptively, allowing for amplitude fading and phase-shifting of the nominal frequency, which is to be allowed to exist, unhindered, in the state it occurs sans compensation. Yet all other frequency components of the network's current are to be marked for deletion.

In the final design this task is implemented by effectively attempting opposite of retaining the parameters of the nominals current. The information concerning the nominal frequency current and its parameters are passed through a filter targeted to select everything but that wave with strong parameter retention for the rest of the band. A notch filter, with a notch frequency of 60Hz generates the desired undesirable patterns with which to determine the current to be delivered by the compensator.

To get an accurate indication of the desired power delivery behavior, this unit must allow tolerably low, or absolutely no passage of 60Hz in any digital-signal representation of the load's current. The nonlinear portion of the signal should be maintained with near-unity gain, with minimal time-delay

or phase offset. When the nature of the signal changes, the filter should quickly adjust to steady-state conditions, characterized by the reduction of 60Hz signal to a tolerable magnitude. Low computational requirements are desired.

The filter employed was designed with aid from the Simulink FDAFilterDesign tool. A 6th-order Butterworth bandstop filter was specified for the sampling frequency of 10kHz. Low order was chosen to strongly reduce the band in which group-delay was greater than one sample (100μs). A narrow stopband, from 59Hz to 61Hz was specified to minimize the band in which group delay was present, and where observably disunity gain would be applied.

The Discrete-Time Fourier Transform r73epresentation of the resulting filter is:

$$H(z) = \prod_{k=1}^{3} H_k(z) = H_1(z)H_2(z)H_3(z) \tag{14}$$

$$H_1(z) = g_1 \frac{(1 - 1.9985793397849145z^{-1} + z^{-2})}{(1 - 1.9979010157116117z^{-1} + 0.9993628193182591z^{-2})} \tag{15}$$

$$H_2(z) = g_2 \frac{(1 - 1.9985793397849145z^{-1} + z^{-2})}{(1 - 1.99800113124215z^{-1} + 0.99938093856920296z^{-2})} \tag{16}$$

$$H_3(z) = g_3 \frac{(1 - 1.9985793397849145z^{-1} + z^{-2})}{(1 - 1.9973243836976358z^{-1} + 0.99874415184596688z^{-2})} \tag{17}$$

$$g_1 = 0.99968579145374092 \tag{18}$$

$$g_2 = 0.99968579145374092 \tag{19}$$

$$g_3 = 0.99937207592298338 \tag{20}$$

$H_1(z)$ $H_2(z)$, and $H_3(z)$ are each 2nd-order "sections" of the biquad-style filter $H(z)$, scaled by the gain parameters, $g_1, g_2$, and $g_3$ are scaled to match passband unity.

As this is an Infinite-Impulse Response (IIR) type filter, it is important to note how close the poles of this filter lie to the unit-radius of the pole-zero plot in Figure 42.

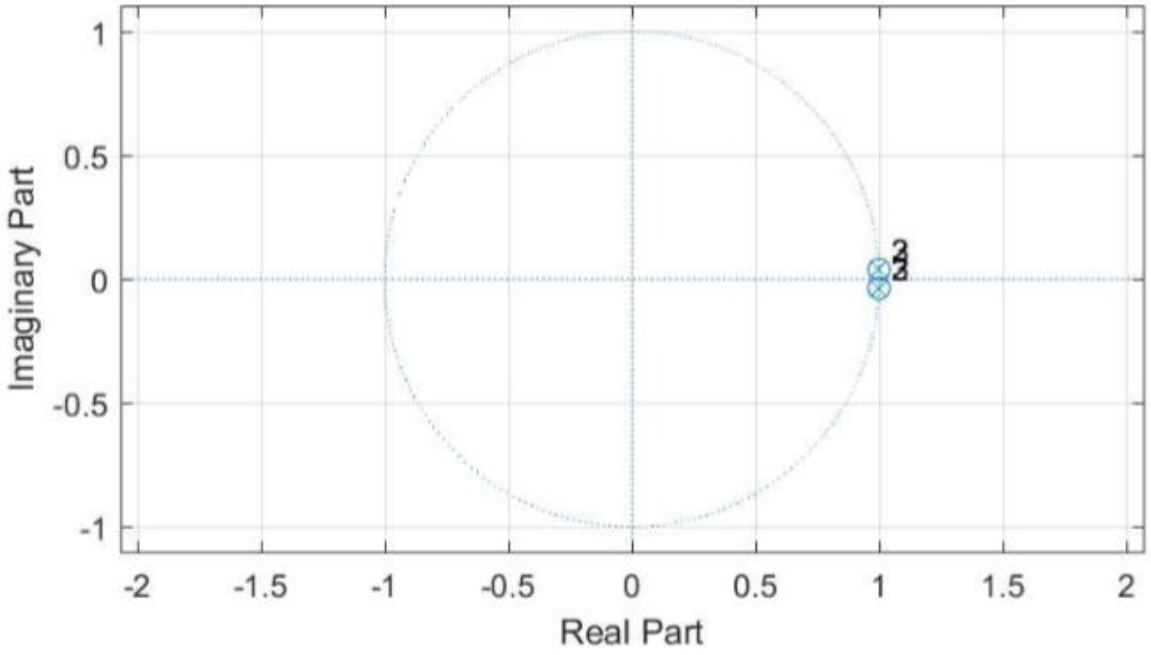


*Figure 42: Pole-Zero Plot of Nonlinear Current Isolation Filter*

As can be seen, all poles lie essentially on-top of the unit-radius at their angular positions. Thus it is critical to ensure, in future work, that the computational hardware of the controller be able to meet the floating-point requirements of the filter. This said, with the relatively-low computational load of the final design, most hardware for which floating-point support is not included should be capable of emulating this filter in real-time.

#### *3.2.4.1 Magnitude Response*

The magnitude response of the above filter appears highly desirable. It may appear to be a unity-gain allpass filter in Figure 43. This is not the case. The region of interest in this filter is 60Hz, displayed in a 5kHz band. Thus, drawing attention to the left, one can observe the sharp drop, almost discontinuous in appearance, as a blue sliver on the left-hand edge of the window.

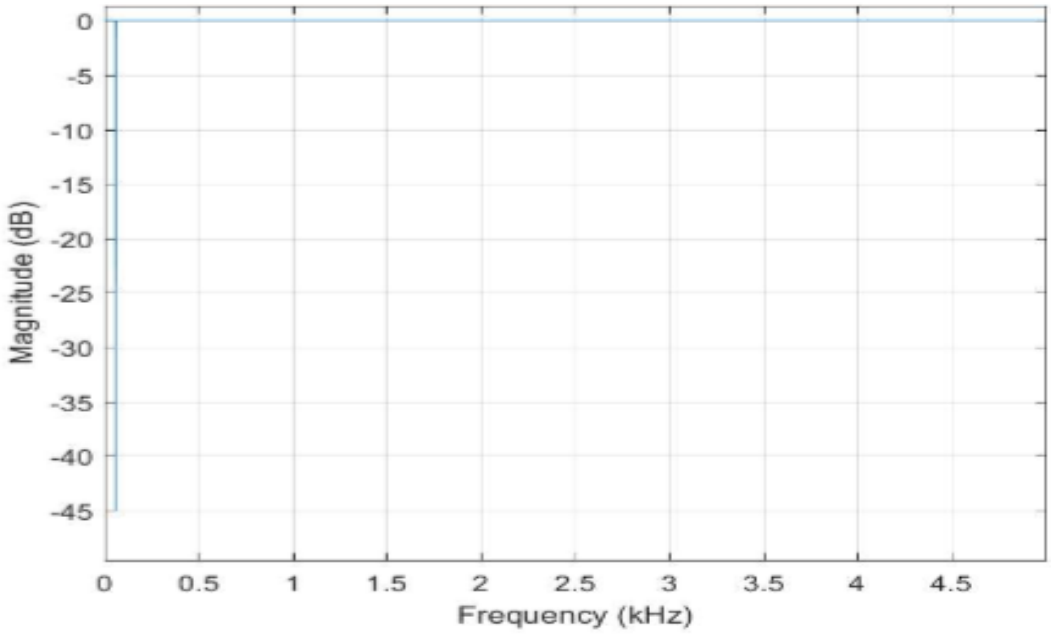


*Figure 43:Magnitude Response of Nonlinear Current Isolation Filter*

To obtain better detail as to the steady-state response, Figure 44 provides far greater detail on the magnitude notch band of the filter. The notch's minimum may be slightly off-nominal, but even if this is not attributable to a tolerance in resolution calculations, the 60Hz mark still coincides with a -39dB attenuation, tolerating passage of just over 1% of the nominal frequency current signal in steady-state.

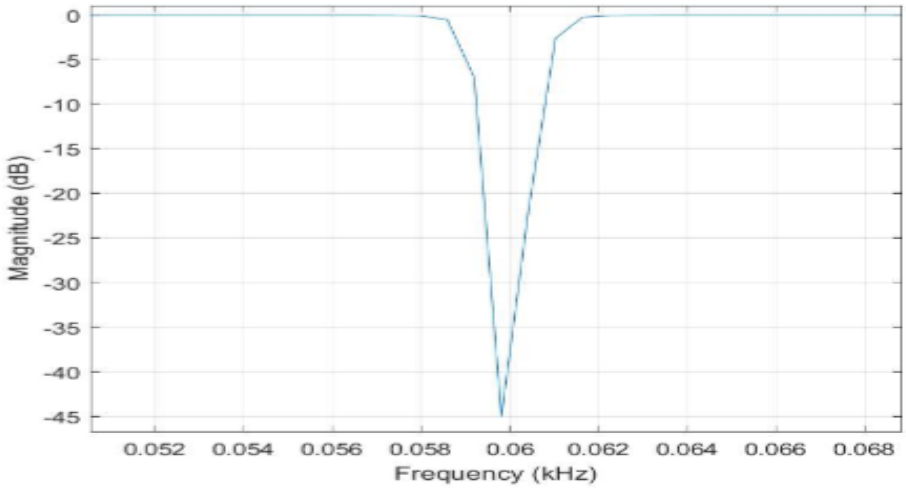


*Figure 44: Detailed View of Magnitude Notch in Nonlinear Current Isolation Filer*

The passband is re-entered within a very small window of error. A metric of reasonable return, --4dB or 63% is present at just under 59Hz, and at almost precisely 61Hz, with almost perfect return to unity by 58Hz and 62Hz.

The phase and time characteristics, of this filter in particular, are absolutely critical. The phase-response, is the frequency-varying additive contribution of the filter to the phase of each input frequency. The group delay, instead, measures the sample-delay in the amplitude envelopes for each output frequency, relative to that of the frequency at input.

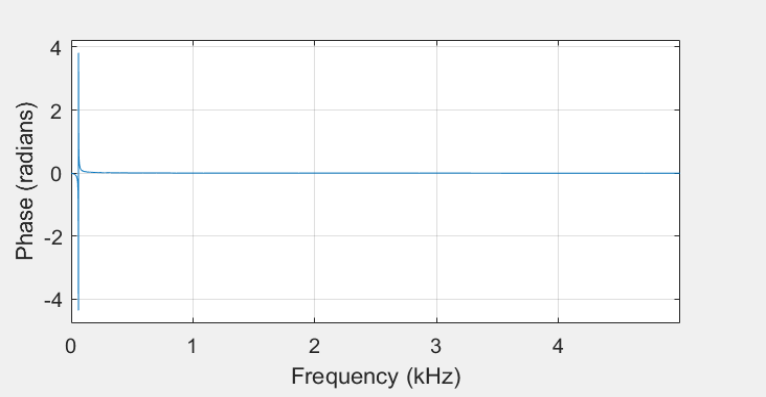


*Figure 45: Phase Response of Nonlinear Current Isolation Filter*

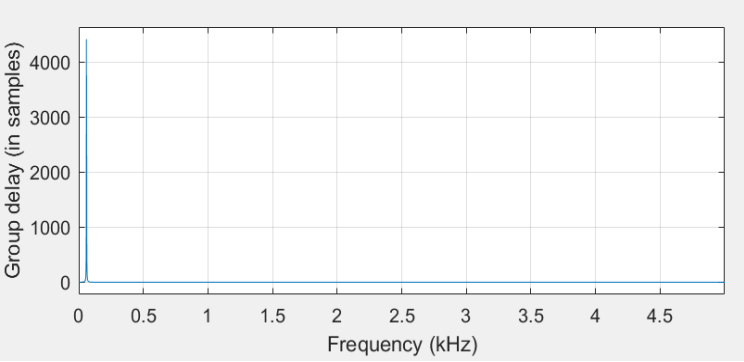


*Figure 46: Group Delay of Nonlinear Current Isolation Filter*

Time delay will ensure that compensation will always follow what the current was a fixed-interval before current conditions. The power delivered could be in a positive polarity despite the the

needs of the network having passed from positive delivery to negative delivery within that interval. Phase-offsets determine how well the system can know the phase of any given frequency component directly after filtration. Both vary with frequency, and thus both possess tremendous potential to fundamentally reshape the signal by shifting different frequency components to different degrees.

As this application is extremely shape-sensitive, it is critical that such effects be examined, and if they cannot be made negligible in this process, must be corrected for elsewhere. Thus, minimal and sharply bandlimited distortion of phase information was very highly prioritized in the design of this unit. The phase and time effects motivated the decision to use an extremely low-order filter at the cost of greater floating-point precision and a more dramatic transient response, which could be more-easily addressed. As with the magnitude response, the phase and delay are affected to a high degree, but only within an extremely limited band. This is very suitable to the signal-shape sensitive application.

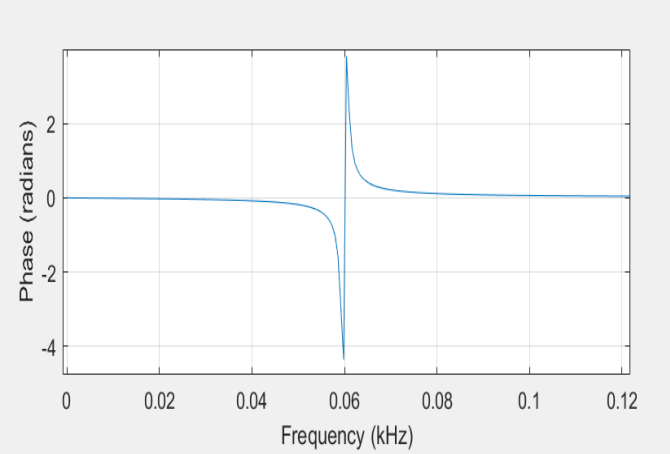


*Figure 47: Phase Response of Nonlinear Current Isolating Filter Scaled to Show Distortion Range*

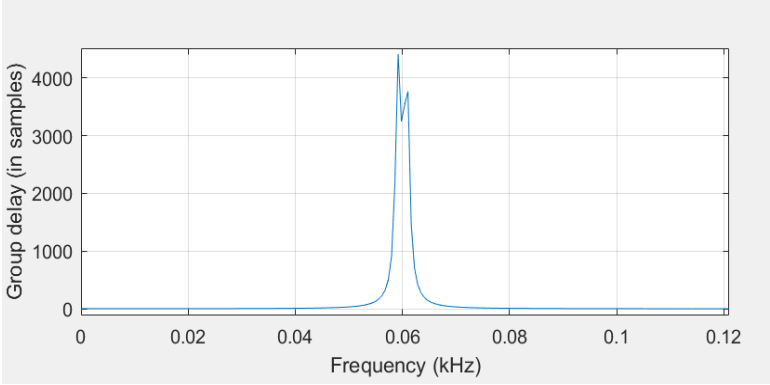


*Figure 48: Group Delay of Nonlinear Current Isolating Filter Scaled to Show Distortion Range*

Still, as in the test environment, the harmonics are tightly grouped above the nominal frequency, it is important to verify the phase effects and delay at the closest neighboring harmonics. In this case, the closest neighbor is 180Hz. Closer examination shows that any 180Hz output component leads the input component by 0.025 radians. Equivalent units are leads of 0.004°, 22.1µs, and 0.221 samples. Inspection of the group delay shows an amplitude envelope propagation lag of 0.277 samples. This is entirely acceptable for the application, as the phase-offsets and group delays continue to converge to zero at higher frequencies.

The significant offset and delay at 60Hz is considered trivial considering that, for this frequency, negligible signal should remain in the output at steady state. There are areas not eliminated which do exhibit more significant phase-shift and group delay. For instance, the band where group delay exceeds one sample is ends at 119.4Hz. There is no equivalent transition into the band, as it begins its spike from zero Hz at a 1.8 sample delay. The one-sample benchmark may be extreme for such low frequencies, as it translates into a 10µs delay, which is a 0.05 radian shift at the transition frequency

#### *3.2.4.2 Transience: Unit-Impulse and Unit-Step Responses*

In a set of experiments, it was shown that, even using an ideal delivery system, operating the compensator to deliver the output of the Nonlinear Current Isolating Filter from the first moment of simulation proved prohibitive to the elimination of the nonlinear current. The compensator would attempt to remove the 60Hz current in addition to the nonlinear current, and while the filter is designed to produce an output without that frequency, the delivery into the network from which the system was reading would push the nominal frequency back into the memory of the filter. Thus, the loop did not allow the filter the opportunity to suppress the 60Hz, a process which is not instantaneous in nature.

The behavior of the filter between the moment a new frequency appears in the input signal, to the moment that it is effectively suppressed in the output, or the filter's transient response, is thus of concern to the application. The transient interval should ideally be instantaneous, yet unfortunately this is very difficult to achieve. Through the FDAFilterDesign tool in Simulink, two options are available for analyzing transient behavior: the *unit-impulse response* and the *unit-step response*. These are generated by plotting time-domain filter output for what occurs when a unit-impulse function and unit-step function are introduced to the filter's input, in isolation, with only zeros being fed to the filter prior to the relevant function.

As both the impulse and step functions are linear, they do bear direct relevance to filter operation, even when other signals have been present for some time, the result simply being the output in their absence plus the impulse or step response, scaled, and shifted in time to whenever such a function is introduced. It is not certain which response bears more relevance to this application. The quick turn-on to turn-off time intervals, can be effectively modelled as impulses. But if any

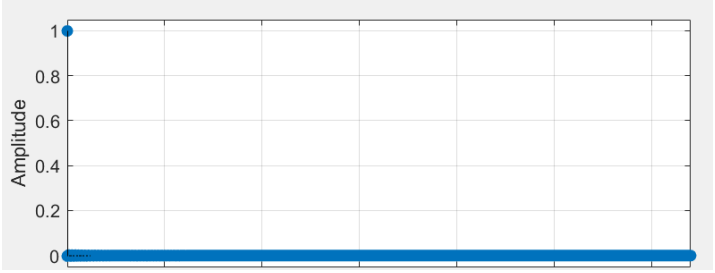

*Figure 49:Impulse Response of Nonlinear Current Isolating Filter*

periodicity exists in the pattern, or even more frustratingly, if new periodicities are introduced at any given moment, they may be modelled as a sum of each frequency component, scaling one or more time or sign-modulated step functions. The relevant model, determined here as an example, for dynamic switching interference, $n(t)$, is as follows.

$$n(t) = \int_{-\infty}^{\infty} \cos(2\pi f t) \sum_{k=0}^{\infty} a_{f,k} u(t - t_{f,k})\, df$$

For the purposes of this model, the first subscript uses an individual frequency as a unique handle for how many amplitude transitions exist for that component., and k corresponds to each step function involved in amplitude scaling.

Unfortunately, the ability to effectively minimize the transient response for this unit was given up on the sacrificial altar of a narrow frequency reduction and phase-distortion frequency range. This tradeoff, while justified, does come with complications, albeit perhaps the most correctible complications of any of the three concerned behaviors. While the impulse response is relatively tame as can be seen in Figure 49, the step response is, for a digital filter, quite protracted, as can be seen in Figure 50.

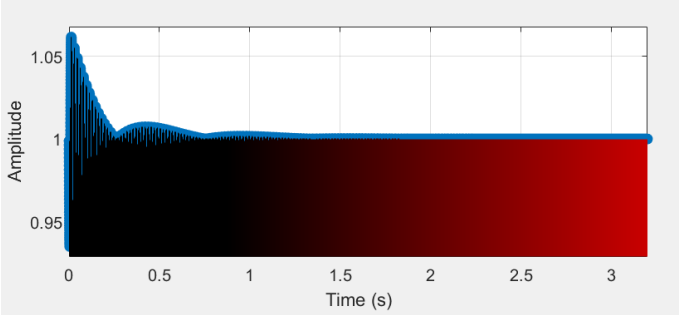

*Figure 50: Step Response of Nonlinear Current Isolating Filter*

The nominal-frequency relevant information for this filter can be better observed with an application-specific experiment in Section 4.1 “Filter Transience Experiment”, where the nominal frequency was measured to take 1.523 seconds to suppress 99% of a 60Hz waveform.

### 3.2.5 Window Comparison

Given the highly volatile power delivery it is necessary that systems be in place to detect and correct out-of-bounds delivery. This is done with a window comparison technique. The concept involves determining window boundaries, scaled to the target current. One is above the target the system is attempting to hit, and one below.

Given the rapid transitions in delivery current, this device must be far, far faster to provide precise control. Input availability to appropriate response timing is prohibitive to function if the delay is too great. Not only can overshooting the target present serious consequences to the load in the instance where it overshoots, but if timed incorrectly in can affect operation of the grid at any time after the error occurs. Should abnormally large currents occur in too many samples then they will pass all attempts at filtration, and be made the norm. If the samples are fed through the system, they will be delivered and appear once-more during sampling. These do not disappear, but routinely circle back through, and artificially scale the target windows. If the target windows increase in magnitude from what is justifiable, given their environment, then the bridge converter will attempt a larger magnitude of delivery, increasing both the power supplied by the battery, and that lost over the semiconductors in short-circuit operation.

#### *3.2.5.1 Recommended Implementation*

Implementation must occur in two pieces: generation and monitoring. The first may be implemented entirely in the digital realm, as it accepts as its parameter the target current, a metric which is only refreshed once every sample interval. Operational details might include the mathematical function used to scale the bounds above and below the target current to provide a range most suitable to the application. While many such scales exist, a linear scaling is the most intuitive and likely the most suitable. Use of a very small tolerance is preferred, but it is necessary to ensure that such a small

tolerance will not be overleapt by the Power Delivery unit before it has been registered and acted upon by this unit.

For this purpose, it is recommended that while the window boundaries be calculated digitally and output by a DAC, that all but the filter element of the Analog Preprocessing unit be implemented to monitor and scale the compensator current to within the DAC's voltage range, and passed, along with the DAC's output window boundaries, to a comparator circuit.

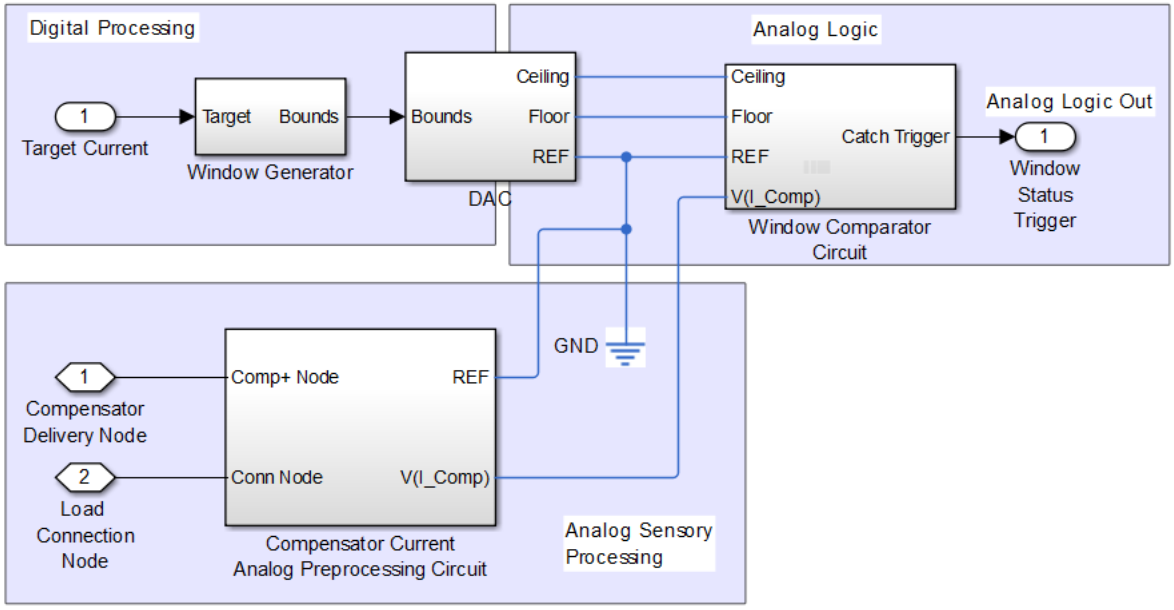


*Figure 51: Proposed Physical Implementation of Window Monitoring and Control*

As this block simply switches operation of Power Delivery between the gating signal, encoded elsewhere and already encompassing the polarity of delivered current, the instances in which current is both OOB (out of bounds) and drifting in polarity opposite the windows are rapid and unlikely. Thus a new subcircuit was introduced into the Compensator Current Analog Preprocessing Circuit, a Full-Wave Rectifier, to physically attempt an absolute value function of the compensator current, between the Current Transformer and Difference Amplifier blocks. The current transformer [12], full-wave rectifier

bridge [5], and difference amplifier [13] blocks are non-functional, and their icons were taken from online sources.

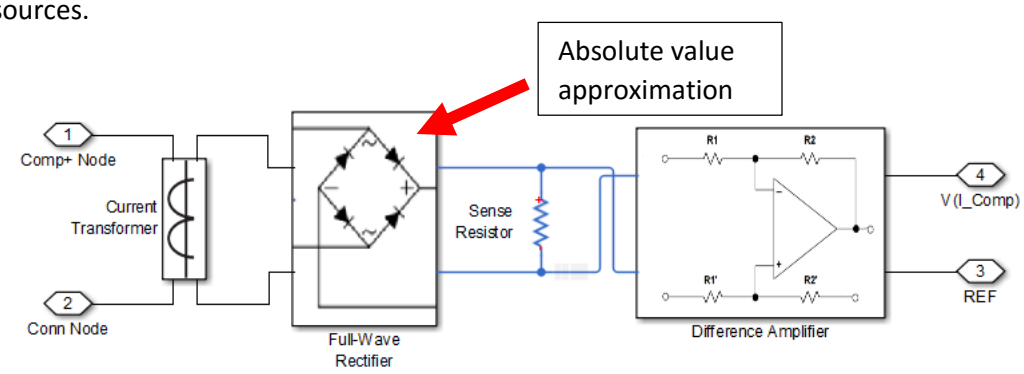


*Figure 52: Proposed Implementation of Analog Compensator Current Preprocessing*

To finish stripping this block of its redundant polarity inclusions, the window generation also includes absolute value functions and outputs the two figures as a vectorized output in the representation used in Figure 51. The leads of the difference amplifier are crossed to prevent signal inversion following the rectifier's absolute value effect.

### *3.2.5.2 Implementation in Simulation*

The requirements for this block are no different from above. The window-scale has varied across recent tests in an attempt to normalize functionality, but only between 1% and 2% linearly scaled tolerances.

$$ceiling = |target| \times \left(1 + \frac{tolerance}{100\%}\right)$$

$$floor = |target| \times (1 - \frac{tolerance}{100\%})$$

The window generator takes a single sample in digital representation of the target current as an input, and if it is double-clicked, a dialog appears allowing edits to its tolerance as the mask parameter "tol". Instead of vectorized outputs, two scalar values are output, one for the window ceiling, and the other for the window floor.

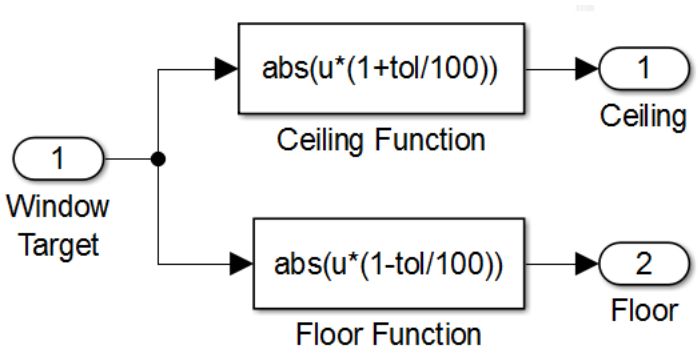


*Figure 53: Simulation Model for Window Synthesiizer*

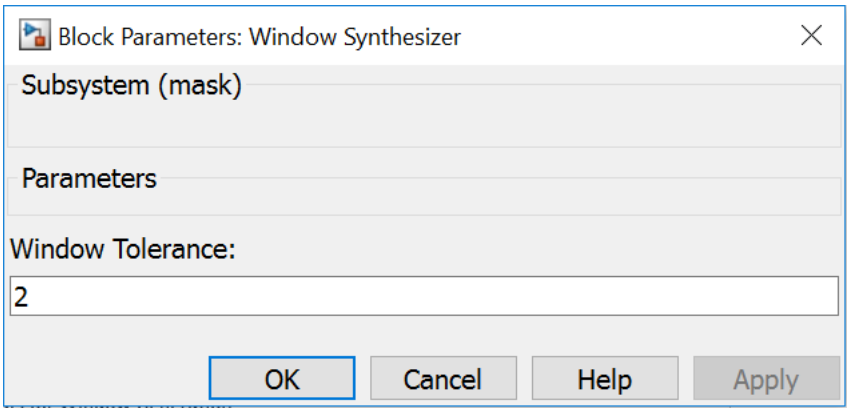


*Figure 54:Window Synthesizer Block Parameters Mask*

So far as timing requirements go, Simulink does not require circuitry models to perform logical and mathematical determinations in simulated continuous-time. These operations are between two blocks. Sensing and required scaling is performed by the "Compensator Current Acquisition" Subsystem, where logical determinations involved in window-checking are performed by the "Window-Comparison" MATLAB function.

Initially assigned-unit mismatches hampered the development of the window-check functionality when it was modelled as an analog circuit, namely a mismatch between a sensed signal in Amperes, and a block taking a voltage-assigned signal as an input. While this is no longer applicable, the

method used to circumvent these problems remains as an artifact, and introduces slightly more realism into the system.

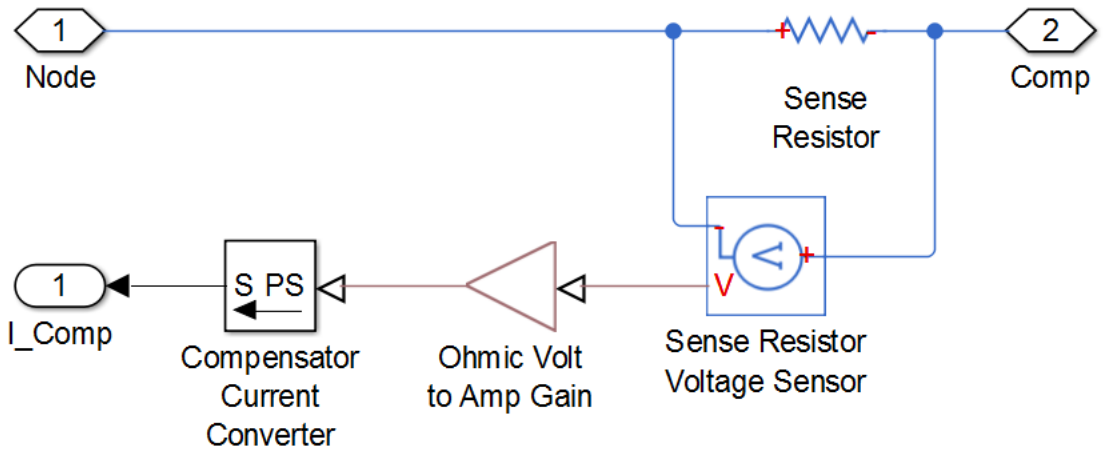


*Figure 55: Simulation Diagram of Compensator Current Acquisition Block*

Instead of directly sensing a current, this block senses the voltage across a small resistance (10mΩ) and multiplies this voltage by the inverse of the same resistance, obtaining the compensator current figure with an attached voltage unit. It then converts this physical signal to a Simulink representation which is passed to the Window Comparison function.

The Window Comparison function operates without modelled circuitry, but still in simulation-modelled continuous-time (which is still dependent upon and equal to the fundamental sample-time of the simulation.) Like the recommended physical implementation, the simulation uses absolute value of the targets and compensator current to gain logical simplicity.

The behavior targeted in simulation was for the Window Comparison to instruct a cessation of compensator current should its absolute value surpass that of the window's ceiling. Once this instruction is sent, it is to be maintained until the absolute value of the target current. The absolute value behavior is justified, in greater detail, in that the state-decisions are made over the same interval

that the window boundaries are calculated. The window monitor does not generate new decisions, but sends a break-command, which forces an idle-state regardless of what state-decision is currently active. Thus the current cannot move in the wrong direction past the zero-reference, and can only move in a direction counter-indicated by the active state-decision if a break command is active, and still only to an effective zero. This window crossing behavior is distinct from a reference crossing in that it is not automatically true or false because of where it stands in relation to a single reference. The break command's activity is dependent on which of two references it crossed last. Thus it must retain some implicit analog or explicit simulated memory.

In addition to this required state memory, this block also tempts the algebraic loop difficulties seen earlier in 3.2.3: Logical State-Decisions: The Decision Engine and Gating Codes. Thus memory is used extensively for both the "drift-state" (the reference to the last window boundary exceeded), as well as the window ceiling and floor, visible in Figure 56.

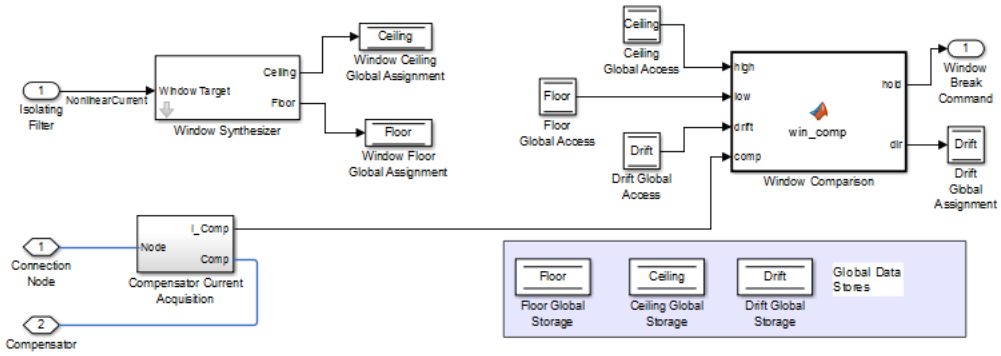


*Figure 56: Final Simulation Window Comparator Control Diagram*

### *3.2.5.3 Window Comparison Code*

```
function [hold, dir] = win_comp(high, low, drift, comp)

%% DRIFT STATES
RELEASE = 1;              % Recent Floor Crossing
CATCH = -1;               % Recent Ceiling Crossing

%% HOLD STATES
INTERRUPT = 1;            % Break Command
```

```
ALLOW = 0;                  % No Break

%% OPERATIONS
comp = abs(comp);           % Absolute Compensator Current

% Determine Most Recent Crossing State
if comp > high
    dir = CATCH;
elseif comp < low
    dir = RELEASE;
else
    dir = drift;
end

% Determine Break or No Break
if dir == CATCH
    hold = INTERRUPT;
else
    hold = ALLOW;
end
```

### 3.2.6 Transience Control

Filters take time to delete component frequency information from the moment it is introduced. The behavior with regard to this frequency is referred to as the *transient response*. As the Fourier Transform is a linear transform, and sinusoids are linear functions, the aggregate response will be the sum of the individuals. The moment a filter starts operation, the waveforms passed can be considered new information, as they can at the moment that they change amplitude.

As this system is built around the isolating notch filter, it is important that its operation be guaranteed. This is done with the subsystem designed for this project, and herein is referenced as the "Flush-State Controller", which contains some of the most sensitive signals processing in the overall design.

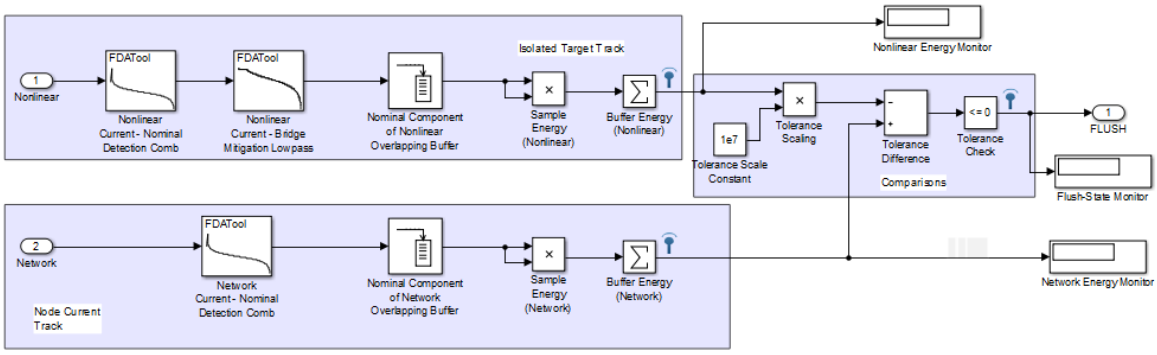


*Figure 57: Flush-State Controller Diagram*

The issue of 60Hz current remaining in the notch filter's output, and being fed to the compensator is discussed alongside the isolating notch filter's profile, as well as in the filter-transience measurement. This is the attempted solution. The intended concept is to compare the 60Hz component waveforms of the signal before and after filtration. If there remains 60Hz signal outside of a given tolerance, then the compensator accessing the filter's output is enormously detrimental to the operational health of the system, which will forever attempt to compensate for the nominal-frequency current, producing amplitude shifts that will force the filter to always regard the 60Hz input components as new information.

### *3.2.6.1 Development*

Originally, two identical signal processing tracks existed, desired to function as bandlimited energy detectors. A narrow bandpass, or *comb* filter, was used to isolate the 60Hz current, to allow for comparison of the pure nominal frequency components before and after filtration. Each output was fed into a FIFO, simulated using a buffer of 256 entries, overlapping by 255. This allowed for new comparisons at every sample-interval. When output, each sample of these buffers was squared to obtain the sample-energy. Their elements were summed to find the time-domain-window-energy, which for the isolating filter's output track, was multiplied by 100, and subtracted from that of the

original signal's track, to determine if the isolating filter's 60Hz component held less than one-percent of the energy of the frequency it was to eliminate.

This proved insufficient. Break commands were sent after short intervals of compensator operation as highly variable magnitude spectrum could not be eliminated by the bandpass filter's quickly enough to stay below the tolerance. For this reason, the nonlinear current's path includes a lowpass filter to eliminate these higher-frequency intrusions, although several short-lived exits in the flush-state are observed before compensation can be considered a persistent process/

# 4 Experiments and Results

Numerous experiments were run on a number of topics, ranging from model examinations, to H-Bridge behavior. Some of these tests existed to observe practical implementations (in a simulated environment) for already familiar theory. Some existed in attempts to explore unfamiliar ideas or new notions. Some were performed in attempts to experimentally gain insight into material deemed unfamiliar, to learn how one might make efficient use of new concepts.

## 4.1 Filter Transience Experiment

A set of experiments showed that early operation of the filter connected to an idealized controlled current source would fail to eliminate nonlinear currents indefinitely. It was determined that this was due to existing 60Hz signal, which had yet to be fully reduced, in the isolating filter. Thus the compensator was trying to eliminate 60Hz current at the same rate.

The next experiment was an examination of filter transient intervals for the isolating filter. The transient interval was measured by feeding the filter a 60Hz sine wave, and measuring how long it took the filter to suppress the signal below a benchmark of 1% original amplitude.

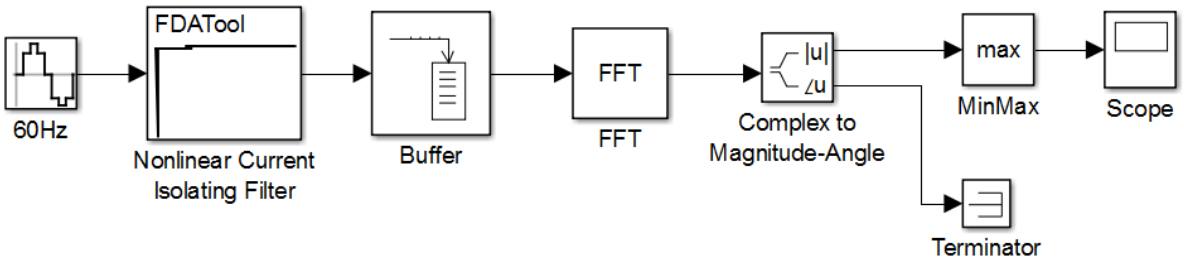


*Figure 58: Simulation Diagram for Isolating-Filter Relevant Transient Response*

The wave marked for suppression, 60Hz, was fed into the filter. The filter output was fed into an overlapping buffer of 128 samples, and the buffers FFT taken for each sample-rate. The signals magnitude response was taken from the FFT, and its maximum value taken, each of which were plotted against the time at which they occurred.

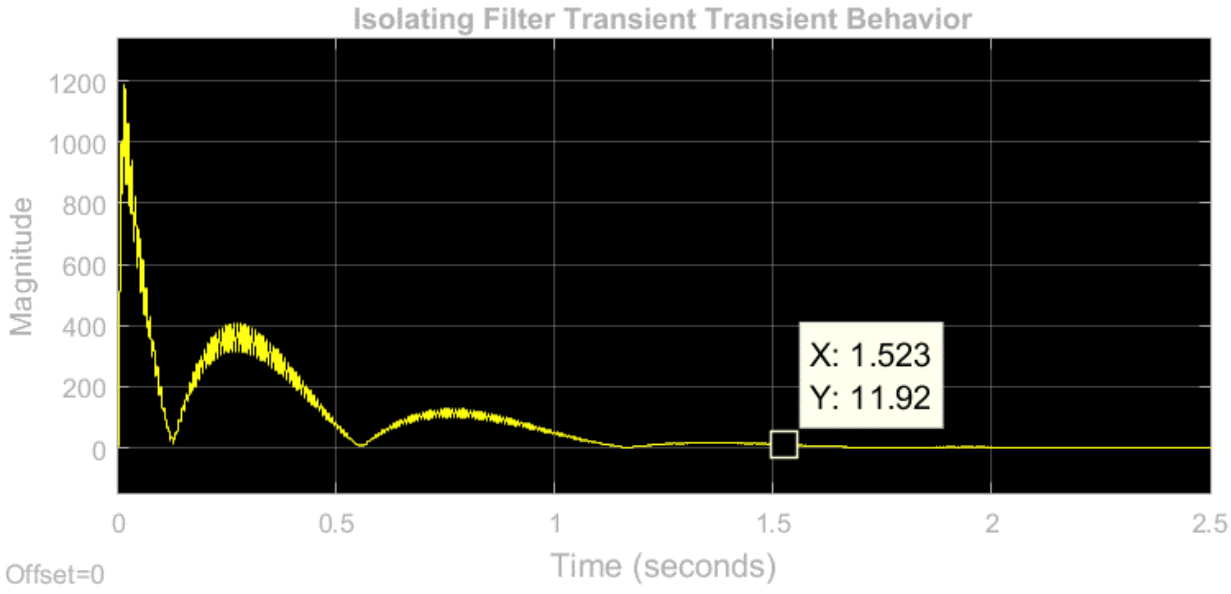


*Figure 59: 60Hz Transient Adjustment Period for Isolating Filter*

## 4.2 Early Warning Signs

Perhaps the most interesting and confusing experiment arose from an examination of H-bridge transient behavior. The test was setup to examine the behaviors exhibited by a particular state-transition in the IGBT H-Bridge configuration. One state was intended to provide a short circuit at the leads of a current source (a stand-in for a voltage source, considering that current-delivery is the project's goal, and analog methods of further-controlled switching hadn't yet been considered), and the other was intended to provide a short-circuit across the load. A month later it was realized that both shorted out the source, and neither the load, but results remain significant to the project's conclusion.

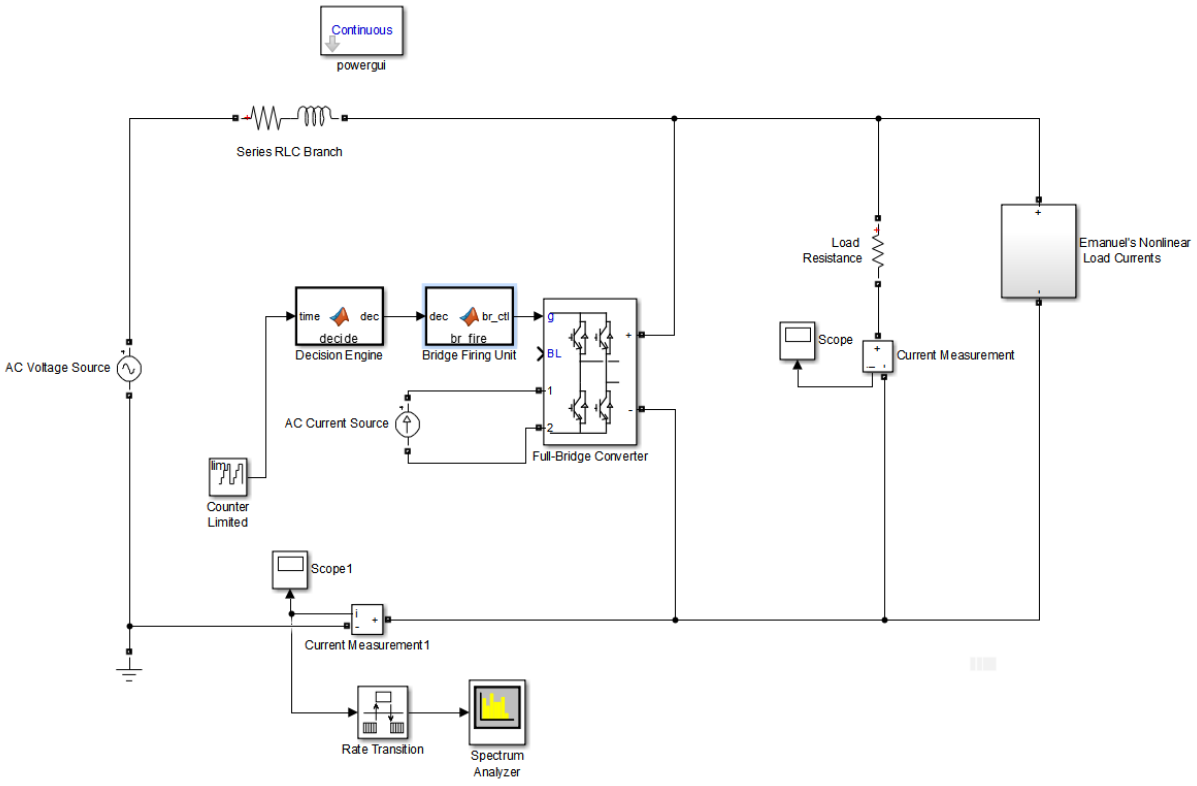


*Figure 60: Simulation Diagram of H-Bridge Transience Experiment*

This experiment, upon first glance, appeared to achieve the goal, despite its intention to just exhibit isolated behaviors. The examination of what I thought would be transient states yielded an attractive current spectrum for the device stated as the ultimate goal of the project.

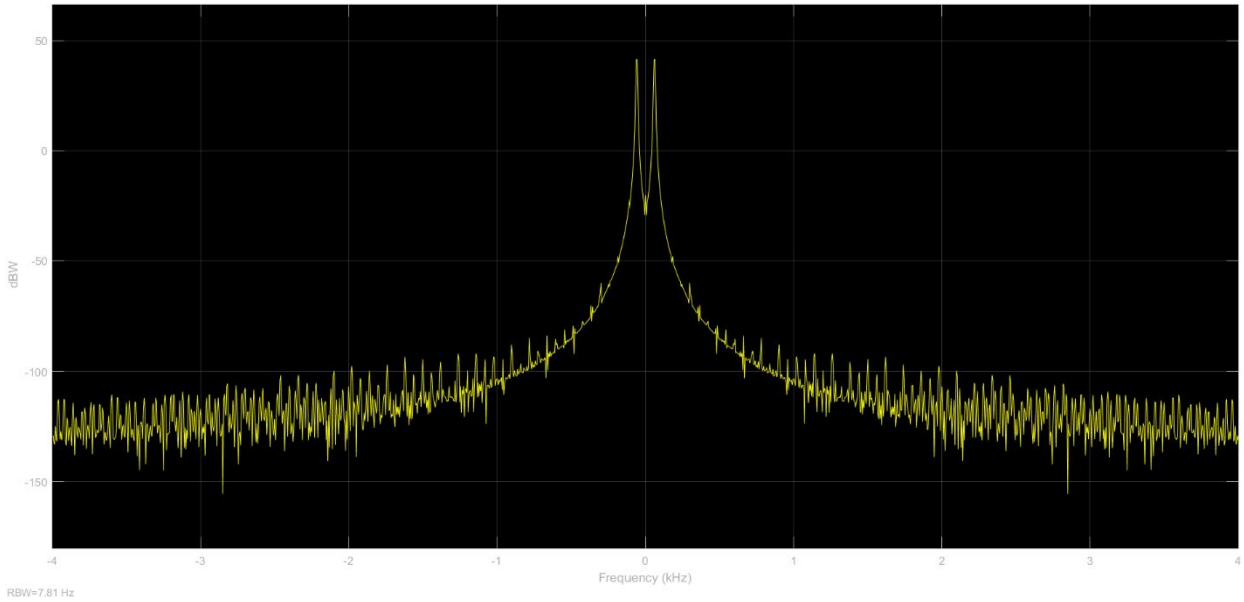


*Figure 61: Spectrum of H-Bridge Switching Transience Experiment*

Those two peaks occur at 60Hz, the target frequency to be retained in the network. While some other frequency peaks seem present, they appear to be negligible in the logarithmic scale. This can be confirmed by examining the time-domain signal.


*Figure 62: Grid Current in H-Bridge Switching Transience Experiment*

No harmonics seem to be present in this wave, and the period sits nicely in the vicinity of 16.6ms, the period of a 60Hz oscillation. Unfortunately, this did not prove to be a satisfying end to the project.

The test was in no way supposed to satisfy any operational requirements, it was purely observational, and the data seemed far from scale. The steady-state amplitude of the current is 277 Amperes, and 14.2kW peak in the frequency spectrum. The time-domain current figure alone was enough to indicate something was amiss. The current sources in the nonlinear load are meant to be the currents present when the H-bridge is idle, which it essentially was for this experiment, and they sum to 53 Ampere ceiling if the maxima of all three superimposed current waves were to coincide.

This issue should have been investigated in greater detail earlier on. Rather it was glossed over with the dismissal that the model under examination was not intended as a solution, and therefore was of no consequence. This was incorrect. As it turns out, common threads between simulations inspired the behavior, and it was not the last time the behavior would invalidate an experiment.

## 4.3 The (Almost) Final Model

### 4.3.1 Significant Limitations

The first run of what was thought to be the final model (and to slightly-lesser extents, each model previous and most subsequent) exhibited wholly discouraging behavior, not immediately with operation, but primarily with data availability. Simulink required painful amounts of time solely to calculate the operation of the simulation in which both the compensator and test-model were present.

Physical models are challenging to simulate as-is. The software possesses a set of assumptions regarding abstraction of circuit behavior that may not be shared by the user. Generation of such data, especially given the bidirectional nature of physical connections, is a computationally expensive process to perform with any accuracy. Simulink favors iterative approaches, generating adaptive models which attempt to converge to a sensible answer within a tolerance. Sharp transitions, that change the behavior to which the algorithm has adapted, may result in a failure to converge, as might nonlinear models. Logging too many variables, at too-high of a time-resolution, may proliferate logged data on a scale which could prove unmanageable for the simulating devices RAM, nonvolatile memory, or both.

This simulation, involving nonlinear circuit elements, critical simulation of physical system behavior, and frequent state-transitions, and extremely time-sensitive operation and corresponding signals to be examined, checks every box on the list of challenges to a simulator. First attempts at simulation regularly returned nonlinear convergence failure errors.

To bypass this, the simulation had to be altered to use behavior-wise less versatile fixed-step solvers (as opposed to variable-step), at a reduced sample rate. Higher tolerances had to be allowed. And still, the simulator was only capable of producing several milliseconds of run-time data in an hour of real-time. This posed a significant hurdle, not fully mounted, as data-collection has crashed the simulation if too great. Ten seconds of run-time data was desired to see if and when the compensator

would stabilize in that window, and if not, to inform a guess as to whether or not operations would converge soon thereafter. The compensator, containing a break-case where it idles while waiting for the wave isolation to stabilize, should be in this idle state for a minimum of one-and-a-half seconds. Thus days would be required, even in the final configuration, to simulate sufficient run-time to witness the device begin operation.

This is not to say that simulation yielded no results of interest that would be useful to any future work. While the compensator's integrated operation has not yet been verified, a significant flaw in the approach was exposed.

### 4.3.2 Running the Final Simulation

The diagram used in this simulation is large both in concept and display space, but reference to the block design may inform what is seen in the overall simulation diagram.

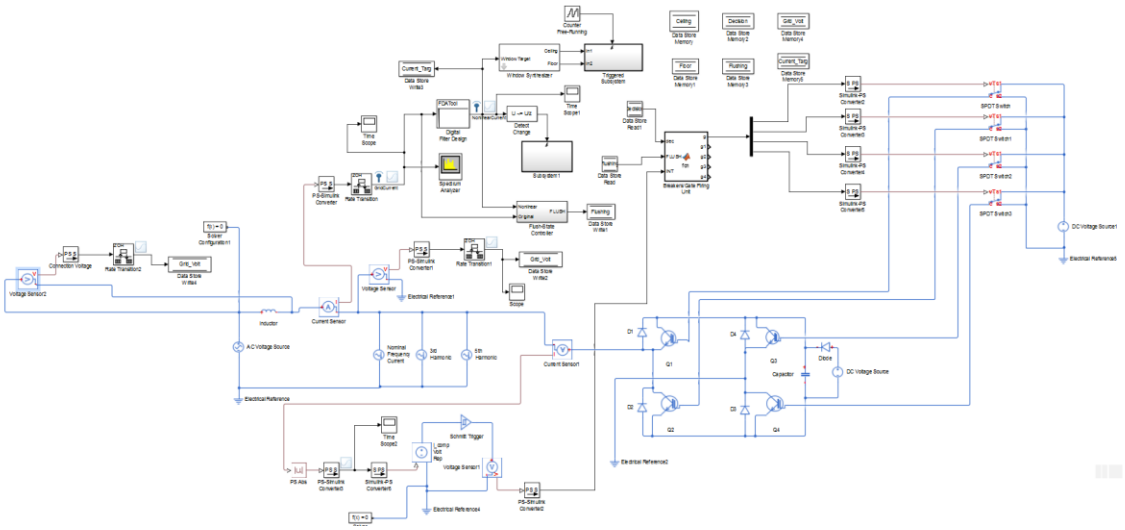

*Figure 63:Final Compensator Simulation Diagram With Monitoring Configuration*

The simulation slowly progressed, but had never been allowed to enter the 1.5 to 3 second range where the compensator is expected to exit the "idle" state. But concerning behaviors were present in the simulation long before the device was expected to begin operation within the circuit. The grid

current immediately adjusted to a simple wave, displaying none of the expected 180Hz and 300Hz current harmonics. The wave possessed a 400 Ampere amplitude. Investigating further, it was discovered that the compensator current, which was supposed to be effectively zero during the idle-state, was actually quite significant. This compensator current appeared as a 355A distorted half-wave, with part of its rise to its peak apparently clipped, but rising to this distortion and falling back to seemingly in synchronization with the grid current.

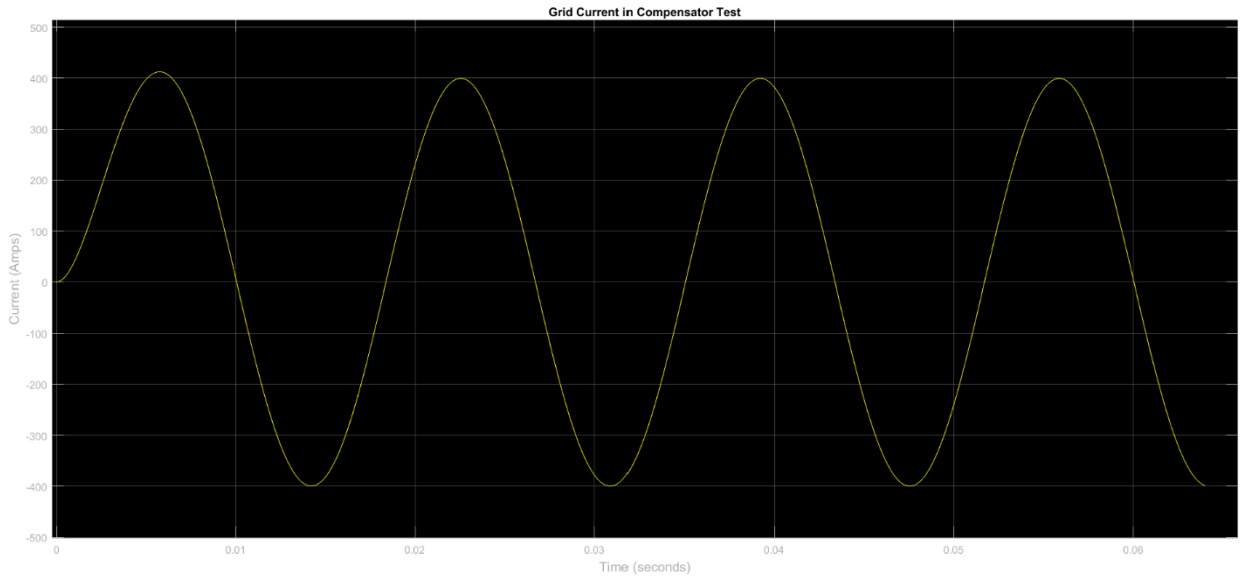


*Figure 64:Startup Grid Current with Provided Model and Final Compensator Design*

The startup (but idle steady-state) compensator current (in green), in comparison with this follows.

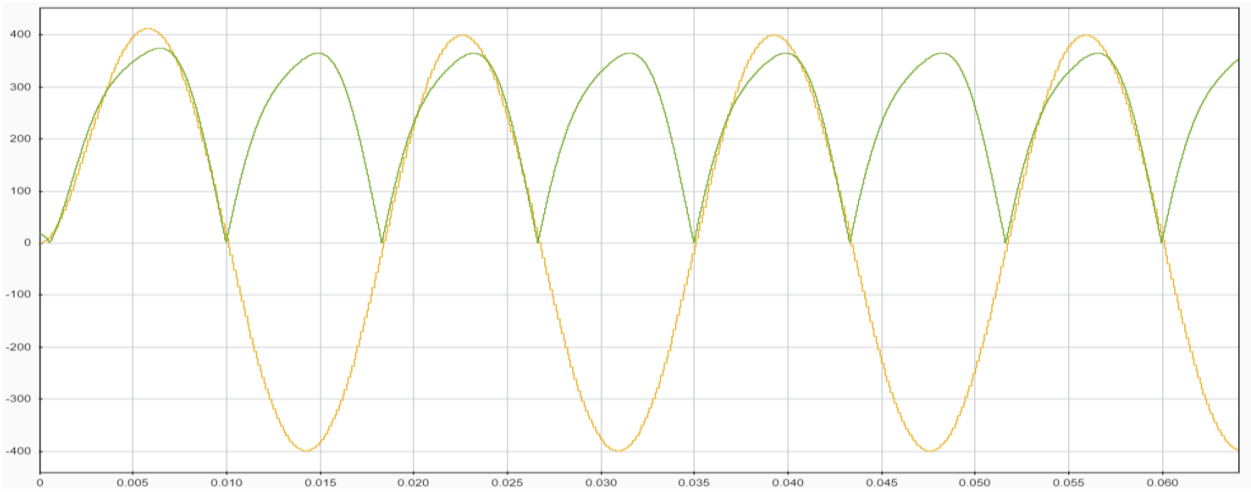


*Figure 65: Comparison of Grid Current and the Compensator's Delivered Current*

Upon debugging of the simulation, what is believed to be the culprit-fault for this behavior was discovered. The circuit voltages in the test model were intended to remain approximately constant regardless of amplitude, with almost the entire loop voltage being applied across the load. Yet the reality of the simulation proved far different from this intention and suspicion, as shown in the behavior of the load voltage with time.

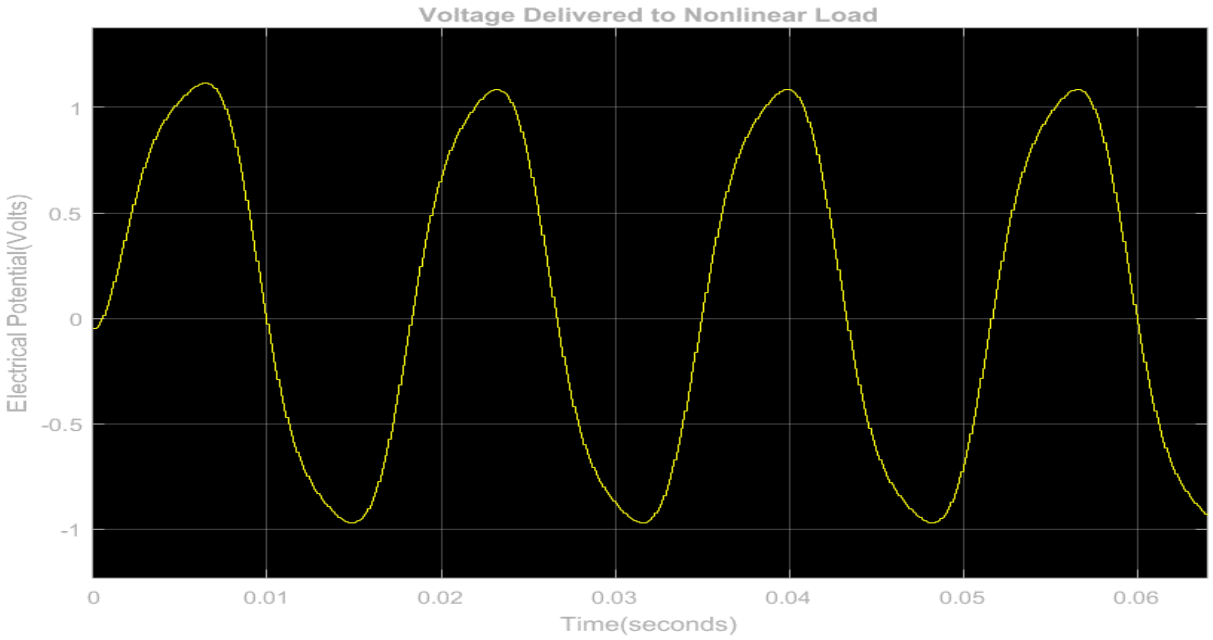


*Figure 66: Load Voltage in Simulation of Final Compensator with Provided Test Model*

Initial examination of the load voltage, examining solely its shape, did not seem too prohibitive to attaining solid results, alone. But the true issue appears when it is compared to other circuit voltages.

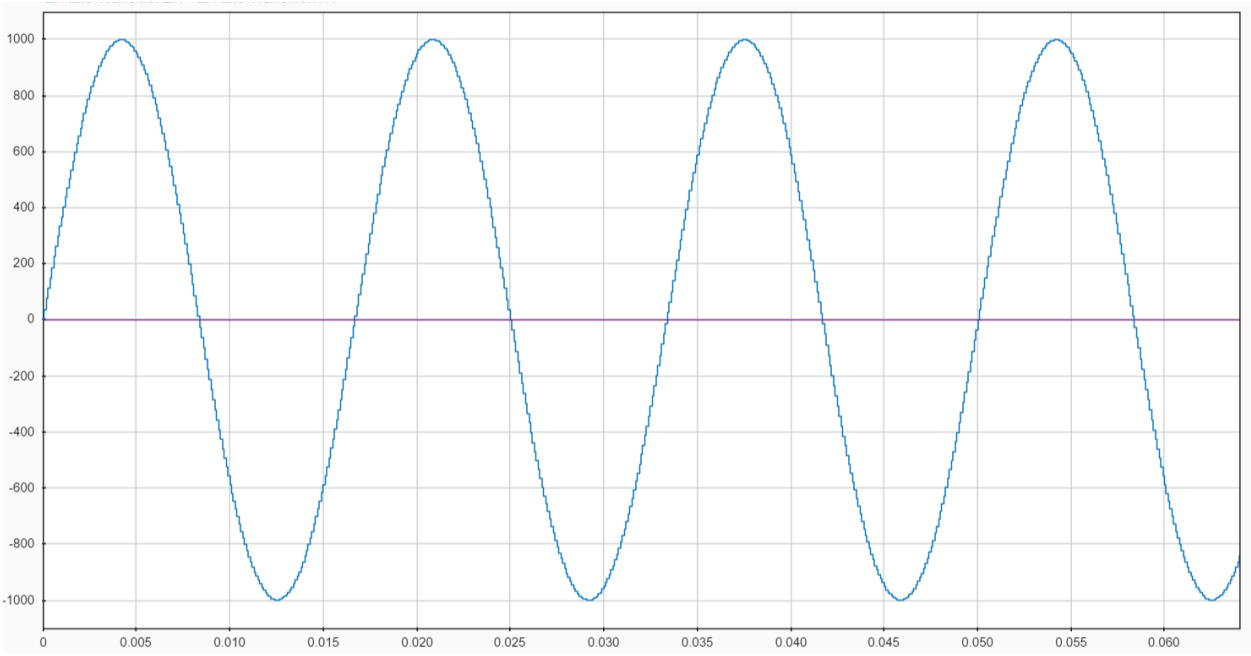


*Figure 67: Load Voltage and Connection Impedance Voltage Drop*

When the load voltage, in purple, was compared to the voltage across the connection impedance, in blue, the load voltage waveform was returned to, and it was noticed that the amplitude was hardly greater than one volt.

## 4.4 The (Actual) Final Model

"Two truly disappointing conclusions are drawn from this project. While many individual components have been shown to function as intended, examination of the project's target operation was precluded by both limitations of simulation software, and inapplicability of the test environment model. There is little that can be done regarding limitations of simulation software in the scope of this project. And, unfortunately, the behavior of the model was noticed far too late for a new model to be developed, tested, applied, and documented."

This was the first paragraph of what was believed to be a finalized Conclusions section. Much to the joy and the dismay (now that this and the Conclusions section must be rewritten), that it now concluded the model was not at fault. The impracticalities were introduced in compensator design for both the Accidental Compensator and the previous model. Enabling the shoot-through cases in the Accidental Compensator attached a short-circuit across the terminals of the load. With the other, the actual culprit was far more difficult to notice.

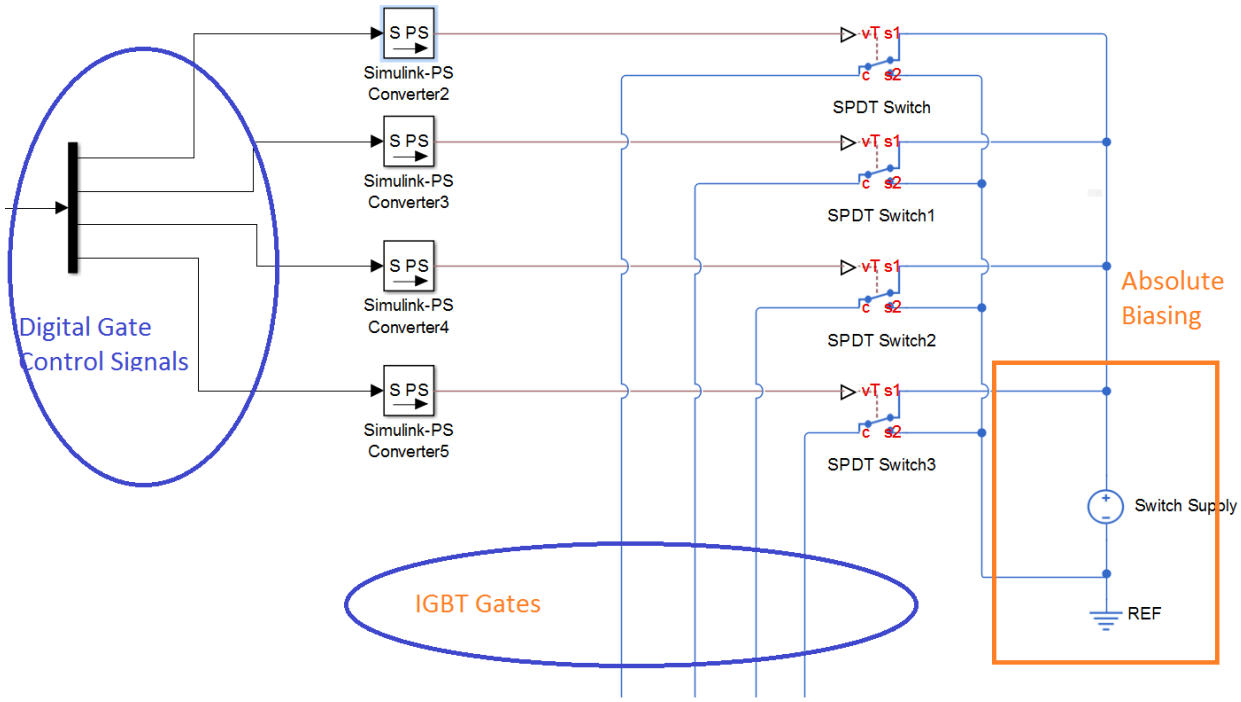


*Figure 68: Outlining the critical error in the (Almost) Final Compensator*

Even ignoring the observation that the switches were improperly configured to, if other parts of the circuit had been properly configured, exist in the opposite states as intended. The gates are either being supplied 0V, or a fixed DC-bias above. Gate voltage is not the only important signal to determining whether an IGBT is on or not. It is the difference between the *gate* and the *emitter* which allows conductance if it surpasses the device threshold voltage. Given that the emitter voltages, with a

single exception, are not fixed, and some are supposed to vary quite significantly, the gate bias had to be tied to the emitter with the methods seen in Figure 18.

While digging in documentation it was discovered that the Simscape Electronics Library IGBT model used in the previous simulation could not be switched had off until it had finished its off-state to on-state transition. For a model that operates by catching transitions before they have a chance to reach their final state, this was very problematic. Thus the IGBT blocks were replaced with those currently used as indicated in any simulation diagrams of the Power Delivery block. The resulting system schematic is as follows:

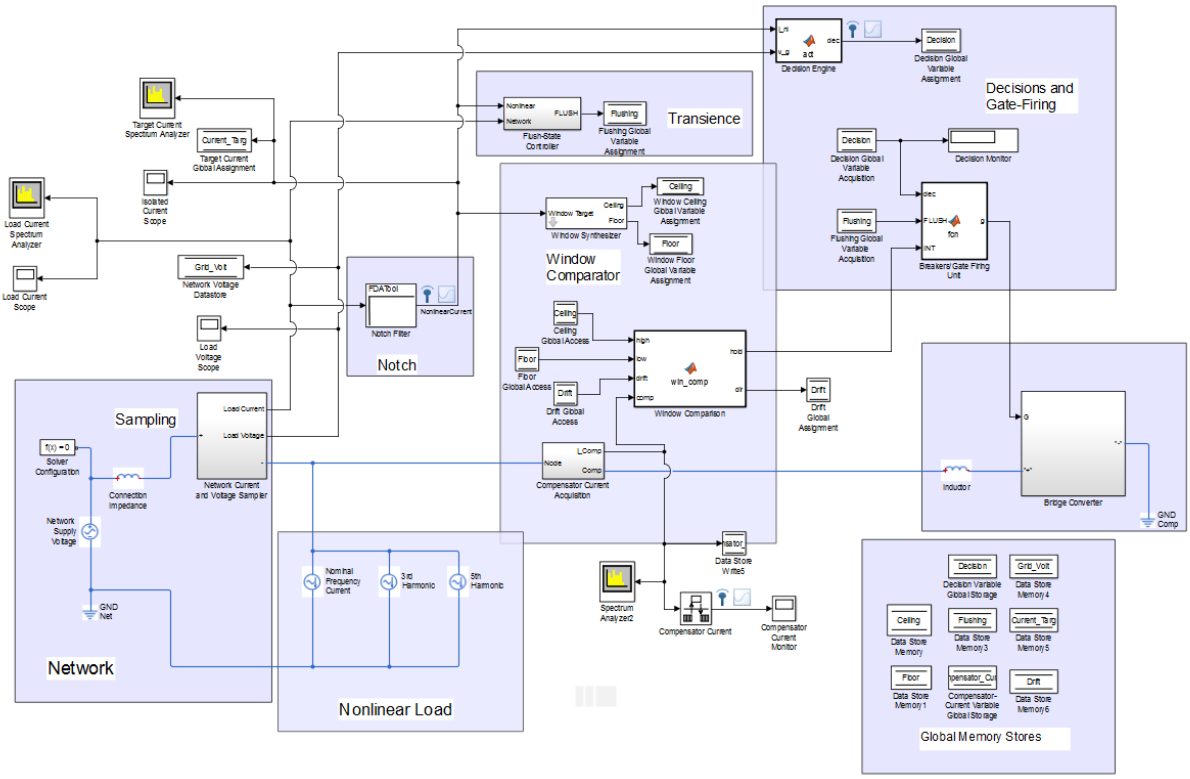


*Figure 69: Final Compensator Simulation Diagram*

The simulation was able to be configured to run at a reasonable speed. And results were achieved that established some proof of concept. The first noticeable behavior, after repeatedly scaling down the tolerance in the flush-state controller due to premature entry of the compensator, was the

non-static nature of the flush-state. This was noticed in the compensator current, as the compensator would operate at several short intervals before it could pass the flush-state logical test with perpetual consistency. Three distinct pulses can be noticed before this moment.

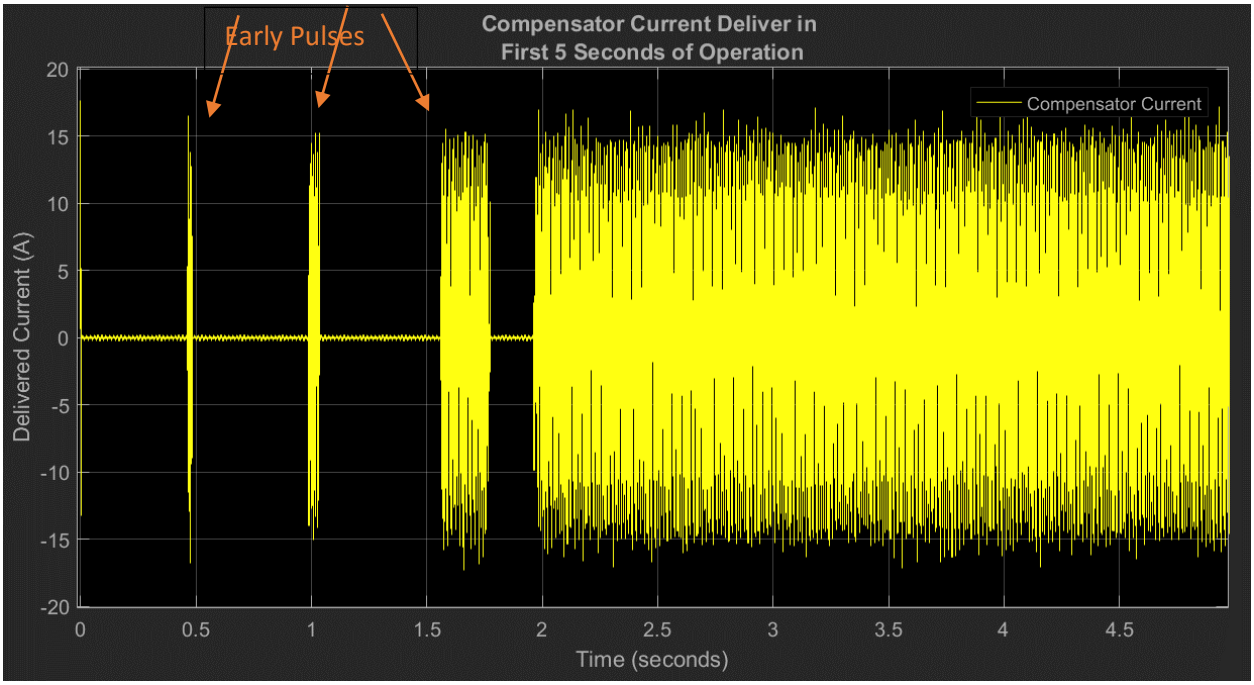


*Figure 70: Compensator Current from 0 to 5 Seconds, Early Pulses Indicated*

This is evidence that the filter and transience control are functioning in the neighborhood of intended operation, where the transience control "Flush-state controller" block is choking off compensator current in the spacing between these pulses.

Further evidence of this is available in the nonlinear current, which does not stabilize if it both still contains significant 60Hz current, and the compensator is not held in an idle state. Due to the simulator deleting past data points, to demonstrate the nonlinear characteristics of the network current.

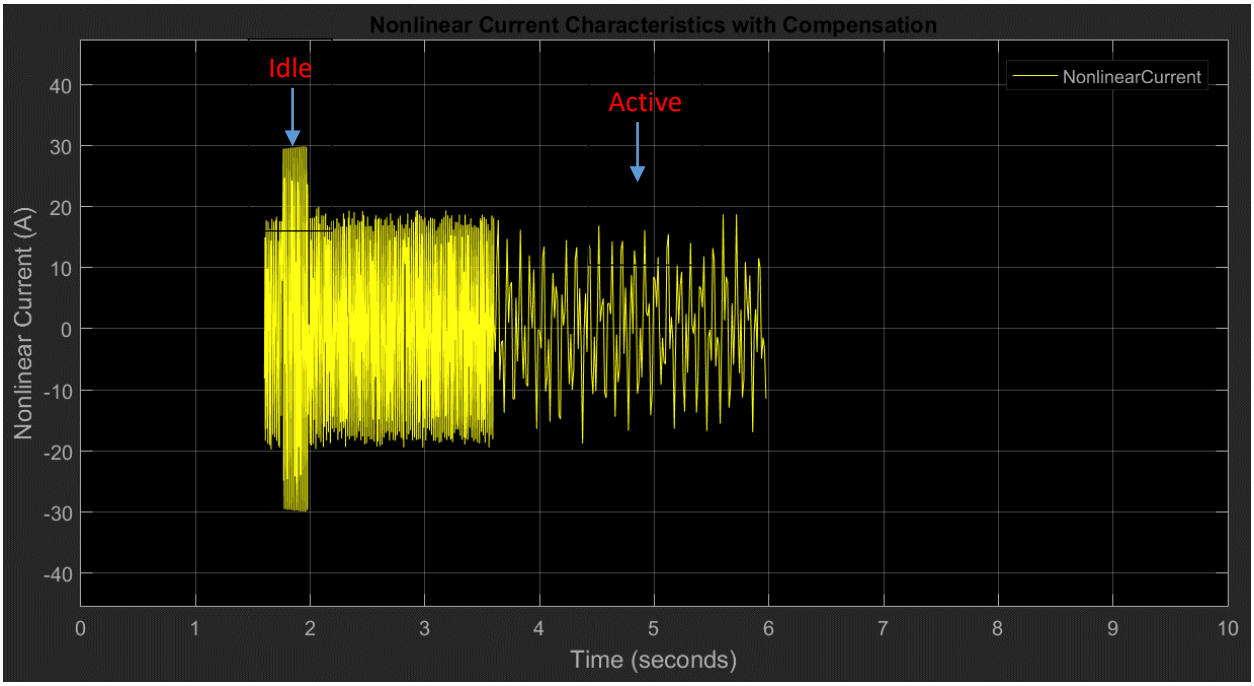


*Figure 71:Nonlinear Current of Most Recent Simulation under Compensator Operation*

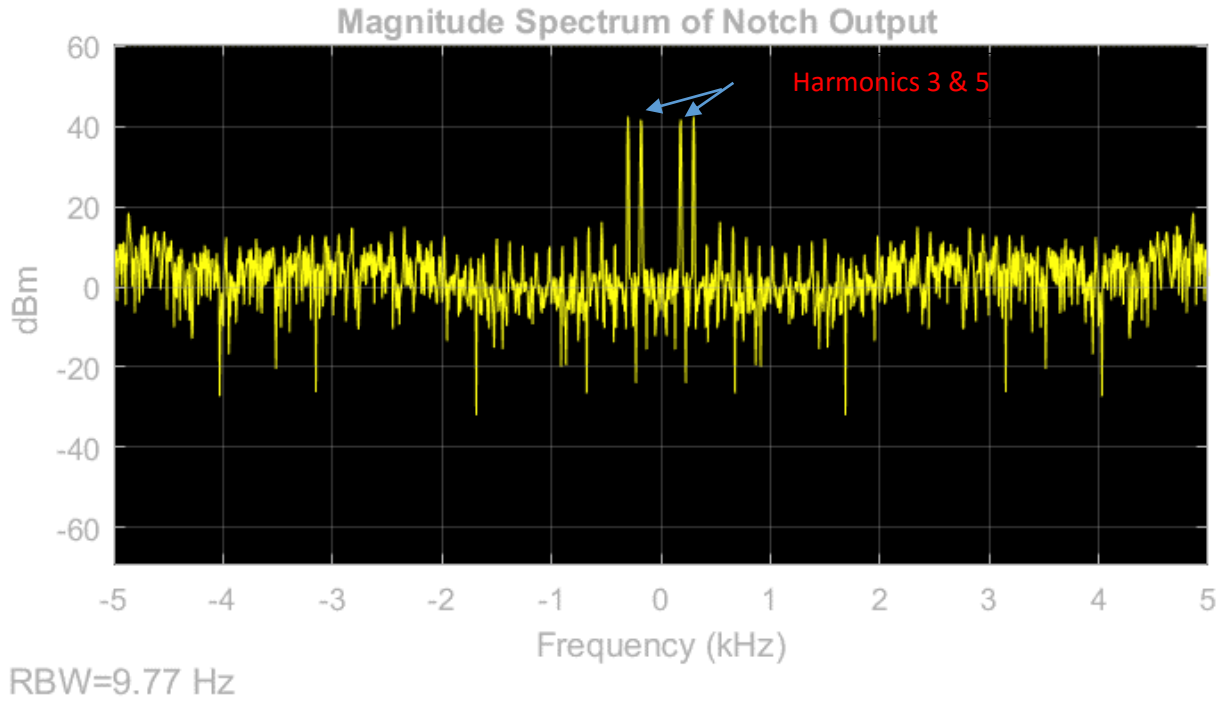


*Figure 72:Magnitude Spectrum of Nonlinear Current*

As can be seen in Figure 72, the 60Hz signal has been successfully removed from the filter's output. Even more encouraging is the loss of amplitude at time-instances where the compensator is active. This suggests that the nonlinear current is being actively suppressed by the compensator. But this is all peripheral. The volatile nature of the bands outside of those harmonics present in the network may be alarming at first glance, but while all harmonic currents, 1 through 5, are given similar amplitudes by the load, there is some interest in how they compare in a linear scale, as opposed to the semi-log scale shown above. This linear scale network current may be seen in Figure 74.

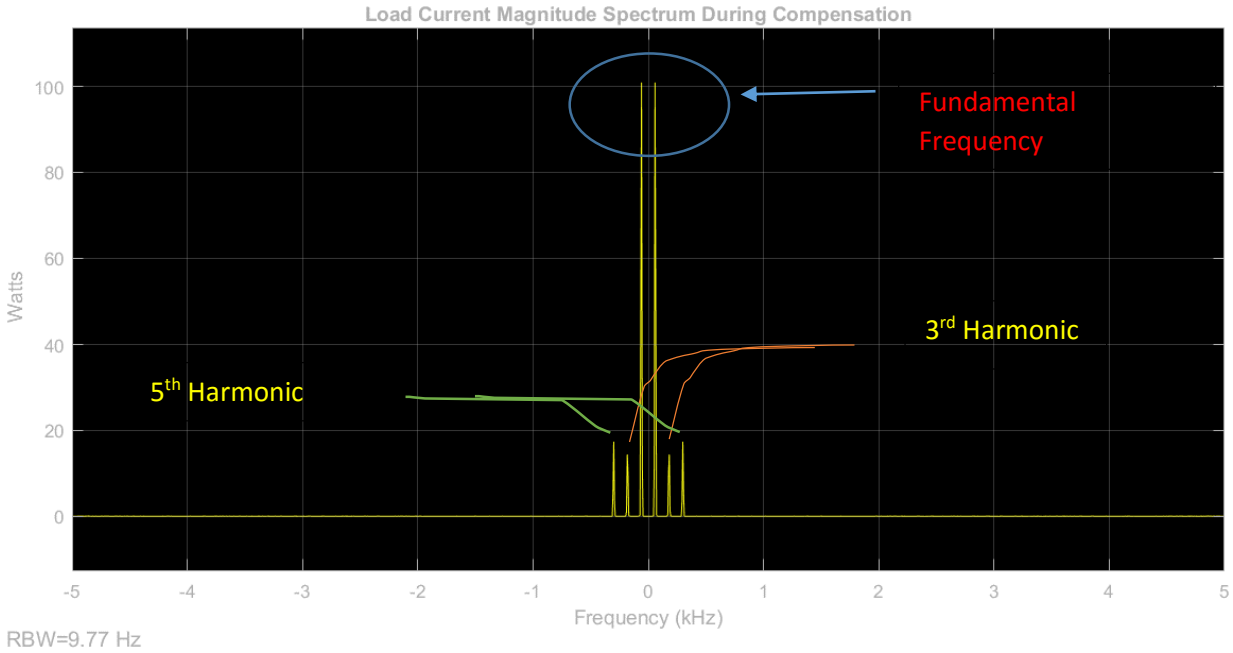


*Figure 73: Linear Scaling of Harmonic Magnitudes in Load Current During Compensation*

This is rather encouraging when compared to the form of its existence before compensator operation, as seen in the following figure.

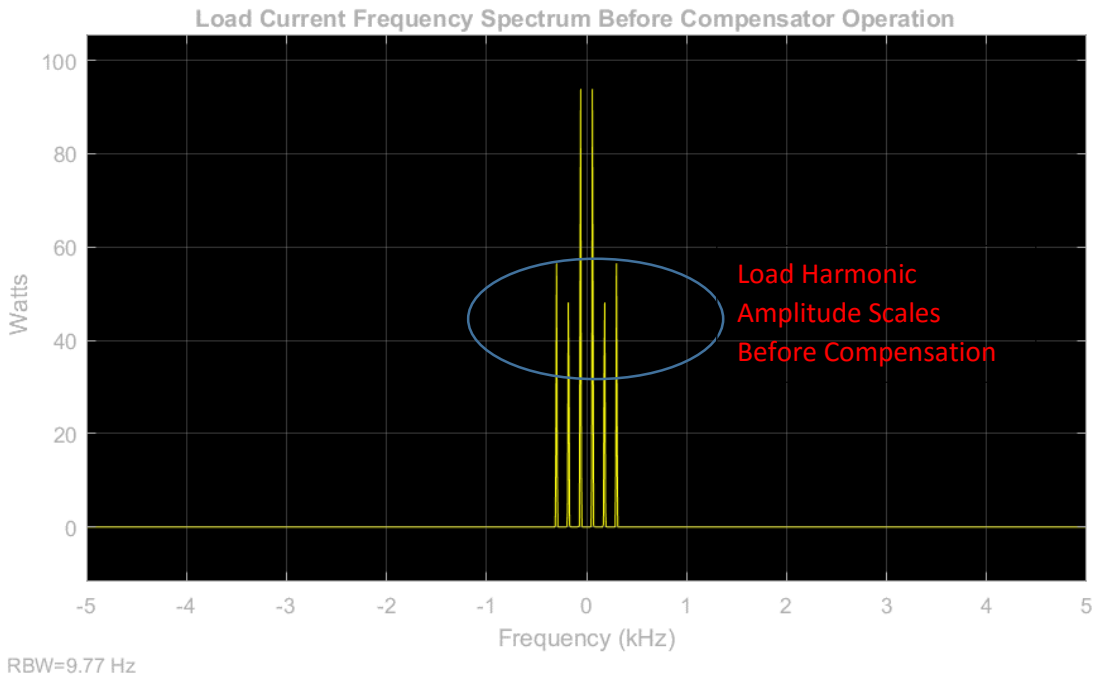


*Figure 74: Load Current Linear Magnitude Spectrum Prior to Compensator Operation*

To verify that such behavior does not come at the cost of unrealistic measures, and to examine the exact shape of the controlled current at the load's terminals, still far from perfect.

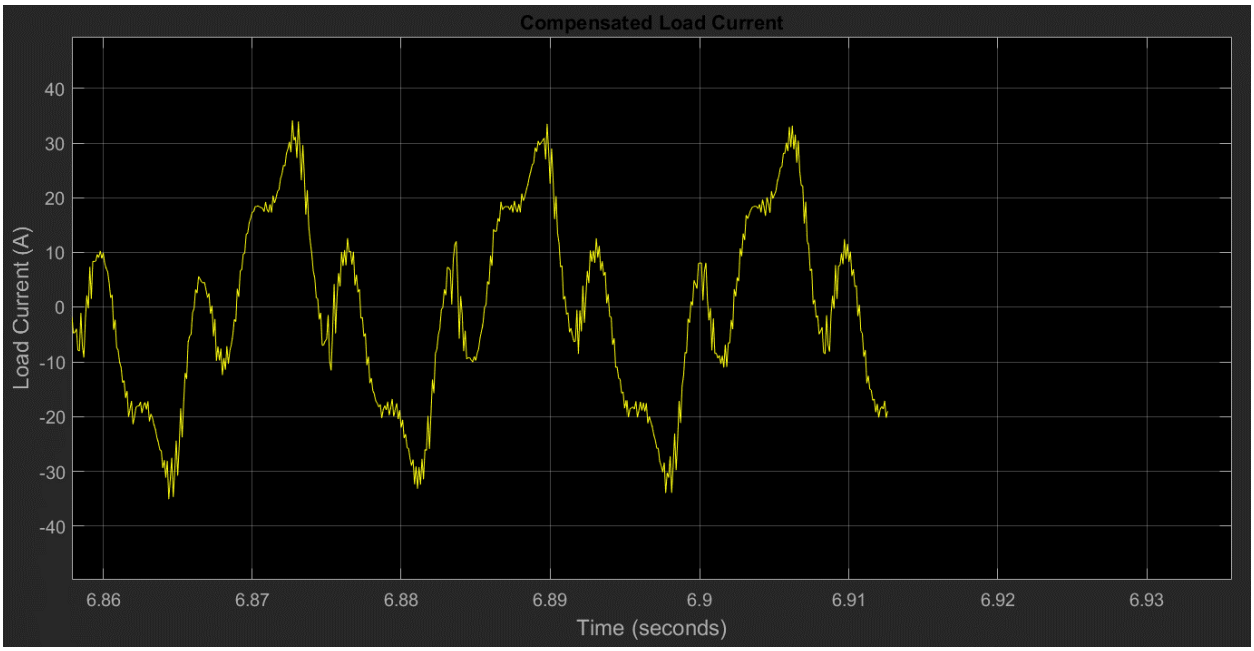


*Figure 75: Compensated Load Current*

# 5 Conclusions and Future Work

Given the difference in the magnitude spectrums of the latter two in the prior chapter are interpreted as very encouraging results. This encouragement is felt in no small due to the resignation to a perceived impossibility involved in simulating the compensator results, as recently as a week before the project deadline. Yet simulation was achieved, and the harmonics demonstrably halved, at the very least, in operation of the compensator.

Unfortunately, the best results achieved have not been presented here, due to the limited number of oscillograms acquired. At this stage in development, the tweaking of parameters such as the smoothing inductance, the internal resistances and inductances of the IGBTs, and the voltage in the DC Supply, seems to determine a substantial difference in operational integrity and effectiveness at harmonic compensation.

The spikes, superimposed over what is certainly a visible 60Hz sine wave, of amplitude just below its original 20V, still remain somewhat unaddressed. Referenced work does have similar phenomena. They could be remnant or reintroduced harmonics, or perhaps sudden current discharges from the smoothing inductance, triggered by a switching event in the bridge converter.

The next steps required to further this process begin with the determination of parameters for the system to better achieve the goal of harmonic elimination. Relevant values seem to be the window tolerance, the smoothing inductance, the DC supply for the bridge inverter, and the IGBT internal parameters. From this point, power loss analysis and related design decisions can be executed. Ultimately, a physical implementation, and then extension to a three-phase network are desired.

# 6 Appendices

## 6.1 Appendix A: Supporting MATLAB Scripts

```
%% Cosine Superposition Demonstration
% Demonstrate effects of adjusting phase.

time = 4*pi;
del_t = 1/100;

t = 0:del_t:time;
signal = cos(t);
noise = 0.1*cos(10*t);
real = signal + noise;

plot(t, signal, t, noise, t, real);
title('Demonstration of a Two-Wave Superposition');
xlabel('Time, t, in Seconds');
ylabel('Signal Observed In System');
```

impulse_demo.m

```
%% Demonstrate Behaviors
% Plot Impulse Functions with Different Scales and Delays
% -- Setup Time Data
time = 10;
t = -time/2:0.01:time/2;     % Time vector
% -- Generate Delta Functions
delt_orig = impulse(t);      % Unit-Impulse Function
delt_delay = impulse(t-2.5);% Delayed Impulse
delt_scale = -3*impulse(t); % Scaled Impulse
delt_fun = 2*impulse(t+4);  % Negative Impulse with Lead
% -- Generate Plot
figure
plot(t, delt_fun, t, delt_scale, t, ...
    delt_delay, t, delt_orig);
xlabel('Time in seconds');
ylabel('Amplitude');
title('Impulse Characteristics Plot');
```

impulse.m

```
%% Impulse Function
% Define the Impulse Function
function del = impulse(t_vec)
del = zeros(1, length(t_vec));
```

```
for n=1:length(t_vec)
    if t_vec(n)==0
        del(n) = 1;
    end
end
end
```

### 6.1.1 Circuit Theory

#### *6.1.1.1 Loads*

##### 6.1.1.1.1 Nonlinear Loads

```
%% Nonlinear Load Demonstration Data Processing
%   Saves desired data to appropriate variables.
%   Generates time-domain plots
%   Downsamples to show well-scaled complex-frequency domain plots
%   Calculates magnitude and phase responses
%   Make frequency vector for use in plotting
%   Generates magnitude and phase plots
% ------ Desired Data ----- %
%       - Current
%       - Load Voltage

%% Save Desired Data to More Convenient Handles
%   Use tout for time vector
%   Structure of "data"
%       data.time                   1D Time Vector
%       data.signals                Held Signals and Info in struct
%           data.signals.values     Circuit Data
%           data.dimensions         Number of Circuit Values
%           data.label
%       data.blockName
%   Desire time vector, current (1st value vector), load-voltage (2nd
%       value vector)
time = data.time;
current = data.signals.values(:,1);
load_voltage = data.signals.values(:,2);

%% Generate Plots
figure
%   Generate Load Voltage Plot
subplot(2, 1, 1);
plot(time, load_voltage);
title('Voltage Applied to Nonlinear Load');
%   Generate Load Current
subplot(2, 1, 2);
plot(time, current);
title('Current Passed by Nonlinear Load');
```

```
%% Downsample to Scale Complex-Frequency Domain Data
ds = 90;   % Downsampling factor
time_ds = downsample(time, ds);
load_voltage_ds = downsample(load_voltage, ds);
current_ds = downsample(current, ds);

%% Calculate Magnitude and Phase Responses
%   Calculate Fourier Transforms
Vl_fft = fft(load_voltage_ds);
I_fft = fft(current_ds);
%   Eliminate Fourier Transform Repetition
Vl_fr = Vl_fft(1:length(Vl_fft)/2);
I_fr = I_fft(1:length(I_fft)/2);
%   Calculate Magnitude Spectra
Vl_mag = abs(Vl_fr);
I_mag = abs(I_fr);
%   Calculate Phase Spectra
Vl_ps = angle(Vl_fr);
I_ps = angle(I_fr);

%% Make Frequency Vector
freq_min = 0;   % Minimum Frequency is 0Hz
% Sampling Frequency
fs = length(time_ds)/time_ds(length(time_ds));
f = linspace(freq_min, fs/2, length(Vl_fr));

%% Generate Magnitude and Phase Plots
figure
%   Magnitude Spectrum of Load Voltage
subplot(2, 2, 1);
plot(f, Vl_mag);
title('Load Voltage Magnitude Spectrum');
%   Magnitude Spectrum of Load Current
subplot(2, 2, 2);
plot(f, I_mag);
title('Load Current Magnitude Spectrum');
%   Phase Spectrum of Load Voltage
subplot(2, 2, 3);
plot(f, Vl_ps);
title('Load Voltage Phase Spectrum');
%   Phase Spectrum of Load Current
subplot(2, 2, 4);
plot(f, I_ps);
title('Load Current Phase Spectrum');
```

## 6.2 Appendix B: Simulink Model Diagrams

### 6.2.1 Nonlinear Load

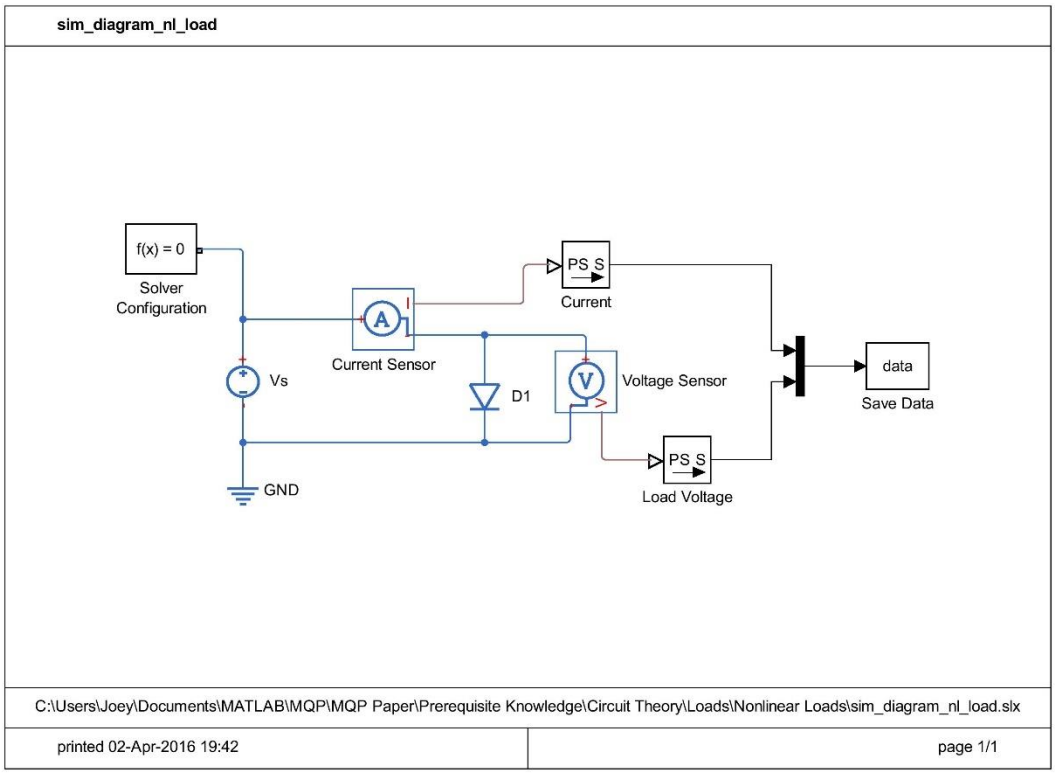


*Figure 76: Simulation Diagram for Nonlinear Load Demo*

# 7 Bibliography


[1] PacifiCorp, "Engineering Handbook," 25 July 1996. [Online]. Available: https://www.pacificpower.net/content/dam/pacific_power/doc/Contractors_Suppliers/Power_Quality_Standards/1C_1.pdf. [Accessed 27 April 2016].

[2] E. C. Aprilla, "Modelling of Photovoltaic (PV) Inverter for Power Quality Studies," August, 2012.

[3] Siemens, "Harmonics in power systems," May 2013. [Online]. Available: https://www.industry.usa.siemens.com/drives/us/en/electric-drives/ac-drives/Documents/DRV-WP-drive_harmonics_in_power_systems.pdf.

[4] MIRUS International, Inc., "What is an SMPS and how does it generate harmonics?," 28 10 2003. [Online]. Available: http://www.mirusinternational.com/downloads/hmt_faq04.pdf. [Accessed 28 April 2016].

[5] Hammond Manufacturing, "Design Guide for Rectifier Use," [Online]. Available: http://www.hammondmfg.com/pdf/5c007.pdf.

[6] R. G. Ellis, "Power System Harmonics," Rockwell Automation, Cambridge, ON, 1994.

[7] G. M. Williams, "IDC Technologies," [Online]. Available: https://www.idc-online.com/technical_references/pdfs/electrical_engineering/Generators_and_nonlinear_loads.pdf. [Accessed 27 April 2016].

[8] D. A. Torrey and A. M. A. M. Al-Zamel, "Single-Phase Active Power Filters for Multiple Nonlinear Loads," *IEEE Transactions on Power Electronics,* vol. 10, no. 3, pp. 263-272, 1995.

[9] H.-L. Jou, J.-C. Wu and H.-Y. Chu, "New single-phase active power filter," *IEEE Proceedings - Electric Power Applications,* vol. 141, no. 3, pp. 129-134, 1994.

[10] MIRUS International Inc., "Harmonics and Harmonic Mitigating Transformers (HMT's) Questions and Answers," MIRUS International, Inc., 28 October 2003. [Online]. Available: http://www.mirusinternational.com/downloads/hmt_faq01.pdf. [Accessed 2 April 2016].

[11] MathWorks, Inc., "N-Channel IGBT".

[12] Eaton Corporation, "Commonly used electrical symbols," Eaton Corporation, August 2010. [Online]. Available: http://www.eaton.com/ecm/idcplg?IdcService=GET_FILE&dID=338822. [Accessed 10 April 2016].

[13] Analog Devices, "MT-068: Difference and Current Sense Amplifiers," [Online]. Available: http://www.analog.com/media/en/training-seminars/tutorials/MT-068.pdf.

[14] A. R. Hambley, "Differential and Instrumentation Amplifiers," in *Electrical Engineering Principles and Applications*, 5th ed., Upper Saddle River, New Jersey: Prentice Hall, 2011, pp. 693-695.

[15] P. Enjeti and S. Kim, "A New DC-Sider Active Filter for Inverter Power Supplies Compensates for Unbalanced and Nonlinear Loads," Texas A&M University, Dearborn, MI, 1991.

[16] Analog Devices, "Analog Filters," in *Basic Linear Design*, Norwood, MA, Analog Devices, 2006, pp. 8.21-8.107.