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Design of an Efficient Wall Adapter

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Efficient Wall Adapter

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Abstract

This report presents a design for an efficient AC adapter that uses 85% less power than conventional adapters when idle, for an additional cost of only $1.21. The design exceeds the team's initial targets of 75% increased power efficiency at a cost of $1.30. The team logically derived the final polling design from three initially proposed solutions. This project addresses the inefficiencies of modern AC adapters, whose increased utilization has become an increasing detriment to both economy and environment.

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Component Samples

Coilcraft	A9619-C Flyback Transformer
	RFB0807-102L EMI Inductor
ON Semiconductor	NCP1011 Monolithic Switcher
Vishay	SFH-615A-4 Optocoupler

Executive Summary

The world today faces many challenges regarding the use of energy and its conservation since the shortage of fossil fuels is becoming an increasing reality. As mobile devices have woven themselves into the fabric of society, the collective energy wasted in powering handheld electronics has become a global issue. Most of the energy wasted while charging a mobile device occurs within the charger, which is also known as an AC adapter.

AC adapters are devices that transform high-voltage, alternating current energy from a wall socket into a low-voltage, direct current form that is usable for several appliances at home and in the office. Larger appliances, such as television sets, dishwashers, and refrigerators are designed with this device internally. Small electronics, such as mobile communication devices and compact appliances, are designed to use external adapters to minimize product size and allow for mobility. Adapters alone have evolved greatly throughout their existence. Original, linear designs of an adapter were highly inefficient with regards to power consumption. Therefore, most modern adapters utilize a switching application to transform the high voltage with a high frequency to the DC output. Switch-mode power supplies (SMPS) are able to use smaller transformers for power conversion as a result. Moreover, smaller transformers operate at a higher efficiency than linear transformers.

While much progress has been made to improve the design and efficiency of modern power adapters, one critical drawback remains inherent within the circuit. Normally, mobile devices are connected to adapters for only a matter hours before they are disconnected. When a mobile device is disconnected from the charger, it may be assumed that the adapter deactivates itself until later use. However, this is not the true behavior of an AC adapter. In reality, the adapter remains active, supplying power to most of the circuit. Although smaller, high-efficiency transformers are being used in modern adapters, they continuously consume a majority of the power when no devices are connected to the adapter. Unless an adapter is disconnected from the wall socket, internal components draw and dissipate power.

On an individual adapter basis, the amount of energy wasted per year is negligible ($0.64 of energy per year). However, there are hundreds of millions of adapters in use today, mainly attributed to the increase of cell phones and PDAs across the globe. In effect, millions of dollars are spent on wasted energy every year. Therefore, a demand exists for an efficient wall adapter that limits the amount of

energy wasted during no-load conditions. The large-scale incorporation of such a device would benefit the planet both economically and environmentally.

This project focuses on improving the design of the modern adapter in order to create an efficient model. In the early stages of the product, a list of specifications was created for the new efficient AC adapter to follow in order to be a viable alternative:

- Negligible increase in adapter sizes with little additional circuitry
- A target energy efficiency improvement of 75%
- Additional cost to consumer no greater than two-year cost for wasted energy (i.e., $1.30)
- Fully-integrated solution (not to be marketed as separate device)

After performing research on the product's prospective demand on the market, the team researched existing adapter designs. Once an adapter model had been chosen from ON Semiconductor, the team designed a test bed according to the model's specifications. Next, three possible approaches to designing an efficient wall adapter were formulated: *Polling Timer*, *Jump Start*, and *Hijack*. After further review, the team decided that neither the *Jump Start* idea nor the *Hijack* idea would be pursued as a general design approach for the project. The *Polling Timer* involves the use of timing circuitry to periodically re-enable adapter functionality during standby conditions so the system may check for the presence of a load. A high-level functional diagram of the *Polling Timer* is shown in Figure ES-1.

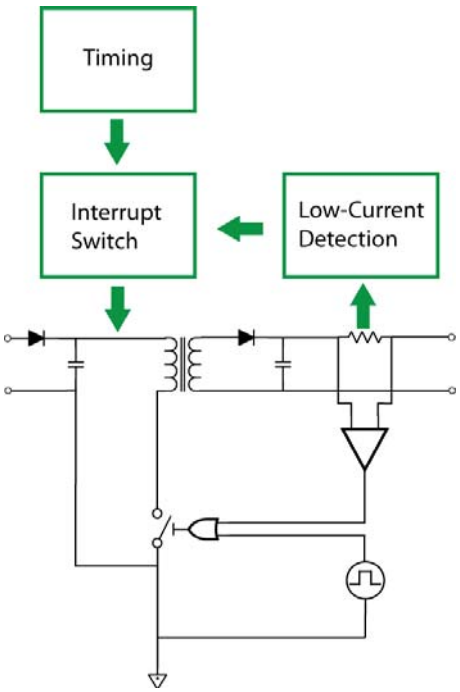

Figure ES-1: *Polling Timer* Functional Diagram

The low-current detection measures the output current level while the adapter is activated. Accordingly, the timer triggers the interrupt switch to disconnect the input of the adapter from the transformer.

Within this approach, the team developed two methods to achieve a polling function in the circuit: 555 timer and a capacitor. The capacitive-polling technique was investigated, but was deemed too expensive as well as inefficient. Therefore, the team began to implement a 555-based polling timer. Once a working design was achieved, the team collected power measurements to compare the new design with the original adapter test bed. While only marginally increasing power during charging mode, the efficient adapter design improved standby power consumption by 85% for an additional cost of $1.21. Since the solution is also compact in size and fully-integrated into the original adapter, all the necessary design requirements were met for the project.

In future efforts to improve adapter design, the team hopes that one not only improves the efficiency of the proposed adapter, but also makes it more cost effective. It is critical that the additional cost to the consumer be as small as possible in order to encourage either separate purchase or to entice electronic manufacturers to include an efficient adapter design in their chargers. On another note, future teams should further investigate the possibility of passive polling using a storage component such as an inductor or capacitor. If passive polling can be realized, it would further decrease the standby power consumption over time, since no active devices would be in use. However, the team's overall hopes are to further increase the awareness of wasted energy in electronic devices' standby power consumption, so the world can pursue alternative fuel sources and mitigate its dependency on fossil fuels.

The outcome of this project is an efficient wall adapter that meets the following specifications:

- **85% reduction of standby power consumption over original design**
- **$1.21 additional component cost which fell within the project's budget of $1.30**
  Fully-integrated, compact design that negligibly affects spatial dimensions of adapter

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Introduction 1

Today's world faces a widespread problem regarding the conservation of energy resources. Global warming and the increasing scarcity of fossil fuels have highlighted the importance of this issue and its impact on humanity [1]. Possible future repercussions of a fossil fuel shortage have lead to initiatives to develop energy-efficient cars and appliances, as well as an increase in renewable energy utilization [2].

Many of the items that require energy from fossil fuels are modern necessities in society. Automobiles have become the world's primary conveyance, home appliances perform everyday household functions, and artificial lights illuminate offices and homes everywhere. In order to operate more efficiently, designers of these products are working constantly to minimize energy consumption of electronic devices. For instance, the automotive industry is in the process of designing cars that consume less gasoline while idle [3]. The U.S. Government's ENERGY STAR program stipulates low-power specifications for a variety of household appliances [4]. In addition, several countries have legislation in place to ban the production and sale of incandescent light bulbs, which are notoriously inefficient [5].

Appliances in the home rely on electrical energy to perform specific tasks. Many household and office appliances use power adapters to transform high-voltage electrical energy into a workable form. Most adapters take the standardized 120V alternating current (AC) voltage from a wall socket and convert it to a low, direct current (DC) voltage. Larger appliances such as televisions and desktop computers have their power adapters located internally within the device. Smaller electronics, such as cell phones, utilize external power adapters to maintain compactness in design. Traditionally, these external adapters are called AC adapters, and serve a great purpose in powering commonly-used devices around the globe.

The market for consumer electronics is rapidly expanding on a world-wide scale, evolving toward a seemingly universal goal: portability. What was once a stereo and record collection has been condensed to a handheld MP3 player. Mainframes and personal computers have proliferated as laptops and PDAs. In the 1980s, AT&T's primary source of revenue was Plain Old Telephone Service (POTS) and their budget rivaled that of the fifth largest economy in the world [6]. Two decades later, cellular phones have taken over the communications market with a total of 2.3 billion global subscribers in 2007

and an estimated 3.96 billion by 2011, over half of the world's population [7]. However, portability of electronic devices heavily depends on the need for portable power. Therefore, the use of AC adapters around the world has grown significantly in the past 10 years. According to the United States Environmental Protection Agency, "as many as 1.5 billion power adapters are in use in the United States, about five for every American" in 2005 [8]. Each adapter supplies the power that drives the portable electronics world we live in today, but also provides an additional byproduct that adversely affects our planet.

The Problem 1.1

Due to escalating energy costs and the shortage of fossil fuels, a strong emphasis is being placed on the energy efficiency of AC adapters. In fact, external adapters have been referred to as *energy vampires* because they constantly consume power, regardless of load connectivity [9]. Granted, the power wasted by a single adapter is negligible, but AC adapters have a widespread application across the portable electronics market, posing a large-scale issue.

Anytime AC power is transformed into DC power, energy is wasted through losses by internal components. Not only does this occur while a load is connected to the adapter but also during no-load conditions. In fact, power is constantly drawn and dissipated by the adapter's internal circuitry as long as it is connected to an AC power source. The transformer inside the adapter, which converts the high voltage input into a lower voltage signal, consumes a majority of the energy during standby. The remaining components also contribute to the wasted power consumed every day without an end purpose.

Today's consumers are reminded that they should unplug their chargers from the wall when they are not in use [10]. However, even if one conscientiously practices this habit, it places too much burden on the consumer to conserve energy. Turning off a light in an unoccupied room is an easy task, but adapters are often located in tight quarters and are not readily accessible (e.g., behind furniture). Common sense dictates the need for a practical solution involving an automatic control system for the modern AC adapter, making decisions regarding the system's power state according to the presence of a load. It seems necessary to design an efficient wall adapter that will fit into a society of convenience. A closer look into its marketability will show that the world demands the incorporation of such a device.

The Economics 1.2

The cell phone industry has boomed during the last decade by enormous proportions. Between 1995 and 2005, wireless subscribers in the U.S. have increased by 174.1 million [11]. Figure 1-1 illustrates the rapidly increasing number of wireless subscribers in the United States.

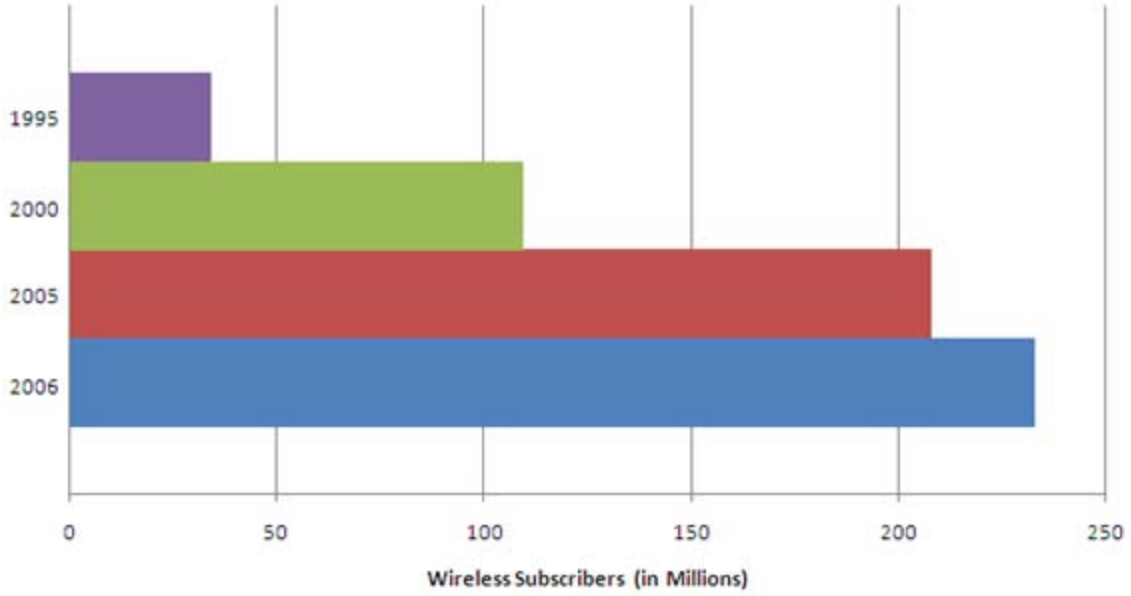


Figure 1-1: Wireless Subscribers in United States in the years 1995, 2000, 2005, and 2006 [11].

According to the Cellular Telecommunications Industry Association (CTIA), 76% of the United States population owns a cell phone, translating to 233 million wireless subscribers in 2006 [11]. Since almost every cell phone has its own adapter, approximately 233 million mobile phone chargers are also in use across the country. Assuming all of these adapters remain plugged in year-round and their no-load power consumption follows the ENERGY STAR standard of 500mW [12] on average, the total power consumption of ordinary cell phone adapters is equal to:

$$\frac{0.5\ Watts}{1\ Charger} \times \frac{24\ Hours}{1\ Day} \times \frac{365\ Days}{1\ Year} \times 233{,}000{,}000\ Chargers = \frac{1.02\ TWh}{1\ Year} \quad (1\text{-}1)$$

While this figure may seem impressive, it is only a small percentage of the total U.S. energy consumption, which equals around 30000TWh yearly [13]. On the other hand, the ENERGY STAR website mentions that a total of 300TWh of energy flows through all external power adapters every year [14]. Figure 1-2 shows that this amount accounts for 1.01% of the national energy consumption.

Therefore, it is important to realize that despite zero-load consumption of cell phone adapters constituting only a small fraction of total adapter consumption, the creation of an efficient wall adapter could provide long-term savings. ENERGY STAR predicts a potential energy savings of 5TWh if all adapters were designed to their idle power consumption standard [15]. This notion introduces the first potential market for efficient wall adapters: national governments.

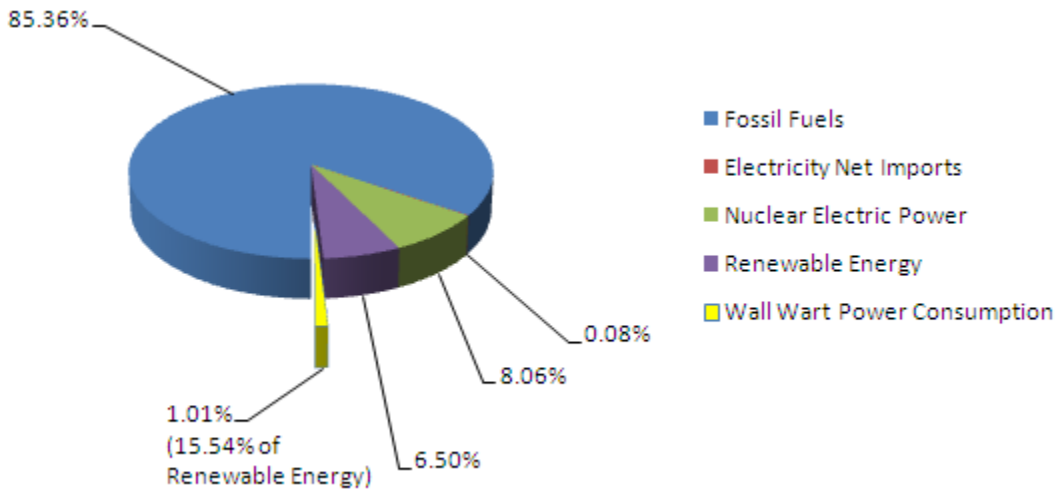


Figure 1-2: Energy Consumption Breakdown in the United States for 2005 [13].

In the United States, the ENERGY STAR campaign is the most publicized program for power efficiency. In Europe, the European Commission (EC) Code of Conduct on Energy Efficiency of External Power Supplies provides guidelines for power-saving adapters [16]. The code specifies a plan to reduce zero-load consumption for all external power supplies consuming fewer than 60W of output power to 300mW. The EC believes they can reduce zero-load power losses by 5TWh per year if all adapters meet this requirement starting in 2010. The prospective savings would be 500 million euro [16].

National governments may also assist in developing potential markets. For instance, the United States has environmental and energy agencies that would be compelled to recommend an efficient wall adapter to be used in cell phone charging applications (e.g., ENERGY STAR). Moreover, if the product can be patented or approved, governments have the ability to pass legislation mandating its distribution. For example, on December 18, 2007, the United States Congress voted in a new energy bill that will reduce the country's dependency on oil and increase the utilization of alternative energy sources [17]. The provisions of this bill call for automobile and lighting products to become more

energy-efficient. Automobiles will be required to consume an average of 35 miles per gallon by the year 2020, and lighting products will be forced to meet ENERGY STAR standards by the year 2012 [17]. The downside of marketing to national governments is the delays inherent in passing the necessary legislation. However, there are several other potential markets that could be pursued concurrently.

As mentioned previously, and illustrated in Figure 1-2, power adapters do not occupy a significant percentage of the total energy consumption in the United States [13]. These figures seem to imply that the consumer's incentive will not be centered on short-term economic savings, but on long-term economic and environmental benefits. If the efficient wall adapter costs $2.00 more than present models, and if electricity costs equate to 14.6 cents per kWh [18], then it would take three to four years to recover the difference in cost. However, since energy costs continue to rise due to the increasing scarcity of resources, the economic savings will also increase. If the adapter could be manufactured at a smaller premium (e.g., $1.00), the energy savings would cover the additional cost within one or two years, which is the typical duration of a cellular phone contract [19]. Such an inexpensive, efficient adapter could easily become a neutral value proposition to the consumer on a purely monetary basis.

Conversely, the corporate market's incentive for a more efficient wall adapter differs from that of the everyday consumer. Cell phone manufacturers such as Nokia and Motorola look to entice customers to buy their products using different marketing schemes. Many of these manufacturers market their products from a *green* angle (i.e., an environmental friendliness standpoint), in order to appeal to the consumers' morality or concern for the environment [20].

An overview of the economics landscape suggests that a more efficient wall adapter would be generally welcomed. Although the improved design may not be particularly attractive to the average consumer, corporations involved in the retail of small electronics would invite such a device. Furthermore, the marketability of a low-power adapter could benefit greatly from newfound federal impetus for energy legislation [17]. Overall, there appears to be global demand for a more energy-efficient AC adapter from a variety of sources.

Specification Goals 1.3

The following objectives were established at the beginning of the project in order to provide guidelines for the final product:

- Universal Application

AC adapters have a wide variety of applications, so it follows logically that numerous variations have been designed. Therefore, the project's implementation should be universal so that it may apply to all external power adapters. The fulfillment of this objective requires the product to consist of mostly basic components, such as resistors, capacitors, inductors, and transistors. Using simple electrical parts minimizes complexity and possible incompatibilities with certain designs. In addition, the utilization of basic components allows the product's size to remain as compact as possible. It should be noted that devices such as transformers and relays can considerably increase the size of an existing adapter.

Although the project's aim is to develop a universal product, the scope of the project concerns adapters utilized in North America ($120V_{RMS}$, 60Hz input).

- Fully Integrated Solution

The anticipated, high-efficiency product could be based on two distinct implementations. One design consists of an intermediary device that would placed in series between the wall and an external power adapter. Another design involves an integrated modification within the adapter itself. The first solution provides an easy way for the consumer to improve the efficiency of existing adapter models. As a result, new, more efficient adapters would not have to be purchased. However, this option has a few setbacks. The overall cost of implementing such a device would be an expensive investment compared to the integrated solution. Moreover, some modern wall adapters are designed with physical casings that cling to the wall when plugged into an electrical socket, invoking the term *wall warts* due to the way they bulge from the wall [9]. Consequently, adding a device between the *wart* and the wall would only increase the bulk of the implementation and reduce aesthetics. Furthermore, it is likely that modifying the adapter's internal circuitry would provide more opportunities for increasing the efficiency of the system compared to its external counterpart. These considerations were significant enough that an internal, fully-integrated solution was chosen as the best implementation for the design.

- Added Cost of $1.30

Energy Star-endorsed wall adapters consume a maximum 500mW of power, equivalent to approximately $0.64 over the course of a year. The typical cell phone contract term, which frequently

represents the lifetime use of the associated cell phone, is two years [19]. Therefore, it can be assumed that the consumer would break even economically by the end of their contract if the additional cost of an efficient wall adapter is less than $1.30. Consequently, a neutral cost proposition increases the appeal of an efficient wall adapter.

- Minimum Idle Power Reduction of 75%

Ideally, the efficient wall adapter designed in this project will consume 0W of power during idle conditions. However, the economic and spatial constraints established in previous specifications affect the plausibility of achieving ideal functionality. Therefore, the team decided that the product should be designed to consume at least 75% less power than the efficient models currently on the market. This reduction will be maximized if passive components are predominantly used throughout the solution, since a circuit containing mostly passive parts will consume less power during idle times compared to a configuration with several active devices. The more the adapter reduces standby power consumption, the more the consumer benefits economically.

- Maximum Output Threshold Current of 15mA

In order to determine whether a load is connected at the DC output of the adapter, sensing circuitry is needed to measure the output current within a specified range. Therefore, the current detection circuit must be able to alert the necessary components when the output load is nonexistent. In order to achieve this functionality, the sensing circuitry must be designed around a threshold level of current. The threshold must be signficantly less than the minimum current drawn by a connected load while large enough for the low-current sense to measure. The minimum level of current drawn by a battery load to maintain a full amount of charge is called *trickle current*. Although adapter trickle currents vary, the smallest trickle current rate uncovered during research was 3% of the battery's capacity per hour [21]. If a small cell phone battery (900mAh) is connected to the adapter, then the trickle current would be around 27mA. Therefore, the team chose a value of 15mA as the maximum threshold current, which is about half of the lowest observed trickle current. Figure 1-3 below shows the relationship between the output current and the output voltage of the sensing circuit. For this particular cell phone, the trickle current is around 30 mA. At $t_{DISCONNECT}$, the phone is disconnected from the adapter. Once the current decays past the threshold current of at least 15 mA, the output of the current sensing circuit will switch from logic *low*, or 0V, to logic *high*, or a 5V level. It is important that

the current sensing circuit output remains low when the phone is connected so the battery is able to maintain its charge.

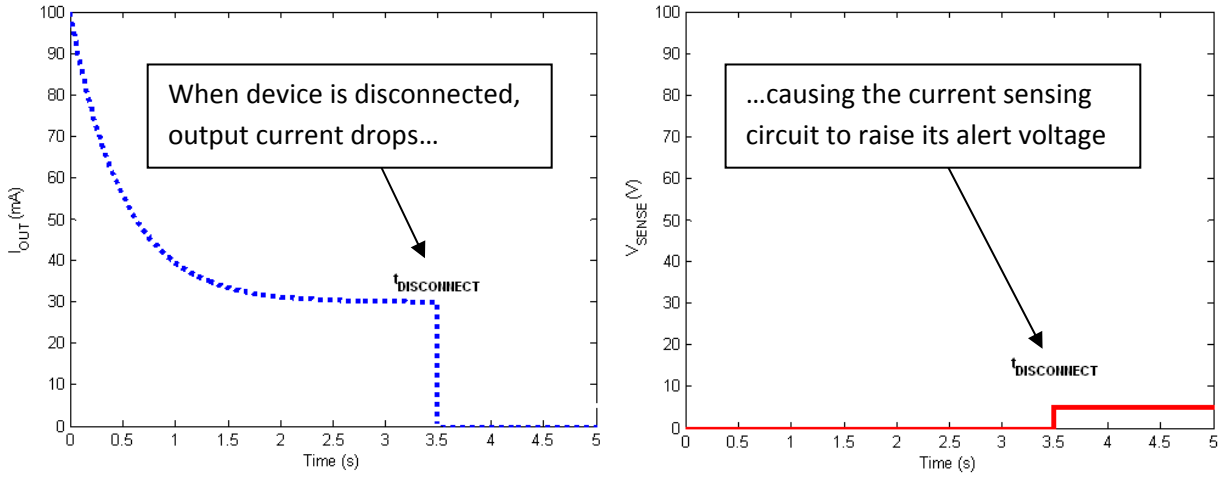


Figure 1-3: Adapter output current (left) and the current-sensing logic output voltage (right) versus time. The load is disconnected from adapter at $t_{DISCONNECT}$, causing the output current to drop, and the current-sensing alert to rise.

Collectively, these specifications constitute the team's efforts to design an efficient wall adapter that will enhance society both economically and environmentally. Over the course of this project the team has designed an adapter that meets all of its goals. It is a modular design that can be integrated into any AC adapter, and deactivates itself when the adapter's output current drops below 15mA. In addition, the team bettered its cost goal with a **final cost of $1.21** per 1000 units. Most significantly, the adapter's **idle power consumption was reduced by 85%** over the original adapter model, which is one of the most efficient adapter designs on the market today. The remainder of this report explains how the team managed to achieve and exceed these goals.

The ensuing chapter addresses the background of the project, including a summary of modern switch mode power supply design as well as the assembly and analysis of the adapter test bed. The third chapter describes the team's three top-level approaches to designing an efficient wall adapter. Three proposed solution ideas are discussed and subsequently narrowed down to the modified adapter's most basic stages: current detection and power disconnection. Chapter 4 describes the specific circuitry used to implement the approaches specified in Chapter 3. The fifth chapter discusses results of the adapter design in terms of power savings, cost, and relevant output waveforms. Chapter 6 discusses the team's recommendations for future teams interested in improving this project's adapter design, while the seventh chapter concludes the report.

The Modern Power Adapter 2

After exploring the possible economic and environmental implications of an efficient wall adapter, the team became educated on the progression of power adapters over time. Several questions were asked prior to conducting this research:

1. *How do modern AC adapters work?*
2. *What previous efforts have been made in developing an efficient AC adapter?*
3. *Which adapter design should be chosen for testing and experimentation?*

Before designing a solution for an existing product, it is only customary to familiarize oneself with its functionality and internal components. It is crucial not only to understand the purpose of particular stages in the circuit, but to also understand the function of each component in the design. Secondly, the team felt it was necessary to investigate whether previous efforts had been made in developing an efficient wall adapter. For instance, it would be wise to analyze previous designs of AC adapters. If an existing design can be altered to improve efficiency, then the team's efforts would be a success. Lastly, the team chose an efficient wall adapter design to use as a test bed. Choosing an existing design with great efficiency allowed the team to manipulate and subsequently improve a present-day adapter.

Switch-Mode Supply Development 2.1

The need for transforming AC power into a DC signal has always had significance in electrical applications since Faraday introduced the first of its kind in 1831 [22]. The first power supplies were designed in a linear arrangement. A linear power supply takes the AC, high-voltage input and attenuates the signal using a step-down transformer. From the secondary winding of the transformer, the attenuated signal is rectified into the DC output signal. Figure 2-1 shows a top-level diagram of a linear power supply.

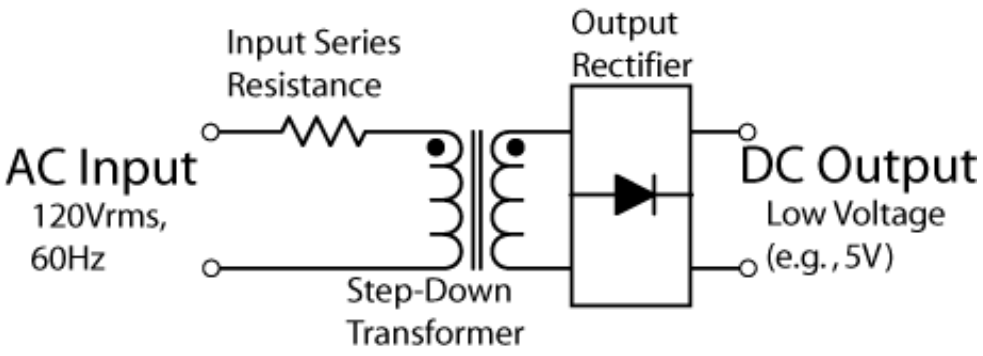


Figure 2-1: Shown is a top-level diagram of a linear power supply. The input, with series resistance, is directly connected to the primary winding of the transformer. The transformer attenuates the input voltage to a low-amplitude voltage on its secondary winding. Finally, the output rectifier with capacitive peak detection converts the AC signal into the DC output.

For many years, linear power supplies were predominantly used to operate electrical appliances. However, the significant downside in using a linear power supply is its poor power efficiency. Due to losses experienced in the transformer's primary winding and iron core, power delivered at the output is much less than the power supplied to the input. Therefore, large, expensive transformers are generally used in linear power supplies to cope with heat dissipated due to such losses [23]. For instance, large transformers are used on power lines to convert high-power electricity from the regional supplier to households across the United States.

Since the invention of the transistor in the mid-1940s, the power supply community has been investigating ways to use switching applications to reduce losses and minimize the size of adapters. Although the original theory was conceived in the 1950s, the switched-mode power supply (SMPS) did not come to fruition until the late 1970s [24]. At this time, IC manufacturers began creating controller ICs that performed high-frequency switching [24]. The inception of controller ICs in the SMPS allowed smaller transformers to be used in the design, effectively allowing the SMPS to become more marketable and cost-effective. Currently, the SMPS is now widely used in smaller-sized electronic applications, more so than its linear counterpart due to its compact design [24].

In SMPS design, switching is conducted at high frequencies for a couple reasons. As previously mentioned, the power losses in a SMPS are minimized if the frequency of the signal across the primary winding is high. In addition, the typical range of human hearing includes frequencies between 20Hz and 20kHz [25]. If switching occurred at a frequency within this range, there is a possibility of acoustic noise generation that would be irritating to the consumer. Therefore, a switching frequency between 50kHz and 150kHz is generally used in SMPS applications [24].

There are a multitude of SMPS designs used in modern adapters today. Figure 2-2 shows a top-level diagram of a common Flyback converter [26]. Beginning with a standard AC input of $120V_{RMS}$, the input rectifier converts the high-voltage AC into a high-voltage DC signal. Meanwhile, the monolithic switcher, driven by an internal flip-flop, switches the bottom node of transformer's primary winding from AC ground to the potential seen at the top node. The high-frequency, high-voltage signal on the primary winding is translated into an attenuated version on the secondary winding. At this point, operation continues in line with a linear power supply, rectifying the high-frequency signal into a DC voltage.

Often employed as a safety measure, switching power supplies will also include some level of current-sensing capability near the output. This circuitry sends feedback to the switching IC which is capable of shutting down in case the load attached to the adapter attempts to draw more current than the adapter can supply.

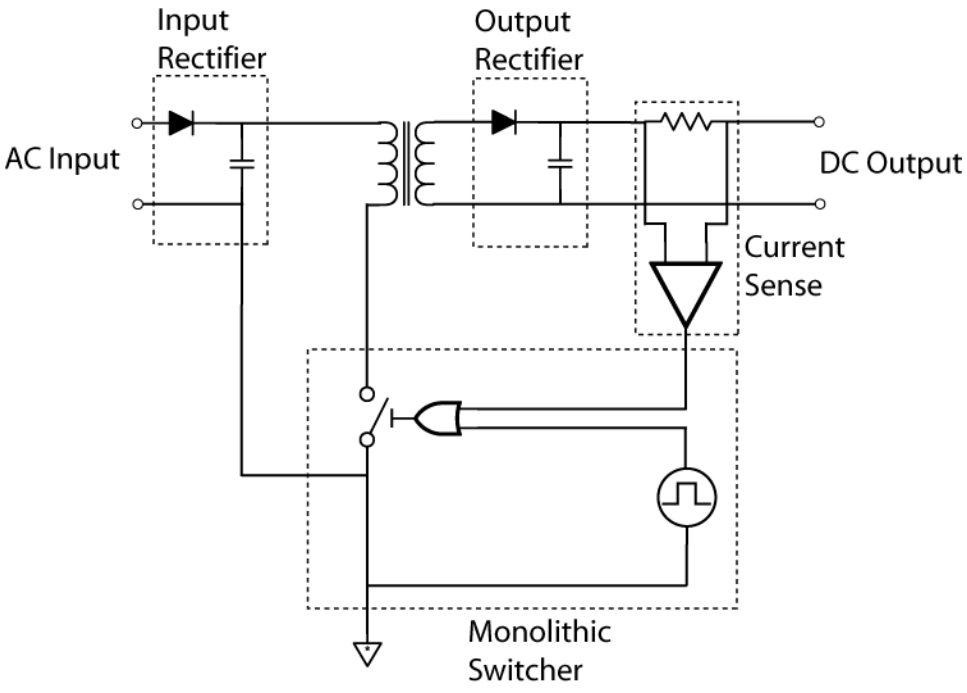


Figure 2-2: Functional diagram of a Flyback converter, representing the 5 principle qualities of modern power adapters; input rectification, high speed switching, step-down transforming, output rectification, and built-in overload current sensing [26].

Specific Example 2.2

In efforts to find an existing, efficient SMPS adapter, the team found a design note from ON Semiconductor, labeled as an *Efficient, Low Cost, Low Standby Power (<100 mW), 2.5 W Cell Phone Charger* [27]. Design note DN06017/D is filed as an application of the NCP1011 IC, or a *Self-Supplied Monolithic Switcher for Low Standby-Power Offline SMPS* [28]. Like the monolithic switcher described in Figure 2-2, the NCP1011 provides idle-state recognition for enabling a low standby power mode in addition to switching at a frequency of 100kHz. If the NCP1011 detects an idle condition at the output, the adapter transitions into a *skip-cycle* mode, reducing the duty cycle of the output during no-load conditions. Moreover, the adapter uses feedback from an output current-sensing circuit to execute its *latch-off mode* if an excessive amount of current is detected. During *latch-off mode*, the NCP1011 disables adapter operations for a period of time, after which the adapter is reactivated. In effect, the NCP1011 protects against possible permanent damage to the load and internal circuitry. The schematic for the adapter in design note DN06017/D is shown in Figure 2-3 [27].

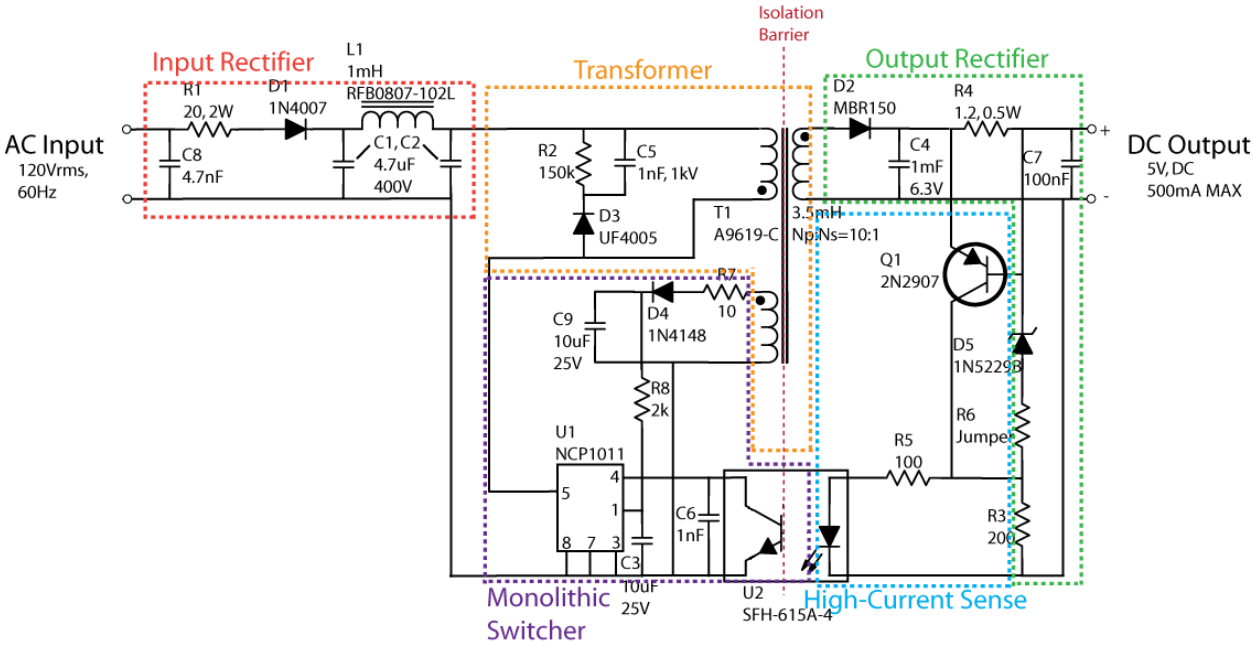


Figure 2-3: Efficient, Low Cost, Low Standby Power (<100mW), 2.5W Cell Phone Charger from ON Semiconductor Design Note DN06017/D [27].

This particular SMPS design follows the top-level diagram shown in Figure 2-2, with an input rectifier, transformer, output rectifier, high-current sense, and a monolithic switcher. After the input has been connected, AC voltage is rectified by diode D1, and filtered by the tank circuit arranged by inductor L1 and capacitors C1 and C2. The high-voltage DC signal of around 170V is then passed to the primary winding of the transformer. The NCP1011 uses power from its output pin (pin 5) for initial startup, charging capacitor C3 on its V_{cc} pin (pin 1). Once the charge on this capacitor reaches approximately 8.5V, the NCP1011 IC begins switching at 100kHz [28].

After the NCP1011 commences switching operation, pulses from 0V to 170V and 10µs apart are observed across the transformer. In order to save power, a transformer with an auxiliary winding is used to power the NCP1011 once switching begins. A simple diode rectifier (D4) is used with a filter capacitor (C9) to convert the AC signal into a DC signal. Resistor R8 and capacitor C3 constitute an RC timing circuit that controls the operation of the NCP1011. Capacitor C6 and device U2 are connected in parallel with the feedback pin (pin 4) of the NCP1011. U2 is an optocoupler used to provide feedback from the high-current sense on the DC side of the isolation to the monolithic switcher. During normal operation, the BJT in the optocoupler is in cutoff mode, applying a high resistance between pin 4 of the NCP1011 and AC ground. Capacitor C6 contributes to the isolation between these two nodes as well. If a sufficiently-high amount of current is detected at the output, U2 activates the BJT into saturation, effectively shorting the feedback pin of the NCP1011 to AC ground. If a ground fault is detected by the NCP1011 on its feedback pin, the chip transitions into *latch-off mode* [28]. Figure 2-4 shows a simplified block diagram of the NCP1011's functionality.

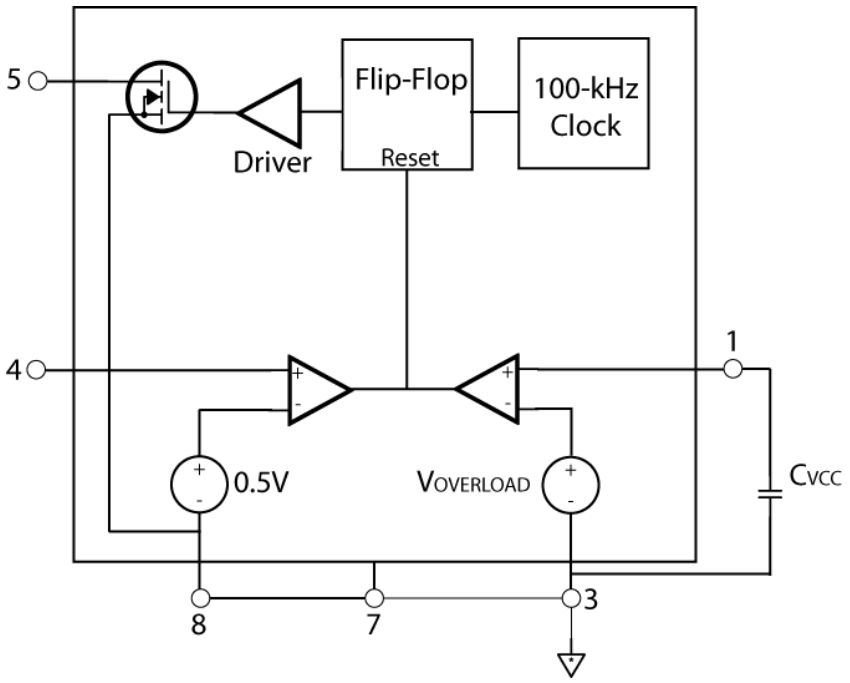


Figure 2-4: The simplified block diagram of the NCP1011's functionality portrays each of the three operating conditions. During normal operation, the power MOSFET driver is controlled by a flip-flop coupled with the 100-kHz clock, periodically reset by the V_{CC} capacitor when the voltage at pin 1 equals $V_{OVERLOAD}$. If pin 4 is grounded, signifying a high-current output condition, the Flip-Flop is reset. Lastly, the chip operates in *latch-off mode* when the charge/discharge cycle of C_{VCC} is extended during no-load conditions [28].

Capacitor C5, resistor R2, and diode D3 are arranged in what is known as a snubber configuration [29]. Snubbers are circuits that protect electrical components, such as transformers, relays, other inductive devices, and surrounding components from transient voltage spikes caused by current interruptions. When current to an inductive device is suddenly cut, the magnetic energy stored therein will naturally attempt to sustain current flow. This current, now inhibited by an open circuit, has the potential to build up brief, high-magnitude voltages that could stress or damage nearby components. For example, this effect can be seen in arching across relay contacts [29].

Since the large voltage spike is created in a reversed direction of normal operation, one of the most basic snubber designs is simply a diode installed in reverse parallel with the target inductive coils. This gives the current a small, but closed path to follow, preventing high voltages from occurring. There are also snubbers, such as the RC snubber, that use capacitors to control the voltage across the coils directly, rather than the current produced by them. The capacitor's transient nature performs a *controlled absorption* of the energy spike and typically dissipates it through a resistor [29].

The snubber in the NCP1011 power adapter model makes use of both the diode and capacitor snubber principles. It performs a helpful role for the output of the switcher as well, absorbing most of the output current upon shutdown. This decreases the peak power dissipation of the switcher by dissipating power through the snubber instead, thus increasing the reliability of the IC. Controlling the voltages in shutdown circuit operations has also been shown to lower the high-frequency electromagnetic interference potentially created by uncontrolled switching.

The DC stage of the circuit is implemented according to the top-level diagram shown in Figure 2-2. Diode D2 and capacitor C4 provide the output rectification required for AC-to-DC conversion. Capacitor C7 is placed in parallel with the output to filter out remaining high-frequency components in the signal. On the other hand, resistor R4 is placed in series with the top rail to provide a measure of the output current. As the load draws power from the adapter, the voltage drop across R4 is linearly proportional to the current. The base and emitter of PNP BJT Q1 are placed across this voltage drop. If the voltage drop reaches approximately 600mV, the output current level has eclipsed the 500mA maximum. At this point, Q1 is biased into the active region, sourcing current to the optocoupler U2. U2 notifies the switcher of the high-current condition and the adapter is subsequently deactivated.

Finally, to ensure a consistent output voltage regardless of component imperfections, the Zener diode D5 is place in reverse bias with respect to the top DC voltage rail. The rating on this particular Zener diode is 4.3V, so in order to achieve an output of 5V, resistor R3 of 200Ω is placed from the anode of D5 to DC ground to serve as a pull-up resistor. Resistor R6 is placed in the design as a means to further manipulate the output voltage, but is assigned a value of 0Ω to maintain a DC output of 5V [27].

It is clear that the SMPS contains a significant amount of additional components when compared to a linear power supply. In addition to switching controllers, feedback circuitry and additional diode rectifiers are among several added devices to the SMPS adapter design. Therefore, SMPS are marketable today because the cost of the smaller transformer and additional parts is much less than the cost of the large, linear transformer overall.

Simulation 2.3

Once an existing adapter model was chosen as the project's test bed, it was necessary to simulate the design in PSpice in order to confirm functionality of each stage. Figure 2-5 shows the node numbering used in the simulation netlist.

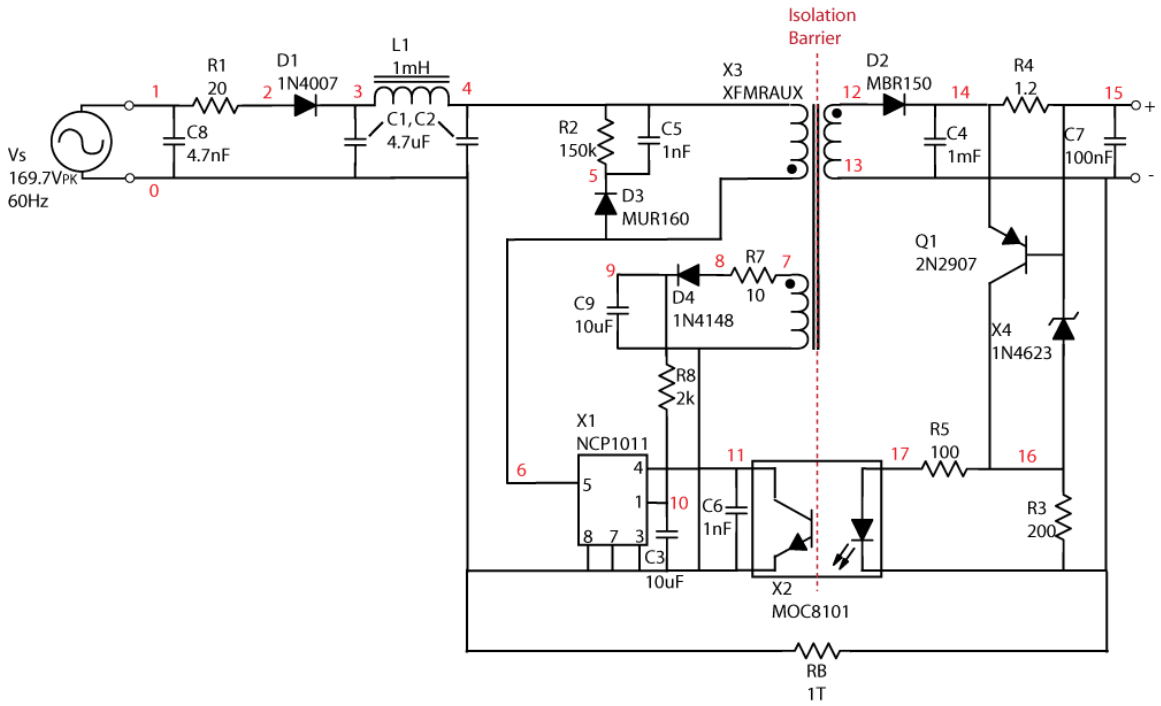


Figure 2-5: Schematic of adapter test bed from Figure 2-3; netlist used to perform PSpice simulation on entire system.

Due to the unavailability of simulation models for some components or the non-existence thereof, some of the semiconductor components as well as the transformer were modeled using different parameters. The netlist of the full adapter simulation can be found in Appendix C. All initial conditions for energy storage components (e.g., capacitors and inductors) were set to 0V for all simulations unless otherwise specified.

Results *2.3.1*

Simulation results of the full adapter simulation were accurate for some measurements while inaccurate for others. Figure 2-6 displays the output voltage behavior between 5ms and 15ms. The DC output climbs steadily at a rate of 367nV per 1ms. While this voltage increase is negligible compared to the expected output level, the behavior can be attributed to the voltage ripple produced by the input rectifier. The slight voltage variation is translated from the primary winding to the secondary winding, causing a steady output current to charge the output filter capacitors C4 and C7.

Figure 2-7 shows the voltage at the V_{cc} pin of the IC climbing steadily toward 8.5V. The voltage across the primary winding can also be seen to be at a level of 169V, with the previously-mentioned voltage ripple produced by the rectifier affecting the stability of the signal.

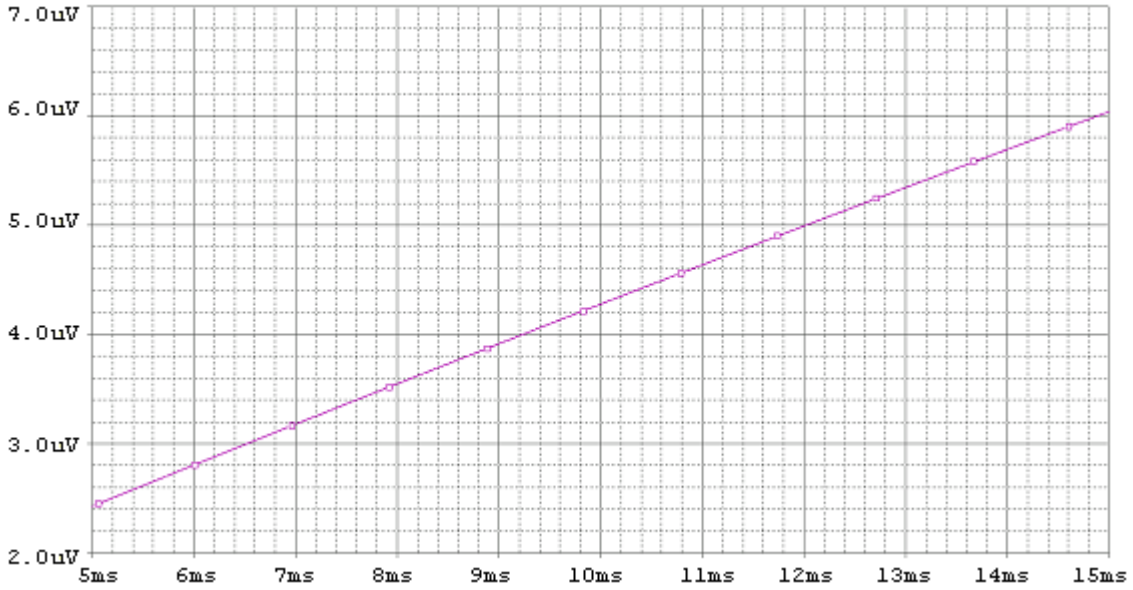


Figure 2-6: PSpice simulation results; output voltage of adapter versus time, prior to activation of switching IC. Output voltage increases linearly by 3µV, likely as a result of energy transferred by the input rectifier ripple through the transformer.

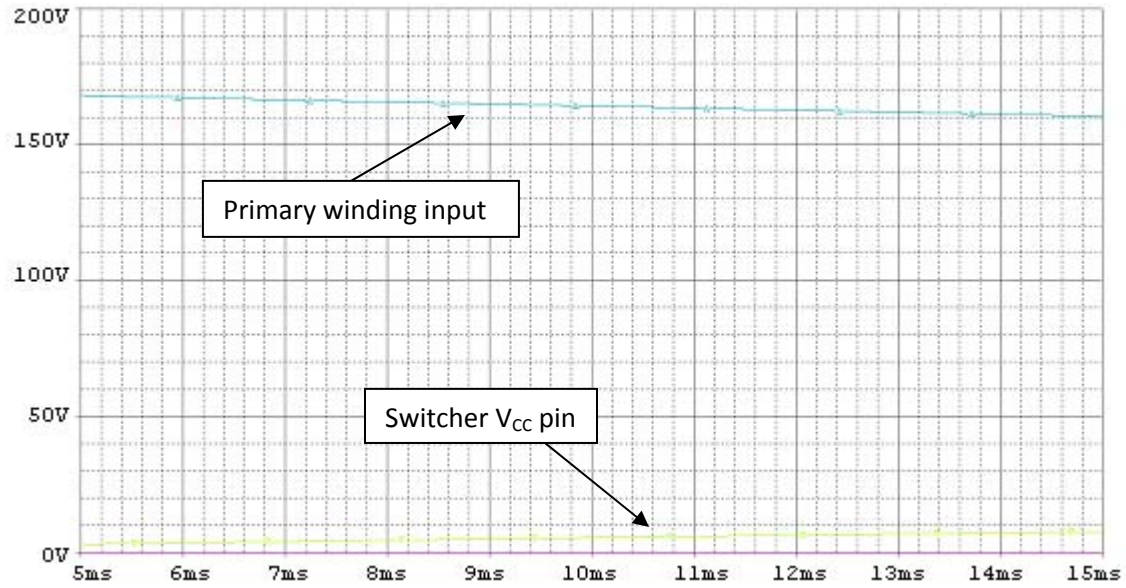


Figure 2-7: PSpice simulation results; input voltage at primary winding and Vcc pin on switching IC versus time, prior to activation of switching IC. Primary winding voltage remains close to rectified mains voltage, while the IC's power capacitor charges toward its activation trigger of 8.5V.

In order to observe the system's behavior while in normal operation, the simulation was altered to record data from 10ms to 20ms. Figure 2-8 shows the voltage at the V_{CC} pin of the NCP1011. After 17.2ms, the voltage at pin 1 reaches a level of 8.5V. The parabolic behavior between 17.2ms and 20ms of pin 1 can be attributed to the introduced output load once switching begins. However, after the startup time of 17.2ms has elapsed, the adapter begins internally switching, providing a high-frequency signal across the primary winding of the transformer. The voltage at pin 5 of the NCP1011, which is its output, is shown on the same timescale in Figure 2-9 and Figure 2-10. When looking at these plots, the team noticed an unusual level of voltage detected at the output of the NCP1011. In fact, Figure 2-9 shows a signal with an amplitude of $700V_{PEAK}$. The magnified plot shown in Figure 2-10 shows that 700V is reached during switching transitions from low to high. It was puzzling to understand why these spikes occurred, since a snubber is used in parallel with the primary winding of the transformer to mitigate voltage spikes. The team was unsure whether this phenomenon was a product of simulation or a true representation of circuit operation. The only way to verify either case was to conduct physical measurement on the system.

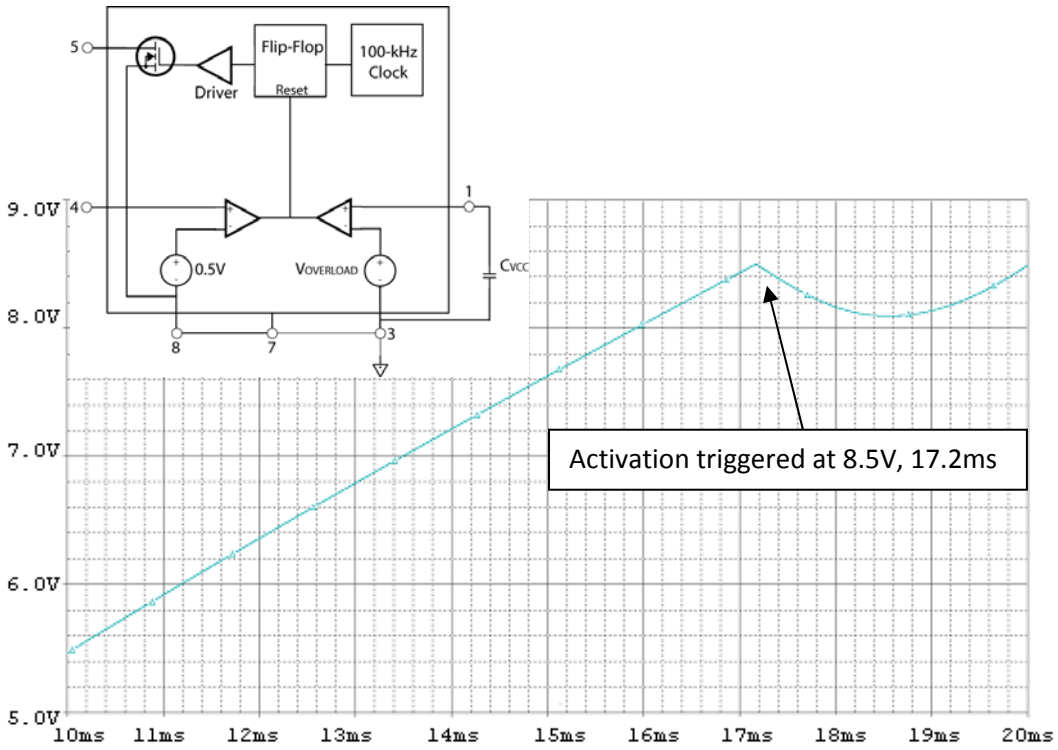


Figure 2-8: PSpice simulation results; voltage at Vcc pin on switching IC versus time. Voltage hits its activation trigger of 8.5V and begins oscillations. The V_{CC} pin is located on pin 1 of the NCP1011 block diagram.

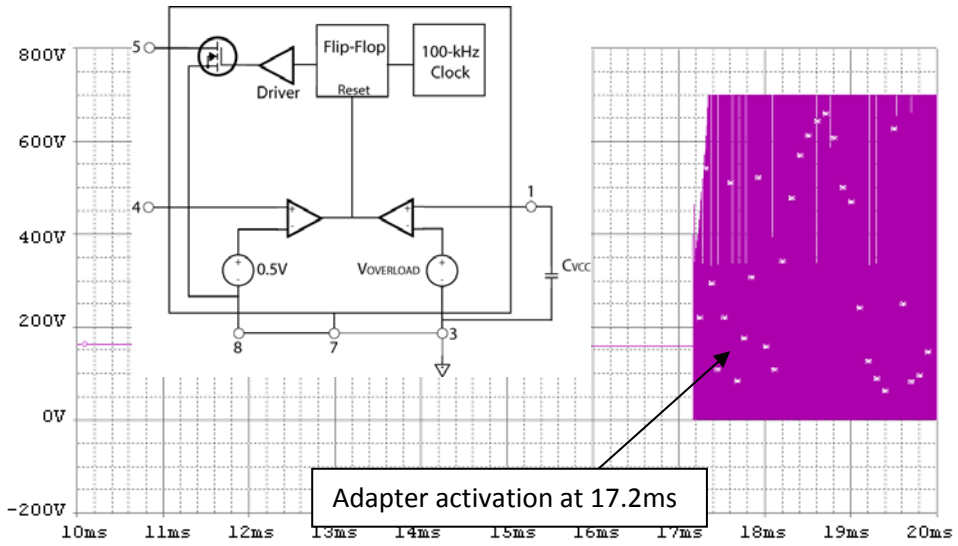


Figure 2-9: PSpice simulation results; output voltage of NCP1011 versus time. Switching begins when the voltage at the Vcc pin reaches 8.5V (Figure 2-8). The output of the NCP1011 is equivalent to pin 5 on the block diagram.

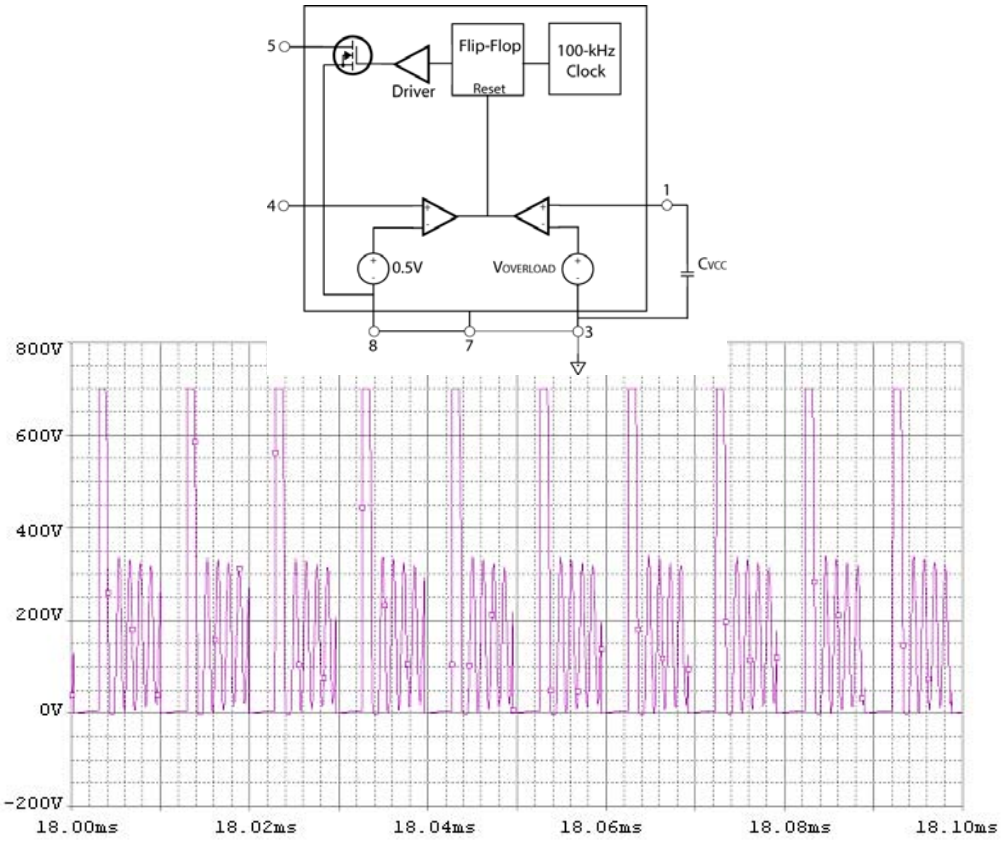


Figure 2-10: PSpice simulation results; voltage outputted by switching IC versus time. Same as Figure 2-9, but with a smaller time scale to show IC's oscillation pattern. The output of the NCP1011 is equivalent to pin 5 on the block diagram.

A plot of the adapter's DC output versus time is shown in Figure 2-11. At the critical time when the startup period ends (17.2ms), the adapter's output voltage rate increases from 367nV per 1ms to 50mV per 1ms. The output current is relatively constant due to a resistive load at the output, so the expected time the output voltage reaches 5V is around 100ms after adapter activation. Since a full simulation of 20ms requires a significant amount of time to run, the notion of conducting a simulation for 100ms is not plausible. Therefore, the team formulated a solution to provide an alternative way to simulate the adapter in a timely manner.

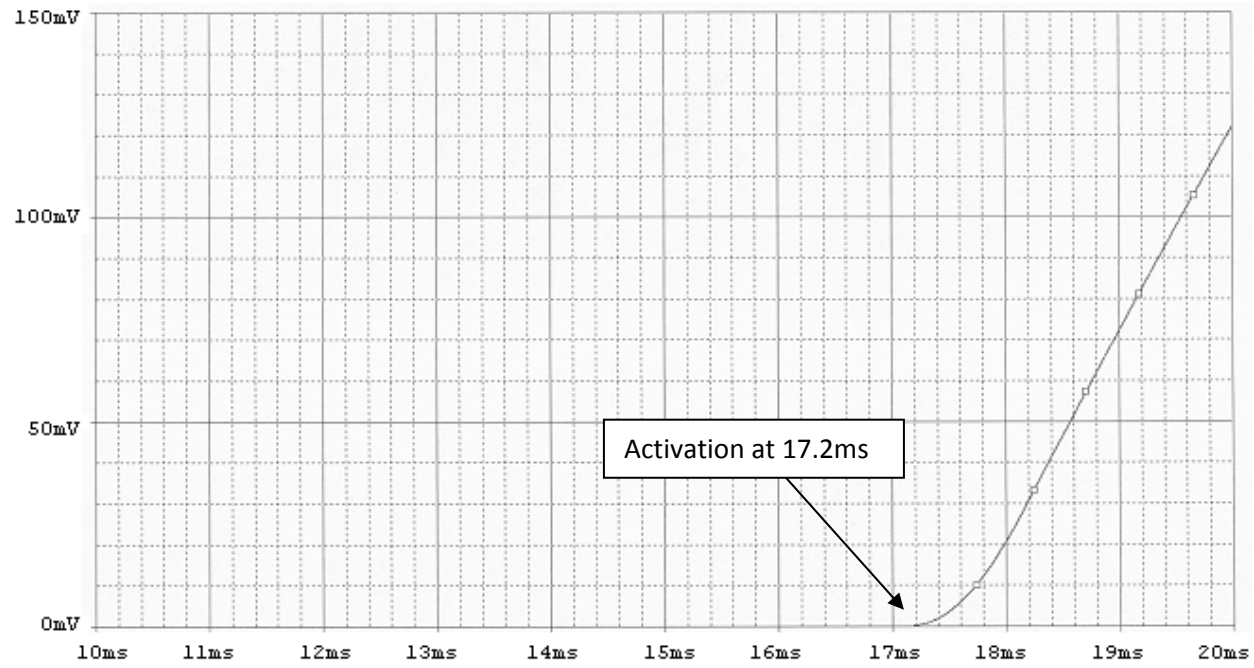


Figure 2-11: PSpice simulation results; voltage at the DC output of the adapter versus time. Again, switching IC activates at 17.2ms, causing the output to increase toward its eventual 5V level.

The team dissected the netlist in efforts to locate the source responsible for elongating simulation runtime. It was determined that the model of the NCP1011 IC provided by ON Semiconductor performed several calculations during simulations, shortening the time step significantly. Therefore, the IC would need to be replaced with a subcircuit that imitated its functionality.

In order to simulate the adapter in a more time-effective way while preserving the integrity of system functionality, the team modeled the NCP1011 using a pair of controlled switches. A voltage-controlled switch (S1) was used to switch the voltage through the transformer to ground at 100kHz. The feedback control subsystem was replaced by a current-controlled switch (W1). Since an auxiliary winding was not required to power the NCP1011 in the simplified model, the transformer was reduced

to a primary winding and a secondary winding. Figure 2-12 represents the configuration used for the simplified simulation. The PSpice netlist used in the simplified simulation can be found in Appendix C.

Initial trials of the simplified model of the adapter yielded promising results. Figure 2-13 displays the expected rectification of the AC input voltage, while Figure 2-14 shows the output voltage of the adapter between 0ms and 400ms. The voltage level converges at around 6V, which is 1V higher than the expected value. It is possible that this discrepancy is due to the Zener diode model used for the simulation (1N4623). It is noticeable that the simplified simulation was run much longer than the initial version. However, the runtime of the simplified simulation was significantly less than the full simulation, proving that ON Semiconductor's NCP1011 model was responsible for the team's initial simulation difficulties.

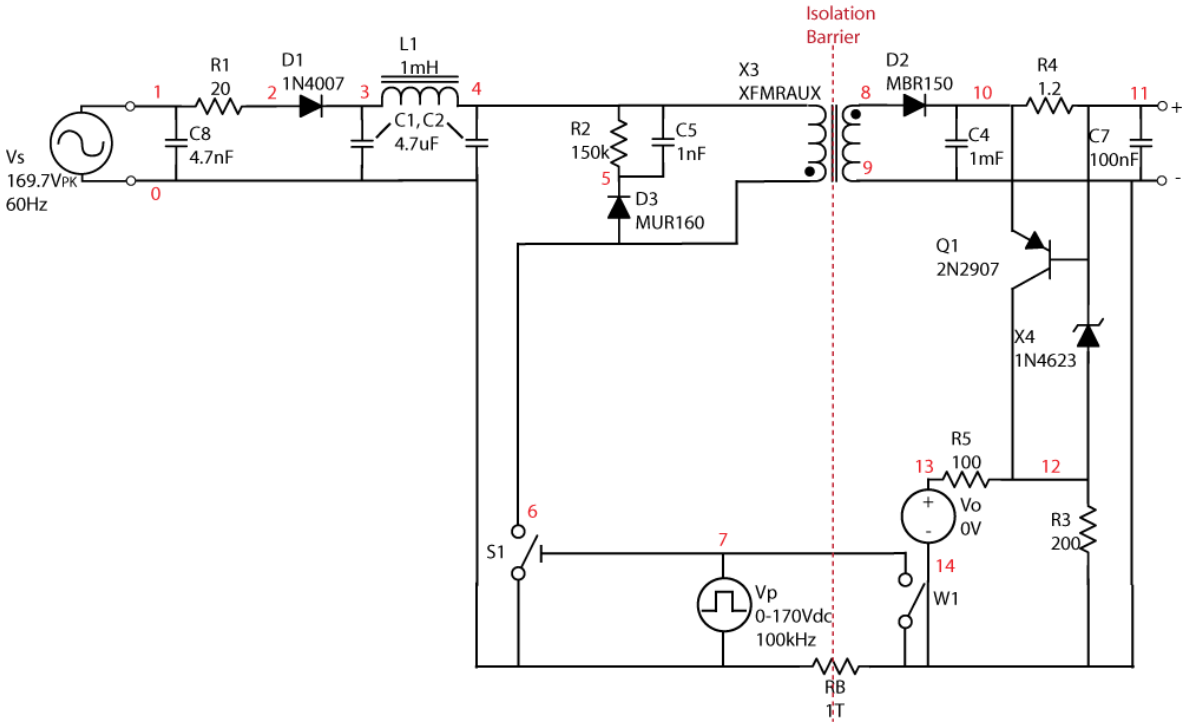


Figure 2-12: Simplified schematic of adapter test bed from Figure 2-3 used for netlist of simplified system, which was created for faster simulation runtimes.

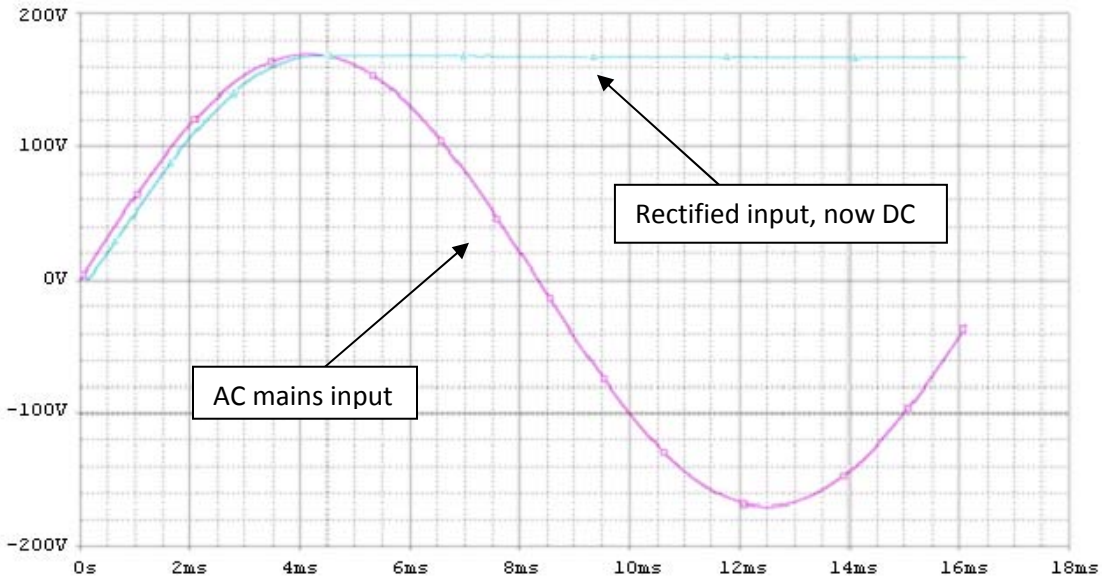


Figure 2-13: PSpice (simplified) simulation results; mains input voltage and rectified mains voltage versus time. Input voltage is rectified before being switched to 100kHz by switching IC.

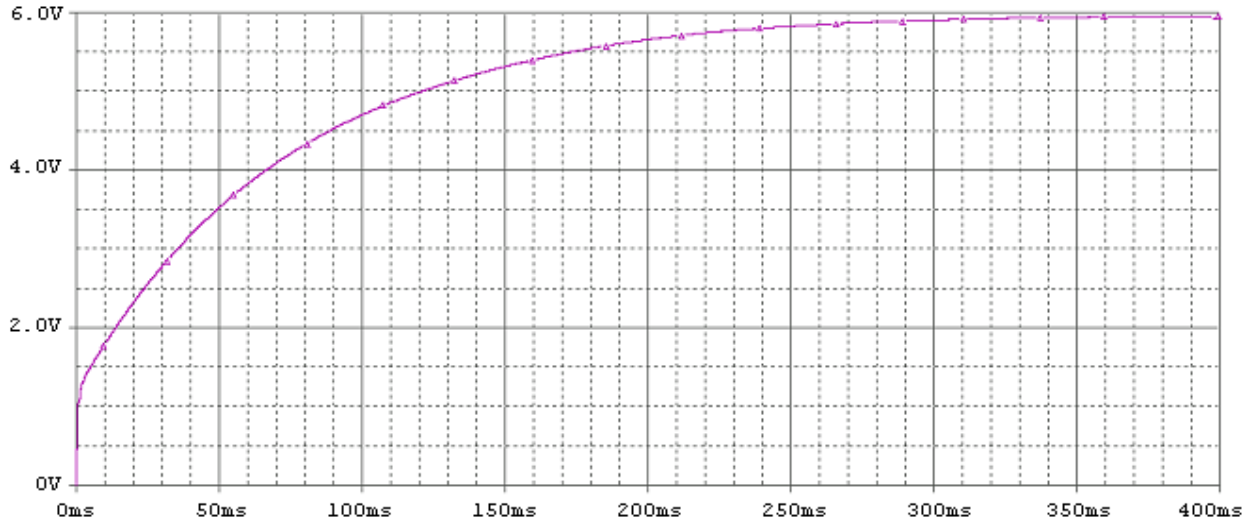


Figure 2-14: PSpice simulation results; voltage at the DC output of the simplified adapter versus time. Voltage converges at 6V DC within half of a second.

The team later revisited the complete adapter model in efforts to obtain results while expediting simulation runtime. In order to shorten simulation duration, initial conditions were applied to capacitors throughout the circuit. If voltages across the capacitors were preset above 0V, the team believed the time required for the output voltage to reach 5V would be shortened. Therefore, the input rectifier capacitors were preset to 169V, since the 169.7V_{PK} AC signal will be rectified to a 169V DC

signal. Output filter capacitors were set to maintain a level of around 5V, since this is the expected output voltage level.

However, some problems were experienced in the first trial with initial conditions applied to the various capacitors. Specifically, an error was observed indicating *overflow: convert*. In the second trial, the initial conditions of the output capacitors C4 and C7 were reduced to 1V while leaving the preset voltages of the input rectifier capacitors unchanged. Figure 2-15 shows the results of the second trial.

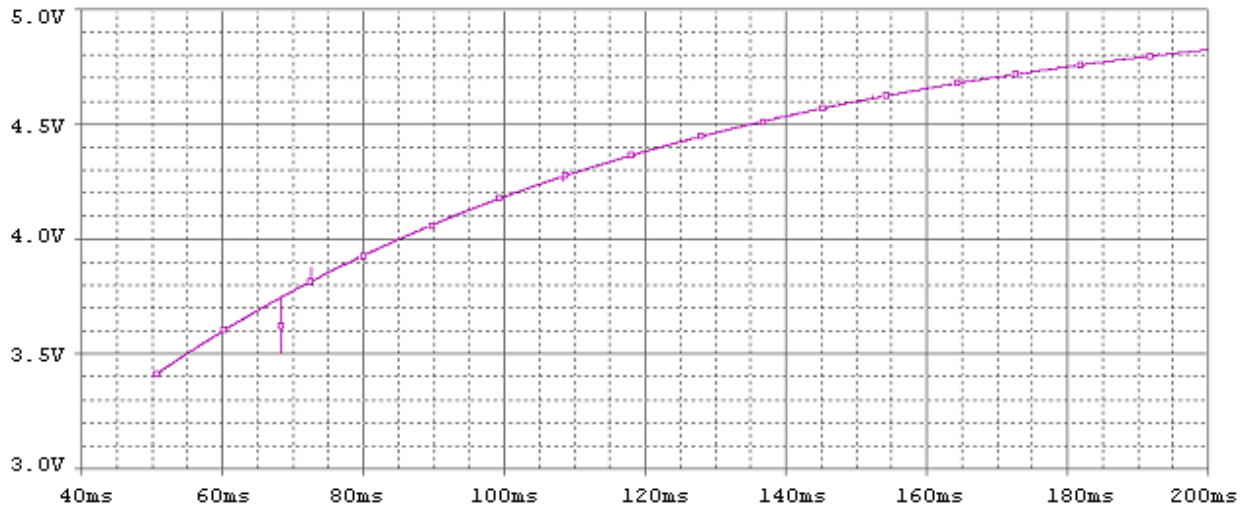


Figure 2-15: PSpice simulation results; voltage at the DC output of the simplified adapter versus time. Output filter capacitors were simulated with an initial condition of 1V, to shorten the time required to observe 5V at the output of the adapter.

The voltage waveform shown in Figure 2-15 is representative of the expected adapter output. The main takeaway from the team's simulations is the time required to observe the rated 5V at the DC output. Although the simulated time period may seem excessive, the large filter capacitor C4 explains why it may take a timescale of above 200ms to reach the appropriate value. Moreover, a timescale of 200ms is negligable to the user, so it is very plausible that the simulated timescale is representative of its actual value.

Simulation Challenges *2.3.2*

In addition to previous difficulties, the team experienced several other complications while running simulations. One of the first problems encountered by the team in its full simulation trials was PSpice's interpretation of isolated circuits. It was discovered that circuit connectivity checks in PSpice require paths to node 0 for all nodes. Therefore, isolated circuits such as AC adapters require a connection between DC ground and AC ground. However, a direct connection cannot be made since isolation between both stages must be preserved. The team found that placing a high resistance between AC ground and DC ground was common practice in simulating isolated circuits [30]. The large resistor RB of 1TΩ satisfies PSpice's connectivity requirements while preserving isolation between the AC and DC stages of the adapter.

Another complication of simulating the adapter was PSpice convergence issues. In one of the initial trials of the full simulation, PSpice reported issues in calculating voltages within the subcircuit model of the optocoupler. This problem was resolved by performing a transient analysis between 5ms and 15ms. The time delay of 5ms eliminated the effect of startup transients on the simulation results, and allowed PSpice to record data without difficulty.

Still another problem was found in the team's original model of the transformer. Initially, the transformer was modeled using a combination of voltage-dependent voltage sources and current-dependent voltage sources. Figure 2-16 shows both the modified transformer model and the original transformer used in PSpice simulations. Although voltage ratios were set according to specifications, the old transformer model failed to emulate true device operation since inductors were excluded from the subcircuit.

```
*New Transformer*
X3 6 4 12 13 7 0 XFMRAUX
.SUBCKT XFMRAUX 1 2 3 4 5 6
RATIO2=0.05
*PRIMARY
L1 1 2 2000
*SECONDARY
L2 3 4 20
L3 5 6 39.2
*MAGNETIC COUPLING
K12 L1 L2 0.99999
K13 L1 L3 0.99999
.ENDS
```

```
*Old Transformer*
X3 6 4 12 13 7 0 XFMRAUX
.SUBCKT XFMRAUX 1 2 3 4 10 11 PARAMS: RATIO1=0.1

RP 1 2 1MEG
E1 5 4 VALUE = { V(1,2)*RATIO1 }
G1 1 2 VALUE = { I(VM1)*RATIO1 }
RS1 6 3 1U
VM1 5 6
E2 20 11 VALUE = { V(2,1)*RATIO2 }
G2 2 1 VALUE = { I(VM2)*RATIO2 }
RS2 21 10 1U
VM2 20 21
.ENDS
```

Figure 2-16: PSpice transformer models, original noisy model (right) was replaced with an improved magnetically coupled model (left) [30].

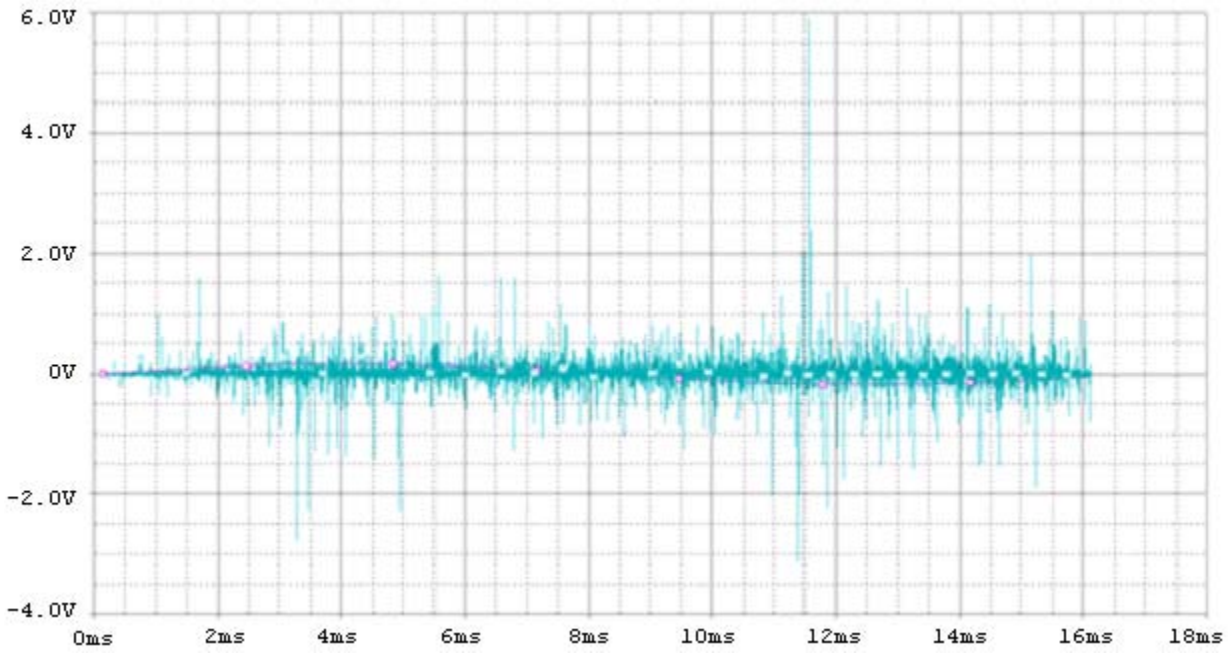


Figure 2-17: PSpice (simplified) simulation results; voltage at the DC output of the adapter versus time. This noise is likely the result of the simulation model of the circuit's transformer having an exaggerated reaction to the high speed switching of the IC.

Figure 2-17 shows the output voltage of the adapter when the old transformer model was used. It was clear that the high-voltage, high-frequency pulses experienced across the primary winding of the

transformer were not properly translated to the secondary winding. It was determined that although the old transformer model may be useful for low-frequency or low-voltage applications, it was not operating appropriately for the adapter configuration.

Therefore, a modified subcircuit, shown alongside the old model in Figure 2-16, was substituted in for the transformer [30]. The new model uses multiple inductors to represent the windings of the transformer and mutual inductance to emulate the magnetic coupling relationships between the windings. Inductor L1 is used as the primary winding in the subcircuit, with L2 functioning as the secondary winding and L3 as the auxiliary winding. An inductance of 2000H was chosen for the primary winding to minimize the effect of series resistance on transformer operation. The inductances of L2 and L3 were calculated using the following equation [31]:

$$\frac{L1}{L2} = \left(\frac{N1}{N2}\right)^2 \quad (2\text{-}1)$$

Since the turn ratio of the secondary winding to the primary winding is 0.1, the value of L2 is 100 times less than L1, or 20H. Similarly, the turn ratio of the auxiliary winding to the primary winding is 0.14, giving the value of 39.2H for L3. The new model of the transformer allowed the team to observe the waveforms presented in the results portion of the simulation section.

Despite the many complications experienced running the various simulations of the adapter, the team was able to obtain waveforms that resembled accurate representation of system functionality. In many electrical design projects, simulation is beneficial to determine behavioral irregularities within the circuit so troubleshooting can be done and adjustments can be made. However, the design of an efficient wall adapter consists of low-cost components, so physical measurements and adjustments can be made without spending a substantial amount financially. Therefore, the team used a trial and error approach to building the adapter test bed and implementing additional circuitry, using the results of simulation trials to reinforce their findings.

Test Bed 2.4

After running the full and simplified simulations, the team focused on purchasing the necessary parts to build an adapter prototype. Assembling the adapter described in ON Semiconductor's design note DN06017/D proved beneficial in several ways [27]. First, creating an adapter parts list allowed the team to see the total cost of building an adapter, in addition to comparing the prices of the various components. Second, the team discovered the physical space required to build an adapter while

delicately soldering the components onto a perfboard. Most importantly, the physical measurements conducted on the finished test bed helped verify as well as disprove preconceptions on system behavior. Therefore, this section is divided into the following three subsections:

1. *Preparing for adapter assembly by creating parts list and ordering necessary components*
2. *Assembling the adapter test bed on a perfboard and later a printed circuit board (PCB)*
3. *Recording measurements and waveforms from test bed to confirm overall behavior of circuit*

Preparations *2.4.1*

Before purchasing parts for the test bed, the team first created a list of all components to compare cost, distributor, and quantity. The parts list for the current, completed version of the test bed is given in Table 2-1 [27].

Table 2-1: The final revision of a parts list for the adapter test bed. To fit the table in this document, the manufacturer part number field has been excluded. The final cost of the adapter assumes that each part in the list is purchased in a bulk of at least 1000. The table is sorted by the total price of each component [27].

Quantity	Label	Part Type	Value	Distributor	Distributor Part #	Unit Price (1000)	Total Price
1	T1	Transformer	3.5 mH	Coilcraft	A9619-C	$1.680	$1.680
1	U3	IEC AC PCB	Pin	Mouser	693-GSP2.8101.13	$1.150	$1.150
1	U1	Switcher IC	NCP1011ST	Mouser	863-NCP1011AP100G	$0.604	$0.604
1	L1	Inductor	1mH	Mouser	652-SDR1005-102KL	$0.310	$0.310
1	R1	Resistor	20Ω, 2W	Mouser	71-CPF2-F-20-E3	$0.299	$0.299
2	C1, C2	Capacitor	4.7uF, 400V	Mouser	647-UVR2G4R7MPD	$0.137	$0.274
1	U2	Optocoupler	SFH-615A-4	Mouser	782-SFH615A-4	$0.250	$0.250
2	C5, C6	Capacitor	1nF, 1kV	Mouser	81-DEHR33A102KA2B	$0.088	$0.176
1	D2	Diode	MBR150	Mouser	863-MBR150G	$0.097	$0.097
2	C3, C9	Capacitor	10uF	Mouser	647-USR1E100MDD	$0.048	$0.096
1	Q1	BJT	2N2907	Mouser	610-PN2907A	$0.090	$0.090
1	C8	Capacitor	4.7nF	Mouser	140-500P5-472K-RC	$0.080	$0.080
1	D3	Diode	MUR160	Mouser	512-UF4005	$0.059	$0.059
1	C4	Capacitor	1mF	Mouser	647-UVR0J102MPD1TA	$0.059	$0.059
1	R4	Resistor	1.2Ω, 0.5W	Mouser	660-MF1/2LC1R2J	$0.057	$0.057
1	C7	Capacitor	100nF	Mouser	594-K104K15X7RF53H5	$0.050	$0.050
1	D1	Diode	1N4007	Mouser	863-1N4007G	$0.019	$0.019
1	D5	Zener	1N5229B	Mouser	512-1N5229B	$0.015	$0.015
1	R2	Resistor	150kΩ	Mouser	660-CFS1/4CT52R154J	$0.009	$0.009

1	R7	Resistor	10Ω	Mouser	660-CFS1/4CT52R100J	$0.009	$0.009
1	R8	Resistor	2kΩ	Mouser	660-CFS1/4CT52R202J	$0.009	$0.009
1	R3	Resistor	200Ω	Mouser	660-CFS1/4CT52R201J	$0.009	$0.009
1	D4	Diode	1N4148	Mouser	78-1N4148	$0.008	$0.008
1	R5	Resistor	100Ω	Mouser	660-CFS1/4CT52R101J	$0.008	$0.008
1	R6	Jumper	0Ω	Mouser	660-Z25YC	$0.007	$0.007
						Total	$5.42

Date: 11/28/2007

Most of the parts in Table 2-1 were available from Mouser Electronics, so the team chose to purchase a majority of the items from this particular distributor. The one exception in the list was the transformer, since it was sold directly from its manufacturer (Coilcraft) [32]. Overall, the total cost of the adapter test bed's parts was $5.42. The team believed this was a reasonable price, since many adapters available at retail outlets are sold up to four times that amount.

Once the parts were ordered from Mouser Electronics and Coilcraft, respectively, the team debated on the type of board to be used for the test bed. The two choices presented before the group were a solderless breadboard or a pre-punched perfboard. Each option has its own advantages and drawbacks.

The prominent benefit of using a solderless breadboard is the ease of implementation. Since the pinholes in each horizontal row are connected and each vertical column of connections is divided, the breadboard would allow the team to assemble the adapter without the use of solder. Moreover, circuit troubleshooting is very much simplified when using a breadboard since each component can be easily replaced. On the other hand, the pre-punched perfboard does not provide the same ease of implementation. Each pinhole on the perfboard is completely isolated from the surrounding pins, requiring the circuit assembler to solder leads together. If the design contains a multitude of components, this can prove to be an arduous process. Therefore, a circuit prototype is often implemented on a breadboard in the interest of time and troubleshooting.

Although the breadboard seemed to be the logical choice, the team discovered a critical flaw in using a breadboard for the adapter test bed implementation. The vertical columns on the breadboard are separated by a parasitic capacitance of 4pF from one another. This characteristic is not a major issue when building circuits that process low-frequency signals. However, the adapter test bed uses 100-kHz switching from the NCP1011. Therefore, the inter-column impedance of the breadboard is significantly reduced for high-frequency applications. Since the impedance of a capacitor follows the

statement (1/jωC), the isolation between select vertical columns of the breadboard would be a mere 400kΩ for the adapter test bed. There are many hazardous sideeffects introduced by low-impedance separation of nodes, including the possiblity of shorted nodes and leakage currents.

Notwithstanding, the perfboard provides a very high-impedance internode isolation. As long as interconnections are soldered properly, the adapter test bed would operate without the possibility of leakage currents or shorted nodes. In the end, the team believed the perfboard was the right choice for implementing the adapter test bed.

Separate from ensuring proper curcuit functionality, there are many safety concerns associated with testing and building high-voltage, fast-switching circuitry. In particular, high-power circuits can have fatal consequences if not treated with caution. According to the Electronic Library of Construction Occupational Safety and Health (eLCOSH), $120V_{RMS}$ at currents as low as 50mA can have fatal implications on a human being [33].

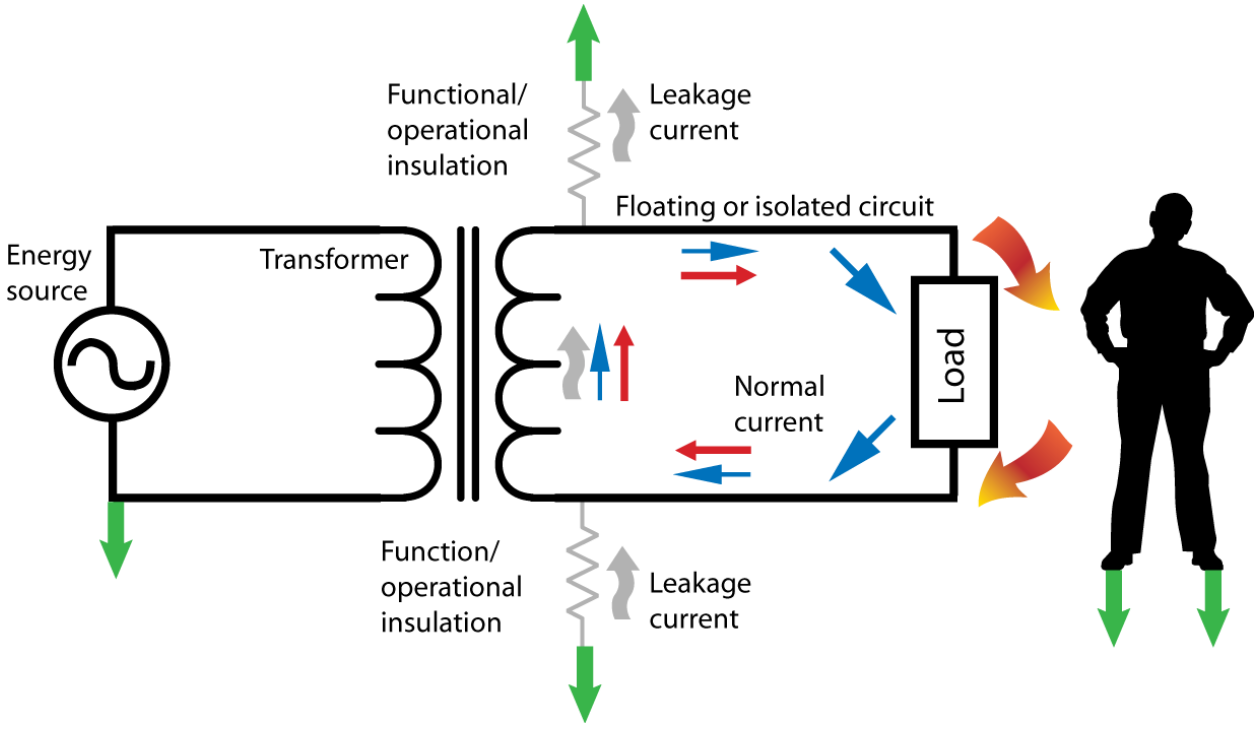


Figure 2-18: Rendition of isolated circuit hazard; floating circuits will readily seek an introduced ground, such as a human being in close proximity [33].

Constructing an AC adapter introduces the hazard of isolated circuits. An IEEE article details how isolated circuits have subsections that have no direct ground [33]. In Figure 2-18, circuitry connected to the secondary winding of the transformer has no return path to the original AC ground of

the energy source. Therefore, the nodes located on the isolated side of the circuit are *floating* with respect to earth ground. In effect, a person in close proximity of a floating node can be in danger of electric shock. For instance, the man's feet in Figure 2-18 are shown to be connected to earth ground. If he made contact with a node on the floating side of the circuit, a path to earth ground would be introduced, and he could be electrocuted provided a high level of current is allowed to run through his body. In addition, he could experience electric shock by simultaneously touching one node of the isolated circuit and another ground. Although the isolated nodes on the DC side of the test bed are relatively low-power, the potential danger introduced by isolated circuits were kept in mind while building the adapter.

Assembly *2.4.2*

Once all of the necessary parts were available, the team began building the test bed on a perfboard. In efforts to simplify circuit troubleshooting, the adapter was built and tested in stages from the AC input to the DC output. The first subcircuit assembled on the perfboard was the input rectifier. The physical arrangement and circuit schematic are shown in Figure 2-19.

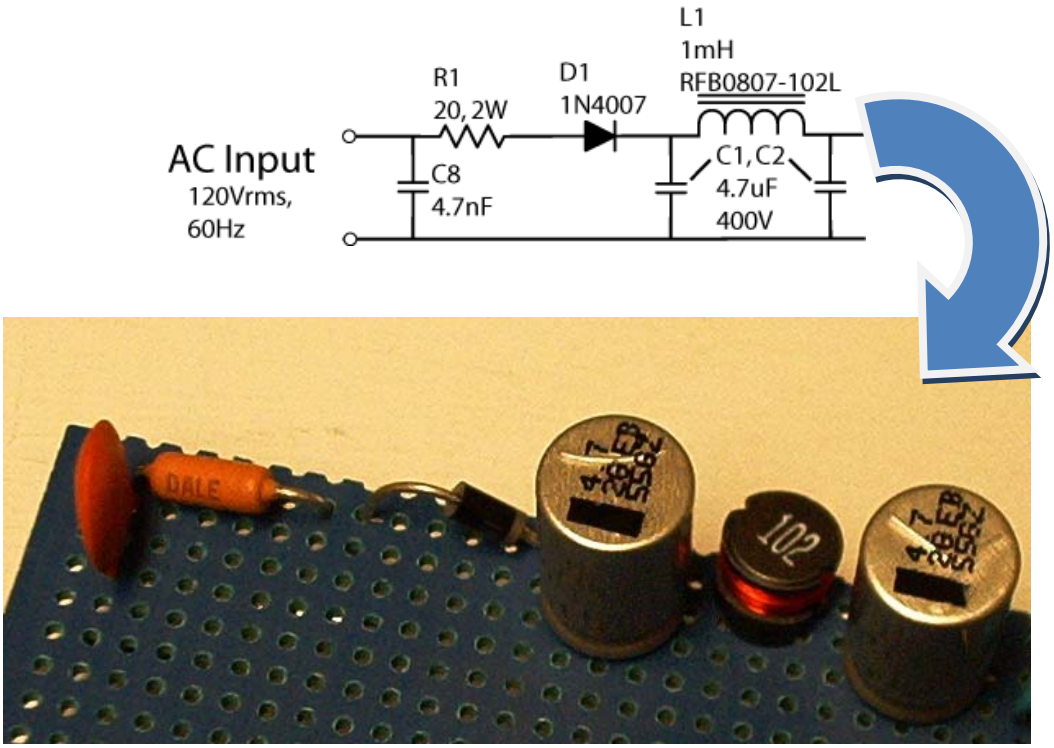


Figure 2-19: Input rectifier of test bed, circuit diagram (top) and soldered circuit (bottom).

Before connecting the $120V_{RMS}$ signal to the rectifier, the team setup a function generator to provide the circuit with a sinusoidal input wave of approximately 10.5V at a frequency of 60Hz. An oscilloscope probe was connected first to the input signal and then to the output of the rectifier, which recorded the voltage across capacitor C2. Figure 2-20 shows three cycles of the input signal to the rectifier, and Figure 2-21 shows the DC voltage recorded across C2. The DC voltage was observed to be approximately 10V. The slight attenuation of the peak voltage of the input to the DC output can be attributed to the voltage drop across rectifier diode D1.

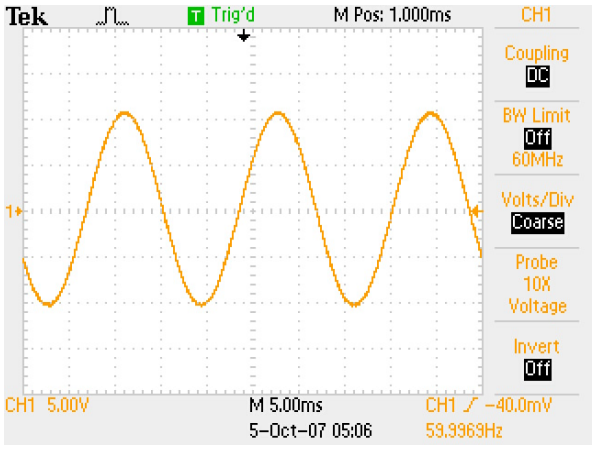


Figure 2-20: Input test wave from function generator; 10V sinusoid.

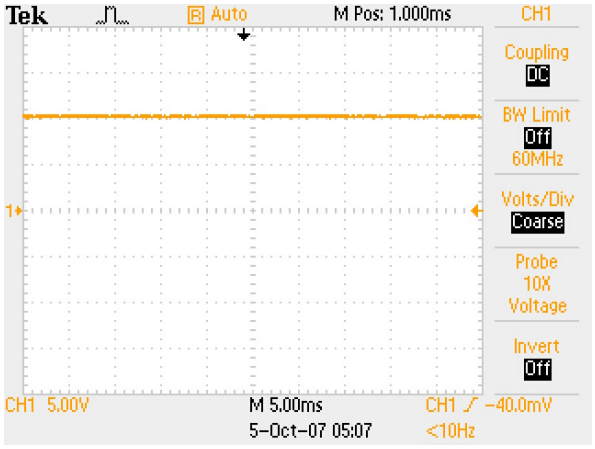


Figure 2-21: Rectifier/filter stage output resulting from application of input test wave in Figure 2-20; $10V_{DC}$.

In addition, the ripple voltage of the rectifier's output waveform was also observed. In an effort to observe the variation in the signal, the oscilloscope's voltage precision was increased to 100mV per

division. Although a small oscillation was observed on the oscilloscope plot shown in Figure 2-22, the team was satisfied with the overall stability of the signal.

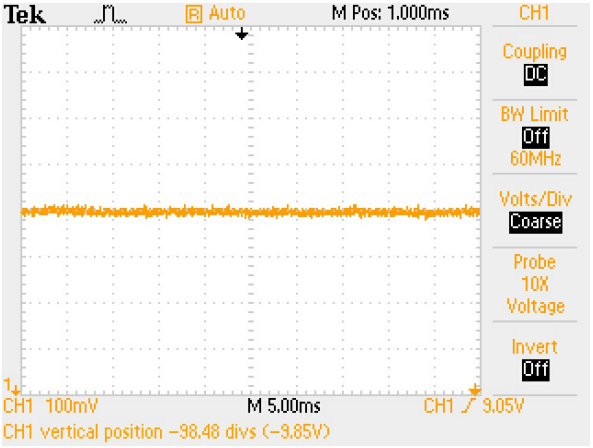


Figure 2-22: Magnification of rectifier/filter stage output from Figure 2-21. The lack of visible ripple demonstrates the functionality of the tank filter comprised of capacitors C1 and C2 and inductor L1.

After verifying the functionality of the input rectifier, the remaining circuitry located on the AC side of the isolation was assembled on the perfboard. The remaining subcircuits to be assembled included the snubber in parallel with the primary winding of the transformer, the transformer, and the NCP1011 IC. Optocoupler U2 was not yet placed in the perfboard since feedback control functionality requires the current sense circuitry located on the DC side of the adapter. Figure 2-23 shows the schematic for all circuitry located on the AC portion of the adapter as well as the physical implementation of the schematic on the perfboard.

Testing of the present configuration required the standard $120V_{RMS}$, 60Hz input to the rectifier. In order to safely connect this high-power signal to the perfboard, a three-connection power cable was used. The cable was stripped of its outer insulator so the three inner connections could be accessed. Since the individual copper wires in the power cable were too thick to connect directly to the perfboard, each wire gauge was adapted by soldering a segment of 10-gauge wire. The three connections were each insulated using shrink tubes, heated to fit around the soldered wires. The adapted $120V_{RMS}$ wire (black) and the neutral wire (white) are shown in Figure 2-23. The earth ground connection (green) was fastened to the metal backing of a test bench.

Once the adapted power connections were soldered to the perfboard, the half-constructed adapter was plugged into a wall socket. No adverse effects or phenomena were experienced after one

minute of $120V_{RMS}$ running through the AC side of the adapter. The team proceeded to disconnect the power connection and connected an oscilloscope probe across capacitor C2 to measure the output voltage of the rectifier. When power was reconnected, the oscilloscope showed a 0V potential across C2. Therefore, the team connected the probe across the auxiliary winding of the transformer in order to observe an expected waveform oscillating at 100kHz. When power was reconnected to the perfboard, the primary winding of the transformer experienced a surge of current that caused it to overheat. The heat caused the material in the winding to vaporize, producing an acoustic explosion and a noticeable spark. Subsequent troubleshooting yielded the reason this event occurred.

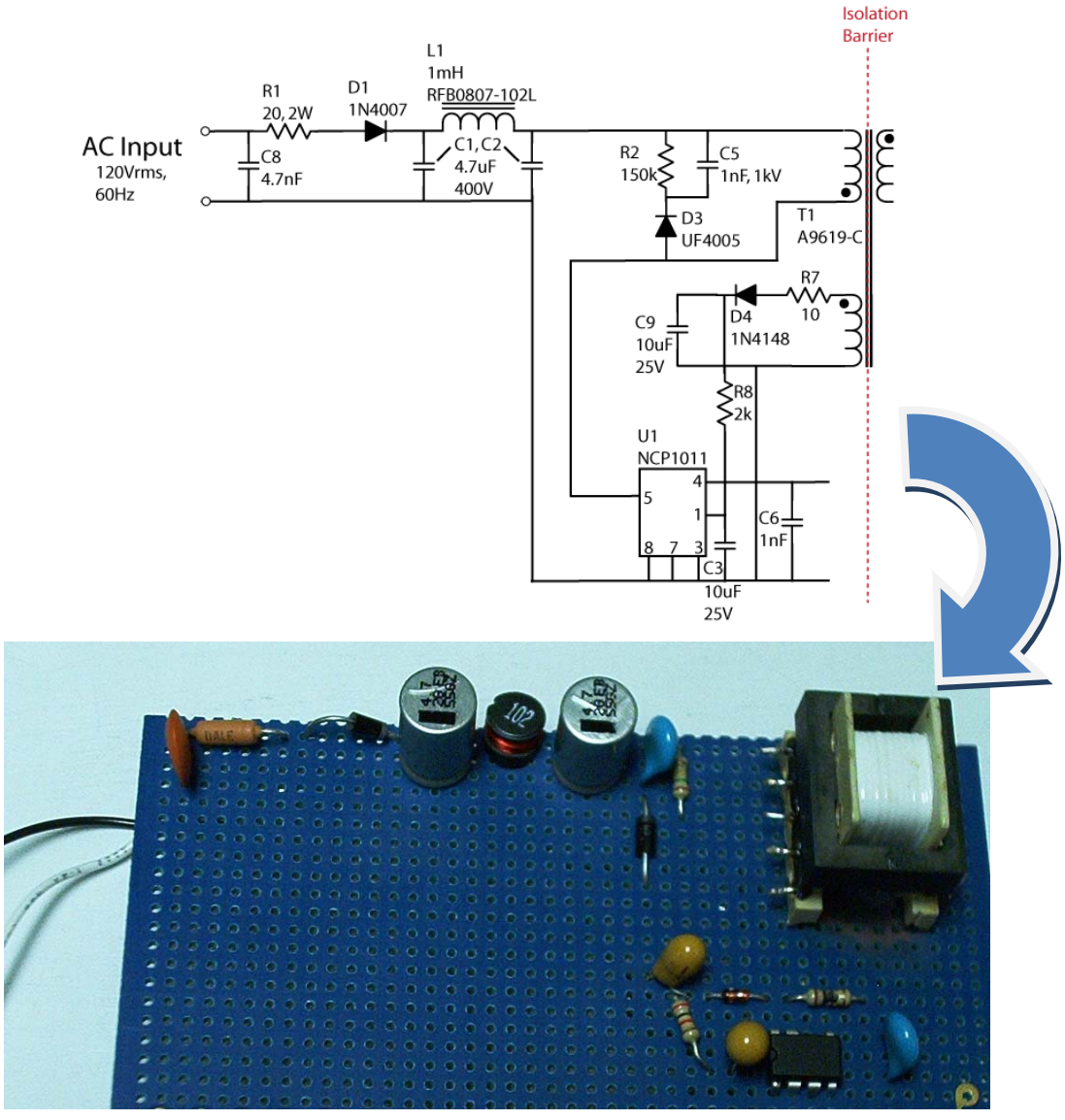


Figure 2-23: AC side of test bed, circuit diagram (top) and soldered circuit (bottom), (11/20/2007).

The tip of a typical oscilloscope probe has a high impedance, while the alligator clip provides an earth ground connection. According to the conventional dot labeling of an inductor, the high voltage is connected to the side of the winding where the dot is located. Theoretically, connecting the probe ground to the low-potential node of the auxiliary winding is not hazardous since the adapter schematic shows that the auxiliary winding is in fact connected to earth ground. However, the team discovered that the input power connections were connected with the $120V_{RMS}$ signal at the bottom rail and the neutral connection at the top rail. Since the neutral input connection was attached to the top rail, the input rectifier produced a 0V output. More importantly, the $120V_{RMS}$ connection was shorted to earth ground via the oscilloscope probe, causing an excessive level of current to flow through the primary winding. Figure 2-24 shows a representation of the nodes in a typical wall socket and the connections made to the each node [34].

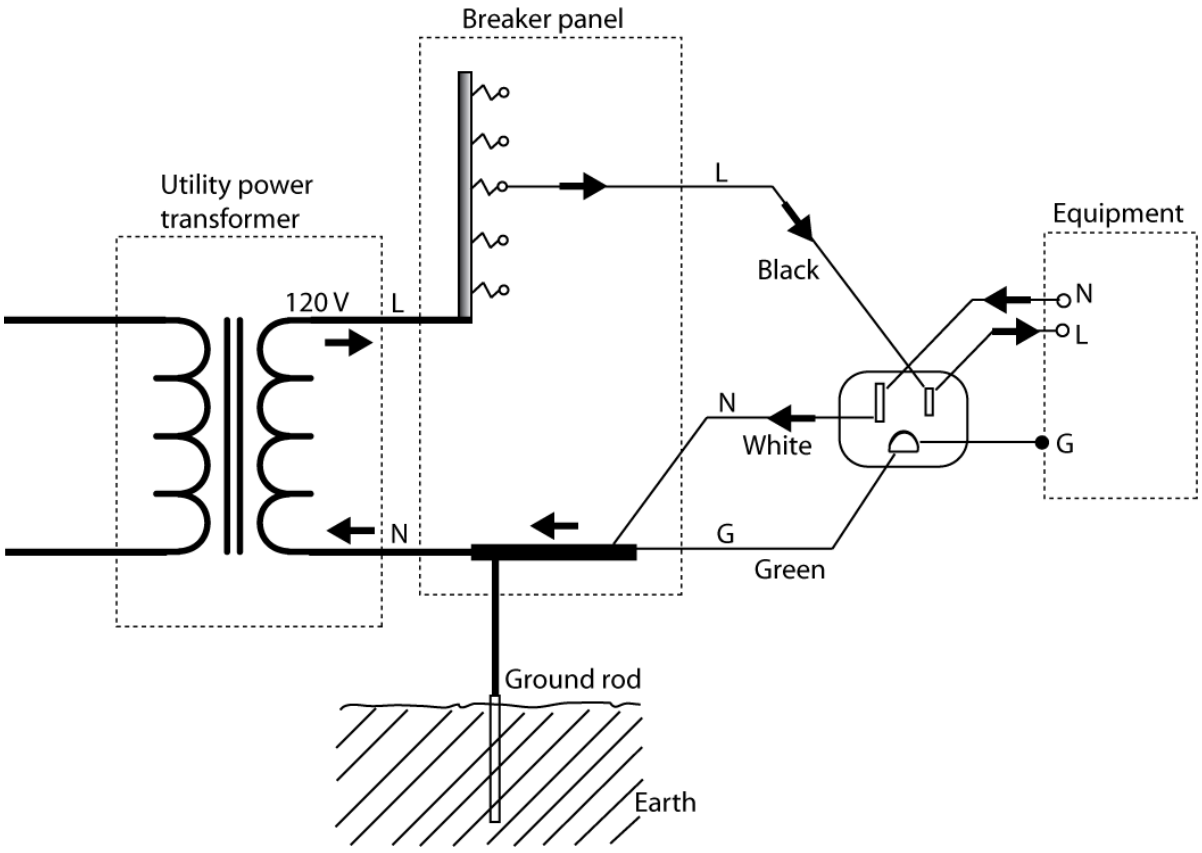


Figure 2-24: Diagram depicting the delivery of AC power, from the utility transformer to the outlet and the eventual device's interface with it. Note that line is represented as a white wire while neutral is black [34].

The wall socket's ground and neutral connections are given access to earth ground via a ground rod. Since the neutral input has a path to earth ground, a third connection from the adapter to the ground connection of the wall socket is not required. However, the live connection (denoted by *L*) oscillates between 170V and -170V. AC adapters designed around the linear power supply configuration shown in Figure 2-1 can transform the input signal regardless if the input is connected in a reverse manner or not. If the neutral and live connections are interchanged in a linear power supply, the transformer is able to translate in an inverted signal (180° out of phase) to the output. This is harmless to the linear power adapter, since the input is a symmetrical AC signal with little DC bias. The adapter test bed used in this project, on the other hand, requires a neutral connection to the bottom rail of the AC input in order for the input rectifier and NCP1011 to operate appropriately. Figure 2-3 shows the several ground connections in the adapter.

The team realized that resistors R8 and R1 were also damaged during the initial testing of the AC side of the adapter. Once both resistors as well as the transformer were replaced, the team switched the polarity of the input connections. Next, the DC side of the adapter was implemented. Since the first perfboard was not wide enough to fit all circuitry, a second perfboard was used to build the DC stage. Two 10-gauge wires were attached to the positive and negative DC output connections. Since the prototype would undergo many trials using a variety of resistive loads, the wire connections allow load connections to be made through a breadboard. Figure 2-25 and Figure 2-26 show the front and back of the completed perfboards.

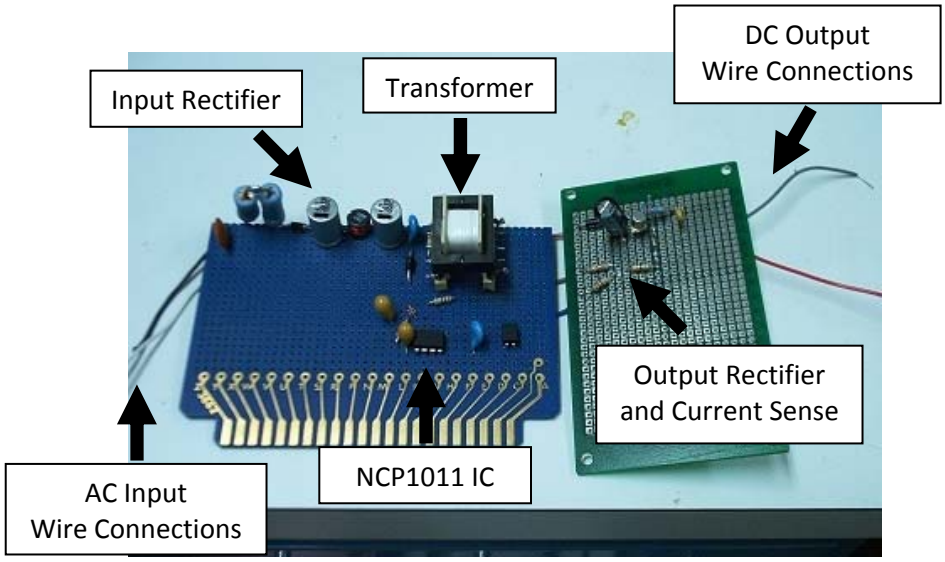


Figure 2-25: Top view of first prototype of adapter test bed implemented on perfboards (11/21/2007). Major circuit stages are labeled with arrows and descriptions.

Since the adapter is implemented on two separate perfboards, connections between the DC and AC side were made via 10-gauge wire. Figure 2-26 show the connections made throughout the prototype, including the crossover connections between the AC and DC stages.

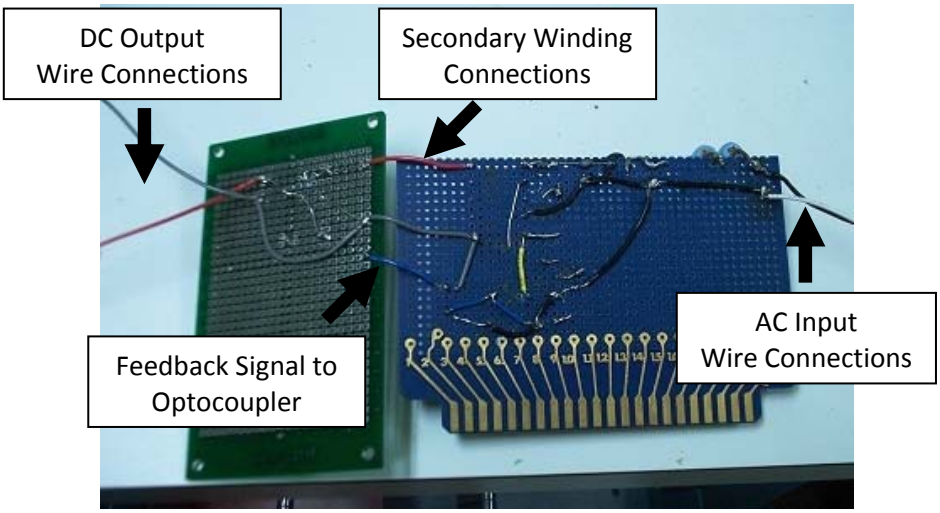


Figure 2-26: Bottom view of the first prototype of the adapter test bed implemented on perfboards (11/21/2007). Connections between both perfboards have been labeled with arrows and descriptions in addition to input and output connections.

Before connecting the input power to the prototype, an oscilloscope was connected across the DC output of the adapter. When the AC input connection was made to a wall socket, a 5.6V DC signal was observed at the output, shown in Figure 2-27.

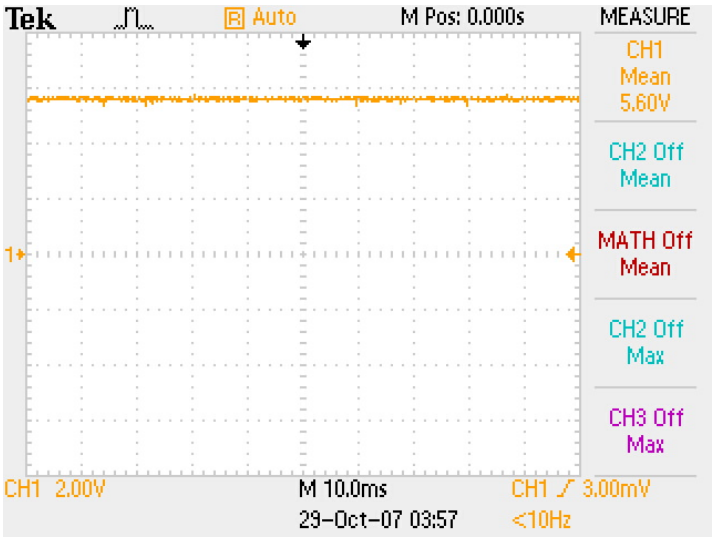


Figure 2-27: 5.6V DC output of first adapter prototype.

Like the input rectifier output, the team pursued to increase the volts per division scale of the oscilloscope to analyze the noise level of the signal. Figure 2-28 shows a small amount of high-frequency noise at the output because capacitor C4 was unable to filter the entire 100-kHz signal from the secondary winding. However, the amplitude of the noise is small enough to be negligible for battery charging applications.

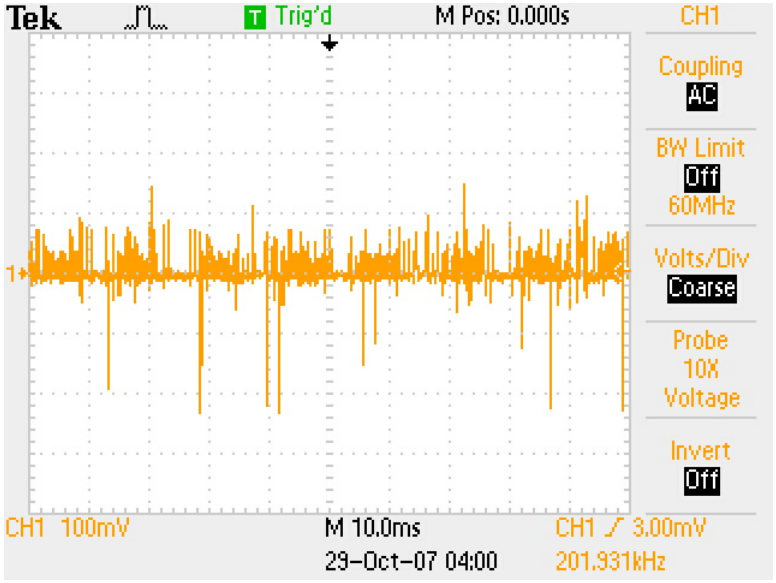


Figure 2-28: Close-up probe capture of noise observed at the DC output of the first test bed implementation. The level of noise varies slightly relative to the DC bias, so the effect of these oscillations on the battery load is negligible.

Once an operational model of the adapter was accomplished, the team designed a PCB of the test bed. Building the test bed on a PCB had a few benefits. For instance, board space was conserved since all connections were pre-made by the PCB manufacturer. An array of 868 pinholes was placed in the vacant area above the adapter circuitry so experimental circuitry could be implemented later in the project. Another advantage to building the test bed onto a PCB was integrating both the AC and DC stages onto one board. The interconnections between one perfboard and the other were under much tension due to the two-board arrangement. Constructing the test bed on one board eliminated the possibility of connectivity issues throughout the circuit. The original PCB design is shown in Figure 2-29.

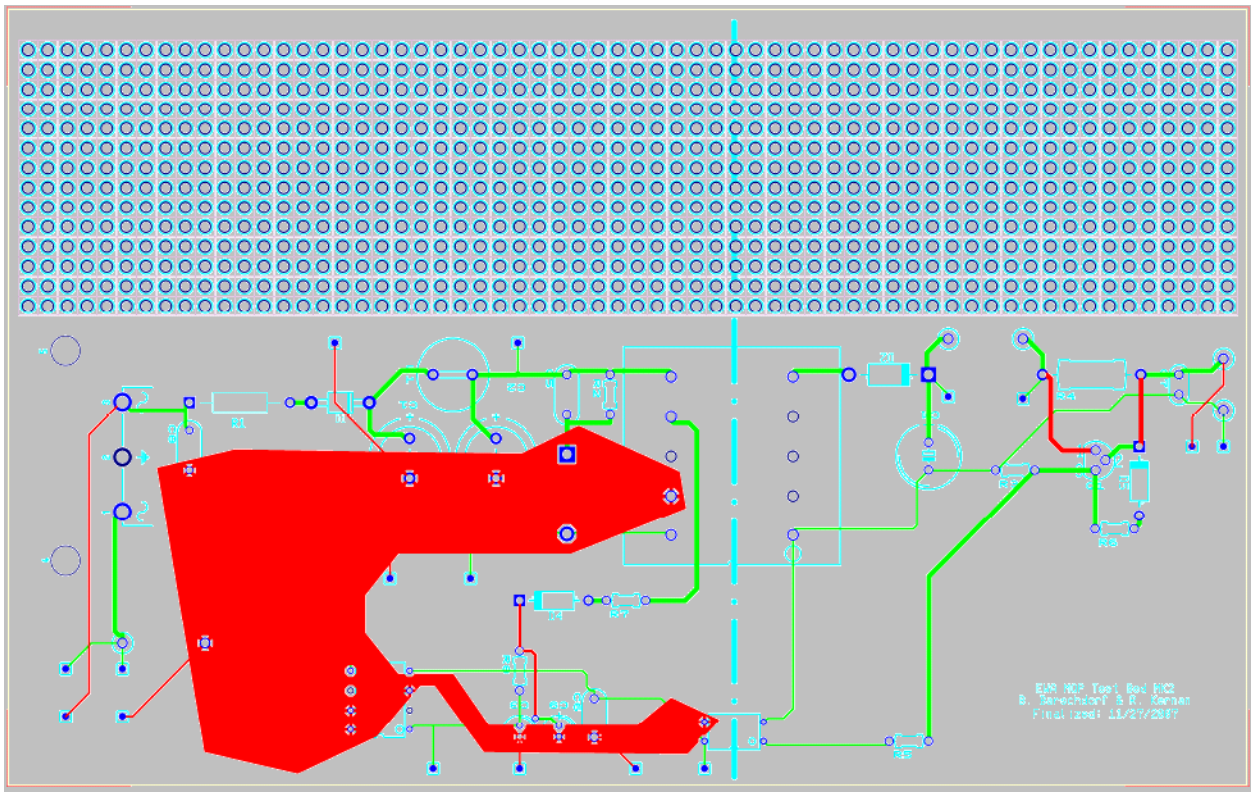


Figure 2-29: First revision of adapter PCB design (11/29/2007). Green traces represent top-level copper connections while red traces represent bottom copper connections. The top silkscreen is shown as light blue to outline component footprints and pin holes. The bottom copper area on the AC portion of the PCB is connected to AC ground via a jumper [27].

The light blue traces indicate the silkscreen prints used for component footprints and identification markings. The two-level board's trace layers are shown in Figure 2-29 by color. The light green traces represent top-layer copper connections, while the red traces show bottom-layer traces located underneath the board. The dashed line on the top silkscreen layer represents the isolation between the AC side and the DC side of the adapter.

The red area located on the left-hand side of the board provides a power plane for all connections made to AC ground. Its odd shape is attributed to the team's efforts in minimizing charge collection at particular points in the plane. If the plane was shaped as a polygon with right angles, charge would collect at these points of transition. In effect, charge differentials could occur between other points in the circuit and the charge collections on the power plane. Ideally, the plane should have a uniform charge density, so the area is enclosed by obtuse angles in order to minimize charge collection. The ground plane was also designed to flow under the top-layer copper trace connecting pin

5 of the NCP1011 (output) and pin 10 of the transformer (top node of primary winding) to minimize the effect of noise on the 100-kHz signal.

The PCB design contains other changes from the perfboard implementation. A footprint for an AC power cable connection plug was placed before the input to the adapter for simplification. Also, test points were implemented throughout the design so probe measurements could be made at critical nodes. The ground plane's connection to the neutral input is intentionally disrupted by a resistor footprint. This way, the adapter's supplied current can be measured using Ohm's Law. If normal adapter operation is desired, the team has the option of placing a 0Ω jumper in lieu of a true resistor to directly connect the neutral input to the ground plane. Finally, the connection between the DC output and the output rectifier was broken in the same manner. The team intended to place a current-sensing resistor in this footprint to measure the output current delivered to the connected load, since a current sense implementation of some kind was expected in the final design.

Measured Waveforms of Test Bed 2.5

After completing a working adapter test bed, the team obtained measurements of various waveforms in the design. All test bed measurements were obtained using the first prototype of the test bed. Notwithstanding, the measured waveforms throughout the adapter test bed were consistent with the team's preconceptions of circuit behavior.

A variety of waveforms of the adapter test bed were captured and analyzed. Input power signals, NCP1011-related waveforms, and DC output voltages were observed via an oscilloscope. Before presenting the waveforms and the team's analysis thereof, the test bed schematic is shown again in Figure 2-30 for convenience [27].

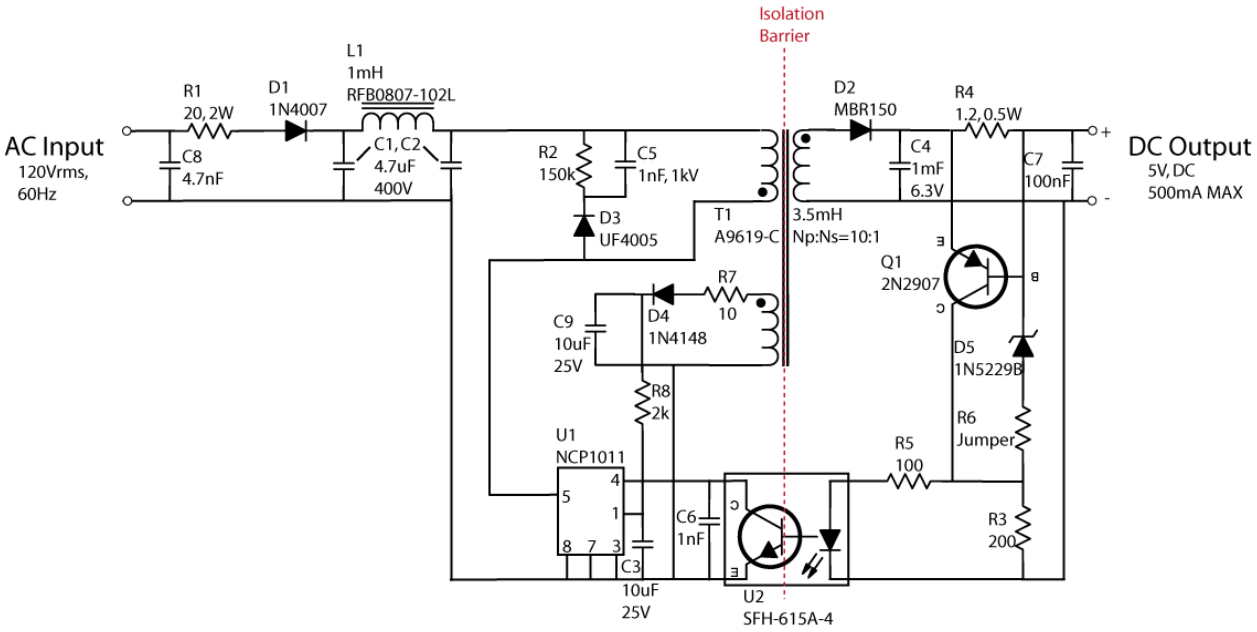


Figure 2-30: Test bed schematic from ON Semiconductor's DN06017/D Design Note.

Initial waveforms were captured of the adapter's DC output, but these waveforms were obtained under no-load conditions. Figure 2-31 shows the DC output of the adapter with a purely resistive load 200Ω. The DC bias level of the output waveform during no-load conditions and load conditions remains the same. Therefore, a large variation in drawn current does not dramatically affect the output voltage, which is a desired characteristic of an AC adapter.

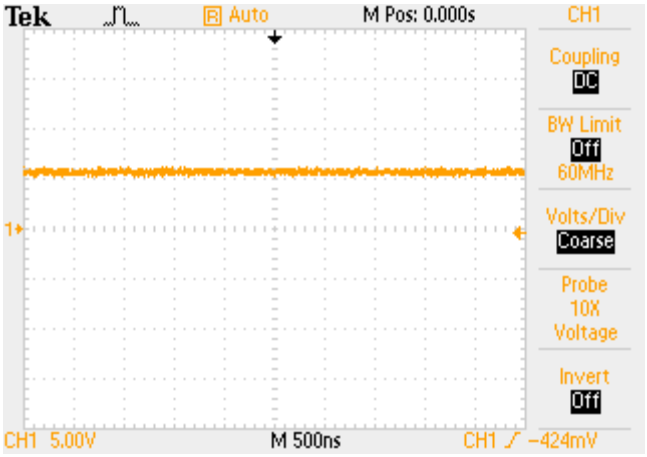


Figure 2-31: Oscilloscope capture of DC output voltage with 200Ω load using the first test bed implementation. The mean voltage was observed to be slightly above 5V.

While the voltage level remained constant regardless of load connectivity, the team wondered why the DC bias was significantly greater than the nominal voltage. The reason for this discrepancy is due to two components in the circuit: transformer T1 and Zener diode D5. The transformer used in this project is different from the one specified in ON Semiconductor's original schematic of the adapter. In fact, the transformer model used by ON Semiconductor was designed by Mesa Power Systems. Since the exact transformer model specified in the original design was unavailable, the team chose Coilcraft's A9619-C Flyback transformer. The Coilcraft A9619-C was created specifically for SMPS applications designed around the NCP101X IC family [32]. Although both models are similar, the specifications of each vary slightly. The turn ratio between the primary and secondary windings are equal in both models, but there may be a small discrepancy between the waveforms produced by each transformer.

It is also possible that Zener diode D5 may contribute to the output voltage difference. Although Zener diodes are designed for specific reverse breakdown voltages, each diode model requires a rated *avalanche* current to produce the expect voltage drop. Therefore, the reverse breakdown voltage may vary slightly between Zener diodes of the same model. In addition, the pull-up resistor of 200Ω may vary between 190Ω and 210Ω, causing a variation in voltage on the DC output. However, the team decided that a small discrepancy of 600mV was acceptable, since many batteries are designed with a reasonable tolerance of charging voltages.

Once the DC output waveform was measured, the switching behavior of the NCP1011 was observed. Figure 2-32 shows two waveforms each oscillating at 100kHz. Figure 2-33 redisplays the simplified diagram of the NCP1011 switcher for reference [28].

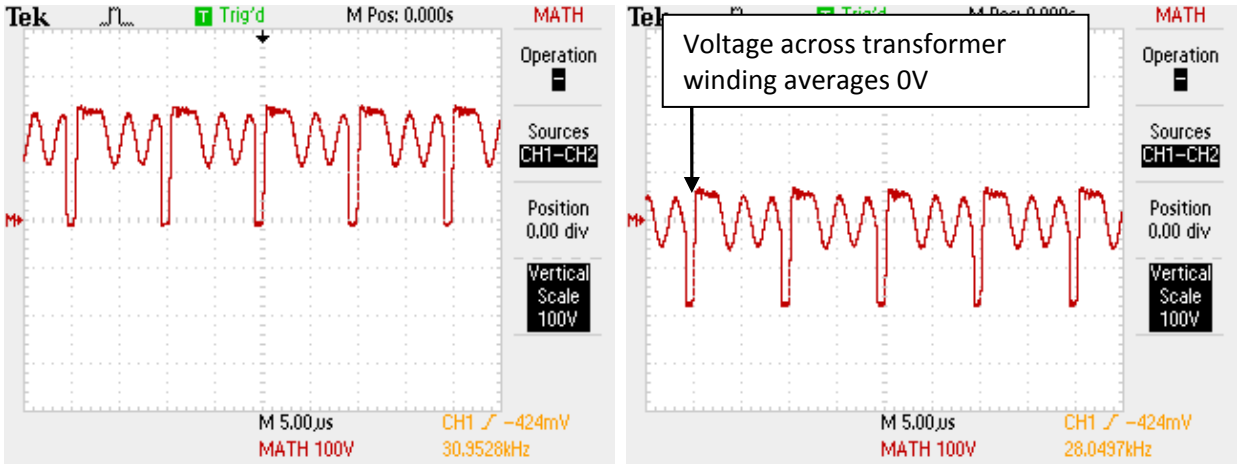


Figure 2-32: IC output with 200Ω load (left), Voltage across primary winding with 200Ω load (right) using first test bed implementation.

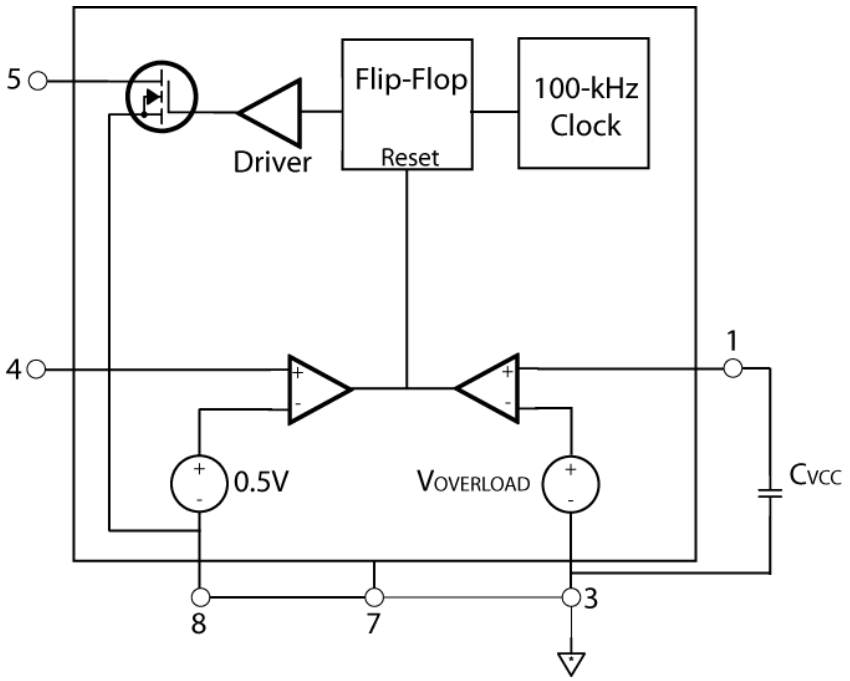


Figure 2-33: The simplified block diagram of the NCP1011. Pin 1 is the V_{CC} pin, and pins 3, 7, and 8 are connected to AC ground. Pin 4 is the feedback pin from optocoupler U2 and pin 5 is the output of the switcher. Pins 2 and 6 are not connected, and are therefore absent from the diagram [28].

The left-hand waveform shown in Figure 2-32 shows the voltage at the output of the NCP1011. As expected, the internal power MOSFET in the IC switches the output between AC ground and the voltage output of the input rectifier ($170V_{DC}$). The sinusoidal oscillations that are observed after low-to-high transitions can be attributed to damping effects introduced by the snubber circuit [29]. Without a snubber, high-voltage transients would appear across the power MOSFET's drain and source terminals. The inclusion of a snubber circuit dampens the high-voltage transients caused by fast-switching applications by creating an alternative path for current to flow during transitions. When current flows through the snubber, the system comprised of resistor R2, capacitor C5, and the inductance of the primary winding is underdamped, causing oscillations to occur in the voltage waveform until the switch is closed.

Next, the voltage at the V_{CC} pin of the NCP1011 (pin 1) was observed. Figure 2-34 shows the voltage waveform measured at the V_{CC} pin. The left waveform shows a small voltage ripple at a DC bias level of approximately 8V. The frequency of the ripple was measured to be 83.3Hz. Therefore, the duration of each ripple lasts 12ms. According to the datasheet of the NCP1011, the ripple frequency is

contingent on the adapter load. If the adapter is delivering a significant amount of power to the load, the ripple frequency increases. Conversely, the ripple period increases if a high-impedance load is connected to the adapter.

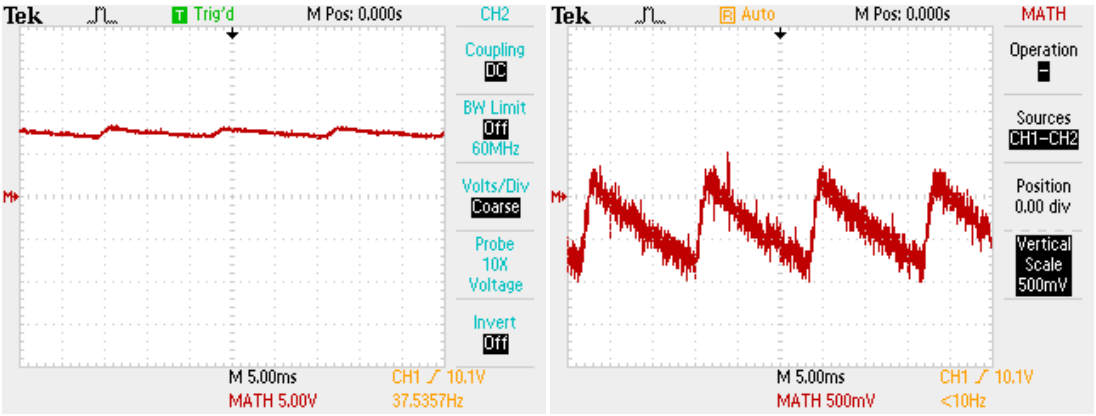


Figure 2-34: The left waveform shows the voltage on the NCP1011's Vcc pin with 200Ω load, while the right waveform shows a 10X magnification of the left waveform using the first implementation of the test bed.

After collecting the various waveforms measured under a DC output load of 200Ω, the adapter was then tested under the two extreme conditions: no load and a 0Ω load (output short). The right-hand waveform in Figure 2-35 shows the output voltage of the NCP1011 (pin 5) with no load attached to the output. The left-hand waveform redisplays the IC's output voltage for a 200Ω load to juxtapose the no-load waveform. The no-load waveform, while maintaining signal integrity, has a much smaller duty cycle than the 200Ω waveform. The reduced duty cycle follows the specifications of the NCP1011's behavior under standby conditions (i.e., no load).

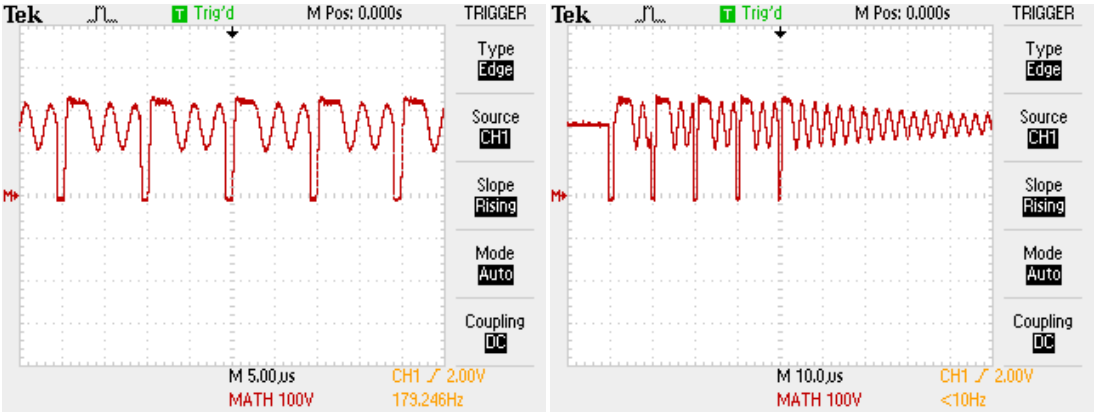


Figure 2-35: IC output with 200Ω load (left), no load (right) using first test bed implementation.

On the other hand, the 0Ω load exhibited a much different behavior. After shorting the positive DC output connection to the negative output, the voltage waveform shown in the right oscilloscope capture in Figure 2-36 was observed. In order to prevent the transformer from delivering an excessive amount of power to the DC side of the adapter, the duty cycle of the NCP1011 output is decreased to almost 0%. Under the shorted load condition, the high-current sense circuitry signals the optocoupler to alert the NCP1011 of a high output current condition. The NCP1011 reactivates momentarily every 10µs to check for a load condition change. The NCP1011 resumes normal switching behavior once the output terminals of the adapter are opened. This behavior follows the specifications stipulated in the datasheet for the NCP1011 [28].

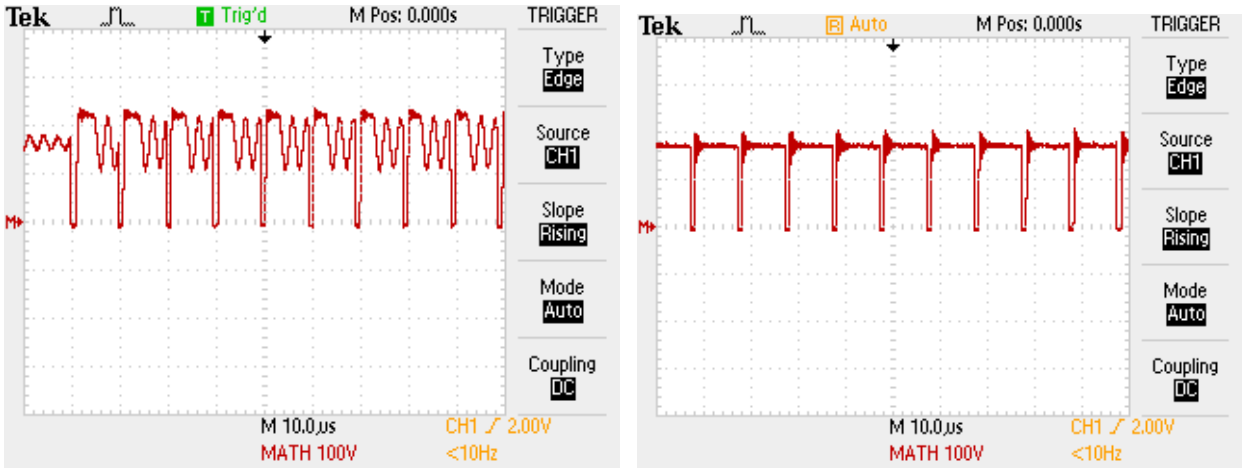


Figure 2-36: IC output with 200Ω load (left), shorted load (right) using the first test bed implementation.

The short-circuit protection feature of the NCP1011 was further tested by connecting its feedback pin (pin 4) directly to AC ground. The resulting waveform of the IC's output shows that switching behavior is ceased while the feedback pin is constantly grounded. Under this condition, the IC is unable to power itself via the auxiliary winding, so power is drawn from the high DC voltage produced by the input rectifier. Figure 2-37 shows the output of the NCP1011 when the feedback pin is shorted to AC ground.

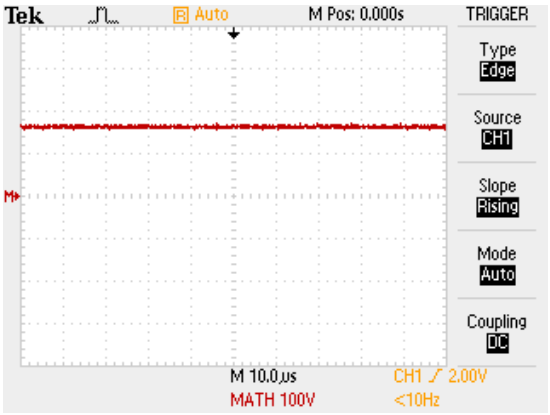


Figure 2-37: Using the first test bed implementation, IC output is shown with pin 4 of the NCP1011 shorted to AC ground, simulating a high-current condition. Switching behavior is completely ceased under this condition.

After the test bed was tested under extreme output conditions, the team simulated a defective battery load by introducing an output current above the maximum of 500mA. Instead of connecting a low-impedance output, a voltage source was placed across the current sense resistor R4. The output of the voltage source was set to $736mV_{DC}$, producing a current of 587mA through R4. Theoretically, the 736mV drop across base-emitter junction of PNP BJT Q1 would cause the transistor to source current through its collector and emitter terminals. In effect, the sourced current from the top DC rail would drive the internal LED of the optocoupler on, signaling the NCP1011 of an over-current condition at the output. Figure 2-38 shows that the theoretical operation of the adapter under this condition matches its actual behavior. Similar to the shorted feedback pin, the adapter halts high-frequency switching until the high-current condition is cleared.

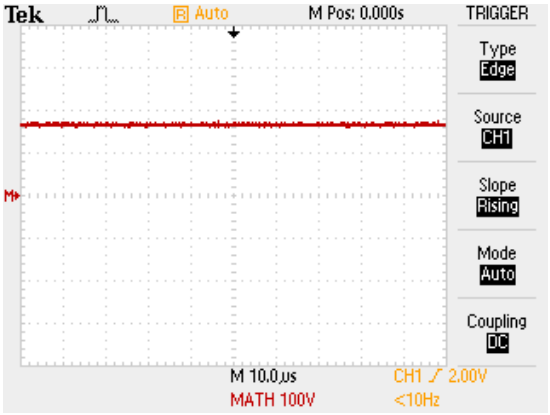


Figure 2-38: Using the first test bed implementation, IC output is shown with 587mA flowing through the current-sensing resistor R4, simulating a high-current condition. Switching behavior is completely ceased under this condition.

At this point, the team confirmed many of the specifications described in ON Semiconductor's datasheet of the NCP1011 monolithic switcher. However, the output of the adapter was observed once more to capture the ripple voltage. Figure 2-39 shows waveforms of voltages measured across filter capacitor C4. The left waveform shows the waveform under a 100Ω load condition, and the right waveform was captured while no load was connected to the output. After placing the oscilloscope on a 50mV per division vertical scale, a small ripple effect was observed. The waveform measured under the 100Ω condition shows a periodic occurrence of voltage spikes at a frequency of 100kHz. While the left waveform exhibits a 50% duty cycle, the no-load waveform shows a much smaller duty cycle across capacitor C4. In addition, the DC bias level is reduced by 100mV. Overall, the power consumption of the adapter is significantly reduced under standby conditions.

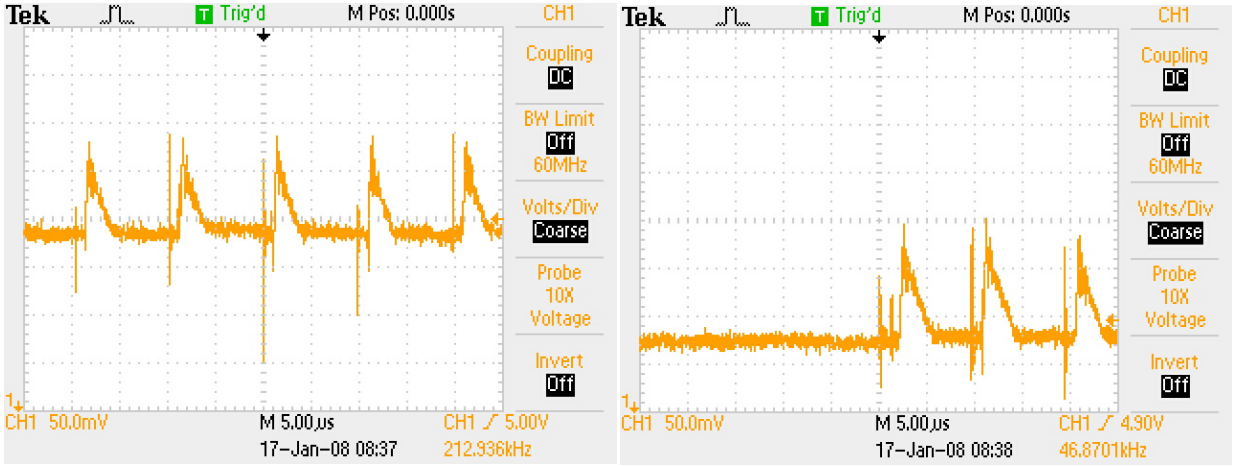


Figure 2-39: Voltage across C4, 50mA load (left), open (no) load (right) using first test bed implementation.

Once various waveforms of the NCP1011 were analyzed under selected load conditions, the team focused on obtaining power efficiency measurements of the adapter. Since the ON Semiconductor design note claims that the adapter is highly-efficient, it was important to verify the adapter's small level of power loss. Power efficiency is defined as the ratio of power delivered to the output compared to power supplied by the input. Measuring the power delivered to the output was simple using the following relationship:

$$P_{OUT} = \frac{{V_{OUT}}^2}{R_{LOAD}} \qquad (2\text{-}2)$$

On the other hand, calculating the power supplied by the input is more challenging.

Initially, the team attempted to calculate the input power using an ammeter at the input of the adapter. Figure 2-40 shows the setup used to measure the input power with the ammeter.

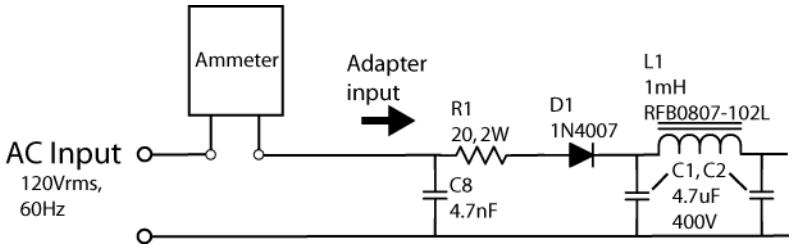


Figure 2-40: Initial input power measurement setup for adapter test bed. The ammeter is placed in series, separating the live, 120V_{RMS} input from the adapter input.

In order to measure current, the connection between the live, 120V_{RMS} node and the adapter input was broken. Subsequently, the ammeter was placed in series with the two inputs. The continuous power supplied by the input was then measured by calculating the product of the input RMS current and voltage:

$$P_{IN} = V_{IN,RMS} I_{IN,RMS} \quad (2\text{-}3)$$

When the adapter was plugged in with a 200Ω DC load, the ammeter measured an RMS current of 1mA. According to (2-3), the supplied power to the adapter was 120mW. Likewise, (2-2) yields a delivered power of 28mW. Dividing the output power by the input power gives an efficiency of 23.3%. Realizing that the adapter is a SMPS and is described to operate at a high efficiency, the team was skeptical at the calculated efficiency.

It was later determined that the ammeter was designed to measure RMS currents of sinusoidal waveforms. Since the adapter utilizes an input rectifier for its operation, the input current is not sinusoidal. Figure 2-41 shows the schematic of a typical half-wave rectifier with a filtering capacitor and the output waveform produced by a rectifier. The diode in the rectifier eliminates the negative voltage swing of the sinusoidal AC voltage, yielding a half-wave signal. The filter capacitor then charges up to the peak amplitude of the signal. Once the voltage of the half-wave signal begins decreasing, the capacitor slowly discharges, producing a relatively stable output signal with a slight ripple voltage. Therefore, current is drawn from the adapter only during time periods when the capacitor recharges back to the peak amplitude of the half-wave signal. Therefore, a new method is required to measure power supplied by the AC input.

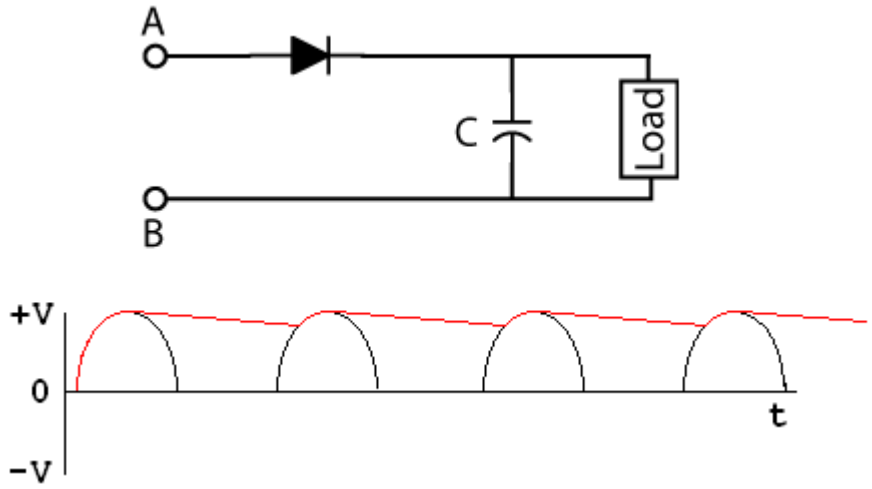


Figure 2-41: Example of a typical rectifier with smoothing capacitor, and its output waveform. Current is only drawn during the periods in which the capacitor's voltage is charging, so the current waveform will not be sinusoidal [35].

An alternative way of measuring current is by placing a series resistance in the path of the supplying voltage source. As long as the resistance is small in value, the circuit is not affected by its presence. Therefore, the team placed a series resistance in the return path of the AC input. Using Ohm's Law, the voltage measured across the resistor is linearly proportional to current flowing through the resistor. An oscilloscope probe can then be placed across the introduced resistor, while another probe can be placed in parallel with the voltage source. Figure 2-42 explains this arrangement, showing Scope A measuring the input voltage while Scope B measures a voltage proportional to the input current. The MATH function of the oscilloscope allowed the team to use the continuous power relationship in (2.3) by multiplying the waveforms of Scope A and Scope B together.

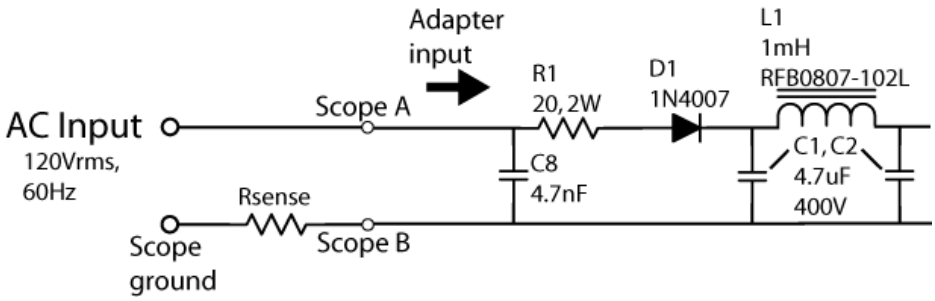


Figure 2-42: The second arrangement used in test bed power measurements. Input voltage is measured by scope A, while a voltage directly related to the input current is measured by probe B.

R_{sense} was selected to be 1Ω for initial measurements using the alternative method. The team rationalized that the voltage drop across R_{sense} would equal the exact value of current in amperes. Figure 2-43 shows the oscilloscope probes arranged according to Figure 2-42. Looking at Figure 2-44, Probe B is connected across R_{sense}, while Probe A is connected across the AC input. The output load was connected to the adapter using the green and white alligator clips as depicted in Figure 2-43.

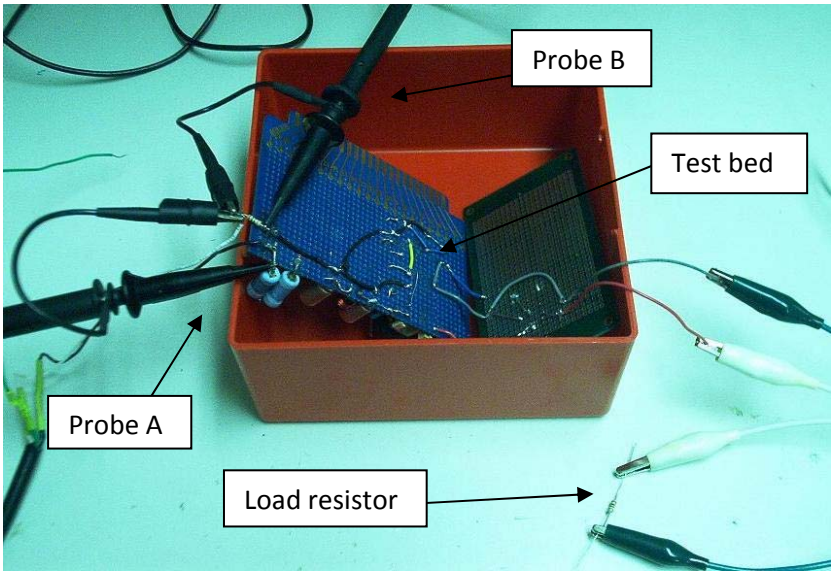


Figure 2-43: Test setup for measuring the power efficiency of the original test bed configuration.

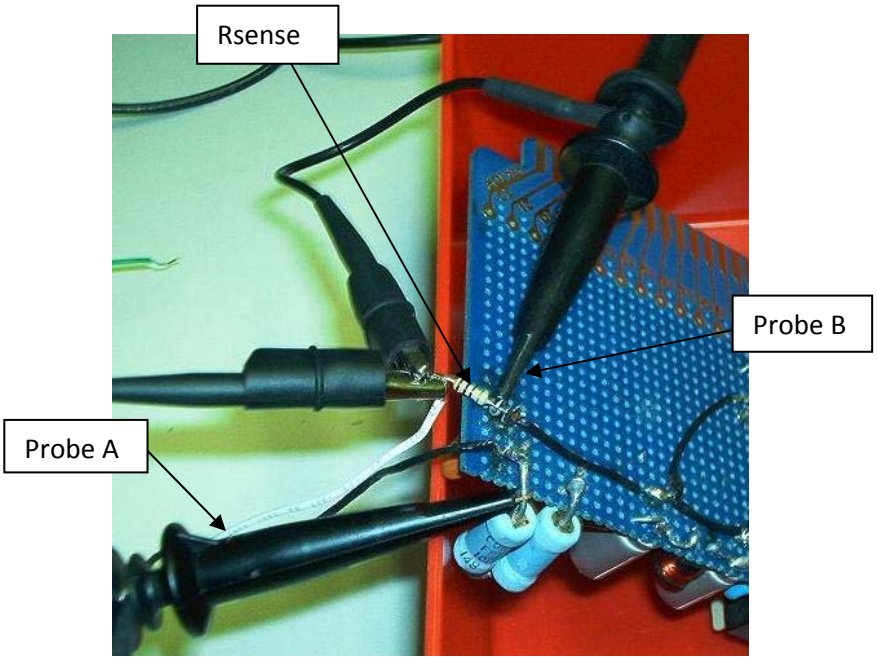


Figure 2-44: Configuration of oscilloscope probes for input current measurement of initial adapter test bed.

Under the test setup shown in Figure 2-43 and Figure 2-44, waveforms shown in Figure 2-45 were observed on the oscilloscope. Channel 1 shows the voltage across R_{sense} and Channel 2 shows the AC input voltage. Although the AC input voltage waveform was observed as expected, Channel 1 resembled a 180Hz distorted sinusoid. The signal observed on Channel 1 was determined to be noise from the three-phase power system [36]. Although the supplied power to the adapter is clearly a single-phase sinusoid, a three-phase to single-phase power conversion takes place prior to reaching the wall socket. This converts most of the three-phase signal to a single-phase signal, but produces noise on the AC line connected to the wall socket. Since each signal of the three-phase system is separated by a third of a cycle from the others, the noise grants the illusion of a 180Hz signal. Therefore, the team needed a way to eliminate the noise produced by the three-phase power system in order to accurately measure the power efficiency of the adapter.

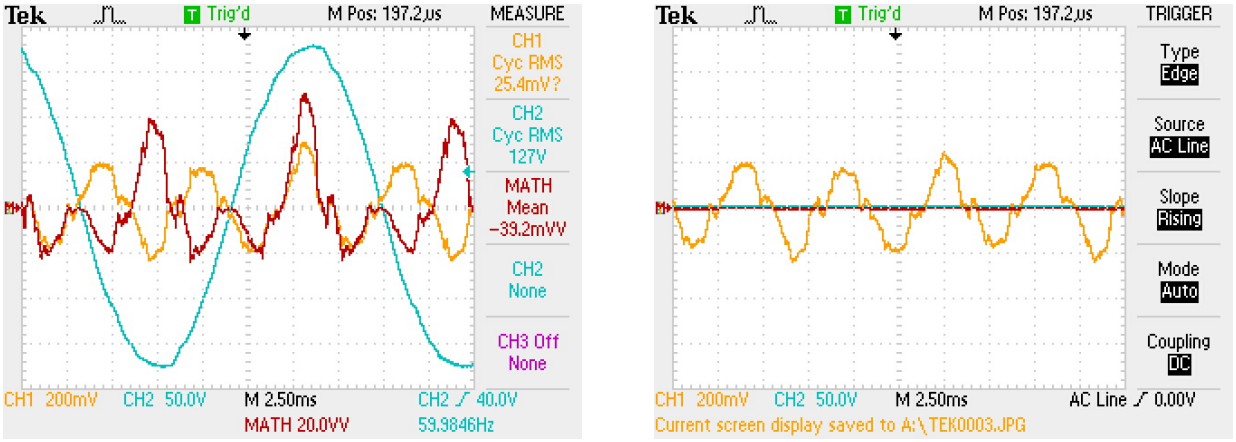


Figure 2-45: Oscilloscope capture of input power measurement using 1Ω sensing resistor (left) for the initial adapter test bed. The adapter is connected to AC power via a surge protector. The observed noise was attributed to the three-phase to single-phase power conversion. The right-hand signal shows the noise produced while the surge protector is switched off.

In order to minimize the effect the 180Hz noise had on input current measurements, a value of 100Ω was substituted in for R_{sense}. Using a resistance 100 times the original value amplified the power measurement by an equal factor. However, a simple division by the same amount yielded an accurate measurement of the power supplied to the adapter. Therefore, the next input power measurement was conducted using a 100Ω resistor for R_{sense} and a 51Ω resistor for the output load. Figure 2-46 displays the results of the input voltage and current waveforms. While a noticeable amount of noise was observed between cycles, the periodic current spikes were located where expected. The true RMS value

of the input current was displayed as 1.76V which, given the 100 Ω sensing resistor, converts to 17.6mA. The MATH function of the oscilloscope was observed at an average of $78V^2$, which translates to an average power of 780mW. The output voltage was calculated using a multimeter to be 5.474V. Using (2-2), the power delivered to the output load was 588mW. The power efficiency was subsequently calculated to be 75.4%, providing a more representative value of the adapter's efficiency under normal operation.

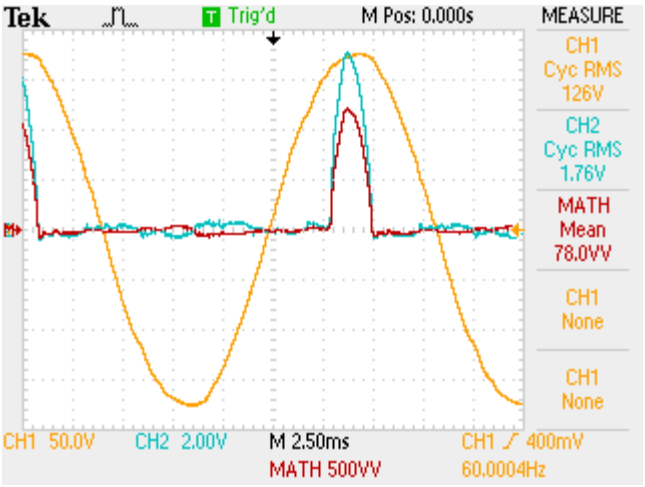


Figure 2-46: Efficiency measurement with 100 Ω sensing resistor – 51 Ω load.

In order to analyze a relationship between power efficiency and load resistance, power measurements were repeated for eight other resistive loads. Table 2-2 shows the numerical results of each measurement.

Table 2-2: Original Test Bed Adapter - Efficiency Measurements and Calculations.

Load (Ω, nominal)	Load (Ω, measured)	V_{out} (V, measured)	I_{load} (mA, calculated)	P_{load} (mW, calculated)	P_{in} (mW, measured)
51	50.87	5.461	107.35	586.25	902
100	99.27	5.471	55.11	301.52	540
150	149.66	5.476	36.59	200.36	483
200	199.67	5.476	27.43	150.18	428
300	298.16	5.476	18.37	100.57	423
510	504.88	5.477	10.85	59.42	279
750	743.19	5.477	7.37	40.36	238
1000	987.81	5.478	5.55	30.38	235
2000	1966.4	5.478	2.79	15.26	236

After obtaining results for all loads in question, a characteristic showing the relationship between power efficiency versus load resistance was obtained. Figure 2-47 shows the relationship between the two values graphically. As the impedance of the output load increases, the efficiency of the adapter decreases. On the other hand, the power consumed by components in the adapter does not change proportionally to the power delivered to variable loads. Therefore, high-impedance loads use a smaller portion of the supplied power than the internal circuitry, yielding a poor efficiency rating. However, battery loads have characteristically small impedances, so the reduction of power efficiency is never experienced by the adapter.

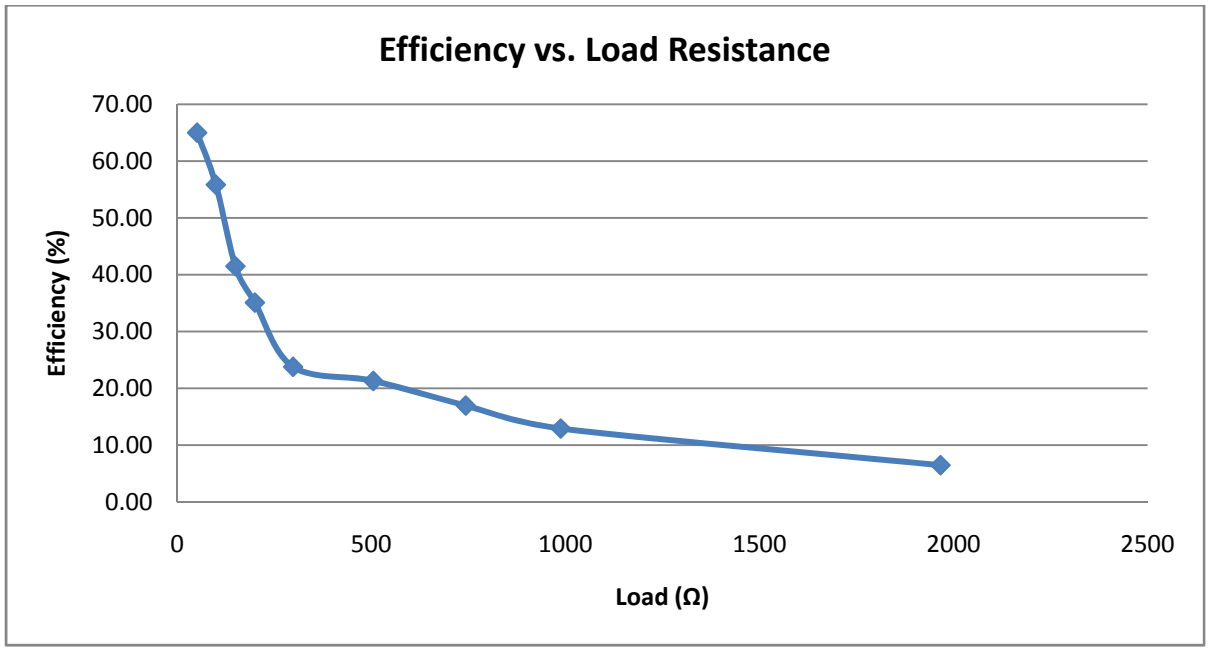


Figure 2-47: Plot of efficiency percentage versus load resistance.

Next, the team analyzed the relationship between the output power and the input power of the adapter. Figure 2-48 shows the plot of the two values. According to Figure 2-48, the operating region of the adapter is 300mW and 2.5W delivered to the DC load. In other words, the adapter is designed for a maximum nominal load of 100Ω. Once the output load exceeds this resistance, the efficiency decreases significantly. The power efficiency dramatically decreases under 100mW output power, since the NCP1011 operates in *latch-off mode*. In the operating region, the power efficiency is around 80%, which is calculated by measuring the inverse slope of the curve. Immediately below 300mW, the power

efficiency is approximately 50%. Since most battery impedances are much less than 100Ω, the operating region is wide enough for the intended application.

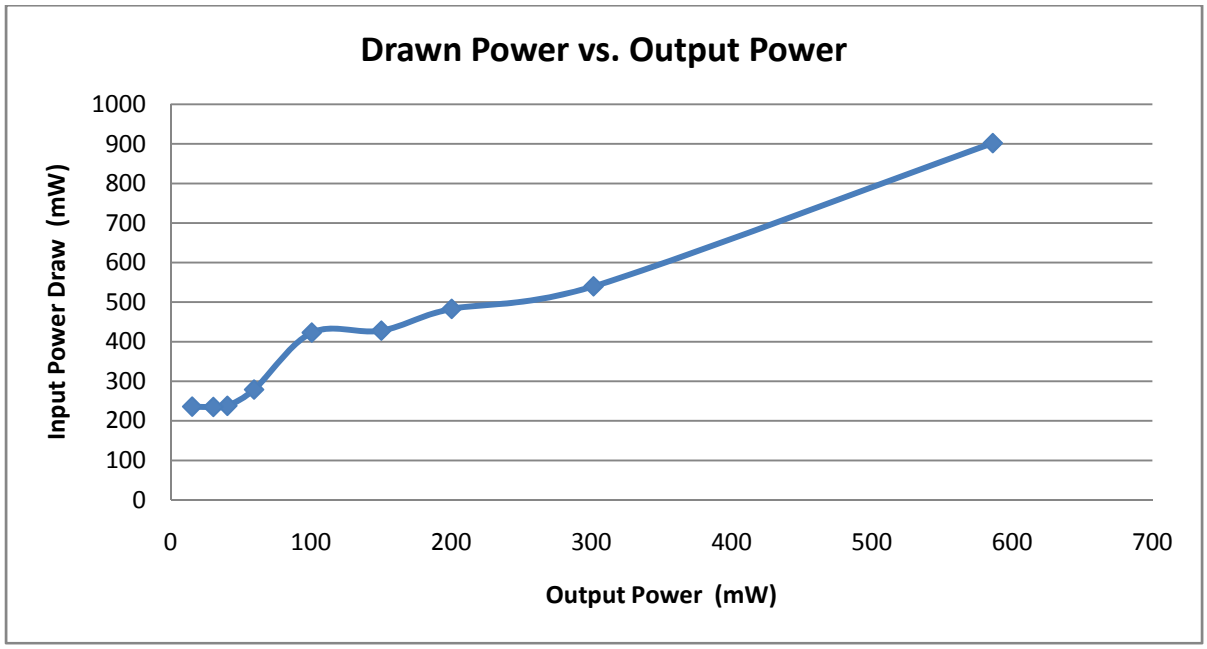


Figure 2-48: Plot of power drawn by the adapter versus power delivered to output.

After measuring the power efficiency of the adapter under a variety of resistive load conditions, the two extreme output cases were examined. An analysis of each condition provided the team with information regarding the adapter's performance under such terms. Figure 2-49 shows waveforms observed when the DC output rails were shorted, emulating a 0Ω load. The measured input current was equal to 13.9mA$_{RMS}$, yielding an input power of 1.67W. The supplied power under the output short condition is about 1W higher than the largest power consumption observed during resistive load testing. However, the input power level does not meet nor does it exceed the maximum output power rating of 2.5W. Therefore, the adapter uses less power during a short load condition, improving efficiency and meeting the over-current protection specification stipulated in the NCP1011 datasheet [28].

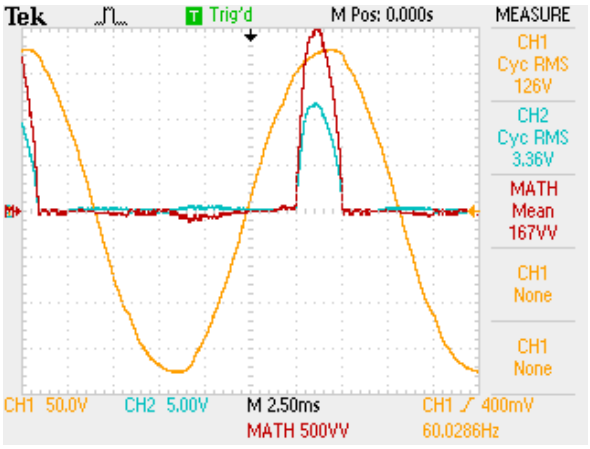


Figure 2-49: Original test bed power measurement with 100Ω sensing resistor under a shorted load condition.

In order to verify the power efficiency of less than 100mW during standby conditions, the shorted load was opened at the DC output. Figure 2-50 shows the input voltage and current waveforms used to measure the input power under the no-load condition. According to the oscilloscope's measurement of the average current, the power consumed by the adapter during standby equaled 201mW. Therefore, the actual power measured was over double the amount stipulated by ON Semiconductor's design note. Unless the Coilcraft A9619-C transformer consumes a significant amount of excess power relative to the Mesa model used by ON Semiconductor, the calculation is accurate for the adapter design. Nevertheless, the team believed that standby power could be significantly reduced.

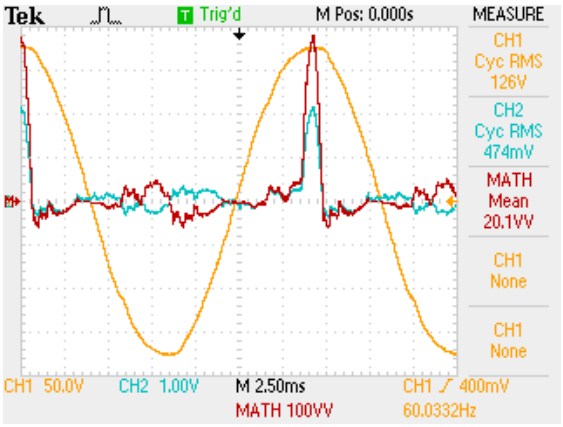


Figure 2-50: Original test bed power measurement with 100Ω sensing resistor under a no-load condition.

The final measurement of the test bed involved the connection of a cell phone battery load to the adapter. The plug that connected the cell phone to its actual charger was disconnected. The outer

sheath was then stripped to reveal the positive and negative connections to the plug. Similar to connecting the input of the adapter to the AC power cable, the plug from the cell phone's charger was soldered onto the DC output. Once this was completed, the adapter was setup to charge the cell phone.

The cell phone was turned off and then plugged into the adapter. When the adapter was plugged in, the phone began charging. In order to measure the current delivered to the battery, an ammeter was connected in series with the DC output of the adapter and the cell phone battery. When the phone indicated that it was fully charged, the ammeter was observed during the *trickle current* operation of the adapter. The trickle current delivered by the adapter allows the cell phone battery to remain charged up to peak capacity while connected to the adapter. Over a period of a couple minutes, the output current averaged 37.4mA, with occasional and very brief current spikes over 100mA.

After completing test bed assembly and measurements, the team both confirmed and disproved adapter specifications stipulated by design note DN06017/D from ON Semiconductor [27]. In the design of a more efficient wall adapter, the team plans on using an output current detection much like the high-current sensing subcircuit implemented by ON Semiconductor's design. However, the planned use of the detection would be to evaluate when the output current is insufficient, indicating a nonexistence of a load. In the specification goals section of this report, one of the stipulations for the design is the ability to detect a threshold current of 15mA. Since the lowest trickle current observed during the cell phone charging test was 37.4mA, the specified threshold is sufficiently low enough to prevent the hindering of the test bed's operation while activated. Moreover, the capacity of the battery used in the charging test was 850mAh, which is relatively small for a cell phone. Given that larger cell phone batteries draw even higher levels of trickle current, the threshold current of 15mA is reasonable.

The assembly and subsequent measurement of test bed characteristics was critical in developing the team's understanding of a modern efficient cell phone adapter. In addition, specifications made by the designers of the adapter were mostly confirmed, while some were disproved. The knowledge of the test bed's operation allowed to the team to begin formulating ideas to increase the efficiency of the original adapter.

Approach 3

The early stages of the project involved the development of three methods for creating an efficient wall adapter. All three solutions address the efficiency of the adapter while approaching the problem in different ways. Once three ideas were formulated, each proposed method was evaluated according to a particular set of criteria, producing the most viable idea. Next, two general approaches were developed to achieve desired functionality. At this point, a detailed design was needed to properly evaluate the remaining options.

Initial Proposals 3.1

In order to formulate ideas for an efficient wall adapter, it was necessary to address the specification goals outlined in Chapter 1. A low-current sense subcircuit would be required to measure the output current and determine if its value is below the threshold built into the design. Secondly, a power interrupt circuit is needed to deactivate or reactivate the adapter according to readings from the low-current sense. Finally, an interface will have to be developed between the two so the low-current sense readings and decisions will be relayed to the power interrupt. Therefore, three specific approaches to developing these stages were designed on a functional level to meet the specified requirements. Each of these solutions will be illustrated in relation to the simplified model of the AC adapter, established in Chapter 2. It is provided for reference in Figure 3-1.

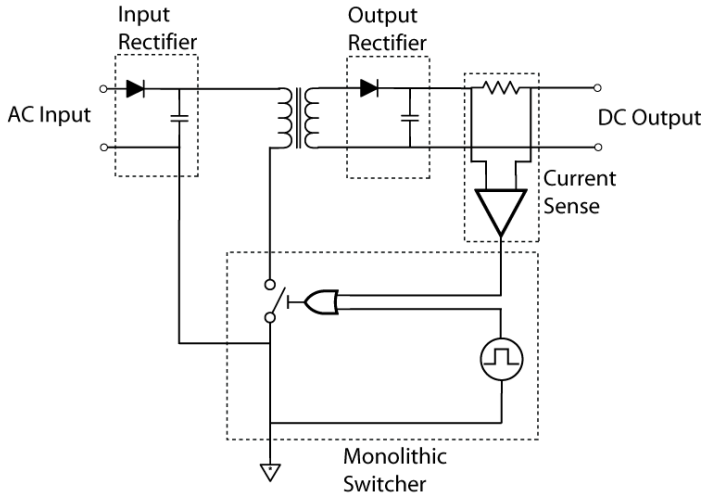


Figure 3-1: Simplified functional diagram of a modern switch mode power supply.

Polling Timer *3.1.1*

Functionally, there are two fundamental ways to actively monitor and record voltages and currents in a circuit. Both of these ways are similar to their software counterparts, and perform identical functionality in different ways. In programming, the first of these methods involves executing a `while` loop continuously under a certain condition. This behavior is called *polling*, as the loop repeatedly runs a set code while the Boolean expression given is true. In analog design, polling can be realized with a timer IC.

In whatever manner it is implemented, the timer activates monitoring circuitry and adapter functionality periodically according to a configured timescale. In the adapter design, it is desired to activate polling only when the load is disconnected. Otherwise, the timer needlessly polls the adapter while a load is connected. Therefore, the monitoring circuitry detects the DC current draw and signals the interruption circuit to either turn the adapter off or leave the adapter on according to the reading. When the adapter's power throughput drops below typical *active* levels, the power interruption circuit disables as many components as allowable. Since the timer reactivates the adapter periodically, the previously mentioned monitoring circuitry will have regular opportunities to reassess whether the adapter should remain idle, or whether it is needed for sourcing a device. The interruption circuit can then respond accordingly. The relationship of these subcircuits is illustrated in Figure 3-2.

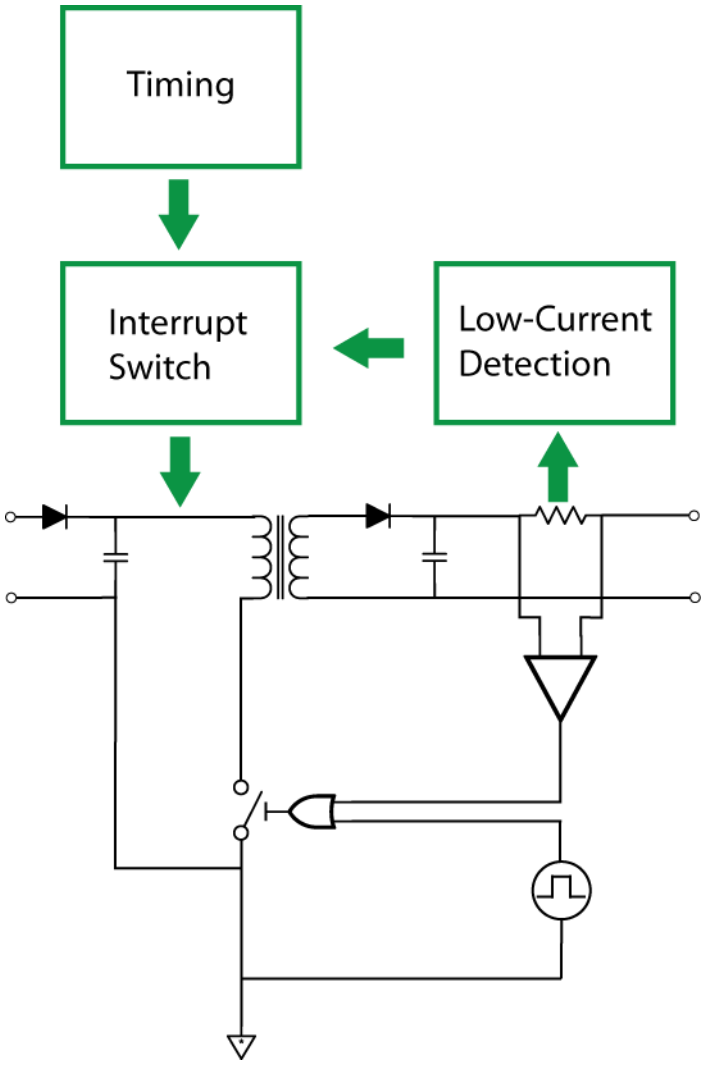


Figure 3-2: Top-level schematic of Polling Timer implementation. Using some form of current sensing at the output of the adapter, the Low-Current Detection stage alerts the Interrupt Switch, which disconnects the input to the adapter. The Timing circuitry periodically deactivates the Interrupt Switch, allowing the Low-Current Detection to re-evaluate the adapter's current state.

The benefits of using this solution are threefold. One prime advantage of utilizing the polling timer solution is that it can be used in any adapter configuration. Since the solution needs only to monitor an output and disconnect an input, it does not rely on any of the existing adapter circuitry. This non-reliance allows the solution to be self-contained and modular. Another benefit of the polling timer circuit is that the configuration is reliable. The polling feature allows room for error since the next poll can rectify any potential miscalculations, and the adapter will never become permanently dormant.

Of course, there are also some drawbacks of implementing this solution. While the self-containment of the device is a benefit in implementation and versatility, it adversely affects the cost of

such a solution. In other words, all components used in the solution circuit are additional to the components used in the original adapter design. Therefore, it is unlikely that existing parts will serve dual purposes. The additional circuitry would inevitably increase adapter size if it is integrated with present products.

Finally, it should be noted that the concept of polling can be a very inefficient technique for monitoring devices. For instance, a software program can use two techniques to trigger an event: polling or interrupts. Polling forces the processor to rerun the program code every so often, which in turn forces the processor to run constantly until the event is triggered. The program therefore uses processing power that could otherwise be allocated to other tasks. An interrupt is the most efficient technique because it *interrupts* the processor's operation to trigger an event only when a certain condition is met. Since *processing power* in this analogy is similar to power consumption, an ideal solution would have the ability to inform the adapter when a certain condition is met (i.e., when the cell phone is plugged in).

Jump Start *3.1.2*

Building off the idea that an ideal solution would utilize *interrupts*, the team concocted its second solution, nicknamed the *Jump Start*. Illustrated in Figure 3-3, this configuration utilizes the *interrupt* technique to reactivate the adapter after a disconnection. The solution works in a similar way to the *Polling Timer* idea, in that when low-current throughput is detected, the adapter is deactivated. However, instead of polling, the adapter only responds to an external trigger. When the user connects the cell phone, the remaining charge from the phone's battery triggers the current-sensing circuit. The sensing circuit flips the interrupt switch to reconnect the AC input to the adapter, effectively restarting the entire adapter. Conversely, when the user disconnects the cell phone from the adapter, the current sense signals the interrupt switch to disconnect the AC mains from the adapter. Since batteries in rechargeable devices are rarely completely depleted of energy, this technique should work even at the most critical of battery charge levels. However, to prevent an adapter from becoming inoperable due to insufficient battery charge, a simple pin-hole manual reset switch could be implemented that would re-enable the supply.

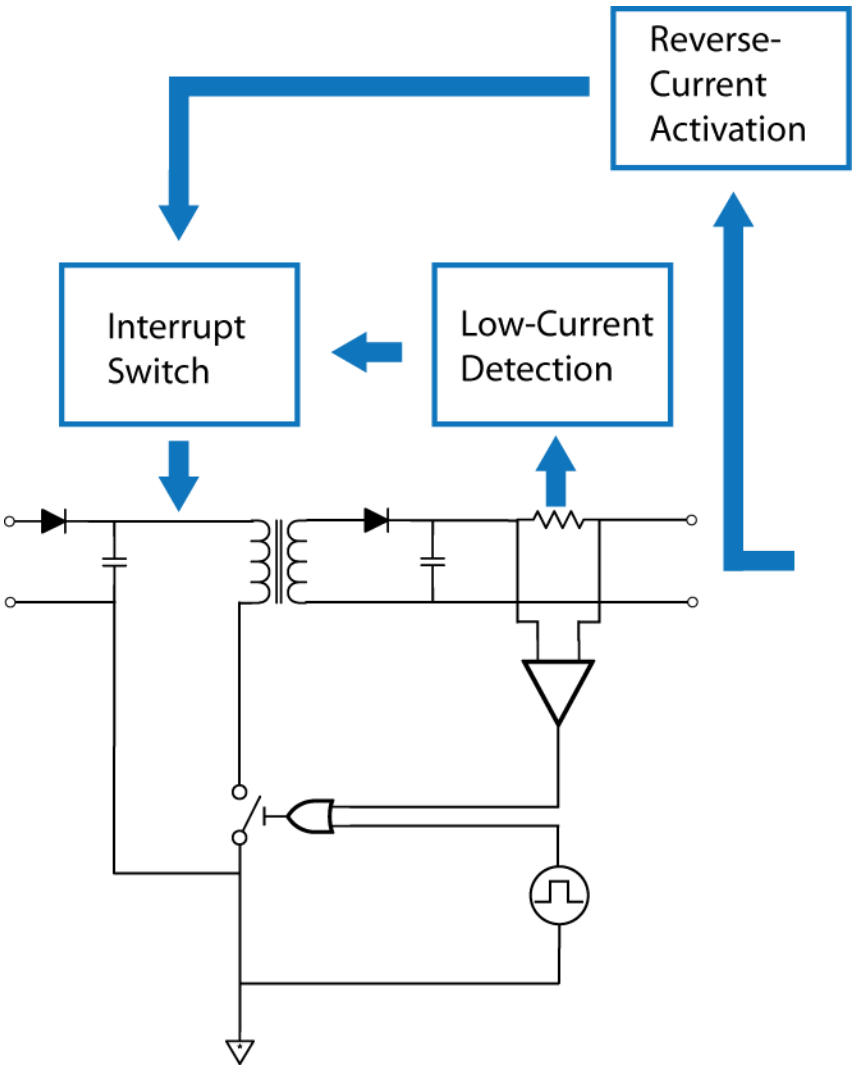


Figure 3-3: Top-level schematic of Jump Start implementation. Using some form of current sensing at the output of the adapter, the Low-Current Detection stage alerts the Interrupt Switch, which disconnects the input to the adapter. The Reverse-Current Activation deactivates the Interrupt Switch using residual power in a reconnected load device.

The *Jump Start* configuration has many positive aspects that advocate its implementation. Since a deactivated adapter receives power from the external *interrupt*, the adapter can be completely disconnected from the AC mains when idle. In addition, the current-controlled switch and monitoring components require little additional circuitry to be added to adapters.

Although this solution may seem ideal, the *Jump Star*t does contain a critical inherent flaw. The configuration depends on the energy from an external source (which is a cell phone battery in this particular application). This flaw would become a major obstacle if the cell phone battery contained too

little energy to *jump start* the adapter. The manual reset option allows adapter functionality to resume, but this is an inconvenience that the consumer should not have to endure.

Hijack *3.1.3*

The *Hijack* solution was the third idea formulated by the team, and is illustrated in Figure 3-4. The *Hijack* uses existing adapter functionality to consume little power when no load is attached to the output. In the previously discussed ON Semiconductor 2.5W Low-Power Cell Phone Charger, the NCP1011 high-frequency switching IC contains a low-power standby function [28]. The current configuration utilizes this function when high-current conditions are detected to prevent potential overloads. In the original configuration, high output current is detected by a PNP transistor switch. When the PNP turns on, current is sourced to the optoisolator. The activated optoisolator shorts the feedback pin on the NCP1011 Switcher to AC ground, forcing the IC into the low-power standby function. The *Hijack* idea reapplies this standby function to the detection of a no-load output current. When a no-load current is detected, the *Hijack* sends feedback to the IC, which would in turn cause the adapter to transition into standby mode.

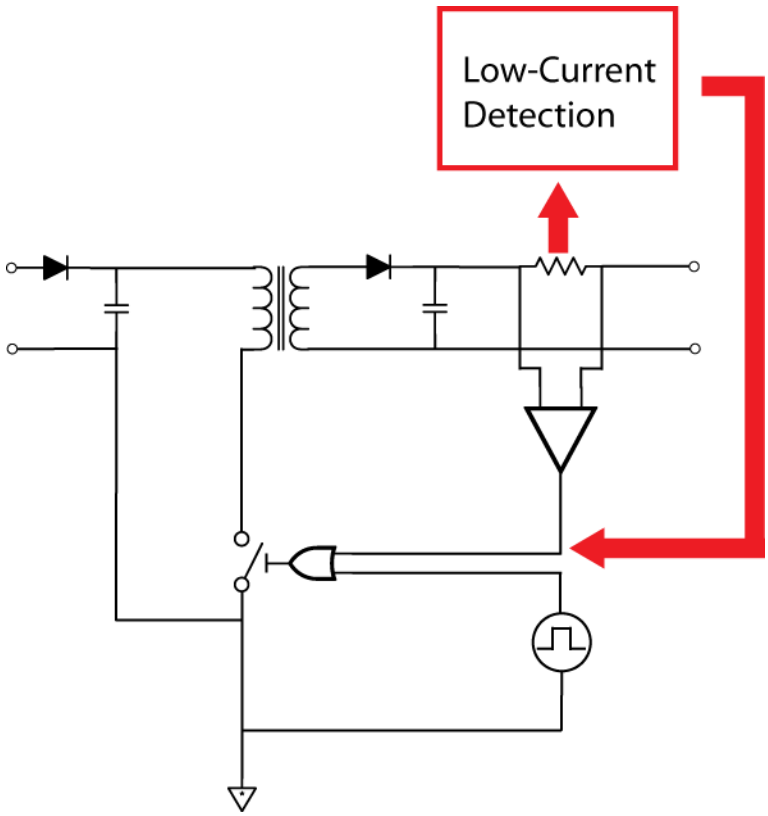


Figure 3-4: Top-level schematic of hijack implementation. Using some form of current sense at the output of the adapter, the Low-Current Detection stage triggers pre-existing reduced power state in the switching IC, typically reserved for high-current protection.

The *Hijack*'s main selling point is that it requires little additional circuitry to implement for the concerned adapter. The high-current sense arrangement on the output would simply have to be manipulated so that the optoisolator is triggered during no-load current conditions in addition to high-current conditions. Moreover, adapter size does not have to be increased since little additional circuitry is required.

However, while the idea requires few design changes to be made, there are quite a few drawbacks to using the *Hijack*. First, the switcher IC must remain powered in order for the adapter to operate in standby. It is therefore impossible to disconnect all power to the adapter during idle-use periods. Moreover, the IC's latch-off mode is not consistent with all input voltages. In other words, power savings are not consistent across different AC power signals, so savings would be unpredictable. The biggest drawback, however, is that the configuration is not universal for all SMPS AC adapters. This particular configuration utilizes a unique function of a specific IC from a certain adapter design. Other

SMPS adapters do not have the NCP1011 IC to utilize for a low-power standby function, so the *Hijack* could not be implemented.

Evaluation 3.2

After creating three approaches to address inefficiencies of the original adapter, it became necessary to evaluate each approach against the others in terms of both plausibility and potential reward. Assessing all ideas critically allowed the team to make an educated choice for preliminary design. The *Jump Start* idea seemed to be the ideal implementation since it would allow the adapter to consume 0W during standby. However, the *Jump Start*'s dependence on an external source outweighed its potential to eliminate standby power consumption. Moreover, the team discovered during initial tests with a sample cell phone that adapter reactivation via the load battery was impossible. Even with a fully-charged battery, 0V was observed across the power connections to the phone. This is likely due to the phone's internal circuitry which prevents battery discharge through the adapter.

The elimination of the *Jump Start* as a potential candidate left the *Polling Timer* and *Hijack* approaches for building an efficient wall adapter. The *Hijack* seemed like the next logical choice seeing that it required little additional circuitry for its implementation. However, the first problem associated with implementing the *Hijack* was that it relied too heavily on specific power adapter technology, such as the power saving modes of the NCP1011 switching IC. The team preferred a solution that would be applicable to any power adapter.

The effectiveness of the *Hijack* was another concern. While building the test bed, the team recorded waveforms of the NCP1011's output (pin 5). Figure 2-36 below shows the IC's typical active output characteristic, as well as the output of the same pin taken after the adapter had entered its low-power protection mode. While there is some reduction in the amplitude and frequency of the minor oscillations, the base oscillations still occur at 100kHz while the switcher moves in and out of low-power mode. Such constant oscillations were considered to be far too wasteful, a point supported by the data sheet proclaiming that the low-power *latch-off mode* allows the adapter to consume under 0.3W during standby [28]. Considering the team's goal was to reduce the original adapter's consumption by at least 75%, the *Hijack* implementation would not provide sufficient improvement to meet the stated power consumption requirement.

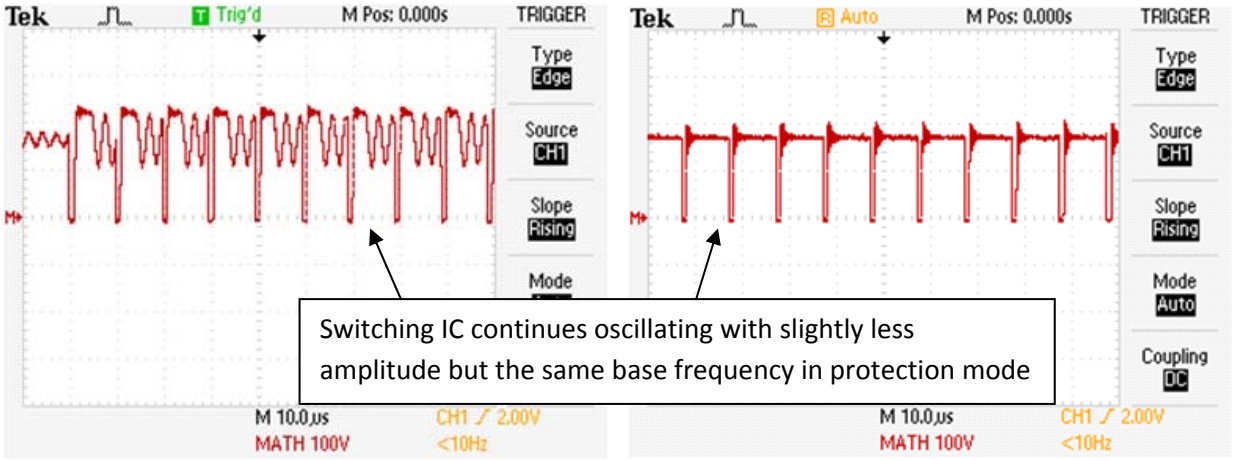


Figure 3-5: Active switching IC output (left), low power switching IC output (right). Note that even in low power mode, there is still a significant amount of 100kHz activity produced by the IC. Since the *Hijack* idea relies on this mode, it would not be able to reduce power consumption much below 300mW.

Having logically eliminated two of the three original propositions, the team was left to further develop the *Polling Timer* idea. Each of the team's ideas for the *Polling Timer* had two main functions in common: current sensing and power interrupt. It was necessary to first decide at a top level how both of these subcircuits would be implemented.

Current Sensing *3.2.1*

In order to deactivate the adapter under appropriate circumstances and decrease idle power consumption, the solution must have circuitry that can sense current. The ability to sense current would allow the adapter to identify when a load is connected and decide whether it is appropriate to deactivate. The team reasoned that the easiest way to identify such a standby condition was to monitor the current flowing through the output of the adapter. Several current-sensing options were proposed by the team as potential choices for the current-sensing stage. These ideas fell into one of two categories: magnetic devices or resistive devices. The following section describes the physical characteristics and operations of each device and reveals how the team made its choice.

Hall Effect Sensor

Hall Effect sensors utilize the Lorenz Force to output a voltage that is linearly proportional to the input current within a specified range. This effect was discovered by Edwin Hall in 1879 [37]. When an

electrical carrier carries a current of charge, and this carrier experiences an external uniform magnetic field, a force called the Lorenz Force acts perpendicular to both the current and the direction of the magnetic flux density. Mathematically, this force is expressed as:

$$F_m = qu \times B \tag{3-1}$$

The value *q* is representative of a particle's charge, *u* is the velocity of the particle, and *B* is the magnetic flux density. Figure 3-6 shows the direction of the Lorenz Force according to the configuration.

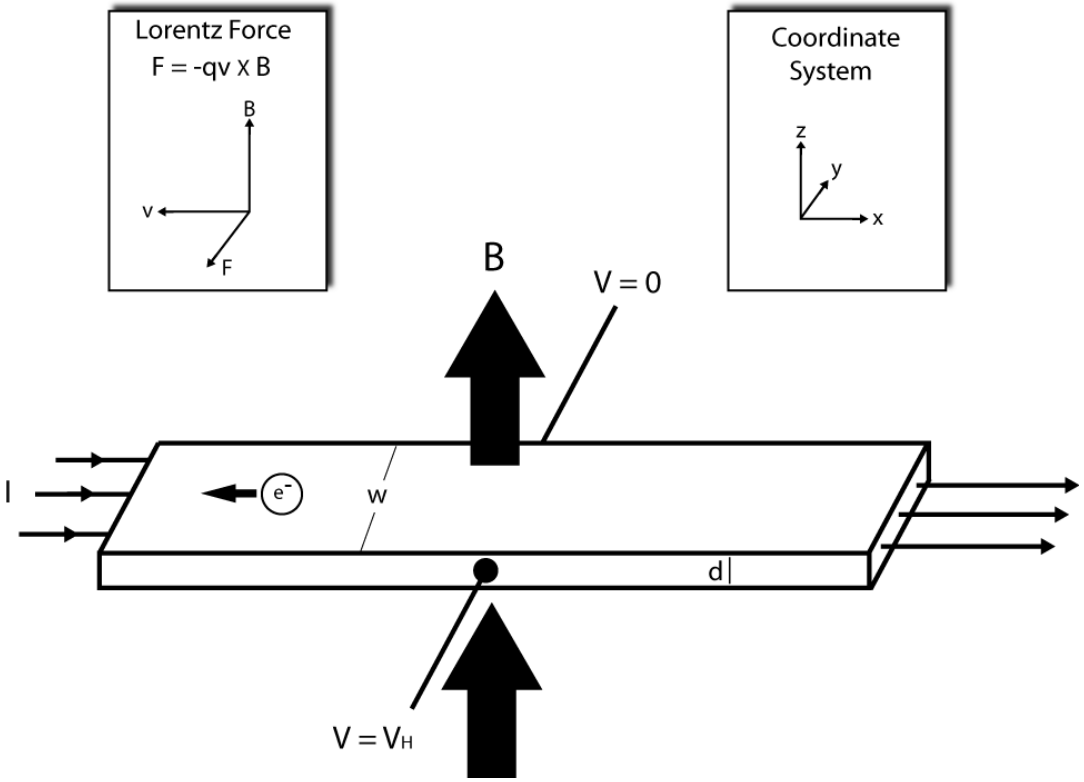


Figure 3-6: NIST Representation of Hall Effect [37].

The Lorenz Force is directed out of the page in the above arrangement. If an electrical conductor is placed in series with the current, the electron paths through the conductor will be arched toward the side of the Lorenz Force (out of the page). The arched path allows a buildup of charge on the side coming out of the page which in turn creates a potential difference between both narrow sides of the conductor, as indicated in Figure 3-6. This voltage is termed the *Hall voltage*. The Hall Effect is a powerful tool that allows a circuit to monitor current.

Hall Effect sensors exclusively monitor RMS current and output a proportional small signal AC voltage with a DC offset. If the application is set up to monitor DC voltage, small signal AC can be

eliminated using a filter capacitor, while the DC offset can be eliminated using a coupling capacitor. From this point on the representative DC voltage can be analyzed using digital or analog comparing techniques. Schmitt triggers and other op-amp-based comparators are possible solutions for analog comparison of voltages while a combination of logic gates and ADCs and DACs provide a possible digital comparator circuit. Finally, an interrupt switch would be implemented to disconnect or reconnect the adapter according to the comparator output. Latching relays and power MOSFETs are two considerations for the interrupt switch.

The principle downside to Hall Effect sensors is their overall cost to implement. The sensor itself is can cost over $1 per unit, and around $0.50 per unit in bundles of 1,000 [38]. Moreover, amplifiers and comparators are required to monitor the Hall voltage appropriately. Collectively, the cost of a Hall Effect centered current monitor can be very expensive relative to the cost of the end product.

Current Transformer

A current transformer is designed around the principle of coupled inductors with an iron core. Its basic schematic is shown in Figure 3-7 [39]. AC current is sent through the primary winding of the coupled configuration, causing a magnetic flux to appear in the iron core. The magnetic flux also varies in value causing a current to flow through the secondary winding. According to Faraday's Law this alternating magnetic flux is related to the coil voltage by:

$$V_p = N_p \frac{d\varphi}{dt} \tag{3-2}$$

Similarly, the secondary voltage can also be related to the same magnetic flux:

$$V_s = N_s \frac{d\varphi}{dt} \tag{3-3}$$

The terms N_p and N_s refer to each coil's number of turns. Dividing one equation by the other gives a ratio of:

$$\frac{V_p}{V_s} = \frac{N_p}{N_s} \tag{3-4}$$

In an ideal transformer, the conservation of energy dictates that the power input must equal the power output. In other words,

$$\frac{V_p}{V_s} = \frac{I_s}{I_p} = \frac{N_p}{N_s} \tag{3-5}$$

According to (3-5), the currents through the primary and secondary coils are also proportional to the turn ratio.

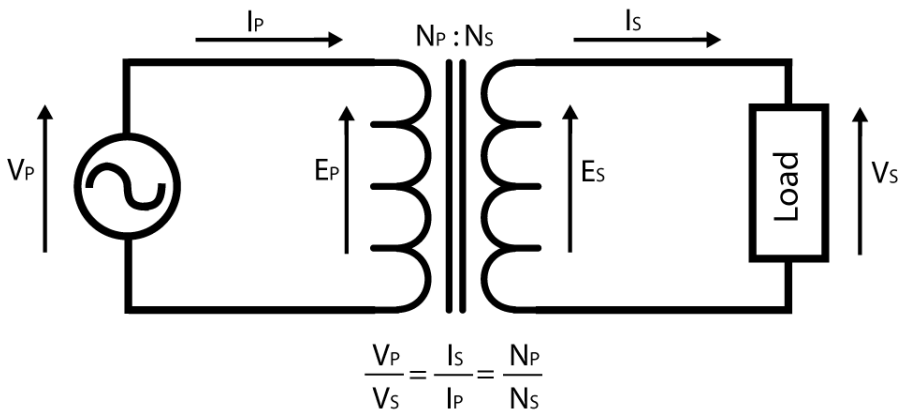


Figure 3-7: Schematic of an ideal transformer [39].

Similar to the Hall Effect sensor, the current transformer implementation would require additional circuitry to process the output of the transformer and activate an interrupt switch accordingly. The same comparing and interrupt switching techniques outlined in the Hall Effect sensor section would also be considered for the current transformer current detector.

The main downside of the current transformer is its inefficiency. Real current transformers are unable to output power equal to its input power due to internal losses. Leakage currents and magnetizing inductances in the transformer dissipate a fraction of the input power. In addition, the size and cost of current transformers are large compared to other electrical components, causing the end product to become much larger, heavier, and more expensive than originally planned.

Difference Amplifier IC

Analog Devices offers a product called the *ADM4073: Low Cost, Voltage Output, High-side Current Sense Amplifier* [40]. The IC utilizes an internal op-amp in an adder configuration biased with resistors to apply to one input a gain of 1, and the other input a gain of -1. The ADM4073 could be applied to the current-sensing circuit exactly as suggested in the schematic in Figure 3-8, with R_{sense} placed in series with the DC output of the adapter. V_{out} on the IC would then provide the current-sensing system with a voltage proportional to I_{load}. When the adapter's current drops, such as when a load device is unplugged, the output voltage of the IC would also drop. This output voltage could be used by the current-sensing stage, sending an alert to the power disconnect stage when the output current drops below the specified threshold.

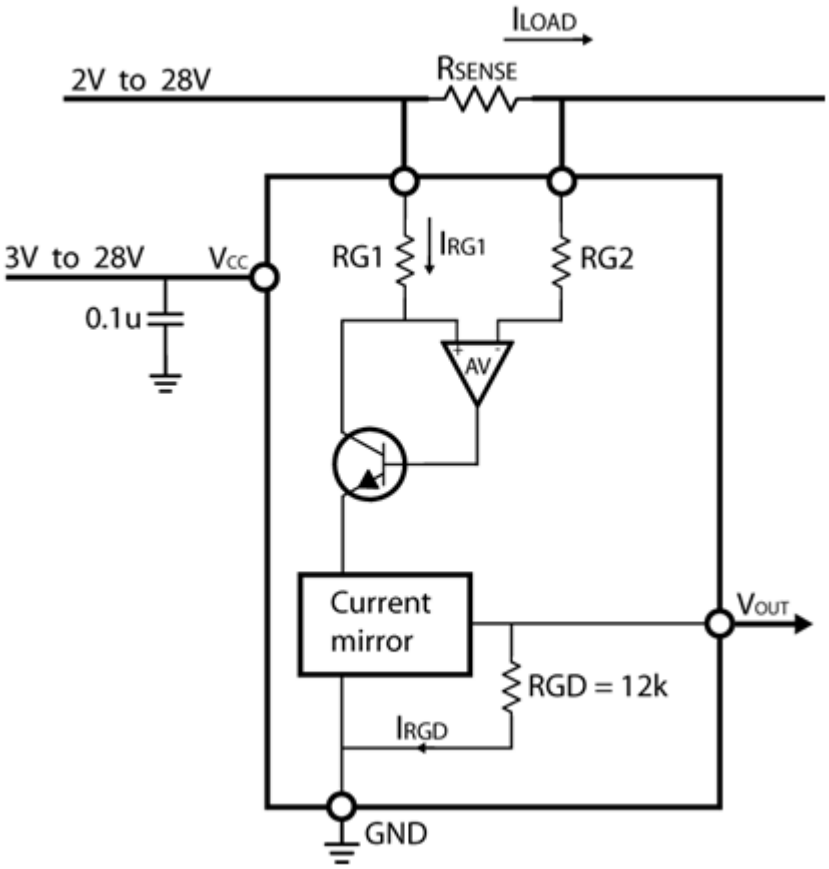


Figure 3-8: ADM4073 Low Cost, Voltage Output, High-Side, Current-Sense Amplifier Internal Schematic [40].

Pre-built for a current-sensing application, the ADM4073 would represent the easiest of the possible approaches to implement. However, it also has three potential setbacks.

1. *Cost. The ADM4073 is currently priced at $0.60 for 1000 pieces from Analog Devices [41]. While it was possible the team could fit this into its solution budget of approximately $1, it was higher than preferred.*
2. *Any tuning that may have to be done with regard to the I_{load} to V_{out} relationship and interfacing with the interrupt stage would have to be done externally since the IC is pre-built.*
3. *The device's need for supply voltage. As an active device, it will need a dedicated power connection to operate, and while the required current is a low 500µA, ensuring that it remains powered when needed presents an additional complication for the circuit's overall layout and operation.*

Custom Difference Amplifier

Often referred to as a *high-side current-sensing amplifier*, this circuit is a custom implementation of the Analog Devices ADM4073 IC described previously [40]. The high-side current-sense amplifier refers to the placement of the current-sensing resistor between the source and load, which avoids adding resistance to the ground of the circuit. Similar to the implementation of the ADM4073, load current passing through the sensing resistor develops a linearly proportional voltage across that resistor, according to Ohm's Law. This voltage is amplified by the op-amp and then subsequently used to drive the MOSFET, drawing current through R. The voltage drop across R would be equal to the voltage drop across the sensing resistor, allowing the following calculation:

$$KI_S R_S = I_O R \tag{3-6}$$

$$I_O = KI_S \frac{R_S}{R} \tag{3-7}$$

$$V_O = KI_S \frac{R_S}{R} R_O \tag{3-8}$$

The sensor output voltage is proportional to the load current as derived by (3-8). A current mirror can be included to amplify the output current by a factor of K, if a larger output voltage is desired. The entire schematic is shown in Figure 3-9 [40].

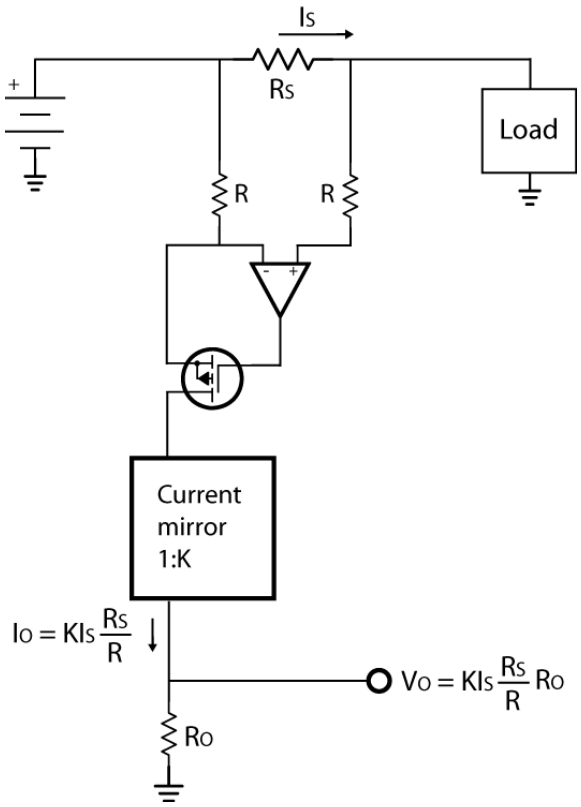


Figure 3-9: Current-sensing amplifier outputs a voltage proportional to the load current [40].

This approach to current sensing offers a couple potential benefits over buying the pre-built Analog Devices implementation.

1. Buying an inexpensive op-amp allows the custom difference amplifier to be more cost-effective than the ADM4073.
2. Each component in the custom difference amplifier can be manipulated to produce the appropriate output voltage.

BJT-Based Current Detection with Input Interrupt

The BJT-based current detection utilizes a current-sensing resistor to incur a voltage drop proportional to the output current. This technique is similar to the built-in high current detection in the ON Semiconductor adapter configuration [27]. The proportional voltage is connected in parallel to the base and emitter respectively of a NPN bipolar junction transistor (BJT). The BJT turns on when the voltage difference is around 0.65V nominal. If the BJT is turned on, it operates in the active region,

allowing a large amount of current to flow through the collector and emitter terminals. This current is directed through an optocoupler with a series resistance. The resistance drives the LED within the optocoupler when current is experienced. When sufficient current flows through the LED, the switch on the opposite terminals of the optocoupler is activated.

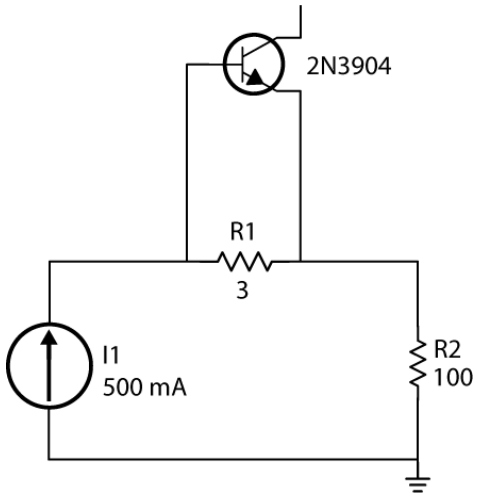


Figure 3-10: Transistor-Based Current Detection Schematic [27].

The model in Figure 3-10 exemplifies the general implementation of the current sense. The current source I1 represents the output current of the adapter, which is 500mA. Most of the current flows through current-sensing resistor R1 while a small amount of current flows through the base of the 2N3904 BJT. When current through the 3Ω resistor produces a voltage of about 0.7V, the BJT turns on and allows current to flow from its emitter to its collector terminals. The collector-emitter current equals the voltage across the 1kΩ resistor divided by its resistance, which is around 30mA. The same current activates the optocoupler. Once the output current of the adapter drops below 200mA, the voltage across the base and emitter of the BJT becomes less than 0.7V. In effect, the transistor and the LED in the optocoupler are turned off.

Once the presented current-sensing ideas were conceived, the team created a qualitatitive selection table for the various methods. This way, an educated, deliberate decision was made to implement each idea. This is shown in

Table 3-1.

Table 3-1: Qualitative Analysis of Current-Sensing Devices.

	Hall Effect	Transformer Based	Difference Amplifier IC	Custom Diff. Amplifier	BJT
Cost-Effectiveness	**NO**	**NO**	*Yes*	*Yes*	*Yes*
Low Power	---	---	*Yes*	*Yes*	*Yes*
Availability	---	---	*Yes*	*Yes*	*Yes*
Durability	---	---	*Yes*	*Yes*	**NO**
Ease of Manipulation	---	---	**NO**	*Yes*	---
Compactness	---	---	---	*Yes*	---

The criteria shown in the first column of the table are listed in order of importance. Since the purpose of the envisioned device is to save money, the final product must be designed for the smallest cost possible. The Hall Effect and transformer-based options are simply too expensive, so they were quickly eliminated as viable options. Low power consumption is an inherent requirement for an efficient wall adapter, and the remaining three options consume a negligable amount of power compared to the overall consumption of the adapter. Furthermore, each of the three current-sensing devices are readily available at several electronic distributors.

However, the BJT current-sensing operation varies greatly with introduced temperature change. It was determined that the BJT current sensor was not plausible for the adapter design due to its high rate of variability during operation. The pre-built difference amplifier was also subsequently removed as a viable implementation. Although the ADM4073 provides an integrated current-sensing solution, the manipulation of internal components is not possible. Since manipulation of the current sensing will be needed to obtain a threshold output current of 15mA, the custom difference amplifier implementation was chosen as the most beneficial approach to building a low-current sense for the adapter.

Power Interrupt *3.2.2*

The power interrupt stage is vital to the *Polling Timer*'s power saving method. In order to shut down or disconnect parts of the adapter to save power, a component capable of interrupting power is necessary. Several power interrupt methods were discussed as potential choices to disconnect the high-voltage rail of the adapter from the primary winding of the transformer. These ideas fell into one of two

categories: semiconductor devices or electromechanical switches. The TRIAC, power MOSFET, and the power BJT are all semiconductor devices, and the optorelay is an electromechanical switch. The following section will describe the physical characteristics and operations of each device and present the criteria used in choosing the actual implementation.

Power BJT

In general, power transistors are similar in operation compared to their small-signal counterparts. However, power transistors are custom-designed to handle higher voltages. One of the primary advantages of using a power BJT is its high bandwidth and its isolation between the base and the transistor's other two terminals. It is also capable of handling high-power signals between its collector and emitter. However, there are many downsides to using a power BJT as a disconnect device.

Power BJTs have relatively smaller gain factors compared to small signal BJT's [42]. While a β-factor of 100 is typical for a small signal BJT, an active-region amplification of 10 is not uncommon for a power BJT. The small β-factor of the power BJT necessitates a large bias current at the base of the transistor in order to produce a large current through the collector and emitter terminals. In addition, the β-factor varies greatly with a change in temperature, which could pose a problem due to the heat dissipated by the transformer.

Power MOSFET

Unlike the power BJT, a power MOSFET requires little input current to bias the device due to its gate isolation. Moreover, it is well-known that "the gates of some 10-A power MOSFET's can be driven by the output of standard logic gates" [42]. Furthermore, this driving current does not fluctuate greatly with temperature variation. In addition, the channel resistance is designed to be very small, which allows the input current from the AC line to pass through uninhibited.

One of the major downsides of using a power MOSFET is that the breakdown voltages between the drain and source and vice-versa are not equivalent. In other words, most power MOSFET's are not able to handle high-voltage AC signals. When an N-Channel MOSFET is placed in reverse bias, the reverse breakdown voltage is high, allowing much of the source current to flow. On the other hand, if the N-Channel MOSFET is placed in forward bias, the breakdown voltage is low. Overall, power

MOSFET's are used widely in high-power DC disconnect circuits, but not as an alternating-current signal disconnect.

TRIAC

The acronym TRIAC stands for *triode for alternating currents*. It is therefore not surprising that TRIAC's are used heavily in AC power applications like dimmer circuits. Like other transistors, the TRIAC is driven via its gate terminal to allow current to flow through its anode and cathode terminals. Unlike the power BJT, the TRIAC can be driven with a low power signal. Therefore, the output of a logic gate or an operational amplifier would be suitable drivers of a TRIAC power disconnect.

Relays

Relays are electromechanical switches that rely on magnetism to physically connect and disconnect contacts. Unlike semiconductor devices, relays are able to physically break a circuit and provide total isolation between the break. This feature allows relays to be effective power interrupt switches.

The types of relays chosen by the team for possible implementations was the optorelay and the latching relay. The optorelay utilizes the principle design of an optoisolator but uses a relay in lieu of a transistor. The latching relay is triggered at its gate and *latches* on one contact until a second trigger voltage is experienced. The benefit of the optorelay is that it disconnects the input while maintaining isolation between the input and output stages. The latching relay, on the other hand, holds its position even when the gate power is disconnecting, providing independence from a constant supply power source.

However, because of its mechanical nature, relays have inherent flaws for relatively small electronic applications. First, relays are larger in size compared to semiconductor devices. Since AC adapters are small in nature, it would be difficiult to implement a relay in a cell phone wall adapter. In addition, most relays require a significant bias current to drive.

Table 3-2 shows how each of the potential power interrupt devices were evaluated against the others. Like Table 3-1, the criteria listed in the first column of the table are in order of importance from top to bottom. The first criterion used to evaluate the power interrupt devices was cost-effectiveness.

The capability of handling high voltage is next in importance since the determined method must disconnect an input rated at 170V. Low power consumption is third in the list to comply with one of the team's long term goals of lowering power consumption of the adapter. Thereafter, the chosen implementation must be widely available for future mass production.

Table 3-2: Qualitative Analysis on Power Interrupt Devices.

	Power MOSFET	Optorelay	TRIAC	BJT	Solid-State Relay
Cost-Effectiveness	*Yes*	**NO**	*Yes*	*Yes*	**NO**
High Voltage Capability	*Yes*	---	*Yes*	*Yes*	---
Low Power	*Yes*	---	*Yes*	*Yes*	---
Availability	*Yes*	---	*Yes*	*Yes*	---
Durability	*Yes*	---	*Yes*	**NO**	---
Compactness	*Yes*	---	*Yes*	---	---
Ease of Switching	*Yes*	---	*Yes*	---	---
AC-Disconnect Capability	**NO**	---	*Yes*	---	---

After evaluating each potential method by its cost-effectivness, the three semiconductor options still remained: the power MOSFET, the TRIAC, and the power BJT. Although each of these devices is comparable in size, the power BJT has a small β-factor, thus requiring a significant bias current to drive it. Moreover, active-region operation of the power BJT introduces unwanted complication in design. Lastly, the power BJT is highly susceptible to voltage spikes and can fail under high-temperature conditions (e.g. heat from transformer). It was for these reasons that the power BJT was dropped from the team's power interrupt considerations.

The last criterion shown in Table 3-2 is the AC disconnect capability. While there are a multitude of power MOSFETs that can handle high-voltage DC signals across their drain and source terminals, there are few that can withstand high-voltage AC signals. TRIACs, on the other hand, are designed for such conditions. Normally, the difference between disconnecting the power before and after the rectifier is negligible. However, since the final product would ideally consume close to 0W during no-load conditions, the team chose the triac as their power disconnecting device.

Consolidation 3.3

After evaluating each initial proposal, the polling timer technique was chosen as the team's general approach to designing an efficient wall adapter. In particular, it was determined that the polling timer would be designed with a low-current sensing circuit as well as a power interrupt switch. After critiquing several options for each, the custom difference amplifier was chosen for detecting the adapter's output current and the TRIAC was selected to activate and reactivate the adapter accordingly. The next step involved the further specification of the polling timer design. The team first determined that there were two passive devices that could serve as the foundation of the control input to the timer: inductors and capacitors. While capacitors charge and discharge to certain voltages, inductors vary between current peaks and troughs. However, inductors are relatively expensive compared to their capacitive counterparts. In addition, the team previously discovered the difficulties of monitoring current levels in a circuit. These reasons encouraged the team in choosing a capacitive-based control for the polling timer.

Once the polling method was defined, the team formulated ideas that utilized capacitive polling. Two basic implementations were discussed; one configuration placed the capacitive control on the output stage of the circuit, while the other arranged the control on the input side. In order to determine which implementation was most logical, the team analyzed each by several criteria: size, cost, and power consumption.

Capacitor-Based Polling Configuration *3.3.1*

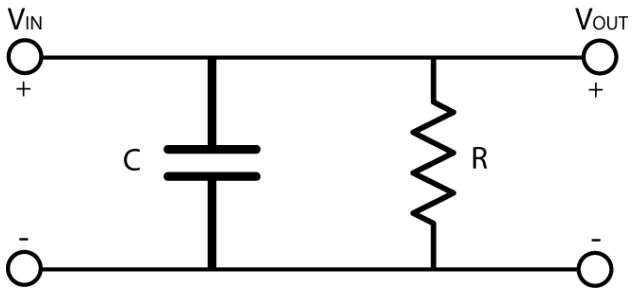


Figure 3-11: First-order RC circuit.

In order to meet the low-power specification goal stipulated in Chapter 1, the team made a concerted effort to utilize passive components as much as possible. The passive timer consists of a simple, first-order RC circuit whose time constant is determined by the product of the resistance and capacitance as given in (3-9).

$$\tau = RC \tag{3-9}$$

For long delays between polling, a large combination of the resistance and capacitance is needed. The time constant specifies the delay required for the output voltage to match 63% of the input voltage. If a polling duty cycle of 50% is desired, the capacitor can charge during polling and discharge when dormant.

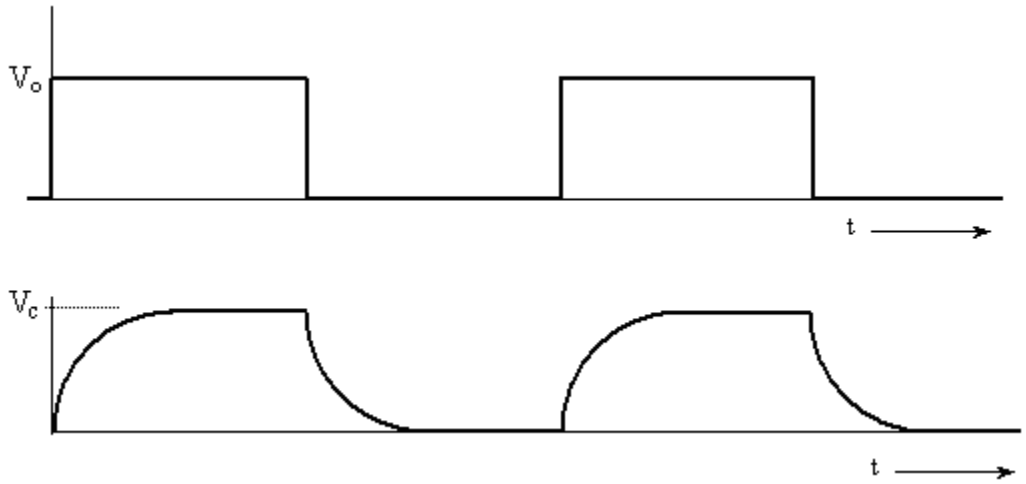


Figure 3-12: Example polling duty cycle of 50% for capacitive-based polling method.

The voltage across the capacitor V_c in Figure 3-12 shows the charging and discharging characteristics of a capacitor.

Ideally, this particular solution would involve a much shorter duty cycle. When the adapter polls, a large surge of current is experienced at the output, and power dissipation reaches a maximum. Therefore, keeping this polling as short as possible attenuates this surge. The complication in obtaining the characteristic shown in Figure 10 is that it requires two time constants: one for the charging voltage and another for the discharging voltage.

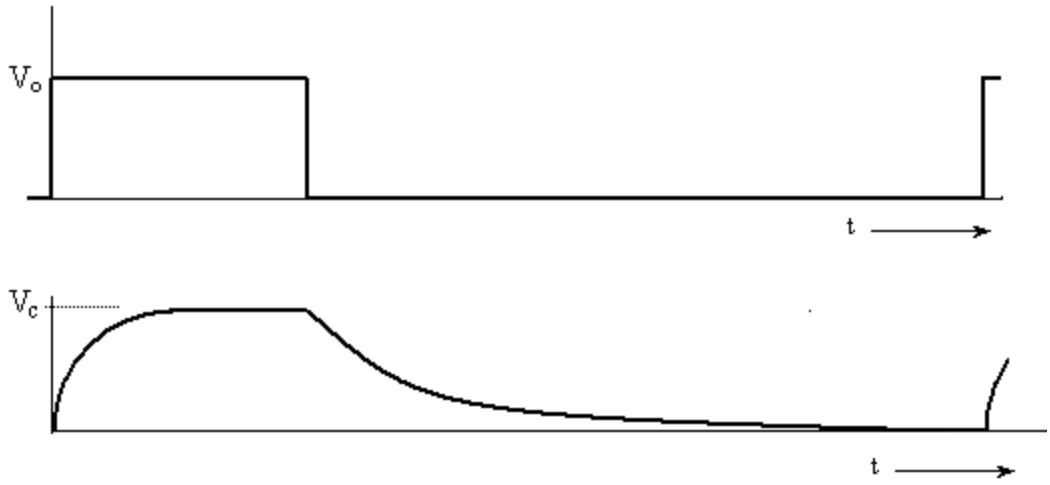


Figure 3-13: Example polling duty cycle much less than 50% for capacitive-based polling method.

The transient behavior of the capacitor during charging and discharging is the characteristic used to provide a passive way of polling the adapter. The intended flow of such a system can be explained using the block diagram in Figure 3-14.

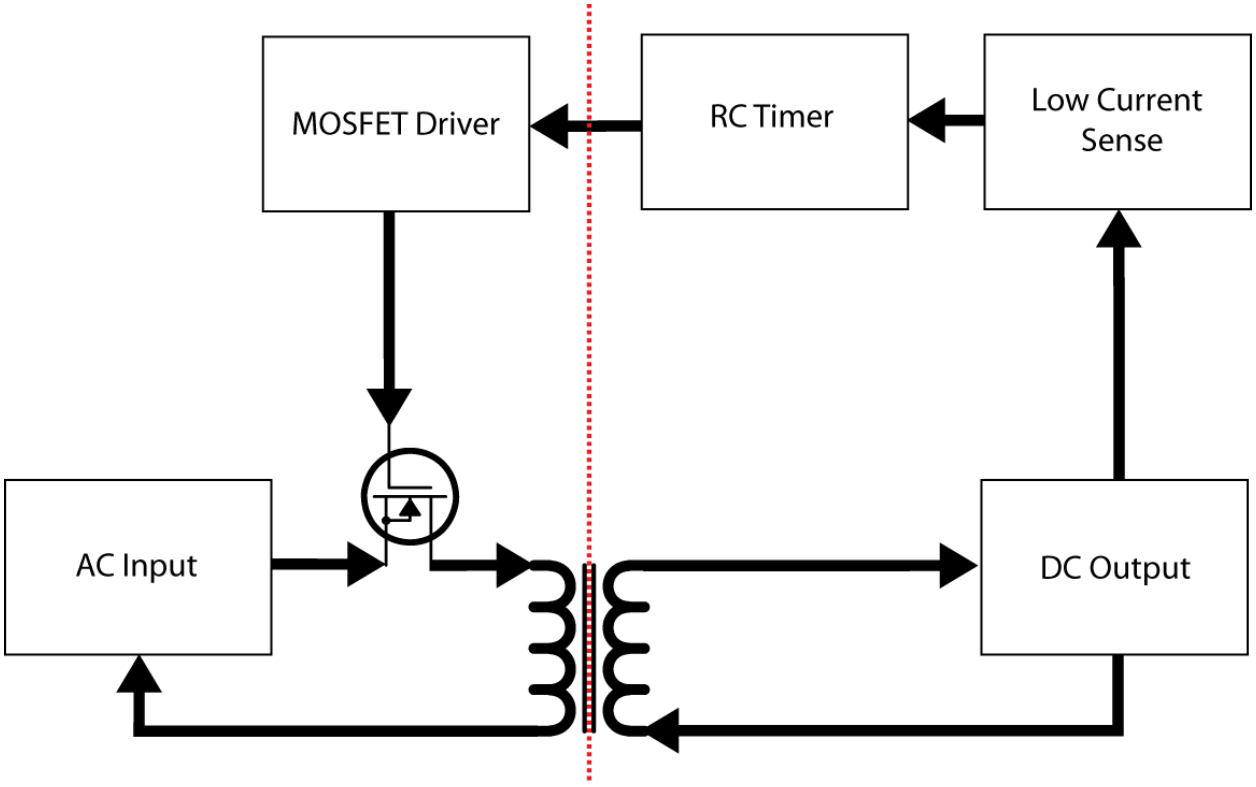


Figure 3-14: Functional block diagram of efficient wall adapter with capacitive-based polling.

Prior to a detailed analysis and design of this configuration, the team ascertained the several advantages and disadvantages of using the capacitive-based polling method. In terms of cost, the natural inclination of purchasing one capacitor instead of multiple components for a timing subcircuit suggests a benefit. However, large-value capacitors required for such a circuit may be large in physical size as well, providing complications in implementing the circuit into a present adapter. In addition, the power consumption of this method is questionable, since extra energy will be required to charge the capacitor to the proper voltage. Moreover, power surges caused by the constant reactivation of the adapter may increase power consumption. Although simplistic in operation, the capacitive-based polling timer may provide many complications if implemented in the adapter.

Monostable Multivibrator-Based Polling Configuration 3.3.2

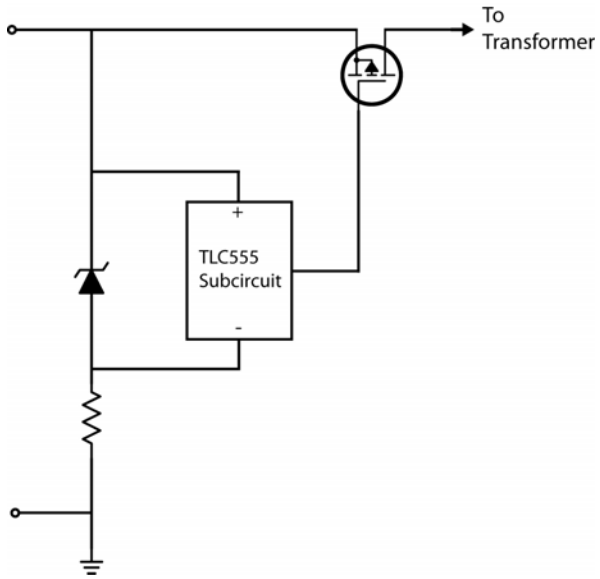


Figure 3-15: Schematic for adapter reactivation. The TLC555 subcircuit periodically reactivates the P-Channel MOSFET to re-enable connection between the top voltage rail to the transformer. The Zener-based voltage regulator provides the necessary voltage level to the TLC555 subcircuit.

Clearly, the capacitive-based polling timer has inherent flaws that must be addressed during the design phases. An alternative to this configuration is one built around a timer IC. The multivibrator-based polling timer uses a low power oscillator to drive the adapter on and off. One of the most popular timer IC's on the market is the 555 timer. The following table overviews the 555 timer's pin descriptions [43]:

Table 3-3: Pin Descriptions of 555 Timer [43].

Pin #	*Pin Label*	*Description*
1	Ground	Reference Voltage
2	Trigger	High Signal Starts Timer
3	Output	Output of Timer
4	Reset	Low Signal Stops Timer
5	Control Voltage	Allows Manipulation of Cycle
6	Threshold	Allows Normal Cycle to go Low
7	Discharge	Timing Capacitor Discharges through Pin
8	V_{DD}	Supply Power

Using the pin layout described above, the timer can operate in several multivibrator modes: astable, monostable, or bistable. The astable multivibrator is one of the most popular timer configurations due to its perpetual operation. In fact, the team considered using this configuration in the polling circuit. However, its constant operation is also a drawback. Even if a load was connected at the output, an astable multivibrator, by definition, would not settle into a stable state, but would rather continue polling the adapter. Polling while a load is connected does not necessarily disrupt functionality, but repeats a needless task. Therefore, the team chose to operate the timer in monostable mode.

A monostable multivibrator, like its astable counterpart, operates continuously regardless of its output state. However, unlike the astable multivibrator, a monostable multivibrator operates under one stable output condition. In order to disrupt this steady output, a signal must be sent to the trigger pin of the 555 timer. The timer remains in the unstable state until the designated time period expires. At this moment, the output switches levels and returns to the stable state. For the polling timer approach, this interrupt event would occur during low-current conditions on the output. The event would cause the trigger pin to switch from low to high, turning off the adapter. After a programmed amount of time, the output would return high, activating the adapter.

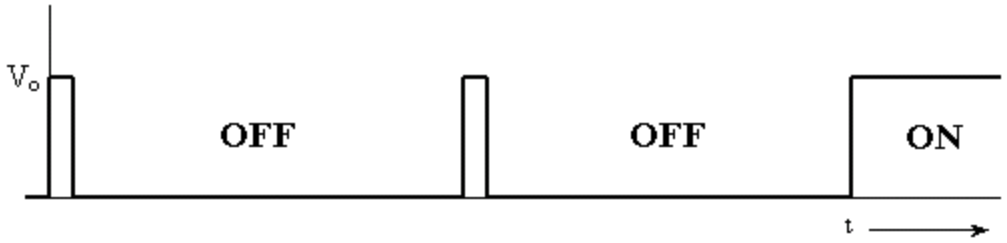


Figure 3-16: Example polling cycle of monostable multivibrator [44].

The first two pulses in Figure 3-16 resemble the temporary reactivation of the adapter. When the circuit determines an insufficient amount of current is being drawn by the output, the monostable 555 timer returns to a low state, effectively deactivating the adapter. The third reactivation resembles the output voltage when a DC load is connected. At this point, the 555 timer returns to its stable state, leaving the adapter active.

The 555 timer subcircuit is shown below for monostable mode. Resistors R and capacitor C form the RC timing circuit for the unstable region of operation. This configuration was chosen as the baseline design for the polling timer.

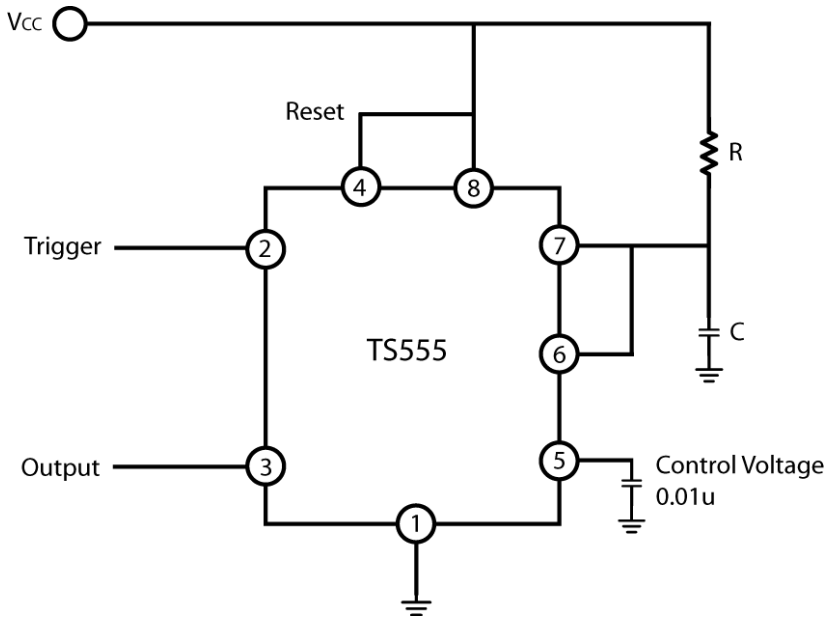


Figure 3-17: Schematic showing monostable configuration of the TS555 timer [44].

Overall, it seems that the monostable multivibrator-based polling timer has several positives that make it an attractive choice. However, there are two key drawbacks to this implementation. Along with the possible cost increase of a monostable configuration, the multivibrator-based polling timer must operate on the AC-side of the adapter. The absolute maximum supply voltage for the 555 timer is 18V, so a voltage of 170V is incompatible. Therefore, a voltage regulator is needed to supply the necessary power to the 555 timer subcircuit.

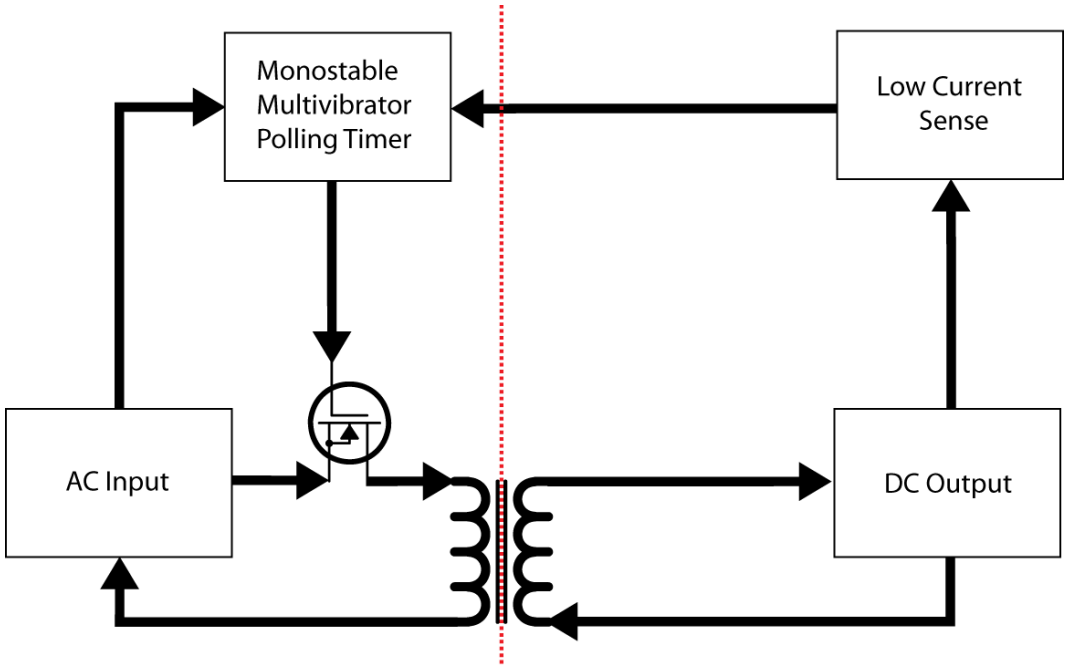


Figure 3-18: Functional Block Diagram of Adapter with Monostable Multivibrator Polling.

Once the team determined the means to power the multivibrator subcircuit, a functional block diagram of the entire adapter circuit was created, shown in Figure 3-18. The next step involves the analysis of each functional block in order to determine the detailed design of the entire system.

This chapter determined the following important points:

- A polling timer would be used as the foundation of the efficient adapter design.
- A custom difference amplifier would serve as a basis for designing the current-sensing subcircuit.
- A TRIAC would serve as the basis for designing the power disconnect subcircuit.
- A monostable multivibrator would be used to implement the polling, or periodic reactivation of the adapter.

Detailed Design 4

Once preliminary design was completed for each functional block of the proposed solution, the team began implementing each stage at the component level. While two separate techniques are presented for periodic adapter reactivation, the manner in which the output current was detected as well as how the input to the adapter was disconnected from remainder of the circuit is consistent for both approaches. Therefore, this section describes the systematic progression of designing the current-sensing and power interrupt functionality of the efficient wall adapter.

Looking at the specification goals of this project, the additional circuitry must reduce the power consumption by 75% while only adding $1.30 to the overall cost of the adapter. Therefore, the following guidelines were used while designing the added circuit stages:

1. *A large majority of additional components should be passive*
2. *Only basic ICs should be implemented (op-amps, optocouplers, timers)*
3. *Capacity of energy storage devices (i.e., capacitors and inductors) should be minimized*

The list of guidelines above allowed the team to design an efficient wall adapter that met the specification goals outlined for this project.

Low-Current Sensing Circuit 4.1

In the previous chapter, a functional flowchart was presented to demonstrate low-current sensing functionality. In addition, it was determined that the team would use a difference amplifier and current-sensing resistor combination to measure the output current. Since a current-sensing resistor already exists in the original adapter design, the team used resistor R4 for low-current sensing as well. The functional diagram in Figure 4-1 lists the interface stages required to process the information from the current-sensing circuit in order to make a decision with regards to raising the low-current flag.

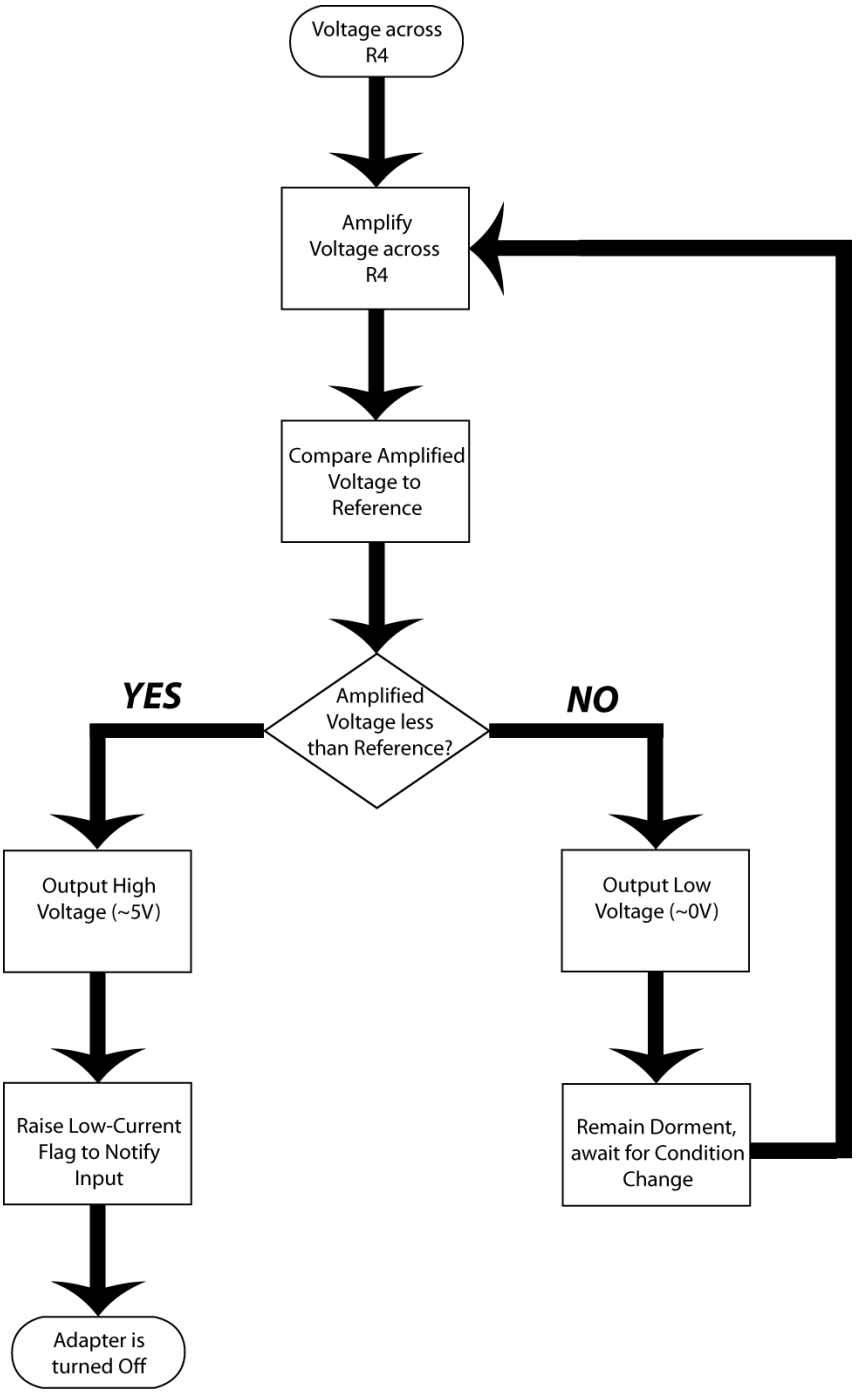


Figure 4-1: Processing diagram for current sense stage of proposed solution, from sensing resistor to flag output.

As current flows through the DC top rail, a proportional voltage drop appears across resistor R4. The magnitude of the voltage is on the scale of tens of mV, so measuring the output current according to the proportional voltage drop across R4 is difficult using basic electrical components. In fact, an output current of 50mA produces a voltage drop across R4 of 60mV.

In order to appropriately measure the current, the proportional voltage must be amplified. Once the voltage drop across the current sense resistor is amplified between 0V and 5V, the output current can be effectively measured. Despite amplification, the proportionality between the amplified voltage and the output current around the 15mA threshold is linear. Therefore, the amplified voltage is indicative of the output current for measured currents around 15mA.

To determine whether the measured output current is above or below the threshold of 15mA, a reference voltage indicative of a 15mA output current is required for comparison. The sensing circuitry can then make a simple one-to-one comparison of the amplified voltage and the reference voltage. If the amplified voltage is greater than the reference, the low-current sense should take no action, since the output current is sufficiently high. However, if the amplified voltage is less than or equal to the reference, the circuit must notify the power cutoff stage of a low-current condition so the adapter can be deactivated temporarily due to an insufficient amount of output current.

Once the functional operation of sensing circuitry was determined, the team listed a set of requirements for the low-current sense subcircuit. Methods required for functionality are:

1. Measurement of the adapter's output current
2. Manipulation of current measurement for comparison with threshold value
3. Comparison of reference indicative of threshold current to measured output current
4. Notification of low-current condition to input stage

The first and second requirements were met by using the custom difference amplifier with a current-sensing resistor. The remaining requirements were met using an open loop comparator and an optoisolator.

In analog design, the operational amplifier can be arranged to function as a digital gate. Figure 4-2 shows the op-amp configured as an open-loop amplifier with an inverted output. If the voltage input V_{DIFF} is higher than the reference voltage V_{REF}, the voltage at V_{OUT} will be low. On the other hand, V_{OUT} will be high if V_{DIFF} is less than V_{REF}. In the open loop configuration, the voltage difference at the input is amplified with a very high gain. When V_{DIFF} is slightly greater than V_{REF}, the negative voltage difference between the non-inverting and the inverting terminals drive V_{OUT} down to the minimum possible output voltage. In the same way, V_{OUT} is pulled up to the maximum allowable output voltage when V_{DIFF} is less than V_{REF} due to a positive voltage difference between the input terminals. If both V_{DIFF} and V_{REF} equal the same voltage, V_{OUT} will equal the average of the supply rails. When both inputs of the open loop comparator are equal, the amplifier is functioning at its DC operating point. Many amplifiers

are designed with an output voltage of half the supply voltage range at the DC operating point. For the comparator shown in Figure 4-2, V_{OUT} would equal 2.5V. The three input scenarios and related output voltage conditions are shown in Table 4-1.

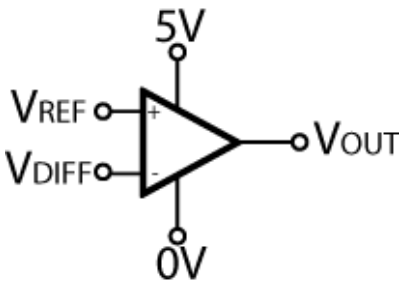


Figure 4-2: Inverting open loop comparator configuration used in low-current sensing for proposed solution; used to raise a flag high if sensing resistor's voltage is low, and vice-versa. Also sets the cutoff level with V_{REF}.

Table 4-1: Input/output characteristic of inverting comparator (Figure 4-2) for three possible input scenarios. A flag voltage sufficient to activate the disconnect stage should be raised in any of the cases.

Input Scenario	Output Behavior
$V_{ref}>V_{diffamp}$	$V_{out} \approx 5V$
$V_{ref}=V_{diffamp}$	$V_{out} \approx 2.5V$
$V_{ref}<V_{diffamp}$	$V_{out} \approx 0V$

Realistically, operational amplifiers contain non-idealities that affect their operation. For instance, the output of a general-purpose op-amp is only able to come within a few hundred mV of the supply rails. This behavior is attributed to the internal MOSFETs of the output stage within the op-amp. When the output voltage is between its minimum and maximum values, the MOSFETs in the output stage operate in the active region. However, when the voltage difference at the input drives the output toward a supply rail, one of the MOSFETs in the output stage is forced to operate in the triode region, causing the output voltage to converge before hitting the supply rails. Another characteristic of an op-amp is a voltage offset at the input of the device. Since all MOSFETs cannot be manufactured exactly to design parameters, a very small voltage difference is required between the non-inverting and inverting inputs in order to obtain a 2.5V output.

In the design of an efficient wall adapter, the input offset of a general-purpose op-amp will not adversely affect system functionality. Since the output threshold current was selected to be a value

much less than the smallest trickle current drawn by cell phone batteries [21], the comparator output will only change with the disconnect or the reconnect of an output load. On the other hand, the output voltage limits must be taken into consideration when choosing an optoisolator. Nevertheless, the function of an open-loop comparator configuration meets the third requirement for the low-current sensing circuit design.

Like the high-current sensing circuitry already existent in the original adapter design, the low-current sense needs a way to communicate output current status to the AC side of the adapter. Optoisolators are often used to relay information from one isolated circuit to the other. The LED inside an optoisolator is placed in the circuit that communicates the information. When the LED is turned on by one circuit, a photosensitive switch is closed to communicate the necessary information to the other circuit. In the efficient wall adapter, the low-current sense needs to be interfaced with an optoisolator to alert power cutoff circuitry of a low output current condition. Figure 4-3 shows the open loop comparator directly connected to a MOC3023 optoisolator [45]. Theoretically, the output of the comparator should be able to drive the LED of the optoisolator either on or off. However, there are many issues with connecting the LED directly to the output of the comparator.

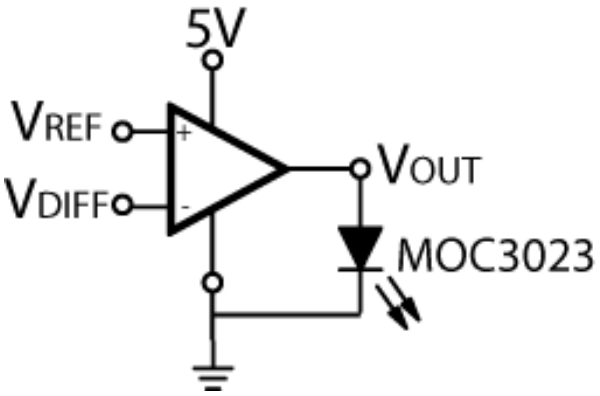


Figure 4-3: Theoretical arrangement of inverting comparator and LED of optoisolator. However, current and voltage limitations must be overcome.

Fundamentally, there are two reasons why this arrangement will not function as expected. First, an activated LED incurs a specific voltage drop and requires a minimum amount of current. Therefore, a resistor must be placed in series with the LED to incur the remaining voltage drop, as well as regulate the amount of current that flows through the LED. Moreover, the output current limit of an op-amp introduces another non-ideality of the device. However, if a transistor was used in an emitter

follower configuration, the output of the comparator would be able to drive the LED on and off without sourcing an excess amount of current. Figure 4-4 shows the actual implementation of low-current sensing feedback circuitry.

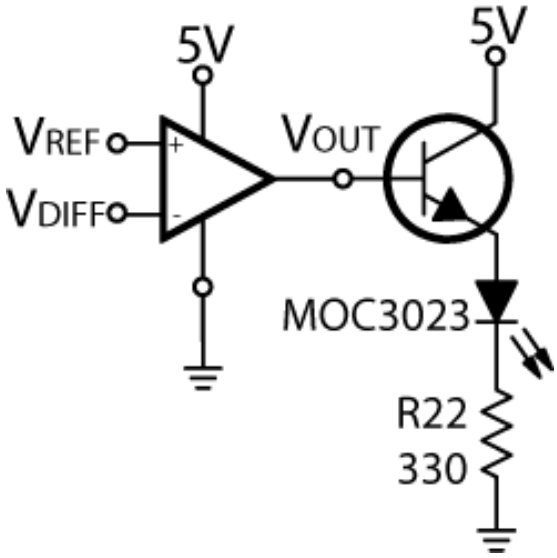


Figure 4-4: Inverting comparator with current amplifier on output to drive LED. This circuit should light properly and on command.

Assuming the comparator has a rail-to-rail output, V_{OUT} can either be 5V or 0V. If V_{OUT} is equal to 0V, the NPN BJT will operate in the cutoff region, since the voltage drop across the base-emitter junction is 0V. In effect, the LED will be off, and the voltage drop across the collector and emitter of the BJT will be 5V. When V_{OUT} is 5V, the base-emitter voltage drop will be around 0.7V (if silicon-based), and the potential at the emitter of the BJT will be 4.3V. Since the LED in the MOC3023 optoisolator is rated for a forward bias voltage drop of 1.15V, the voltage drop across resistor R22 will consequently be 3.15V. As a result, around 9.5mA would flow through the LED, allowing it to emit light given that the minimum forward bias current rating is 5mA.

Figure 4-5 shows a comprehensive schematic of low-current sense circuitry. The difference amplifier stage precedes the comparator and optoisolator. The input terminals of the difference amplifier are connected across the current sense resistor R4, and its output is connected to the inverting input of the open loop comparator. Once the general layout of the circuit was determined, the values of individual components were calculated.

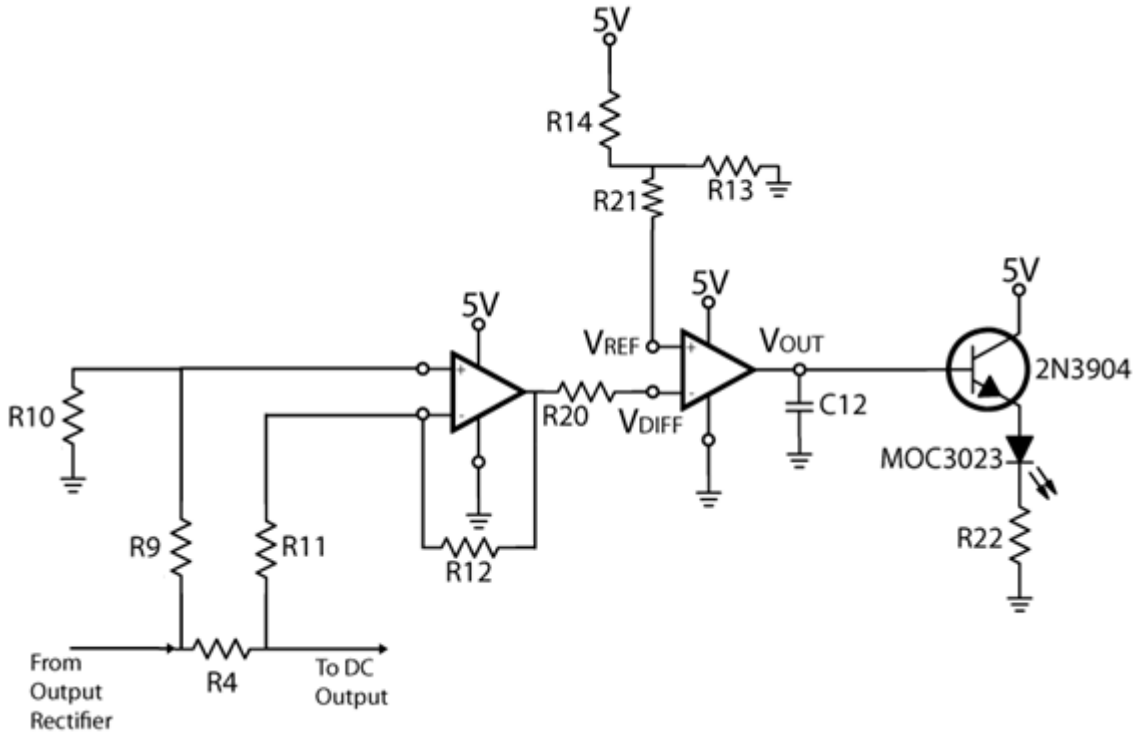


Figure 4-5: Preliminary schematic of low-current sense stage prior to calculation of component values.

The OPA344 was chosen by the team to perform comparing and difference amplification for the low-current sense circuit since it was a rail-to-rail input and output op-amp compatible for a single supply of 5V [46]. Although other less-expensive options could have been pursued, the OPA344 was readily available, so the team used it for both purposes during initial testing of the modified adapter.

Capacitor C12 is placed at the output of the comparator as a signal filter. Since the adapter uses a switching frequency of 100kHz, high-frequency behavior can be observed at output filter capacitor C4. To prevent the possibility of high-frequency noise activating the LED in the optoisolator, capacitor C12 is chosen large enough to filter unwanted components out of the signal. The capacitance of C12 was chosen to be 10µF since it was both a sufficiently-high value and a common component in the adapter.

Given a 1.2Ω value for R4, the ratio of resistances in the difference amplifier can be determined. According to equations specified in the last chapter for the difference amplifier, the output voltage of the subcircuit is as follows:

$$V_{DIFF} \cong \frac{R_{10,12}}{R_{9,11}}(V_+ - V_-) \cong \frac{R_{10,12}}{R_{9,11}} V_{R4} \qquad (4\text{-}1)$$

The output of the difference amplifier is simplified by (4-1) to be equal to the voltage drop across R4 multiplied by the ratio of the resistances in the configuration. In the difference amplifier,

resistances R10 and R12 are equal, and R9 and R11 have equal resistances. Choosing the right values for resistors R9 through R12 was done according to system level requirements. In particular, the difference amplifier needed to magnify the voltage drop to equal V_{REF} when the output current was 15mA. Initially, V_{REF} was chosen to be 2.5V to provide the maximum range of amplification for both sufficient and insufficient currents. If the expected amplified voltage is divided by the measured voltage drop across R4, the gain of the difference amplifier can be estimated:

$$A_{DIFF} \cong \frac{R_{10,12}}{R_{9,11}} = \frac{V_{REF}}{(15mA)(1.2\Omega)} = \frac{2.5V}{18mV} \cong 140 \quad (4\text{-}2)$$

In order for the output of the difference amplifier to be 2.5V, the ratio of R10 and R12 to R11 and R9 must be at least 140. Assuming that 5% tolerance resistors are used, the gain of the difference amplifier should be designed slightly above this calculation to compensate for variable resistances. Therefore, a value of 2kΩ was chosen for R9 and R11. R10 and R12 were assigned resistances of 360kΩ to provide an approximate gain of 180. Ideally, the threshold current for the adapter is equal to 2.5V divided by the gain of 180, which is then divided by the 1.2Ω resistance of R4. The resulting nominal threshold is 11.6mA.

Next, the values of R14 and R13 can be determined since V_{REF} is equal to 2.5V. Accordingly, R14 and R13 were set to 510kΩ in an effort to minimize power consumption of the voltage divider. Resistors R20 and R21 were each set to 100kΩ to bias the inputs to the comparator equally. Using Kirchhoff's Voltage Law (KVL), the maximum resistance of R22 was calculated:

$$V_{out} - V_{BE} - V_{LED} - I_{LED}R_{LED} = 0 \rightarrow 4 - 0.7 - 1.15 - (0.005)R_{22} = 0 \quad (4\text{-}3)$$

$$R_{22} \leq 430\Omega \quad (4\text{-}4)$$

To ensure consistent functionality, R22 was chosen to be 330Ω. Figure 4-6 depicts the first schematic of the current-sense subcircuit with all appropriate component values included.

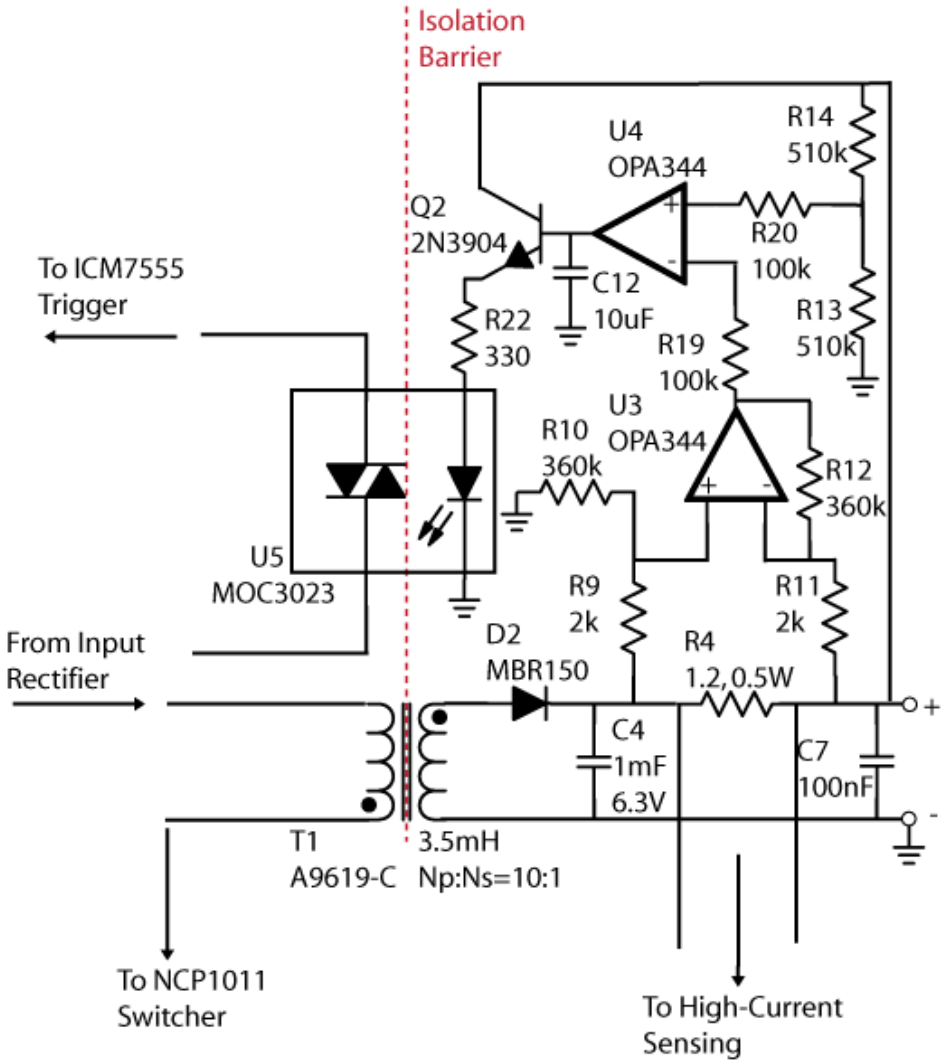


Figure 4-6: First schematic of low-current sense stage of proposed solution, with component values.

Given a DC current, a proportional voltage is produced across the 1.2Ω resistor, which is amplified by approximately 180. If the current is sufficiently high, the comparator output will remain low and the current amplifier will remain off. The moment this current falls below a certain value (between 10mA and 15mA), the amplified voltage will be less than the reference voltage of 2.5V, and the comparator will be driven high. NPN BJT Q2 will provide current to the LED of the MOC3023, signaling a low-current condition. Since this stage of the solution includes active devices, the output current will be monitored as long as the adapter is on. Once the adapter is deactivated, the current sense circuit shown in Figure 4-6 will turn off.

The low-current sense stage provides all necessary processing to correctly calculate output voltage and to signal adapter reactivation when appropriate. The first requirement stipulated in the

beginning of this section is met using the current-sensing resistor R4 to output a linearly proportional voltage to the experienced current. The voltage drop across R4 is appropriately handled through amplification, which is realized by the difference amplifier implementation. The amplified output of the difference amplifier can be accurately compared to the reference voltage set by a simple resistor-based voltage divider. Depending on the level of output current, the feedback stage of the low-current sense can alert the input stage of an undercurrent condition via the MOC3023 optoisolator. In order to poll the adapter effectively, power cutoff and timing circuitry are required on the AC side of the adapter.

Earlier in this section, it was explained that the OPA344 was used for implementing the op-amps in both the comparator and difference amplifier parts of the low-current sense. Although the OPA344 is low-power and its input and output voltage range are rail-to-rail, the price of each op-amp is expensive compared to the project's overall budget (*See Appendix A*). Consequently, a cost-effective op-amp with similar specifications was needed for the final design of the low-current sense. Texas Instruments also manufacturers a dual-channel operational amplifier IC called the TLC27L2 [47]. This particular model was chosen for two reasons. The cost of purchasing a dual-channel IC was less than the total cost of two, one-channel ICs, and the output voltage range is rated 1V less than the supply rail difference. The *TLC27L2 Dual-Channel Operational Amplifier* [47] from Texas Instruments provides a cost-efficient alternative to the OPA344 [46].

Adapter Cutoff and Reactivation Circuit 4.2

Once the low-current sensing subcircuit was completed, the team began designing the power cutoff and reactivation circuitry. Circuitry is required to reactivate or deactivate the adapter on the AC side of the circuit according to the output load condition. Shown in Figure 4-7 is the required processing flow of the cutoff circuitry.

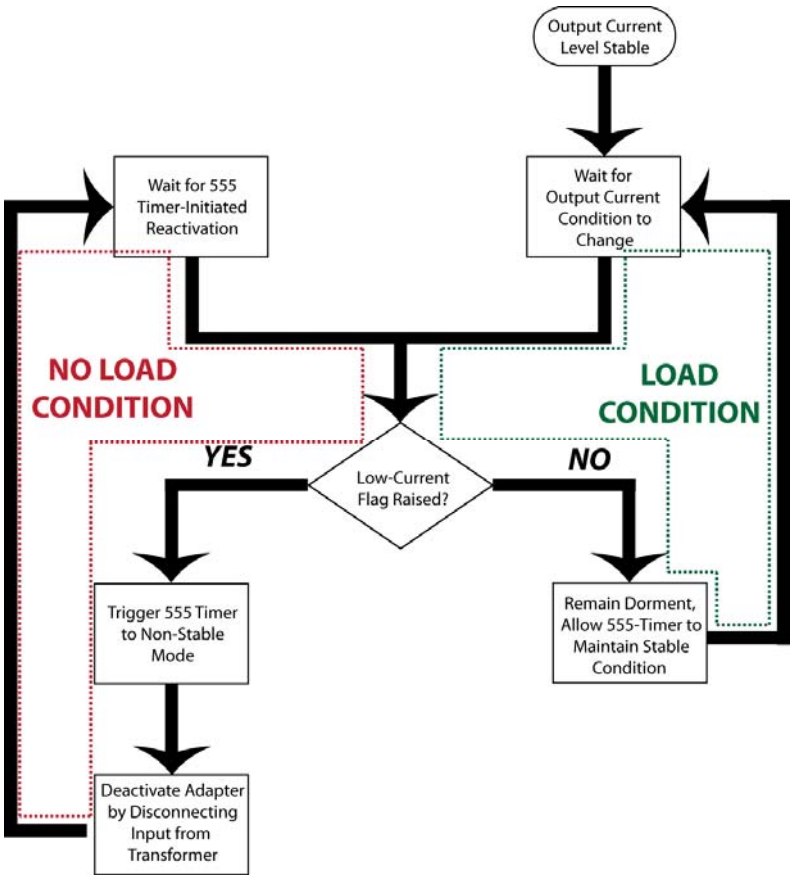


Figure 4-7: Processing diagram for power cutoff stage of proposed solution, including low-current flag reaction.

The flowchart begins with the initial condition that the output current level is sufficient and the adapter is operating normally. At this point, the cutoff and reactivation subcircuit awaits input from the feedback of the MOC3023 optoisolator. If the output current condition changes from normal to an excessive amount above the maximum rating, the subcircuit maintains stable operation since the high-current sense preconfigured in the adapter handles such cases. However, when the output load is disconnected, the MOC3023 triggers the cutoff circuitry to deactivate the adapter. Once the cutoff circuitry cuts the power connection to the primary winding of the transformer, the system waits for a determined period of time before reactivating the adapter. While there is a no-load condition on the adapter output, the flowchart follows the left-hand process flow. When a load is connected to the DC output, the process flow follows the right-hand side of the chart. The active nature of the cutoff and reactivation circuitry eliminates the possibility of a permanently deactivated adapter.

Once the functional operation of cutoff and reactivation circuitry was determined, the team listed a set of requirements for the subcircuit. Methods required for functionality were:

1. *Utilization of a TRIAC for adapter deactivation and reactivation*
2. *Triggering polling of adapter during no-load conditions via MOC3023 optoisolator*
3. *Periodic reactivation of adapter during polling*

Unlike the low-current sensing circuitry, there were two proposed ideas to implement the power cutoff function. Although both methods used the polling timer approach described in Chapter 3, one design utilized active polling while the other depended on passively polling the adapter.

555 Timer-Based Polling Method *4.2.1*

555 timers are versatile ICs that are widely applied in many analog and digital circuits. Using a combination of resistors and capacitors, the 555 timer can be implemented as a bistable, monostable, or astable multivibrator. Each type of multivibrator configuration could be used to realize the periodic reactivation requirement for the power cutoff circuitry. However, the 555 IC requires continuous power for proper operation. Therefore, the timer must be powered whenever the adapter is plugged into the AC input, regardless of output load connectivity. The problem with powering the 555 timer on the AC side of the isolation is producing a constant low DC voltage from a high-voltage source.

Since most inexpensive 555 timers require input sources of 5V to 15V, the team analyzed ways to step down the $170V_{DC}$ rail to a workable low-voltage signal. Common voltage regulators, such as buck-boost converters, are relatively expensive to purchase. LED driver devices were also researched as a possibility, like the Supertex HV9921 [48]. The Supertex HV9921 accepts a DC voltage ranging from 20V to 400V and converts it into a 7V output. While the Supertex HV9921 was cost-effective, it consumed a substantial amount of power, particularly between 175 mW and 300mW on its own [48]. It was finally determined that a Zener-based voltage regulator provided the ideal solution.

Zener regulators are often overlooked as a voltage converter utility because they operate at poor efficiencies with high-impedance loads. For instance, a Zener diode may only deliver 100µA to the load while sinking 10mA. However, because the Zener breakdown voltage is only around 3% of the supply voltage of 170V, a very large resistor can be placed as a pull-up resistor between the diode's anode and AC ground. The presence of a large pull-up resistor would significantly reduce the power consumed by the Zener regulator.

Using a Zener rectifying diode to step down voltage is a fairly simple process. The $170V_{DC}$ input to the converter encounters a series resistance. This resistance is high in value in order to incur a large

portion of the voltage while producing a low current. The latter part of the converter consists of the Zener diode and the 555 timer as the load. The 1N5229B breaks down in the neighborhood of 4.3V given a minimum current of 20mA [49]. Since the timer is placed in parallel with the 1N5229B Zener, the 555 IC experiences the same voltage at its supply. At a supply between 3V and 5V, the TS555 timer draws a nominal 250µA of current [44]. Therefore, the difference between the source current from the high-voltage rail and the supply current of the timer is the sink current of the Zener diode. There is no issue of damaging the diode in this configuration since the power rating of the 1N5229B is 500mW [49].

The following scenario demonstrates the viability of this configuration. The series resistance RS is assigned a value of 500kΩ and the load resistance RL is assigned a value of 12kΩ. Although the nominal value of the 1N5229B is 4.3V, the resulting voltage drop in this scenario will be 3.7V in order to limit power consumption. If there is a 3.7V drop across the Zener, then there is a 166.3V drop across RS. The source current can then be calculated:

$$I_S = \frac{166.3}{500k} = 333\ \mu A \tag{4-5}$$

The source power, in turn, can also be determined:

$$P_S = 170 \times I_s = 56.5\ mW \tag{4-6}$$

Assuming this is the finalized value, the adapter's standby consumption would be greatly reduced, since 56.5mW is much less than the rated 300mW.

In the same manner, the load current can be found:

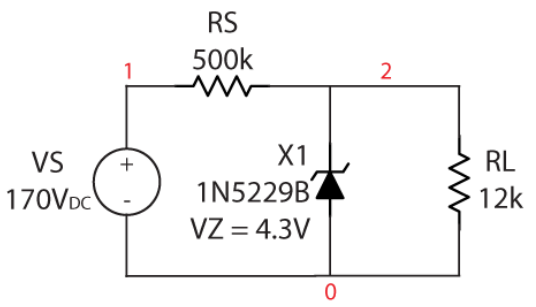
$$I_L = \frac{3.7}{12k} = 308\ \mu A \tag{4-7}$$

This value is slightly larger than the nominal supply current of 250µA, but can still represent an actual load current. The sink current of the Zener diode is now found subtracting the source and load currents:

$$I_Z = 333\ \mu A - 308\ \mu A = 24.3\ \mu A \tag{4-8}$$

This current value is very small, allowing a majority of the source current to flow through the load. The efficiency of this regulator is attributed to the large attenuation of the source voltage to the load voltage. If a small supply voltage was applied to the regulator, the sink current of the Zener would become a larger proportion of the total current supplied by the source, effectively decreasing the efficiency of the system.

The netlist and schematic shown in Figure 4-8 represent the scenario described above. The configuration was simulated in PSpice using a model created by Diodes, Inc. for the 1N5229B [50].




```
*EWA Reactivation Simulation*

Vs 1 0 170
RS 1 2 500k
X1 0 2 DI_1N5229B
RL 2 0 12k
.SUBCKT DI_1N5229B 1 2
*        Terminals A K
D1 1 2 DF
DZ 3 1 DR
VZ 2 3 2.18
.MODEL DF D ( IS=95.8p RS=0.620 N=1.10
+ CJO=244p VJ=0.750 M=0.330 TT=50.1n )
.MODEL DR D (IS=19.2f RS=0.377 N=2.82 )
.ENDS

.PROBE
.TRAN 10us 10ms 0ms
.END
```

Figure 4-8: PSpice schematic and netlist of Zener-based voltage converter for supplying power to 555 timer; created to determine the viability of using the 170V adapter input to run a low power IC and associated circuitry [50].

The simulated circuit produced the plots shown in Figure 4-9 and Figure 4-10, which represent critical voltages, currents, and power values.

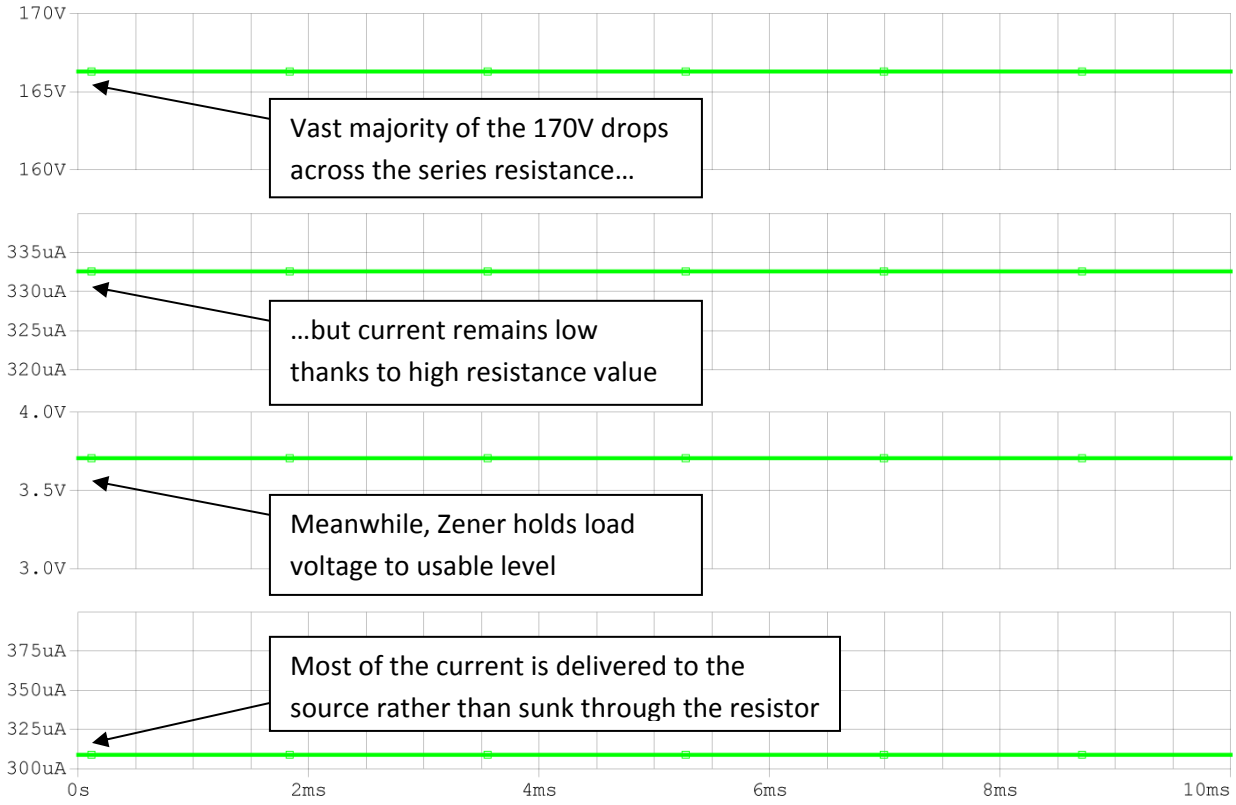


Figure 4-9: PSpice simulation results; voltage and current plots for Zener-based voltage converter configuration shown in Figure 4-8 schematic. Circuit appears to function as expected, creating a relatively small voltage drop across the Zener.

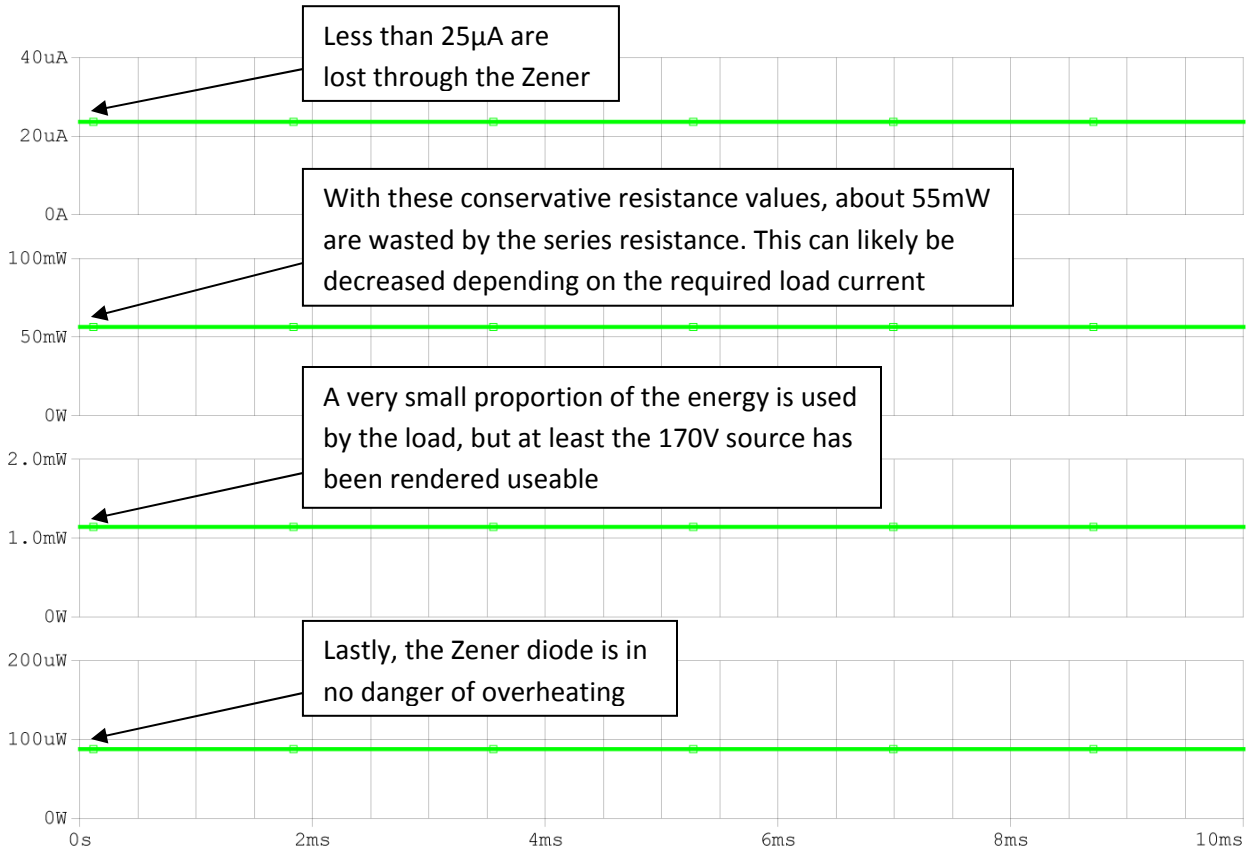


Figure 4-10: PSpice simulation results; current and power plots for Zener-based voltage converter configuration shown in Figure 4-8 schematic. Resistor and Zener values may need modification to save power and increase load voltage, but this step-down application appears to work.

The last three plots show the power consumption calculations for RS, RL, and X1. The power consumed by RS is very close to the source power of 56.5mW, since it experiences a large proportion of the 170V source. The load power consumption is shown to be around 1.1mW, which is around the 1mW nominal supply power of the micro-power 555 timer [44]. Lastly, the Zener power consumption is under 100µW, a value much less than the maximum of 500mW. Overall, the simulation provided assurance of the Zener regulator operation. Based on simulation and analysis, the team chose to use the Zener-based voltage regulator to deliver the necessary power to the 555 timer subcircuit.

After finding a viable way to power the 555 circuit, the team explored the possibility of using the MOC3023's TRIAC output as the power interrupt switch. The idea seemed plausible for initially shutting down the adapter, but it would be impossible to reactivate the adapter without breaching the isolation. Therefore, the team developed a way to disconnect the adapter while maintaining polling functionality.

Initially, the power cutoff circuitry for the adapter was designed as illustrated in Figure 4-11. When current is flowing through the output of the adapter, the current-sensing stage keeps the

MOC3023 active and the input current flowing regardless of the state of the polling stage. When the load device is unplugged and the current stops flowing, the current-sensing stage will shut off the TRIAC, deactivating the adapter. With the TRIAC deactivated, the only way for current to flow into the adapter is through the MOSFET in the lower branch, controlled by the polling circuit. The polling circuit now effectively has control over the entire adapter, which is desired while the adapter operates in standby.

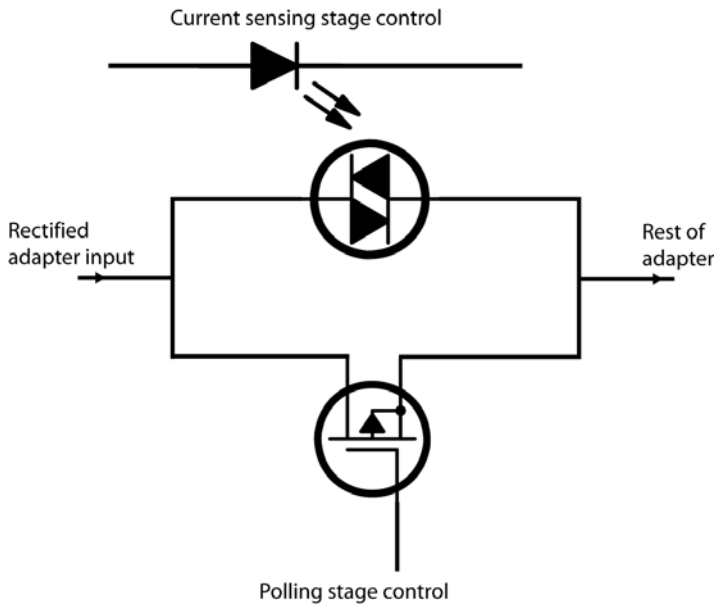


Figure 4-11: Branching the input path for dual controls would allow for the current-sensing circuitry to directly control the functionality of the adapter while the 555 can still reactivate it from the opposite side of the isolation barrier.

The schematic in Figure 4-12 shows the planned implementation for polling the adapter. The rectified AC input is connected to the top rail and AC ground. The Zener is chosen to have a 5V breakdown voltage. The resistor, on the other hand, takes on the remaining 165V. The 5V across the Zener is connected to the supply terminals of the 555 timer subcircuit, which includes resistors and capacitors, along with the actual IC. The subcircuit outputs a trigger voltage with a low duty cycle. The short time period when the 555 timer outputs a high voltage is set to be long enough to allow for the adapter's reactivation. The pulse drives a power MOSFET which intercepts the rectified AC line. When the MOSFET experiences a sufficient voltage drop across its gate and source terminals, the adapter is reactivated.

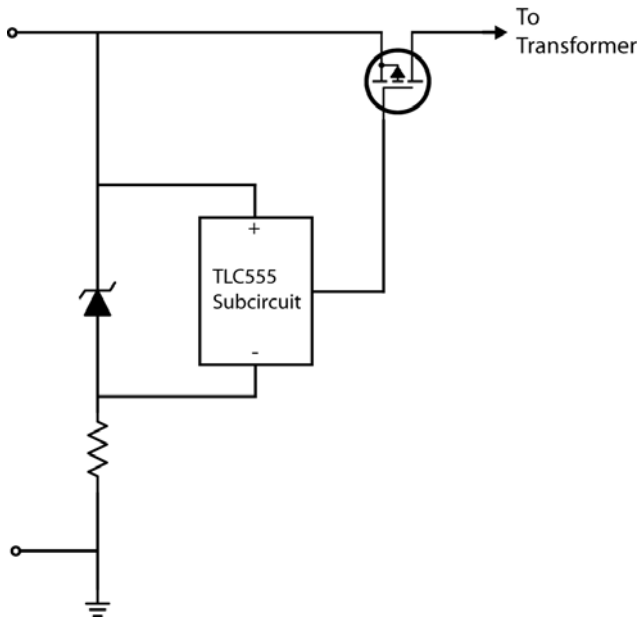


Figure 4-12: First top-level drawing of the adapter polling circuit layout. The TLC555 subcircuit periodically activates the P-Channel MOSFET, which impedes the top voltage rail from reaching the transformer's primary winding. The Zener-based voltage regulator supplies the TLC555 subcircuit with an appropriate voltage.

Although the team planned on using an N-Channel enhancement mode power MOSFET to deactivate and reactivate the adapter, the present configuration did not accommodate its implementation. Since the output of the 555 timer is 170V, the necessary voltage difference between the gate and source terminals of the MOSFET cannot be obtained. The high output of the 555 timer was measured at around 170V, and the low output was measured around 150V. Therefore, a P-Channel MOSFET was used instead. When the MOSFET was activated, the voltage at its drain terminal was measured to be 168V. In the case that the MOSFET was operating in the cutoff region, the voltage level at the drain drops to around 1mV. Both of these voltages show that the adapter would be activated and deactivated effectively.

Once the first two requirements were met for the cutoff circuitry, the polling requirement was met after the team decided the multivibrator operation of the 555 timer. At first, the astable operation of the 555 seemed to be the necessary implementation. However, an astable multivibrator continuously polls regardless of adapter operation. When the adapter is functioning normally with an output load, there is no need for the 555 timer to continue its polling behavior. Therefore, the team investigated the possibility of a monostable multivibrator configuration. The 555 timer's output could be set to low during stable mode, which is when the adapter is in normal operation. Then, using the

MOC3023 as an intermediary device, the 555 timer could be set to its polling operation during standby. In order to alert the 555 of a low-current condition, the MOC3023 could be placed to switch the voltage at the trigger pin of the timer to the 555 IC's ground, causing the output to transition from stable to polling. While the 555 timer is unstable, a resistor and capacitor combination dictate the delays between polling. While the output of the adapter has no load, the MOC3023 will repeatedly short the trigger pin of the 555 whenever the adapter is reactivated. Only when a load is connected will the 555 timer resume stable mode, and the adapter will consequently resume normal operation. The monostable operation of the 555 timer was chosen as the correct implementation to conserve energy while maintaining system functionality.

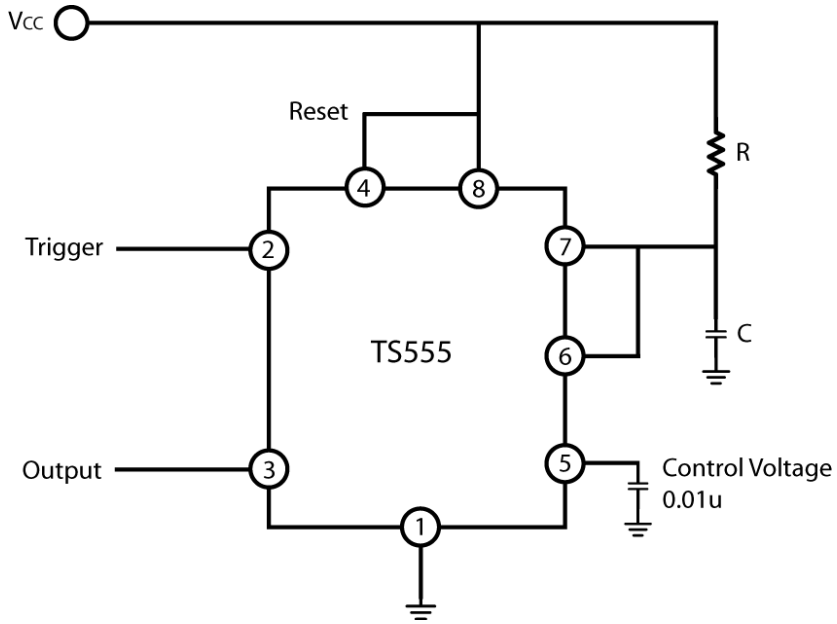


Figure 4-13: 555 timer configured for monostable operation; pulse time is determined by RC combination [44].

In lieu of the TS555 timer, the ICM7555 was chosen due to its lower cost as well as its lower power consumption. The resistor R and capacitor C were chosen in the monostable configuration shown in Figure 4-13 so the polling period would equal approximately a minute. Since higher-rated resistors are less expensive than higher-rated capacitors, a relatively large resistance value was chosen for R, and a medium-sized capacitance was selected for C. The team chose C to be 10µF, and R can be calculated. In the monostable configuration, the polling period can be expressed by the following equation [44]:

$$T_{POLLING} = 1.1RC \quad (4\text{-}9)$$

Therefore, in order to obtain a polling period of at least one minute, R must be greater than 5.45MΩ. A value of 5.6MΩ was chosen for R since it is a standard 5% resistor value.

Using the resistor and capacitor combination as well as the trigger pin of the 555 timer, the monostable multivibrator configuration is able obtain long polling periods while consuming a minimal amount of power.

Capacitive Polling Method *4.2.2*

Although the 555 timer-based polling circuit offers a low-power method of polling the adapter, it falls short of providing an overall power consumption of 0W. Therefore, the team designed an alternative polling method that exclusively utilized passive components. In order to create a circuit to perform this functionality, an energy storage device is required. The rate at which energy is stored and discharged from the device determines polling frequency of the adapter during standby. A large capacitor could serve as this energy storage device, providing long charging and discharging characteristics. Figure 4-14 shows the capacitive-polling design designed by the team in efforts to minimize standby power consumption.

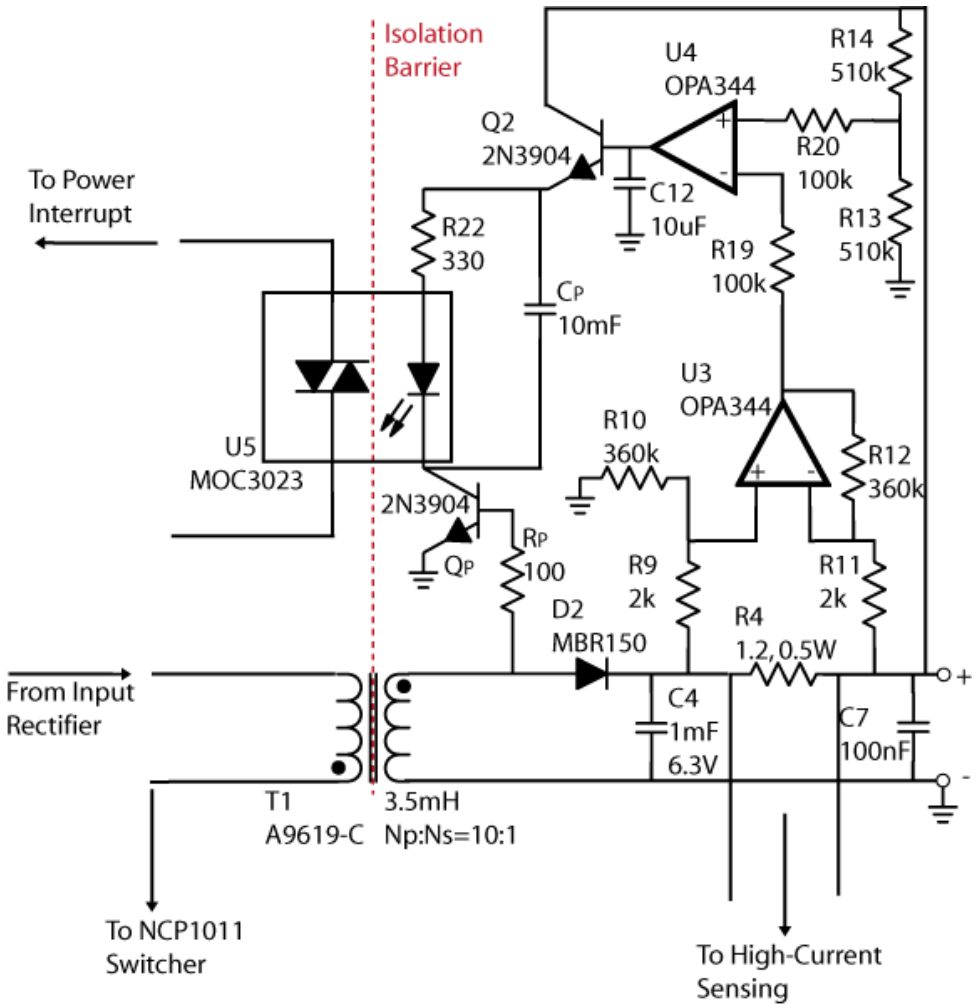


Figure 4-14: Final low-current sensing schematic with added polling capacitor CP. Capacitor will hold the low-current flag voltage, keeping the adapter deactivated until it discharges.

Polling capacitor C_P is placed in parallel with the MOC3023's internal LED and R22. When the current-sensing circuit detects a low level of current, it charges the capacitor and activates the LED, which in turn triggers the disconnect circuitry. Once power has been disconnected from the entire adapter, the capacitor begins to discharge through MOC3023's LED and R22. While C_P discharges its stored energy, the LED in the optoisolator remains active, keeping the adapter in a dormant state. When the capacitor discharges below a certain voltage, the LED is unable to emit light and the adapter is thereby reactivated via the TRIAC output of the MOC3023. The time period between adapter deactivation and reactivation is dependent on the length of the discharge cycle for capacitor C_P.

The low-current sensing in the capacitive-polling adapter uses the same implementation as the 555-timer-based adapter. However, the feedback circuitry from the 555 timer-based adapter has been

modified in the capacitive-polling design to include the capacitor C_P. In order to minimize the polling frequency of the adapter, the value of C_P must be very large. Therefore, the value chosen for C_P was 10mF. The 10mF capacitor provides the polling nature for the adapter in zero-load conditions.

When a load is connected to the adapter, the capacitor is discharged due to the low output state of the comparator. The LED in the MOC3023, meanwhile, remains deactivated. When the load is disconnected, the comparator switches to a high output state, activating the NPN switch to supply 5V to the capacitor and LED driver. The 10mF capacitor subsequently charges toward the 5V rail. Once the voltage reaches around 3V, which is the sum of the voltage drops across the LED and series resistance, the LED is activated. The reactivation circuitry is then signaled to switch the AC input off. At this point, the power connection is removed from the DC portion of the adapter, causing all active devices to turn off. In particular, the NPN switch located at the cathode of the MOC3023 LED is turned off, effectively blocking the 10mF capacitor and LED from the DC ground.

The capacitor, LED, and resistance remain in their own circuit loop, causing the capacitor to discharge its stored energy through the LED and the resistance. The LED remains activated until capacitor C_P discharges to approximately 2.8V. At this value, the forward bias voltage drop across the LED forces the current to drop below the holding current, turning the device off. However, the delay caused by the 10mF capacitor allows the system to poll for a load connection before periodically reactivating itself.

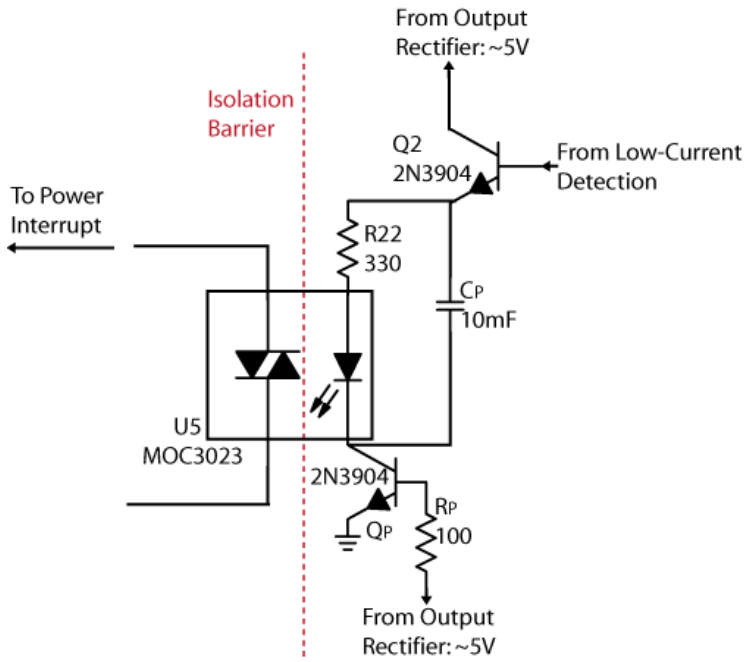


Figure 4-15: Polling capacitor implementation; transistor QP prevents the capacitor from discharging through ground, allowing it to stay charged for longer, thereby increasing the time between polls.

The circuit loop comprised of capacitor C_P, resistor R22, and the MOC3023's LED is disconnected from both supply rails when the TRIAC output of the optoisolator is activated. Subsequently, the capacitor dissipates its energy through the resistor and the LED in this first-order system. The value of the capacitor was obtained using the first order time constant relationship between the resistance and capacitance:

$$\tau = RC \tag{4-10}$$

For a first order system, this constant represents the time needed for the voltage to drop to 37% above its final value. In this circuit, the LED will be deactivated after one time constant due to the forward bias voltage drop. Therefore, the capacitance needed for the adapter to be off for 10s is calculated:

$$10 = 330C \rightarrow C = 30.3mF \tag{4-11}$$

According to (4-10), a capacitor of 30.3mF is needed for the desired polling period. However, a capacitor of that value is very expensive and relatively large compared to other devices in the adapter. The team decided to use a 10mF capacitor, as its physical size was not too hindering. Plugging this value into (4-8) resulted in a much smaller polling period:

$$\tau = RC = 330 \times 10m = 3.3s \tag{4-12}$$

Although it is only one-third of the desired value, the 3.3s period should still be long enough to effectively poll the adapter.

After designing the capacitive-polling adapter's DC circuitry, focus was shifted to implementing the power cutoff subcircuit. Although the TRIAC was originally chosen to perform as the power interrupt for the adapter, the team was unable to use the MOC3023's output to deactivate the adapter. Since the MOC3023 remains on while the adapter is supposedly deactivated, the TRIAC output cannot be used to interrupt power to the transformer. The cutoff circuitry called for an inverting implementation that deactivated the adapter while the MOC3023 was active. Therefore, a P-Channel enhancement mode MOSFET was used to implement this inverting functionality and power disconnect [51]. Figure 4-16 shows the power cutoff circuitry used in the capacitive-polling adapter.

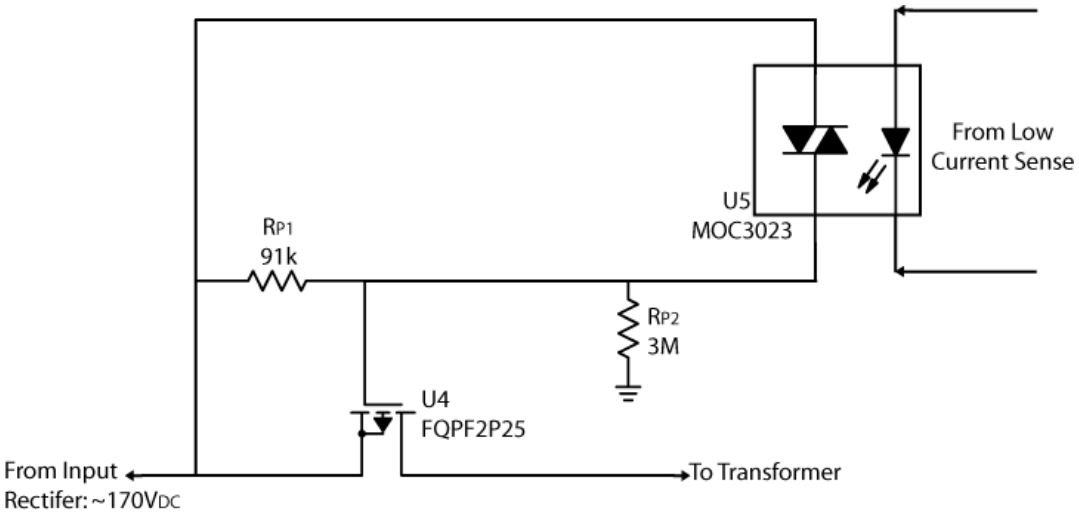


Figure 4-16: Adapter cutoff schematic; disconnection circuitry was redesigned to allow an active TRIAC to disable the adapter, which is opposite to its foreseen function. Resistive voltage divider keeps MOSFET's gate-source voltage from exceeding component limits, while simultaneously keeping TRIAC current below active holding level [51].

The adapter cutoff was designed to break the rectified 170V input line when low current is detected at the output, and to connect the input to the transformer when a sufficient value of current is detected at the DC load. If the MOC3023 is activated, the 170V line is connected directly to the P-Channel MOSFET gate via its TRIAC output. In effect, the voltage drop from the source of the MOSFET to its gate is 0V. The MOSFET operates in cutoff mode under this condition, and no current flows from source to drain. However, if the MOC3023 is deactivated, a voltage division occurs at the gate between 170V and ground. The ratio of the resistances was chosen such that approximately 165V is experienced

at the MOSFET gate. With a 5V difference between the source and gate of the MOSFET, the 170V line is connected to the transformer, resuming adapter functionality.

Once the power cutoff circuitry was developed, the capacitive-polling adapter design was completed. The layout of the capacitive-polling method meets the requirement specified for the power cutoff circuitry and adapter reactivation. Although a TRIAC was not used as the actual power interrupt switch, the MOC3023's output was used to trigger a power MOSFET to activate and reactivate the adapter, which satisfied the circuit's first two requirements. The third requirement was achieved using a large capacitor to poll the adapter periodically. In order to determine which polling adapter consumes less power during standby and operates more efficiently, a series of tests was completed on both adapters. The results of these tests allowed the team to choose the appropriate design for an efficient wall adapter.

Results 5

In the previous chapter, the team designed two separate adapter models that utilize polling during standby mode. In order to definitively determine which model consumes the least amount of energy while maintaining adapter functionality, a variety of tests were conducted on each design. The two designs each contain their own advantages and drawbacks. While the capacitive-polling adapter uses passive devices exclusively in its layout, the polling period of the adapter during standby is limited by the time constant determined by the polling capacitance and the series resistance. On the other hand, the 555 timer-based polling adapter can be programmed for a long polling period, but constantly consumes power regardless of the output load condition. However, the desired outcome of the following measurements is to determine at least one configuration that will reduce the original adapter's standby power consumption by 75%, as specified in Chapter 1 of this report.

Capacitive Polling 5.1

The capacitive-polling adapter configuration was tested prior to the 555 timer-based polling adapter because it would have been the ideal choice had it performed up to the project's specification goals. The team believed that the design would only meet specifications if the polling period was lengthened as much as possible. Efforts were made in designing the capacitive-polling adapter to maximize the polling period by disconnecting the supply rails during polling as well as increasing the polling capacitance value. However, the MOC3023's LED and the neighboring series resistance could not be altered without sacrificing system functionality.

In order to test the polling period of the configuration, the TRIAC output of the MOC3023 was placed in series with a typical 2V, 10mA LED. The series arrangement was placed in parallel with a DC power source set to 2V. Figure 5-1 shows the test setup used to determine the polling frequency of the capacitive-polling adapter.

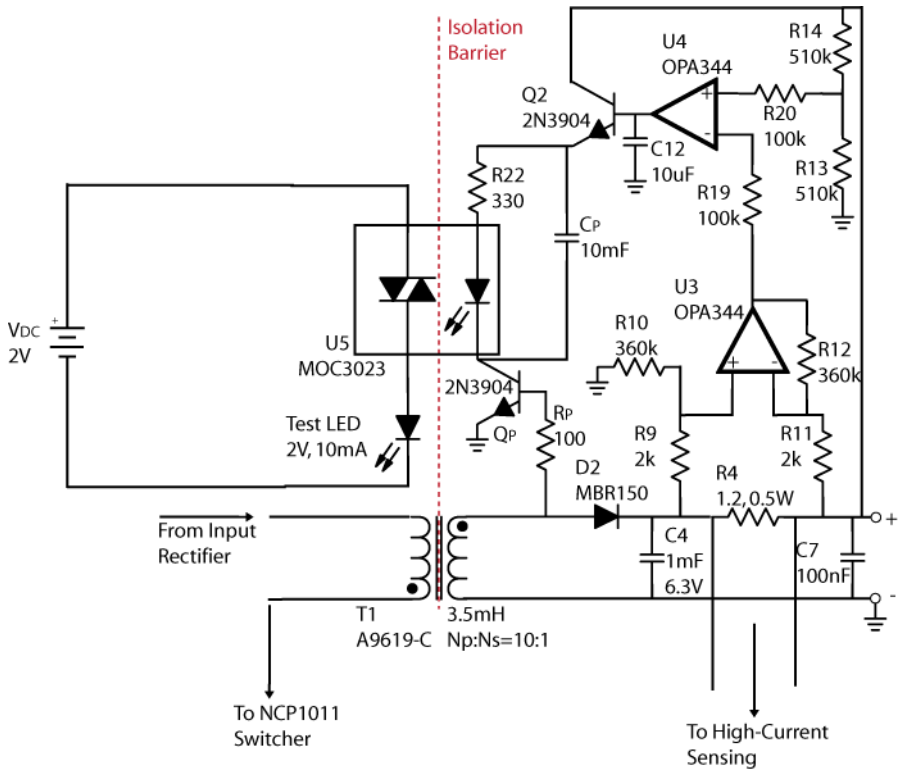


Figure 5-1: Initial test setup of capacitive-polling adapter using an external DC source and test LED.

To emulate the power cutoff circuitry deactivating the adapter when the low-current flag was raised at the output, the AC input was manually disconnected from the adapter once the LED was observed to be emitting light. Subsequently, the polling period was recorded as the duration the test LED emitted light before becoming inactive. The full test procedure is shown in Table 5-1.

Table 5-1: Initial procedure followed to record polling period of capacitive-polling adapter.

Step	Description
1	Place a resistive load to adapter output between 100Ω and 300Ω.
2	Connect adapter input to AC power source via wall outlet.
3	Remove resistive load from output while adapter is activated.
4	Simultaneous to output disconnect, unplug adapter input from wall outlet.
5	Record the amount of time the test LED remains active.

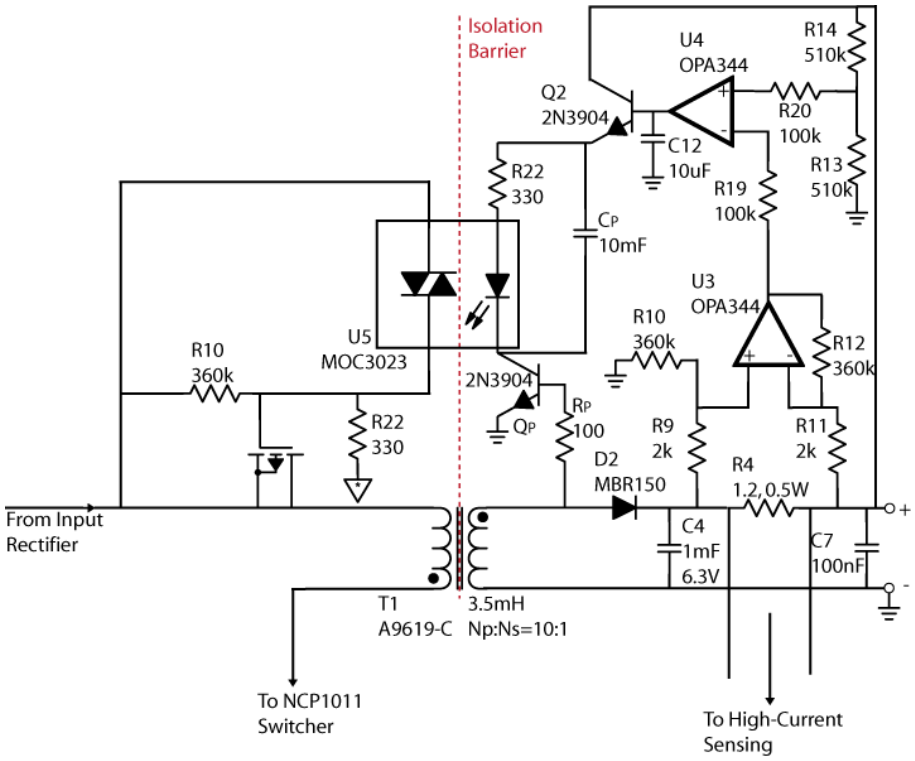


Figure 5-2: Capacitive polling solution schematic; 10mF capacitor charges when low-current alert is activated, and holds the TRIAC's LED on (and thereby the adapter off) until it discharges.

The results of initial tests yielded a polling period approximately equal to the value calculated in Chapter 4. When the adapter was connected to AC power with no output load, the test LED remained active for a time of 3s to 4s, which encompasses the theoretical value of 3.3s. However, this test was performed using an incomplete adapter model. The test LED emulates the time period during which the power cutoff circuitry will deactivate the adapter, but may not represent the actual time period. In addition, the manual disconnect of the AC input power is not a true representation of power cutoff functionality. Therefore, the remaining circuitry was integrated into the adapter so a test of the full configuration could be conducted.

Figure 5-2 shows the final configuration of the capacitive polling solution used in testing. After integrating the power cutoff subcircuit into the adapter, the team connected the input to the AC power source and once again observed the polling period with no load at the output. Since the TRIAC output of the MOC3023 was now connected to the power cutoff circuitry, an oscilloscope was used to visually measure the polling period. One of the scope probes was connected across the capacitor voltage so the polling period could be observed.

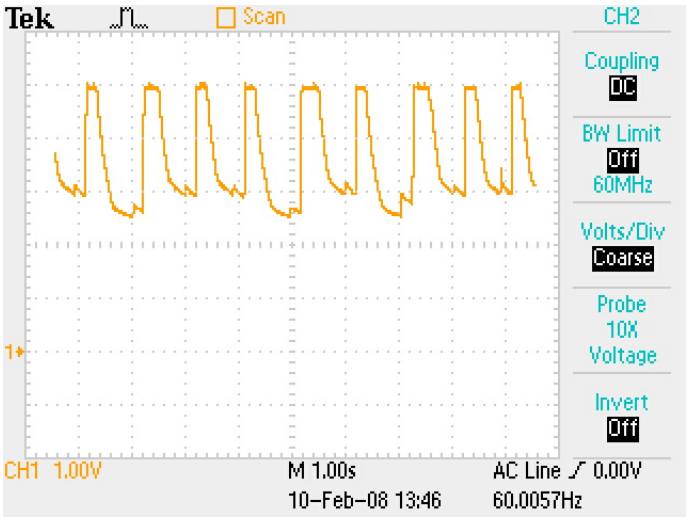


Figure 5-3: Oscilloscope capture of output voltage for capacitive-based polling timer configuration. The polling period was limited to around 1s.

The results of the full configuration test can be seen in Figure 5-3. Unlike results from the initial test with the LED and DC power source, the polling period of the full configuration was observed to be a mere 1s. The reason a dramatically-shortened polling period was observed is due to the speed at which the low-current sense alerts the power cutoff circuitry of a no-load condition. In the first test of the capacitive-polling adapter, the capacitor was allowed to discharge its energy well after the MOC3023 began to deactivate. Since the propagation delay of low-current sense processing is small with respect to the time constant of the polling capacitor's voltage characteristic, capacitor C_P is only able to discharge to a 2.5V potential in the actual adapter model. Once the low-current sense alerts the power cutoff circuitry of the insufficient amount of output current, power is disconnected from the DC side of the adapter and C_P begins to discharge. Therefore, the polling period is limited by the propagation delay of the low-current sense subcircuit. The limitation of the polling period forced the team to deem the capacitive polling adapter as an unusable design for this project since the design would not be able to reduce standby power consumption by 75%.

555 Timer Polling 5.2

After the capacitive-polling adapter was ruled out as a potential design implementation, the team focused its efforts on manipulating the 555 timer-based polling adapter to meet project specifications. Figure 5-4 shows the fully-integrated adapter with low-current sensing and polling stages.

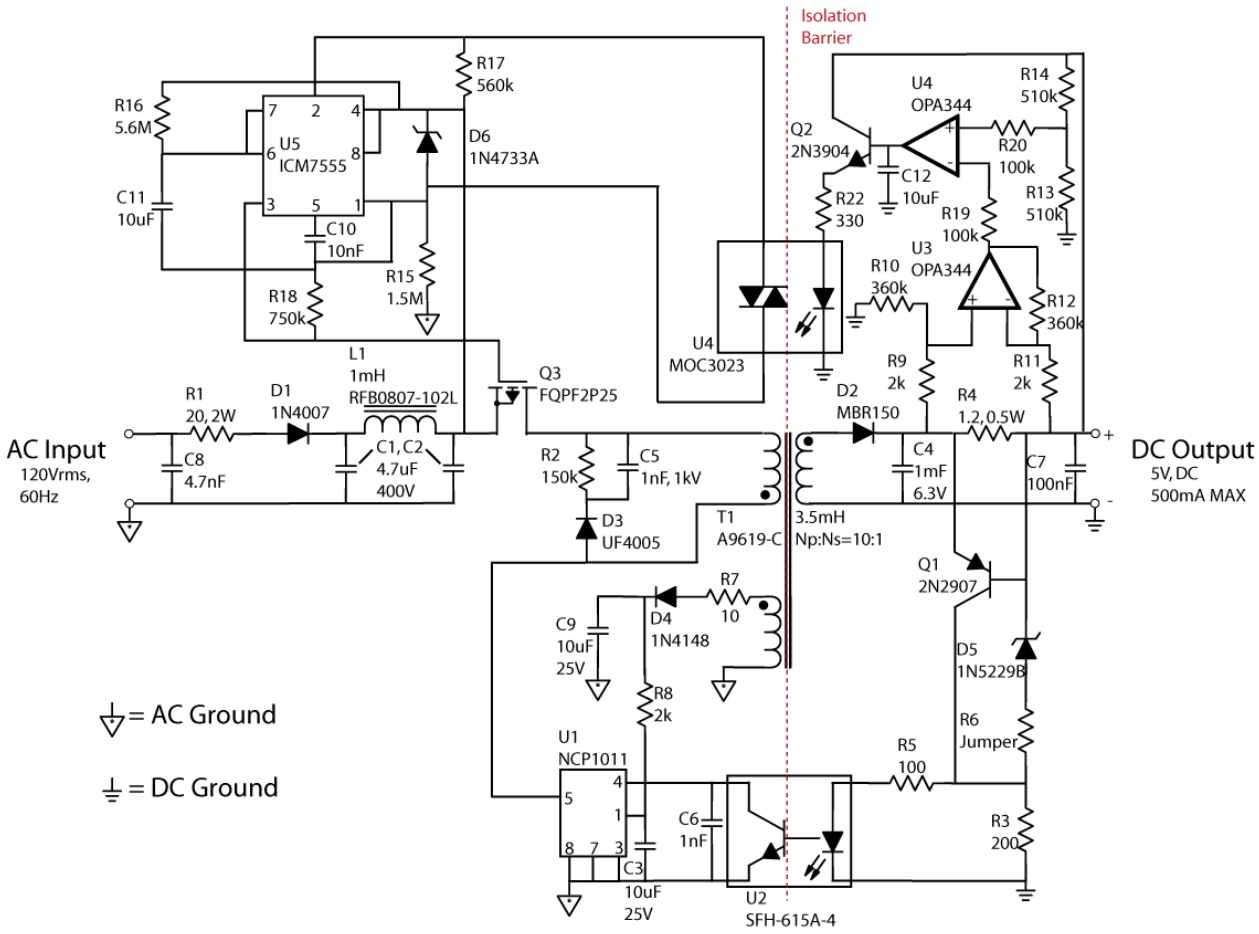


Figure 5-4: Final schematic; adapter with monostable multivibrator timing.

In Chapter 4, it was determined that the 555 timer would be configured for monostable operation to consume the least amount of power during both operating and standby conditions. The large values of capacitor C11 and resistor R16 allows the polling period of the adapter to equal approximately 60s according to calculations made in Chapter 4. In order for the 555 timer-based polling adapter design to remain a practical solution, the polling period must first be verified according to this calculation.

Originally, the team planned to use the pinhole array on the upper portion of the first PCB board to implement possible solutions. However, to allow for easy manipulation and substitution of additional circuitry, breadboards were used to implement the low-current sense as well as the polling circuitry. Wire connections were attached to specific nodes of the test bed and then connected to the appropriate nodes on the breadboard implementations. Figure 5-5 shows the additional wires connected to the original adapter test bed in order to implement the low-current sensing and polling circuitry. Figure 5-6 shows the entire implementation of the 555 timer-based polling adapter on the PCB and two breadboards collectively.

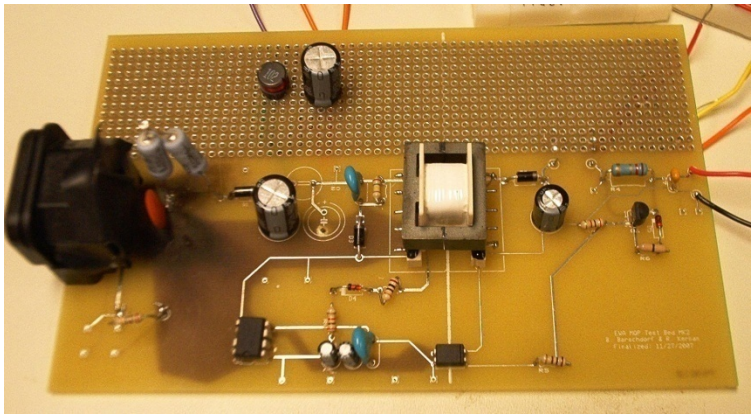


Figure 5-5: Shown is a close-up view of the adapter test bed configuration used for 555 timer-based polling adapter tests. The red and black wires on the right are attached to the DC output and the orange and yellow wires above the DC output are connected across the current-sensing resistor R4. In addition, two more wires were connected across output filter capacitor C4 to provide a 5V supply for low-current sense circuitry. The purple and leftmost orange wires were attached to the $170V_{DC}$ rail and AC ground respectively to provide power for the 555 timer subcircuit. The rightmost wire provided the drain of the p-channel power MOSFET with a connection to the primary winding of the transformer.

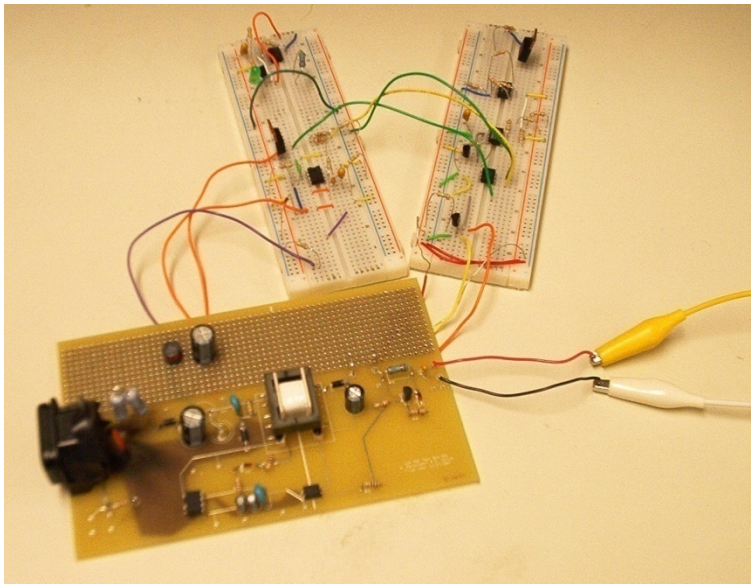


Figure 5-6: Shown is the interconnections between the original adapter test bed and the additional low-current sensing and polling circuitry. The right-hand breadboard in the figure holds all circuitry for the low-current sense, while the left-hand breadboard holds the 555 timer polling subcircuit. The green and yellow wires provide the feedback connection between the TRIAC output of the MOC3023 and the 555 timer. The white and yellow alligator clips were use to connect DC output to a resistive load. Moreover, oscilloscope probes were connected to the alligator clips to measure the DC output voltage during testing.

Once the physical arrangement depicted in Figure 5-6 represented the adapter schematic shown in Figure 5-4, the 555 timer-based polling adapter was ready for testing. The first test conducted on the adapter was a measurement of the polling period. It was necessary to verify the functionality of the 555 timer's polling of the adapter before power consumption measurements were undertaken. After plugging in the adapter, the team attached an oscilloscope probe to its DC output. Figure 5-7 shows the output waveform of the adapter with no load connected.

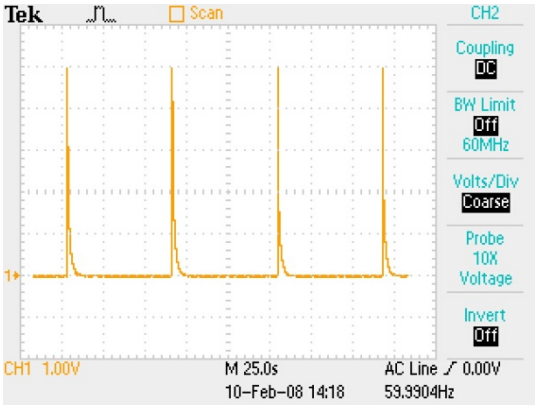


Figure 5-7: Output waveform of adapter; 555 Timer polling intervals are shown to be around 62s.

Using the time cursors of the oscilloscope, the observed polling period was measured to be 62s. In addition to polling the adapter according to previous calculations, the output voltage reached the nominal 5V rating. Therefore, the adapter polls according to specifications and is able to resume normal operation once it is reactivated with a load connected.

After the functionality of the 555 timer's polling of the adapter was confirmed, the team moved on to testing the power consumption of the system. While the output power consumption is simple to measure, the input power consumption is more difficult. Chapter 2 describes the process of measuring the input power measurement via a series resistance in the return path of the adapter input. In the same manner, a sensing resistance of 10Ω is placed as shown in Figure 5-8. Scope A is used to measure the input AC voltage, while Scope B is placed across resistor R_{SENSE} to measure the experienced voltage drop. The input current can be determined by attenuating the signal observed on Scope B by 10, since the voltage drop is ten times the current flowing through R_{SENSE}.

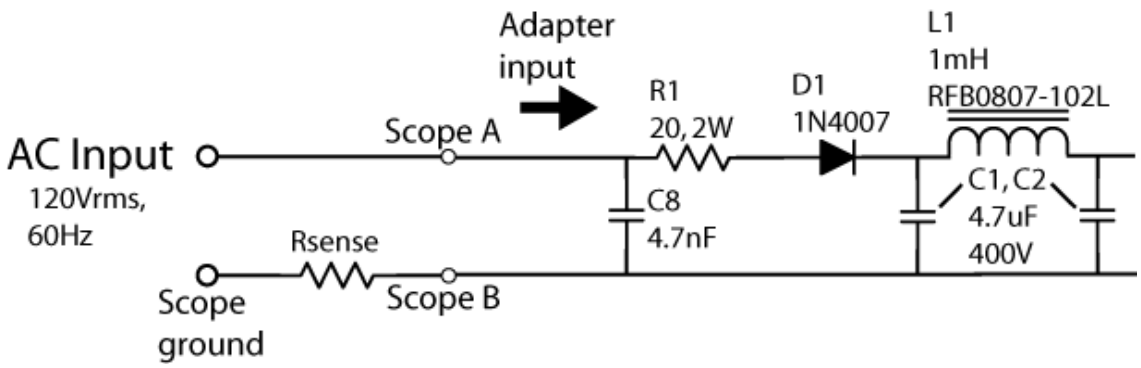


Figure 5-8: Power measurement setup; input voltage measured by Scope B, input current related to voltage on Scope B.

Once two oscilloscope probes were arranged according to the layout shown in Figure 5-8, the adapter was plugged in so the team could observed the resulting waveforms. Figure 5-9 shows a standard $120V_{RMS}$ voltage reading on channel 2 of the oscilloscope, but channel 1 shows the input current coupled with noise from the AC line. It was determined in Chapter 2 that this noise is due to the three-phase to single-phase power conversion carried out before power is delivered to the consumer. In previous input power consumption measurements, R_{SENSE} was increased to 100Ω to attenuate the noise and the MATH function of the oscilloscope was used to produce a 100X power signal. However, the team discovered a more precise way of measuring the input power to the adapter.

While R_{SENSE} is maintained at 10Ω, the adapter is connected to the wall outlet via a surge protector. When the surge protector is switched to the off position, the oscilloscope observes the waveforms shown in Figure 5-10. Although the input voltage is completely disconnected from the adapter's input, the noise on the AC line is still observed across resistor R_{SENSE}. Using the SAVE option on the oscilloscope, the noise was converted into a series of voltages over time and stored as a CSV file.

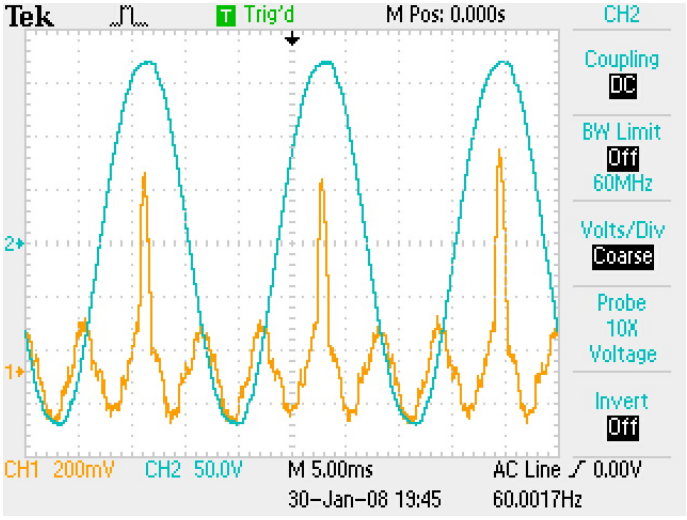


Figure 5-9: Input voltage (CH2) and amplified Input Current (CH1) waveforms of initial 555 timer-based polling adapter with 200Ω load.

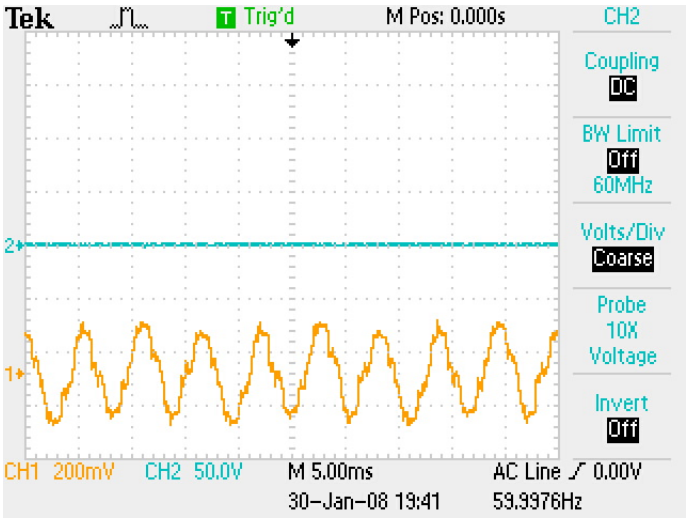


Figure 5-10: Noise observed on CH1 when surge protector is switched to off position. The noise is attributed to three-phase to single-phase power conversion.

After subsequently switching the surge protector to the on position, the oscilloscope reading shown in Figure 5-11 was observed during the adapter's polling period. Although the input current signals from Figure 5-10 and Figure 5-11 appear to be identical, the input current peaks that occur whenever the input voltage swings to its peaks are slightly higher when the adapter is active. However, the slight difference between the two oscilloscope plots implies that the power consumption of the 555 timer subcircuit is very small with respect to the overall test bed's power consumption.

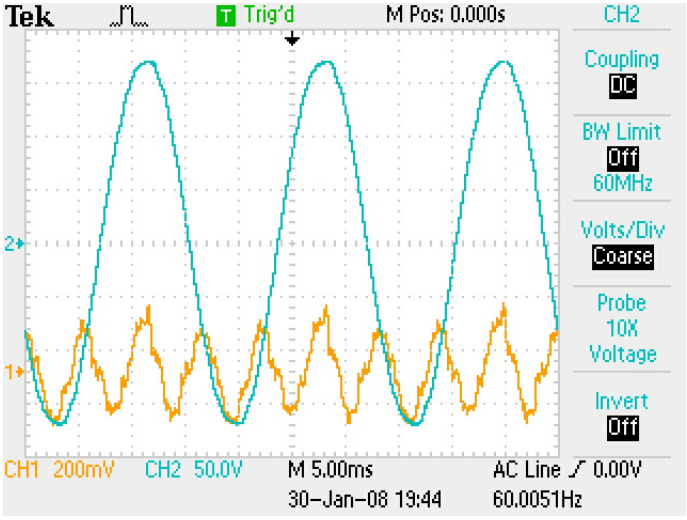


Figure 5-11: Input voltage (CH2) and amplified Input Current (CH1) waveforms of initial 555 timer-based polling adapter during standby (no load).

When the adapter's output is coupled with a resistive load, a much different input current is observed. Figure 5-9 shows an oscilloscope reading of the input voltage and current when a 200Ω output load is connected to the adapter.

Although the current peaks are much higher while the output is coupled with a load, the observed noise inherent in the signal remains the same. Therefore, if the noise is subtracted from the input current signal, an accurate measurement of the current can be obtained. In efforts to eliminate the noise, the voltages from the waveforms captured in Figure 5-11 and Figure 5-9 were saved as CSV files. For each input current measurement, the data from the noise captured in Figure 5-10 was subtracted, resulting in data truly representative of the input current. Finally, the data field for each input current measurement was divided by the measured resistance of R_{SENSE} to attenuate the data to the actual current level. Figure 5-12 shows the data transformation of the input current.

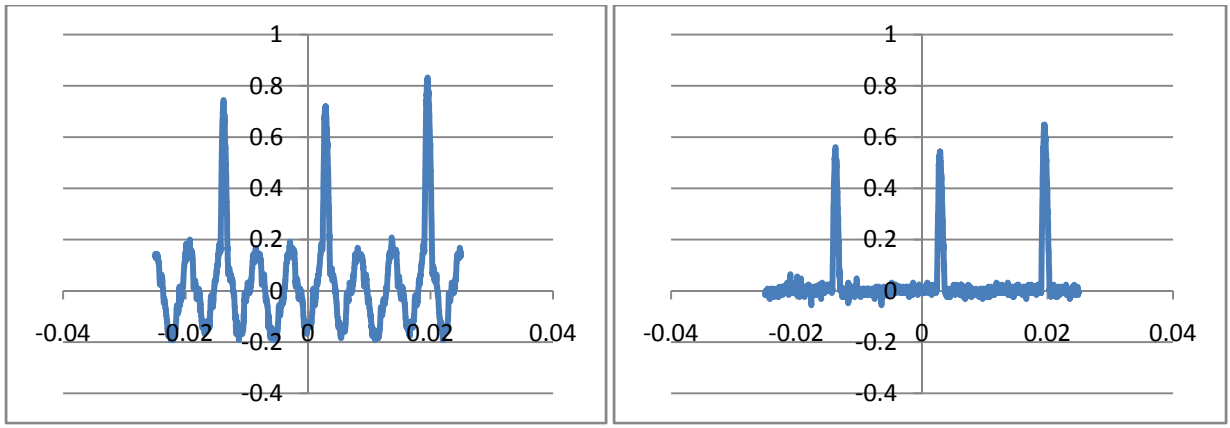


Figure 5-12: Noisy current measurement (left) and true current measurement with noise subtracted (right).

While the left-hand plot shows the presence of the AC line noise, the right-hand plot shows a filtered signal that is representative of the actual current supplied to the adapter. Using this technique, power measurements were obtained by multiplying the RMS value of the actual current data by the RMS voltage.

Table 5-2 shows the results of input power measurements for the 555 timer-based polling adapter and the original adapter with an output load of 200Ω.

Table 5-2: Input power measurements of the modified and original adapter with 200Ω load.

Consumed Power During Normal Operation (200Ω load)	
Unmodified Power Adapter	Modified Power Adapter
447 mW	461 mW

Although the additional circuitry consumes an extra 3% of the original adapter's overall power consumption when active, the difference between the power consumption of the original adapter and the modified adapter is negligible during charging. Moreover, since adapters operate in standby more than they operate in charging mode, the small increase in power consumption experienced by the 555 timer-based polling adapter over the original design is a nonissue.

In the same way, standby power consumption was tested by disconnecting the 200Ω load from the adapter and reacquiring data from the oscilloscope. Table 5-3 shows the results of standby power consumption measurements for both the original and modified adapters after the data was manipulated to represent actual values.

Table 5-3: Input power measurements of the modified and original adapter with no load.

Consumed Power During Idle Operation (No Load)	
Unmodified Power Adapter	The Modified Power Adapter
224 mW	34 mW (momentary 263 mW spikes)

While the original test bed was measured to consume 201mW standby power, the PCB implementation was measured to consume 224mW during no-load conditions. The discrepancy in power values can be credited to either the deviation of component values or the increased precision of measurement used in the new calculations. Nevertheless, the results showed a substantial savings of 85% less power consumption with the modified adapter implemented, exceeding the specification goal of a 75% reduction. Figure 5-13 shows a simulated plot of the modified adapter's power consumption and the unmodified adapter's power consumption over a period of 250 seconds. The adapters both start at 0s, supplying a 200Ω load which is disconnected after 50 seconds. The shaded areas indicate energy savings, which will only continue to accumulate for as long as the adapter is in the idle state.

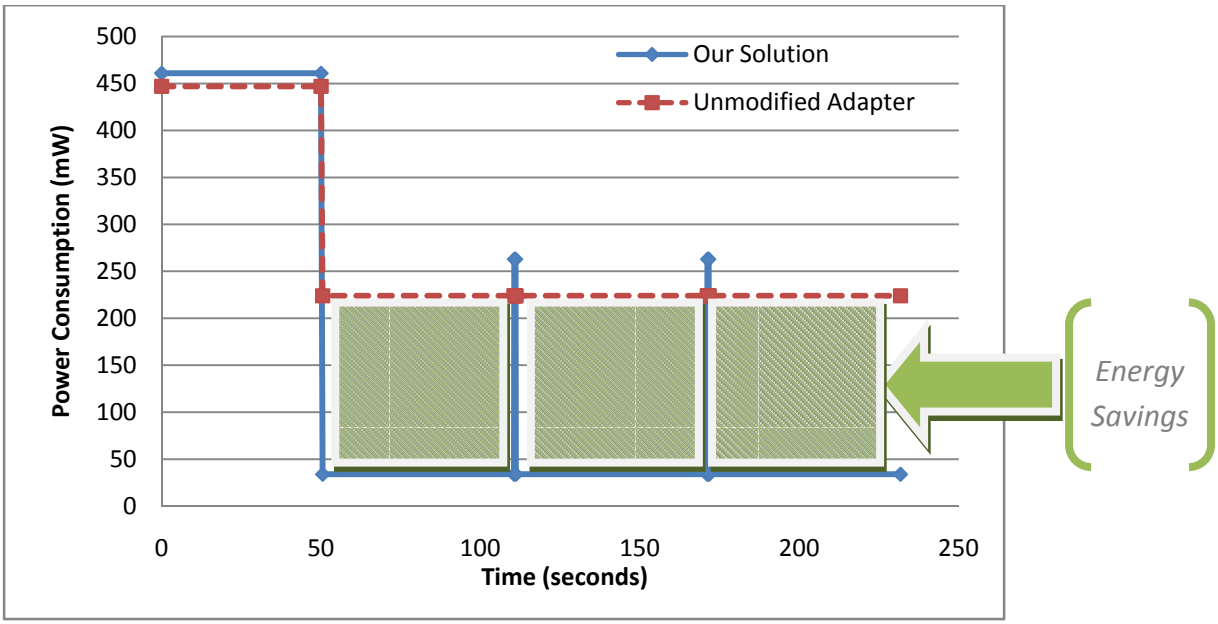


Figure 5-13: Power consumption comparison of modified adapter and original test bed over time. Load is disconnected after 50 seconds.

Figure 5-14 shows the adapter's power usage as a function of the amount of resistance used for a load. To collect the necessary data, 16 resistor values in the range of 100Ω to 1.5kΩ were each connected to the output load and the output power was measured for both the original and modified adapter implementations. The resulting plot of the measured data provides an alternative visual representation for seeing the effect of the modified solution on standby power consumption. It should be noted that the shaded area representing energy savings extends toward an infinite resistance, creating a large window in which the modified adapter consumes a much smaller amount of power than the original adapter test bed.

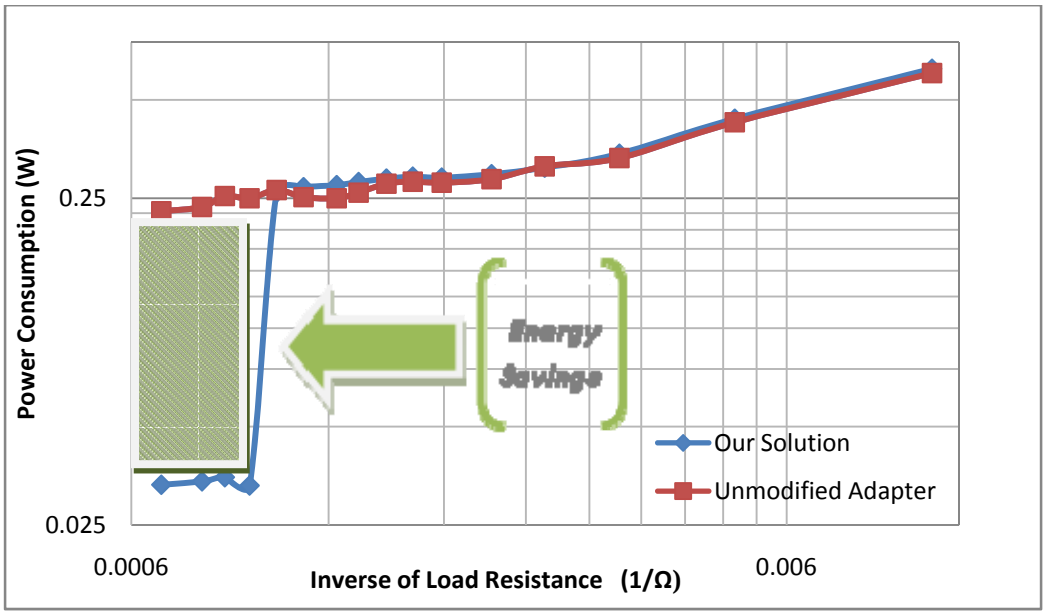


Figure 5-14: Plot of power consumption for both the modified and the unmodified adapter versus the inverse of the attached load resistance.

The measurements of standby power consumption for the modified adapter provided the team assurance that the 555 timer-based adapter has viability. However, one specification goal remained to be accomplished in the design. Since the tested 555 timer-based adapter model utilized operational amplifiers and power MOSFETs whose individual costs exceeded the project's budget, the team researched for potential alternatives to substitute into the design. In Chapter 4, the team describes how a dual-channel op-amp IC called the TLC27L2 was used to replace the two OPA344 op-amps used in the low-current sensing circuitry, and how the FQPF2P25 p-channel power MOSFET was purchased to replace the IRF9640. Originally, the team believed that the specifications for the substituted components were similar to the original parts used in the design. While the FQPF2P25 power MOSFET was successfully implemented in the design, the incorporation of the TLC27L2 disrupted system functionality. Figure 5-15 shows the PCB layout of the 555 timer-based polling adapter using the TLC27L2 and the FQPF2P25 power MOSFET.

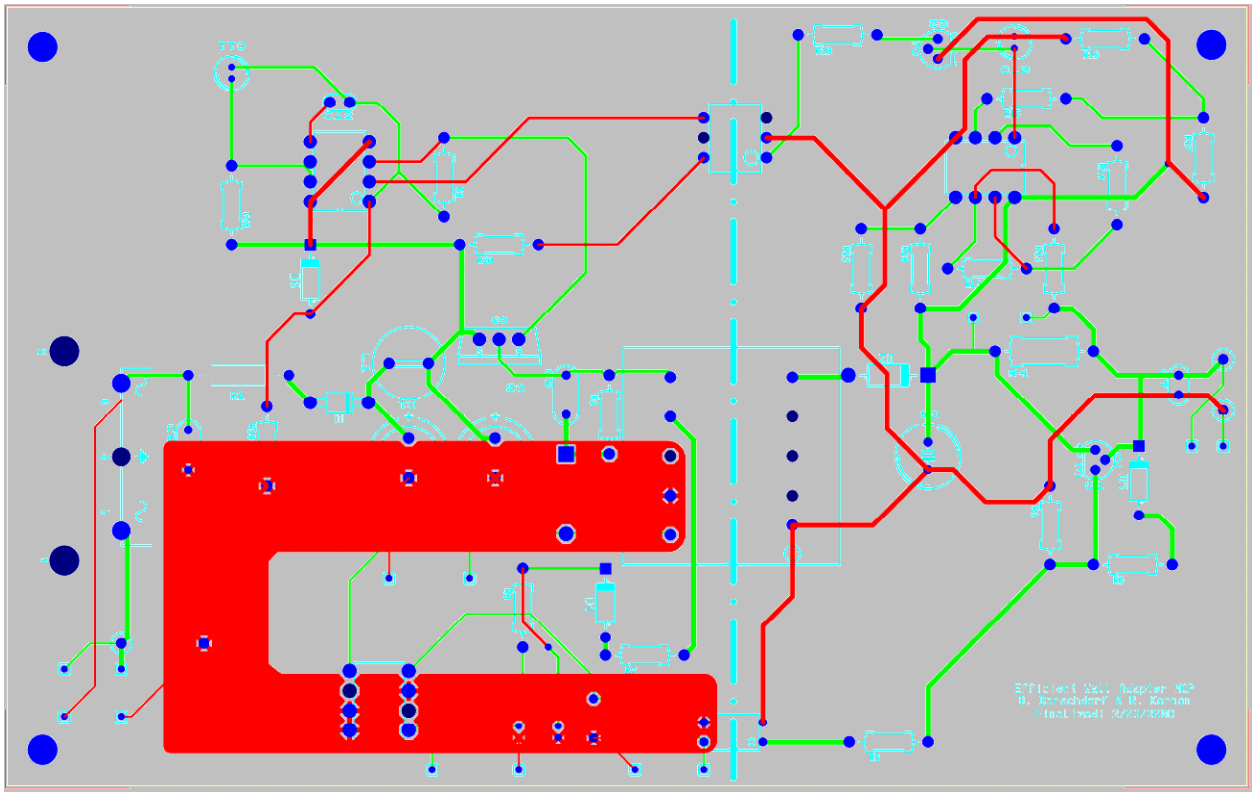


Figure 5-15: PCB layout of the 555 timer-based polling adapter. Original test bed circuitry is located on the lower half of the PCB while additional circuitry such as the low-current sense and the 555 timer subcircuit are located on the upper half of the board.

After troubleshooting the circuit, the team reexamined the datasheet specifications for the TLC27L2. It was determined that although the TLC27L2 consumes much less power (135µW) than two OPA344 ICs, the input and output voltage ranges of each op-amp are much less. The output voltage range is stipulated to be between 50mV and 4.1V given a supply of 5V. The common mode input range, on the other hand, is between -0.2V and 4.2V when the TLC27L2 is operating at 5V. While the shortened output voltage range does not affect system functionality, the introduced limitation of the common mode input range provides a hindrance for the low-current sensing operation. Since both voltages connected to the inputs of the difference amplifier arrangement are within only a few mV of the supply rail, the TLC27L2 was not able to appropriately interpret the voltages outside its input range. After manipulating the resistors in the low-current sensing circuit, a functional adapter was realized according to the schematic shown in Figure 5-16. The team reasoned that lowering the reference voltage and reducing the amplification of the difference amplifier would help the system regain its normal operation.

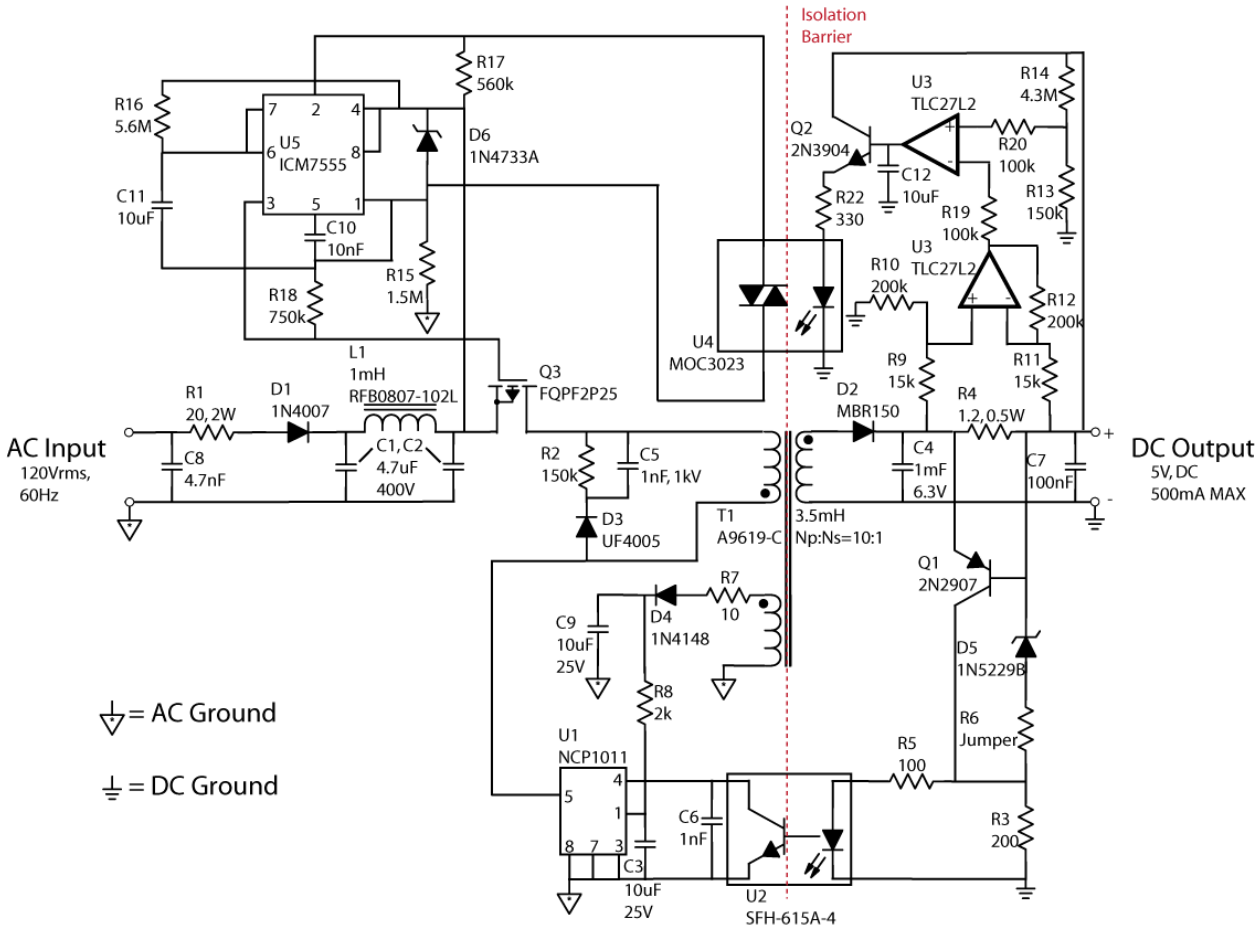


Figure 5-16: Final schematic; adapter with monostable multivibrator timing.

In order to return the proper functionality to the adapter, the values of resistors R9, R10, R11, and R12 from the difference amplifier as well as resistors R13 and R14 of the voltage divider were altered. The voltage reference was reduced to 169mV by setting R14 equal to 4.3MΩ and R13 equal to 150kΩ. In addition, the amplification of the input voltage of the difference amplifier was reduced to 13.3 by substituting a resistance of 200kΩ for R10 and R12 and placing resistances of 15kΩ for R9 and R11. In effect, the newly-established threshold current was calculated by the following equation:

$$I_T = \frac{(V_{REF})}{(A_{DIFF})(R4)} = \frac{169mV}{(13.3)(1.2\Omega)} = 10.5mA \qquad (5\text{-}1)$$

Therefore, the new implementation of the low-current sensing signals the 555 timer of a standby condition when the output current drops below 10.5mA. In addition to changing the output threshold current, the reduced amplification factor of the difference amplifier shortens the linear range of its output voltages. Besides these changes, however, the adapter operates in the same manner as it did using the OPA344 and the IRF9640.

Although adapter functionality was restored, the team pursued alternatives for a dual-channel op-amp that had a rail-to-rail input and output voltage range. The LMV932 dual-channel operational amplifier manufactured by Texas Instruments provides a rail-to-rail input and output voltage range and costs only a few cents more than the TLC27L2 [52]. The LMV932's common mode input voltage range is between -0.2V and 5.3V and the output voltage can range between 0.12V and 4.89V when operated at 5V. Although the LMV932 consumes more power than the TLC27L2, the power consumption is still less per amplifier than one OPA344 [52]. In fact, each amplifier's supply current of the LMV932 is 34µA less than the OPA344's supply current of 150µA. Since it matches the specifications of two OPA344 op-amps and costs only $0.04 per 1000 units more than the TLC27L2, the LMV932 dual-channel operational amplifier was chosen for implementation in the efficient wall adapter design. The implementation of the LMV932 IC allowed the team to revert all other components in the design back to their original values while remaining under budget. Once the team obtained a cost-effective solution to the OPA344, the final design met all specification goals laid out for the project. The final schematic of the 555 timer-based polling timer can be found in Appendix A.

Future Work 6

The efficient wall adapter designed in this project significantly reduces power consumption compared to present-day models. However, the team acknowledges that the design presented in this report does not represent an ideal solution. In fact, it may be that additional research into different adapter reactivation methods would yield a more efficient product. The purpose of this chapter is to provide a framework that could be used in further, related research. In Figure 6-1, the basic adapter functionality is shown and described on a high level.

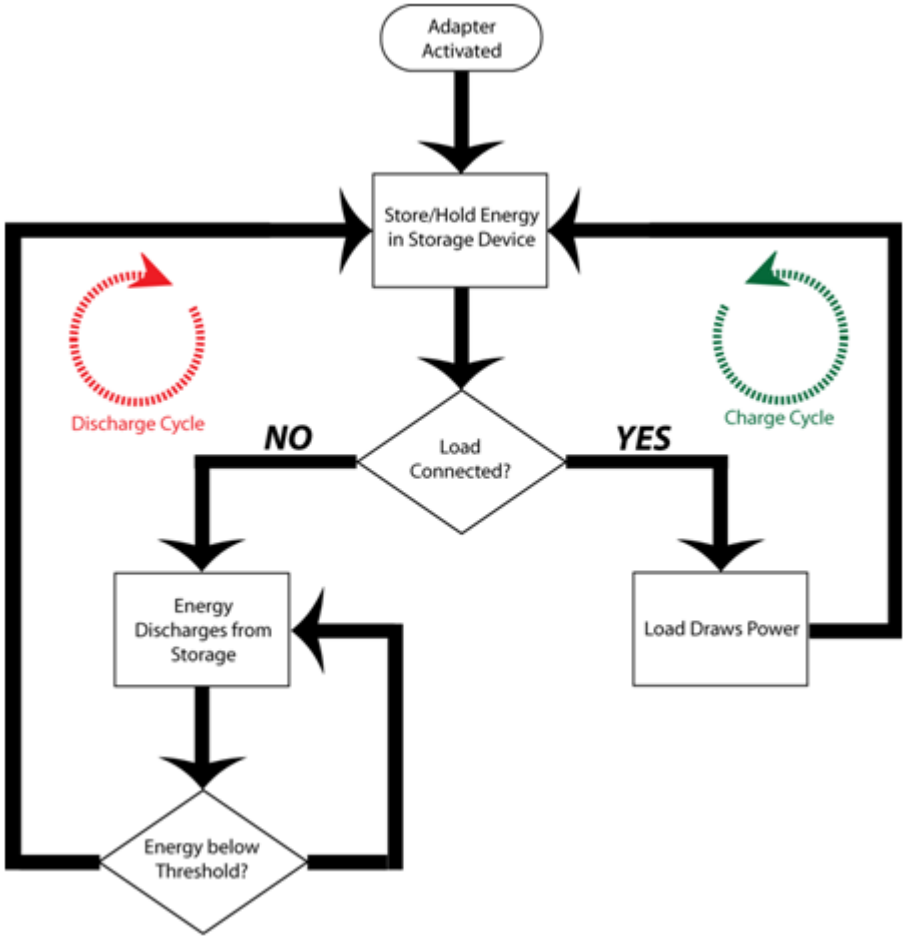


Figure 6-1: Basic adapter functionality. When the adapter is activated, storage device is filled to full capacity with electrical or magnetic energy. During this time, the load is charged. When the load is disconnected, energy is discharged from the storage device until the energy drops below a particular threshold. When this occurs, the adapter is reactivated. Notice the charge cycle when the adapter is activated and the discharge cycle when the adapter is deactivated.

Figure 6-1 shows a flowchart of an efficient wall adapter with a low-power standby mode. The critical components for implementing this functionality lie with the decisions made by the control system:

1. *Is a load connected to the DC output?*
2. *When the adapter is off, has the energy in the storage device depleted past a particular level?*

One potential way of using passive components to reactivate the adapter was explored in the *Jump Start* approach presented in Chapter 3. In this case, the passive nature of the design should cause the system to react to a load reconnect. The adapter presented in this report performs this function using active devices that signal the 555 timer subcircuit when the load is disconnected. However, it would be more efficient if an adapter modeled around the *Jump Start* approach utilized passive components to realize this precise functionality of flagging the power interrupt circuitry whenever low current is detected.

In theory, the *Jump Start* could provide an ideal standby power consumption of 0W. However, the team encountered a number of functional problems that could not be overcome within the scope of this project. Mainly, a voltage could not be obtained across the power connections to the cell phone's battery. While a phone manufacturer can design a phone to accommodate the *Jump Start* idea, it would require prior acceptance of the design amongst the cellular phone community. Other problems inherent in the idea, such as reactivating the adapter from a completely dead battery, could be overcome with additions like a manual reset switch on the adapter. Therefore, the team believes that although the *Jump Start* approach may be feasible and potentially rewarding, it would require more of a concerted *full-system* design effort from a phone manufacturer.

Another idea inspired by the design process, but left undeveloped within the scope of this project was that of capacitive current sensing. The team implemented a capacitive polling method as one solution, though it underperformed expectations. Yet, capacitors still have potential as current-sensing devices. In particular, it would be particularly efficient to make use of the already existing capacitors located across the output of the adapter, as seen in Figure 6-2.

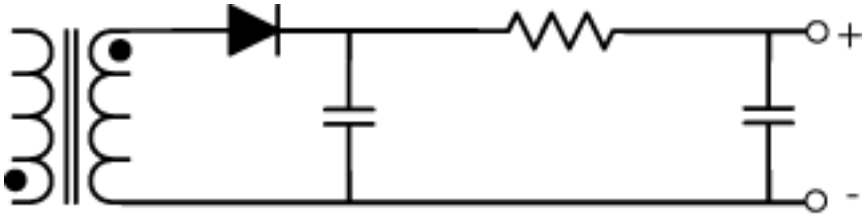


Figure 6-2: The output stage of the power adapter, showing two filter capacitors.

The capacitor on the left, with its proximity to the active transformer, seems like a viable option. When the transformer coil produces positive current, the diode becomes forward biased and the capacitor charges to about 5V, as seen in Figure 6-3. When the current from the transformer reverses, the diode becomes reverse biased, and the current drawn at the adapter output is supplied by the capacitor only, as seen in Figure 6-4.

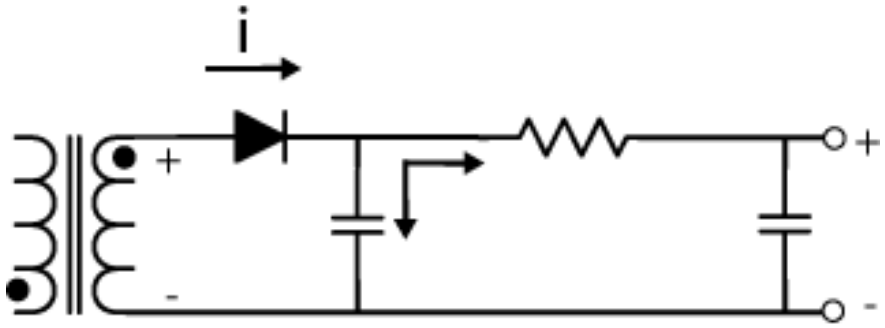


Figure 6-3: Output stage of an adapter. Rectifier diode is forward biased, capacitor is charging.

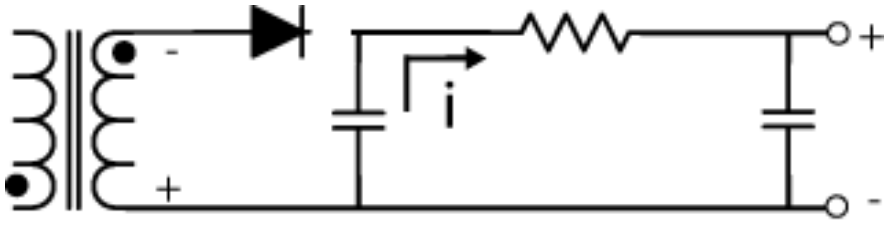


Figure 6-4: Output stage of an adapter. Rectifier diode is reverse biased, capacitor is discharging.

This period of discharging provides an opportunity to determine how much current is being drawn by the output. A capacitor's current-voltage relationship is given by the following formula:

$$I = C\frac{dV}{dt} \qquad (6\text{-}1)$$

Notice that the more current that is drawn from the capacitor, the faster its voltage will drop. This relationship is illustrated in Figure 6-5. Given equal run times, a capacitor with a high current draw will fall to a lower voltage than a capacitor with a lower current draw. Monitoring the voltage across the capacitor, then, becomes a viable way of determining how much current is being drawn by the source.

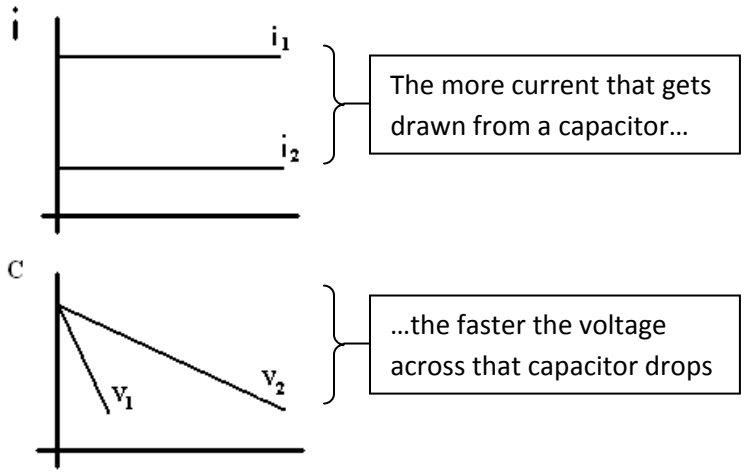


Figure 6-5: Current-voltage relationship for a capacitor; the voltage across an adapter drops as the integral of the current being drawn from it. Therefore, by monitoring how low the capacitor's voltage gets between recharges, the current that was being drawn from it can be determined.

However, in attempting to find a way to use this technique in sensing current, there are three key roadblocks. The first problem arises due to the frequency at which the current cycles from the transistor. The NCP1011 switching IC that runs this switch mode power supply runs at 100kHz. This provides only 5µs for the capacitor to act as a source for the DC load. The output voltage is intended to remain as constant as possible, but it makes the task of detecting meaningful voltage differences difficult. The expected voltage drop across the 1mF capacitor for a 50mA load can be determined using the following equations:

$$I = C\frac{dV}{dt} \tag{6-2}$$

$$dV = \frac{I}{C}dt = \frac{0.05}{0.001}5 \times 10^{-6} = 25\mu V \tag{6-3}$$

With only a $25\mu V$ drop appearing across the capacitor, it would seem far more practical to continue to amplify the 60mV difference that would appear across current-sensing resistor R4 with a 50mA load.

The second problem was a logistical problem with triggering. It is necessary to be able to trigger an adapter shutdown when the load current becomes too low. However, the capacitor's voltage actually drops *less* when there is a lower load current. In this case, any trigger set would also be exceeded by a large load current, which drops the capacitor voltage even further. The only apparent way around this would involve polling the capacitor voltage at the end of every 100kHz cycle, at which point a high voltage would indicate low current and a low voltage would indicate high current.

However, this form of polling would likely require additional components to implement, removing some of the benefit of switching to capacitive current sensing.

The third problem is one that may not be immediately recognizable until investigating the circuit with an oscilloscope. By monitoring the voltage across the capacitor with both a 50mA load and an open (no) load, it is possible to capture the two plots shown in Figure 6-6.

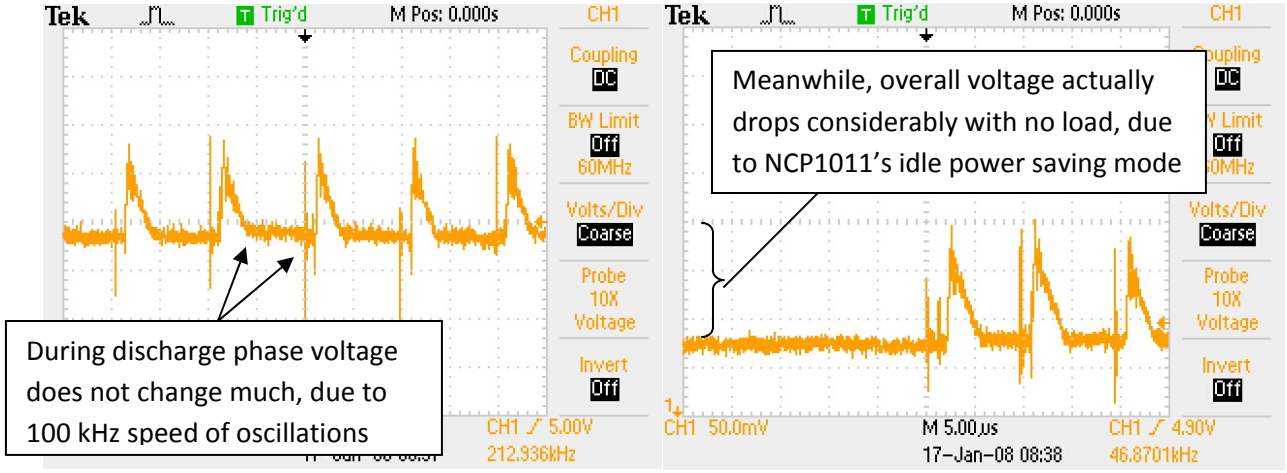


Figure 6-6: Voltage across adapter's output capacitor; with 50mA load (left), open load (right). The discharging voltage drop is relatively very small, due to the fast 100 kHz charge-discharge cycles. The capacitive voltage drop is further confused by a large overall voltage drop when no load is applied and the NCP1011 switcher enters power saving mode.

The voltage across the capacitor with no load was significantly less than the voltage across the capacitor when a load was present. This seems to contradict the theory that high currents would reduce the voltage across the capacitor faster. However, this drop was not being caused by current draining the capacitor. It instead appears to be the result of the NCP1011's built-in idle power saving technique, in which it slows or stops its oscillation momentarily, resulting in this drop in voltage at the output [28]. The result of this is added complication to any monitoring technique that may be implemented, as higher current produces larger and larger voltage drops.

Therefore, it does not appear that it would be possible to easily make use of the $I = C\frac{dV}{dt}$ relation of the capacitor. However, it is conceivable that the voltage drop caused by the NCP's power saving mode could be used to trigger a full shutdown. Capacitive current sensing might also be made more effective if a switcher was used that did not have its own power saving modes, making the voltage level on the output capacitors more reliable. The team simply decided that for this project, it would not

be suitable to implement a solution that relies on proprietary or specific technology implemented in the basic adapter itself, instead opting for a solution that could be applied to any manufacturer's adapter design since the end product was intended as an adapter modification and not a new design altogether.

In addition to using an output capacitor as a current-sensing component, future work can be conducted regarding the improvement of the capacitive-polling proposition in this project. Capacitors are used predominantly for energy storage since they are relatively inexpensive compared to inductors. It can therefore be assumed that efforts made to simplify and improve the design will utilize capacitors rather than inductors. Assuming an initial condition of 0V, a capacitor's step response follows an exponential relationship:

$$V_{OUT} = V - Ve^{\frac{-t}{\tau}} \tag{6-4}$$

The time constant τ is defined as time required for the capacitor to charge up to 63% of V. In addition, it is known that the capacitor has nearly discharged all of its energy after 5 time constants, or (5τ)s.

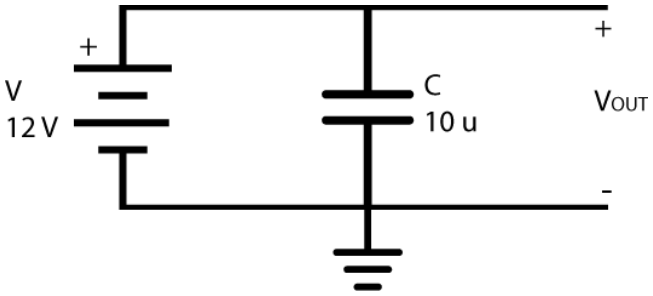


Figure 6-7: Schematic of modeled DC output of adapter. V represents the DC output voltage, and the capacitance C1 represents the total capacitance at the output of the adapter.

Figure 6-7 shows the circuit described by the step response equation. The voltage V is a model of the DC output voltage as soon as the user plugs in the adapter. V_{OUT} will charge toward the voltage level V. The capacitor's energy, like other energy storage devices, depends upon its capacity of energy and the amount of energy supplied. Given the values stipulated by the schematic in Figure 6-7, the energy stored in the capacitor once V_{OUT} equals V is 720μJ:

$$W_C = \frac{1}{2}CV_{OUT}{}^2 = \frac{1}{2}(10\mu F)12^2 = 720\mu J \tag{6-5}$$

This energy remains constant as long as the adapter is functioning. If the user unplugs the adapter, the energy will slowly decay as the energy is dissipated in other areas of the circuit. Figure 6-8 provides an illustration of a segment of the adapter's output stage.

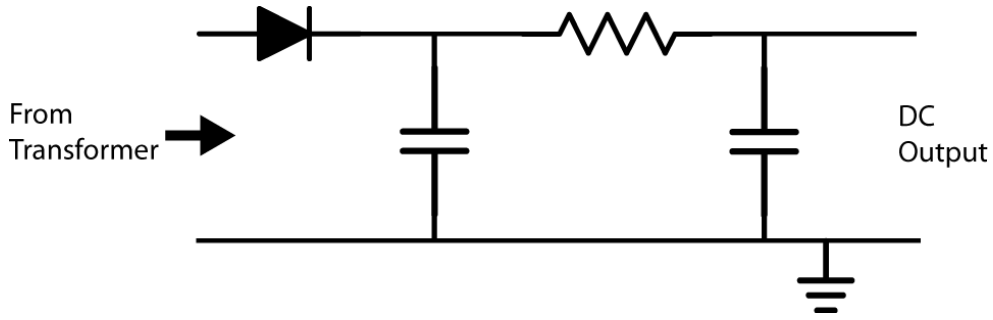


Figure 6-8: Segment of the DC output stage of the efficient wall adapter.

When the adapter is functioning, the voltage across C8 and C9 is approximately 5V, since the small series resistance incurs an infinitesimal amount of voltage. When a capacitor experiences a square pulse or step response as mentioned earlier, the time required to meet the expected value is 5τ. The relationship between τ and C8 is shown below:

$$\tau = R_{TOTAL}C_{TOTAL} = R6(C9||C8) \quad (6\text{-}6)$$

According to (6-6), the time taken to discharge all the energy in capacitor C8 is equal to R6(C9||C8). While R6 has a very low resistance, the impedance of capacitor C8 is extremely large (ideally $Z_{C9} = \infty$). Taking into account a high impedance combination of R6 and C9, the time required for C8 to drain all of its energy will be very long in duration. An important reason this duration is rather long is due to the rectifier diode D4. This diode provides another high impedance component between the transformer winding and C8, R6, and C9. A long time constant τ is required for a polling reactivation technique using passive components.

According to these results, an efficient wall adapter with passive polling is plausible, but includes several complications yet to be discussed. For instance, necessary feedback interfaces are required to relay the capacitor's energy status with the control circuitry. In particular, a feedback network is required with a high impedance input. If the feedback stage requires a significant amount of power, the energy stored in the capacitor C8 will discharge at a more rapid rate. If this rate is too high, the validity of the passive polling idea is jeopardized.

Figure 6-9 describes the top-level approach of implementing a passive polling adapter. Once again, a high-impedance feedback network is necessary to maintain a sufficiently long discharge characteristic. Therefore, an optoisolator may not be useful in this situation, since the LED trigger requires a significant amount of power to activate.

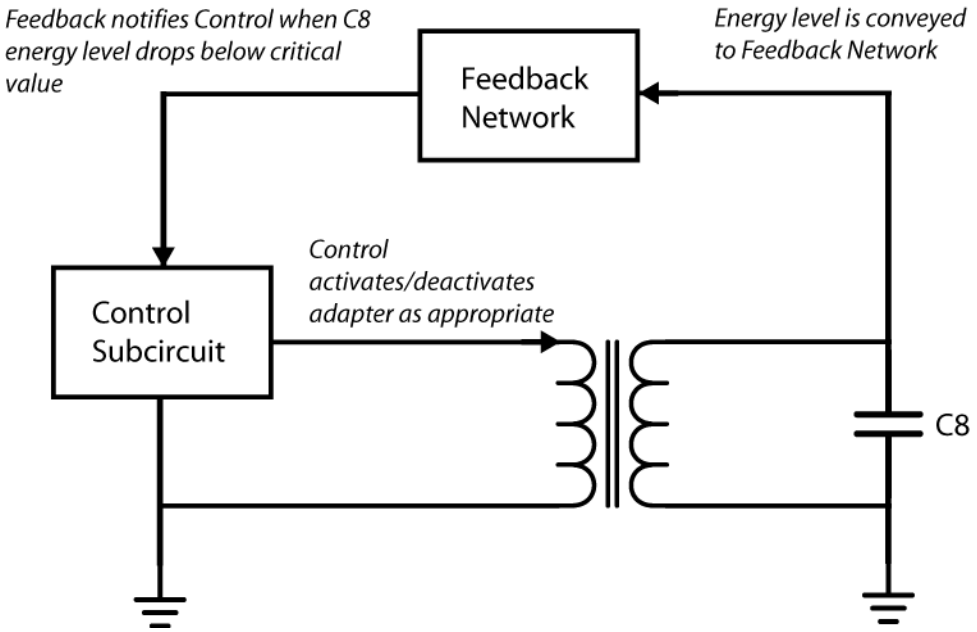


Figure 6-9: Top-level design of efficient wall adapter with passive polling.

A reasonable response to developing a high-impedance feedback network is to circumvent the network altogether. This idea, however, has many inherent flaws, such as isolation infringements. Connecting the capacitor C8 directly to the control subcircuit would provide a connection between the DC signal and DC ground with the AC signal and AC ground. Since the grounds of both circuits are not identical, safety issues become prevalent and circuit functionality will become questionable. In fact, these particular issues encouraged the team to steer away from utilizing passive polling in its adapter configuration. In order to build a functioning circuit consuming equal or less power than the project's model, the problems of interfacing and isolation need to be addressed.

Although the team largely had to dismiss passive ideas such as capacitive polling and current sensing during this project, the actual concept of using exclusively passive components for circuit reactivation and other functions is ideal. Instead of a proactive solution, a reactive design would store energy during operation and discharge this energy during idle use. As long as the circuit reactivates when the detected stored energy plummets below a lower threshold, the adapter would never become trapped in a dormant condition.

Any of these potential avenues for future work, or perhaps others not mentioned here, could be expanded in an effort to achieve or approach the ideal solution to the problem posed by this project. That is, when there is no load, there should be no loss.

Conclusion 7

The Efficient Wall Adapter project provided the team from beginning to end with unique requirements and guidelines that called for simplicity in design to achieve a complex function. It is hoped that the report highlighted the deliberate, logical progression undertaken by the team to respond to necessary concerns in such a design. Working at the component level, an arrangement of commonly-used configurations was configured to exceed expectations in creating an adapter that is 85% more efficient than modern adapters when idle at an additional cost of only $1.21.

In the first chapter of this report, the team outlined its goals and objectives in the hope that they would be fully met and completed. The first objective was to develop a product that could be universally applied to any variety of external power adapters on the market. The simplicity of the final design could provide universal application capability through the simple manipulation of critical component values, such as the resistors used in the difference amplifier or 555 timer subcircuits. Moreover, a slight change in these component values would have no affect on the overhead cost of the product. The next objective discussed the hopes of integrating the solution with present adapter designs in efforts to minimize an increase in device size. Much of the final circuit's functionality is performed using ICs and basic components, so integration is plausible due to its compactness in design. Another specification goal for the project stipulated that the cost impact of the final circuit to existing adapters should be minimal. Calculations were based on a maximum two-year *break-even* proposition, equating to an overall budget of $1.30 for this project. Based upon the prices of the final design's components at the date of this report's publication, the cost of additional circuitry is under budget.

In terms of functionality, it was desired to reduce the modern efficient power adapter's power consumption by 75%. According to the Energy Star initiative, the United States government hopes to reduce no-load power consumption to 150mW [17]. Presently, the requirement is 500mW. The efficient power adapter designed by the team consumes 34mW in standby mode, which is a 77% reduction of even Energy Star's desired goal. In order to assure that the product would adapt well to future, more efficient cell phones, a requirement was set to operate the adapter above a maximum output current threshold of 15mA. The low-current sensing performed in this design permits a minimum output current of around 11.6mA. Although this may not seem to be a prevalent issue, it is

likely that future cell phones will be smaller in size and more efficient in power consumption. The ability to allow low-current loads is thus important to the design of the adapter.

The project was successful in achieving each objective set in its early stages. However, the team concedes its inability to design the ideal solution, which would consume zero power during no-load conditions. The scope and timetable for this project did not warrant a thorough investigation of the validity of the *Jump Start* concept. Once a power supply of this magnitude is designed, the idle losses incurred by all users of consumer electronics will be vanquished and deemed obsolete. In fact, this shortcoming provides motivation for similar projects to be pursued. Indeed, it is hoped that one day this *no load, no loss* functionality will be realized.

Specifically, the team hopes that parties interested in this project concur with and continue to develop the solution proposed for creating an efficient wall adapter. Furthermore, it is hoped that the logical, deliberate approach that was taken to design the final product demonstrates the thorough nature in which this project was conducted. In addition to the problem of external power supplies, attention should also be focused on other integrated power supplies, such as those found in large household appliances. The sooner the problem is addressed, the more relief can be granted to the scarcity of the world's energy sources.

When an engineer sits down to work, they can often picture the end user happily enjoying their creation. However, for 23 hours per day, the common reality of the device sitting in a corner, unused, fails to come across the designer's mind. As a result, society encounters problems such as the idle adapter energy waste addressed by this project. The adapter presented in this report is one of the first power adapters specifically designed to not be used. For the sake of both our wallet and our planet, we hope it is not the last.

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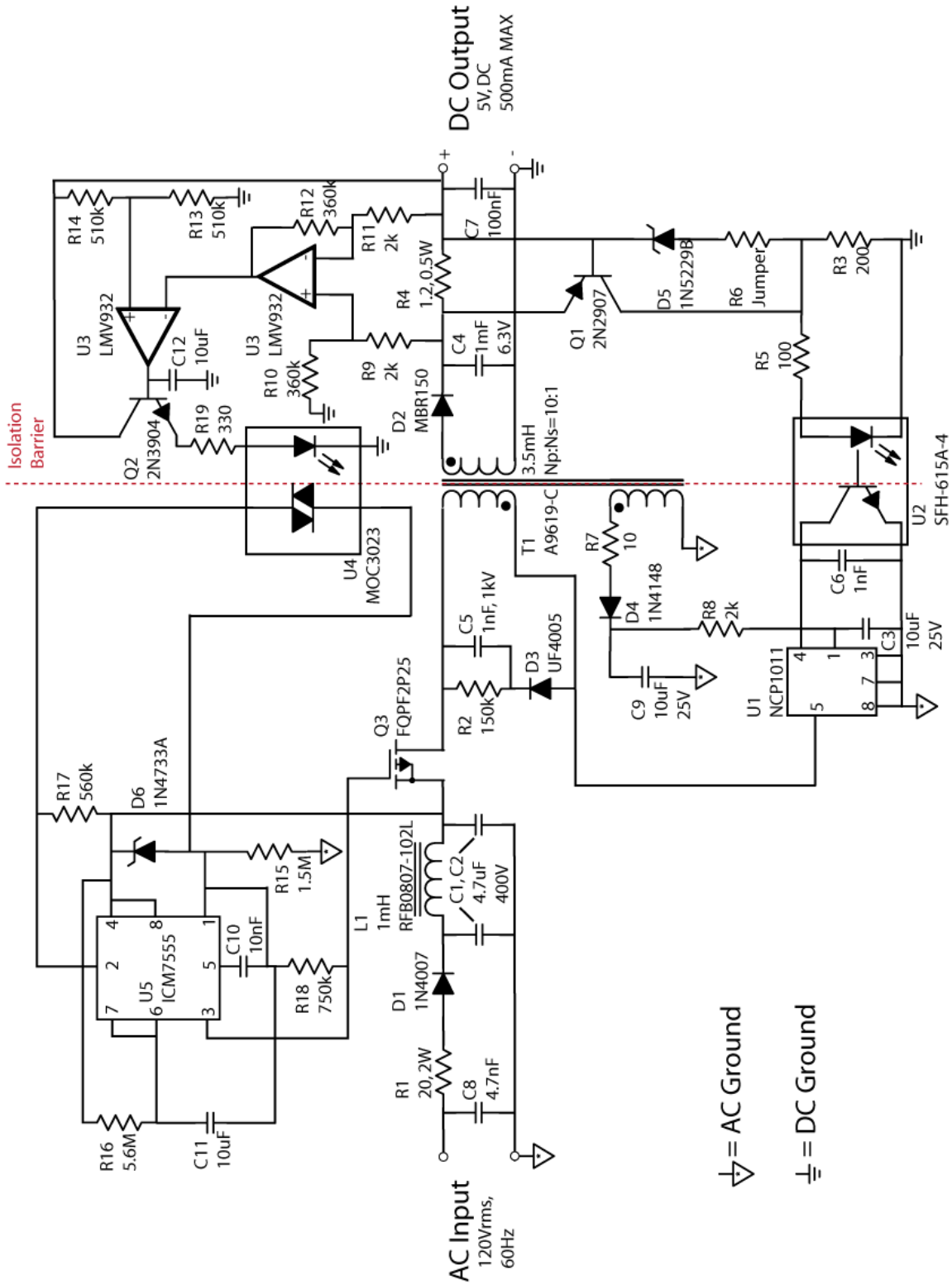
Appendix A – Final Schematic and Parts List



Test Bed Parts - Revision D

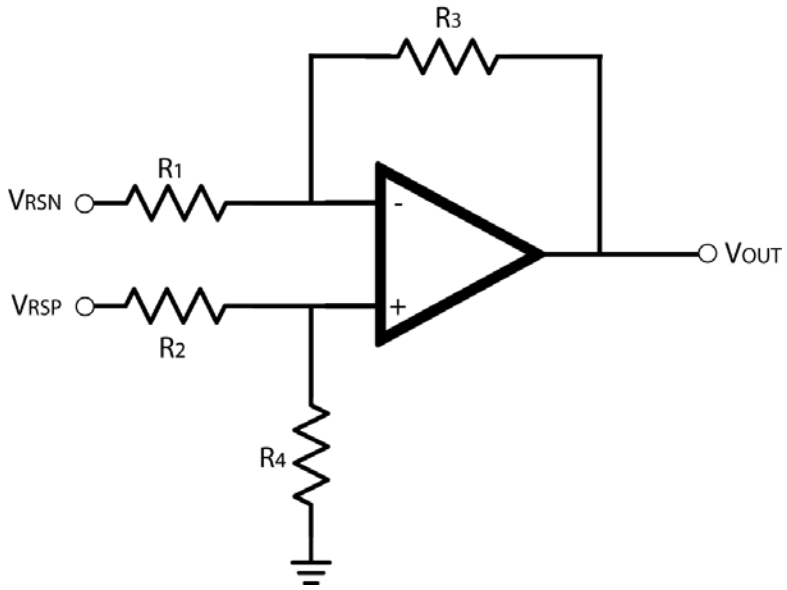
Quantity	Label	Part Type	Value	Distributor	Manufacturer Part #	Distributor Part #	Unit Price (1000)	Total Price
1	T1	Transformer	3.5 mH	Coilcraft	A9619-C	A9619-C	$1.680	$1.680
1	U3	IEC AC PCB	Pin	Mouser	GSP2.8101.13	693-GSP2.8101.13	$1.150	$1.150
1	U1	Switcher IC	NCP1011ST	Mouser	NCP1011AP100G	863-NCP1011AP100G	$0.604	$0.604
1	L1	Inductor	1mH	Mouser	SDR1005-102KL	652-SDR1005-102KL	$0.310	$0.310
1	R1	Resistor	20Ω, 2W	Mouser	CPF220R000FKE14	71-CPF2-F-20-E3	$0.299	$0.299
1	U2	Optocoupler	SFH-615A-4	Mouser	SFH615A-4	782-SFH615A-4	$0.250	$0.250
2	C1, C2	Capacitor	4.7uF, 400V	Mouser	UVR2G4R7MPD	647-UVR2G4R7MPD	$0.137	$0.274
1	D2	Diode	MBR150	Mouser	MBR150G	863-MBR150G	$0.097	$0.097
1	Q1	BJT	2N2907	Mouser	PN2907A	610-PN2907A	$0.090	$0.090
2	C5, C6	Capacitor	1nF, 1kV	Mouser	DEHR33A102KA2B	81-DEHR33A102KA2B	$0.088	$0.176
1	C8	Capacitor	4.7nF	Mouser	140-500P5-472K-RC	140-500P5-472K-RC	$0.080	$0.080
1	D3	Diode	UF4005	Mouser	UF4005	512-UF4005	$0.059	$0.059
1	C4	Capacitor	1mF	Mouser	UVR0J102MPD1TA	647-UVR0J102MPD1TA	$0.059	$0.059
1	R4	Resistor	1.2Ω, 0.5W	Mouser	MF1/2LC1R2J	660-MF1/2LC1R2J	$0.057	$0.057
1	C7	Capacitor	100nF	Mouser	K104K15X7RF53H5	594-K104K15X7RF53H5	$0.050	$0.050
4	C3, C9, C10, C13	Capacitor	10uF	Mouser	USR1E100MDD	647-USR1E100MDD	$0.048	$0.192
1	D1	Diode	1N4007	Mouser	1N4007G	863-1N4007G	$0.019	$0.019
1	D5	Zener	1N5229B	Mouser	1N5229B	512-1N5229B	$0.015	$0.015
1	R2	Resistor	150kΩ	Mouser	CFS1/4CT52R154J	660-CFS1/4CT52R154J	$0.009	$0.009
1	R7	Resistor	10Ω	Mouser	CFS1/4CT52R100J	660-CFS1/4CT52R100J	$0.009	$0.009
3	R8, R10, R11	Resistor	2kΩ	Mouser	CFS1/4CT52R202J	660-CFS1/4CT52R202J	$0.009	$0.027
1	R3	Resistor	200Ω	Mouser	CFS1/4CT52R201J	660-CFS1/4CT52R201J	$0.009	$0.009
1	D4	Diode	1N4148	Mouser	1N4148-TR	78-1N4148	$0.008	$0.008
1	R5	Resistor	100Ω	Mouser	CFS1/4CT52R101J	660-CFS1/4CT52R101J	$0.008	$0.008
1	Q3	PMOSFET	FQPF2P25	Mouser	FQPF2P25	512-FQPF2P25	$0.218	$0.218
1	U6	Opto-TRIAC	MOC3023	Digi-Key	MOC3023	160-1378-5-ND	$0.210	$0.210
1	D6	Zener	1N4733A	Mouser	1N4733A	78-1N4733A	$0.025	$0.025

1	R19	Resistor	1.5MΩ	Digi-Key	CFR-25JB-1M5	1.5MQBK-ND	$0.008	$0.008
1	R9	Resistor	750kΩ	Digi-Key	CFR-25JB-750K	750KQBK-ND	$0.008	$0.008
1	R21	Resistor	5.6MΩ	Digi-Key	CFR-25JB-5M6	5.6MQBK-ND	$0.008	$0.008
2	C11, C12	Capacitor	0.01uF	Mouser	140-50Q5-103Z-RC	140-50Q5-103Z-RC	$0.020	$0.040
1	R20	Resistor	560kΩ	Digi-Key	CFR-25JB-560K	560KQBK-ND	$0.008	$0.008
2	R12, R13	Resistor	360kΩ	Digi-Key	CFR-25JB-360K	360KQBK-ND	$0.008	$0.016
2	R16, R17	Resistor	510kΩ	Digi-Key	CFR-25JB-510K	510KQBK-ND	$0.008	$0.016
1	R18	Resistor	330Ω	Digi-Key	CFR-25JB-330R	330QBK-ND	$0.008	$0.008
1	Q2	BJT	2N3904	Mouser	2N3904TA	512-2N3904TA	$0.017	$0.017
1	U5	Amplifier	LMV932	Mouser	LMV932ID	595-LMV932ID	$0.372	$0.372
1	U4	Timer IC	ICM7555	Digi-Key	ICM7555CN/01	568-1819-5-ND	$0.133	$0.133
1	R6	Jumper	0Ω	Mouser	Z25YC	660-Z25YC	$0.007	$0.007
							Total	$6.63

Date: 3/5/2007

Appendix B – Common Mode Effect Derivation

The team's current-monitoring solution is centered on the differential amplifier, such the one shown in Figure B-1. One of the potential issues with differential amplifiers is that, unless the resistors are matched precisely, the ideal formula of $V_{out} = \frac{R_3}{R_1}(V_{RSP} - V_{RSN})$ does not hold. If the resistor ratio is not $\frac{R_4}{R_2} = \frac{R_3}{R_1}$, noise will be introduced in the form of what is called *common mode amplification*. If, for example, the input nodes of a difference amplifier were 5V and 5.01V, the output would ideally be 0.01V, amplified by the given resistor ratio. If this resistor ratio is not accurate, however, the 5V common to each input node begins to affect the output voltage as well. The quality of differential amplifiers is often judged by the degree of *common mode rejection* they offer.



FigureB-1: Generic differential amplifier configuration.

Typical resistors have tolerances of 5%, though 1% and lower tolerances are available at added cost. In order to see what effect these variances could have on amplifier in the low-current sense, the amplifier's performance when its associated resistors vary in value must be determined.

Kirchhoff's Current Law, as applied to the inverting node of the op-amp, assuming infinite input impedance is:

$$\frac{V_{RSN} - V_-}{R_1} = -\frac{V_{out} - V_-}{R_3} \qquad \text{(B-1)}$$

Solving for V_{out}:

$$V_{out} = -\frac{V_{RSN}-V_-}{R_1}R_3 + V_- \quad \text{(B-2)}$$

$$V_{out} = -V_{RSN}\frac{R_3}{R_1} + V_-\frac{R_3}{R_1} + V_- \quad \text{(B-3)}$$

$$V_{out} = -V_{RSN}\frac{R_3}{R_1} + V_-\left(\frac{R_3}{R_1}+1\right) \quad \text{(B-4)}$$

The voltage at the non-inverting node of the op-amp is:

$$V_+ = V_{RSP}\frac{R_4}{R_2+R_4} \quad \text{(B-5)}$$

Due to the *virtual ground* effect, the voltages at the inverting and non-inverting nodes are equal. Substituting into (B-4):

$$V_{out} = -V_{RSN}\frac{R_3}{R_1} + V_{RSP}\left(\frac{R_4}{R_2+R_4}\right)\left(\frac{R_1+R_3}{R_1}\right) \quad \text{(B-6)}$$

So:

$$V_{out} = V_{RSP}\frac{R_4(R_1+R_3)}{R_1(R_2+R_4)} - V_{RSN}\frac{R_3}{R_1} \quad \text{(B-7)}$$

(B-7) defines the resistor-based factors each input is amplified by before the difference is taken. Ideally these factors are equal, but it is clear that as resistor values vary this will not be the case. This lopsided amplification factor can be emphasized with some further manipulation:

$$V_{out} = V_{RSP}\left(\frac{R_4}{R_2+R_4}\right)\left(\frac{R_1+R_3}{R_1}\right) - V_{RSN}\frac{R_3}{R_1} \quad \text{(B-8)}$$

$$V_{out} = V_{RSP}\left(\frac{1}{\frac{R_2+R_4}{R_4}}\right)\left(1+\frac{R_3}{R_1}\right) - V_{RSN}\frac{R_3}{R_1} \quad \text{(B-9)}$$

$$V_{out} = V_{RSP}\left(\frac{1}{\frac{R_2}{R_4}+1}\right)\left(1+\frac{R_3}{R_1}\right) - V_{RSN}\frac{R_3}{R_1} \quad \text{(B-10)}$$

$$V_{out} = V_{RSP}\left(\frac{1}{\frac{R_2}{R_4}+1}\right)\left(\frac{R_1}{R_3}+1\right)\frac{R_3}{R_1} - V_{RSN}\frac{R_3}{R_1} \quad \text{(B-11)}$$

$$V_{out} = \frac{R_3}{R_1}\left[\left(\frac{\frac{R_1}{R_3}+1}{\frac{R_2}{R_4}+1}\right)V_{RSP} - V_{RSN}\right] \quad \text{(B-12)}$$

(B-12) clearly illustrates the results of resistor mismatching, amplifying some of the absolute (common) voltage at the input rather than just the relative (difference). Notice that if $\frac{R_4}{R_2} = \frac{R_3}{R_1}$, the equation simplifies to the ideal difference-amplifying case.

There is even a third way to look at this unwanted amplification, by explicitly separating the difference and common mode amplification factors. We will begin with Equation 3, but first note that this equation is in the form:

$$V_{out} = aV_{RSP} - bV_{RSN} \tag{B-13}$$

Where:

$$a = \frac{R_4(R_1+R_3)}{R_1(R_2+R_4)} \text{ and } b = \frac{R_3}{R_1} \tag{B-14}$$

We can then make the following manipulations:

$$V_{out} = \frac{aV_{RSP}}{2} + \frac{aV_{RSP}}{2} - \frac{bV_{RSN}}{2} - \frac{bV_{RSN}}{2} \tag{B-15}$$

$$V_{out} = \left(\frac{aV_{RSP}}{2} - \frac{bV_{RSN}}{2}\right) + \left(\frac{aV_{RSP}}{2} - \frac{bV_{RSN}}{2}\right) \tag{B-16}$$

$$V_{out} = \left(\frac{aV_{RSP}}{2} - \frac{bV_{RSN}}{2}\right) + \left(\frac{aV_{RSP}}{2} - \frac{bV_{RSN}}{2}\right) + \frac{aV_{RSN}}{2} - \frac{aV_{RSN}}{2} + \frac{bV_{RSP}}{2} - \frac{bV_{RSP}}{2} \tag{B-17}$$

$$V_{out} = \left(\frac{aV_{RSP}}{2} + \frac{bV_{RSP}}{2} - \frac{aV_{RSN}}{2} - \frac{bV_{RSN}}{2}\right) + \left(\frac{aV_{RSP}}{2} - \frac{bV_{RSP}}{2} + \frac{aV_{RSN}}{2} - \frac{bV_{RSN}}{2}\right) \tag{B-18}$$

$$V_{out} = \frac{(a+b)(V_{RSP}-V_{RSN})}{2} + \frac{(a-b)(V_{RSP}+V_{RSN})}{2} \tag{B-19}$$

So:

$$V_{out} = \left(\frac{a+b}{2}\right)[V_{RSP} - V_{RSN}] + (a-b)\left[\frac{V_{RSP}+V_{RSN}}{2}\right] \tag{B-20}$$

Note that the first half of (B-20) is an amplification factor for the difference between the input voltages, and the second half of the equation is an amplification factor for the average of the input voltages, or the common mode. More explicitly:

Difference gain:

$$\frac{a+b}{2} = \frac{R_4(R_1+R_3)}{2R_1(R_2+R_4)} + \frac{R_3}{2R_1} = \frac{R_4(R_1+R_3)}{2R_1(R_2+R_4)} + \frac{R_3(R_2+R_4)}{2R_1(R_2+R_4)} \tag{B-21}$$

$$G_d = \frac{R_4(R_1+R_3)+R_3(R_2+R_4)}{2R_1(R_2+R_4)} \quad \text{(B-22)}$$

Common mode gain:

$$a - b = \frac{R_4(R_1+R_3)}{R_1(R_2+R_4)} - \frac{R_3}{R_1} = \frac{R_4(R_1+R_3)}{R_1(R_2+R_4)} - \frac{R_3(R_2+R_4)}{R_1(R_2+R_4)} \quad \text{(B-23)}$$

$$G_c = \frac{R_1R_4-R_2R_3}{R_1(R_2+R_4)} \quad \text{(B-24)}$$

Now that we have defined the difference and common mode gains, we can return to our original concern. Note that the common mode gain in (B-24) reduces to zero if $\frac{R_4}{R_2} = \frac{R_3}{R_1}$. However, what happens when the resistor ratio is disturbed by inaccuracies, such that $\frac{R_4}{R_2} = (1+\epsilon)\frac{R_3}{R_1}$? To determine this effect we will assume R_1 is equal to R_2, but replace R_3 with $R_3\left(1-\frac{\epsilon}{2}\right)$ and R_4 with $R_3\left(1+\frac{\epsilon}{2}\right)$. Starting with (B-24), and assuming G_d remains approximately $\frac{R_3}{R_1}$, this effects performance as follows:

$$G_c = \frac{R_1R_4-R_2R_3}{R_1(R_2+R_4)} = \frac{R_1R_3\left(1+\frac{\epsilon}{2}\right)-R_1R_3\left(1-\frac{\epsilon}{2}\right)}{R_1\left(R_1+R_3\left(1+\frac{\epsilon}{2}\right)\right)} \quad \text{(B-25)}$$

$$G_c = \frac{R_1R_3\epsilon}{{R_1}^2+R_1R_3\left(1+\frac{\epsilon}{2}\right)} \quad \text{(B-26)}$$

$$G_c = \frac{\frac{R_3}{R_1}\epsilon}{1+\frac{R_3}{R_1}\left(1+\frac{\epsilon}{2}\right)} \quad \text{(B-27)}$$

Assuming a relatively small tolerance, $\left(1+\frac{\epsilon}{2}\right)$ approaches 1, leaving:

$$G_c = \frac{\epsilon\, G_d}{1+G_d} \quad \text{(B-28)}$$

G_c is clearly directly related to resistor tolerance. But common mode rejection is usually measured in what is called the Common Mode Rejection Ratio, or CMRR. The CMRR is found by simply dividing the difference gain by the common mode gain. It is commonly measured in decibels, with

$$CMRR = 20\ log\left(\frac{G_d}{G_c}\right) \quad \text{(B-29)}$$

This ratio can be derived using our tolerance-added resistors as follows:

$$\frac{G_d}{G_c} = \left(\frac{R_4(R_1+R_3)+R_3(R_2+R_4)}{2R_1(R_2+R_4)}\right)\left(\frac{R_1(R_2+R_4)}{R_1R_4-R_2R_3}\right) \quad \text{(B-30)}$$

$$\frac{G_d}{G_c} = \frac{R_4(R_1+R_3)+R_3(R_2+R_4)}{2(R_1R_4-R_2R_3)} \tag{B-31}$$

$$\frac{G_d}{G_c} = \frac{R_3\left(1+\frac{\epsilon}{2}\right)\left(R_1+R_3\left(1-\frac{\epsilon}{2}\right)\right)+R_3\left(1-\frac{\epsilon}{2}\right)\left(R_1+R_3\left(1+\frac{\epsilon}{2}\right)\right)}{2\left(R_1R_3\left(1+\frac{\epsilon}{2}\right)-R_1R_3\left(1-\frac{\epsilon}{2}\right)\right)} \tag{B-32}$$

$$\frac{G_d}{G_c} = \frac{R_1R_3\left(1+\frac{\epsilon}{2}\right)+{R_3}^2\left(1-\frac{\epsilon^2}{4}\right)+R_1R_3\left(1-\frac{\epsilon}{2}\right)+{R_3}^2\left(1-\frac{\epsilon^2}{4}\right)}{2R_1R_3\epsilon} \tag{B-33}$$

$$\frac{G_d}{G_c} = \frac{2R_1R_3+2{R_3}^2\left(1-\frac{\epsilon^2}{4}\right)}{2R_1R_3\epsilon} \tag{B-34}$$

$$\frac{G_d}{G_c} = \frac{1}{\epsilon} + \frac{R_3}{R_1}\frac{\left(1-\frac{\epsilon^2}{4}\right)}{\epsilon} \tag{B-35}$$

Given any reasonably low tolerance, $\left(1-\frac{\epsilon^2}{4}\right)$ will be very near 1, so:

$$\frac{G_d}{G_c} = \frac{1+\frac{R_3}{R_1}}{\epsilon} \tag{B-36}$$

$$\frac{G_d}{G_c} = \frac{1+G}{\epsilon} \tag{B-37}$$

$$CMRR = 20\ log\left(\frac{1+G}{\epsilon}\right) \tag{B-38}$$

(B-38) describes the relation between common mode reduction and resistor tolerance, where G is the desired gain. Notice that by either reducing tolerance or increasing the desired gain, common mode rejection can be improved.

Appendix C – PSpice Simulation Code

Full Adapter

```
**ON Semiconductor DN06017/D Cell Phone Charger**
*
*
*Brendan Barschdorf & Russell Kernan
*Worcester Polytechnic Institute
*Dept.  of Electrical & Computer Engineering
*Major Qualifying Project - Design of an Efficient Wall Adapter
*
*
*Friday, September 14, 2007

*Input Rectifier Model*

Vs 1 0 AC 1 SIN(0V 169.7V 60Hz) ; AC Input
C8 1 0 4.7n IC=0
R1 1 2 20
D1 2 3 D1N4007GP
C1 3 0 4.7u IC=0
L1 3 4 1m IC=0
C2 4 0 4.7u IC=0

*Snubber*

C5 4 5 1n IC=0
R2 4 5 150k
D3 6 5 DMUR160

*NCP1011 Subcircuit*

X1 10 11 6 0 NCP1011P10
*.SUBCKT NCP1011P10 VCC FB DRAIN GND
*X1 VCC FB DRAIN GND NCP101X PARAMS: Fsw=100k Conso=1m Ipeak=250m Rdson=26
*.ENDS
.LIB NCP101X.LIB

*Aux Winding Rectifier*

R7 7 8 10
D4 8 9 D1N4148
C9 9 0 10u IC=0

*NCP1011 Vcc Voltage Regulation*

R8 9 10 2k
C3 10 0 10u IC=0

*Transformer*

X3 6 4 12 13 7 0 XFMRAUX
.SUBCKT XFMRAUX 1 2 3 4 5 6
*PRIMARY
L1 1 2 2000
RT 1 7 1u
RU 2 8 1u
L2 7 8 2000
```

```
*SECONDARY
L3 3 4 20
L4 5 6 39.2
*MAGNETIC COUPLING
K13 L1 L3 0.99999
K24 L2 L4 0.99999
.ENDS

*Optocoupler Isolator*

C6 11 0 1n IC=0
X2 17 13 11 0 MOC8101
.SUBCKT MOC8101 1 2 3   5
* ISOLATOR AN CA CO EM
RB 4 0 1T
VM 1 6
D1 6 2 LED
H1 7 0 VM .0055
R1 7 8 1K
C1 8 0 3.35nF
G1 3 4 8 0 1
Q1 3 4 5 MPSA06
.MODEL LED D(N=1.7 RS=.7 CJO=23.9P IS=85.3p BV=6 IBV=10U
+ VJ=0.75 M=0.333 TT=4.32U)
.MODEL MPSA06 NPN (IS=15.2F NF=1 BF=589 VAF=98.6 IKF=90M ISE=3.34P NE=2
+ BR=4 NR=1 VAR=16 IKR=0.135 RE=0.343 RB=1.37 RC=0.137 XTB=1.5
+ CJE=9.67P VJE=1.1 MJE=0.5 CJC=7.34P VJC=0.3 MJC=0.3 TF=10.29n TR=276N)
.ENDS

*Output Filter*

D2 12 14 DMBR150RL
C4 14 13 1m IC=0
R4 14 15 1.2
C7 15 13 100n IC=0
Q1 16 15 14 D2N2907
X4 16 15 D1N4623
.SUBCKT D1N4623 4 2
.MODEL DHIGH  D (
+IS=1E-7 RS=9.11 N=4.989)
.MODEL DLO  D (IS=3.1E-7 RS=1.5K
+N=14.589)
.MODEL DF  D (IS=1.76E-13
+RS=1.638M N=1.18 CJO=296.3P
+VJ=.547 M=.294)
V1 1 4 3.281
D2 2 3 DLO
V3 3 4 1.916
D3 4 2 DF
D1 2 1 DHIGH
.ENDS
R3 16 13 200
R5 16 17 100

*Output Load*

RL 15 13 100

*Resistive Isolation*

RB 13 0 1T
```

```
.MODEL D1N4007GP  D (
+   IS =  6.698e-07
+   RS =  0.04255
+   CJO =  1.949e-11
+   VJ =  0.3909
+   TT =  4.933e-06
+   M =  0.3577
+   BV =  1000
+   N =  2.412
+   EG =  1.11
+   XTI =  3
+   KF =  0
+   AF =  1
+   FC =  0.5
+   IBV =  0.005177
+   TNOM =  27
+ )

.MODEL DMUR160  D (
+IS=1.08U
+RS=55.5M
+N=2.59
+BV=800
+IBV=5U
+CJO=15.7P
+VJ=.75
+M=.310
+TT=108N
+ )

.MODEL D1N4148  D (
+IS=0.1P
+RS=16
+CJO=2P
+TT=12N
+BV=100
+IBV=3.867E-10
+ )

.MODEL DMBR150RL  D (
+IS=6.47666e-09
+RS=0.184739
+N=0.832706
+EG=0.673879
+XTI=0.05
+BV=50
+IBV=0.0001
+CJO=2.81635e-10
+VJ=0.4
+M=0.559152
+FC=0.5
+TT=0
+KF=0
+AF=1
+ )

.MODEL D2N2907  PNP (
+IS=1.1p
+BF=200
+NF=1.2
+VAF=50
+IKF=0.1
```

```
+ISE=13p
+NE=1.9
+BR=6
+RC=0.6
+CJE=23p
+VJE=0.85
+MJE=1.25
+TF=0.5n
+CJC=19p
+VJC=0.5
+MJC=0.2
+TR=34n
+XTB=1.5
+ )

.END
```

Simplified Adapter

```
**Simplified ON Semiconductor DN06017/D Cell Phone Charger**
*
*
*Brendan Barschdorf & Russell Kernan
*Worcester Polytechnic Institute
*Dept.  of Electrical & Computer Engineering
*Major Qualifying Project - Design of an Efficient Wall Adapter
*
*
*Friday, September 18, 2007

*Input Rectifier Model*

Vs 1 0 AC 1 SIN(0V 169.7V 60Hz) ; AC Input
C8 1 0 4.7n IC=0
R1 1 2 20
D1 2 3 D1N4007GP
C1 3 0 4.7u IC=0
L1 3 4 1m IC=0
C2 4 0 4.7u IC=0

*Snubber*

C5 4 5 1n IC=0
R2 4 5 150k
D3 6 5 DMUR160

*Transformer*

X3 6 4 8 9 XFMRAUX
.SUBCKT XFMRAUX 1 2 3 4
*PRIMARY
L1 1 2 3.5m
*SECONDARY
L2 3 4 3.5m
*MAGNETIC COUPLING
K12 L1 L2 0.2500
.ENDS
```

```
*Output Filter*

D2 8 10 DMBR150RL
C4 10 9 1m IC=0
R4 10 11 1.2
C7 11 9 100n IC=0
RL 11 9 100
Q1 12 11 10 D2N2907
X4 12 11 D1N4623
.SUBCKT D1N4623 4 2
.MODEL DHIGH  D (
+IS=1E-7 RS=9.11 N=4.989)
.MODEL DLO  D (IS=3.1E-7 RS=1.5K
+N=14.589)
.MODEL DF  D (IS=1.76E-13
+RS=1.638M N=1.18 CJO=296.3P
+VJ=.547 M=.294)
V1 1 4 3.281
D2 2 3 DLO
V3 3 4 1.916
D3 4 2 DF
D1 2 1 DHIGH
.ENDS
R3 12 9 200
R5 12 13 100
RB 9 0 1T

*Optocoupler Isolator*

Vo 13 14 0
Ro 14 0 1m

*NCP1011 Output*

Vp 7 0 PULSE(0 339.4 0ms 20ns 10ns 5us 10us)
S1 6 0 7 0 Smod
.MODEL Smod VSWITCH(Ron=22 Roff=1MEG Von=339.4V Voff=0V)

.MODEL D1N4007GP  D (
+   IS =  6.698e-07
+   RS =  0.04255
+   CJO =  1.949e-11
+   VJ =  0.3909
+   TT =  4.933e-06
+   M =  0.3577
+   BV =  1000
+   N =  2.412
+   EG =  1.11
+   XTI =  3
+   KF =  0
+   AF =  1
+   FC =  0.5
+   IBV =  0.005177
+   TNOM =  27
+ )

.MODEL DMUR160  D (
+IS=1.08U
+RS=55.5M
+N=2.59
+BV=800
```

```
+IBV=5U
+CJO=15.7P
+VJ=.75
+M=.310
+TT=108N
+ )

.MODEL DMBR150RL  D (
+IS=6.47666e-09
+RS=0.184739
+N=0.832706
+EG=0.673879
+XTI=0.05
+BV=50
+IBV=0.0001
+CJO=2.81635e-10
+VJ=0.4
+M=0.559152
+FC=0.5
+TT=0
+KF=0
+AF=1
+ )

.MODEL D2N2907  PNP (
+IS=1.1p
+BF=200
+NF=1.2
+VAF=50
+IKF=0.1
+ISE=13p
+NE=1.9
+BR=6
+RC=0.6
+CJE=23p
+VJE=0.85
+MJE=1.25
+TF=0.5n
+CJC=19p
+VJC=0.5
+MJC=0.2
+TR=34n
+XTB=1.5
+ )

.END
```

Appendix D – Related Patent

When first approaching the project, and occasionally throughout the process, the team searched journals and patents for any possible insight that might be had there. While largely coming up empty, in the final month of the project the team happened upon United States Patent 6,339,314, a *Battery Charger Circuit with Low Standby Power Dissipation*. The patent, presented here over the next 8 pages, lists Gert W. Bruning as inventor and Philips Electronics as assignee and address the same problem of no-load waste current in battery charging AC adapters.

The patent describes a similar polling solution to ours, vaguely referencing load detection and timing circuitry. Interestingly, all of this added solution circuitry is placed on the AC side of the adapter, including the current-sensing subcircuit. The team feels that this puts too much reliance on predictable transformer performance. Additionally, the team discovered over the course of the project that the apparent input current is not always accurate or easily measured, and believes sensing the current at the output logically results in a value much closer to what is actually being sourced to the load. Therefore, while it was interesting to find another effort made previously to solve the same problem, the team considers their solution more complete and efficient.

US006339314B1

(12) **United States Patent**
Bruning

(10) **Patent No.: US 6,339,314 B1**
(45) **Date of Patent: Jan. 15, 2002**

(54) **BATTERY CHARGER CIRCUIT WITH LOW STANDBY POWER DISSIPATION**

(75) Inventor: **Gert W. Bruning**, Briarcliff Manor, NY (US)

(73) Assignee: **Philips Electronics North America Corporation**, New York, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/749,712**

(22) Filed: **Dec. 27, 2000**

(51) **Int. Cl.**[7] **H02J 7/00**
(52) **U.S. Cl.** **320/128**
(58) **Field of Search** 320/108, 122, 320/128; 307/30, 38, 126, 112

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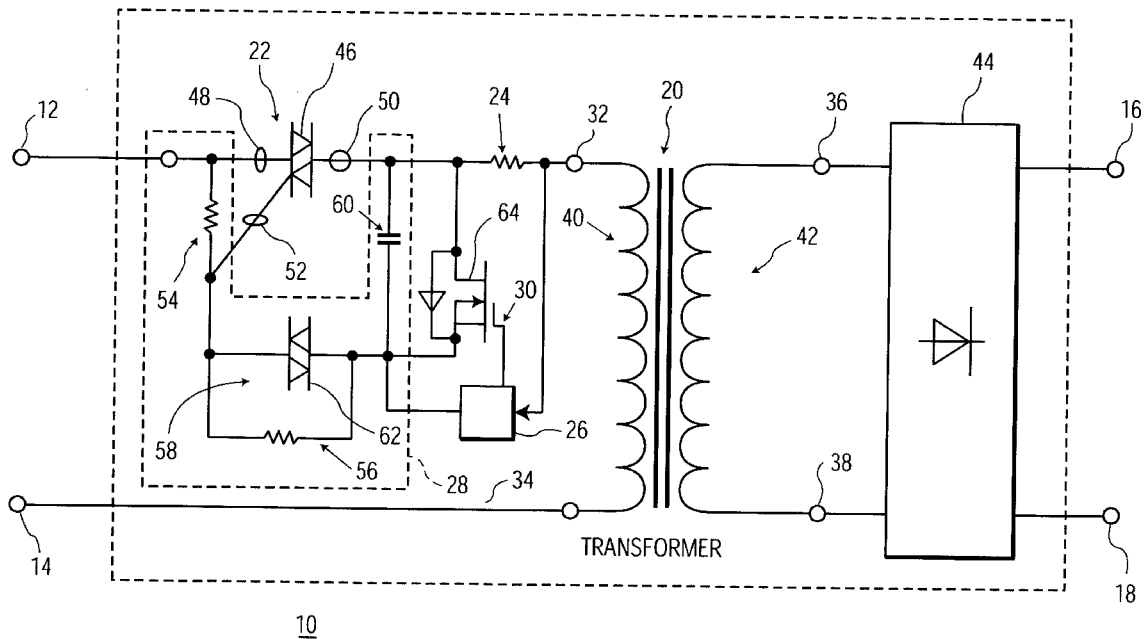
* cited by examiner

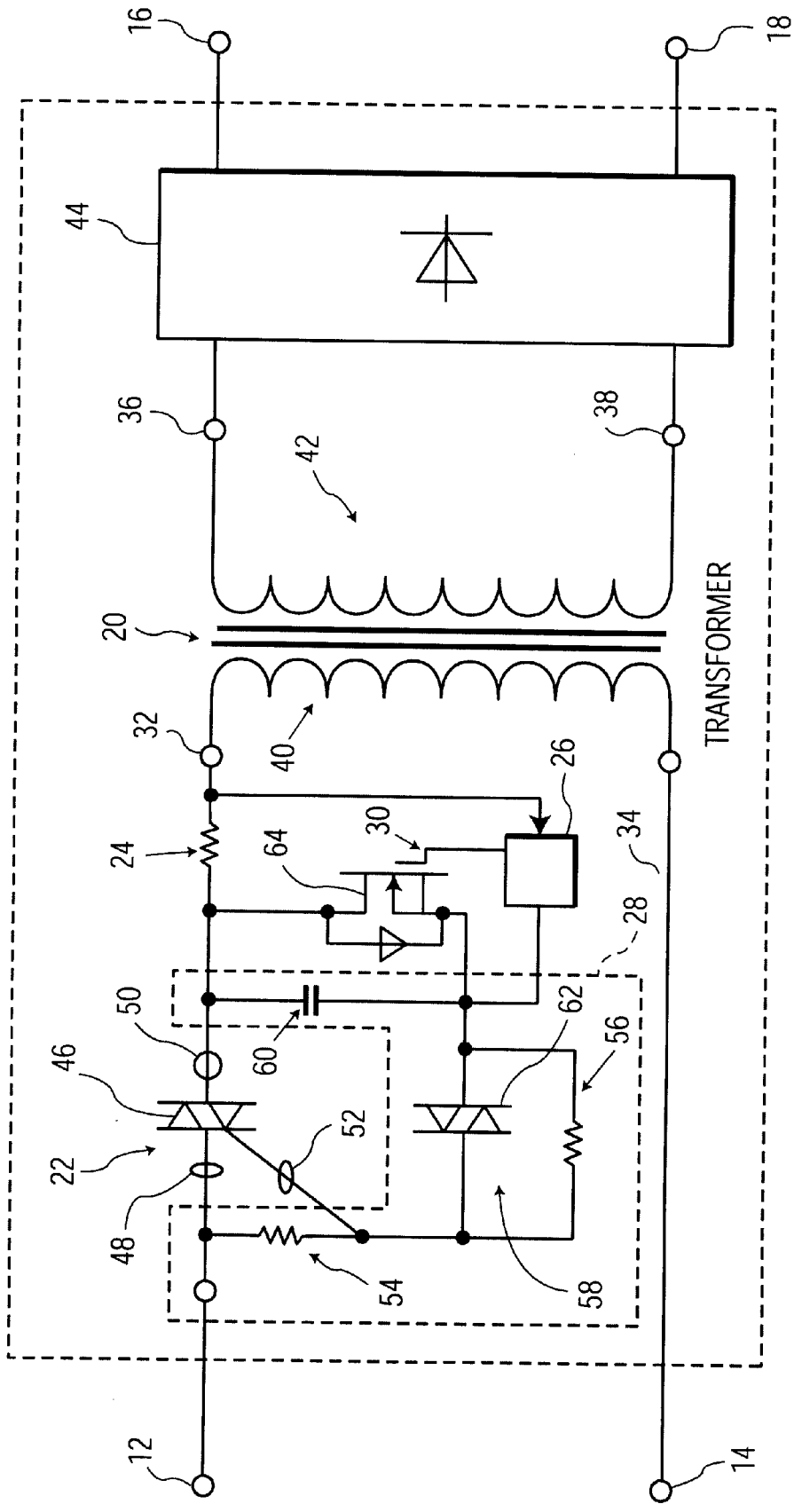
Primary Examiner—Peter S. Wong
Assistant Examiner—Pia Tibbits
(74) *Attorney, Agent, or Firm*—Dicran Halajian

(57) **ABSTRACT**

The invention concerns an electronic circuit for reducing the current consumption of a transformer (**1**). This circuit comprises a control circuit in the secondary circuit of the transformer (**1**) and a switch (**2**), controlled by the control circuit, in the primary circuit of the transformer (**1**) for separating the primary circuit of the transformer (**1**) from the power supply (**3**). The control circuit comprises a detector (**6**) for detecting the no-load state of the transformer (**1**). If the transformer (**1**) is in the no-load state, the switch (**2**) on the primary side is opened at least temporarily.

27 Claims, 2 Drawing Sheets

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52
22
48
54
58
10
12
14

FIG. 1

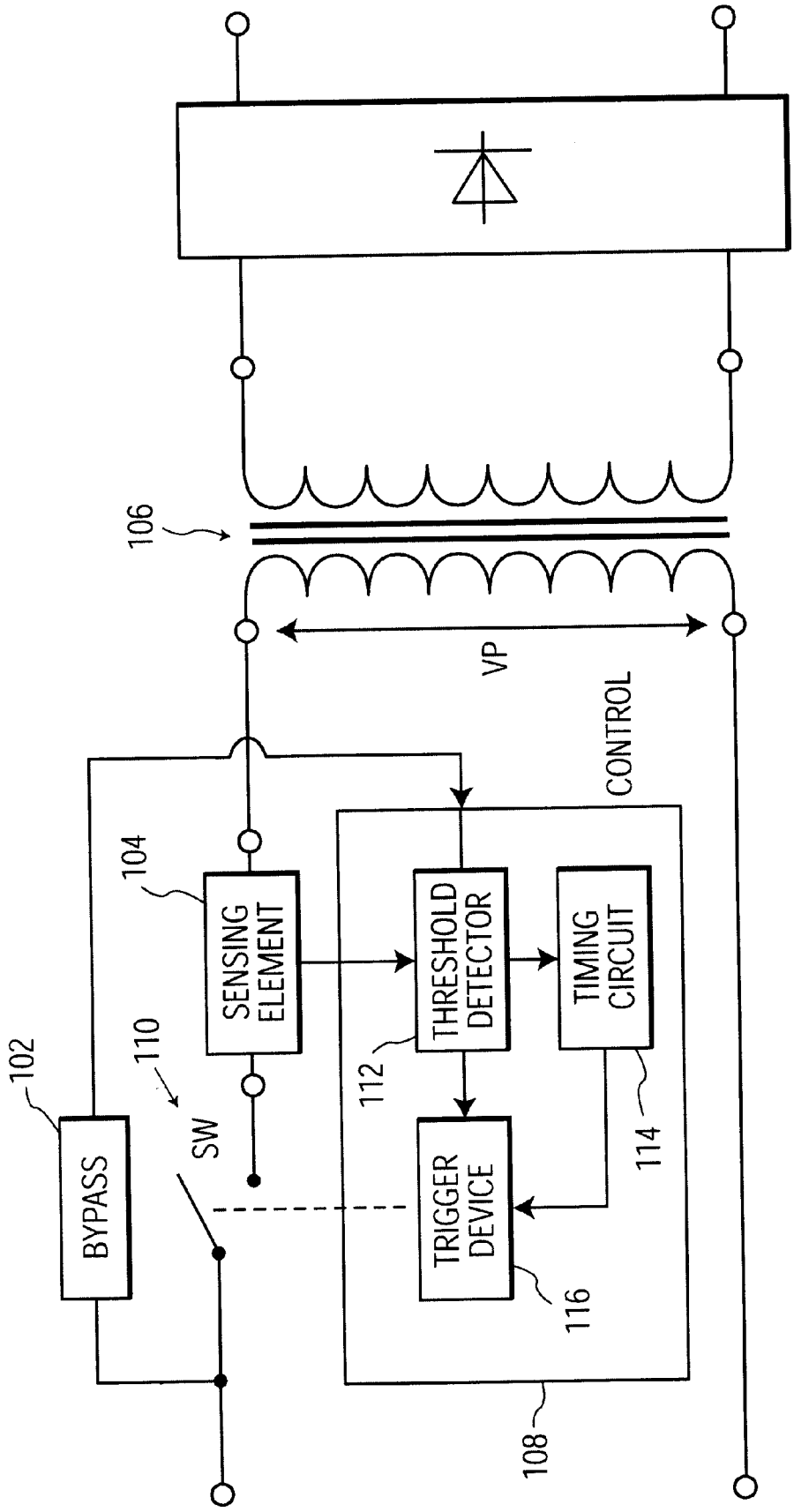
106
VP
CONTROL
104
SENSING ELEMENT
THRESHOLD DETECTOR
TIMING CIRCUIT
102
110
SW
BYPASS
112
114
TRIGGER DEVICE
116
108
100

FIG. 2

BATTERY CHARGER CIRCUIT WITH LOW STANDBY POWER DISSIPATION

FIELD OF THE INVENTION

The present invention relates generally to a battery charger circuit, and, more particularly, to a circuit arrangement to reduce standby current.

BACKGROUND OF THE INVENTION

Battery chargers for electric shavers, mobile phones, fax machines, cordless phones, and other electronic devices generally include a relatively simple, low cost, low frequency (i.e., 50/60 Hz) transformer circuit. Typically, the transformer circuit has a simple diode rectifier at the output of a secondary winding. Although this type of transformer circuit may be adequate for certain applications, these transformer circuits consume a considerable amount of electrical energy without a load being coupled to the output. This condition is usually referred to as standby.

The consumption of electrical energy during standby results from the non-ideal input characteristics of the transformer (i.e., magnetizing inductance) that permit magnetizing current to flow in a primary winding of the transformer circuit when connected to a power source. This magnetizing current flows through the primary winding of the transformer and also induces magnetic flux within the iron core of the transformer, both of which usually have power losses. In a typical situation, the losses of a transformer circuit during standby may exceed one (1) watt of power.

To prevent this standby loss, battery charger circuits have been developed with common high frequency inverter circuits. These circuits often utilize sophisticated integrated control circuits which can reduce power consumption during standby. However, these battery charger circuits are relatively expensive and have limited consumer acceptance.

SUMMARY OF THE INVENTION

The present invention provides a relatively simple, low cost battery charger circuit to reduce power consumption during standby. The battery charger circuit controls the current supplied to a transformer. The battery charger circuit determines the magnitude of the value of the current flowing to a primary winding of the transformer. When the value of the primary current includes a load current and a magnetizing current, the battery charger circuit continues to supply current to the primary winding of the transformer to charge the load. When the value of the primary current only includes a magnetizing current, the primary current is prevented from flowing to the transformer for a pre-set time or interval. Accordingly, the magnetizing current only flows to the primary winding of the transformer for a relatively short period of time, thereby reducing power consumption during standby.

A battery charger circuit in accordance with the present invention includes a switching element in series with a primary winding of a transformer. Control circuitry renders the switching element conductive during an on period so as to produce a current through the series arrangement and renders the switching element non-conductive during an off period.

Another battery charger circuit in accordance with the present invention includes a triggerable electronic switch to provide charging current when a load is present and to shut off the charging current when there is no load. A threshold detector is coupled to the triggerable electronic switch to trigger the triggerable electronic switch when the voltage of the threshold detector reaches a predetermined value.

Another battery charger circuit in accordance with the present invention includes a triggerable electronic switch having a gate terminal and first and second terminals through which an alternating current is supplied. The triggerable electronic switching allows current to flow to the transformer when there is a load and prevents current from flowing to the transformer when there is no load. A sensing element is coupled between the second terminal of the triggerable electronic switch and a primary winding of the transformer, and a capacitive element is coupled to the second terminal of the triggerable electronic switch. An input of the threshold detector is coupled to the gate of the triggerable electronic switch to allow current to flow to the gate terminal of the triggerable electronic switch at a predetermined voltage of the capacitive element. A load detector circuit is coupled to the sensing resistor. A switching element allows the capacitive element to be charged when a first current is sensed by the load detection circuit and to prevent the capacitive element from charging when a second current is sensed by the load detection circuit.

A method in accordance with the present invention includes the steps of providing current to charge a capacitive element, rendering a threshold switch conductive when the voltage of the capacitive element reaches a predetermined voltage to supply a latching current through threshold switch, and rendering a triggerable electronic switch conductive in response to the latching current to provide a primary current. The method also includes the steps of sensing the primary current at predetermined intervals to determine whether there is a load, maintaining the triggerable electronic switch in a conductive position when the value of the primary current includes a load current plus a magnetizing current, and opening the triggering electronic switch to interrupt the primary current for a predetermined interval when the value of the primary current only consists of the magnetizing current.

Another method in accordance with the present invention includes the steps of defining a current path in series with a first winding of a transformer, and sensing current flowing through the current path. The method also includes the steps of allowing the current to flow to the first winding when the current includes a load current and a magnetizing current, and preventing the current from flowing to the first winding when the current includes only a magnetizing current.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

The invention, together with attendant advantages, will be best understood by reference to the following detailed description of the preferred embodiment of the invention, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of an embodiment of a battery charger circuit accordance with a preferred embodiment of the present invention; and

FIG. **2** is a schematic diagram of another embodiment of a battery charger circuit accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

Before explaining the present embodiments in detail, it should be understood that the invention is not limited in its

application or use to the details of construction and arrangement of parts illustrated in the accompanying drawings and description. It will be recognized that the illustrative embodiments in accordance with the invention may be implemented or incorporated in other embodiments, variations and modifications, and may be practiced or carried out in various ways. Furthermore, unless otherwise indicated, the terms and expressions employed herein have been chosen for the purpose of describing the illustrative embodiments of the present invention for the convenience of the reader and are not for the purpose of limitation.

Referring now to the drawings, and more particularly to FIG. **1**, a schematic diagram of an embodiment of a battery charger circuit **10** is illustrated. The battery charger circuit **10** controls the supply of current to reduce power dissipation during standby. The battery charger circuit **10** generally includes input terminals **12**, **14**, output terminals **16**, **18**, a transformer **20**, a triggerable electronic switch **22**, a sensing element **24**, a load or current sensing circuit **26**, a triggering circuit **28**, and a switching element **30**.

The input terminals **12**, **14**, of the battery charger circuit **10** are connected to a power supply or reference source (not shown). The power supply provides primary or charging current to the transformer **20**. The power supply can be an alternating voltage source having an AC line voltage of 120 volts and a frequency of 60 hertz or an AC line voltage of 230 volts and a frequency of 50 hertz. It will be recognized that the power supply can be any suitable power source to provide power to the battery charger circuit **10**.

The transformer **20** of the battery charger circuit **10** has two input terminals **32**, **34** and two output terminals **36**, **38**. The input terminals **32**, **34** of the transformer **20** are connected to a primary winding or inductive element **40**, and the output terminals **36**, **38** are connected to a secondary winding or inductive element **42**. When current flows through the primary winding **40**, a voltage is induced in the secondary winding **42** to supply an output current to a load (not shown), such as, a battery, to be charged. The output terminals **36**, **38** of the transformer are preferably coupled to the load output by an output rectifier circuit or diode rectifier **44**. The positive terminal of the load can be connected to the terminal **16** of the charger circuit **10** and the negative terminal of the load can be connected to the terminal **18** of the charger circuit **10**.

The triggerable electronic switch **22** of the battery charger circuit **10** controls current supplied to the transformer **20**. For example, when the triggerable electronic switch **22** is in an "on" state (closed) or conductive state, current will flow to the primary winding **40** of the transformer **20**. When the triggerable electronic switch **22** is in an "off" state (open) or non-conductive state, current will be prevented from flowing to the transformer **20**. The triggerable electronic switch **22** preferably includes a bi-directional switch or triac **46** having a first main electrode **48**, a second main electrode **50**, and a gate electrode **52**. The first main electrode **48** of the triac **46** is connected to the input terminal **12** of the battery charger circuit **10** and the second main electrode **50** is connected to the sensing element **24**. The gate electrode **52** of the triac is connected to the input terminal **12** via a resistive element **54** of the triggering circuit **28**.

The gate electrode **52** controls the switching or conduction (i.e., firing) of the triac **46**. When the current supplied to the gate electrode **52** reaches a predetermined value (i.e., a latching current), the triac **46** turns "on" (closes) or conducts permitting current to flow through the triac **46** to the sensing element **24**. The triac will remain on as long as the current flowing into the gate electrode remains above a predetermined value to sustain conduction of the triac (i.e., a holding current). When the level of the current in the gate electrode decreases below the holding current, the triac turns "off" (non-conductive). The firing angle, that is, the angle between 0 and 180 degrees at which the triac first conducts, can be adjusted or controlled by the triggering circuit **28**.

The triggering circuit **28** of the battery charging circuit **10** triggers or fires the triac at an arbitrary selected angle for phase conduction. The triggering circuit **28** preferably includes resistive elements **54**, **56**, a threshold device **58**, and a capacitor element **60**. One end of the resistive element **54** is connected to the input terminal **12** of the battery charger circuit **10** and the other end of the resistive element **54** is connected to the gate electrode **52** of the triac **46**. One end of the resistive element **56** is connected to the gate electrode **52** of the triac **46** and the other end of the resistive element **56** is connected to the capacitive element **60**.

The capacitive element **60** of the triggering circuit **28** supplies current to the gate electrode **52** of the triac **46** to fire the triac. Preferably, the capacitive element includes a capacitor. One end of the capacitive element **60** is connected to the second main electrode **50** of the triac **46** and the other end of the capacitive element is connected to a node or junction formed between the resistive element **56** and the threshold device **58**. When power is supplied to the input terminals **12**, **14** of the battery charger circuit **10**, the capacitive element **60** charges through the serial combination of resistive elements **54** and **56**. Once the voltage of the capacitive element **60** reaches a predetermined valve, the threshold device **58** turns "on" (closes) or conducts.

The threshold device **58** of the triggering circuit **28** controls the triggering of the triac **46** by providing current to the gate electrode **52** of the triac **46**. One end of the threshold device **58** is connected to the gate electrode **52** of the triac **46** and the other end of the threshold device **58** is connected to a node formed between the resistive element **56** and the capacitive element **60**. Preferably, the threshold device **58** is a diac **62**. When the voltage on the capacitive element **60** reaches a breakdown voltage of the diac **62**, the diac **62** turns "on" (closes) to allow current (i.e., a latching current) to be supplied through diac **62** to the gate electrode **52** of the triac **46**.

The switching element **30** of the battery charger circuit **10** controls the activation of the triggering circuit **28** in order to supply current to the primary winding **40** of the transformer **20**. The switching element **30** preferably includes a transistor **64** having an emitter, a collector and a base. The transistor **64** is preferably a MOSFET transistor. The collector of the transistor **64** is connected to the sensing element **24**, and the emitter of the transistor **64** is connected to a node formed between the resistor **56**, the triggerable element **58**, and the capacitive element **60**. The gate of the transistor **64** is connected to the load sensing circuit **26**.

The load detection circuit **26** of the battery charger circuit **10** senses or measures the magnitude of the value of the primary current flowing through the sensing element **24** at predetermined times or intervals (i.e., 0.01% duty cycle) to detect whether a load is connected to the output terminals **16**, **18** of the battery charging circuit **10**. If the value of the primary current includes a load current plus a magnetizing current, the load detection circuit **26** opens the switching element **30** to cause the triggerable electronic switch to turn "on" (close) or conduct since a load is detected to be charged. If the value of the primary current only includes a magnetizing current, the load detection circuit **26** turns "on"

(closes) the switching element **30** to prevent the triggering circuit **28** from firing or closing the triggerable electronic switch **22** since there is no load to be charged. When there is no load, the load detection circuit **26** maintains the switching element **30** in a conductive position for the pre-set interval. Thereafter, the load detection circuit **26** senses the magnitude of the value of the primary current flowing through the sensing element **24** and, depending on the magnitude, causes the triggerable electronic switch **22** to be conductive or non-conductive to control the current to the transformer **20**. The load detection circuit **26** can include a voltage comparator, a current difference detection circuit, a timing circuit and/or other suitable circuits known by those skilled in the art for determining the current flowing through the sensing element **24** at predetermined times.

The operation of the battery charger circuit **10** will now be described with reference to FIG. **1**. Initially, the voltage across the capacitive element **60** is assumed to be zero with the diac **62** in its "off" state (non-conductive) so that the diac **62** is non-operative. The triac **46** is also "off" (non-conductive) and no current is flowing to the primary winding **40** of the transformer **20**. The switching element **30** is in its "off" state (non-conductive) to allow the capacitive element **60** to be charged. The current through the sensing element **24** is negligible and the voltage across the load is initially equally to zero.

During the positive half wave cycle of the supply voltage and as long as the triac **46** is not yet conducting, current flows through resistive elements **54, 56** to charge the capacitive element **60**. When the voltage of the capacitive element **60** reaches a breakover or breakdown voltage of the diac **62**, the diac breaks downs and switches to its "on" (closed) or conductive state. During the breakdown voltage, the capacitive element **60** discharges causing current to flow through the diac **62** and into the gate electrode **52** of the triac **46**. The current supplied to the gate electrode **52** causes the triac **46** to fire (i.e., conduct) allowing alternating current to flow through the sensing element **24** and into the primary winding **40** of the transformer **20**.

Near or at the end of the positive half wave cycle, the level of the current flowing into the gate electrode **52** of the triac **46** will not be adequate to sustain conduction of the triac **46** and the triac turns "off" (non-conductive). This can occur at approximately the "zero crossing point" between alternate half cycles of the alternating voltage applied to the input terminals **12, 14** of the battery charger circuit **10**. A similar situation occurs in the negative half wave cycle, except that the gate current is generated once the voltage of the capacitor exceeds a negative breakdown voltage.

During the positive and negative half wave cycles, the load detection circuit **26** can sense the current flowing through the sensing element **24** at preset or predetermined intervals. Preferably, the load detection circuit **26** closes the switching element **30** at predetermined intervals and senses the current. When there is no load connected to the output terminals **16, 18** of the battery charging circuit **10**, the current sensed through the sensing element **24** by the load detection circuit **26** will only include magnetizing current. As a result, the load detection circuit **26** maintains the switching element **30** in an "on" state (closed) to prevent the diac **62** from firing the triac **46**. Thus, the triac will be switched off and no current will flow to the primary winding **40** of the transformer **20**. The triac **46** will not be triggered as long as the switching element **30** is conductive. After a pre-set interval, the load detection circuit **26** renders non-conductive the switching element **30** to allow the triggering circuit **28** to fire the triac **46** and senses the current flowing through the sensing element **24**.

When a load is connected to the output terminals **16, 18** of the battery charger circuit **10**, the current sensed through the sensing element **24** by the load detection circuit **26** will include a load current plus a magnetizing current. As a result, the load detection circuit **26** turns "off" or renders non-conductive the switching element **30** to allow the triggering circuit **28** to fire the triac **46**. The triac **46** will continue to be fired as long as the switching element **30** is non-conductive. After a predetermined time or period, the load detection circuit **26** closes the switching element and senses the current.

FIG. **2** illustrates a schematic diagram of another embodiment of a battery charger circuit **100**. The battery charger circuit **100** controls the supply of current to reduce power dissipation during standby. The battery charger circuit **100** includes a bypass device **102**, a sensing element **104**, a transformer **106**, control circuitry **108**, and a switching element **110**.

The switching element **110** of the battery charger circuit **100** controls current supplied to the transformer **106**. When the switching element **110** is in an "on" state (closed) or conductive state, current will flow to the primary winding of the transformer **106**. When the switching element **110** is in an "off" state (open) or non-conductive state, current will be prevented from flowing to the transformer **106**. The switching element **110** can include any suitable switch, such a transistor or triac.

The bypass device **102** of the battery charger circuit **100** energizes or activates the control circuitry **108** when the switching element **110** is non-conductive. The bypass device **102** can include a resistor, a capacitor, an inductor, or a combination thereof.

The control circuitry **108** controls the triggering of the switching element **110**. When there is no load, the control circuitry **108** maintains the switching element **110** in a conductive position for a pre-set interval. Thereafter, the control circuitry **108** senses the magnitude of the value of the primary current flowing through the sensing element **104** and causes the switching element **110** to conductive or non-conductive to control the current to the transformer **106**. The control circuitry **108** preferably includes a threshold detector **112**, a timing circuit **114**, and a trigger device **116**.

The threshold detector **112** of the control circuitry **108** senses or measures the magnitude of the value of the primary current flowing through the sensing element **104** to detect whether a load is connected to the battery charging circuit **110**. If the value of the primary current includes a load current plus a magnetizing current, the threshold detector **112** causes the trigger device **116** to close the switching element **110**. If the value of the primary current only includes a magnetizing current, the threshold detector **112** causes the trigger device **116** to open the switching element **110** or prevents the closing of the switching element **110** since there is no load to be charged. The threshold detector **112** can include a comparator circuit with a threshold generator or any other suitable integrated circuit. The triggering device **116** can include a diac device with a capacitor, a gate driver, or any other suitable device.

The timing circuit **110** triggers the control circuitry **108** at predetermined intervals to check for the presence of the load current. The timing circuit can include a R-C time constant timer circuit, a digital counter, or any other suitable timing circuit. The sensing element **104** of the battery charger circuit can include a resistor, a coil, a resistive element or trace, a suitable integrated circuit, or other suitable sensing element.

The battery charger circuits described herein are a relatively simple, low cost circuits that reduce power consumption during standby. The battery charger circuits control the current supplied to the primary winding of a transformer. The battery charger circuits can determine the magnitude of the value of the current flowing to the primary winding of the transformer. When the value of the primary current includes a load current and a magnetizing current, the battery charger circuits continue to supply current to the primary winding of the transformer to charge the load. When the value of the primary current only includes a magnetizing current, the primary current is prevented from flowing to the transformer for a pre-set time or interval. Therefore, the magnetizing current only flows to the primary winding of the transformer for a relatively short period of time, thereby reducing power consumption during standby.

Although the battery charger circuits have been described in detail by way of illustration and example, it should be understood that a wide range of changes and modifications can be made to the preferred embodiments described above without departing in any way from the scope and spirit of the present invention. Thus, the described embodiment is to be considered in all aspects only as illustrative and not restrictive, and the scope of the invention is, therefore, indicated by the appended claims rather than the foregoing description. All changes that come within the meaning and range of equivalency of the claims are to be embraced within their scope.

I claim:

1. A battery charger circuit for controlling a current through a primary winding of a transformer comprising:

a triggerable electronic switch having a gate terminal and first and second terminals through which an alternating current is supplied, the triggerable electronic switching allowing current to flow to the transformer when there is a load and preventing current from flowing to the transformer when there is no load;

a sensing element coupled between the second terminal of the triggerable electronic switch and the primary winding of the transformer;

a capacitive element coupled to the second terminal of the triggerable electronic switch;

a threshold detector having an input and an output, the input of the threshold detector coupled to the gate terminal of the triggerable electronic switch to allow current to flow to the gate terminal of the triggerable electronic switch at a predetermined voltage of the capacitive element;

a load detector circuit coupled to the sensing element to sense the current flowing through the sensing element; and

a switching element to allow the capacitive element to be charged when a first current is sensed by the load detection circuit and to prevent the capacitive element from charging when a second current is sensed by the load detection circuit.

2. The battery charger circuit of claim **1**, wherein the triggerable electronic switch comprises one of a triac and a bi-directional switch.

3. The battery charger circuit of claim **1**, wherein the threshold detector comprises a diac.

4. The battery charger circuit of claim **1**, wherein the switching element comprises a transistor.

5. The battery charger circuit of claim **1**, wherein the predetermined voltage is a breakdown voltage of the threshold detector.

6. The battery charger circuit of claim **1**, further comprising a resistor coupled to the gate terminal of the triggerable electronic switch and the in put of the threshold detector.

7. The battery charger circuit of claim **1**, further comprising a power supply to p provide current to the first terminal of the triggerable electronic switch.

8. The battery charger circuit of claim **1**, wherein the first current includes a load current and a magnetizing current and the second current only includes the magnetizing current.

9. A battery charger circuit comprising:

a transformer having a primary winding and a secondary winding;

a triggerable electronic switch to provide a charging current when a load is connected to the secondary winding and to shut off the charging current when the load is disconnected from the secondary winding;

a sensing element connected between the triggerable electronic switch and the primary winding; and

a threshold detector coupled to the sensing element to trigger the triggerable electronic switch to a conductive state when a voltage of the threshold detector reaches a predetermined value and to maintain said conductive state when a load current is flowing through said sensing element.

10. The battery charger circuit of claim **9**, wherein the triggerable electronic switch includes one of a triac switch and a bi-directional switch.

11. The battery charger circuit of claim **9**, wherein the threshold detector comprises a diac.

12. The battery charger circuit of claim **9**, further comprising a capacitive element coupled to the threshold detector.

13. The battery charger circuit of claim **9**, further comprising a switching element coupled to the threshold detector.

14. The battery charger circuit of claim **9**, further comprising a load detection circuit coupled to threshold detector.

15. A battery charger circuit comprising:

a switching element;

a sensing element connected in series between the switching element and a primary winding of a transformer; and

a control circuitry for rendering the switching element conductive when a load current is flowing through the sensing element and for rendering the switching element non-conductive when the load current is not flowing through the sensing element.

16. The battery charger circuit of claim **15** further comprising a bypass device coupled to the control circuitry.

17. The battery charger circuit of claim **15** wherein the control circuitry comprises a threshold detector.

18. The battery charger circuit of claim **15** wherein the control circuitry comprises a timing circuit.

19. The battery charger circuit of claim **15** wherein the control circuitry comprises a trigger device.

20. The battery charger circuit of claim **15** wherein the control circuitry comprises a threshold detector coupled to a triggering device and a timing circuit.

21. The battery charger circuit of claim **15**, wherein said load current is greater than a magnetizing current, said magnetizing current flowing through said primary winding when a load is not connected to a secondary winding of said transformer.

22. A method of charging a load comprising:

providing current to charge a capacitive element;

rendering a threshold switch conductive when a voltage of the capacitive element reaches a predetermined voltage to supply a latching current through the threshold switch;

rendering a triggerable electronic switch conductive in response to the latching current to provide a primary current in a primary winding of a transformer;

sensing the primary current at predetermined intervals to determine whether there is a load;

maintaining the triggerable electronic switch in a conductive position when the primary current includes a load current plus a magnetizing current; and

opening the triggering electronic switch to interrupt the primary current for a predetermined interval when the primary current only consists of the magnetizing current.

23. The method of claim **22** wherein the triggerable electronic switch is one of a triac switch and a bi-directional switch.

24. The method of claim **22** wherein the threshold detector comprises a diac.

25. The method of claim **22**, wherein said load current is greater than a magnetizing current, said magnetizing current flowing through said primary winding when the load is not connected to a secondary winding of said transformer.

26. A method to reduce standby current comprising:

defining a current path in series with a primary winding of a transformer;

sensing a current flowing through the current path;

allowing the current to flow to the primary winding when the current includes a load current and a magnetizing current; and

preventing the current from flowing to the primary winding when the current includes only a magnetizing current.

27. The method of claim **26**, wherein said load current is greater than a magnetizing current, said magnetizing current flowing through said primary winding when a load is not connected to a secondary winding of said transformer.

* * * * *

Appendix E – Datasheets

The following pages contain the datasheets of all major ICs referenced within this report. They are, in order:

NCP1011	Self-Supplied Monolithic Switcher for Low Standby-Power Offline SMPS
OPA344	Low Power, Single-Supply, Rail-to-Rail Operational Amplifiers
TLC27L2	Precision Dual Operational Amplifiers
LMV932	Operational Amplifiers with Rail-to-Rail Input and Output
ICM7555	General Purpose Timers
FQPF2P25	250V P-Channel MOSFET
MOC3023	Optocouplers/Optoisolators

NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

Self-Supplied Monolithic Switcher for Low Standby-Power Offline SMPS

The NCP101X series integrates a fixed−frequency current−mode controller and a 700 V MOSFET. Housed in a PDIP−7, PDIP−7 Gull Wing, or SOT−223 package, the NCP101X offers everything needed to build a rugged and low−cost power supply, including soft−start, frequency jittering, short−circuit protection, skip−cycle, a maximum peak current setpoint and a Dynamic Self−Supply (no need for an auxiliary winding).

Unlike other monolithic solutions, the NCP101X is quiet by nature: during nominal load operation, the part switches at one of the available frequencies (65 − 100 − 130 kHz). When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so−called skip−cycle mode and provides excellent efficiency at light loads. Because this occurs at typically 1/4 of the maximum peak value, no acoustic noise takes place. As a result, standby power is reduced to the minimum without acoustic noise generation.

Short−circuit detection takes place when the feedback signal fades away, e.g. in true short−circuit conditions or in broken Optocoupler cases. External disabling is easily done either simply by pulling the feedback pin down or latching it to ground through an inexpensive SCR for complete latched−off. Finally soft−start and frequency jittering further ease the designer task to quickly develop low−cost and robust offline power supplies.

For improved standby performance, the connection of an auxiliary winding stops the DSS operation and helps to consume less than 100 mW at high line. In this mode, a built−in latched overvoltage protection prevents from lethal voltage runaways in case the Optocoupler would brake. These devices are available in economical 8−pin dual−in−line and 4−pin SOT−223 packages.

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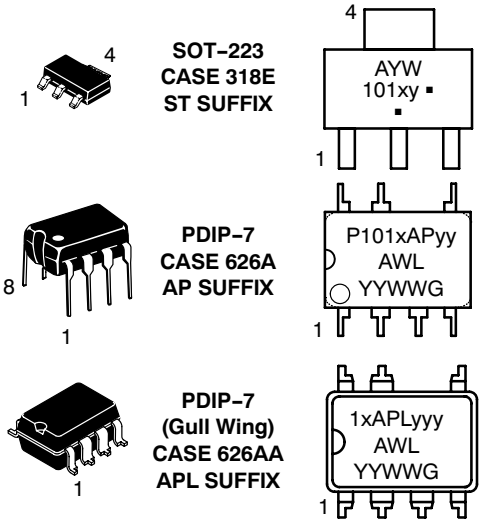
http://onsemi.com

MARKING DIAGRAMS



x = Current Limit (0, 1, 2, 3, 4)
y = Oscillator Frequency
A (65 kHz), B (100 kHz), C (130 kHz)
yy = 06 (65 kHz), 10 (100 kHz), 13 (130 kHz)
yyy = 065, 100, 130
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
▪ or G = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

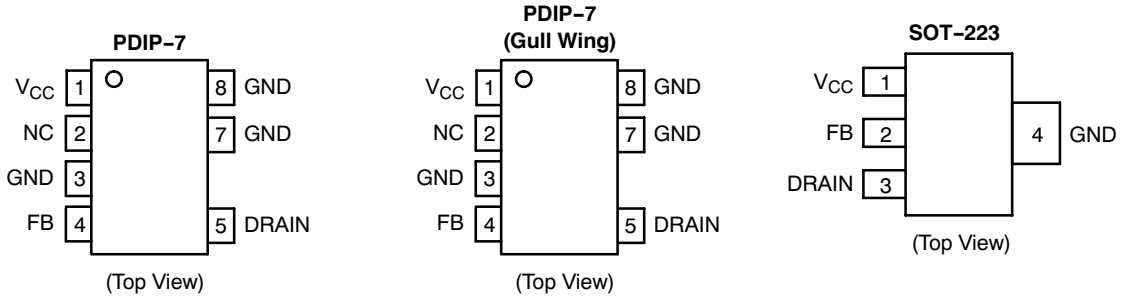
Features

- Built−in 700 V MOSFET with Typical R_{DSon} of 11 Ω and 22 Ω
- Large Creepage Distance Between High−Voltage Pins
- Current−Mode Fixed Frequency Operation: 65 kHz – 100 kHz - 130 kHz
- Skip−Cycle Operation at Low Peak Currents Only: No Acoustic Noise!
- Dynamic Self−Supply, No Need for an Auxiliary Winding
- Internal 1.0 ms Soft−Start
- Latched Overvoltage Protection with Auxiliary Winding Operation
- Frequency Jittering for Better EMI Signature
- Auto−Recovery Internal Output Short−Circuit Protection
- Below 100 mW Standby Power if Auxiliary Winding is Used
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient Analysis
- Pb−Free Packages are Available

Typical Applications

- Low Power AC/DC Adapters for Chargers
- Auxiliary Power Supplies (USB, Appliances,TVs, etc.)

PIN CONNECTIONS



Indicative Maximum Output Power from NCP1014

R_{DSon} − Ip	230 Vac	100 − 250 Vac
11 Ω − 450 mA DSS	14 W	6.0 W
11 Ω − 450 mA Auxiliary Winding	19 W	8.0 W

1. Informative values only, with: Tamb = 50°C, Fswitching = 65 kHz, circuit mounted on minimum copper area as recommended.

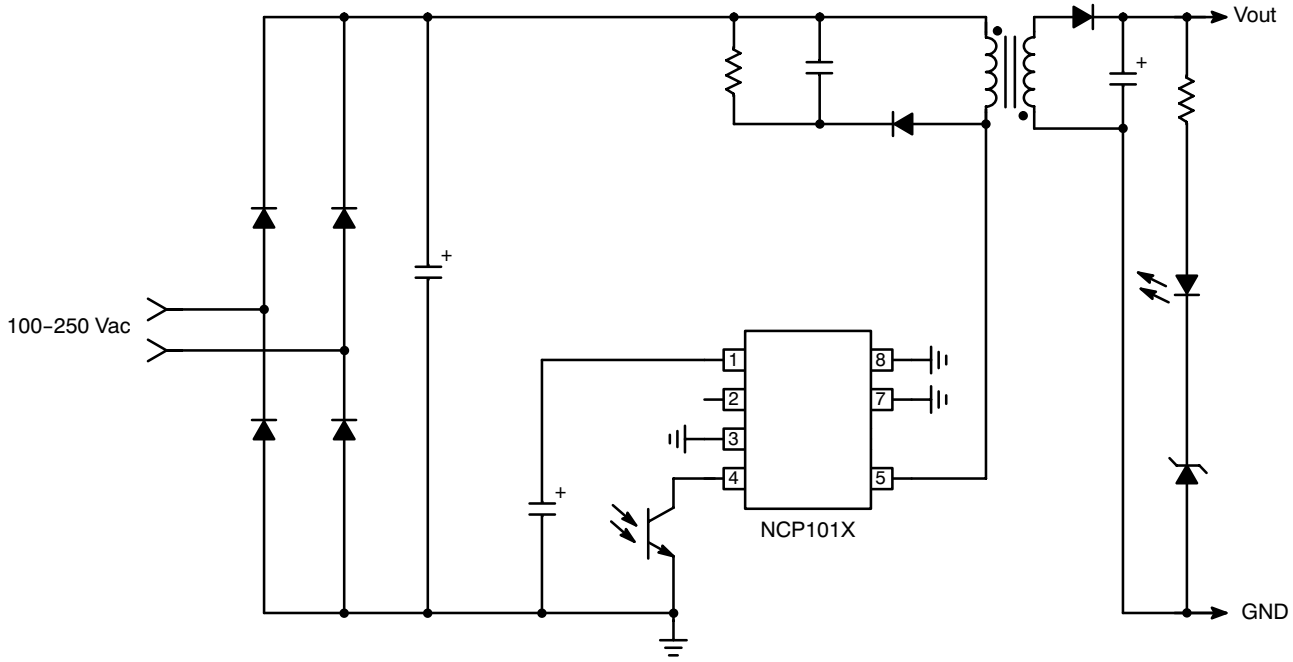


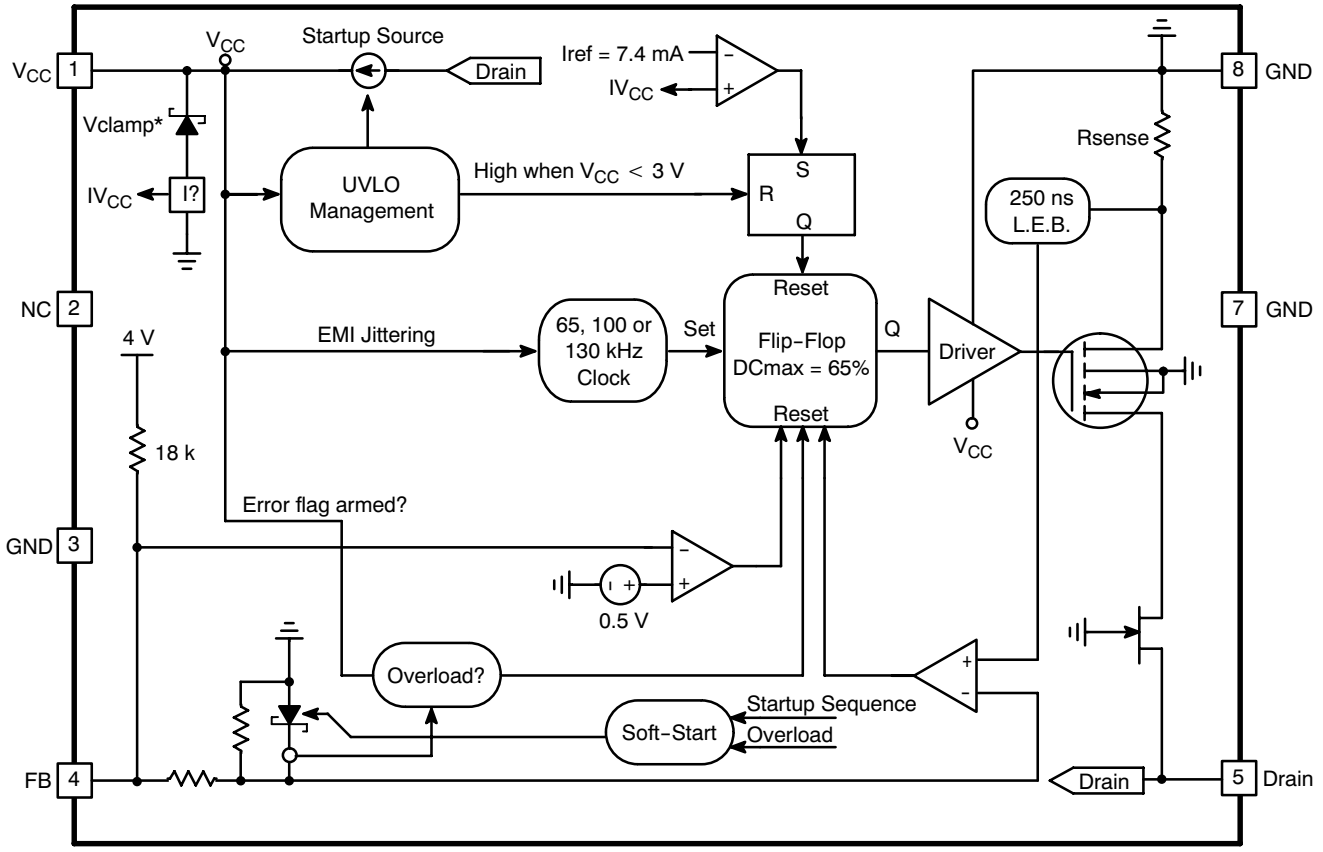
Figure 1. Typical Application Example

Quick Selection Table

	NCP1010			NCP1011			NCP1012			NCP1013			NCP1014	
R_{DSon} [Ω]	22						11							
Ipeak [mA]	100			250			250			350			450	
Freq [kHz]	65	100	130	65	100	130	65	100	130	65	100	130	65	100

PIN FUNCTION DESCRIPTION

Pin No. (SOT−223)	Pin No. (PDIP−7, PDIP−7/Gull Wing)	Pin Name	Function	Description
1	1	V_{CC}	Powers the Internal Circuitry	This pin is connected to an external capacitor of typically 10 μF. The natural ripple superimposed on the V_{CC} participates to the frequency jittering. For improved standby performance, an auxiliary V_{CC} can be connected to Pin 1. The V_{CC} also includes an active shunt which serves as an opto fail−safe protection.
−	2	NC	−	−
−	3	GND	The IC Ground	−
2	4	FB	Feedback Signal Input	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand.
3	5	Drain	Drain Connection	The internal drain MOSFET connection.
−	−	−	−	−
−	7	GND	The IC Ground	−
4	8	GND	The IC Ground	−



*Vclamp = VCC_{OFF} + 200 mV (8.7 V Typical)

Figure 2. Simplified Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage on all pins, except Pin 5 (Drain)	V_{CC}	−0.3 to 10	V
Drain Voltage	−	−0.3 to 700	V
Drain Current Peak during Transformer Saturation	$I_{DS(pk)}$		
NCP1010/11		550	mA
NCP1012/13/14		1.0	A
Maximum Current into Pin 1 when Activating the 8.7 V Active Clamp	I_V_{CC}	15	mA
Thermal Characteristics			°C/W
P Suffix, Case 626A			
Junction−to−Lead	$R_{\theta JL}$	9.0	
Junction−to−Air, 2.0 oz (70 μm) Printed Circuit Copper Clad	$R_{\theta JA}$		
0.36 Sq. Inch (2.32 Sq. Cm)		77	
1.0 Sq. Inch (6.45 Sq. Cm)		60	
PL Suffix (Gull Wing), Case 626AA			
Junction−to−Lead	$R_{\theta JL}$	11.9	
Junction−to−Air, 2.0 oz (70 μm) Printed Circuit Copper Clad	$R_{\theta JA}$		
0.36 Sq. Inch (2.32 Sq. Cm)		92	
1.0 Sq. Inch (6.45 Sq. Cm)		71	
ST Suffix, Plastic Package Case 318E			
Junction−to−Lead	$R_{\theta JL}$	14	
Junction−to−Air, 2.0 oz (70 μm) Printed Circuit Copper Clad	$R_{\theta JA}$		
0.36 Sq. Inch (2.32 Sq. Cm)		74	
1.0 Sq. Inch (6.45 Sq. Cm)		55	
Maximum Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	−	−60 to +150	°C
ESD Capability, Human Body Model (All pins except HV)	−	2.0	kV
ESD Capability, Machine Model	−	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, Max T_J = 150°C, V_{CC} = 8.0 V unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
V_{CC} Increasing Level at which the Current Source Turns−off	1	VCC_{OFF}	7.9	8.5	9.1	V
V_{CC} Decreasing Level at which the Current Source Turns−on	1	VCC_{ON}	6.9	7.5	8.1	V
Hysteresis between VCC_{OFF} and VCC_{ON}	1	−	−	1.0	−	V
V_{CC} Decreasing Level at which the Latch−off Phase Ends	1	VCC_{latch}	4.4	4.7	5.1	V
V_{CC} Decreasing Level at which the Internal Latch is Released	1	VCC_{reset}	−	3.0	−	V
Internal IC Consumption, MOSFET Switching at 65 kHz	1	ICC1	−	0.92	1.1 (Note 2)	mA
Internal IC Consumption, MOSFET Switching at 100 kHz	1	ICC1	−	0.95	1.15 (Note 2)	mA
Internal IC Consumption, MOSFET Switching at 130 kHz	1	ICC1	−	0.98	1.2 (Note 2)	mA
Internal IC Consumption, Latch−off Phase, V_{CC} = 6.0 V	1	ICC2	−	290	−	μA
Active Zener Voltage Positive Offset to VCC_{OFF}	1	Vclamp	140	200	300	mV
Latch−off Current NCP1012/13/14 NCP1010/11	1	ILatch	 6.3 5.8	 7.4 7.3	 9.2 9.0	mA
POWER SWITCH CIRCUIT						
Power Switch Circuit On−state Resistance NCP1012/13/14 (Id = 50 mA) T_J = 25°C T_J = 125°C NCP1010/11 (Id = 50 mA) T_J = 25°C T_J = 125°C	5	R_{DSon}	−	 11 19 22 38	 16 24 35 50	Ω
Power Switch Circuit and Startup Breakdown Voltage ($ID_{(off)}$ = 120 μA, T_J = 25°C)	5	BVdss	700	−	−	V
Power Switch and Startup Breakdown Voltage Off−state Leakage Current T_J = 25°C (Vds = 700 V) T_J = 125°C (Vds = 700 V)	 5 5	$I_{DS(OFF)}$	 − −	 50 30	 − −	μA
Switching Characteristics (RL = 50 Ω, Vds Set for Idrain = 0.7 x Ilim) Turn−on Time (90%−10%) Turn−off Time (10%−90%)	 5 5	 ton toff	 − −	 20 10	 − −	ns
INTERNAL STARTUP CURRENT SOURCE						
High−voltage Current Source, V_{CC} = 8.0 V NCP1012/13/14 NCP1010/11	1	IC1	 5.0 5.0	 8.0 8.5	 10 10.3	mA
High−voltage Current Source, V_{CC} = 0	1	IC2	−	10	−	mA
CURRENT COMPARATOR T_J = 25°C (Note 2)						
Maximum Internal Current Setpoint, NCP1010 (Note 3)	5	Ipeak (22)	90	100	110	mA
Maximum Internal Current Setpoint, NCP1011 (Note 3)	5	Ipeak (22)	225	250	275	mA
Maximum Internal Current Setpoint, NCP1012 (Note 3)	5	Ipeak (11)	225	250	275	mA
Maximum Internal Current Setpoint, NCP1013 (Note 3)	5	Ipeak (11)	315	350	385	mA
Maximum Internal Current Setpoint, NCP1014 (Note 3)	5	Ipeak (11)	405	450	495	mA
Default Internal Current Setpoint for Skip−Cycle Operation, Percentage of Max Ip	−	I_{Lskip}	−	25	−	%
Propagation Delay from Current Detection to Drain OFF State	−	T_{DEL}	−	125	−	ns
Leading Edge Blanking Duration	−	T_{LEB}	−	250	−	ns

2. See characterization curves for temperature evolution.
3. Adjust di/dt to reach Ipeak in 3.2 μsec.

ELECTRICAL CHARACTERISTICS (continued) (For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, Max T_J = 150°C, V_{CC}= 8.0 V unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
INTERNAL OSCILLATOR						
Oscillation Frequency, 65 kHz Version, T_J = 25°C (Note 4)	–	f_{OSC}	59	65	71	kHz
Oscillation Frequency, 100 kHz Version, T_J = 25°C (Note 4)	–	f_{OSC}	90	100	110	kHz
Oscillation Frequency, 130 kHz Version, T_J = 25°C (Note 4)	–	f_{OSC}	117	130	143	kHz
Frequency Dithering Compared to Switching Frequency (with active DSS)	–	f_{dither}	–	±3.3	–	%
Maximum Duty−cycle	–	Dmax	62	67	72	%
FEEDBACK SECTION						
Internal Pull−up Resistor	4	Rup	–	18	–	kΩ
Internal Soft−Start (Guaranteed by Design)	–	Tss	–	1.0	–	ms
SKIP−CYCLE GENERATION						
Default Skip Mode Level on FB Pin	4	Vskip	–	0.5	–	V
TEMPERATURE MANAGEMENT						
Temperature Shutdown	–	TSD	140	150	160	°C
Hysteresis in Shutdown	–	–	–	50	–	°C

4. See characterization curves for temperature evolution.

TYPICAL CHARACTERISTICS

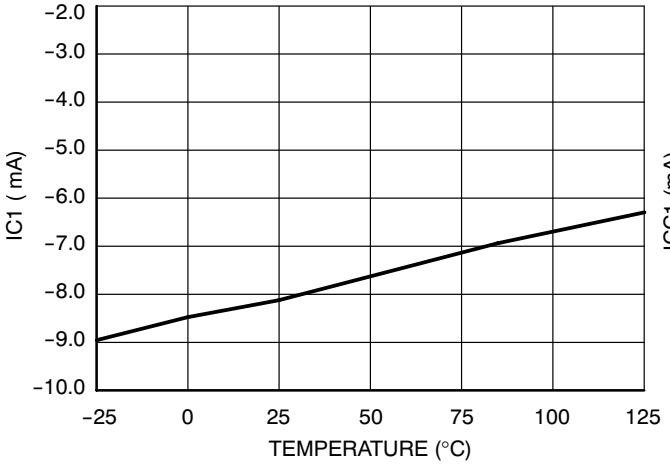


Figure 3. IC1 @ V_{CC} = 8.0 V, FB = 1.5 V vs. Temperature

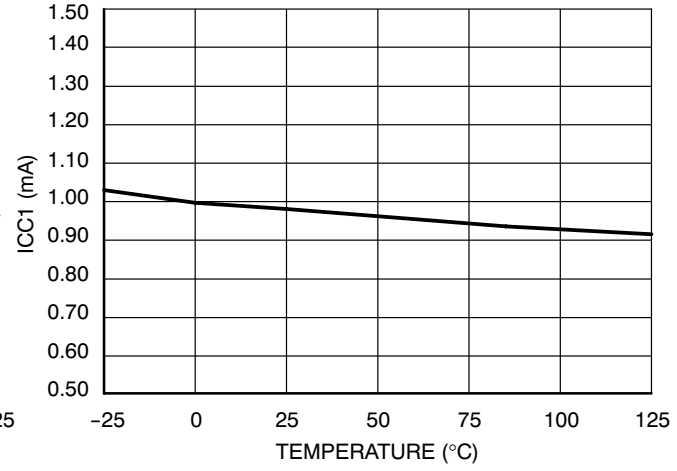


Figure 4. ICC1 @ V_{CC} = 8.0 V, FB = 1.5 V vs. Temperature

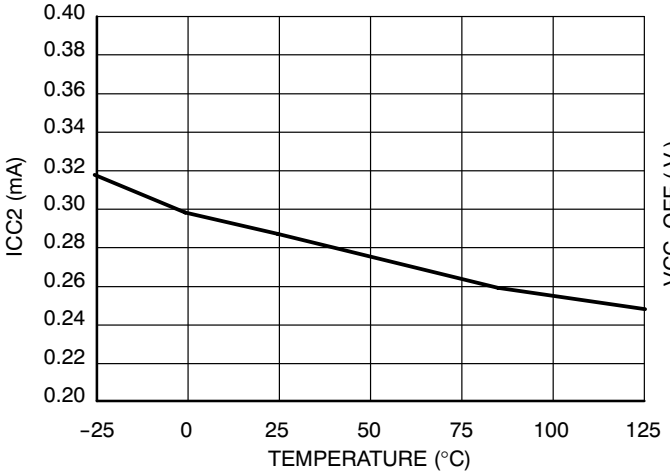


Figure 5. ICC2 @ V_{CC} = 6.0 V, FB = Open vs. Temperature

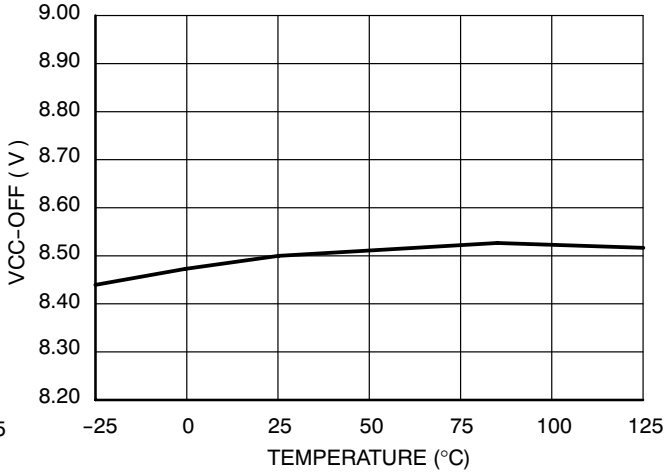


Figure 6. V_{CC} OFF, FB = 1.5 V vs. Temperature

TYPICAL CHARACTERISTICS

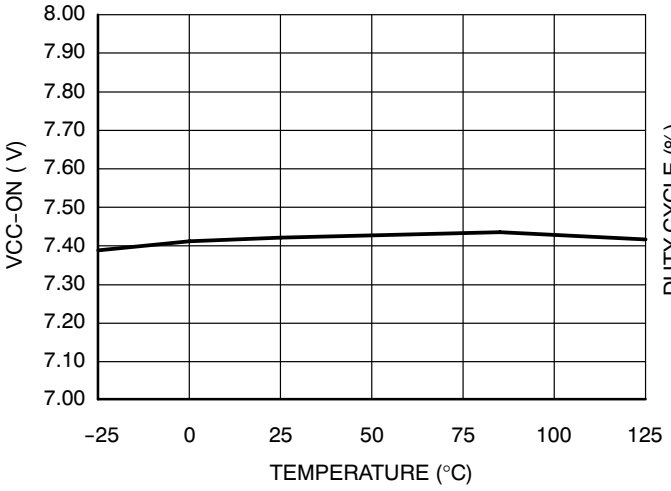


Figure 7. V_{CC} ON, FB = 3.5 V vs. Temperature

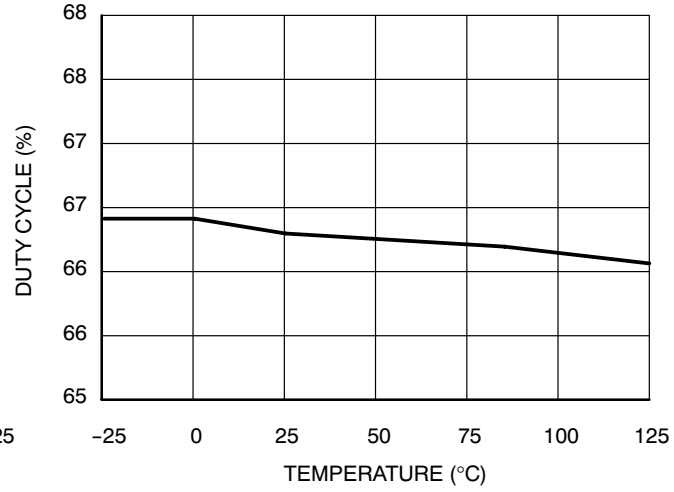


Figure 8. Duty Cycle vs. Temperature

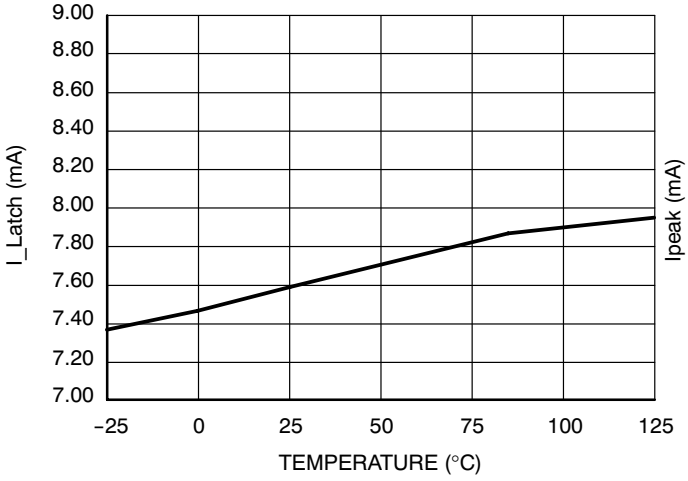


Figure 9. ILatch, FB = 1.5 V vs. Temperature

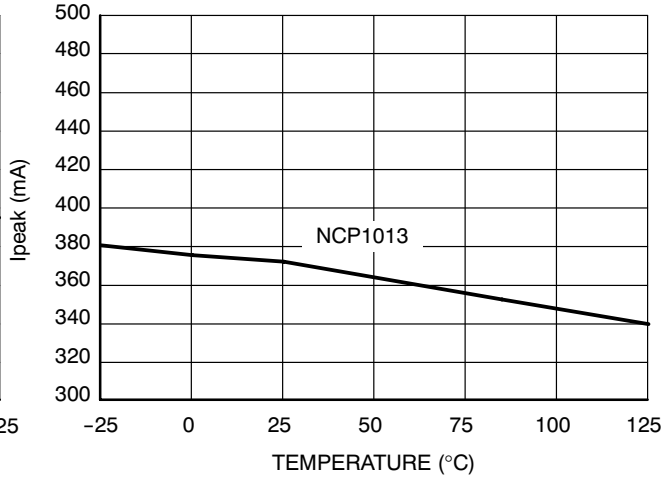


Figure 10. Ipeak−RR, V_{CC} = 8.0 V, FB = 3.5 V vs. Temperature

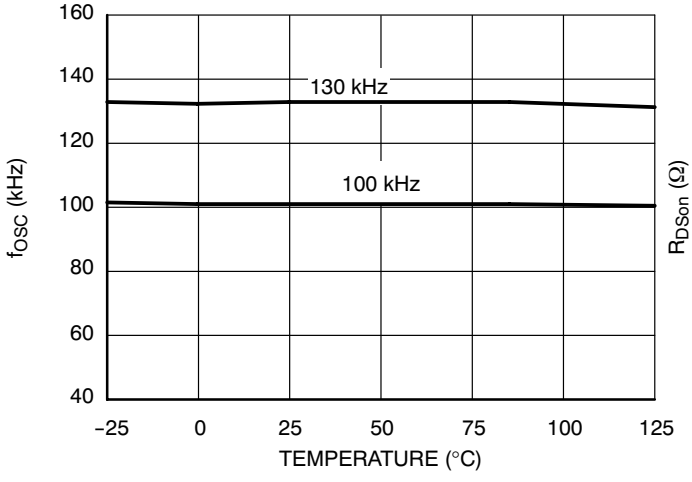


Figure 11. Frequency vs. Temperature

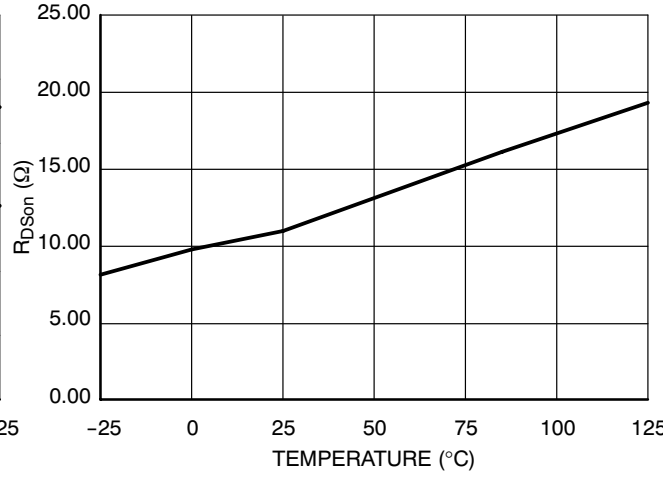


Figure 12. ON Resistance vs. Temperature, NCP1012/1013

APPLICATION INFORMATION

Introduction

The NCP101X offers a complete current−mode control solution (actually an enhanced NCP1200 controller section) together with a high−voltage power MOSFET in a monolithic structure. The component integrates everything needed to build a rugged and low−cost Switch−Mode Power Supply (SMPS) featuring low standby power. The Quick Selection Table on Page 2, details the differences between references, mainly peak current setpoints and operating frequency.

No need for an auxiliary winding: ON Semiconductor Very High Voltage Integrated Circuit technology lets you supply the IC directly from the high−voltage DC rail. We call it Dynamic Self−Supply (DSS). This solution simplifies the transformer design and ensures a better control of the SMPS in difficult output conditions, e.g. constant current operations. However, for improved standby performance, an auxiliary winding can be connected to the V_{CC} pin to disable the DSS operation.

Short−circuit protection: By permanently monitoring the feedback line activity, the IC is able to detect the presence of a short−circuit, immediately reducing the output power for a total system protection. Once the short has disappeared, the controller resumes and goes back to normal operation.

Fail−safe optocoupler and OVP: When an auxiliary winding is connected to the V_{CC} pin, the device stops its internal Dynamic Self−Supply and takes its operating power from the auxiliary winding. A 8.7 V active clamp is connected between V_{CC} and ground. In case the current injected in this clamp exceeds a level of 7.4 mA (typical), the controller immediately latches off and stays in this position until V_{CC} cycles down to 3.0 V (e.g. unplugging the converter from the wall). By adjusting a limiting resistor in series with the V_{CC} terminal, it becomes possible to implement an overvoltage protection function, latching off the circuit in case of broken optocoupler or feedback loop problems.

Low standby−power: If SMPS naturally exhibits a good efficiency at nominal load, it begins to be less efficient when the output power demand diminishes. By skipping unneeded switching cycles, the NCP101X drastically reduces the power wasted during light load conditions. An auxiliary winding can further help decreasing the standby power to extremely low levels by invalidating the DSS operation. Typical measurements show results below 80 mW @ 230 Vac for a typical 7.0 W universal power supply.

No acoustic noise while operating: Instead of skipping cycles at high peak currents, the NCP101X waits until the peak current demand falls below a fixed 1/4 of the maximum limit. As a result, cycle skipping can take place without having a singing transformer … You can thus select cheap magnetic components free of noise problems.

SPICE model: A dedicated model to run transient cycle−by−cycle simulations is available but also an averaged version to help close the loop. Ready−to−use templates can be downloaded in OrCAD's PSpice, and INTUSOFT's IsSpice4 from ON Semiconductor web site, NCP101X related section.

Dynamic Self−Supply

When the power supply is first powered from the mains outlet, the internal current source (typically 8.0 mA) is biased and charges up the V_{CC} capacitor from the drain pin. Once the voltage on this V_{CC} capacitor reaches the VCC_{OFF} level (typically 8.5 V), the current source turns off and pulses are delivered by the output stage: the circuit is awake and activates the power MOSFET. Figure 13 details the internal circuitry.

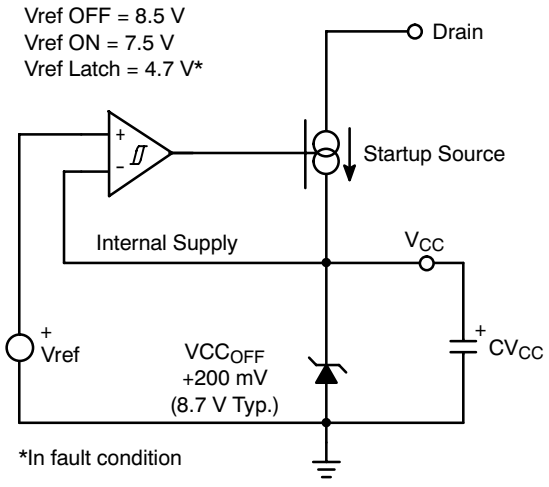


Figure 13. The Current Source Regulates V_{CC} by Introducing a Ripple

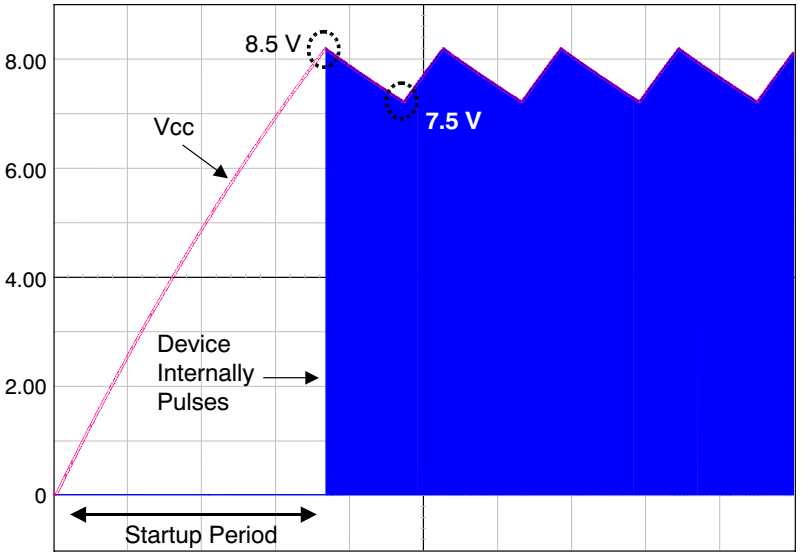


Figure 14. The Charge/Discharge Cycle Over a 10 μF V_{CC} Capacitor

The protection burst duty−cycle can easily be computed through the various timing events as portrayed by Figure 16.

Being loaded by the circuit consumption, the voltage on the V_{CC} capacitor goes down. When the DSS controller detects that V_{CC} has reached 7.5 V (VCC_{ON}), it activates the internal current source to bring V_{CC} toward 8.5 V and stops again: a cycle takes place whose low frequency depends on the V_{CC} capacitor and the IC consumption. A 1.0 V ripple takes place on the V_{CC} pin whose average value equals (VCC_{OFF} + VCC_{ON})/2. Figure 14 portrays a typical operation of the DSS.

As one can see, the V_{CC} capacitor shall be dimensioned to offer an adequate startup time, i.e. ensure regulation is reached before V_{CC} crosses 7.5 V (otherwise the part enters the fault condition mode). If we know that ΔV = 1.0 V and ICC1 (max) is 1.1 mA (for instance we selected an 11 Ω device switching at 65 kHz), then the V_{CC} capacitor can be calculated using: $C \geq \frac{ICC1 \cdot tstartup}{\Delta V}$ (eq. 1). Let's suppose that the SMPS needs 10 ms to startup, then we will calculate C to offer a 15 ms period. As a result, C should be greater than 20 μF thus the selection of a 33 μF/16 V capacitor is appropriate.

Short Circuit Protection

The internal protection circuitry involves a patented arrangement that permanently monitors the assertion of an internal error flag. This error flag is, in fact, a signal that instructs the controller that the internal maximum peak current limit is reached. This naturally occurs during the startup period (Vout is not stabilized to the target value) or when the optocoupler LED is no longer biased, e.g. in a short−circuit condition or when the feedback network is broken. When the DSS normally operates, the logic checks for the presence of the error flag every time V_{CC} crosses VCC_{ON}. If the error flag is low (peak limit not active) then the IC works normally. If the error signal is active, then the NCP101X immediately stops the output pulses, reduces its internal current consumption and does not allow the startup source to activate: V_{CC} drops toward ground until it reaches the so−called latch−off level, where the current source activates again to attempt a new restart. When the error is gone, the IC automatically resumes its operation. If the default is still there, the IC pulses during 8.5 V down to 7.5 V and enters a new latch−off phase. The resulting burst operation guarantees a low average power dissipation and lets the SMPS sustain a permanent short−circuit. Figure 15 shows the corresponding diagram.

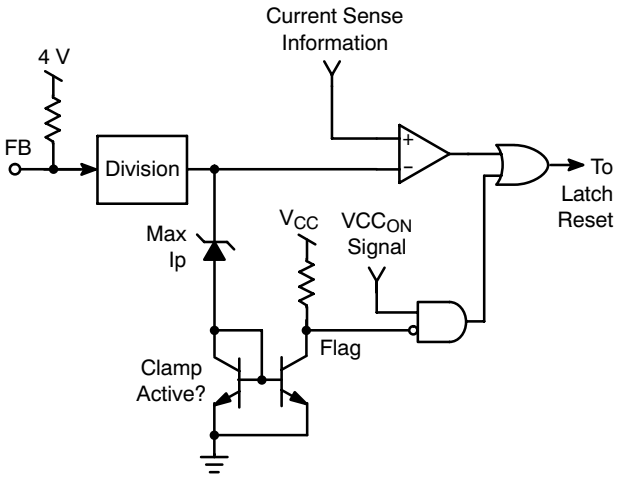


Figure 15. Simplified NCP101X Short−Circuit Detection Circuitry

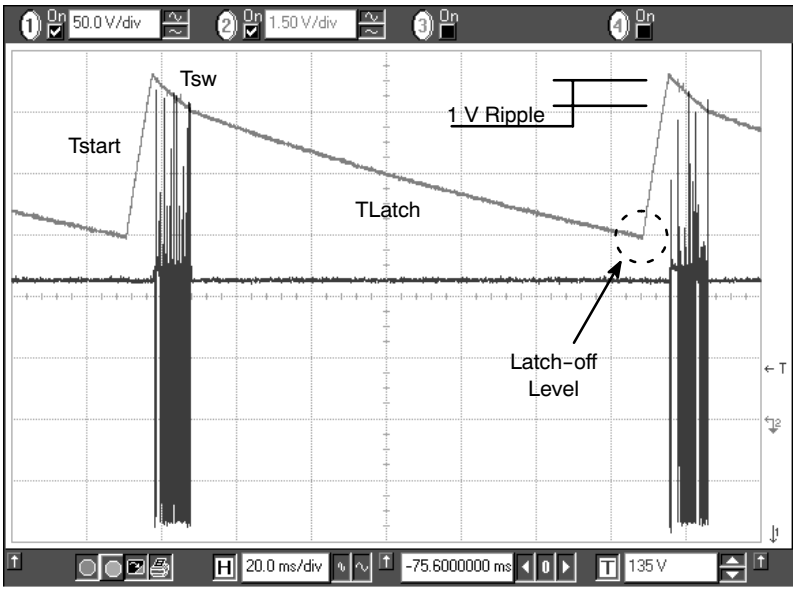


Figure 16. NCP101X Facing a Fault Condition (Vin = 150 Vdc)

The rising slope from the latch−off level up to 8.5 V is expressed by: $Tstart = \frac{\Delta V1 \cdot C}{IC1}$. The time during which the IC actually pulses is given by $tsw = \frac{\Delta V2 \cdot C}{ICC1}$. Finally, the latch−off time can be derived using the same formula topology: $TLatch = \frac{\Delta V3 \cdot C}{ICC2}$. From these three definitions, the burst duty−cycle can be computed: $dc = \frac{Tsw}{Tstart + Tsw + TLatch}$ (eq. 2) . $dc = \frac{\Delta V2}{ICC1 \cdot \left(\frac{\Delta V2}{ICC1} + \frac{\Delta V1}{IC1} + \frac{\Delta V3}{ICC2}\right)}$ (eq. 3) . Feeding the equation with values extracted from the parameter section gives a typical duty−cycle of 13%, precluding any lethal thermal runaway while in a fault condition.

DSS Internal Dissipation

The Dynamic Self−Supplied pulls energy out from the drain pin. In Flyback−based converters, this drain level can easily go above 600 V peak and thus increase the stress on the DSS startup source. However, the drain voltage evolves with time and its period is small compared to that of the DSS. As a result, the averaged dissipation, excluding capacitive losses, can be derived by: $P_{DSS} = ICC1 \cdot < Vds(t) >$. (eq. 4) . Figure 17 portrays a typical drain−ground waveshape where leakage effects have been removed.

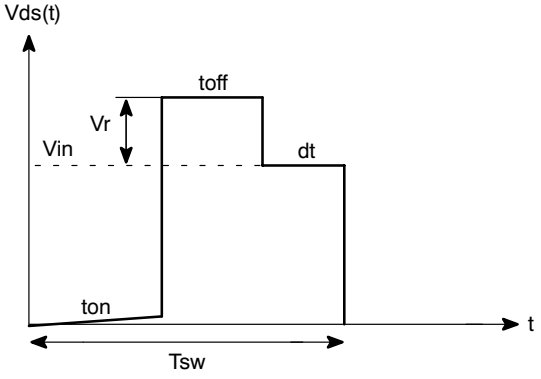


Figure 17. A typical drain−ground waveshape where leakage effects are not accounted for.

By looking at Figure 17, the average result can easily be derived by additive square area calculation:

$$< Vds(t) > = Vin \cdot (1 - d) + Vr \cdot \frac{toff}{Tsw} \quad \text{(eq. 5)}$$

By developing Equation 5, we obtain:

$$< Vds(t) > = Vin - Vin \cdot \frac{ton}{Tsw} + Vr \cdot \frac{toff}{Tsw} \quad \text{(eq. 6)}$$

toff can be expressed by: $toff = Ip \cdot \frac{Lp}{Vr}$ (eq. 7) where ton can be evaluated by: $ton = Ip \cdot \frac{Lp}{Vin}$ (eq. 8) .

Plugging Equations 7 and 8 into Equation 6 leads to $< Vds(t) > = Vin$ and thus, $P_{DSS} = Vin \times ICC1$ (eq. 9) .

The worse case occurs at high line, when Vin equals 370 Vdc. With ICC1 = 1.1 mA (65 kHz version), we can expect a DSS dissipation around 407 mW. If you select a higher switching frequency version, the ICC1 increases and it is likely that the DSS consumption exceeds that number. In that case, we recommend to add an auxiliary winding in order to offer more dissipation room to the power MOSFET.

Please read application note AND8125/D, “Evaluating the Power Capability of the NCP101X Members” to help in selecting the right part/configuration for your application.

Lowering the Standby Power with an Auxiliary Winding

The DSS operation can bother the designer when its dissipation is too high and extremely low standby power is a must. In both cases, one can connect an auxiliary winding to disable the self−supply. The current source then ensures the startup sequence only and stays in the off state as long as V_{CC} does not drop below VCC_{ON} or 7.5 V. Figure 18 shows that the insertion of a resistor (Rlimit) between the auxiliary DC level and the V_{CC} pin is mandatory to not damage the internal 8.7 V active Zener diode during an overshoot for instance (absolute maximum current is 15 mA) and to implement the fail−safe optocoupler protection as offered by the active clamp. Please note that there cannot be bad interaction between the clamping voltage of the internal Zener and VCC_{OFF} since this clamping voltage is actually built on top of VCC_{OFF} with a fixed amount of offset (200 mV typical).

Self−supplying controllers in extremely low standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V (Vnom), this voltage can drop to below 10 V (Vstby) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency refueling rate of the V_{CC} capacitor is not enough to keep a constant auxiliary voltage. Figure 19 portrays a typical scope shot of a SMPS entering deep standby (output unloaded). So care must be taken when calculating Rlimit 1) to not trigger the V_{CC} over current latch [by injecting 6.3 mA (min. value) into the active clamp] in normal operation but 2) not to drop too much voltage over Rlimit when entering standby. Otherwise the DSS could reactivate and the standby performance would degrade. We are thus able to bound Rlimit between two equations:

$$\frac{Vnom - Vclamp}{Itrip} \leq Rlimit \leq \frac{Vstby - VCC_{ON}}{ICC1} \quad \text{(eq. 10)}$$

Where:

Vnom is the auxiliary voltage at nominal load.

Vstdby is the auxiliary voltage when standby is entered.

Itrip is the current corresponding to the nominal operation. It must be selected to avoid false tripping in overshoot conditions.

ICC1 is the controller consumption. This number slightly decreases compared to ICC1 from the spec since the part in standby almost does not switch.

VCC_{ON} is the level above which Vaux must be maintained to keep the DSS in the OFF mode. It is good to shoot around 8.0 V in order to offer an adequate design margin, e.g. to not reactivate the startup source (which is not a problem in itself if low standby power does not matter).

Since Rlimit shall not bother the controller in standby, e.g. keep Vaux to around 8.0 V (as selected above), we purposely select a Vnom well above this value. As explained before, experience shows that a 40% decrease can be seen on auxiliary windings from nominal operation down to standby mode. Let’s select a nominal auxiliary winding of 20 V to offer sufficient margin regarding 8.0 V when in standby (Rlimit also drops voltage in standby…). Plugging the values in Equation 10 gives the limits within which Rlimit shall be selected:

$$\frac{20 - 8.7}{6.3\ m} \leq Rlimit \leq \frac{12 - 8}{1.1\ m}, \text{ that is to say:}$$
$$1.8\ k < Rlimit < 3.6\ k \quad \text{(eq. 11)}$$

If we design a power supply delivering 12 V, then the ratio between auxiliary and power must be: 12/20 = 0.6. The OVP latch will activate when the clamp current exceeds 6.3 mA. This will occur when Vaux increases to: 8.7 V + 1.8 k x (6.4m + 1.1m) = 22.2 V for the first boundary or 8.7 V + 3.6 k x (6.4m +1.1m) = 35.7 V for second boundary. On the power output, it will respectively give 22.2 x 0.6 = 13.3 V and 35.7 x 0.6 = 21.4 V. As one can see, tweaking the Rlimit value will allow the selection of a given overvoltage output level. Theoretically predicting the auxiliary drop from nominal to standby is an almost impossible exercise since many parameters are involved, including the converter time constants. Fine tuning of Rlimit thus requires a few iterations and experiments on a breadboard to check Vaux variations but also output voltage excursion in fault. Once properly adjusted, the fail−safe protection will preclude any lethal voltage runaways in case a problem would occur in the feedback loop.

When an OVP occurs, all switching pulses are permanently disabled, the output voltage thus drops to zero. The V_{CC} cycles up and down between 8.5–4.7 V and stays in this state until the user unplugs the power supply and forces V_{CC} to drop below 3.0 V (VCC_{reset}). Below this value, the internal OVP latch is reset and when the high voltage is reapplied, a new startup sequence can take place in an attempt to restart the converter.

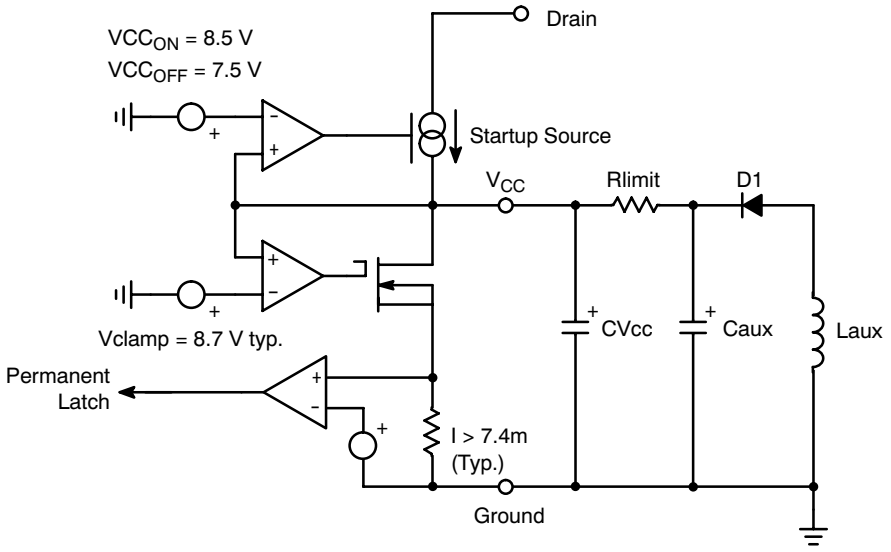


Figure 18. A more detailed view of the NCP101X offers better insight on how to properly wire an auxiliary winding.

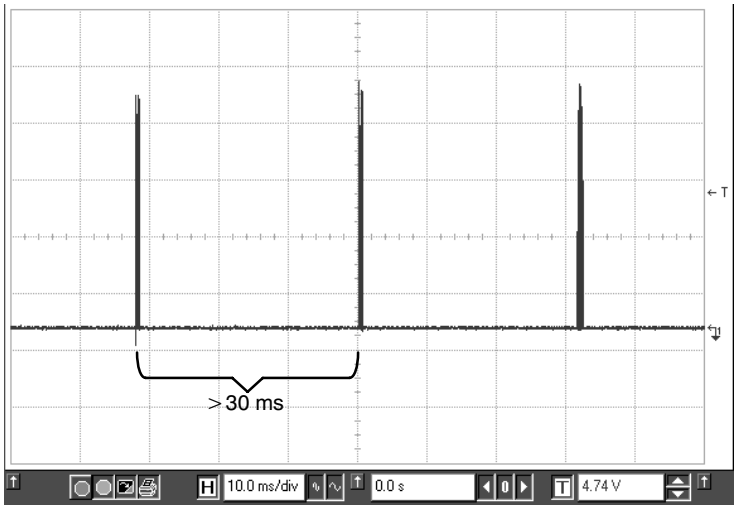


Figure 19. The burst frequency becomes so low that it is difficult to keep an adequate level on the auxiliary V$_{CC}$ . . .

Lowering the Standby Power with Skip−Cycle

Skip−cycle offers an efficient way to reduce the standby power by skipping unwanted cycles at light loads. However, the recurrent frequency in skip often enters the audible range and a high peak current obviously generates acoustic noise in the transformer. The noise takes its origins in the resonance of the transformer mechanical structure which is excited by the skipping pulses. A possible solution, successfully implemented in the NCP1200 series, also authorizes skip−cycle but only when the power demand has dropped below a given level. At this time, the peak current is reduced and no noise can be heard. Figure 20 pictures the peak current evolution of the NCP101X entering standby.

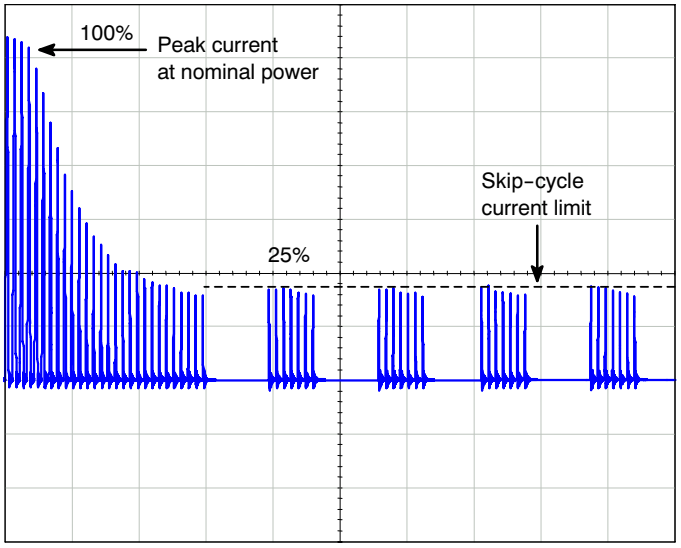


Figure 20. Low Peak Current Skip−Cycle Guarantees Noise−Free Operation

Full power operation involves the nominal switching frequency and thus avoids any noise when running.

Experiments carried on a 5.0 W universal mains board unveiled a standby power of 300 mW @ 230 Vac with the DSS activated and dropped to less than 100 mW when an auxiliary winding is connected.

Frequency Jittering for Improved EMI Signature

By sweeping the switching frequency around its nominal value, it spreads the energy content on adjacent frequencies rather than keeping it centered in one single ray. This offers the benefit to artificially reduce the measurement noise on a standard EMI receiver and pass the tests more easily. The EMI sweep is implemented by routing the V_{CC} ripple (induced by the DSS activity) to the internal oscillator. As a result, the switching frequency moves up and down to the DSS rhythm. Typical deviation is $\pm 3.3\%$ of the nominal frequency. With a 1.0 V peak−to−peak ripple, the frequency will equal 65 kHz in the middle of the ripple and will increase as V_{CC} rises or decrease as V_{CC} ramps down. Figure 21 portrays the behavior we have adopted.

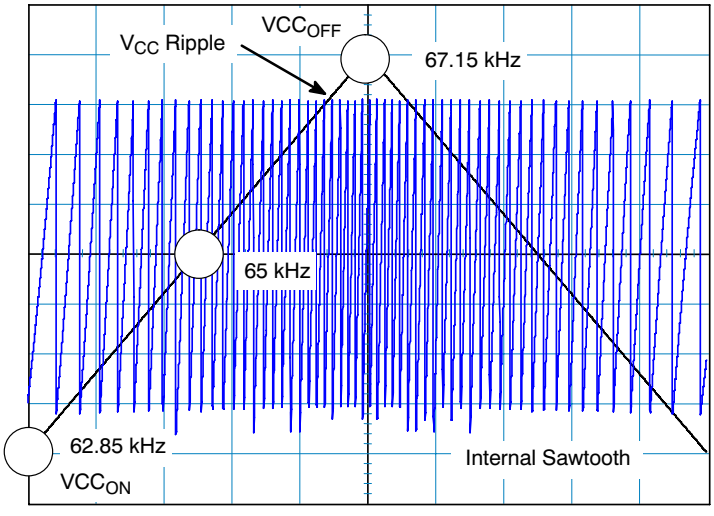


Figure 21. The V_{CC} ripple is used to introduce a frequency jittering on the internal oscillator sawtooth. Here, a 65 kHz version was selected.

Soft−Start

The NCP101X features an internal 1.0 ms soft−start activated during the power on sequence (PON). As soon as V_{CC} reaches VCC_{OFF}, the peak current is gradually increased from nearly zero up to the maximum internal clamping level (e.g. 350 mA). This situation lasts 1.0 ms and further to that time period, the peak current limit is blocked to the maximum until the supply enters regulation. The soft−start is also activated during the over current burst (OCP) sequence. Every restart attempt is followed by a soft−start activation. Generally speaking, the soft−start will be activated when V_{CC} ramps up either from zero (fresh power−on sequence) or 4.7 V, the latch−off voltage occurring during OCP. Figure 22 portrays the soft−start behavior. The time scales are purposely shifted to offer a better zoom portion.

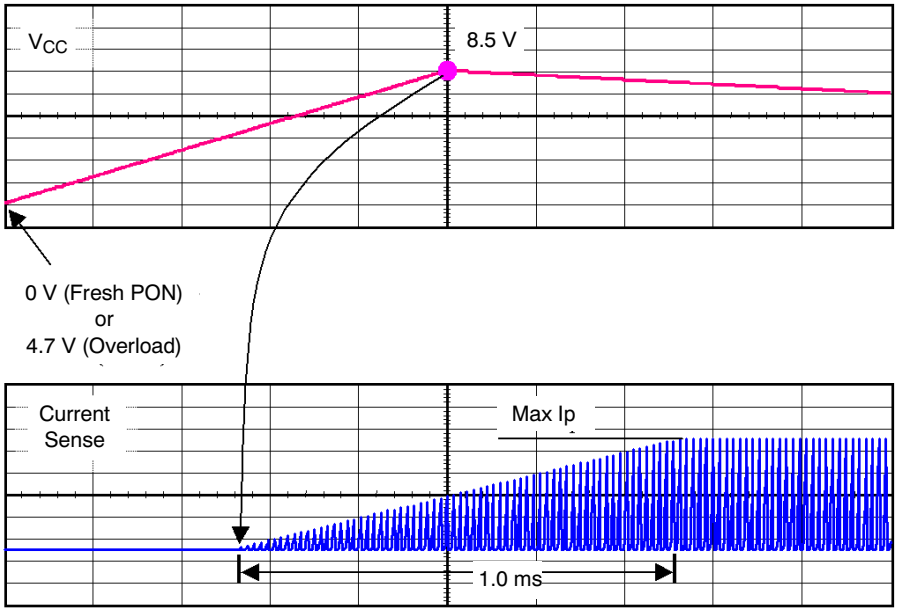


Figure 22. Soft−Start is activated during a startup sequence or an OCP condition.

Non−Latching Shutdown

In some cases, it might be desirable to shut off the part temporarily and authorize its restart once the default has disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB and ground. By pulling FB below the internal skip level (Vskip), the output pulses are disabled. As soon as FB is relaxed, the IC resumes its operation. Figure 23 depicts the application example.

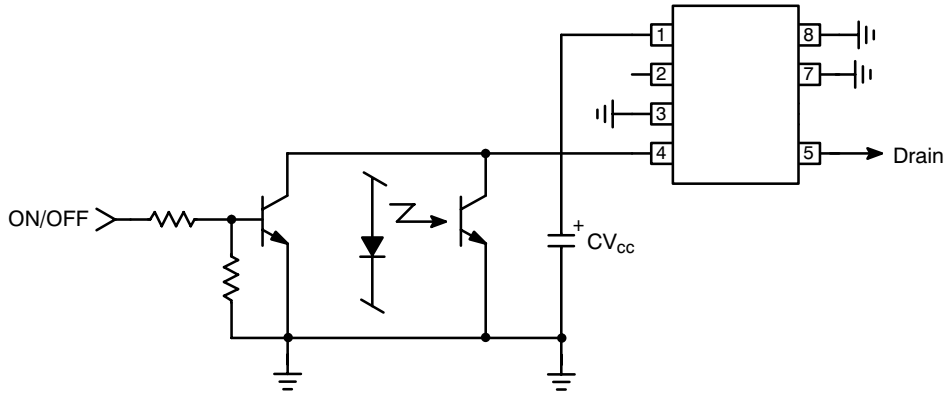


Figure 23. A non−latching shutdown where pulses are stopped as long as the NPN is biased.

Full Latching Shutdown

Other applications require a full latching shutdown, e.g. when an abnormal situation is detected (overtemperature or overvoltage). This feature can easily be implemented through two external transistors wired as a discrete SCR. When the OVP level exceeds the Zener breakdown voltage, the NPN biases the PNP and fires the equivalent SCR, permanently bringing down the FB pin. The switching pulses are disabled until the user unplugs the power supply.

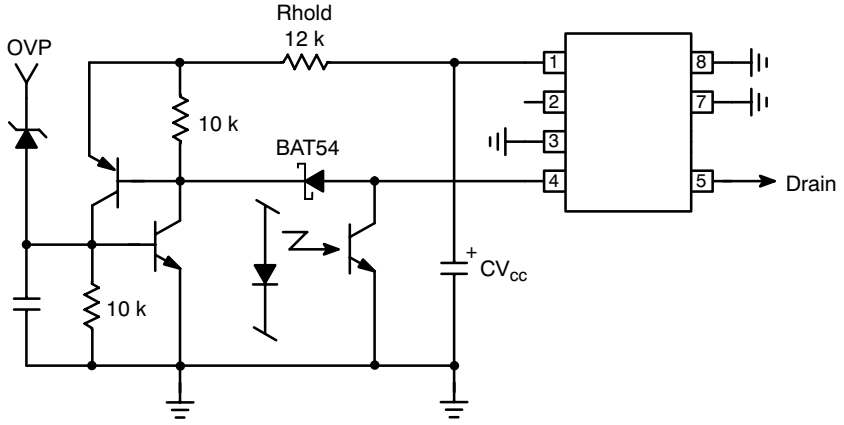


Figure 24. Two Bipolars Ensure a Total Latch−Off of the SMPS in Presence of an OVP

Rhold ensures that the SCR stays on when fired. The bias current flowing through Rhold should be small enough to let the V_{CC} ramp up (8.5 V) and down (7.5 V) when the SCR is fired. The NPN base can also receive a signal from a temperature sensor. Typical bipolars can be MMBT2222 and MMBT2907 for the discrete latch. The MMBT3946 features two bipolars NPN+PNP in the same package and could also be used.

Power Dissipation and Heatsinking

The NCP101X welcomes two dissipating terms, the DSS current−source (when active) and the MOSFET. Thus, Ptot = P_{DSS} + P_{MOSFET}. When the PDIP−7 package is surrounded by copper, it becomes possible to drop its thermal resistance junction−to−ambient, $R_{\theta JA}$ down to 75°C/W and thus dissipate more power. The maximum power the device can thus evacuate is: $Pmax = \frac{T_{Jmax} - T_{ambmax}}{R_{\theta JA}}$ (eq. 12) which gives around 1.0 W for an ambient of 50°C. The losses inherent to the MOSFET R_{DSon} can be evaluated using the following formula: $Pmos = \frac{1}{3} \cdot Ip^2 \cdot d \cdot R_{DSon}$ (eq. 13) , where Ip is the worse case peak current (at the lowest line input), d is the converter operating duty−cycle and R_{DSon}, the MOSFET resistance for T_J = 100°C. This formula is only valid for Discontinuous Conduction Mode (DCM) operation where the turn−on losses are null (the primary current is zero when you restart the MOSFET). Figure 25 gives a possible layout to help drop the thermal resistance. When measured on a 35 μm (1 oz) copper thickness PCB, we obtained a thermal resistance of 75°C/W.

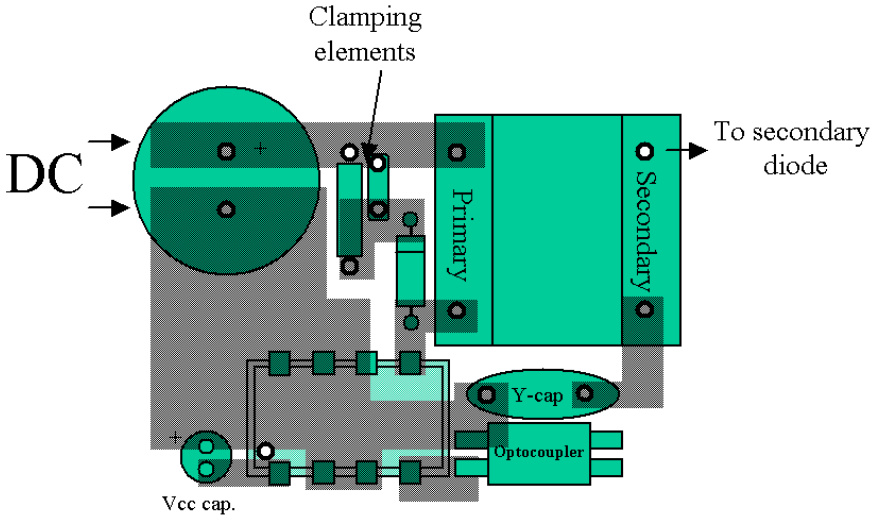


Figure 25. A Possible PCB Arrangement to Reduce the Thermal Resistance Junction−to−Ambient

Design Procedure

The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices:

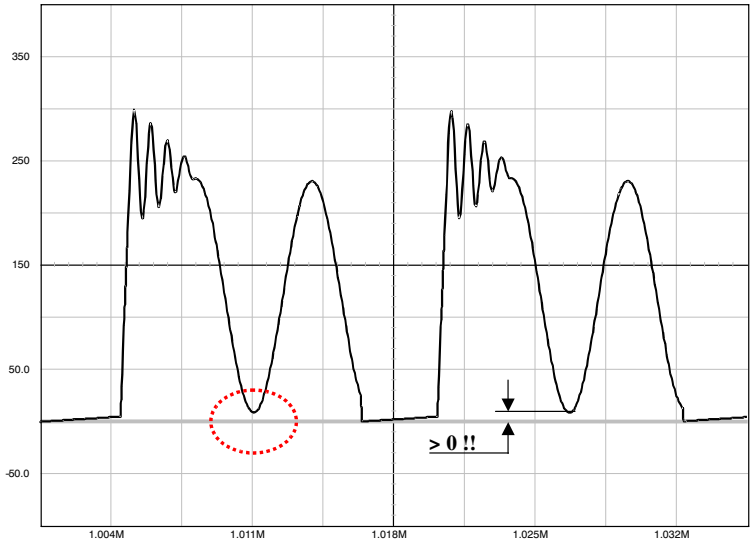


Figure 26. The Drain−Source Wave Shall Always be Positive . . .

1. In any case, the lateral MOSFET body−diode shall never be forward biased, either during startup (because of a large leakage inductance) or in normal operation as shown by Figure 26.

As a result, the Flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation: $N \cdot (Vout + Vf) < Vin_{min}$ (eq. 14) . For instance, if operating from a 120 V DC rail, with a delivery of 12 V, we can select a reflected voltage of 100 Vdc maximum: 120–100 > 0. Therefore, the turn ratio Np:Ns must be smaller than 100/(12 + 1) = 7.7 or Np:Ns < 7.7. We will see later on how it affects the calculation.

2. A current−mode architecture is, by definition, sensitive to subharmonic oscillations. Subharmonic oscillations only occur when the SMPS is operating in Continuous Conduction Mode (CCM) together with a duty−cycle greater than 50%. As a result, we recommend to operate the device in DCM only, whatever duty−cycle it implies (max = 65%). However, CCM operation with duty−cycles below 40% is possible.
3. Lateral MOSFETs have a poorly dopped body−diode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since

$$Vdrain\ max = Vin + N \cdot (Vout + Vf) + Ip \cdot \sqrt{\frac{Lf}{Ctot}}$$

(eq. 15) , where Lf is the leakage inductance, Ctot is the total capacitance at the drain node (which is increased by the capacitor wired between drain and source), N the Np:Ns turn ratio, Vout the output voltage, Vf the secondary diode forward drop and finally, Ip the maximum peak current. Worse case occurs when the SMPS is very close to regulation, e.g. the Vout target is almost reached and Ip is still pushed to the maximum.

Taking into account all previous remarks, it becomes possible to calculate the maximum power that can be transferred at low line.

When the switch closes, Vin is applied across the primary inductance Lp until the current reaches the level imposed by the feedback loop. The duration of this event is called the ON time and can be defined by:

$$ton = \frac{Lp \cdot Ip}{Vin} \qquad \text{(eq. 16)}$$

At the switch opening, the primary energy is transferred to the secondary and the flyback voltage appears across Lp, resetting the transformer core with a slope of $\frac{N \cdot (Vout + Vf)}{Lp}$. toff, the OFF time is thus:

$$toff = \frac{Lp \cdot Ip}{N \cdot (Vout + Vf)} \qquad \text{(eq. 17)}$$

If one wants to keep DCM only, but still need to pass the maximum power, we will not allow a dead−time after the core is reset, but rather immediately restart. The switching time can be expressed by:

$$Tsw = toff + ton = Lp \cdot Ip \cdot \left(\frac{1}{Vin} + \frac{1}{N \cdot (Vout + Vf)}\right) \qquad \text{(eq. 18)}$$

The Flyback transfer formula dictates that:

$$\frac{Pout}{\eta} = \frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw \quad \text{(eq. 19)}$$ which, by extracting Ip and plugging into Equation 19, leads to:

$$Tsw = Lp \sqrt{\frac{2 \cdot Pout}{\eta \cdot Fsw \cdot Lp}} \cdot \left(\frac{1}{Vin} + \frac{1}{N \cdot (Vout + Vf)} \right) \quad \text{(eq. 20)}$$

Extracting Lp from Equation 20 gives:

$$Lp_{critical} = \frac{(Vin \cdot Vr)^2 \cdot \eta}{2 \cdot Fsw \cdot [Pout \cdot (Vr^2 + 2 \cdot Vr \cdot Vin + Vin^2)]}$$

(eq. 21) , with Vr = N . (Vout + Vf) and η the efficiency.

If Lp critical gives the inductance value above which DCM operation is lost, there is another expression we can write to connect Lp, the primary peak current bounded by the NCP101X and the maximum duty−cycle that needs to stay below 50%:

$$Lpmax = \frac{DCmax \cdot Vinmin \cdot Tsw}{Ipmax} \quad \text{(eq. 22)}$$ where Vinmin corresponds to the lowest rectified bulk voltage, hence the longest ton duration or largest duty−cycle. Ip max is the available peak current from the considered part, e.g. 350 mA typical for the NCP1013 (however, the minimum value of this parameter shall be considered for reliable evaluation). Combining Equations 21 and 22 gives the maximum theoretical power you can pass respecting the peak current capability of the NCP101X, the maximum duty−cycle and the discontinuous mode operation:

$$Pmax := Tsw^2 \cdot Vinmin^2 \cdot Vr^2 \cdot \eta \cdot \frac{Fsw}{(2 \cdot Lpmax \cdot Vr^2 + 4 \cdot Lpmax \cdot Vr \cdot Vinmin + 2 \cdot Lpmax \cdot Vinmin^2)} \quad \text{(eq. 23)}$$

From Equation 22 we obtain the operating duty−cycle $d = \frac{Ip \cdot Lp}{Vin \cdot Tsw}$ (eq. 24) which lets us calculate the RMS current circulating in the MOSFET:

$$IdRMS = Ip \cdot \sqrt{\frac{d}{3}} \quad \text{(eq. 25)}$$. From this equation, we obtain the average dissipation in the MOSFET: $Pavg = \frac{1}{3} \cdot Ip^2 \cdot d \cdot R_{DSon}$ (eq. 26) to which switching losses shall be added.

If we stick to Equation 23, compute Lp and follow the above calculations, we will discover that a power supply built with the NCP101X and operating from a 100 Vac line minimum will not be able to deliver more than 7.0 W continuous, regardless of the selected switching frequency (however the transformer core size will go down as Fswitching is increased). This number increases significantly when operated from a single European mains (18 W). Application note AND8125/D, “Evaluating the Power Capability of the NCP101X Members” details how to assess the available power budget from all the NCP101X series.

Example 1. A 12 V 7.0 W SMPS operating on a large mains with NCP101X:

Vin = 100 Vac to 250 Vac or 140 Vdc to 350 Vdc once rectified, assuming a low bulk ripple

Efficiency = 80%

Vout = 12 V, Iout = 580 mA

Fswitching = 65 kHz

Ip max = 350 mA – 10% = 315 mA

Applying the above equations leads to:

Selected maximum reflected voltage = 120 V

with Vout = 12 V, secondary drop = 0.5 V → Np:Ns = 1:0.1

Lp critical = 3.2 mH

Ip = 292 mA

Duty−cycle worse case = 50%

Idrain RMS = 119 mA

P_{MOSFET} = 354 mW at R_{DSon} = 24 Ω (T_J > 100°C)

P_{DSS} = 1.1 mA x 350 V = 385 mW, if DSS is used

Secondary diode voltage stress = (350 x 0.1) + 12 = 47 V (e.g. a MBRS360T3, 3.0 A/60 V would fit)

Example 2. A 12 V 16 W SMPS operating on narrow European mains with NCP101X:

Vin = 230 Vac ± 15%, 276 Vdc for Vin min to 370 Vdc once rectified

Efficiency = 80%

Vout = 12 V, Iout = 1.25 A

Fswitching = 65 kHz

Ip max = 350 mA – 10% = 315 mA

Applying the equations leads to:

Selected maximum reflected voltage = 250 V

with Vout = 12 V, secondary drop = 0.5 V → Np:Ns = 1:0.05

Lp = 6.6 mH

Ip = 0.305 mA

Duty−cycle worse case = 0.47

Idrain RMS = 121 mA

P_{MOSFET} = 368 mW at R_{DSon} = 24 Ω (T_J > 100°C)

P_{DSS} = 1.1 mA x 370 V = 407 mW, if DSS is used below an ambient of 50°C.

Secondary diode voltage stress = (370 x 0.05) + 12 = 30.5 V (e.g. a MBRS340T3, 3.0 A/40 V)

Please note that these calculations assume a flat DC rail whereas a 10 ms ripple naturally affects the final voltage available on the transformer end. Once the Bulk capacitor has been selected, one should check that the resulting ripple (min Vbulk?) is still compatible with the above calculations. As an example, to benefit from the largest operating range, a 7.0 W board was built with a 47 μF bulk capacitor which ensured discontinuous operation even in the ripple minimum waves.

MOSFET Protection

As in any Flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET BV_{DSS} which is 700 V. Figure 27 presents possible implementations:

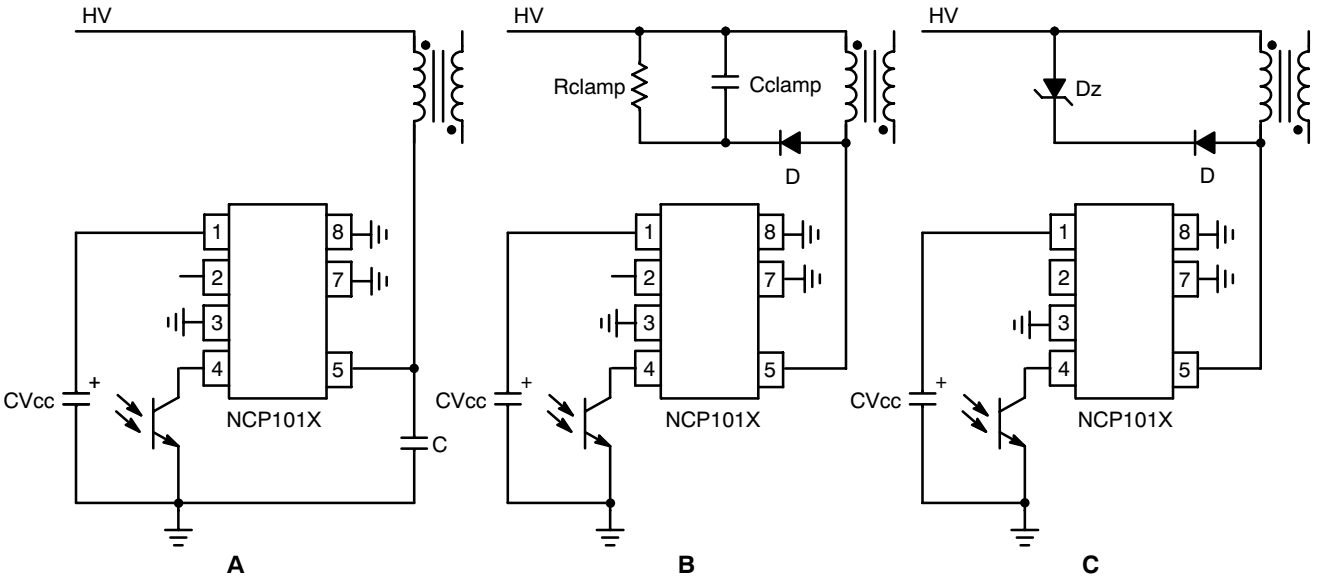


Figure 27. Different Options to Clamp the Leakage Spike

Figure 27A: The simple capacitor limits the voltage according to Equation 15. This option is only valid for low power applications, e.g. below 5.0 W, otherwise chances exist to destroy the MOSFET. After evaluating the leakage inductance, you can compute C with Equation 15. Typical values are between 100 pF and up to 470 pF. Large capacitors increase capacitive losses.

Figure 27B: This diagram illustrates the most standard circuitry called the RCD network. Rclamp and Cclamp are calculated using the following formulas:

$$Rclamp = \frac{2 \cdot Vclamp \cdot (Vclamp - (Vout + Vf\,sec) \cdot N)}{Lleak \cdot Ip^2 \cdot Fsw} \quad \text{(eq. 27)}$$

$$Cclamp = \frac{Vclamp}{Vripple \cdot Fsw \cdot Rclamp} \quad \text{(eq. 28)}$$

Vclamp is usually selected 50−80 V above the reflected value N x (Vout + Vf). The diode needs to be a fast one and a MUR160 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. Worse case occurs when Ip and Vin are maximum and Vout is close to reach the steady−state value.

Figure 27C: This option is probably the most expensive of all three but it offers the best protection degree. If you need a very precise clamping level, you must implement a Zener diode or a TVS. There are little technology differences behind a standard Zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of Zener. A 5.0 W Zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal Zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5.0 W of continuous power but is able to accept surges up to 600 W @ 1.0 ms. Select the Zener or TVS clamping level between 40 to 80 V above the reflected output voltage when the supply is heavily loaded.

Typical Application Examples

A 6.5 W NCP1012−Based Flyback Converter

Figure 28 shows a converter built with a NCP1012 delivering 6.5 W from a universal input. The board uses the Dynamic Self−Supply and a simplified Zener−type feedback. This configuration was selected for cost reasons and a more precise circuitry can be used, e.g. based on a TL431:

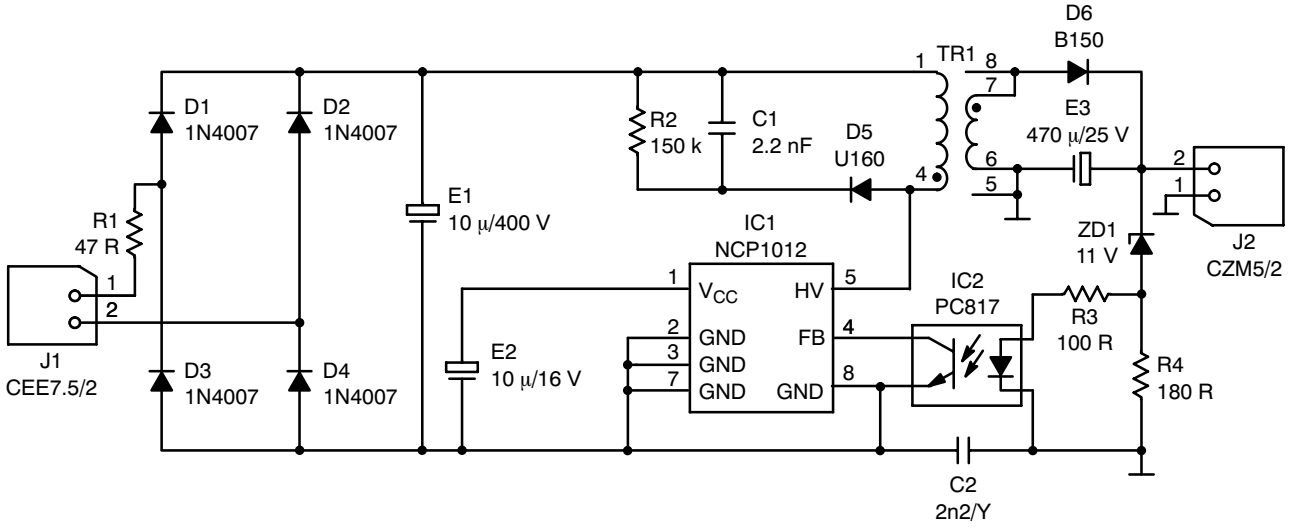


Figure 28. An NCP1012−Based Flyback Converter Delivering 6.5 W

The converter built according to Figure 29 layouts, gave the following results:

- Efficiency at Vin = 100 Vac and Pout = 6.5 W = 75.7%
- Efficiency at Vin = 230 Vac and Pout = 6.5 W = 76.5%

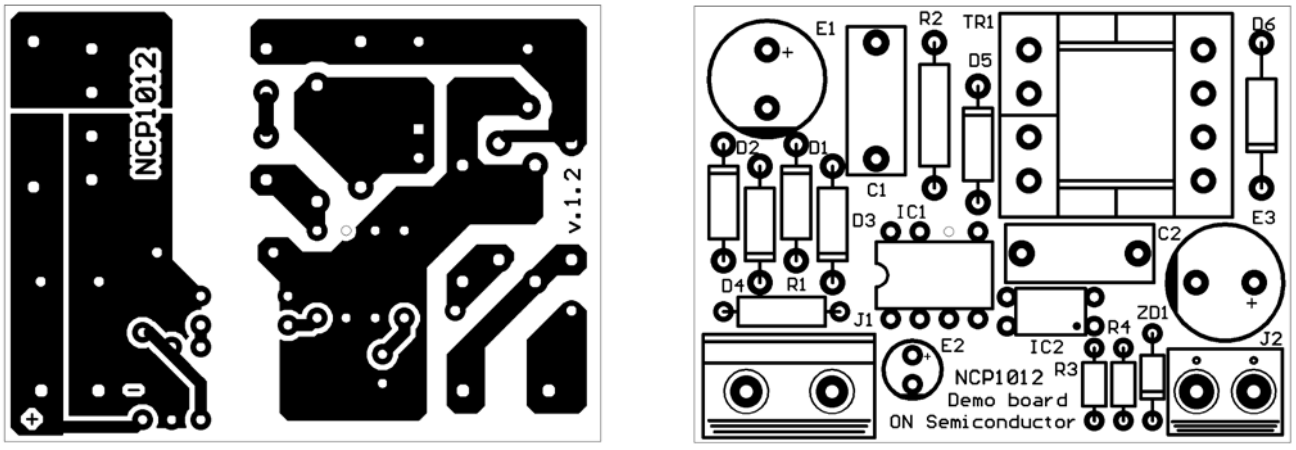


Figure 29. The NCP1012−Based PCB Layout . . . and its Associated Component Placement

A 7.0 W NCP1013−based Flyback Converter Featuring Low Standby Power

Figure 30 depicts another typical application showing a NCP1013−65 kHz operating in a 7.0 W converter up to 70°C of ambient temperature. We can increase the output power since an auxiliary winding is used, the DSS is disabled, and thus offering more room for the MOSFET. In this application, the feedback is made via a TLV431 whose low bias current (100 μA min) helps to lower the no−load standby power.

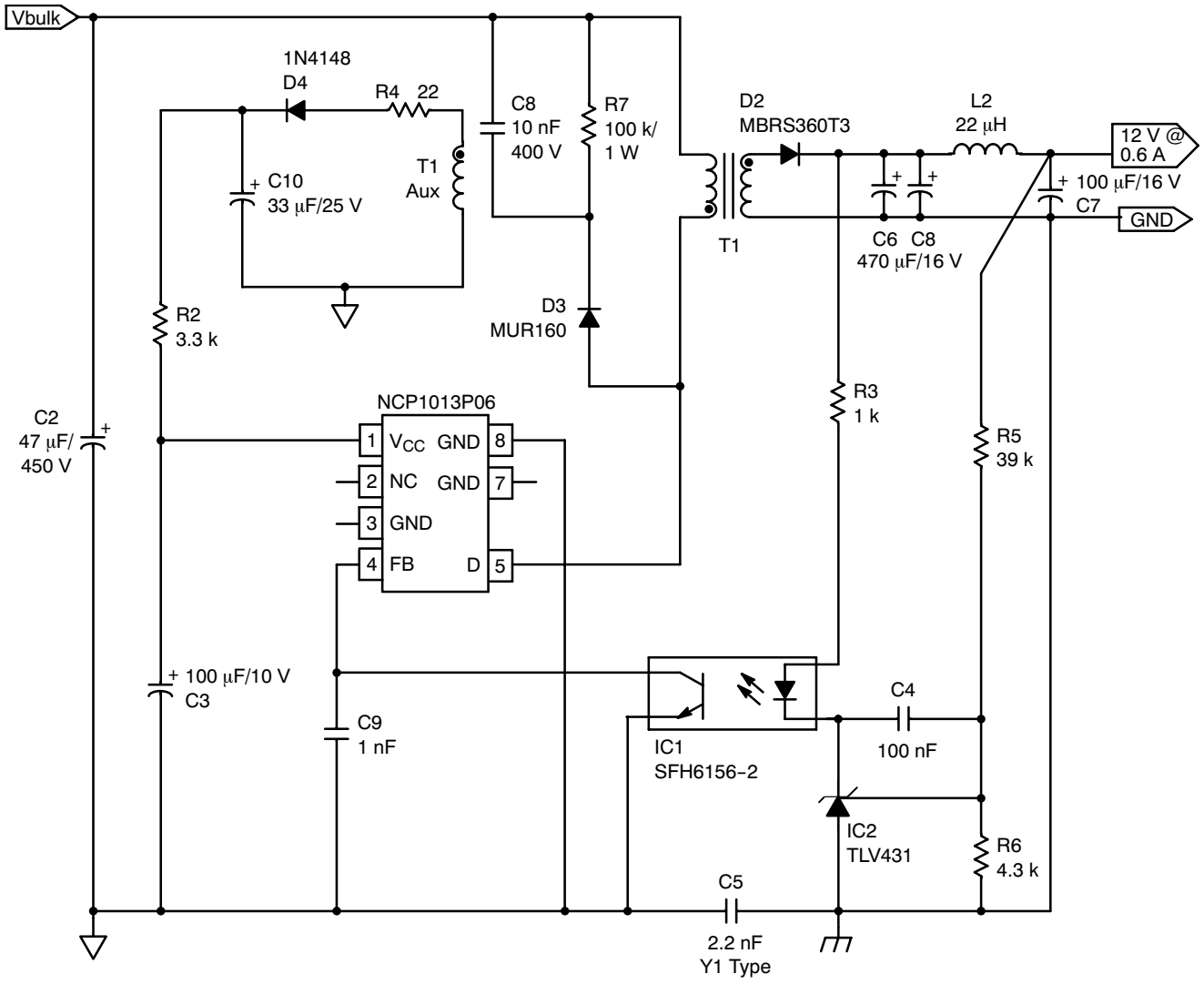


Figure 30. A Typical Converter Delivering 7.0 W from a Universal Mains

Measurements have been taken from a demonstration board implementing the diagram in Figure 30 and the following results were achieved, with either the auxiliary winding in place or through the Dynamic Self−Supply:

Vin = 230 Vac, auxiliary winding, Pout = 0, Pin = 60 mW

Vin = 100 Vac, auxiliary winding, Pout = 0, Pin = 42 mW

Vin = 230 Vac, Dynamic Self−Supply, Pout = 0, Pin = 300 mW

Vin = 100 Vac, Dynamic Self−Supply, Pout = 0, Pin = 130 mW

Pout = 7.0 W, η = 81% @ 230 Vac, with auxiliary winding

Pout = 7.0 W, η = 81.3 @ 100 Vac, with auxiliary winding

For a quick evaluation of Figure 30 application example, the following transformers are available from Coilcraft:

A9619−C, Lp = 3.0 mH, Np:Ns = 1:0.1, 7.0 W application on universal mains, including auxiliary winding, NCP1013−65kHz.

A0032−A, Lp = 6.0 mH, Np:Ns = 1:0.055, 10 W application on European mains, DSS operation only, NCP1013−65 kHz.

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Email: info@coilcraft.com
Tel.: 847−639−6400
Fax.: 847−639−1469

ORDERING INFORMATION

Device Order Number	Frequency (kHz)	Package Type	Shipping†	R_{DSon} (Ω)	Ipk (mA)
NCP1010AP065	65	PDIP−7	50 Units / Rail	23	100
NCP1010AP065G	65	PDIP−7 (Pb−Free)		23	100
NCP1010AP100	100	PDIP−7		23	100
NCP1010AP100G	100	PDIP−7 (Pb−Free)		23	100
NCP1010AP130	130	PDIP−7		23	100
NCP1010AP130G	130	PDIP−7 (Pb−Free)		23	100
NCP1011APL065R2G	65	PDIP−7 (Gull Wing) (Pb−Free)	1000 / Tape & Reel	23	250
NCP1010ST65T3	65	SOT−223	4000 / Tape & Reel	23	100
NCP1010ST65T3G	65	SOT−223 (Pb−Free)		23	100
NCP1010ST100T3	100	SOT−223		23	100
NCP1010ST100T3G	100	SOT−223 (Pb−Free)		23	100
NCP1010ST130T3	130	SOT−223		23	100
NCP1010ST130T3G	130	SOT−223 (Pb−Free)		23	100
NCP1011AP065	65	PDIP−7	50 Units / Rail	23	250
NCP1011AP065G	65	PDIP−7 (Pb−Free)		23	250
NCP1011APL065R2G	65	PDIP−7 (Gull Wing) (Pb−Free)	1000 / Tape & Reel	23	250
NCP1011AP100	100	PDIP−7	50 Units / Rail	23	250
NCP1011AP100G	100	PDIP−7 (Pb−Free)		23	250
NCP1011AP130	130	PDIP−7		23	250
NCP1011AP130G	130	PDIP−7 (Pb−Free)		23	250
NCP1011APL130R2G	130	PDIP−7 (Gull Wing) (Pb−Free)	1000 / Tape & Reel	23	250
NCP1011ST65T3	65	SOT−223	4000 / Tape & Reel	23	250
NCP1011ST65T3G	65	SOT−223 (Pb−Free)		23	250
NCP1011ST100T3	100	SOT−223		23	250
NCP1011ST100T3G	100	SOT−223 (Pb−Free)		23	250
NCP1011ST130T3	130	SOT−223		23	250
NCP1011ST130T3G	130	SOT−223 (Pb−Free)		23	250
NCP1012AP065	65	PDIP−7	50 Units / Rail	11	250
NCP1012AP065G	65	PDIP−7 (Pb−Free)		11	250
NCP1012APL065R2G	65	PDIP−7 (Gull Wing) (Pb−Free)	1000 / Tape & Reel	11	250
NCP1012AP100	100	PDIP−7	50 Units / Rail	11	250
NCP1012AP100G	100	PDIP−7 (Pb−Free)		11	250

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
Additional Gull Wing option may be available upon request. Please contact your ON Semiconductor representative.

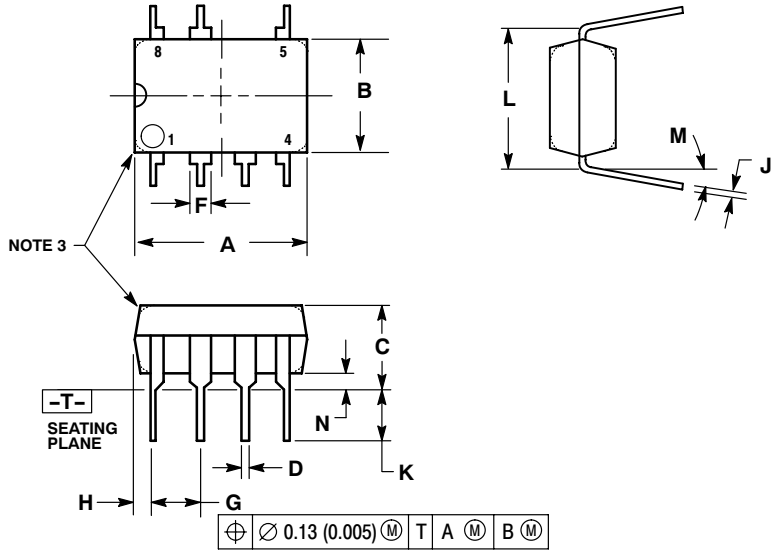
ORDERING INFORMATION

Device Order Number	Frequency (kHz)	Package Type	Shipping†	R_{DSon} (Ω)	Ipk (mA)
NCP1012APL100R2G	100	PDIP−7 (Gull Wing) (Pb−Free)	1000 / Tape & Reel	11	250
NCP1012AP133	130	PDIP−7	50 Units / Rail	11	250
NCP1012AP133G	130	PDIP−7 (Pb−Free)		11	250
NCP1012APL130R2G	130	PDIP−7 (Gull Wing) (Pb−Free)	1000 / Tape & Reel	11	250
NCP1012ST65T3	65	SOT−223	4000 / Tape & Reel	11	250
NCP1012ST65T3G	65	SOT−223 (Pb−Free)		11	250
NCP1012ST100T3	100	SOT−223		11	250
NCP1012ST100T3G	100	SOT−223 (Pb−Free)		11	250
NCP1012ST130T3	130	SOT−223	4000 / Tape & Reel	11	250
NCP1012ST130T3G	130	SOT−223 (Pb−Free)		11	250
NCP1013AP065	65	PDIP−7	50 Units / Rail	11	350
NCP1013AP065G	65	PDIP−7 (Pb−Free)		11	350
NCP1013AP100	100	PDIP−7		11	350
NCP1013AP100G	100	PDIP−7 (Pb−Free)		11	350
NCP1013AP133	130	PDIP−7		11	350
NCP1013AP133G	130	PDIP−7 (Pb−Free)		11	350
NCP1013ST65T3	65	SOT−223	4000 / Tape & Reel	11	350
NCP1013ST65T3G	65	SOT−223 (Pb−Free)		11	350
NCP1013ST100T3	100	SOT−223		11	350
NCP1013ST100T3G	100	SOT−223 (Pb−Free)		11	350
NCP1013ST130T3	130	SOT−223		11	350
NCP1013ST130T3G	130	SOT−223 (Pb−Free)		11	350
NCP1014AP065	65	PDIP−7	50 Units / Rail	11	450
NCP1014AP065G	65	PDIP−7 (Pb−Free)		11	450
NCP1014APL065R2G	65	PDIP−7 (Gull Wing) (Pb−Free)	1000 / Tape & Reel	11	450
NCP1014AP100	100	PDIP−7	50 Units / Rail	11	450
NCP1014AP100G	100	PDIP−7 (Pb−Free)		11	450
NCP1014APL100R2G	100	PDIP−7 (Gull Wing) (Pb−Free)	1000 / Tape & Reel	11	450
NCP1014ST65T3	65	SOT−223	4000 / Tape & Reel	11	450
NCP1014ST65T3G	65	SOT−223 (Pb−Free)		11	450
NCP1014ST100T3	100	SOT−223		11	450
NCP1014ST100T3G	100	SOT−223 (Pb−Free)		11	450

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
Additional Gull Wing option may be available upon request. Please contact your ON Semiconductor representative.

PACKAGE DIMENSIONS

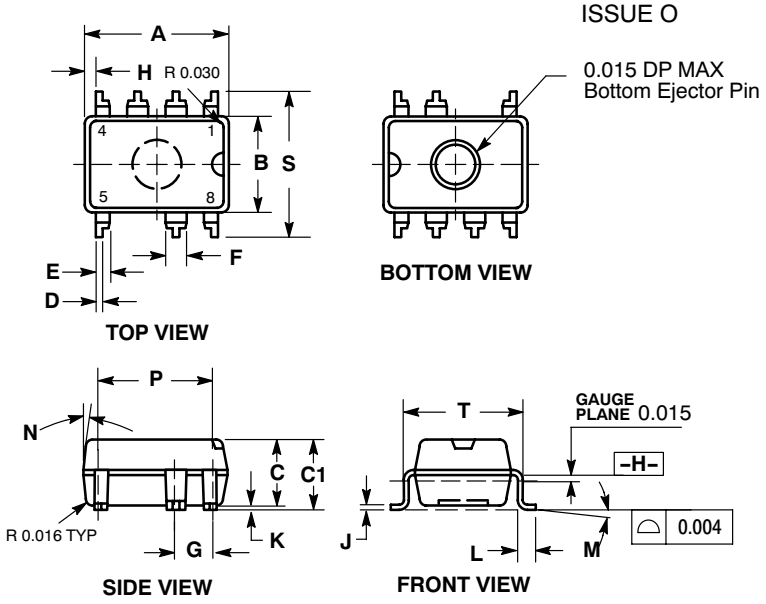
PDIP−7
AP SUFFIX
CASE 626A−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B ARE DATUMS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PDIP−7, GULL WING
APL SUFFIX
CASE 626AA−01
ISSUE O

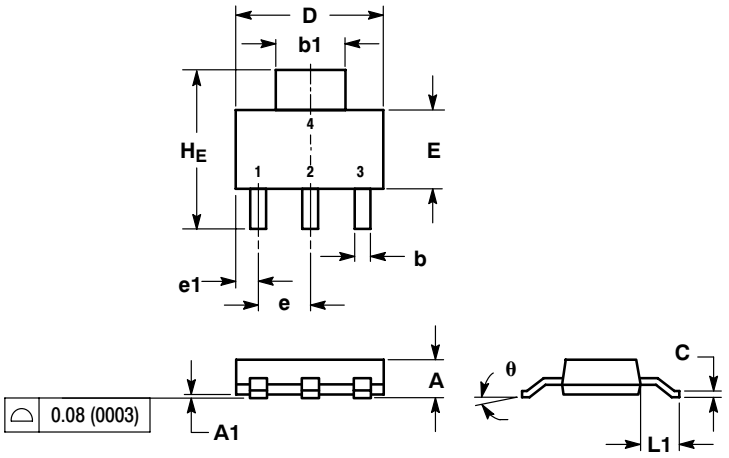


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN INCHES.

	INCHES	
DIM	MIN	MAX
A	0.365	0.385
B	0.240	0.260
C	0.120	0.150
C1	0.124	0.162
D	0.018 TYP	
E	0.039 TYP	
F	0.045	0.065
G	0.100 BSC	
H	0.023	0.033
J	0.010 TYP	
K	0.004	0.012
L	0.036	0.044
M	0 °	8 °
N	12 ° TYP	
P	0.300 BSC	
S	0.372	0.388

PACKAGE DIMENSIONS

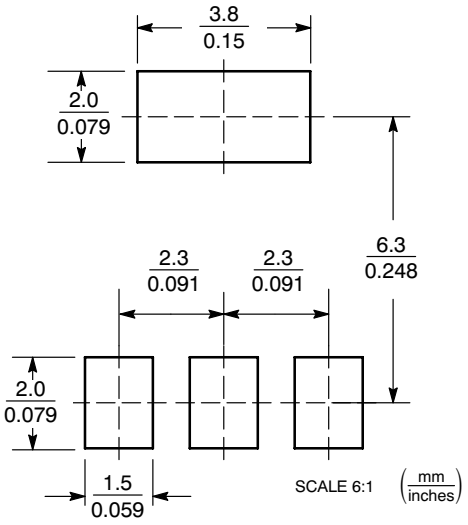
SOT−223
ST SUFFIX
CASE 318E−04
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NCP1010, 1011, 1012, 1013, 1014), may be covered by one or more of the following U.S. patents: 6,271,735, 6,362,067, 6,385,060, 6,429,709, 6,587,357, 6,633,193. There may be other patents pending.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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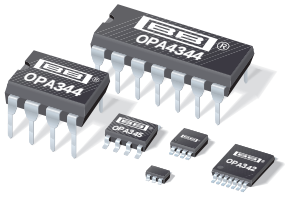
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

BURR-BROWN®



OPA344
OPA2344
OPA4344

OPA345
OPA2345
OPA4345

For most current data sheet and other product information, visit www.burr-brown.com

LOW POWER, SINGLE-SUPPLY, RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

*Micro*Amplifier™ Series

FEATURES

- RAIL-TO-RAIL INPUT
- RAIL-TO-RAIL OUTPUT (within 1mV)
- LOW QUIESCENT CURRENT: 150μA typ
- *Micro*SIZE PACKAGES
  - SOT23-5
  - MSOP-8
  - TSSOP-14
- GAIN-BANDWIDTH
  - OPA344: 1MHz, G ≥ 1
  - OPA345: 3MHz, G ≥ 5
- SLEW RATE
  - OPA344: 0.8V/μs
  - OPA345: 2V/μs
- THD + NOISE: 0.006%

APPLICATIONS

- PCMCIA CARDS
- DATA ACQUISITION
- PROCESS CONTROL
- AUDIO PROCESSING
- COMMUNICATIONS
- ACTIVE FILTERS
- TEST EQUIPMENT

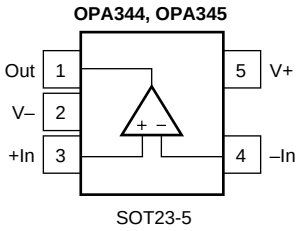
DESCRIPTION

The OPA344 and OPA345 series rail-to-rail CMOS operational amplifiers are designed for precision, low-power, miniature applications. The OPA344 is unity gain stable, while the OPA345 is optimized for gains greater than or equal to five, and has a gain-bandwidth product of 3MHz.

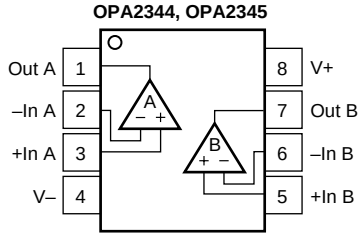
The OPA344 and OPA345 are optimized to operate on a single supply from 2.5V and up to 5.5V with an input common-mode voltage range that extends 300mV beyond the supplies. Quiescent current is only 250μA (max).

Rail-to-rail input and output make them ideal for driving sampling analog-to-digital converters. They are also well suited for general purpose and audio applicaitons and providing I/V conversion at the output of D/A converters. Single, dual and quad versions have identical specs for design flexibility.

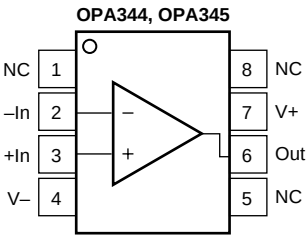
A variety of packages are available. All are specified for operation from –40ºC to 85ºC. A SPICE macromodel is available for design analysis.



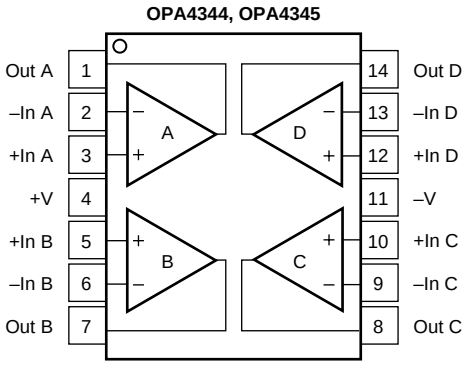
SOT23-5



SO-8, MSOP-8, 8-Pin DIP (OPA2344 Only)



SO-8, 8-Pin DIP (OPA344 Only)



TSSOP-14, SO-14, 14-PIn DIP (OPA4344 Only)

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1486A

Printed in U.S.A. April, 2000

SBOS107

SPECIFICATIONS: V_S = 2.7V to 5.5V

At T_A = +25°C, R_L = 10kΩ connected to $V_S/2$ and $V_{OUT} = V_S/2$, unless otherwise noted.
Boldface limits apply over the temperature range, T_A = –40°C to +85°C.

PARAMETER		CONDITION	OPA344NA, UA, PA OPA2344EA, UA, PA OPA4344EA, UA, PA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = +5.5V, $V_{CM} = V_S/2$		±0.2	±1	mV
Over Temperature				**±0.8**	**±1.2**	mV
vs Temperature	**dV_{OS}/dT**			**±3**		µV/°C
vs Power Supply	PSRR	V_S = 2.7V to 5.5V, V_{CM} < (V+) -1.8V		30	200	µV/V
Over Temperature		**V_S = 2.7V to 5.5V, V_{CM} < (V+) -1.8V**			**250**	µV/V
Channel Separation, dc				0.2		µV/V
f = 1kHz				130		dB
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.2	±10	pA
Over Temperature				**See Typical Curve**		pA
Input Offset Current	I_{OS}			±0.2	±10	pA
NOISE						
Input Voltage Noise		f = 0.1 to 50kHz		8		µVrms
Input Voltage Noise Density	e_n	f = 10kHz		30		nV/√Hz
Current Noise Density	i_n	f = 10kHz		0.5		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		–0.3		(V+) + 0.3	V
Common-Mode Rejection Ratio	CMRR	V_S = +5.5V, –0.3V < V_{CM} < (V+)-1.8	76	92		dB
Over Temperature		**V_S = +5.5V, –0.3V < V_{CM} < (V+)-1.8**	**74**			dB
Common-Mode Rejection	CMRR	V_S = +5.5V, –0.3V < V_{CM} < 5.8V	70	84		dB
Over Temperature		**V_S = +5.5V, –0.3V < V_{CM} < 5.8V**	**68**			dB
Common-Mode Rejection	CMRR	V_S = +2.7V, –0.3V < V_{CM} < 3V	66	80		dB
Over Temperature		**V_S = +2.7V, –0.3V < V_{CM} < 3V**	**64**			dB
INPUT IMPEDANCE						
Differential				10^{13} || 3		Ω || pF
Common-Mode				10^{13} || 6		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 100kΩ, 10mV < V_O < (V+) –10mV	104	122		dB
Over Temperature		**R_L = 100kΩ, 10mV < V_O < (V+) –10mV**	**100**			dB
		R_L = 5kΩ, 400mV < V_O < (V+) –400mV	96	120		dB
Over Temperature		**R_L = 5kΩ, 400mV < V_O < (V+) –400mV**	**90**			dB
FREQUENCY RESPONSE		C_L = 100pF				
Gain-Bandwidth Product	GBW			1		MHz
Slew Rate	SR			0.8		V/µs
Settling Time, 0.1%		V_S = 5.5V, 2V Step		5		µs
0.01%		V_S = 5.5V, 2V Step		8		µs
Overload Recovery Time		$V_{IN} \bullet G = V_S$		2.5		µs
Total Harmonic Distortion + Noise	THD+N	V_S = 5.5V, V_O = 3Vp-p, G = 1, f = 1kHz		0.006		%
OUTPUT						
Voltage Output Swing from Rail[1]		R_L = 100kΩ, $A_{OL} \geq$ 96dB		1		mV
		R_L = 100kΩ, $A_{OL} \geq$ 104dB		3	10	mV
Over Temperature		**R_L = 100kΩ, $A_{OL} \geq$ 100dB**			**10**	mV
		R_L = 5kΩ, $A_{OL} \geq$ 96dB		40	400	mV
Over Temperature		**R_L = 5kΩ, $A_{OL} \geq$ 90dB**			**400**	mV
Short-Circuit Current	I_{SC}			±15		mA
Capacitive Load Drive	C_{LOAD}			See Typical Curve		
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		5.5	V
Operating Voltage Range				2.5 to 5.5		V
Quiescent Current (per amplifier)	I_Q	V_S = 5.5V, I_O = 0		150	250	µA
Over Temperature					**300**	µA
TEMPERATURE RANGE						
Specified Range			–40		85	°C
Operating Range			–55		125	°C
Storage Range			–65		150	°C
Thermal Resistance	θ_{JA}					
SOT23-5 Surface Mount				200		°C/W
MSOP-8 Surface Mount				150		°C/W
8-Pin DIP				100		°C/W
SO-8 Surface Mount				150		°C/W
TSSOP-14 Surface Mount				100		°C/W
14-Pin DIP				80		°C/W
SO-14 Surface Mount				100		°C/W

NOTE: (1) Output voltage swings are measured between the output and power-supply rails.

SPECIFICATIONS: V_S = 2.7V to 5.5V

At T_A = +25°C, R_L = 10kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.
Boldface limits apply over the temperature range, T_A = –40°C to +85°C.

PARAMETER		CONDITION	OPA345NA, UA OPA2345EA, UA OPA4345EA, UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = +5.5V, V_{CM} = V_S/2		±0.2	±1	mV
Over Temperature				**±0.8**	**±1.2**	mV
vs Temperature	**dV_{OS}/dT**			**±3**		µV/°C
vs Power Supply	PSRR	V_S = 2.7V to 5.5V, V_{CM} < (V+) -1.8V		30	200	µV/V
Over Temperature		**V_S = 2.7V to 5.5V, V_{CM} < (V+) -1.8V**			**250**	µV/V
Channel Separation, dc				0.2		µV/V
f = 1kHz				130		dB
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.2	±10	pA
Over Temperature				**See Typical Curve**		pA
Input Offset Current	I_{OS}			±0.2	±10	pA
NOISE						
Input Voltage Noise		f = 0.1 to 50kHz		8		µVrms
Input Voltage Noise Density	e_n	f = 10kHz		30		nV/√Hz
Current Noise Density	i_n	f = 10kHz		0.5		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		–0.3		(V+) + 0.3	V
Common-Mode Rejection Ratio	CMRR	V_S = +5.5V, –0.3V < V_{CM} < (V+)-1.8	76	92		dB
Over Temperature		**V_S = +5.5V, –0.3V < V_{CM} < (V+)-1.8**	**74**			dB
Common-Mode Rejection Ratio	CMRR	V_S = +5.5V, –0.3V < V_{CM} < 5.8V	70	84		dB
Over Temperature		**V_S = +5.5V, –0.3V < V_{CM} < 5.8V**	**68**			dB
Common-Mode Rejection Ratio	CMRR	V_S = +2.7V, –0.3V < V_{CM} < 3V	66	80		dB
Over Temperature		**V_S = +2.7V, –0.3V < V_{CM} < 3V**	**64**			dB
INPUT IMPEDANCE						
Differential				10^{13} || 3		Ω || pF
Common-Mode				10^{13} || 6		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 100kΩ, 10mV < V_O < (V+) –10mV	104	122		dB
Over Temperature		**R_L = 100kΩ, 10mV < V_O < (V+) –10mV**	**100**			dB
		R_L = 5kΩ, 400mV < V_O < (V+) –400mV	96	120		dB
Over Temperature		**R_L = 5kΩ, 400mV < V_O < (V+) –400mV**	**90**			dB
FREQUENCY RESPONSE		C_L = 100pF				
Gain-Bandwidth Product	GBW			3		MHz
Slew Rate	SR			2		V/µs
Settling Time, 0.1%		G = 5, 2V Output Step		1.5		µs
0.01%		G = 5, 2V Output Step		1.6		µs
Overload Recovery Time		V_{IN} • G = V_S		2.5		µs
Total Harmonic Distortion + Noise	THD+N	V_S = 5.5V, V_O = 2.5Vp-p, G = 5, f = 1kHz		0.006		%
OUTPUT						
Voltage Output Swing from Rail[1]		R_L = 100kΩ, A_{OL} ≥ 96dB		1		mV
		R_L = 100kΩ, A_{OL} ≥ 104dB		3	10	mV
Over Temperature		**R_L = 100kΩ, A_{OL} ≥ 100dB**			**10**	mV
		R_L = 5kΩ, A_{OL} ≥ 96dB		40	400	mV
Over Temperature		**R_L = 5kΩ, A_{OL} ≥ 90dB**			**400**	mV
Short-Circuit Current	I_{SC}			±15		mA
Capacitive Load Drive	C_{LOAD}			See Typical Curve		
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		5.5	V
Operating Voltage Range				2.5 to 5.5		V
Quiescent Current (per amplifier)	I_Q	V_S = 5.5V, I_O = 0		150	250	µA
Over Temperature					**300**	µA
TEMPERATURE RANGE						
Specified Range			–40		85	°C
Operating Range			–55		125	°C
Storage Range			–65		150	°C
Thermal Resistance	θ_{JA}					
SOT23-5 Surface Mount				200		°C/W
MSOP-8 Surface Mount				150		°C/W
SO-8 Surface Mount				150		°C/W
TSSOP-14 Surface Mount				100		°C/W
SO-14 Surface Mount				100		°C/W

NOTE: (1) Output voltage swings are measured between the output and power-supply rails.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V-	7.5V
Signal Input Terminals, Voltage[2]	(V–) –0.5V to (V+) +0.5V
Current[2]	10mA
Output Short-Circuit[3]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Tolerance (Human Body Model)	4000V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

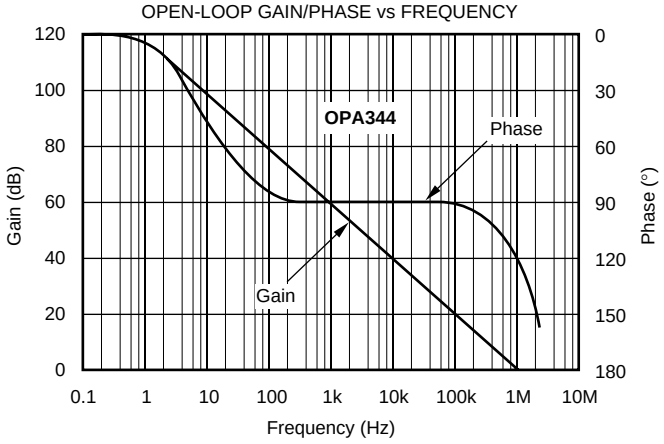
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
OPA344NA	SOT23-5	331	–40°C to +85°C	B44	OPA344NA/250	Tape and Reel
"	"	"	"	"	OPA344NA/3K	Tape and Reel
OPA344UA	SO-8	182	–40°C to +85°C	OPA344UA	OPA344UA	Rails
"	"	"	"	"	OPA344UA/2K5	Tape and Reel
OPA344PA	8-Pin Dip	006	–40° C to +85°C	OPA344PA	OPA344PA	Rails
OPA2344EA	MSOP-8	337	–40°C to +85°C	C44	OPA2344EA/250	Tape and Reel
"	"	"	"	"	OPA2344EA/2K5	Tape and Reel
OPA2344UA	SO-8	182	–40°C to +85°C	OPA2344UA	OPA2344UA	Rails
"	"	"	"	"	OPA2344UA/2K5	Tape and Reel
OPA2344PA	8-Pin DIP	006	–40°C to +85°C	OPA2344PA	OPA2344PA	Rails
OPA4344EA	TSSOP-14	357	–40°C to +85°C	OPA4344EA	OPA4344EA/250	Rails
"	"	"	"	"	OPA4344EA/2K5	Tape and Reel
OPA4344UA	SO-14	235	–40°C to +85°C	OPA4344UA	OPA4344UA	Rails
"	"	"	"	"	OPA4344UA/2K5	Tape and Reel
OPA4344PA	14-Pin DIP	010	–40°C to +85°C	OPA4344PA	OPA4344PA	Rails
OPA345NA	SOT23-5	331	–40°C to +85°C	A45	OPA345NA/250	Tape and Reel
"	"	"	"	"	OPA345NA/3K	Tape and Reel
OPA345UA	SO-8	182	–40°C to +85°C	OPA345UA	OPA345UA	Rails
"	"	"	"	"	OPA345UA/2K5	Tape and Reel
OPA2345EA	MSOP-8	337	–40°C to +85°C	B45	OPA2345EA/250	Tape and Reel
"	"	"	"	"	OPA2345EA/2K5	Tape and Reel
OPA2345UA	SO-8	182	–40°C to +85°C	OPA2345UA	OPA2345UA	Rails
"	"	"	"	"	OPA2345UA/2K5	Tape and Reel
OPA4345EA	TSSOP-14	357	–40°C to +85°C	OPA4345EA	OPA4345EA/250	Tape and Reel
"	"	"	"	"	OPA4345EA/2K5	Tape and Reel
OPA4345UA	SO-14	235	–40°C to +85°C	OPA4345UA	OPA4345UA	Rails
"	"	"	"	"	OPA4345UA/2K5	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA344UA/2K5" will get a single 2500-piece Tape and Reel.

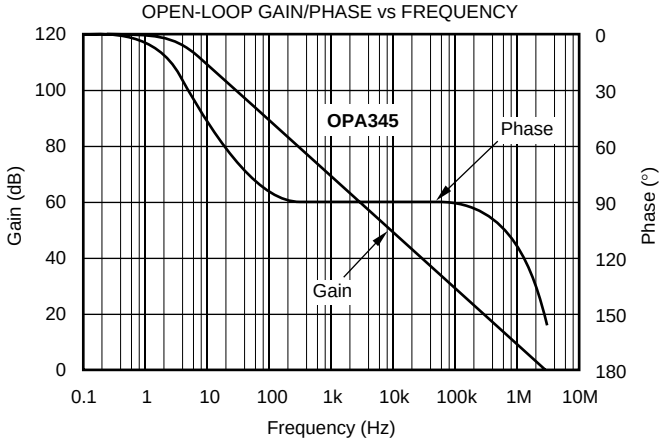
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +5V, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.

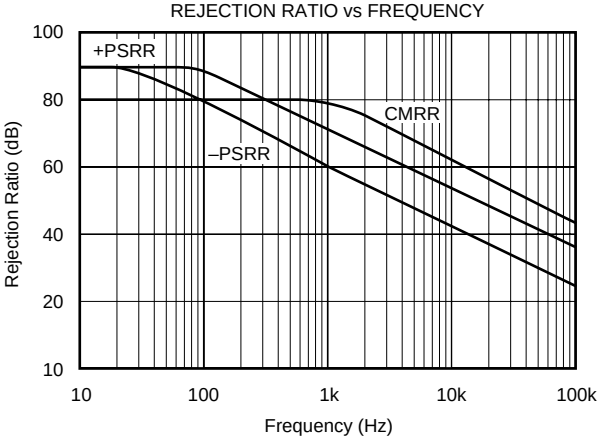
OPEN-LOOP GAIN/PHASE vs FREQUENCY



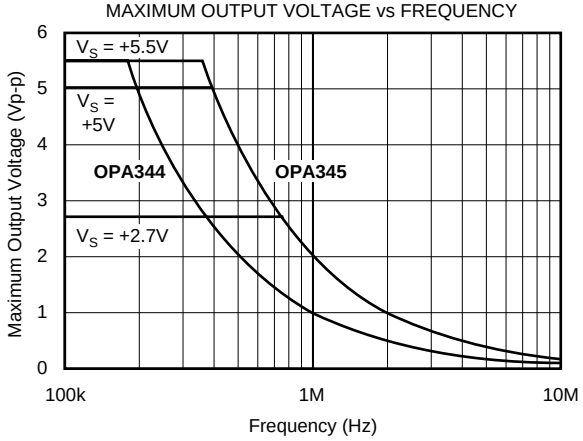
OPEN-LOOP GAIN/PHASE vs FREQUENCY



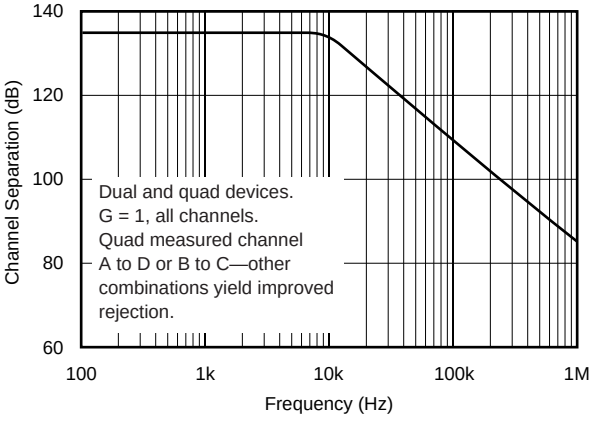
POWER SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY



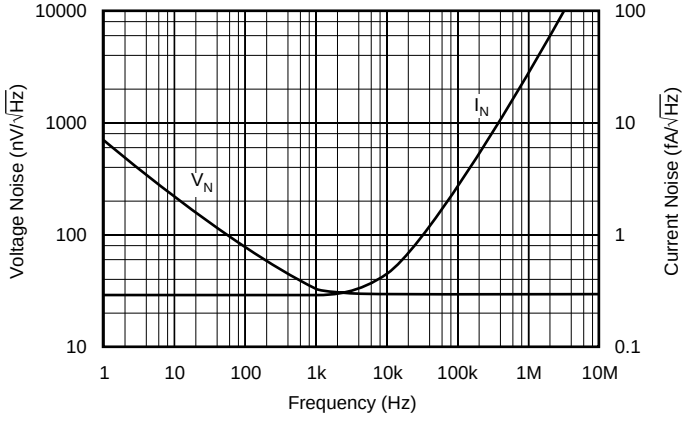
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



CHANNEL SEPARATION vs FREQUENCY



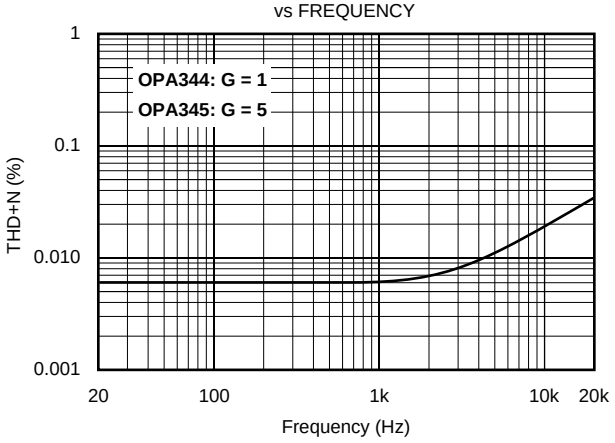
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



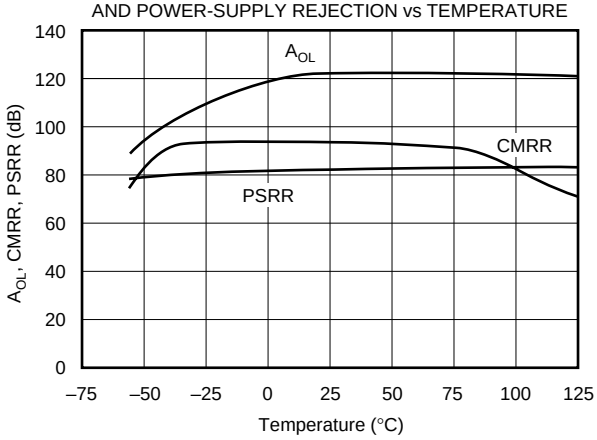
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.

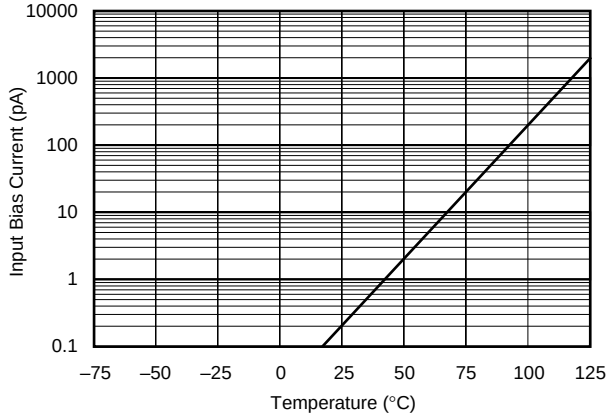
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



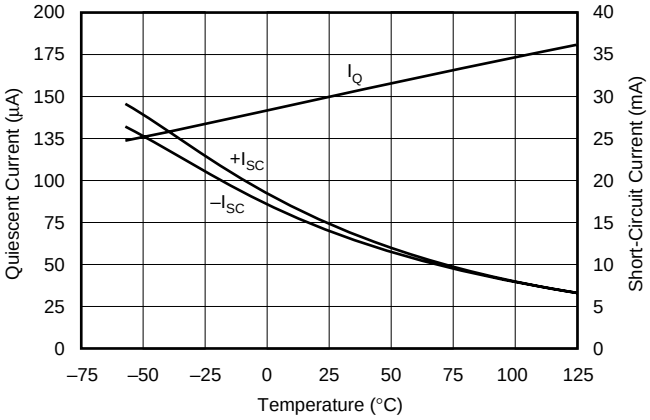
OPEN-LOOP GAIN, COMMON-MODE REJECTION RATIO, AND POWER-SUPPLY REJECTION vs TEMPERATURE



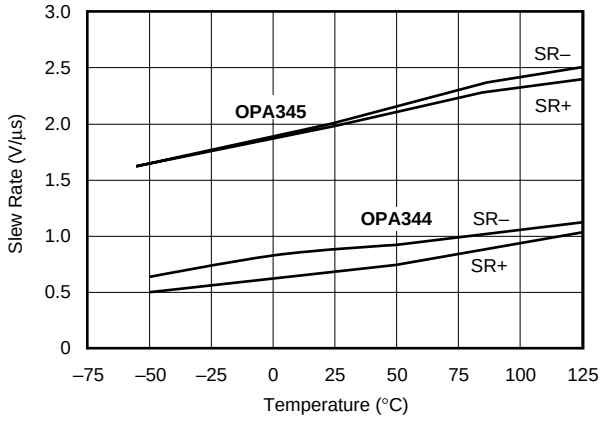
INPUT BIAS CURRENT vs TEMPERATURE



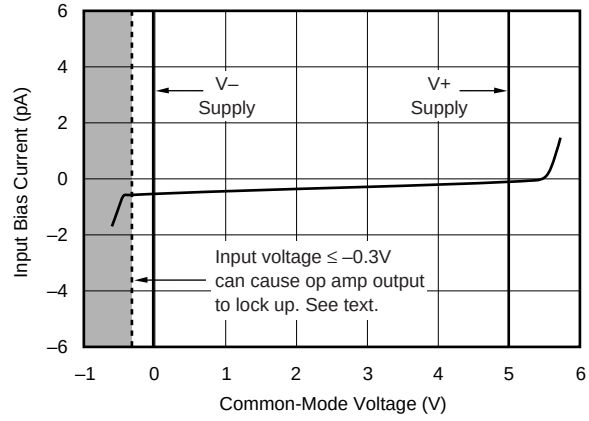
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



SLEW RATE vs TEMPERATURE



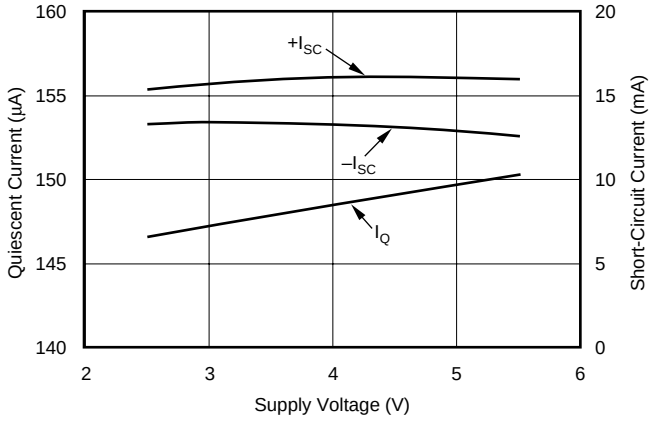
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



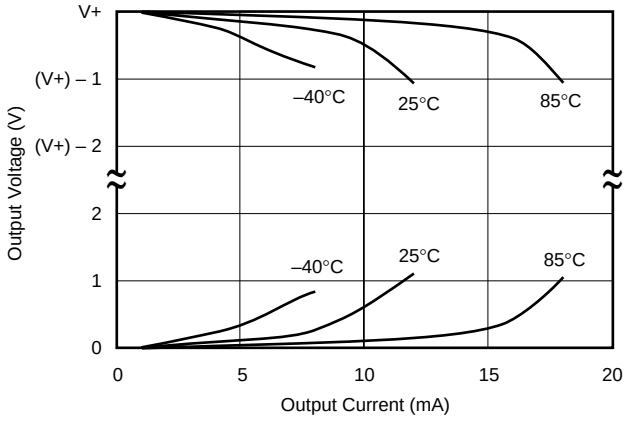
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.

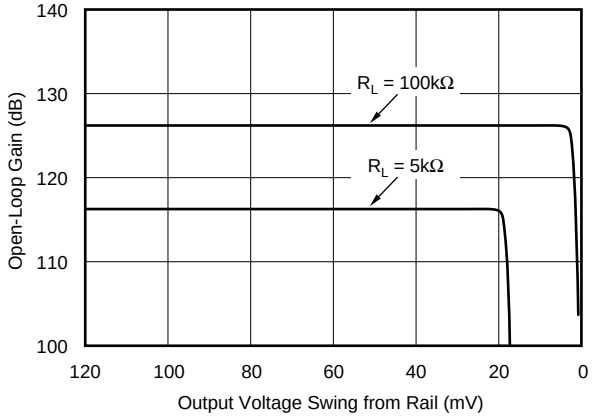
QUIESCENT CURRENT AND
SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE



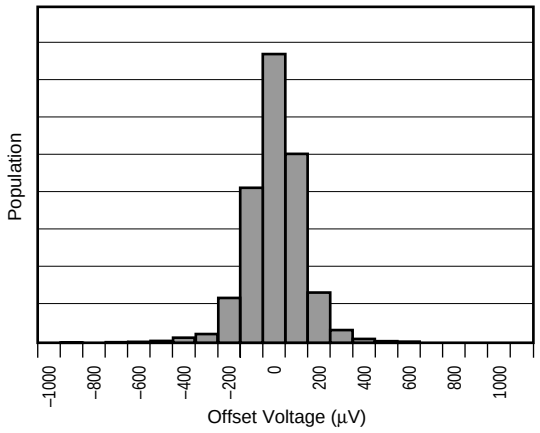
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



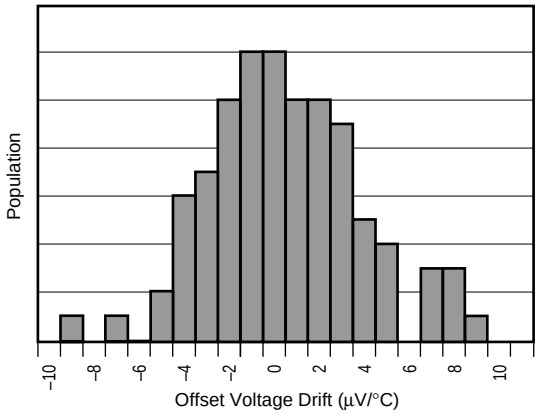
OPEN-LOOP GAIN vs OUTPUT VOLTAGE SWING



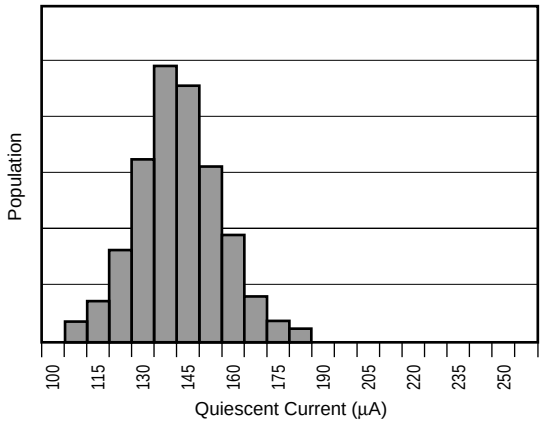
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



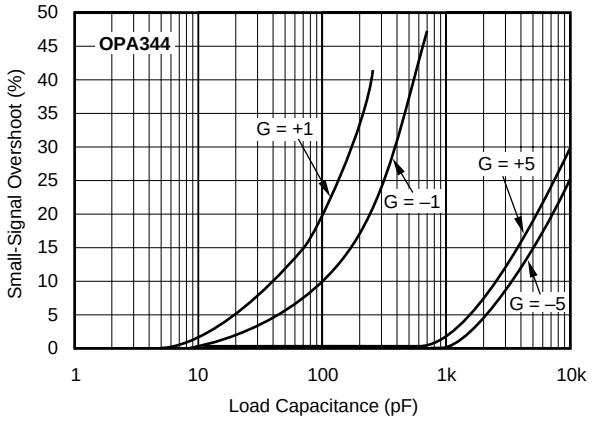
QUIESCENT CURRENT
PRODUCTION DISTRIBUTION



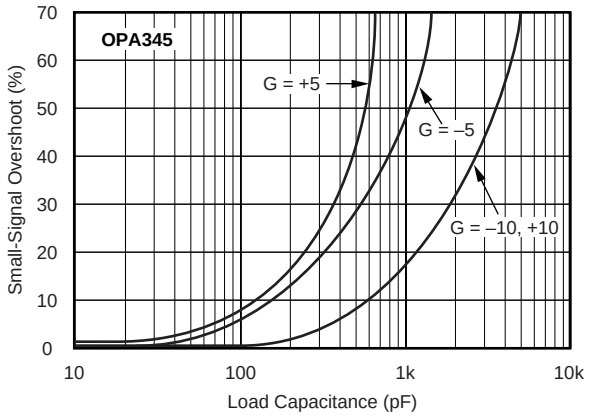
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.

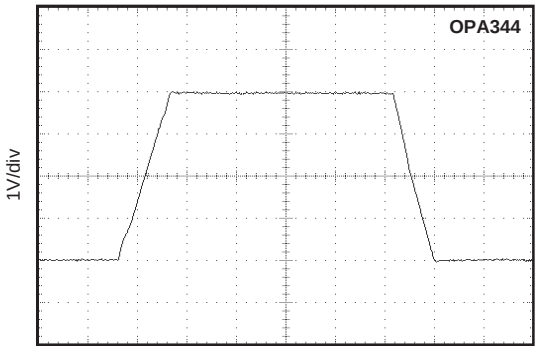
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



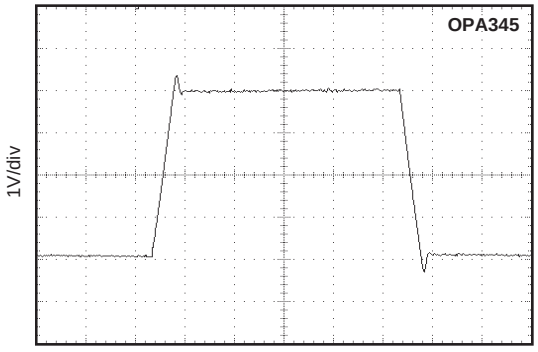
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



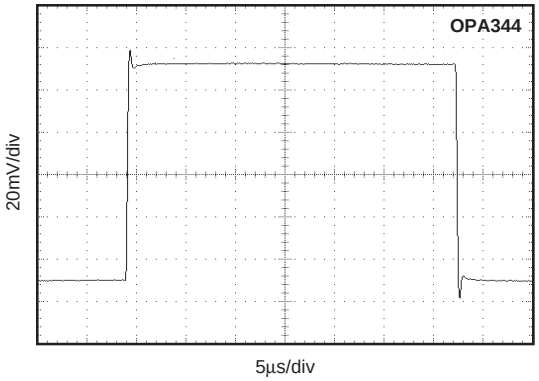
LARGE-SIGNAL STEP RESPONSE: OPA344
G = +1, R_L = 10kΩ, C_L = 100pF



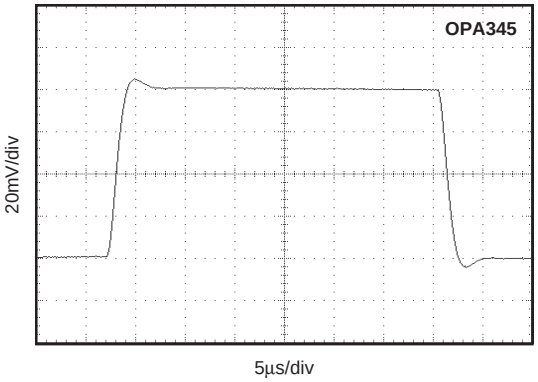
LARGE-SIGNAL STEP RESPONSE: OPA345
G = +5, R_L = 10kΩ, C_L = 100pF



SMALL-SIGNAL STEP RESPONSE: OPA344
G = +1, R_L = 10kΩ, C_L = 100pF



SMALL-SIGNAL STEP RESPONSE: OPA345
G = +5, R_L = 10kΩ, C_L = 100pF



APPLICATIONS INFORMATION

OPA344 series op amps are unity gain stable and can operate on a single supply, making them highly versatile and easy to use. OPA345 series op amps are optimized for applications requiring higher speeds with gains of 5 or greater.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low supply applications. Figure 1 shows the input and output waveforms for the OPA344 in unity-gain configuration. Operation is from V_S = +5V with a 10kΩ load connected to V_S/2. The input is a 5Vp-p sinusoid. Output voltage is approximately 4.997Vp-p.

Power supply pins should be by passed with 0.01pF ceramic capacitors.

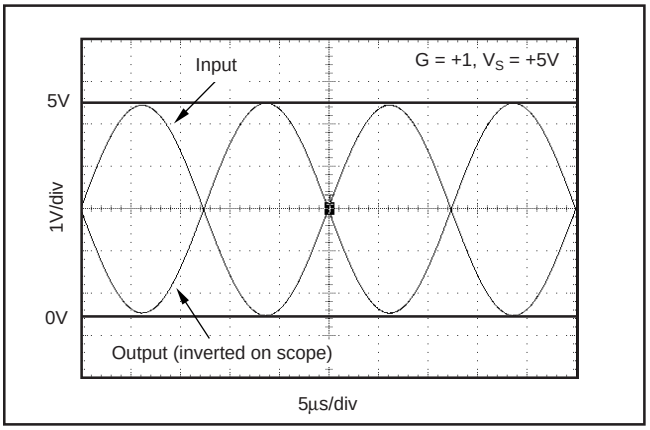


FIGURE 1. Rail-to-Rail Input and Output.

OPERATING VOLTAGE

OPA344 and OPA345 series op amps are fully specified and guaranteed from +2.7V to +5.5V. In addition, many specifications apply from –40°C to +85°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Performance Curves.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA344 and OPA345 series extends 300mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair (see Figure 2). The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3V to 300mV above the positive supply, while the P-channel pair is on for inputs from 300mV below the negative supply to approximately (V+) –1.3V. There is a small transition region, typically (V+) – 1.5V to (V+) – 1.1V, in which both pairs are on. This 400mV transition region can vary 300mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.8V to (V+) – 1.4V on the low end, up to (V+) – 1.2V to (V+) – 0.8V on the high end. Within the 400mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region. For more information on designing with rail-to-rail input op amps, see Figure 3 “Design Optimization with Rail-to-Rail Input Op Amps.”

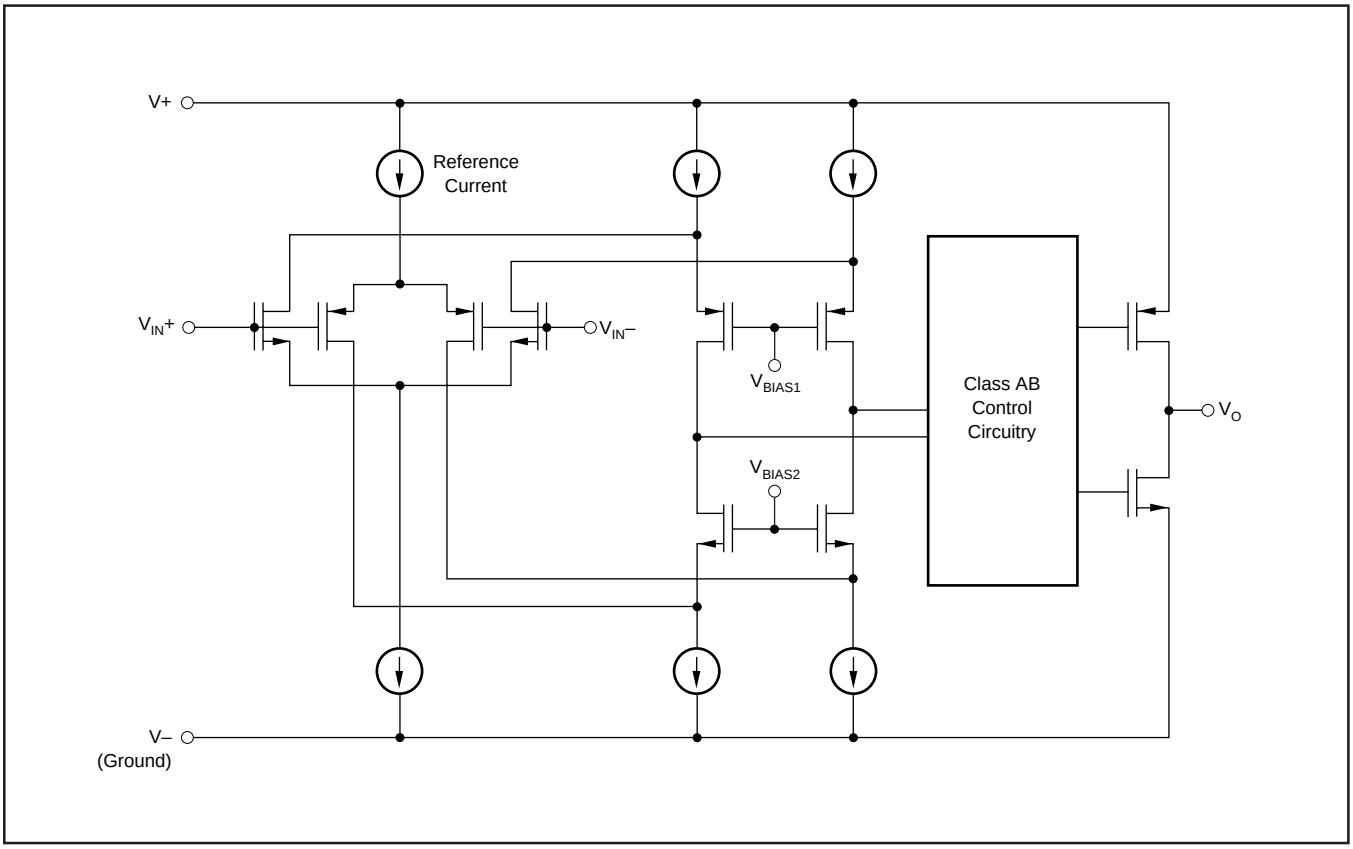


FIGURE 2. Simplified Schematic.

DESIGN OPTIMIZATION WITH RAIL-TO-RAIL INPUT OP AMPS

Rail-to-rail op amps can be used in virtually any op amp configuration. To achieve optimum performance, however, applications using these special double-input-stage op amps may benefit from consideration of their special behavior.

In many applications, operation remains within the common-mode range of only one differential input pair. However some applications exercise the amplifier through the transition region of both differential input stages. Although the two input stages are laser trimmed for excellent matching, a small discontinuity may occur in this transition. Careful selection of the circuit configuration, signal levels and biasing can often avoid this transition region.

With a unity-gain buffer, for example, signals will traverse this transition at approximately 1.3V below V+ supply and may exhibit a small discontinuity at this point.

The common-mode voltage of the non-inverting amplifier is equal to the input voltage. If the input signal always remains less than the transition voltage, no discontinuity will be created. The closed-loop gain of this configuration can still produce a rail-to-rail output.

Inverting amplifiers have a constant common-mode voltage equal to V_B. If this bias voltage is constant, no discontinuity will be created. The bias voltage can generally be chosen to avoid the transition region.

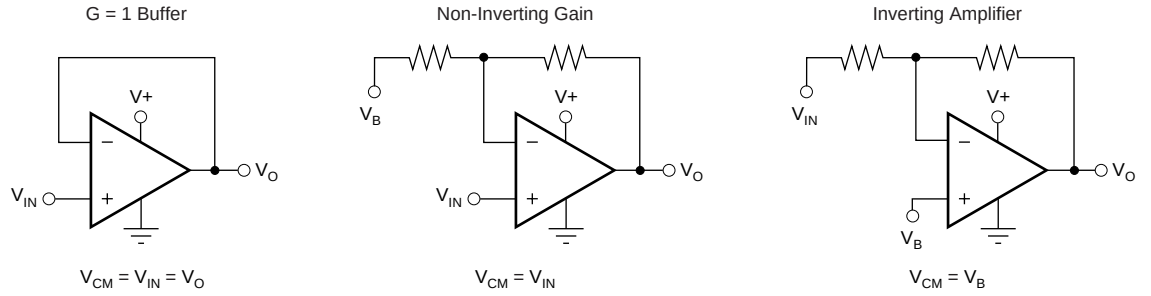


FIGURE 3. Design Optimization with Rail-to-Rail Input Op Amps.

COMMON-MODE REJECTION

The CMRR for the OPA344 and OPA345 is specified in several ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region (V_{CM} < (V+) – 1.8V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at V_S = 5.5V over the entire common-mode range is specified. Third, the CMRR at V_S = 2.7V over the entire common-mode range is provided. These last two values include the variations seen through the transition region.

INPUT VOLTAGE BEYOND THE RAILS

If the input voltage can go more than 0.3V below the negative power supply rail (single-supply ground), special precautions are required. If the input voltage goes sufficiently negative, the op amp output may lock up in an inoperative state. A Schottky diode clamp circuit will prevent this—see Figure 4. The series resistor prevents excessive current (greater than 10mA) in the Schottky diode and in the internal ESD protection diode, if the input voltage can exceed the positive supply voltage. If the signal source is limited to less than 10mA, the input resistor is not required.

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving 600Ω loads connected to any potential between V+ and ground. For light resistive loads (> 50kΩ), the output voltage can typically swing to within 1mV from supply rail. With moderate resistive loads (2kΩ to 50kΩ), the output can swing to within a few tens of milli-volts from the supply rails while maintaining high open-loop gain. See the typical performance curve "Output Voltage Swing vs Output Current."

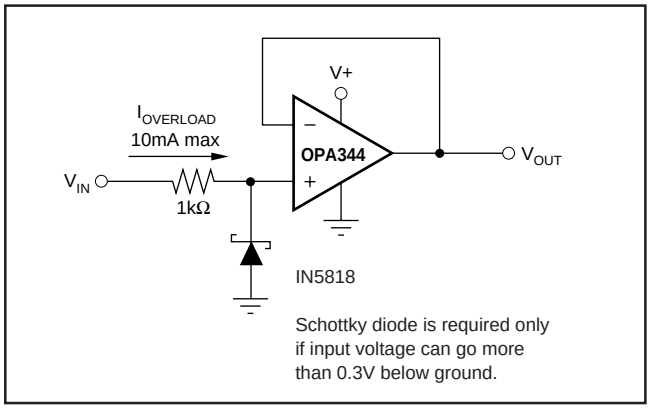


FIGURE 4. Input Current Protection for Voltages Exceeding the Supply Voltage.

CAPACITIVE LOAD AND STABILITY

The OPA344 in a unity-gain configuration and the OPA345 in gains greater than 5 can directly drive up to 250pF pure capacitive load. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. See the typical

performance curve "Small-Signal Overshoot vs Capacitive Load." In unity-gain configurations, capacitive load drive can be improved by inserting a small (10Ω to 20Ω) resistor, R_S, in series with the output, as shown in Figure 5. This significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a dc error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L, and is generally negligible.

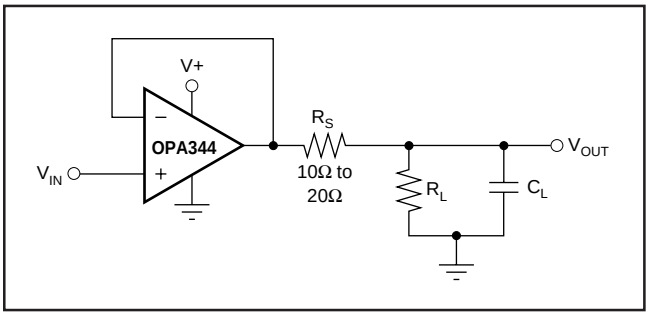


FIGURE 5. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive.

DRIVING A/D CONVERTERS

The OPA344 and OPA345 series op amps are optimized for driving medium-speed sampling A/D converters. The OPA344 and OPA345 op amps buffer the A/D's input capacitance and resulting charge injection while providing signal gain.

Figures 6 shows the OPA344 in a basic noninverting configuration driving the ADS7822. The ADS7822 is a 12-bit, micro-power sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPA344, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the A/D's input can be used to filter charge injection.

Figure 7 shows the OPA2344 driving an ADS7822 in a speech bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit will operate with V_S = +2.7V to +5V with less than 500µA quiescent current.

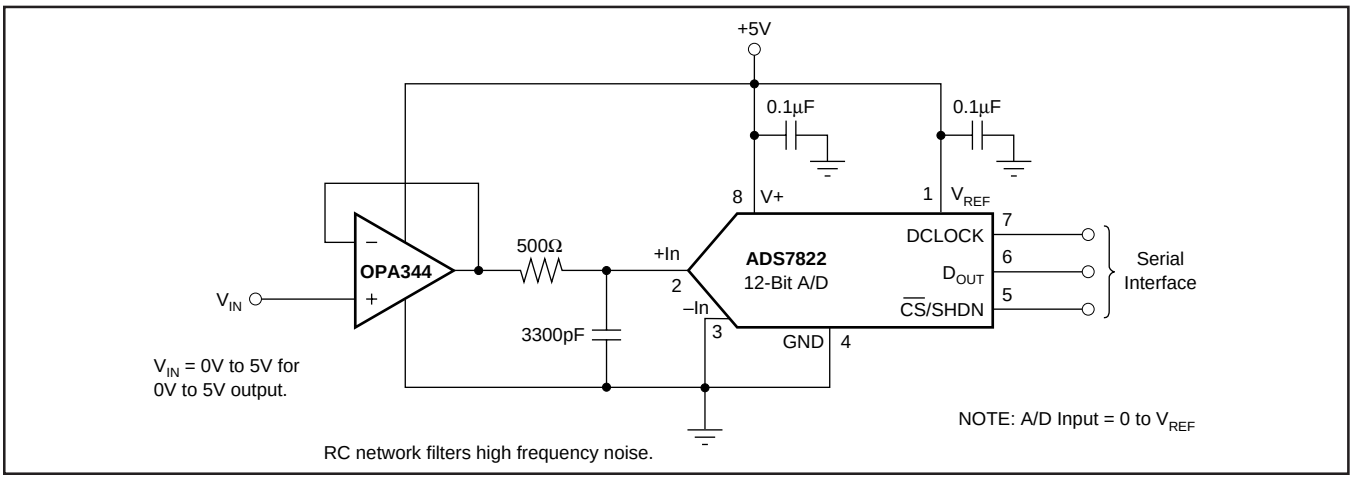


FIGURE 6. OPA344 in Noninverting Configuration Driving ADS7822.

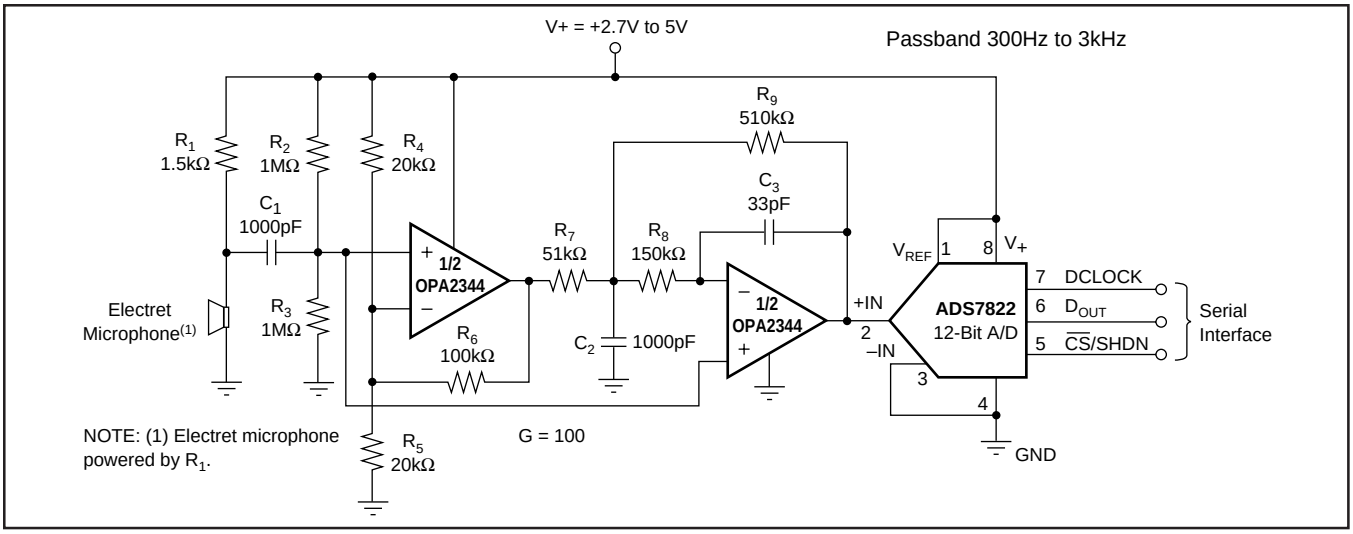


FIGURE 7. Speech Bandpass Filtered Data Acquisition System.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA2344EA/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2344EA/250G4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2344EA/2K5	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2344EA/2K5G4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2344PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2344PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2344UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2344UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2344UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2344UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2345EA/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2345EA/250G4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2345EA/2K5G4	ACTIVE	MSOP	DGK	8		TBD	Call TI	Call TI
OPA2345UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2345UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2345UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2345UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA344NA/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA344NA/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA344NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA344NA/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA344PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA344PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA344UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA344UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
OPA344UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA344UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA345NA/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA345NA/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA345NA/3KG4	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI
OPA345UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA345UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4344EA/250	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA4344EA/250G4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA4344EA/2K5	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA4344EA/2K5G4	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA4344PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4344PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4344UA	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
OPA4344UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
OPA4344UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
OPA4344UAG4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
OPA4345EA/250	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4345EA/250G4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4345UA	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA4345UA/2K5G4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI
OPA4345UAG4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

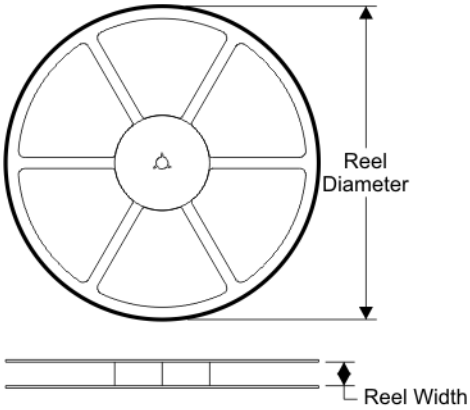
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

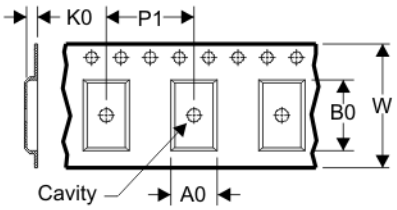
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

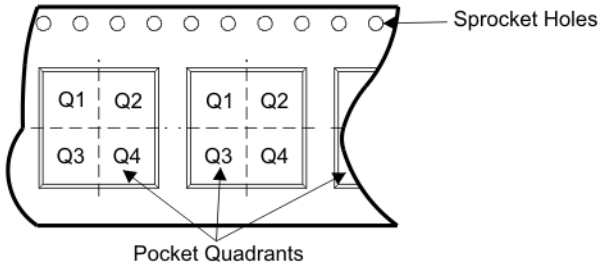


TAPE DIMENSIONS



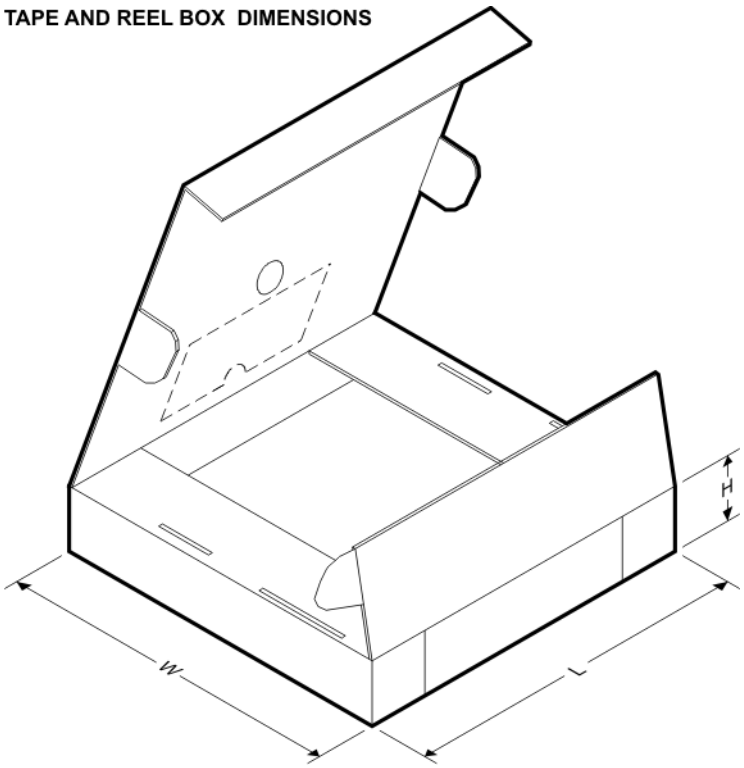
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2344EA/250	DGK	8	SITE 41	180	12	5.3	3.4	1.4	8	12	Q1
OPA2344EA/2K5	DGK	8	SITE 41	330	12	5.3	3.4	1.4	8	12	Q1
OPA2344UA/2K5	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1
OPA2345EA/250	DGK	8	SITE 41	180	12	5.3	3.4	1.4	8	12	Q1
OPA2345UA/2K5	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1
OPA344NA/250	DBV	5	SITE 41	180	8	3.2	3.1	1.39	4	8	Q3
OPA344NA/3K	DBV	5	SITE 41	180	8	3.2	3.1	1.39	4	8	Q3
OPA344UA/2K5	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1
OPA345NA/250	DBV	5	SITE 41	180	8	3.2	3.1	1.39	4	8	Q3
OPA4344EA/250	PW	14	SITE 41	180	12	7.0	5.6	1.6	8	12	Q1
OPA4344EA/2K5	PW	14	SITE 41	330	12	7.0	5.6	1.6	8	12	Q1
OPA4344UA/2K5	D	14	SITE 41	330	16	6.5	9.0	2.1	8	16	Q1
OPA4345EA/250	PW	14	SITE 67	177	12	6.95	5.6	1.6	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
OPA2344EA/250	DGK	8	SITE 41	184.0	184.0	50.0
OPA2344EA/2K5	DGK	8	SITE 41	346.0	346.0	29.0
OPA2344UA/2K5	D	8	SITE 41	346.0	346.0	29.0
OPA2345EA/250	DGK	8	SITE 41	184.0	184.0	50.0
OPA2345UA/2K5	D	8	SITE 41	346.0	346.0	29.0
OPA344NA/250	DBV	5	SITE 41	190.0	212.7	31.75
OPA344NA/3K	DBV	5	SITE 41	190.0	212.7	31.75
OPA344UA/2K5	D	8	SITE 41	346.0	346.0	29.0
OPA345NA/250	DBV	5	SITE 41	190.0	212.7	31.75
OPA4344EA/250	PW	14	SITE 41	184.0	184.0	50.0
OPA4344EA/2K5	PW	14	SITE 41	346.0	346.0	29.0
OPA4344UA/2K5	D	14	SITE 41	346.0	346.0	33.0
OPA4345EA/250	PW	14	SITE 67	187.0	187.0	25.6

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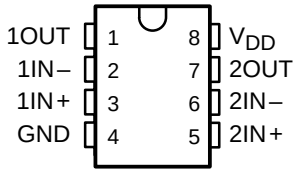
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

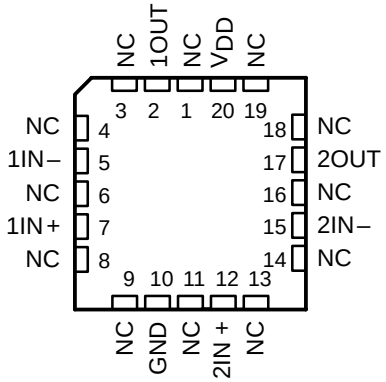
Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

- **Trimmed Offset Voltage: TLC27L7 . . . 500 μV Max at 25°C, V_{DD} = 5 V**
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  –40°C to 85°C . . . 4 V to 16 V
  –55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Ultra-Low Power . . . Typically 95 μW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)

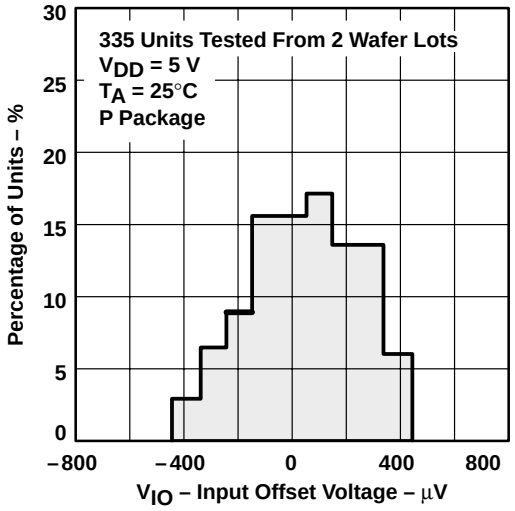


NC – No internal connection

description

The TLC27L2 and TLC27L7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

DISTRIBUTION OF TLC27L7 INPUT OFFSET VOLTAGE



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV 2 mV 5 mV 10 mV	TLC27L7CD TLC27L2BCD TLC27L2ACD TLC27L2CD	—	—	TLC27L7CP TLC27L2BCP TLC27L2ACP TLC27L2CP
–40°C to 85°C	500 μV 2 mV 5 mV 10 mV	TLC27L7ID TLC27L2BID TLC27L2AID TLC27L2ID	—	—	TLC27L7IP TLC27L2BIP TLC27L2AIP TLC27L2IP
–55°C to 125°C	500 μV 10 mV	TLC27L7MD TLC27L2MD	TLC27L7MFK TLC27L2MFK	TLC27L7MJG TLC27L2MJG	TLC27L7MP TLC27L2MP

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L7CDR).

LinCMOS is a trademark of Texas Instruments.

description (continued)

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L2 (10 mV) to the high-precision TLC27L7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L2 and TLC27L7. The devices also exhibit low voltage single-supply operation and ultra-low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

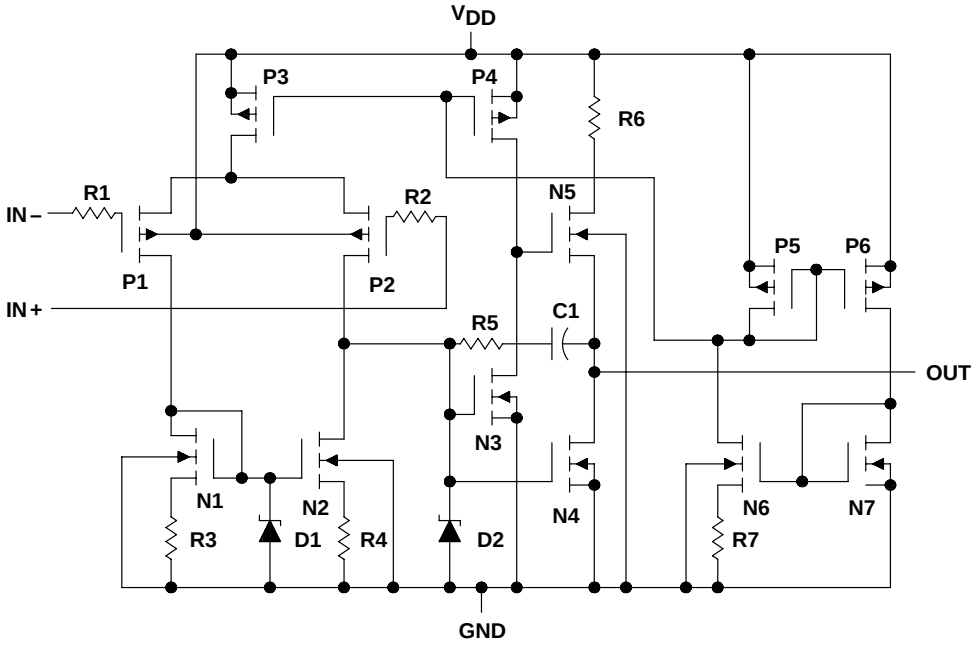
A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC27L2 and TLC27L7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-Suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . –0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} . . . . . 45 mA
Total current out of GND . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
M suffix . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	–0.2	3.5	–0.2	3.5	0	3.5	V
	V_{DD} = 10 V	–0.2	8.5	–0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2C, TLC27L2AC, TLC27L2BC, TLC27L7C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		204	2000	μV
					Full range			3000	
		TLC27L7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		170	500	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1	60	pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6	60	pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					0°C	3	4.1		
					70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	700		V/mV
					0°C	50	700		
					70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	94		dB
					0°C	60	95		
					70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		20	34	μA
					0°C		24	42	
					70°C		16	28	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2C, TLC27L2AC, TLC27L2BC, TLC27L7C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		235	2000	μV
					Full range			3000	
		TLC27L7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		190	800	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1	60	pA
					70°C		8	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7	60	pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					0°C	7.8	8.9		
					70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					0°C	50	1025		
					70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	97		dB
					0°C	60	97		
					70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	μA
					0°C		36	66	
					70°C		22	40	

† Full range is 0°C to 70°C.

NOTES: 4 The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5 This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27L2AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			7	
		TLC27L2BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		240	2000	μV
					Full range			3500	
		TLC27L7I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		170	500	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1	60	pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6	60	pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					−40°C	3	4.1		
					85°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	480		V/mV
					−40°C	50	900		
					85°C	50	330		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	94		dB
					−40°C	60	95		
					85°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		20	34	μA
					−40°C		31	54	
					85°C		15	26	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27L2AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			7	
		TLC27L2BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		235	2000	μV
					Full range			3500	
		TLC27L7I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		190	800	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1	60	pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7	60	pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−40°C	7.8	8.9		
					85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					−40°C	50	1550		
					85°C	50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	97		dB
					−40°C	60	97		
					85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	μA
					−40°C		49	86	
					85°C		20	36	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2M TLC27L7M			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		170	500	μV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1	60	pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6	60	pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					−55°C	3	4.1		
					125°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	500		V/mV
					−55°C	25	1000		
					125°C	25	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	94		dB
					−55°C	60	95		
					125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		20	34	μA
					−55°C		35	60	
					125°C		14	24	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2M TLC27L7M			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		190	800	μV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1	60	pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7	60	pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−55°C	7.8	8.8		
					125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					−55°C	25	1750		
					125°C	25	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	97		dB
					−55°C	60	97		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	μA
					−55°C		56	96	
					125°C		18	30	

† Full range is −55 °C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2C, TLC27L2AC, TLC27L2BC, TLC27L7C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2C, TLC27L2AC, TLC27L2BC, TLC27L7C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2I, TLC27L2AI, TLC27L2BI, TLC27L7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				–40°C		0.04		
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				–40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				–40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				–40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				–40°C		38°		
				85°C		29°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2I, TLC27L2AI, TLC27L2BI, TLC27L7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				–40°C		0.06		
				85°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				–40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				–40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				–40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				–40°C		42°		
				85°C		32°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2M TLC27L7M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				–55°C		0.04		
				125°C		0.02		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				–55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				–55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				–55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				–55°C		39°		
				125°C		25°		

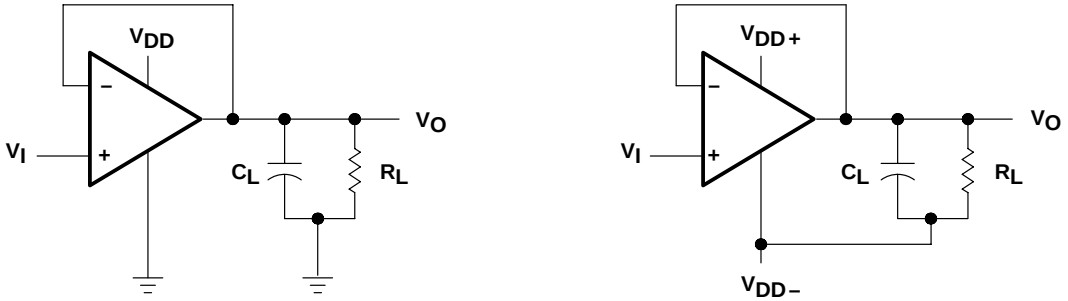
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2M TLC27L7M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				–55°C		0.06		
				125°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				–55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				–55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				–55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				–55°C		43°		
				125°C		29°		

PARAMETER MEASUREMENT INFORMATION

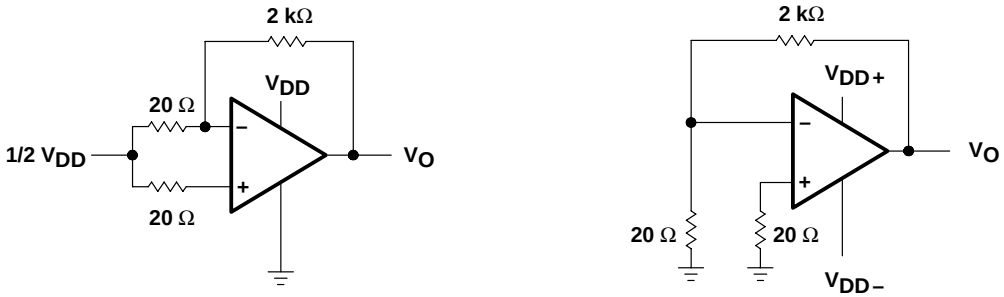
single-supply versus split-supply test circuits

Because the TLC27L2 and TLC27L7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



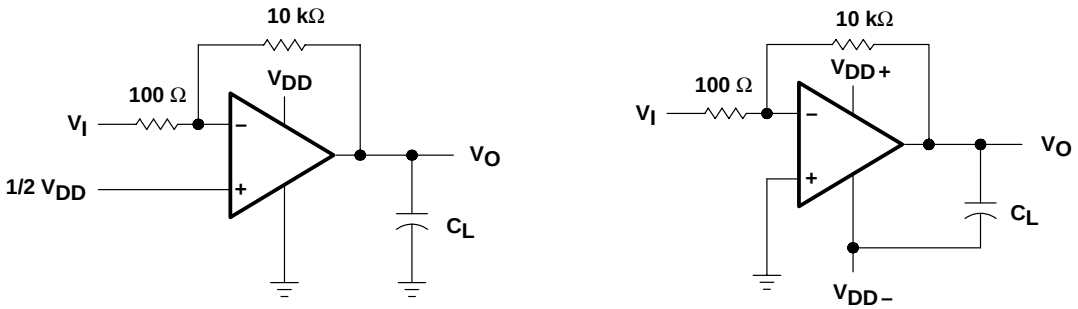
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L2 and TLC27L7 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources.Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

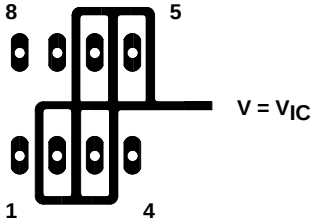


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

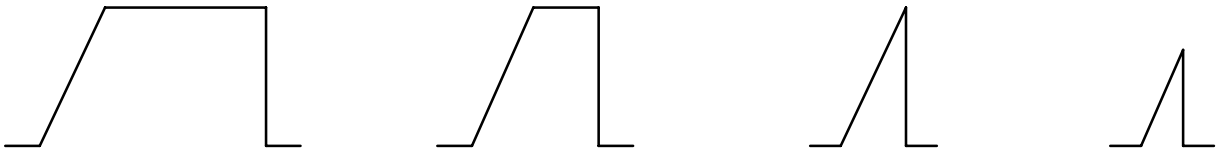
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 kHz **(b) B_{OM} > f > 100 kHz** **(c) f = B_{OM}** **(d) f > B_{OM}**

Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL}	Low-level output voltage	vs Differential input voltage vs Free-air temperature vs Low-level output current	14,16 15,17 18, 19
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I_{IB}	Input bias current	vs Free-air temperature	22
I_{IO}	Input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitive Load	34 35 36
V_n	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE**

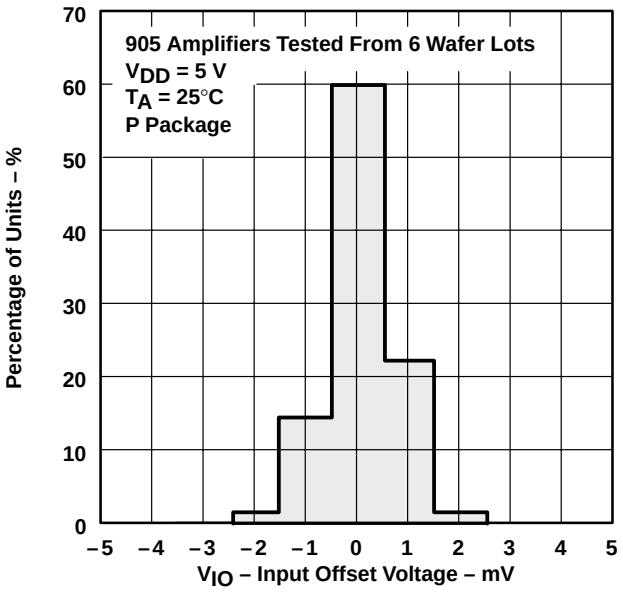


Figure 6

**DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE**

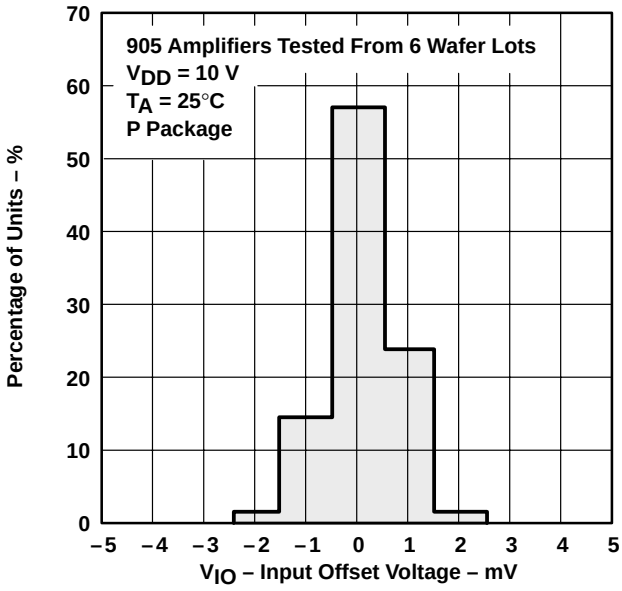


Figure 7

**DISTRIBUTION OF TLC27LC AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

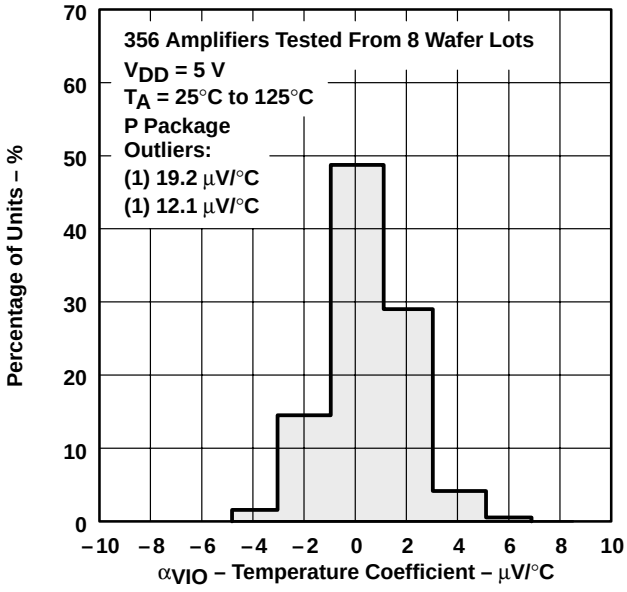


Figure 8

**DISTRIBUTION OF TLC27LC AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

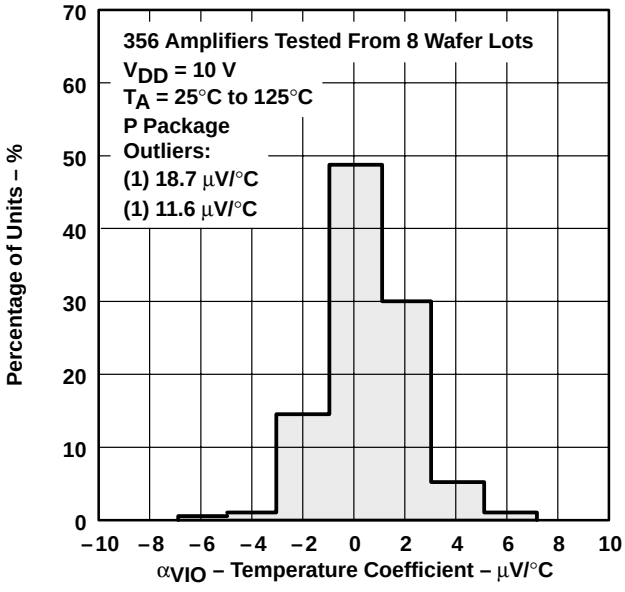


Figure 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

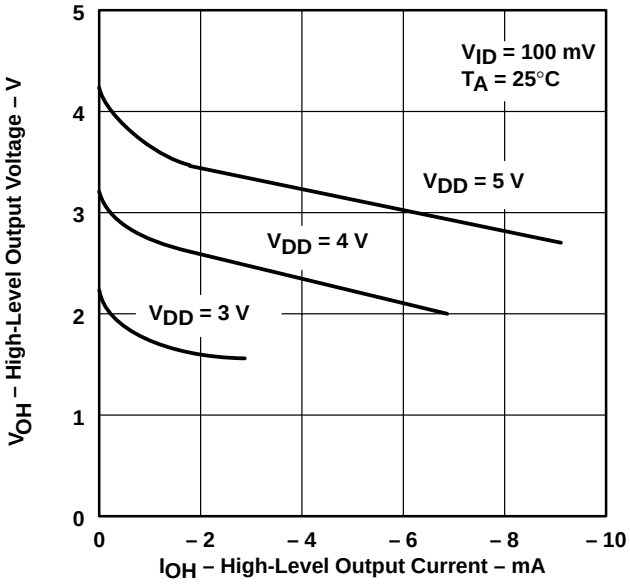


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

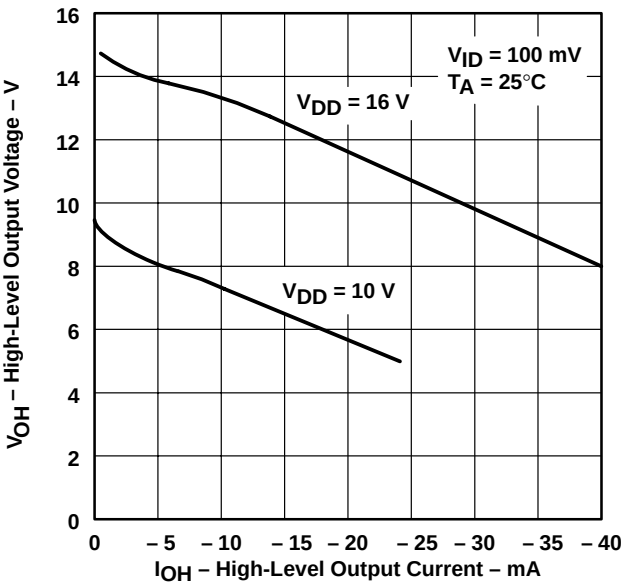


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

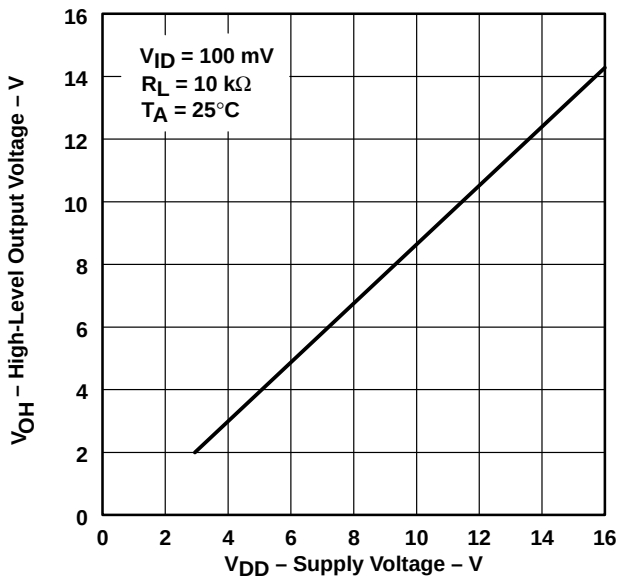


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

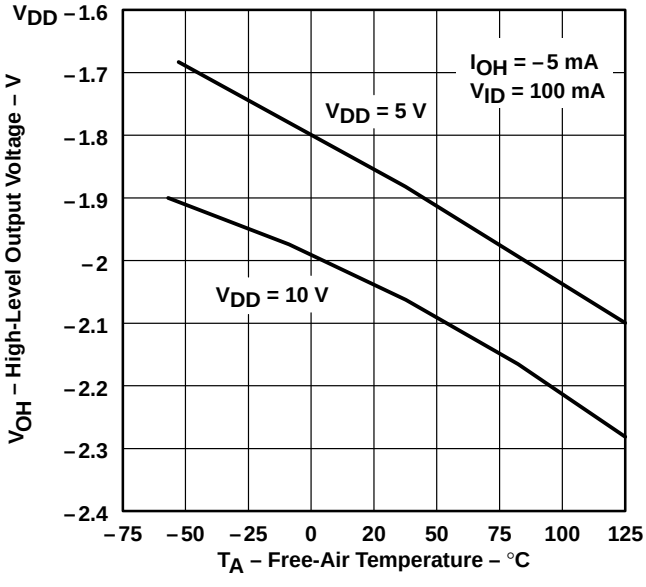


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

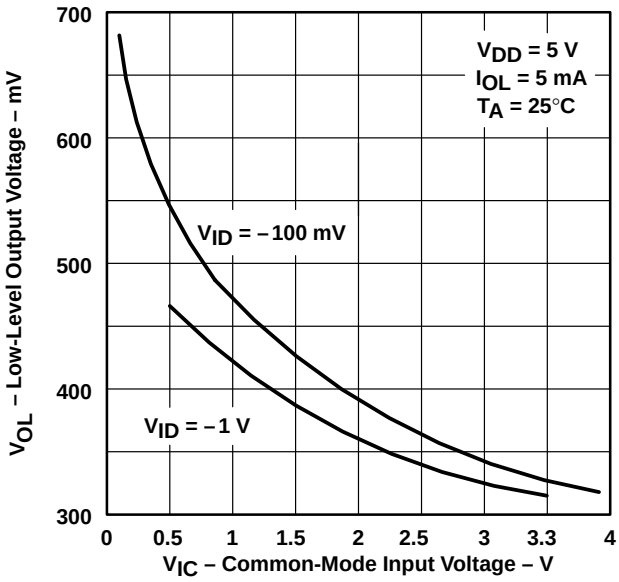


Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

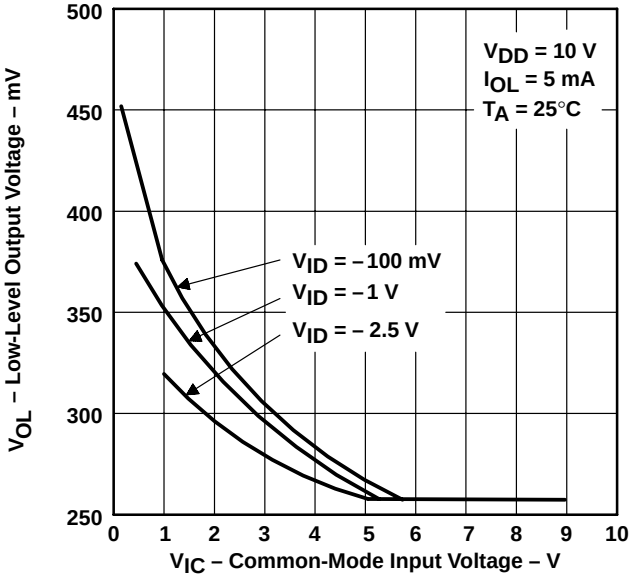


Figure 15

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

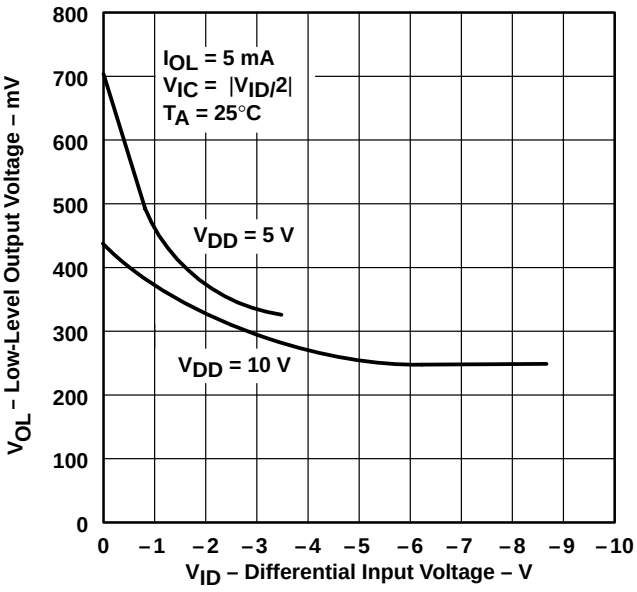


Figure 16

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

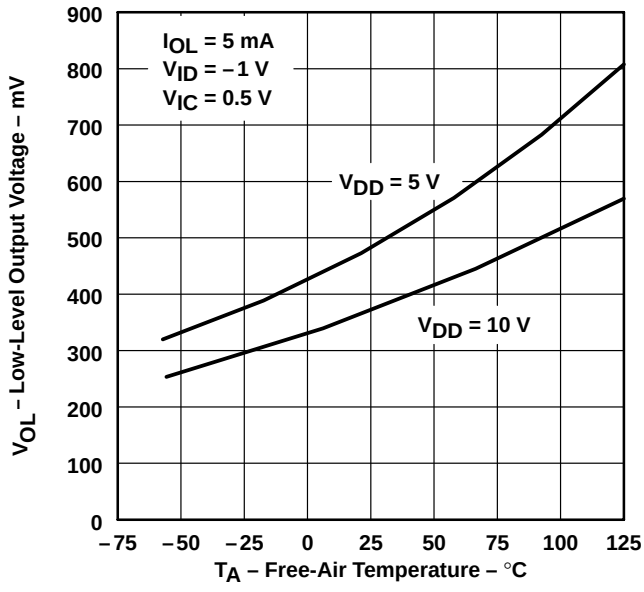


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

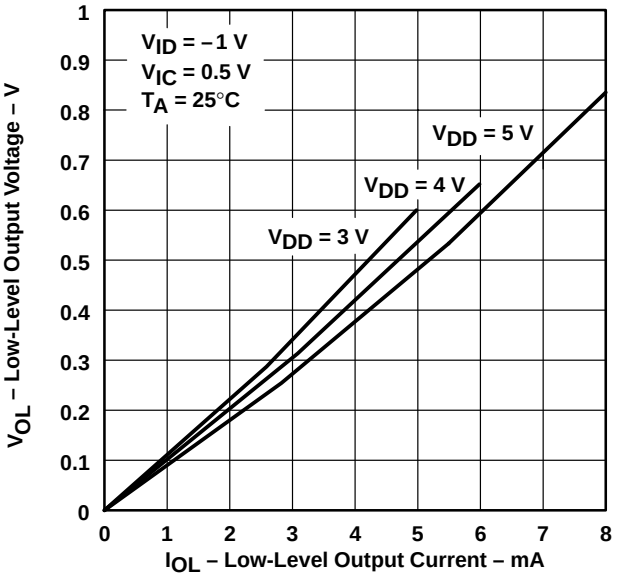


Figure 18

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

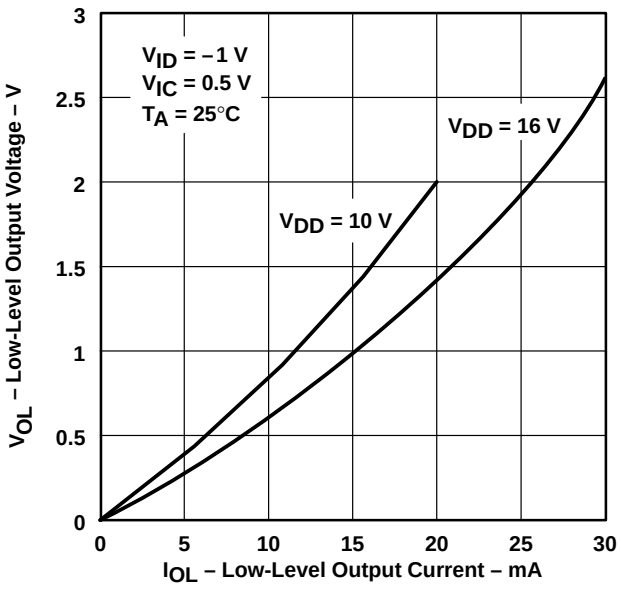


Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

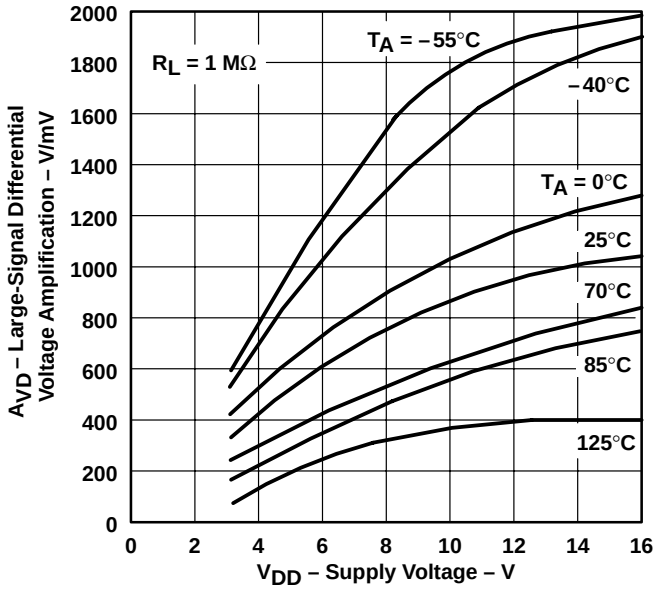


Figure 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

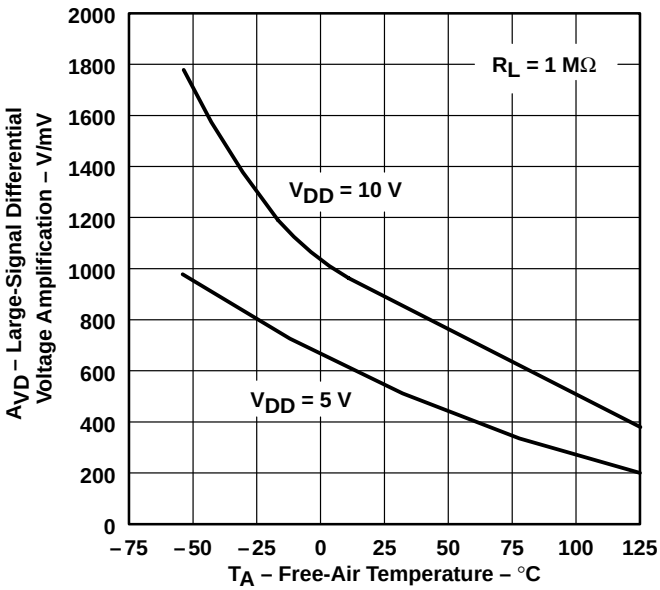
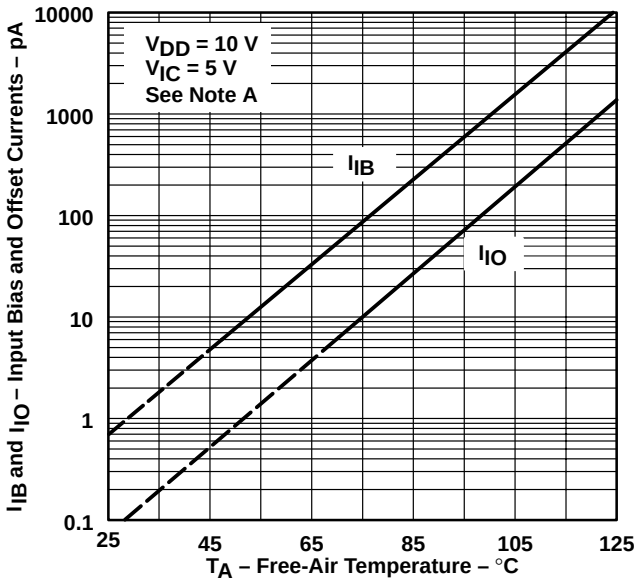


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

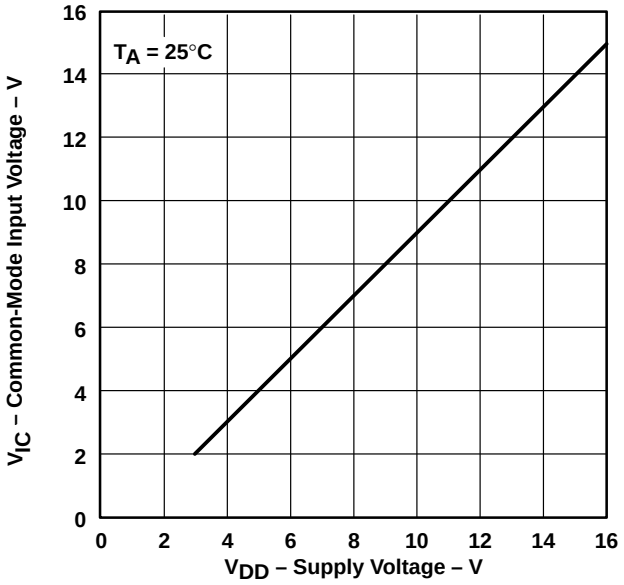


Figure 23

SUPPLY CURRENT vs SUPPLY VOLTAGE

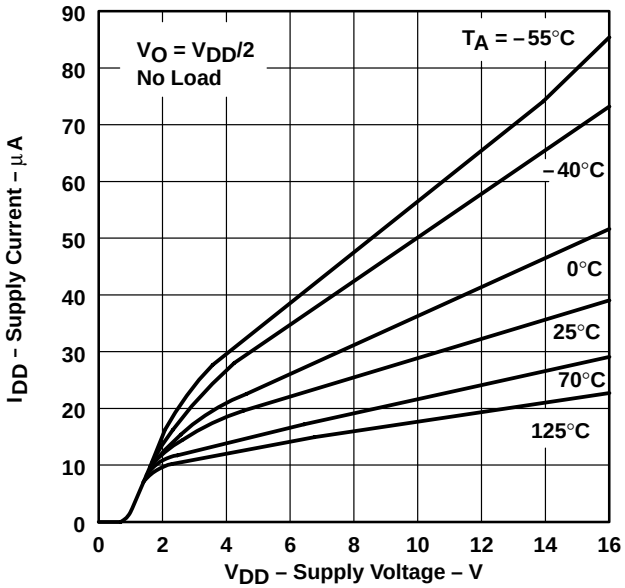


Figure 24

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

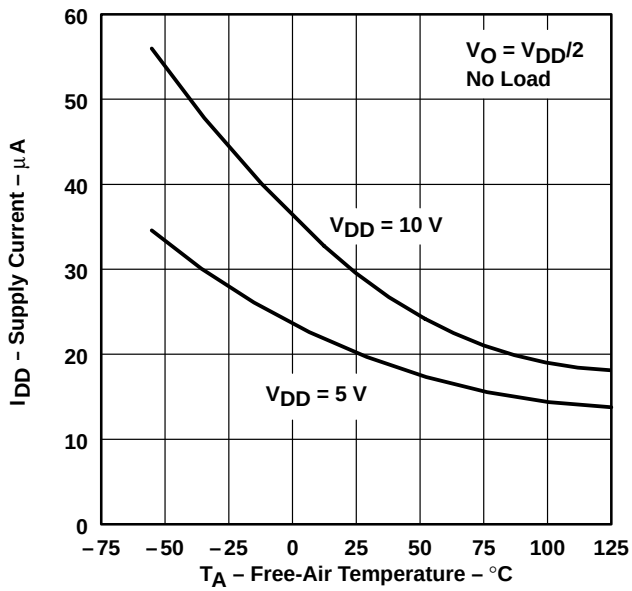


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs SUPPLY VOLTAGE

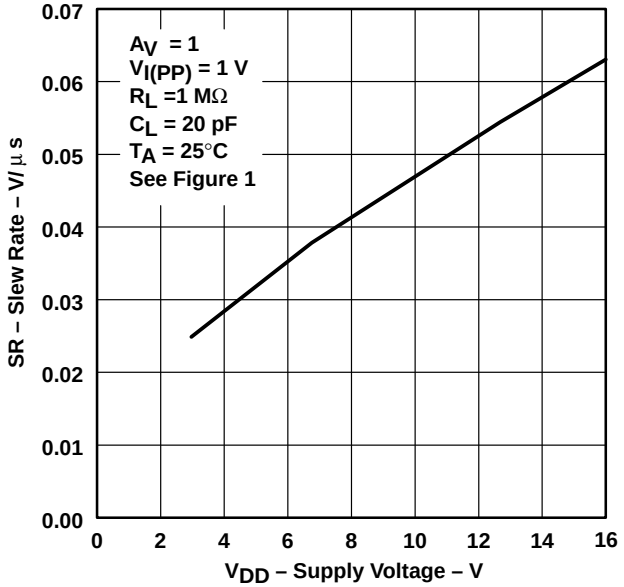


Figure 26

SLEW RATE vs FREE-AIR TEMPERATURE

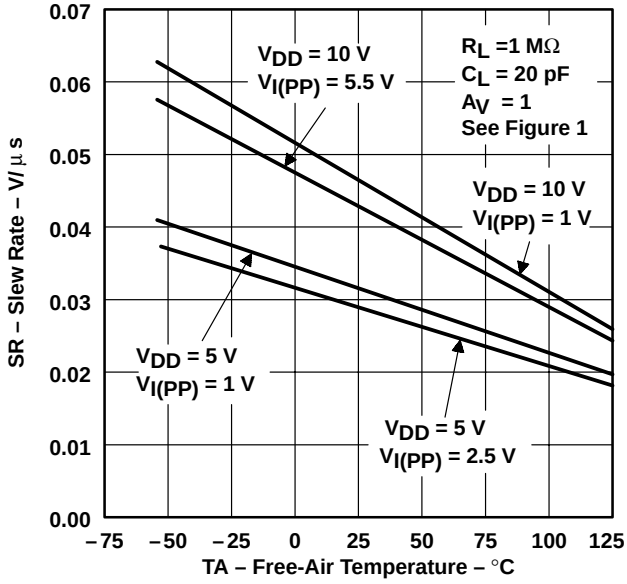


Figure 27

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

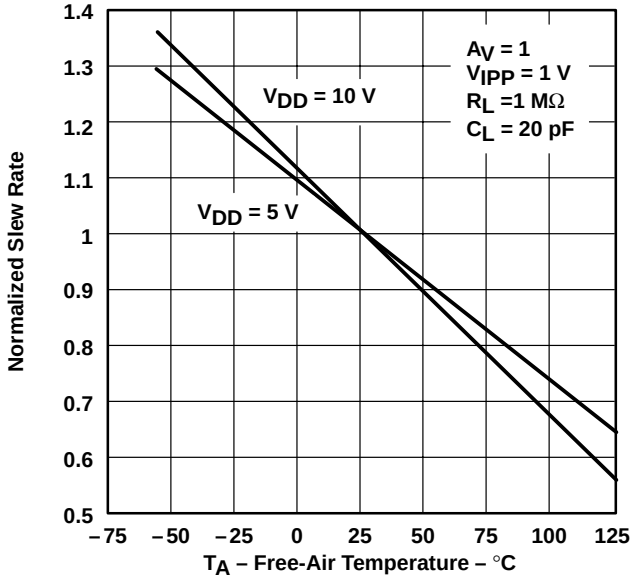


Figure 28

MAXIMUM-PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

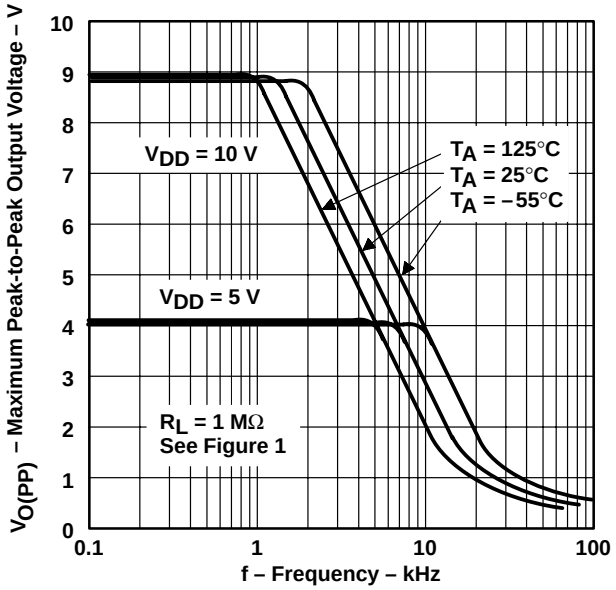


Figure 29

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

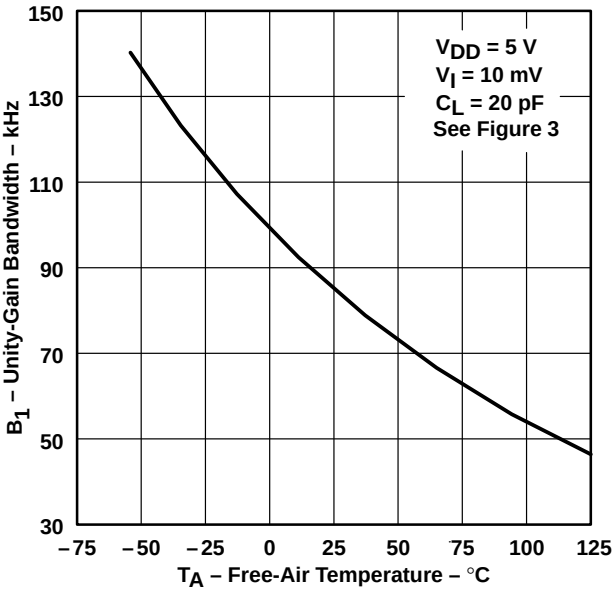


Figure 30

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

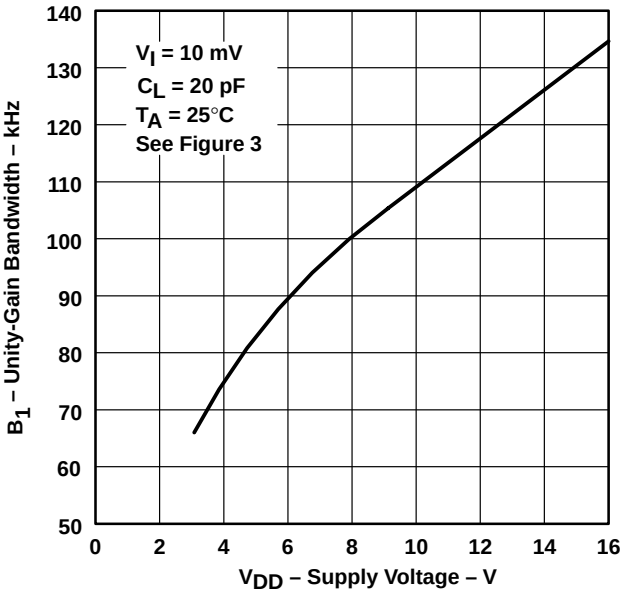


Figure 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

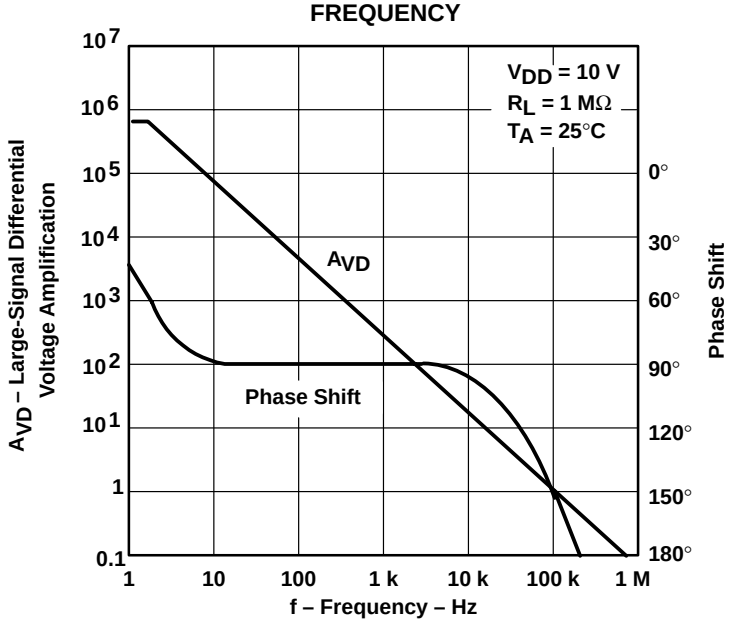


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

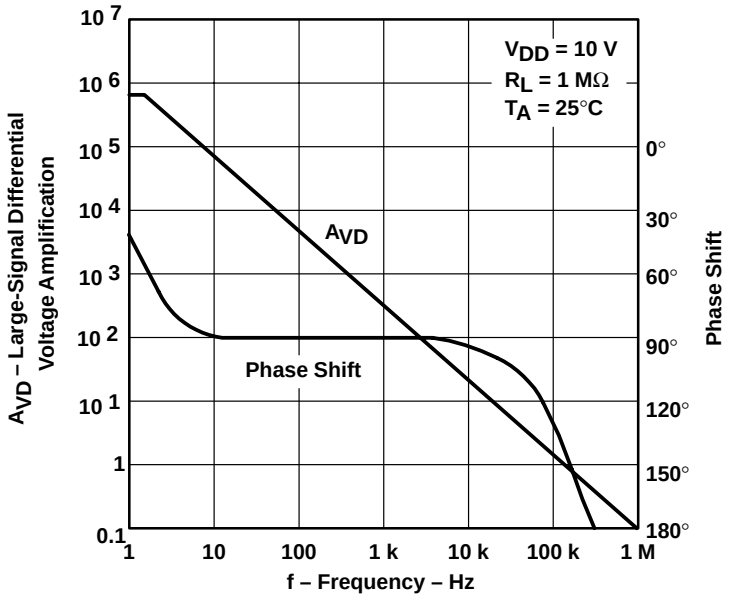


Figure 33

PHASE MARGIN vs SUPPLY VOLTAGE

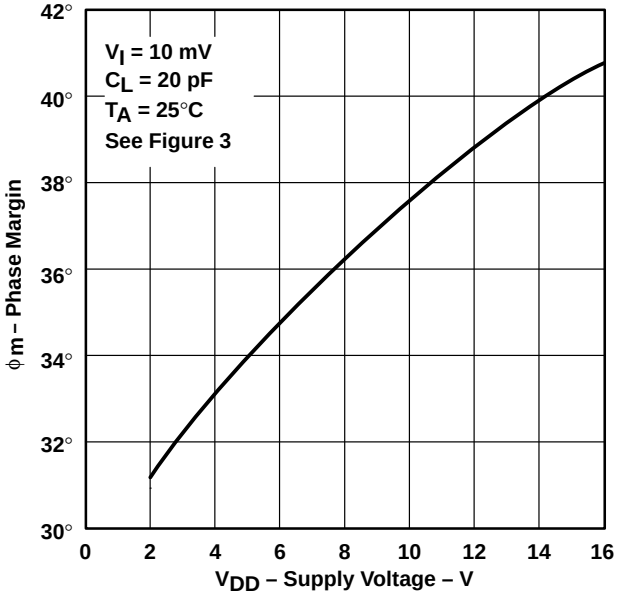


Figure 34

PHASE MARGIN vs FREE-AIR TEMPERATURE

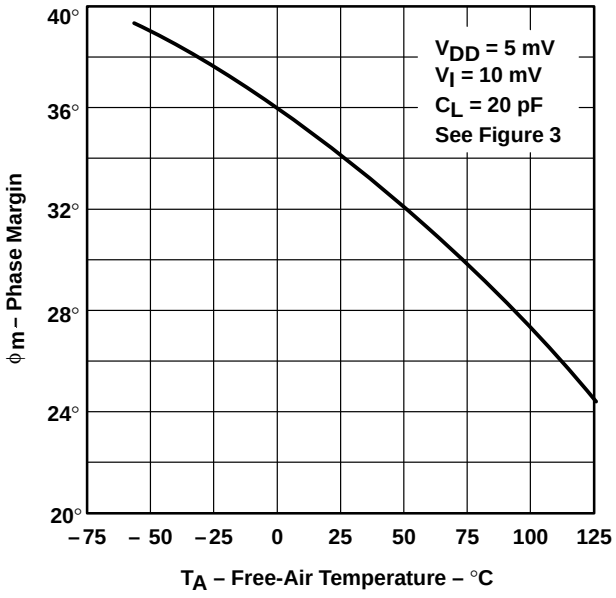


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN vs CAPACITIVE LOAD

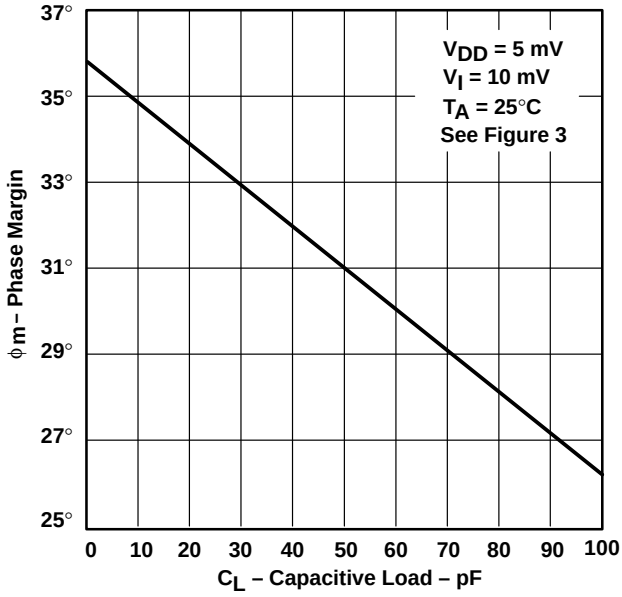


Figure 36

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

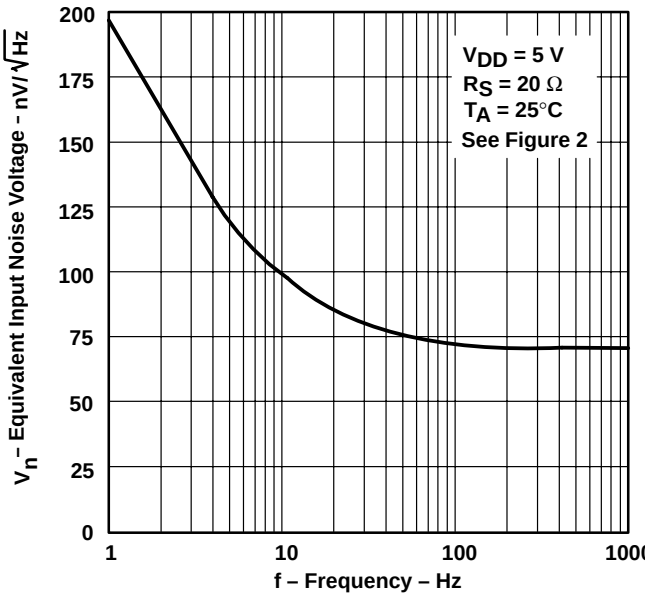


Figure 37

APPLICATION INFORMATION

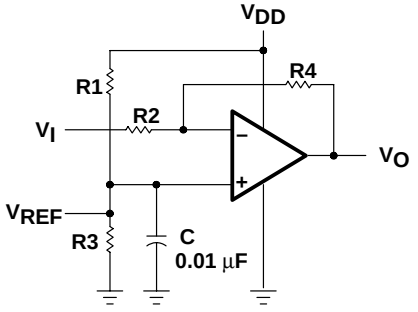
single-supply operation

While the TLC27L2 and TLC27L7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L2 and TLC27L7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L2 and TLC27L7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

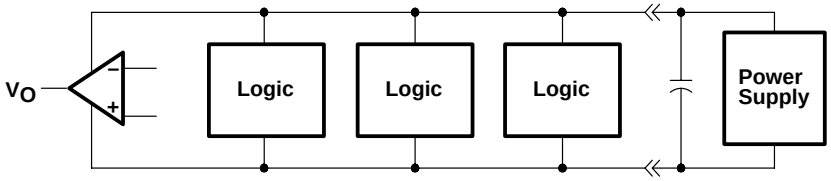
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



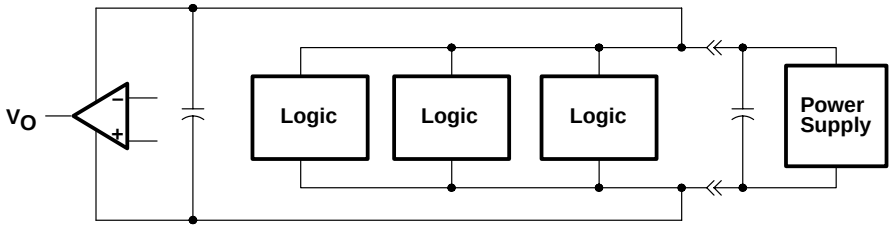
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

Figure 38. Inverting Amplifier With Voltage Reference



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common Versus Separate Supply Rails

APPLICATION INFORMATION

input characteristics

The TLC27L2 and TLC27L7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} –1 V at T_A = 25°C and at V_{DD} –1.5 V at all other temperatures.

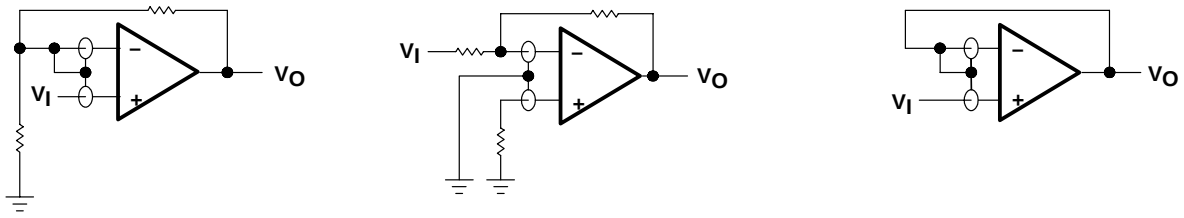
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L2 and TLC27L7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L2 and TLC27L7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L2 and TLC27L7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER **(b) INVERTING AMPLIFIER** **(c) UNITY-GAIN AMPLIFIER**

Figure 40. Guard-Ring Schemes

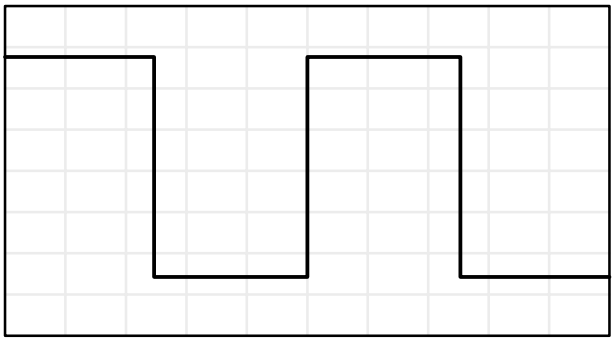
output characteristics

The output stage of the TLC27L2 and TLC27L7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27L2 and TLC27L7 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

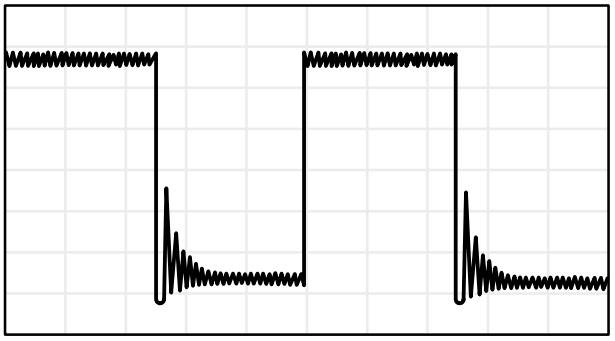
APPLICATION INFORMATION

output characteristics (continued)

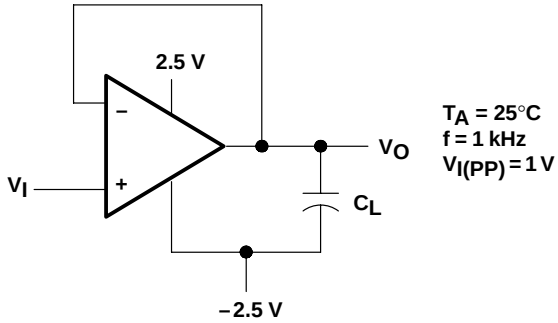


(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 260 pF, R_L = NO LOAD



(c) C_L = 310 pF, R_L = NO LOAD



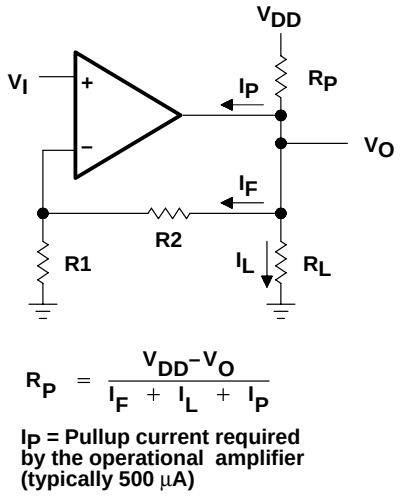
(d) TEST CIRCUIT

Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC27L2 and TLC27L7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

APPLICATION INFORMATION

output characteristics (continued)



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 μA)

Figure 42. Resistive Pullup to Increase V_{OH}

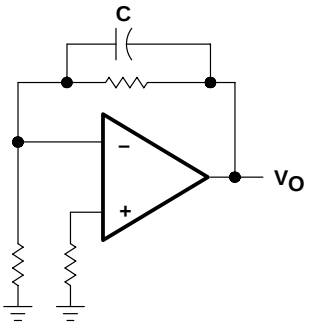


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27L2 and TLC27L7 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L2 and TLC27L7 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

APPLICATION INFORMATION

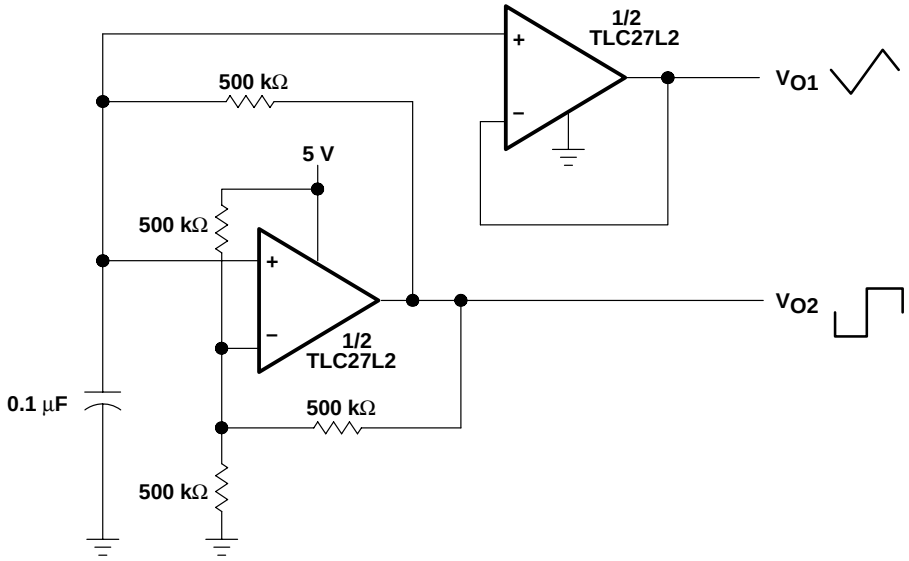
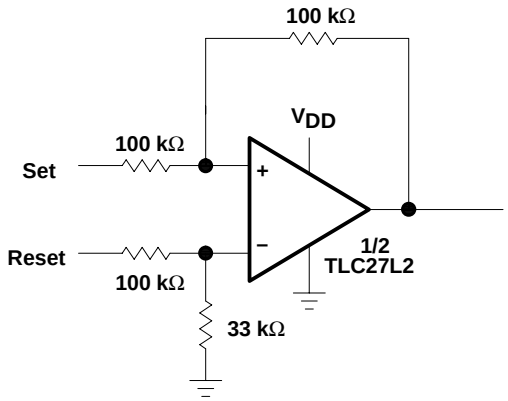


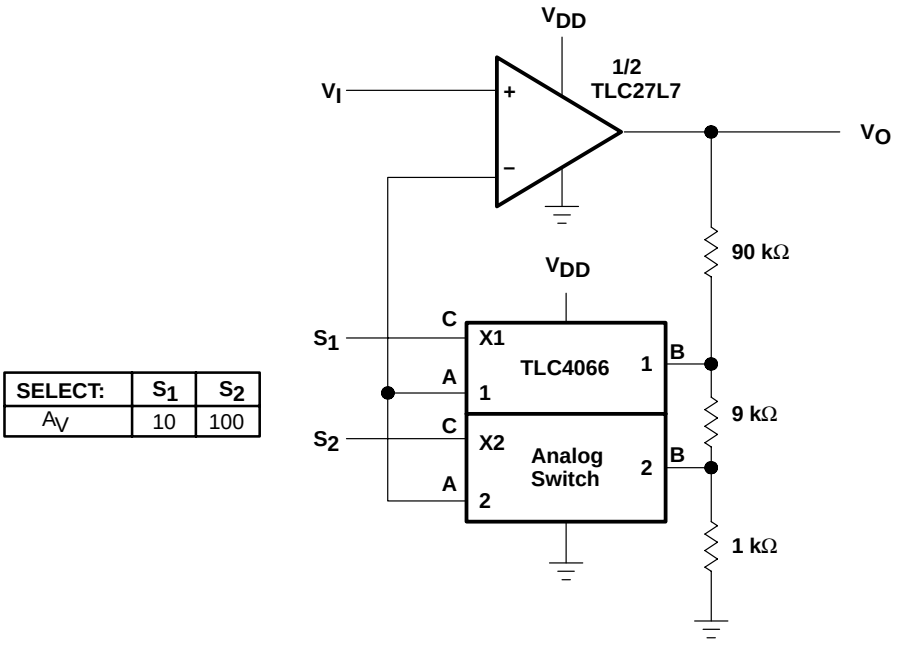
Figure 44. Multivibrator



NOTE: V_{DD} = 5 V to 16 V

Figure 45. Set/Reset Flip-Flop

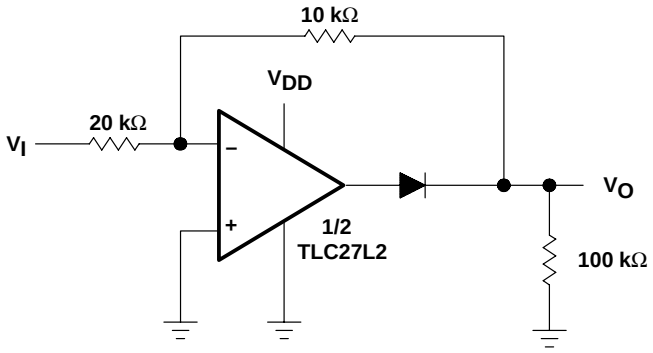
APPLICATION INFORMATION



SELECT:	S_1	S_2
A_V	10	100

NOTE: V_{DD} = 5 V to 12 V

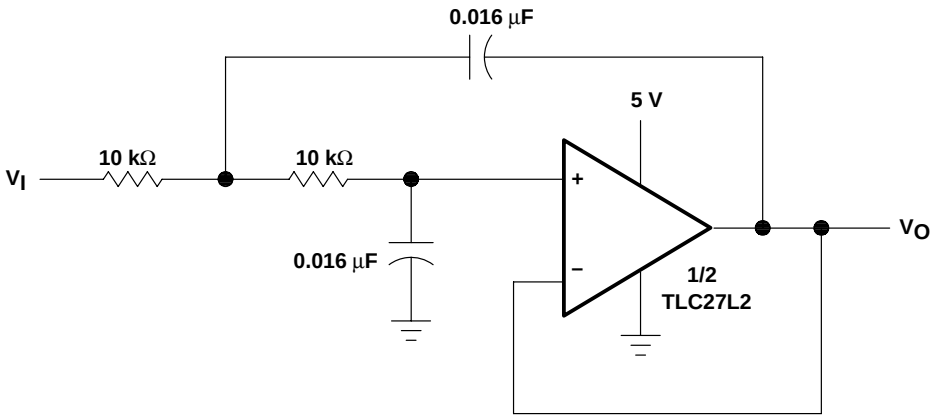
Figure 46. Amplifier With Digital Gain Selection



NOTE: V_{DD} = 5 V to 16 V

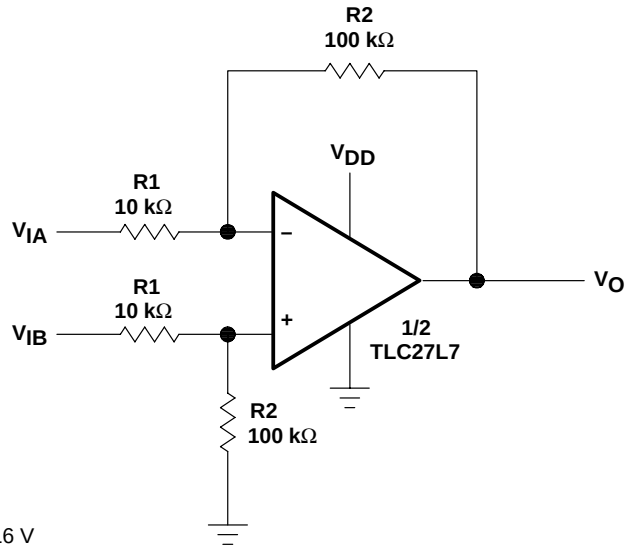
Figure 47. Full-Wave Rectifier

APPLICATION INFORMATION



NOTE: Normalized to f_c = 1 kHz and R_L = 10 kΩ

Figure 48. Two-Pole Low-Pass Butterworth Filter



NOTE: V_{DD} = 5 V to 16 V

$$V_O = \frac{R2}{R1}\left(V_{IB} - V_{IA}\right)$$

Figure 49. Difference Amplifier

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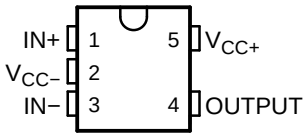
FEATURES

- 1.8-V, 2.7-V, and 5-V Specifications
- Rail-to-Rail Output Swing
  - 600-Ω Load . . . 80 mV From Rail
  - 2-kΩ Load . . . 30 mV From Rail
- V_{ICR} . . . 200 mV Beyond Rails
- Gain Bandwidth . . . 1.4 MHz
- Supply Current . . . 100 μA/Amplifier
- Max V_{IO} . . . 4 mV
- Space-Saving Packages
  - LMV931: SOT-23 and SC-70
  - LMV932: MSOP and SOIC
  - LMV934: SOIC and TSSOP

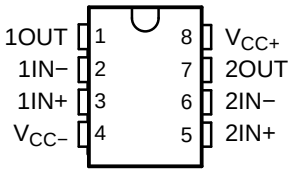
APPLICATIONS

- Industrial (Utility/Energy Metering)
- Automotive
- Communications (Optical Telecom, Data/Voice Cable Modems)
- Consumer Electronics (PDAs, PCs, CDR/W, Portable Audio)
- Supply-Current Monitoring
- Battery Monitoring

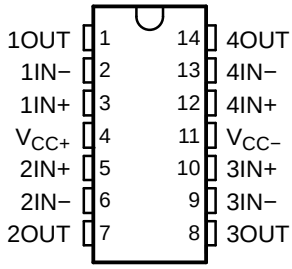
LMV931 . . . DBV (SOT-23-5) OR DCK (SC-70) PACKAGE
(TOP VIEW)



LMV932 . . . D (SOIC) OR
DGK (VSSOP/MSOP) PACKAGE
(TOP VIEW)



LMV934 . . . D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

ORDERING INFORMATION

T_A	PACKAGE(1)			ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 125°C	Single	SOT-23 – DBV	Reel of 3000	LMV931IDBVR	RBB_
			Reel of 250	LMV931IDBVT	PREVIEW
		SC-70 – DCK	Reel of 3000	LMV931IDCKR	RB_
			Reel of 250	LMV931IDCKT	PREVIEW
	Dual	MSOP/VSSOP – DGK	Reel of 2500	LMV932IDGKR	RD_
			Reel of 250	LMV932IDGKT	PREVIEW
		SOIC – D	Tube of 75	LMV932ID	MV932I
			Reel of 2500	LMV932IDR	
	Quad	SOIC – D	Tube of 50	LMV934ID	LMV934I
			Reel of 2500	LMV934IDR	
		TSSOP – PW	Tube of 90	LMV934IPW	MV934I
			Reel of 2000	LMV934IPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK/DGK: The actual top-side marking has one additional character that designates the assembly/test site.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

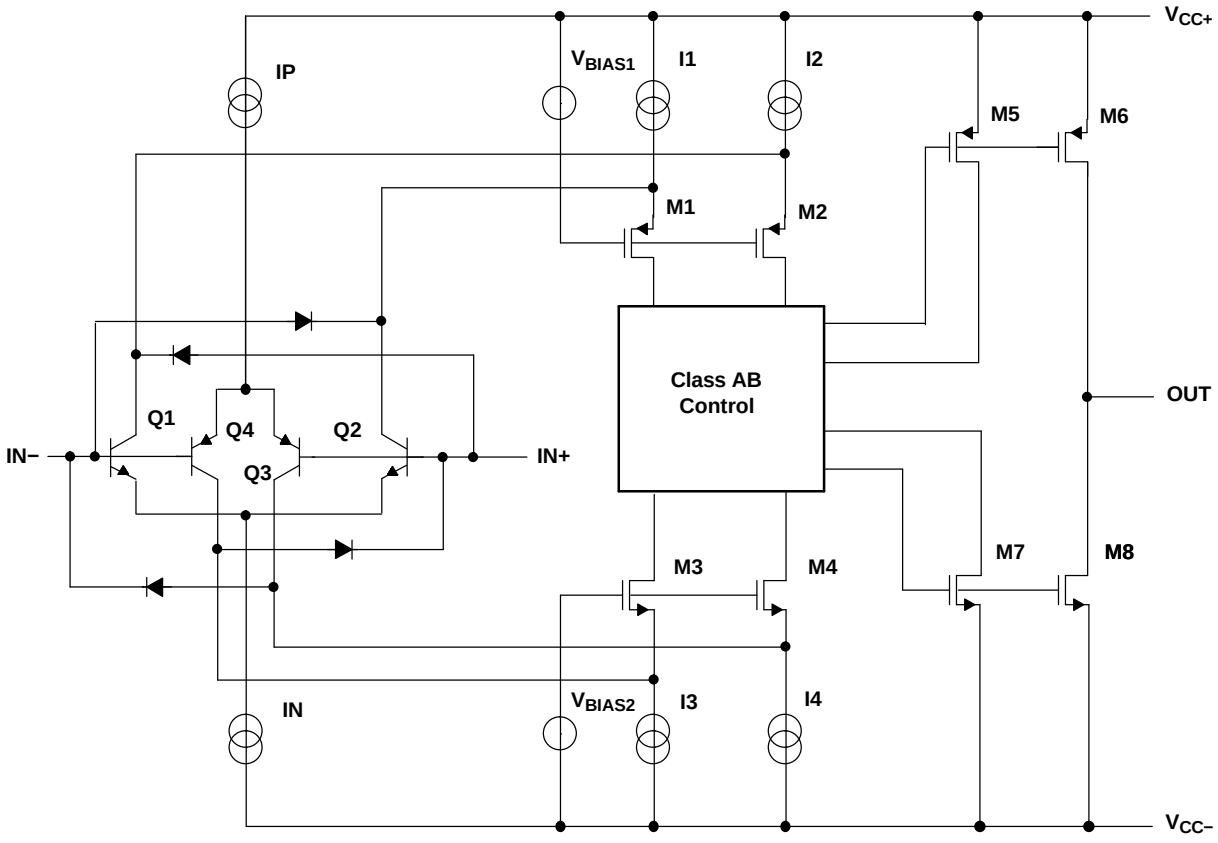
The LMV93x devices are low-voltage low-power operational amplifiers that are well suited for today's low-voltage and/or portable applications. Specified for operation of 1.8 V to 5 V, they can be used in portable applications that are powered from a single-cell Li-ion or two-cell batteries. They have rail-to-rail input and output capability for maximum signal swings in low-voltage applications. The LMV93x input common-mode voltage extends 200 mV beyond the rails for increased flexibility. The output can swing rail-to-rail unloaded and typically can reach 80 mV from the rails, while driving a 600-Ω load (at 1.8-V operation).

During 1.8-V operation, the devices typically consume a quiescent current of 103 μA per channel, and yet they are able to achieve excellent electrical specifications, such as 101-dB open-loop DC gain and 1.4-MHz gain bandwidth. Furthermore, the amplifiers offer good output drive characteristics, with the ability to drive a 600-Ω load and 1000-pF capacitance with minimal ringing.

The LMV93x devices are offered in the latest packaging technology to meet the most demanding space-constraint applications. The LMV931 is offered in standard SOT-23 and SC-70 packages. The LMV932 is available in the traditional MSOP and SOIC packages. The LMV934 is available in the traditional SOIC and TSSOP packages.

The LMV93x devices are characterized for operation from –40°C to 125°C, making the part universally suited for commercial, industrial, and automotive applications.

SIMPLIFIED SCHEMATIC



Absolute Maximum Ratings(1)

over free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage(2)			5.5	V
V_{ID}	Differential input voltage(3)		Supply voltage		
V_I	Input voltage range, either input		V_{CC-} – 0.2	V_{CC+} + 0.2	V
	Duration of output short circuit (one amplifier) to $V_{CC\pm}$(4)(5)		Unlimited		
θ_{JA}	Package thermal impedance(5)(6)	D package (8 pin)		97	°C/W
		D package (14 pin)		86	
		DBV package		206	
		DCK package		252	
		DGK package		172	
		PW package		113	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Applies to both single-supply and split-supply operation. Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.
(5) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage ($V_{CC+} - V_{CC-}$)	1.8	5	V
T_A	Operating free-air temperature	–40	125	°C

ESD Protection

	TYP	UNIT
Human-Body Model	2000	V
Machine Model	200	V

Electrical Characteristics

V_{CC+} = 1.8 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		LMV931 (single)		25°C		1	4	mV
					Full range			6	
			LMV932 (dual), LMV934 (quad)		25°C		1	5.5	
					Full range			7.5	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage				25°C		5.5		µV/°C
I_{IB}	Input bias current		V_{IC} = V_{CC+} – 0.8 V		25°C		15	35	nA
					25°C			65	
					Full range			75	
I_{IO}	Input offset current				25°C		13	25	nA
					Full range			40	
I_{CC}	Supply current (per channel)				25°C		103	185	µA
					Full range			205	
CMRR	Common-mode rejection ratio		0 ≤ V_{IC} ≤ 0.6 V, 1.4 V ≤ V_{IC} ≤ 1.8 V		25°C	60	78		dB
					–40°C to 85°C	55			
			0.2 ≤ V_{IC} ≤ 0.6 V, 1.4 V ≤ V_{IC} ≤ 1.6 V		–40°C to 125°C	55			
			–0.2 ≤ V_{IC} ≤ 0 V, 1.8 V ≤ V_{IC} ≤ 2 V		25°C	50	72		
k_{SVR}	Supply-voltage rejection ratio		1.8 V ≤ V_{CC+} ≤ 5 V, V_{IC} = 0.5 V		25°C	75	100		dB
					Full range	70			
V_{ICR}	Common-mode input voltage range		CMRR ≥ 50 dB		25°C	V_{CC-} – 0.2	–0.2 to 2.1	V_{CC+} + 0.2	V
					–40°C to 85°C	V_{CC-}		V_{CC+}	
					–40°C to 125°C	V_{CC-} + 0.2		V_{CC+} – 0.2	
A_V	Large-signal voltage gain	LMV931	V_O = 0.2 V to 1.6 V, V_{IC} = 0.5 V	R_L = 600 Ω to 0.9 V	25°C	77	101		dB
					Full range	73			
				R_L = 2 kΩ to 0.9 V	25°C	80	105		
					Full range	75			
		LMV932, LMV934		R_L = 600 Ω to 0.9 V	25°C	75	90		
					Full range	72			
				R_L = 2 kΩ to 0.9 V	25°C	78	100		
					Full range	75			
V_O	Output swing		R_L = 600 Ω to 0.9 V, V_{ID} = ±100 mV	High level	25°C	1.65	1.72		V
					Full range	1.63			
				Low level	25°C		0.077	0.105	
					Full range			0.120	
			R_L = 2 kΩ to 0.9 V, V_{ID} = ±100 mV	High level	25°C	1.75	1.77		
					Full range	1.74			
				Low level	25°C		0.024	0.035	
					Full range			0.040	
I_{OS}	Output short-circuit current		V_O = 0 V, V_{ID} = 100 mV	Sourcing	25°C	4	8		mA
					Full range	3.3			
			V_O = 1.8 V, V_{ID} = –100 mV	Sinking	25°C	7	9		
					Full range	5			

Electrical Characteristics (continued)

V_{CC+} = 1.8 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
GBW	Gain bandwidth product		25°C		1.4		MHz
SR	Slew rate(1)		25°C		0.35		V/µS
Φ_m	Phase margin		25°C		67		°
	Gain margin		25°C		7		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V_{IC} = 0.5 V	25°C		60		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.06		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_{ID} = 1 V_{p-p}	25°C		0.023		%
	Amplifier-to-amplifier isolation(2)		25°C		123		dB

(1) Number specified is the slower of the positive and negative slew rates.
(2) Input referred, V_{CC+} = 5 V and R_L = 100 kΩ connected to 2.5 V. Each amplifier is excited, in turn, with a 1-kHz signal to produce V_O = 3 V_{p-p}.

Electrical Characteristics

V_{CC+} = 2.7 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		LMV931 (single)		25°C		1	4	mV
					Full range			6	
			LMV932 (dual), LMV934 (quad)		25°C		1	5.5	
					Full range			7.5	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage				25°C		5.5		µV/°C
I_{IB}	Input bias current		V_{IC} = V_{CC+} – 0.8 V		25°C		15	35	nA
					25°C			65	
					Full range			75	
I_{IO}	Input offset current				25°C		8	25	nA
					Full range			40	
I_{CC}	Supply current (per channel)				25°C		105	190	µA
					Full range			210	
CMRR	Common-mode rejection ratio		0 ≤ V_{IC} ≤ 1.5 V, 2.3 V ≤ V_{IC} ≤ 2.7 V		25°C	60	81		dB
					–40°C to 85°C	55			
			0.2 ≤ V_{IC} ≤ 1.5 V, 2.3 V ≤ V_{IC} ≤ 2.5 V		–40°C to 125°C	55			
			–0.2 ≤ V_{IC} ≤ 0 V, 2.7 V ≤ V_{IC} ≤ 2.9 V		25°C	50	74		
k_{SVR}	Supply-voltage rejection ratio		1.8 V ≤ V_{CC+} ≤ 5 V, V_{IC} = 0.5 V		25°C	75	100		dB
					Full range	70			
V_{ICR}	Common-mode input voltage range		CMRR ≥ 50 dB		25°C	V_{CC-} – 0.2	–0.2 to 3	V_{CC+} + 0.2	V
					–40°C to 85°C	V_{CC-}		V_{CC+}	
					–40°C to 125°C	V_{CC-} + 0.2		V_{CC+} – 0.2	
A_V	Large-signal voltage gain	LMV931	V_O = 0.2 V to 2.5 V	R_L = 600 Ω to 1.35 V	25°C	87	104		dB
					Full range	86			
				R_L = 2 kΩ to 1.35 V	25°C	92	110		
					Full range	91			
		LMV932, LMV934		R_L = 600 Ω to 1.35 V	25°C	78	90		
					Full range	75			
				R_L = 2 kΩ to 1.35 V	25°C	81	100		
					Full range	78			
V_O	Output swing		R_L = 600 Ω to 1.35 V, V_{ID} = ±100 mV	High level	25°C	2.55	2.62		V
					Full range	2.53			
				Low level	25°C		0.083	0.11	
					Full range			0.13	
			R_L = 2 kΩ to 1.35 V, V_{ID} = ±100 mV	High level	25°C	2.65	2.675		
					Full range	2.64			
				Low level	25°C		0.025	0.04	
					Full range			0.045	
I_{OS}	Output short-circuit current		V_O = 0 V, V_{ID} = 100 mV	Sourcing	25°C	20	30		mA
					Full range	15			
			V_O = 2.7 V, V_{ID} = –100 mV	Sinking	25°C	18	25		
					Full range	12			
GBW	Gain bandwidth product				25°C		1.4		MHz

Electrical Characteristics (continued)

V_{CC+} = 2.7 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate(1)		25°C		0.4		V/µS
Φ_m	Phase margin		25°C		70		°
	Gain margin		25°C		7.5		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V_{IC} = 0.5 V	25°C		57		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.082		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_{ID} = 1 V_{p-p}	25°C		0.022		%
	Amplifier-to-amplifier isolation(2)		25°C		123		dB

(1) Number specified is the slower of the positive and negative slew rates.
(2) Input referred, V_{CC+} = 5 V and R_L = 100 kΩ connected to 2.5 V. Each amplifier is excited, in turn, with a 1-kHz signal to produce V_O = 3 V_{p-p}.

Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		LMV931 (single)		25°C		1	4	mV
					Full range			6	
			LMV932 (dual), LMV934 (quad)		25°C		1	5.5	
					Full range			7.5	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage				25°C		5.5		µV/°C
I_{IB}	Input bias current		V_{IC} = V_{CC+} – 0.8 V		25°C		15	35	nA
					25°C			65	
					Full range			75	
I_{IO}	Input offset current				25°C		9	25	nA
					Full range			40	
I_{CC}	Supply current (per channel)				25°C		116	210	µA
					Full range			230	
CMRR	Common-mode rejection ratio		0 ≤ V_{IC} ≤ 3.8 V, 4.6 V ≤ V_{IC} ≤ 5 V		25°C	60	86		dB
					–40°C to 85°C	55			
			0.3 ≤ V_{IC} ≤ 3.8 V, 4.6 V ≤ V_{IC} ≤ 4.7 V		–40°C to 125°C	55			
			–0.2 ≤ V_{IC} ≤ 0 V, 5 V ≤ V_{IC} ≤ 5.2 V		25°C	50	78		
k_{SVR}	Supply-voltage rejection ratio		1.8 V ≤ V_{CC+} ≤ 5 V, V_{IC} = 0.5 V		25°C	75	100		dB
					Full range	70			
V_{ICR}	Common-mode input voltage range		CMRR ≥ 50 dB		25°C	V_{CC-} – 0.2	–0.2 to 5.3	V_{CC+} + 0.2	V
					–40°C to 85°C	V_{CC-}		V_{CC+}	
					–40°C to 125°C	V_{CC-} + 0.3		V_{CC+} – 0.3	
A_V	Large-signal voltage gain	LMV931	V_O = 0.2 V to 4.8 V	R_L = 600 Ω to 2.5 V	25°C	88	102		dB
					Full range	87			
				R_L = 2 kΩ to 2.5 V	25°C	94	113		
					Full range	93			
		LMV932, LMV934		R_L = 600 Ω to 2.5 V	25°C	81	90		
					Full range	78			
				R_L = 2 kΩ to 2.5 V	25°C	85	100		
					Full range	82			
V_O	Output swing		R_L = 600 Ω to 2.5 V, V_{ID} = ±100 mV	High level	25°C	4.855	4.89		V
					Full range	4.835			
				Low level	25°C		0.12	0.16	
					Full range			0.18	
			R_L = 2 kΩ to 2.5 V, V_{ID} = ±100 mV	High level	25°C	4.945	4.967		
					Full range	4.935			
				Low level	25°C		0.037	0.065	
					Full range			0.075	
I_{OS}	Output short-circuit current		V_O = 0 V, V_{ID} = 100 mV	Sourcing	25°C	80	100		mA
					Full range	68			
			V_O = 5 V, V_{ID} = –100 mV	Sinking	25°C	58	65		
					Full range	45			

Electrical Characteristics (continued)

V_{CC+} = 5 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
GBW	Gain bandwidth product		25°C		1.5		MHz
SR	Slew rate(1)		25°C		0.42		V/µS
Φ_m	Phase margin		25°C		71		°
	Gain margin		25°C		8		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V_{IC} = 0.5 V	25°C		50		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.07		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_{ID} = 1 V_{p-p}	25°C		0.022		%
	Amplifier-to-amplifier isolation(2)		25°C		123		dB

(1) Number specified is the slower of the positive and negative slew rates.
(2) Input referred, V_{CC+} = 5 V and R_L = 100 kΩ connected to 2.5 V. Each amplifier is excited, in turn, with a 1-kHz signal to produce V_O = 3 V_{p-p}.

TYPICAL CHARACTERISTICS

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

SUPPLY CURRENT vs SUPPLY VOLTAGE

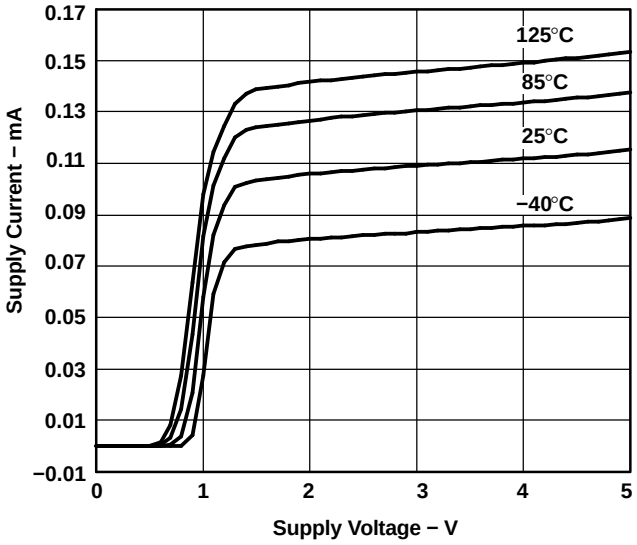


Figure 1.

SLEW RATE vs SUPPLY VOLTAGE

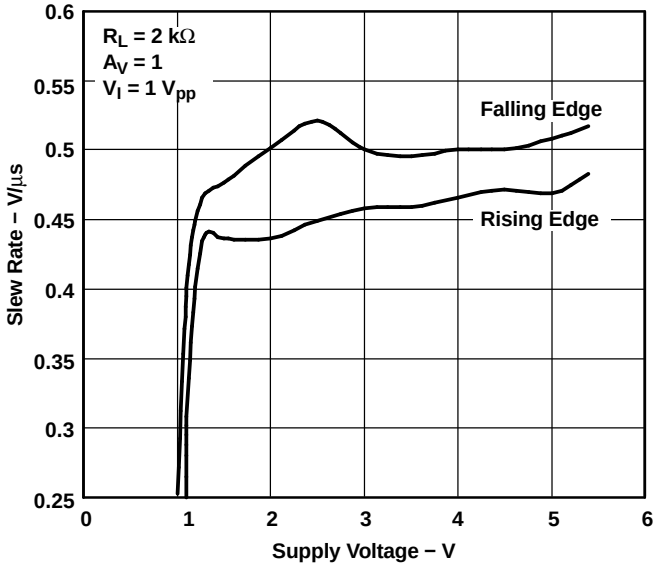


Figure 2.

SOURCE CURRENT vs OUTPUT VOLTAGE

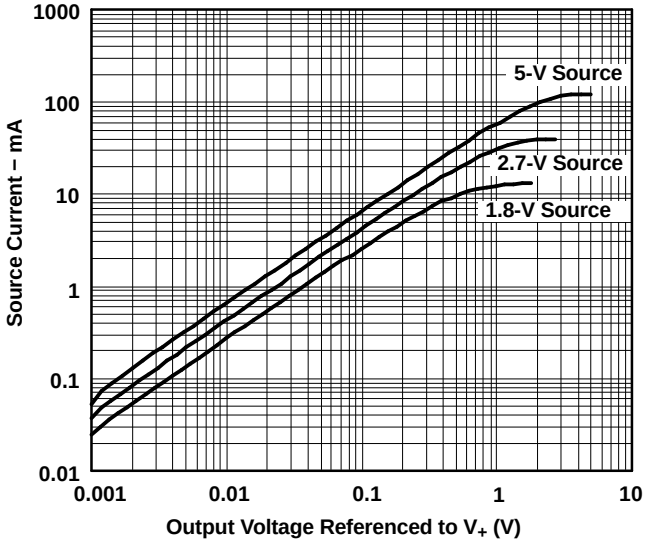


Figure 3.

SINK CURRENT vs OUTPUT VOLTAGE

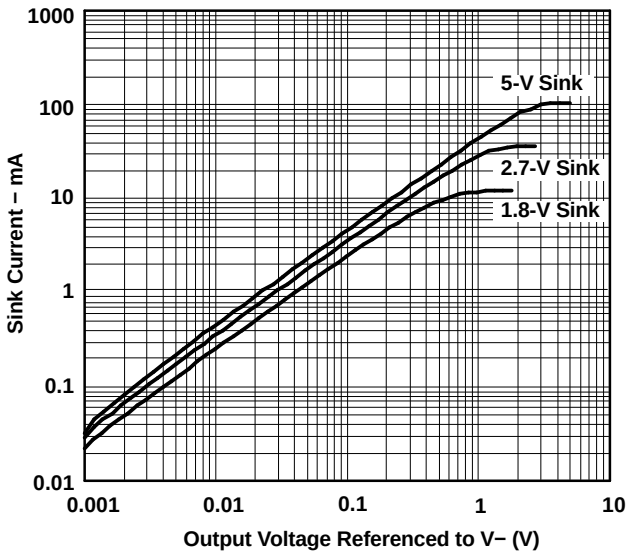


Figure 4.

TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

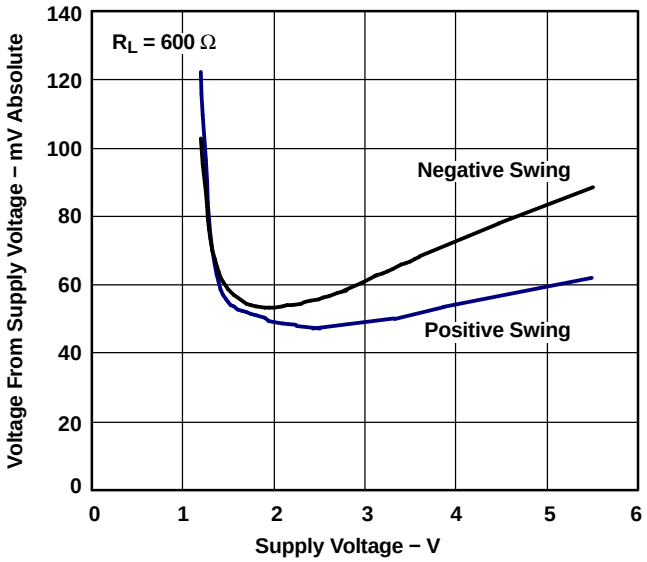


Figure 5.

OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

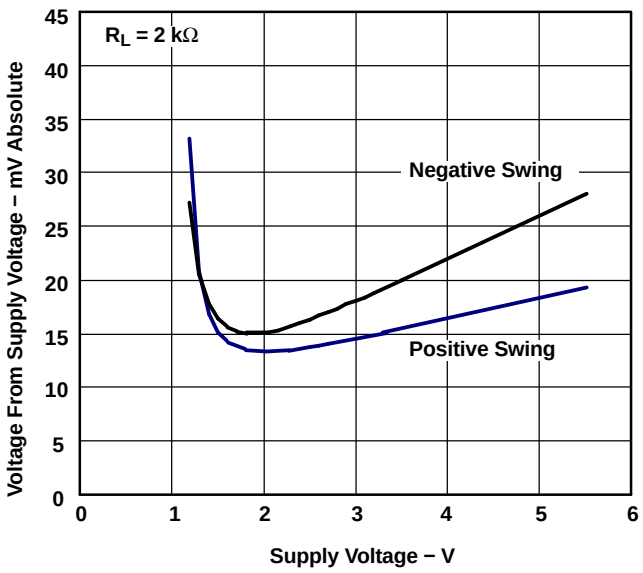


Figure 6.

SHORT-CIRCUIT CURRENT (SINK) vs TEMPERATURE

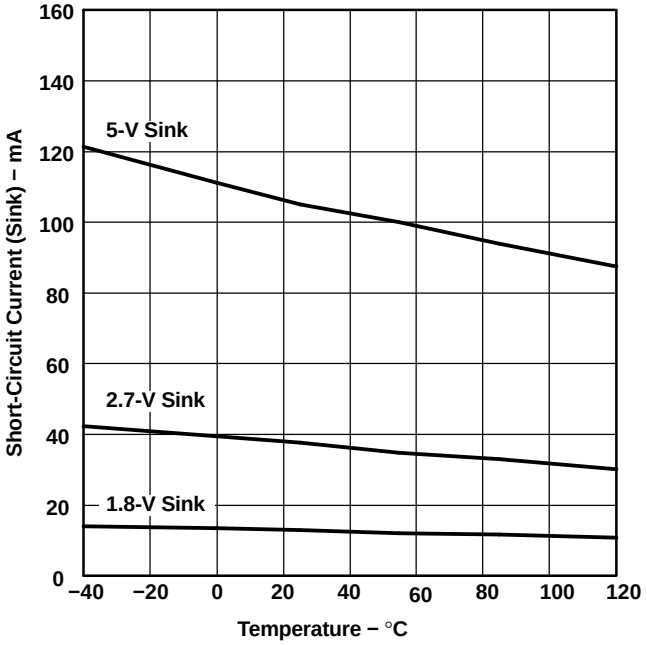


Figure 7.

SHORT-CIRCUIT CURRENT (SOURCE) vs TEMPERATURE

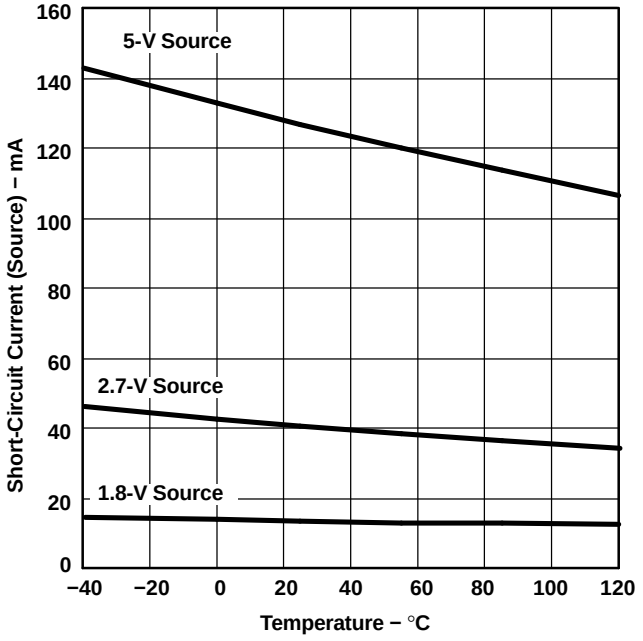


Figure 8.

TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

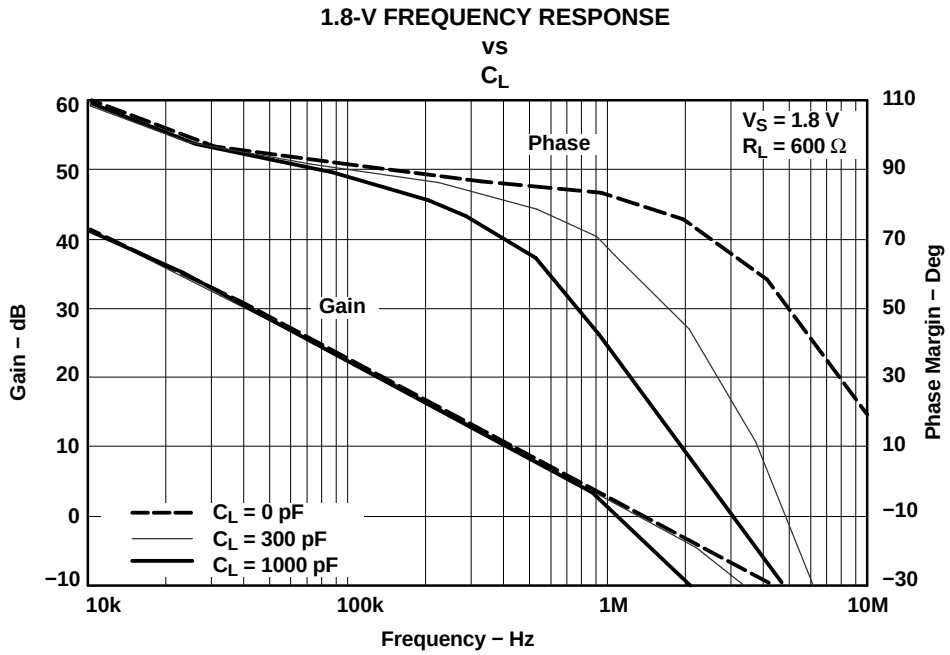


Figure 9.

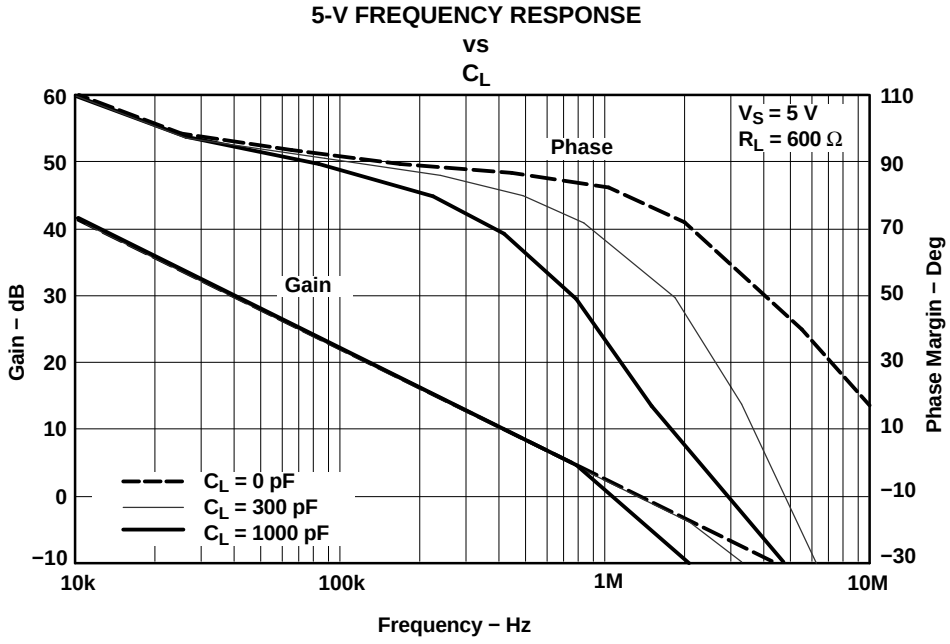


Figure 10.

TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

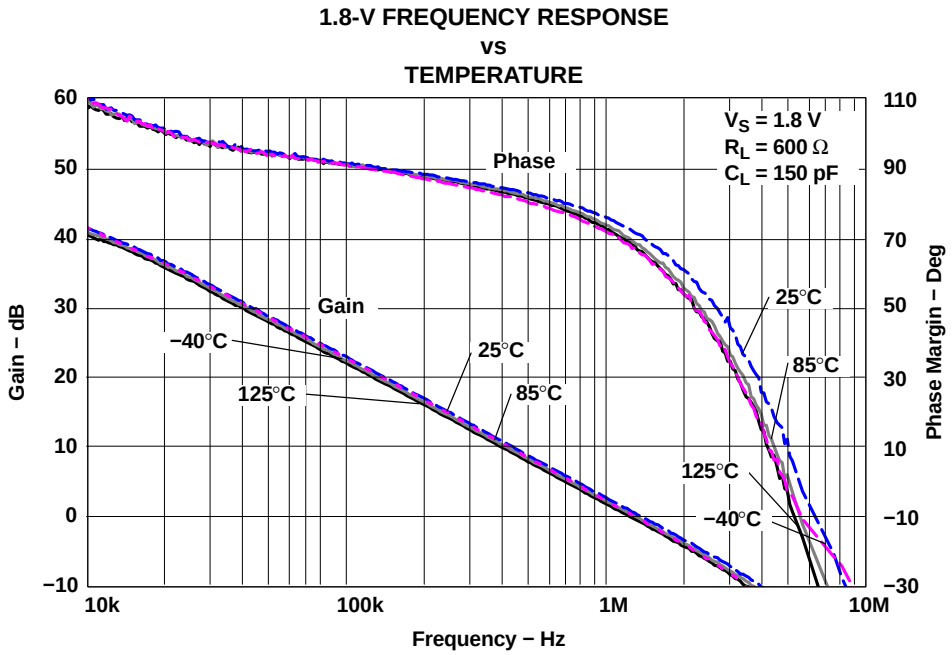


Figure 11.

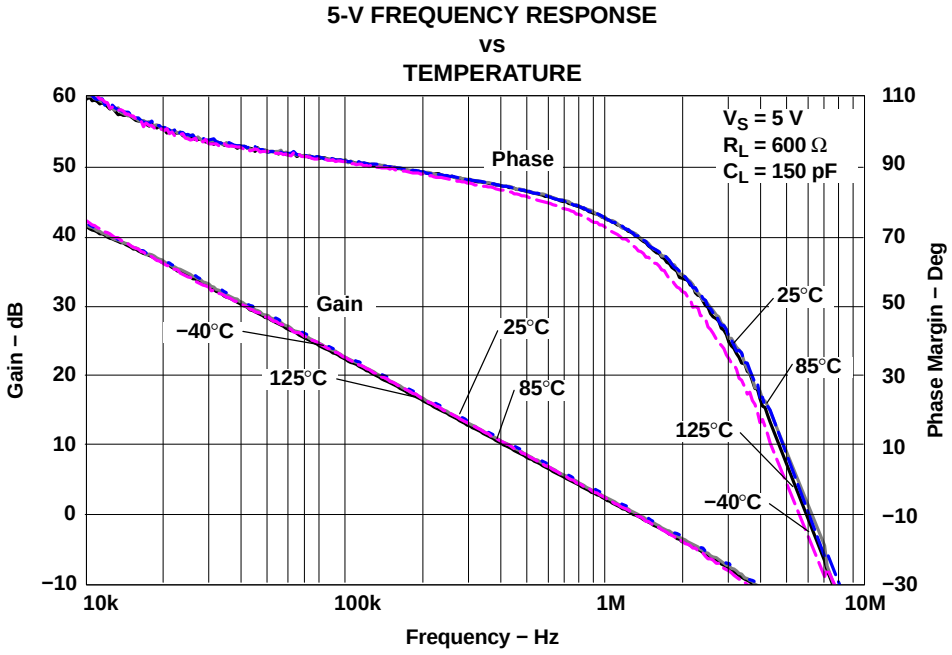


Figure 12.

TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

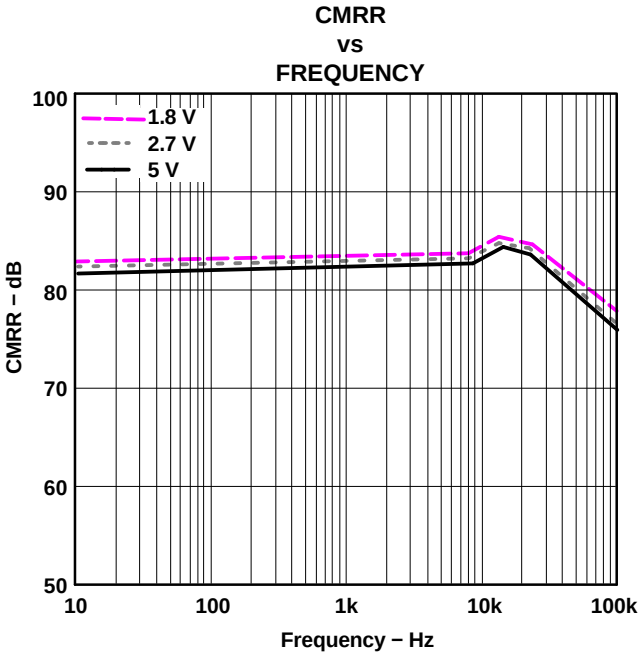


Figure 13.

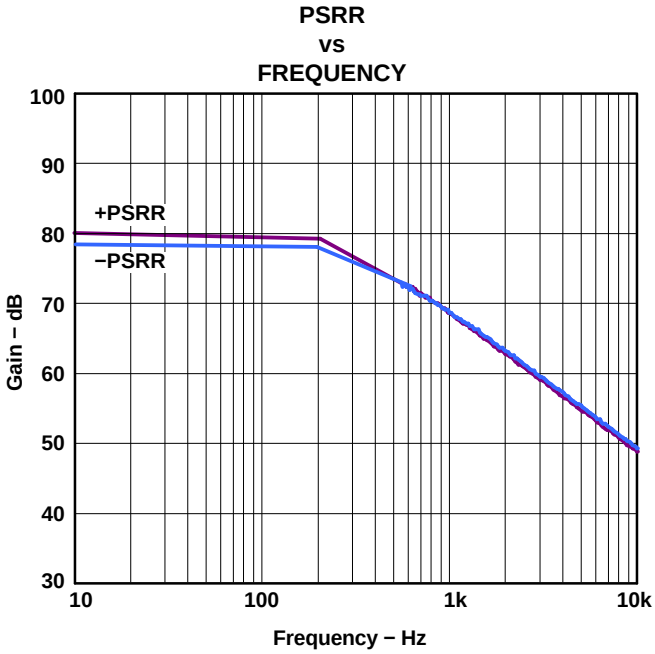


Figure 14.

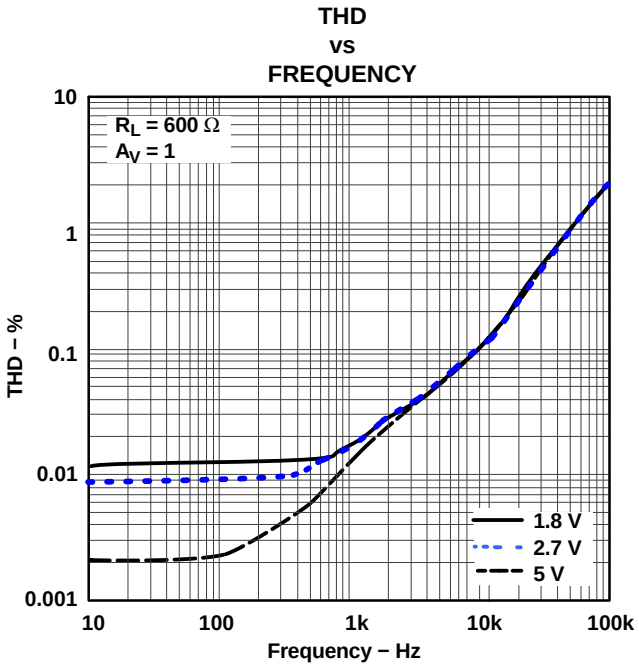


Figure 15.

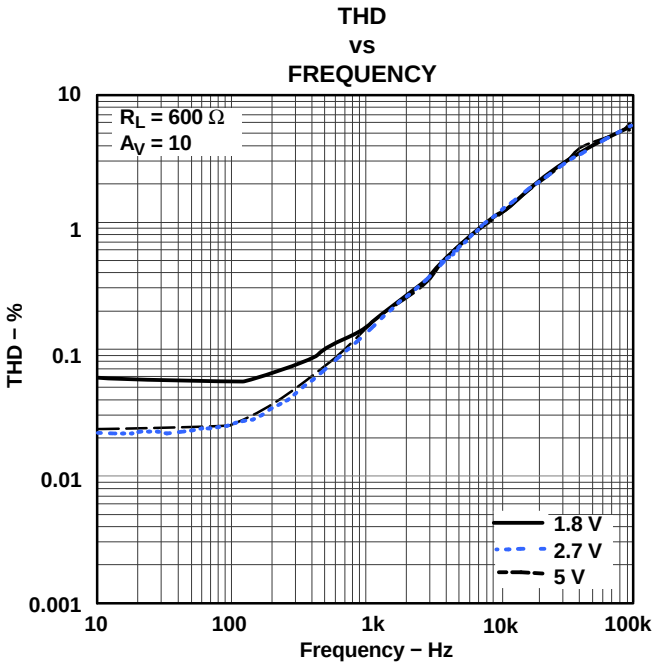


Figure 16.

TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

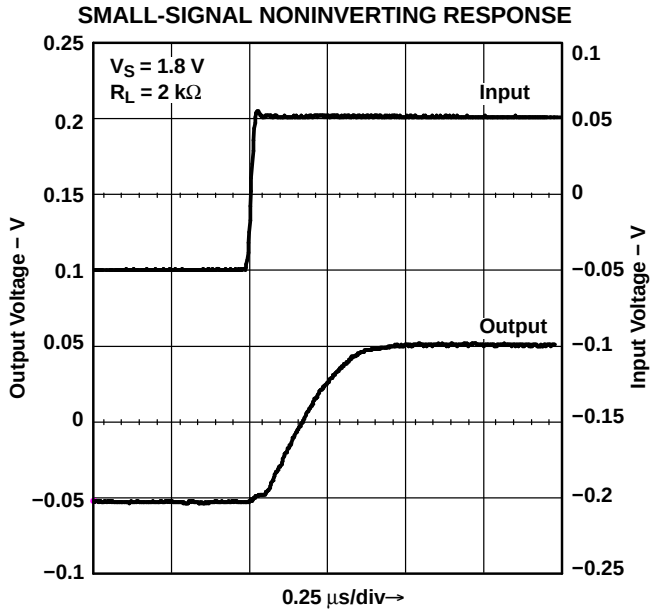


Figure 17.

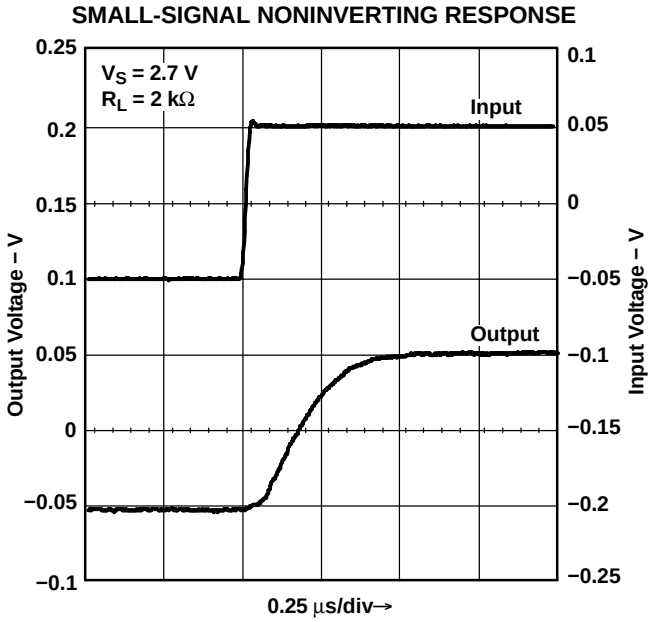


Figure 18.

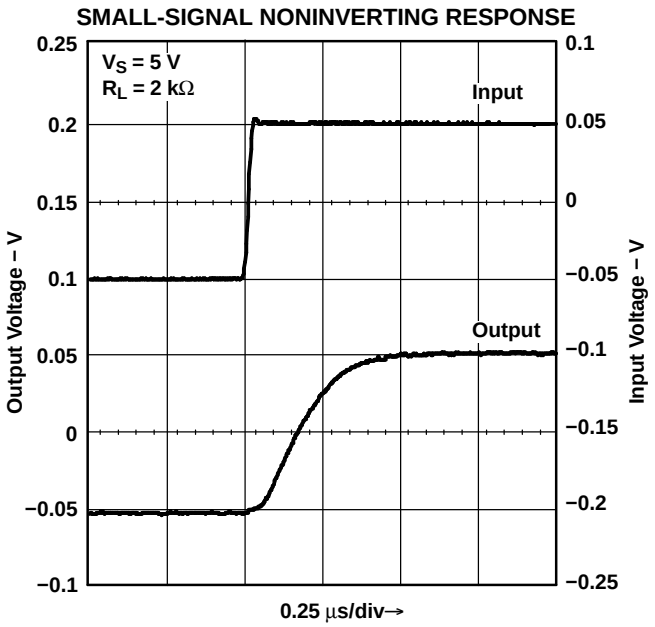


Figure 19.

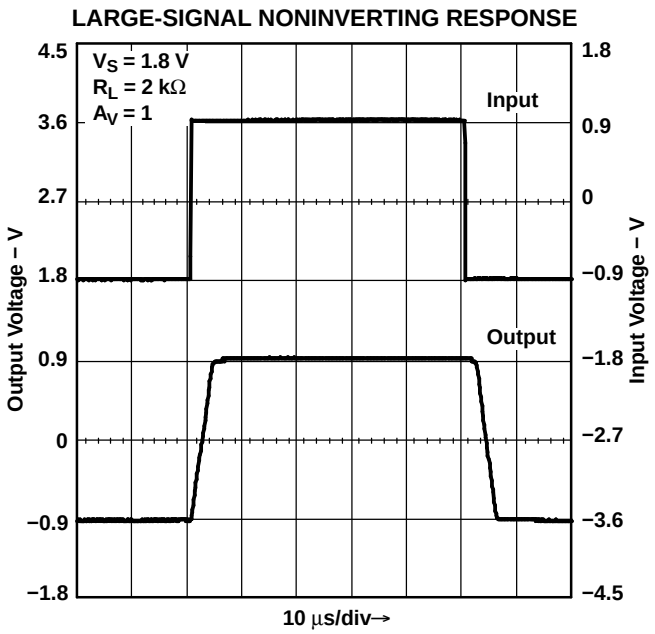


Figure 20.

TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

LARGE-SIGNAL NONINVERTING RESPONSE

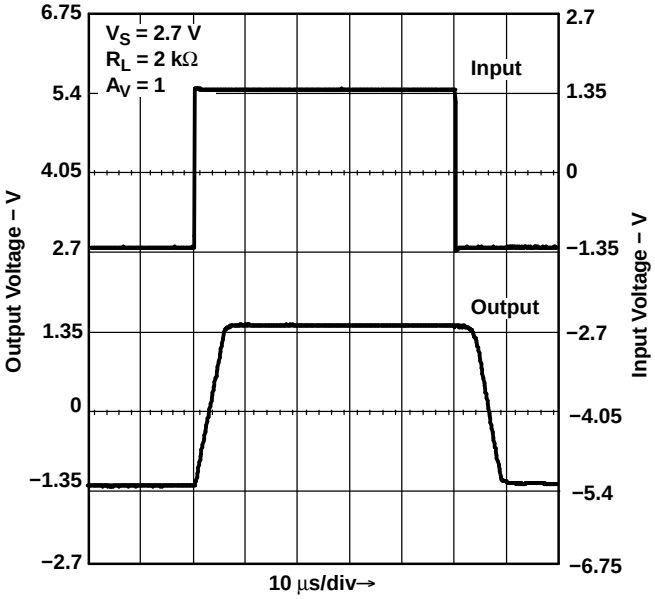


Figure 21.

LARGE-SIGNAL NONINVERTING RESPONSE

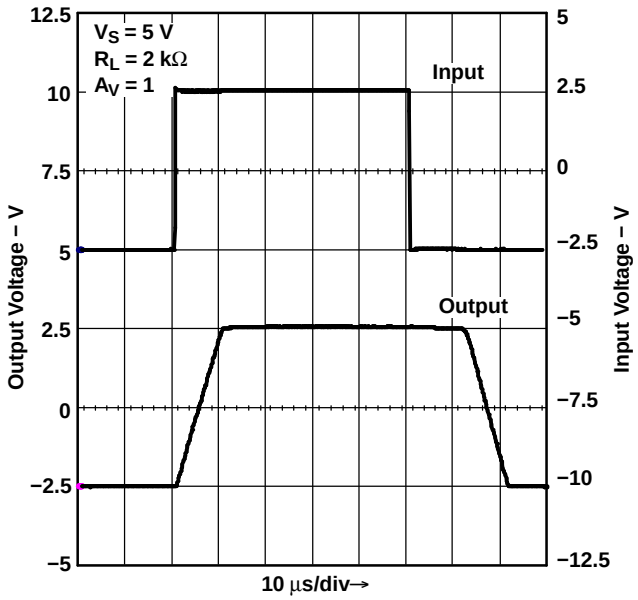


Figure 22.

OFFSET VOLTAGE vs COMMON-MODE RANGE

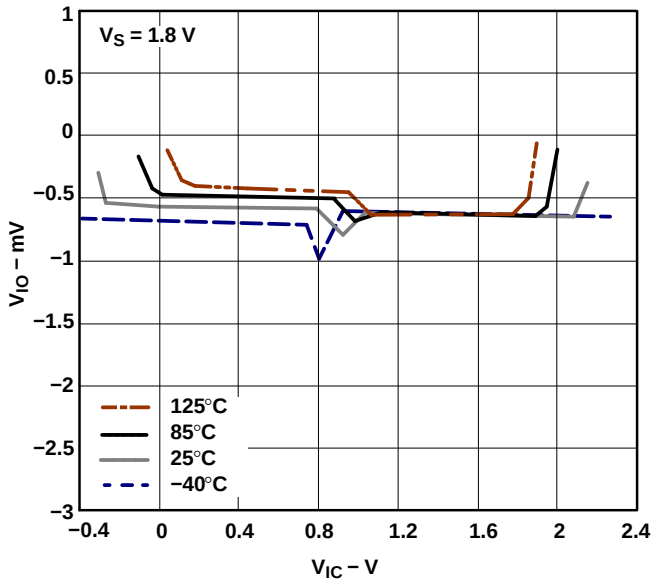


Figure 23.

OFFSET VOLTAGE vs COMMON-MODE RANGE

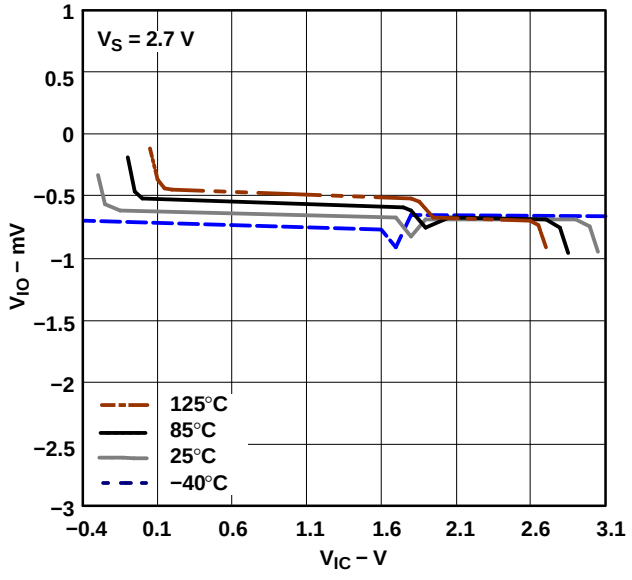


Figure 24.

TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

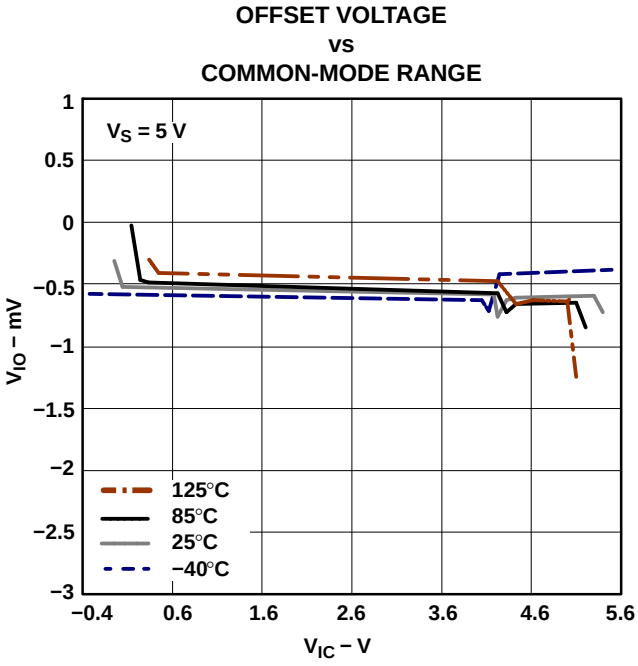


Figure 25.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
LMV931IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV931IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV931IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV931IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV931IDCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV931IDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV932ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV932IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV932IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV932IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV932IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV932IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV932IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV932IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934IPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV934IPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
LMV934IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

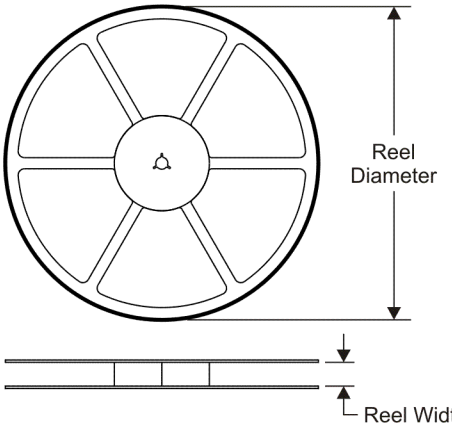
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

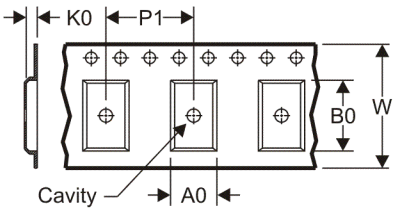
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

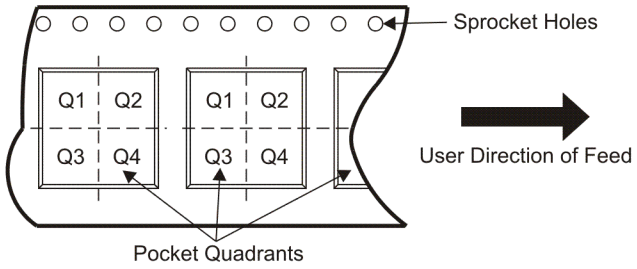


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

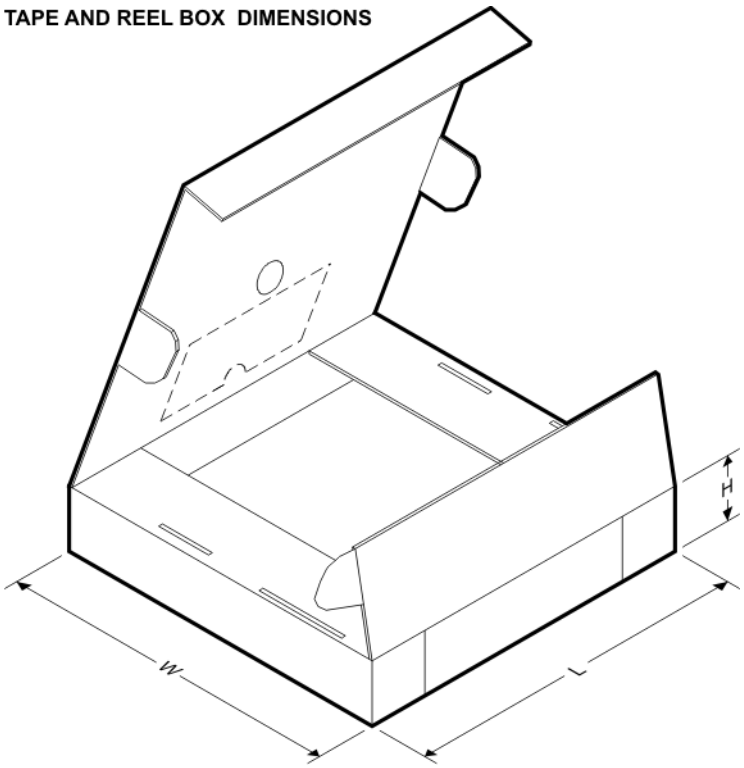
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV931IDBVR	SOT-23	DBV	5	3000	179.0	8.0	3.0	3.0	1.0	4.0	8.0	Q3
LMV931IDCKR	SC70	DCK	5	3000	179.0	8.0	2.0	3.0	1.0	4.0	8.0	Q3
LMV932IDGKR	MSOP	DGK	8	2500	330.0	12.0	5.0	3.0	1.0	8.0	12.0	Q1
LMV932IDGKR	MSOP	DGK	8	2500	330.0	13.0	5.0	3.0	1.0	8.0	12.0	Q1
LMV932IDR	SOIC	D	8	2500	330.0	12.0	6.0	5.0	2.0	8.0	12.0	Q1
LMV934IDR	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
LMV934IPWR	TSSOP	PW	14	2000	330.0	12.0	7.0	6.0	2.0	8.0	12.0	Q1

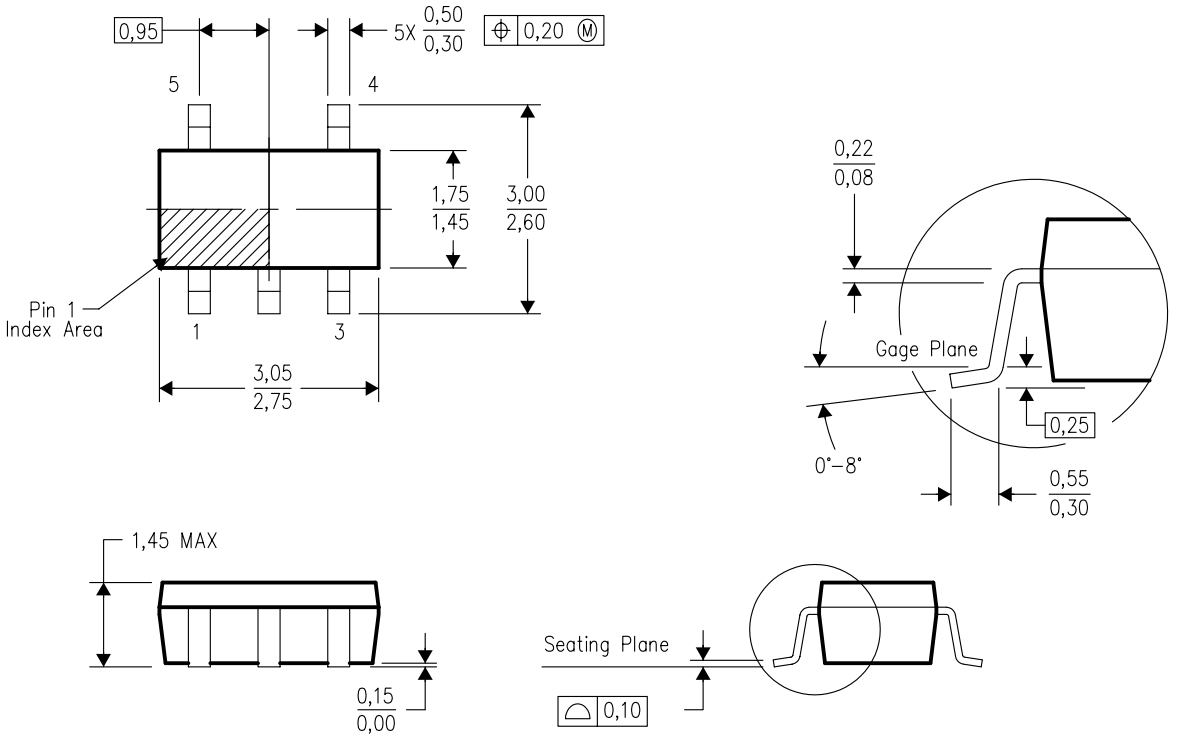
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV931IDBVR	SOT-23	DBV	5	3000	220.0	205.0	50.0
LMV931IDCKR	SC70	DCK	5	3000	220.0	205.0	50.0
LMV932IDGKR	MSOP	DGK	8	2500	370.0	355.0	55.0
LMV932IDGKR	MSOP	DGK	8	2500	358.0	335.0	35.0
LMV932IDR	SOIC	D	8	2500	343.0	338.0	21.0
LMV934IDR	SOIC	D	14	2500	346.0	346.0	33.0
LMV934IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

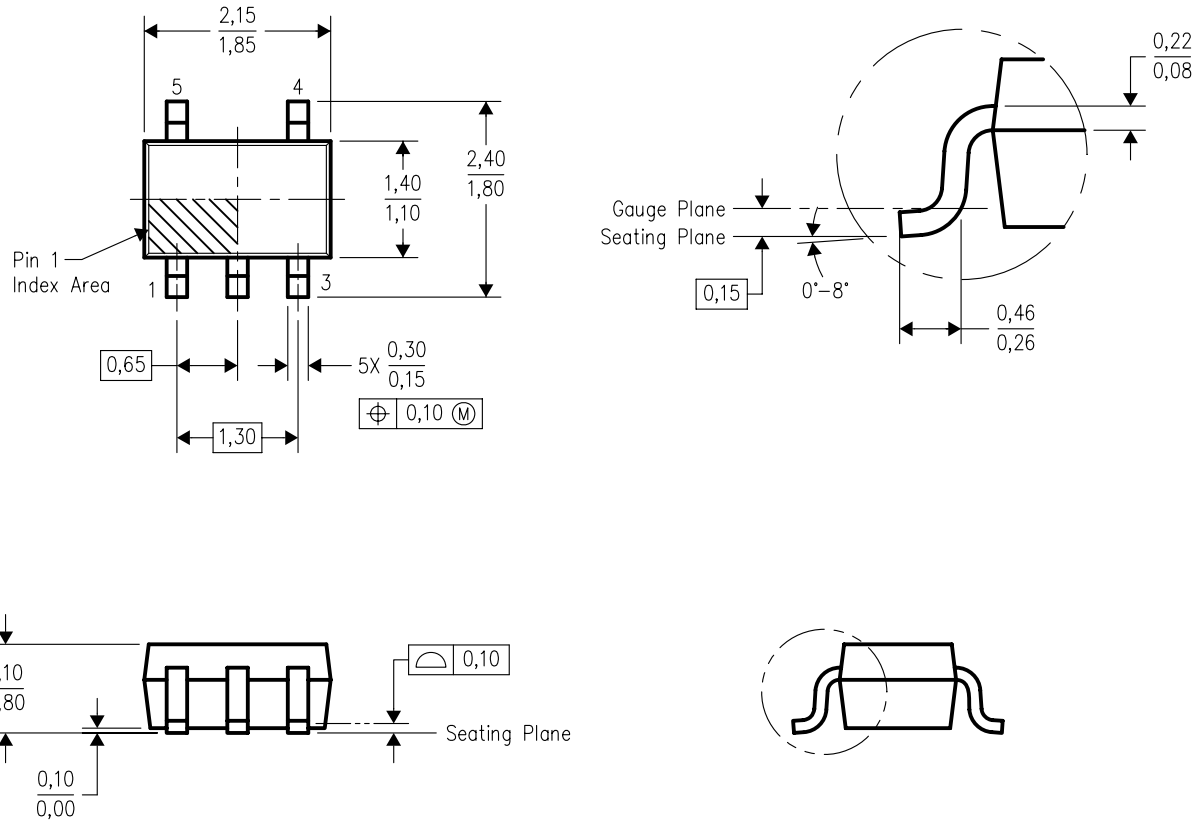
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

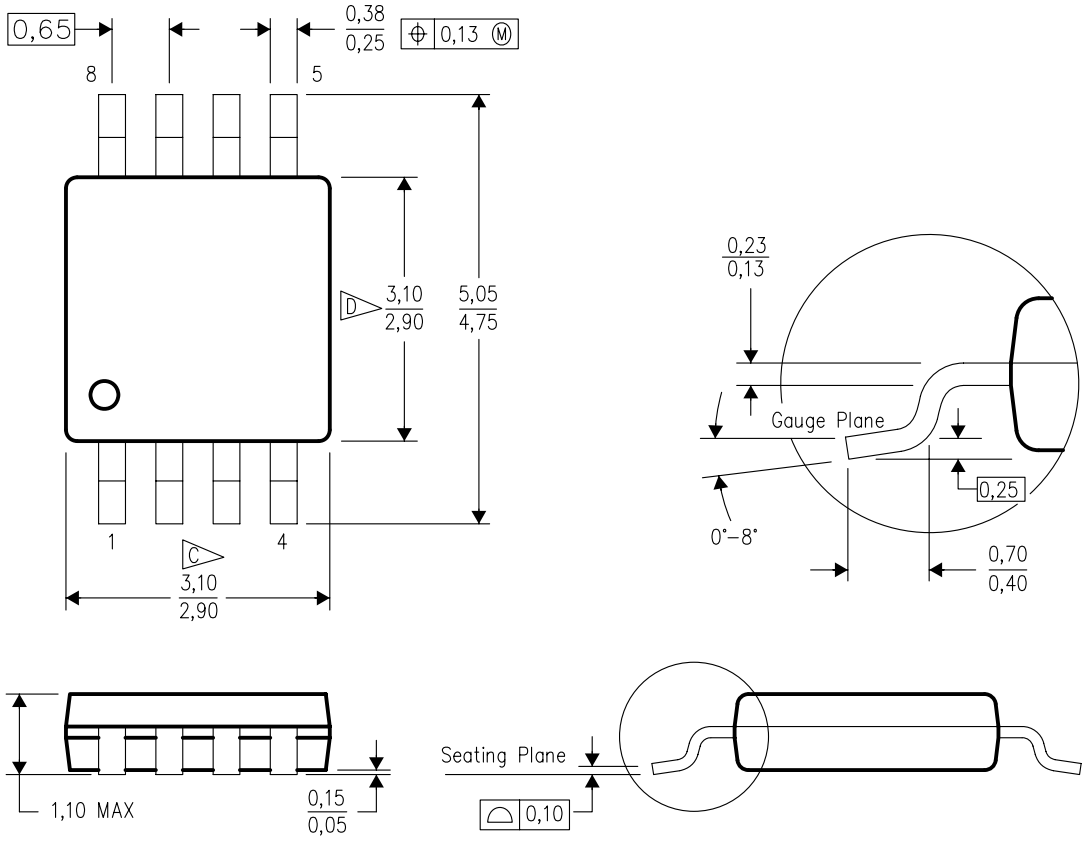
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

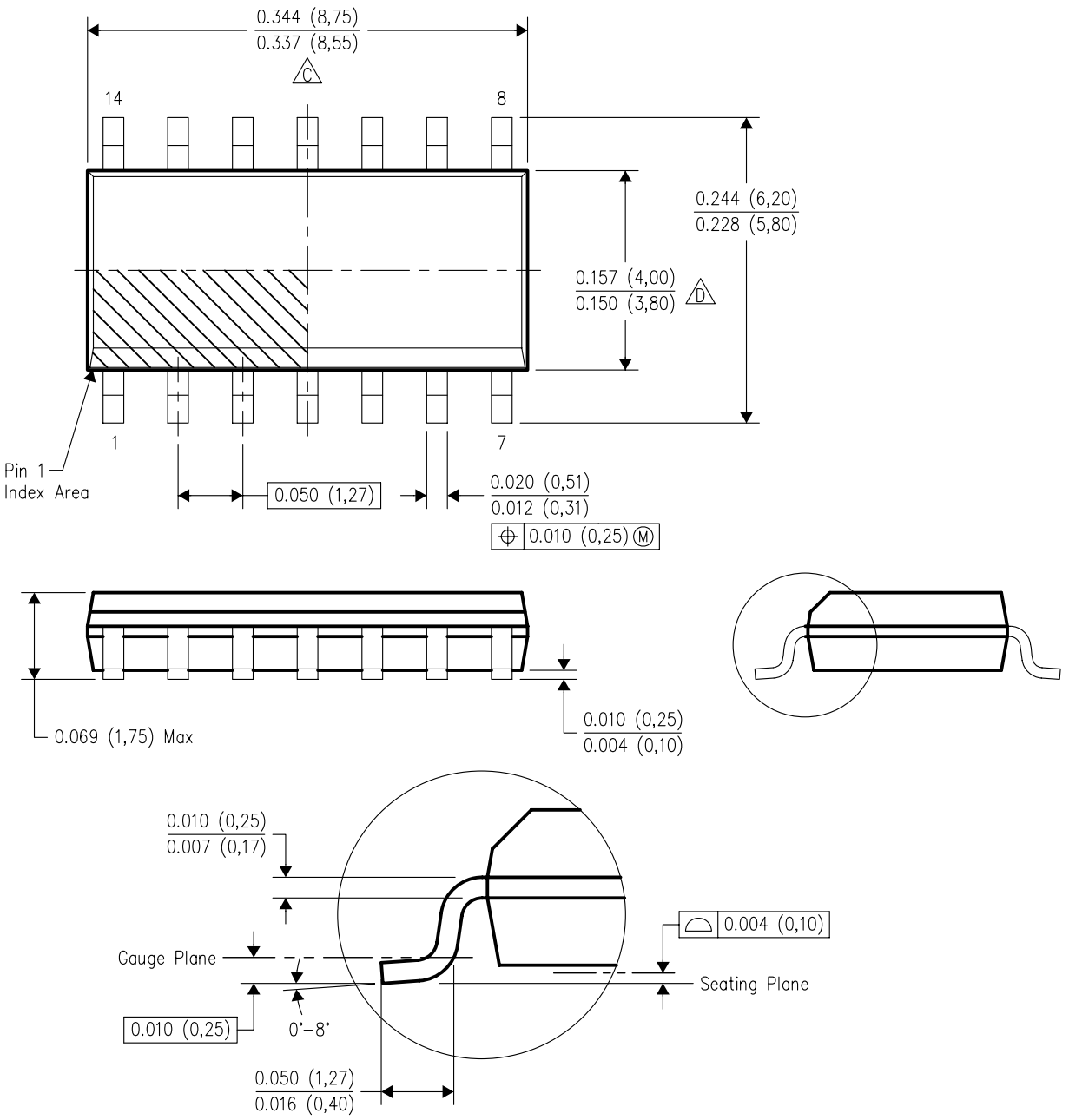
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

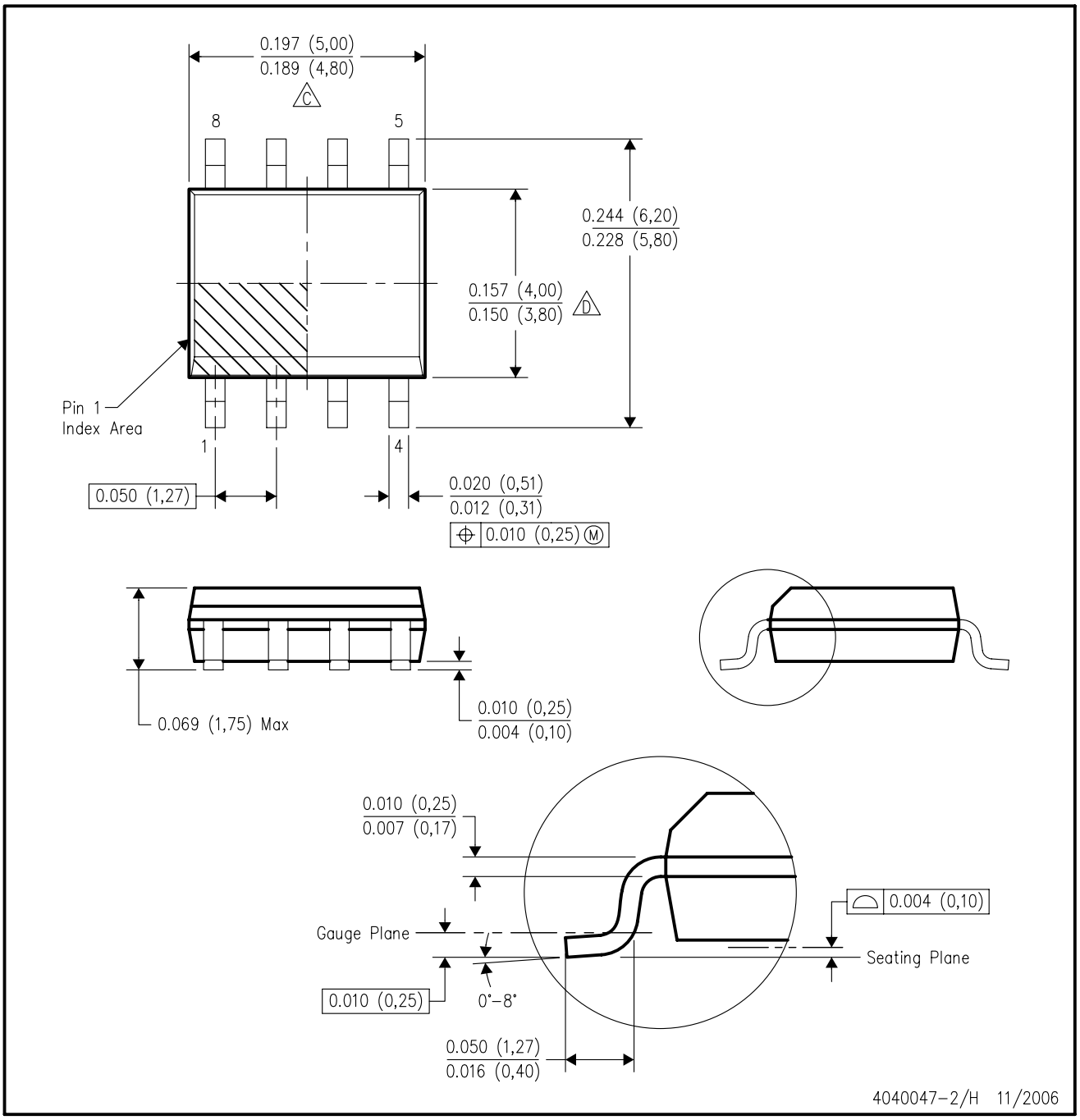
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

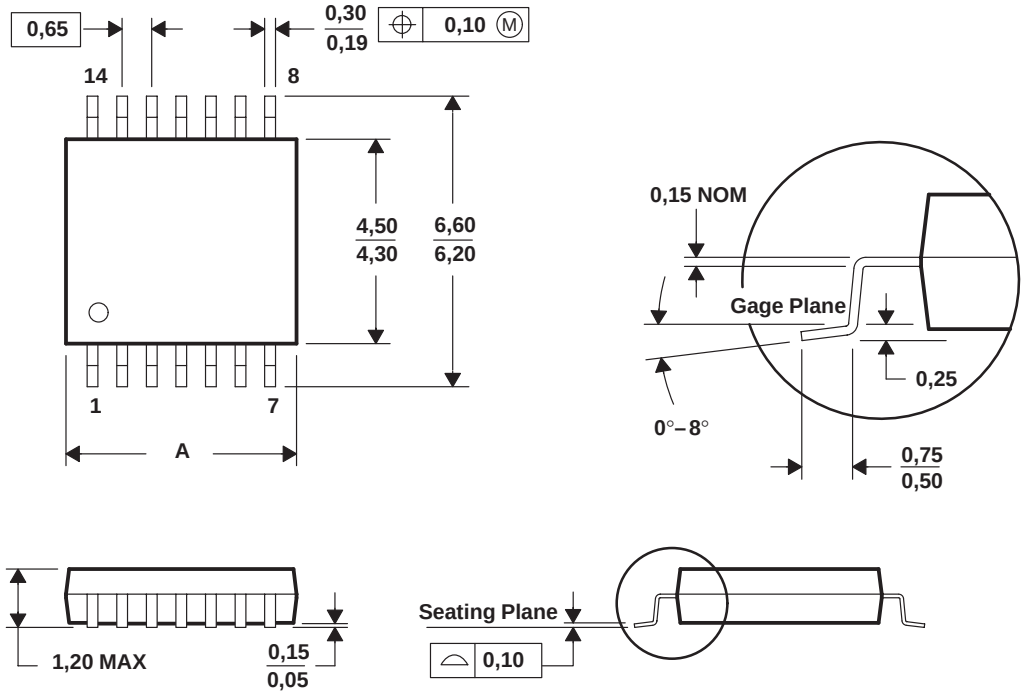
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
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19-0481; Rev 2; 11/92

MAXIM
General Purpose Timers

General Description

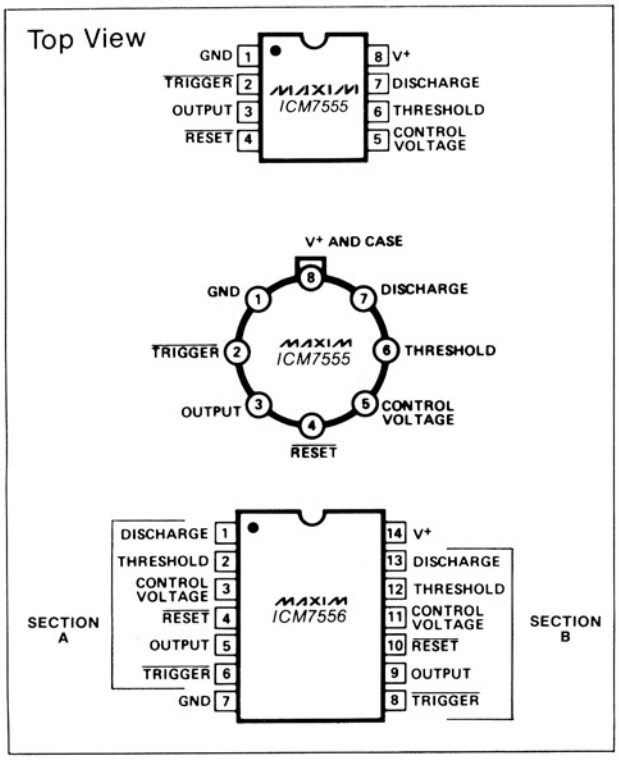
The Maxim ICM7555 and ICM7556 are respectively single and dual general purpose RC timers capable of generating accurate time delays or frequencies. The primary feature is an extremely low supply current, making this device ideal for battery-powered systems. Additional features include low THRESHOLD, TRIGGER, and RESET currents, a wide operating supply voltage range, and improved performance at high frequencies.

These CMOS low-power devices offer significant performance advantages over the standard 555 and 556 bipolar timers. Low-power consumption, combined with the virtually non-existent current spike during output transitions, make these timers the optimal solution in many applications.

Applications

Pulse Generator	Pulse Position Modulation
Precision Timing	Sequential Timing
Time Delay Generation	Missing Pulse Detector
Pulse Width Modulation	

Pin Configuration



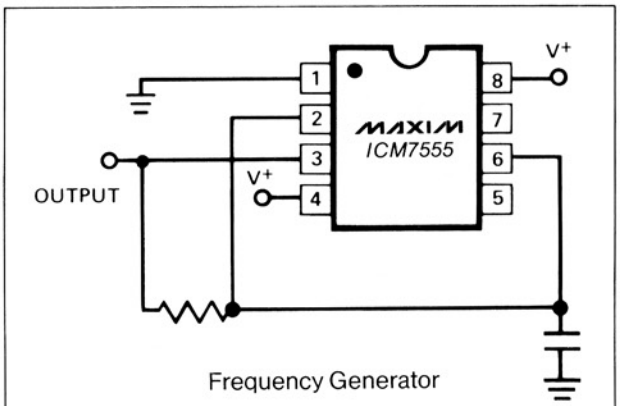
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Wide Supply Voltage Range: 2-18V**
- **No Crowbarring of Supply During Output Transition**
- **Adjustable Duty Cycle**
- **Low THRESHOLD, TRIGGER and RESET Curents**
- **TTL Compatible**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7555IPA	-20°C to +85°C	8 Lead Plastic DIP
ICM7555IJA	-20°C to +85°C	8 Lead CERDIP
ICM7555ITV	-20°C to +85°C	TO-99 Can
ICM7555MJA	-55°C to +125°C	8 Lead CERDIP
ICM7555MTV	-55°C to +125°C	TO-99 Can
ICM7555ISA	-20°C to +85°C	8 Lead Small Outline
ICM7555/D	0°C to +70°C	Dice
ICM7556IPD	-20°C to +85°C	14 Lead Plastic DIP
ICM7556MJD	-55°C to +125°C	14 Lead CERDIP
ICM7556ISD	-20°C to +85°C	14 Lead Small Outline
ICM7556/D	0°C to +70°C	Dice

Typical Operating Circuit



(Detailed Circuit Diagram — Figure-1a)

General Purpose Timers

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... +18 Volts
Input Voltage TRIGGER
Control Voltage THRESHOLD $<V^+ + 0.3V$ to $\geq -0.3V$
RESET

Output Current 100mA
Power Dissipation[2] ICM7556 ..... 300mW
ICM7555 ..... 200mW
Operating Temperature Range
ICM7555IJA (Maxim) ..... −20°C to +85°C
ICM7555ISA (Maxim) ..... −20°C to +85°C
ICM7555IPA ..... −20°C to +85°C
ICM7555ITV ..... −20°C to +85°C
ICM7556IPD ..... −20°C to +85°C
ICM7555MTV ..... −55°C to +125°C
ICM7556MJD ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 60 Seconds) ..... +300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V^+ = +2$ to $+15$ volts; $T_A = 25°C$, Unless Noted)

PARAMETER	SYMBOL	TEST CONDITIONS			VALUE MIN	VALUE TYP	VALUE MAX	UNITS
Supply Voltage	V^+	$-20°C \leq T_A \leq +70°C$ $-55°C \leq T_A \leq +125°C$			2 3		18 16	V V
Supply Current [3]	I^+	ICM7555	$V^+ = 2V$ $V^+ = 18V$			60 120	200 300	µA µA
		ICM7556	$V^+ = 2V$ $V^+ = 18V$			120 240	400 600	µA µA
Timing Error		R_A, R_B = 1k to 100k, $C = 0.1\mu F$	$5V \leq V^+ \leq 15V$					
Initial Accuracy		Note 4				2.0	5.0	%
Drift with Temperature		Note 4	$V^+ = 5V$ $V^+ = 10V$ $V^+ = 15V$			50 75 100		ppm/°C
Drift with Supply Voltage		$V^+ = 5V$				1.0	3.0	%/V
Threshold Voltage	V_{TH}		$V^+ = 5V$		0.63	0.66	0.67	V^+
Trigger Voltage	V_{TRIG}		$V^+ = 5V$		0.29	0.33	0.34	V^+
Trigger Current	I_{TRIG}	$V^+ = 18V$ $V^+ = 5V$ $V^+ = 2V$				50 10 1		pA pA pA
Threshold Current	I_{TH}	$V^+ = 18V$ $V^+ = 5V$ $V^+ = 2V$				50 10 1		pA pA pA
Reset Current	I_{RST}	V_{RESET} = Ground	$V^+ = 18V$ $V^+ = 5V$ $V^+ = 2V$			100 20 2		pA pA pA
Reset Voltage	V_{RST}	$V^+ = 18V$ $V^+ = 2V$			0.4 0.4	0.7 0.7	1.0 1.0	V V
Control Voltage Lead	V_{CV}		$V^+ = 5V$		0.62	0.66	0.67	V^+
Output Voltage Drop	V_O	Output Lo	$V^+ = 18V$ $V^+ = 5V$	$I_{SINK} = 3.2mA$ $I_{SINK} = 3.2mA$		0.1 0.15	0.4 0.4	V V
		Output Hi	$V^+ = 18V$ $V^+ = 5V$	$I_{SOURCE} = 1.0mA$ $I_{SOURCE} = 1.0mA$	17.25 4.0	17.8 4.5		V V
Rise Time of Output	t_r	$R_L = 10M\Omega$	$C_L = 10pF$	$V^+ = 5V$	35	40	75	ns
Fall Time of Output	t_f	$R_L = 10M\Omega$	$C_L = 10pF$	$V^+ = 5V$	35	40	75	ns
Guaranteed Max Osc Freq	f_{max}	Astable Operation			500			kHz

Note 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than $V^+ + 0.3V$ or less than $V^- - 0.3V$ may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.

Note 2: Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).

Note 3: The supply current value is essentially independent of the TRIGGER, THRESHOLD and RESET voltages.

Note 4: Parameter is not 100% tested. Majority of all units meet this specification.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

- **Lower Supply Current**
- **Increased Output Source Current**
- **Guaranteed THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ Input Currents**
- **Guaranteed Discharge Output Voltage**
- **Supply Current Guaranteed Over Temperature**
- **Significantly Improved ESD Protection (Note 6)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = +2 to +15 volts; T_A = 25°C, unless noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V^+	$-20°C \le T_A \le +85°C$ $-55°C \le T_A \le +125°C$	2 3		16.5 16	V V
Supply Current (Note 3)	I^+	**ICM 7555** **V^+ = 2-16.5V; T_A = +25°C** **V^+ = 5V; T_A = +25°C** **V^+ = 5V; $-20°C \le T_A \le +85°C$** **V^+ = 5V; $-55°C \le T_A \le +125°C$**		**30**	**250** **120** **250** **300**	**µA** **µA** **µA** **µA**
		ICM 7556 **V^+ = 2-16.5V; T_A = +25°C** **V^+ = 5V; T_A = +25°C** **V^+ = 5V; $-20°C \le T_A \le +85°C$** **V^+ = 5V; $-55°C \le T_A \le +125°C$**		**60**	**500** **240** **500** **600**	**µA** **µA** **µA** **µA**
Timing Error (Note 4)		Circuit of figure 1(b); $R_A = R_B$ = 100kΩ, C = 0.1µF, V^+ = 5V				
Initial Accuracy (Note 5)				2.0	5.0	%
Drift with Temperature		V^+ = 5V V^+ = 10V V^+ = 15V		50 75 100		ppm/°C ppm/°C ppm/°C
Drift with Supply Voltage		V^+ = 5V		1.0	3.0	%/V
Threshold Voltage	V_{TH}	V^+ = 5V	0.63	0.66	0.67	V^+
Trigger Voltage	V_{TRIG}	V^+ = 5V	0.29	0.33	0.34	V^+
Trigger Current	I_{TRIG}	**V^+ = 16.5V** V^+ = 5V V^+ = 2V		**50** 10 1		**pA** pA pA
Threshold Current	I_{TH}	**V^+ = 16.5V** V^+ = 5V V^+ = 2V		**50** 10 1		**pA** pA pA
Reset Current	I_{RST}	**V_{RESET} = Ground** **V^+ = 16.5V** V^+ = 5V V^+ = 2V		**100** 20 2		**pA** pA pA
Reset Voltage	V_{RST}	V^+ = 16.5V V^+ = 2V	0.4 0.4	0.7 0.7	1.2 1.2	V V
Control Voltage	V_{CV}	V^+ = 5V	0.62	0.66	0.67	V^+
Output Voltage Drop	V_O	Output Lo V^+ = 16.5V I_{SINK} = 3.2mA V^+ = 5V I_{SINK} = 3.2mA		0.1 0.15	0.4 0.4	V V
		Output Hi **V^+ = 16.5V** **I_{SOURCE} = 2.0mA** **V^+ = 5V** **I_{SOURCE} = 2.0mA**	15.75 4.0	16.25 4.5		V V
Discharge Output Voltage	V_{DIS}	**V^+ = 5V, I_{DIS} = 3.2mA**		**0.1**	**0.4**	**V**
Rise Time of Output (Note 4)	t_r	R_L = 10MΩ C_L = 10pF V^+ = 5V	35	40	75	ns
Fall Time of Output (Note 4)	t_f	R_L = 10MΩ C_L = 10pF V^+ = 5V	35	40	75	ns
Guaranteed Max Osc. Freq. (Note 4)	f_{max}	Astable Operation	500			kHz

Note 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ +0.3V or less than V^- −0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.

Note 2: Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).

Note 3: The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD AND $\overline{\text{RESET}}$ voltages.

Note 4: Parameter is not 100% tested. Majority of all units meet this specification.

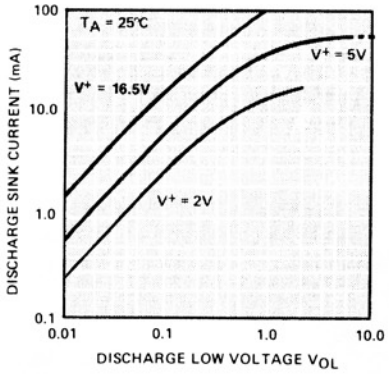
Note 5: Deviation from $f = 1.46/(R_A + 2R_B)C$, V^+ = 5V.

Note 6: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Mil Std 883B, Method 3015.1 Test Circuit.)

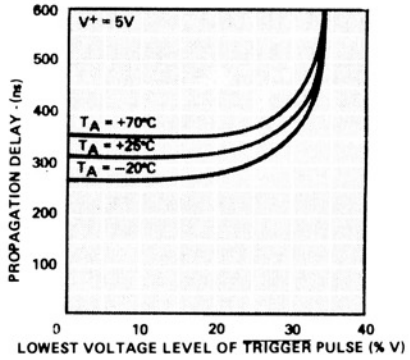
General Purpose Timers

Typical Operating Characteristics

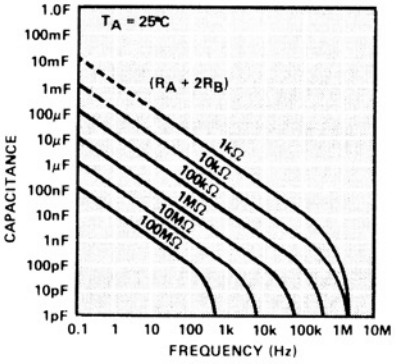
DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



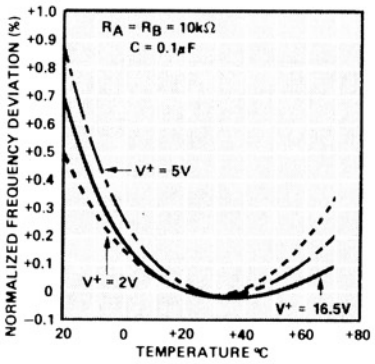
PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



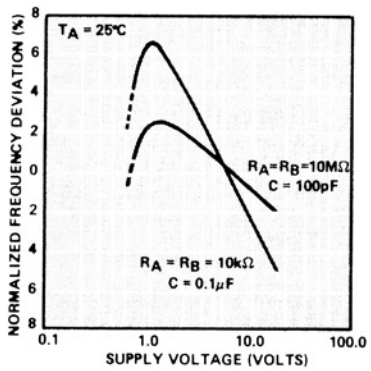
FREE RUNNING FREQUENCY AS A FUNCTION OF R_A, R_B AND C



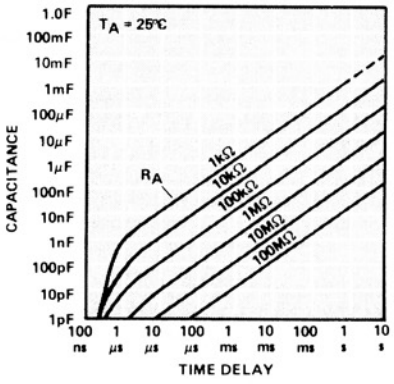
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



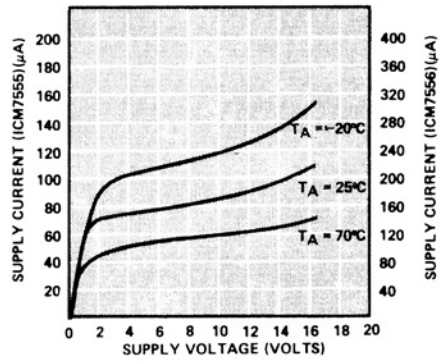
TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF R_A AND C



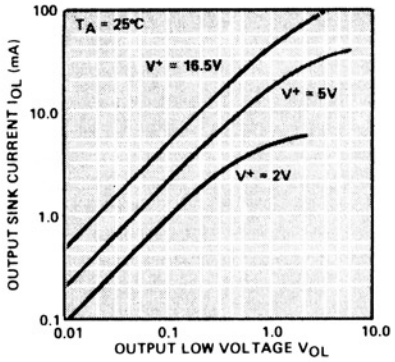
MAXIM

Typical Operating Characteristics

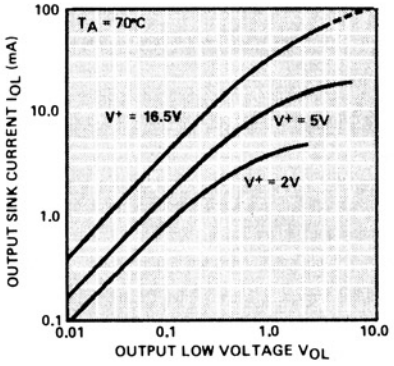
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



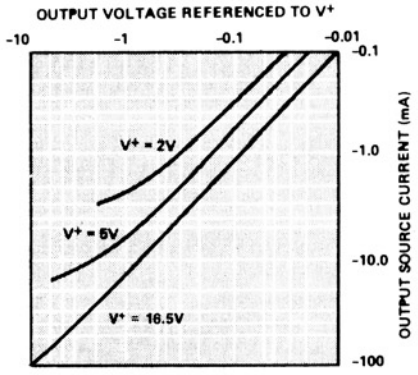
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



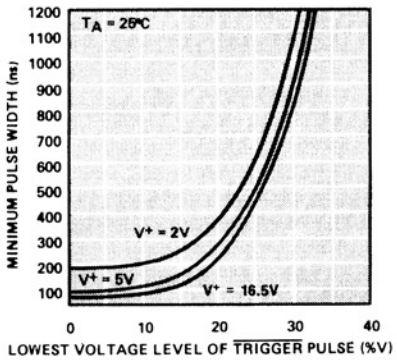
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



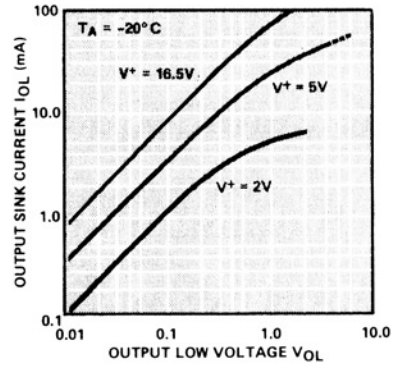
OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



General Purpose Timers

Detailed Description

Both the ICM7555 timer and the ICM7556 dual timer can be configured for either astable or monostable operation. In the astable mode the free running frequency and the duty cycle are controlled by two external resistors and one capacitor. Similarly, the pulse width in the monostable mode is precisely controlled by one external resistor and capacitor.

The external component count is decreased when replacing a bipolar timer with the ICM7555 or ICM7556. The bipolar devices produce large crowbar currents in the output driver. To compensate for this spike, a capacitor is used to decouple the power supply lines. The CMOS timers produce supply spikes of only 2-3mA vs. 300-400mA (Bipolar), therefore supply decoupling is typically not needed. This current spike comparison is illustrated in Figure 3. Another component is eliminated at the control voltage pin. These CMOS timers, due to the high impedance inputs of the comparators, do not require decoupling capacitors on the control voltage pin.

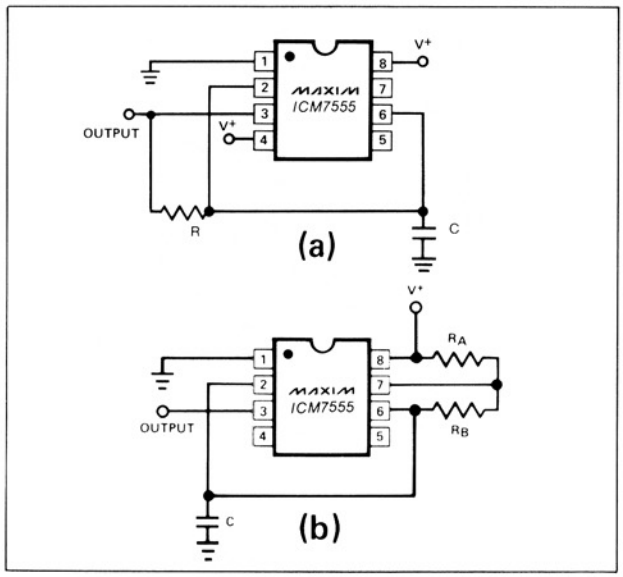


Figure 1. Maxim ICM7555 used in two different astable configurations.

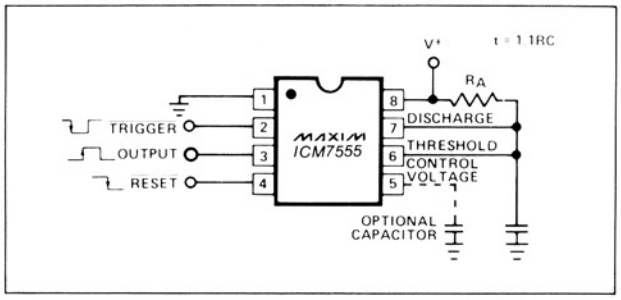


Figure 2. Maxim ICM7555 in a monostable operation.

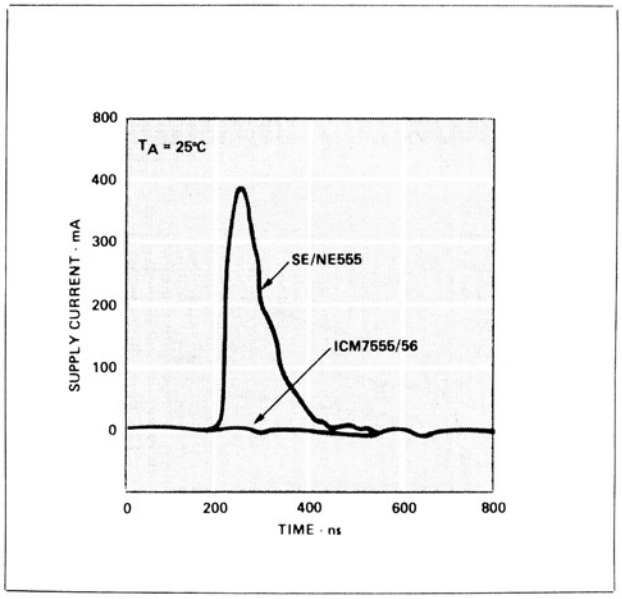


Figure 3. Supply current transient compared with a standard bipolar 555 during an output transition.

Applications Information

Astable Operation

We recommend either of the two astable circuit configurations illustrated in Figure 1. The circuit in (1a) provides a 50% duty cycle output using one timing resistor and capacitor. The oscillator waveform across the capacitor is symmetrical and triangular, swinging from ⅓ to ⅔ of the supply voltage. The frequency generated is defined by:

$$f = \frac{1}{1.4\ RC}$$

The circuit in (1b) provides a means of varying the duty cycle of the oscillator. The frequency is defined by:

$$f = \frac{1.46}{(R_A + 2R_B)C}$$

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

Monostable Operation

The circuit diagram in Figure 2 illustrates monostable operation. In this mode the timer acts as a one shot. Initially the external capacitor is held discharged by the discharge output. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the capacitor begins to charge exponentially through R_A. The device resets after the voltage across the capacitor reaches ⅔(V^+).

$$t_{output} = -\ln(⅓)R_AC = 1.1\ R_AC$$

Reset

The reset function is significantly improved over the standard bipolar 555 and 556 in that it controls only the internal flip-flop, which in turn simultaneously controls the state of the Output and Discharge pins. This avoids the multiple threshold problems sometimes encountered with slow-falling edges of the bipolar devices. This input is designed to have essentially the same trip voltage as the standard bipolar devices (0.6 to 0.7V). At all supply voltages this input maintains an extremely high impedance.

Control Voltage

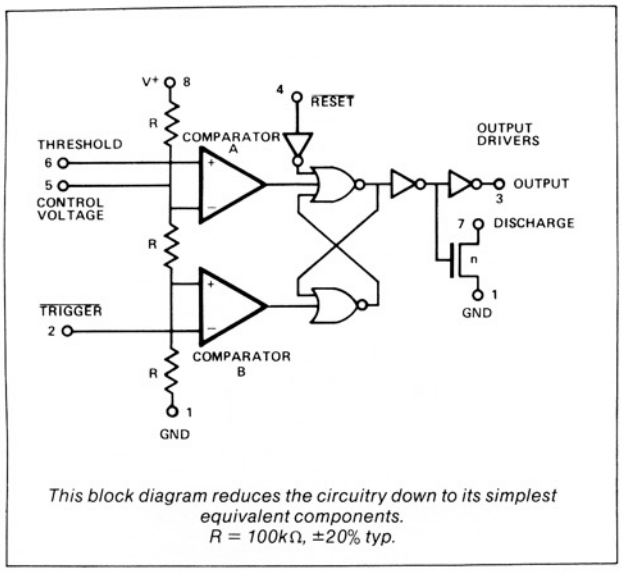
The control voltage regulates the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators. This pin can be used for frequency modulation in the astable mode. By varying the applied voltage to the control voltage pin, delay times can be changed in the monostable mode.

Power Supply Considerations

Since the $\overline{\text{TRIGGER}}$, THRESHOLD and Discharge leakage currents are very low, high impedance timing components may be used, keeping total system supply current at a minimum.

Output Drive Capability

The CMOS output stage is capable of driving most logic families including CMOS and TTL. The ICM7555 and ICM7556 will drive at least two standard TTL loads at a supply voltage of 4.5V or greater. When driving CMOS, the output swing at all supply voltage levels will equal the supply voltage.



This block diagram reduces the circuitry down to its simplest equivalent components.
R = 100kΩ, ±20% typ.

Figure 4. Block diagram of ICM7555.

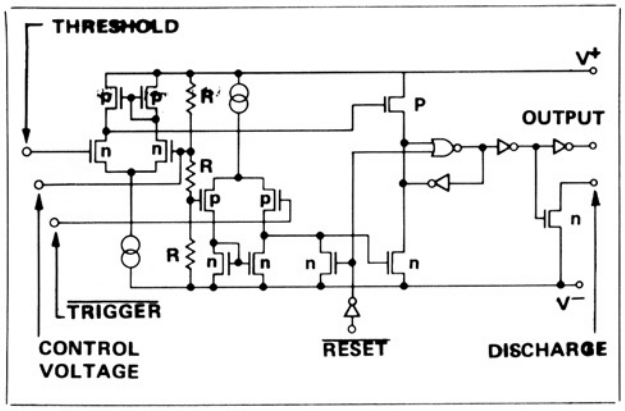


Figure 5. Equivalent circuit.

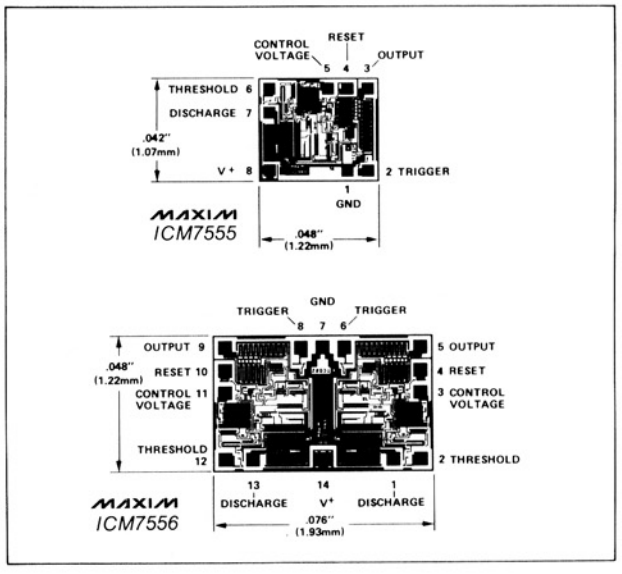
Function Table

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	$< \frac{1}{3} V^+$	Irrelevant	High	Off
High	$> \frac{1}{3} V^+$	$> \frac{2}{3} V^+$	Low	On
High	$> \frac{1}{3} V^+$	$< \frac{2}{3} V^+$	As previously established	

†Voltages levels shown are nominal.

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs. $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

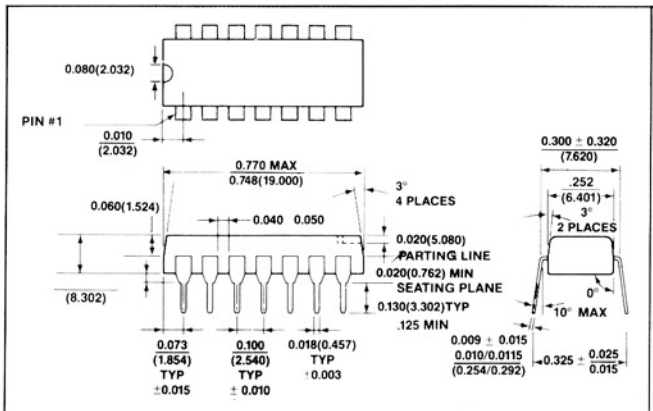
Chip Topographies



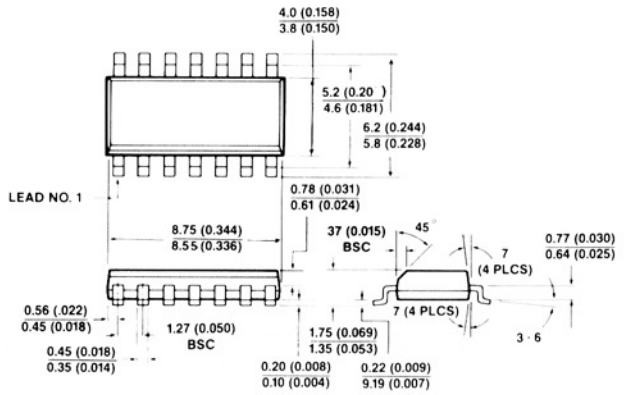
General Purpose Timers

Package Information

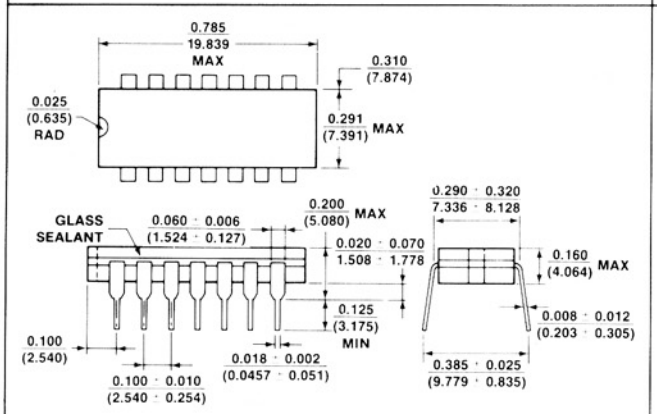
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



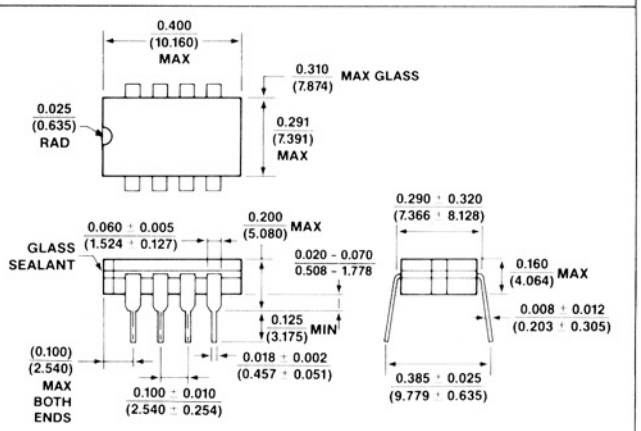
14 Lead Plastic DIP (PD)
θ_{JA} = 140° C/W
θ_{JC} = 70° C/W



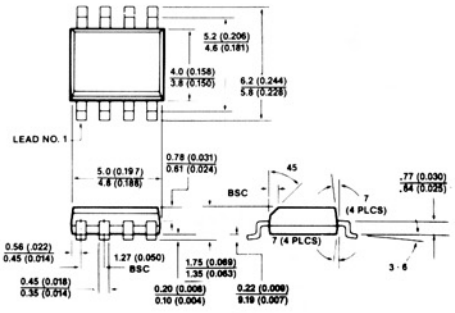
14-Lead Small Outline (SO)



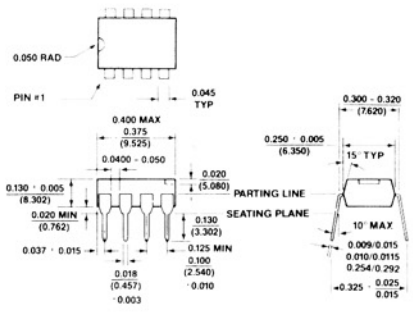
14 Lead CERDIP (JD)
θ_{JA} = 105° C/W
θ_{JC} = 50° C/W



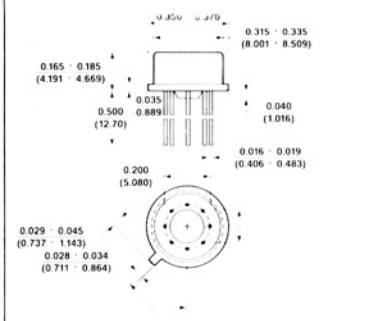
8 Lead CERDIP (JA)
θ_{JA} = 125° C/W
θ_{JC} = 55° C/W



8-Lead Small Outline (SO)



8 Lead Plastic DIP (PA)
θ_{JA} = 160° C/W
θ_{JC} = 75° C/W



8 Lead TO-99 Can (TV)
θ_{JA} = 150° C/W
θ_{JC} = 45° C/W

FAIRCHILD SEMICONDUCTOR™

April 2000

QFET™

FQPF2P25

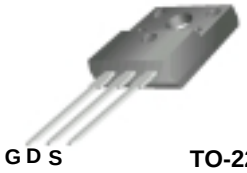
250V P-Channel MOSFET

General Description

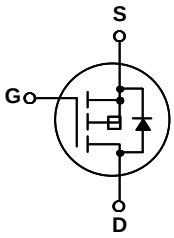
These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters.

Features

- -1.8A, -250V, $R_{DS(on)}$ = 4.0Ω @V_{GS} = -10 V
- Low gate charge (typical 6.5 nC)
- Low Crss (typical 6.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220F
FQPF Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQPF2P25	Units
V_{DSS}	Drain-Source Voltage		-250	V
I_D	Drain Current - Continuous (T_C = 25°C)		-1.8	A
	- Continuous (T_C = 100°C)		-1.14	A
I_{DM}	Drain Current - Pulsed	(Note 1)	-7.2	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	120	mJ
I_{AR}	Avalanche Current	(Note 1)	-1.8	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	3.2	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-5.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		32	W
	- Derate above 25°C		0.26	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	3.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-250	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 µA, Referenced to 25°C	--	-0.2	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -250 V, V_{GS} = 0 V	--	--	-1	µA
		V_{DS} = -200 V, T_C = 125°C	--	--	-10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -0.9 A	--	3.15	4.0	Ω
g_{FS}	Forward Transconductance	V_{DS} = -40 V, I_D = -0.9 A (Note 4)	--	1.08	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	190	250	pF
C_{oss}	Output Capacitance		--	40	55	pF
C_{rss}	Reverse Transfer Capacitance		--	6.5	8.5	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -125 V, I_D = -2.3 A, R_G = 25 Ω (Note 4, 5)	--	8.5	25	ns
t_r	Turn-On Rise Time		--	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		--	12	35	ns
t_f	Turn-Off Fall Time		--	25	60	ns
Q_g	Total Gate Charge	V_{DS} = -200 V, I_D = -2.3 A, V_{GS} = -10 V (Note 4, 5)	--	6.5	8.5	nC
Q_{gs}	Gate-Source Charge		--	1.8	--	nC
Q_{gd}	Gate-Drain Charge		--	3.0	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-1.8	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	7.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.8 A	--	--	-5.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -2.3 A, dI_F / dt = 100 A/µs (Note 4)	--	110	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.4	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 59mH, I_{AS} = -1.8A, V_{DD} = -50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ -2.3A, di/dt ≤ 300A/µs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

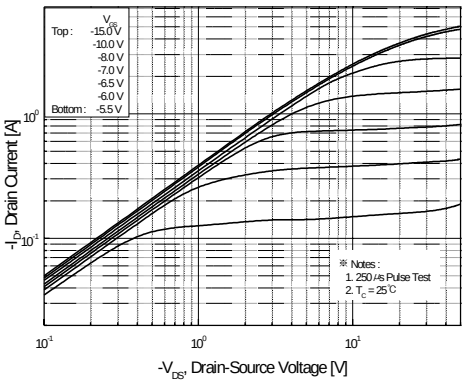


Figure 1. On-Region Characteristics

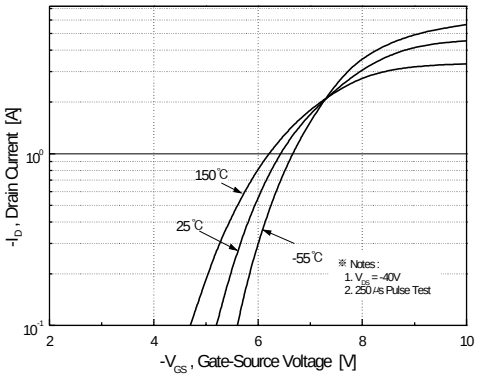


Figure 2. Transfer Characteristics

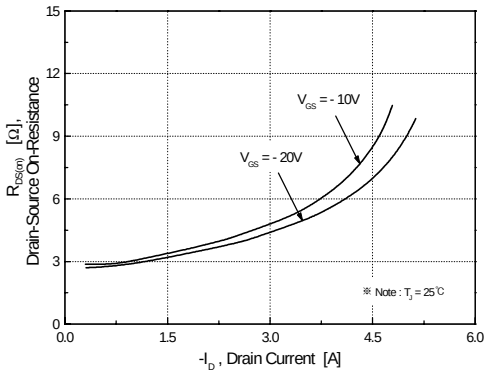


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

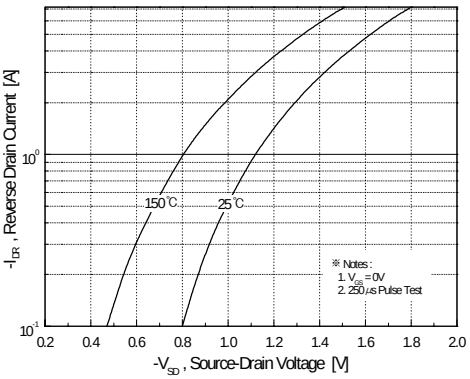


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

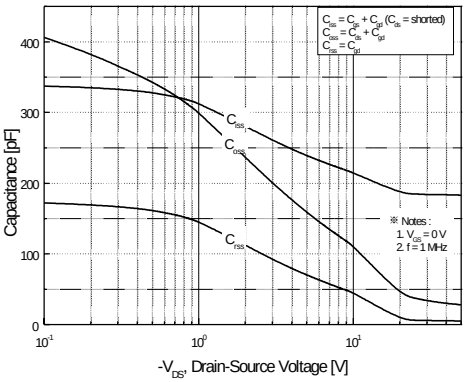


Figure 5. Capacitance Characteristics

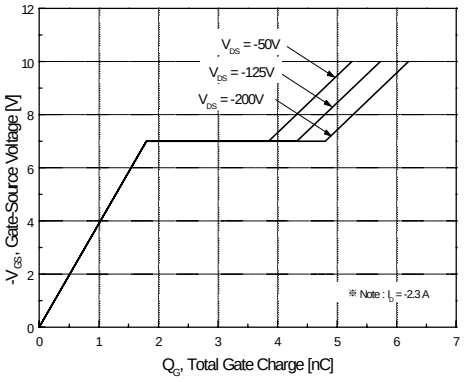


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

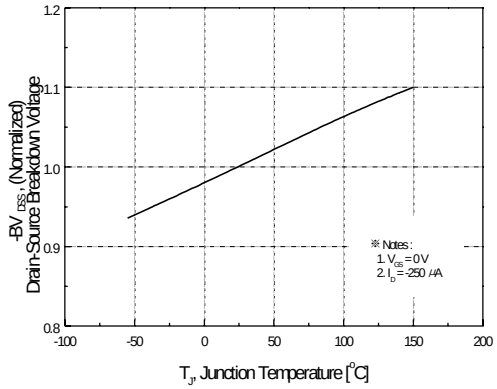


Figure 7. Breakdown Voltage Variation vs. Temperature

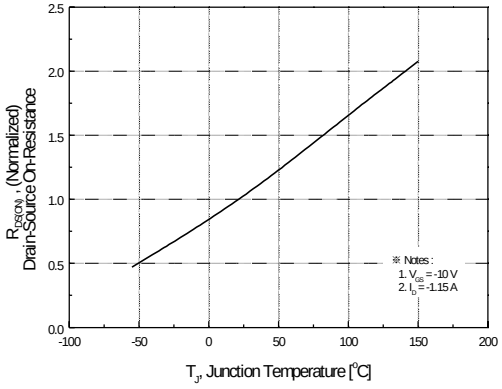


Figure 8. On-Resistance Variation vs. Temperature

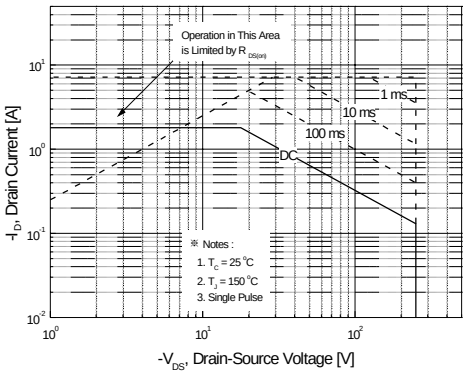


Figure 9. Maximum Safe Operating Area

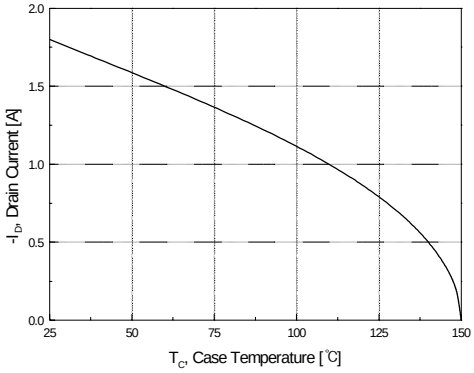


Figure 10. Maximum Drain Current vs. Case Temperature

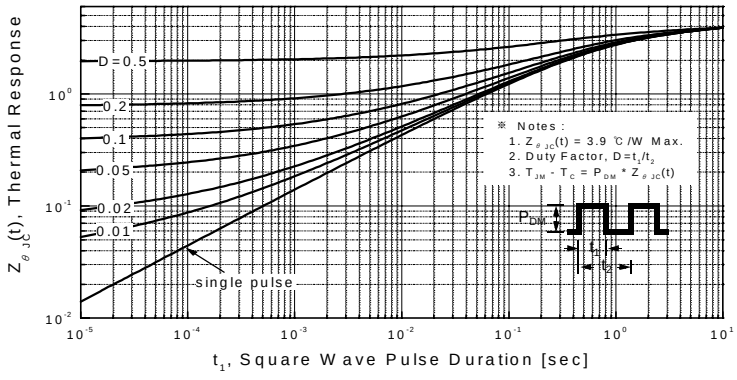
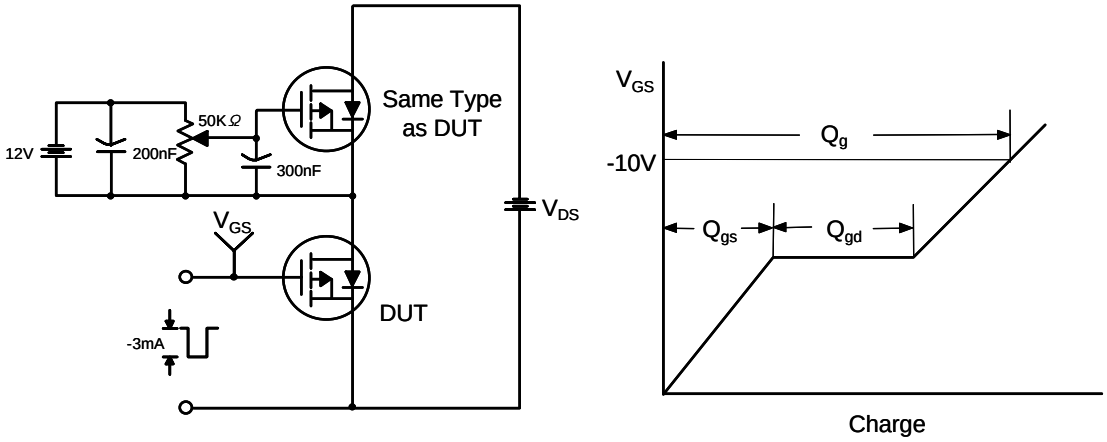
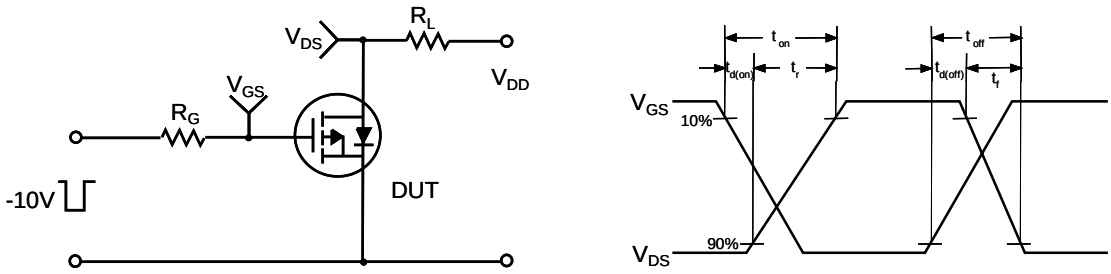


Figure 11. Transient Thermal Response Curve

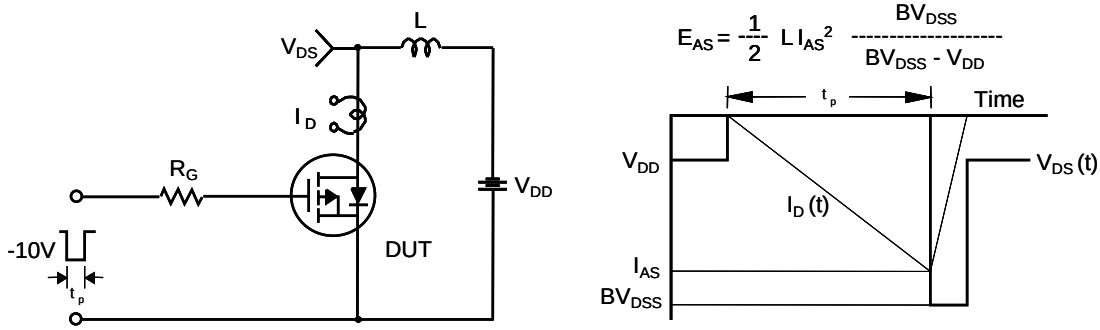
Gate Charge Test Circuit & Waveform



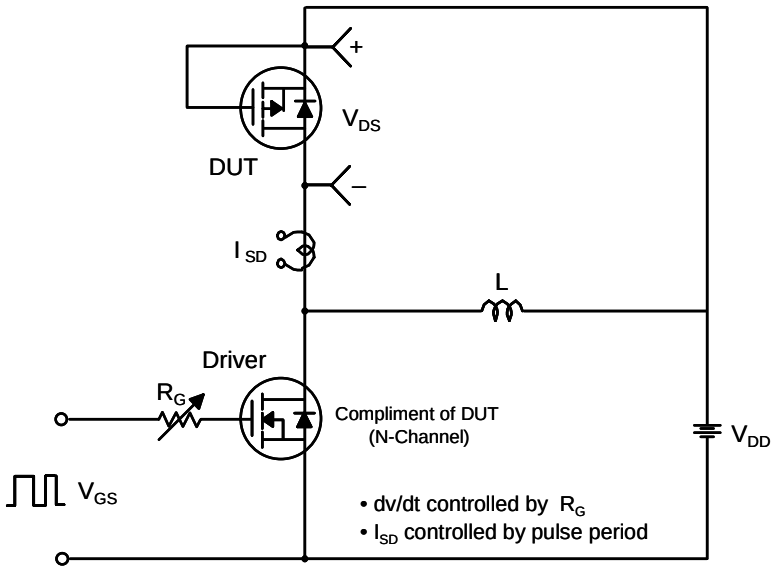
Resistive Switching Test Circuit & Waveforms

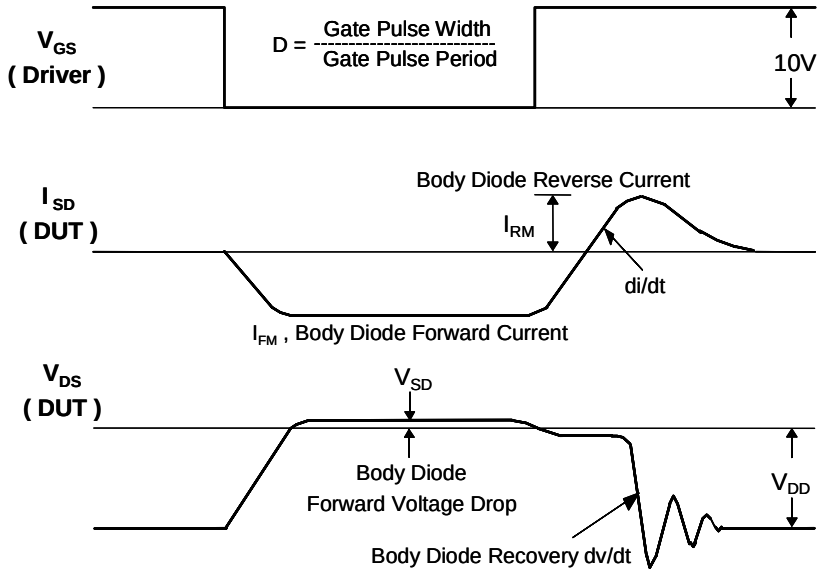


Unclamped Inductive Switching Test Circuit & Waveforms



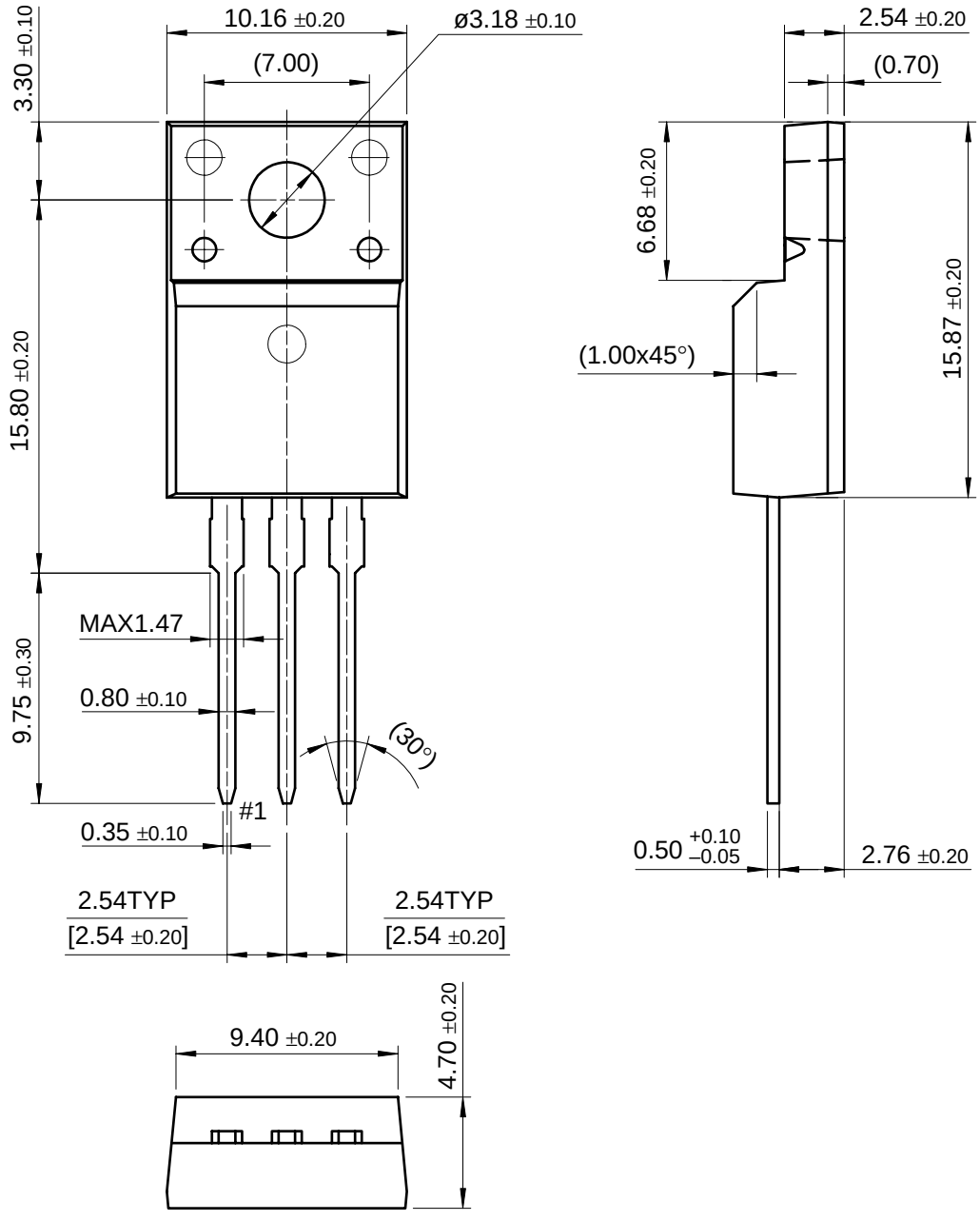
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimensions

TO-220F



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GTO™
HiSeC™
ISOPLANAR™
MICROWIRE™
POP™
PowerTrench®
QFET™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TinyLogic™
UHC™
VCX™

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

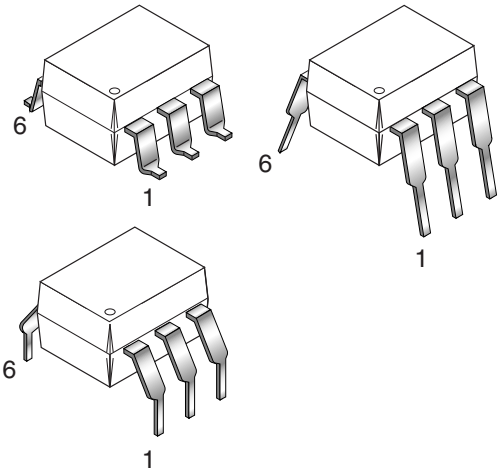
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FAIRCHILD
SEMICONDUCTOR®

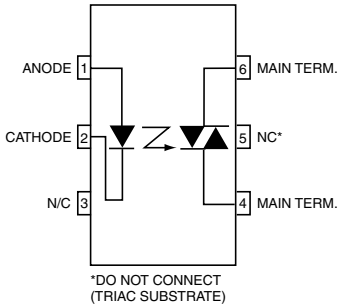
6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

MOC3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

PACKAGE



SCHEMATIC



DESCRIPTION

The MOC301XM and MOC302XM series are optically isolated triac driver devices. These devices contain a GaAs infrared emitting diode and a light activated silicon bilateral switch, which functions like a triac. They are designed for interfacing between electronic controls and power triacs to control resistive and inductive loads for 115 VAC operations.

FEATURES

- Excellent I_{FT} stability—IR emitting diode has low degradation
- High isolation voltage—minimum 5300 VAC RMS
- Underwriters Laboratory (UL) recognized—File #E90700
- Peak blocking voltage
  - 250V-MOC301XM
  - 400V-MOC302XM
- VDE recognized (File #94766)
  - Ordering option V (e.g. MOC3023VM)

APPLICATIONS

- Industrial controls
- Traffic lights
- Vending machines
- Solid state relay
- Lamp ballasts
- Solenoid/valve controls
- Static AC power switch
- Incandescent lamp dimmers
- Motor control

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameters	Symbol	Device	Value	Units
TOTAL DEVICE				
Storage Temperature	T_{STG}	All	-40 to +150	°C
Operating Temperature	T_{OPR}	All	-40 to +85	°C
Lead Solder Temperature	T_{SOL}	All	260 for 10 sec	°C
Junction Temperature Range	T_J	All	-40 to +100	°C
Isolation Surge Voltage(1) (peak AC voltage, 60Hz, 1 sec duration)	V_{ISO}	All	7500	Vac(pk)
Total Device Power Dissipation @ 25°C	P_D	All	330	mW
Derate above 25°C			4.4	mW/°C
EMITTER				
Continuous Forward Current	I_F	All	60	mA
Reverse Voltage	V_R	All	3	V
Total Power Dissipation 25°C Ambient	P_D	All	100	mW
Derate above 25°C			1.33	mW/°C
DETECTOR				
Off-State Output Terminal Voltage	V_{DRM}	MOC3010M/1M/2M MOC3020M/1M/2M/3M	250 400	V
Peak Repetitive Surge Current (PW = 1 ms, 120 pps)	I_{TSM}	All	1	A
Total Power Dissipation @ 25°C Ambient	P_D	All	300	mW
Derate above 25°C			4	mW/°C

Note

1. Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameters	Test Conditions	Symbol	Device	Min	Typ	Max	Units
EMITTER							
Input Forward Voltage	I_F = 10 mA	V_F	All		1.15	1.5	V
Reverse Leakage Current	V_R = 3 V, T_A = 25°C	I_R	All		0.01	100	µA
DETECTOR							
Peak Blocking Current,Either Direction	Rated V_{DRM}, I_F = 0 (note 1)	I_{DRM}	All		10	100	nA
Peak On-State Voltage,Either Direction	I_{TM} = 100 mA peak, I_F = 0	V_{TM}	All		1.8	3	V

TRANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

DC Characteristics	Test Conditions	Symbol	Device	Min	Typ	Max	Units
LED Trigger Current	Voltage = 3V (note 3)	I_{FT}	MOC3020M			30	mA
			MOC3010M			15	
			MOC3021M				
			MOC3011M			10	
			MOC3022M				
			MOC3012M			5	
			MOC3023M				
Holding Current, Either Direction		I_H	All		100		µA

Note

1. Test voltage must be applied within dv/dt rating.
2. This is static dv/dt. See Figure 5 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.
3. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (30 mA for MOC3020M, 15 mA for MOC3010M and MOC3021M, 10 mA for MOC3011M and MOC3022M, 5 mA for MOC3012M and MOC3023M) and absolute max I_F (60 mA).

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

Fig. 1 LED Forward Voltage vs. Forward Current

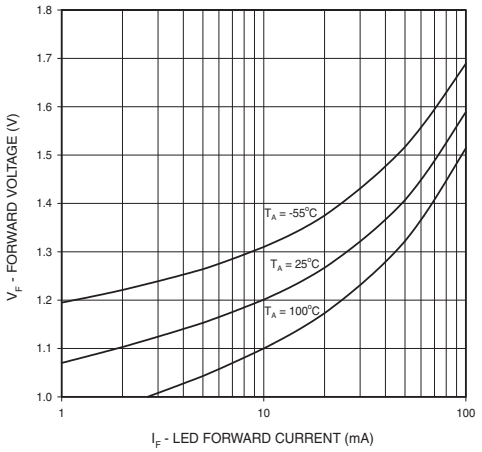


Fig. 2 On-State Characteristics

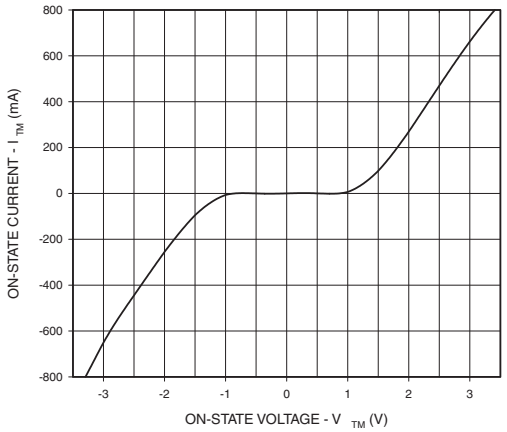


Fig. 3 Trigger Current vs. Ambient Temperature

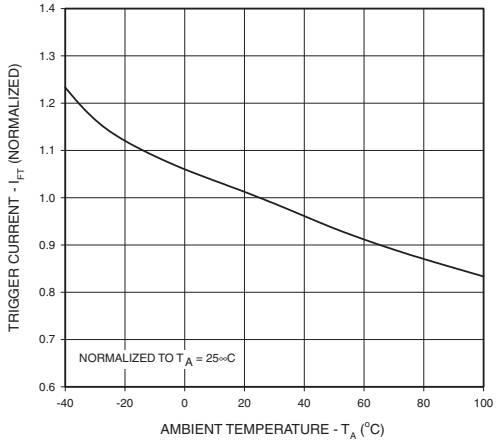


Fig. 4 LED Current Required to Trigger vs. LED Pulse Width

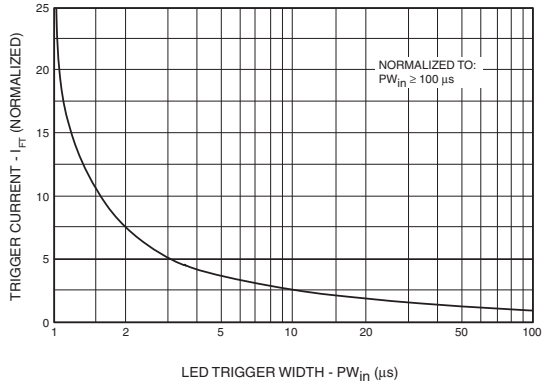


Fig. 5 dv/dt vs. Temperature

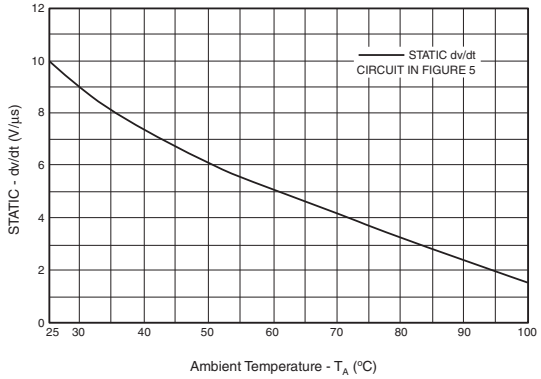
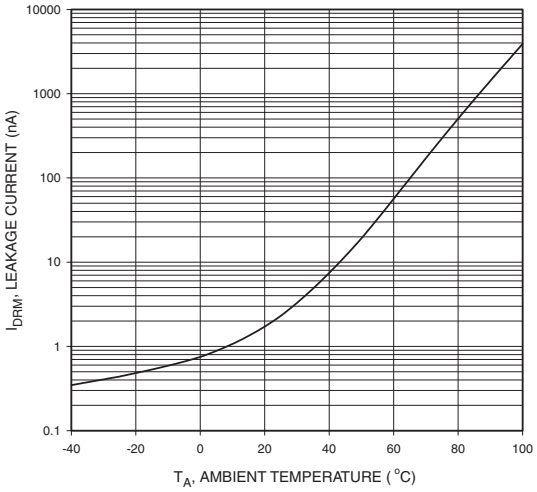
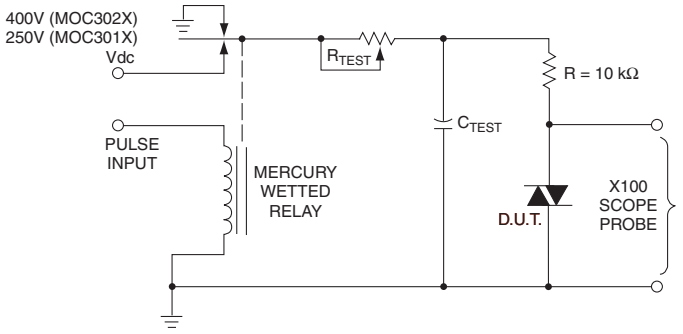


Fig. 6 Leakage Current, I_{DRM} vs. Temperature





1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst-case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

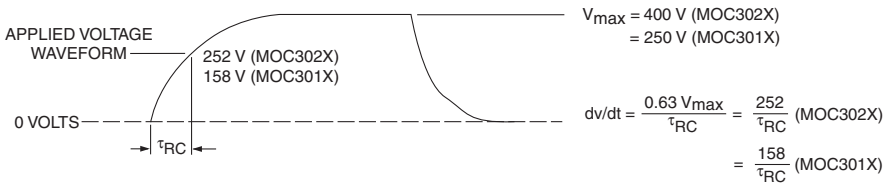


Figure 5. Static dv/dt Test Circuit

Note: This optoisolator should not be used to drive a load directly. It is intended to be a trigger device only.

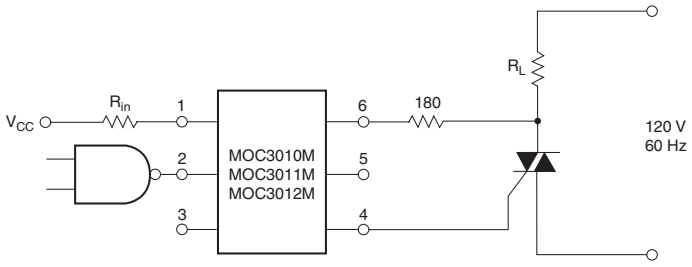


Figure 6. Resistive Load

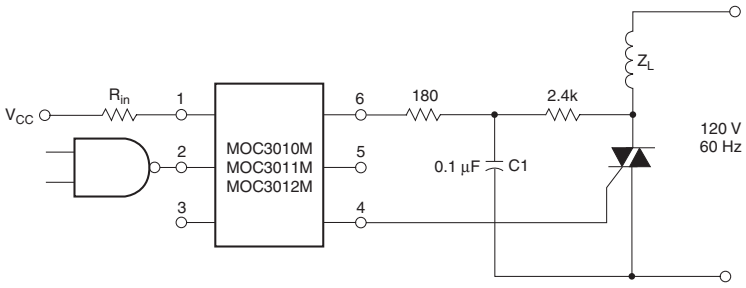


Figure 7. Inductive Load with Sensitive Gate Triac ($I_{GT} \leq 15$ mA)

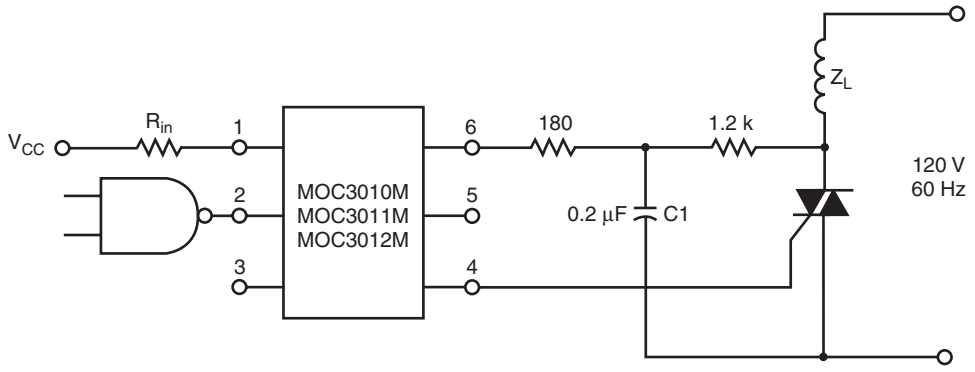
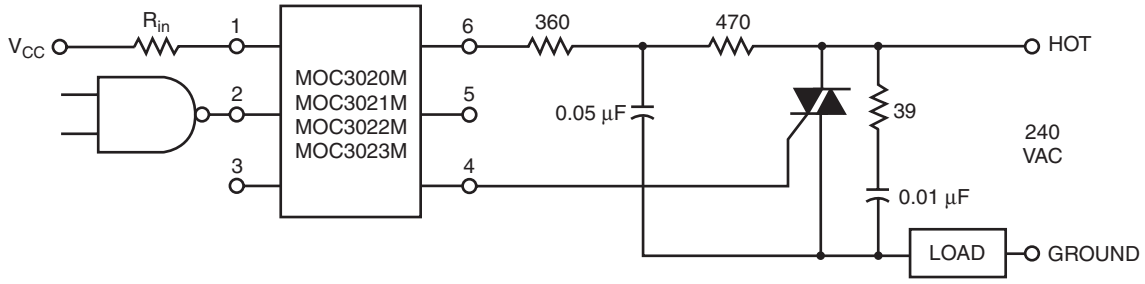


Figure 8. Inductive Load with Sensitive Gate Triac ($I_{GT} \leq 15$ mA)



In this circuit the “hot” side of the line is switched and the load connected to the cold or ground side.

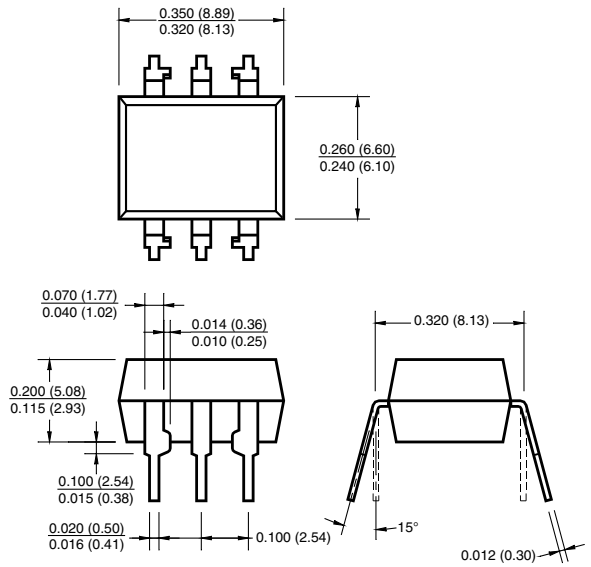
The 39 ohm resistor and 0.01µF capacitor are for snubbing of the triac, and the 470 ohm resistor and 0.05 µF capacitor are for snubbing the coupler. These components may or may not be necessary depending upon the particular and load used.

Figure 9. Typical Application Circuit

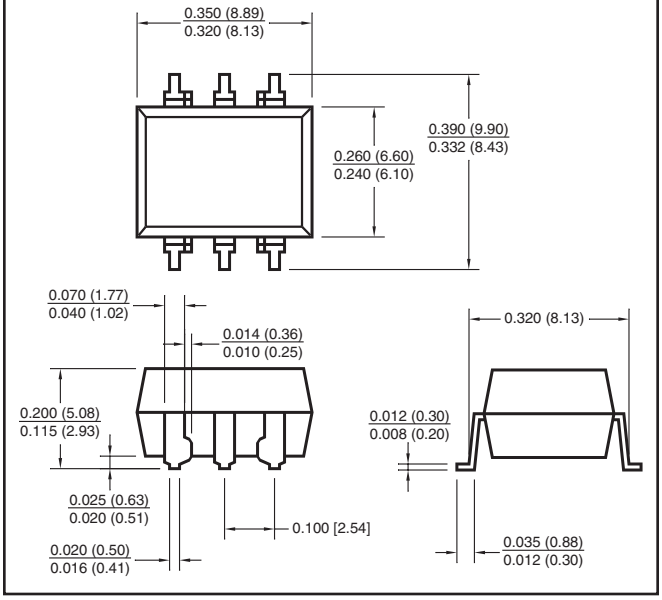
6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

MOC3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

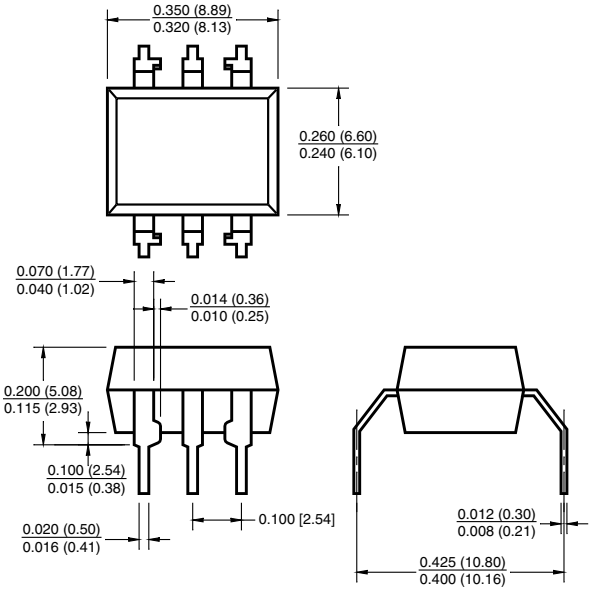
Package Dimensions (Through Hole)



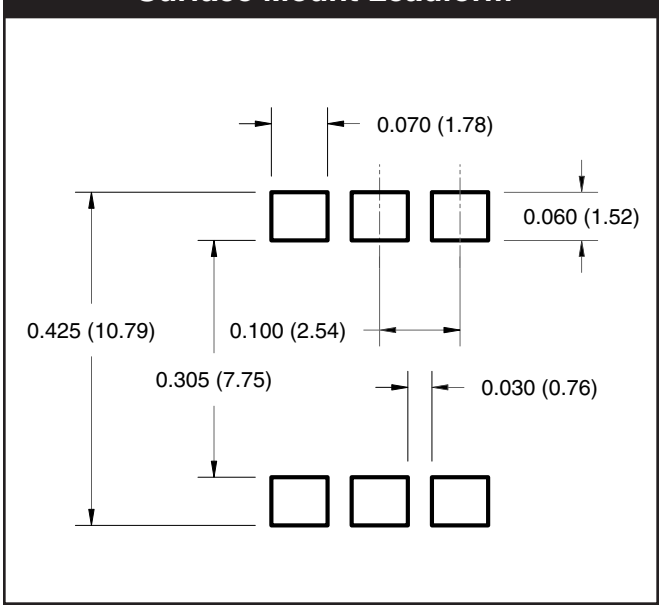
Package Dimensions (Surface Mount)



Package Dimensions (0.4” Lead Spacing)



Recommended Pad Layout for Surface Mount Leadform

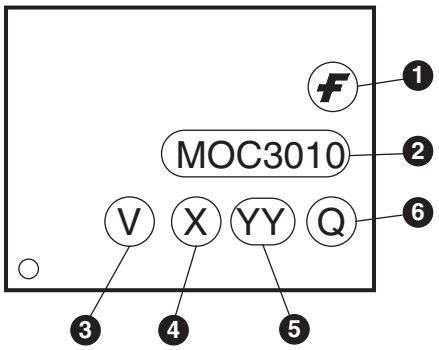


NOTE
All dimensions are in inches (millimeters)

ORDERING INFORMATION

Option	Order Entry Identifier	Description
S	S	Surface Mount Lead Bend
SR2	SR2	Surface Mount; Tape and reel
T	T	0.4" Lead Spacing
V	V	VDE 0884
TV	TV	VDE 0884, 0.4" Lead Spacing
SV	SV	VDE 0884, Surface Mount
SR2V	SR2V	VDE 0884, Surface Mount, Tape & Reel

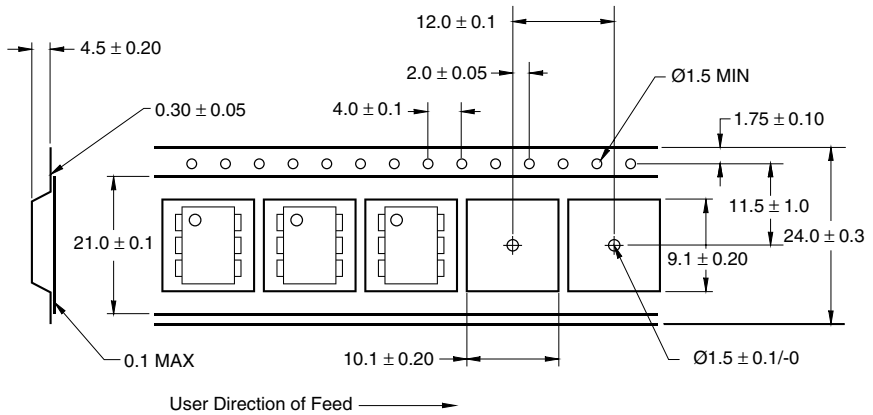
MARKING INFORMATION



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '3'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

*Note – Parts that do not have the 'V' option (see definition 3 above) that are marked with date code '325' or earlier are marked in portrait format.

Carrier Tape Specifications



NOTE
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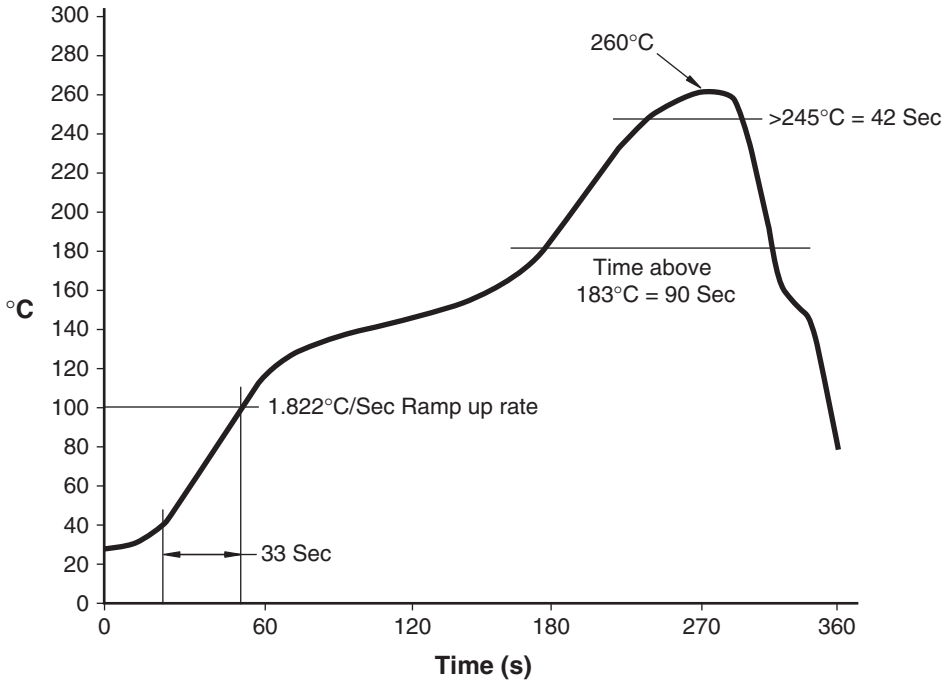
Reflow Profile (White Package, -M Suffix)



6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

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