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An 8x1 Wideband Antenna Phased Array

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An 8x1 Wideband Antenna Phased Array



A Major Qualifying Project Report submitted to the Faculty of
WORCESTER POLYTECHNIC INSTITUTE
in partial fulfillment of the requirements for the Degree of Bachelor of Science

Submitted By

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Abstract

In this project, we are trying to detect the direction of arrival of incoming radiation in the far-field region. To achieve this, we implemented a very flexible and low cost wideband 8x1 antenna phased array receiver system that performs digital beamforming. We designed and built ten aperture coupled patch antennas, radio-frequency (RF) front ends for each channel, intermediate-frequency (IF) stage blocks. Finally, we stored the data on the first-in-first-out (FIFO) memory placed on a Virtex5 FPGA on which we built a microblaze microcontroller that uses SPI to control programmable RF devices and transfers data to computer for further processing. Super-resolution direction of arrival and model order detection algorithms were implemented to perform the digital beamforming.

Acknowledgements

This project would not have been possible without the academic and financial support of our advisor Professor Sergey N. Makarov and wise guidance of Professor Alexander E. Emanuel. In addition, we wish to express our gratitude to Mr. Eric Newman from Analog Devices, Inc. and to Mr. Steve Janesch from RFMD for their generous support in providing us with evaluation boards for several RF components and their guidance at various stages of our project. We would also like to thank Mr. Angelo Puzella from Raytheon for his willingness to share his valuable experience with us. We are thankful to Professor Reinhold Ludwig for his guidance during the development of our filter design. We are also grateful to Professors Alexander Wyglisnki and Berk Sunar for providing us with laboratory equipment necessary to make some of the measurements in this report. We are also thankful to Mr. Jeffrey Elloian for his help in debugging our antenna simulation in Ansoft HFSS. Finally, we would like to thank Mr. Neil R. Whitehouse for his support during the manufacturing of the antenna.

Executive Summary

Phased array antenna receiver is a combination of multiple antennas to form a complex geometry. This combination can be useful to extract additional features of the received signal. One aspect that can be extracted is the varying phase across antennas due to their relative spacing. This allows for the manipulation of phases of the incoming signal in each channel in order to point the radiation pattern in specific direction. The original goal of our project was to read data from temperature wireless sensors placed in unfriendly environments. Due to economic hardship faced by our original sponsor, we were to change the project goals to something more generally applicable and marketable. A product that detects the direction of arrival of GSM signals appeared to fulfill that requirement. Our project objective was then defined as estimating the direction of arrival of incoming radiation in the far field using an eight element one-dimensional phased array with the entire receiver system that performs digital beam forming in a wide range of frequencies. Our frequency band of interest was 800 MHz to 950 MHz, since we wanted to cover several GSM bands. Relatively wide band of frequencies at such a popular range makes our product very attractive. Since the cost of building phased arrays is very large, they are commercially not very widely used. Therefore, we aimed to scale down the cost of our phased array system by proposing an innovative design. In addition, we wanted to create a flexible solution that would allow users to utilize our product for various wireless applications. Software modifications enable our product to assess various information about data, frequency or spatial location of radiators in our band of interest. The principle of operation of our phased array system design is described in the next section.

Brief description of phased arrays and beam-forming

Wireless communication allows a transmitter and a receiver to share the data using electromagnetic waves in space. After passing a very small distance, the radiated wave enters the far field region, where it becomes almost a perfect plane wave. Once it reaches the first antenna element of the one-dimensional array, it excites the antenna usually with a very weak signal (between -80 dBm and -40 dBm). The second element in the array will receive the same signal, but with some time delay. This time delay effectively becomes the phase shift. The same scenario will occur for all subsequent antennas, and therefore, the signal strength is the same in

all of them, but the respective phase is different. If we introduce an incremental phase shift in each of the channels, we can find where the signal strength is the largest due to constructive interference of the waves. Depending on the phase shift that we introduced, the corresponding directional angle of the received signal can be determined. This technique is called beamforming and can be done in two ways. The analog method usually involves a microwave or radio frequency manually tunable phase shifters at each channel in order to steer in a specific direction. Digital beamforming, on the other hand, collects all the data, and introduces the phase shift after capturing the data. Advantage of analog phase shifters is that we can point in the desired direction, and hence, reduce the strength of signals generated by unwanted radiators. This feature greatly reduces the complexity of digital backend. A disadvantage of this approach is the large cost of each phase shifter, which greatly exceeds the budget of our project. A digital beamforming approach became very popular recently due to smaller cost, and greater flexibility that is associated with the nature of digital algorithms that can be easily re-programmed in case they need improvement. The price that we pay for this commodity is the complexity of algorithms that we will use, and the computational power that is required by whatever processor we are planning to use.

System-level solution overview

To meet such ambitious design requirements as outlined in the previous section, we developed a complex receiver system that has eight channels, each of which including an antenna, a radio-frequency (RF) front end, intermediate-frequency (IF) stage, interface board to route the high-speed and low-speed lines and finally a field programmable gate array (FPGA) with first-in-first-out (FIFO) memory. Our system is described in the following figure:

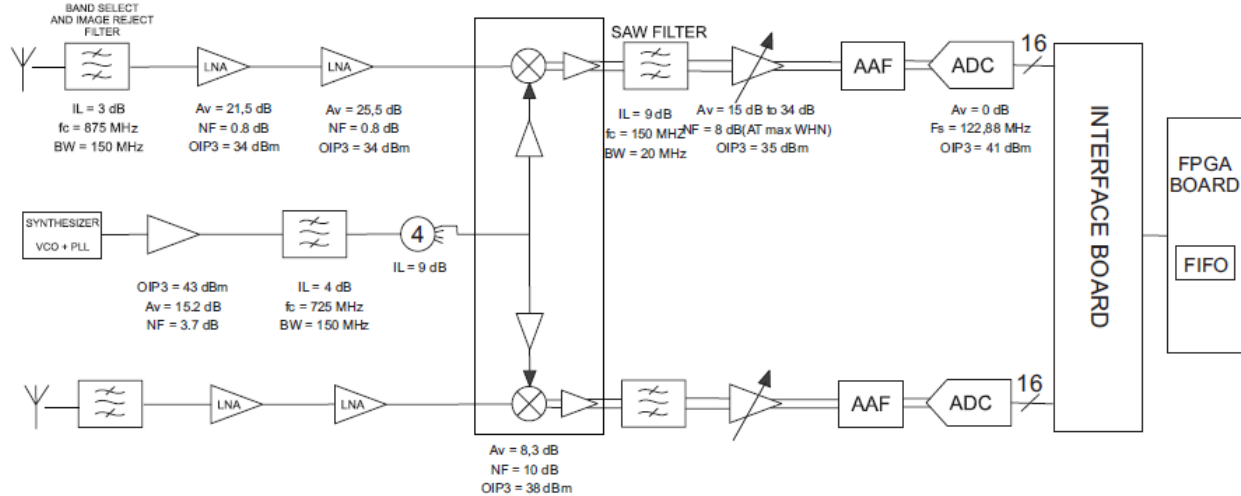


Figure 1. The block schematic of the receiver system and all stages in our signal chains

The block diagram represents only two channels, and includes characteristics of each block including third-order output intercept point, noise figure, insertion loss and/or gain. Wideband aperture coupled patch antennas were designed and manufactured as the first element in the signal chain. This type of antenna combines the resonance frequencies of a stripline, slot and a patch to create a wideband response in our band of interest. The antenna is followed by a fifth order microstrip coupled bandpass filter with a center frequency of 875 MHz, a bandwidth of 150 MHz, and insertion loss of 5 dB. The filter's purpose is to filter out-of-band interferers, and thus greatly reduce the noise. Since the signal strength at this stage is very weak, we need to amplify the signal, while keeping the noise low and SNR high. Therefore, two cascaded low-noise amplifiers (LNAs) that have noise figure of 0.8 dB were selected to boost the signal by approximately 42 dB.

Since the bandwidth of our signal at the output of that stage is 150 MHz centered at 875 MHz, the cost of any analog to digital converter (ADC) that could directly sample that signal would not meet our cost requirements. Therefore, we decrease the bandwidth of the signal as well as to decrease the carrier frequency. We used an RF mixer to downconvert the signal to an intermediate frequency of 150 MHz. We also decreased the bandwidth by connecting a synthesizer to the LO input of the mixer, and changing the frequency in increments of 10 MHz (from 950 MHz to 1100 MHz) to make the IF bandwidth 20 MHz centered at 150 MHz. This method then requires a precise filtering at the output of the mixer, and therefore used a surface-

acoustic wave (SAW) filter. Considering that the signal strength is dependent on the location of the radiator, we need some way of having a maximum dynamic range regardless of the position of the radiator. Therefore, we employed a parallel 5-bit variable gain amplifier (VGA) that has a gain from -4 dB to 24 dB. A low pass antialiasing filter (AAF) at corner frequency of 160 MHz just improves the noise floor of the ADCs by removing noise from higher Nyquist zones. We used 14-bit ADCs with the clock of 130 MHz. As the clock frequency is lower than the IF frequency, we will observe an image of the 150MHz signal at 20MHz. We utilized undersampling to extract signal information from the image that appears at 20 MHz.

Once the signal was converted into digital form, the ADC data was stored in a memory buffer for processing. We used a Virtex5 FPGA with an integrated FIFO memory buffer to store all the unprocessed data. A microblaze microcontroller was implemented on the FPGA to control the RF programmable components and to send the information to computer for further processing. On the computer, various digital beamforming algorithms including super resolution methods that are described in the main body of report are implemented to find the information about the direction of arrival of incoming radiation.

Results and conclusion

We successfully designed all eight wideband aperture coupled patch antennas. Their performance satisfies our requirements and more information about them can be found in the Results section of the report. In addition, we designed and implemented a bandpass microstrip coupled filters and we built the board that has the components for RF front end and the IF stage. All the analog parts of the project are working and they provide enough information for the digital algorithms to extract the information that we are seeking.

Digital portion of the project works; however, due to limited time, it is not integrated with analog card, and with software created for digital beamforming. The beamforming algorithms in simulations were able to achieve high-resolution signal location even when signals were separated by a few degrees.

Authorship

Branislav Jovanovic – Mr. Jovanovic served as the primary designer of aperture coupled patch antennas, microstrip coupled bandpass filters, RF front end and the synthesizer circuit to synchronize all channels in our phased array system. Mr. Jovanovic also tested all the analog components in this system, including IF stage blocks.

Tayyar Rzayev – Mr. Rzayev served as the primary designer of the interface board schematic and its PCB layout, as well as designer of the digital data capturing FIFO memory with its interface to the microblaze processor. Mr. Rzayev also produced testbenches with the description of processor's behavior to test the synthesizable VHDL.

Brennan Ashton – Mr. Ashton served as the primary designer of the digital beamforming simulations. He also implemented Xilinx project architecture, including configuration of hardware cores used in the FPGA. Mr. Ashton also performed soldering, rework, and CAM processing for boards used in the project. He was responsible to integrate hardware and software.

All team members contributed equally to this project and have developed an understanding for many problems associated with the designing of phased antenna array systems.

Table of Contents

| | |
|--|------|
| Abstract | i |
| Acknowledgements | ii |
| Executive Summary | iii |
| Brief description of phased arrays and beam-forming | iii |
| System-level solution overview | iv |
| Results and conclusion | vi |
| Authorship | vii |
| Table of Contents | viii |
| List of Figures | x |
| List of Tables | xiii |
| Chapter 2 Introduction: | 1 |
| Chapter 3 Literature review: | 2 |
| 3.1. Phased Arrays: | 2 |
| 3.2. Proposed Phased Array characteristics | 2 |
| 3.3.1. Market Research and Approximate Cost of an Analog Phased Array | 4 |
| 3.3.2. Analog Phase Shifters with Delay Lines | 4 |
| 3.3.3.. Loaded Line Phase Shifters | 5 |
| 3.3.4. Variable Reactance Reflection Phase Shifter | 6 |
| 3.4. Digital Beamforming | 6 |
| 3.5 Solution for array radiation using the k-space method (spatial Fourier transform) .. | 9 |
| 3.5.1. Method description | 9 |
| 3.5.2. Example – a 4x4 array | 11 |
| 3.5. Total Anticipated Cost of the Array | 13 |
| Chapter 4 Methodology: | 14 |
| 4.1. Antenna design | 14 |
| 4.2. Filter design | 21 |
| 4.3. Synthesizer circuit | 23 |

| | |
|---------------------------------|----|
| 4.4. IF Board..... | 23 |
| 4.5. Interface Card Design..... | 24 |
| 4.6. FPGA data capturing..... | 29 |
| 4.7. Digital Beamforming..... | 32 |
| Chapter 5 Results:..... | 37 |
| 5.1. Antenna design..... | 37 |
| 5.2. Filter design..... | 43 |
| 5.3. LNA stage | 45 |
| 5.4. Synthesizer circuit..... | 46 |
| 5.5. IF board | 47 |
| 5.6. FPGA FIFO..... | 52 |
| 5.7. Digital beamforming | 54 |
| 5.8. Value analysis | 60 |
| Chapter 6 Conclusion:..... | 61 |
| References..... | 62 |

List of Figures

| | |
|---|----|
| Figure 1. The block schematic of the receiver system and all stages in our signal chains . v | |
| Figure 2. Geometry of aperture coupled patch antennas | 3 |
| Figure 3. Typical analog phase shifters available on the market | 4 |
| Figure 4. Delay-line phase shifter | 5 |
| Figure 5. Delay-line phase shifter | 5 |
| Figure 6. Delay-line phase shifter | 6 |
| Figure 7: Adjustable Mobile Communication Cell | 7 |
| Figure 8 DOA time delay | 8 |
| Figure 9 4x4 array geometry under study. | 11 |
| Figure 10. Geometry of aperture coupled patch antenna | 15 |
| Figure 11. S11 vs. frequency during the step 2 of our design | 16 |
| Figure 12. Lambda quarter transformer | 17 |
| Figure 13. Antenna feed..... | 18 |
| Figure 14. Feed that looks like a connector with all the vias..... | 19 |
| Figure 15. Geometry of our final design to the left, and to the right there is a lambda quarter transformer and the feed | 19 |
| Figure 16. Final S11 vs. frequency which shows the bandwidth of almost 200 MHz | 20 |
| Figure 17. Smith Chart of the final design..... | 20 |
| Figure 18. Lumped element filter design..... | 21 |
| Figure 19. ADS Design of microstrip coupled filter..... | 22 |
| Figure 20. ADS Simulations for bandpass filter | 22 |
| Figure 21 VHDC connectors | 25 |
| Figure 22 Timing Diagram for the Interleaved mode | 27 |
| Figure 23 The aggressor-victim trace pair | 28 |
| Figure 24 PLB Interface..... | 31 |
| Figure 25 PLB Single Data Beat Read Timing..... | 31 |
| Figure 26 PLB Single Data Beat Write Transfer Timing | 32 |
| Figure 27 Sub Array Division..... | 36 |
| Figure 28. Dimensions of our aluminum box | 38 |
| Figure 29. 4-layer PCB layout showing top ground plane and a stripline | 38 |

| | |
|---|----|
| Figure 30. Our assembled antenna..... | 39 |
| Figure 31. S11 vs. frequency measurement when we are holding the connector | 40 |
| Figure 32. S11 of our antenna with washer between ground plane and connector | 40 |
| Figure 33. S11 vs. frequency of the antenna with 510 pF cap to the left, and SVWR to the right of 3 in worst case scenario | 41 |
| Figure 34. S21 of the antenna with 510pF cap | 41 |
| Figure 35. Narrow band S21 measurements (to the left) and wideband S21 measurements (to the right) | 42 |
| Figure 36. Patch antenna S21 showing narrow band characteristics | 42 |
| Figure 37. Measuring S21 of our aperture coupled patch antenna | 43 |
| Figure 38. Microstrip coupled filter..... | 43 |
| Figure 39. Narrowband view of the S21 performance of our filter | 44 |
| Figure 40. Wideband view of the S21 performance of our filter..... | 45 |
| Figure 41. Testing of the LNA..... | 45 |
| Figure 42. Synthesizer circuit | 46 |
| Figure 43. Output of power splitter has 0 dBm of power at 950 MHz | 47 |
| Figure 44. IF board during testing stage of our project | 48 |
| Figure 45. Output of the mixer at 150 MHz frequency | 48 |
| Figure 46. Testing the RFin-IF isolation..... | 49 |
| Figure 47. Testing LO-IF isolation | 49 |
| Figure 48. The set-up for analog system level measurements | 50 |
| Figure 49. Receiving signals in our band from the antenna before the RF input to the mixer | 50 |
| Figure 50. Wideband view of the RF input..... | 51 |
| Figure 51. IF output of the mixer, where we can see the main signal at 150 MHz | 51 |
| Figure 52 Post Place and Route simulation showing the write transaction | 52 |
| Figure 53 Post Place and Route simulation showing the flag read transaction | 53 |
| Figure 54 Post Place and Route simulation showing the data read transaction..... | 53 |
| Figure 55 Post Place and Route simulation showing the serialized data from the ADC.. | 54 |
| Figure 56 Standard Beamformer..... | 54 |
| Figure 57Capon's Beamformer..... | 55 |

| | |
|---|----|
| Figure 58 Linear prediction beamformer | 55 |
| Figure 59 MUSIC beamformer | 56 |
| Figure 60 MUSIC with minimum norm | 57 |
| Figure 61 MUSIC with minimum norm and spacial smoothing..... | 57 |
| Figure 61. ATC Model Order with 5 passes | 58 |
| Figure 62. ATC Determination Histogram for model order | 59 |
| Figure 64. Impedance of the stripline during step 1 | 64 |
| Figure 65. S11 vs. frequency during the step 2..... | 64 |
| Figure 66. Impedance of the wave port after making a lambda quarter transformer..... | 65 |
| Figure 67. Lambda quarter transformer inside the aluminum box | 65 |
| Figure 68. S11 vs. frequency during step 3 | 66 |
| Figure 69. Realized gain of the final design at 0 degrees and 90 degrees | 66 |
| Figure 70. Radiation pattern of our antenna, showing that there are no back lobes. | 67 |
| Figure 71. 3D caption of realized gain of our antenna | 67 |

List of Tables

| | |
|---|----|
| Table 1 Electric field distributions in different observation planes. Array field at $\lambda/8$ is simulated using the second-order Yee FDTD scheme. Array fields at all other distances are found using the <i>direct propagator</i> in the k -space described in the first section. | 12 |
| Table 2 A. Cost Analysis for Analog Components..... | 13 |
| Table 3 B. Cost Analysis for Digital Components | 14 |
| Table 4 Signal Schedule..... | 26 |
| Table 5. Parameters in Antenna design..... | 68 |

Chapter 2 Introduction:

Phased arrays are currently used in a wide variety of applications. They are used both on the receiver and the transmitter end. As a transmitter, a phased array creatively adds in certain phase delays across its channels to reinforce the signal strength at certain location in space and to destructively interfere at others. This allows a transmitting phased array to send its signal only in a certain pattern, known as the radiation pattern. Similarly, a receiving phased array can alter the phase delays of each of its channels, so that when all of the received signals combine, signals received from a particular direction in space will be reinforced, while signals from other directions will get annihilated. This is useful when in presence of a large number of sources of information all transmitting at the same time with the same frequency, i.e. some kind of RFID tags. Another useful application is geolocation of transmitting nodes. For example, people in critical situations can be found just by using their cell phone signal that will “tell” people where it is coming from if a proper phased array is used. The process by which the phased array steers its beam is known as beamforming. Beamforming is equally applicable to both the transmitting and the receiving phased arrays. Beamforming can be done in a number of different ways. The majority of solutions are subdivided into analog solutions and digital solutions. The goal of our project was to prove the concept of a phased array with the digital beamforming solution. The advantage of this solution is the extreme flexibility, because both the beamforming algorithm and the further decision making can be altered in the digital domain. Another advantage is that just by capturing the raw surrounding data, signals from every direction can be found just by applying the corresponding filter with certain weights on the phase shifts. Thus, signals from all directions can be obtained from the same raw collected data. Another advantage is that after discovering the direction of arrival of a wanted signal, it can be also decoded offline, which was not possible with analog phase shifters.

With this project, we propose an architecture capable of implementing the digital beamforming as well as necessary RF and analog signal processing prior to that. Our proposed design will be able to capture signals transmitted in the 800-950MHz GSM band, and do all the necessary processing to determine the respective direction of arrival.

Chapter 3 Literature review:

3.1. Phased Arrays:

The idea of a phased array is the combination of the received signals from individual radiators with proper phase shifts. Such a combination is maximized when the RF source is at the scan angle corresponding to the chosen phase shift. An angular scan of the scene, including locations of RFID tags, is obtained by sweeping over all possible phase shifts.

3.2. Proposed Phased Array characteristics

A phased array that we aimed for should have the following characteristics:

1. Rx mode of operation
2. 16 dB gain of the main beam at zenith scan
3. Linear polarization
4. 5 degrees angular resolution
5. ± 50 degrees scanning angle from broadside
6. 8 or less individual radiators
7. Center frequency of 875 MHz
8. Bandwidth of about 150 MHz
9. The overall maximum size of 1.5 m
10. Light weight design

Those characteristics are subject to change and may be modified. For the phased array we researched various antennas that we could build and our requirements for gain and bandwidth pointed us at aperture coupled patch antennas, which combine the geometry of slot antenna and patch antenna, and the basic geometry is shown in the next picture:

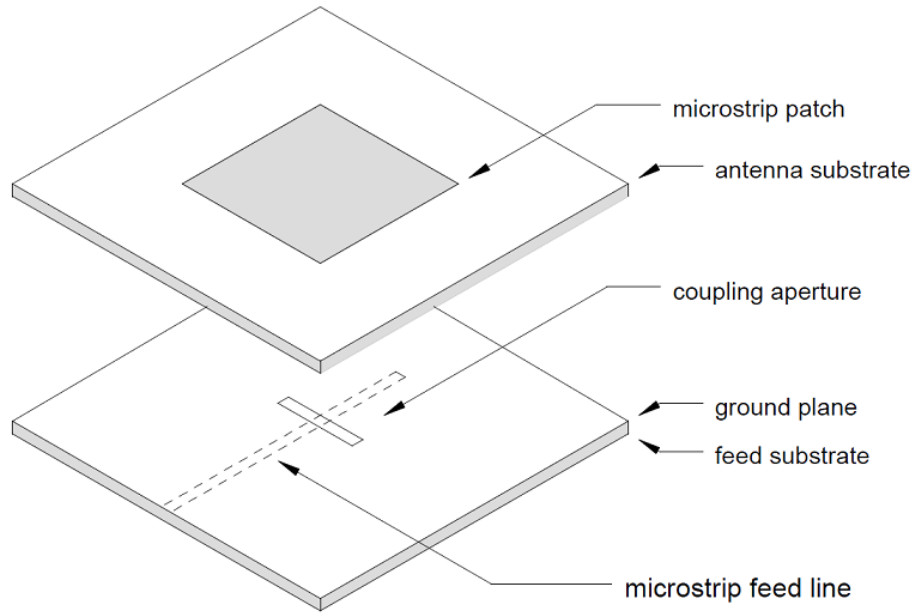


Figure 2. Geometry of aperture coupled patch antennas

The feed touches the stripline, and when stripline is underneath the slot, it couples its energy through the slot and once it reaches the patch it excites its resonance. Therefore, with this geometry we are able to combine resonances of the slot, stripline and patch, in order to create a wideband phased array. The relatively high gain of patch antenna is desired in our application, and necessary to meet our design requirements. The width of the stripline affects the match in Smith chart by moving the contours left or right. On the other hand, the length, changes the contours in Smith Chart by moving it up and down. Patch antenna size should be slightly lower than half lambda (wavelength), and the slot length should also be between lambda half and lambda quarter.

3.3. Phase shifters

Thus, phase shifters or delay lines, either analog or digital, represent the centerpiece of a phased array. It is shown in Appendix A that the cost of our phased array with low loss analog phase shifters is estimated as \$45,000. Such high cost is the major challenge with phased arrays today. As another example, one square meter of a phased array delivered by Raytheon at X band currently costs about one millions dollars.

3.3.1. Market Research and Approximate Cost of an Analog Phased Array

After we completed a thorough market research, we briefly summarize here the main characteristics of the analog phased shifters. Typical analog phase shifters that we found on the market are shown in Figure 1.

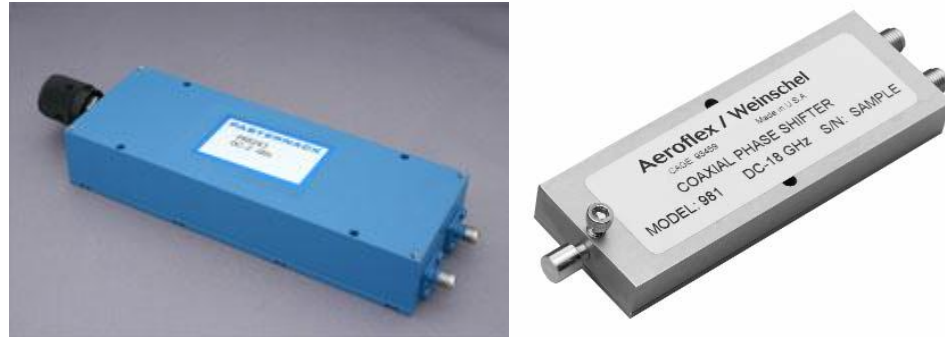


Figure 3. Typical analog phase shifters available on the market

We were looking for phase shifters that operate a frequency of 900 MHz. Based on data sheets from several products, we attained a good estimate of typical insertion losses, VSWRs, incremental phase shifts and cost of analog phase shifters. Using this data we determined that the insertion loss for 900 MHz is typically 0.5 ± 0.3 dB. Voltage standing wave ratios were 1.5 ± 0.2 . Incremental phase shifts were generally 26° .

However, the average price, which is probably the crucial parameter, is as high as \$630 per phase shifter. Since our antenna array will have 64 elements, and each of them will need a phase shifter, that means that the total cost of analog phase shifters would be around \$ 40,000. This cost does not include the considerable cost of components to dynamically control the phase, the cost of LNAs, filters, PCB, mixers, etc.

3.3.2. Analog Phase Shifters with Delay Lines

In analog phase shifters there is a continuous change in phase that can be controlled in several different ways. One of the ways that it can be controlled is by delay lines. In figure 1, we have an illustrated version of a delay-line phase shifter.

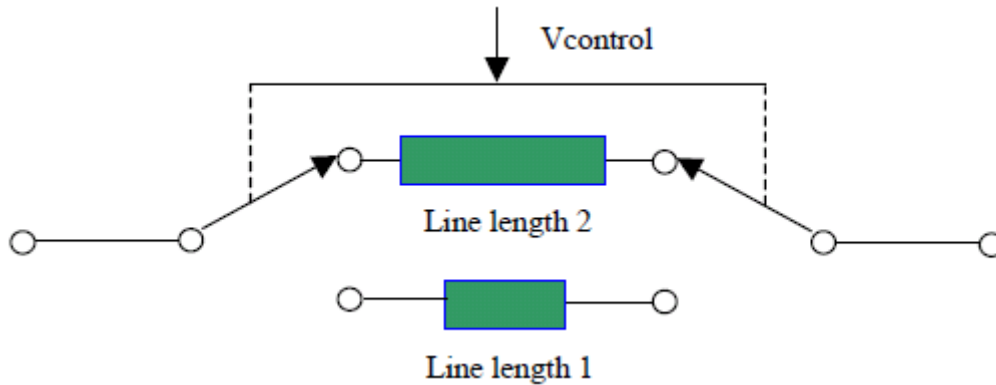


Figure 4. Delay-line phase shifter

If there is a difference in electrical length between two transmission lines, there will be also a time delay between them and therefore a phase shift. At very high frequencies it is difficult to create switches which would control the phase. Most popular choices for switches are FETs, PIN diodes and MEMS (Micro-electrical mechanical systems) switches. The choice of switches is based on the frequency. Delay line phase shifters can be also used for SAW technologies. The main idea is to instead of transmission lines we use SAW devices, and then each line would have different separation between IDTs.

3.3.3.. Loaded Line Phase Shifters

Loaded line phase shifters have a capability to create a phase shift of less than 45 degrees. In Figure X, we showed a version of a loaded line phase shifter.

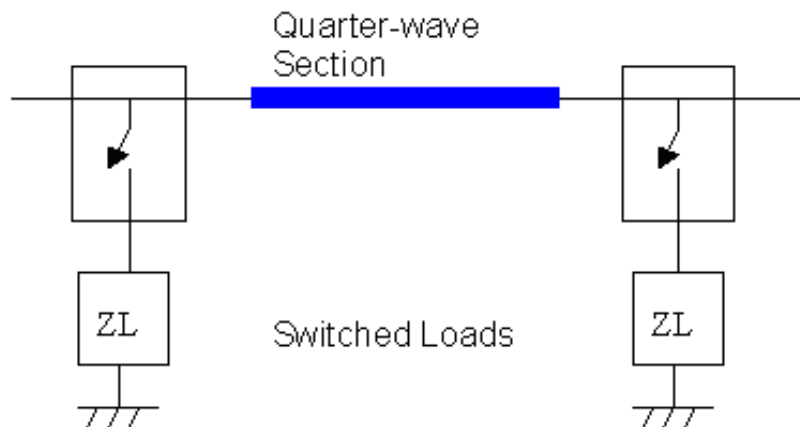


Figure 5. Delay-line phase shifter

Loads in these phase shifters are set in such a way that the difference between them creates a phase shift when they are switched into the circuit, while the amplitude of the signal remains the

same. Since it is important to minimize the losses, loads should have very high reflection coefficients; therefore they should utilize purely reactive elements, capacitors or inductors. Section between two loads is just a quarter-wave transformer.

3.3.4. Variable Reactance Reflection Phase Shifter

Variable Reactance Reflection Phase Shifter is a very common phase shifter technique, where the circuit shown in Figure Z, uses a 90-degree hybrid and variable reactance (varactors).

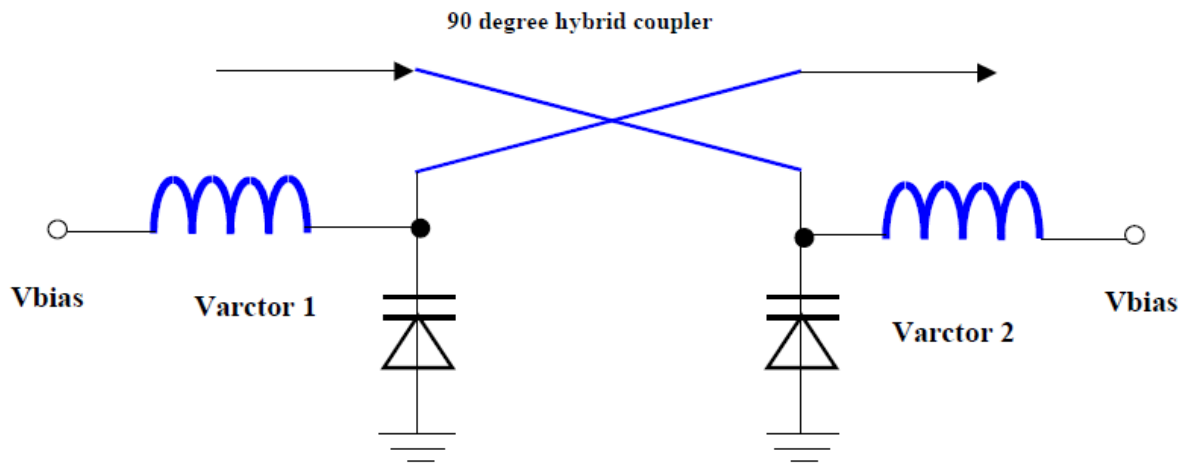


Figure 6. Delay-line phase shifter

A variable reactance is in effect a variable electrical length. Changing electrical length with a variable reactance will cause a phase shift. This was the basic principle of a variable reactance reflection phase shifters.

3.4. Digital Beamforming

Phased array antennas have become critical component of communication technology and are largely responsible for the level of service that can be provided to mobile phone users. They have allowed a substantial increase in the number of nodes that can communicate to a single base station by spatially isolating nodes. A substantial number of methods have been developed for utilizing phased array technology for improving quality in communications from everything from ground verticals to mobile telephones.[1] The advantage of beam steering is not solely limited to increasing the number of nodes that can communicate in a channel, but also includes the ability to dramatically increase the gain of an antenna by focusing the gain of all of the antenna elements in a single direction. This provides performance substantially higher than that

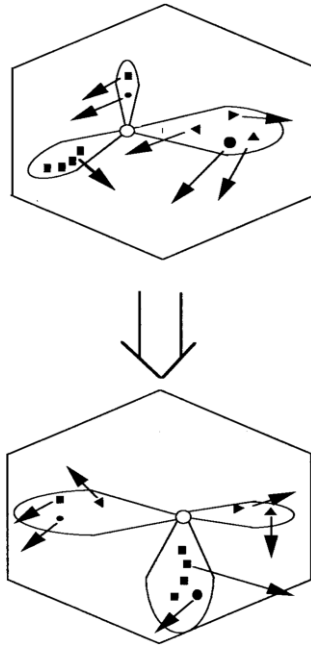


Figure 7: Adjustable Mobile Communication Cell

of a omnidirectional antenna.[3] The ideal phased array antenna is able to produce both high gain in the direction of interest while providing nulls in other directions.

The base premises for creating a phased array antenna is to create a set of phase shifts and gains on each of the array elements through the use of analog elements including but not limited to delay lines. These methods are both expensive and limiting as in many cases they are expensive and only able to identify a single element at once. A set of digital methods have been developed to take the raw elements and impose a “steering vector” to transmit or receive data from spatially separated nodes. In cellular applications the areas where the beam is directed are know as cells. By implementing digital beamforming these cells can adjusted depending on demand to balance the number of nodes in a given channel. [1]

Due to the substantial benefits of digital beamforming, substantial work has taken place in this area to optimize array response. One small component of this is improving the ability to location of signals, specifically direction of arrival (DOA) determination. Many beamforming methods are narrow band and require band selective filters to be used to keep all of the signal of interest near the same center frequency.[2] It should be noted that the majority of array processing

algorithms are frequency independent as long as the sample size is both large enough and that the SNR is high enough.[3]

The core idea behind standard methods for DOA determination depends on determining the steering vector for pointing the array beam by only phase shift. Consider the following figure:

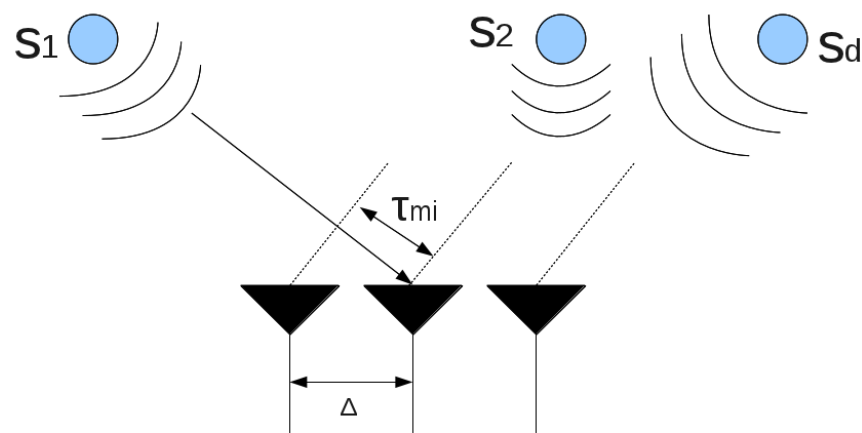


Figure 8 DOA time delay

By knowing both the angle of incidence of the signal the center frequency and the element spacing of the array the delay of the signal can be determined for each element so that with the proper phase shift the same signal is the same on each element, and the corresponding sum of signal power on the elements is maximized. The conventional method works by sliding the phase shift to maximize gain and locate the signal. The apparent limitation of this method is when in a multi-signal environment and two signals may impinge from similar directions, the appropriate angles to cause destructive interference. The standard method is considered only appropriate when signals are sufficiently separated, normally 20 degrees or more. This method is also one of the computationally simple methods.[3]

By improving this method, introducing nulls in the directions of no interest, the interference caused by spatially close signals can be somewhat minimized. This allows for approximately doubling resolution, with down to 10 degrees of separation to be identified. This algorithm includes matrix inversion, which substantially increases the amount of computational operation necessary, increasing the cost of hardware to perform analysis in real-time applications. An additional method known as Linear Prediction can be used to slightly improve

the performance, to around 7 degrees. This method however requires that a unity element vector be associated with the array, and performance greatly depends on this vector which has little criterion for optimal selection.[3]

Real performance gains are available especially in environments with a high number of impinging signals through the use of super-resolution and subspace algorithms, such as Multiple Signal Classification (MUSIC) and Estimation of Signal Parameters via Rotational Invariance Techniques. MUSIC focuses on the identification of eigenvectors in an element signal covariance matrix that represent actual signals rather than environment noise. This can be highly computational intensive. ESPRIT, has several advantages, it has much lower requirements for array calibration of phase and gain across elements and it uses shift invariance of symmetric arrays to substantially reduce the storage and computational requirements of the DOA determination. While the number of computation is substantially reduced, computations that are performed can be substantially more complex than other methods.[3]

3.5 Solution for array radiation using the k-space method (spatial Fourier transform)

3.5.1. Method description

In this section, we describe the standard direct and inverse propagator for horizontal observation planes based on Fourier transform in the k -space. This method solves Maxwell's equations analytically, in the spectral domain. The k -space method is best suited for a homogeneous medium, but may be also used in a multilayered medium. Note that other propagator models in the near field exist.

Only tangential electric field components E_x , E_y are included into considerations. The spatial Fourier transform over a finite plane aperture ($a \times b$) reads

$$\begin{aligned} f_x &= \int_{-b/2-a/2}^{+b/2+a/2} \int_{-b/2-a/2}^{+b/2+a/2} E_x(x', y', z' = 0) \exp(jk_x x' + jk_y y') dx' dy' \\ f_y &= \int_{-b/2-a/2}^{+b/2+a/2} \int_{-b/2-a/2}^{+b/2+a/2} E_y(x', y', z' = 0) \exp(jk_x x' + jk_y y') dx' dy' \end{aligned} \quad (1)$$

Direct and inverse propagators (in the z -direction) have the form

$$\begin{aligned}
E_x(x, y, z) &= \frac{1}{4\pi^2} \int_{k_x^2+k_y^2 \leq k^2} f_x(k_x, k_y) \exp\left(-jk_x x - jk_y y - j\sqrt{k^2 - k_x^2 - k_y^2} z\right) dk_x dk_y + \\
&\quad \frac{1}{4\pi^2} \int_{k_x^2+k_y^2 > k^2} f_x(k_x, k_y) \exp\left(-jk_x x - jk_y y - \sqrt{k_x^2 + k_y^2 - k^2} z\right) dk_x dk_y \\
E_y(x, y, z) &= \frac{1}{4\pi^2} \int_{k_x^2+k_y^2 \leq k^2} f_y(k_x, k_y) \exp\left(-jk_x x - jk_y y - j\sqrt{k^2 - k_x^2 - k_y^2} z\right) dk_x dk_y + \\
&\quad \frac{1}{4\pi^2} \int_{k_x^2+k_y^2 > k^2} f_y(k_x, k_y) \exp\left(-jk_x x - jk_y y - \sqrt{k_x^2 + k_y^2 - k^2} z\right) dk_x dk_y
\end{aligned} \tag{2}$$

Positive values of z correspond to *forward* propagation; negative z – to *back*-propagation. Dimensionless variables may further be introduced to quantify the effect of evanescent modes corresponding to $k_x^2 + k_y^2 > k^2$

$$\begin{aligned}
X &= \frac{x}{\lambda}, Y = \frac{y}{\lambda}, Z = \frac{z}{\lambda}, \quad A = \frac{a}{\lambda}, B = \frac{b}{\lambda} \\
K_x &= \frac{k_x}{k}, K_y = \frac{k_y}{k}, k = \frac{2\pi}{\lambda}
\end{aligned}$$

In the dimensionless form, the propagator reads

$$\begin{aligned}
f_{x,y} &= \lambda^2 \int_{-B/2-A/2}^{+B/2+A/2} \int E_{x,y}(x', y', z' = 0) \exp\left(2\pi jK_x X' + 2\pi jK_y Y'\right) dX' dY' \\
E_{x,y}(X, Y, Z) &= \\
&\quad \frac{1}{\lambda^2} \int_{K_x^2+K_y^2 \leq 1} f_{x,y}(k_x, k_y) \exp\left(-2\pi jK_x X - 2\pi jK_y Y - 2\pi j\sqrt{1 - K_x^2 - K_y^2} Z\right) dK_x dK_y + \\
&\quad \frac{1}{\lambda^2} \int_{K_x^2+K_y^2 > 1} f_{x,y}(k_x, k_y) \exp\left(-2\pi jK_x X - 2\pi jK_y Y - 2\pi \sqrt{K_x^2 + K_y^2 - 1} Z\right) dK_x dK_y
\end{aligned} \tag{3}$$

Except for truncating the observation plane, direct and inverse Fourier propagators (constituting the angular spectrum method) satisfy Maxwell's equation precisely. The direct propagator is equivalent to Rayleigh (Rayleigh-Sommerfeld) diffraction integral – see **Error! eference source not found.** ,

$$U(x, y, z) = -\frac{1}{2\pi} \int_{-\infty-\infty}^{+\infty+\infty} \int U_0(x_0, y_0) \frac{\partial}{\partial z} \left(\frac{\exp(-jk|\vec{r} - \vec{r}_0|)}{|\vec{r} - \vec{r}_0|} \right) dx_0 dy_0 \tag{4a}$$

However, the inverse propagator is still the precise result whereas the commonly used approximation of the inverse Rayleigh-Sommerfeld integral in the form of the conjugate Green's function,

$$U(x, y, z) = -\frac{1}{2\pi} \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} U_0(x_0, y_0) \frac{\partial}{\partial z} \left(\frac{\exp(+jk|\vec{r} - \vec{r}_0|)}{|\vec{r} - \vec{r}_0|} \right) dx_0 dy_0 \quad (4b)$$

ignores evanescent modes.

3.5.2. Example – a 4x4 array

A 4x4 planar array of linearly-polarized square patch antennas spaced at $\lambda/2$ or less is chosen as shown in Fig. 1. The ground plane (or the reflecting plane) extends to approximately twice the array size. The large reflector size is important for accurate restoration results.

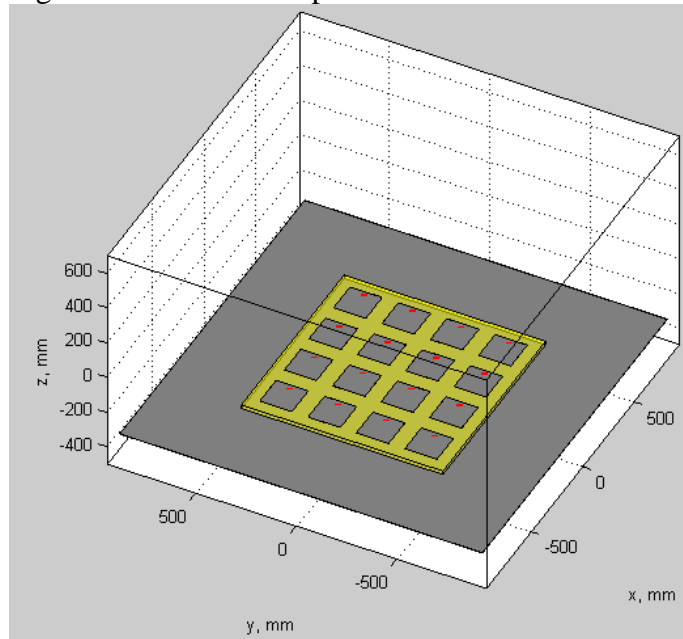


Figure 9 4x4 array geometry under study.

Six observation planes used for sampling transversal electric (and magnetic) fields are shown in Table 1. They are spaced at distances

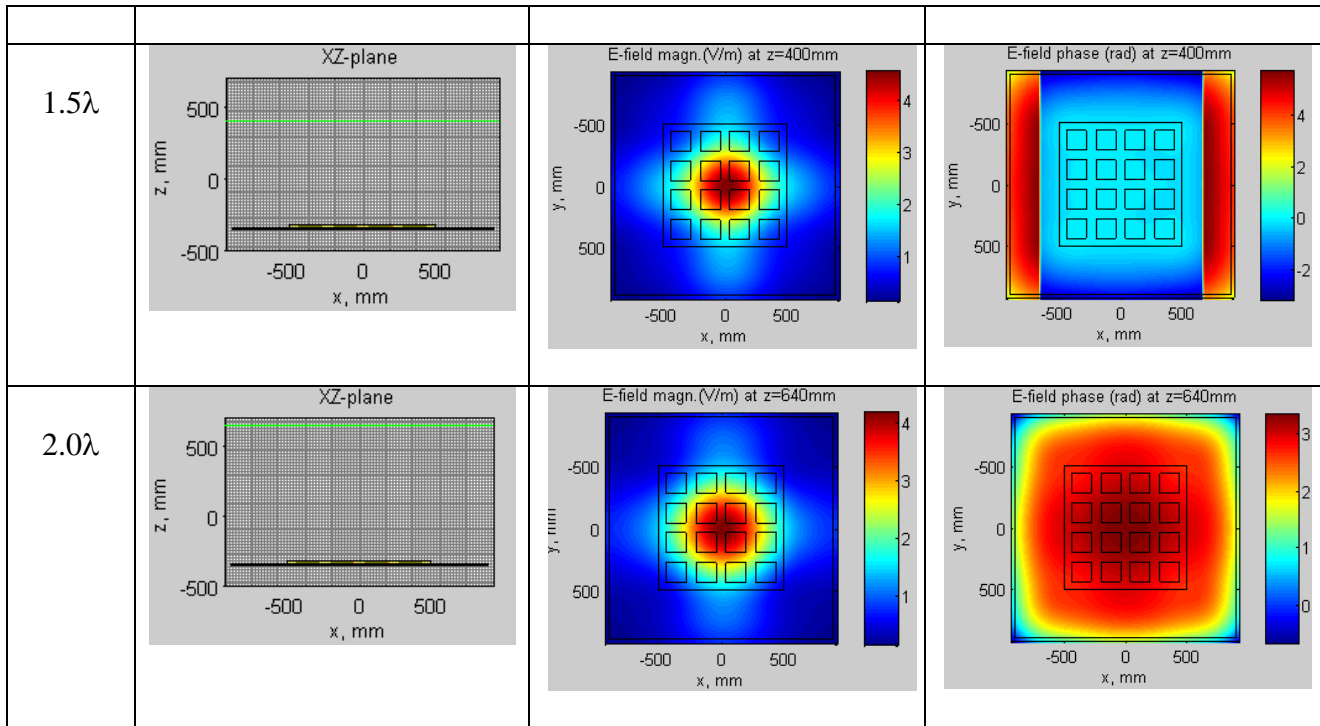
$$\frac{\lambda}{8}, \frac{\lambda}{4}, \frac{\lambda}{2}, \lambda, \frac{3\lambda}{2}, 2\lambda \quad (5)$$

from the physical top of the antenna array. The array field at $\lambda/8$ is simulated using the second-order Yee FDTD scheme and standard MATLAB[®] environment. All radiators are terminated into an ideal sinusoidal generator voltage source in series with a 50Ω resistance. All elements have source amplitudes of 1V and equal phases.

The array fields at all other distances are found using the *direct propagator* in the *k*-space described in the first section. Table 1 shows field distributions for the co-polar electric field at different distances from the array i.e. in the different observation planes.

Table 1 Electric field distributions in different observation planes. Array field at $\lambda/8$ is simulated using the second-order Yee FDTD scheme. Array fields at all other distances are found using the *direct propagator* in the *k*-space described in the first section.

| Plane height | Plane location | Co-polar electric field - magnitude | Co-polar electric field-phase |
|--------------|-----------------|--|--|
| $\lambda/8$ | <p>XZ-plane</p> | <p>E-field magn. (V/m) at z=-260mm</p> | <p>E-field phase (rad) at z=-260mm</p> |
| $\lambda/4$ | <p>XZ-plane</p> | <p>E-field magn. (V/m) at z=-200mm</p> | <p>E-field phase (rad) at z=-200mm</p> |
| $\lambda/2$ | <p>XZ-plane</p> | <p>E-field magn. (V/m) at z=-80mm</p> | <p>E-field phase (rad) at z=-80mm</p> |
| λ | <p>XZ-plane</p> | <p>E-field magn. (V/m) at z=160mm</p> | <p>E-field phase (rad) at z=160mm</p> |



One can see that the fine structure of the fields close to individual patches is lost, as long as the distance from the array surface exceeds $\lambda / 4$.

3.5. Total Anticipated Cost of the Array

An array which is implementing the proposed digital beamforming at IF will include components listed in Table 1. This table separated into two parts, one for analog components and another for digital components. Table 1 also lists cost for all components.

Table 2 A. Cost Analysis for Analog Components

| Analog Components | Maximum cost (\$) | Quantity | Total Price |
|--|-------------------|----------|----------------|
| LNA | \$5 | 16 | \$80 |
| Mixers | \$15 | 16 | \$240 |
| Synthesizer | \$15 | 1 | \$15 |
| SAW filter | \$30 | 8 | \$240 |
| Band Pass Filter | \$100 | 8 | \$800 |
| Individual Radiators, Cables, Connectors, Adaptors | \$3,600 | 1 | \$3,600 |
| Total cost | | | \$4,975 |

Table 3 B. Cost Analysis for Digital Components

| Digital Component | Quantity | Unit Cost | Total Cost |
|--|-----------------|------------------|-------------------|
| AD9283 8-bit ADC50MSP | 64 | \$5 | \$320 |
| Xilinx Virtex-6 ML605 Development Board | 2 | \$2000 | \$4000 |
| Total Component Costs | | | \$4320 |

So the total cost of this system should be around \$10,000, and that is what we were aiming for.

Chapter 4 Methodology:

4.1. Antenna design

As explained in the literature review section, we will use Ansoft HFSS simulation tool to design the antenna that we will use for our phased array. Ansoft HFSS is a finite element method (FEM) simulator for various electromagnetic problems. The first step in designing an antenna in HFSS is to draw a specific form or shape of our antenna and to parameterize all the parameters, so that we can change them for optimization. In addition, we have to draw a specific radiation box that will be outside of our antenna structure and that sets the boundary values that allow Ansoft to solve the wave equation derived from differential form of Maxwell's equations:

$$\nabla \times E = - \frac{\partial B}{\partial t} \quad (6)$$

$$\nabla \times H = J + \frac{\partial D}{\partial t} \quad (7)$$

$$\nabla \cdot D = \rho \quad (8)$$

$$\nabla \cdot B = 0 \quad (9)$$

Transforming these equations into integral form by applying Divergence theorems and Green's theorems, we can arrive at equations that are easier to apply in hand-analysis of standard

electromagnetic problems. However, for computational purposes, differential form of Maxwell's equations is dominant.

Considering that all antennas have some sort of feed, we need to model it as either a wave port or a lumped port that touches the signal path. Lumped port is usually by default matched to 50 Ohms impedance and can be placed anywhere on the feed line, while the wave port is placed at the edge of the radiation box. Wave port's impedance is equivalent to the impedance of the line that it is touching, and therefore it is not normalized with respect to desired characteristic impedance of the line.

We separated our design in 6 different steps. In the first step, we just drew the basic geometry of our aperture coupled patch antenna with wave port, and that can be seen below:

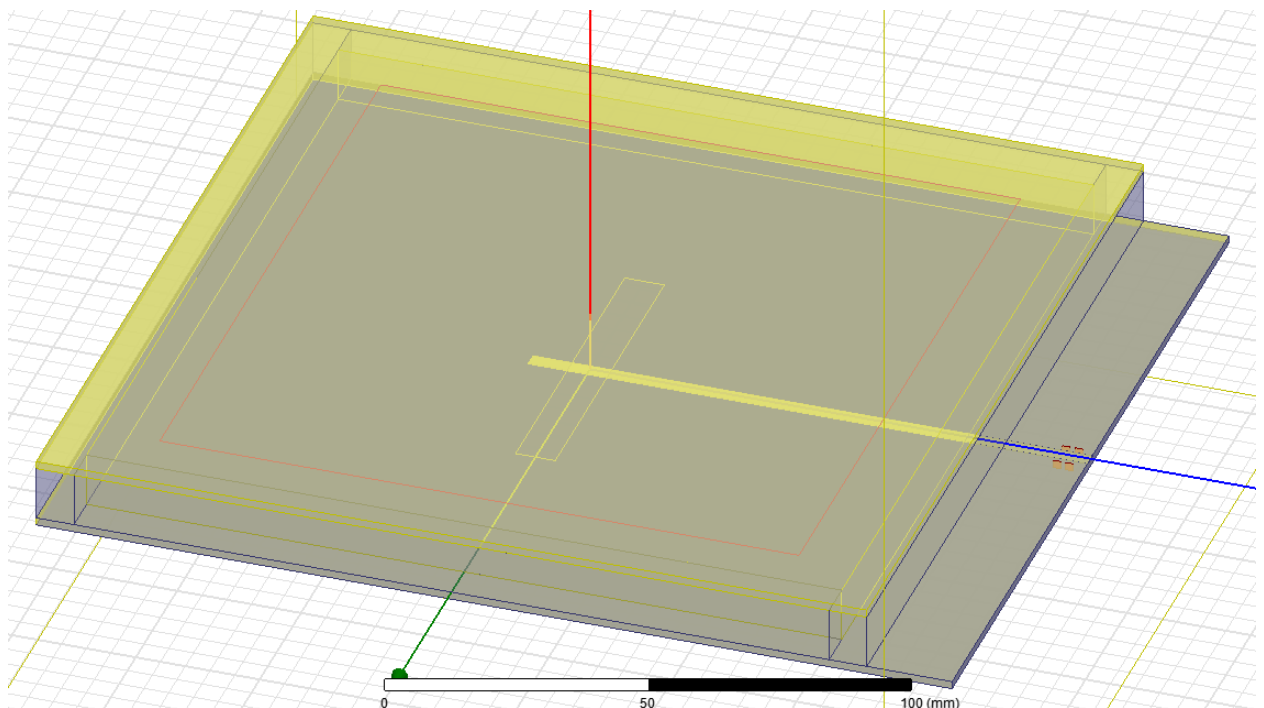


Figure 10. Geometry of aperture coupled patch antenna

Considering that the separation between two antennas should be $\lambda/2$, we had a set constraint that the base of the box should be around 6.6 inches by 6.6 inches. Considering that the cost of the phased array system is crucial, we could only use cheap dielectrics, like FR4, that has unstable relative permittivity that at 1 GHz ranges from 4.2 to 4.5. Additionally, for metal surfaces that we modeled in Ansoft as perfect conductors, we used only aluminum and copper.

Also, the stripline was 10mil below the ground plane and considering that standard 4-layer boards provide such an arrangement, we could not really change that parameter. Parameters that we could vary are: slot width, slot length, stripline width and length, patch size and aluminum box height. We initially set the values of these parameters based on the expected geometries that should bring the resonance in our band of interest. Considering that this method did not generate great results, we chose to fix all parameters while varying only one of them. Clearly, to meet such an ambitious objective like 150 MHz of bandwidth, we had to optimize a significant number of parameters, and therefore, we spent at least two months running various tests to find the solution. In our first step, we generated the following graph, which is a good basis to go to step 2 of the design.

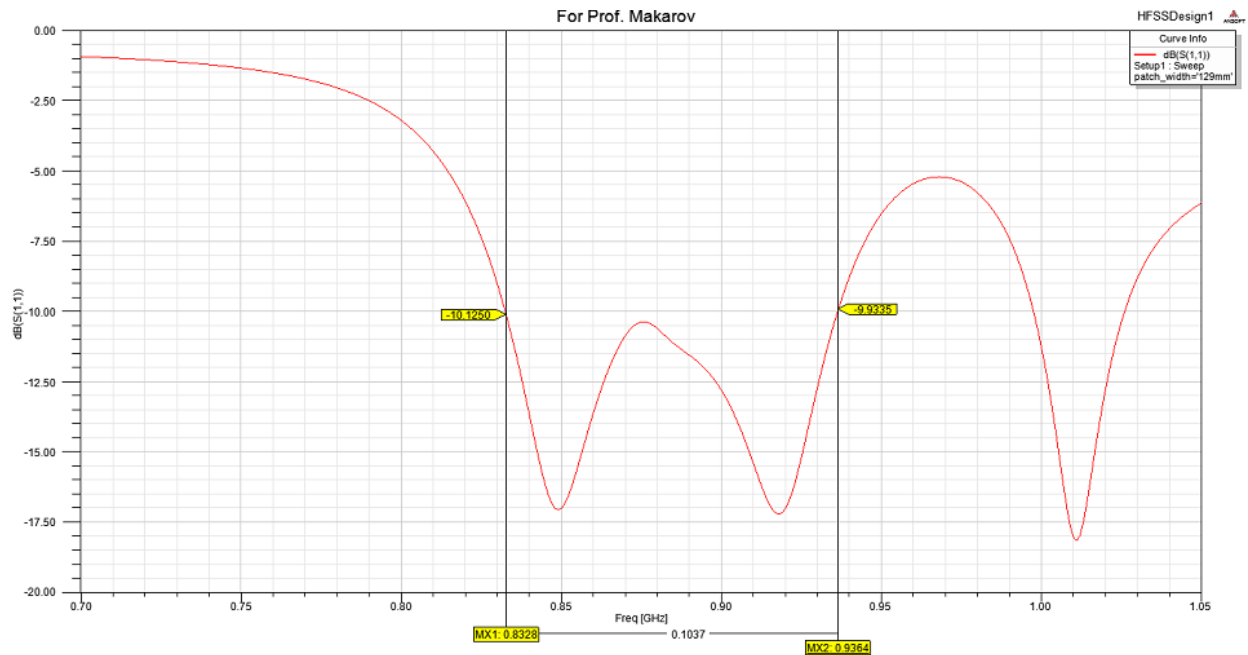


Figure 11. S11 vs. frequency during the step 2 of our design

Clearly, the bandwidth is not 150 MHz, but it is pretty close to our desired bandwidth. Considering that the impedance of the stripline was 11.38 Ohms, as seen in the appendix A, we had to create a lambda quarter transformer to bring the wave port to impedance of 50 Ohms, which corresponds to impedance of standard RF connectors, and that is shown in the following figure:

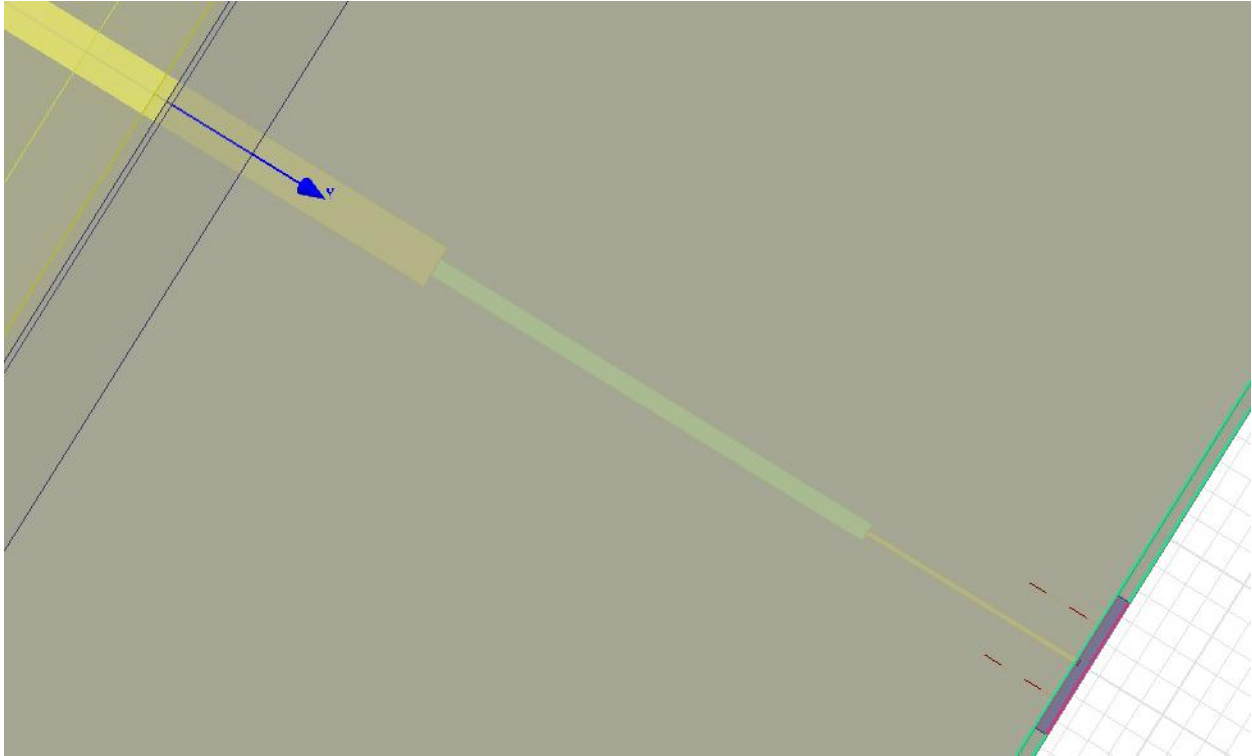


Figure 12. Lambda quarter transformer

To find the characteristic impedance of the line between 50 Ohm connector and stripline of impedance of 11.4 Ohms, we used the formula:

$$Z_0 = \sqrt{Z_{load}Z_{in}} \quad (10)$$

This is the formula that was derived from the expression for input impedance and setting the condition that the length of transmission line is $\lambda/4$. In the appendix B and C, we can see how the S11 over frequency varied and how the new characteristic impedance of the port is estimated to be 49.9 Ohms. The only thing that changes impedance of the line is its width, and considering that we have a stripline, with very strange geometry that is just slightly below ground plane, it turns out to be 50mil wide and the 50 Ohm line at the end is only 15mil wide.

Considering that we placed the lambda quarter transformer outside of the aluminum box, we increased the size of the board by several inches, and therefore, we increased the cost of manufacturing the PCB board. In step 3, we brought the transformer inside the box, in order to reduce the size of the extra piece of PCB board that has the connector. That can be seen in appendix D.

The fourth step is almost the same as third step, except that we put the 50 Ohm lumped port, shown in the next figure:

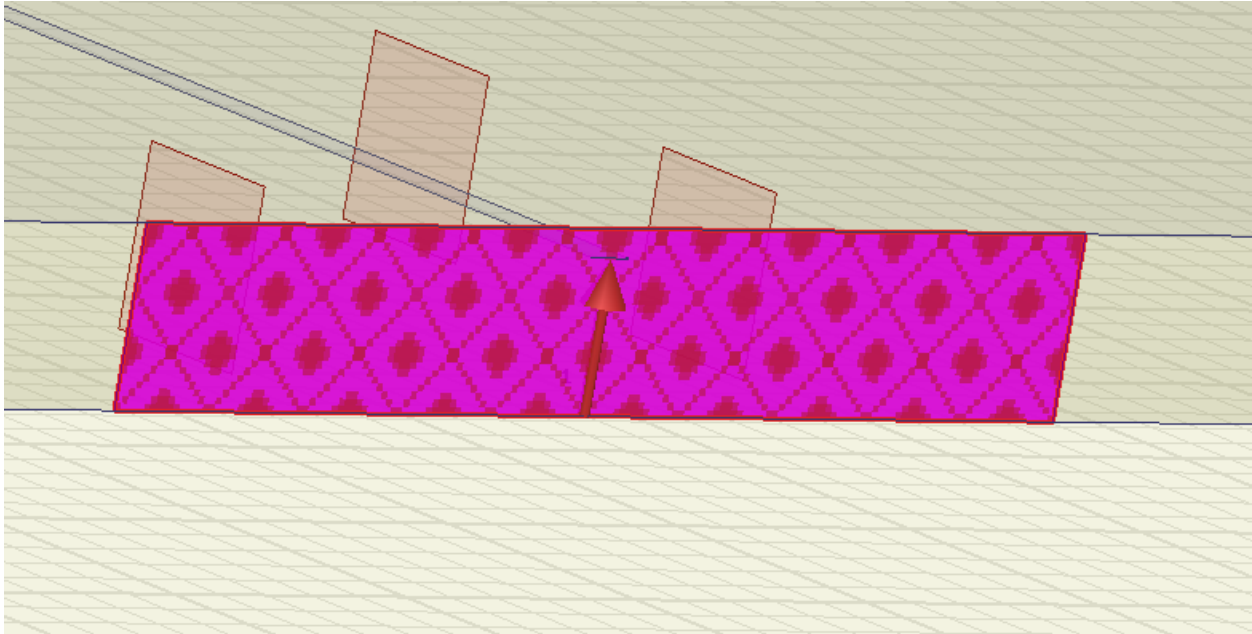


Figure 13. Antenna feed

The arrow represents the direction of electric field, from ground plane to the stripline. At this point we are generating great response that is shown in Appendix E, which shows S11 over frequency, where the bandwidth is almost 200 MHz. The fifth step included a very complex step of adding all plated vias to connect ground planes close to stripline and the connector. The connector was modeled more realistically, where the pin had diameter of 50 mil, which was included in the model.

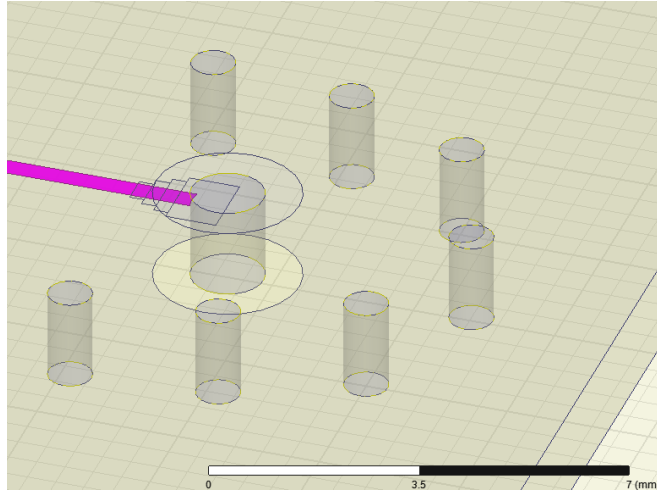


Figure 14. Feed that looks like a connector with all the vias

With all these vias, the performance changed slightly from the previous figure. Finally, we even modeled the coaxial cable that will be long and we put a port at the top of radiation box in order to make a model as close as possible to the real world scenario:

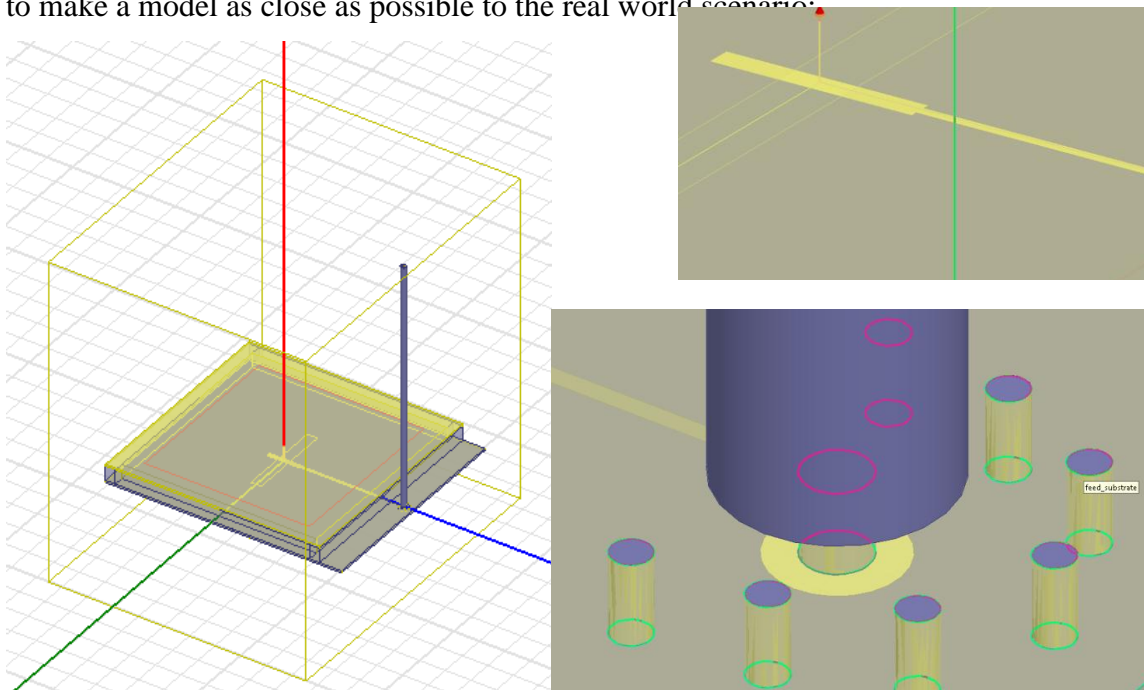


Figure 15. Geometry of our final design to the left, and to the right there is a lambda quarter transformer and the feed

Clearly, in this figure, we can see the gray line, which represents the coaxial cable that we will use once we want to start making the product. The final S11 vs. frequency response is shown below and it shows that we are successful in achieving our goal of making a wideband antenna.

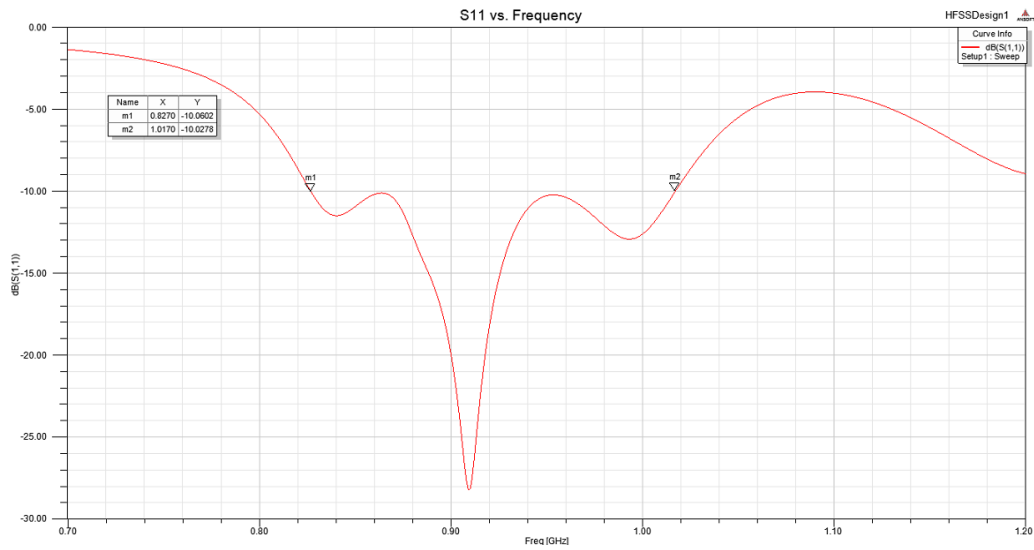


Figure 16. Final S11 vs. frequency which shows the bandwidth of almost 200 MHz

The drawback of our design is that at 800 MHz, the S11 is around -6 dB.

Finally, the Smith Chart was our main guide throughout our design, and the final version is included in the next figure:

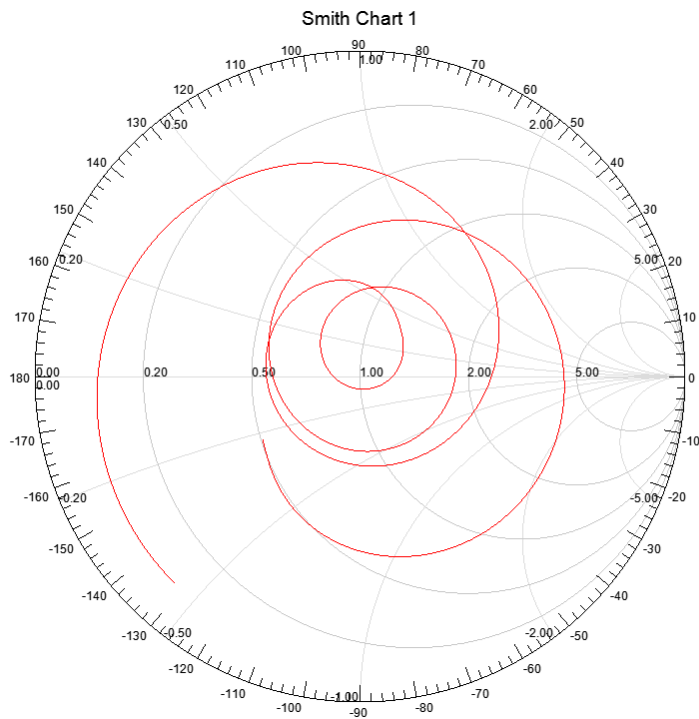


Figure 17. Smith Chart of the final design

Clearly, from the Smith Chart we can see that we have a decent match for most of our band of interest.

In addition, we included the figures in appendices that show the realized gain of this antenna that is 4.2 dB (with all the losses), radiation pattern that shows that the scanning angle is from -45 degrees to 45 degrees and a realized gain in 3D.

Finally, we included all our parameters and their values in the appendix I.

4.2. Filter design

In order to build a bandpass filter with 150 MHz of bandwidth at center frequency of 875 MHz, we considered two approaches. One of them was to build a lumped-element bandpass filter and another one was to build the microstrip coupled filters. We designed the lumped-element filter in ADS and that is shown below:

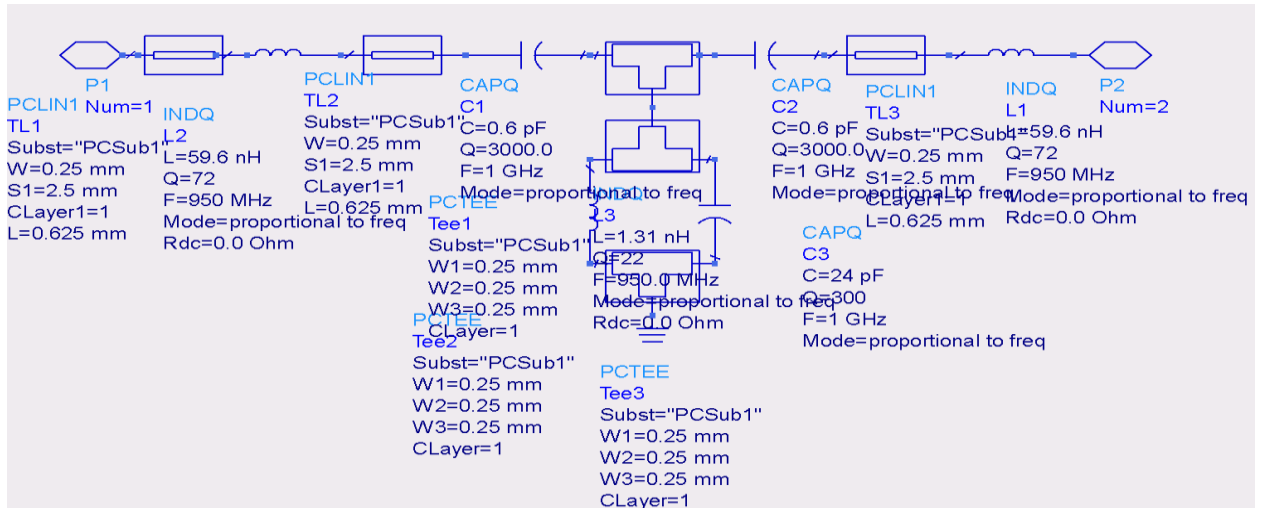


Figure 18. Lumped element filter design

The problem with this approach is that we could not find reliable parts online that had high enough Q and consistent value at our band of interest. It was very unstable, and 10% of change in capacitor value, would degrade the whole performance of the transfer function. The only way to implement this filter at such a high frequency is by using a trim capacitor. Considering that we did not have any experience in building this filter we turned to easier solution, which was to build microstrip coupled filter, since it does not depend on quality factor of any components. The ADS schematic is shown below.

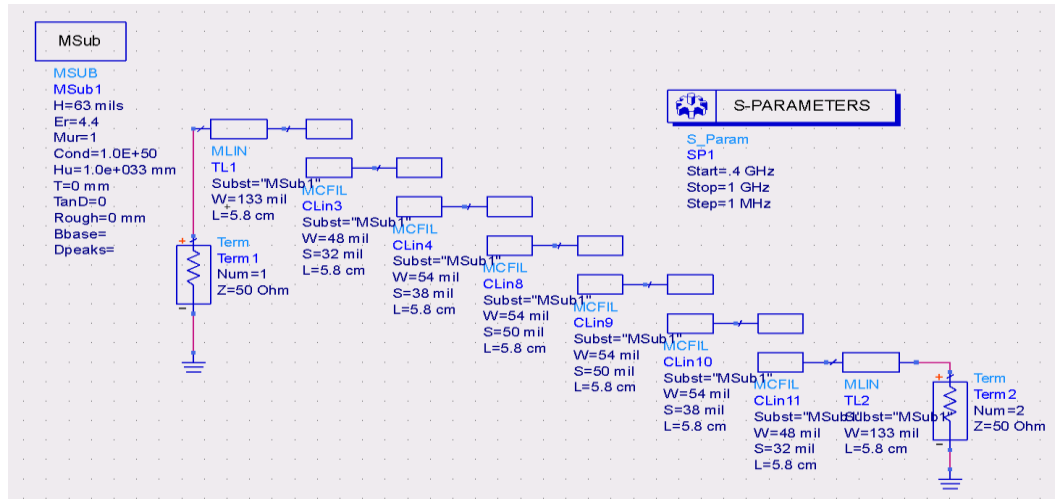


Figure 19. ADS Design of microstrip coupled filter

We calculated the separation between microstrips by examining and calculating the even and odd mode impedances that we used from RF Circuit Design book by Prof. Ludwig Reinhold. We understood that our design would need a very careful layout, and therefore, we paid special attention to that detail. The only drawback of our design was the permittivity of FR4, and we assumed it to be 4.3.

The following figure shows the result of the ADS simulation:

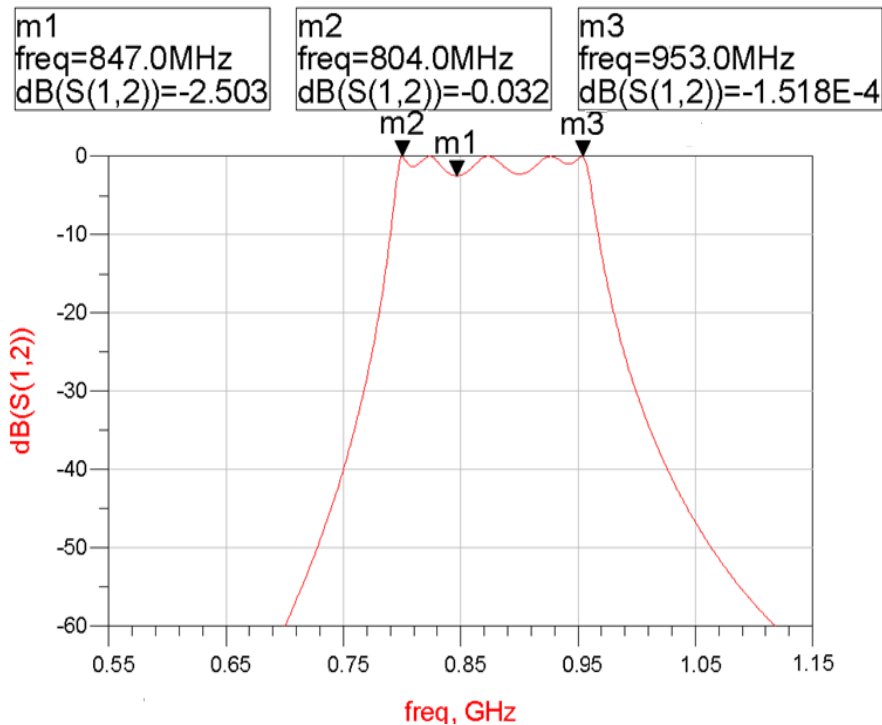


Figure 20. ADS Simulations for bandpass filter

Clearly, the transfer function has the characteristics that we were looking for, and we continued with the next step to actually, build this piece.

4.3. Synthesizer circuit

For the synthesizer circuit we are aiming to create a circuit that outputs 0 dBm of power to four different lines that are fed to LO inputs of dual-mixers in the IF boards. Our constraint was that we only had a signal from synthesizer RFMD2071 (VCO + PLL) that had 0dBm output power at one channel. Therefore, we decided to use a power splitter to divide power of one channel to four channels that are each isolated from each other. Mini circuits offer power splitter that perform such action, and they have according to data sheet 8 dB of loss. Therefore, we needed to use some sort of amplifying stage to boost the signal. We found a great product ADL5601 from Analog Devices, Inc. that had constant gain of 15 dB across a very wide band of frequencies. Therefore, this looked as a feasible choice for our design. Finally, to make the gain around 0 dBm, we are planning to buy 5dB and 7 dB attenuators, to tune the synthesizer so that it outputs signal of around 0 dBm.

Synthesizer is SPI programmable and controlled by the microblaze controller on the FPGA. The SPI code has only three lines in our case, since we are only sending information from master to slave (from microblaze to synthesizer). We also found all the registers that need to be changed to increment the frequency of the synthesizer from 950 MHz to 1100 MHz.

4.4. IF Board

Prior to IF Board we selected two LNAs ADL5521, that are pHEMT amplifiers that have 21 dB of noise figure, high linearity OIP3 of 34 dBm and noise figure of only 0.8 dB. The mixer that we chose a passive double balanced ADL5358 with low SSB noise figure 9.9 dB, and a single ended 50 Ohm input port. There are also various other parameters that we looked at, and the performance beat their competition, from Texas Instruments, Mini Circuits, RFMD... We observed the spurious effects of the mixer, and we estimated that it is safe to operate at frequency of 150 MHz. This mixer is followed by a very sharp SAW filter, that has high insertion loss, which is quite usual because of their nature. 5-bit parallel DGA allows us to maximize the dynamic range before the ADC, and therefore to enhance signal strength of far-away signals, and reduce the strength of signals that are close. Finally, the 16-bit ADC that we are using runs from

the reference clock of 130 MHz, and will sample the data fast enough so that we can easily reconstruct the picture since our bandwidth is 20 MHz. We expect our components to be SPI programmable so that we can easily enable them when needed.

4.5. Interface Card Design

In the Design of the Interface Card, we had to meet the requirements on one hand interfacing the analog to digital converters and the serial control lines on the IF boards, but also interfacing to the FPGA. The FPGA interface was our design “bottleneck”: it featured 80 high speed ports on the Very High Density Connectors as seen in Figure 21 (VHDC, 2 of which were allocated for the clock), and 32 low speed ports on the PMOD connectors.

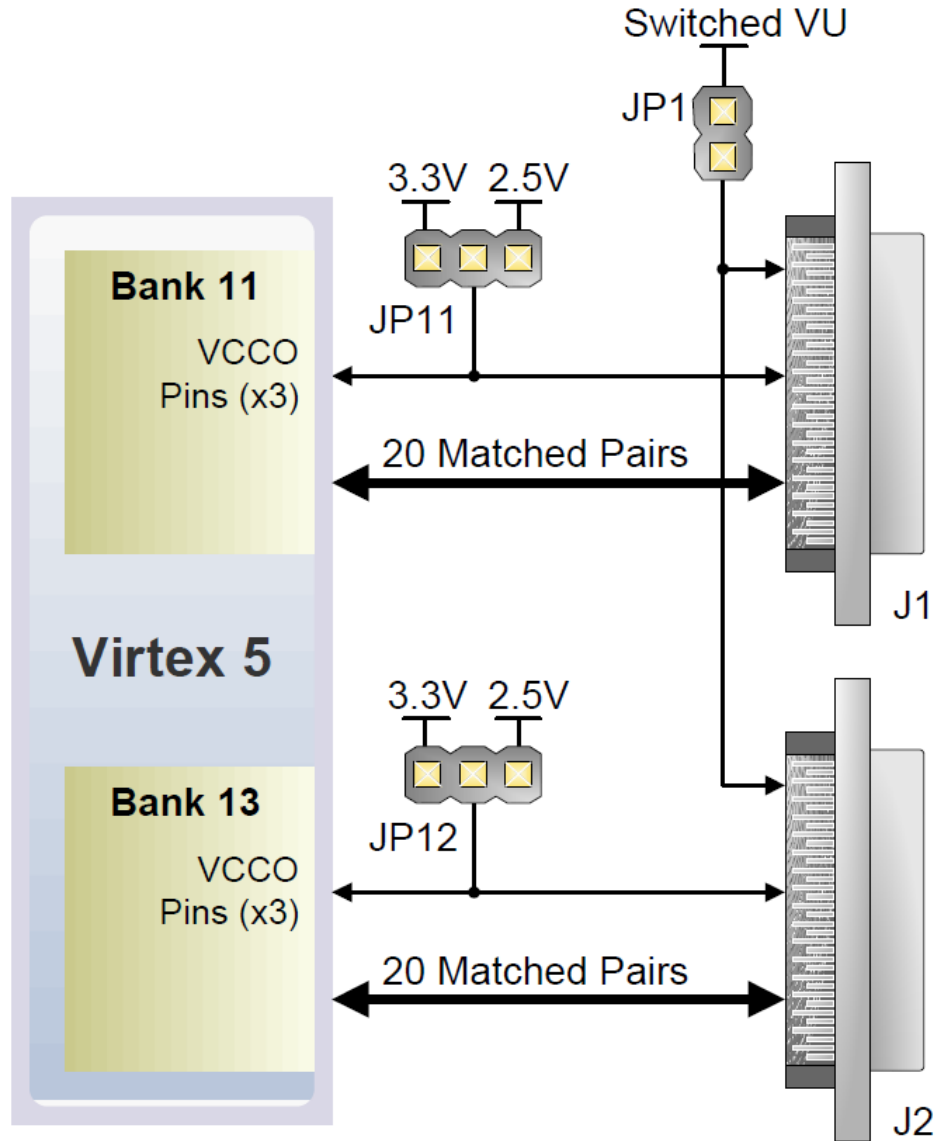


Figure 21 VHDC connectors

This became a challenge, because that on the analog to digital converter interface we had to include 144 high speed and 240 low speed signals. The analog to digital converter signal schedule can be seen in the following table:

Table 4 Signal Schedule

| | | | | | | | | | | | | |
|------|--------------|-------------------|-----|-----------|-------------|-----|--------|--------------------|-----|-----------|--------------|--|
| P903 | | | | | | | | | | | | |
| A1 | NC | | B1 | NC | | C1 | O_D0A | ADC A Data | D1 | AD8376A0 | VGA-ADATA | |
| A2 | O_D1A | ADC A Data | B2 | AD8376A1 | VGA-ADATA | C2 | O_D2A | ADC A Data | D2 | AD8376A2 | VGA-ADATA | |
| A3 | O_D3A | ADC A Data | B3 | AD8376A3 | VGA-ADATA | C3 | O_D4A | ADC A Data | D3 | AD8376A4 | VGA-ADATA | |
| A4 | O_D5A | ADC A Data | B4 | NC | | C4 | O_D6A | ADC A Data | D4 | NC | | |
| A5 | O_D7A | ADC A Data | B5 | V5DIV_ON | DIV 5V Rail | C5 | O_D8A | ADC A Data | D5 | NC | | |
| A6 | O_D9A | ADC A Data | B6 | NC | | C6 | O_D10A | ADC A Data | D6 | NC | | |
| A7 | O_D11A | ADC A Data | B7 | NC | | C7 | O_D12A | ADC A Data | D7 | NC | | |
| A8 | O_D13A | ADC A Data | B8 | NC | | C8 | O_D14A | ADC A Data | D8 | NC | | |
| A9 | O_D15A | ADC A Data | B9 | NC | | C9 | NC | | D9 | NC | | |
| A10 | O_CLK_A | ADC A Data CLK | B10 | NC | | C10 | O_ORA | ADC A Out of Range | D10 | V5MAIN_ON | MAIN 5V Rail | |
| P902 | | | | | | | | | | | | |
| A1 | NC | | B1 | NC | | C1 | O_D0B | ADC B Data | D1 | AD8376B0 | VGA-B-DATA | |
| A2 | O_D1B | ADC B Data | B2 | AD8376B1 | VGA-B-DATA | C2 | O_D2B | ADC B Data | D2 | AD8376B2 | VGA-B-DATA | |
| A3 | O_D3B | ADC B Data | B3 | AD8376B3 | VGA-B-DATA | C3 | O_D4B | ADC B Data | D3 | AD8376B4 | VGA-B-DATA | |
| A4 | O_D5B | ADC B Data | B4 | NC | | C4 | O_D6B | ADC B Data | D4 | NC | | |
| A5 | O_D7B | ADC B Data | B5 | NC | | C5 | O_D8B | ADC B Data | D5 | NC | | |
| A6 | O_D9B | ADC B Data | B6 | NC | | C6 | O_D10B | ADC B Data | D6 | NC | | |
| A7 | O_D11B | ADC B Data | B7 | NC | | C7 | O_D12B | ADC B Data | D7 | NC | | |
| A8 | O_D13B | ADC B Data | B8 | NC | | C8 | O_D14B | ADC B Data | D8 | NC | | |
| A9 | O_D15B | ADC B Data | B9 | NC | | C9 | NC | | D9 | NC | | |
| A10 | O_CLK_B | ADC B Data CLK | B10 | NC | | C10 | O_ORB | ADC B Out of Range | D10 | NC | | |
| P901 | | | | | | | | | | | | |
| A1 | LIN_EN1V82 | DRVDD and DVDD EN | B1 | LIN_EN3V3 | 3V_CLK | C1 | NC | | D1 | NC | | |
| A2 | LIN_EN1V81 | ADC AVDD EN | B2 | SW_EN2 | V_REG EN | C2 | NC | | D2 | NC | | |
| A3 | NC | | B3 | SW_EN1 | V_REG EN | C3 | NC | | D3 | NC | | |
| A4 | NC | | B4 | USB_SDO | VCO SDO | C4 | NC | | D4 | NC | | |
| A5 | AD9517_CSB | N_CS ADC VCO | B5 | USB_SDI | VCO ADC SDI | C5 | NC | | D5 | NC | | |
| A6 | USB_CSB | ADC CSB | B6 | USB_SCLK | VCO ADC CLK | C6 | NC | | D6 | NC | | |
| A7 | ADL5356_PWDN | Mixer PWDN | B7 | FPGA_CSB | ADC CSB | C7 | NC | | D7 | NC | | |
| A8 | AD8376ENBB | VGA EN A | B8 | FPGA_SDO | VCO SDO | C8 | NC | | D8 | NC | | |
| A9 | AD8376ENBA | VGA EN B | B9 | FPGA_SDI | VCO ADC SDI | C9 | NC | | D9 | NC | | |
| A10 | AD9517_PWDN | VCO PWDN | B10 | FPGA_SCLK | VCO ADC CLK | C10 | NC | | D10 | NC | | |

Reanalyzing the design, we have decided that the analog to digital converter could be used in the interleaved mode, where both outputs of the dual converter appear in the bits of just one, but at double the rate (like the Dual Data Rate Standard). Details of this transaction can be seen in Figure 22.

Timing Diagrams

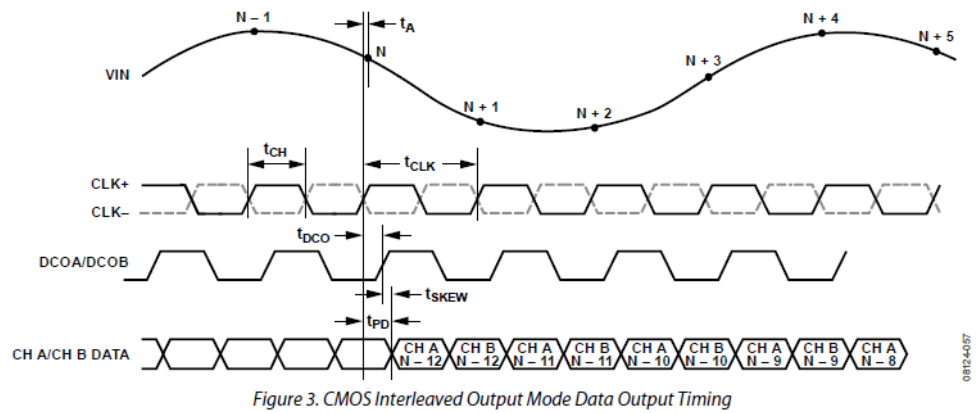
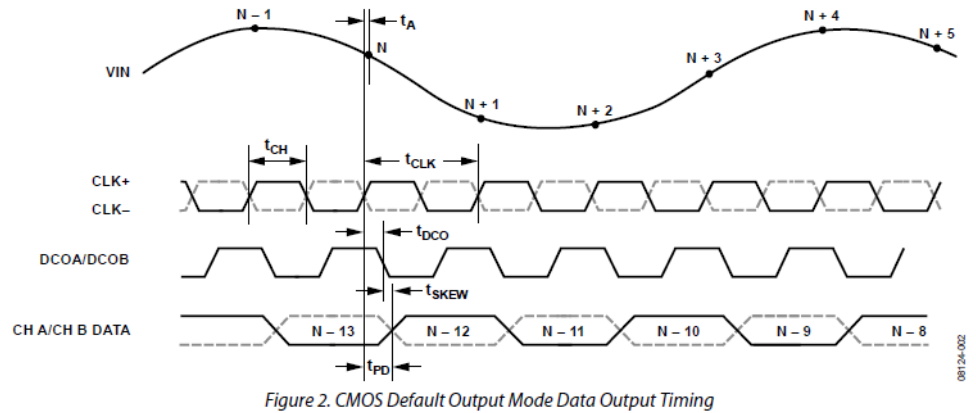


Figure 22 Timing Diagram for the Interleaved mode

This allowed us to decrease the number of high speed signals routed through the interface card by almost a factor of 2, because the sixteen bits of each channel of the dual ADC appear on the same output pins. This allowed us to interface the high speed signals into the FPGA through the very high density connectors.

Regarding the relatively low speed control signals, we have decided to route them out to standard 0.1 inch connectors on the interface card for the flexibility to further route them to the FPGA.

This will also allow to tie some of the control signals, such as the variable gain amplifier gain control pins together for initial testing. This can be desirable, because we do not expect the gain

to vary by a large amount cross channel, so the gain can be initially set as equal across all eight channels.

In the design of the interface card some of the other design problems were crosstalk and phase shift. Due to the fact that the design required all four IF board to be routed into the FPGA through the very high density connectors, the interface board had to be rather large, which implied the length of the traces carrying data from analog to digital converters to the FPGA. The length of the traces may lead to significant phase delay which will vary from channel to channel. It could also lead to crosstalk between bits of the same channel. As seen in Figure 23, when the aggressor trace is making a transition, there is a sudden spike in current, which will leak through the capacitance between the traces, inducing voltage in the victim trace.

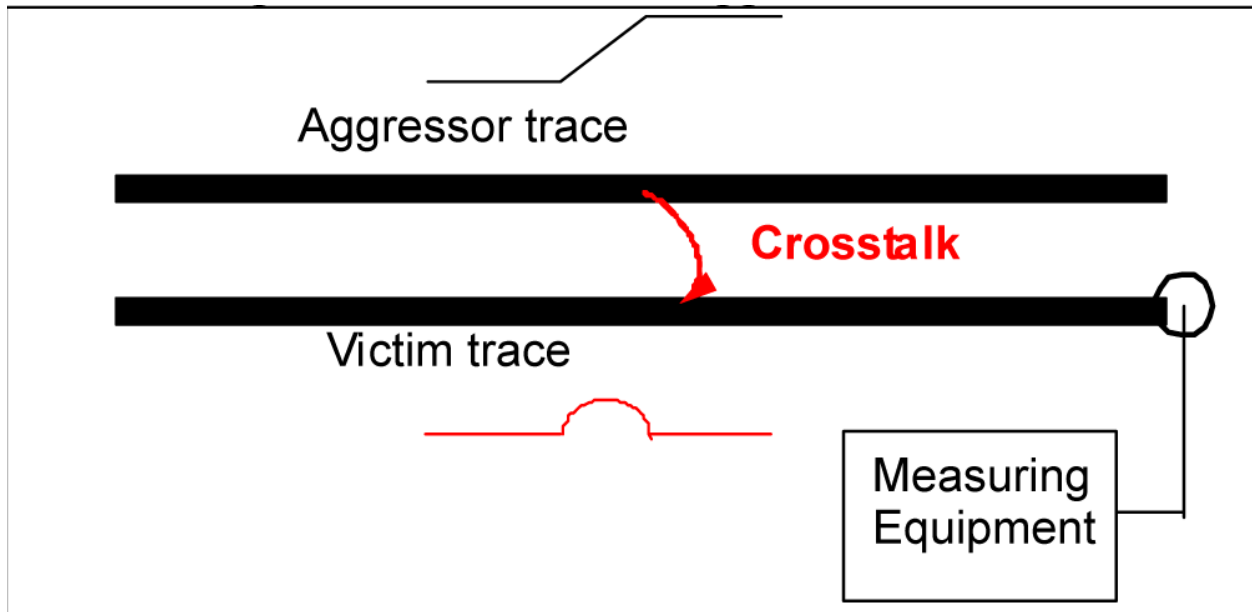


Figure 23 The aggressor-victim trace pair

The crosstalk problem can be accounted for using several “good” design techniques. To begin with, it is good practice to keep the high speed data traces as far away from other traces and each other as possible. Usually the separation of four times the trace width will reduce the crosstalk

tremendously. In our design, we used five-six times the trace width separations right until the very high-density connectors at the FPGA. Therefore, the majority of crosstalk may happen there, but the trace lengths at the connector are very short, which will account for little crosstalk. Another important design decision was to use multiple ground planes, which will isolate traces on the bottom plane from the trace on the top plane, but will also isolate trace that are spaced relatively far apart on the same plane. However, this can introduce currents that will flow from the high speed traces directly into the ground plane, thus creating voltage difference between ground planes on different layers of the printed circuit board, which is highly undesirable. Luckily, routing multiple vias can solve this problem by shorting the ground planes together in critical locations and thus isolating the signals in a much better fashion.

4.6. FPGA data capturing

In the design of the FPGA data capturing circuit several requirements came into play. First, design restrictions that came from designing the interface card, such as the interleaved data format, and the fact that all four analog to digital converter clocks are asynchronous to each other. Another design constraint is the way we plan to process the data after the capturing. There is no need to do real time data processing, because this is not an application where every sample needs to receive an output. Therefore, we will stick to capturing the data first and doing the processing offline later. In order to perform this, we need to first capture the data and store it in some memory array, RAM for example. However, to do this we need to synchronize all of the data to an edge of one clock. This was done in two steps. First, all of the analog to digital converter data was deserialized, and synchronized to the rising edge of its own clock, which produced eight data streams synchronous to four clocks (four clocks are asynchronous of each other, because they ran on traces of different lengths on the interface board). After all of the data

is deserialized, we then need to synchronize it to just one clock, which will be used to store all of the samples in the RAM. This requires a clock domain operation, which can be achieved by means of First-In-First-Out buffers. These buffers can read the data using the native analog to digital converter clocks synchronized with the data. Later, when the buffers fill up, one clock can be used to read all eight channels of data synchronously. Using this technique we can synchronize all of the captured data to the edge of just one clock. At this point it is possible to either read all eight channels at the same time or read all data from one channel followed by the data from the next and so on. This allows for much greater flexibility for further data processing. In our design we really wanted the flexibility to be able to reconfigure the functionality of our system on the go, therefore this versatile block proved to fit our needs the best. Another addition to our system that makes it flexible is the microblaze processor. This piece pulls all of the parts of our design together. We have decided to place this piece in charge of controlling all of the transactions that happen in the whole system. The processor can control when the data is sampled and when it is read from the buffers and later placed in the RAM. It also decides what will happen to the data after that. We implemented a number of interfaces to the processor to be able to fulfill this functionality. The interfaces had to be built involving both hardware and low-level firmware to allow for the communication between the processor and the peripherals, such as the RAM, Serial Peripheral Interface (SPI), Serial Port (RS232), First-In-First-Out buffers, and so on. The processor was not designed by our MQP team, rather it is an intellectual property of Xilinx, just like some other blocks like SPI, or RS232, however all of the interfaces and configurations are indeed our own work.

In order to set up a transaction between the processor and the FIFO blocks, it was critical to understand how the processor functions and how the data and address busses are scheduled for

read and write cycles. For this we had to turn to the documentation on the microblaze processor. Some of the important details can be seen in Figure 24, Figure 25, and Figure 26.

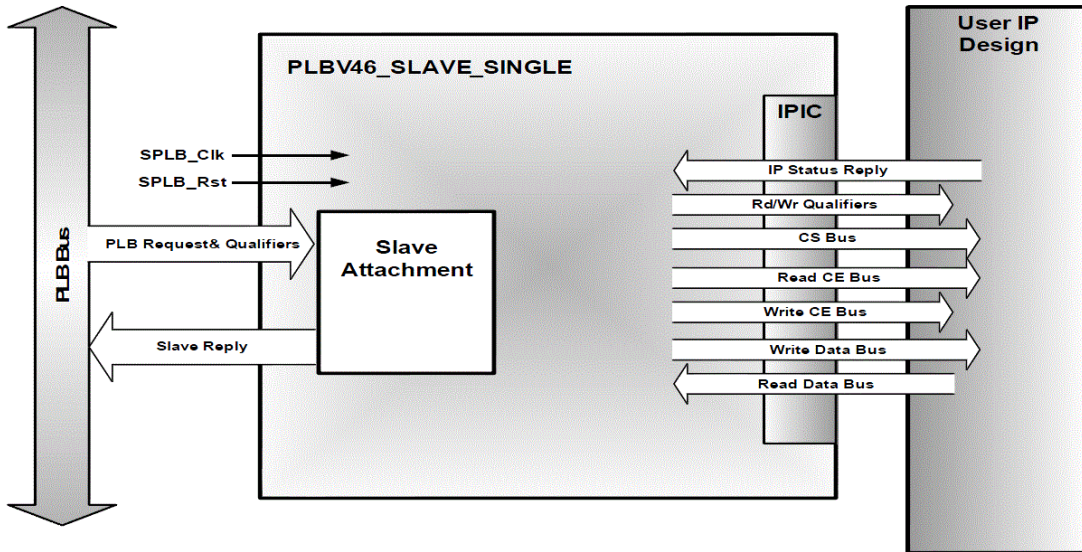


Figure 1: PLBV46 Slave Single Core Block Diagram

Figure 24 PLB Interface

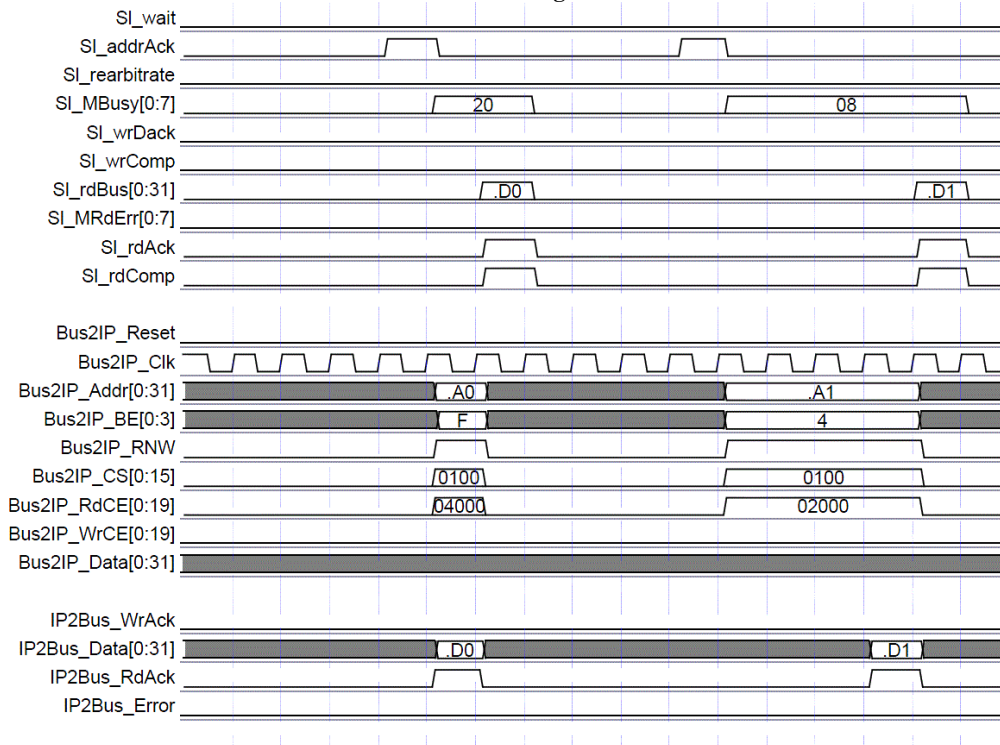


Figure 4: PLB Single Data Beat Read Timing (C_SPLB_P2P = 0)

Figure 25 PLB Single Data Beat Read Timing

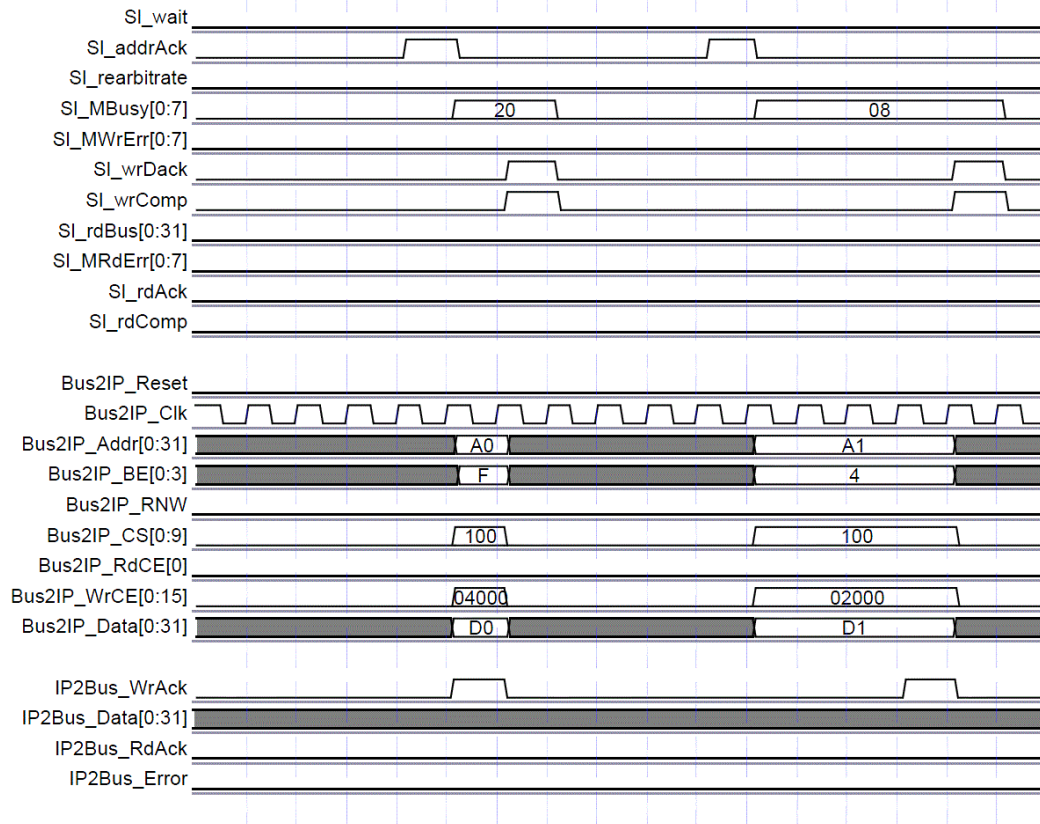


Figure 26 PLB Single Data Beat Write Transfer Timing

The interface was implemented in a fashion of a custom IP (intellectual property) block, abstracted away from the processor by the interface that makes it seem just like a standard memory device with standard read and write cycles. Therefore, the interface has to play the role of a translator from the language of the microblaze PLB (peripheral local bus) to the language of the FIFO memory block in order to control it.

4.7. Digital Beamforming

Initial evaluation of beamforming methods was performed using the MATLAB Phased Array Toolbox. While this was valuable for understanding some of the performance of the algorithms, the included ones were limited, difficult to customize, and proved near impossible to port to standard C code in a manner that would be targetable to and FPGA. Simulations were constructed by using standard MATLAB that would be simple to later transfer to C through the use of LPACK or similar linear algebra C libraries. The algorithms evaluated are as follows:

- ⤴ Conventional Beamformer
- ⤴ Capon's Beamformer
- ⤴ Linear Prediction
- ⤴ MUSIC (Multiple Signal Classification)

ESPRIT while quite powerful is better tailored to arrays of a larger size, and was excluded from analysis in this project.

First the signal model must be considered. Figure 2 outlines the physical interaction between the array and the impinging signals, specifically with consideration for the phase shift. The phase shift is represented in its complex form of:

$$e^{-j\beta\beta_m} \quad (11)$$

$$e^{-j\frac{2\pi}{\lambda}\Delta_m\sin(\theta)} \quad (12)$$

The phase shift can then be used to generate a steering vector a that can be applied to an impinging signal to determine the signal received by the array elements:

Consider

$$\mu = \frac{2\pi}{\lambda} \Delta_m \sin(\theta) \quad (13)$$

Where Δ is constant for all elements

The steering vector $a(\mu)$ is represented as

$$a(\mu) = [1e^{-j\mu} \dots e^{-j(M-1)\mu}]$$

Combining a set of steering vectors for each signal the full steering matrix A is generated:

$$A = [a(u_1) \ a(u_2) \ \dots \ a(u_d)] = \begin{bmatrix} 1 & 1 & \dots & 1 \\ e^{j\mu_1} & e^{j\mu_2} & \dots & e^{j\mu_d} \\ \dots & \dots & \dots & \dots \\ e^{j(M-1)\mu_1} & e^{j(M-1)\mu_2} & \dots & e^{j(M-1)\mu_d} \end{bmatrix} \quad (14)$$

With the time domain signals stored in the S matrix:

$$s(t) = \begin{bmatrix} s_1(t) \\ s_2(t) \\ \vdots \\ s_d(t) \end{bmatrix} \quad (15)$$

The matrix X which represents the signals seen at each of the elements can be determined:

$$x(t) = As(t) + n(t) \quad (16)$$

This matrix represents the signals on which the DOA algorithms will be tested against. The signals generated were uncorrelated and all centered at the same center frequently.

Spatial Covariance Matrix

The signals at the array elements are correlated while the noise at the elements is highly uncorrelated. The goal is to find the spatial covariance matrix R_{xx} , which represents the statistical estimation:

$$R_{xx} = E\{x(t)x^H(t)\} \quad (17)$$

If two conditions are met: the noise can be classified as ergodic (such as the Gaussian noise used) and that enough samples are collected, the approximation of R_{xx} can be computed through time averaging:

$$R_{xx} \approx \hat{R}_{xx} = \frac{1}{N} \sum_{n=1}^N x(t_n)x^H(t_n) = \frac{1}{N} X^H X \quad (18)$$

This value is critical for all of the evaluated DOA algorithms.

Conventional Beamformer

The conventional beamformer creates normalized weightings of a steering vector $a(\theta)$ and applies them to the Spatial Covariance Matrix to determine signal power across the scanned angles:

$$w(\theta) = \frac{a(\theta)}{\sqrt{a^H(\theta)a(\theta)}} \quad (19)$$

$$P(w) = w^H R_{xx} w \quad (20)$$

$$P(\theta) = \frac{a^H \hat{R}_{xx} a(\theta)}{a^H(\theta) a(\theta)} \quad (21)$$

Capon's Beamformer

Capon's Beamformer uses some nulling to help limited the effect of signals outside of the selected beam with a weighting vector:

$$w(\theta) = \frac{\hat{R}_{xx}^{-1} a(\theta)}{a(\theta)^H \hat{R}_{xx}^{-1} a(\theta)} \quad (22)$$

Resulting in the signal power vector:

$$P(\theta) = \frac{1}{a^H(\theta) \hat{R}_{xx}^{-1} a(\theta)} \quad (23)$$

Linear Prediction Beamformer

Rather than using the steering vector to create the weightings, a vector representing a single unity gain array element is used. The selection of this element was temperamental as the research had shown. Improper selection would result in no distinct signals being located. For the results the element that produced the best response was used. In most cases this was an end element.

The weighting vector is represented as:

$$w(\theta) = \frac{\hat{R}_{xx}^{-1} u}{u^H \hat{R}_{xx}^{-1} u} \quad (24)$$

With a signal power vector of:

$$P(\theta) = \frac{u^H \hat{R}_{xx}^{-1} u}{|u^H \hat{R}_{xx}^{-1} a(\theta)|^2} \quad (25)$$

MUSIC Beamformer

This is the first of the so called “super-resolution” beamformers which work by breaking the Spatial Covariance Matrix down into signal and noise components. When the eigenvalues are evaluated for Rxx and sorted, two groups are identified, a set of smaller values which represent the noise component, and a set of larger values which represent the signal component. It was determined that the corresponding eigenvectors are in fact orthogonal to the true steering vector A. The orthogonal eigenvectors are stored in the vector V. From this relationship it is know that:

$$a^H(\theta) V V^H a(\theta) = 0, \quad (263)$$

when θ is equal to a signal DOA

The power is inversely proportional to this.

$$P(\theta) = \frac{1}{a^H(\theta)VV^H a(\theta)} \quad (26)$$

An additional improvement to the MUSIC algorithms is known as Minimum Norm, and simply serves to increase the sharpness of the peaks by squaring the denominator of the MUSIC power equation. A square matrix of dimensions equal to the number of array elements with a 1 in (1,1) is used to preserve the matrix dimensions.

$$P(\theta) = \frac{1}{|a^H(\theta)VV^H WV^H a(\theta)|} \quad (27)$$

All of these methods require to some extent that the signals are not correlated to be impinging on the array. In most environments, this is not the case, especially when there is opportunities for multipath interference. A method known as spatial smoothing was evaluated which divides the array into overlapping sub arrays.

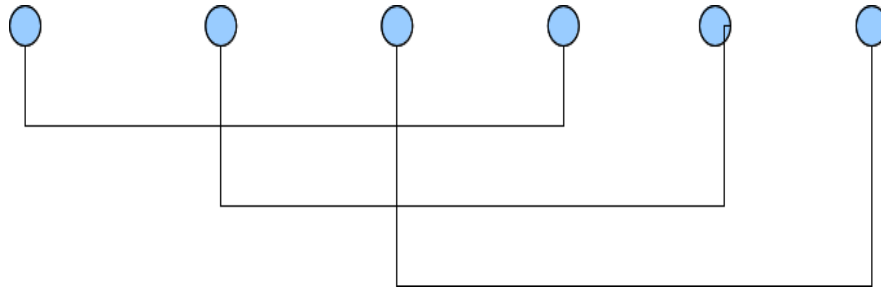


Figure 27 Sub Array Division

Shown in Figure 27 a 6-element array is divided into three four-element arrays. The more arrays the more effective the spatial smoothing is, however the maximum number of signals is reduced to one less than the number of element in the sub array. Spatial smoothing computes the Spatial Covariance Matrix for each of the sub arrays and takes the mean to generate a new Spatial Covariance Matrix which any of the previously mentioned algorithms can be applied to. In order to perform any of the MUSIC algorithms the number of signals or Model Order needs to be determined. One of the most effective methods for doing this is by evaluating the eigenvalues and attempting to locate the small values representing the noise and the large values representing the signals. In this case a version of Akaike Information Theoretic Criterion(AIC) was used.

$$AIC(d) = -2N(M-d) \log \left\{ \frac{\prod_{i=d+1}^M \lambda_i^{M-d}}{\frac{1}{M-d} \sum_{i=d+1}^M \lambda_i} \right\} + 2d(2M-2-d) \quad (28)$$

There are various version of this model, and most of the differences relate to the cost function on the end of the equation. The minimum of this function represents the Model Order.

In order to evaluate all of these models sample sizes of 1,000,000 were used and 5 passes were performed with 4 impinging signals, 0, 10, 20, 30 degrees. The peak power points were determined through the use of a quadratic interpolation. There are many ways to determine these peaks, but this is out of the scope of this analysis.

Chapter 5 Results:

In this section, we will present the results that we generated so far. We made subsections in which we will describe the results of antenna design, filter design, LNA stage, IF board, Synthesizer circuit, FPGA block and DSP Algorithms.

5.1. Antenna design

For our aperture coupled patch antenna, we wanted to create a hardware that is as close as possible to the model that was simulated in Ansoft HFSS. Our antenna had three main components, patch placed on top of FR4 sheet, aluminum box and 4-layer PCB board. We ordered FR4 sheets that we cut in dimensions of 6.6in x 6.6 in. Then we placed a copper tape in the middle to correspond to 134mm x 129 mm patch size. Considering the difficulty of making aluminum box with machinery that is available at Worcester Polytechnic Institute, we used services from Hydro-Cutter Inc., a company specialized in water jetting. We sent them the following file:

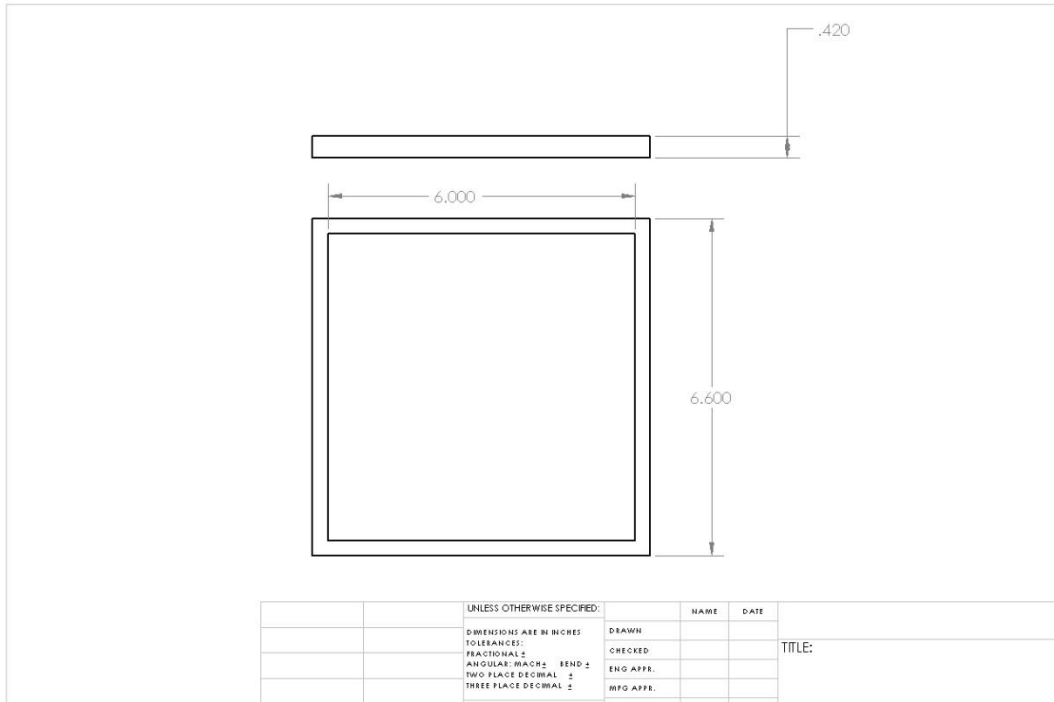


Figure 28. Dimensions of our aluminum box

Finally, we had to make a 4-layer PCB board that we sent to Advanced Circuits, Inc. In our design we basically made almost identical shape as the one created in Ansoft HFSS and that can be seen in the following figure.

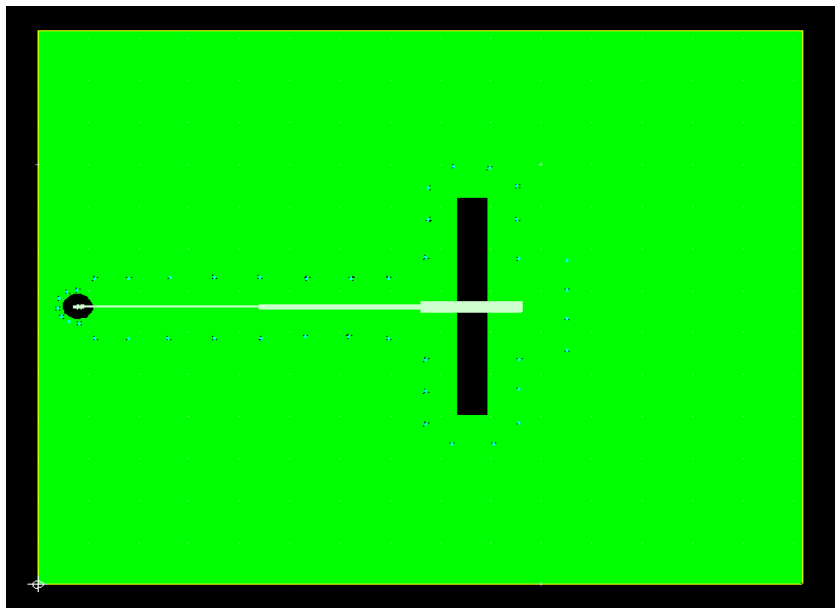


Figure 29. 4-layer PCB layout showing top ground plane and a stripline

Since the bottom ground plane is identical to top ground plane, it can't be seen in two dimensional plot. Once the boards came-in, we assembled the antennas as shown below:

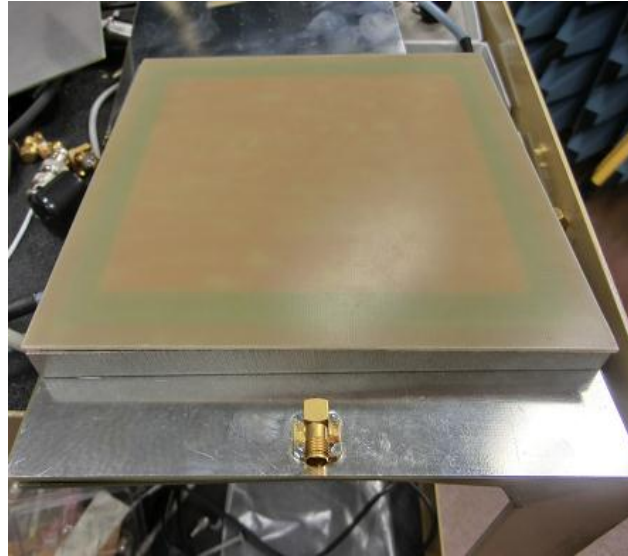


Figure 30. Our assembled antenna

The only mistake that we created in this antenna design was that we did not model correctly the Teflon part of the RF connector that is between the signal and ground. Since we didn't find its dimensions online, we assumed its dimensions in the final layout, and as a result, the FR4 region on the top ground plane is larger than the Teflon portion of the connector. The result is that only 10mil of FR4 separates stripline and RF connector, and therefore, once connector is soldered, the performance is completely degraded since it acts as a short circuit. Therefore, the only possible option was to capacitively feed the signal to the antenna. If we hold the connector with our hands, we get the response predicted from our simulations:

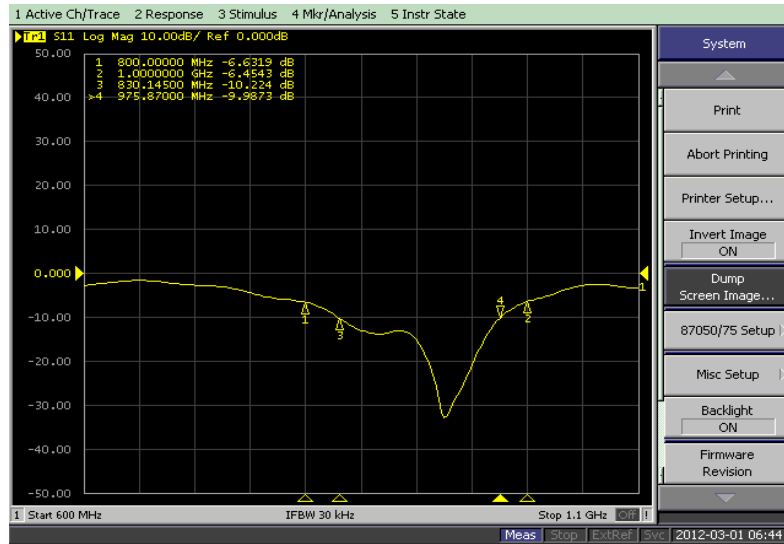


Figure 31. S11 vs. frequency measurement when we are holding the connector
 Since our body has a certain capacitance, the performance is improved. This gave us idea to create a capacitor using washers between the antenna and RF connector. This was somewhat successful idea considering that we got S11 shown below.

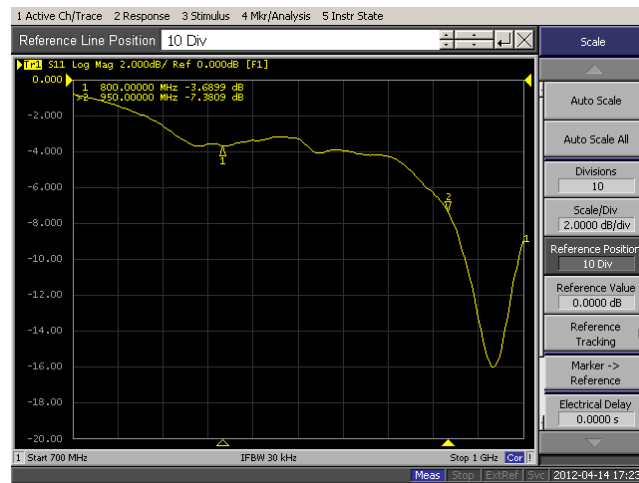


Figure 32. S11 of our antenna with washer between ground plane and connector
 We were not satisfied with S11 = -4 to -6dB in our band of interest, and therefore we tried to tune the antenna using capacitors. We tried capacitors that had values of 5pF, 10pF, 100pF, 200pF, 510pF, 1nF, 10nF and 100nF. The capacitor value of 510pF had by far the best performance and that is shown below:

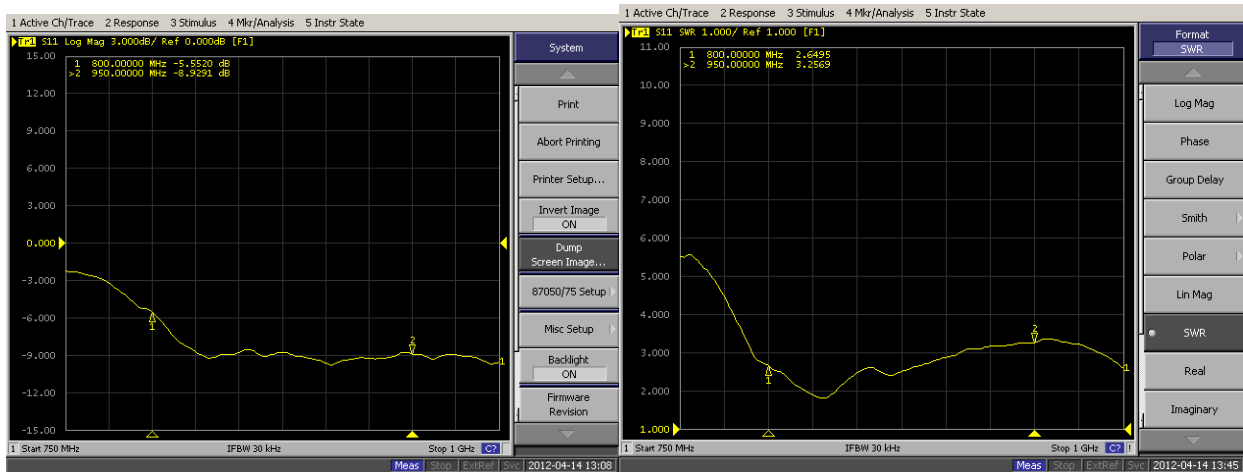


Figure 33. S11 vs. frequency of the antenna with 510 pF cap to the left, and SVWR to the right of 3 in worst case scenario

Clearly, this is a great improvement that we achieved with tuning. However, the problem with this approach is that we used cheap ceramic caps, and therefore, the resistive losses from parasitic effects will be manifested in S21 measurements as a loss at specific bands and that is emphasized in the next plot:

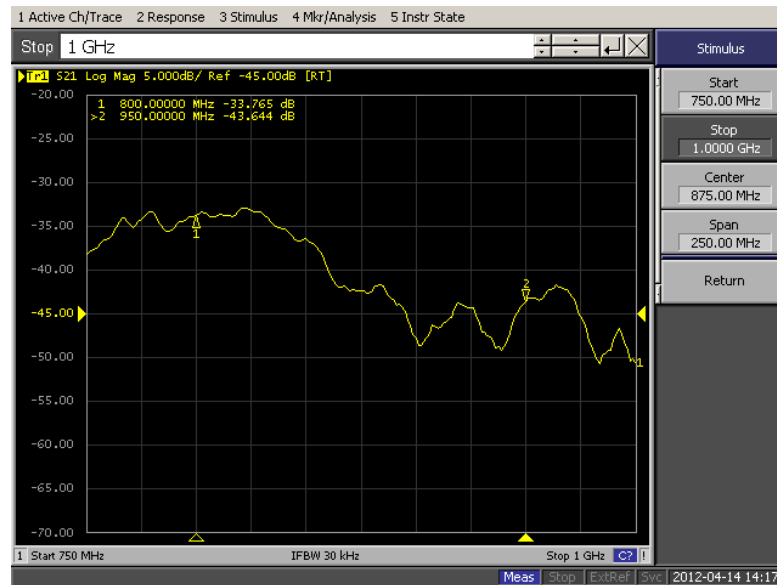


Figure 34. S21 of the antenna with 510pF cap

So, during the rest of D term we will try to buy a capacitor with high quality factor at high frequencies. S21 is a scattering parameter that is associated with a gain of two port system. We temporarily kept the design with washer and without the capacitor for our final prototype, since its S21 is actually quite impressive:

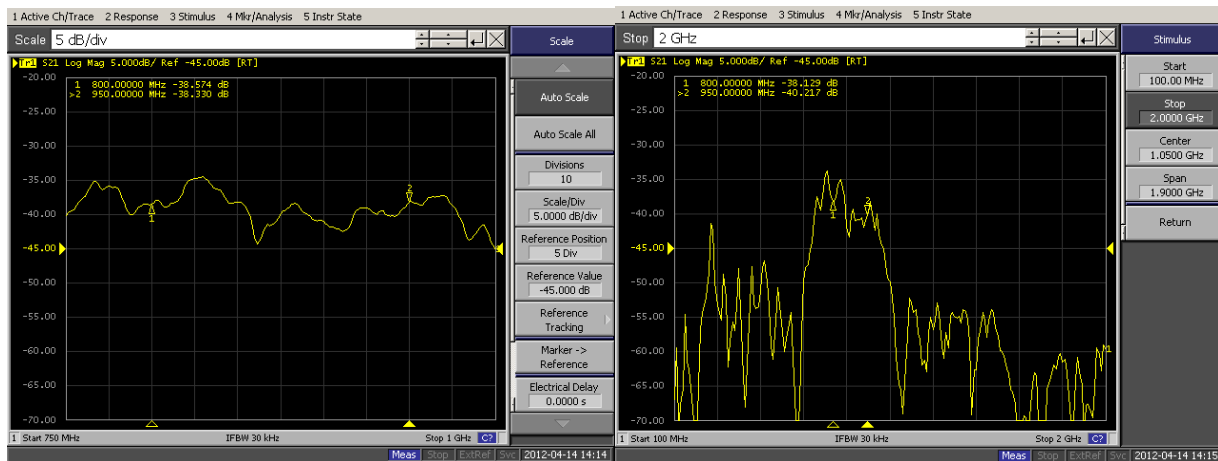


Figure 35. Narrow band S21 measurements (to the left) and wideband S21 measurements (to the right)

In the left picture we set the frequency range from 750 MHz to 1 GHz, and the markers represent our band of interest. Clearly, the S21 is quite stable for these frequencies (between -40 and -35 dBm). The picture to the right shows that our antenna is indeed a wideband antenna which receives EM waves of frequencies in our band. For comparison purposes we included also the S21 of a patch antenna that is centered at frequency of 950 MHz.

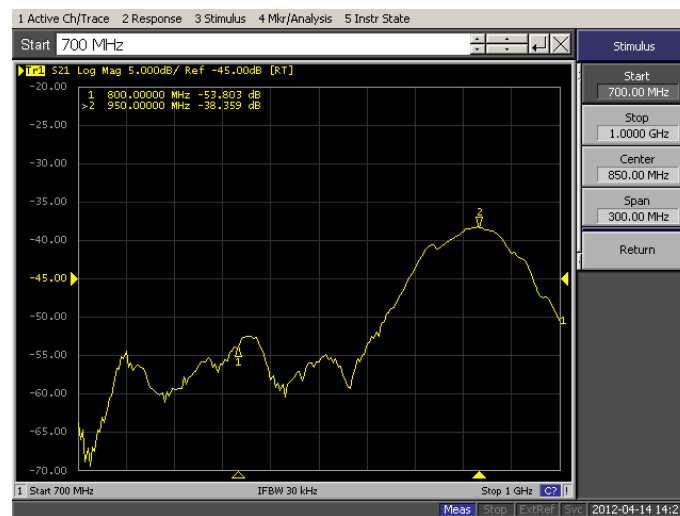


Figure 36. Patch antenna S21 showing narrow band characteristics

Comparing this figure with the previous one, we can observe the difference between narrow and wide band antennas. The set-up that was used for all these S21 measurements is best described by the following figure:



Figure 37. Measuring S21 of our aperture coupled patch antenna

The antenna that was transmitting the signal is a special type of Horn antenna, with very wide band and highly directive gain. Finally, we tried to measure the radiation pattern of our antenna. However, we experienced too much scattering and our chamber was certainly not appropriate for those measurements.

5.2. Filter design

For our filter design, we put on a 2-layer PCB board the simulation that was made in ADS, and the hardware that we received is shown below:

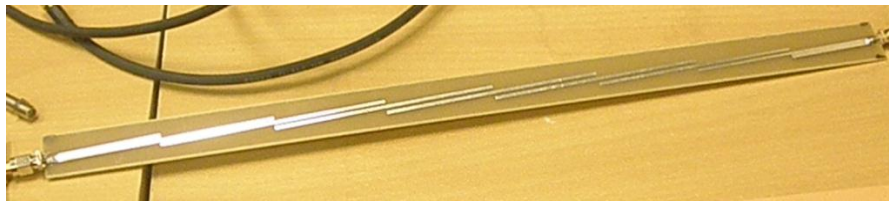


Figure 38. Microstrip coupled filter

Clearly, the immediate drawback is the size of this filter. Since there were no constraints on size, we only cared about its performance. We connected our filter, therefore, to network analyzer and we received excellent results. They are shown in the figure below:

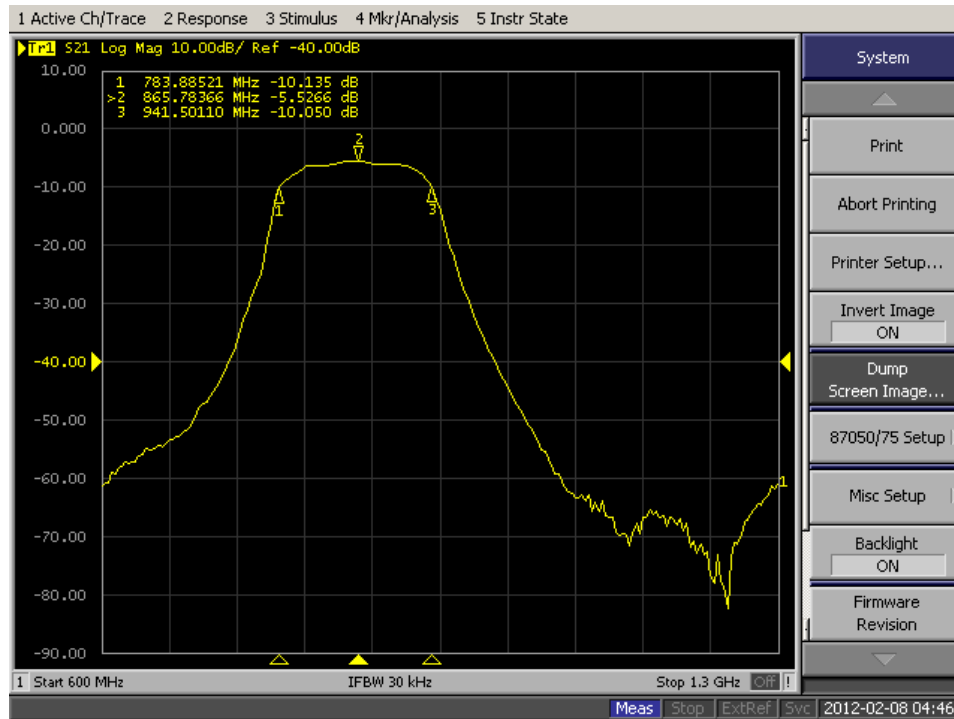


Figure 39. Narrowband view of the S21 performance of our filter

From the snapshot we can see that the insertion loss is -5.5 dB, and is pretty flat across most of the band. The response is quite sharp, which is not surprising considering that we built a fifth order filter. The upper corner frequency is slightly moved to 941.5 MHz, but at 950 MHz, the losses are only 6 dB lower than the ones in the rest of our band. We also included a wide view of our filter design, since we wanted to emphasize the interesting nature of distributed circuits that have periodic nature. This periodic nature is however of not concern to us, since next resonance has a peak at -20 dB.

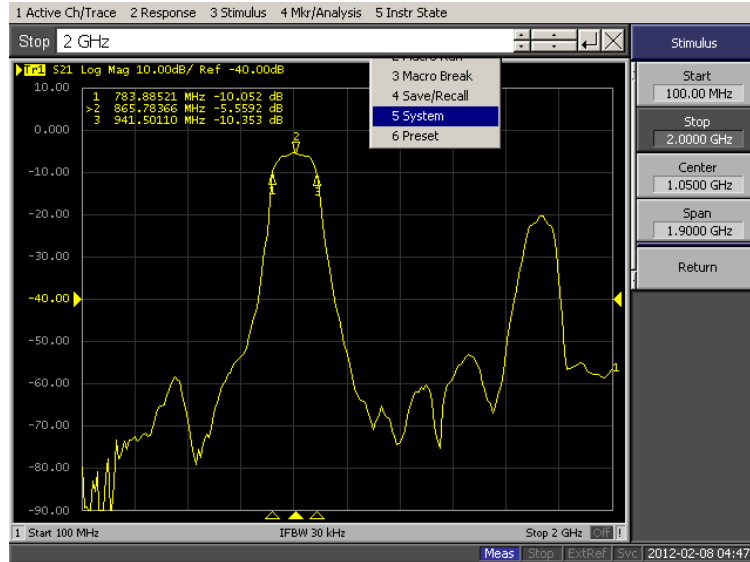


Figure 40. Wideband view of the S21 performance of our filter

5.3. LNA stage

We tested ADL5521 low-noise amplifiers that we will use in our front end. We printed 16 circuits boards with corresponding footprints for the IC chip and external matching network. The expected gain of the LNA is 21 dB. In the following figure, we show how we measured that the gain was 20.8 dB, since the input signal was at -50 dBm and output signal was at -29.2 dBm.

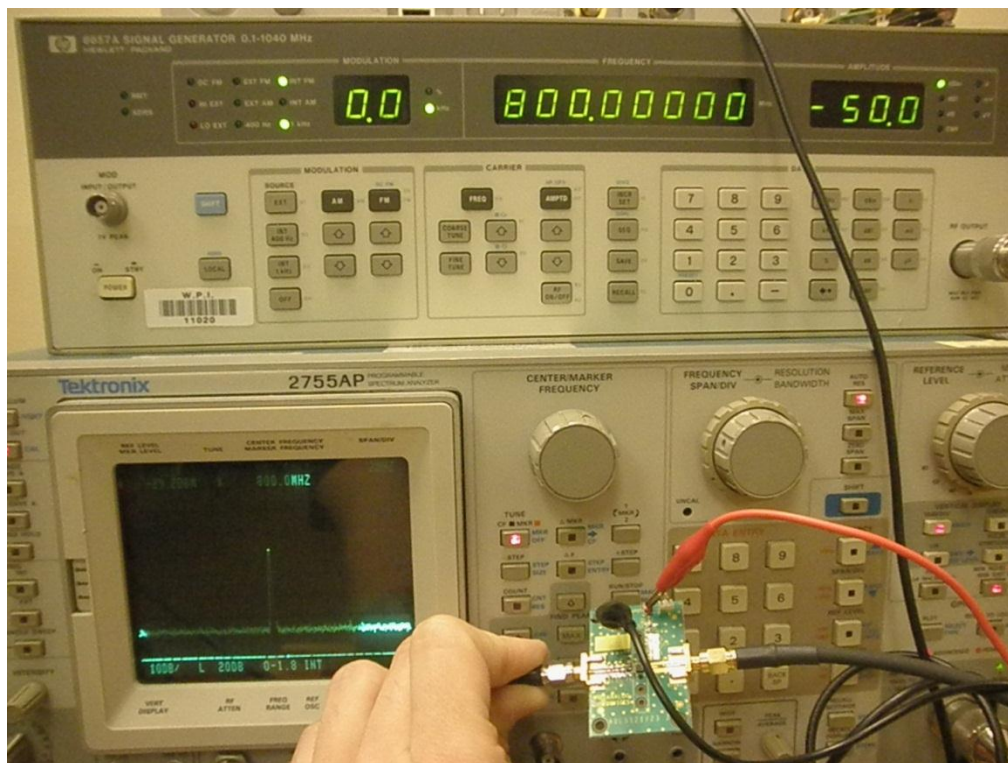


Figure 41. Testing of the LNA

The RF input was connected to signal generator, and the RF output was measured by spectrum analyzer. We tested this LNA at frequencies ranging from 800 MHz to 950 MHz in increments of 5 MHz, and the gain is constantly between 20dB and 21dB.

5.4. Synthesizer circuit

Considering the synchronization problem associated with phased arrays, we decided to run all LO input mixer ports with the same oscillator, so that we all channels experience the same phase shift introduced by each device in the signal chain. As explained in the methodology we stacked synthesizer with attenuator, wideband gain block and finally 1:4 power splitter with decent isolation. We first tested the power splitter, and each channel has 8 dB of loss relative to the RF input. This is slightly higher than the theoretical limit of 6 dB. The synthesizer circuit is shown below:

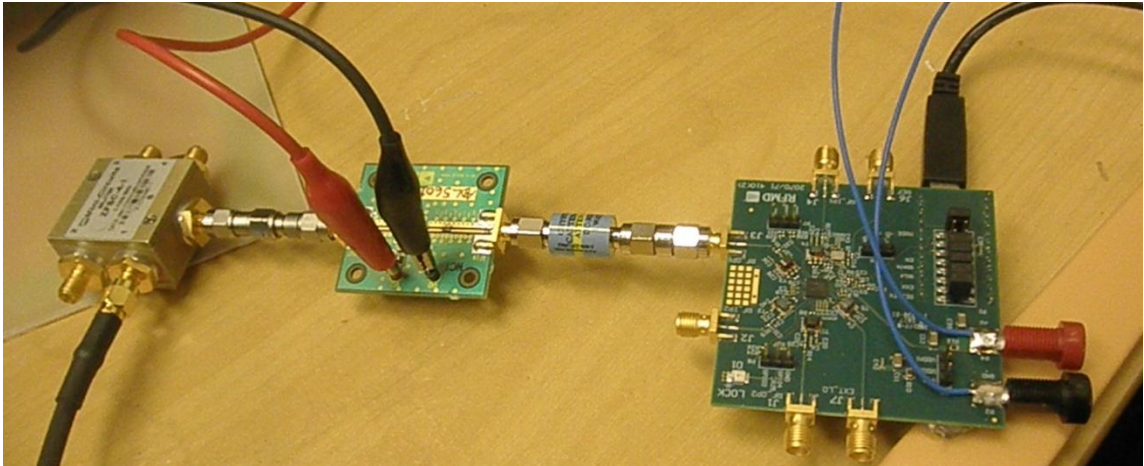


Figure 42. Synthesizer circuit

The reason why we do not have 1:8 power splitter, is because we need to supply power to only four dual-mixers. The required LO input power is at 0 dBm, and therefore, we had to amplify the signal from the synthesizer, and once we stacked all these elements we got the following signal at the output:

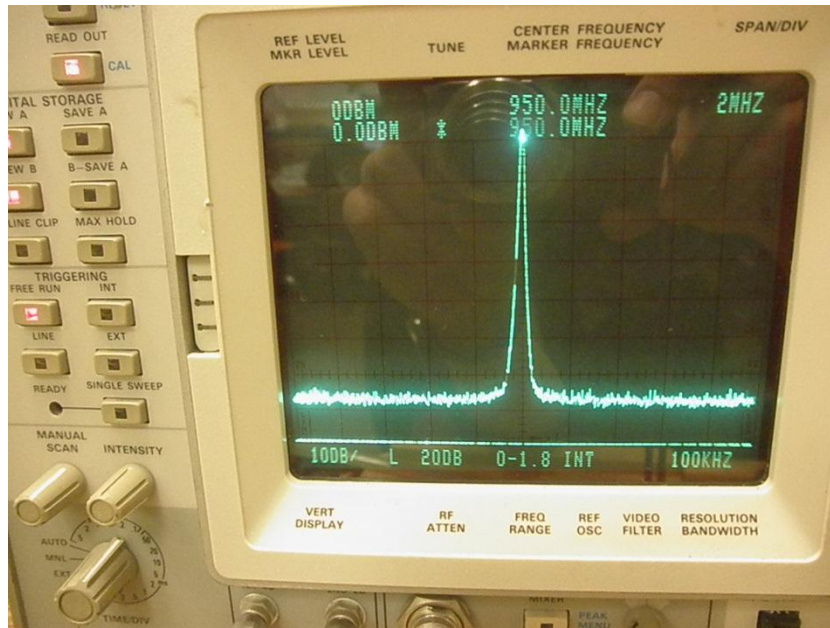


Figure 43. Output of power splitter has 0 dBm of power at 950 MHz

We originally planned to do low side injection to the LO input, however, the mixer that we chose has RF balun that is optimized for high side injection, and therefore, it doesn't produce any output if we feed it with the signal at 650 MHz. Therefore, the LO frequency range is 950 MHz to 1100 MHz.

5.5. IF board

Testing the IF board was really a giant piece, and we focused on doing that in two parts. First part was to measure the components using the signal from signal generator, and later to use the signal from the antenna and entire RF front end. Since the board has only two test points at the output of SAW filter that is after RF mixer, and also after the DGA, we didn't really have chance to test other nodes in the IF board, since everything operated at 150 MHz that is higher than our oscilloscope maximum limit. The IF board during measurements is shown below:

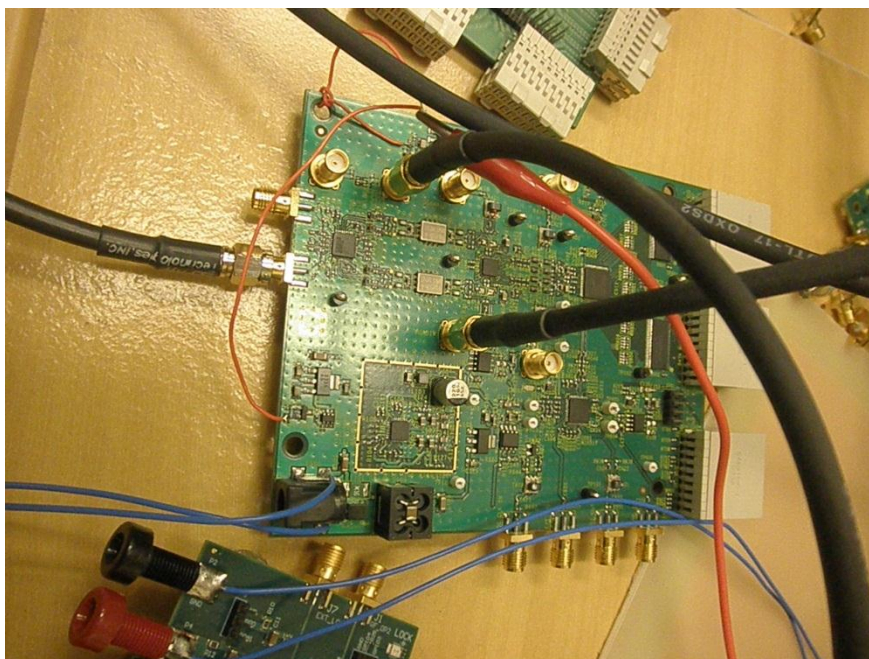


Figure 44. IF board during testing stage of our project

The input to our mixer was a signal generator set at power of -26 dBm and frequency of 800 MHz. We selected the LO input using the User Interface for the RFMD to be at 950 MHz at 0 dBm, and the output of the mixer is shown below:

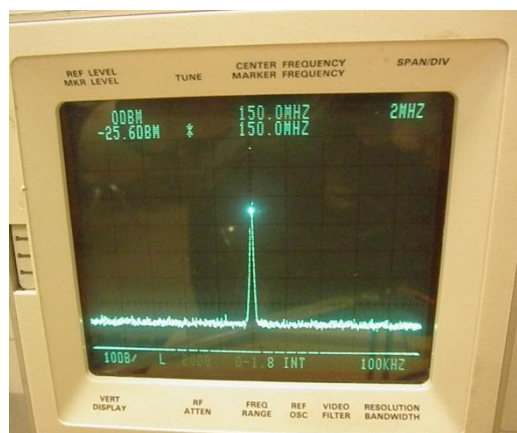


Figure 45. Output of the mixer at 150 MHz frequency

So the power of the signal at the output is almost identical to the power of the RF input. In addition, we measured the RF input to IF isolation, by sending a 0 dBm signal to the mixer, and checking its output:

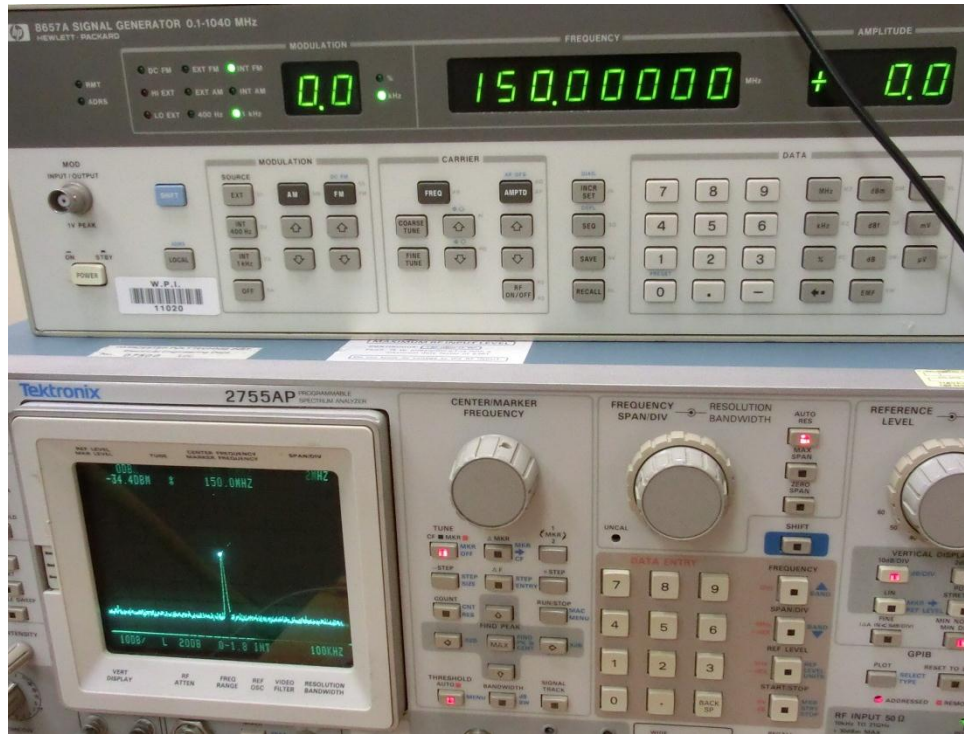


Figure 46. Testing the RFin-IF isolation

The RF input to IF isolation is -34.4 dBm, which is slightly worse than the specifications that say that it is -37 dBm. We also tested the LO to IF isolation, and from the data sheet it is -43 dBm, and here we tested it to be at -44.0 dBm as shown in the next figure.

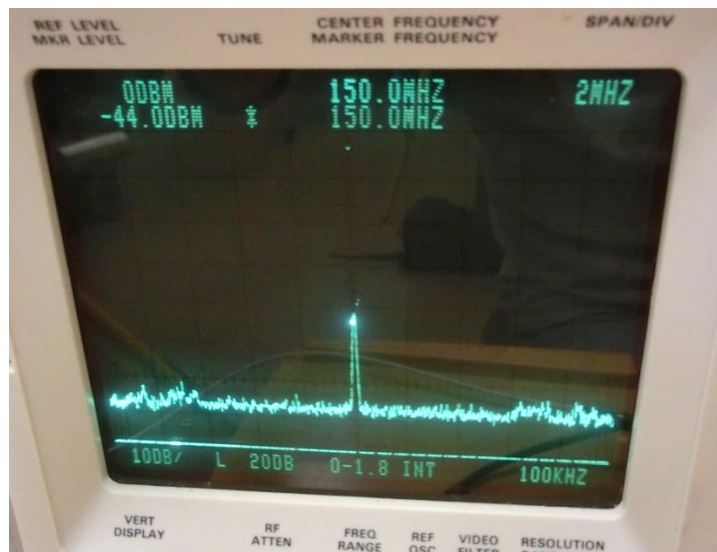


Figure 47. Testing LO-IF isolation

Getting satisfactory results from the mixer we continued to test with the “real signal” that would be received from an antenna. We set a horn antenna to transmit signal of 0 dBm at 800 MHz, and the receiver set-up is shown below:

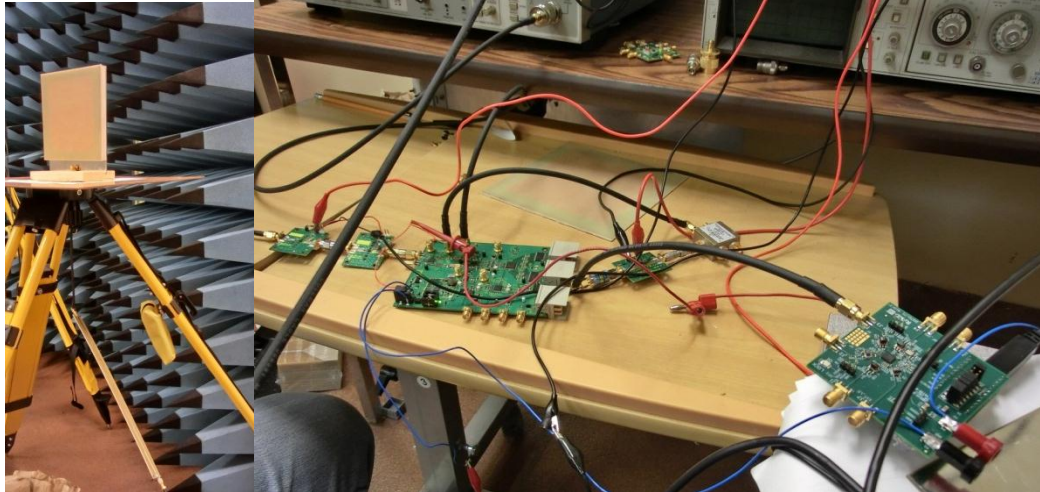


Figure 48. The set-up for analog system level measurements

The signal that we received at the RF input after cascaded LNA stage is shown below:

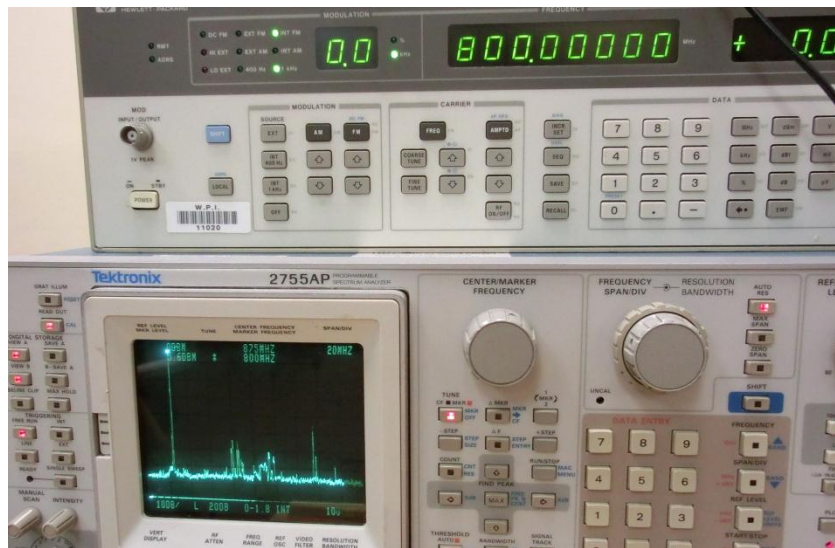


Figure 49. Receiving signals in our band from the antenna before the RF input to the mixer

In order to show that our antenna really picked the frequencies that are in our band of interest, we recorded the next spectrum analyzer shot that has a step of 150 MHz around 1.25 GHz. Clearly all our signals are either close or in our band of interest. It's important to notice that there is one more filtering stage after the mixer, which will get rid of jammers.

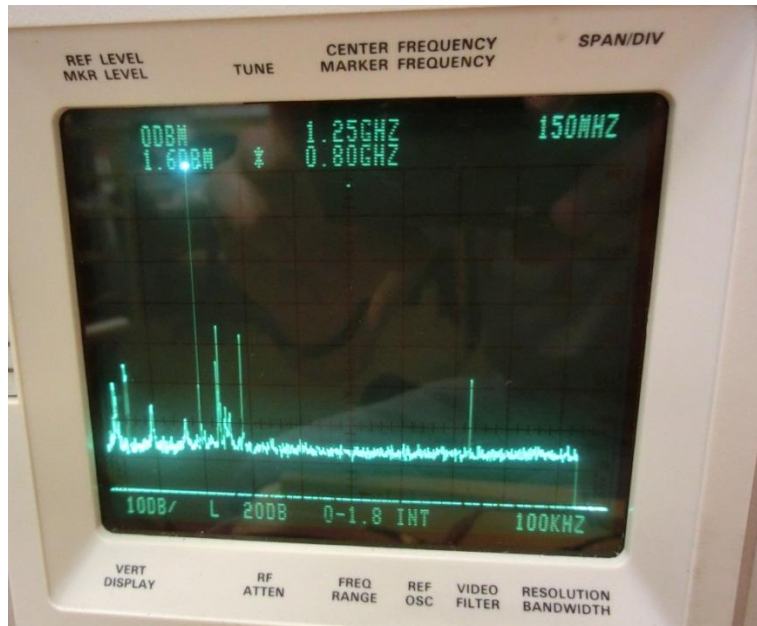


Figure 50. Wideband view of the RF input

After making sure that the performance of our RF input is expected, we went the step further and we recorded the measurements at the IF output of the mixer:

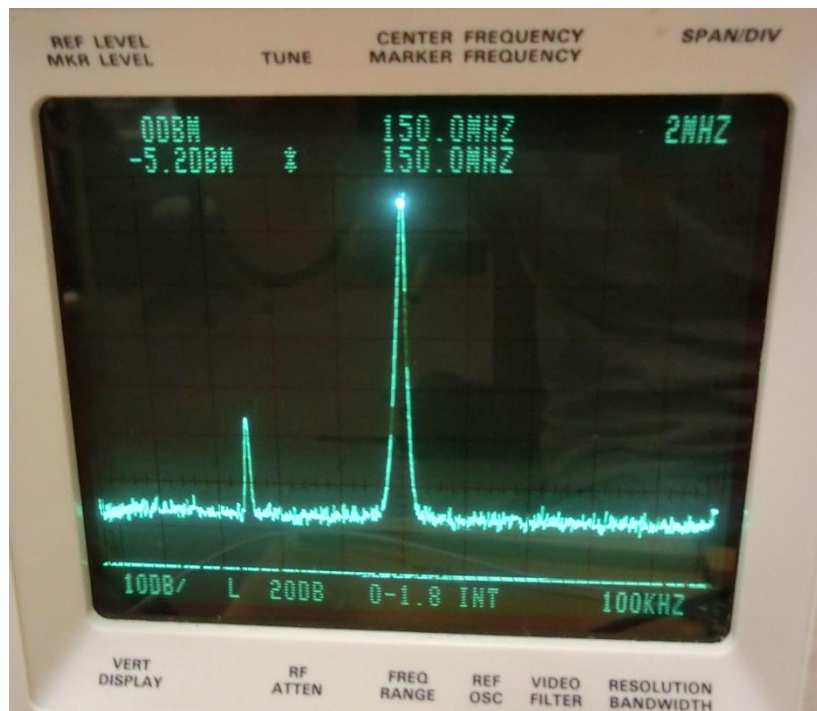


Figure 51. IF output of the mixer, where we can see the main signal at 150 MHz

We also observe that there is another signal at 145 MHz, which would be signal from which we would try to extract phase information. In addition, it is important to note that all these different waveforms that we recorded on spectrum analyzer are scaled versions of expected strength of

these signals, since our measurements were done in antenna lab that basically acts as a Faraday's cage and additionally, it has a chamber to absorb any radiation. Therefore, with this we proved that our analog components work perfectly and that they are ready in this stage to be digitized and processed.

5.6. FPGA FIFO

Verifying the FPGA logic design, we ran a number of simulations. First, the processor behavior was described as inferred from the master-slave datasheet provided by Xilinx. This VHDL description was used as part of the testbench to stimulate the IP interface design. The results proved to meet the timing specifications as indicated in the same master-slave datasheet from Xilinx IP.

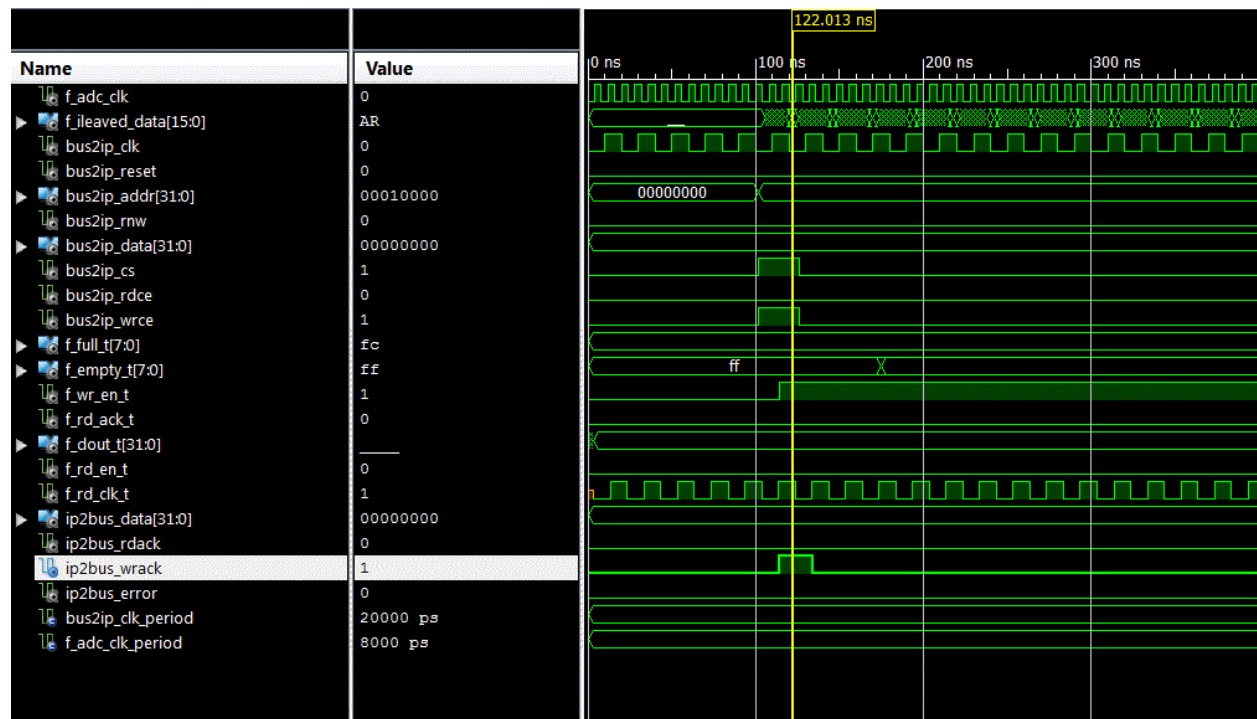


Figure 52 Post Place and Route simulation showing the write transaction

As can be seen in the following figures, we have produced and tested three separate transactions: flag read (read transaction), data capture (write transaction), and data read (read transaction).

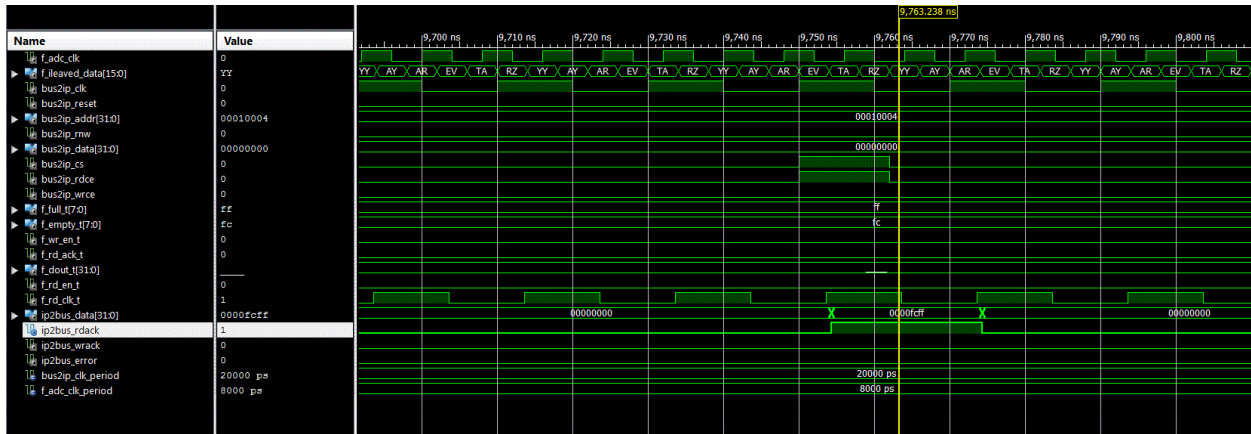


Figure 53 Post Place and Route simulation showing the flag read transaction

Each transaction was designated by the assertion and deassertion of the respective control signals, such as chip select, read enable, write enable, read not write, etc. The performance in this simulations was compared against the timing diagram provided in the datasheet for the master-slave pair.

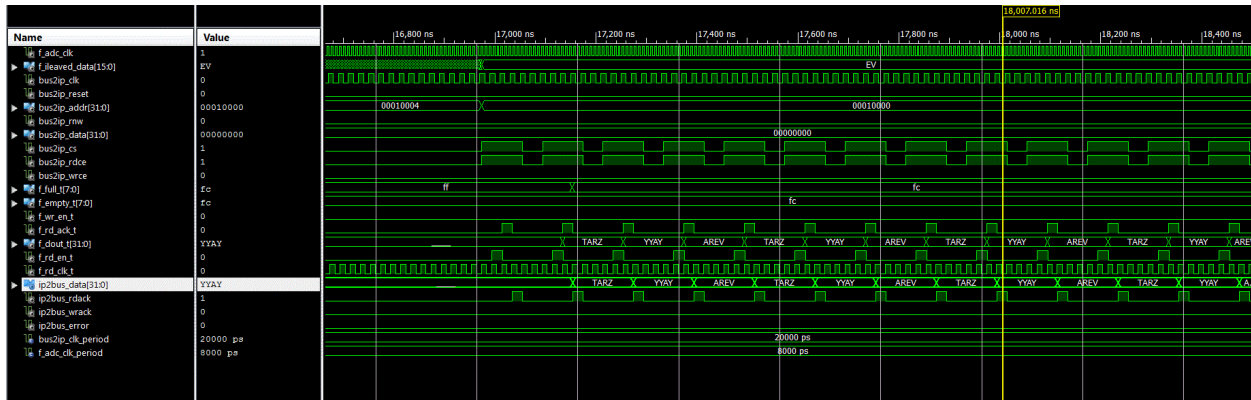


Figure 54 Post Place and Route simulation showing the data read transaction

Lastly, we can see in the following figure how we started with serialized data coming from the analog to digital converters and in all of the previous figures the data has been split into two 16bit data busses and then fed onto the 32 bit processor data bus.

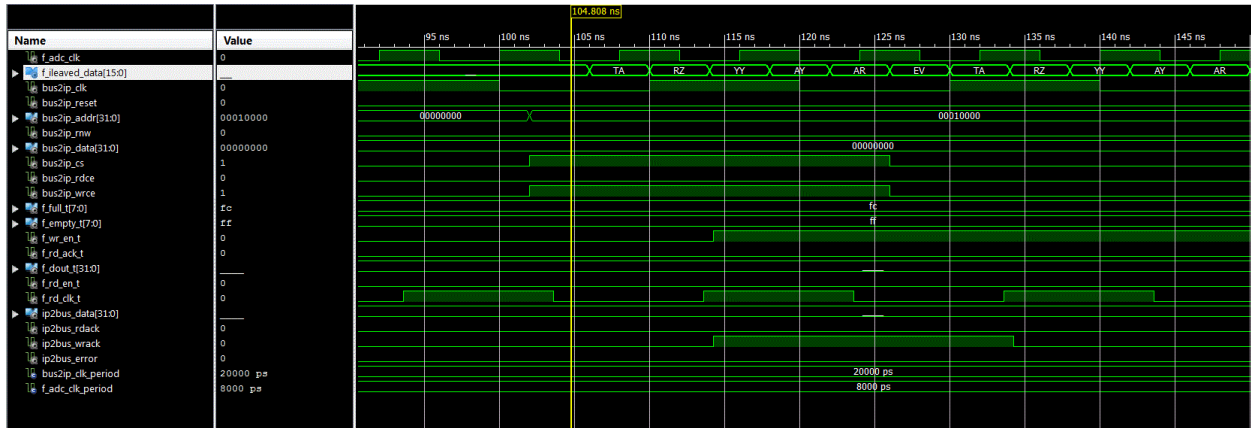


Figure 55 Post Place and Route simulation showing the serialized data from the ADC

5.7. Digital beamforming

The results of the simulations for:

- ✦ Conventional Beamformer
- ✦ Capon's Beamformer
- ✦ Linear Prediction
- ✦ MUSIC (Multiple Signal Classification)
 - ✦ Standard
 - ✦ Minimum Norm
 - ✦ Minimum Norm with Spatial Smoothing with 6 Element Sub-Array

The amount of error for each simulation is also shown.

Standard Beamformer

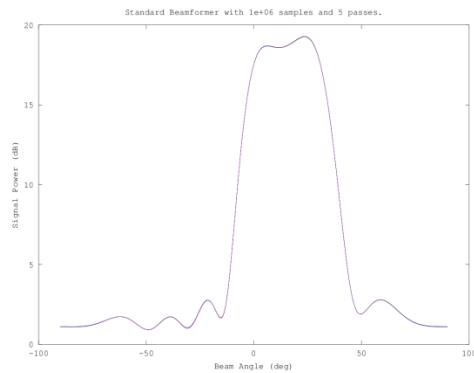


Figure 56 Standard Beamformer
Beam identification (deg)

| | | | | |
|-----------|---------|-------|--------|--------|
| Beams at: | -21.097 | 6.477 | 23.765 | 58.915 |
| Error: | 21.097 | 3.523 | 3.7646 | 28.915 |

Capon's Beamformer

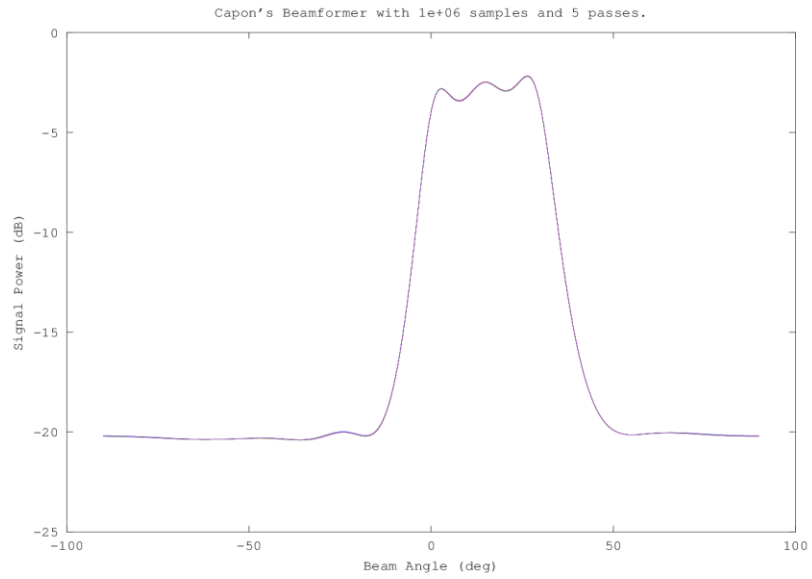


Figure 57 Capon's Beamformer

Beams at: -89.5 3.0631 15.141 26.59

Error: 89.5 6.9369 4.8586 3.4103

Linear Prediction Beamformer

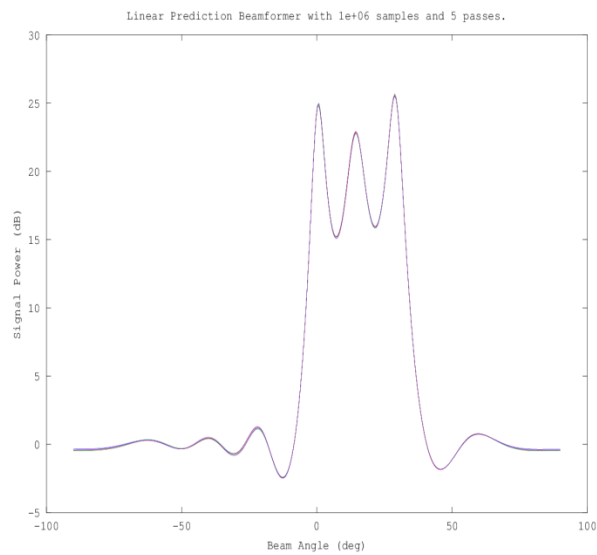


Figure 58 Linear prediction beamformer

Beams at: -21.577 0.84855 14.638 28.988

Error: 21.577 9.1515 5.3615 1.0124

MUSIC Beamformer

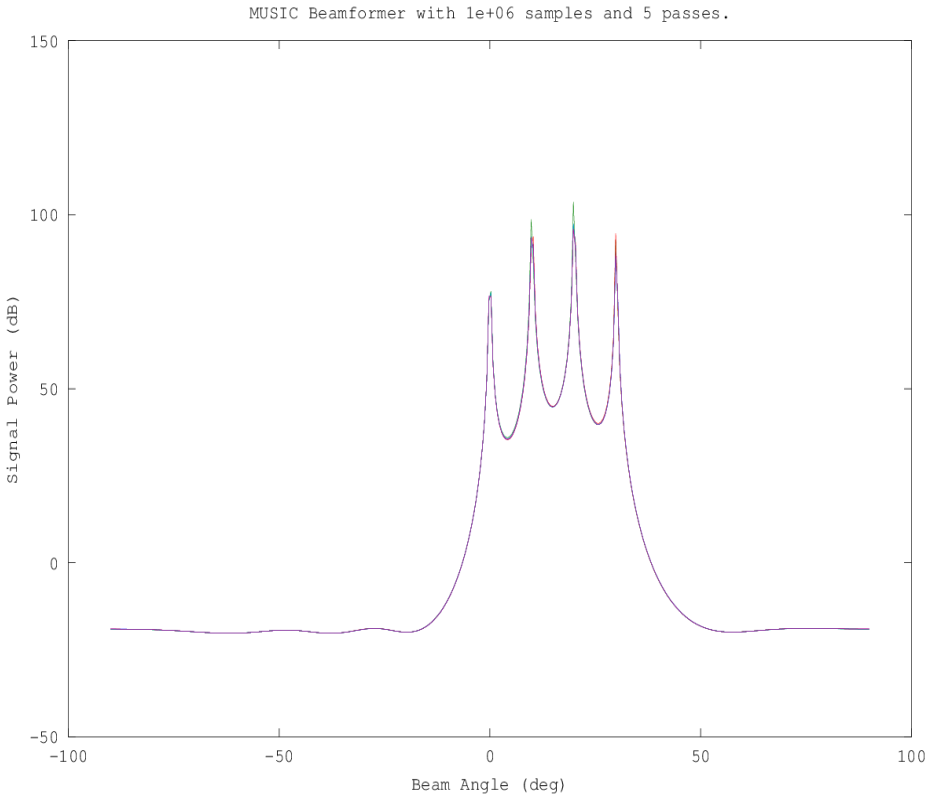


Figure 59 MUSIC beamformer
Beams at: 0.3225 10.126 20.061 30.02
Error: 0.3225 0.1263 0.0611 0.0198

MUSIC with Minimum Norm

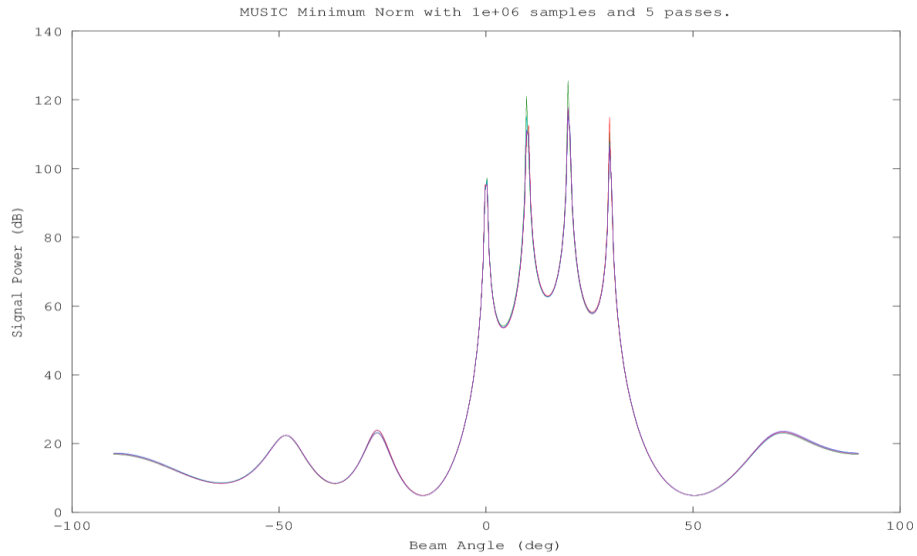


Figure 60 MUSIC with minimum norm
Beams at: 0.333 10.097 20.045 30.019
Error: 0.3339 0.0971 0.0445 0.0196

MUSIC with minimum norm and spacial smoothing

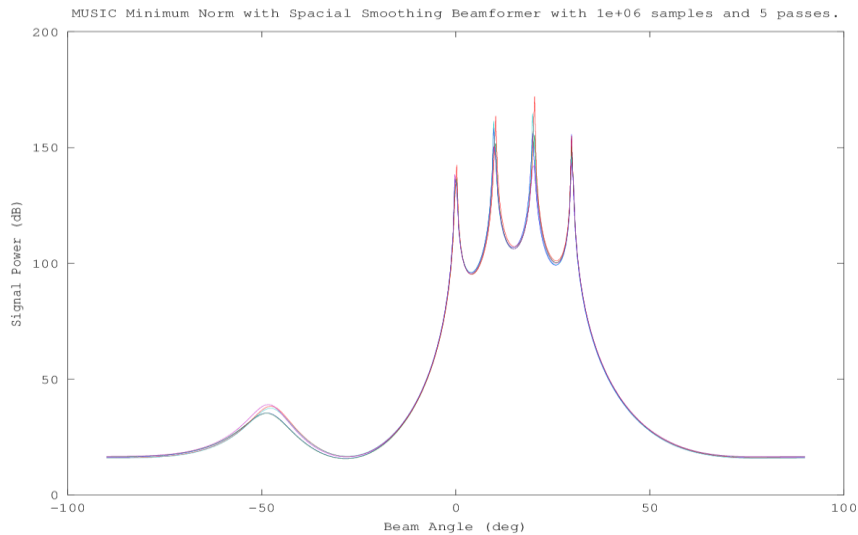


Figure 61 MUSIC with minimum norm and spacial smoothing
Beams at: 0.3305 10.185 20.382 30.014
Error: 0.3305 0.1849 0.382 0.014

All of the methods for identifying signal direction were able to identify the region in which the signals were located. The Linear Prediction method was the only one of the non super-resolution beamformers to show any significant gain on the actual signals, and in reality was still

missing on of the signals. All of the super-resolution beamformers were able to identify the signals with surprising accuracy and very high gain. Performing spatial smoothing had little impact on the results as the signals were all uncorrelated, however having the ability to deal with a multi-path environment would be imperative for locating cellular signals inside of a building as was the goal of this project. While the MUSIC methods avoid having to directly perform matrix inversion that are computationally complex, it does require that both eigenvalues and eigenvectors be computed for the Spatial Covariance Matrix, which is also a computationally complex task.

The Model Order determination was less effective than desired, while averaging over the 5 passes it was able to identify the correct order of 4, there was an instance of identifying 5 and another identifying 6 signals. Looking at the AIC plot, it appears that the cost function may not be high enough, after the sharp roll off the cost does not increase fast enough as model order increases.

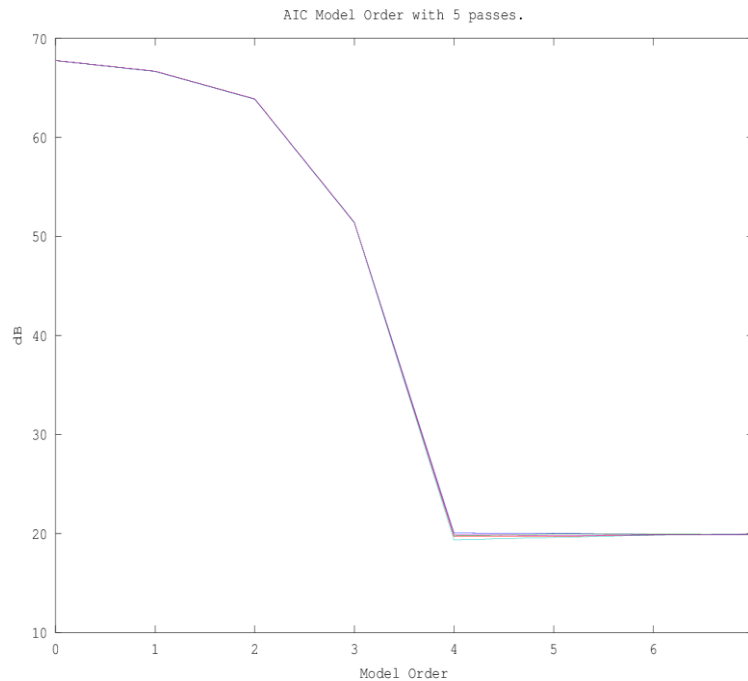


Figure 62. ATC Model Order with 5 passes

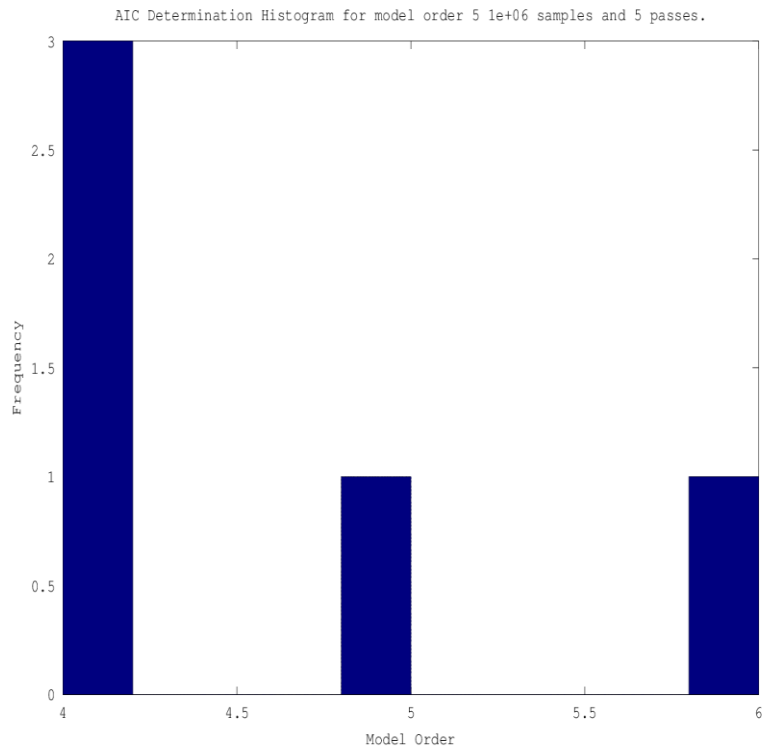


Figure 63. AIC Determination Histogram for model order

5.8. Value analysis

The following table outlines the cost of our project:

| Analog Components | Price | Quantity | Total Cost |
|---------------------|-------------|----------|------------|
| LNA | \$30 | 16 | \$480 |
| IF board | \$20 0 | 4 | \$800 |
| Filters | \$20 0 | 1 | \$200 |
| Radiators | \$11 0 | 10 | \$1,100 |
| Cables, adaptors... | \$10 | 50 | \$500 |
| FPGA | \$1,0 00 | 1 | \$1,000 |
| | | | |
| Total | | | \$4,080 |

Clearly, the cost is less than half of the cost that we expected to spend for the project. Therefore, we met the cost requirements that were outlined in our literature review. It is also important to emphasize that we used various discounts that lowered the cost of the overall design. Even though, if we include the full price, it would be still significantly lower than \$10,000 that we set as our upper limit.

Chapter 6 Conclusion:

In this project we have achieved most of the stated objectives: we have designed the proposed architecture, capable of estimating the direction of arrival. Having designed each piece, we manufactured/obtained all of the necessary RF and analog hardware for the eight channels of our design. We have also completed the interface from the analog cards to the digital FPGA domain, as well as the hardware in the FPGA. We have completed a number of simulations proving the concept of digital beamforming, yet we have not performed beamforming on experimental data, which we suggest for future work. Additionally, we have completed and tested every major piece of the design. Major portions of the design were tested and proven to perform as required by the initial specifications that we constrained our design to meet. For additional future work we recommend the full integration of the major pieces of our design. Integration of the analog cards to the digital domain would be necessary, as well as the integration of the digital hardware with the signal processing software. Since each block has been rigorously tested as specified in the previous sections of this paper, we do not anticipate major bugs in combining the portions of the project, yet we do anticipate significant amount of time that will be required to accomplish that, hence the recommendation of full integration for future work on this project. We believe that the proposed architecture shows some empirical proof of concept and that more rigorous proof can be obtained once the system is fully assembled by a future team. With this we would like to summarize our design and invite the reader to evaluate additional resources in the appendices.

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Appendix A

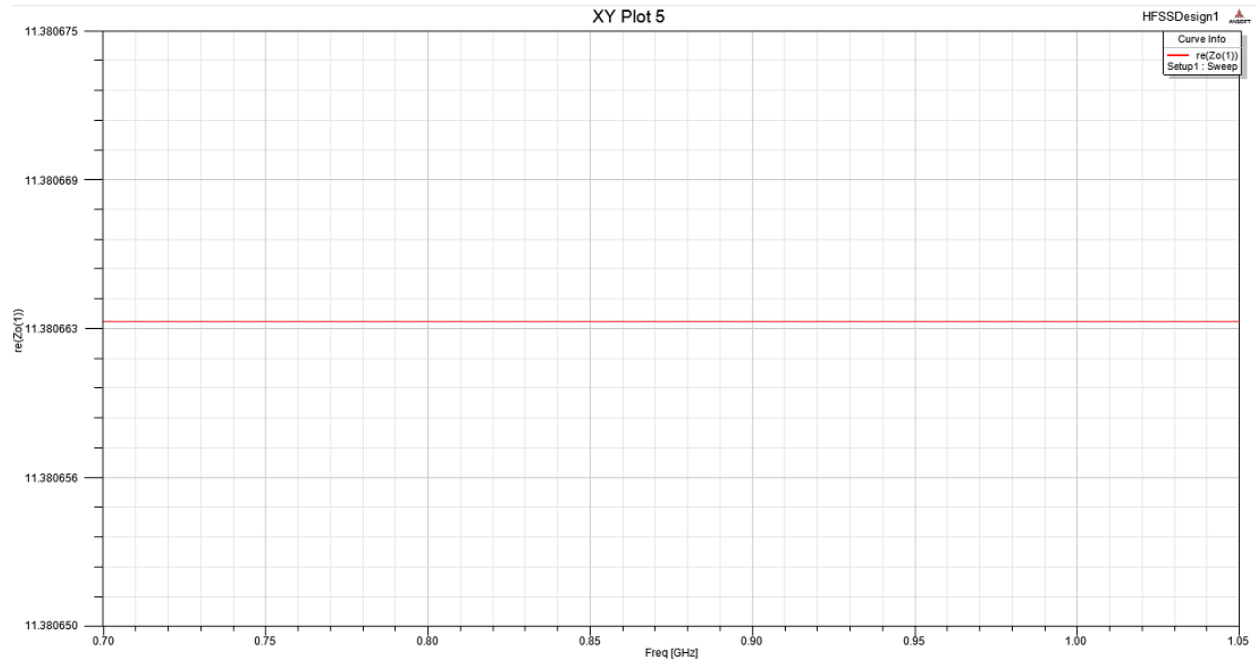


Figure 64. Impedance of the stripline during step 1

Appendix B

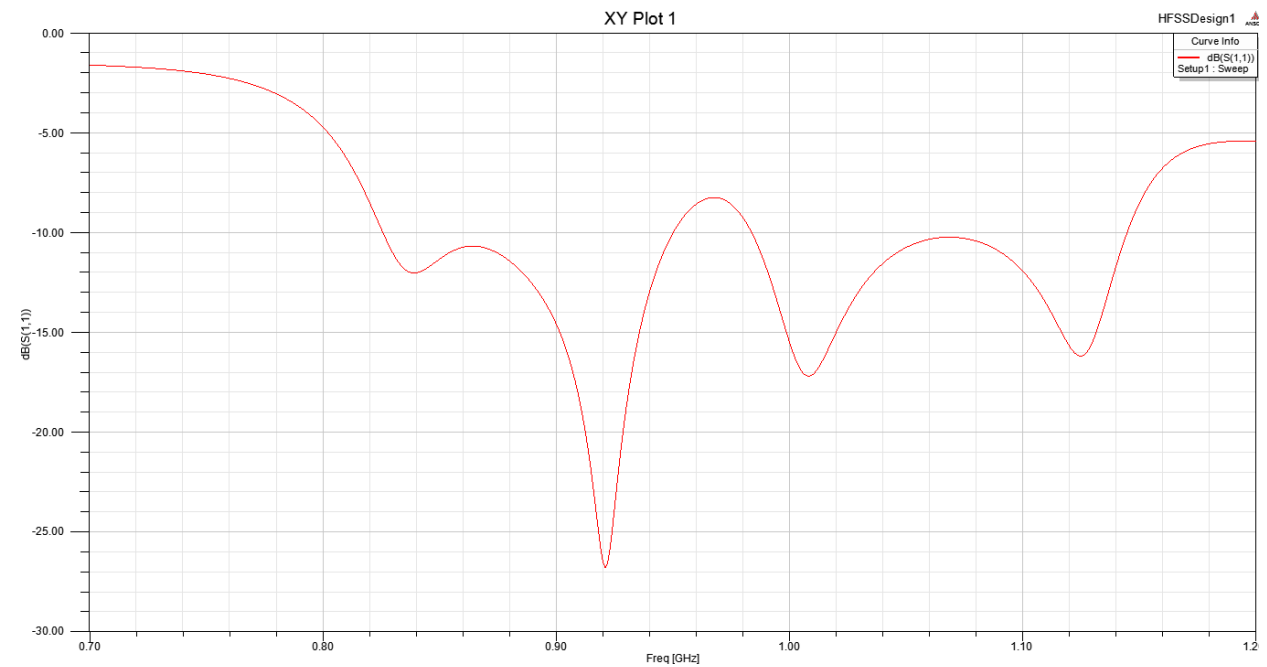


Figure 65. S11 vs. frequency during the step 2

Appendix C

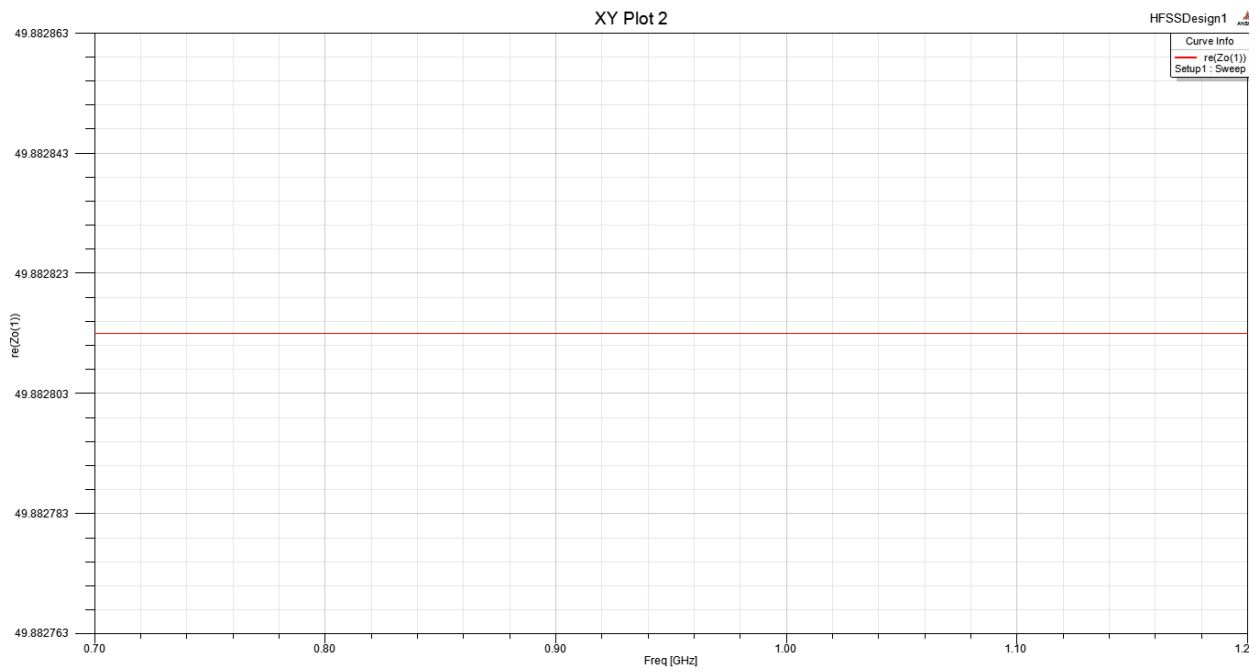


Figure 66. Impedance of the wave port after making a lambda quarter transformer

Appendix D

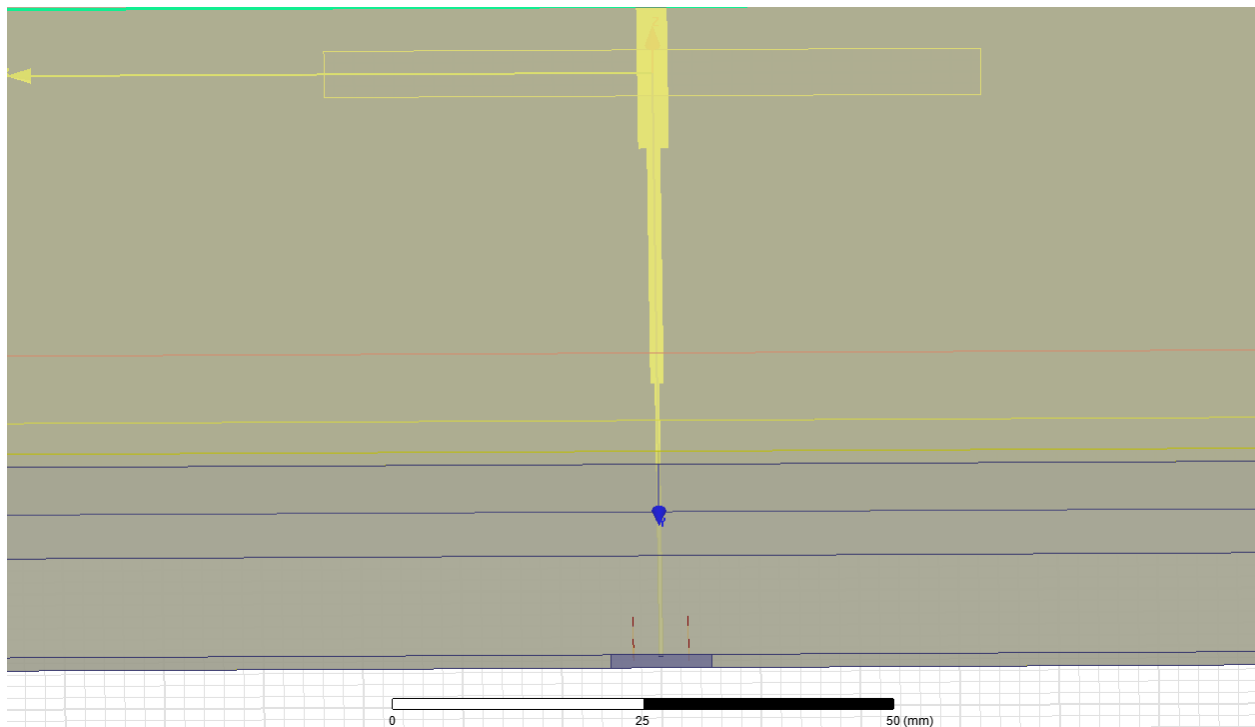


Figure 67. Lambda quarter transformer inside the aluminum box

Appendix E

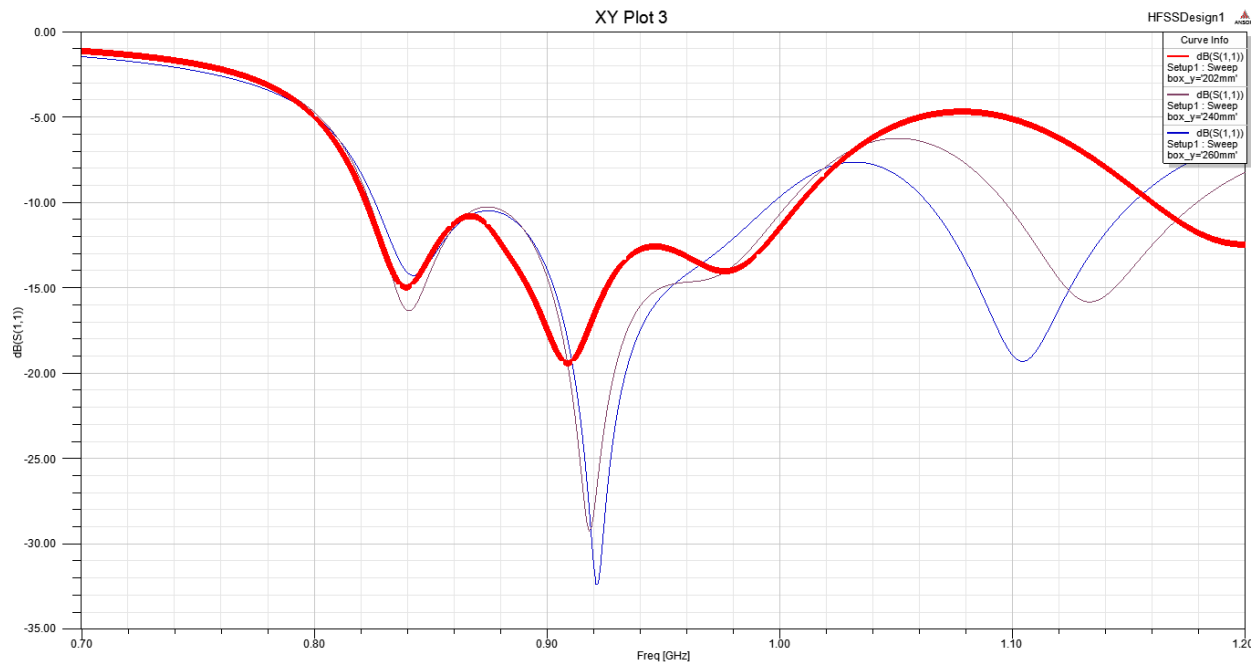


Figure 68. S11 vs. frequency during step 3

Appendix F

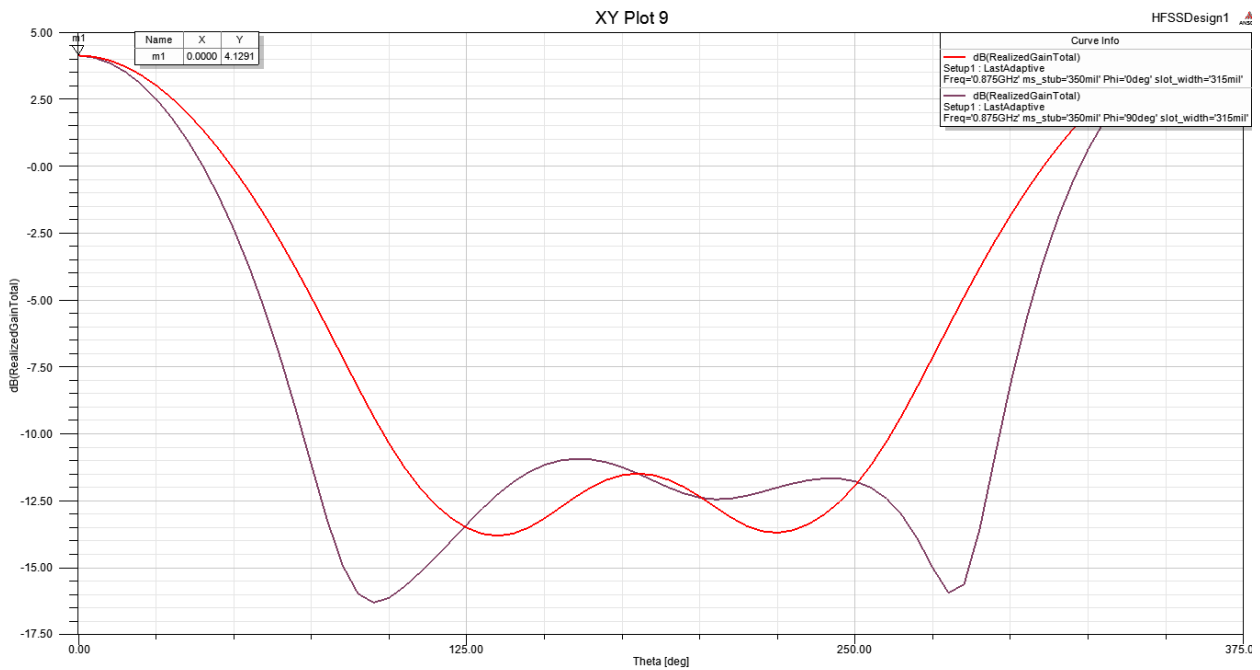


Figure 69. Realized gain of the final design at 0 degrees and 90 degrees

Appendix G

| Name | Theta | Ang | Mag |
|------|----------|---------|--------|
| m1 | 360.0000 | -0.0000 | 4.1291 |

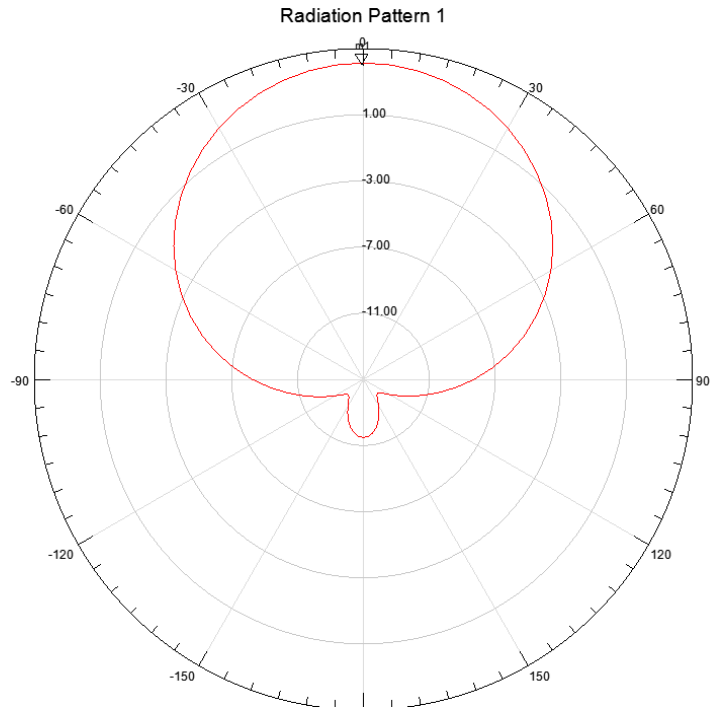


Figure 70. Radiation pattern of our antenna, showing that there are no back lobes.

Appendix H

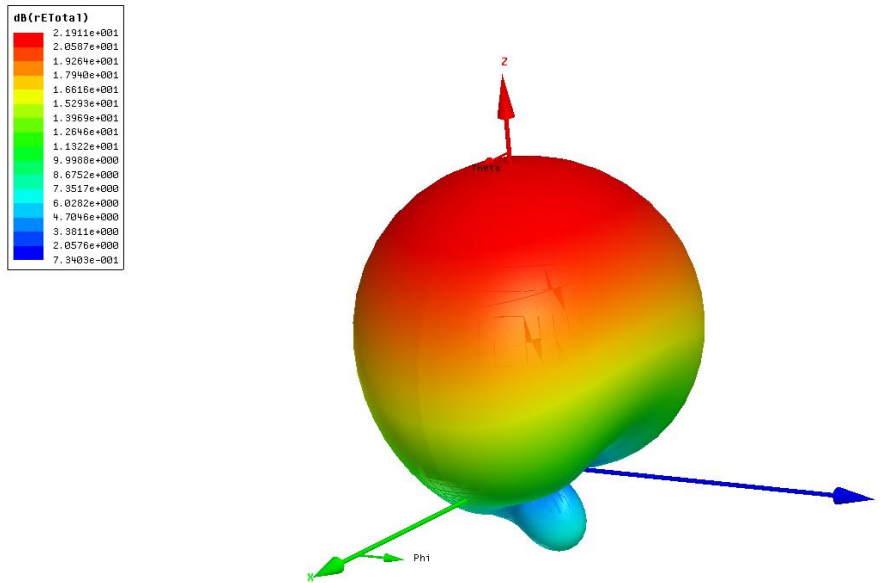


Figure 71. 3D caption of realized gain of our antenna

Appendix I

Table 5. Parameters in Antenna design

| Name | Value | Unit | Evaluated Value |
|--------------------------------|-----------|------|-----------------|
| ms_width | 118 | mil | 118mil |
| ms_length | box... | | 87.8205mm |
| slot_length | 2600 | mil | 2600mil |
| slot_width | 315 | mil | 315mil |
| move_slot | 0 | mm | 0mm |
| substrate_height | 63 | mil | 63mil |
| patch_width | 129 | mm | 129mm |
| patch_length | 134 | mm | 134mm |
| box_x | 250 | mm | 250mm |
| box_y | 202 | mm | 202mm |
| box_z | 250 | mm | 250mm |
| Height_of_additional_substrate | 6 | mm | 6mm |
| Wall_thickness | 300 | mil | 300mil |
| box_in_width | 6 | in | 6in |
| box_in_length | 6 | in | 6in |
| box_in_height | 437.5 | mil | 437.5mil |
| FR4_2layer | 1/16 | in | 0.0625in |
| FR4_4layer | 63 | mil | 63mil |
| box_width | box... | | 167.64mm |
| box_length | box... | | 167.64mm |
| ms_stub | 350 | mil | 350mil |
| ms_feed | stripl... | | 17.18mm |
| striplineY_offset | box... | | 17.18mm |
| ms_height_offset | 10 | mil | 10mil |
| Drill_radius | 32 | mil | 32mil |
| y_drill_offset | 30 | mil | 30mil |
| x_drill_offset | 5 | mil | 5mil |
| epsilon | 4.4 | | 4.4 |
| xport_offset | 3.1 | in | 3.1in |
| box_y_wide1 | box... | | 363.36mm |
| lambda_quarter | 40.8... | mm | 40.862mm |
| stripline2_width | 50 | mil | 50mil |
| Ohm50length | stripl... | | 39.818mm |
| stripline3_width | 15 | mil | 15mil |
| ms1_depth | 2.8 | in | 2.8in |
| signal_radius | 50 | mil | 50mil |
| signal_offset | 300 | mil | 300mil |
| signal_radius_out | 100 | mil | 100mil |
| via_radius | 30 | mil | 30mil |
| radius_coaxial | 80 | mil | 80mil |