Worcester Polytechnic Institute
Digital WPI

Major Qualifying Projects (All Years) | Major Qualifying Projects

June 2008

Class D Audio Amplifier

Jayce Silvia
Worcester Polytechnic Institute

John Durst
Worcester Polytechnic Institute

Justin Cox
Worcester Polytechnic Institute

Follow this and additional works at: https://digitalcommons.wpi.edu/mqp-all

Repository Citation

Silvia, J., Durst, J., & Cox, J. (2008). *Class D Audio Amplifier*. Retrieved from https://digitalcommons.wpi.edu/mqp-all/3311

This Unrestricted is brought to you for free and open access by the Major Qualifying Projects at Digital WPI. It has been accepted for inclusion in Major Qualifying Projects (All Years) by an authorized administrator of Digital WPI. For more information, please contact digitalwpi@wpi.edu.

CLASS D AUDIO AMPLIFIER

A Major Qualifying Project Report:

submitted to the Faculty

of the

WORCESTER POLYTECHNIC INSTITUTE

in partial fulfillment of the requirements for the

Degree of Bachelor of Science

by

____

Justin Cox

____

John Durst

____

Jayce Silvia

Date: April 20, 2008

Approved:

____

Professor Stephen J. Bitar, Advisor

Abstract

This project consisted of the design, construction, and comparison testing of two implementations of analog pulse-width modulation Class D audio amplifiers. The main goal of the project was to maximize the efficiency of the amplifier designs while maintaining a high-power, low-noise output signal. PCB testing confirmed that the amplifiers met our goals of greater than 90% efficiency, less than 1% total harmonic distortion and greater than 50 W output power.

Table of Contents

Table of Figures

Table of Tables

Table of Equations

1. Background

1.1. What is Class D?

Class D audio amplifiers are used to amplify audio signals. They are sometimes called switching amplifiers, as they contain switches which play a key role in the amplification of the signal. The amplified signal is filtered to smooth out the audio, removing any undesired noise.

Class D amplifiers use modulation techniques to convert the input signal to a sequence of pulses. A pulse frequency of greater than ten times the highest frequency in the input signal is typically used. The output pulses have a fixed amplitude, allowing the transistors to switch on and off quickly. The result of this is significantly smaller power dissipation compared to linear audio amplifiers. Class D amplifiers have a theoretical efficiency of 100%, but efficiencies in the range of 80% to 95% are common [1].

Figure 1.1 shows the schematic of a typical class D amplifier [2]. The input signal is compared to a triangle wave, producing a square wave. This square wave is the input for the switching controller and output stage which drives the controller. For an analog Class D, the input signal information is encoded into the width of the square wave pulses.

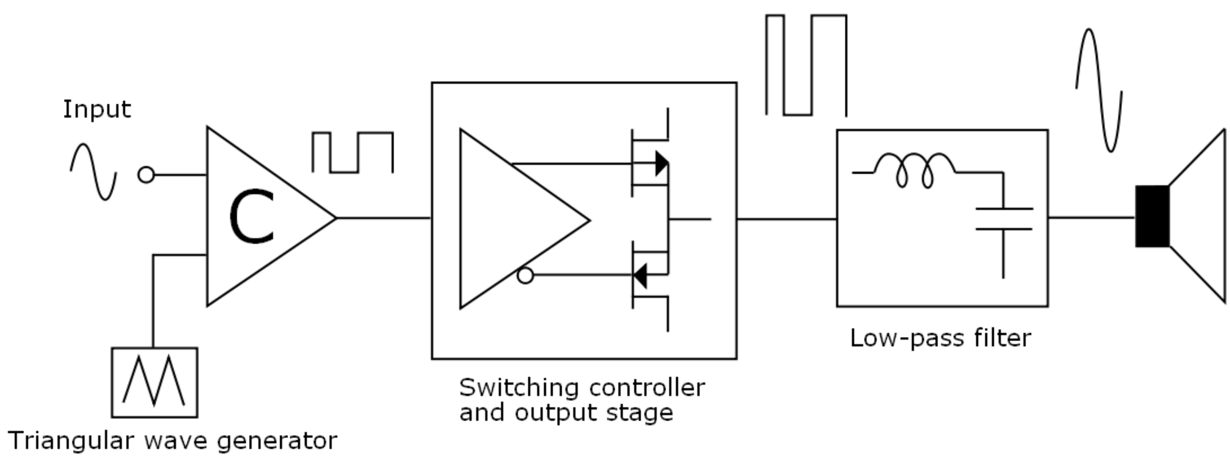


Figure 1.1 Class D Diagram

One disadvantage of high-power Class D is the need for a filter. A LC filter will significantly add cost and board space to a design. In low-power devices, the filter can cost more than the rest of the

[1] (Moreno, 2005)
[2] http://upload.wikimedia.org/wikipedia/en/4/4c/Pwm_amp.svg

amplifier circuit, making it a poor investment. A filter-less design can be used to address this concern, no filter leads to smaller board space and less cost. Unfortunately, a filter-less design can also lead to unwanted electromagnetic interference, or EMI [3].

1.1.1. Other Classes

Other classes of audio amplifiers have their strengths and weaknesses as well. While there are over ten classes of electronic amplifiers, the three most common audio amplifier classes, in addition to class D, are: A, B, and AB [4].

Class A amplifiers utilize the whole input signal so that the output is a scaled-up version of input. The transistor is biased so the device is always conducting. If there is no input, power is still drawn from the power supply. This is a major loss of power, and the main reason for Class A's inefficiency. A maximum of 50% efficiency is theoretically possible, although typical values range from 20% to 50%. Figure 1.2 displays a typical Class A amplifier [5]:

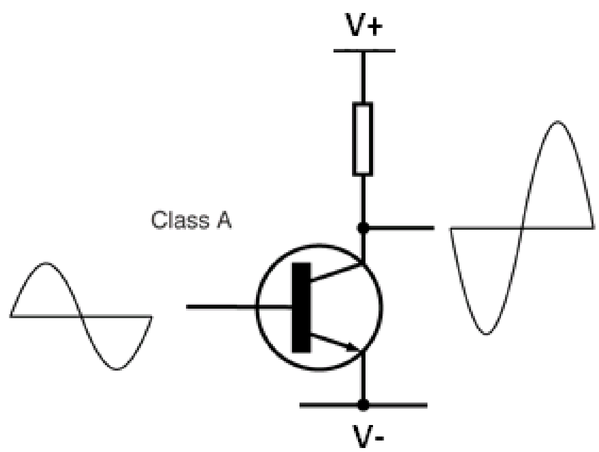


Figure 1.2 Class A Diagram

[3] (Gaalaas, Sound advice on Class D audio amps designs, 2007)
[4] (Electronic Amplifier, 2007)
[5] http://upload.wikimedia.org/wikipedia/en/9/9b/Electronic_Amplifier_Class_A.png

Class B amplifiers amplify only half of the input wave. The transistor is switched off half the time, stopping all power loss during that time. This creates distortion, but also increases efficiency compared to Class A. Class B amplifiers' efficiency are much higher than Class A, up to a theoretical 78.5%. Figure 1.3 shows the functionality of a Class B amplifier [6]:

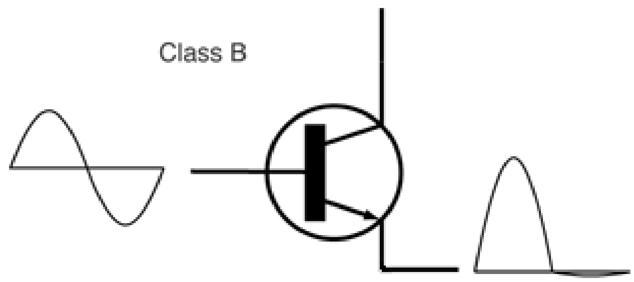


Figure 1.3 Class B Diagram

A "push-pull" configuration, shown in Figure 1.4 can be used to increase efficiency. Complimentary devices are uses to amplify opposite halves of the input and recombine them at the output [7]. One drawback of this configuration is the creation of crossover distortion, an undesired output created at the point where the amplifier switches between the two devices.

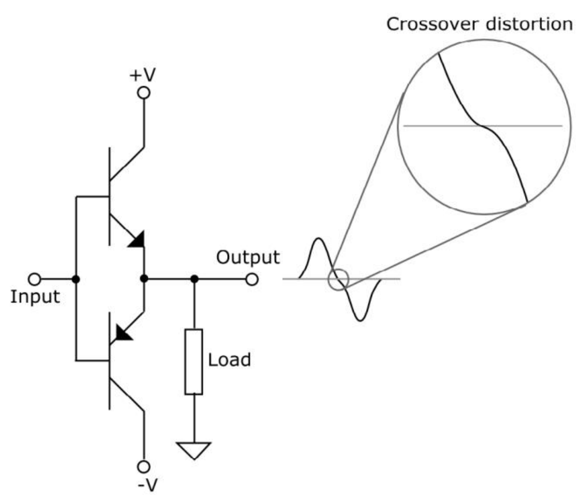


Figure 1.4 Class B Push-Pull Configuration with Crossover Distortion

---

[6] http://upload.wikimedia.org/wikipedia/en/b/b6/Electronic_Amplifier_Class_B_fixed.png
[7] http://en.wikipedia.org/wiki/Image:Crossover_distortion.png

Class AB amplifiers have characteristics of both Class A and Class B amplifiers. As shown in Figure 1.5, the output is non-zero for the negative half of the waves [8]. This is implemented by biasing the device on, instead of off, while it is not in use. When connected in a push-pull configuration, crossover distortion is reduced due to the devices non-zero value when not in use. This technique provides the output with anywhere from 50% to 100% of the input signal. Because the devices are non-zero for half of the waveform, class AB has less efficiency than class B; therefore it has a theoretical efficiency less than 78.5%. Common class AB amplifiers have efficiencies between 35–55% [9].

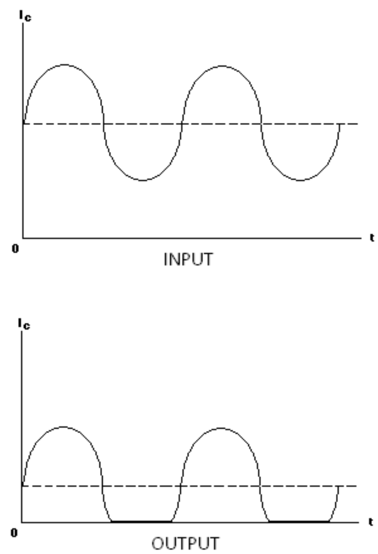


Figure 1.5 Class AB Diagram

1.1.2. Common applications

Class D amplifiers can be found in any market demanding small size, low standby current, and high power efficiency. Power consumption decreases battery life and play time in portable applications. New amplifier circuits are being designed for cell phones, hearing aids, personal digital assistants (PDAs), and other battery powered devices with audio capabilities [10].

There is a market for high efficiency automotive audio as well. High efficiency is desired for enthusiast automotive applications due to the high power demand (sometimes over 1000 watts) and limited power supply. The greater efficiency allows the amplifier to run much cooler without extra fans or ventilation to prevent overheating.

---

[8] http://www.uoguelph.ca/~antoon/tutorial/xtor/xtor1/1fig5.gif
[9] (Amplifier, 2007)
[10] (Lynch, 2001)

Home audio does not have as much need for energy efficient devices as the portable or automotive markets. This is due to the relatively low cost of electricity in homes. Class D amplifiers are used in some home audio devices, but the portable and automotive markets are far larger.

1.1.3. Market Share

As of January 2006, there are at least 108 varieties of Class D audio integrated circuits. The four major manufactures of Class D ICs are [11]:

- Texas Instruments – 41% of market share
- Phillips – 14% of market share
- Maxim – 13% of market share
- National Semiconductor – 11% of market share

All of these major manufacturers offer Class D amplifiers in single-chip IC solutions which are then sold to manufacturers of electronic devices. The small size and low cost of these chips make them attractive but not very user-friendly for the Do-It-Yourself electronic hobbyist. However, test boards and Class D amplifier "kits" are also available for end users.

1.2. Design Considerations

This section is a survey of available technologies for each fundamental stage of a Class D amplifier product. Where applicable, charts and figures are included to summarize and compare various techniques or concepts. One of the critical stages of any new product design is the research done to understand current market trends and what technologies are commonly implemented in currently available products. Many of the design specifications stated in Section 2 were decided upon based on the design considerations documented here.

1.2.1. Half Bridge vs. Full Bridge

One of the critical decisions that must be made for a Class D amplifier design is the choice of the output power stage. This choice defines how the power flows from the amplifier to the load, and also defines the level of switching (two or three-level) that can be used. The half-bridge stage ties the load between two voltage levels. The PWM signal drives the two switches depending on the duty cycle

---

[11] (Class D Audio Amplifier IC Market Report 2005-2006, 2006)

output by the PWM stage. The two switches can be connected to V+ and Ground, or V+ and V- in a dual-supply application. Figure 1.6 shows an example of a half-bridge configuration.

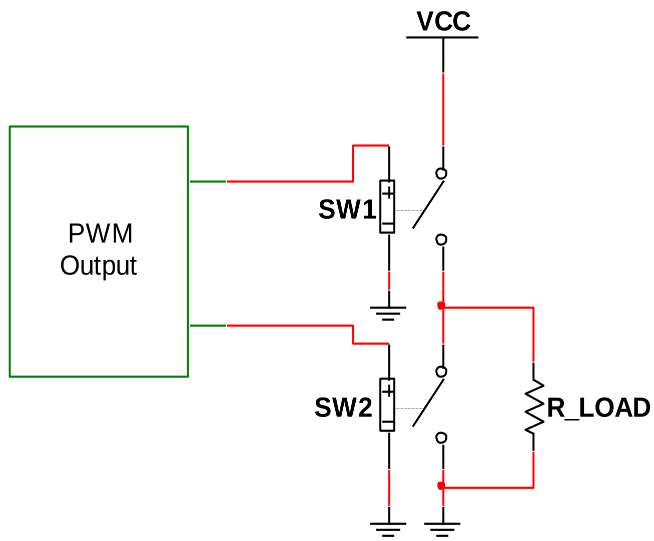


Figure 1.6 Half Bridge With Connected Load Schematic

The half-bridge configuration is attractive for several reasons. Firstly, the half-bridge can achieve efficiency levels of greater than 90% in low power applications, partly due to the low switching losses. Having two power switches also saves valuable PCB space in a low-power design such as a portable media player or laptop where space is a significant factor in component selection. Furthermore, overall component costs are kept low with a half-bridge due to the fact that only two switches and a single filter is required at the output [12].

Despite its many advantages, the half bridge is not an ideal solution. Due to the nature of the two-level switching, when under single supply operation the load experiences a DC offset consisting of the average of the switching from the supply voltage and ground level. The solution to this, placing DC blocking capacitors to shield the load, is bulky, adds component costs, and may increase distortion in the output signal due to the filtering nature of capacitors. When operating from dual supply rails, the switches must idle at a 50% duty cycle when the output is near zero in order to achieve an average voltage level of zero at the load. This results in unnecessary switching near the zero crossing that wastes power. Lastly, the flow of power in the half-bridge results in a "pumping" effect that causes variations and spikes in the supply voltage.

---

[12] (Maxim Engineering Journal Vol. #59, 2007)

A full bridge, on the other hand, consists of a load connected between two pairs of switches. This configuration is also called Bridge-Tied Load, or BTL for short. Using four switches allows 3-level PWM (the load can be connected to V+, V-, or Ground) which results in power savings, since the drive stage doesn't have to idle at 50% duty cycle when the audio signal is small. The full bridge configuration is displayed in Figure 1.7.

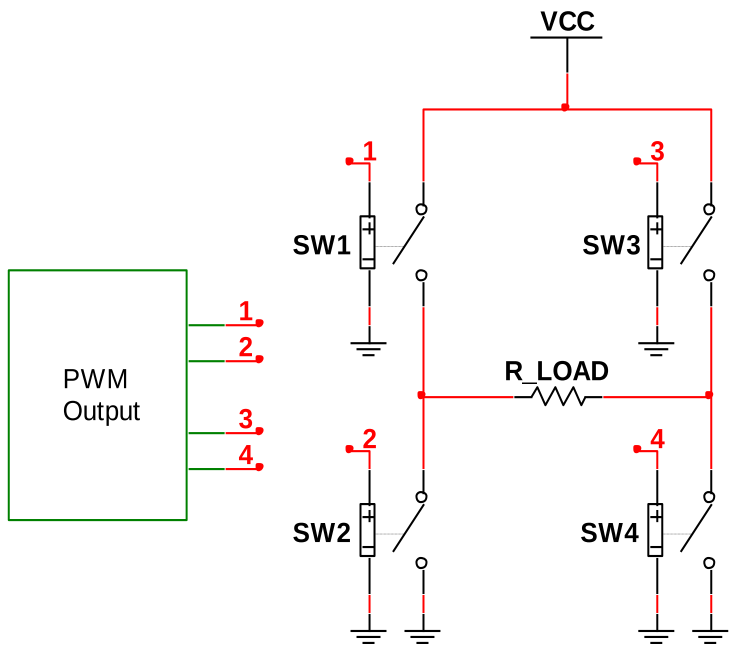


Figure 1.7 Example BTL configuration

Why is the full bridge a popular alternative? To begin, the Class D full bridge has significantly higher efficiency than its Class AB BTL counterpart. While overall efficiency is slightly lower than the half bridge for high-power applications, at low power levels (under 10 W) the two are relatively close [13]. The full bridge design also enables the designer to implement three-level switching, further reducing switching losses compared to the half bridge.

[13] (Maxim Engineering Journal Vol. #59, 2007)

The full bridge can also achieve twice the output voltage swing of the half bridge when the load is driven differentially. This results in the ability to theoretically deliver four times the power using the same supply [14]. For portable applications, the ability to deliver more power while keeping switching losses low makes the full bridge a favorable option.

1.2.2. Two-level vs. Three-level PWM

One important design choice for Class D amplifiers is the decision to include multi-level switching. In a typical two-level application, the load may experience one of two voltage levels. In a single-supply half-bridge design, therefore, the load will experience a DC average voltage equal to half the supply voltage for a 50% duty cycle (zero-input situation). For a full-bridge two-level design, the load will not experience a DC offset, but the unnecessary switching at 50% duty cycle remains.

A three-level (full bridge) switching scheme allows the designer to apply three voltage levels to the load: the positive and negative supply voltage or ground (zero voltage). This scheme has the additional benefit of minimizing the switching losses in the power MOSFETs for input voltages near zero where the duty cycle would otherwise be near 50%.

1.3. MOSFETs vs. BJTs

Another important decision to be made for our design is to choose switches for the power output stage of the amplifier. Due to the nature of Class D technology (see Section 1.1), several requirements for the switches are immediately apparent:

- Fast switching time
- Low ON resistance
- Low gate driving current
- High current delivery capability
- Large reverse voltage tolerance

According to Eric Gaalaas, the selection of a switch is often a balance between power losses resulting from the ON resistance and power losses resulting from gate capacitance [15]. Switching losses caused by the charge and discharge of gate capacitances increase proportionally with switching frequency. This means that higher switching frequencies are not necessarily better for efficiency, even if

---

[14] (Maxim Engineering Journal Vol. #59, 2007)
[15] (Gaalaas, Class D Audio Amplifiers: What, Why, and How, 2007)

they reduce the component size of the output filter. For a Class D amplifier, the switching speeds will be well in excess of the Nyquist rate for the input audio signal; therefore, for an audio band defined up to 20 kHz, the switching frequency must be at least 40 kHz for the amplifier to operate at all. Manufacturers typically attempt to minimize the $R_{ON} \times C_G$ product for each switch in order to achieve maximum power savings.

While MOSFETs have replaced BJTs in many applications due to their fast switching times, in the world of consumer audio things are slightly different. BJTs are commonly used in Class A and Class AB amplifiers for their large current handling capabilities and "warm sound". MOSFETs also have fast switching times, often in the nanosecond range for modern devices. MOSFETs are often preferred for applications involving high power due to their ability to withstand simultaneous application of high voltage and high current without breakdown [16]. In high frequency applications, however, BJTs are sometimes selected due to their low gate capacitance, which means that they may be driven at high frequencies by devices which cannot source significant amounts of current [17]. This makes BJTs an attractive option for very-high-frequency applications such as wireless communications.

While Bipolar Junction Transistors can handle higher collector-emitter currents than MOSFETs, they are by their nature current-controlled devices. The current flow from collector to emitter is proportional to the small current flowing from base to emitter. This means that turning on a BJT requires current to be flowing between the base-emitter junction, which typically has a forward voltage drop of approximately 0.7 V. The current flow results in power loss, especially when the BJT is used as an amplifier and the turn-on current must be supplied almost continually to the switch.

In contrast to the BJT, the MOSFET is not a current-controlled switch. Rather than supplying a base-emitter current to turn on the device, when driving a MOSFET the tiny gate capacitance must be charged by a voltage at the gate (voltage-controlled switch). While the charging and discharging of the gate capacitance results in power losses, these losses are significantly smaller than the power dissipated by a Bipolar Junction Transistor under similar operating conditions. The high input impedance of the MOSFET also enables the designer to drive several switches with the same voltage source if necessary. However, the MOSFET requires significantly more voltage in order to turn on, typically between 4-5 V. Compared to the 0.7 V required by the PN junction of an NPN BJT, this is more demanding for the driving circuit. MOSFETs can operate at high switching frequencies in the MHz range, but the drivers

---

[16] (Barkhordarian)
[17] (Gaalaas, Class D Audio Amplifiers: What, Why, and How, 2007)

must be able to supply the turn-on voltage and gate charge quickly enough for the switches to operate properly.

The comparison charts below summarize the advantages and disadvantages of each technology.

Bipolar Junction Transistors (BJTs)	
Advantages	***Disadvantages***
High current handling capability	Current-controlled switches (larger switching loss)
Low forward voltage drop (0.7 V typical)	Thermal runaway possible
Small gate capacitance	

Table 1.1 BJT Advantages And Disadvantages

Metal Oxide Silicon Field Effect Transistors (MOSFETs)	
Advantages	***Disadvantages***
Primarily voltage-controlled switches	Susceptible to ESD damage
High input impedance	Low breakdown voltage
No thermal runaway (resistance not temperature-dependant)	Gate-source capacitance
Large fan-out capability	Large on resistance
Medium current handling capability (can also be combined in parallel)	Requires 4-5 V for turn-on
Fast switching behavior (MHz and above)	

Table 1.2 MOSFET Advantages And Disadvantages

Other switching devices, such as IGBTs (which combine a MOSFET and BJT) have somewhat different characteristics. The IGBT, for example, uses the fast switching speed of the MOSFET to control a BJT, which handles the current sourcing. This configuration has its limitations, however, since the power loss in an IGBT device is significantly higher than the power loss for a single switch.

1.3.1. MOSFET Selection parameters

As an initial investigation into the capabilities of current MOSFET technology we went through several companies' catalogs of available MOSFETs. A list of the links to the data sheets of these MOSFETs is located in Appendix B. We chose several promising MOSFETs of varying rated current capacities to get an idea of what is possible at this juncture in time at several possible power levels. We than compiled a table of several key component characteristics for ease of comparison.

I_D [A]	$C_{iss} + C_{oss}$ [pF]	R_{DS} typical [mΩ]
0.7	280	350
0.85	100	500
0.85	159	400
1	156	480
5	310	130
5.8	810	50
6.6	1650	40
9.2	265	137
11	1940	12
15	3200	4.6
25	7050	1.8
60	5700	4
75	4670	7.2

Table 1.3 Max I_D vs. Capacitance and Expected R_{DS}

Table 1.3 enabled us to see that there is a tradeoff between gate capacitance and the drain to source resistance, $R_{DS(on)}$, of the device while it is on. Typically, the higher the sum of the input and output capacitances, the lower the $R_{DS(on)}$ of the MOSFET. There also there appears to be a correlation between the values of the maximum drain current, I_D , the $R_{DS(on)}$ and the total gate capacitance. As the device's capability to handle drain current increases, $R_{DS(on)}$ decreases while the total gate capacitance grows larger. This is to be expected, since larger current handling capability also demands a low $R_{DS(on)}$ in order to minimize switching power losses.

1.4. Battery Selection

Another important consideration that we must take into consideration is the power supply. The power supply in our application will be one that we as designers will have very little control over. Therefore, we must adapt our design to meet the specifications of currently established power sources. In our design we will have to make a tradeoff between output power and battery lifetime. Batteries are rated by amp hours (the amount of time the battery can source a given current) and output voltage. Table 1.4 displays the typical characteristics of several types of commonly available batteries [18]:

---

[18] (Appendix C)

Class	Battery Name	Voltage [V]	Capacity [mAh]
AA	EN91	1.5	2850
AAA	EN92	1.5	1250
C	EN93	1.5	8350
D	EN95	1.5	20500
9V	EN22	9	625

Table 1.4 Battery Class And Associated Parameters

The batteries in Table 1.4 are typical alkaline battery voltages. For portable applications, designers often utilize higher energy-density batteries such as Lithium Ion technology. In the laptop market, 3.6V Lithium Ion cells are combined to yield batteries ranging from 10.4V to 14V and higher. When designing it will be necessary to select one of the available power supplies and attempt to model it as accurately as possible. Besides voltage and current parameters, the series resistance of the voltage supply may also need to be taken into consideration.

1.5. Modulation Techniques

Modulation is the process of varying a periodic waveform through the use of another signal [19]. Class D amplifiers use pulse modulation methods to help achieve their high efficiency. Two types of modulation were investigated: pulse-width modulation, and pulse-density modulation.

1.5.1. Pulse-width Modulation

Pulse-width modulation (PWM) utilizes a square wave which is modulated based on the average value of the input signal. A common way to generate a PWM signal is with a sawtooth or triangle wave that, using a comparator, is compared with the original signal.

PWM systems are often used to control switches. The state of the switches is controlled by the square wave. The discrete nature of a PWM signal helps to increase efficiency as the switches stop current while they are off and have no voltage drop across them when on, reducing power loss [20]. Figure 1.8 shows how a PWM signal is created by comparing a sine wave to a sawtooth wave [21]:

[19] (Modulation, 2007)
[20] (Pulse-width modulation, 2007)
[21] http://upload.wikimedia.org/wikipedia/commons/a/af/Pwm.png

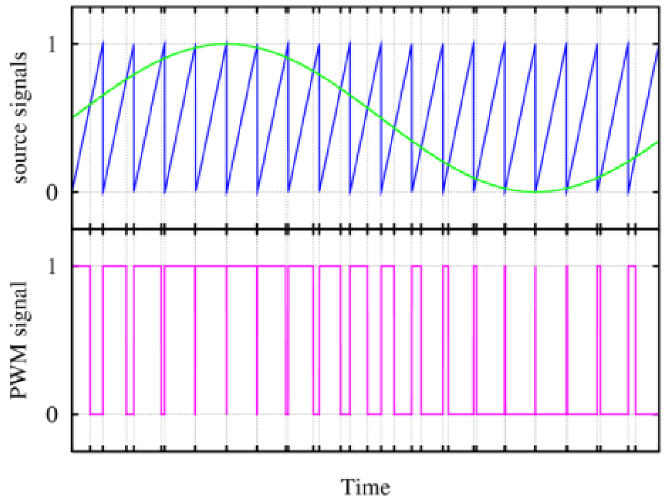


Figure 1.8 Typical Pulse-width Modulation Signal

1.5.2. Pulse-density Modulation

Pulse-density modulation (PDM) is a modulation technique used to represent an analog signal in the digital domain. Encoded is the density of the pulses corresponding to the analog signal's amplitude. More logic high pulses in a region of time means higher amplitudes. Inversely, more logic low pulses in a region of time means lower amplitudes.

A PDM signal is encoded from an analog signal through the process of delta-sigma modulation. Delta-sigma modulation quantizes the signal into 1's or 0's depending on the amplitude of the analog signal [22]. Figure 1.9 shows the quantized signal (blue representing '1' and white representing '0') [23]:

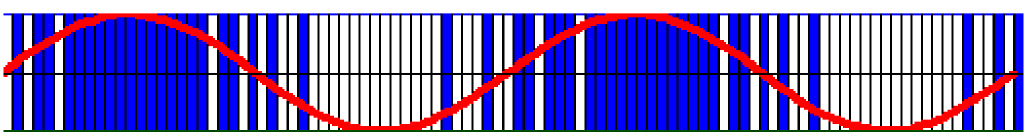


Figure 1.9 Pulse-density Modulation

1.6. EMI Reduction Techniques

Electromagnetic Interference, or EMI, is a serious concern for engineers designing products that utilize oscillators or other high-frequency components. By definition, EMI is undesired interference caused by electromagnetic radiation (EMR) from a local source [24]. The interference can cause erratic

---

[22] (Pulse-density modulation, 2007)
[23] http://upload.wikimedia.org/wikipedia/en/2/20/Pulse-density_modulation_1_period.gif
[24] (EMI Reduction and PCB Layout Techniques, 2003)

behavior or poor performance in nearby devices that are affected. For digital devices, noise can result in data corruption and errors [25]. Katrai and Arcus emphasize that EMI is a design problem first and foremost; McCulley agrees that EMI techniques implemented "after the fact" are not good design policy and do not perform well. EMI must be a design consideration from day one. Class D designs that are built from the ground up with EMI concerns in mind (designs that take advantage of all possible EMI reduction practices) are preferred. McCulley summarizes in his presentation: "EMI…is a design issue, not just a test and measurement issue…" [26]. Spread Spectrum Modulation, or SMM, is one of the few techniques available that enable a designer to cut off EMI at its inception before it has a chance to cause damage. SSM is discussed in detail in Section 1.6.2.

Switching power supplies such as Class D audio amplifiers and DC/DC converters commonly use pulse-width modulation (PWM) to drive their power output stages. As a result, the output of the amplifier contains all of the high-frequency energy from the fast switching in addition to the amplified baseband audio signal. Harmonics of the switching frequency are also present in the signal. For high-power amplifiers used with external speakers, there is a danger of this high-frequency energy being transmitted by the long speaker wires. Class D amplifiers also have EMI problems with their power supplies, since the fast switching draws current from the power supply in short bursts [27].

In practice, the output of the PWM stage consists of square waves of varying width. In producing this waveform, there is a danger of overshoot, which makes the corners of the square wave sharper and results in the presence of unnecessary high-frequency energy. For audio applications, overshoot and poor settling time can result in audible hiss or inaccurate amplification of the audio signal. Figure 1.10 shows the parameters associated with the classification of square waves [28].

---

[25] (EMI Reduction and PCB Layout Techniques, 2003)
[26] (McCulley, National_ReducingEMIinClassDAudioApps.pdf, 2007)
[27] (McCulley, National_ReducingEMIinClassDAudioApps.pdf, 2007)
[28] (McCulley, National_ReducingEMIinClassDAudioApps.pdf, 2007)

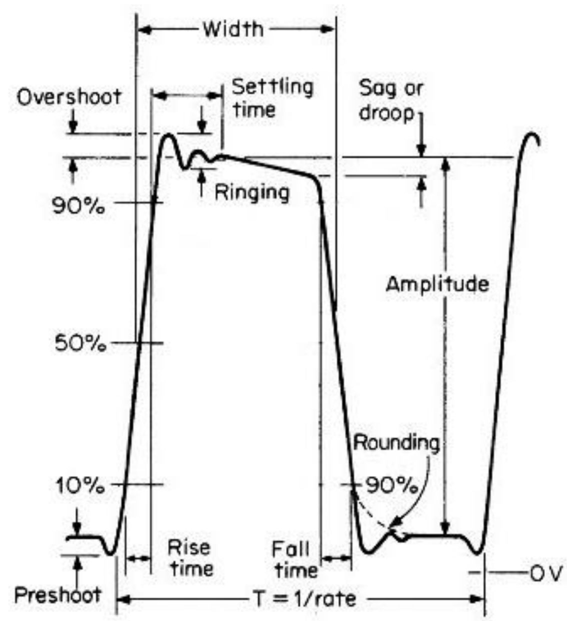


Figure 1.10 Square Wave Parameters

According to Katrai and Arcus, there are two types of EMI radiation: Differential mode and Common mode [29]. Differential mode EMI is caused by current loops formed by traces on PCBs that act as unintended antennas at high frequencies. Common mode EMI is caused by ground noise that affects circuit components attached to ground. While these EMI sources are secondary in magnitude for a Class D device whose EMI spectrum hinges on the switching frequency, they are still legitimate concerns for all designers of high-frequency analog and mixed-signal devices.

In this section we compare several options for EMI reduction in a modern electronic circuit. The methods discussed here are traditionally used by electronics designers when EMI performance is of great importance. Techniques for reducing EMI fall into two basic categories: filtering and shielding. In the past, shielding was commonly used in lieu of other methods due to the lack of space restrictions. Modern engineers prefer to design products that do not require extensive shielding from other electronic devices.

1.6.1. EMI Testing Standards

In the United States, the Federal Communications Commission (FCC) must test and verify the EMI characteristics of electronics that will be sold to consumers. The FCC Part 15 document specifies the full regulations for devices that radiate potentially harmful EMR. Other international agencies have also

---

[29] (Katrai & Arcus, 1998)

specified basic guidelines for EMI compliance (such as the CE/EMC guidelines in Europe). The FCC emissions standards for U.S. products are shown in Figure 1.11 [30]. Products are grouped into two general categories, "intentional radiators", such as cell phones, GPS, and Wi-Fi, and "unintentional radiators", which are devices that are not intended to radiate energy [31]. In the car audio market, EMI testing standards are more rigorous, since cars use electronic control systems that must be shielded from EMI to achieve safe operating conditions [32].

FCC and CE Class D radiated emissions standards		
Frequency range (MHz)	FCC Class B limit (μV)	CE Class B limit (dBμV)
0.45 to 1.705	48	–
1.705	48	–
0.15 to 0.50	–	56
0.50 to 5	–	56
5 to 30	–	60

Figure 1.11 FCC Radiated Emissions Standards

1.6.2. Spread-Spectrum Modulation (SSM)

Spread-Spectrum Modulation is a relatively new development for consumer products. By varying the switching frequency of the sawtooth or triangle waveform entering a comparator, the high-frequency switching energy is "spread" over a wider frequency spectrum instead of a single switching frequency and its harmonics. The switching frequency can be varied over a specific range (typically up to ±10% of the nominal frequency) or randomized by a digital controller [33]. While SSM signals are difficult to generate, integrated circuits are available that generate custom spread-spectrum signals if an external solution is desired. According to Maxim, the use of SSM clocking can result in a 12-15 dB drop in EMI output [34]. Some modern Class D products allow customers to set the SSM level externally via pins on the IC so that efficiency and performance can be customized based on EMI reduction needs. SSM significantly reduces the peak energy concentrated at the center frequency, as shown in Figure 1.12

[30] http://www.portabledesign.com/images/archive/images/0701pdreducing05.gif
[31] (FCC Part 15: Radio Frequency Devices, 2007)
[32] (Class D Amplifiers are designed for car audio, 2006)
[33] (Maxim Engineering Journal Vol. #59, 2007)
[34] (Clock Generation with Spread Spectrum, 2005)

[35]. The ability to keep a high switching frequency maintains the efficiency and low THD of the Class D topology while reducing EMI, one of the main drawbacks of switching amplifiers [36].

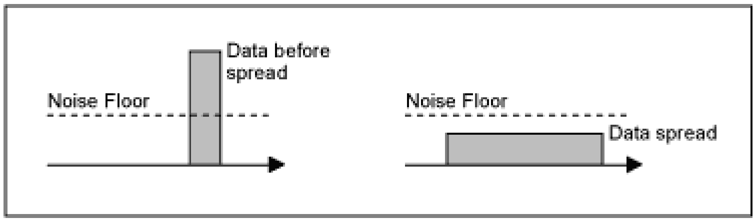


Figure 1.12 Spread-spectrum Modulation Theory

While Maxim Semiconductor claims to have a patent on this technique, several other companies claim to have this patent as well [37].

Because SSM does not eliminate high-frequency energy content from the output signal, it cannot be used in high-power applications without further EMI reduction technology. According to Stutz and Schmidt, SSM cannot be used in filterless applications where the output power exceeds a few hundred milliwatts [38]. Attempting to increase the clock frequency only results in worse performance, since the speaker wires become more efficient antennas as the wavelength of the RF energy decreases. SSM is not typically used in applications for speaker wires longer than a few inches for this reason. In high power applications, however, SSM can reduce the complexity and cost of the output filter, so it is still a helpful addition to a design.

1.6.3. Other techniques for EMI reduction

While Spread-Spectrum Modulation is a common feature of modern Class D amplifiers, other technologies are also used to reduce harmful EMI in these products. New third and fourth-generation Class D amplifiers include special patented EMI reduction circuitry that improves upon the EMI reduction performance of Spread-Spectrum Modulation. One such technique, Active Emissions Limiting, is discussed in Section 1.6.3.3.

---

[35] (McCulley, National_ReducingEMIinClassDAudioApps.pdf, 2007)
[36] (McCulley & Higashi, Reducing EMI in Class D audio applications by spread- spectrum modulation techniques, 2007)
[37] (Rako, 2007)
[38] (Stutz & Schmidt, 2007)

1.6.3.1. Filtering

Filter choice is also a significant decision to be made. The first filter type which was encountered in our research into current product designs was the second-order LC filter, shown in Figure 1.13 [39]. This filter is useful when EMI needs to be significantly reduced. It uses a larger number of parts for the reduction in EMI emitted and it also protects the speaker from seeing virtually any of the ultra sonic signals that resulted from the higher switching frequency at the previous stages. In the documents which give a comparison between varying filter designs and this style had low quiescent current, low efficiency, low EMI, high THD+N and high part numbers. When designed with Butterworth criteria, the LC filter can have a very flat passband, making it an attractive option for audio applications where distortion should be kept low.

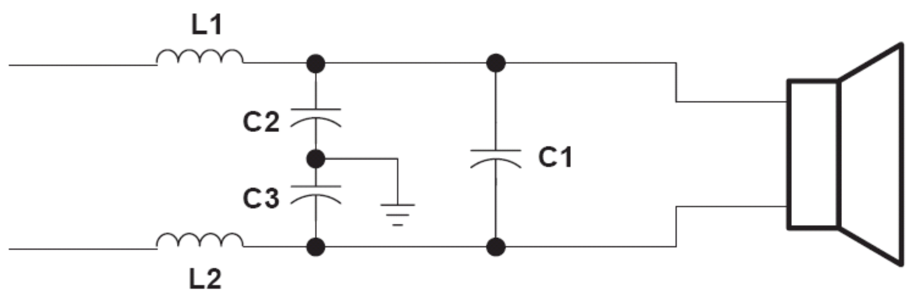


Figure 1.13 Second Order Balanced Filter

A second filtering solution was to use a Half Filter, shown in Figure 1.14 [40]. The half filter is a compromise between the 2nd order Butterworth filter and the use of no filter. This device has fewer components than a second order filter, yet it has many of the same benefits. The half filter designs tend to have a lower quiescent current, higher efficiency, lower THD+N and lower part numbers than the butter worth. However, their ability to reduce EMI for a bridge-tied load is significantly hindered by the component placement. Therefore, this filter is useful in situations where EMI is not one of the primary concerns.

---

[39] http://focus.ti.com/lit/an/sloa023/sloa023.pdf
[40] http://focus.ti.com/lit/an/sloa023/sloa023.pdf

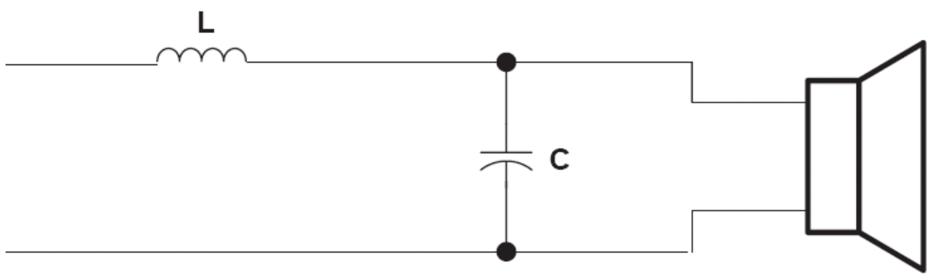


Figure 1.14 Half Filter

The least expensive filtering method is to use the speaker itself as a filter. This method requires a different design approach than the previous two methods. The speaker in this situation sees the full output of the amplifier system. This reduces the overall losses of the filter system significantly. However, the high switching frequencies may damage the speaker. With proper speaker selection, this damage can be prevented. The use of a speaker with a high inductive value is recommended in this situation. The speaker itself than acts as a low pass filter in this situation; as the applied frequency rises, the impedance of the speaker also rises. This filter design has very high quiescent current, high efficiency, very low THD+N, and the fewest possible number of parts. However, the high-frequency signal is allowed to traverse the speaker wires, making this “filterless” method nearly impossible for applications with long speaker wires.

1.6.3.2. Ferrite Beads

Ferrite (iron-based) beads can be placed in series with loudspeakers that are connected closely to an amplifier. The beads introduce an inductance to the speaker wire that can attenuate high-frequency signal components [41]. However, they are difficult to select due to the fact that they can only attenuate signals over a narrow frequency range. In a Class D amplifier, unwanted noise exists at the switching frequency and its harmonics. Figure 1.15 shows the characteristic resistance and inductance of a ferrite bead versus frequency. Ideally, the frequency-dependent resistance of the bead would exceed the inductance for the desired frequency range [42].

---

[41] (McCulley & Higashi, Reducing EMI in Class D audio applications by spread- spectrum modulation techniques, 2007)
[42] (McCulley, National_ReducingEMIinClassDAudioApps.pdf, 2007)

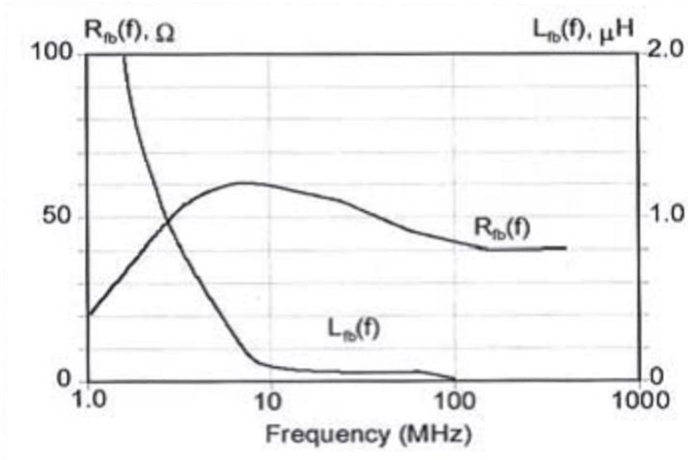


Figure 1.15 Ferrite Bead Frequency Response

While ferrite beads may help reduce the presence of high-frequency content in speaker wires, they cannot be the only EMI reducing system in a higher power design [43]. Other methods must be used if a high-power device is to pass FCC testing.

1.6.3.3. Active Emissions Limiting (AEL)

New third-generation Class D audio products offered by manufacturers utilize Active Emissions Limiting (AEL) to further reduce EMI radiation from their products. AEL and SSM can be used concurrently in Class D designs. AEL is a method of shaping the PWM waveforms used to drive the Class D power stage switches. By eliminating the overshoot (and "sharpness") of square-wave switching while keeping the fast switching speed, THD and performance are not significantly impacted, but spectral components of the switching frequency and its harmonics are reduced considerably [44]. Figure 1.16 illustrates the theory of AEL and the resulting EMI performance boost (note the drop in power efficiency with AEL enabled) [45]. The resulting drop in EMI emissions allows the third-generation parts to operate with significantly longer speaker wires while passing tests for FCC EMI regulations. Furthermore, the combination of SSM+AEL allows low-power Class D amplifiers to operate without an output filter while using external speakers. Elimination of the output filter saves component costs and PCB space.

[43] (Maxim Engineering Journal Vol. #59, 2007)
[44] (Maxim's Active-Emissions-Limiting (AEL) Circuitry Demystified, 2006)
[45] http://media.maxim-ic.com/images/appnotes/3973/3973Fig02.gif

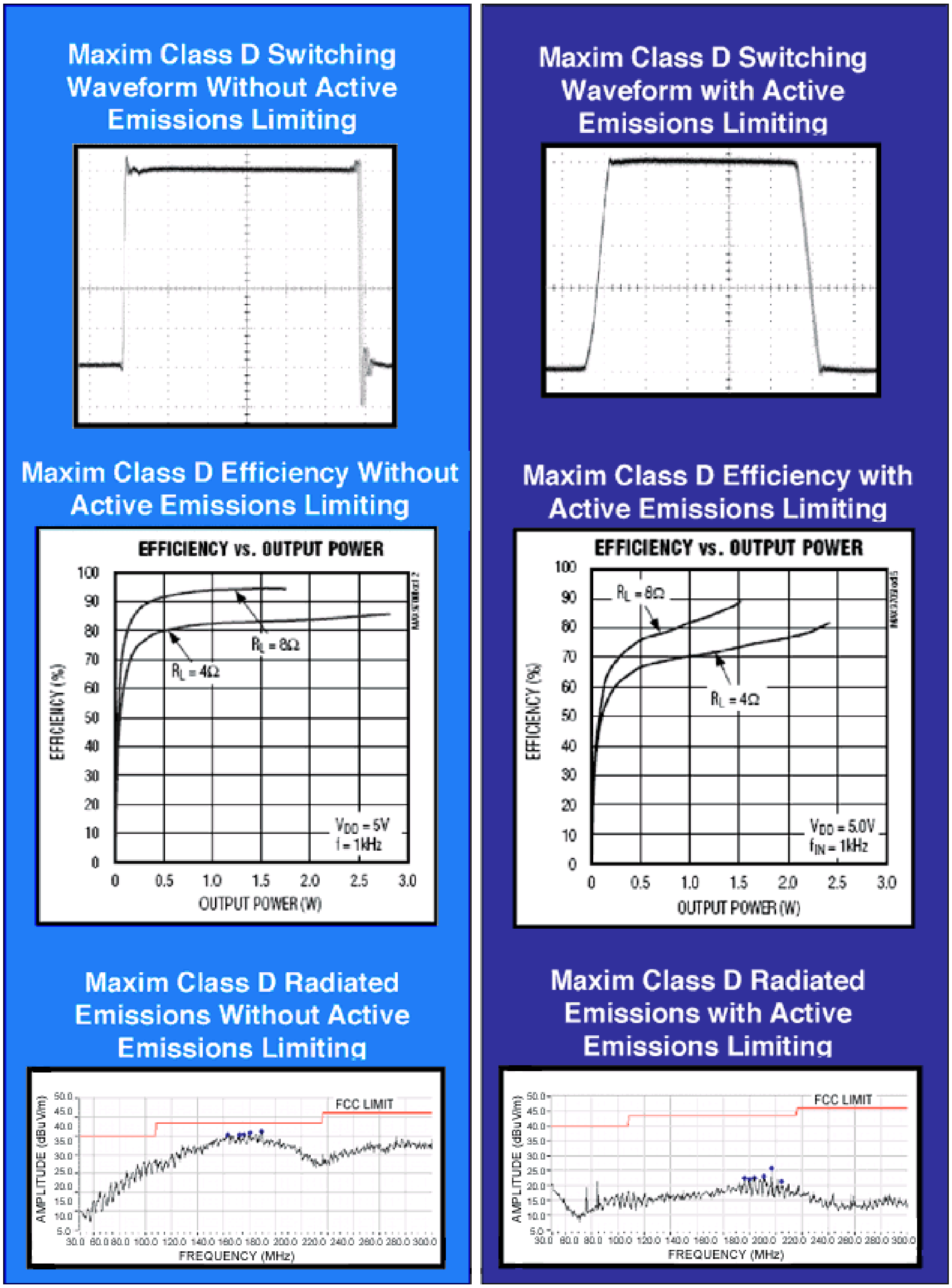


Figure 1.16 Maxim AEL Performance

Figure 1.17 displays the Maxim method of implementing AEL in a filterless design [46]. The NOR gate and Zener diode is used to modify the waveforms that drive each side of the full bridge power stage. The full manufacturer's description of this circuit's behavior can be found in Appendix D. Maxim notes that the speaker should appear inductive at the switching frequency range in order to achieve the best power output from the device [47].

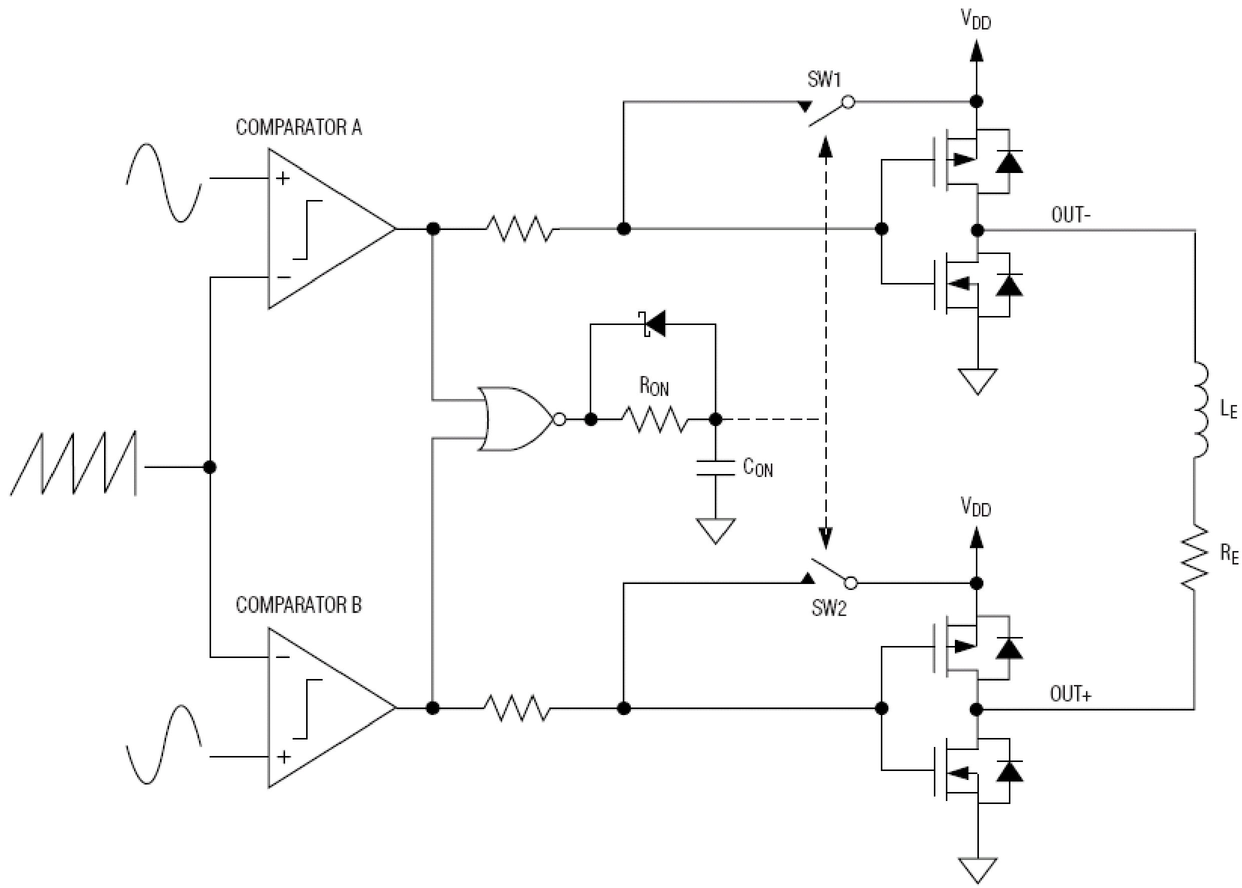


Figure 1.17 Maxim Filterless Design With AEL

1.6.4. PCB Layout Optimization

Because EMI is primarily a design concern, it is therefore helpful to survey the practices used by engineers when designing low-EMI products. Proper PCB component layout can significantly reduce the EMI radiation and susceptibility of a device, especially in embedded applications where PCB traces and wires are in very close proximity. According to Honda and Adams, "PCB layout is crucial for both

[46] http://pdfserv.maxim-ic.com/en/ej/EJ59.pdf
[47] (Maxim Engineering Journal Vol. #59, 2007)

ruggedness of the design and reduction of EMI" [48]. McCulley and Higashi note that, as Class D products become smaller and saturate the portable device market, the need for filterless low-EMI designs are increasing significantly. The following is a list of PCB design guidelines for reducing EMI [49]:

- Use de-coupling capacitors to reduce power supply ripple (<50 mV)
- Use lower-frequency clocks whenever possible
- Keep signal traces on PCB short and rounded (no 'T' intersections or right-angle corners)
- Place the highest-clock signal at the center of PCB
- Run traces to the clock before all other traces to ensure proper placement
- Do not cross high-frequency lines whenever possible on a multi-layer PCB
- Route differential pairs (such as BTL speaker wires) close to each other and away from other signals
- Keep analog and digital signals separated where possible
- Connect all power and ground pins of an IC
- Terminate unused pins on an IC (for example, unused op-amps by tying positive input pin to ground and negative input pin to the output pin)
- Place traces with high-speed periodic signals between ground and power planes or between two ground planes
- Do not run traces under the clock or other high-frequency components
- Keep power and ground leads parallel and adjacent to each other (no loops)

These guidelines are some of the many recommended practices for reducing EMI. This list is by no means comprehensive. Compared to SSM or filtering, the reduction in EMI output that results from these guidelines may be small, but this could be the difference between passing and failing rigorous EMI testing.

[48] (Honda & Adams, 2005)
[49] (EMI Reduction and PCB Layout Techniques, 2003)

1.7. Special Features

Class D amplifiers have been developed with a variety of special features to set themselves apart from the rest. Each manufacturer offers different features in each of their amplifiers. Texas Instruments' TPA032D04 is a 10 watt stereo Class D audio power amplifier that has several of the common special features commonly found in audio amplifiers [50]. The majority of amplifiers on the market include at least one of these features found on the TPA032D04:

- De-pop protection – reduces the amount of pops and clicks during power up
- Mute – prevents audible output
- Thermal Shutdown – prevents unit from overheating
- Current Shutdown – limits total supply current, increasing battery life in portable applications

Size is the one of the major concerns for portable applications. Today's portable devices are getting smaller and smaller. National Semiconductor's LM4673 is, as of 2005, is the world's smallest Class D audio amplifier. This filter-less, 2.5 W amplifier comes in a 1.44 mm x 1.44 mm micro-SMD package. Leads for this device are spaced only 0.4 mm apart. The small size allows the chip to be placed closer to speakers, reducing EMI. Figure 1.18 shows the size of the LM4673 (left), as well as the LM4674 (right) compared to a cell phone [51].

Figure 1.18 LM4673 and LM4674

[50] (TPA032D04, 2000)
[51] http://www.national.com/news/images/LM4673_74.jpg

1.8. Power Losses and System Efficiency

In this section, we attempt to find the sources of power loss in Class D amplifiers. Instead of designing an amplifier and then locating the sources of loss in our own design, we chose use previous art to our advantage. We found several documents detailing power loss issues; however, one source in particular summarized the information in other documents very well [52].

The main sources of power loss are the MOSFETs (power switches). When the MOSFET is on and the drain-source resistance ($R_{DS(on)}$) is at its minimum, there is still a significant amount of power wasted by the MOSFET due to the $R_{DS(on)}$ (typically several mΩ or larger). Another source of loss is when switching MOSFETS between their “on” and “off” gate voltages; there is a significant amount of charge that must be supplied and drained from the gate capacitance. This charge is discharged and replaced during each cycle. This results in an increase in power consumed proportional to switching frequency. Another source of loss can be the voltage dropped across the interconnecting wires of the system. This may or may not be significant depending on the length and quality of the wires and traces connecting the system. The Filter is also another source of power loss within the system. The filter itself is comprised of LC components which all have some parasitic resistances associated with them. This results in lower than ideal voltages at the load and also parasitic resistive loads in parallel with the speaker result in additional power being wasted. All of which contributes to preventing the full output power of the system being applied to the speaker. An initial equation for the efficiency of the amplifier is presented in Equation 1.1. This formula is located within the maxim application notes. Where R_{on} is the resistance of the MOSFET when active, R_F is the parasitic resistance of the filter, R_L is the resistance of the load, and R_P is the resistance of wires and traces. For the complete derivation, see [52].

$$\eta = \frac{P_{OUT}}{P_{SUPPLY} + P_{SWITCH}} = \frac{{I_{OUT}}^2 R_L}{{I_{OUT}}^2 (2R_{ON} + 2R_F + R_P + R_L) + \frac{1}{2} f_{OSC} {I_{OUT}}^2 (t_{ON} + t_{OFF}) 2R_{ON}}$$

Equation 1.1 Formula For Efficiency of An Amplifier

1.8.1. Power Output

The power output of a Class D amplifier depends directly on the power supply available for the device and the intended application of the amplifier. Low power outputs (less than 5 watts) are typical in portable applications where battery life depends greatly on the efficiency of the electronic subsystems. A low power output is also desirable in a portable device in order to minimize the heat

---

[52] (Class D Audio Amplifiers Save Battery Life, 2002)

dissipated by the audio amplifier due to inefficiencies. In home theater applications, power levels between 100 and 1000 watts RMS are possible since home audio amplifiers draw power from the home's AC system. Modern computer speakers and car audio systems can also have a peak power output of over 500 watts RMS. However, Class D amplifiers are not typically used for home audio since efficiency is not of great concern and the performance of a Class A or Class AB amplifier is regarded by many audiophiles to be of superior quality.

1.9. Ideal Circuit Simulations

To get a firm understanding of what we are trying to achieve, we decided to model an ideal three-level system. In this model we used ideal components to show what we are trying to achieve in our system design. Over the course of the project we introduced more and more non-ideal parameters into our model in order to better design for a practical situation. The system diagram we came up with is shown in Figure 1.19.

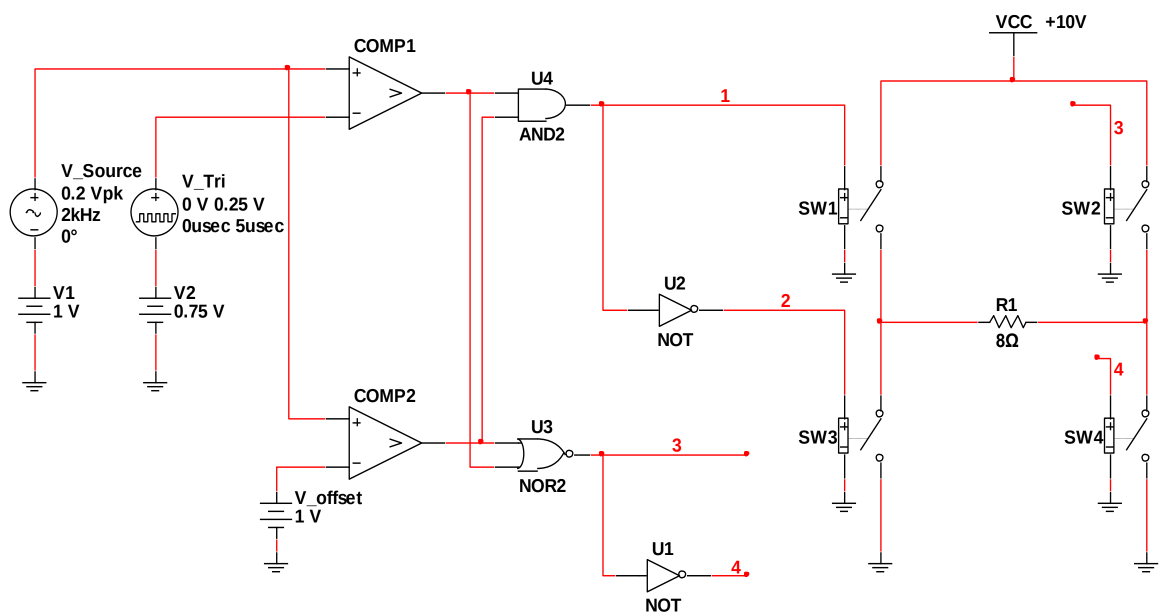


Figure 1.19 Ideal Model

Figure 1.20 displays the plot generated by the SPICE simulation for this circuit. The top waveform is the input baseband audio signal. The lower waveform is the three-level PWM signal experienced by the load. The triangle-wave frequency used by the PWM stage is low for simulation purposes in order to illustrate the basic functionality of the amplifier. Note that the width of the PWM pulses depends on the amplitude of the input signal. Once filtered, the PWM signal should reproduce the same sine wave with minimal distortion.

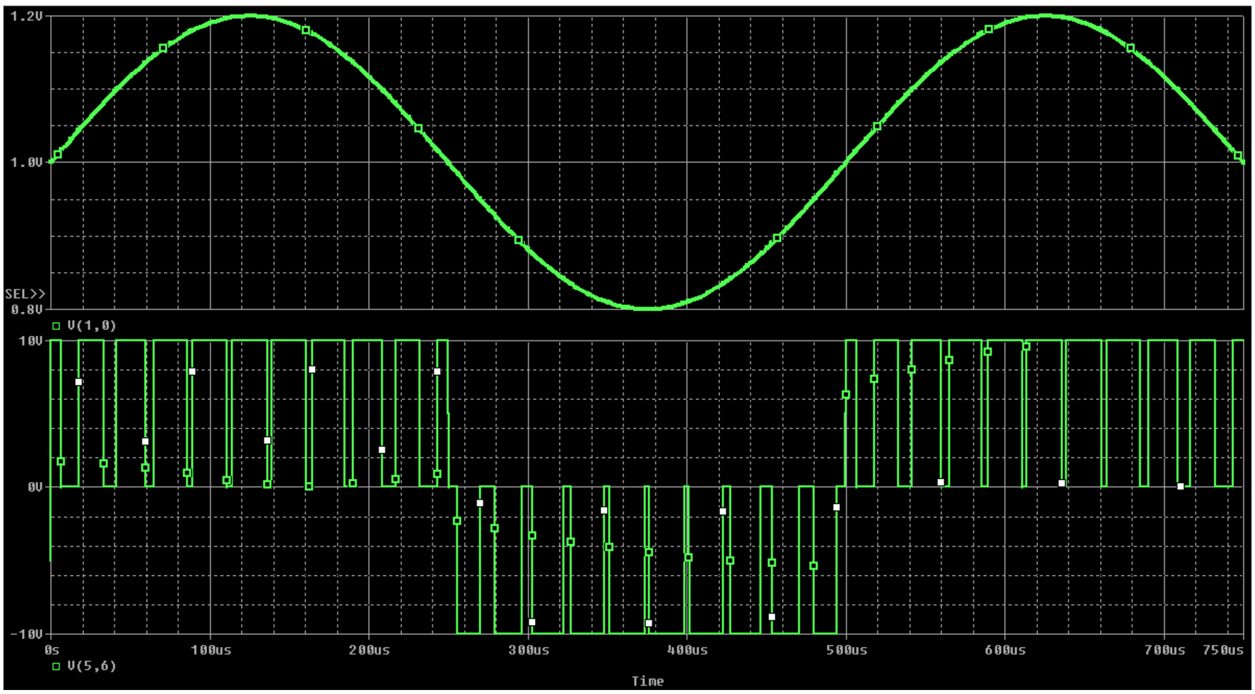


Figure 1.20 Ideal Waveforms

2. Project Definition

The following are the chosen specifications for our design:

- Total Harmonic Distortion: < 1%
- Frequency response: 20 Hz-20 kHz
- Output Power: Greater than 2 W
- Spread Spectrum Modulation
- Three Level Switching
- Single Power Supply
- Full bridge-tied load
- Filter in power stage

Our project was designed to have less than 1% total harmonic distortion measured in the amplified audio signal. This is necessary because the audio quality of our product must be comparable to other commonly available products in order to compete in the market. Several revisions of the final design will likely be necessary in order to meet and exceed this objective.

Power efficiency was another prime concern for our project. Class D audio amplifiers' main advantage, when compared to other classes of amplifiers, are their efficiency. In order to have a competitive product in our chosen power range, the efficiency of our device must be at least 90%. Devices available from major chipmakers on the market today offer efficiencies of well over 90%.

The output power goal of 2 W was chosen because it is on the upper end of what is used in the portable audio market. Portable devices such as cell phones and laptops typically have volume restrictions which limit the size of any speakers that may be built into the device.

Spread Spectrum Modulation was considered in combination with a filter so that our design can meet the necessary FCC specifications for emitted EMI while maintaining the high characteristic power efficiency of a Class D product.

The use of a three level switching system will allow the amplifier to be more efficient at lower power levels. The additional design time for a three-level switching scheme is offset by the potential gains in efficiency afforded by three-level switching. A single power source was chosen due to the weight and size constraints of the portable audio market. A single power supply is often the only feasible option, and portable devices typically only operate from a single battery as the power source. The choice to go with a three level system and a single power source demanded a full bridge for our design, since a half bridge configuration cannot perform three-level switching (based on our research).

3. Project Design

In this section we document the design process for each of our fundamental system blocks. Each subsystem was first designed based on theoretical calculations before performing software simulations. Based on the results of these simulations, we then proceeded to select appropriate parts for our amplifier. Upon receiving these parts, real-world testing was performed when possible.

3.1. PWM Switching

Our first task was to create a pulse-width modulator which would allow us to sample our input signal and obtain the information necessary to drive our full bridge power stage with a three-level switching scheme. Figure 3.1 displays our first simulation circuit for a three-level modulator.

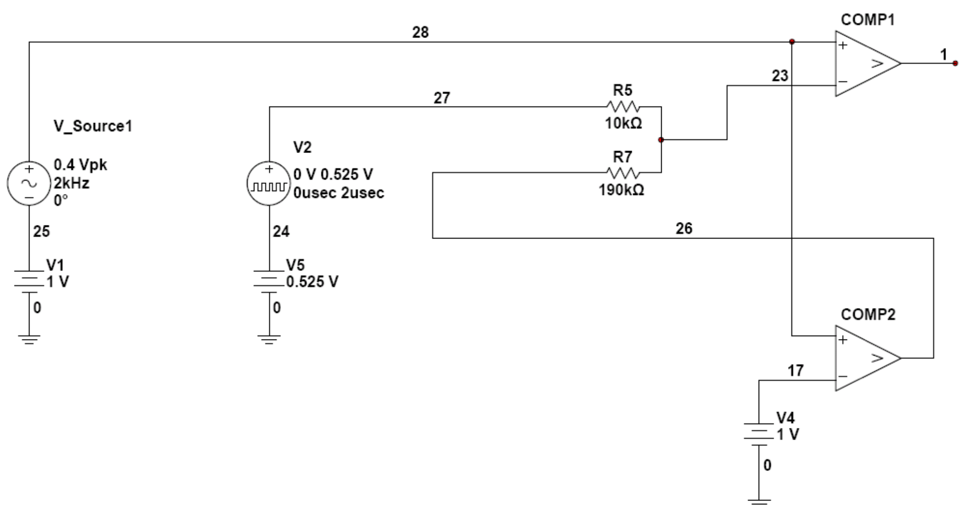


Figure 3.1 Schematic for PWM Switching Scheme

This block is responsible for comparing the input signal with a triangle wave. The output generated is a waveform which can be used as an input for our driver functional block. In this simulation, the modulator is designed for an input voltage signal between 0-20 kHz with an amplitude of 0.4 V peak and riding on a 1 V offset voltage. We also treat the triangle wave generator as a functional black box which creates a triangle wave of amplitude 0.525 V.

3.1.1. Switching Logic and Basic Concepts

The use of two comparators in this functional block is required due to the fact two sets of information are needed to properly drive the output. The top comparator (COMP1) compares the input audio signal to the modulating signal. COMP1 is the comparator which results in the modulating of the input signal. The output of this system is the modulated signal which is used by the driver to switch between connecting speaker load to a power source or to ground. This comparator needs to be able to output enough current that the requirements of the inputs of the driver circuit are met. The non-inverting input is connected to the input signal and the inverting input is connected to a summer circuit. This circuit adds a given percent of the output of the other comparator (COMP2) to the triangle wave's DC component. However a negative effect of the summer circuit is a slight attenuation of the triangle wave. This attenuation is compensated for by increasing the initial amplitude of the generated triangle wave. The COMP2 compares the input signal to a DC reference value equal to its own DC offset. This allows us to know whether the input signal is negative or positive. The output signal is used both as feedback into the PWM functional block and also as an input into the driver logic block. The driver uses the signal from this comparator to control which pair of MOSFETs are switching and which are not switching and thus are locked in their "on or off" modes. This comparator must be able to output enough current to satisfy the input requirements of both the COMP1 and the driver functional block.

3.1.2. Offset Voltage

A DC offset is required on both the input signal and the triangle wave. The DC offset on the input signal is necessary due to the fact if the sine wave was centered around 0 V the input would dip below 0 V and in our system we did not choose our comparators to operate within this condition (a dual power supply would be necessary). The DC offset of the triangle wave establishes the position of the comparing wave with reference to the input signal. When the triangle wave and input signal are perfectly aligned, the system will operate with maximum performance.

3.2. Filter Design

3.2.1. Introduction & Theory

As stated in the background section, an output filter is one of the most effective methods for reducing Electromagnetic Interference (EMI) in a switching power amplifier. The bandwidth of a typical audio signal is between 20 Hz-20 kHz. In a Class D amplifier, however, the output also contains significant amounts of the switching frequency energy (in our case, over 300 kHz). While this energy is not audible to the human ear, it was important to us to not waste energy trying to drive the speaker beyond its mechanical capabilities. Furthermore, with long speaker wires, the switching energy would cause the speaker wires to radiate the PWM waveform and blast unwanted RF interference through the air.

We wanted our final product to meet or exceed the FCC regulations for radiated EMI. The incorporation of spread spectrum clocks into our design could help us, but we understood from our market research that a filter would be required for amplifiers at power levels larger than a few watts. This would allow us to extract our baseband audio signal from the PWM waveform.

3.2.2. Design Process

We began the filter design process by selecting an appropriate filter structure. Due to the additional costs associated with adding an output filter, we knew that we wanted to keep the component cost low while still achieving the desired performance. Our original idea was to incorporate a simple low-pass second-order Butterworth filter between the power switches and speaker. As we will see later, some complications arose due to our H-Bridge power stage configuration. Figure 3.2 displays a typical filter setup for a two-level Class D amplifier [53]. Note that the inductor is in series with the load, whereas the capacitor is in parallel. This means that the inductor must be capable of handling all of the current driven to the load.

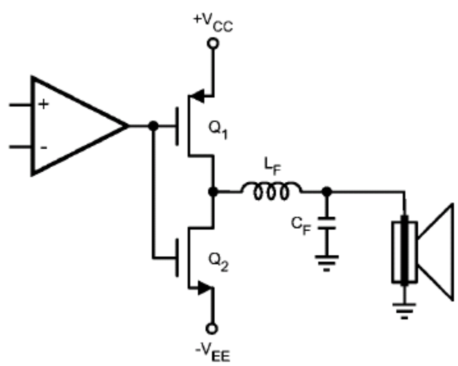


Figure 3.2 Typical LC Output Filter (Shown With Power Stage)

It is important to note that the speaker impedance is not constant with respect to frequency. Figure 3.3 displays a plot of speaker impedance versus frequency for a small 8 Ω, 1.75'' speaker [54]. While the speaker impedance rises with high frequency signals, it is relatively flat over the audio band. The series inductance of this sample speaker (10 µH according to Maxim) allows the speaker to function as a filter at low power levels [55]. For high power applications, however, it is critical to have an output filter placed between the amplifier power stage and speaker wire connectors so that the PWM waveform is not allowed to travel along the speaker wires unfiltered.

---

[53] http://www.national.com/onlineseminar/2007/emi/National_ReducingEMIinClassDAudioApps.pdf
[54] http://www.maxim-ic.com/appnotes.cfm/an_pk/624
[55] (Class D Audio Output Filter Optimization, 2002)

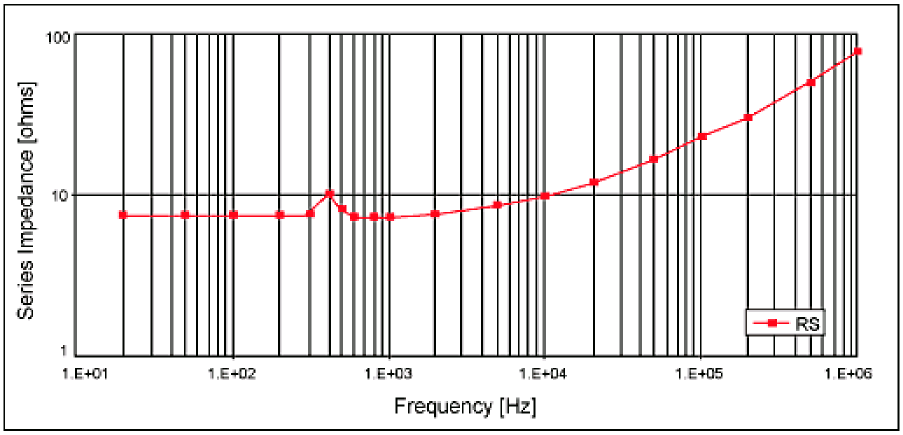


Figure 3.3 Example Speaker Impedance vs. Frequency

We chose a passive filter design due to its simplicity and low cost. Furthermore, the passive filter can also handle a large power output without protection circuitry. We chose a Butterworth filter due to the Butterworth filter's flat frequency response in the passband. Any passband ripple would result in distortion of the output's frequency response with respect to the input.

3.2.3. Alternative Structures

While the single-sided LC filter seemed to be a good choice, our team also stumbled upon some promising balanced filter arrangements for full-bridge amplifiers. The filter in Figure 3.4, found in an Analog Devices document written by Eric Gaalaas, shows a balanced design using two capacitors and two inductors of equal value [56].

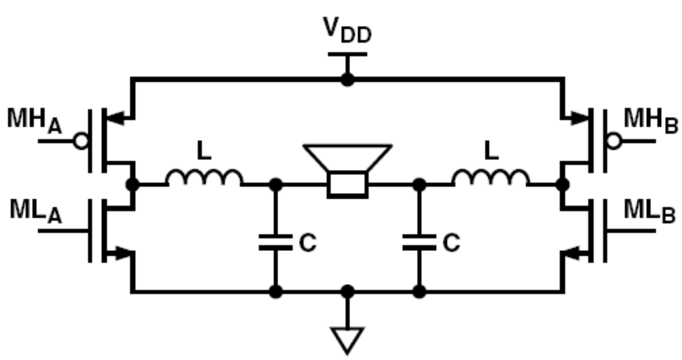


Figure 3.4 Balanced Filter Design

What are the potential benefits of such a design? Maxim Application Note 624 recommends a balanced design to ensure that each side of the load in a full-bridge configuration "sees" the same filter structure.

---

[56] http://www.maxim-ic.com/appnotes.cfm/an_pk/624

For example, consider the simple LC filter shown in Figure 3.5, constructed for a full-bridge configuration [57]:

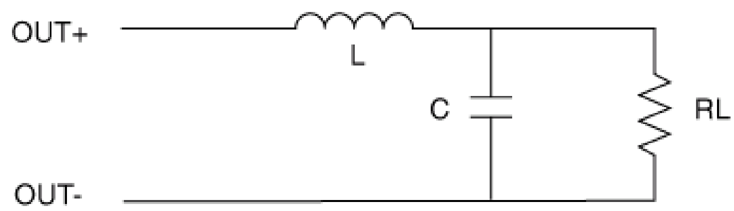


Figure 3.5 Low Pass Filter For Full Bridge

The result is that OUT- is not filtered before the load, and the PWM waveform may radiate from the lower wire. This can be prevented by modifying the design such that the filter is divided equally between both speaker wires, as shown in Figure 3.6 [58]:

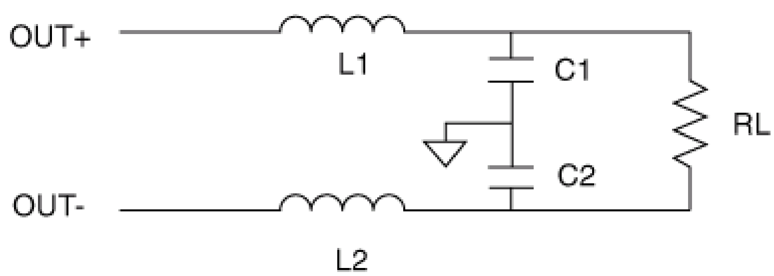


Figure 3.6 Divided Low Pass Filter For Full Bridge

This configuration is exactly the same as the configuration proposed by Gaalaas.

3.2.4. Transfer Function

We continue our filter design by deriving the transfer function for the single-sided LC filter proposed earlier. Based on the values calculated for our desired cutoff frequency, the filter component placement may then be modified to suit our needs in a full-bridge configuration.

---

[57] http://www.maxim-ic.com/appnotes.cfm/an_pk/624
[58] http://www.maxim-ic.com/appnotes.cfm/an_pk/624

We begin by taking the output of the filter across the speaker, and determining the impedance seen at the output:

$$Z_{OUT} = R \parallel C(R \parallel C) + L = \frac{\frac{\frac{R}{j\omega C}}{R + \frac{1}{j\omega C}}}{\frac{\frac{R}{j\omega C}}{R + \frac{1}{j\omega C}} + j\omega L} = \frac{\frac{R}{j\omega C}}{\frac{R}{j\omega C} + \left(R + \frac{1}{j\omega L}\right) j\omega L} =$$

$$\frac{\frac{R}{j\omega C}}{\frac{R}{j\omega C} + Rj\omega L + 1} = \frac{R}{R + R(j\omega C)(j\omega L) + j\omega C} = \frac{R}{-\omega^2 RCL + j\omega C + R}$$

We know that for a Butterworth filter, the transfer function magnitude is $\frac{1}{\sqrt{2}}$ at the cutoff frequency:

$$\frac{1}{\sqrt{2}} = \frac{1}{\omega \frac{L}{R}} = \frac{R}{\omega^2}$$

$$\Rightarrow \omega L = R\sqrt{2}$$

$$L = \frac{R\sqrt{2}}{\omega_0}$$

To find the capacitor value, we use the fact that the cutoff frequency, ω_0, is equal to $\left(\frac{1}{\sqrt{LC}}\right)$:

$$\omega_0^2 = \frac{1}{LC}$$

$$C = \frac{1}{\omega_0^2 L}$$

3.2.5. Calculating Values

Based on these two equations, we may now calculate values for *L* and *C*. Table 3.1 below displays the reference capacitor and inductor values for several values of *R*, the nominal speaker impedance. These values assume a cutoff frequency, f_0, equal to 20 kHz.

Speaker Impedance ***R***	Capacitance ***C***	Inductance ***L***
2 Ω	2.8 µF	22.5 µH
4 Ω	1.4 µF	45.0 µH
8 Ω	0.7 µF	90.0 µH
16 Ω	0.35 µF	180 µH

Table 3.1 Calculated Values For 20 kHz Cutoff Frequency

These values appear to be very practical for real-world use. For many Class D amplifiers, companies will set their cutoff frequencies higher than 20 kHz in order to reduce component size and prevent attenuation at frequencies near the cutoff. Due to the significant gap between the audio band and the PWM switching frequency, this is a very practical design consideration. If we wish to minimize the component size of our filter, setting a higher cutoff frequency (such as 30 kHz) is an attractive option. This would also ensure that high-frequency audio signal content is not attenuated by the output filter. Table 3.2 displays the capacitor and inductor values calculated for a 30 kHz cutoff frequency.

Speaker Impedance R	***Capacitance C***	***Inductance L***
2 Ω	1.8 µF	15 µH
4 Ω	0.9 µF	30 µH
8 Ω	0.45 µF	60 µH
16 Ω	0.225 µF	120 µH

Table 3.2 Calculated Values For 30 kHz Filter

3.2.6. Software Simulation

In order to ensure that the filter component values were correct, we utilized National Instruments' Multisim 10 software package to simulate the filter design. Figure 3.7 shows the test circuit used for the filter simulation. The speaker load for the simulation had a nominal 8 Ω impedance.

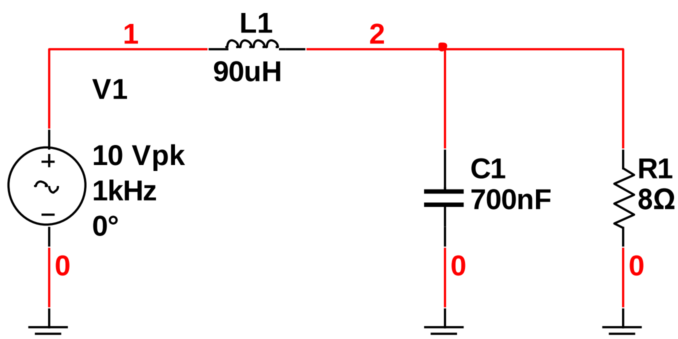


Figure 3.7 Filter Simulation Circuit

A frequency sweep from 10 Hz to 100 kHz revealed that the filter was performing as intended. The 20 kHz cutoff frequency is clearly labeled on the magnitude Bode plot as the -3 dB point. We also observe a very flat passband region, a characteristic of the Butterworth-criteria design. Not shown is the phase response indicating a -90° phase shift at the cutoff frequency.

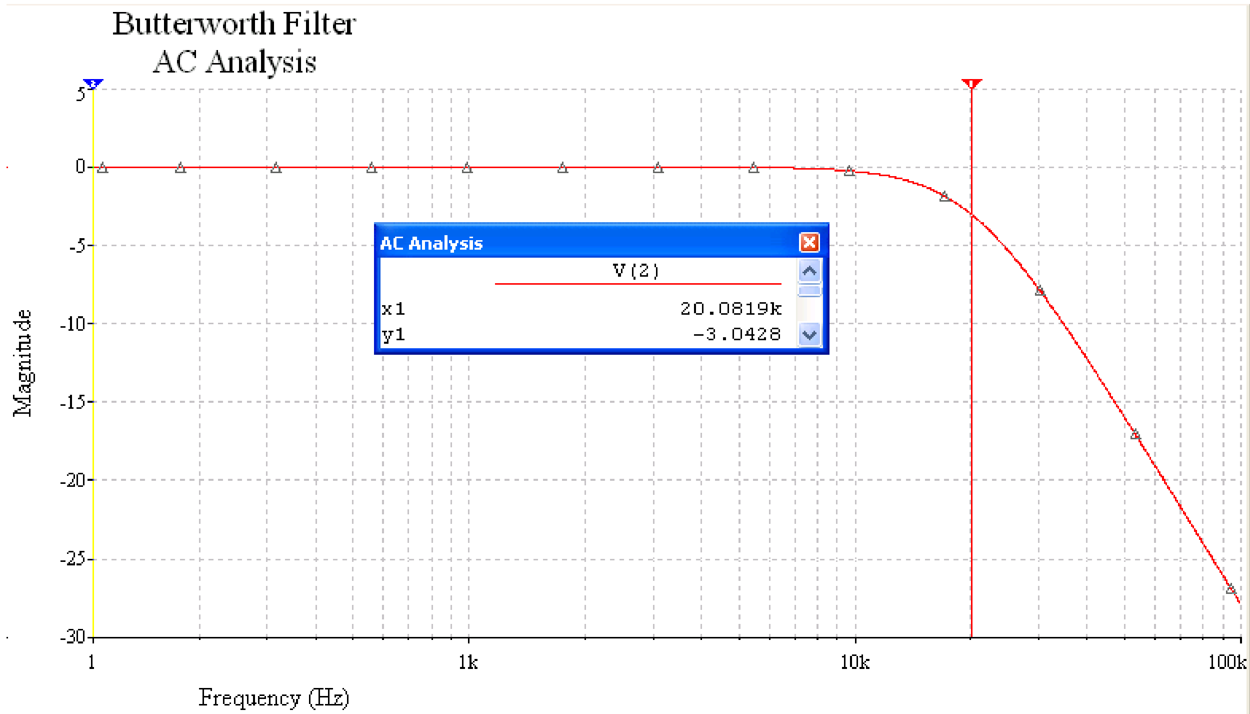


Figure 3.8 Filter Magnitude Response vs. Frequency

A balanced filter is the preferred option for the full bridge configuration. We decided to simulate several configurations of balanced (split) filters in an attempt to emulate the performance of the single-ended filter for the differential case. Figure 3.9 shows the split balanced filter with equal capacitor and inductor values on each end of the load. Note that each inductance is half the value of the original calculated inductance of 90 µH, while each capacitance is twice the original value of 700 nF.

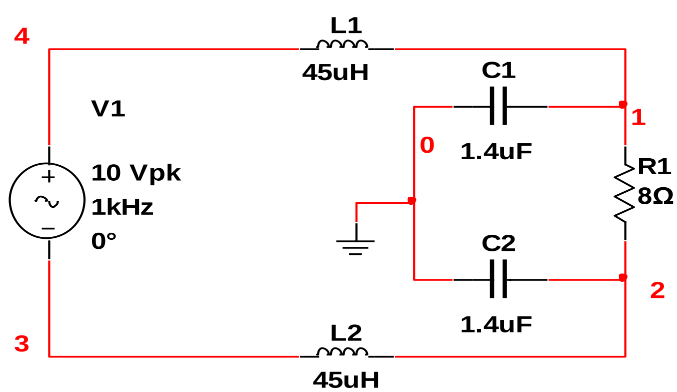


Figure 3.9 Balanced Filter Simulation Circuit

Using the above circuit, we perform the same AC analysis frequency sweep as the previous simulation and observe the voltage across the load (nodes 1 and 2). The frequency sweep magnitude response revealed similar performance compared to the single-ended filter. The balanced component configuration maintains the -3 dB cutoff at 20 kHz as specified during the design process.

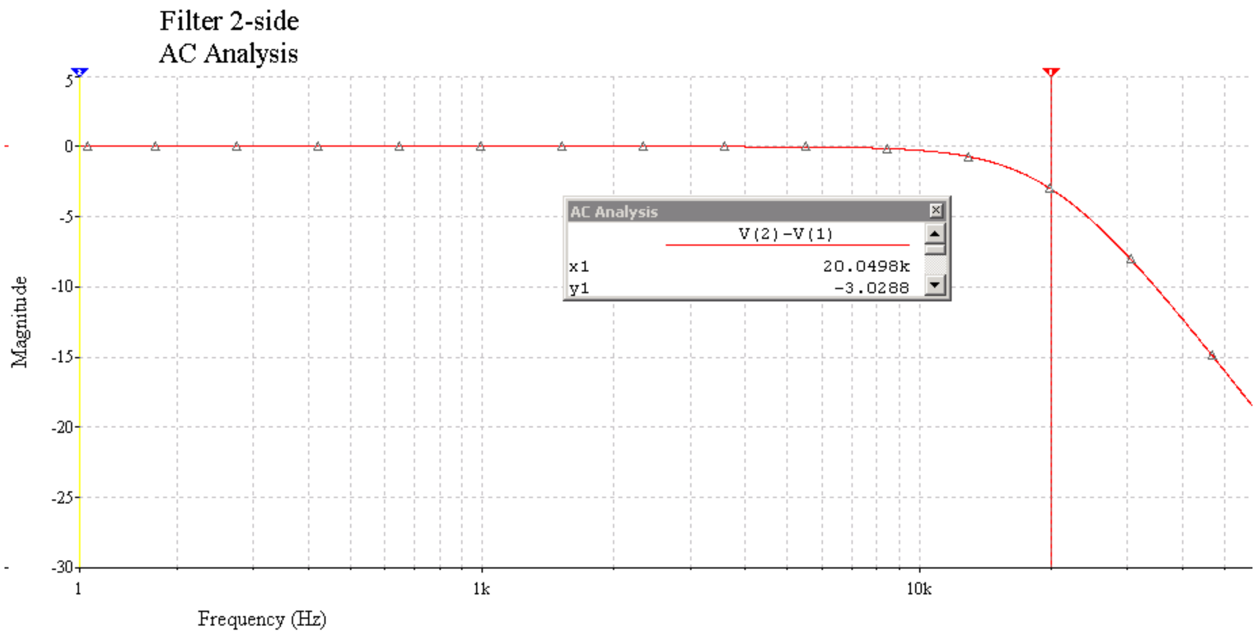


Figure 3.10 Balanced Filter Frequency Response

3.2.7. Part Selection

Based on the previous calculations, we established a need for capacitors and inductors to realize our filter. For the single-side case, we require a capacitor of 0.7 µF and an inductor of approximately 90 µH. In order to select parts, we established a list of requirements for the filter components:

Capacitor	***Inductor***
Must be capable of withstanding >12 V peak	Must be capable of handling > 1.3 A peak
Low series resistance	Low series resistance
Low change over time/temperature (±10%)	Accurate value (±10%)
Small size	Small size

Table 3.3 Part Selection Criterion

We searched several online retailers in order to find appropriate parts. The final selected parts are summarized in the table below. For detailed specifications, please refer to the datasheets included in Appendix G. Note that the balanced filter may use components from the same product line with alternate capacitance or inductance values.

Capacitor	***Inductor***
Series: Panasonic KBP Ceramic Capacitor	Series: Triad Magnetics Switchmode/ High-Frequency
Model Number: ECK-D3A681KBP	Model Number: FIT68-1
Capacitance: 680 pF	Inductance: 90 µH
Voltage rating: 1000 V	Current rating: 2.8 A
Type: Disc	Type: Toroidal
Tolerance: ±10% over operating temperatures	Tolerance: ±10%

Table 3.4 Selected Filter Components

We also decided to select filter components for a higher-power design to allow us to implement a high-voltage power stage for our three-level amplifier. We selected inductors with higher current ratings and capacitors with higher voltage ratings in order to satisfy the requirements of a higher supply voltage. Table 3.5 contains the specifications for the inductor and capacitor selected.

Capacitor	***Inductor***
Series: Vishay/BC MKP 417-20	Series: API Delevan Inc. DC630R
Model Number: 2222 417 79104	Model Number: DC630R-333K
Capacitance: 910 pF	Inductance: 33 µH
Voltage rating: 160 V	Current rating: 4.95 A
Type: Radial Poly/Film	Type: Radial
Tolerance: ±2% over operating temperatures	Tolerance: ±10%

Table 3.5 Higher Power Filter Parts

3.2.8. Real-World Testing

Real-world testing of the filter was performed using a Tektronix AFG3021 function generator combined with the single-sided version of the Butterworth filter. A sinusoidal waveform of amplitude 10 V was applied to the filter with a load impedance of 8 Ω. At frequencies above 30 kHz, the waveform across the load was substantially attenuated with respect to the input voltage.

3.3. Triangle Wave Generation

For analog PWM we required a precision triangle wave. A common triangle wave generating circuit consisting of an integrator and a Schmitt trigger was explored. The specifications for the desired triangle wave were determined and from those, the component values were selected. After verifying the design through simulation, an appropriate operational amplifier/comparator was selected and tested.

3.3.1. Op-amp Configuration

A triangle wave generator can be implemented using two high-speed op-amps, three resistors, and one capacitor. A typical layout for this implementation, provided by Maxim Integrated Products, is shown in Figure 3.11 [59]. The component values for this circuit can be adjusted to vary the frequency and amplitude of the triangle wave.

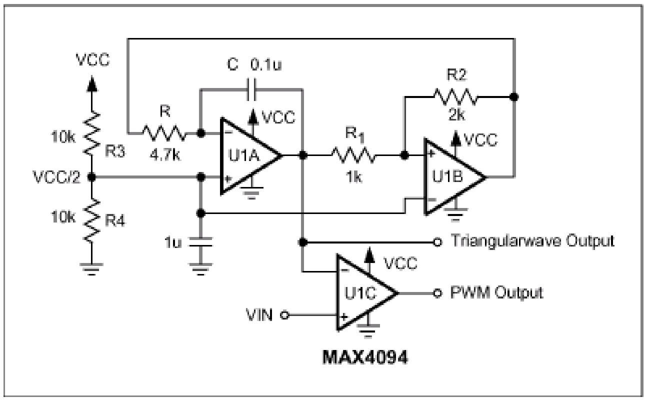


Figure 3.11 Triangle Wave Generator Design

This configuration operates with a single supply, labeled VCC. Typical values range from 5 V to 15 V. Configurations involving a dual power supply are also used in triangle wave generators, but with our limitation to a single supply, those configurations were not explored. The supply voltage powers the two main op-amps (U1A and U1B), and a voltage divider which provides a reference voltage of VCC/2.

The op-amp labeled U1B is connected in a Schmitt trigger configuration. If the noninverting input is greater the inverting input, the output will be driven to the positive rail. This is due to the positive feedback. If the inverting input is higher, then the output will be driven to the negative rail. This produces a square wave on the output terminal of U1B which is connected to the inverting input of U1A.

U1A is connected in an integrator configuration. The integrator integrates the square wave input, producing a triangle wave on its output. The triangle wave is fed into another op-amp (U1C) which is compared with an input voltage. This provides a PWM representation of the input, and is not relevant to the triangle wave generation process.

---

[59] http://media.maxim-ic.com/images/appnotes/3201/3201Fig01.gif

3.3.2. Desired Specifications

The desired specifications of our triangle wave were:

- Frequency: 200 kHz – 350 kHz
- Amplitude: ≥0.5 V_{pp}

According to the Nyquist Theorem [60], to represent a signal properly, it must be sampled at a rate greater than twice its maximum frequency. For our audio application, the minimum sampling frequency was calculated using the maximum audible frequency of 20 kHz:

$$f_s > 2 * f_{max} = 2 * 20 \text{ kHz} = 40 \text{ kHz}$$

To adhere to the Nyquist Theorem, we must sample at a rate of at least 40 kHz. To provide an ever better representation of the signal, we will not sample at the Nyquist rate, but rather at least 5 times that. The oversampling should yield an accurate representation of our input signal.

An amplitude of 0.5 V_{pp} was chosen based on the input specifications. For our design we took the input amplitude as a 0.8 V peak-to-peak sinusoidal waveform. In our three-level PWM design, the triangle wave should be shifted up and down to sample the bottom and top halves. When comparing the triangle wave to the input, it is imperative that the input never exceeds the range of the triangle wave. Any voltage outside the range of the triangle wave will not be sampled correctly and will lead to an inaccurate signal being amplified. To prevent this, an amplitude of 0.5 V was chosen. This is 25% greater than the maximum amplitude of the input and will allow the input to move freely within the range of the triangle wave and sample properly.

---

[60] (eFunda: Introduction to Nyquist Sampling Rate, 2007)

3.3.3. Simulation Results

To simulate our design, we constructed the following schematic in Multisim:

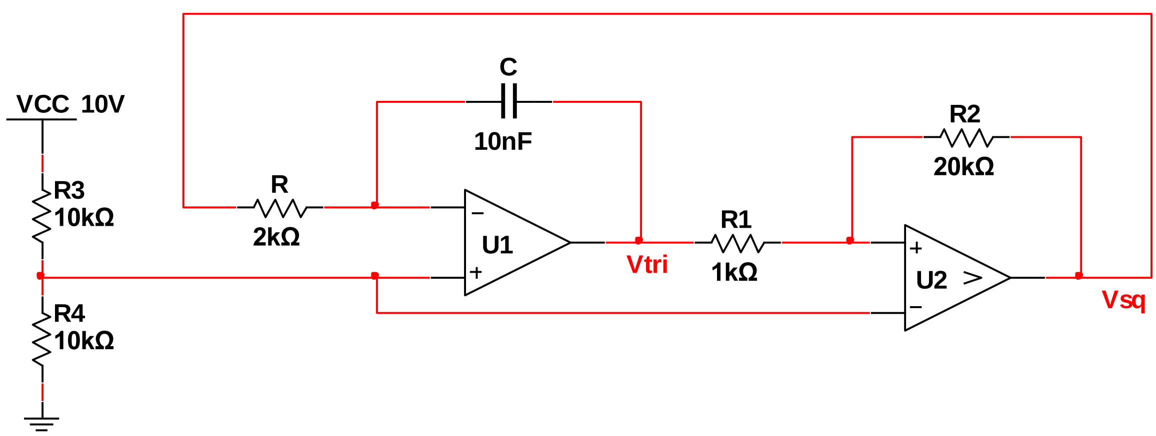


Figure 3.12 Triangle Wave Generator Simulation Circuit

The component values were determined based on the information provided from Maxim Integrated Products [61]. R_1 and R_2 were selected to have a 1-to-20 ratio. This set the amplitude of the triangle wave to a factor of 20 less than the supply, or 0.5 V.

$$V_{p-p} = \left(\frac{R_1}{R_2}\right) V_{CC} = \left(\frac{1\ \text{k}\Omega}{20\ \text{k}\Omega}\right) 10\ \text{V} = 0.5\ \text{V}$$

A frequency of 250 kHz was chosen for the simulation, and the remaining two component values were chosen based on that. A RC time constant of 20 µs was calculated:

$$f = \frac{R_2}{4RCR_1} = 250\ \text{kHz} \Rightarrow$$

$$RC = \frac{R_2}{4fR_1} = \frac{20\ \text{k}\Omega}{(4)(250\ \text{kHz})(1\ \text{k}\Omega)} = 20\ \mu\text{s}$$

R was chosen to be 2 kΩ and C was chosen to be 10 nF, creating the required time constant of 20 µs.

A reference of 5 V was created through a voltage divider consisting of two 10 kΩ resistors. This voltage determined the offset of the triangle wave. This could be altered as necessary to adjust the offset, but for simulation purposes a fixed offset of 5 V was chosen. This should place the triangle wave directly in the middle of the 0 to 10 V supply range.

[61] (Pulse-Width Modulator Operates at Various Levels of Frequency and Power, 2004)

The circuit was simulated with the Transient Analysis function in Multisim, and the resulting waveforms can be seen in Figure 3.13:

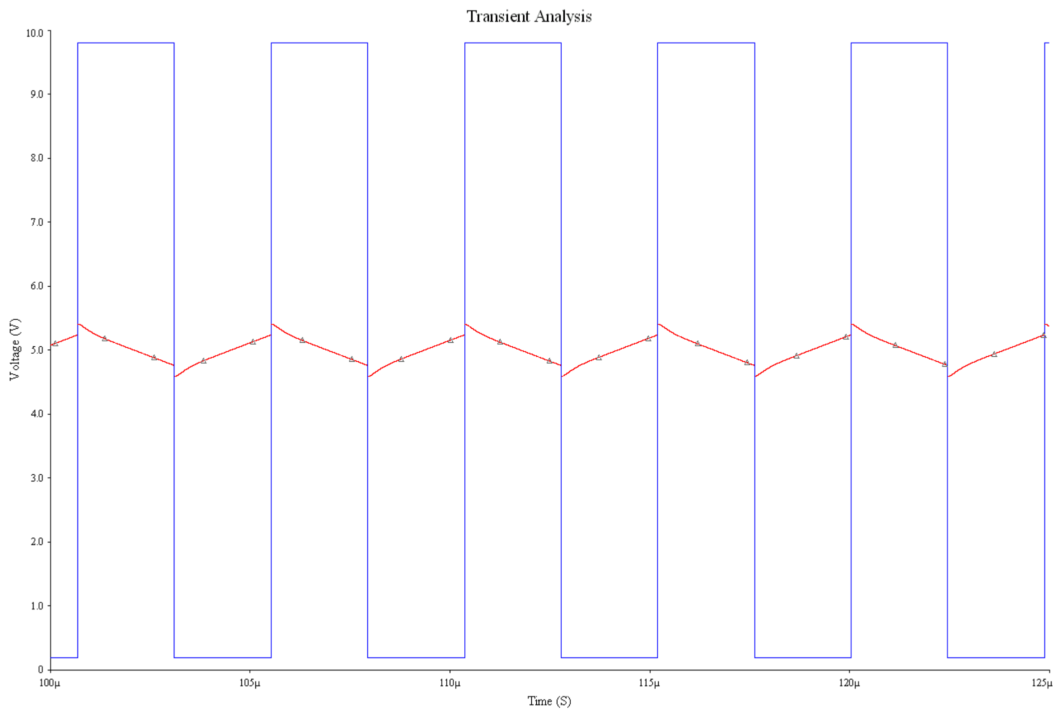


Figure 3.13 Triangle Wave Generator Simulation Waveforms – First Design

The square waveform is the output of the Schmitt trigger; the triangle waveform is the output of the integrator. The generated triangle wave was observed to be triangular in shape with amplitude of 0.65 V and a frequency of 200 kHz. The square wave did not ride on 0 V, therefore there was a DC offset. A DC offset can cause an inaccurate triangle wave.

This was not satisfactory, and the design was re-evaluated. A simple change was made to the circuit, and a drastic change was witnessed. The resistor R was increased by a factor of 100 to 200 kΩ and the capacitor C was decreased by a factor of 100 to 100 pF. The result waveform is shown in Figure 3.14.

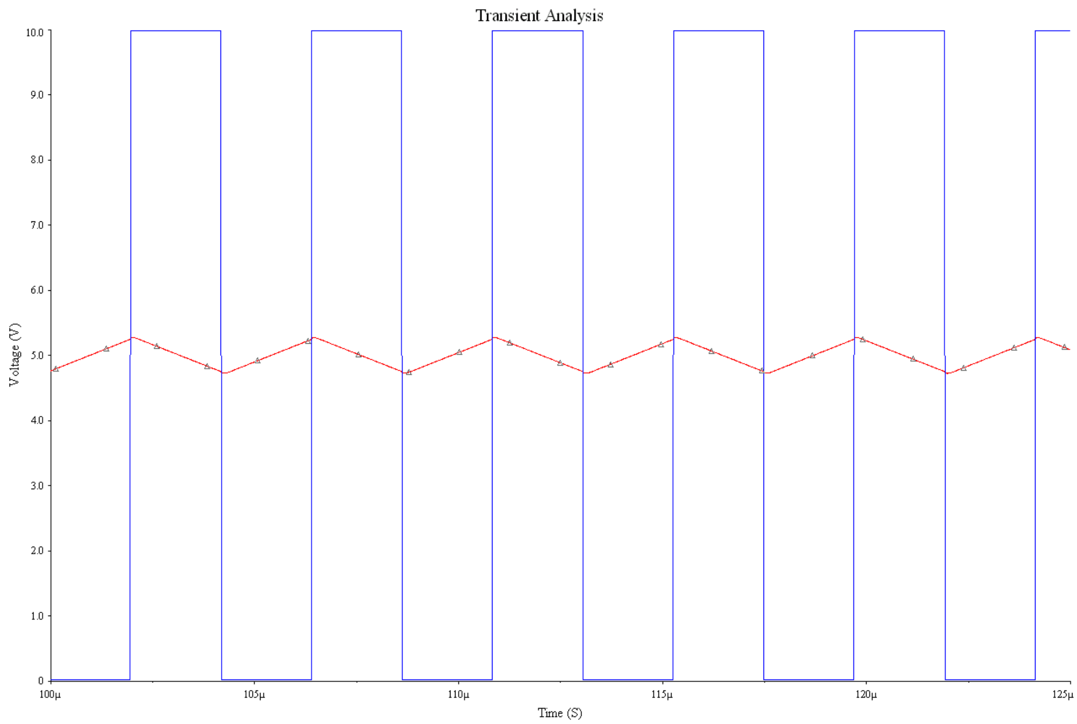


Figure 3.14 Triangle Waveform Simulation Waveforms – Second Design

The DC offset of the square wave was significantly decreased and the triangle wave was much cleaner. The amplitude was approximately 0.45 V and the frequency was 228 kHz. This was satisfactory, and with the circuit now designed using ideal components, real-world testing could begin.

3.3.4. Part Selection

The first step in constructing the designed triangle wave generator was to select the parts. The major parts of the triangle wave generator are the op-amps. For the op-amp in the integrator, we chose Texas Instruments' TLC274IN [62]. For the op-amp used in the Schmitt trigger circuit, Analog Devices' AD826 was chosen [63]. The resistors and capacitors were chosen based on their resistance and capacitance values, respectively. No additional characteristics of those components were investigated at the time of part selection.

---

[62] (tlc274.pdf, 2001)
[63] (AD826.pdf, 2000)

TLC274IN is a quad op-amp package that meets our specifications. The first specification considered in the selection of the op-amp was the supply voltage specification. Our target specification was a single supply from 0 V to 10 V. Any device in our system requiring a power supply would need to operate in that range in order to function properly. The TLC274IN can operate with a single supply in the range of 0V to 16V, this meets the supply specifications.

The second specification for the TLC274IN was the slew rate. The slew rate requirement for this device was calculated by finding the maximum change in voltage per change in time. The maximum change in voltage for the integrator output is equal to the 0.5 V peak to peak amplitude of the triangle wave. The minimum change in time is equal to the time the triangle takes to rise or fall the full 0.5 V, which is equal to half of the period. The period was determined based on a 600 kHz frequency. Since a frequency of 200 kHz to 350 kHz was desired in the end, if the op-amp could operate at 600 kHz it could operate in our target range easily. The slew rate was calculated as follows:

$$Slew\ Rate = \frac{dV}{dt} = \frac{V_{tri(p-p)}}{\left(\frac{1}{2}\right)\left(\frac{1}{f}\right)} = \frac{0.5\ \text{V}}{\left(\frac{1}{2}\right)\left(\frac{1}{600\ \text{kHz}}\right)} = 0.6\ {}^{\text{V}}/_{\mu\text{s}}$$

The TLC274IN op-amp meets the 0.6 ${}^{\text{V}}/_{\mu\text{s}}$ slew rate requirement, as it has a minimum slew rate of 3.5 ${}^{\text{V}}/_{\mu\text{s}}$. The typical value of 5.36 ${}^{\text{V}}/_{\mu\text{s}}$ will be plenty to integrate the square wave from the Schmitt trigger into our desired triangle wave.

The second op-amp, the one used in the Schmitt trigger configuration, was chosen to be an Analog Devices AD826. This is a dual, high-speed op-amp package. This op-amp produces the square wave output based on a triangle wave input. To generate a clean square wave, a very high slew rate is need. A slew rate of at least 100 times greater than the integrator is required. For our design, a minimum slew rate of 60 ${}^{\text{V}}/_{\mu\text{s}}$ is necessary. This is far exceeded by the AD826's specification of 350 ${}^{\text{V}}/_{\mu\text{s}}$ typical slew rate.

3.3.5. Testing

To test the triangle wave generator, the schematic was broken down into two sections and tested separately. The first section tested was the integrator, followed by the Schmitt trigger. The two sections were combined, as shown in Figure 3.15. This circuit did not function as intended at first, due to the inaccuracy in the component values. The values were modified until the desired output was observed on an oscilloscope. It was necessary to change the values due to the parasitic capacitance and other unexplained inaccuracies that arise whenever ever one uses a breadboard. Bypass capacitors were added as needed stabilize the supply and reference voltages.

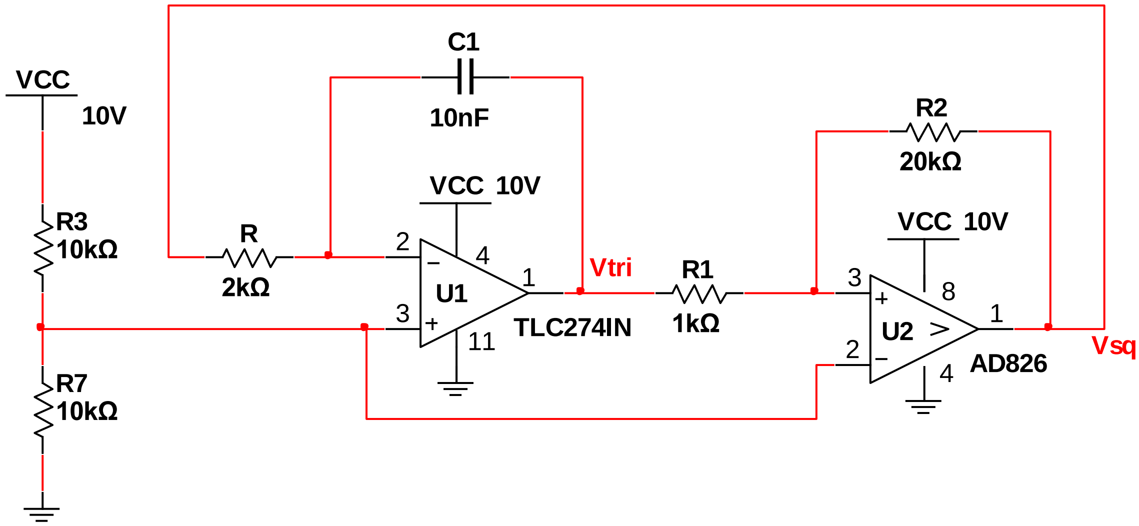


Figure 3.15 Triangle Wave Generator Schematic

Using an oscilloscope, the following waveforms were observed, as shown in Figure 3.16:

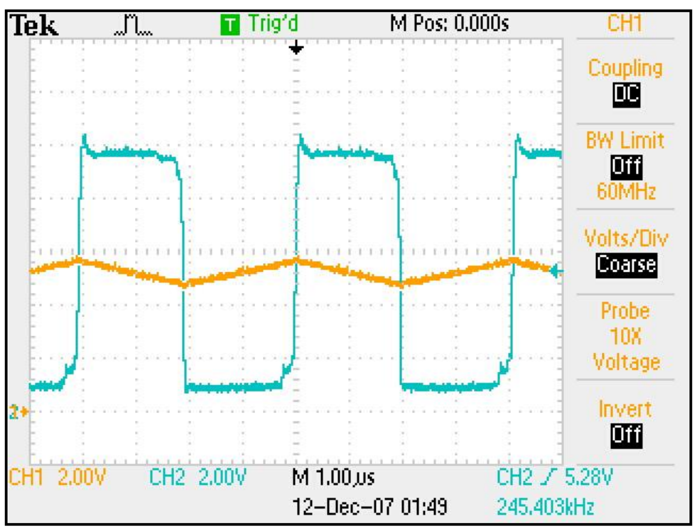


Figure 3.16 Oscilloscope Display Showing Triangle Wave Generator

V_{TRI} is displayed on CH1 and V_{SQ} is displayed on CH2. The generated triangle wave was measured to be 0.704 V peak-to-peak and have a frequency of 245.1 kHz. This was close to the desired output, but we felt that the triangle wave could be improved. We decided to try constructing a new triangle wave generator using just the AD826 dual op-amp and omitting the TLC274N. The results were striking; the single-chip triangle wave generator exceeded the complicated two-chip design in every regard. Figure 3.17 displays the final circuit used for the triangle wave generator.

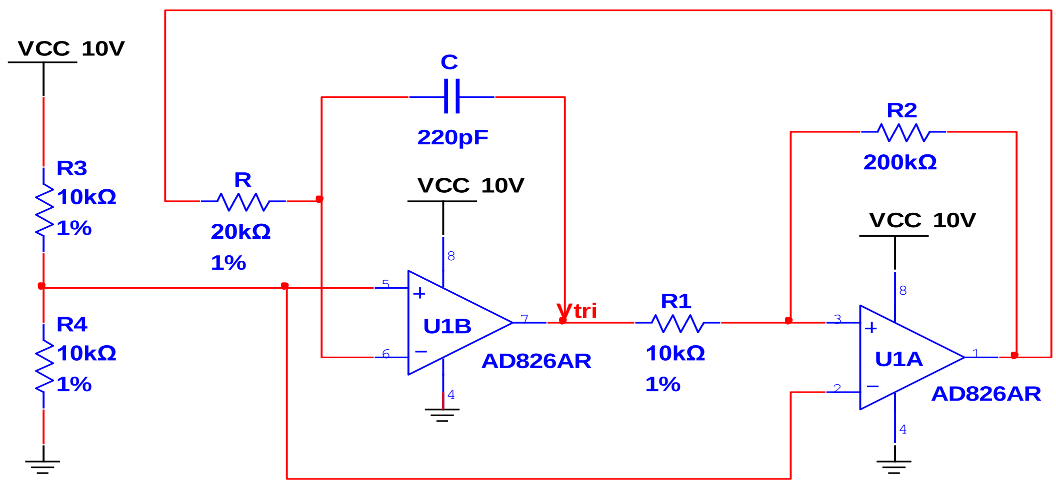


Figure 3.17 Final Triangle Wave Generator

The performance of the final triangle wage generator is discussed in detail in Section 5.1.2.

3.4. Spread Spectrum Design

Spread Spectrum can be implemented simply with a single IC. Maxim's DS1090 is a (relatively) low-frequency programmable spread-spectrum oscillator [64]. The IC outputs a square wave which varies in frequency to achieve Spread Spectrum. This square wave may then be amplified or buffered as necessary before it is integrated to produce a triangle wave of varying frequency.

Maxim offers this IC in a variety of packages, each with a different frequency range. The DS1090U-16+ is most suited for our application with a frequency range of 250 kHz to 500 kHz. The DS1090 can be programmed with external resistors to dither anywhere from 0% to 8%. It offers single supply operation from 3.0 V to 5.0 V. We will be running on a 10 V supply, so the voltage will need to be stepped down if we were to use this chip. The chip comes in one package, µSOP, and is therefore not suitable for breadboard prototyping work.

3.5. Feedback and System Stability

While the typical Class D amplifier is an open-loop design, several researchers have investigated the practical benefits of closed-loop feedback systems for audio as well. New Class D research by product manufacturers has resulted in more sophisticated feedback designs in a effort to reduce the

---

[64] (DS1090.pdf, 2007)

noise of the system [65]. While we have not implemented a feedback system in our own design, we have learned that a closed-loop system is a powerful tool for improving amplifier gain and linearity, reducing THD, and eliminating power loss from unintentional DC offsets. Feedback circuitry adds additional complexity to a Class D design, but as we will see, the potential benefits can be well worth the extra design time.

The simplest form of feedback in a Class D system involves sampling the output PWM waveform (before the filter) and combining the error signal with the input baseband audio [66]. Due to the switching energy contained in the feedback signal, the feedback system must be capable of filtering the signal before using it to modify the PWM system. Figure 3.18 below displays a block diagram of a simple feedback system proposed by Chang et al [67].

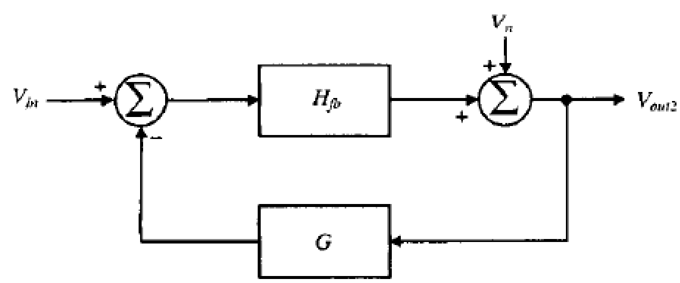


Figure 3.18 Simple Feedback System

---

[65] (Cox & Candy, 2006)
[66] (Leach, 2001)
[67] (Chang, Gwee, Lon, & Tan, 2001)

One simple feedback circuit is shown in Figure 3.19 for a half-bridge configuration [68]. In this circuit, the feedback voltage is proportional to the PWM values as a result of the integrating amplifier which effectively sets the feedback bandwidth.

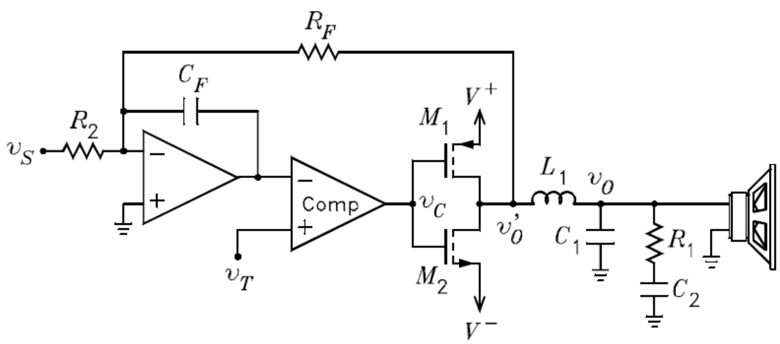


Figure 3.19 Feedback System For Half-Bridge

The amplifier also acts as a filter, removing much of the high-frequency energy from the feedback voltage. For a full-bridge configuration, Leach suggests the use of a differential amplifier (with filtering functionality thanks to capacitors C3) to subtract the two sampled signals before integration to achieve the same functionality as the half bridge feedback loop. This is shown in Figure 3.20 [69].

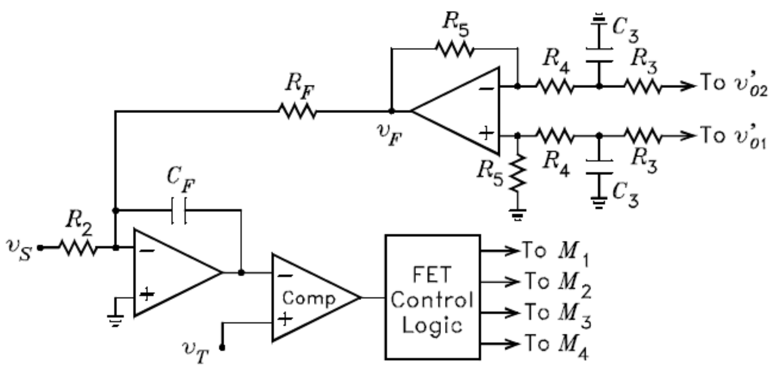


Figure 3.20 Feedback System For Full Bridge

Due to the high input impedance of the operational amplifier, the feedback process has a small effect on the output signal. Chang et al recommend using a feedback system with an overall gain of less than 1; amplification of the error signal would only serve to amplify the residual carrier frequency, thus making the system less stable [70].

---

[68] (Leach, 2001)
[69] (Lynch, 2001)
[70] (Chang, Gwee, Lon, & Tan, 2001)

Unfortunately, we were unable to design a stable feedback system for our own Class D amplifiers. As we will note in later sections, such a feedback system could have notably improved the performance of our system in several regards. We strongly recommend that any future Class D projects begin developing a feedback control system early on for their designs.

3.6. Power Stage

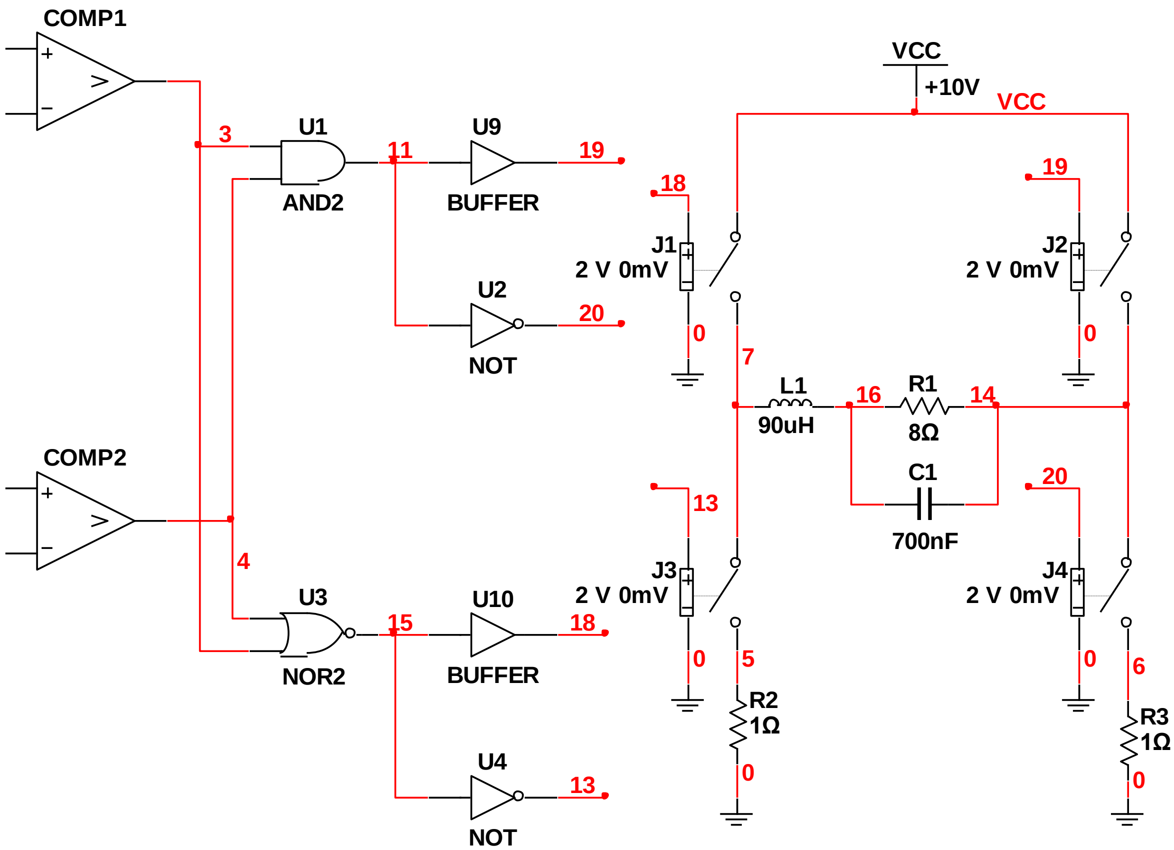


Figure 3.21 Circuit Diagram Of The Power Stage

In our three-level system, the power stage inputs are the outputs of the comparators, COMP1 and COMP2. This input signal is then altered by a logic gate stage to create a signal adapted for each individual MOSFET. The MOSFETs are represented in Figure 3.21 by voltage controlled switches (for simulation purposes). This resulting logic is then used to control the gate voltage of the MOSFET switches in our system. This change in gate voltage of the MOSFETs results in a change in the drain-source resistance, $R_{DS(on)}$ of the MOSFETs. This changing $R_{DS(on)}$ is the direct cause of the output signal being superimposed on the speaker, which we modeled as an 8 ohm resistance.

3.6.1. Power Supply

We have designed our circuit to operate on a steady 10.4 volt voltage source. In our model we treat the source as an ideal with no noise on the input voltage. We believe this treatment is justified because the application this circuit is designed for already has relatively tight requirements on the power supply. One situation where the non-ideal nature of the power supply will be evident is in the real world efficiency of the system. A voltage source also has a parasitic output resistance which reduces the efficiency of the system in which it is used. This parasitic resistance actually has one possible advantage. In the event that the two MOSFETs on either side of the full bridge are in their low $R_{DS(ON)}$ mode the parasitic resistance of the supply will act to limit the current being sourced. This can possibly reduce or prevent damage to the system.

3.6.2. Power Losses

At this stage we have isolated what we believe to be the major sources of power loss in our system. These major sources of loss will be the charging of the capacitive gates of the MOSFETS and the power losses due to the resistance of the power supply and $R_{DS(on)}$ of the MOSFETS. There are other causes of loss in our system such as the power costs associated with creating reference voltages, the triangle wave generation and the signal processing functions of the system. It has been estimated that these losses will be at least one order of magnitude smaller than our two primary sources of loss. In our system, the amount of wasted power due to the on resistance of the MOSFETs is shown in Equation 3.1.

$$P(R_{DS(on)}) = \left(\frac{V}{Rl + 2R_{DS(on)}}\right)^2 * 2 * R_{DS(on)}$$

Equation 3.1 Formula For Power Wasted By On Resistance of MOSFETs

Figure 3.22 shows the setup for the N-channel MOSFETs. There are 16 different on and off combinations for the four devices. However we only utilize two of these combinations (in the case of the two-level design) or three of these combinations (in the case of the three level design) to source power to the load. Both current paths will include two parasitic $R_{DS(on)}$ resistances in series with our load. The factor of two comes from the fact that when the power source is sinking power through load to ground, the current passes though two MOSFETs.

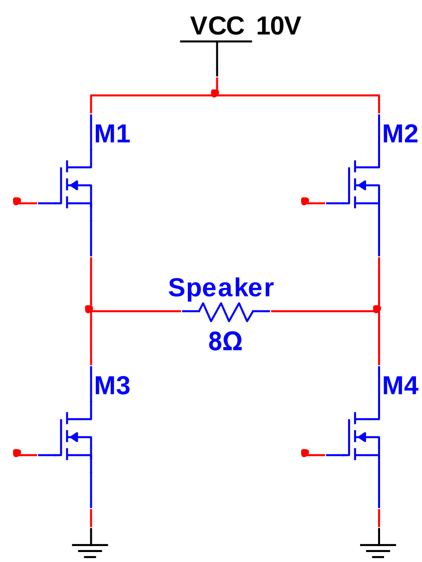


Figure 3.22 MOSFET Switching Scheme

Figure 3.23 shows the two current paths for the two-level switching scheme.

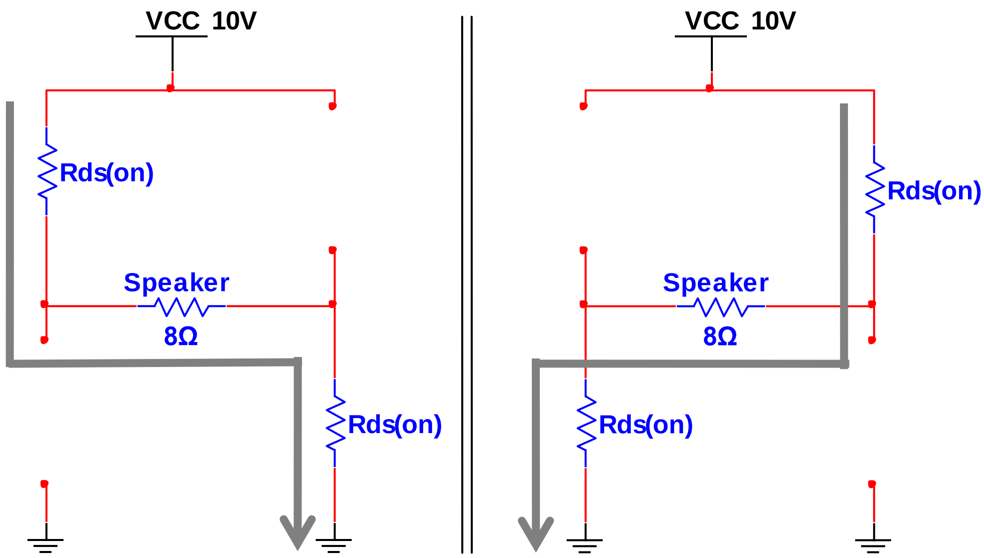


Figure 3.23 Current Paths for Two-Level Amplifier

The other major source of loss in our system is the switching loss associated with charging the gate capacitance of the MOSFETs. This loss is directly proportional the the frequency of the modulating signal and the MOSFET gate capacitance value. In our system we are typically only switching two MOSFETs on or off at any given time. In terms of power loss, this allows us to treat the system as if there are only two MOSFETs switching during each oscillation of the modulating signal. The resulting equation for the switching losses is Equation 3.2, shown below. The C in this formula is the gate capacitence of the MOSFETs. With this formula we assume that the capcitence is the same for all the MOSFETs. This can however be changed later on if we find it is worth while to select MOSFETs with different on-resistance and gate capacitance ratios.

$$P_{switching} = f_{modulator} C V^2$$

Equation 3.2 Equation For Switching Loses

This formula for the power loss is the result of the multiplication of the energy stored per capacitor multiplied by number of times a capacitor must be charged per second which is two times the frequency of the modulator.

The resulting equation for the efficiency of our system is shown in Equation 3.3. This formula is different than the formula used we started out using. There are several differences between the two equations; firstly, our equation yields twice the losses due to switching than the original equation did. This is due to the fact that the original equation was designed for a half bridge and we are using a full bridge. Secondly, at this point in our design the resistances of our PCB traces are unknown; however, we estimate that this resistance will be negligible and will not result in significant deviations from our power loss estimate.

$$\eta = \frac{P_{used}}{P_{used} + P_{wasted}} = \frac{\left(\frac{V}{RL + 2rds}\right)^2 * RL}{\left(\frac{V}{RL + 2rds}\right)^2 * RL + \left(\frac{V}{RL + 2rds}\right)^2 * 2rds + f_{modulator} * CV^2}$$

Equation 3.3 Formula For The Efficiency of The Amplifier

3.6.3. Control Logic

In our system when comparator 1 and comparator 2 are triggered we want the system to be applying a positive voltage from pins 7 to 14 of Figure 3.21 and when both the comparators are low we want the system to apply a negative voltage from pins 7 to 14. In any other situation we have designed the system to apply 0 volts between these two pins. The logic was chosen to make sure that at no time would either M1 and M3 or M2 and M4 be activated at the same time as this could potentially cause damage to the system. The choice to apply 0 volts between the two pins via shorting both pins to ground vs. shorting both of them to power was done for the perceived safety of the choice. The resulting logic table is shown in Table 3.6.

Comp 1	Comp2	M1	M2	M3	M4
0	0	0	1	1	0
0	1	0	0	1	1
1	0	0	0	1	1
1	1	1	0	0	1

Table 3.6 Logic Table for MOSFET Switching

3.6.4. Part Selection

Our primary concern with part selection for this functional block was to select MOSFETs with the lowest possible on-resistance and gate capacitance. The lower we could get these two parameters while maintaining functionality the better our efficiency would be. Our primary concern with these components was making sure to minimize the signal delay time, while also attempting to minimize the possible difference in signal propagation time to the MOSFETs. Any difference in signal delay time can introduce significant distortion in our output signal. When selecting components, the worst case scenario parameters were the numbers used to comply with the required specifications.

4. Project Schedules

4.1. Proposed Schedule for B Term 2007

Table 4.1 displays our proposed schedule for Term B 2007.

Week	*Dates*	*Tasks*
1	Tuesday, October 23 - Friday, October 26	**Complete project definition:** • List full target specifications • List desired features (primary and secondary) • Propose implementation for each feature • Begin adding equations and calculations to report
2	Monday, October 29 - Friday, November 2	**Circuit design for primary features** • Generate Circuit Diagrams • Simulate circuits • Begin part selection process • Choose secondary features to implement
3	Monday, November 5 - Friday, November 9	**Continue circuit design stage** • Implement secondary features into design
4	Monday, November 12 - Friday, November 16	**Draft final circuit schematics**
5	Monday, November 19 - Tuesday, November 20	**Draft first parts list and order parts**
6	Monday, November 26 - Friday, November 30	**Begin prototype construction** • Begin 1st PCB design
7	Monday, December 3 – Friday, December 7	**Prototype testing/debugging** • Revise schematics • Revise parts list • Design PCB layout
8	Monday, December 10 – Thursday, December 13	**Evaluate prototype** **Order first PCBs**

Table 4.1 Proposed Schedule For B Term

4.2. Proposed Schedule for C Term 2008

Table 4.2 displays our proposed schedule for Term C 2008.

Week	*Dates*	*Tasks*
1	Thursday, January 10- Friday, January 11	**Continue Lab Prototyping and PCB Design** • Update report as necessary • Evaluate design and testing methods • Become familiar with PCB design software • Evaluate last-minute additional features
2	Monday, January 14 - Friday, January 18	**Final Board Layout and PCB Design** • Design PCB to comply with EMI reduction techniques • Minimize device footprint • Create list of SMT/reduced-size parts • Include design options for secondary features
3	Monday, January 21 - Friday, January 25	**Order First PCB** • Evaluate PCB • Order additional parts
4	Monday, January 28 - Friday, February 1	**PCB Evaluation** • Learn how to test EMI • How to test for THD+N • Total system gain
5	Monday, February 4 - Friday, February 8	**Revise PCB Design** • Order 2nd PCB before weekend
6	Monday, February 11 - Friday, February 15	**Evaluate new PCB** • Revise if necessary • Begin documentation
7	Monday, February 18 – Friday, February 22	**Document the Testing Process** • Report writing: PCB design, testing & evaluation, results
8	Monday, February 25 – Thursday, February 28	**Finish Report**

Table 4.2 Proposed Schedule For C Term

5. Project Evolution and Design Changes

During C term, our development process accelerated significantly. Due to the lack of a mature three-level PWM prototype, we decided to proceed with the two-level design while continuing to develop the three-level circuit in the background. We began by selecting a final list of parts for the two-level board. We then proceeded to construct the two-level modulator on a breadboard and wire up our first power stage on a protoboard. After some minor changes, we then incorporated the newly matured two-level scheme into a Printed Circuit Board (PCB). This enabled us to work out many of the bugs in our power stage and obtain some valuable experience with PCB design tools that was very useful during the development of the three-level PCB later on.

5.1. Two-Level PWM Board

We wanted to get a PCB of the two-level board into our hands as quickly as possible, and therefore we were forced to rapidly develop a set of desired specifications and functionalities for the board itself. At the core of the design, our two-level modulator is a simple open-loop topology with a single fast comparator and a carefully balanced output stage. As we will see later on, however, the three-level design proved to have better overall performance.

5.1.1. Final Part Selection

Previously, we had constructed our triangle wave generator using two operational amplifier models: one for the integrating stage, and one faster op-amp for the comparison stage. Upon constructing a new triangle wave generator with just the AD826, however, we realized that the new single-chip waveform generator performed far better than the original design; it could deliver a clean triangle wave at much higher frequencies with far less distortion. We therefore decided to keep the AD826 triangle wave generator in the two-level to keep our component count down.

The second stage of the modulator design was the selection of a final comparator. We knew that we needed a fast comparator that could operate at high frequencies with a supply voltage of greater than 10 V. Therefore, we decided to use the standard National LM311 comparator that was included in our ECE lab kits. Furthermore, the NECAMSID lab had a sizeable stock of these chips, so we were able to further develop our modulator without waiting for parts to ship.

5.1.2. Breadboard Prototype and Issues

Construction of the two-level prototype began with the triangle wave generator. The first triangle wave generator built around the AD826 operated with a large peak-to-peak output amplitude that was later adjusted downward to better match a smaller input audio signal. Figure 5.1 displays the output waveform of the triangle wave generator.

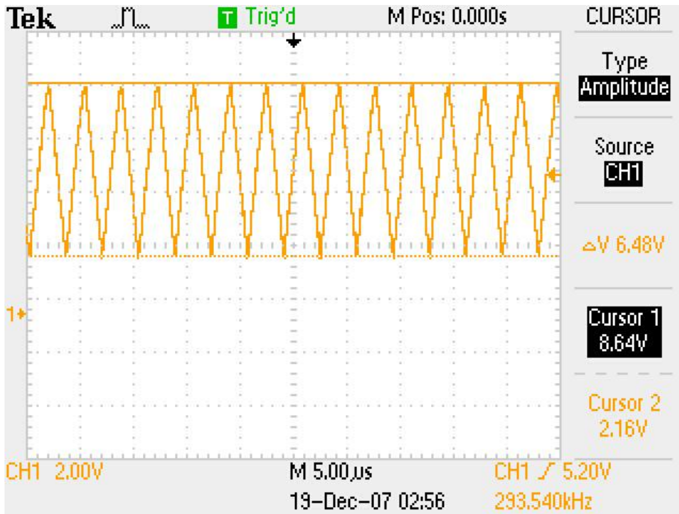


Figure 5.1 First Triangle Wave

Once the triangle wave generator was functional, we hooked up our comparator based on a reference feedback circuit from the datasheet in order to keep it stable. We then connected the triangle wave and input signal to the comparator; at the output, this yielded the desired PWM waveform.

Now that we had our PWM signal, the rest of the modulator was relatively simple to construct. We understood that the PWM signal would need to control the four n-channel MOSFETs in two alternating pairs; therefore, it was necessary to invert the PWM waveform to provide a differential signal to drive the power stage. Our original intent was to use a pair of dual FET drivers, one inverting (model TC1426) and one non-inverting (model TC1427). Early testing, however, showed that the two high-side MOSFETs (the two connected to the supply voltage in the H-bridge) were not fully turning on; this resulted in a high on-resistance and overheating of the chips. We needed a bootstrap driver for the high-side MOSFETs to turn them on fully and ensure proper operation of the power stage.

Fortunately, we had several other models of MOSFET drivers on-hand after ordering samples from other manufacturers. Instead of two dual FET drivers, therefore, we decided to implement a single full-bridge driver with bootstrap functionality, the Intersil HIP4081A. We chose to retain the TC1426 driver in the circuit and use it as an inverter, since the Intersil full-bridge driver did not have logic inputs. Figure 5.2 displays the final two-level schematic used for the breadboard and PCB prototypes.

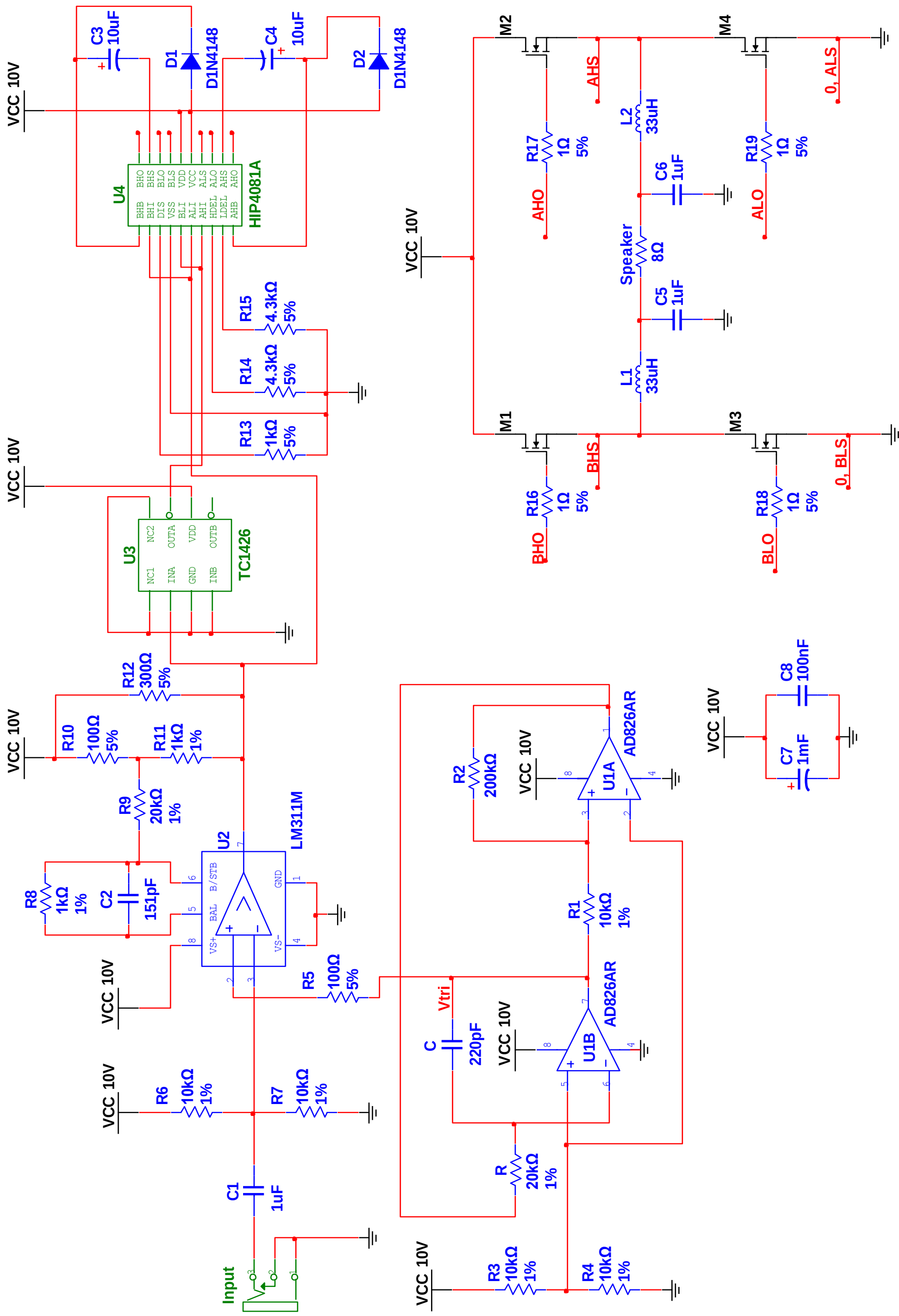


Figure 5.2 Final Two-level Schematic

The two-level breadboard prototype is shown in Figure 5.3. At the displayed stage, the modulator (left) is not yet attached to the driver chip on the right side. The TC1426 chip (functioning as an inverter) is also not present.

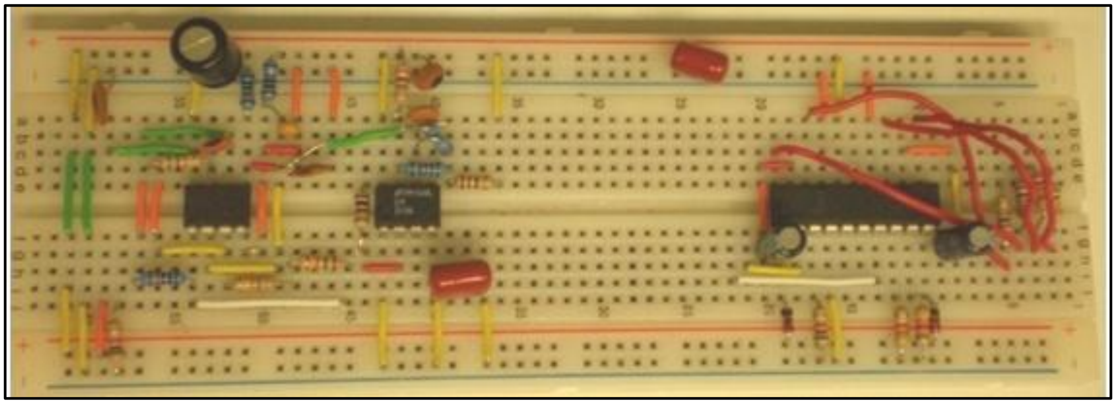


Figure 5.3: Two-level Modulator On Breadboard

We decided early on that it would be impossible for us to fully test our amplifier on breadboards. The power stage alone would draw over 1 A during operation with an 8 Ω load; pulling this amount of current through a breadboard would cause overheating and scoring at best, and would likely cause the board to melt entirely. Since we had already constructed the modulator stage on a breadboard, we hooked up the FET driver IC on the board as well in order to keep the wires between modulator and driver as short as possible. We then constructed our power stage on a protoboard; this included the filter inductors and capacitors, power MOSFETs, and an output jack for attaching the load. This version of the power stage was used to test the breadboard implementation of both the two-level and three-level designs. Figure 5.4 shows the protoboard power stage attached to the driver IC with bridging wires.

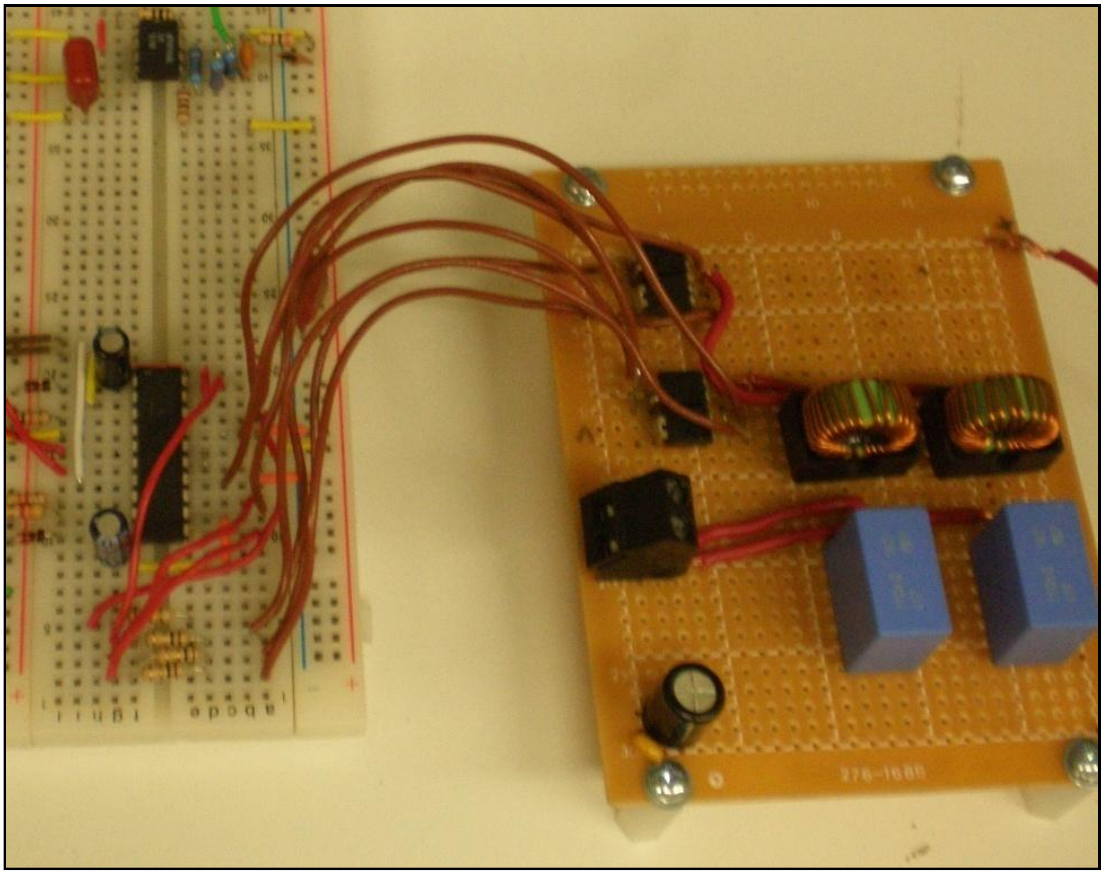


Figure 5.4 Power Stage Attached to Modulator

One of the first issues we ran into with this two-level prototype was the placement of probes for measuring our signals. For high-frequency signals, we found that the oscilloscope would display a much cleaner waveform when we attached the scope probes to a ground close to the measurement point. For measuring across the load itself, it was necessary to use two probes to measure the differential voltage between the two halves of the full bridge. Furthermore, when using dual power supplies (one for the modulator and one for the power stage), we found that creating a common ground between the two reduced some of the noise in the output signal.

5.1.3. First PCB

Our first PCB was created to test our two-level design. The process started with our two-level schematic, presented earlier in Figure 5.2. Once the schematic was determined to be accurate and all the connections were correct, the footprints of all the parts needed to be specified in Multisim. For our first PCB design, we chose through-hole DIP packages for components whenever possible, as they are generally easier to solder than surface mount packages. Since we were concerned with functionality over size, space-saving surface mount components were not explored in this first PCB design.

With the footprints assigned to all the components, we then exported the Multisim file to a PCB layout software package. The schematic files in Multisim export to a PCB layout software called Ultiboard. Using the Ultiboard software, the footprints of all the components were double checked. This was done by first printing the Ultiboard layout to scale and then placing all the components on the printout and verifying they matched up exactly. The input jack, filter inductors, and filter capacitors were created using Ultiboard's component wizard, as those components had packages that were not present in Ultiboard's default library. Once a custom footprint is created, it can be accessed by the user in future revisions. This was very helpful when creating the three-level PCB later on.

We designed the layout of the components next. Using the Ultiboard software, the components were first arranged on the board. As the size of the board was not important in this first PCB design, the size was chosen to be the default size created by Ultiboard size, 6.5'' x 4''. Components were grouped inside the board outline depending on their stage from left to right.

Once the components were laid out in the desired positions, it was time to wire them up. First, two inner planes were added to the design. The positive supply was assigned to the first inner layer, and ground was assigned to second. This was done by adding a "power plane" in Ultiboard. The addition of inner supply layers is typically done to reduce noise on the system, as well as reduce the number of traces on the top and bottom copper layers.

Traces of width 15 mil were added to connect the components. While the default width in Ultiboard is 10 mil, 15 mil was chosen to minimize trace resistance based on the recommendation of Professor Bitar. Wider traces of 25 mil and 35 mil were used in the power stage because of the higher current flow in the stage. Whenever possible, traces on the top copper layer were drawn horizontally and traces on the bottom copper layer were drawn vertically.

Vias were added whenever two traces were going to cross. With a via, or plated hole, a trace can be diverted to any of the other layers of the board, resolving any conflicts. Vias were also used to connect surface mount parts to the inner layers, as the surface mount pad is only part of the top copper layer while the vias pass by all the layers.

BNC jacks were added to the board, and connected to five signals: input, triangle wave, PWM output, left speaker output, and right speaker output. These connectors allow for easy hookup to an oscilloscope using BNC to BNC cables. Left and right outputs were provided so the MATH function of the oscilloscope could be used to output the differential output, which is the true audio output. In addition the BNC jacks, banana jacks were also added to the design. These were used to provide an easy and secure connection to the power supply with banana to banana wires.

To keep PCB boards off the ground, nylon supports were attached to the board with screws. These are helpful to prevent any shorting when the board is placed directly on conductive surfaces. To accommodate the supports, four holes were placed in each corner of the board.

Also, text with the project name, student names, date, and revision number was added. This was done to distinguish the board from other projects and any future revisions of this board. The PCB design was then complete. The top layer of the design is shown in Figure 5.5.

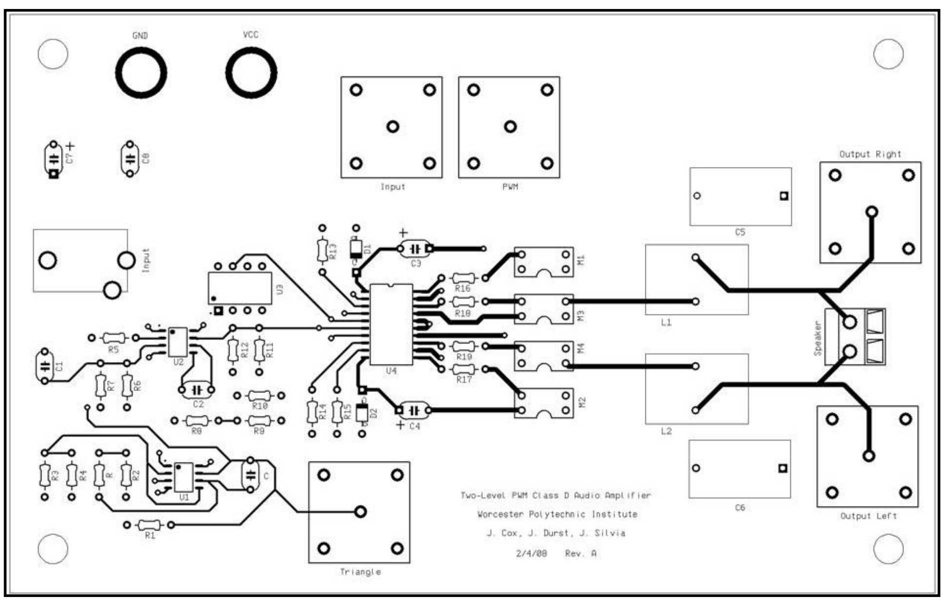


Figure 5.5 Two-level Ultiboard Layout (Top)

The first inner layer, the power plane, is shown in Figure 5.6.

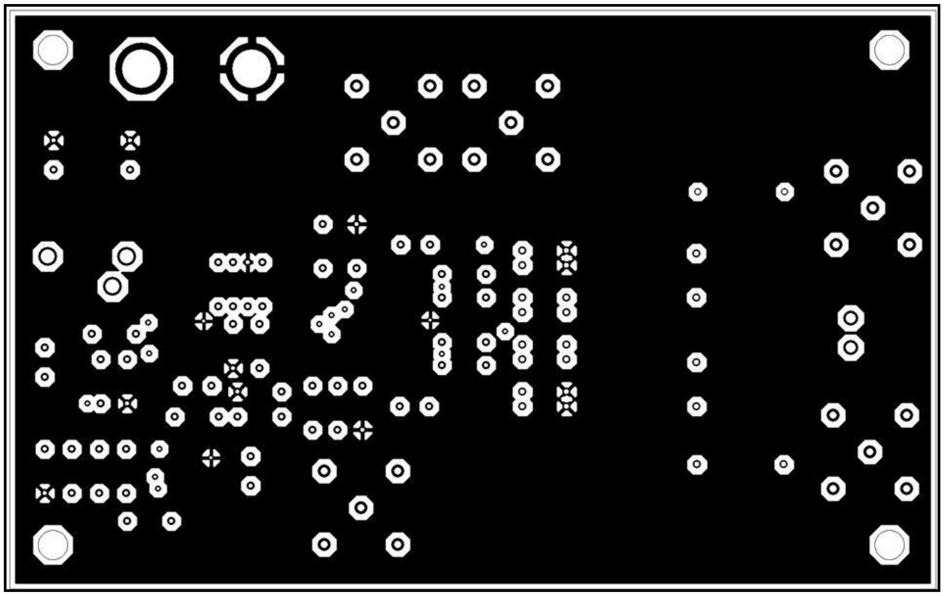


Figure 5.6 Two-level Ultiboard Layout (Power Plane)

The second inner layer, the ground plane, is shown in Figure 5.7.

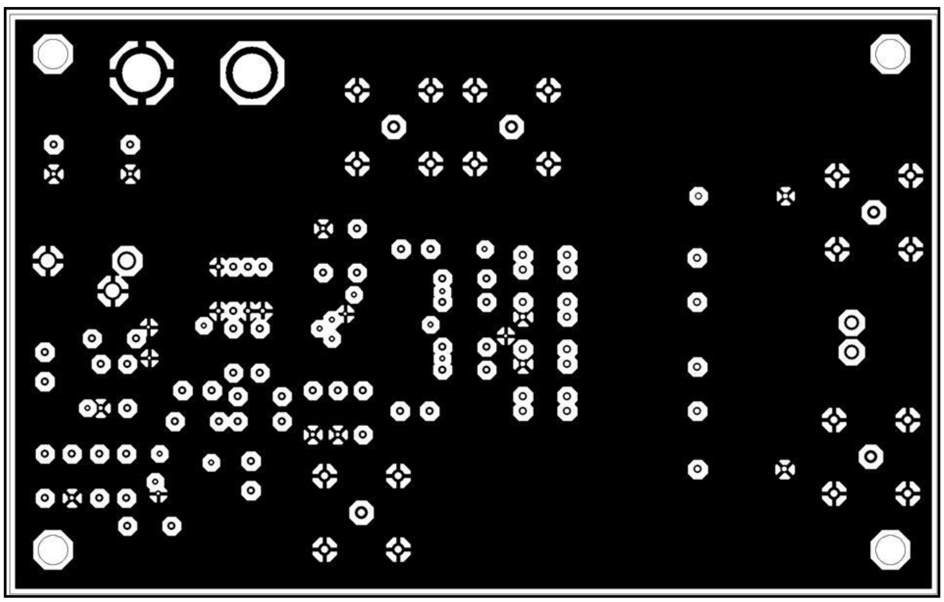


Figure 5.7 Two-level Ultiboard Layout (Ground Plane)

The bottom layer is shown in Figure 5.8.

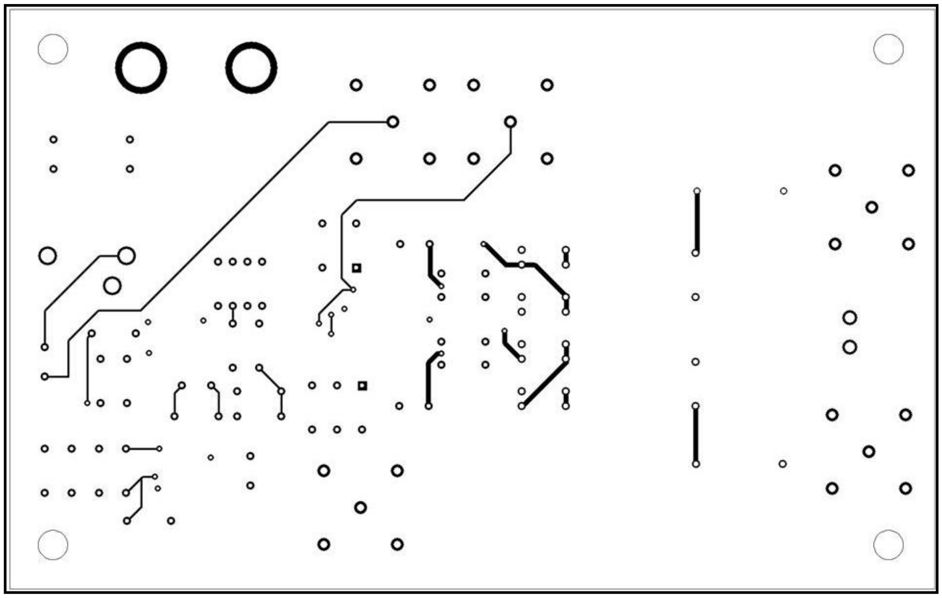


Figure 5.8 Two-level Ultiboard Layout (Bottom)

We then proceeded to export our design to Gerber files. Gerber files are the files which PCB manufacturers require in order to process your order. They provide the PCB manufacturer with all the necessary information about the board. Once these files were created, it was time to upload them to a PCB manufacturer.

Advanced Circuits was chosen as our manufactured based on recommendations of other students. Their website and ordering procedure, at first glance, appeared to be simple and straight forward. They also had a good reputation, which was highly desirable. Furthermore, Advanced Circuits provides a free Gerber file check which scans Gerber files and makes sure that the board can be processed with no errors. Advanced Circuits claims that checking the Gerber files with their free checker will save up to 48% of time from order placement to shipment [71].

The majority of errors uncovered in the first check involved the limitation of the manufacturing process. Ultiboard's default size for text and solder pad sizes was smaller than Advanced Circuits could manufacture. Because of this, all the text and pads were increased in size to meet the manufacturer's specifications. These were eventually corrected and after a few tries, the design was error free and compatible with Advanced Circuits' system. With the board error free, it was time to place the order. Five boards were ordered, as they were having a buy four, get one free promotion.

---

[71] (Advanced Circuits, 2007)

The manufacturing took five business days and shipping an additional two days. Pictures of one of the five blank PCB boards as they were received are shown in Figure 5.9 and Figure 5.10.

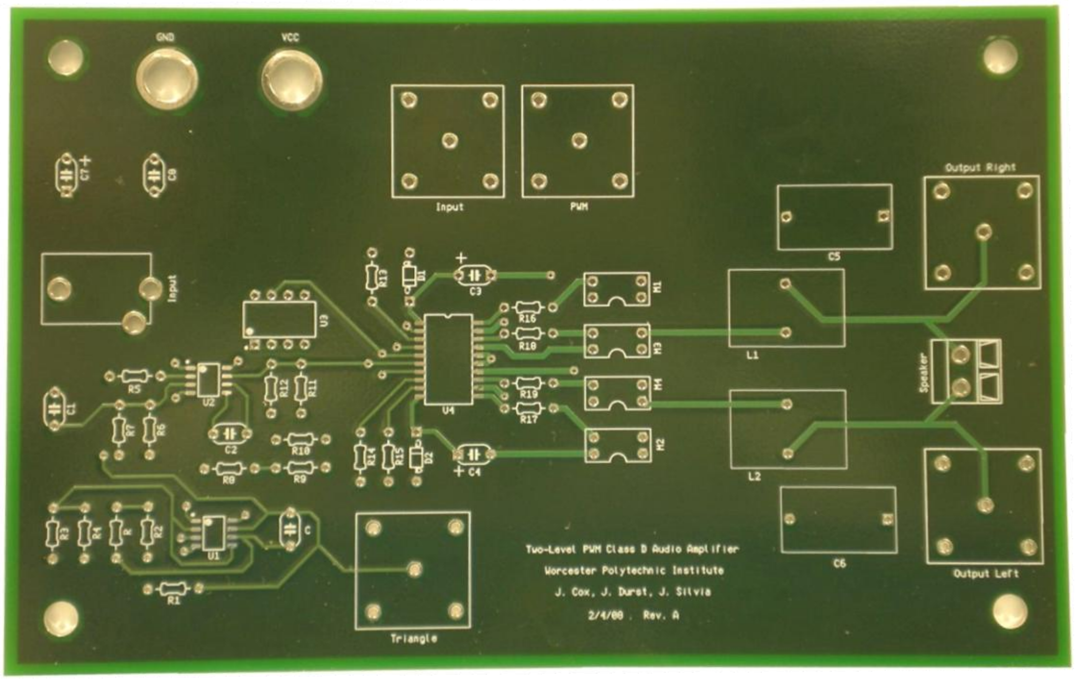


Figure 5.9 Two-level Blank PCB (Top)

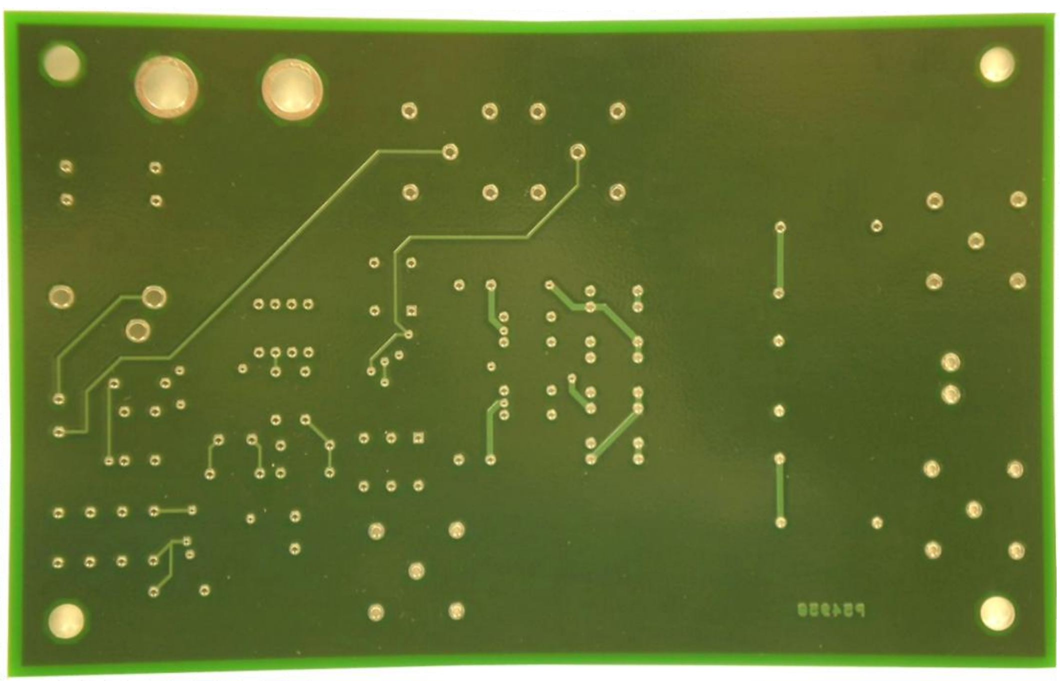


Figure 5.10 Two-level Blank PCB (Bottom)

Once the boards were received, we went right to work testing and assembling. The first task was to test the connections of all the traces. Using a multimeter's continuity test, each connection in our system was tested to verify the connections were properly placed. After all the connections were verified, it was determined that the board was manufactured perfectly.

The only problems with the design were the drilled support holes. While these were minor problems, they are worth noting as they were the only errors in this PCB design. When creating a hole in Ultiboard, you supply the radius of the hole. We provided the diameter of our support screws, thus creating a hole that was twice as large as it needed to be. Luckily, the screw heads were larger than the holes and the screws were able to tighten securely, providing a solid support for the board. Also four supports were not enough for the board. The middle of the board was bowing slightly, which is not good for the solder joints. This effect was corrected in the three-level design by adding two additional supports in the middle of the board.

Once the connections were tested and the supports were added, it was time to fully assemble the board. The first components to be soldered were the three surface mount components. These were soldered first as they were the hardest to solder. The first, and only, soldering problem occurred with the first chip to be soldered. We accidentally soldered the chip in backwards, not noting the dot location. While trying to remove the incorrectly placed chip, traces and pads were lifted, rendering this board useless. While this may seem to be a negative issue, it was not. The board was not completely useless, as we now had a scrap board to practice our soldering and de-soldering on. Having a practice board helped prevent any further mistakes while soldering.

After the surface mount connections were made, the through-hole components were added. The through-hole components were installed easily with no errors in the soldering process. The BNC and banana jacks were added next, and the system was fully assembled. The assembled board is shown in Figure 5.11.

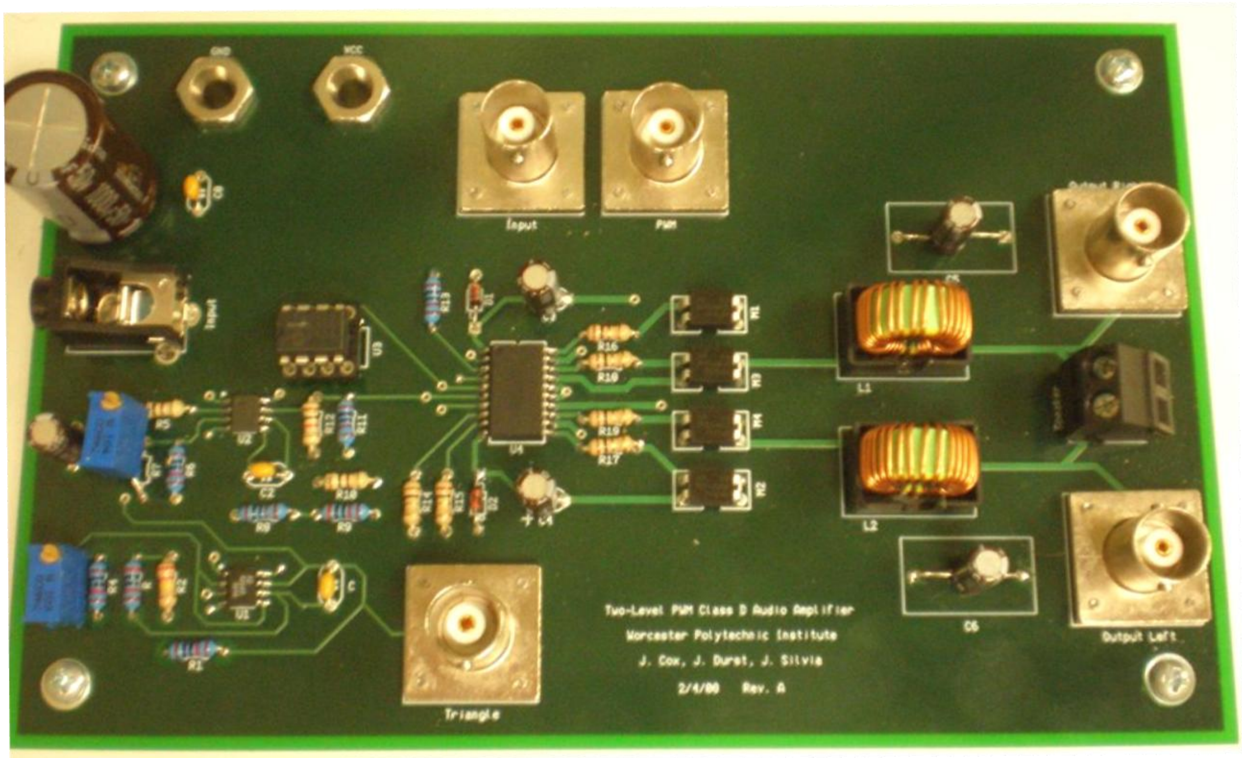


Figure 5.11 Two-level Assembled PCB (Top)

It should be noted that the filter capacitors are smaller than their outline because the original capacitors were replaced with smaller, low equivalent series resistance (ESR) capacitors.

The triangle wave was observed first and it was noted that it was not the desired frequency and amplitude. The triangle wave was approximately 500 kHz and 6 V peak-to-peak. To fix this, the capacitor, C, was replaced with a 220 pF capacitor. The resistor R_2 was then adjusted via potentiometer until the triangle wave had a frequency and amplitude close to the desired value of 300 kHz and 1 V peak-to-peak, respectively. The potentiometer was then replaced with a fixed resistor value. The final value of R_2 was 200 kΩ. This obtained a 397 kHz, 1.24 V peak-to-peak wave, riding on 5.2 V, which was much closer to the desired values. The resulting waveform is shown in Figure 5.12.

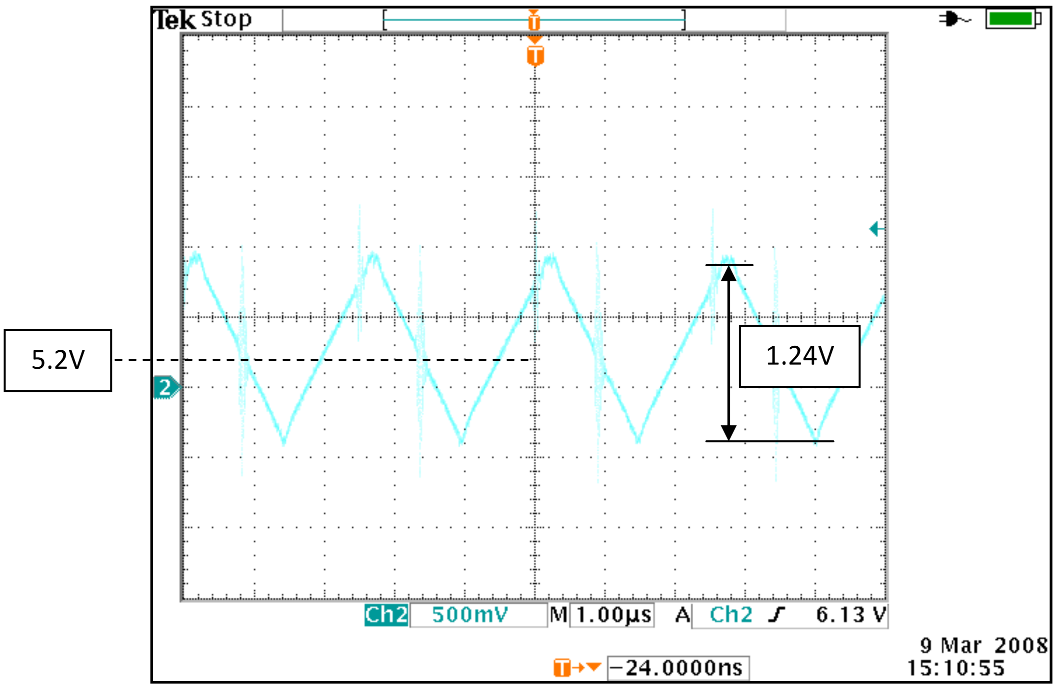


Figure 5.12 Two-level Triangle Wave Waveform

With the triangle wave functioning properly, the input stage was tested. The input, after AC coupling, had a DC offset equal to half of the supply, or 5.2 V, regardless of the actual input DC offset. The amplitude was not attenuated unless the frequency was lowered under 100 Hz, which was expected from the high-pass filter in the AC coupling circuit. A potentiometer was substituted for one of the resistors in the AC coupling circuit so the DC offset of the input could be adjusted. This was necessary to line up the triangle wave and input perfectly. The input signal is shown in Figure 5.13.

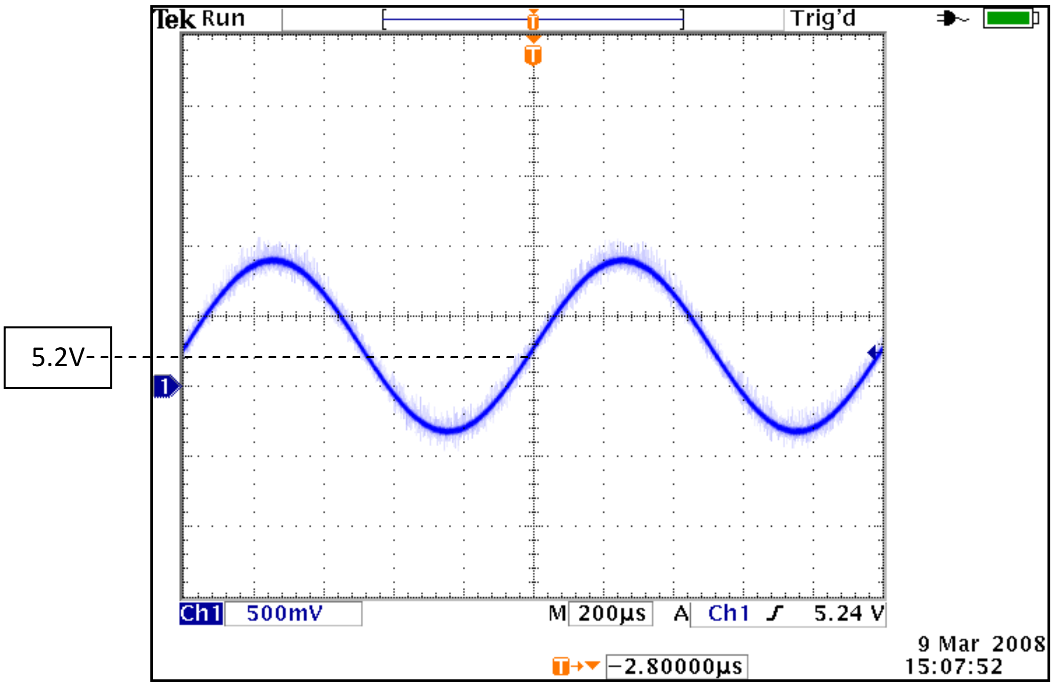


Figure 5.13 Two-level Input Waveform

With the triangle wave and the input functioning correctly, it was verified that the two signals lined up with each other, as seen in Figure 5.14.

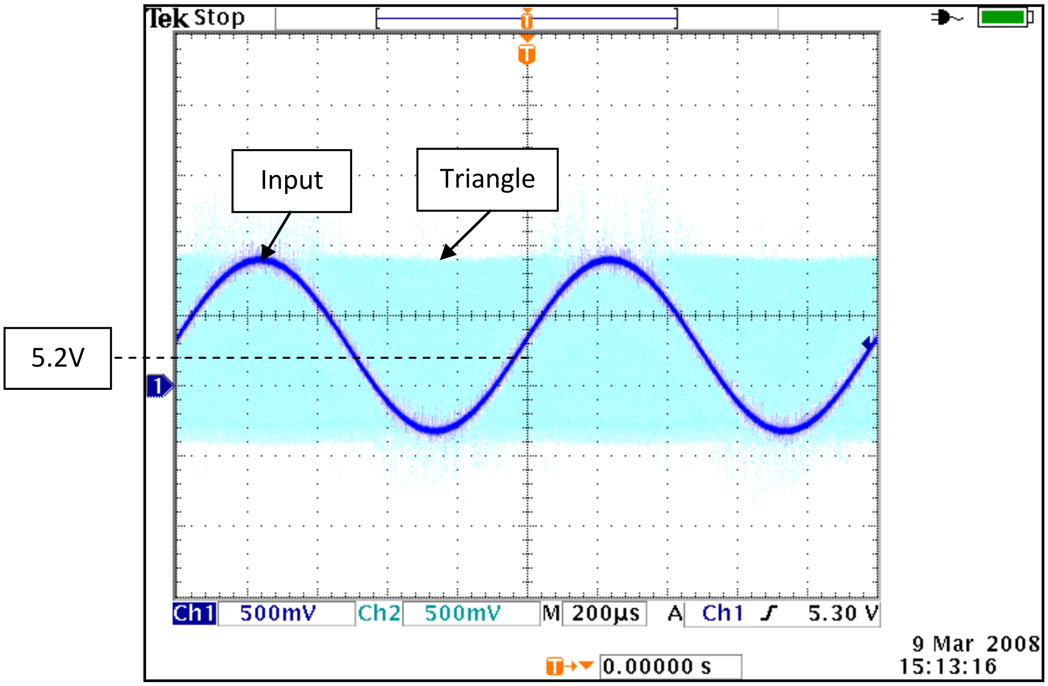


Figure 5.14 Two-level Input and Triangle Wave Waveforms

PWM output was observed to also function properly. As seen in Figure 5.15, the duty cycle of the PWM output varied depending on the input voltage. The minimum and maximum duty cycles occurred at the maximum and minimum input voltages, respectively. A 0.3 V DC offset was also observed on the PWM output.

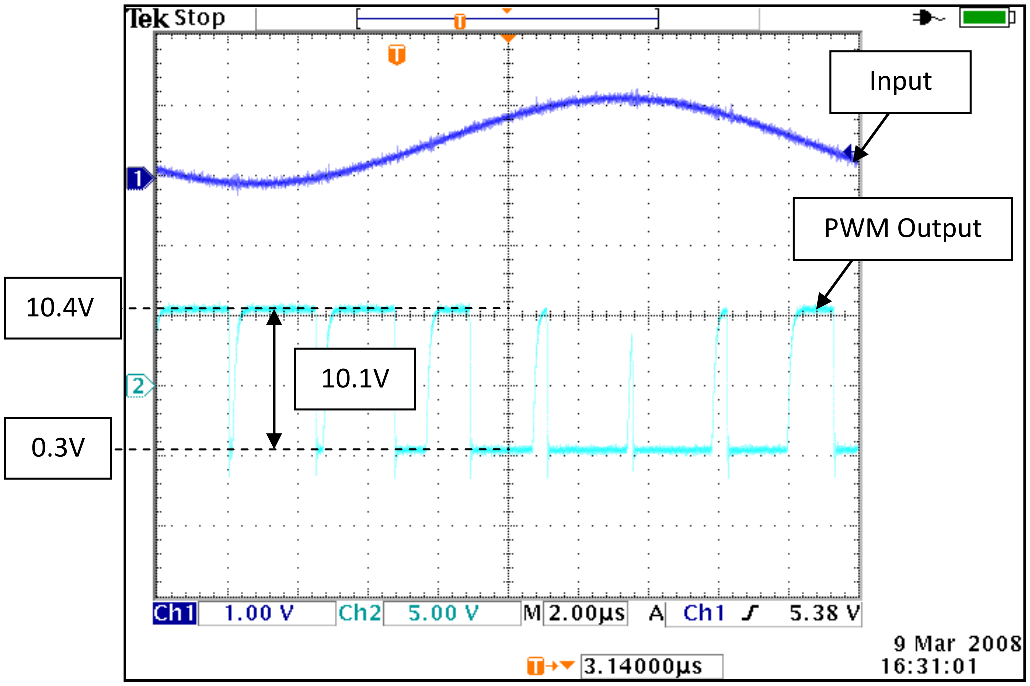


Figure 5.15 Two-level PWM Waveform

The logic stage, consisting of a single inverting chip, functioned properly. The PWM signal coming out of the inverter was a perfect inversion of the input. This was fed into the driver which outputted the same control signals to the gates of the MOSFETs, only with more current.

The full system was then tested, and noise was observed on the triangle wave, occurring whenever the MOSFETs were switching. The output was also not reliable, as it appeared to be severely frequency dependent. These problems were partially due to the lack of bypass capacitors. Bypass capacitors were added to our design, directly across the supply terminals of the ICs. The locations of the capacitors are shown in Figure 5.16.

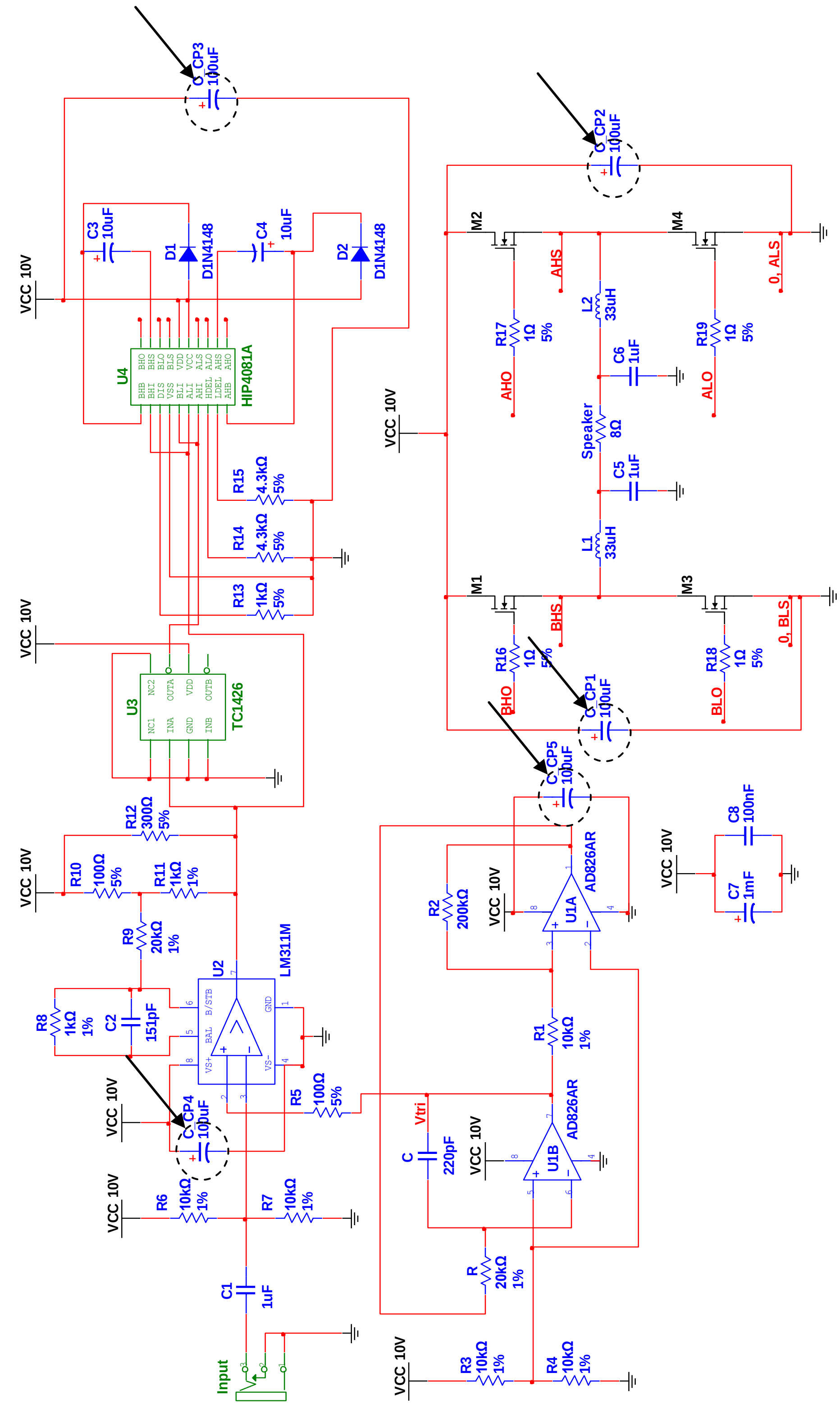


Figure 5.16 Two-level Schematic with Bypass Capacitors

The capacitors were added to the assembled PCB on the bottom, as seen in Figure 5.17.

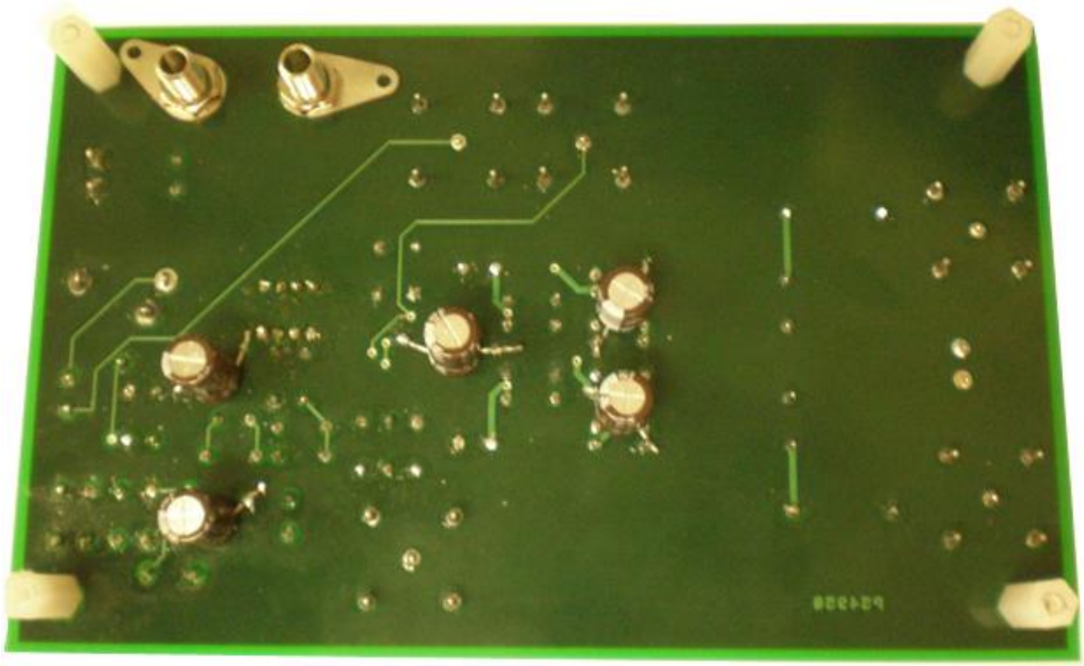


Figure 5.17 Two-level PCB Assembled with Bypass Capacitors (Bottom)

The addition of bypass capacitors significantly reduced the noise in the system. It was also observed that the output functioned as expected, and for a wide range of frequencies. When inputting a signal, a larger signal resulted as the output. Figure 5.18 shows the input signal and the two output signals (the left and right sides of the H-bridge).

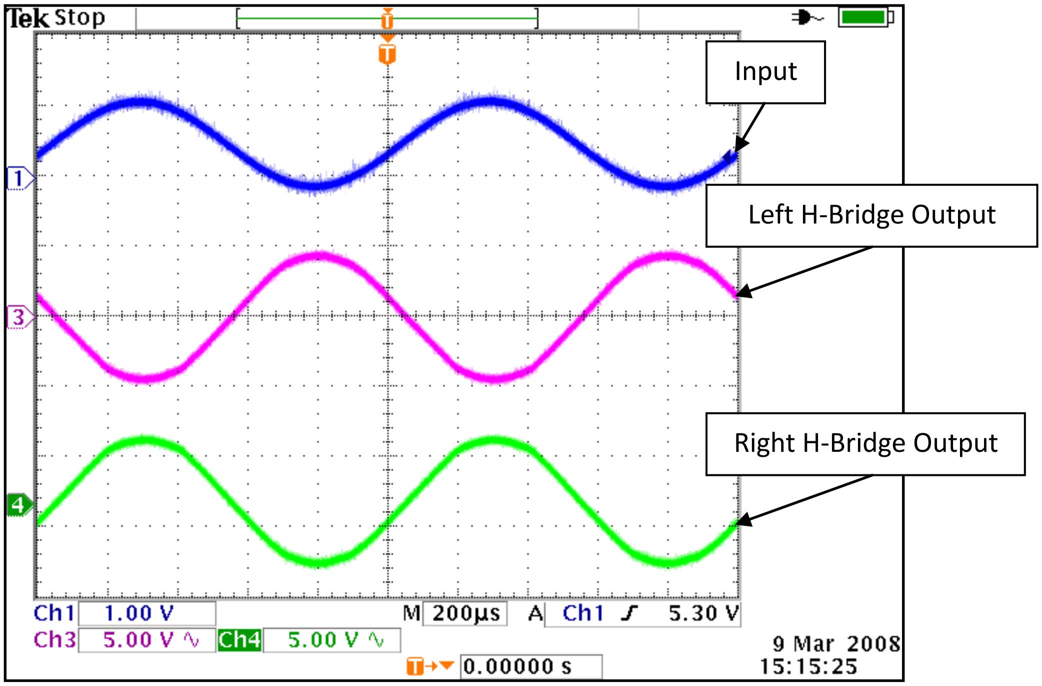


Figure 5.18 Two-level Input and Output Waveforms

The differential output was plotted using the Math function of the oscilloscope. As seen in Figure 5.19, the output was a linear scaling of the input.

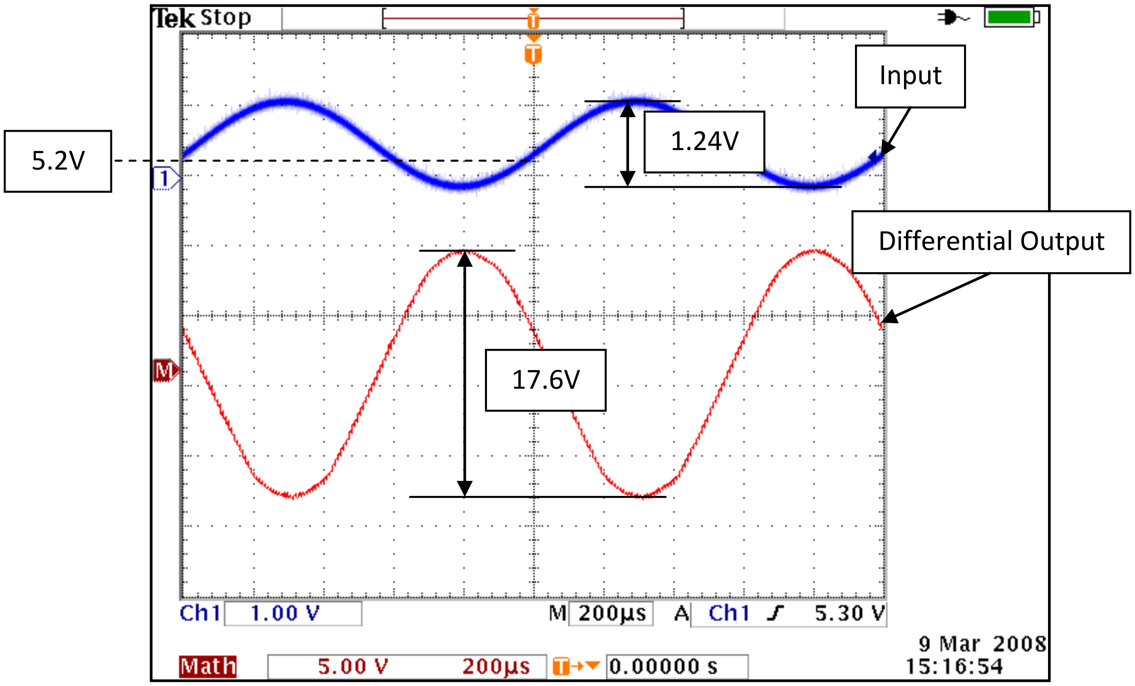


Figure 5.19 Two-level Input and Differential Output (MATH) Waveforms

This confirmed the fact that our two-level system was indeed a functional amplifier.

5.2. Three-Level PWM Board

The schematic used to design the three-level PCB board is shown in Figure 5.20.

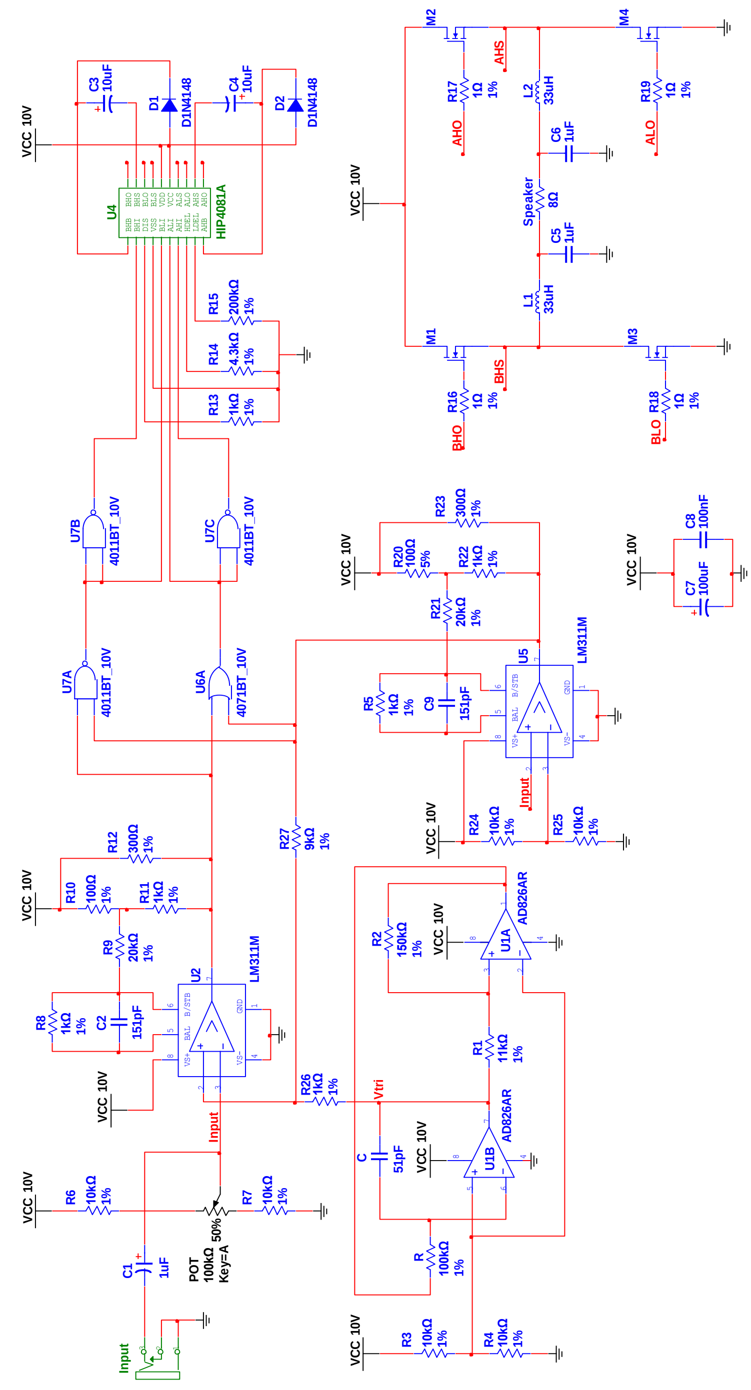


Figure 5.20 Final Three Level Schematic With Actual Components

Our final three-level design incorporates several individual stages. First in the lower left side of Figure 5.20 is our triangle wave generator U1. This triangle wave generator operates independently of the rest of the circuit. Comparators U2 and U5 compare the input signal to an adjusted triangle wave and a reference voltage. The triangle wave offset is dictated by comparator U5, which adds a DC offset to the triangle wave to “follow” the input signal when it goes positive or negative. The resulting PWM waveforms are than processed by the logic gates in chips U7 and U6. The output of these logic gates is the driver signal to each of the 4 MOSFETs. The output of the logic gates however is connected to the inputs of the driver chip U4. This chip then drives the gates of the MOSFETs. This switching pattern of these MOSFETs drives power though the Butterworth low-pass filter formed by inductors L1 and L2 and capacitors C5 and C6. The speaker will then experience an amplified version of the input sinusoidal waveform.

5.2.1. Final Component Selection

In this section we will list and discuss our choice of major components and the reasoning behind each decision. In general, the major issues in deciding which component to use in each situation included energy efficiency, output quality and size. Each component had a different weighting for each one of these characteristics. The final component list was as follows:

- AD826AR - High-Speed, Low-Power Dual Operational Amplifier
- CD4011B - Quad CMOS NAND Gate
- CD4071B - Quad CMOS Or Gate
- LM311M - Voltage Comparator
- HIP4081AIBZ - 80V/2.5A Peak, High Frequency Full Bridge FET Driver
- ZXMN4A06GCT - 40V N-Channel Enhancement Mode MOSFET
- DC630R - High Current Power Line Chokes (Inductor)
- PW Series Capacitors
- RC1206 – General Purpose Chip Resistors

One of the first choices on components we had to make was what chip should we use to make our triangle wave generator. We chose the AD826AR. The AD826AR met all our requirements as far as operating voltage supply and power consumption. Our choice to go with this chip over other chips was dual op-amp package. This gave us the two comparators we needed while not giving us too many which would have wasted space and power. Another characteristic was its slew rate. We needed to drive a 10 volt square wave on a capacitive load. We needed an op-amp which could drive the current in an acceptable time.

We chose the CD4011B for several reasons. The primary reason why we decided on this chip was the fact that we were having substantial problems trying to find any other chip which would meet our requirements of operating at a 10V input and output voltage swing. The choice to go with the 4 gate package was due to the fact that we needed an inverter as well. We were able to configure two NAND gates as inverters and this allowed us to save room on our board by reducing the number of chips needed. The CD4071B was selected for the same supply voltage capabilities of the CD4011B. These chips also have lower power dissipation compared to other logic solutions.

The LM311 comparator was chosen because it met our desired specifications for slew rate and voltage supply that we required. We sacrificed some degree of efficiency for functionality. We decided to continue using this component from the original two-level circuit despite its relative inefficiency.

The HIP4081AIBZ full bridge driver chip was chosen due to its bootstrap functionality. This chip allowed us to drive 4 MOSFETs with individual signals for each chip. The bootstrap functionality allowed us to apply gate voltages to the MOSFETs at levels equal to or greater than the 10 volt supply to the driver chip. The lower power dissipation of this chip was also a plus.

The ZXMN4A06GCT MOSFETs were chosen because of their very low maximum RDs and their low gate capacitance. These low values make a very significant difference in the efficiency of the system. These chips also had a high maximum current rating and a high maximum drain to source rating. This was important because if decided these higher ratings would allow us to apply significantly more power to our load.

DC630R inductors were chosen because of their low series resistance. For our application we did not want to be dissipating significant amounts of power in our filter. We selected inductors with significant current handling capabilities since our maximum deliverable current would dictate our maximum supply voltage and therefore our power output at the load.

The PW series capacitors were chosen because of their small ESR and small package size. Here, we needed to compromise between package size and ESR. Our amplifier is a design which would lend itself towards mobile applications, so component size was a major concern for us.

The RC1206 series resistors were chosen due to their small size and low percent variation. For our design to have smaller trace lengths it was beneficial for us to have smaller resistors. This gave us more control over the layout of the PCB. The low tolerance was necessary due to the fact that our voltage references needed to be balanced to a high degree of precision.

5.2.2. Breadboard Prototype and Issues

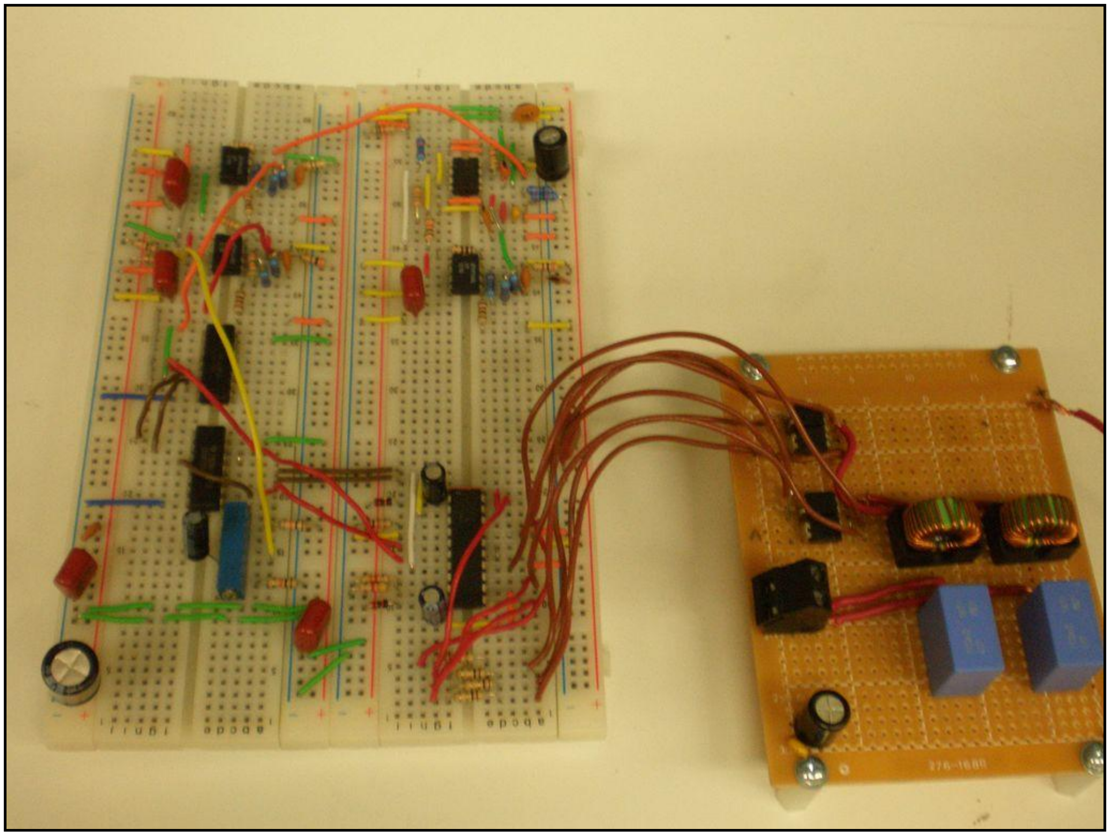


Figure 5.21 Three Level Breadboard

For our three-level prototype we used through-hole versions of the surface-mount chips we would use later in our PCB design. One of the major issues we had with the initial prototype was the significant amount of noise on our power rails. To build our prototype we used two breadboards tied together. Even with multiple bypass capacitors in place, we were startled to discover 1.2 V_{pp} noise between supply rails on opposite sides of the breadboards. Although this was disconcerting, this noise was also present on our two-level design and had little noticeable effect on the output signal.

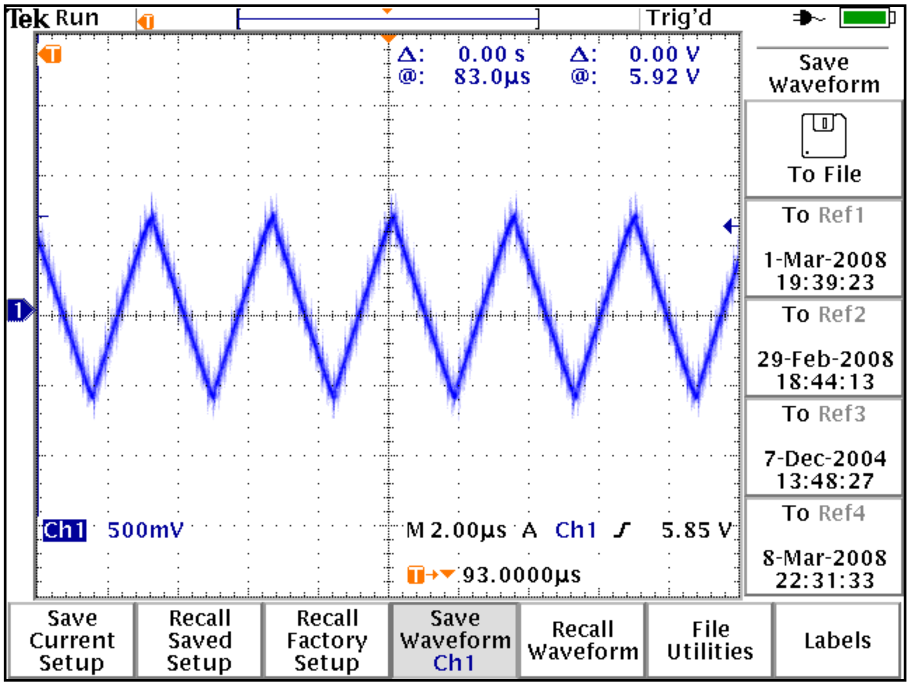


Figure 5.22 Three level Triangle Wave (Pre-shifting)

In the end, we were able to get a relatively clean output signal from our three-level prototype based on our oscilloscope observations. This was misleading, however. The output signal contained a significant amount of audible noise. This may be attributed to the power supply noise we observed during testing; furthermore, breadboards are not known for being good environments for high-frequency signals such as our MOSFET driving square waves. Figure 5.23 displays the MOSFET control signals as observed on the breadboard.

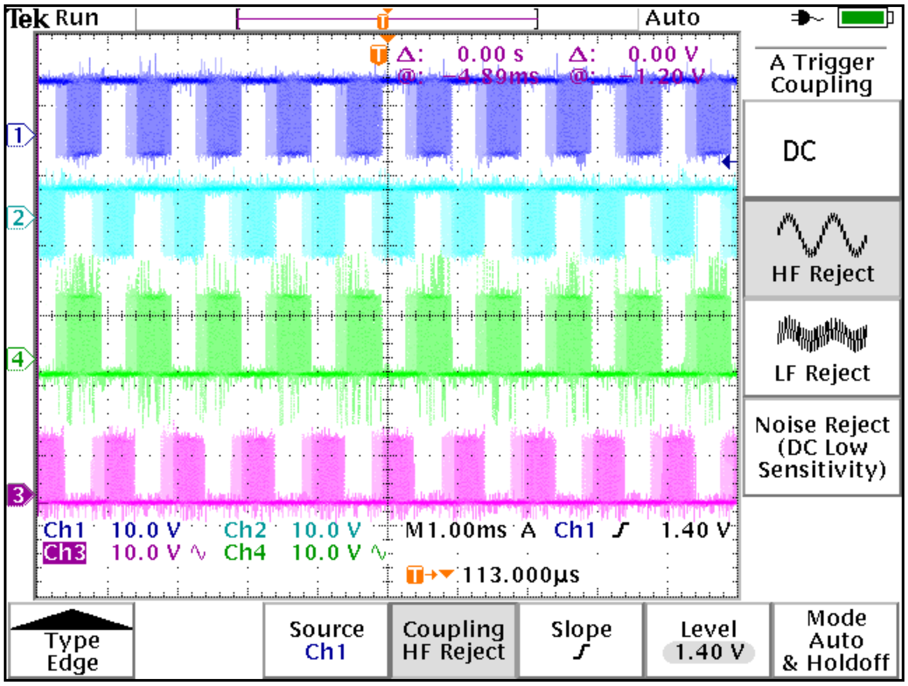


Figure 5.23 MOSFET Gate Control Signals.

The final output audio signal had more noise than we would have liked, but the audio signal was high enough quality to be recognizable. We decided to proceed with the PCB design for the three-level board.

5.2.3. First PCB

The design process for the three-level PCB was essentially the same as the two-level process discussed earlier. The process started with our three-level schematic, presented earlier in Figure 5.20. The footprints of the new parts were specified in Multisim. Footprints from the two-level design were preserved in the Multisim file, so it was not necessary to add them again. This saved substantial time in the three-level PCB design process.

Since this was our second PCB design, we decided to try using surface mount packages. The two-level PCB had been assembled relatively easily; the three-level PCB was designed to be 1cm shorter, even though the number of parts had increased. This was achieved by using the space-saving surface mount components.

With the footprints assigned to all the components, we then exported the Multisim file to the Ultiboard software, and the footprints of all the components were double checked. This was done again by first printing the Ultiboard layout to scale and then placing all the components on the printout to verifying that they matched up exactly. The input jack, filter inductors, and filter capacitors did not need to be created again using Ultiboard's component wizard, as those components had packages that were saved from the previous design.

The layout of the components was designed next. Using the Ultiboard software, the components were first arranged on the board. As the size of the board was not changed in this PCB design, the size remained approximately the same as before (6.5'' x 4''). Components were grouped inside the board outline depending on their stage from left to right.

Once the components were laid out in the desired positions, it was time to wire them up. Two inner planes were added to the design, just as was done in the two-level design. The positive supply was assigned to the first inner layer, and ground was assigned to second. The positive supply plane was split in half, to create a dual supply board. The left half of the plane powered everything up to the power stage and the right half of the plane powered the power stage exclusively.

Traces of width 15mil were added to connect the components. Wider traces of up 300mil were used in the power stage because of the significantly higher current that could possibly flow in the stage. As was done in the two-level design, traces on the top copper layer were drawn horizontally and traces on the bottom copper layer were drawn vertically whenever possible.

Vias, BNC jacks, and text were added to the board in the same manner as the two-level design. The diameter of the support holes was corrected and two extra supports were added in the center of the board to prevent bowing. The three-level PCB design was then complete. The top layer of the design is shown in Figure 5.24.

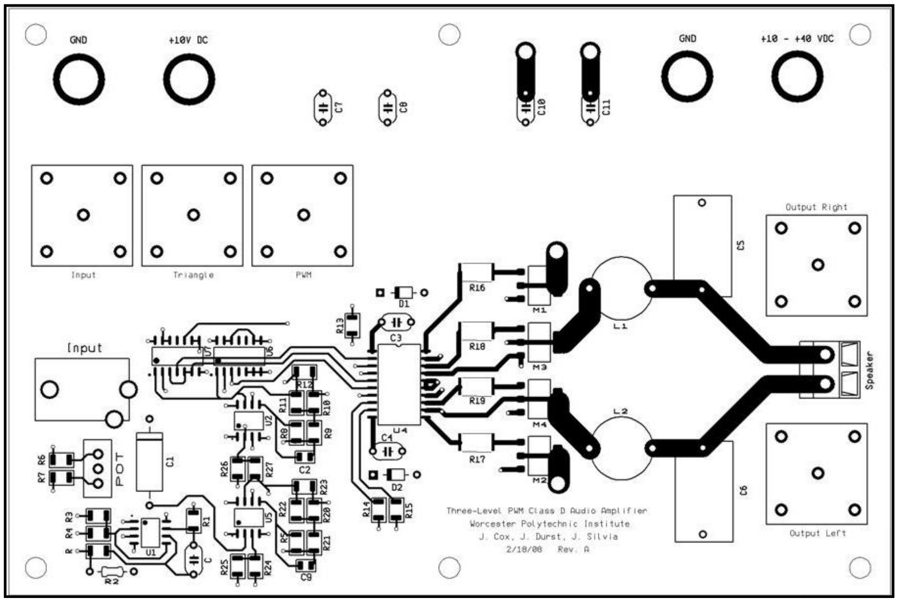


Figure 5.24 Three-level Ultiboard Layout (Top)

The first inner layer, the power plane, is shown in Figure 5.25.

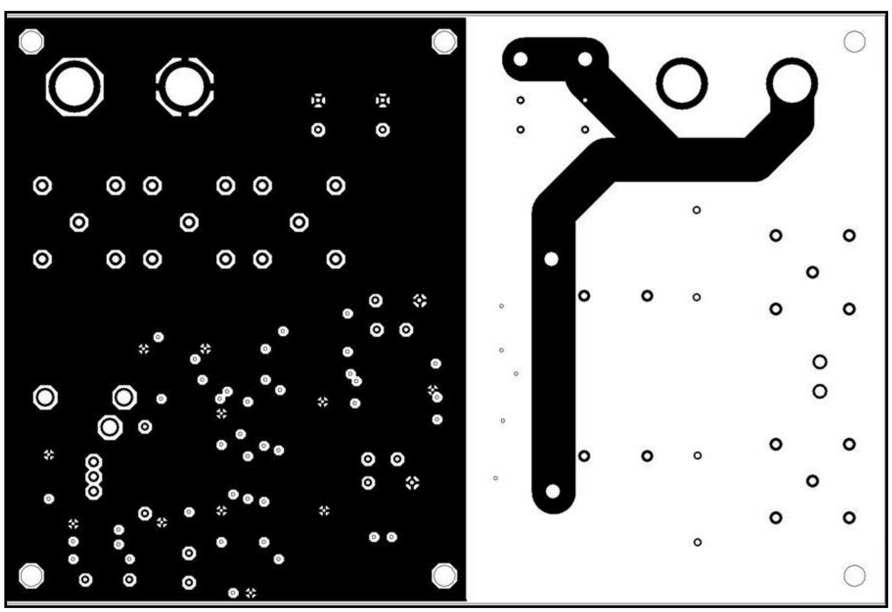


Figure 5.25 Three-level Ultiboard Layout (Power Plane)

The second inner layer, the ground plane, is shown in Figure 5.26

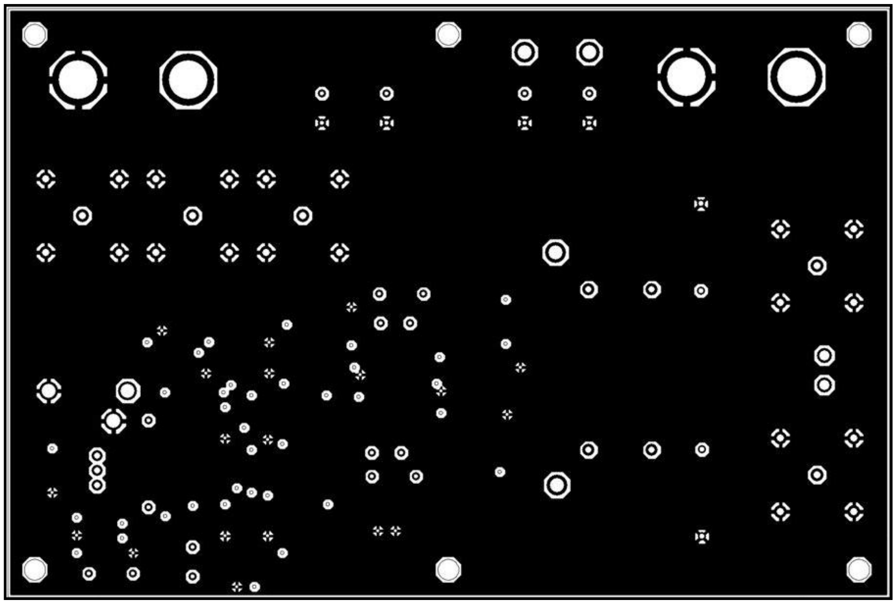


Figure 5.26 Three-level Ultiboard Layout (Ground Plane)

The bottom layer is shown in Figure 5.27.

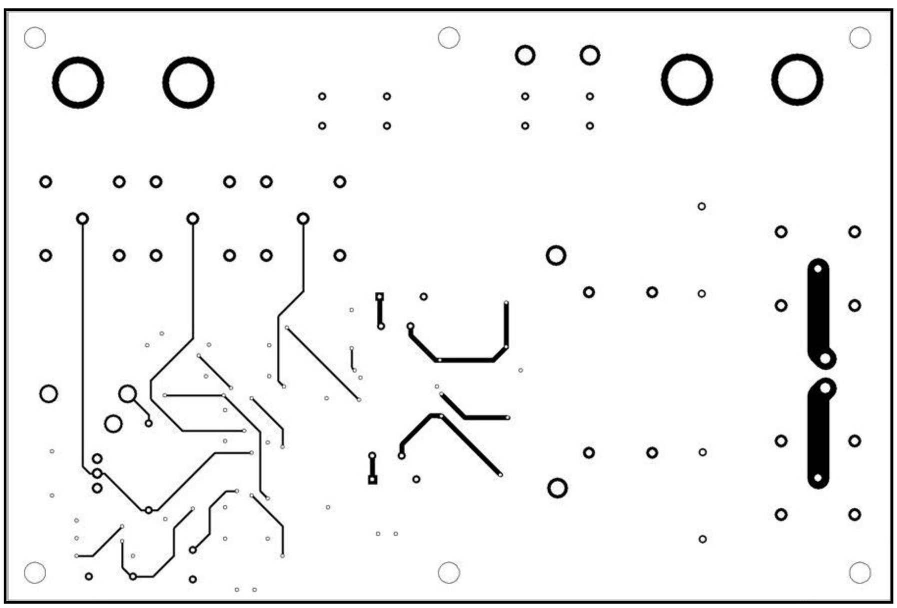


Figure 5.27 Three-level Ultiboard Layout (Bottom)

From this design, the Gerber files were exported and checked by Advanced Circuits. Amazingly, the error check returned with no errors the first time through. This was because all the errors that were uncovered in the two-level design were noted and immediately corrected for the three-level design. With the board error free, it was time to place the order. Five boards were ordered of this design.

Similar to our first production, the manufacturing took five business days and shipping took two. This confirmed that Advanced Circuits was reliable as they quoted a five day turnaround on all 4-layer productions. A picture of one of the blank PCB boards, as they were received, is shown in Figure 5.28 and Figure 5.29.

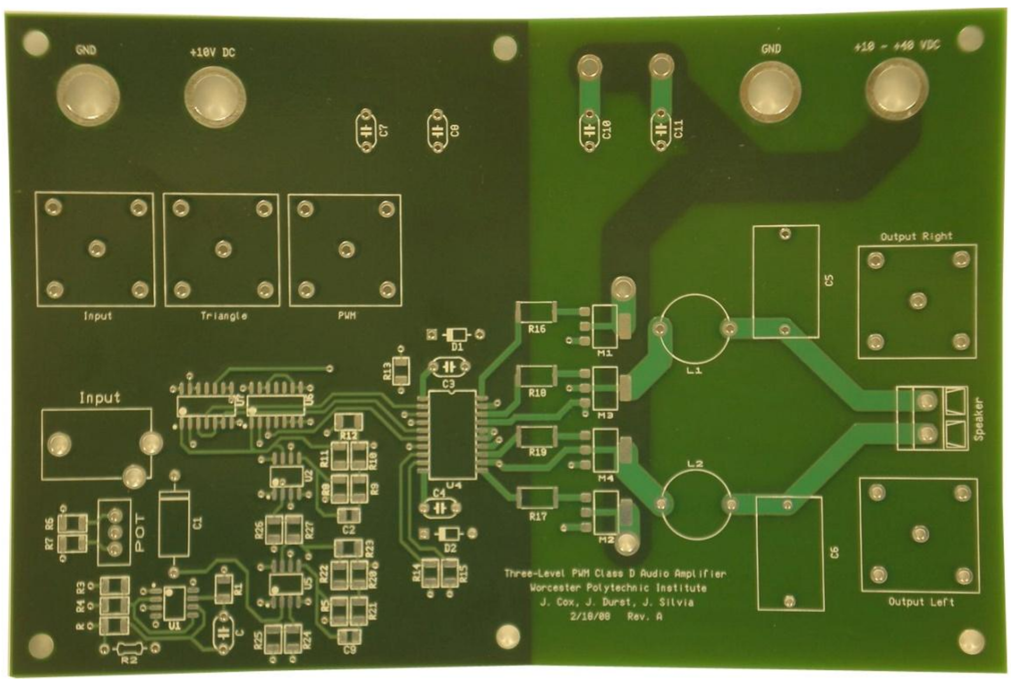


Figure 5.28 Three-level Blank PCB (Top)

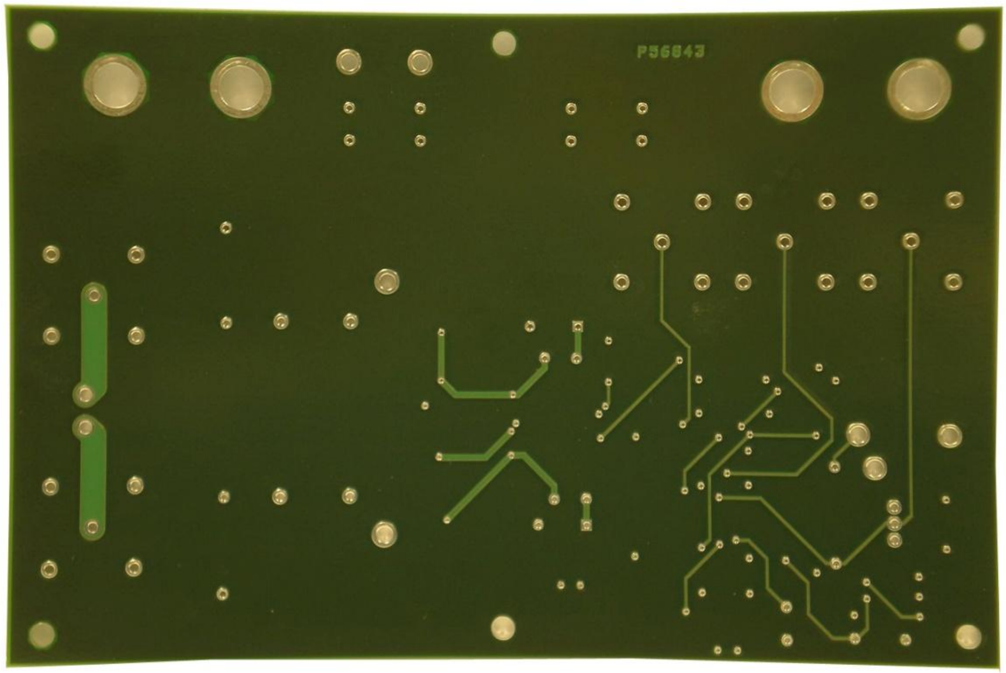


Figure 5.29 Three-level Blank PCB (Bottom)

Once the boards were received, we they were tested and assembled immediately. The first task was to test the connections of all the traces. After all the connections were verified, it was determined that the board was manufactured perfectly.

The supports were added and the components were soldered on. No mistakes were made in the soldering process, and with the addition of the banana jacks, the board was complete. The assembled board is presented in Figure 5.30.

Figure 5.30 Three-level PCB Assembled (Top)

The additional two potentiometers seen in the figure were added in place of resistors to help size and offset the signals properly.

The triangle wave was observed first and it was noted that it was not the desired frequency and amplitude. The triangle wave for the three-level design needed to be half the size of the one in the two-level design. This was achieved by changing the capacitor C to 100 pF and resistor R_2 to 300kΩ. The final triangle wave had a peak-to-peak amplitude of 0.65 V and a frequency of 303 kHz. The waveform is shown in Figure 5.31.

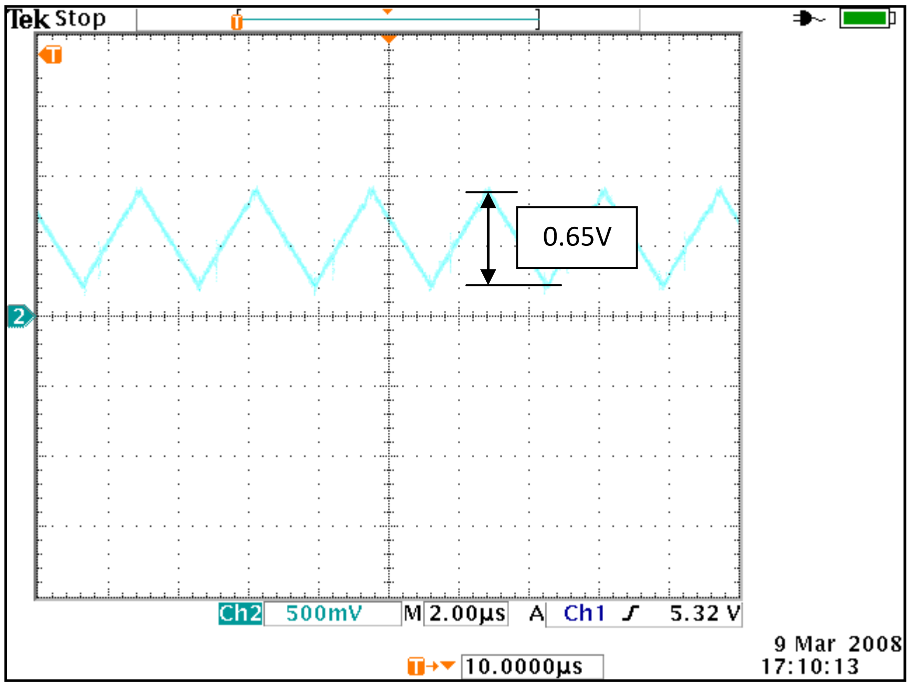


Figure 5.31 Three-level PCB Triangle Wave Waveform

The noise that was observed on the triangle wave in the previous design was significantly reduced. Switching noise did not occur on the control side of the board because of the dual supplies. Even though the noise was not present on this board, bypass capacitors were still added to the design, as seen in Figure 5.32. There installed on the bottom of the PCB board, similar to the two-level board.

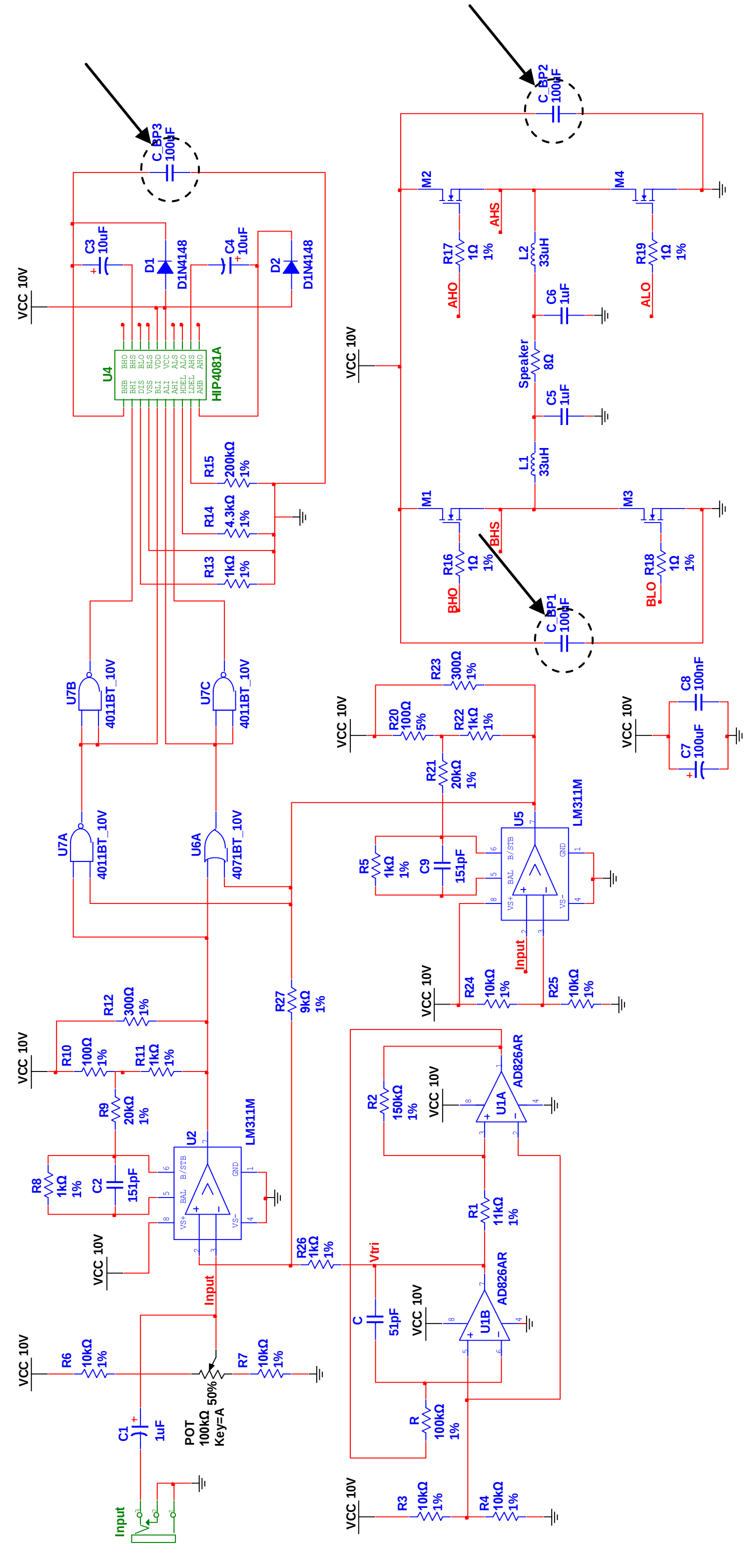


Figure 5.32 Three-level Schematic with Bypass Capacitors

As seen in Figure 5.33, the triangle wave shifted up and down to follow the input signal as desired.

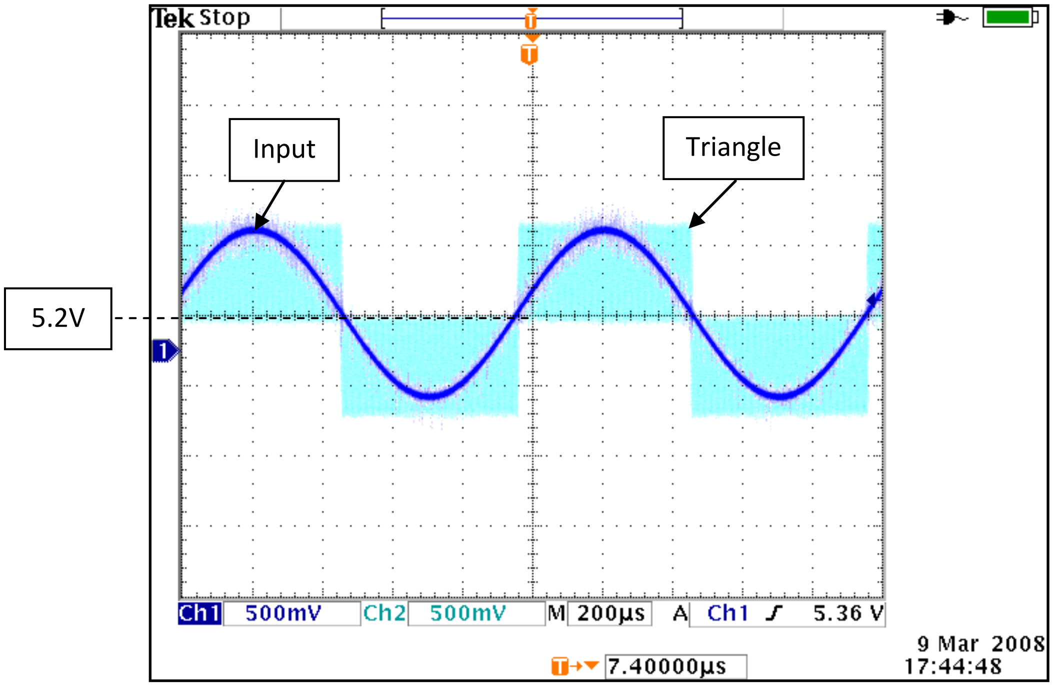


Figure 5.33 Three-level PCB Input and Shifting Triangle Wave Waveforms

As seen in Figure 5.34, the PWM output functioned properly, in the same manner as the two-level.

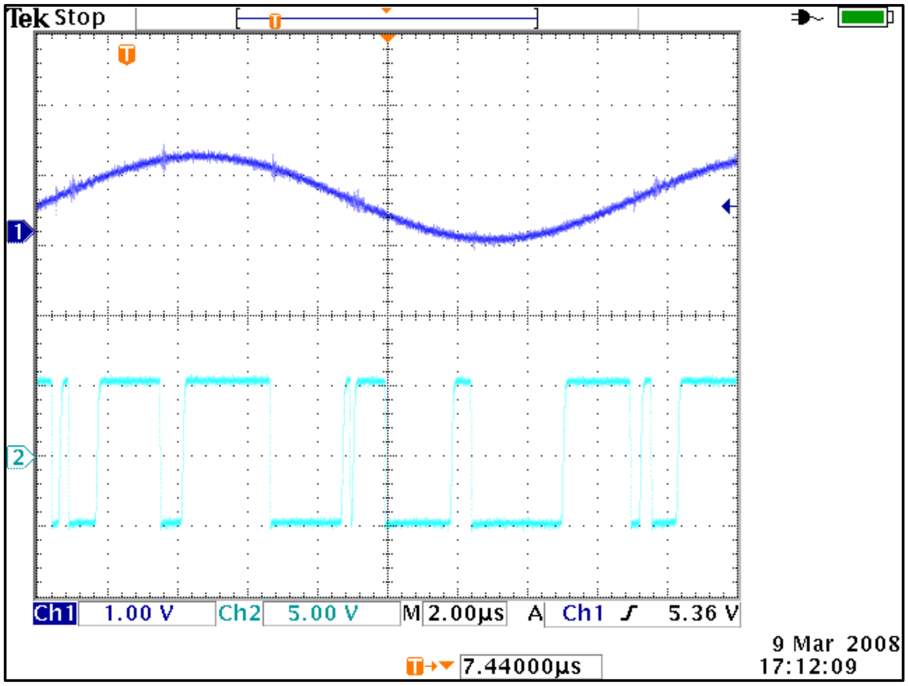


Figure 5.34 Three-level PCB Input and PWM Waveforms

After further testing, it was determined that the output was not a linear representation of the input. When inputting a sine wave, the output was not a larger sine wave. Each half of the output was flipped horizontally, producing a non-desirable waveform. This was caused by an inaccuracy in the original schematic. The two inputs to one of the LM311 comparators were mistakenly reversed on the schematic used to design the PCB. We corrected this error by lifting up the two pins of the chip and rewiring the two connections manually to bypass the PCB traces.

With the connections corrected, the outputs were observed on the oscilloscope, as seen in Figure 5.35.

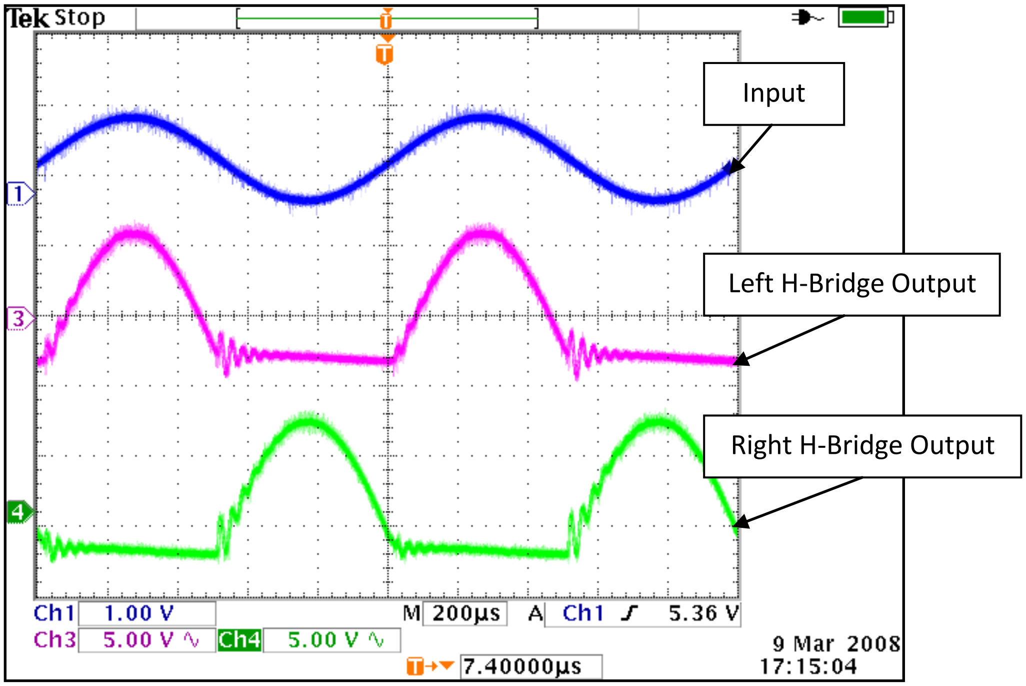


Figure 5.35 Three-level PCB Input and Output Waveforms

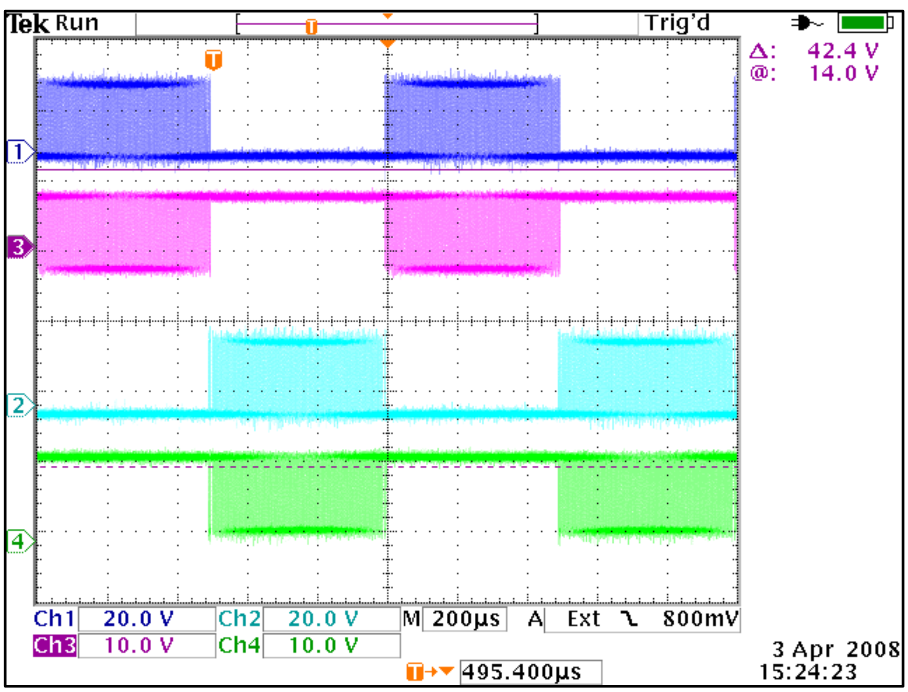


Figure 5.36: MOSFET Gate Driving Waveforms

Using the Math function of the oscilloscope, the differential output was plotted, as seen in Figure 5.37.

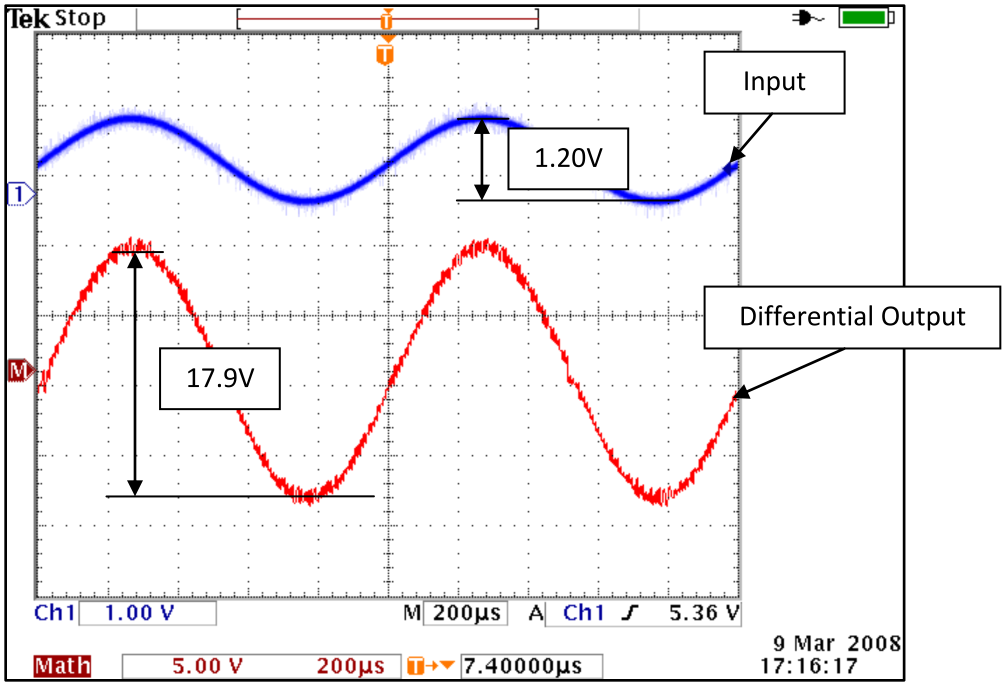


Figure 5.37 Three-level PWM Input and Differential Output Waveforms

It was observed that the output was a linear scaling of the input, thus confirming that our three-level design was indeed an amplifier.

6. Performance Testing and Characterization

After completing the prototypes, we tested our PCB assemblies of both the two level and the three level designs to characterize their performance. During this process, we occasionally located sources of inefficiency in our design and adjusted component values accordingly. The end result was a more efficient output and an overall higher quality signal. Our testing process involved mostly quantitative evaluations but in the end there was also a qualitative evaluation of the product. This qualitative evaluation stemmed from the fact that our design is a product that if manufactured would most likely end in consumer goods. During our testing we altered a single parameter at a time to give us the most accurate view of its effects.

6.1. System Gain

For these tests, we set our power supply voltage to 10.4 V and applied an input signal to our system. We than measured the magnitude of the output waveform. During these tests we also continuously monitored the magnitude of the input signal to verify that this did not change with frequency. The results were as we expected; when plotted against frequency, the gain in our system for both the two and three level boards took the form of an inverted parabola. The primary factors responsible for this shape were the high pass filter on the input stage and the low pass output filter across the connected load.

In order to determine the source of these attenuations, we first attempted to characterize the cutoff frequency for the input stage. Figure 6.1 displays the setup of the AC-coupled audio input on the PCB. The input jack is connected through a 1 uF capacitor to the voltage divider formed by R6 and R7. The resulting waveform, if measured between the resistors, shows the original input waveform riding on a DC offset whose value is determined by the voltage divider. The potentiometer was added to the PCB later for troubleshooting purposes so that we could adjust the input offset for the best possible performance.

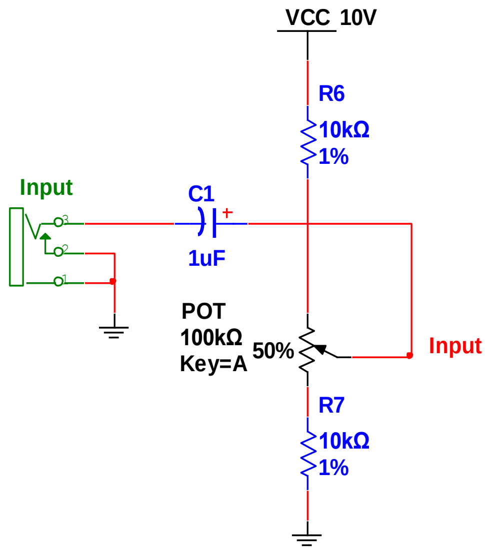


Figure 6.1 AC Coupling At Input

Assuming the resistance of the potentiometer is small, the cutoff frequency of the high-pass RC filter formed by C1 and R7 is given by:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi(10\text{E}3)(1\text{E}-6)} = 15.92\text{ Hz}$$

Thus, we would expect to see significant attenuation of the output amplitude for lower frequencies. This phenomenon is clearly visible in the frequency response of the two-level system as shown in Figure 6.2.

6.1.1. Two-Level Board

The gain data for the two-level board is presented in Table 6.1. The supply voltage was set at 10.4V and the input amplitude was set to 1.00 V_{pp}.

Frequency [Hz]	Output Amplitude [V_{pp}]	Calculated Gain [V/V]	Frequency [Hz]	Output Amplitude [V_{pp}]	Calculated Gain [V/V]
1	4.52	4.52	4k	14.50	14.50
10	4.72	4.72	5k	14.00	14.00
20	8.16	8.16	6k	13.75	15.40
30	10.70	10.70	7k	12.90	12.90
40	11.90	11.90	8k	12.90	12.90
50	12.90	12.90	9k	12.10	12.10
60	13.45	13.45	10k	11.70	11.70
70	13.70	13.70	11k	11.40	11.40
80	14.00	14.00	12k	11.10	11.10
90	14.20	14.20	13k	10.80	10.80
100	14.60	14.60	14k	10.40	10.40
200	15.00	15.00	15k	9.62	9.62
300	15.20	15.20	16k	9.64	9.64
400	15.30	15.30	17k	9.32	9.32
500	15.40	15.40	18k	8.95	8.95
600	15.20	15.20	19k	8.95	8.95
700	15.20	15.20	20k	8.52	8.52
800	15.20	15.20	22k	8.08	8.08
900	15.20	15.20	24k	7.50	7.50
1k	15.20	15.20	26k	7.08	7.08
2k	15.20	15.20	28k	6.56	6.56
3k	14.80	14.80	30k	6.12	6.12

Table 6.1 Two-level Output Amplitude And Gain vs. Frequency Data

From this table we can extrapolate several bits of information. Firstly, the gain of our system is not completely flat within the full range of human hearing. However, if you reduce this further to more common hearing ranges the response of our system becomes more even. Next, the frequencies slightly out of the audio range (beyond 20 kHz) are still transmitted. This is due to the fact that there is not a hard cut off at the output filter. Ideally, there would be no signal beyond 20 kHz passed through the system and therefore no energy filtered from the output. This is not a significant audio quality issue, however, because frequencies beyond 20 kHz are outside of the typical human hearing range. Another important fact is the location of the peak gain. A maximum peak gain of 15.4 (23.8 dB) was measured at 500 Hz and 6 kHz.

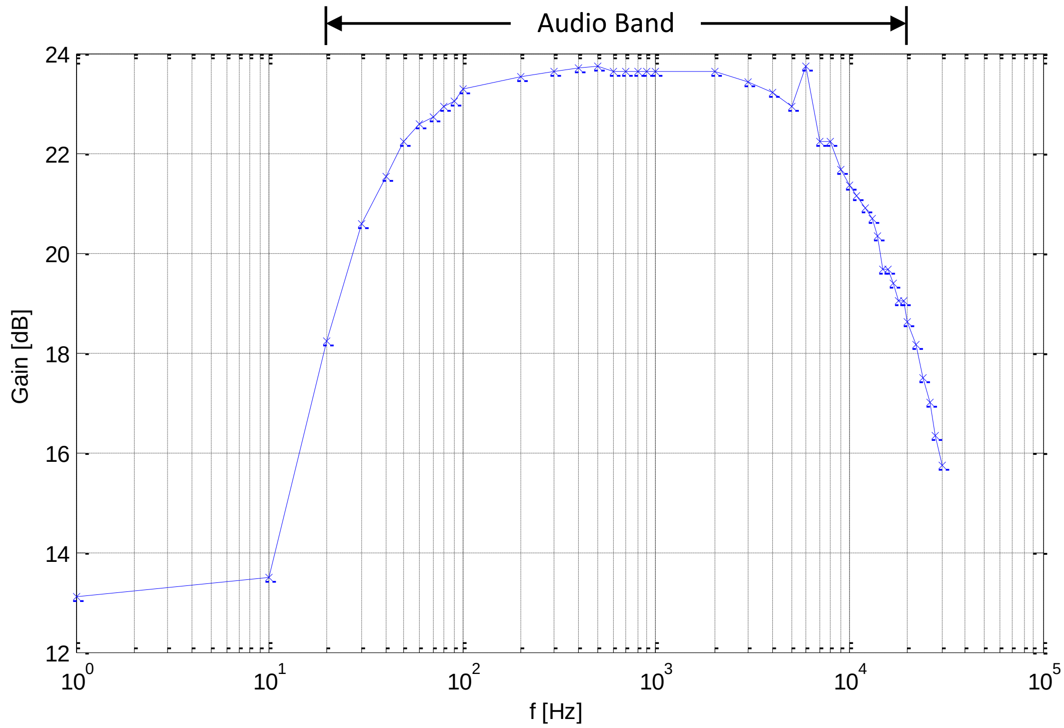


Figure 6.2 Voltage Gain Frequency Response of Two-level PCB

Figure 6.2 shows the parabolic nature of our gain. After approximately 20 kHz ($2*10^4$), the gain of our system begins to drop off linearly on a logarithmic scale. We believe this is due to the low pass filter on the output. It is projected that higher frequencies would continue to drop off even further due to the filter. Table 6.2 summarizes the gain data for the two-level amplifier board.

	1 Hz to 30 kHz	20 Hz to 20 kHz
Average Gain [V/V]	11.757	12.776
Peak Gain [V/V]	15.400	15.400

Table 6.2 Summary of Gain Data for Two-level Board

6.1.2. Three-Level Board

The gain data for the three-level board is presented in Table 6.2. The supply voltage was set at 10.4V and the input amplitude was set to 1.08 V_{pp}.

Frequency [Hz]	Output Amplitude [V_{pp}]	Calculated Gain [V/V]	Frequency [Hz]	Output Amplitude [V_{pp}]	Calculated Gain [V/V]
1	1.54	1.426	4k	16.2	15.000
10	14.5	13.426	5k	16.1	14.907
20	15.3	14.167	6k	16.1	15.000
30	15.5	14.352	7k	16.1	14.907
40	15.9	14.722	8k	16.1	14.907
50	15.9	14.722	9k	16.0	14.815
60	16.1	14.907	10k	15.8	14.630
70	16.2	15.000	11k	15.6	14.444
80	16.2	15.000	12k	15.4	14.259
90	16.2	15.000	13k	15.1	13.981
100	16.2	15.000	14k	14.8	13.704
200	16.2	15.000	15k	14.2	13.148
300	16.2	15.000	16k	13.9	12.870
400	16.2	15.000	17k	13.9	12.870
500	16.2	15.000	18k	13.5	12.500
600	16.2	15.000	19k	13.1	12.130
700	16.2	15.000	20k	13.0	12.037
800	16.2	15.000	22k	12.5	11.574
900	16.2	15.000	24k	12.0	11.111
1k	16.2	15.000	26k	11.5	10.648
2k	16.2	15.000	28k	11.0	10.185
3k	16.2	15.000	30k	10.3	9.537

Table 6.2 Output Amplitude And Gain vs. Frequency for Three-level PCB

The frequency response of the amplifier was greatly improved in the transition from two-level PWM to three-level PWM. The gain in the three-level design varies less in the human hearing range than the two-level PCB did. The three-level design once again has the same characteristic parabolic shape as the two-level. The maximum of gain of 15.00 (23.52 dB) this time occurs for a large range of frequencies starting at 70 Hz and ending at 6 kHz. However, this maximum gain is slightly lower than the maximum gain on our two-level design. Figure 6.3 displays the frequency response of the three-level PCB.

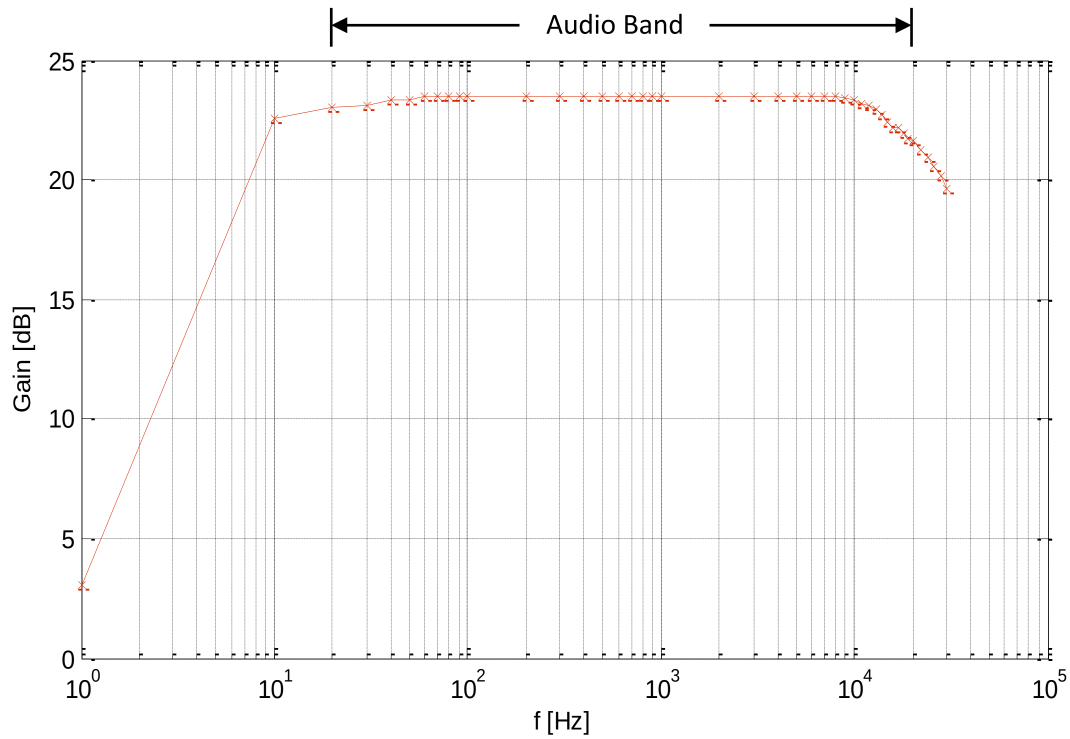


Figure 6.3 Voltage Gain Frequency Response of Three-level PCB

Aside from the predicted effect of the low pass filter on our output and the high pass filter on the input, there is very little noticeable variation in the gain. At the upper end of our test range the amplitude does begin to drop as expected. This slow drop-off is due to our increase of the filter cutoff to 30 kHz to further increase the flatness of the gain curve in our operating domain. Table 6.3 summarizes the gain data collected for the three-level PCB.

	Up to 30 kHz	Up to 20 kHz
Average Gain [V/V]	13.679	14.432
Peak Gain [V/V]	15.000	15.000

Table 6.3 Summary of Gain Data for Three-level

Figure 6.4 shows a comparison between the gains of the two-level and three-level boards. It can be seen that for the middle of the audio band, the two boards have approximately the same gain. The three-level outperforms the two-level for the bottom and top of the audio band.

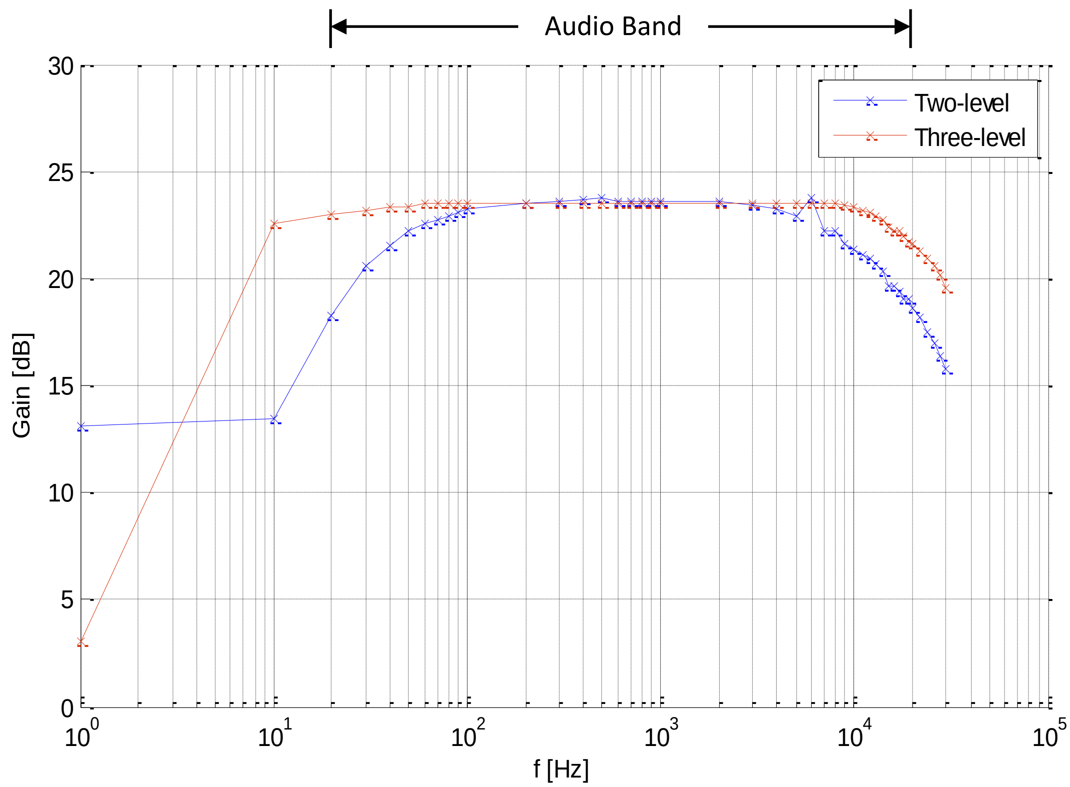


Figure 6.4 Voltage Gain Frequency Response Comparison

6.2. Output Power

6.2.1. Calculations and Measurement Methodology

As part of our performance testing, we wanted to see how much power our amplifier could actually produce. The output power is closely tied to the system gain; the voltage produced across the speaker will determine the power output of the system. Two specific equations were used to calculate our power values; the power output is estimated by:

$$P_{avg} = \frac{(V_{rms})^2}{R}$$

Where V_{rms} is the RMS voltage produced across the load. For the input power, we used the values displayed on our power supply for supplied voltage and current:

$$P = VI$$

Using these two equations, we can calculate the input and output power of the system and determine the real-world efficiency. This is done is Section 6.3.

One of the implied goals of audio amplifier design is the expectation that the designed system will accurately reproduce an input audio signal. This requirement demands an amplifier that is capable of amplifying the entire audio spectrum without attenuation or distortion of certain frequencies relative to others. We performed a frequency sweep of our system to determine if our system met this criterion. With the input amplitude held constant, we recorded the amplitude of the observed output waveform at each frequency stop over a wide range of frequency values.

Based on our supply voltage of 10.4 V, we expected to see a theoretical maximum amplitude of 20.8 V peak-to-peak across the load, assuming an ideal filter response and neglecting the on-resistance of the MOSFETs. With our standard input amplitude of 1 V peak-to-peak, this corresponds to a maximum gain of 20.8, or 26.36 dB. Using the 20.8 V maximum output level, we can modify the average power equation to calculate the theoretical maximum instantaneous power output:

$$P_{max} = \frac{\left(V_{peak}\right)^2}{R} = \frac{(10.4)^2}{8} = \frac{108.16}{8} = 13.52 \text{ W}$$

This is not a very conservative value, since it assumes that the MOSFETs have zero resistance, that the switching delay is instantaneous, and that no power is lost due to the removal of noise through the low-pass filter. It also assumes a perfectly resistive load, which is accurate in our case, since we used a "dummy" 8 Ω resistive test load rather than an actual speaker. Figure 6.5 displays our test load, a resistor rated for 50 W maximum power dissipation.

Figure 6.5 Test Load Resistor

We measured the voltage across the load using a TDS3014B oscilloscope. The power supply used for all testing was a Hewlett Packard E3632A DC power supply. The input signal for the frequency sweeps was taken from a Hewlett Packard 33120A function generator connected to the boards through their 1/8'' audio jacks.

6.2.2. Two Level Power Testing

Our first power test was a frequency sweep of the two-level system to determine how constant the power output was over a wide range of frequencies. With a 1 V peak-to-peak input, we recorded the output amplitude for a wide range of frequencies in the audio band (1 Hz-20 kHz) and beyond (20 kHz to 30 kHz). We expected to see the gain of the system decrease sharply near 30 kHz, since this was the cutoff value of our filter. Near 1 kHz, the system approaches the ideal gain of 26.36 dB calculated earlier. The system also produces its maximum power output in this range.

Table 6.4 summarizes the performance characteristics of the two-level board for the 1 Hz-20 kHz frequency sweep.

Average RMS Power	2.616 W
Peak Power	7.411 W
Avg. RMS Power Gain	22.128 dB
Peak Power Gain	23.750 dB

Table 6.4 Two-level PWM Power Data

6.2.3. Three Level Power Testing

We also measured the power output and frequency response of the three-level board. Due to the part changes made between the three-level and two-level designs, we expected to achieve higher performance levels with this board. Specifically, the high-current output filter inductors and more robust MOSFETs should allow the power stage of the board to operate at higher voltage levels, thereby raising the overall output power of the system. While the two-level PCB was a single-supply power plane, the three-level board was split into two power planes and a common ground. With PCB traces allowing for approximately 5 A of current, we are able to raise the operating voltage up to 40 V, which gives us a theoretical peak power output of:

$$P_{max} = \frac{(V_{peak})^2}{R} = \frac{(40)^2}{8} = \frac{1600}{8} = 200\text{W}$$

Which is equivalent to an RMS output power value of 100W.

We performed the same frequency sweep as the two-level test for the three-level board. Note that the supply voltage is equal to that of the two-level board (10.4 V).

As expected, we observe some attenuation at lower frequencies under 100 Hz. Fortunately, the response of the three-level board is much flatter than the two-level board over the audio spectrum, and we do not observe attenuation at the high end until approximately 10 kHz.

Figure 6.8 shows a comparison of the two-level and three-level output power over the audio spectrum. The output power for the two-level board appears to peak just before 1 kHz; for the three-level board, peak power is near 100 Hz, but the spectrum is flatter overall, and the board lingers close to 4W constant RMS output for a wide range of frequencies.

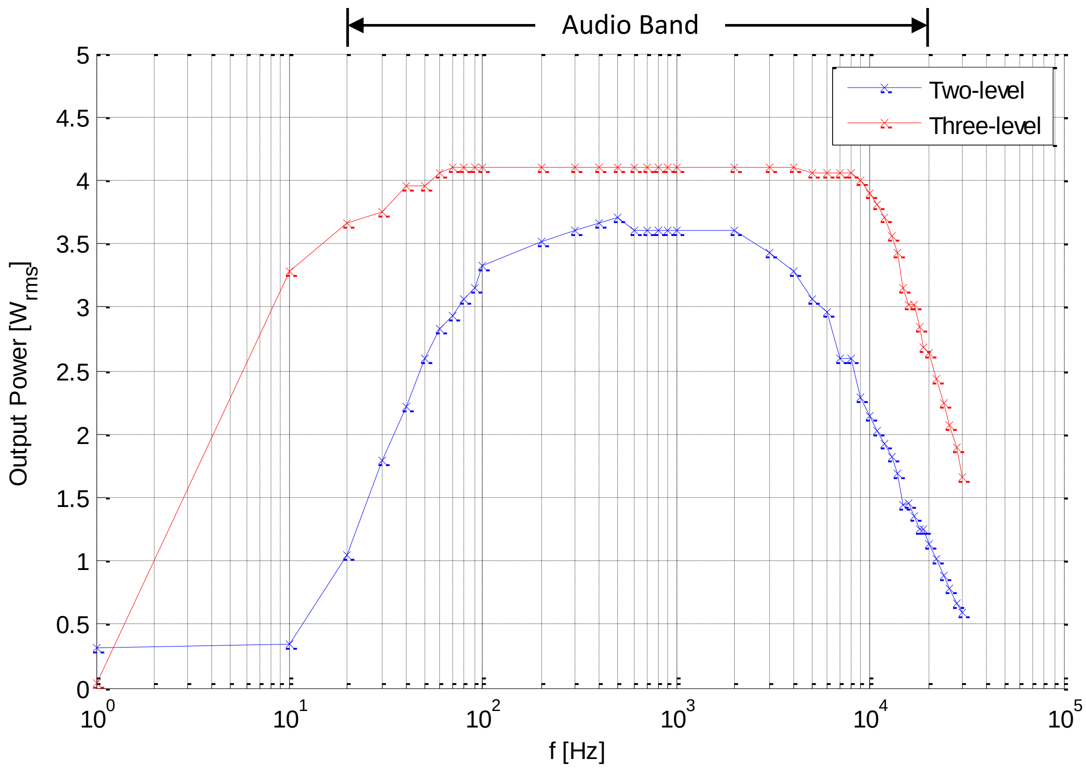


Figure 6.6 Power Output vs. Frequency Comparison

Table 6.5 summarizes the power measurements taken for the three-level PWM board. The overall gain of the system is greater than that of the two-level board, and we observe a much larger maximum peak power output of approximately 8 W as a result.

Average RMS Power	3.81 W
Peak Power	8.20 W
Avg. RMS Power Gain	23.19 dB
Peak Power Gain	23.52 dB

Table 6.5 PWM Power Data

Due to the dual power supply design of the three-level PCB, we are able to boost the output power of the device by raising the power stage supply voltage independently of the modulator supply voltage. We decided to perform testing on our board at higher voltage levels in order to characterize the performance of the device under more stressful operating conditions. Table 6.6 and Figure 6.7 show the collected data for the higher-power testing. All data points were taken with a 1V peak-to-peak input at 1 kHz.

Supply Voltage [V]	Output Amplitude [Vpp]	RMS Output Power [W]	Peak Output Power [W]
5	7.2	0.81	1.62
10	14.2	3.15	6.30
15	21.8	7.43	14.86
20	28.6	12.78	25.56
25	35.4	19.58	39.16
30	42.8	28.63	57.26

Table 6.6 High Voltage Power Outputs

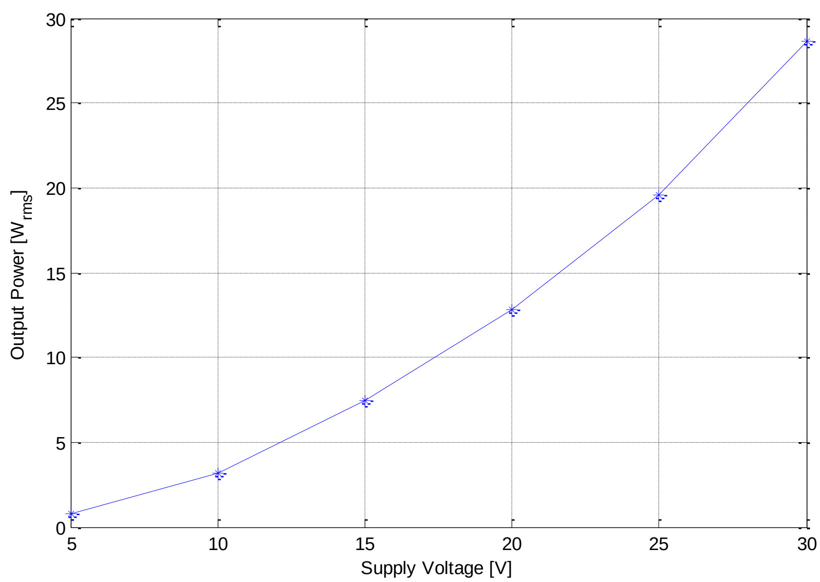


Figure 6.7 Plot of High Power Voltage Sweep

We observe that, at supply voltages near 30 V, our amplifier is capable of delivering more than 50 W into an 8 Ω load. We were very pleased with this result, and we feel that this value could be further increased by utilizing higher supply voltages. Unfortunately, the power supply used for our testing was unable to deliver more than 30 V to the PCB, and the supply was nearing its maximum allowable current output as well. We were also concerned about potentially destroying our PCB or MOSFETs at higher voltage levels, especially since we had no spare MOSFETs available if one was destroyed.

6.3. Efficiency

One of the goals of this project was to design a Class-D amplifier with an overall efficiency of greater than 90%. Based on our measurements of the input and output power for each of our boards, we were able to calculate the efficiency of our amplifier over the desired frequency range.

In order to maximize our efficiency, we needed to understand the major sources of power loss in our amplifier. On the power stage, we knew that the on-resistance of the MOSFETs would cause a small drop in the voltage supplied to the speaker, resulting in power loss. Therefore, we were careful to choose FETs with a small on-resistance whenever possible. The International Rectifier IRDF014 MOSFETs used in the two-level design have an on-resistance of 0.2 Ω; for a 10.4 V power supply, this resistance yields a loss of 0.65 W from the theoretical peak power value. In the three-level design, the Zetex ZXMN4A06 MOSFETs have a smaller on-resistance of 0.05 Ω. The bursts of current used to charge and discharge the gate capacitance of the MOSFETs also results in significant loss for our system. We also knew that noise in the input signal, once amplified by the PWM system, would be filtered out of the output signal by the low-pass filter; the removal of this high-frequency noise represents the removal of energy from the system.

Once we calculated values for the input and output power, determining the efficiencies was a trivial task. The efficiency of the amplifier is given by the ratio of produced output power to consumed power:

$$Efficiency = \frac{P_{out}}{P_{in}} * 100\%$$

From this equation, we produced efficiency values for both of our amplifier designs. We plotted these values versus input frequency as shown in Figure 6.8.

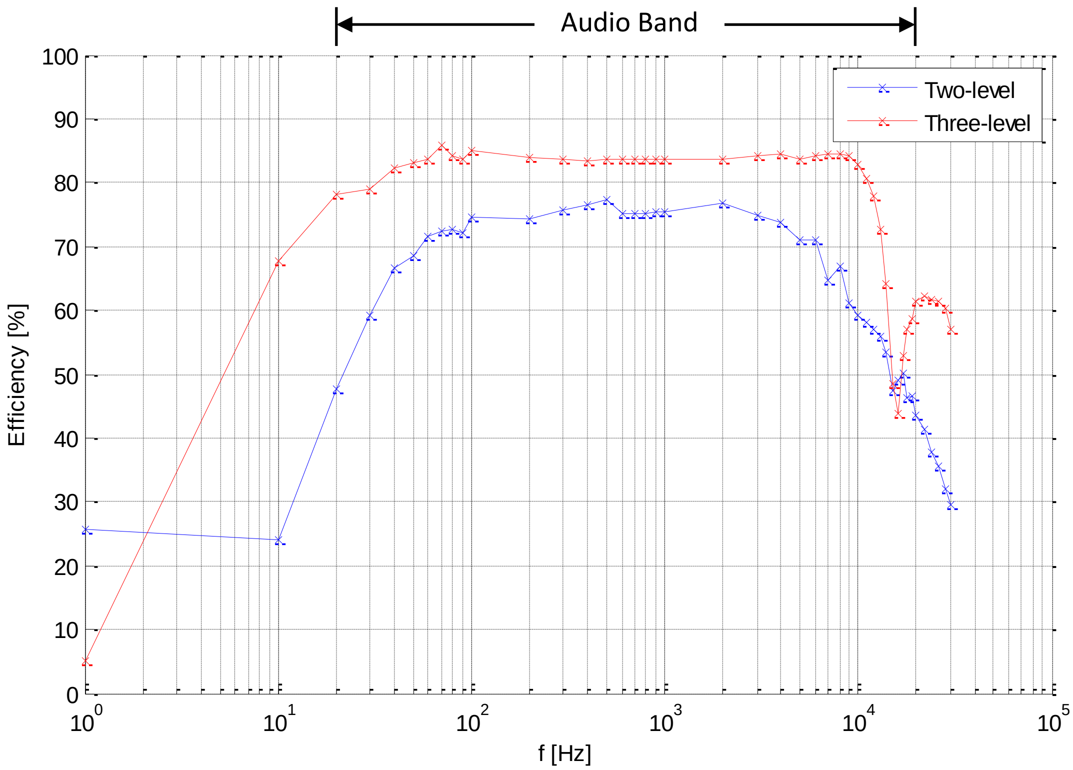


Figure 6.8 Efficiency Comparison for Two and Three-level PWM

The three-level board has better efficiency overall, typically near 85% within the audio band. The two-level board is also competitive at midrange frequencies. Table 6.7 displays a summary of the collected efficiency data for the two- and three-level amplifiers. The average efficiencies are calculated by mathematically averaging the set of data points plotted in Figure 6.8.

Two Level Board	
Efficiency, Average	65.179%
Efficiency, Peak	77.459%
Three Level Board	
Efficiency, Average	76.372%
Efficiency, Peak	85.715%

Table 6.7 Efficiency Comparison Data

We also wanted to know if our three-level amplifier remained efficient at higher output power levels. Based on the data we had previously collected, we calculated the input and output power values for each supply voltage up to 30 V. Figure 6.9 displays the efficiency data calculated for higher supply voltage values.

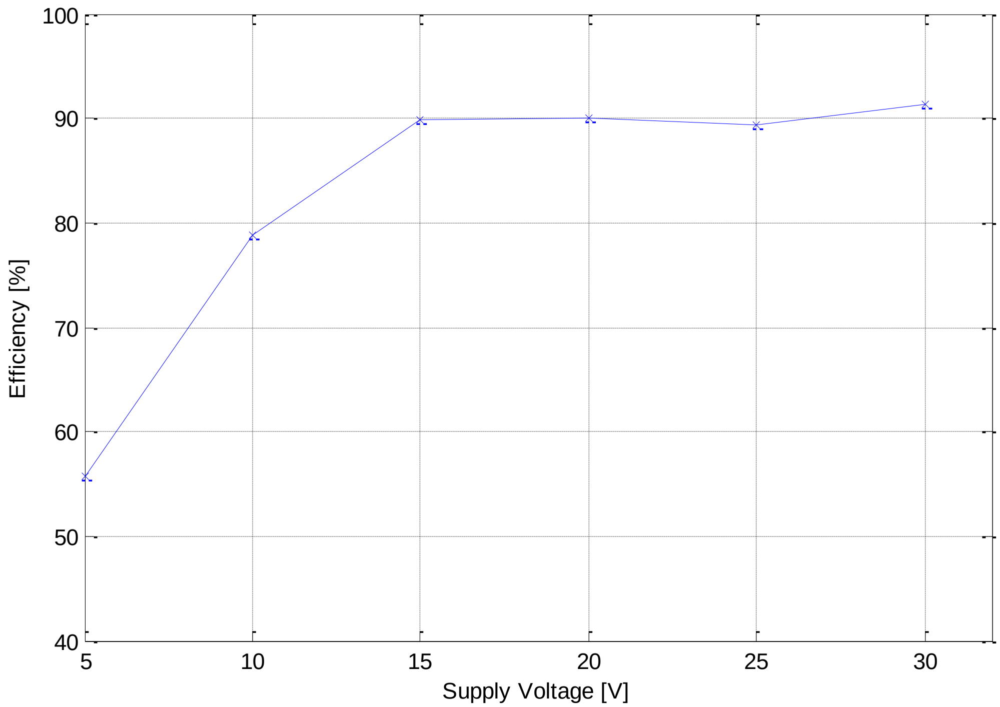


Figure 6.9 Efficiency versus Supply Voltage for 3-Level Amplifier

We observe that the amplifier performs well under high-load conditions and reaches 90% efficiency for supply voltages above 15 V.

6.4. Total Harmonic Distortion

Total harmonic distortion, or THD, is the ratio of RMS voltage of the harmonics to that of the fundamental component [72]. Using the FFT function of the oscilloscope, the voltage levels of the first ten harmonics were measured. The THD was calculated using the following equation:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \cdots + V_{10}^2}}{V_1}$$

6.4.1. Two-Level Board

The THD of the two-level PCB was measured for frequencies in the range of 20 Hz to 20 kHz. Table 6.8 presents a summary of the data. A complete table of the measured data points is presented in Appendix E.

Frequency [Hz]	THD [%]	Frequency [Hz]	THD [%]
20	1.126	3000	1.618
30	1.135	4000	2.013
40	1.384	5000	2.612
50	0.994	6000	3.020
60	1.125	7000	3.038
70	1.732	8000	2.888
80	2.202	9000	3.038
90	2.366	10000	3.365
100	2.424	11000	3.364
200	2.378	12000	2.555
300	2.279	13000	2.852
400	2.312	14000	2.757
500	2.161	15000	2.528
600	2.110	16000	2.303
700	1.967	17000	2.209
800	1.966	18000	2.192
900	1.846	19000	2.001
1000	1.866	20000	1.810
2000	1.382		
		Average THD [%]	2.187
		Min THD [%]	0.994
		Max THD [%]	3.365

Table 6.8 Two-level THD Data

[72] (Audio Specifications, 2000)

The minimum THD for the two-level design was determined to be 0.994%. A plot of the data is presented in Figure 6.10. The THD of the two-level PCB was not below our goal of 1% THD for the frequency range 20 Hz to 20 kHz.

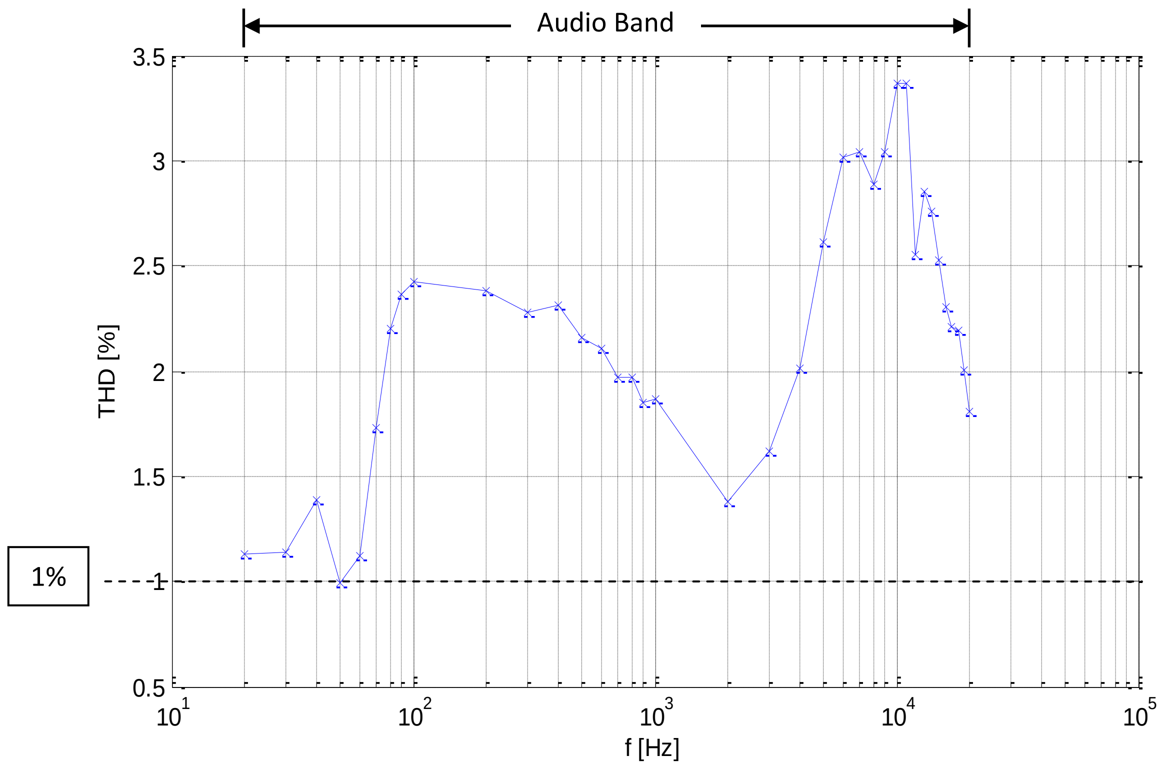


Figure 6.10 Two-level THD vs. Frequency Plot

6.4.2. Three-Level Board

The THD of the three-level PCB was measured for frequencies in the range of 20 Hz to 20 kHz. Table 6.9 presents a summary of the data. A complete table of the measured data points is presented in Appendix E.

Frequency [Hz]	THD [%]	Frequency [Hz]	THD [%]
20	1.044	3000	0.792
30	1.054	4000	1.134
40	0.692	5000	0.884
50	1.161	6000	1.040
60	1.114	7000	1.301
70	1.054	8000	1.797
80	0.963	9000	1.329
90	1.185	10000	1.997
100	1.183	11000	1.204
200	0.299	12000	1.874
300	0.871	13000	1.051
400	0.781	14000	1.958
500	0.834	15000	1.889
600	0.878	16000	3.869
700	0.717	17000	2.569
800	0.806	18000	2.385
900	1.102	19000	1.762
1000	1.275	20000	2.046
2000	0.649		
		Average THD [%]	1.312
		Min THD [%]	0.299
		Max THD [%]	3.869

Table 6.9 Three-level THD Data

The minimum THD for the three-level design was determined to be 0.299%. A plot of the data is presented in Figure 6.11.

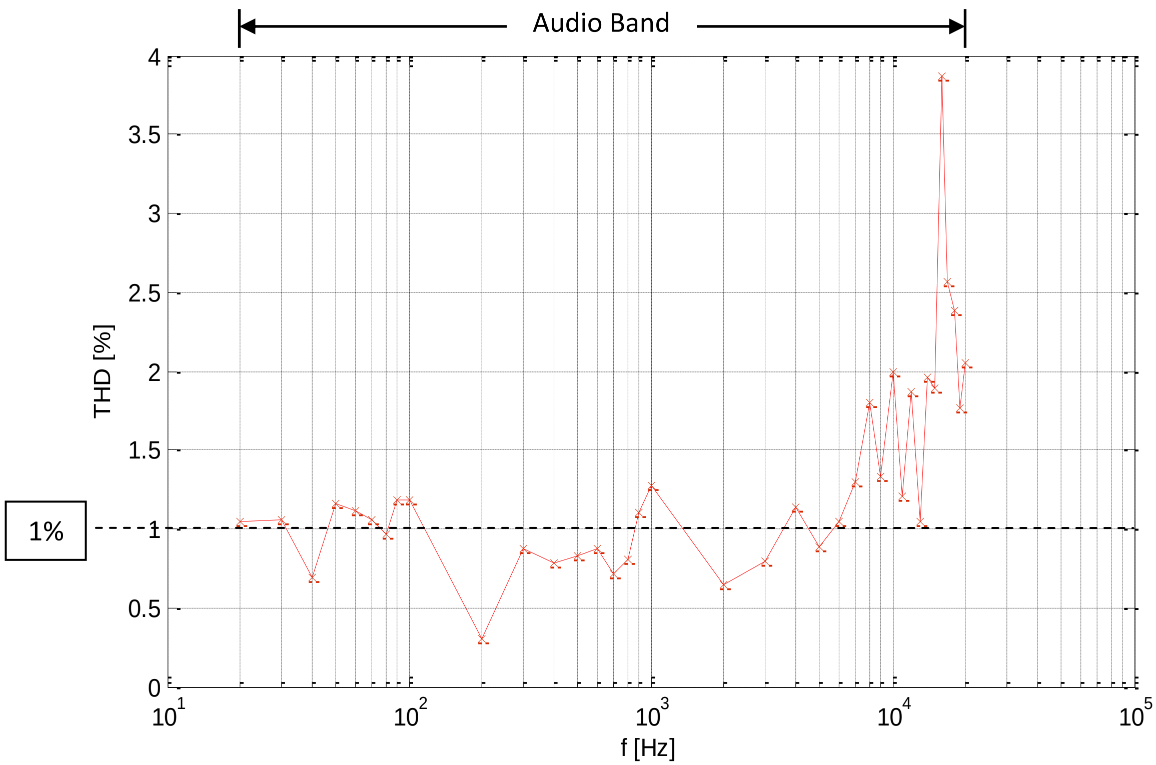


Figure 6.11 Three-level THD vs. Frequency Plot

Figure 6.12 shows the comparison between the THD of two-level and three-level boards. Besides the spike at 16 kHz, the three-level outperforms the two-level at almost all frequencies.

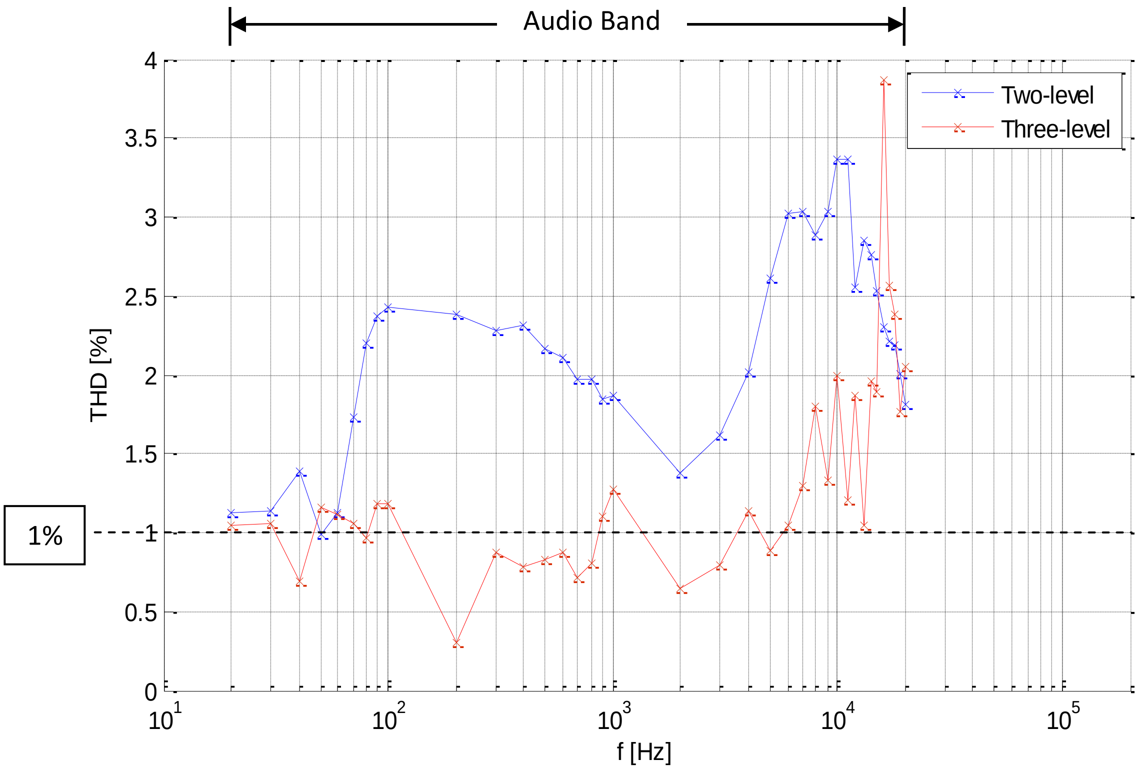


Figure 6.12 THD vs. Frequency Comparison Plot

6.5. Summary of Testing Results

Table 6.10 presents the summary of testing results.

Two Level		
	Value	**Frequency [Hz]**
Lowest THD	0.994%	50
Highest Gain	15.4	500
Highest Output power	3.7 W	500
Highest Efficiency	77.46%	500
Three Level		
	Value	**Frequency [Hz]**
Lowest THD	0.299%	200
Highest Gain	14.75	80, 90, 200-400, 2k
Highest Output power	4.895 W	80, 90, 200-400, 2k
Highest Efficiency	85.715%	700

Table 6.10 Summary of Testing Results

The victor in the final performance specifications alternated between the two and three level design. However, despite the three-level board's higher maximum output power and maximum efficiency, the best of our designs was the two-level. This is because fundamentally the three-level design failed to output an appropriate audio signal for high-fidelity applications. The distortion present in the three-level audio output was not evident when looking at a pure sinusoidal waveform. We believe the source of the distortion to be the shifting of the triangle wave; when we forced the three-level system to behave as a two level system by removing the shifting operation, the audible distortion was eliminated.

6.5.1. Two-Level Board

The two-level PCB did not meet the requirement of 90% or greater efficiency; neither did it meet our requirement of less than 1% THD. Our two-level design worked well fundamentally, but lacked some of the desired performance characteristics exhibited by the three-level amplifier. During the process of testing we isolated several causes of power loss in our system. There was no single source of power loss that prevented us from reaching the 90% goal. We feel that it is possible that another PCB revision would allow us to reduce the sources of loss and reach our goal of 90% efficiency. One potential source of power loss for the two-level system is the slight DC offset we observed superimposed on the output signal. A feedback system, when properly implemented, could improve the stability of the output significantly and also potentially boost the power output of the amplifier.

6.5.2. Three-Level Board

The three-level PCB also did not meet the requirement of 90% efficiency at 10.4 V. However, with supply voltages over 20V, the board hovers slightly over the 90% mark, with a maximum measured value of 91.4% efficiency during 30 V operation. The three-level board improved on the efficiency of the two-level board by several percentage points at all frequencies regardless of supply voltage. The three-level design did meet our THD requirement for a range of frequencies. However, the audible noise caused by crossover distortion in the system is too large to make the amplifier feasible for personal use, and is a topic for future review. Many of the same sources of loss in the two-level board still existed on the three level. Again, we believe that another PCB revision could result in a higher-performance product overall.

6.6. Qualitative Testing

An important part in the testing of any audio amplifier is the subjective listening tests performed by the human ear. One of our important criteria for our final amplifiers was their ability to produce a clean, accurate representation of an audio input signal. For each of the PCBs constructed, we used various audio sources (such as iPods and computers) to test the quality of the audio output. We hooked up one of the speakers located in the NECAMSID lab to the speaker connector on our board. Although the speaker happened to have a 6 Ω impedance, we placed a 2 Ω resistance in series to ensure proper performance.

With music as an input signal, we were able to adjust the potentiometers on the two- and three-level boards to minimize the amount of noise (hiss) audible from the speaker. For the two-level board, the results were nothing short of astounding; the amplifier was capable of reproducing the songs played from an iPod with good clarity, clear bass lines, and a powerful midrange. The attenuation observed in our quantitative testing at low frequencies did not appear to negatively affect the quality of the low-frequency portions of the audio signal.

The listening tests for the three-level board were not as exciting. While the shifted triangle wave can easily follow a sinusoidal input signal up to 20 kHz and beyond, we discovered that there was significant noise on the output. Adjustment of the triangle and input offset reference values helped eliminate some noise, but a hiss was still perceptible in the output signal. While we would have liked to raise the operating voltage of the three-level board to extract a more powerful audio signal, we felt that the risk of destroying a fully assembled PCB was not worth further amplification of the noise we were hearing.

From the listening tests we can conclude that the two-level board seems more promising; perhaps a future revision with an added feedback loop and high-voltage power stage design could replicate the clean audio signal we heard at much higher power levels. It is also worth noting that the three-level board sounded much better for large input amplitudes. Perhaps a pre-amplifier could be added to the input stage to boost the system's audio quality.

7. Recommendations

One of our main issues in this project was time. We originally set out to design a three-level system; however, by the end of B Term we still did not have a final proposed circuit to implement. Our solution to this was to develop a two level system and to develop a PCB of that system first. Although this endeavor was successful as a learning experience, it also cost us significant amounts of time. From that point on we were torn between further development of the two-level system and working on an experimental three-level modulator. This did not allow us to properly develop and debug either system. If we had concentrated all our time and effort onto one system or the other, it is entirely possible that we would have been able to reach all our desired specifications for that particular system. Our recommendation to solve this is to focus on one design. We knew our two-level design would work due to its simplicity, yet we also wanted to develop a fully functional three level analog PWM system as a proof of concept.

This rush also led to more problems. At times we were so caught up just trying to get both systems to work we overlooked trying to make each system perform better. For example, replacing the comparators with a model designed for audio applications could have boosted our performance. If we had spent time finding a viable alternative we could have very likely improved our efficiency by several percentage points. We recommend performing careful research during component selection, and thoroughly investigating any prior art.

A third issue which nearly destroyed our three-level design was the necessity of constantly updating our schematic. At one point during the prototyping process, we were testing a breadboarded circuit and we made a change. This change, however, never made it to the final schematic used to design the PCB. The PCB was then manufactured with this error included. This error could have potentially made the board useless. Fortunately, we were able to fix the error by performing surgery on the board. To solve this error we would recommend not only verifying the PCB design with the current schematic but also verifying the PCB design with any breadboarded prototype.

We would also like to recommend for future projects that software simulation tools be used sparingly. While simulations can be a wonderful tool for circuit design, in reality they often overlook inaccuracies and imperfections that have significant impact in the real world. A software simulator is only as good as the person using it; without proper knowledge of the simulation software's methods and assumptions, any software simulations performed will be inaccurate at best.

As a final recommendation, we would recommend careful calculation and analysis of component values in final circuit designs. Trial and error served us well with this project at times;

however, often it is worthwhile to spend time to characterize a sub-system and verify its correct performance rather than blindly adjusting resistor and capacitor values to achieve the desired performance. This is not necessarily difficult to correct if originally forgotten, but it is important to remember and can save time in the end.

8. Conclusions

We believe our project to be a success. Our group designed, constructed, and characterized two analog implementations of Class D audio amplifiers, and produced two professional-looking high-density printed circuit boards. The three-level PWM board achieved a power output of greater than 57W, more than twenty times our original goal. We also achieved a peak efficiency rating of greater than 90% with the three-level board. The three-level board also yielded a THD value less than 1% for an open-loop design, and three level design sounded good while playing music at high volume levels. With a feedback loop, we feel that both the two and three-level systems could be competitive products in the audio amplifier market.

One of the major questions we encountered in our project was "Is a two or three level system better?" Although we were unable to do a completely equalized head-to-head test between the two boards, we feel that a two level system is indeed better suited for audio purposes at this time. The ease of implementation for a two-level PWM modulator is a significant advantage, and we feel that multi-level Class D amplifiers are perhaps best suited to digital modulation schemes such as sigma-delta designs with much higher sampling rates.

The project required a very strong commitment from the three of us. We would like to thank Professor Bitar for helping us along the way and our NECAMSID sponsors for providing the laboratory equipment and parts we used through the course of our MQP.

A. References

[1] Moreno, S. S. (2005, June). *Class-D Amplifiers*. Retrieved September 27, 2007, from Elliott Sound Products - The Audio Pages: http://sound.westhost.com/articles/pwm.htm
[2] http://upload.wikimedia.org/wikipedia/en/4/4c/Pwm_amp.svg
[3] Gaalaas, E. (2007, June 1). *Sound advice on Class D audio amps designs*. Retrieved September 22, 2007, from Electronic Engineering Times Asia: http://www.eetasia.com/ART_8800466802_480600_NT_f7b4dc4d.HTM#
[4] *Electronic Amplifier*. (2007, September 20). Retrieved September 20, 2007, from Wikipedia, The Free Encyclopedia: http://en.wikipedia.org/w/index.php?title=Electronic_amplifier&oldid=160439334
[5] http://upload.wikimedia.org/wikipedia/en/9/9b/Electronic_Amplifier_Class_A.png
[6] http://upload.wikimedia.org/wikipedia/en/b/b6/Electronic_Amplifier_Class_B_fixed.png
[7] http://en.wikipedia.org/wiki/Image:Crossover_distortion.png
[8] http://www.uoguelph.ca/~antoon/tutorial/xtor/xtor1/1fig5.gif
[9] *Amplifier*. (2007, September 20). Retrieved September 20, 2007, from Wikipedia, The Free Encyclopedia: http://en.wikipedia.org/w/index.php?title=Amplifier&oldid=159520973
[10] Lynch, F. (2001). *win01_pg14-15.pdf.* Retrieved September 22, 2007, from Mircrosemi: http://www.microsemi.com/microcurrents/win01_pg14-15.pdf
[11] *Class D Audio Amplifier IC Market Report 2005-2006*. (2006, January). Retrieved September 22, 2007, from okokok: http://www.okokok.com.cn/Abroad/Class105/Class116/200604/101674.html
[12] *Maxim Engineering Journal Vol. #59*. (2007). Retrieved September 15, 2007, from Maxim: http://pdfserv.maxim-ic.com/en/ej/EJ59.pdf
[13] *Maxim Engineering Journal Vol. #59*. (2007). Retrieved September 15, 2007, from Maxim: http://pdfserv.maxim-ic.com/en/ej/EJ59.pdf
[14] *Maxim Engineering Journal Vol. #59*. (2007). Retrieved September 15, 2007, from Maxim: http://pdfserv.maxim-ic.com/en/ej/EJ59.pdf
[15] Gaalaas, E. (2007, January 23). *Class D Audio Amplifiers: What, Why, and How*. Retrieved September 2007, 2007, from Planet Analog: http://www.planetanalog.com/showArticle.jhtml?articleID=197000135&pgno=1
[16] Barkhordarian, V. (n.d.). *Power MOSFET Basics.* Retrieved September 9, 2007, from International Rectifier: http://www.irf.com/technical-info/appnotes/mosfet.pdf
[17] Gaalaas, E. (2007, January 23). *Class D Audio Amplifiers: What, Why, and How*. Retrieved September 2007, 2007, from Planet Analog: http://www.planetanalog.com/showArticle.jhtml?articleID=197000135&pgno=1
[18] Appendix C
[19] *Modulation*. (2007, September 15). Retrieved September 20, 2007, from Wikipedia, The Free Encyclopedia: http://en.wikipedia.org/w/index.php?title=Modulation&oldid=157981612
[20] *Pulse-width modulation*. (2007, September 13). Retrieved September 20, 2007, from Wikipedia, The Free Encyclopedia: http://en.wikipedia.org/w/index.php?title=Pulse-width_modulation&oldid=157595706
[21] http://upload.wikimedia.org/wikipedia/commons/a/af/Pwm.png
[22] *Pulse-density modulation*. (2007, August 28). Retrieved September 20, 2007, from Wikipedia, The Free Encyclopedia: http://en.wikipedia.org/w/index.php?title=Pulse-density_modulation&oldid=154231513
[23] http://upload.wikimedia.org/wikipedia/en/2/20/Pulse-density_modulation_1_period.gif
[24] *EMI Reduction and PCB Layout Techniques*. (2003, November 11). Retrieved September 12, 2007, from TLSI Inc.: http://www.tlsi.com/images/AN-101%20EMI.pdf
[25] *EMI Reduction and PCB Layout Techniques*. (2003, November 11). Retrieved September 12, 2007, from TLSI Inc.: http://www.tlsi.com/images/AN-101%20EMI.pdf
[26] McCulley, B. (2007, August 29). *National_ReducingEMIinClassDAudioApps.pdf*. Retrieved September 12, 2007, from National Semiconductor: http://www.national.com/onlineseminar/2007/emi/National_ReducingEMIinClassDAudioApps.pdf
[27] McCulley, B. (2007, August 29). *National_ReducingEMIinClassDAudioApps.pdf*. Retrieved September 12, 2007, from National Semiconductor: http://www.national.com/onlineseminar/2007/emi/National_ReducingEMIinClassDAudioApps.pdf
[28] McCulley, B. (2007, August 29). *National_ReducingEMIinClassDAudioApps.pdf*. Retrieved September 12, 2007, from National Semiconductor: http://www.national.com/onlineseminar/2007/emi/National_ReducingEMIinClassDAudioApps.pdf

[29] Katrai, C., & Arcus, C. (1998, December 29). *AN001.pdf*. Retrieved September 14, 2007, from Pericom Semiconductor Corporation: http://www.pericom.com/pdf/applications/AN011.pdf
[30] http://www.portabledesign.com/images/archive/images/0701pdreducing05.gif
[31] *FCC Part 15: Radio Frequency Devices*. (2007). Retrieved September 12, 2007, from Federal Communications Commission (FCC): http://www.fcc.gov/oet/info/rules/part15/part15-5-4-07.pdf
[32] *Class D Amplifiers are designed for car audio*. (2006, March 6). Retrieved September 6, 2007, from Find Articles: http://findarticles.com/p/articles/mi_m0PIL/is_2006_March_6/ai_n16090915
[33] *Maxim Engineering Journal Vol. #59*. (2007). Retrieved September 15, 2007, from Maxim: http://pdfserv.maxim-ic.com/en/ej/EJ59.pdf
[34] *Clock Generation with Spread Spectrum*. (2005, March 25). Retrieved September 15, 2007, from Maxim: http://www.maxim-ic.com/appnotes.cfm/appnote_number/3503
[35] McCulley, B. (2007, August 29). *National_ReducingEMIinClassDAudioApps.pdf*. Retrieved September 12, 2007, from National Semiconductor: http://www.national.com/onlineseminar/2007/emi/National_ReducingEMIinClassDAudioApps.pdf
[36] McCulley, B., & Higashi, R. (2007). *Reducing EMI in Class D audio applications by spread- spectrum modulation techniques*. Retrieved September 15, 2007, from Portable Design: http://www.portabledesign.com/archive_article/20457
[37] Rako, P. (2007, March 13). *Maxim Engineering Journal #59; Class-D audio*. Retrieved 9 2007, 2007, from EDN: Electronics Design, Strategy, News: http://www.edn.com/blog/1700000170/post/1380007538.html
[38] Stutz, B., & Schmidt, K. (2007, October 9). *Designing a multimedia interface with low EMI*. Retrieved September 9, 2007, from Planet Analog: http://www.planetanalog.com/showArticle.jhtml?articleID=191501749
[39] http://focus.ti.com/lit/an/sloa023/sloa023.pdf
[40] http://focus.ti.com/lit/an/sloa023/sloa023.pdf
[41] McCulley, B., & Higashi, R. (2007). *Reducing EMI in Class D audio applications by spread- spectrum modulation techniques*. Retrieved September 15, 2007, from Portable Design: http://www.portabledesign.com/archive_article/20457
[42] McCulley, B. (2007, August 29). *National_ReducingEMIinClassDAudioApps.pdf*. Retrieved September 12, 2007, from National Semiconductor: http://www.national.com/onlineseminar/2007/emi/National_ReducingEMIinClassDAudioApps.pdf
[43] *Maxim Engineering Journal Vol. #59*. (2007). Retrieved September 15, 2007, from Maxim: http://pdfserv.maxim-ic.com/en/ej/EJ59.pdf
[44] *Maxim's Active-Emissions-Limiting (AEL) Circuitry Demystified*. (2006, December 8). Retrieved September 15, 2007, from Maxim: http://www.maxim-ic.com/appnotes.cfm/an_pk/3973
[45] http://media.maxim-ic.com/images/appnotes/3973/3973Fig02.gif
[46] http://pdfserv.maxim-ic.com/en/ej/EJ59.pdf
[47] *Maxim Engineering Journal Vol. #59*. (2007). Retrieved September 15, 2007, from Maxim: http://pdfserv.maxim-ic.com/en/ej/EJ59.pdf
[48] Honda, J., & Adams, J. (2005, February 8). *Class D Audio Amplifier Basics*. Retrieved September 9, 2007, from International Rectifier: http://www.irf.com/technical-info/appnotes/an-1071.pdf
[49] *EMI Reduction and PCB Layout Techniques*. (2003, November 11). Retrieved September 12, 2007, from TLSI Inc.: http://www.tlsi.com/images/AN-101%20EMI.pdf
[50] *TPA032D04*. (2000, June). Retrieved September 17, 2007, from Texas Instruments: http://focus.ti.com/lit/ds/slos203b/slos203b.pdf
[51] http://www.national.com/news/images/LM4673_74.jpg
[52] *Class D Audio Amplifiers Save Battery Life*. (2002, September 28). Retrieved September 20, 2007, from Maxim: http://www.maxim-ic.com/appnotes.cfm/appnote_number/1760
[53] http://www.national.com/onlineseminar/2007/emi/National_ReducingEMIinClassDAudioApps.pdf
[54] http://www.maxim-ic.com/appnotes.cfm/an_pk/624
[55] *Class D Audio Output Filter Optimization.* (2002, April 1). Retrieved December 11, 2007, from Dallas/Maxim Semiconductor: http://www.maxim-ic.com/appnotes.cfm/an_pk/624
[56] http://www.maxim-ic.com/appnotes.cfm/an_pk/624
[57] http://www.maxim-ic.com/appnotes.cfm/an_pk/624
[58] http://www.maxim-ic.com/appnotes.cfm/an_pk/624

[59] http://media.maxim-ic.com/images/appnotes/3201/3201Fig01.gif
[60] *eFunda: Introduction to Nyquist Sampling Rate*. (2007). Retrieved December 8, 2007, from eFunda: The Ultimate Online Reference for Engineers: http://www.efunda.com/DesignStandards/sensors/methods/DSP_nyquist.cfm
[61] *Pulse-Width Modulator Operates at Various Levels of Frequency and Power*. (2004, April 23). Retrieved March 28, 2008, from Maxim: http://www.maxim-ic.com.cn/appnotes.cfm/an_pk/3201
[62] *tlc274.pdf*. (2001, March). Retrieved December 8, 2007, from Texas Instruments: http://focus.ti.com/lit/ds/symlink/tlc274.pdf
[63] *AD826.pdf*. (2000). Retrieved December 8, 2007, from Analog Devices, Inc.: http://www.analog.com/UploadedFiles/Data_Sheets/AD826.pdf
[64] *DS1090.pdf*. (2007, July). Retrieved September 8, 2007, from Maxim/Dallas Semiconductor: http://datasheets.maxim-ic.com/en/ds/DS1090.pdf
[65] Cox, S., & Candy, B. (2006). *Class-D Audio Amplifiers with Negative Needback.* Retrieved December 11, 2007, from SIAM Journal on Applied Mathematics: http://eprints.nottingham.ac.uk/501/1/final.pdf
[66] Leach, W. M. (2001). *The Class-D Amplifier.* Retrieved December 8, 2007, from http://www.ee.ucr.edu/~rlake/EE135/Class_D_amp_notes_AL.pdf
[67] Chang, J. S., Gwee, B. H., Lon, Y. S., & Tan, M. T. (2001). *A Novel Low-Power Low-Voltage Class D Amplifier with Feedback for Improving THD, Power Efficiency and Gain Linearity.* Retrieved December 6, 2007, from ieeexplore.ieee.org/iel5/7344/19933/00921936.pdf
[68] Leach, W. M. (2001). *The Class-D Amplifier.* Retrieved December 8, 2007, from http://www.ee.ucr.edu/~rlake/EE135/Class_D_amp_notes_AL.pdf
[69] Lynch, F. (2001). *win01_pg14-15.pdf.* Retrieved September 22, 2007, from Mircrosemi: http://www.microsemi.com/microcurrents/win01_pg14-15.pdf
[70] Chang, J. S., Gwee, B. H., Lon, Y. S., & Tan, M. T. (2001). *A Novel Low-Power Low-Voltage Class D Amplifier with Feedback for Improving THD, Power Efficiency and Gain Linearity.* Retrieved December 6, 2007, from ieeexplore.ieee.org/iel5/7344/19933/00921936.pdf
[71] (2007). Retrieved March 28, 2008, from Advanced Circuits: http://www.4pcb.com/
[72] *Audio Specifications*. (2000). Retrieved March 28, 2008, from Rane: http://rane.com/note145.html

Un-cited References:

[i] Harden, Paul. (2003).“The Handiman's Guide to MOSFET “Switched Mode” Amplifiers.” *QRP_P.* Retrieved September 8, 2007, from http://www.aoc.nrao.edu/~pharden/hobby/_ClassDEF1.pdf
[ii] Kutkut, Nasser. (Year unknown). “Technical Note: High Efficiency Power Switches.” *Power Designers.* Retrieved September 9, 2007, from http://www.powerdesigners.com/pdf/High%20Efficiency%20Power%20Switches.pdf
[iii] Randall, Ron. (2005). “Choosing IGBTs vs. MOSFETs in SMPS apps.” *Fairchild Semiconductor.* Retrieved September 8, 2007, from http://www.electronicproducts.com/ShowPage.asp?FileName=fairchild.oct2005.html
[iv] [Author Unknown]. (2000). “Application Note 165: CS4297A/CS4299 EMI REDUCTION TECHNIQUES.” *Cirrus Logic.* Retrieved September 12, 2007, from http://www.ortodoxism.ro/datasheets/Cirrus_Logic/mXyqwqs.pdf
[v] Score, Mike. (1999). “Reducing the Output Filter of a Class-D Amplifier.” *Texas Instruments Incorporated.* Retrieved September 10, 2007, from http://focus.ti.com/lit/an/slyt198/slyt198.pdf
[vi] Yu, Shiang-Huwa, and Tseng, Ming Hung. “Modulation and Control of a Three-Level Class D Audio Power Amplifier,” [Online document], National Sun Yat-Sen University. 2005. Accessed on 12/11/2007 from <ieeexplore.ieee.org/iel5/10774/33940/01619916.pdf >

B. MOSFET Data Sheets

<1A:
http://www.diodes.com/datasheets/ds30787.pdf
http://www.nxp.com/acrobat_download/datasheets/BSH103_4.pdf
http://www.nxp.com/acrobat_download/datasheets/BSH114-01.pdf
1A - 5A:
http://rocky.digikey.com/WebLib/Toshiba/Web%20Data/2SK3758,3760,3761,3762,3763.pdf
http://www.semicon.panasonic.co.jp/ds2/SJF00029BED.pdf
5A - 10 A:
http://www.irf.com/product-info/datasheets/data/irf6662pbf.pdf
http://www.irf.com/product-info/datasheets/data/irf7201.pdf
http://www.semicon.panasonic.co.jp/ds2/SJG00008BED.pdf
10A - 20A:
http://www.irf.com/product-info/datasheets/data/irf6636.pdf
http://www.fairchildsemi.com/ds/FD%2FFDZ7296.pdf
http://www.nxp.com/acrobat_download/datasheets/PHD16N03T-01.pdf
>20A:
http://www.irf.com/product-info/datasheets/data/irf6635.pdf
http://documentation.renesas.com/eng/products/transistor/rej03g1190_hat2134hds.pdf
http://www.nxp.com/acrobat_download/datasheets/PHP_PHB176NQ04T-01.pdf

C. Battery Selection Data Sheets

http://data.energizer.com/PDFs/EN91.pdf

http://data.energizer.com/images/en92.jpg

http://data.energizer.com/PDFs/EN93.pdf

http://data.energizer.com/PDFs/EN95.pdf

http://data.energizer.com/PDFs/EN22.pdf

D. Maxim Description of Figure 1.17

Figure 1.17 shows a simplified functional diagram of the MAX9700 filterless modulator topology. Unlike the traditional PWM BTL amplifier, each half bridge has its own dedicated comparator, which allows each output to be controlled independently. The modulator is driven with a differential audio signal and a high-frequency sawtooth waveform. When both comparator outputs are low, each output of the Class D amplifier is high. At the same time, the output of the NOR gate goes high, but is delayed by the RC circuit formed by R_{ON} and C_{ON}. Once the delayed output of the NOR gate exceeds a specified threshold, switches SW1 and SW2 close. This causes OUT+ and OUT- to go low and remain as such until the next sampling period begins. This scheme causes both outputs to be on for a minimum amount of time ($t_{ON(MIN)}$), which is set by the values of R_{ON} and C_{ON}.

E. THD Testing Data

THD Testing: Two-level Board				
Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	20	4.8	1.738E+00	3.020E+00
2	40	-40.0	1.000E-02	1.000E-04
3	60	-37.2	1.380E-02	1.905E-04
4	80	-43.6	6.607E-03	4.365E-05
5	100	-46.0	5.012E-03	2.512E-05
6	120	-58.0	1.259E-03	1.585E-06
7	140	-48.0	3.981E-03	1.585E-05
8	160	-58.0	1.259E-03	1.585E-06
9	180	-54.8	1.820E-03	3.311E-06
10	200	-58.0	1.259E-03	1.585E-06
THD [%]	1.126			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	30	8.0	2.512E+00	6.310E+00
2	60	-48.8	3.631E-03	1.318E-05
3	90	-34.4	1.905E-02	3.631E-04
4	120	-38.4	1.202E-02	1.445E-04
5	150	-39.6	1.047E-02	1.096E-04
6	180	-40.8	9.120E-03	8.318E-05
7	210	-42.0	7.943E-03	6.310E-05
8	240	-46.0	5.012E-03	2.512E-05
9	270	-54.8	1.820E-03	3.311E-06
10	300	-50.8	2.884E-03	8.318E-06
THD [%]	1.135			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	40	8.8	2.754E+00	7.586E+00
2	80	-34.0	1.995E-02	3.981E-04
3	120	-34.0	1.995E-02	3.981E-04
4	160	-48.8	3.631E-03	1.318E-05
5	200	-36.4	1.514E-02	2.291E-04
6	240	-39.6	1.047E-02	1.096E-04
7	280	-39.6	1.047E-02	1.096E-04
8	320	-39.6	1.047E-02	1.096E-04
9	360	-40.8	9.120E-03	8.318E-05
10	400	-58.0	1.259E-03	1.585E-06
THD [%]	1.384			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	50	9.6	3.020E+00	9.120E+00
2	100	-50.8	2.884E-03	8.318E-06
3	150	-44.8	5.754E-03	3.311E-05
4	200	-40.8	9.120E-03	8.318E-05
5	250	-33.2	2.188E-02	4.786E-04
6	300	-41.6	8.318E-03	6.918E-05
7	350	-40.8	9.120E-03	8.318E-05
8	400	-40.4	9.550E-03	9.120E-05
9	450	-43.2	6.918E-03	4.786E-05
10	500	-52.0	2.512E-03	6.310E-06
THD [%]	0.994			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	60	10.0	3.162E+00	1.000E+01
2	120	-54.8	1.820E-03	3.311E-06
3	180	-36.0	1.585E-02	2.512E-04
4	240	-50.8	2.884E-03	8.318E-06
5	300	-30.8	2.884E-02	8.318E-04
6	360	-58.0	1.259E-03	1.585E-06
7	420	-38.4	1.202E-02	1.445E-04
8	480	-58.0	1.259E-03	1.585E-06
9	540	-58.0	1.259E-03	1.585E-06
10	600	-46.8	4.571E-03	2.089E-05
THD [%]	1.125			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	70	10.0	3.162E+00	1.000E+01
2	140	-50.8	2.884E-03	8.318E-06
3	210	-29.2	3.467E-02	1.202E-03
4	280	-50.8	2.884E-03	8.318E-06
5	350	-28.0	3.981E-02	1.585E-03
6	420	-44.0	6.310E-03	3.981E-05
7	490	-38.4	1.202E-02	1.445E-04
8	560	-54.8	1.820E-03	3.311E-06
9	630	-58.0	1.259E-03	1.585E-06
10	700	-52.0	2.512E-03	6.310E-06
THD [%]	1.732			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	80	10.4	3.311E+00	1.096E+01
2	160	-46.0	5.012E-03	2.512E-05
3	240	-25.6	5.248E-02	2.754E-03
4	320	-44.0	6.310E-03	3.981E-05
5	400	-26.4	4.786E-02	2.291E-03
6	480	-46.8	4.571E-03	2.089E-05
7	560	-37.6	1.318E-02	1.738E-04
8	640	-58.0	1.259E-03	1.585E-06
9	720	-58.0	1.259E-03	1.585E-06
10	800	-50.8	2.884E-03	8.318E-06
THD [%]	2.202			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	90	10.4	3.311E+00	1.096E+01
2	180	-48.4	3.802E-03	1.445E-05
3	270	-24.8	5.754E-02	3.311E-03
4	360	-42.0	7.943E-03	6.310E-05
5	450	-26.0	5.012E-02	2.512E-03
6	540	-40.8	9.120E-03	8.318E-05
7	630	-38.4	1.202E-02	1.445E-04
8	720	-54.8	1.820E-03	3.311E-06
9	810	-54.8	1.820E-03	3.311E-06
10	900	-54.8	1.820E-03	3.311E-06
THD [%]	2.366			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	100	10.4	3.311E+00	1.096E+01
2	200	-38.0	1.259E-02	1.585E-04
3	300	-24.8	5.754E-02	3.311E-03
4	400	-40.8	9.120E-03	8.318E-05
5	500	-26.0	5.012E-02	2.512E-03
6	600	-39.2	1.096E-02	1.202E-04
7	700	-38.4	1.202E-02	1.445E-04
8	800	-39.6	1.047E-02	1.096E-04
9	900	-58.0	1.259E-03	1.585E-06
10	1000	-58.0	1.259E-03	1.585E-06
THD [%]	2.424			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	200	10.4	3.311E+00	1.096E+01
2	400	-29.2	3.467E-02	1.202E-03
3	600	-26.4	4.786E-02	2.291E-03
4	800	-37.2	1.380E-02	1.905E-04
5	1000	-26.8	4.571E-02	2.089E-03
6	1200	-50.0	3.162E-03	1.000E-05
7	1400	-47.4	4.266E-03	1.820E-05
8	1600	-50.8	2.884E-03	8.318E-06
9	1800	-35.4	1.698E-02	2.884E-04
10	2000	-40.0	1.000E-02	1.000E-04
THD [%]	2.378			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	300	10.4	3.311E+00	1.096E+01
2	600	-29.2	3.467E-02	1.202E-03
3	900	-28.0	3.981E-02	1.585E-03
4	1200	-37.6	1.318E-02	1.738E-04
5	1500	-26.4	4.786E-02	2.291E-03
6	1800	-53.2	2.188E-03	4.786E-06
7	2100	-40.0	1.000E-02	1.000E-04
8	2400	-53.6	2.089E-03	4.365E-06
9	2700	-36.0	1.585E-02	2.512E-04
10	3000	-40.8	9.120E-03	8.318E-05
THD [%]	2.279			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	400	10.4	3.311E+00	1.096E+01
2	800	-29.2	3.467E-02	1.202E-03
3	1200	-27.2	4.365E-02	1.905E-03
4	1600	-38.0	1.259E-02	1.585E-04
5	2000	-26.4	4.786E-02	2.291E-03
6	2400	-55.0	1.778E-03	3.162E-06
7	2800	-40.8	9.120E-03	8.318E-05
8	3200	-54.0	1.995E-03	3.981E-06
9	3600	-38.4	1.202E-02	1.445E-04
10	4000	-41.6	8.318E-03	6.918E-05
THD [%]	2.312			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	500	10.4	3.311E+00	1.096E+01
2	1000	-29.6	3.311E-02	1.096E-03
3	1500	-29.2	3.467E-02	1.202E-03
4	2000	-38.0	1.259E-02	1.585E-04
5	2500	-26.4	4.786E-02	2.291E-03
6	3000	-50.8	2.884E-03	8.318E-06
7	3500	-46.4	4.786E-03	2.291E-05
8	4000	-56.0	1.585E-03	2.512E-06
9	4500	-35.6	1.660E-02	2.754E-04
10	5000	-42.0	7.943E-03	6.310E-05
THD [%]	2.161			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	600	10.4	3.311E+00	1.096E+01
2	1200	-30.0	3.162E-02	1.000E-03
3	1800	-29.6	3.311E-02	1.096E-03
4	2400	-42.0	7.943E-03	6.310E-05
5	3000	-26.0	5.012E-02	2.512E-03
6	3600	-50.0	3.162E-03	1.000E-05
7	4200	-41.6	8.318E-03	6.918E-05
8	4800	-58.8	1.148E-03	1.318E-06
9	5400	-40.4	9.550E-03	9.120E-05
10	6000	-44.0	6.310E-03	3.981E-05
THD [%]	2.110			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	700	10.4	3.311E+00	1.096E+01
2	1400	-30.0	3.162E-02	1.000E-03
3	2100	-31.2	2.754E-02	7.586E-04
4	2800	-38.8	1.148E-02	1.318E-04
5	3500	-26.8	4.571E-02	2.089E-03
6	4200	-49.2	3.467E-03	1.202E-05
7	4900	-51.2	2.754E-03	7.586E-06
8	5600	-60.0	1.000E-03	1.000E-06
9	6300	-36.4	1.514E-02	2.291E-04
10	7000	-48.4	3.802E-03	1.445E-05
THD [%]	1.967			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	800	10.4	3.311E+00	1.096E+01
2	1600	-30.4	3.020E-02	9.120E-04
3	2400	-33.6	2.089E-02	4.365E-04
4	3200	-38.8	1.148E-02	1.318E-04
5	4000	-26.0	5.012E-02	2.512E-03
6	4800	-48.0	3.981E-03	1.585E-05
7	5600	-41.2	8.710E-03	7.586E-05
8	6400	-63.2	6.918E-04	4.786E-07
9	7200	-38.4	1.202E-02	1.445E-04
10	8000	-50.8	2.884E-03	8.318E-06
THD [%]	1.966			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	900	10.4	3.311E+00	1.096E+01
2	1800	-30.4	3.020E-02	9.120E-04
3	2700	-32.4	2.399E-02	5.754E-04
4	3600	-38.8	1.148E-02	1.318E-04
5	4500	-27.2	4.365E-02	1.905E-03
6	5400	-47.2	4.365E-03	1.905E-05
7	6300	-53.6	2.089E-03	4.365E-06
8	7200	-57.2	1.380E-03	1.905E-06
9	8100	-37.6	1.318E-02	1.738E-04
10	9000	-48.4	3.802E-03	1.445E-05
THD [%]	1.846			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	1000	10.4	3.311E+00	1.096E+01
2	2000	-31.8	2.570E-02	6.607E-04
3	3000	-33.6	2.089E-02	4.365E-04
4	4000	-39.6	1.047E-02	1.096E-04
5	5000	-26.4	4.786E-02	2.291E-03
6	6000	-46.0	5.012E-03	2.512E-05
7	7000	-42.4	7.586E-03	5.754E-05
8	8000	-57.2	1.380E-03	1.905E-06
9	9000	-36.8	1.445E-02	2.089E-04
10	10000	-46.0	5.012E-03	2.512E-05
THD [%]	1.866			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	2000	10.0	3.162E+00	1.000E+01
2	4000	-32.4	2.399E-02	5.754E-04
3	6000	-40.0	1.000E-02	1.000E-04
4	8000	-46.4	4.786E-03	2.291E-05
5	10000	-30.0	3.162E-02	1.000E-03
6	12000	-47.6	4.169E-03	1.738E-05
7	14000	-46.0	5.012E-03	2.512E-05
8	16000	-41.6	8.318E-03	6.918E-05
9	18000	-42.0	7.943E-03	6.310E-05
10	20000	-44.4	6.026E-03	3.631E-05
THD [%]	1.382			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	3000	10.0	3.162E+00	1.000E+01
2	6000	-34.0	1.995E-02	3.981E-04
3	9000	-28.8	3.631E-02	1.318E-03
4	12000	-38.0	1.259E-02	1.585E-04
5	15000	-32.0	2.512E-02	6.310E-04
6	18000	-41.6	8.318E-03	6.918E-05
7	21000	-49.2	3.467E-03	1.202E-05
8	24000	-48.0	3.981E-03	1.585E-05
9	27000	-49.2	3.467E-03	1.202E-05
10	30000	-57.2	1.380E-03	1.905E-06
THD [%]	1.618			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	4000	9.6	3.020E+00	9.120E+00
2	8000	-37.2	1.380E-02	1.905E-04
3	12000	-25.6	5.248E-02	2.754E-03
4	16000	-36.4	1.514E-02	2.291E-04
5	20000	-34.4	1.905E-02	3.631E-04
6	24000	-38.4	1.202E-02	1.445E-04
7	28000	-63.2	6.918E-04	4.786E-07
8	32000	-53.2	2.188E-03	4.786E-06
9	36000	-50.0	3.162E-03	1.000E-05
10	40000	-63.2	6.918E-04	4.786E-07
THD [%]	2.013			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	5000	9.2	2.884E+00	8.318E+00
2	10000	-38.4	1.202E-02	1.445E-04
3	15000	-23.2	6.918E-02	4.786E-03
4	20000	-35.2	1.738E-02	3.020E-04
5	25000	-35.2	1.738E-02	3.020E-04
6	30000	-42.8	7.244E-03	5.248E-05
7	35000	-48.0	3.981E-03	1.585E-05
8	40000	-44.0	6.310E-03	3.981E-05
9	45000	-46.0	5.012E-03	2.512E-05
10	50000	-51.2	2.754E-03	7.586E-06
THD [%]	2.612			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	6000	9.2	2.884E+00	8.318E+00
2	12000	-35.2	1.738E-02	3.020E-04
3	18000	-21.6	8.318E-02	6.918E-03
4	24000	-40.0	1.000E-02	1.000E-04
5	30000	-36.4	1.514E-02	2.291E-04
6	36000	-60.0	1.000E-03	1.000E-06
7	42000	-54.0	1.995E-03	3.981E-06
8	48000	-50.8	2.884E-03	8.318E-06
9	54000	-46.8	4.571E-03	2.089E-05
10	60000	-57.2	1.380E-03	1.905E-06
THD [%]	3.020			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	7000	8.8	2.754E+00	7.586E+00
2	14000	-33.6	2.089E-02	4.365E-04
3	21000	-22.0	7.943E-02	6.310E-03
4	28000	-44.4	6.026E-03	3.631E-05
5	35000	-37.6	1.318E-02	1.738E-04
6	42000	-47.2	4.365E-03	1.905E-05
7	49000	-48.4	3.802E-03	1.445E-05
8	56000	-60.0	1.000E-03	1.000E-06
9	63000	-50.0	3.162E-03	1.000E-05
10	70000	-56.0	1.585E-03	2.512E-06
THD [%]	3.038			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	8000	8.4	2.630E+00	6.918E+00
2	16000	-31.2	2.754E-02	7.586E-04
3	24000	-23.2	6.918E-02	4.786E-03
4	32000	-57.2	1.380E-03	1.905E-06
5	40000	-37.2	1.380E-02	1.905E-04
6	48000	-50.8	2.884E-03	8.318E-06
7	56000	-49.2	3.467E-03	1.202E-05
8	64000	-50.8	2.884E-03	8.318E-06
9	72000	-60.0	1.000E-03	1.000E-06
10	80000	-54.0	1.995E-03	3.981E-06
THD [%]	2.888			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	9000	8.4	2.630E+00	6.918E+00
2	18000	-30.0	3.162E-02	1.000E-03
3	27000	-22.8	7.244E-02	5.248E-03
4	36000	-50.0	3.162E-03	1.000E-05
5	45000	-39.6	1.047E-02	1.096E-04
6	54000	-53.2	2.188E-03	4.786E-06
7	63000	-60.0	1.000E-03	1.000E-06
8	72000	-52.0	2.512E-03	6.310E-06
9	81000	-56.0	1.585E-03	2.512E-06
10	90000	-56.0	1.585E-03	2.512E-06
THD [%]	3.038			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	10000	8.0	2.512E+00	6.310E+00
2	20000	-27.6	4.169E-02	1.738E-03
3	30000	-22.8	7.244E-02	5.248E-03
4	40000	-56.0	1.585E-03	2.512E-06
5	50000	-38.8	1.148E-02	1.318E-04
6	60000	-51.2	2.754E-03	7.586E-06
7	70000	-48.8	3.631E-03	1.318E-05
8	80000	-60.0	1.000E-03	1.000E-06
9	90000	-63.2	6.918E-04	4.786E-07
10	100000	-56.0	1.585E-03	2.512E-06
THD [%]	3.365			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	11000	7.6	2.399E+00	5.754E+00
2	22000	-26.0	5.012E-02	2.512E-03
3	33000	-24.0	6.310E-02	3.981E-03
4	44000	-53.2	2.188E-03	4.786E-06
5	55000	-54.0	1.995E-03	3.981E-06
6	66000	-56.0	1.585E-03	2.512E-06
7	77000	-53.2	2.188E-03	4.786E-06
8	88000	-63.2	6.918E-04	4.786E-07
9	99000	-56.0	1.585E-03	2.512E-06
10	110000	-60.0	1.000E-03	1.000E-06
THD [%]	3.364			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	12000	7.2	2.291E+00	5.248E+00
2	24000	-52.0	2.512E-03	6.310E-06
3	36000	-24.8	5.754E-02	3.311E-03
4	48000	-46.0	5.012E-03	2.512E-05
5	60000	-41.6	8.318E-03	6.918E-05
6	72000	-50.0	3.162E-03	1.000E-05
7	84000	-63.2	6.918E-04	4.786E-07
8	96000	-66.0	5.012E-04	2.512E-07
9	108000	-56.0	1.585E-03	2.512E-06
10	120000	-60.0	1.000E-03	1.000E-06
THD [%]	2.555			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	13000	6.8	2.188E+00	4.786E+00
2	26000	-30.8	2.884E-02	8.318E-04
3	39000	-25.2	5.495E-02	3.020E-03
4	52000	-53.6	2.089E-03	4.365E-06
5	65000	-48.0	3.981E-03	1.585E-05
6	78000	-63.2	6.918E-04	4.786E-07
7	91000	-48.0	3.981E-03	1.585E-05
8	104000	-60.0	1.000E-03	1.000E-06
9	117000	-56.0	1.585E-03	2.512E-06
10	130000	-60.0	1.000E-03	1.000E-06
THD [%]	2.852			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	14000	6.8	2.188E+00	4.786E+00
2	28000	-32.4	2.399E-02	5.754E-04
3	42000	-25.2	5.495E-02	3.020E-03
4	56000	-63.2	6.918E-04	4.786E-07
5	70000	-44.8	5.754E-03	3.311E-05
6	84000	-52.0	2.512E-03	6.310E-06
7	98000	-63.2	6.918E-04	4.786E-07
8	112000	-60.0	1.000E-03	1.000E-06
9	126000	-63.2	6.918E-04	4.786E-07
10	140000	-63.2	6.918E-04	4.786E-07
THD [%]	2.757			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	15000	6.4	2.089E+00	4.365E+00
2	30000	-33.2	2.188E-02	4.786E-04
3	45000	-26.4	4.786E-02	2.291E-03
4	60000	-52.0	2.512E-03	6.310E-06
5	75000	-51.2	2.754E-03	7.586E-06
6	90000	-63.2	6.918E-04	4.786E-07
7	105000	-56.0	1.585E-03	2.512E-06
8	120000	-60.0	1.000E-03	1.000E-06
9	135000	-63.2	6.918E-04	4.786E-07
10	150000	-60.0	1.000E-03	1.000E-06
THD [%]	2.528			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	16000	6.0	1.995E+00	3.981E+00
2	32000	-34.8	1.820E-02	3.311E-04
3	48000	-27.6	4.169E-02	1.738E-03
4	64000	-53.6	2.089E-03	4.365E-06
5	80000	-46.0	5.012E-03	2.512E-05
6	96000	-52.0	2.512E-03	6.310E-06
7	112000	-54.0	1.995E-03	3.981E-06
8	128000	-63.2	6.918E-04	4.786E-07
9	144000	-63.2	6.918E-04	4.786E-07
10	160000	-60.0	1.000E-03	1.000E-06
THD [%]	2.303			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	17000	6.0	1.995E+00	3.981E+00
2	34000	-37.2	1.380E-02	1.905E-04
3	51000	-27.6	4.169E-02	1.738E-03
4	68000	-57.2	1.380E-03	1.905E-06
5	85000	-50.4	3.020E-03	9.120E-06
6	102000	-63.2	6.918E-04	4.786E-07
7	119000	-60.0	1.000E-03	1.000E-06
8	136000	-63.2	6.918E-04	4.786E-07
9	153000	-60.0	1.000E-03	1.000E-06
10	170000	-63.2	6.918E-04	4.786E-07
THD [%]	2.209			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	18000	5.6	1.905E+00	3.631E+00
2	36000	-38.8	1.148E-02	1.318E-04
3	54000	-28.0	3.981E-02	1.585E-03
4	72000	-53.2	2.188E-03	4.786E-06
5	90000	-47.6	4.169E-03	1.738E-05
6	108000	-63.2	6.918E-04	4.786E-07
7	126000	-63.2	6.918E-04	4.786E-07
8	144000	-56.0	1.585E-03	2.512E-06
9	162000	-63.2	6.918E-04	4.786E-07
10	180000	-60.0	1.000E-03	1.000E-06
THD [%]	2.192			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	19000	5.2	1.820E+00	3.311E+00
2	38000	-39.6	1.047E-02	1.096E-04
3	57000	-29.2	3.467E-02	1.202E-03
4	76000	-57.2	1.380E-03	1.905E-06
5	95000	-52.0	2.512E-03	6.310E-06
6	114000	-63.2	6.918E-04	4.786E-07
7	133000	-56.0	1.585E-03	2.512E-06
8	152000	-57.2	1.380E-03	1.905E-06
9	171000	-60.0	1.000E-03	1.000E-06
10	190000	-63.2	6.918E-04	4.786E-07
THD [%]	2.001			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	20000	5.2	1.820E+00	3.311E+00
2	40000	-38.8	1.148E-02	1.318E-04
3	60000	-30.4	3.020E-02	9.120E-04
4	80000	-60.0	1.000E-03	1.000E-06
5	100000	-46.0	5.012E-03	2.512E-05
6	120000	-56.0	1.585E-03	2.512E-06
7	140000	-53.2	2.188E-03	4.786E-06
8	160000	-63.2	6.918E-04	4.786E-07
9	180000	-53.6	2.089E-03	4.365E-06
10	200000	-56.0	1.585E-03	2.512E-06
THD [%]	1.810			

THD Testing: Three-level Board

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	20	15.2	5.754E+00	3.311E+01
2	40	-33.6	2.089E-02	4.365E-04
3	60	-29.6	3.311E-02	1.096E-03
4	80	-31.2	2.754E-02	7.586E-04
5	100	-28.8	3.631E-02	1.318E-03
THD [%]	1.044			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	30	15.2	5.754E+00	3.311E+01
2	60	-30.0	3.162E-02	1.000E-03
3	90	-26.8	4.571E-02	2.089E-03
4	120	-34.4	1.905E-02	3.631E-04
5	150	-36.4	1.514E-02	2.291E-04
THD [%]	1.054			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	40	14.8	5.495E+00	3.020E+01
2	80	-34.0	1.995E-02	3.981E-04
3	120	-30.4	3.020E-02	9.120E-04
4	160	-42.8	7.244E-03	5.248E-05
5	200	-40.8	9.120E-03	8.318E-05
THD [%]	0.692			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	50	15.6	6.026E+00	3.631E+01
2	100	-30.0	3.162E-02	1.000E-03
3	150	-28.4	3.802E-02	1.445E-03
4	200	-30.0	3.162E-02	1.000E-03
5	250	-28.4	3.802E-02	1.445E-03
THD [%]	1.161			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	60	15.2	5.754E+00	3.311E+01
2	120	-31.6	2.630E-02	6.918E-04
3	180	-28.8	3.631E-02	1.318E-03
4	240	-34.4	1.905E-02	3.631E-04
5	300	-27.6	4.169E-02	1.738E-03
THD [%]	1.114			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	70	15.6	6.026E+00	3.631E+01
2	140	-31.2	2.754E-02	7.586E-04
3	210	-28.4	3.802E-02	1.445E-03
4	280	-30.8	2.884E-02	8.318E-04
5	350	-30.0	3.162E-02	1.000E-03
THD [%]	1.054			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	80	15.6	6.026E+00	3.631E+01
2	160	-32.8	2.291E-02	5.248E-04
3	240	-28.4	3.802E-02	1.445E-03
4	320	-34.0	1.995E-02	3.981E-04
5	400	-30.0	3.162E-02	1.000E-03
THD [%]	0.963			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	90	15.6	6.026E+00	3.631E+01
2	180	-32.8	2.291E-02	5.248E-04
3	270	-26.8	4.571E-02	2.089E-03
4	360	-34.0	1.995E-02	3.981E-04
5	450	-26.8	4.571E-02	2.089E-03
THD [%]	1.185			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	100	15.6	6.026E+00	3.631E+01
2	200	-30.4	3.020E-02	9.120E-04
3	300	-28.4	3.802E-02	1.445E-03
4	400	-36.8	1.445E-02	2.089E-04
5	500	-26.0	5.012E-02	2.512E-03
THD [%]	1.183			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	200	15.6	6.026E+00	3.631E+01
2	400	-42.8	7.244E-03	5.248E-05
3	600	-36.8	1.445E-02	2.089E-04
4	800	-50.0	3.162E-03	1.000E-05
5	1000	-42.8	7.244E-03	5.248E-05
THD [%]	0.299			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	300	15.6	6.026E+00	3.631E+01
2	600	-34.8	1.820E-02	3.311E-04
3	900	-26.8	4.571E-02	2.089E-03
4	1200	-40.8	9.120E-03	8.318E-05
5	1500	-36.0	1.585E-02	2.512E-04
THD [%]	0.871			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	400	15.6	6.026E+00	3.631E+01
2	800	-32.8	2.291E-02	5.248E-04
3	1200	-28.4	3.802E-02	1.445E-03
4	1600	-36.8	1.445E-02	2.089E-04
5	2000	-44.4	6.026E-03	3.631E-05
THD [%]	0.781			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	500	15.6	6.026E+00	3.631E+01
2	1000	-34.8	1.820E-02	3.311E-04
3	1500	-30.0	3.162E-02	1.000E-03
4	2000	-33.6	2.089E-02	4.365E-04
5	2500	-31.2	2.754E-02	7.586E-04
THD [%]	0.834			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	600	15.2	5.754E+00	3.311E+01
2	1200	-34.8	1.820E-02	3.311E-04
3	1800	-39.6	1.047E-02	1.096E-04
4	2400	-32.8	2.291E-02	5.248E-04
5	3000	-28.0	3.981E-02	1.585E-03
THD [%]	0.878			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	700	15.6	6.026E+00	3.631E+01
2	1400	-32.8	2.291E-02	5.248E-04
3	2100	-36.0	1.585E-02	2.512E-04
4	2800	-34.0	1.995E-02	3.981E-04
5	3500	-31.6	2.630E-02	6.918E-04
THD [%]	0.717			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	800	15.2	5.754E+00	3.311E+01
2	1600	-34.8	1.820E-02	3.311E-04
3	2400	-28.4	3.802E-02	1.445E-03
4	3200	-34.8	1.820E-02	3.311E-04
5	4000	-43.6	6.607E-03	4.365E-05
THD [%]	0.806			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	900	15.2	5.754E+00	3.311E+01
2	1800	-34.0	1.995E-02	3.981E-04
3	2700	-26.8	4.571E-02	2.089E-03
4	3600	-33.6	2.089E-02	4.365E-04
5	4500	-29.6	3.311E-02	1.096E-03
THD [%]	1.102			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	1000	15.6	6.026E+00	3.631E+01
2	2000	-34.8	1.820E-02	3.311E-04
3	3000	-26.4	4.786E-02	2.291E-03
4	4000	-32.8	2.291E-02	5.248E-04
5	5000	-25.6	5.248E-02	2.754E-03
THD [%]	1.275			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	2000	15.2	5.754E+00	3.311E+01
2	4000	-36.8	1.445E-02	2.089E-04
3	6000	-31.6	2.630E-02	6.918E-04
4	8000	-37.2	1.380E-02	1.905E-04
5	10000	-35.2	1.738E-02	3.020E-04
THD [%]	0.649			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	3000	15.2	5.754E+00	3.311E+01
2	6000	-32.8	2.291E-02	5.248E-04
3	9000	-40.0	1.000E-02	1.000E-04
4	12000	-36.0	1.585E-02	2.512E-04
5	15000	-29.2	3.467E-02	1.202E-03
THD [%]	0.792			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	4000	15.2	5.754E+00	3.311E+01
2	8000	-28.4	3.802E-02	1.445E-03
3	12000	-30.0	3.162E-02	1.000E-03
4	16000	-36.4	1.514E-02	2.291E-04
5	20000	-28.0	3.981E-02	1.585E-03
THD [%]	1.134			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	5000	15.2	5.754E+00	3.311E+01
2	10000	-33.2	2.188E-02	4.786E-04
3	15000	-29.6	3.311E-02	1.096E-03
4	20000	-36.0	1.585E-02	2.512E-04
5	25000	-31.2	2.754E-02	7.586E-04
THD [%]	0.884			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	6000	15.2	5.754E+00	3.311E+01
2	12000	-36.8	1.445E-02	2.089E-04
3	18000	-25.2	5.495E-02	3.020E-03
4	24000	-36.8	1.445E-02	2.089E-04
5	30000	-38.4	1.202E-02	1.445E-04
THD [%]	1.040			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	7000	15.2	5.754E+00	3.311E+01
2	14000	-36.0	1.585E-02	2.512E-04
3	21000	-24.0	6.310E-02	3.981E-03
4	28000	-35.6	1.660E-02	2.754E-04
5	35000	-29.6	3.311E-02	1.096E-03
THD [%]	1.301			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	8000	15.2	5.754E+00	3.311E+01
2	16000	-32.0	2.512E-02	6.310E-04
3	24000	-22.0	7.943E-02	6.310E-03
4	32000	-30.0	3.162E-02	1.000E-03
5	40000	-25.6	5.248E-02	2.754E-03
THD [%]	1.797			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	9000	15.2	5.754E+00	3.311E+01
2	18000	-31.6	2.630E-02	6.918E-04
3	27000	-24.4	6.026E-02	3.631E-03
4	36000	-30.0	3.162E-02	1.000E-03
5	45000	-32.8	2.291E-02	5.248E-04
THD [%]	1.329			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	10000	14.4	5.248E+00	2.754E+01
2	20000	-34.0	1.995E-02	3.981E-04
3	30000	-21.6	8.318E-02	6.918E-03
4	40000	-30.4	3.020E-02	9.120E-04
5	50000	-25.6	5.248E-02	2.754E-03
THD [%]	1.997			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	11000	14.0	5.012E+00	2.512E+01
2	22000	-36.8	1.445E-02	2.089E-04
3	33000	-26.0	5.012E-02	2.512E-03
4	44000	-32.8	2.291E-02	5.248E-04
5	55000	-34.0	1.995E-02	3.981E-04
THD [%]	1.204			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	12000	14.8	5.495E+00	3.020E+01
2	24000	-33.6	2.089E-02	4.365E-04
3	36000	-40.6	9.333E-03	8.710E-05
4	48000	-21.6	8.318E-02	6.918E-03
5	60000	-25.0	5.623E-02	3.162E-03
THD [%]	1.874			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	13000	14.4	5.248E+00	2.754E+01
2	26000	-30.0	3.162E-02	1.000E-03
3	39000	-36.8	1.445E-02	2.089E-04
4	52000	-30.0	3.162E-02	1.000E-03
5	65000	-30.8	2.884E-02	8.318E-04
THD [%]	1.051			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	14000	14.4	5.248E+00	2.754E+01
2	28000	-25.2	5.495E-02	3.020E-03
3	42000	-21.6	8.318E-02	6.918E-03
4	56000	-32.8	2.291E-02	5.248E-04
5	70000	-40.0	1.000E-02	1.000E-04
THD [%]	1.958			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	15000	14.4	5.248E+00	2.754E+01
2	30000	-22.0	7.943E-02	6.310E-03
3	45000	-31.0	2.818E-02	7.943E-04
4	60000	-26.8	4.571E-02	2.089E-03
5	75000	-32.0	2.512E-02	6.310E-04
THD [%]	1.889			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	16000	14.4	5.248E+00	2.754E+01
2	32000	-15.6	1.660E-01	2.754E-02
3	48000	-19.6	1.047E-01	1.096E-02
4	64000	-26.8	4.571E-02	2.089E-03
5	80000	-32.0	2.512E-02	6.310E-04
THD [%]	3.869			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	17000	14.0	5.012E+00	2.512E+01
2	34000	-18.4	1.202E-01	1.445E-02
3	51000	-29.2	3.467E-02	1.202E-03
4	68000	-31.2	2.754E-02	7.586E-04
5	85000	-38.0	1.259E-02	1.585E-04
THD [%]	2.569			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	18000	14.0	5.012E+00	2.512E+01
2	36000	-20.0	1.000E-01	1.000E-02
3	54000	-24.0	6.310E-02	3.981E-03
4	72000	-36.8	1.445E-02	2.089E-04
5	90000	-40.0	1.000E-02	1.000E-04
THD [%]	2.385			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	19000	14.0	5.012E+00	2.512E+01
2	38000	-22.4	7.586E-02	5.754E-03
3	57000	-30.0	3.162E-02	1.000E-03
4	76000	-30.0	3.162E-02	1.000E-03
5	95000	-44.0	6.310E-03	3.981E-05
THD [%]	1.762			

Harmonic	Frequency [Hz]	V_{rms} [dB]	V_{rms} [V]	V_{rms}^2 [V]
1	20000	13.6	4.786E+00	2.291E+01
2	40000	-23.2	6.918E-02	4.786E-03
3	60000	-24.0	6.310E-02	3.981E-03
4	80000	-32.8	2.291E-02	5.248E-04
5	100000	-35.2	1.738E-02	3.020E-04
THD [%]	2.046			

F. Project Expenses

Date	*Vendor*	*Vendor Order #*	*Description*	*Ordered by*	*Cost*	*Shipping*	*Subtotal*
11/28/2007	Digikey	20958202	Parts: FETs, driver/ Op-amp ICs	John Durst	$54.92	$13.52	$68.44
12/12/2007	Digikey	21051705	MOSFETs, resistors	Justin Cox	$22.97	$13.63	$36.60
1/16/2008	Digikey	21233967	Parts: OP-AMPs, inductors, connectors	Jayce Silvia	$59.69	$14.94	$74.63
1/28/2008	Digikey	21309966	Parts: OP-AMPs, driver ICs, connectors	Justin Cox	$55.59	$16.91	$72.50
2/6/2008	Advanced Circuits	54950	2-Level PWM PCB (x5)	Justin Cox	$264.00	$31.09	$295.09
2/11/2008	Digikey	21400376	SMT ICs, resistors, capacitors, connectors	Jayce Silvia	$254.62	$20.31	$274.93
2/19/2008	Advanced Circuits	443286	3-Level PWM PCB (x5)	Stephen J. Bitar	$264.00	$31.09	$295.09
2/22/2008	Mouser	2071552	Low ESR caps, inverters, jacks	Jayce Silvia	$42.00	$18.47	$60.47
						Total	**$1,177.75**

G. Part Datasheets

The following section includes datasheets for all parts used in our amplifier designs.

ANALOG DEVICES

High-Speed, Low-Power Dual Operational Amplifier

AD826

FEATURES

High Speed:
- **50 MHz Unity Gain Bandwidth**
- **350 V/μs Slew Rate**
- **70 ns Settling Time to 0.01%**

Low Power:
- **7.5 mA Max Power Supply Current Per Amp**

Easy to Use:
- **Drives Unlimited Capacitive Loads**
- **50 mA Min Output Current Per Amplifier**
- **Specified for +5 V, ±5 V and ±15 V Operation**
- **2.0 V p-p Output Swing into a 150 Ω Load (V_S = +5 V)**

Good Video Performance
- **Differential Gain & Phase Error of 0.07% & 0.11°**

Excellent DC Performance:
- **2.0 mV Max Input Offset Voltage**

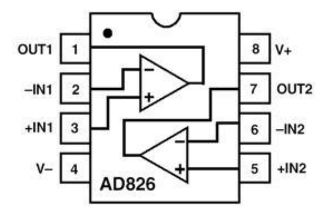
APPLICATIONS

Unity Gain ADC/DAC Buffer
Cable Drivers
8- and 10-Bit Data Acquisition Systems
Video Line Driver
Active Filters

PRODUCT DESCRIPTION

The AD826 is a dual, high speed voltage feedback op amp. It is ideal for use in applications which require unity gain stability and high output drive capability, such as buffering and cable driving. The 50 MHz bandwidth and 350 V/μs slew rate make the AD826 useful in many high speed applications including: video, CATV, copiers, LCDs, image scanners and fax machines.

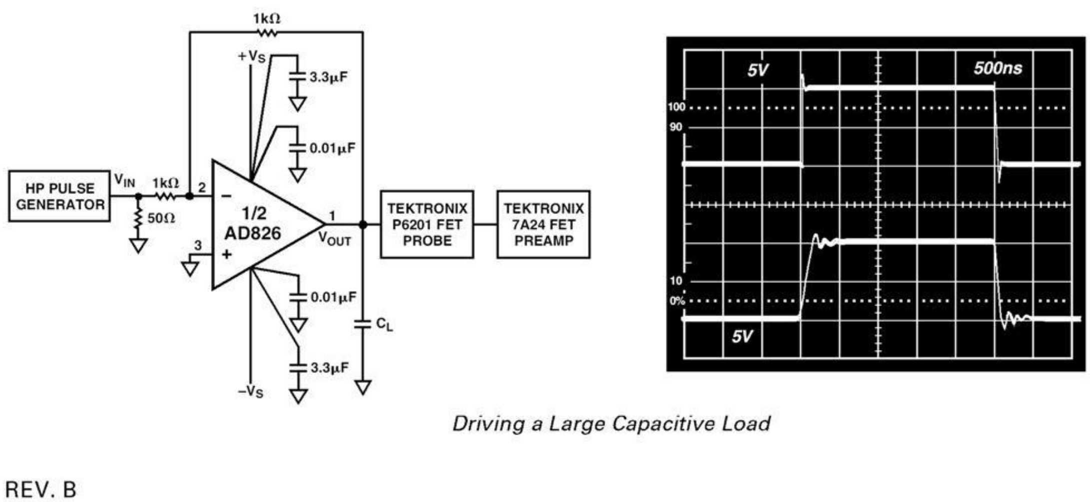
CONNECTION DIAGRAM
8-Lead Plastic Mini-DIP and SO Package



The AD826 features high output current drive capability of 50 mA min per amp, and is able to drive unlimited capacitive loads. With a low power supply current of 15 mA max for both amplifiers, the AD826 is a true general purpose operational amplifier.

The AD826 is ideal for power sensitive applications such as video cameras and portable instrumentation. The AD826 can operate from a single +5 V supply, while still achieving 25 MHz of bandwidth. Furthermore the AD826 is fully specified from a single +5 V to ±15 V power supplies.

The AD826 excels as an ADC/DAC buffer or active filter in data acquisition systems and achieves a settling time of 70 ns to 0.01%, with a low input offset voltage of 2 mV max. The AD826 is available in small 8-lead plastic mini-DIP and SO packages.



Driving a Large Capacitive Load

REV. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
© Analog Devices, Inc., 2000

AD826–SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±5 V	30	35		MHz
		±15 V	45	50		MHz
		0, +5 V	25	29		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±5 V	10	20		MHz
		±15 V	25	55		MHz
		0, +5 V	10	20		MHz
Full Power Bandwidth[1]	V_{OUT} = 5 V p-p					
	R_{LOAD} = 500 Ω	±5 V		15.9		MHz
	V_{OUT} = 20 V p-p					
	R_{LOAD} = 1 kΩ	±15 V		5.6		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	200	250		V/µs
	Gain = –1	±15 V	300	350		V/µs
		0, +5 V	150	200		V/µs
Settling Time to 0.1%	–2.5 V to +2.5 V	±5 V		45		ns
	0 V–10 V Step, A_V = –1	±15 V		45		ns
to 0.01%	–2.5 V to +2.5 V	±5 V		70		ns
	0 V–10 V Step, A_V = –1	±15 V		70		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	F_C = 1 MHz	±15 V		–78		dB
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		15		nV/√Hz
Input Current Noise	f = 10 kHz	±5 V, ±15 V		1.5		pA/√Hz
Differential Gain Error	NTSC	±15 V		0.07	0.1	%
(R1 = 150 Ω)	Gain = +2	±5 V		0.12	0.15	%
		0, +5 V		0.15		%
Differential Phase Error	NTSC	±15 V		0.11	0.15	Degrees
(R1 = 150 Ω)	Gain = +2	±5 V		0.12	0.15	Degrees
		0, +5 V		0.15		Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V to ±15 V		0.5	2	mV
	T_{MIN} to T_{MAX}				3	mV
Offset Drift				10		µV/°C
Input Bias Current		±5 V, ±15 V		3.3	6.6	µA
	T_{MIN}				10	µA
	T_{MAX}				4.4	µA
Input Offset Current		±5 V, ±15 V		25	300	nA
	T_{MIN} to T_{MAX}				500	nA
Offset Current Drift				0.3		nA/°C
Open-Loop Gain	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		2	4		V/mV
	T_{MIN} to T_{MAX}		1.5			V/mV
	R_{LOAD} = 150 Ω		1.5	3		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		3.5	6		V/mV
	T_{MIN} to T_{MAX}		2	5		V/mV
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω (50 mA Output)		2	4		V/mV
INPUT CHARACTERISTICS						
Input Resistance				300		kΩ
Input Capacitance				1.5		pF
Input Common-Mode Voltage Range		±5 V	+3.8	+4.3		V
			–2.7	–3.4		V
		±15 V	+13	+14.3		V
			–12	–13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}	±5 V	80	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
	T_{MIN} to T_{MAX}	±15 V	80	100		dB

Parameter	Conditions	V_S	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
	R_{LOAD} = 500 Ω	0, +5 V	+1.5, +3.5			V
Output Current		±15 V	50			mA
		±5 V	50			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
Output Resistance	Open Loop			8		Ω
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	f = 5 MHz	±15 V		–80		dB
Gain Flatness Match	G = +1, f = 40 MHz	±15 V		0.2		dB
Slew Rate Match	G = –1	±15 V		10		V/µs
DC						
Input Offset Voltage Match	T_{MIN}–T_{MAX}	±5 V to ±15 V		0.5	2	mV
Input Bias Current Match	T_{MIN}–T_{MAX}	±5 V to ±15 V		0.06	0.8	µA
Open-Loop Gain Match	V_O = ±10 V, R_{LOAD} = 1 kΩ, T_{MIN}–T_{MAX}	±15 V	0.15	0.01		mV/V
Common-Mode Rejection Ratio Match	V_{CM} = ±12 V, T_{MIN}–T_{MAX}	±15 V	80	100		dB
Power Supply Rejection Ratio Match	±5 V to ±15 V, T_{MIN}–T_{MAX}		80	100		dB
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current/Amplifier		±5 V		6.6	7.5	mA
	T_{MIN} to T_{MAX}	±5 V			7.5	mA
		±15 V			7.5	mA
	T_{MIN} to T_{MAX}	±15 V		6.8	7.5	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V, T_{MIN} to T_{MAX}		75	86		dB

NOTES

[1]Full power bandwidth = slew rate/2 π V_{PEAK}.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2]
  Plastic (N) . . . . See Derating Curves
  Small Outline (R) . . . . See Derating Curves
Input Voltage (Common Mode) . . . . ±V_S
Differential Input Voltage . . . . ±6 V
Output Short Circuit Duration . . . . See Derating Curves
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Operating Temperature Range . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 seconds) . . . +300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability .

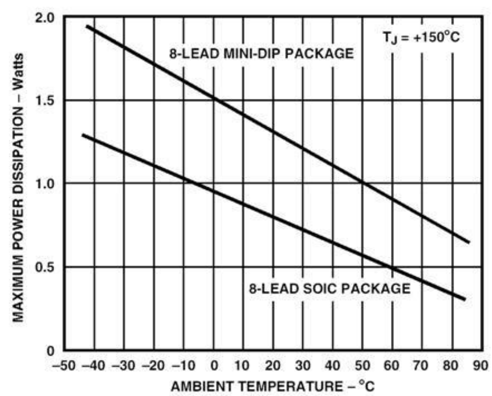
[2]Specification is for device in free air: 8-lead plastic package, θ_{JA} = 100°C/watt; 8-lead SOIC package, θ_{JA} = 155°C/watt.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD826AN	–40°C to +85°C	8-Lead Plastic DIP	N-8
AD826AR	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD826AR-REEL7	–40°C to +85°C	7" Tape & Reel SOIC	SO-8
AD826AR-REEL	–40°C to +85°C	13" Tape & Reel SOIC	SO-8

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD826 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.



Maximum Power Dissipation vs. Temperature for Different Package Types

AD826 – Typical Characteristics

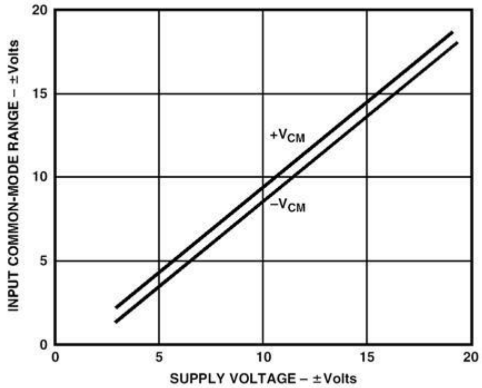


Figure 1. Common-Mode Voltage Range vs. Supply

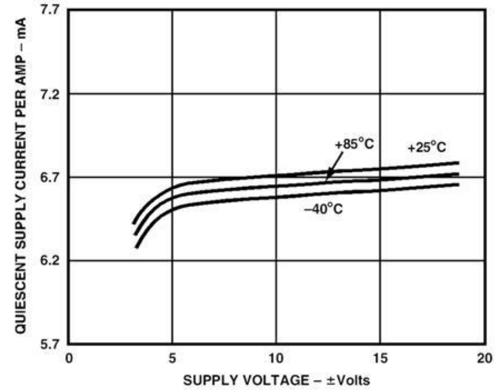


Figure 4. Quiescent Supply Current per Amp vs. Supply Voltage for Various Temperatures

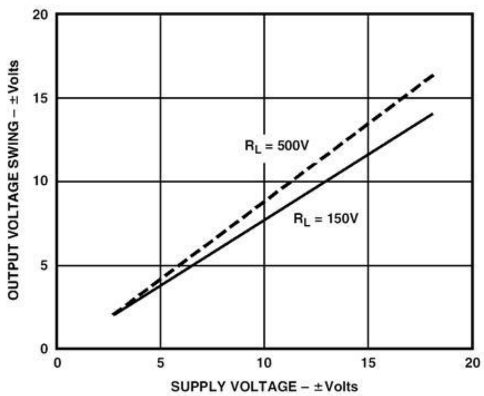


Figure 2. Output Voltage Swing vs. Supply

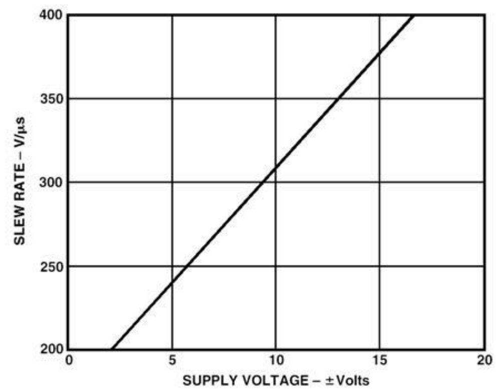


Figure 5. Slew Rate vs. Supply Voltage

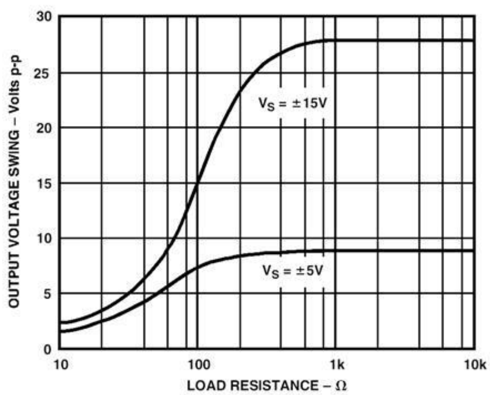


Figure 3. Output Voltage Swing vs. Load Resistance

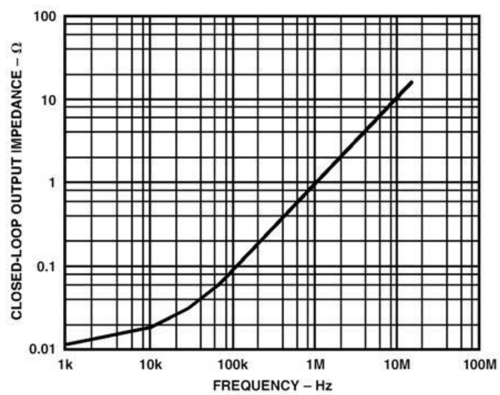


Figure 6. Closed-Loop Output Impedance vs. Frequency

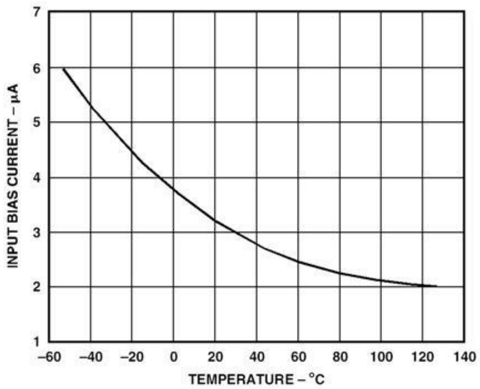


Figure 7. Input Bias Current vs. Temperature

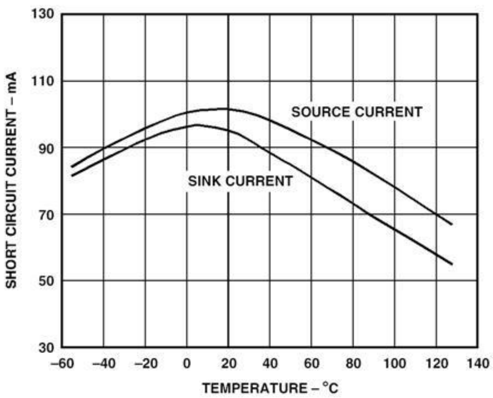


Figure 8. Short Circuit Current vs. Temperature

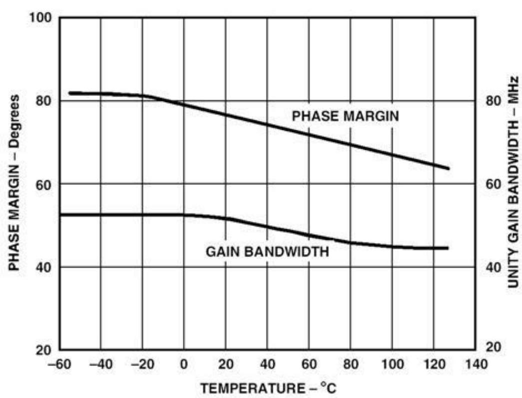


Figure 9. Unity Gain Bandwidth and Phase Margin vs. Temperature

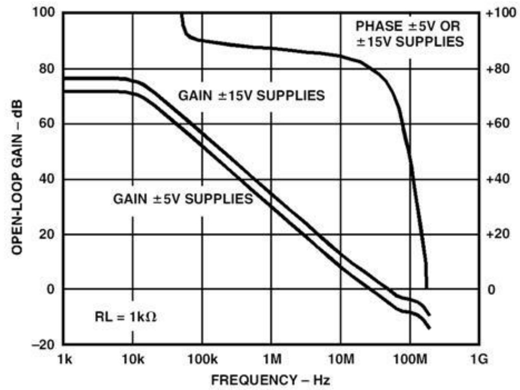


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

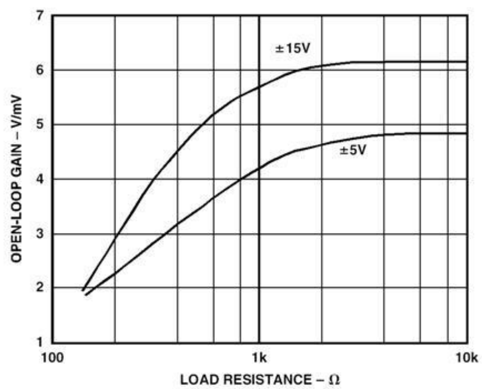


Figure 11. Open-Loop Gain vs. Load Resistance

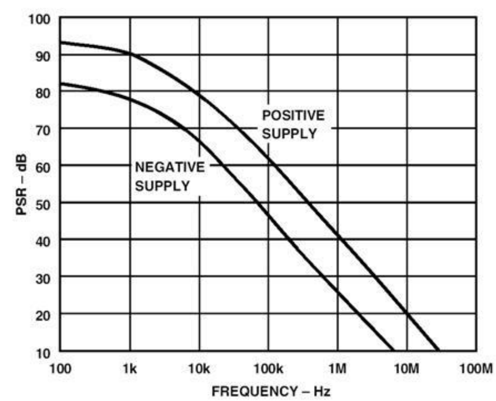


Figure 12. Power Supply Rejection vs. Frequency

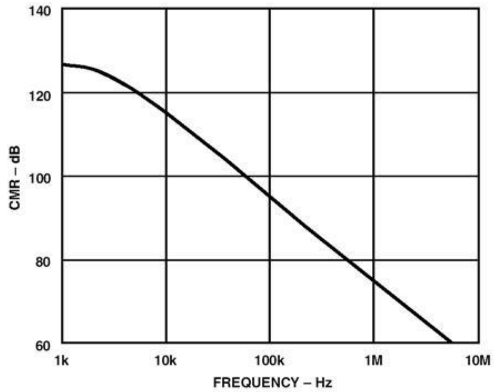


Figure 13. Common-Mode Rejection vs. Frequency

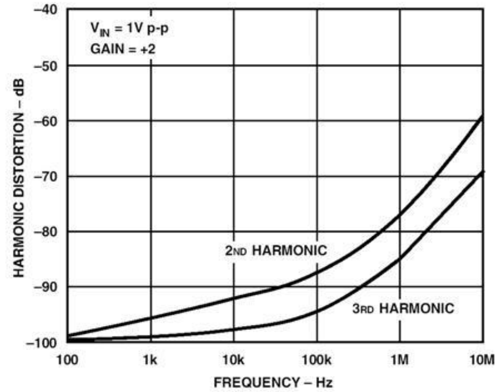


Figure 16. Harmonic Distortion vs. Frequency

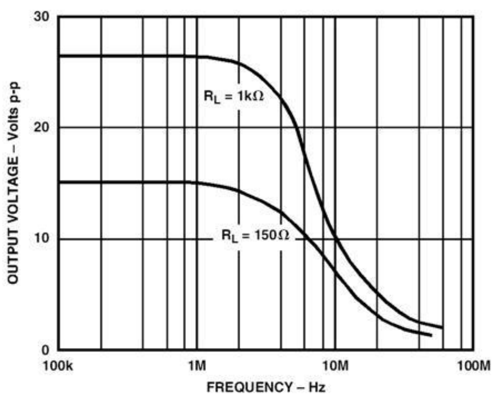


Figure 14. Large Signal Frequency Response

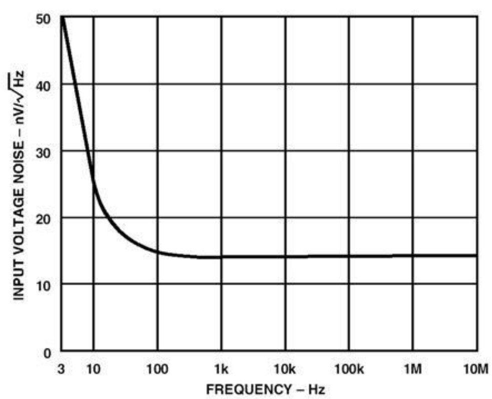


Figure 17. Input Voltage Noise Spectral Density

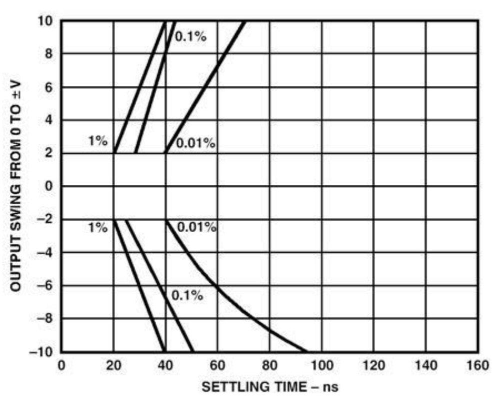


Figure 15. Output Swing and Error vs. Settling Time

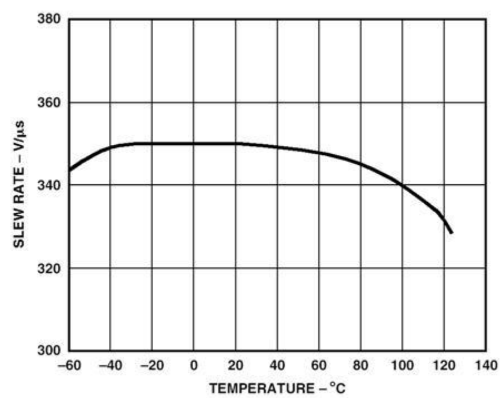


Figure 18. Slew Rate vs. Temperature

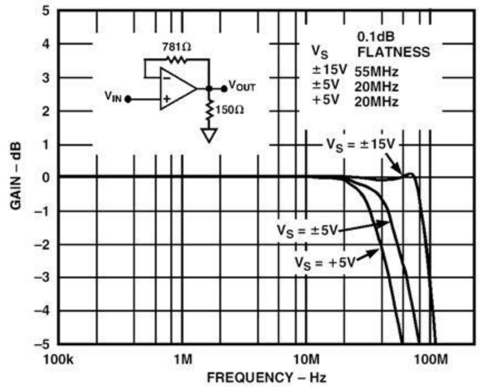


Figure 19. Closed-Loop Gain vs. Frequency

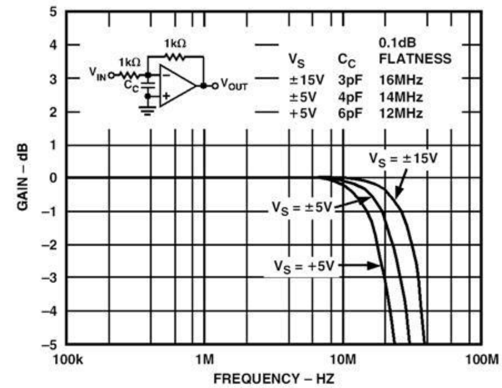


Figure 22. Closed-Loop Gain vs. Frequency, Gain = –1

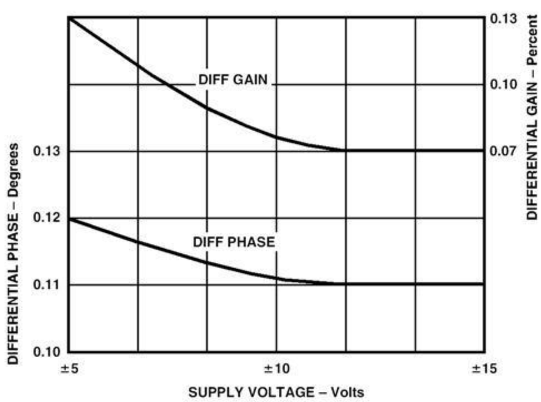


Figure 20. Differential Gain and Phase vs. Supply Voltage

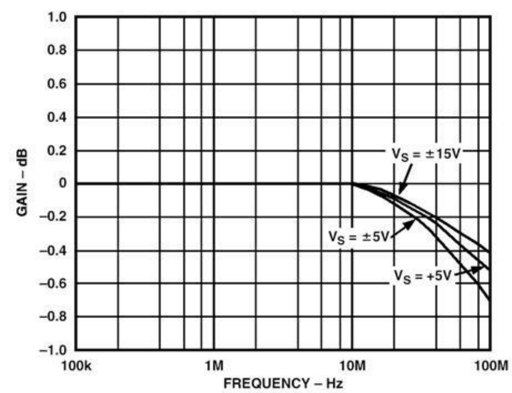


Figure 23. Gain Flatness Matching vs. Supply, G = +1

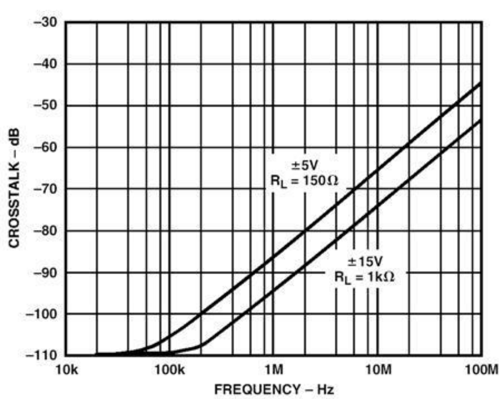


Figure 21. Crosstalk vs. Frequency

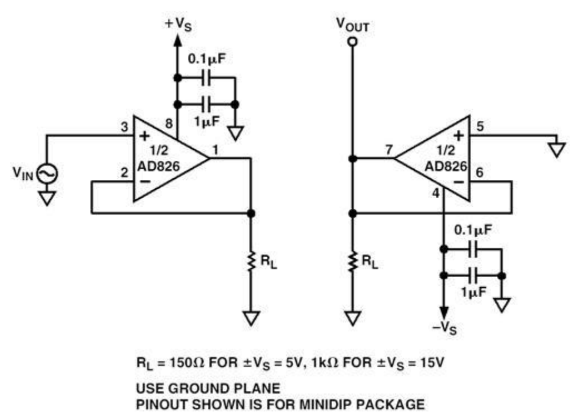


Figure 24. Crosstalk Test Circuit

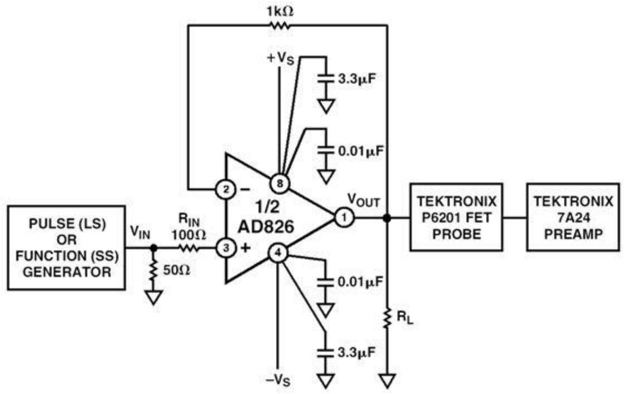


Figure 25. Noninverting Amplifier Configuration

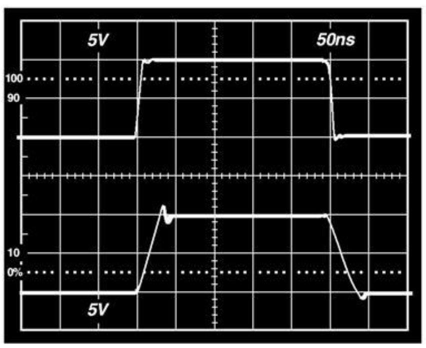


Figure 26. Noninverting Large Signal Pulse Response, $R_L = 1\ k\Omega$

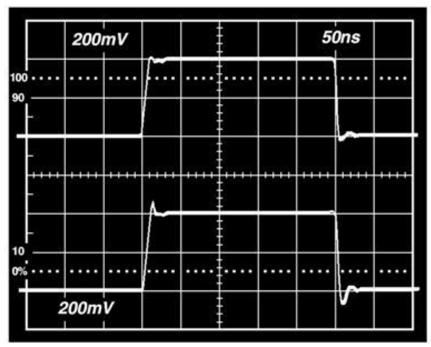


Figure 28. Noninverting Small Signal Pulse Response, $R_L = 1\ k\Omega$

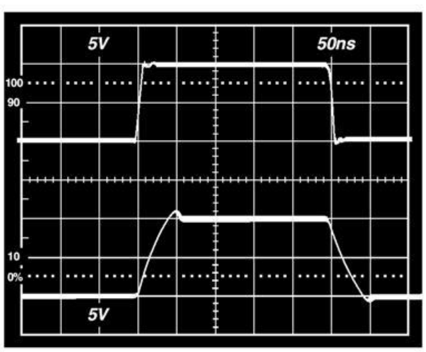


Figure 27. Noninverting Large Signal Pulse Response, $R_L = 150\ \Omega$

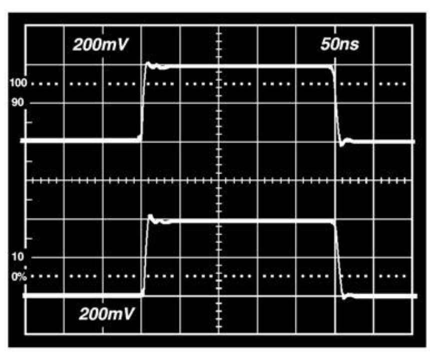


Figure 29. Noninverting Small Signal Pulse Response, $R_L = 150\ \Omega$

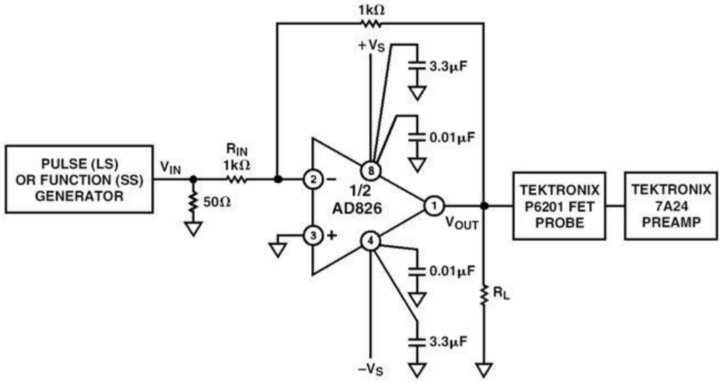


Figure 30. Inverting Amplifier Configuration

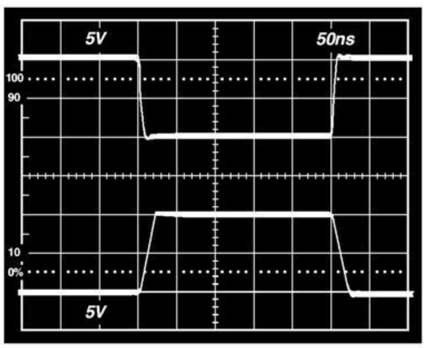


Figure 31. Inverting Large Signal Pulse Response, R_L = 1 kΩ

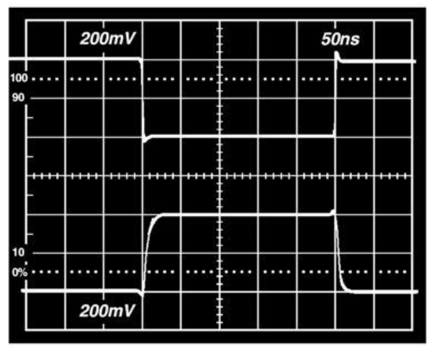


Figure 33. Inverting Small Signal Pulse Response, R_L = 1 kΩ

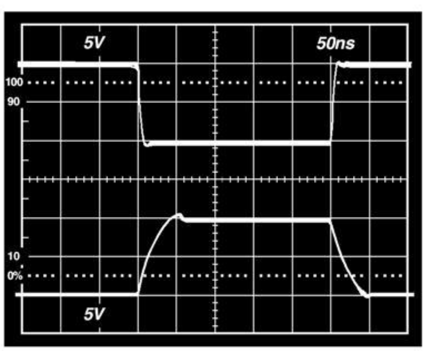


Figure 32. Inverting Large Signal Pulse Response, R_L = 150 Ω

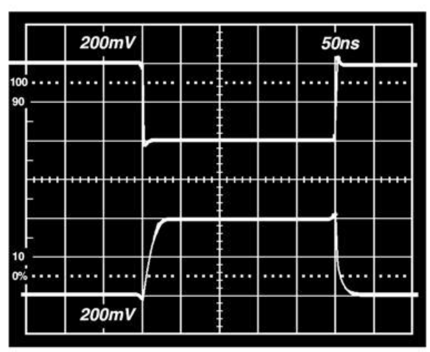


Figure 34. Inverting Small Signal Pulse Response, R_L = 150 Ω

THEORY OF OPERATION

The AD826 is a low cost, wide band, high performance dual operational amplifier which can drive heavy capacitive and resistive loads. It also achieves a constant slew rate, bandwidth and settling time over its entire specified temperature range.

The AD826 (Figure 35) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load while maintaining low levels of distortion.

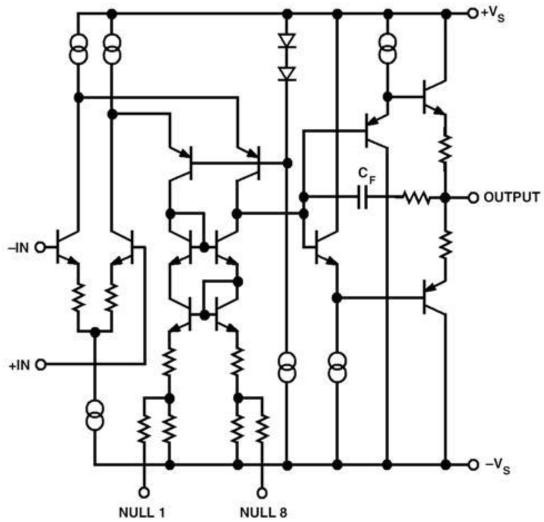


Figure 35. Simplified Schematic

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. With low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C_F is bootstrapped and does not contribute to the overall compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Effectively, some fraction of C_F contributes to the overall compensation capacitance, reducing the unity gain bandwidth. As the load capacitance is further increased, the bandwidth continues to fall, maintaining the stability of the amplifier.

INPUT CONSIDERATIONS

An input protection resistor (R_{IN} in Figure 25) is required in circuits where the input to the AD826 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a "balancing" resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of R_{IN} and R_F and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

APPLYING THE AD826

The AD826 is a breakthrough dual amp that delivers precision and speed at low cost with low power consumption. The AD826 offers excellent static and dynamic matching characteristics, combined with the ability to drive heavy resistive and capacitive loads.

As with all high frequency circuits, care should be taken to maintain overall device performance as well as their matching. The following items are presented as general design considerations.

Circuit Board Layout

Input and output runs should be laid out so as to physically isolate them from remaining runs. In addition, the feedback resistor of each amplifier should be placed away from the feedback resistor of the other amplifier, since this greatly reduces inter-amp coupling.

Choosing Feedback and Gain Resistors

In order to prevent the stray capacitance present at each amplifier's summing junction from limiting its performance, the feedback resistors should be ≤ 1 kΩ. Since the summing junction capacitance may cause peaking, a small capacitor (1 pF–5 pF) may be paralleled with R_F to neutralize this effect. Finally, sockets should be avoided, because of their tendency to increase interlead capacitance.

Power Supply Bypassing

Proper power supply decoupling is critical to preserve the integrity of high frequency signals. In carefully laid out designs, decoupling capacitors should be placed in close proximity to the supply pins, while their lead lengths should be kept to a minimum. These measures greatly reduce undesired inductive effects on the amplifier's response.

Though two 0.1 µF capacitors will typically be effective in decoupling the supplies, several capacitors of different values can be paralleled to cover a wider frequency range.

±SINGLE SUPPLY OPERATION

An exciting feature of the AD826 is its ability to perform well in a single supply configuration (see Figure 37). The AD826 is ideally suited for applications that require low power dissipation and high output current and those which need to drive large capacitive loads, such as high speed buffering and instrumentation.

Referring to Figure 36, careful consideration should be given to the proper selection of component values. The choices for this particular circuit are: (R1 + R3)||R2 combine with C1 to form a low frequency corner of approximately 30 Hz.

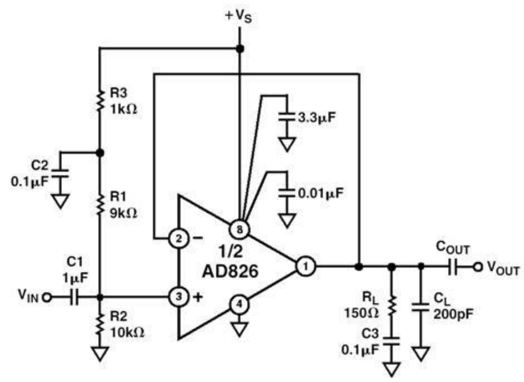


Figure 36. Single Supply Amplifier Configuration

R3 and C2 reduce the effect of the power supply changes on the output by low-pass filtering with a corner at $\frac{1}{2\pi R_3 C_2}$.

The values for R_L and C_L were chosen to demonstrate the AD826's exceptional output drive capability. In this configuration, the output is centered around 2.5 V. In order to eliminate the static dc current associated with this level, C3 was inserted in series with R_L.

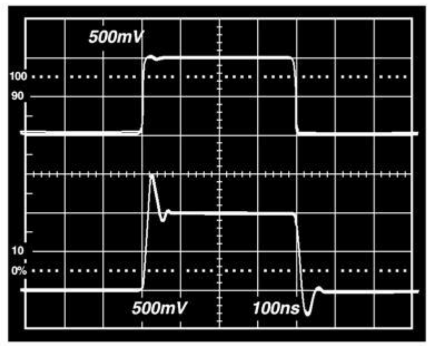


Figure 37. Single Supply Pulse Response, G = +1, R_L = 150 Ω, C_L = 200 pF

PARALLEL AMPS PROVIDE 100 mA TO LOAD

By taking advantage of the superior matching characteristics of the AD826, enhanced performance can easily be achieved by employing the circuit in Figure 38. Here, two identical cells are paralleled to obtain even higher load driving capability than that of a single amplifier (100 mA min guaranteed). R1 and R2 are included to limit current flow between amplifier outputs that would arise in the presence of any residual mismatch.

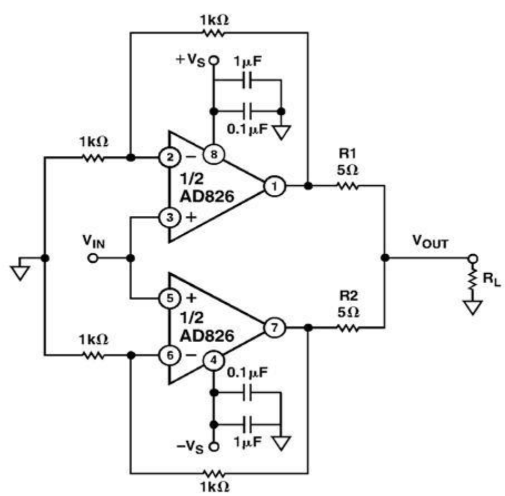


Figure 38. Parallel Amp Configuration

SINGLE-ENDED TO DIFFERENTIAL LINE DRIVER

Outstanding CMRR (> 80 dB @ 5 MHz), high bandwidth, wide supply voltage range, and the ability to drive heavy loads, make the AD826 an ideal choice for many line driving applications. In this application, the AD830 high speed video difference amp serves as the differential line receiver on the end of a back terminated, 50 ft., twisted-pair transmission line (see Figure 40). The overall system is configured in a gain of +1 and has a –3 dB bandwidth of 14 MHz. Figure 39 is the pulse response with a 2 V p-p, 1 MHz signal input.

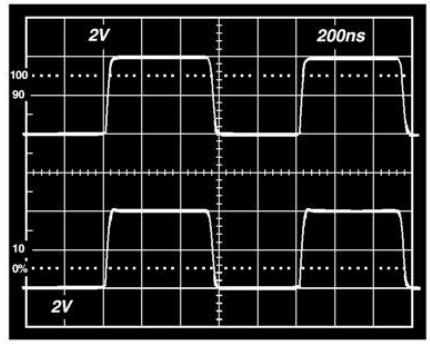


Figure 39. Pulse Response

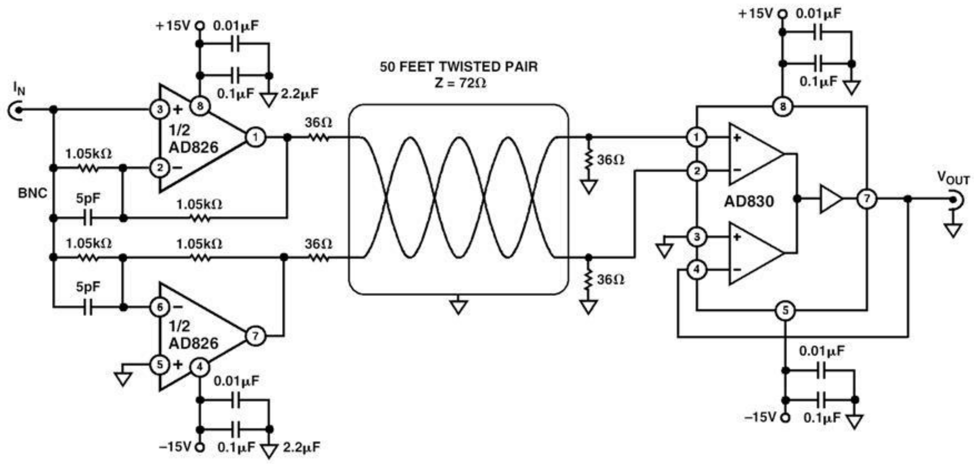


Figure 40. Differential Line Driver

LOW DISTORTION LINE DRIVER

The AD826 can quickly be turned into a powerful, low distortion line driver (see Figure 41). In this arrangement the AD826 can comfortably drive a 75 Ω back-terminated cable, with a 5 MHz, 2 V p-p input; all of this while achieving the harmonic distortion performance outlined in the following table.

Configuration	2nd Harmonic
1. No Load	–78.5 dBm
2. 150 Ω R_L Only	–63.8 dBm
3. 150 Ω R_L 7.5 Ω R_C	–70.4 dBm

In this application one half of the AD826 operates at a gain of 2.1 and supplies the current to the load, while the other provides the overall system gain of 2. This is important for two reasons: the first is to keep the bandwidth of both amplifiers the same, and the second is to preserve the AD826's ability to operate from low supply voltages. R_C varies with the load and must be chosen to satisfy the following equation:

$$R_C = MR_L$$

where M is defined by [(M+ 1) $G_S = G_D$] and G_D = Driver's Gain, G_S = System Gain.

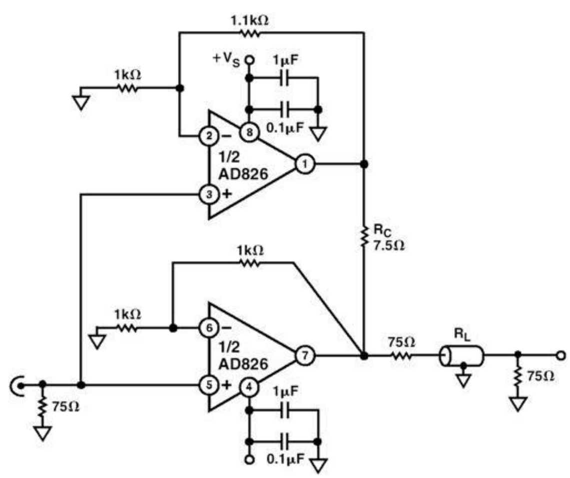


Figure 41. Low Distortion Amplifier

HIGH PERFORMANCE ADC BUFFER

Figure 42 is a schematic of a 12-bit high speed analog-to-digital converter. The AD826 dual op amp takes a single ended input and drives the AD872 A/D converter differentially, thus reducing 2nd harmonic distortion. Figure 43 is a FFT of a 1 MHz input, sampled at 10 MHz with a THD of –78 dB. The AD826 can be used to amplify low level signals so that the entire range of the converter is used. The ability of the AD826 to perform on a ±5 volt supply or even with a single 5 volts combined with its rapid settling time and ability to deliver high current to complicated loads make it a very good flash A/D converter buffer as well as a very useful general purpose building block.

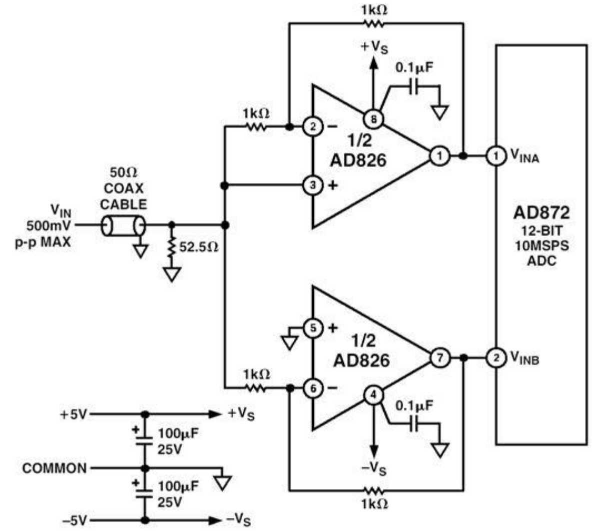


Figure 42. A Differential Input Buffer for High Bandwidth ADCs

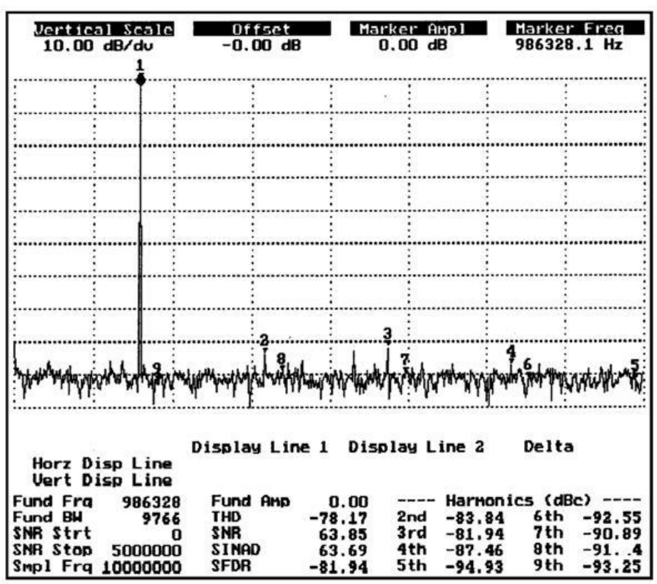
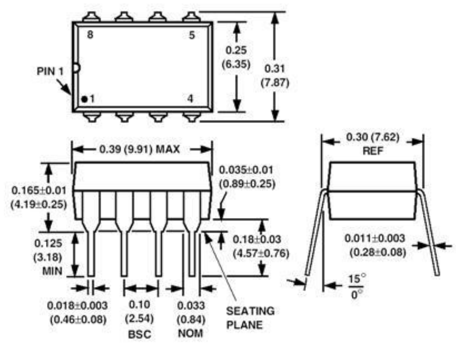


Figure 43. FFT, Buffered A/D Converter

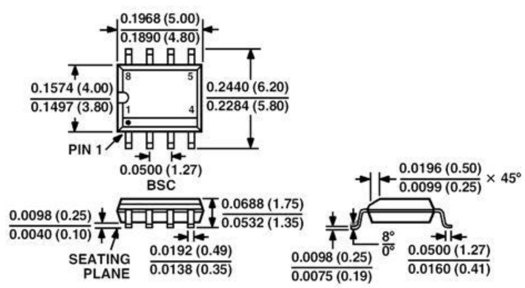
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic Mini-DIP (N) Package



8-Lead SO (R) Package



All brand or product names mentioned are trademarks or registered trademarks of their respective holders.

C1807a–0–6/00 (rev. B) 00877

PRINTED IN U.S.A.

Data sheet acquired from Harris Semiconductor
SCHS021D – Revised September 2003

CMOS NAND GATES

High-Voltage Types (20-Volt Rating)

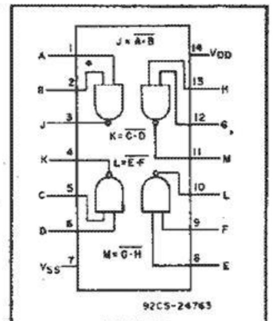
Quad 2 Input – CD4011B
Dual 4 Input – CD4012B
Triple 3 Input – CD4023B

■ CD4011B, CD4012B, and CD4023B NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

The CD4011B, CD4012B, and CD4023B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PWR suffix). The CD4011B and CD4023B types also are supplied in 14-lead thin shrink small-outline packages (PW suffix).

Features:

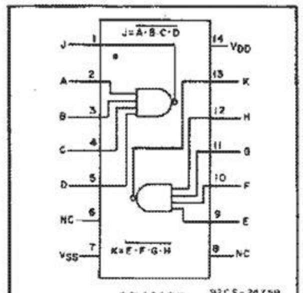
- Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package temperature range:
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"



CD4011B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

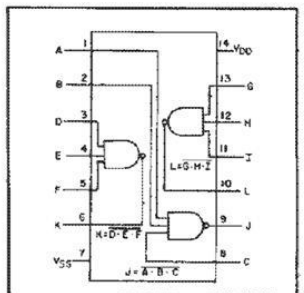


CD4012B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

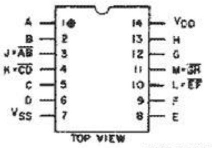
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

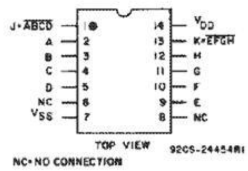


CD4023B
FUNCTIONAL DIAGRAM

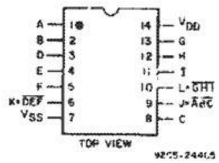
TERMINAL ASSIGNMENTS



CD4011B



CD4012B



CD4023B

Copyright © 2003, Texas Instruments Incorporated

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	μA
	–	0,15	15	1	1	30	30	–	0.01	1	μA
	–	0,20	20	5	5	150	150	–	0.02	5	μA
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	mA
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	mA
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	mA
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	mA
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	mA
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	V
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Input Low Voltage, V_{IL} Max.	4.5	–	5	1.5				–	–	1.5	V
	9	–	10	3				–	–	3	V
	13.5	–	15	4				–	–	4	V
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	V
	1,9	–	10	7				7	–	–	V
	1.5,13.5	–	15	11				11	–	–	V
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

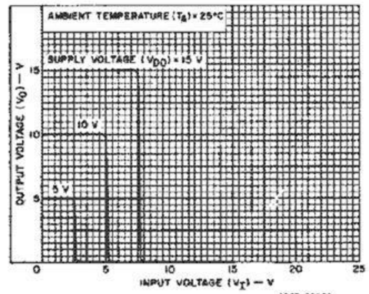


Fig. 1 — Typical voltage transfer characteristics.

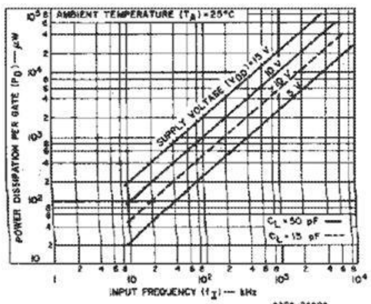


Fig. 2 — Typical power dissipation characteristics.

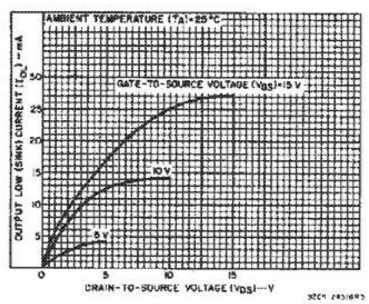


Fig. 3 — Typical output low (sink) current characteristics.

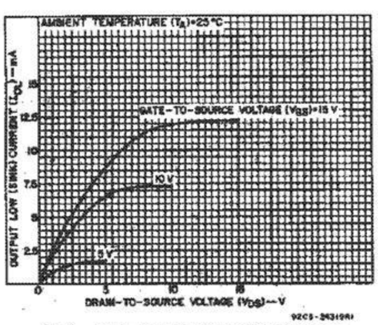


Fig. 4 — Minimum output low (sink) current characteristics.

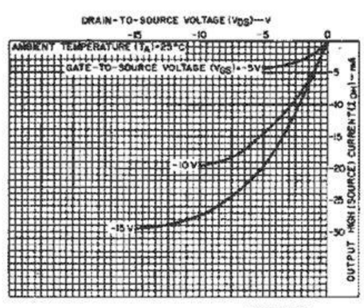


Fig. 5 — Typical output high (source) current characteristics.

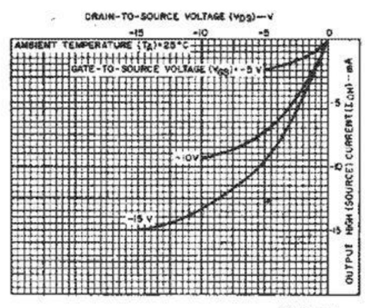


Fig. 6 — Minimum output high (source) current characteristics.

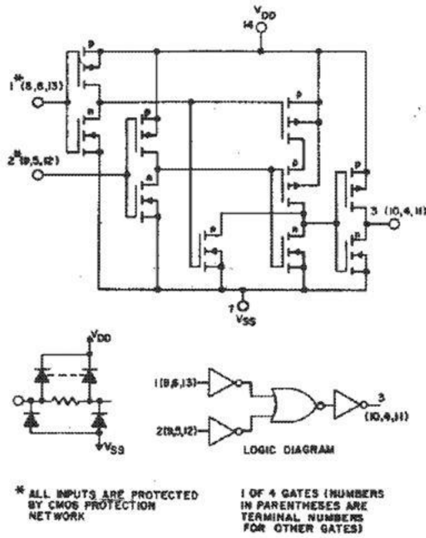


Fig.7 – Schematic and logic diagrams for CD4011B.

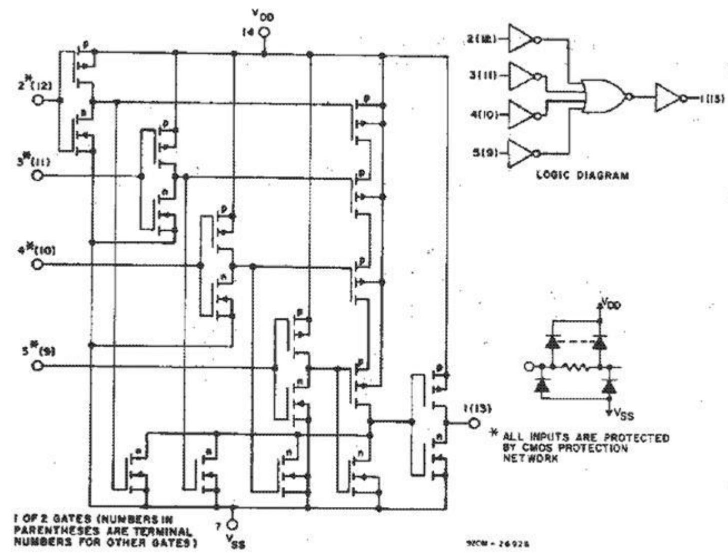


Fig.8 – Schematic and logic diagrams for CD4012B.

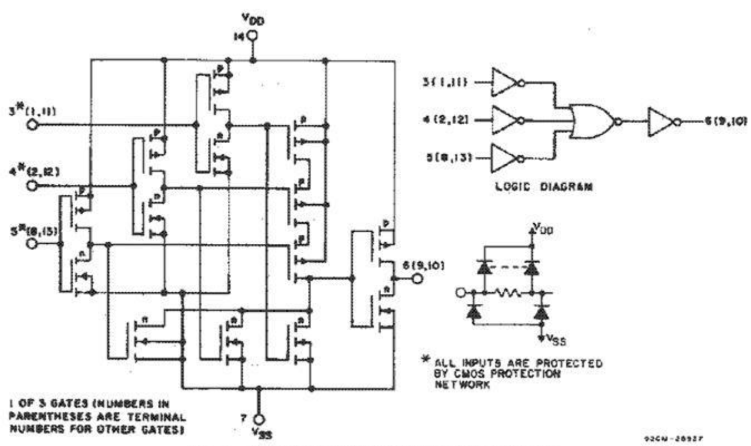


Fig. 9 – Schematic and logic diagrams for CD4023B.

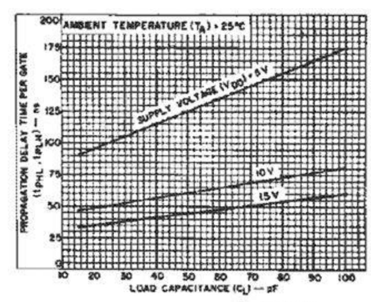


Fig.10 – Typical propagation delay time per gate as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200k\Omega$

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5 10 15	125 60 45	250 120 90	ns
Transition Time, t_{THL}, t_{TLH}		5 10 15	100 50 40	200 100 80	ns
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

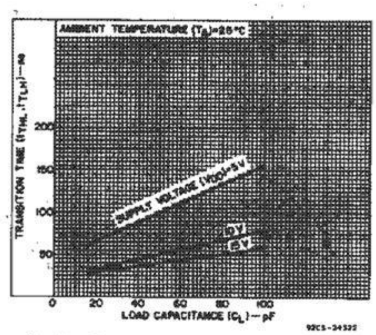


Fig.11 – Typical transition time as a function of load capacitance.

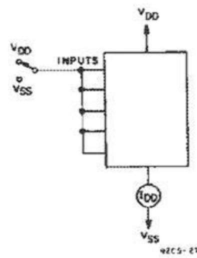


Fig. 12 – Quiescent-device-current test circuit.

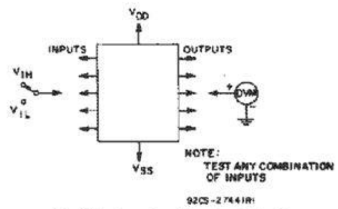


Fig. 13 – Input-voltage test circuit.

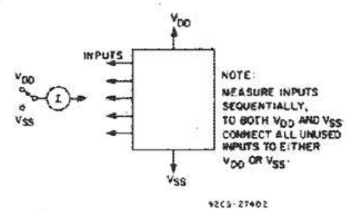
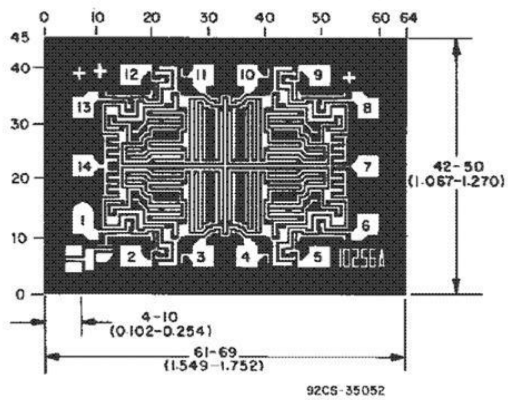
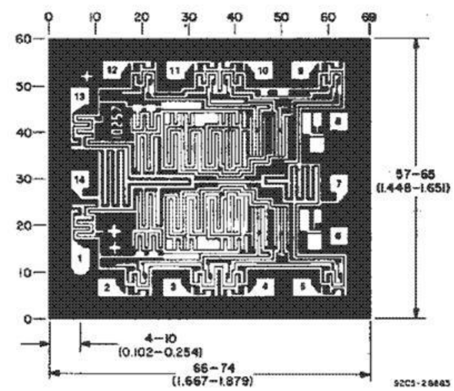


Fig. 14 – Input-current test circuit.

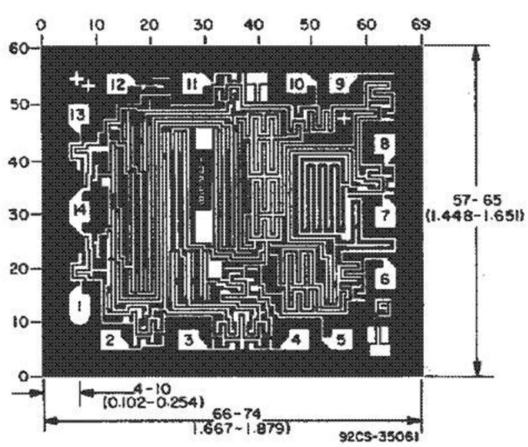
Chip Dimensions and Pad Layouts



CD4011BH



CD4012BH



CD4023BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
89265AKB3T	OBSOLETE	CFP	WR	14		TBD	Call TI	Call TI
89266AKB3T	OBSOLETE	CFP	WR	16		TBD	Call TI	Call TI
89273AKB3T	OBSOLETE	CFP	WR	14		TBD	Call TI	Call TI
CD4011BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4011BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4011BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4011BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4011BK3	OBSOLETE	CFP	WR	14		TBD	Call TI	Call TI
CD4011BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD4012BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4012BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4012BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4023BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4023BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4023BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4023BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD4023BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
JM38510/05051BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/05052BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/05053BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

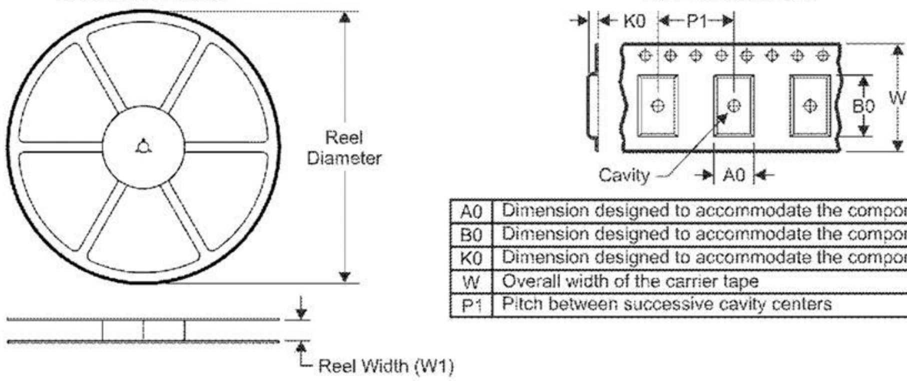
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

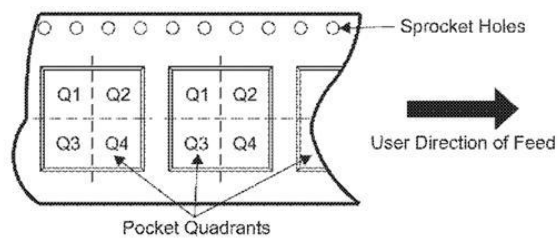
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

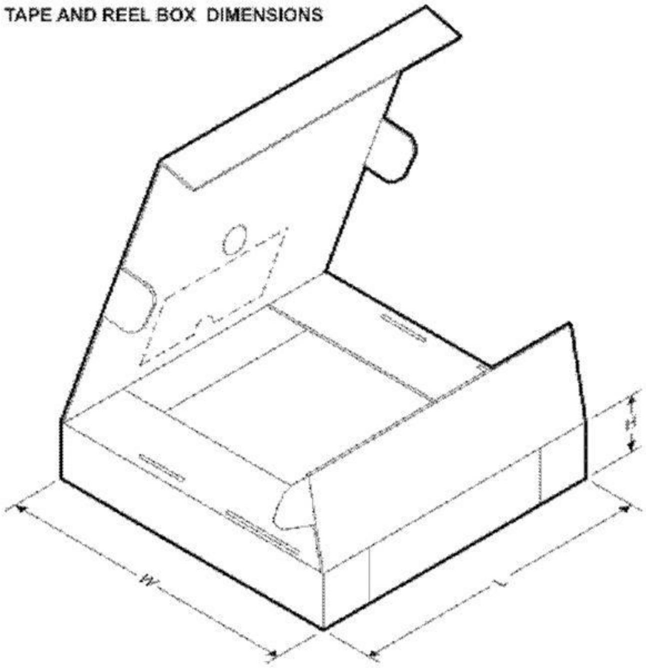
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4011BM96	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
CD4011BNSR	SO	NS	14	2000	330.0	16.0	8.0	11.0	3.0	12.0	16.0	Q1
CD4011BPWR	TSSOP	PW	14	2000	330.0	12.0	7.0	6.0	2.0	8.0	12.0	Q1
CD4012BM96	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
CD4012BNSR	SO	NS	14	2000	330.0	16.0	8.0	11.0	3.0	12.0	16.0	Q1
CD4012BPWR	TSSOP	PW	14	2000	330.0	12.0	7.0	6.0	2.0	8.0	12.0	Q1
CD4023BM96	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
CD4023BNSR	SO	NS	14	2000	330.0	16.0	8.0	11.0	3.0	12.0	16.0	Q1
CD4023BPWR	TSSOP	PW	14	2000	330.0	12.0	7.0	6.0	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



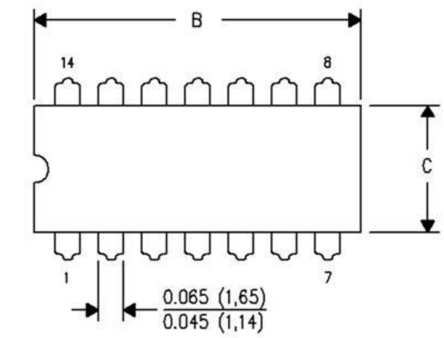
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4011BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4011BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4011BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
CD4012BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4012BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4012BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
CD4023BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4023BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4023BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

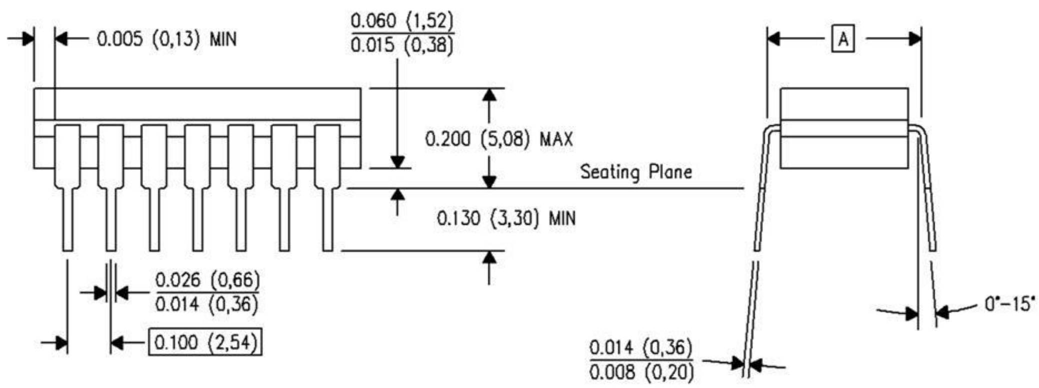
J (R–GDIP–T**)

CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

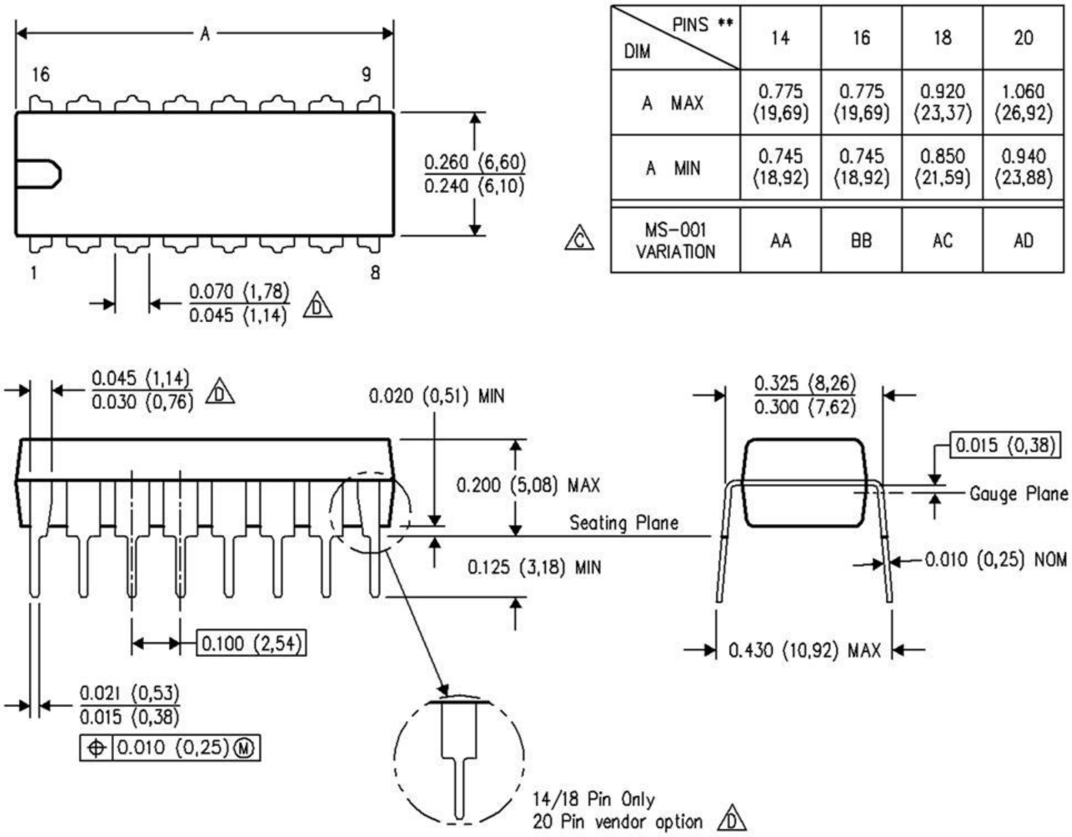


4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

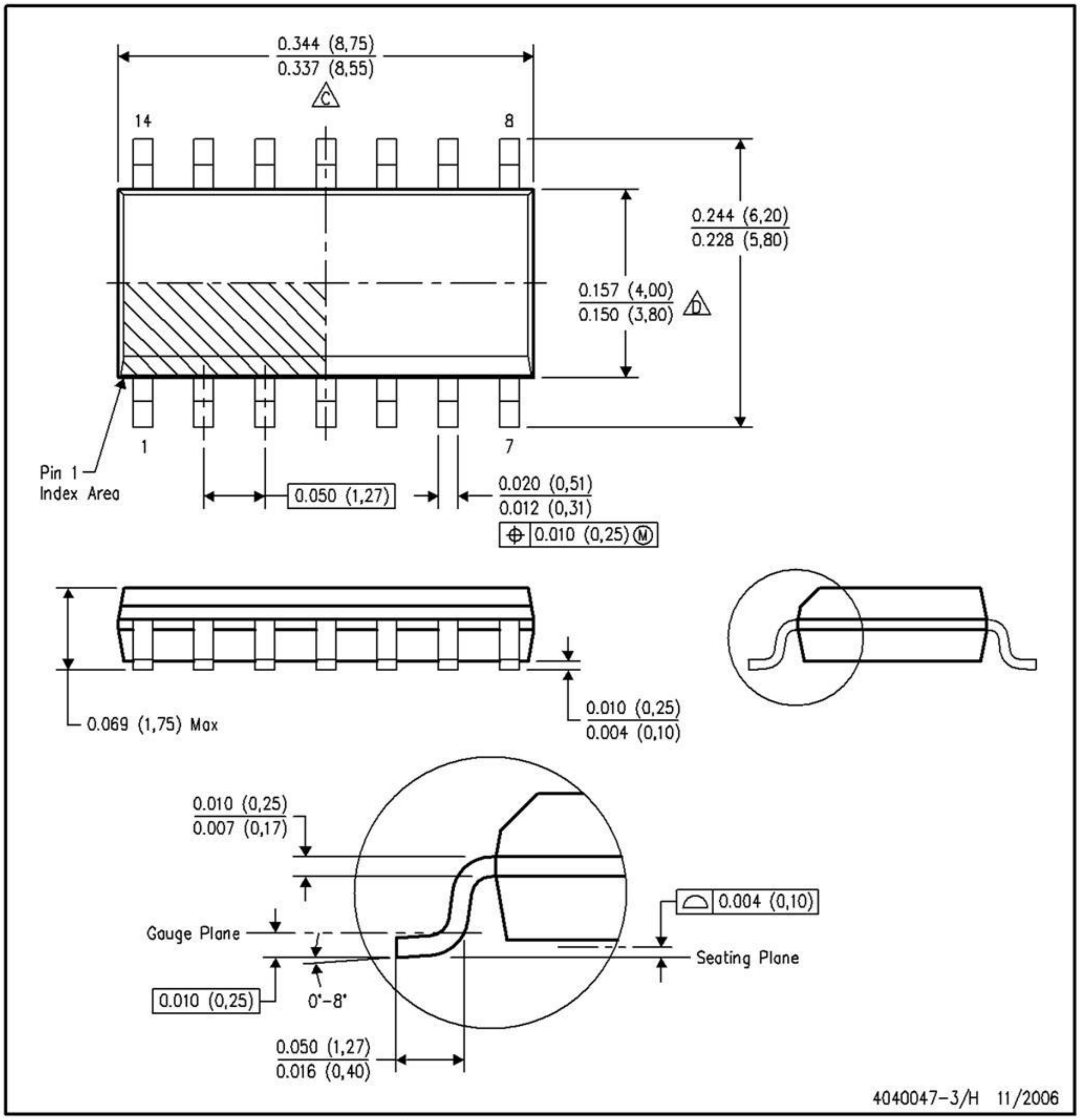


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION (C)	AA	BB	AC	AD

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14) PLASTIC SMALL-OUTLINE PACKAGE

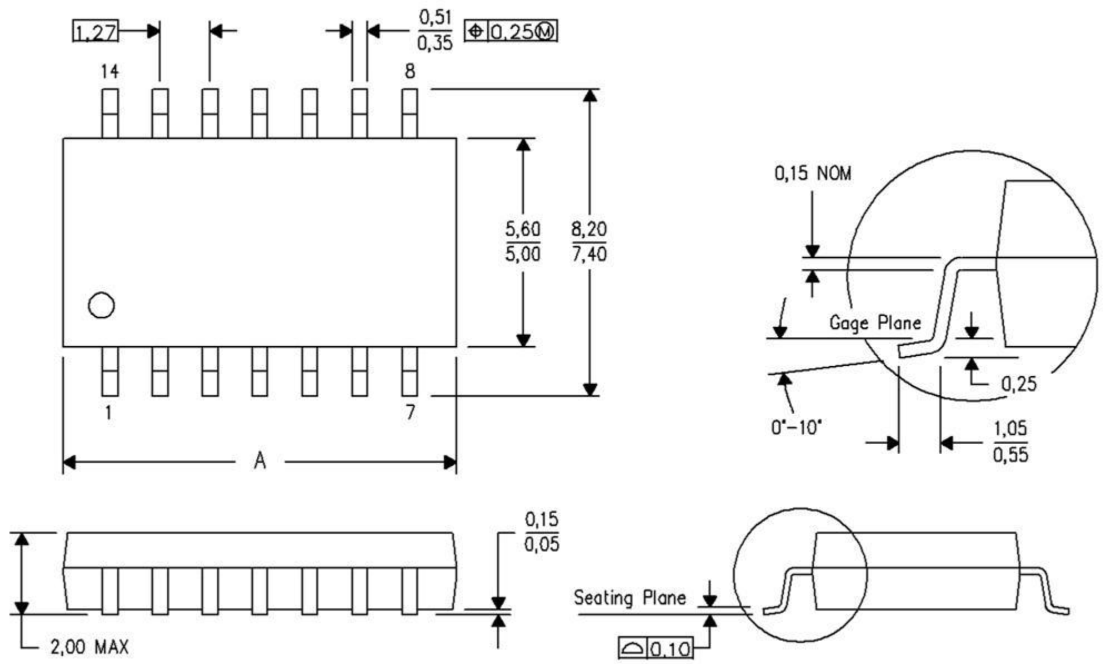


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AB.

TEXAS INSTRUMENTS
www.ti.com

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



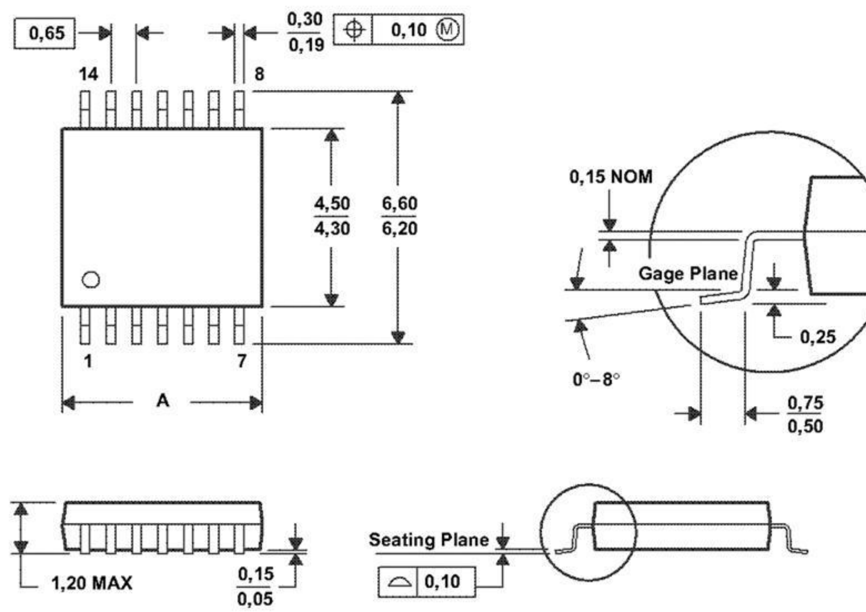
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS021D – Revised September 2003

CD4011B, CD4012B, CD4023B Types

CMOS NAND GATES

High-Voltage Types (20-Volt Rating)

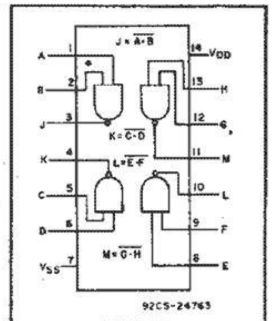
Quad 2 Input – CD4011B
Dual 4 Input – CD4012B
Triple 3 Input – CD4023B

■ CD4011B, CD4012B, and CD4023B NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

The CD4011B, CD4012B, and CD4023B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PWR suffix). The CD4011B and CD4023B types also are supplied in 14-lead thin shrink small-outline packages (PW suffix).

Features:

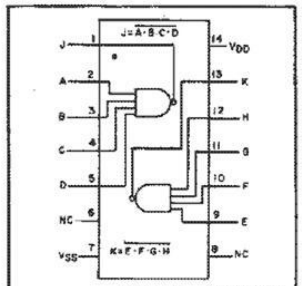
- **Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V**
- **Buffered inputs and outputs**
- **Standardized symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Noise margin (over full package temperature range:**
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"**



CD4011B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

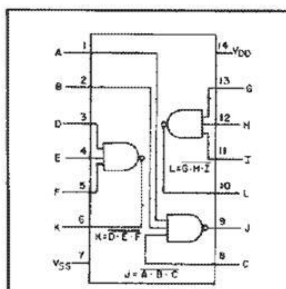


CD4012B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

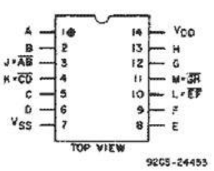
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

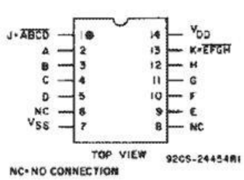


CD4023B
FUNCTIONAL DIAGRAM

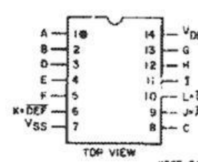
TERMINAL ASSIGNMENTS



CD4011B



CD4012B



CD4023B

Copyright © 2003, Texas Instruments Incorporated

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1.5				–	–	1.5	V
	9	–	10	3				–	–	3	
	13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

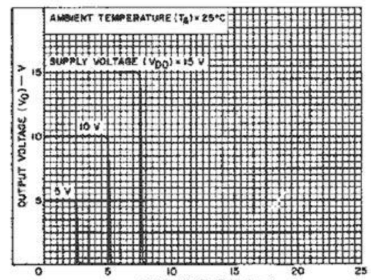


Fig. 1 — Typical voltage transfer characteristics.

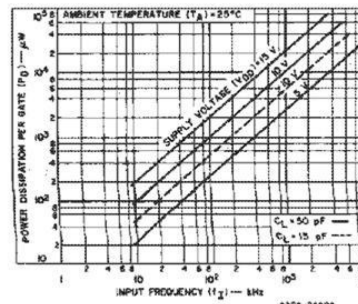


Fig. 2 — Typical power dissipation characteristics.

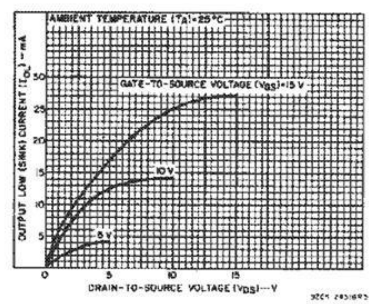


Fig. 3 — Typical output low (sink) current characteristics.

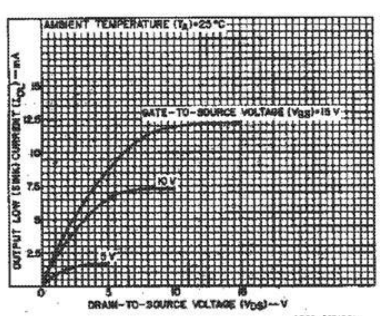


Fig. 4 — Minimum output low (sink) current characteristics.

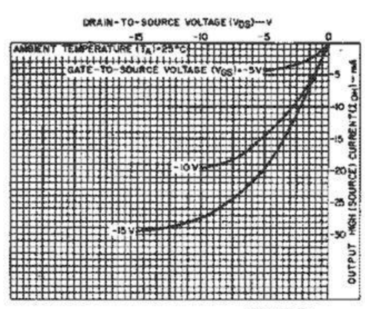


Fig. 5 — Typical output high (source) current characteristics.

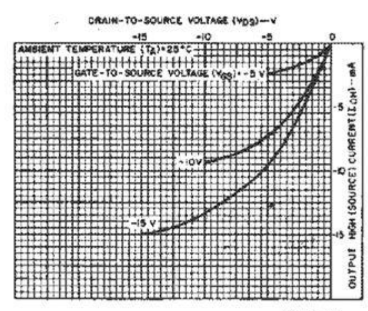


Fig. 6 — Minimum output high (source) current characteristics.

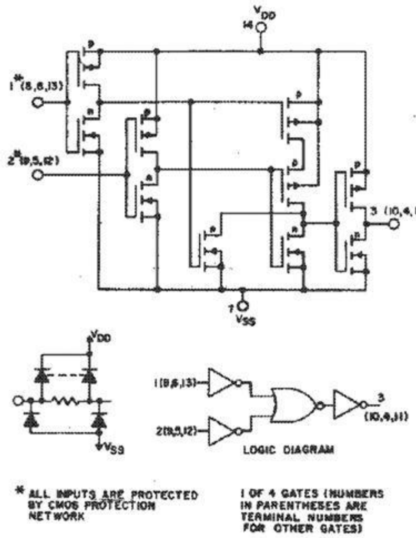


Fig.7 – Schematic and logic diagrams for CD4011B.

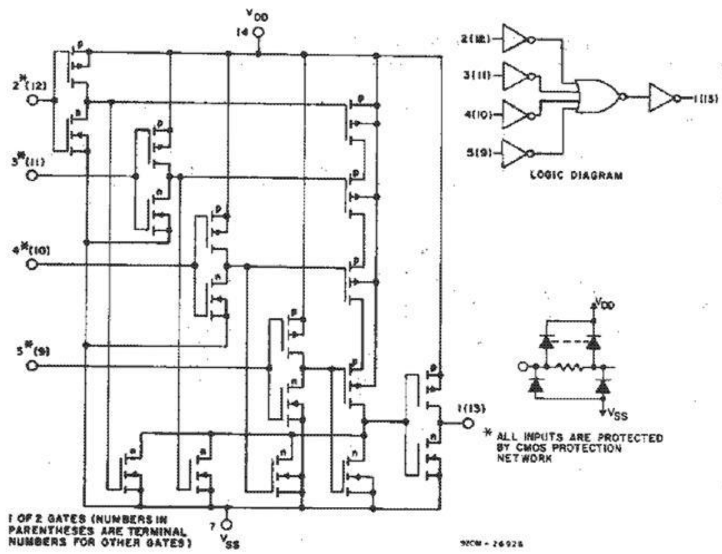


Fig.8 – Schematic and logic diagrams for CD4012B.

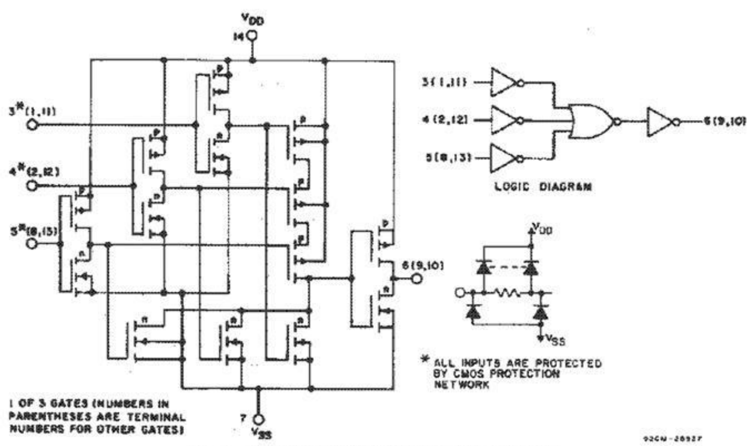


Fig. 9 – Schematic and logic diagrams for CD4023B.

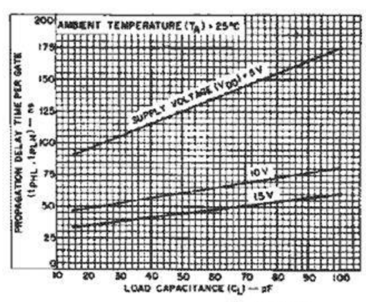


Fig.10 – Typical propagation delay time per gate as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^{\circ}C$; Input t_r, $t_f = 20\ ns$, $C_L = 50\ pF$, $R_L = 200k\Omega$

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

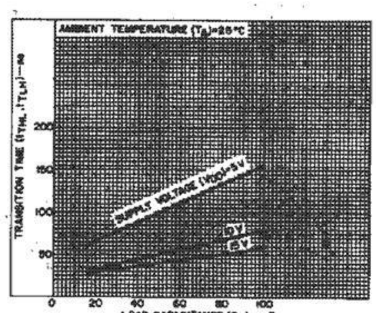


Fig.11 – Typical transition time as a function of load capacitance.

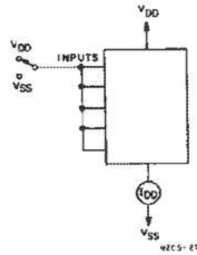


Fig.12 – Quiescent-device-current test circuit.

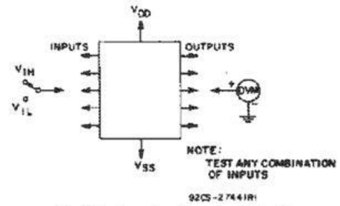


Fig.13 – Input-voltage test circuit.

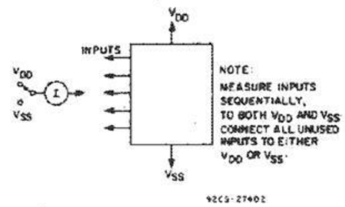
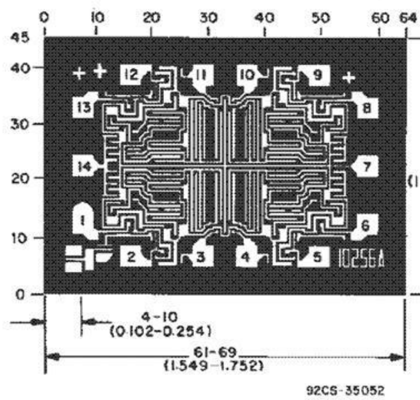
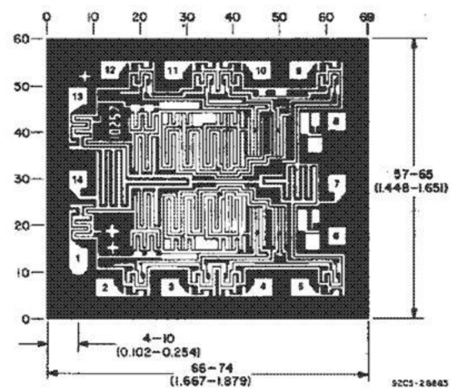


Fig.14 – Input-current test circuit.

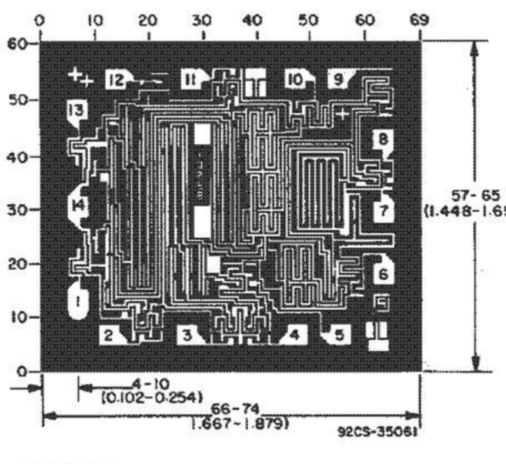
Chip Dimensions and Pad Layouts



CD4011BH



CD4012BH



CD4023BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
89265AKB3T	OBSOLETE	CFP	WR	14		TBD	Call TI	Call TI
89266AKB3T	OBSOLETE	CFP	WR	16		TBD	Call TI	Call TI
89273AKB3T	OBSOLETE	CFP	WR	14		TBD	Call TI	Call TI
CD4011BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4011BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4011BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4011BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4011BK3	OBSOLETE	CFP	WR	14		TBD	Call TI	Call TI
CD4011BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4011BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD4012BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4012BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4012BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4012BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4023BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4023BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4023BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4023BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD4023BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4023BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
JM38510/05051BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/05052BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/05053BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

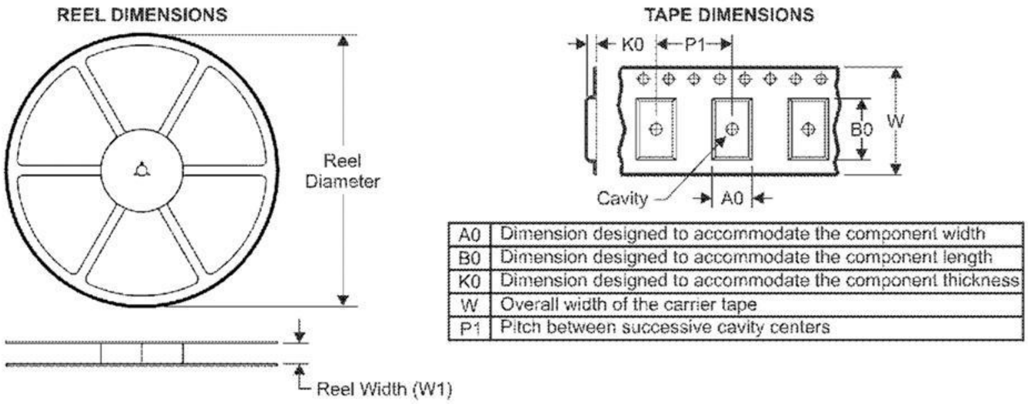
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

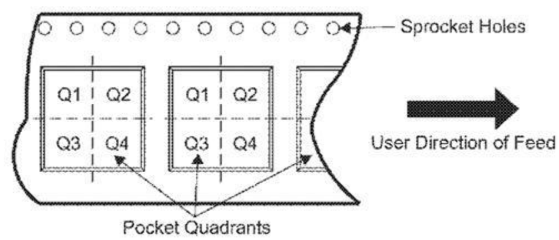
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

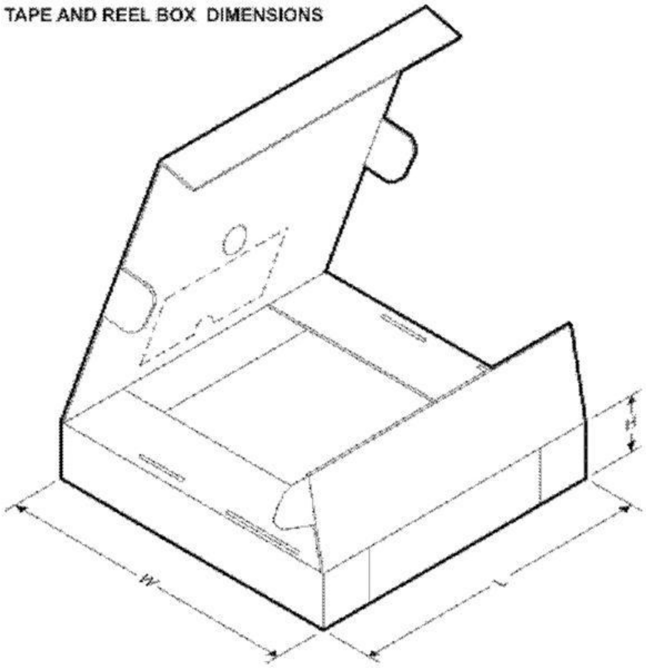
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4011BM96	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
CD4011BNSR	SO	NS	14	2000	330.0	16.0	8.0	11.0	3.0	12.0	16.0	Q1
CD4011BPWR	TSSOP	PW	14	2000	330.0	12.0	7.0	6.0	2.0	8.0	12.0	Q1
CD4012BM96	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
CD4012BNSR	SO	NS	14	2000	330.0	16.0	8.0	11.0	3.0	12.0	16.0	Q1
CD4012BPWR	TSSOP	PW	14	2000	330.0	12.0	7.0	6.0	2.0	8.0	12.0	Q1
CD4023BM96	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
CD4023BNSR	SO	NS	14	2000	330.0	16.0	8.0	11.0	3.0	12.0	16.0	Q1
CD4023BPWR	TSSOP	PW	14	2000	330.0	12.0	7.0	6.0	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

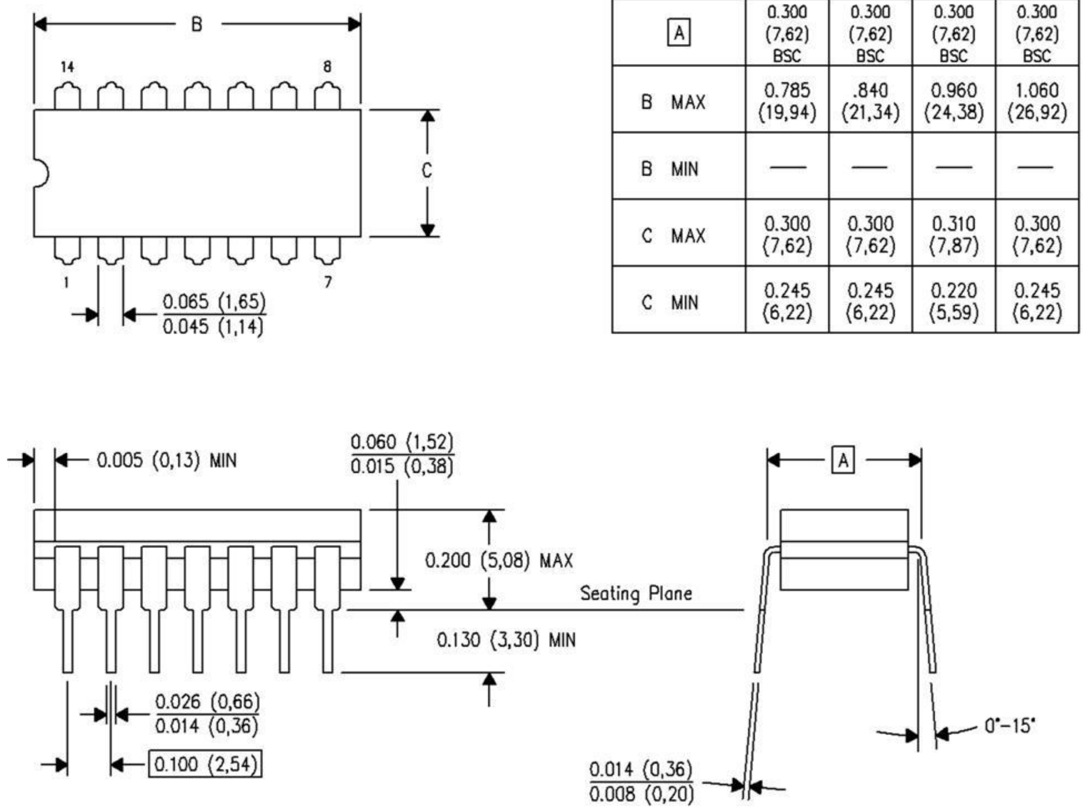


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4011BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4011BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4011BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
CD4012BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4012BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4012BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
CD4023BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4023BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4023BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

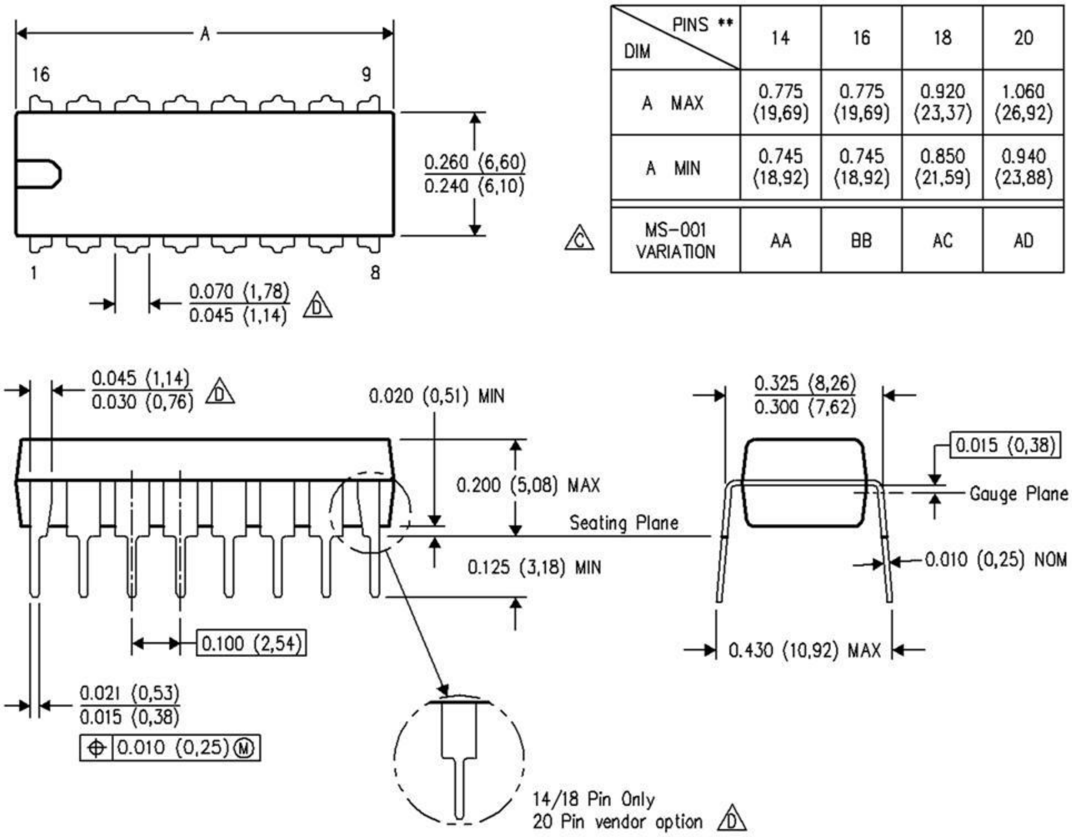
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

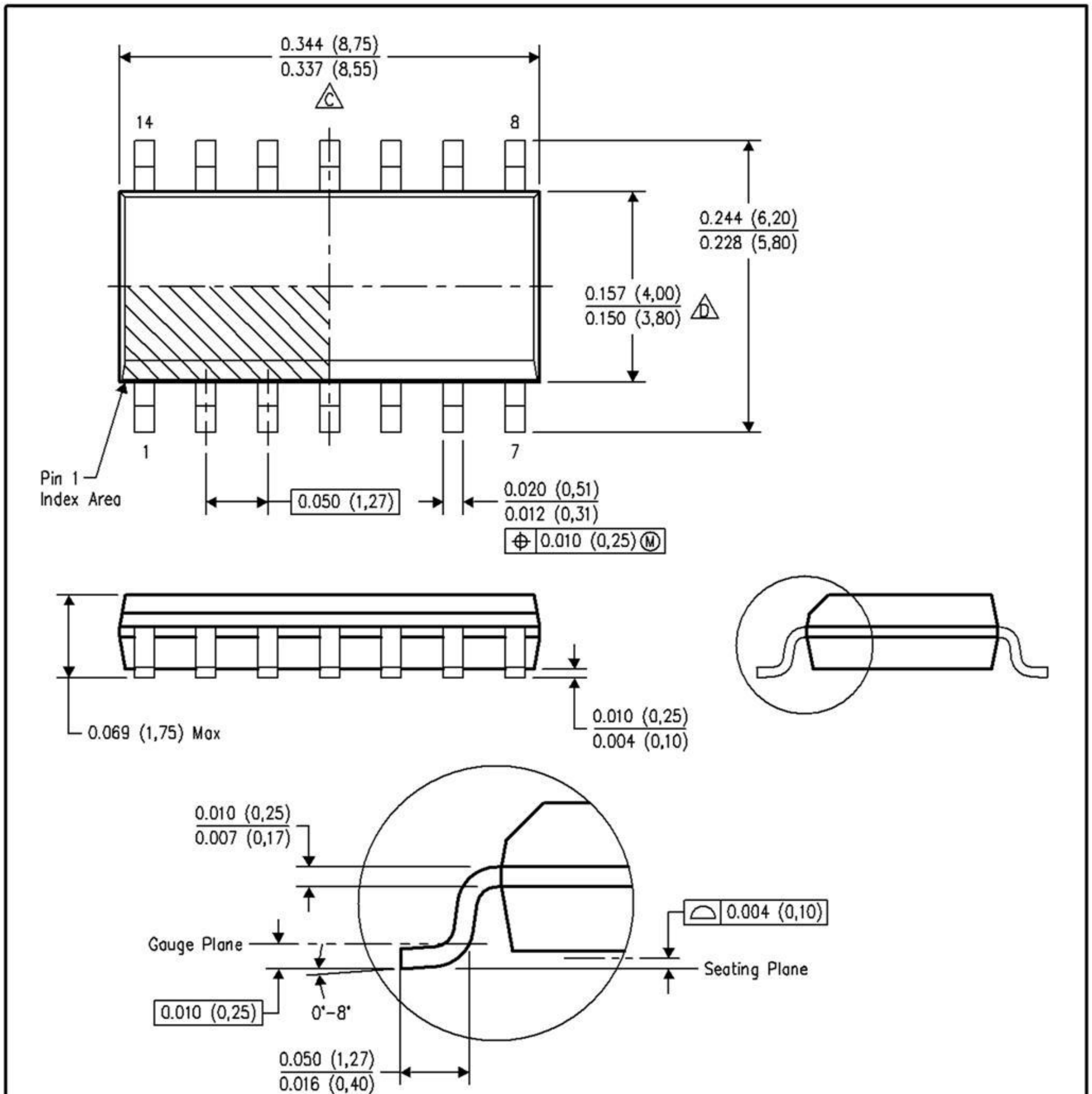
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

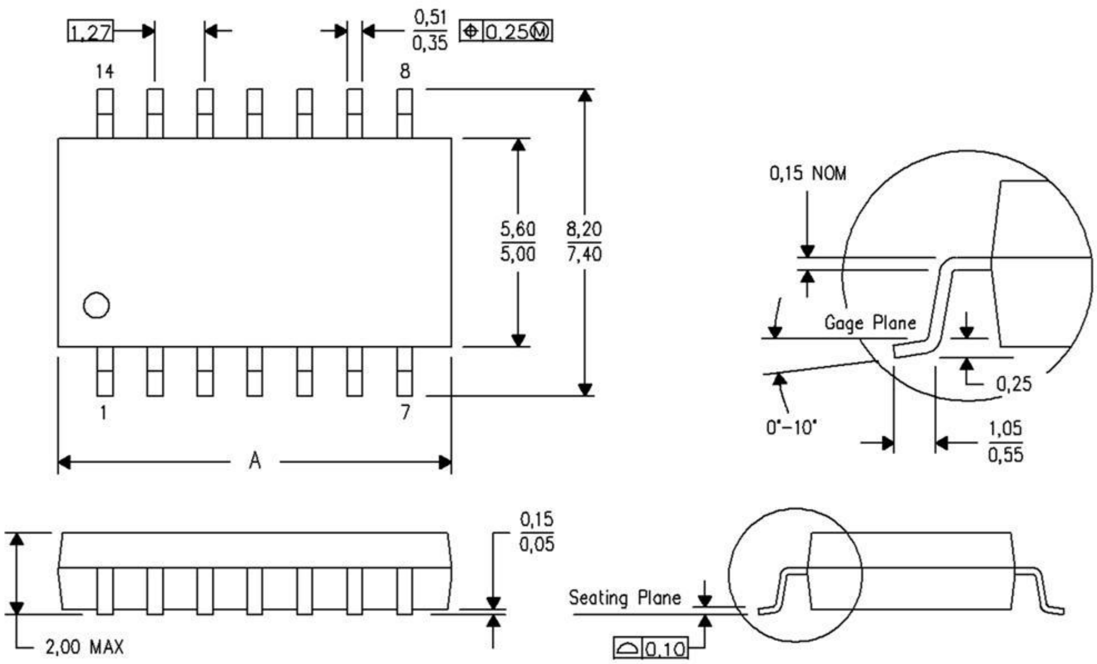
D (R-PDSO-G14) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



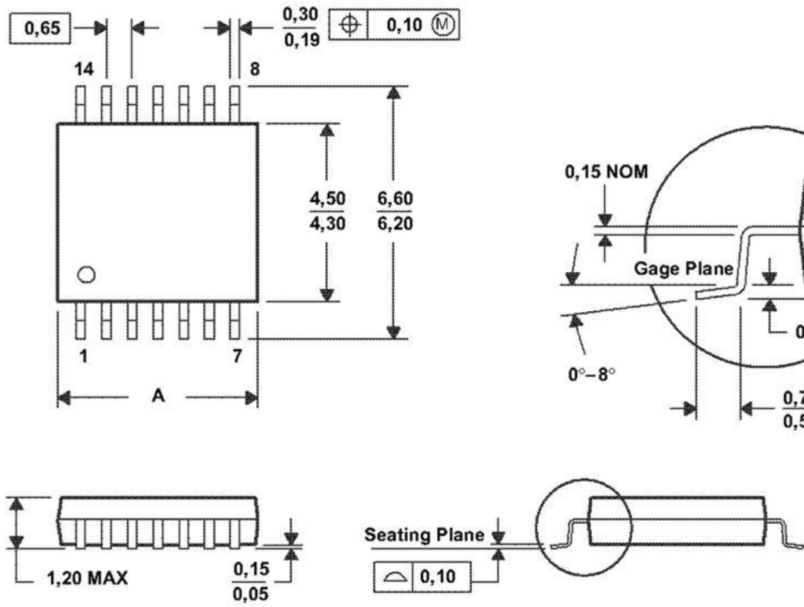
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

National Semiconductor

January 2001

LM111/LM211/LM311 Voltage Comparator

1.0 General Description

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

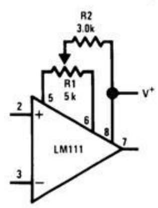
The LM211 is identical to the LM111, except that its performance is specified over a −25˚C to +85˚C temperature range instead of −55˚C to +125˚C. The LM311 has a temperature range of 0˚C to +70˚C.

2.0 Features

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

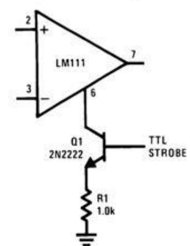
3.0 Typical Applications (Note 3)

Offset Balancing



00570436

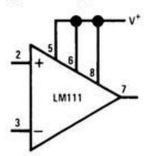
Strobing



00570437

Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

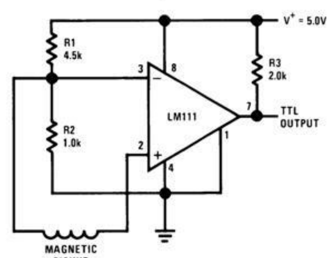
Increasing Input Stage Current (Note 1)



00570438

Note 1: Increases typical common mode slew from 7.0V/µs to 18V/µs.

Detector for Magnetic Transducer

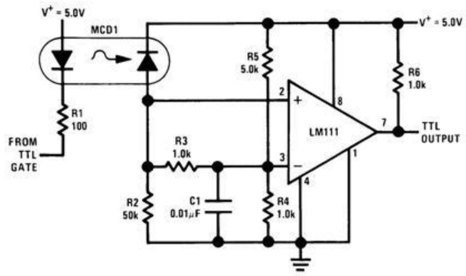


00570439

© 2004 National Semiconductor Corporation DS005704 www.national.com

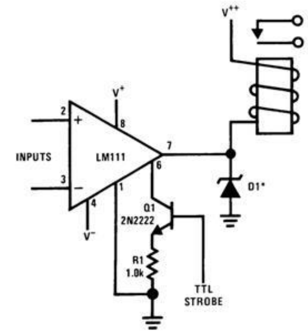
3.0 Typical Applications (Note 3) (Continued)

Digital Transmission Isolator



00570440

Relay Driver with Strobe

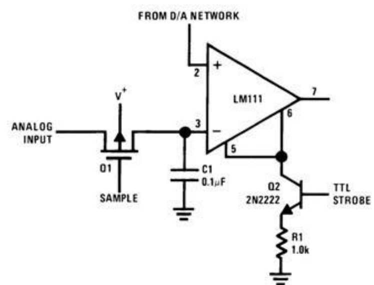


00570441

*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

Note: Do Not Ground Strobe Pin.

Strobing off Both Input and Output Stages (Note 2)



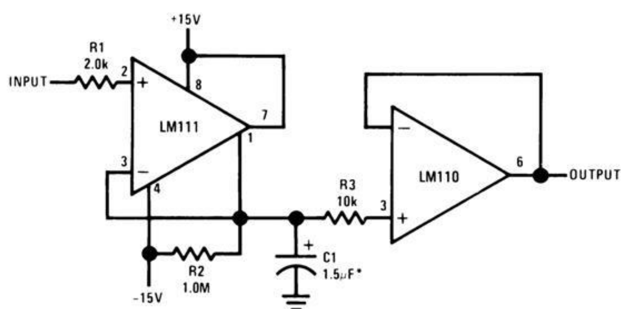
00570442

Note: Do Not Ground Strobe Pin.

Note 2: Typical input current is 50 pA with inputs strobed off.

Note 3: Pin connections shown on schematic diagram and typical applications are for H08 metal can package.

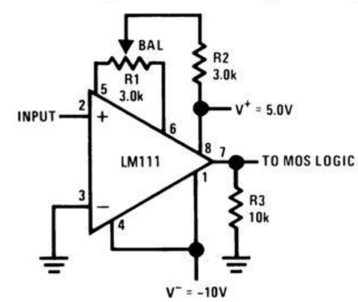
Positive Peak Detector



00570423

*Solid tantalum

Zero Crossing Detector Driving MOS Logic



00570424

4.0 Absolute Maximum Ratings for the LM111/LM211 (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	50V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 4)	±15V
Output Short Circuit Duration	10 sec
Operating Temperature Range	
LM111	−55˚C to 125˚C
LM211	−25˚C to 85˚C
Lead Temperature (Soldering, 10 sec)	260˚C
Voltage at Strobe Pin	V^+−5V
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260˚C
Small Outline Package	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	220˚C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Rating (Note 11)	300V

Electrical Characteristics (Note 6) for the LM111 and LM211

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 7)	T_A=25˚C, R_S≤50k		0.7	3.0	mV
Input Offset Current	T_A=25˚C		4.0	10	nA
Input Bias Current	T_A=25˚C		60	100	nA
Voltage Gain	T_A=25˚C	40	200		V/mV
Response Time (Note 8)	T_A=25˚C		200		ns
Saturation Voltage	V_{IN}≤−5 mV, I_{OUT}=50 mA T_A=25˚C		0.75	1.5	V
Strobe ON Current (Note 9)	T_A=25˚C		2.0	5.0	mA
Output Leakage Current	V_{IN}≥5 mV, V_{OUT}=35V T_A=25˚C, I_{STROBE}=3 mA		0.2	10	nA
Input Offset Voltage (Note 7)	R_S≤50 k			4.0	mV
Input Offset Current (Note 7)				20	nA
Input Bias Current				150	nA
Input Voltage Range	V^+=15V, V^-=−15V, Pin 7 Pull-Up May Go To 5V	−14.5	13.8,-14.7	13.0	V
Saturation Voltage	V^+≥4.5V, V^-=0 V_{IN}≤−6 mV, I_{OUT}≤8 mA		0.23	0.4	V
Output Leakage Current	V_{IN}≥5 mV, V_{OUT}=35V		0.1	0.5	µA
Positive Supply Current	T_A=25˚C		5.1	6.0	mA
Negative Supply Current	T_A=25˚C		4.1	5.0	mA

Note 4: This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 5: The maximum junction temperature of the LM111 is 150˚C, while that of the LM211 is 110˚C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165˚C/W, junction to ambient, or 20˚C/W, junction to case. The thermal resistance of the dual-in-line package is 110˚C/W, junction to ambient.

Note 6: These specifications apply for V_S=±15V and Ground pin at ground, and −55˚C≤T_A≤+125˚C, unless otherwise stated. With the LM211, however, all temperature specifications are limited to −25˚C≤T_A≤+85˚C. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 7: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and R_S.

Note 8: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 9: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 10: Refer to RETS111X for the LM111H, LM111J and LM111J-8 military specifications.

Note 11: Human body model, 1.5 kΩ in series with 100 pF.

5.0 Absolute Maximum Ratings for the LM311 (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 13)	±15V
Power Dissipation (Note 14)	500 mW
ESD Rating (Note 19)	300V
Output Short Circuit Duration	10 sec
Operating Temperature Range	0° to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	260°C
Voltage at Strobe Pin	V^+−5V
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 15) for the LM311

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 16)	T_A=25°C, R_S≤50k		2.0	7.5	mV
Input Offset Current(Note 16)	T_A=25°C		6.0	50	nA
Input Bias Current	T_A=25°C		100	250	nA
Voltage Gain	T_A=25°C	40	200		V/mV
Response Time (Note 17)	T_A=25°C		200		ns
Saturation Voltage	V_{IN}≤−10 mV, I_{OUT}=50 mA T_A=25°C		0.75	1.5	V
Strobe ON Current (Note 18)	T_A=25°C		2.0	5.0	mA
Output Leakage Current	V_{IN}≥10 mV, V_{OUT}=35V T_A=25°C, I_{STROBE}=3 mA V^- = Pin 1 = −5V		0.2	50	nA
Input Offset Voltage (Note 16)	R_S≤50K			10	mV
Input Offset Current (Note 16)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8,−14.7	13.0	V
Saturation Voltage	V^+≥4.5V, V^-=0 V_{IN}≤−10 mV, I_{OUT}≤8 mA		0.23	0.4	V
Positive Supply Current	T_A=25°C		5.1	7.5	mA
Negative Supply Current	T_A=25°C		4.1	5.0	mA

Note 12: "Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits."

Note 13: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 14: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 15: These specifications apply for V_S=±15V and Pin 1 at ground, and 0°C < T_A < +70°C, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 16: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and R_S.

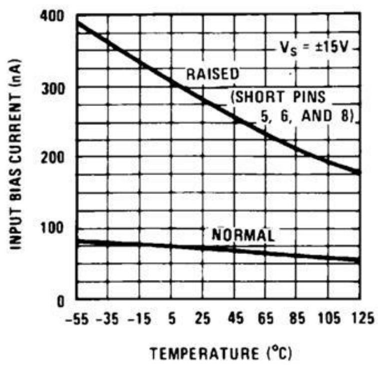
Note 17: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 18: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 19: Human body model, 1.5 kΩ in series with 100 pF.

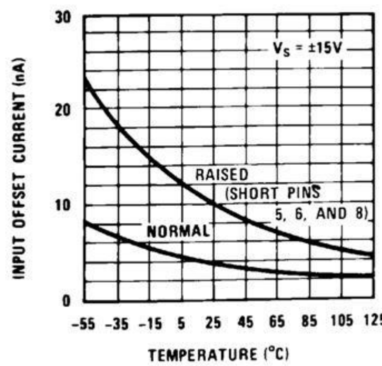
6.0 LM111/LM211 Typical Performance Characteristics

Input Bias Current



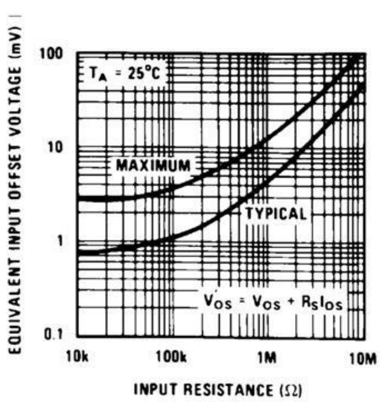
00570443

Input Bias Current



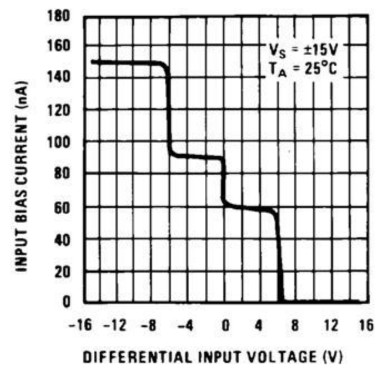
00570444

Input Bias Current



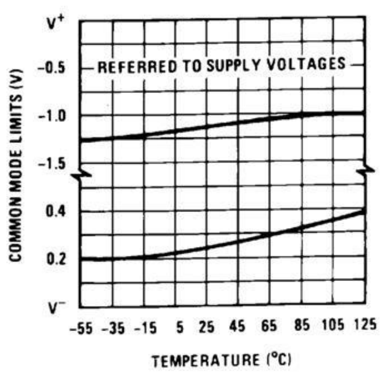
00570445

Input Bias Current



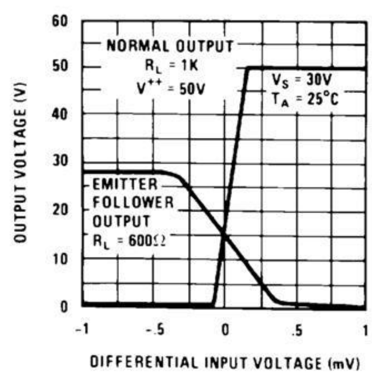
00570446

Input Bias Current



00570447

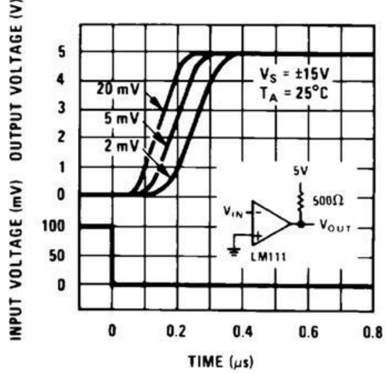
Input Bias Current



00570448

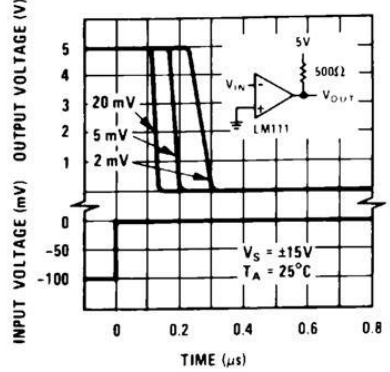
6.0 LM111/LM211 Typical Performance Characteristics (Continued)

Input Bias Current Input Overdrives



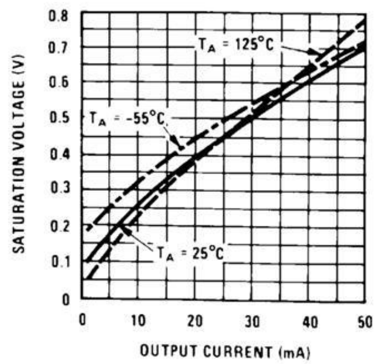
00570449

Input Bias Current Input Overdrives



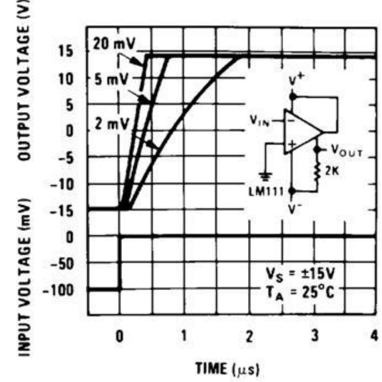
00570450

Input Bias Current



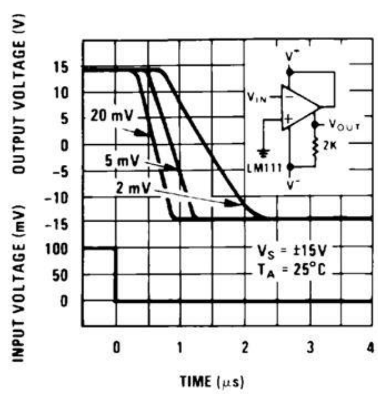
00570451

Response Time for Various Input Overdrives



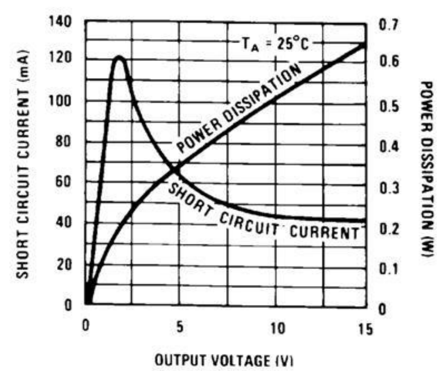
00570452

Response Time for Various Input Overdrives



00570453

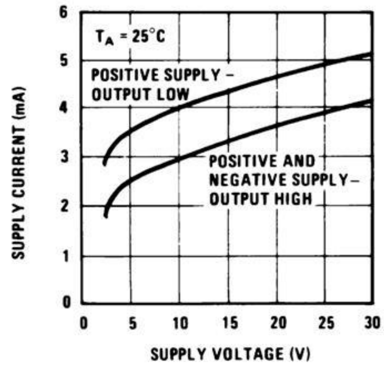
Output Limiting Characteristics



00570454

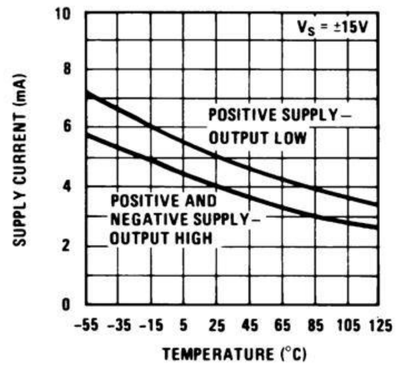
6.0 LM111/LM211 Typical Performance Characteristics (Continued)

Supply Current



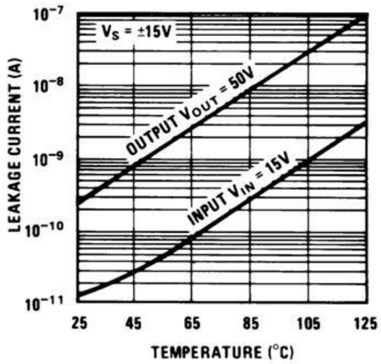
00570455

Supply Current



00570456

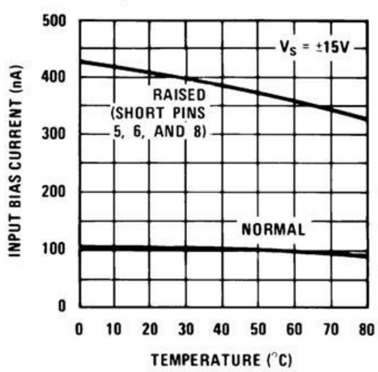
Leakage Currents



00570457

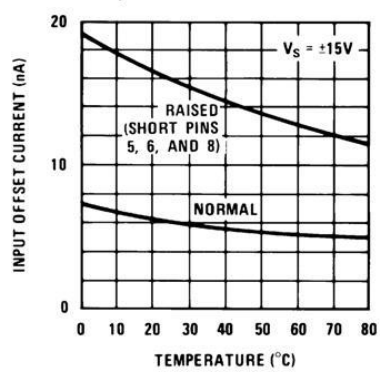
7.0 LM311 Typical Performance Characteristics

Input Bias Current



00570458

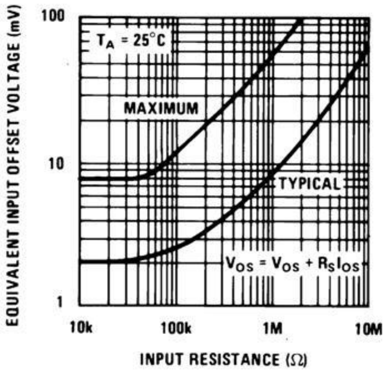
Input Offset Current



00570459

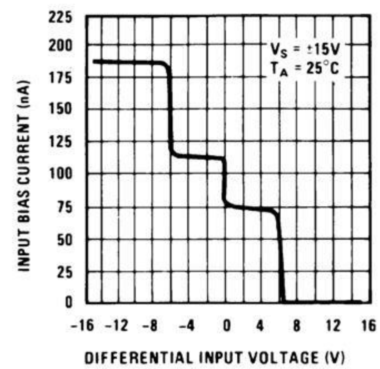
7.0 LM311 Typical Performance Characteristics (Continued)

Offset Error



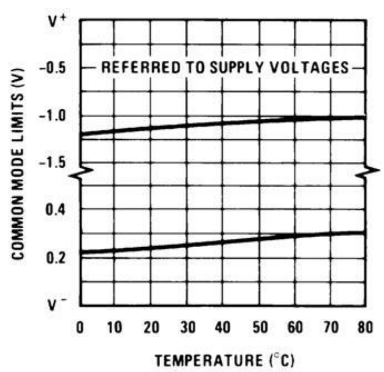
00570460

Input Characteristics



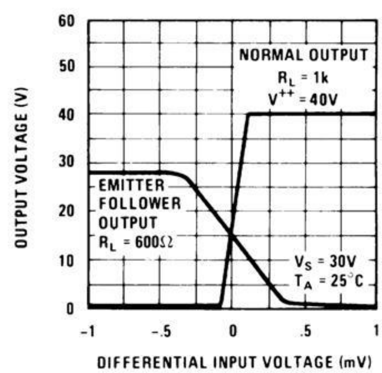
00570461

Common Mode Limits



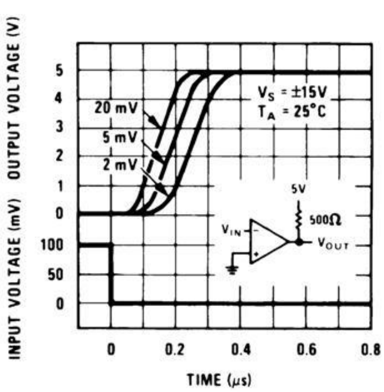
00570462

Transfer Function



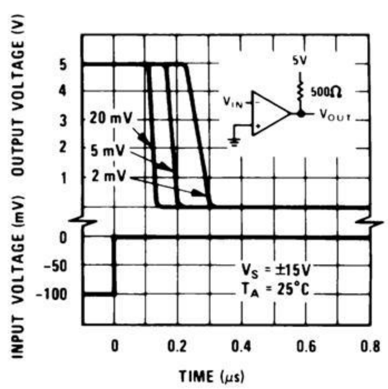
00570463

Response Time for Various Input Overdrives



00570464

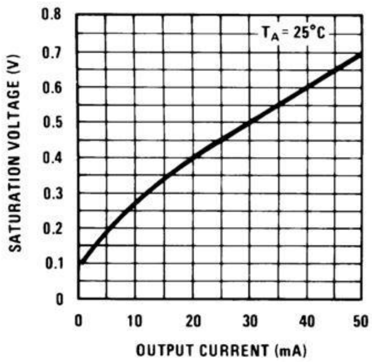
Response Time for Various Input Overdrives



00570465

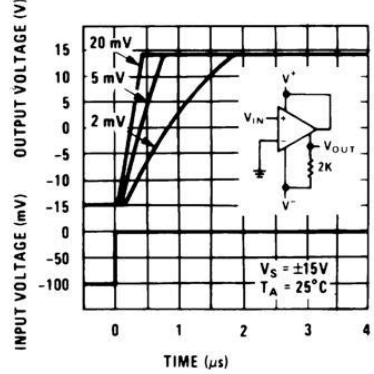
7.0 LM311 Typical Performance Characteristics (Continued)

Output Saturation Voltage



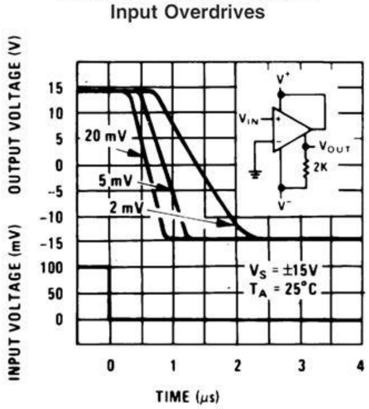
00570466

Response Time for Various Input Overdrives



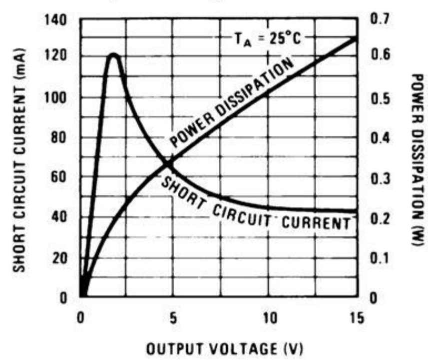
00570467

Response Time for Various Input Overdrives



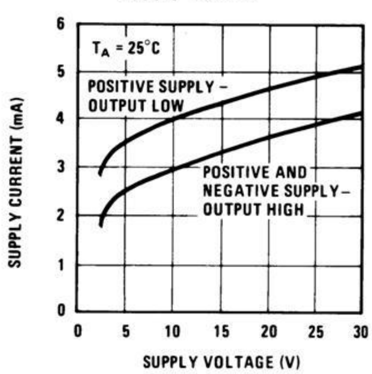
00570468

Output Limiting Characteristics



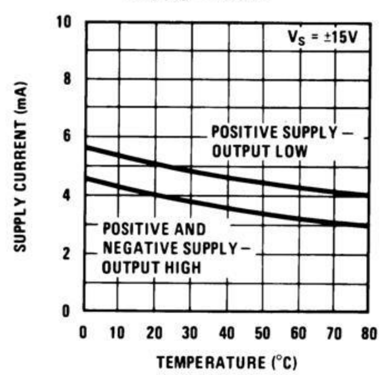
00570469

Supply Current



00570470

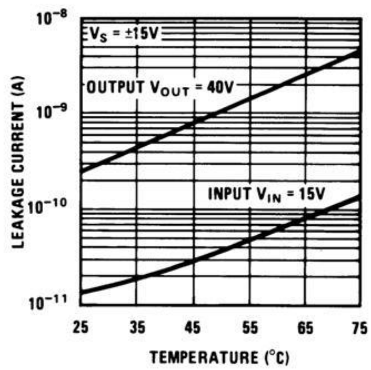
Supply Current



00570471

7.0 LM311 Typical Performance Characteristics (Continued)

Leakage Currents



00570472

8.0 Application Hints

8.1 CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

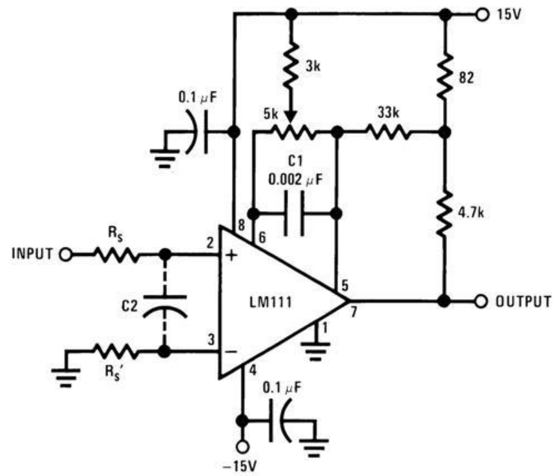
However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 µF capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.
4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S=10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 µF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.

8.0 Application Hints (Continued)

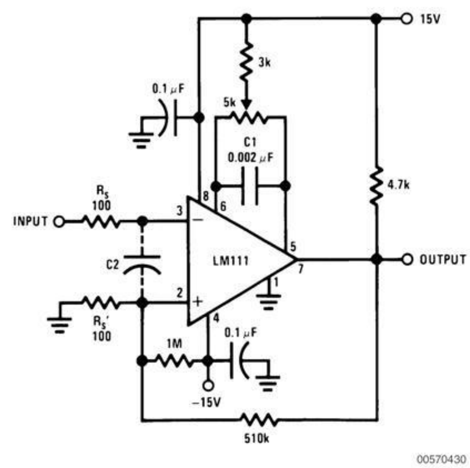
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.

8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 1. Improved Positive Feedback



Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 2. Conventional Positive Feedback

8.0 Application Hints (Continued)

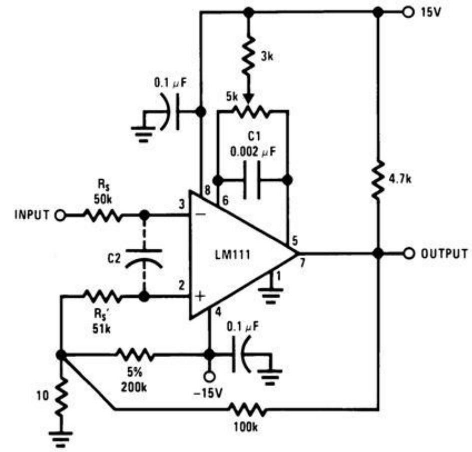
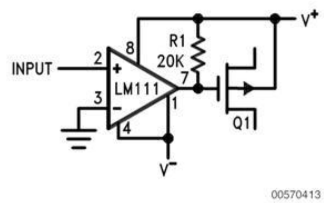


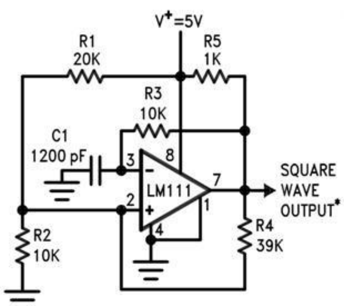
FIGURE 3. Positive Feedback with High Source Resistance

9.0 Typical Applications (Pin numbers refer to H08 package)

Zero Crossing Detector Driving MOS Switch



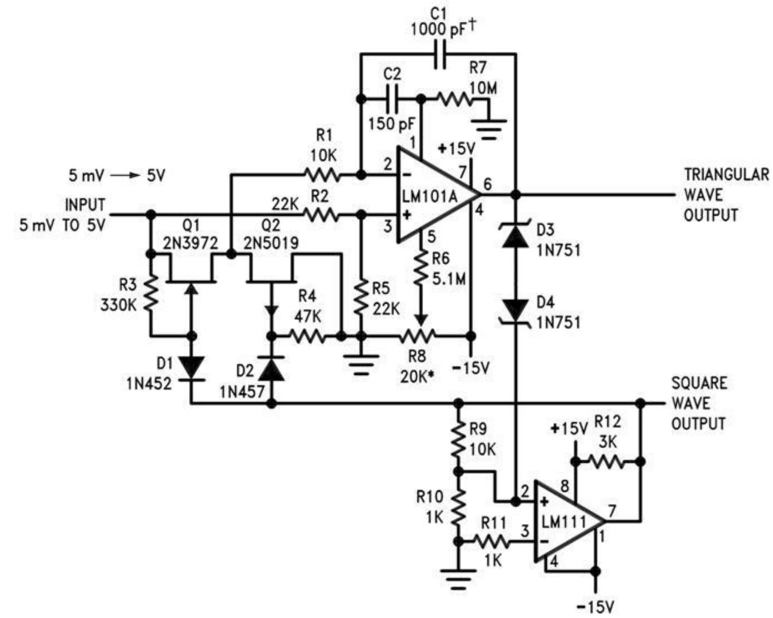
100 kHz Free Running Multivibrator



*TTL or DTL fanout of two

9.0 Typical Applications (Pin numbers refer to H08 package) (Continued)

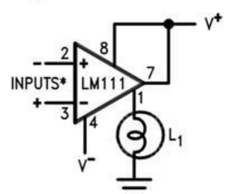
10 Hz to 10 kHz Voltage Controlled Oscillator



*Adjust for symmetrical square wave time when V_{IN} = 5 mV

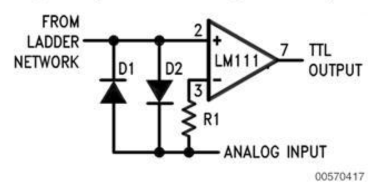
†Minimum capacitance 20 pF Maximum frequency 50 kHz

Driving Ground-Referred Load

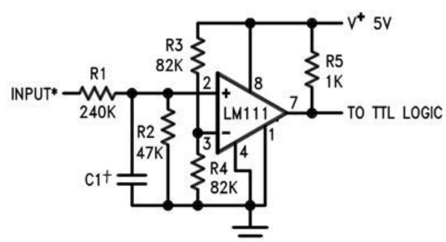


*Input polarity is reversed when using pin 1 as output.

Using Clamp Diodes to Improve Response



TTL Interface with High Level Logic

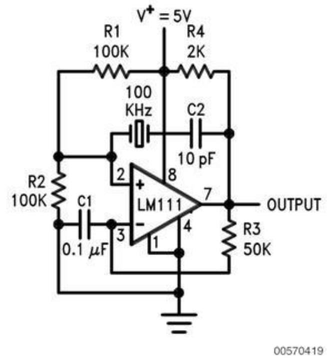


*Values shown are for a 0 to 30V logic swing and a 15V threshold.

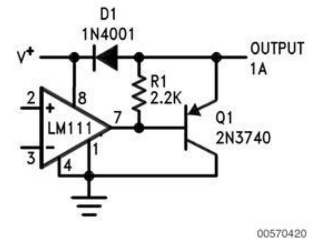
†May be added to control speed and reduce susceptibility to noise spikes.

9.0 Typical Applications (Pin numbers refer to H08 package) (Continued)

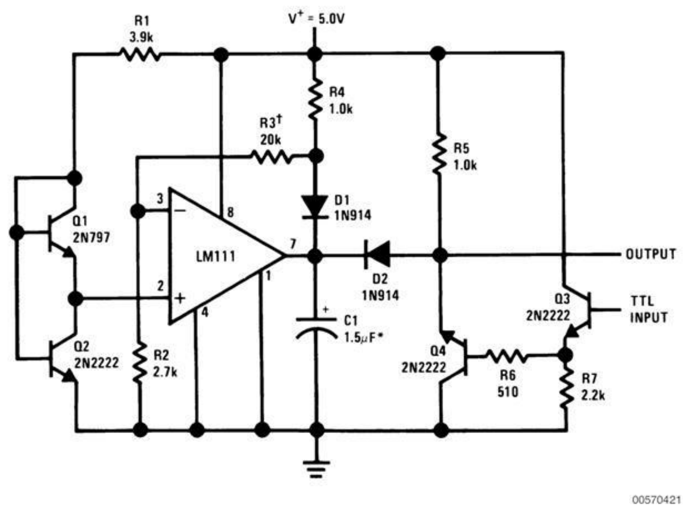
Crystal Oscillator



Comparator and Solenoid Driver



Precision Squarer

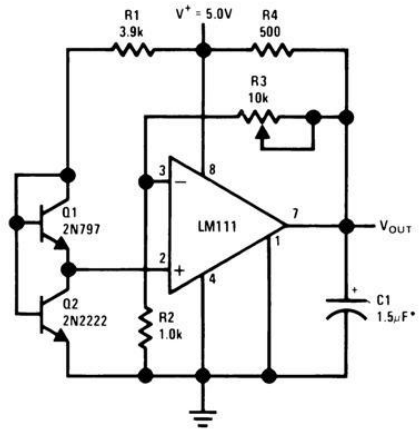


*Solid tantalum

†Adjust to set clamp level

9.0 Typical Applications (Pin numbers refer to H08 package) (Continued)

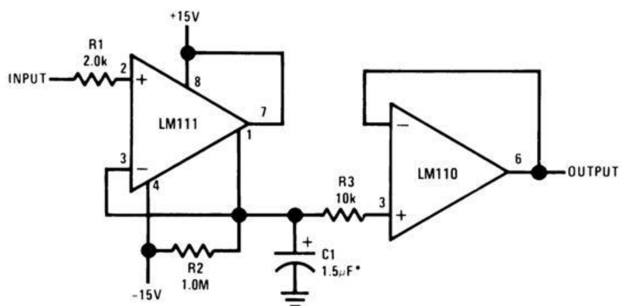
Low Voltage Adjustable Reference Supply



00570422

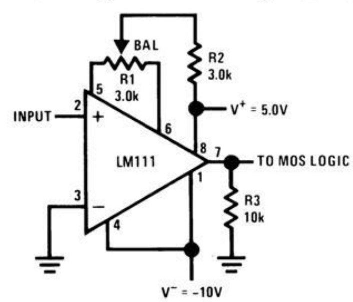
*Solid tantalum

Positive Peak Detector



00570423

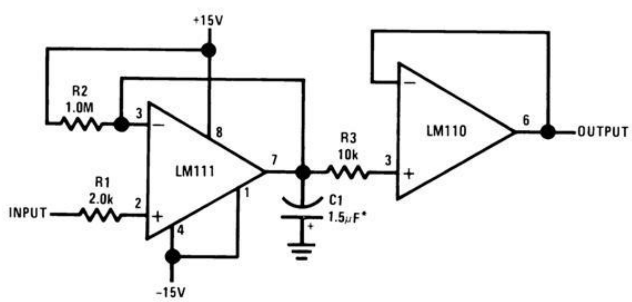
Zero Crossing Detector Driving MOS Logic



00570424

*Solid tantalum

Negative Peak Detector

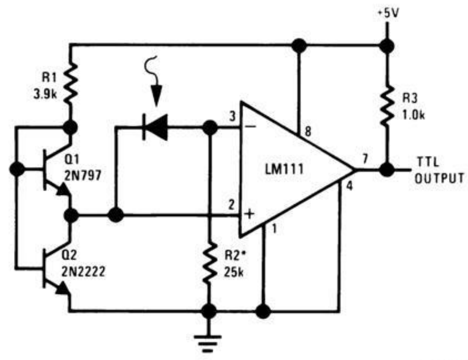


00570425

*Solid tantalum

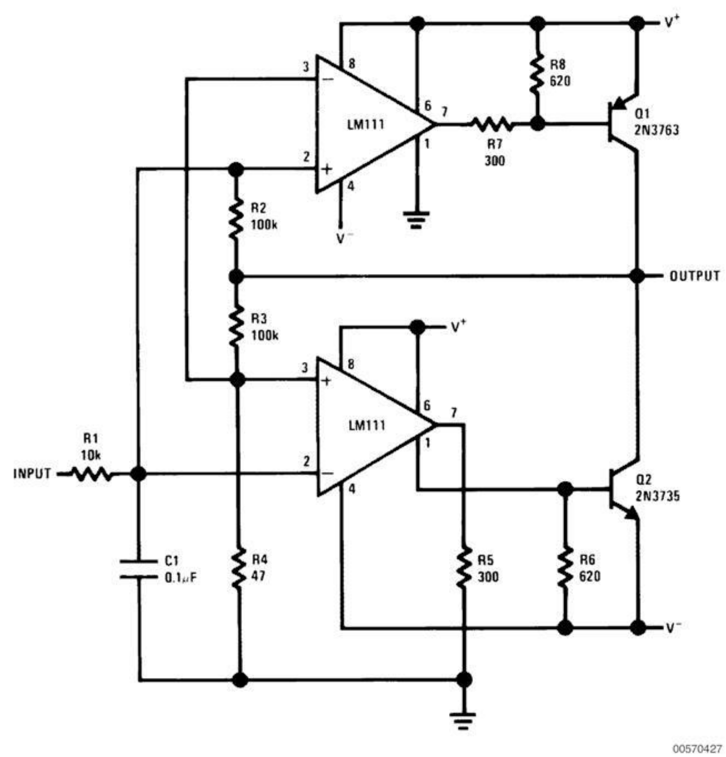
9.0 Typical Applications (Pin numbers refer to H08 package) (Continued)

Precision Photodiode Comparator



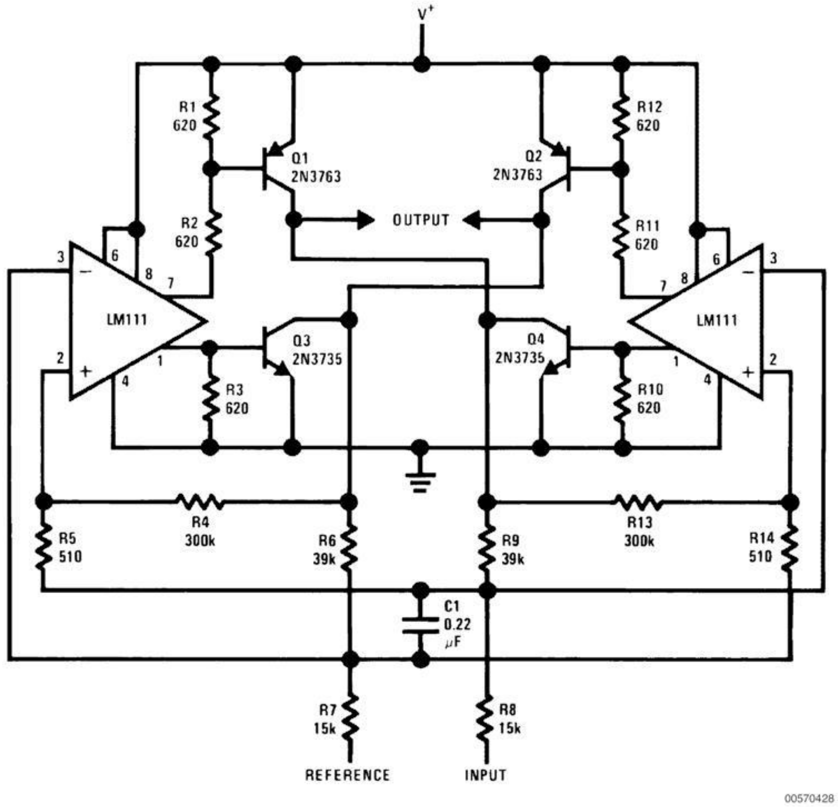
*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

Switching Power Amplifier

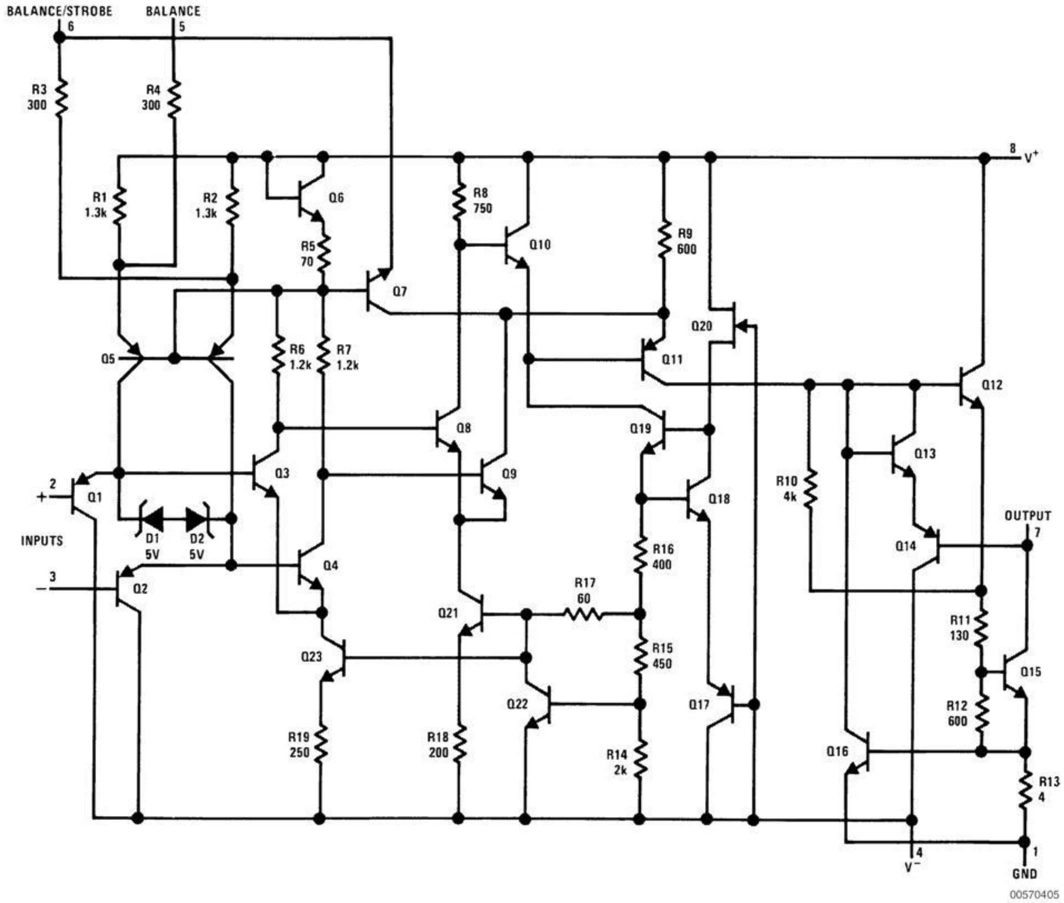


9.0 Typical Applications (Pin numbers refer to H08 package) (Continued)

Switching Power Amplifier



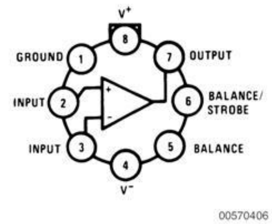
10.0 Schematic Diagram (Note 20)



Note 20: Pin connections shown on schematic diagram are for H08 package.

11.0 Connection Diagrams

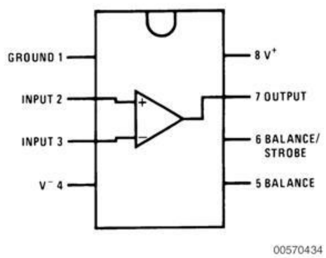
Metal Can Package



Note: Pin 4 connected to case

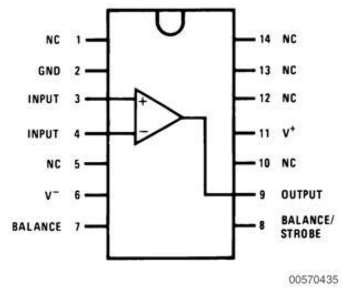
Top View
Order Number LM111H, LM111H/883(Note 21) **, LM211H or LM311H**
See NS Package Number H08C

Dual-In-Line Package

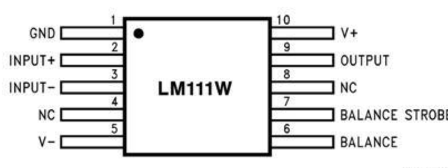


Top View
Order Number LM111J-8, LM111J-8/883(Note 21)**,**
LM311M, LM311MX or LM311N
See NS Package Number J08A, M08A or N08E

Dual-In-Line Package



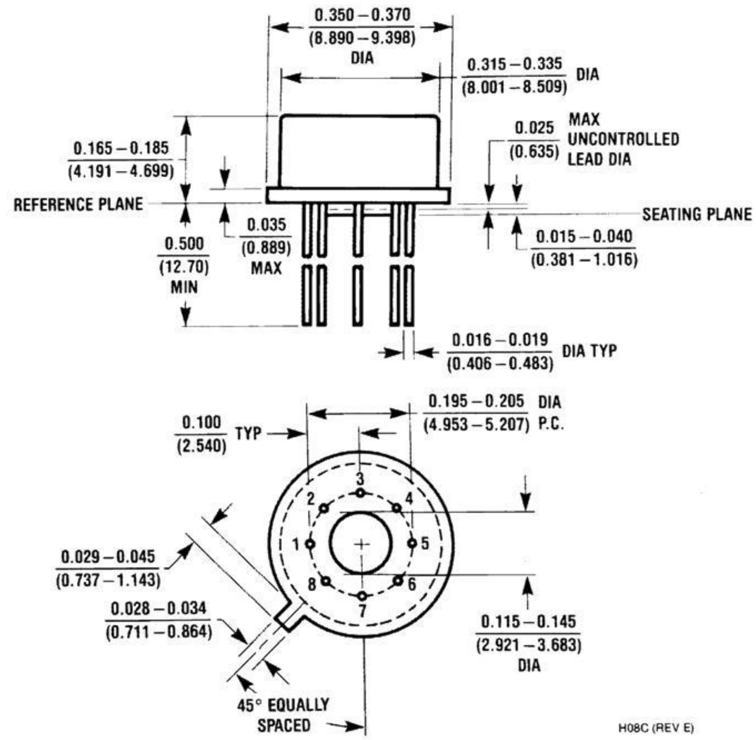
Top View
Order Number LM111J/883(Note 21)
See NS Package Number J14A or N14A



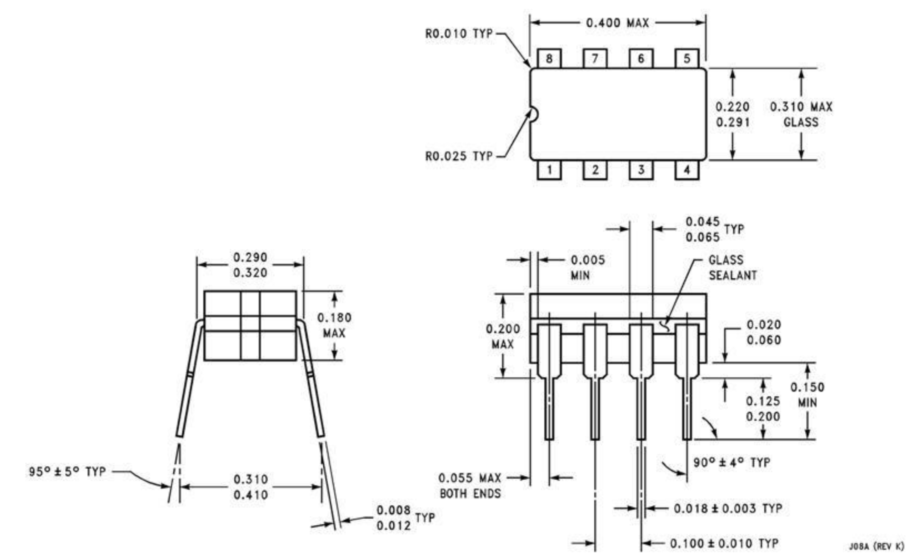
Order Number LM111W/883(Note 21)**, LM111WG/883**
See NS Package Number W10A, WG10A

Note 21: Also available per JM38510/10304

12.0 Physical Dimensions inches (millimeters) unless otherwise noted

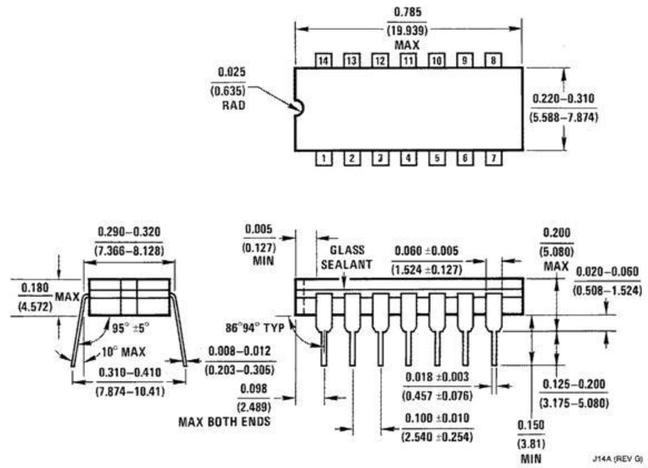


Metal Can Package (H)
Order Number LM111H, LM111H/883, LM211H or LM311H
NS Package Number H08C

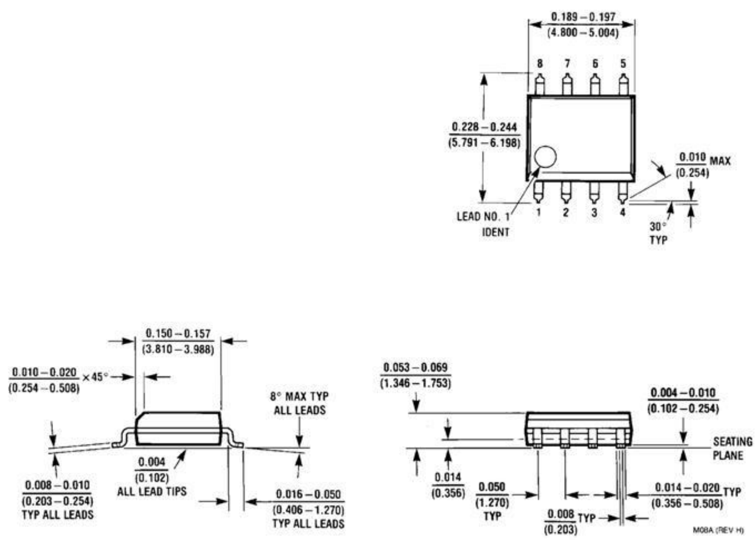


Cavity Dual-In-Line Package (J)
Order Number LM111J-8, LM111J-8/883
NS Package Number J08A

12.0 Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

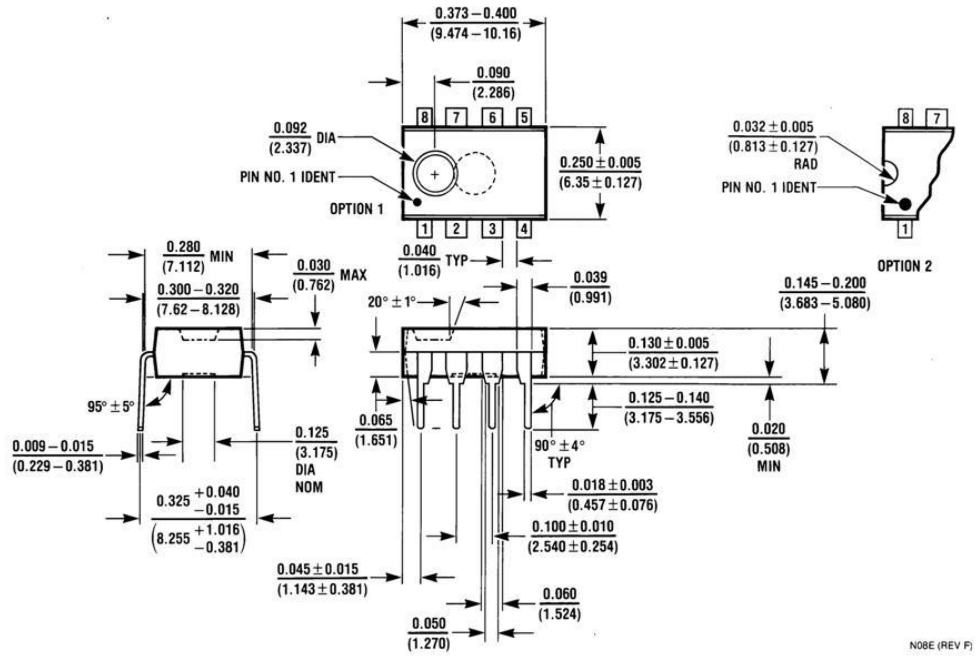


Dual-In-Line Package (J)
Order Number LM111J/883
NS Package Number J14A

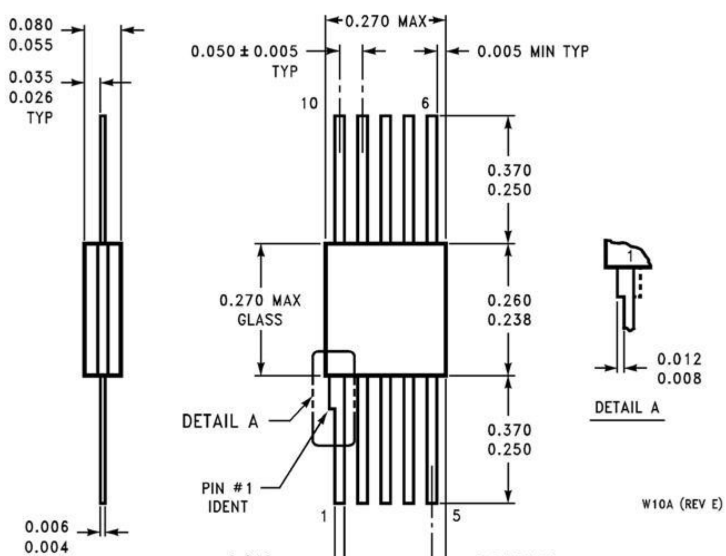


Dual-In-Line Package (M)
Order Number LM311M, LM311MX
NS Package Number M08A

12.0 Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number LM311N
NS Package Number N08E



Order Number LM111W/883, LM111WG/883
NS Package Number W10A, WG10A

Notes

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at www.national.com.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.

National Semiconductor Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560

www.national.com

80V/2.5A Peak, High Frequency Full Bridge FET Driver

The HIP4081A is a high frequency, medium voltage Full Bridge N-Channel FET driver IC, available in 20 lead plastic SOIC and DIP packages. The HIP4081A can drive every possible switch combination except those which would cause a shoot-through condition. The HIP4081A can switch at frequencies up to 1MHz and is well suited to driving Voice Coil Motors, high-frequency switching power amplifiers, and power supplies.

For example, the HIP4081A can drive medium voltage brush motors, and two HIP4081As can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability.

Short propagation delays of approximately 55ns maximizes control loop crossover frequencies and dead-times which can be adjusted to near zero to minimize distortion, resulting in rapid, precise control of the driven load.

A similar part, the HIP4080A, includes an on-chip input comparator to create a PWM signal from an external triangle wave and to facilitate "hysteresis mode" switching.

The Application Note for the HIP4081A is the AN9405.

Ordering Information

PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
HIP4081AIP	-40 to 85	20 Ld PDIP	E20.3
HIP4081AIPZ (Note)	-40 to 85	20 Ld PDIP (Pb-free)	E20.3
HIP4081AIB	-40 to 85	20 Ld SOIC (W)	M20.3
HIP4081AIBZ (Note)	-40 to 85	20 Ld SOIC (W) (Pb-free)	M20.3

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

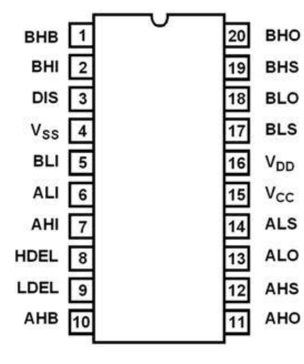
- Independently Drives 4 N-Channel FET in Half Bridge or Full Bridge Configurations
- Bootstrap Supply Max Voltage to $95V_{DC}$
- Drives 1000pF Load at 1MHz in Free Air at 50°C with Rise and Fall Times of Typically 10ns
- User-Programmable Dead Time
- On-Chip Charge-Pump and Bootstrap Upper Bias Supplies
- DIS (Disable) Overrides Input Control
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Very Low Power Consumption
- Undervoltage Protection
- Pb-free Available

Applications

- Medium/Large Voice Coil Motors
- Full Bridge Power Supplies
- Switching Power Amplifiers
- High Performance Motor Controls
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- U.P.S.

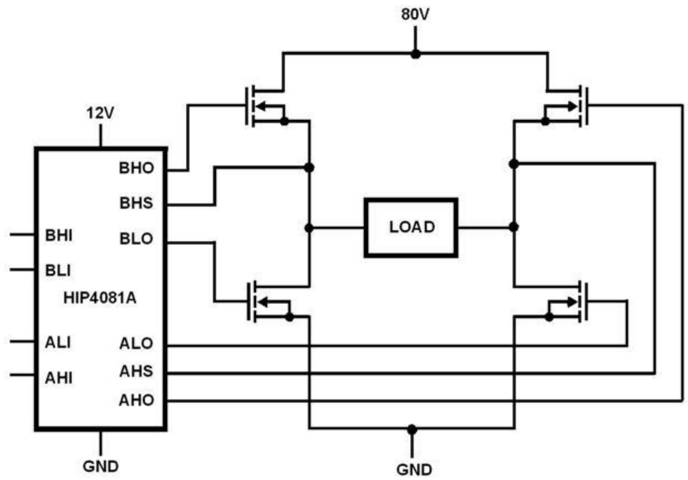
Pinout

HIP4081A
(PDIP, SOIC)
TOP VIEW

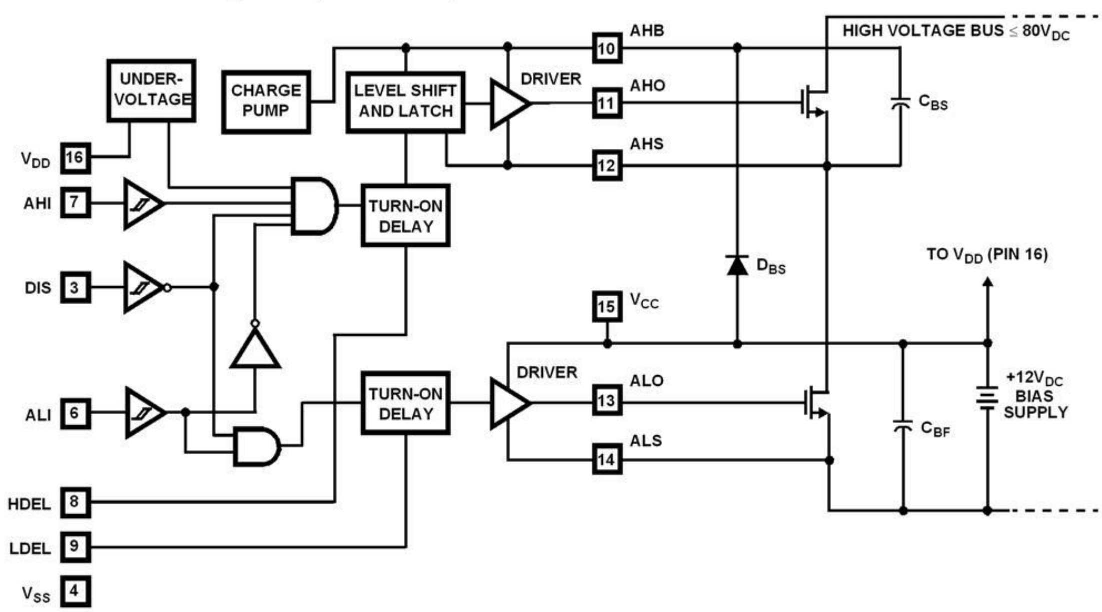


CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 321-724-7143 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
Copyright Harris Corporation. Copyright Intersil Americas Inc. 2003, 2004. All Rights Reserved
All other trademarks mentioned are the property of their respective owners.

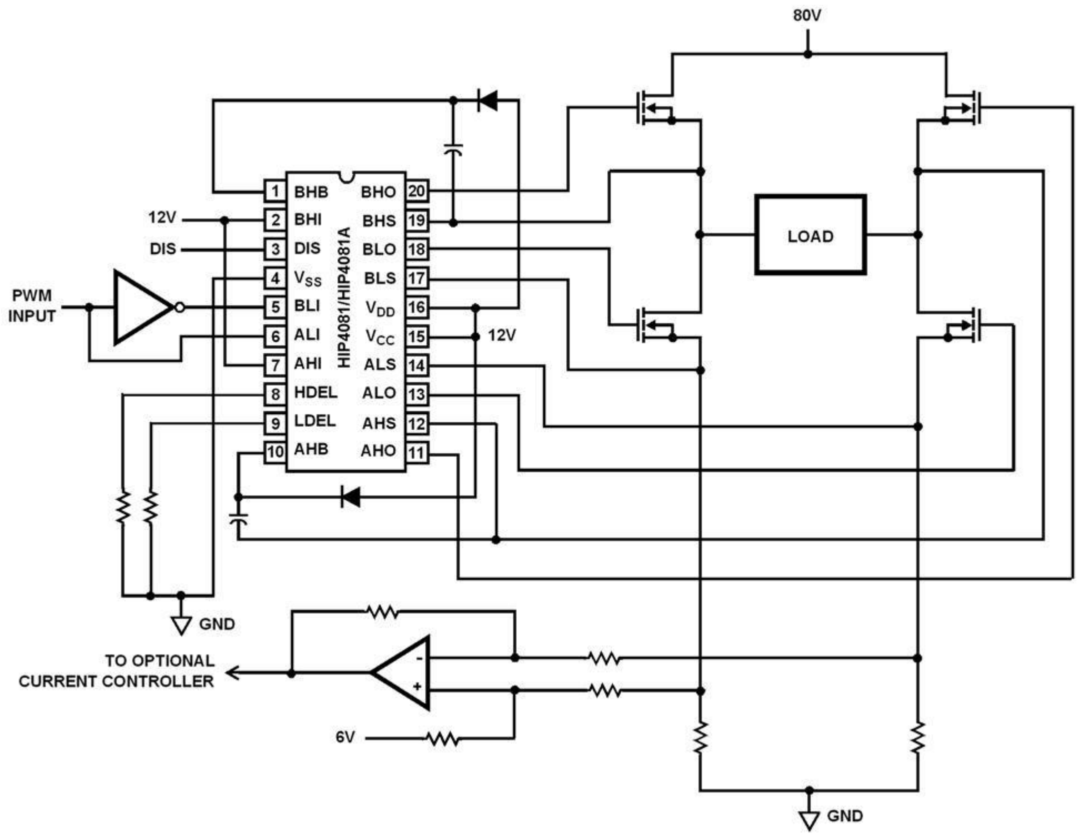
Application Block Diagram



Functional Block Diagram (1/2 HIP4081A)



Typical Application (PWM Mode Switching)



Absolute Maximum Ratings

Supply Voltage, V_{DD} and V_{CC} . . . . -0.3V to 16V
Logic I/O Voltages . . . . -0.3V to V_{DD} +0.3V
Voltage on AHS, BHS . . . -6.0V (Transient) to 80V (25°C to 125°C)
Voltage on AHS, BHS . . . -6.0V (Transient) to 70V (-55°C to 125°C)
Voltage on ALS, BLS . . . . -2.0V (Transient) to +2.0V (Transient)
Voltage on AHB, BHB . . . . $V_{AHS, BHS}$ -0.3V to $V_{AHS, BHS}$ +V_{DD}
Voltage on ALO, BLO . . . . $V_{ALS, BLS}$ -0.3V to V_{CC} +0.3V
Voltage on AHO, BHO . . . . $V_{AHS, BHS}$ -0.3V to $V_{AHB, BHB}$ +0.3V
Input Current, HDEL and LDEL . . . . -5mA to 0mA
Phase Slew Rate 20V/ns
NOTE: All Voltages relative to V_{SS}, unless otherwise specified.

Operating Conditions

Supply Voltage, V_{DD} and V_{CC} . . . . +9.5V to +15V
Voltage on ALS, BLS . . . . -1.0V to +1.0V
Voltage on AHB, BHB . . . . $V_{AHS, BHS}$ +5V to $V_{AHS, BHS}$ +15V
Input Current, HDEL and LDEL . . . . -500μA to -50μA
Operating Ambient Temperature Range . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SOIC Package 85
DIP Package 75
Storage Temperature Range . . . . -65°C to 150°C
Operating Max. Junction Temperature . . . . 125°C
Lead Temperature (Soldering 10s)). . . . . 300°C
(For SOIC - Lead Tips Only

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB}$ = 12V, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS}$ = 0V, $R_{HDEL} = R_{LDEL}$ = 100K and T_A = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = 25°C			T_{JS} = -40°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS AND CHARGE PUMPS								
V_{DD} Quiescent Current	I_{DD}	All inputs = 0V	8.5	10.5	14.5	7.5	14.5	mA
V_{DD} Operating Current	I_{DDO}	Outputs switching f = 500kHz	9.5	12.5	15.5	8.5	15.5	mA
V_{CC} Quiescent Current	I_{CC}	All Inputs = 0V, $I_{ALO} = I_{BLO}$ = 0	-	0.1	10	-	20	μA
V_{CC} Operating Current	I_{CCO}	f = 500kHz, No Load	1	1.25	2.0	0.8	3	mA
AHB, BHB Quiescent Current - Qpump Output Current	I_{AHB}, I_{BHB}	All Inputs = 0V, $I_{AHO} = I_{BHO}$ = 0 $V_{DD} = V_{CC} = V_{AHB} = V_{BHB}$ = 10V	-50	-30	-11	-60	-10	μA
AHB, BHB Operating Current	I_{AHBO}, I_{BHBO}	f = 500kHz, No Load	0.6	1.2	1.5	0.5	1.9	mA
AHS, BHS, AHB, BHB Leakage Current	I_{HLK}	$V_{BHS} = V_{AHS}$ = 80V, $V_{AHB} = V_{BHB}$ = 93V	-	0.02	1.0	-	10	μA
AHB-AHS, BHB-BHS Qpump Output Voltage	V_{AHB}-V_{AHS} V_{BHB}-V_{BHS}	$I_{AHB} = I_{AHB}$ = 0, No Load	11.5	12.6	14.0	10.5	14.5	V
INPUT PINS: ALI, BLI, AHI, BHI, AND DIS								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-130	-100	-75	-135	-65	μA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	μA
TURN-ON DELAY PINS: LDEL AND HDEL								
LDEL, HDEL Voltage	V_{HDEL}, V_{LDEL}	$I_{HDEL} = I_{LDEL}$ = -100μA	4.9	5.1	5.3	4.8	5.4	V
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, AND BHO								
Low Level Output Voltage	V_{OL}	I_{OUT} = 100mA	0.7	0.85	1.0	0.5	1.1	V
High Level Output Voltage	V_{CC}-V_{OH}	I_{OUT} = -100mA	0.8	0.95	1.1	0.5	1.2	V
Peak Pullup Current	I_O+	V_{OUT} = 0V	1.7	2.6	3.8	1.4	4.1	A

Electrical Specifications $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$ and $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = 25°C$			T_{JS} = -40°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
Peak Pulldown Current	I_O-	$V_{OUT} = 12V$	1.7	2.4	3.3	1.3	3.6	A
Undervoltage, Rising Threshold	UV+		8.1	8.8	9.4	8.0	9.5	V
Undervoltage, Falling Threshold	UV-		7.6	8.3	8.9	7.5	9.0	V
Undervoltage, Hysteresis	HYS		0.25	0.4	0.65	0.2	0.7	V

Switching Specifications $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$, $C_L = 1000pF$.

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = 25°C$			T_{JS} = -40°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPHL}		-	30	60	-	80	ns
Upper Turn-off Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPHL}		-	35	70	-	90	ns
Lower Turn-on Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPLH}	$R_{HDEL} = R_{LDEL} = 10K$	-	45	70	-	90	ns
Upper Turn-on Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPLH}	$R_{HDEL} = R_{LDEL} = 10K$	-	60	90	-	110	ns
Rise Time	T_R		-	10	25	-	35	ns
Fall Time	T_F		-	10	25	-	35	ns
Turn-on Input Pulse Width	$T_{PWIN-ON}$	$R_{HDEL} = R_{LDEL} = 10K$	50	-	-	50	-	ns
Turn-off Input Pulse Width	$T_{PWIN-OFF}$	$R_{HDEL} = R_{LDEL} = 10K$	40	-	-	40	-	ns
Turn-on Output Pulse Width	$T_{PWOUT-ON}$	$R_{HDEL} = R_{LDEL} = 10K$	40	-	-	40	-	ns
Turn-off Output Pulse Width	$T_{PWOUT-OFF}$	$R_{HDEL} = R_{LDEL} = 10K$	30	-	-	30	-	ns
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}		-	45	75	-	95	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	55	85	-	105	ns
Disable to Lower Turn-on Propagation Delay (DIS - ALO and BLO)	T_{DLPLH}		-	40	70	-	90	ns
Refresh Pulse Width (ALO and BLO)	T_{REF-PW}		240	410	550	200	600	ns
Disable to Upper Enable (DIS - AHO and BHO)	T_{UEN}		-	450	620	-	690	ns

TRUTH TABLE

INPUT				OUTPUT	
ALI, BLI	AHI, BHI	U/V	DIS	ALO, BLO	AHO, BHO
X	X	X	1	0	0
1	X	0	0	1	0
0	1	0	0	0	1
0	0	0	0	0	0
X	X	1	X	0	0

NOTE: X signifies that input can be either a “1” or “0”.

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30μA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
2	BHI	B High-side Input. Logic level input that controls BHO driver (Pin 20). BLI (Pin 5) high level input overrides BHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 3) high level input overrides BHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
3	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
4	V_{SS}	Chip negative supply, generally will be ground.
5	BLI	B Low-side Input. Logic level input that controls BLO driver (Pin 18). If BHI (Pin 2) is driven high or not connected externally then BLI controls both BLO and BHO drivers, with dead time set by delay currents at HDEL and LDEL (Pin 8 and 9). DIS (Pin 3) high level input overrides BLI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
6	ALI	A Low-side Input. Logic level input that controls ALO driver (Pin 13). If AHI (Pin 7) is driven high or not connected externally then ALI controls both ALO and AHO drivers, with dead time set by delay currents at HDEL and LDEL (Pin 8 and 9). DIS (Pin 3) high level input overrides ALI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
7	AHI	A High-side Input. Logic level input that controls AHO driver (Pin 11). ALI (Pin 6) high level input overrides AHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 3) high level input overrides AHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
8	HDEL	High-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V.
9	LDEL	Low-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V.
10	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30μA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
11	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
12	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	ALS	A Low-side Source connection. Connect to source of A Low-side power MOSFET.
15	V_{CC}	Positive supply to gate drivers. Must be same potential as V_{DD} (Pin 16). Connect to anodes of two bootstrap diodes.
16	V_{DD}	Positive supply to lower gate drivers. Must be same potential as V_{CC} (Pin 15). De-couple this pin to V_{SS} (Pin 4).
17	BLS	B Low-side Source connection. Connect to source of B Low-side power MOSFET.
18	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
19	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
20	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

Timing Diagrams

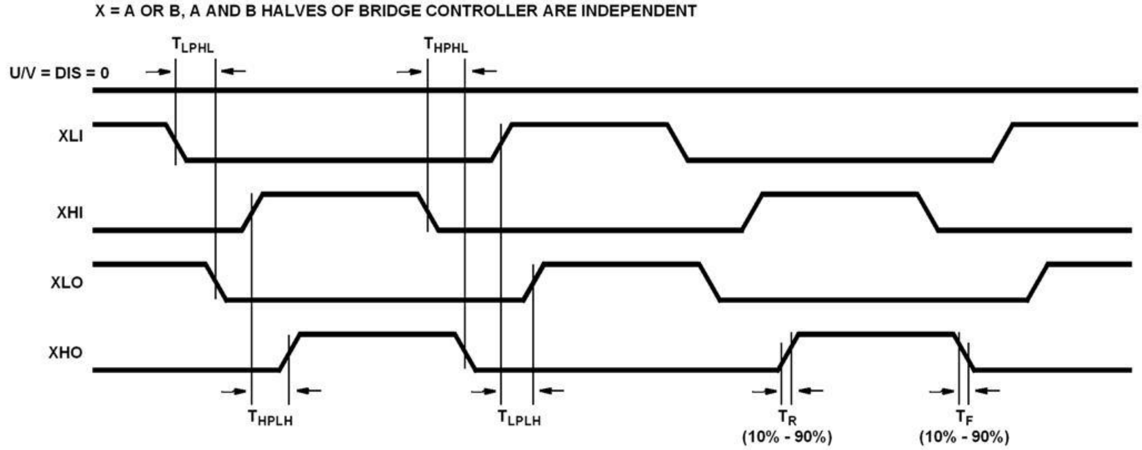


FIGURE 1. INDEPENDENT MODE

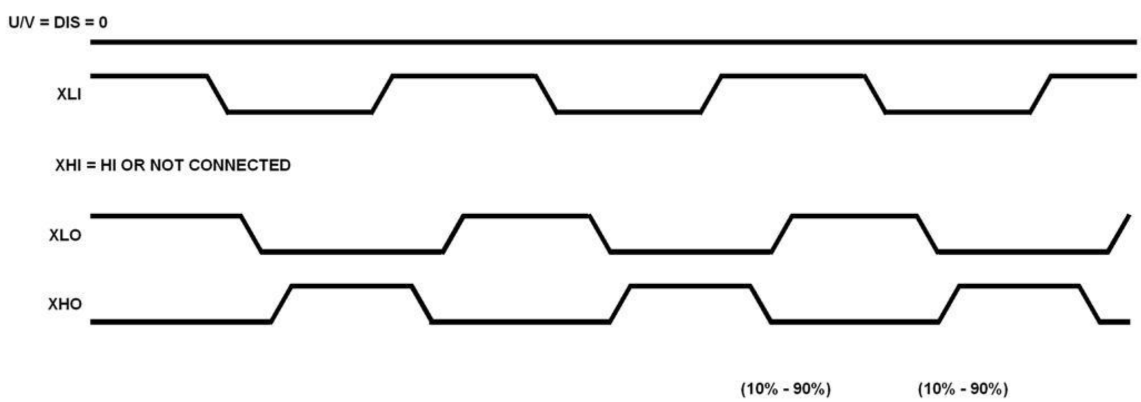


FIGURE 2. BISTATE MODE

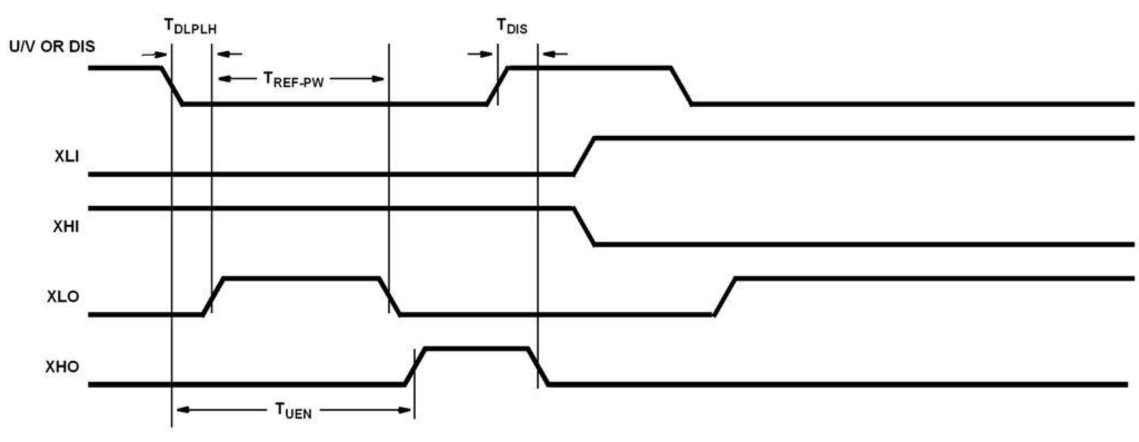


FIGURE 3. DISABLE FUNCTION

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$ and $T_A = 25°C$, Unless Otherwise Specified

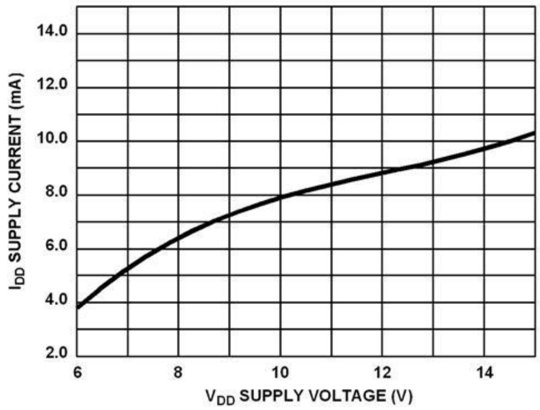


FIGURE 4. QUIESCENT I_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

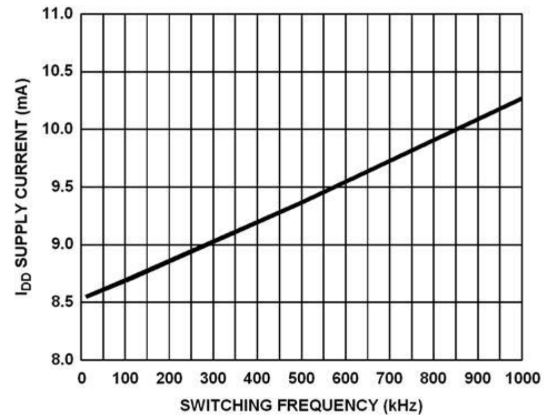


FIGURE 5. I_{DDO}, NO-LOAD I_{DD} SUPPLY CURRENT vs FREQUENCY (kHz)

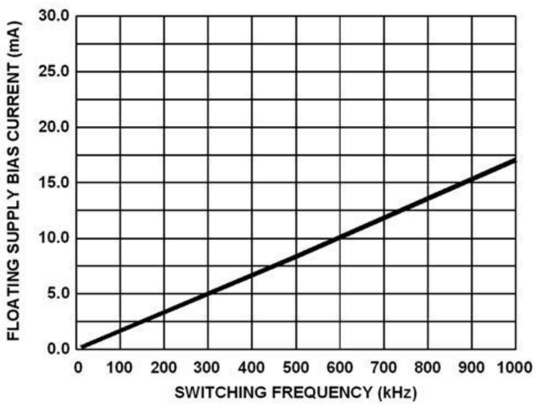


FIGURE 6. SIDE A, B FLOATING SUPPLY BIAS CURRENT vs FREQUENCY (LOAD = 1000pF)

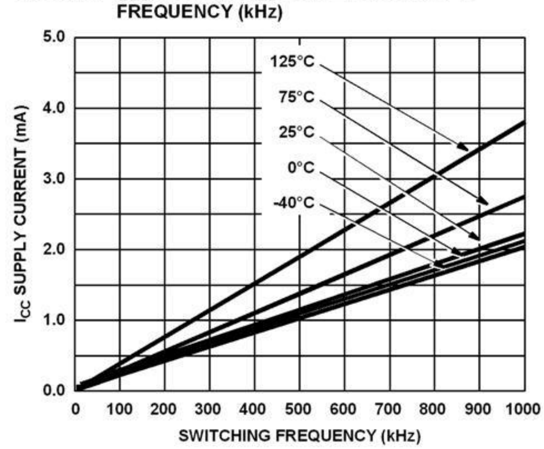


FIGURE 7. I_{CCO}, NO-LOAD I_{CC} SUPPLY CURRENT vs FREQUENCY (kHz) TEMPERATURE

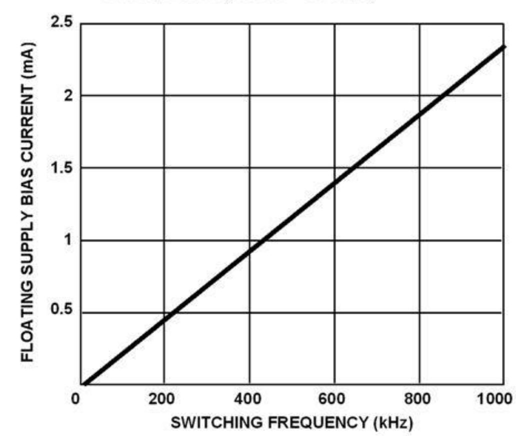


FIGURE 8. I_{AHB}, I_{BHB}, NO-LOAD FLOATING SUPPLY BIAS CURRENT vs FREQUENCY

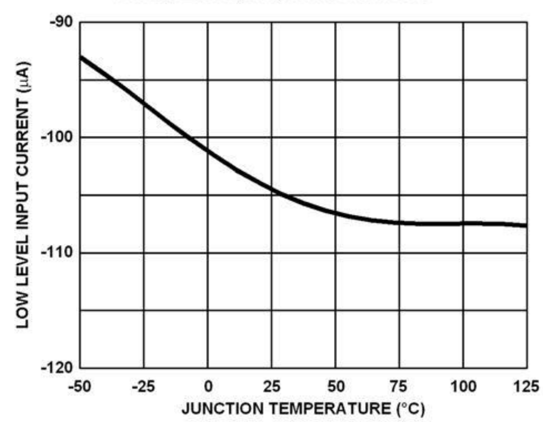


FIGURE 9. ALI, BLI, AHI, BHI LOW LEVEL INPUT CURRENT I_{IL} vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$ and $T_A = 25°C$, Unless Otherwise Specified

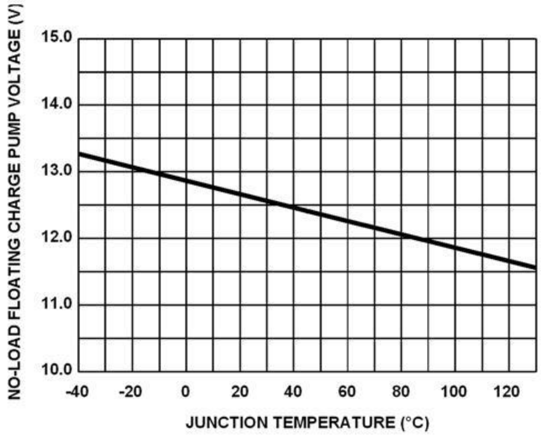


FIGURE 10. AHB - AHS, BHB - BHS NO-LOAD CHARGE PUMP VOLTAGE vs TEMPERATURE

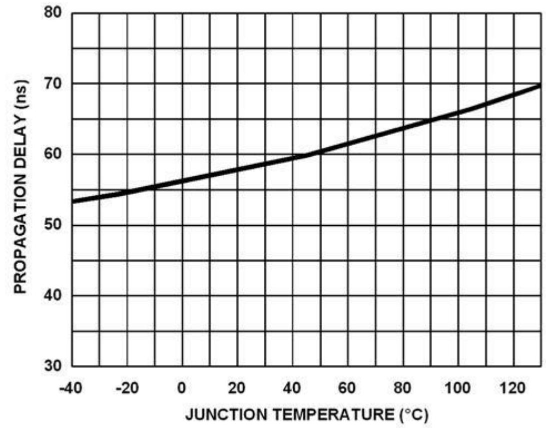


FIGURE 11. UPPER DISABLE TURN-OFF PROPAGATION DELAY $T_{DISHIGH}$ vs TEMPERATURE

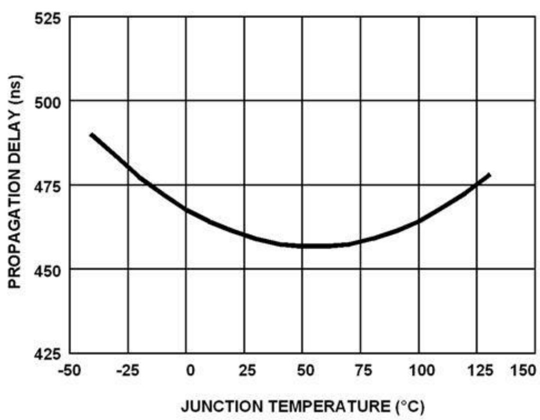


FIGURE 12. DISABLE TO UPPER ENABLE, T_{UEN}, PROPAGATION DELAY vs TEMPERATURE

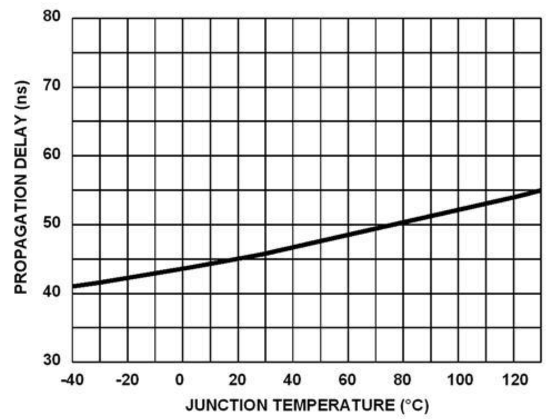


FIGURE 13. LOWER DISABLE TURN-OFF PROPAGATION DELAY T_{DISLOW} vs TEMPERATURE

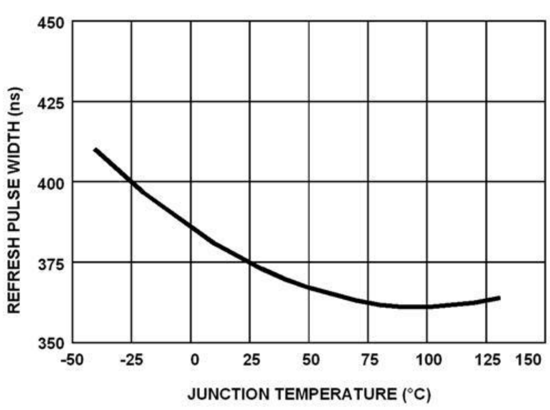


FIGURE 14. T_{REF-PW} REFRESH PULSE WIDTH vs TEMPERATURE

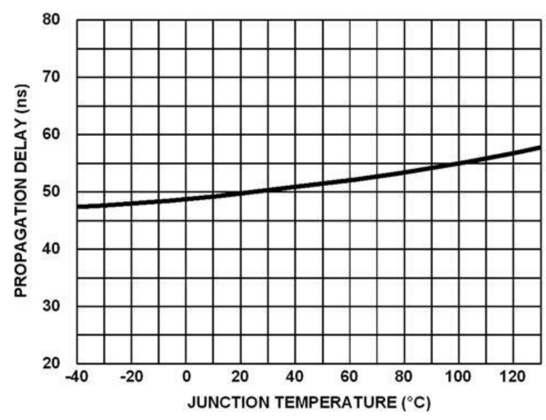


FIGURE 15. DISABLE TO LOWER ENABLE T_{DLPLH} PROPAGATION DELAY vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$ and $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

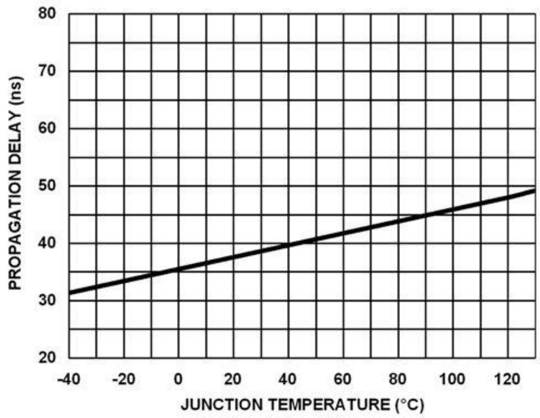


FIGURE 16. UPPER TURN-OFF PROPAGATION DELAY T_{HPHL} vs TEMPERATURE

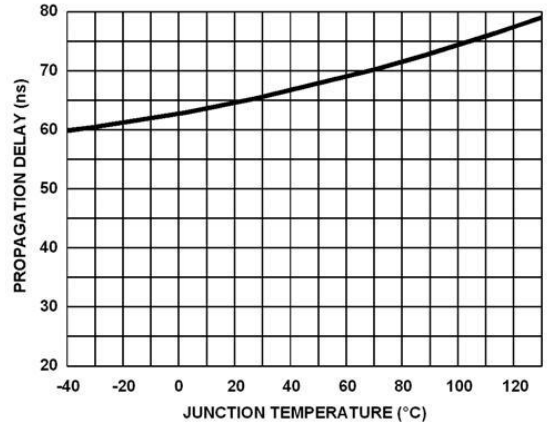


FIGURE 17. UPPER TURN-ON PROPAGATION DELAY T_{HPLH} vs TEMPERATURE

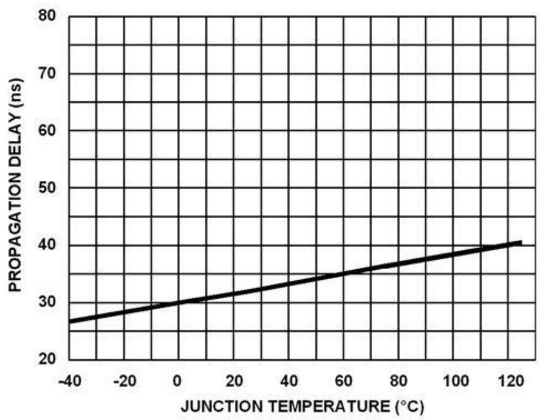


FIGURE 18. LOWER TURN-OFF PROPAGATION DELAY T_{LPHL} vs TEMPERATURE

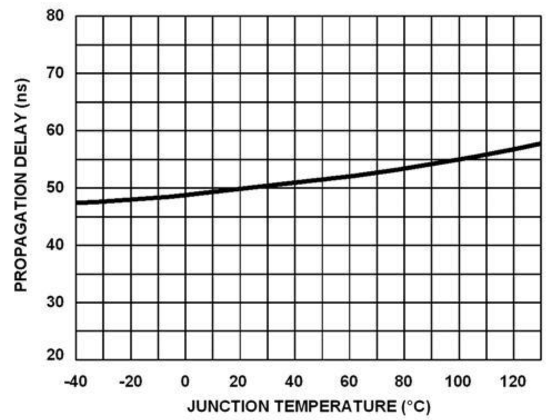


FIGURE 19. LOWER TURN-ON PROPAGATION DELAY T_{LPLH} vs TEMPERATURE

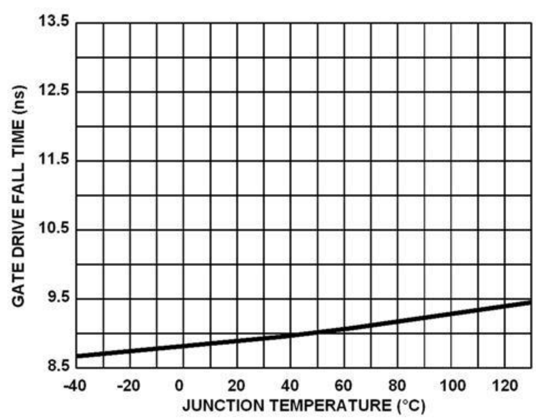


FIGURE 20. GATE DRIVE FALL TIME T_F vs TEMPERATURE

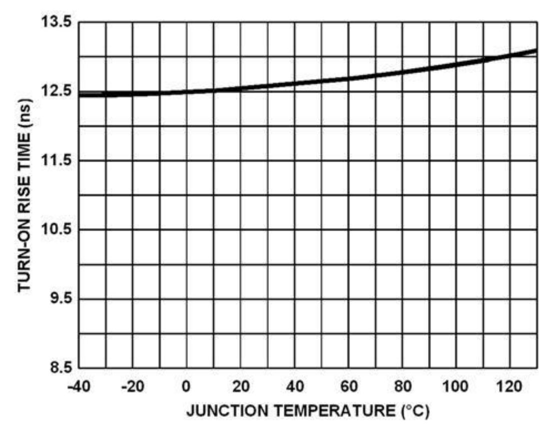


FIGURE 21. GATE DRIVE RISE TIME T_R vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 100K and $T_A = 25°C$, Unless Otherwise Specified

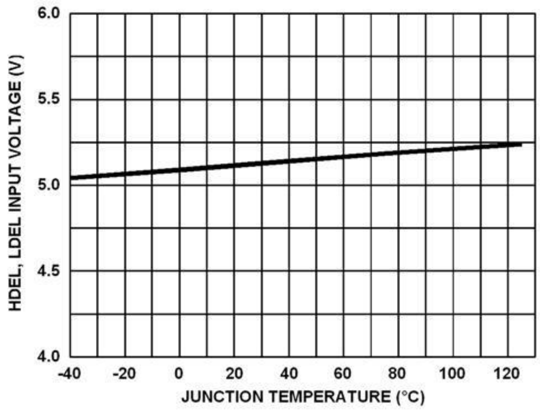


FIGURE 22. V_{LDEL}, V_{HDEL} VOLTAGE vs TEMPERATURE

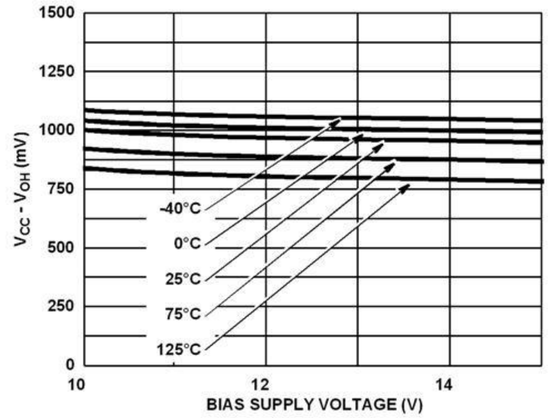


FIGURE 23. HIGH LEVEL OUTPUT VOLTAGE V_{CC} - V_{OH} vs BIAS SUPPLY AND TEMPERATURE AT 100mA

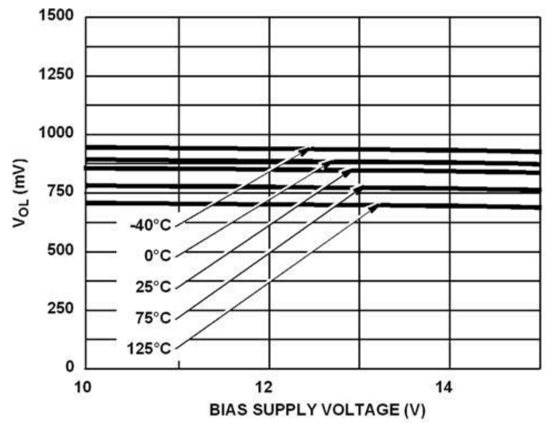


FIGURE 24. LOW LEVEL OUTPUT VOLTAGE V_{OL} vs BIAS SUPPLY AND TEMPERATURE AT 100mA

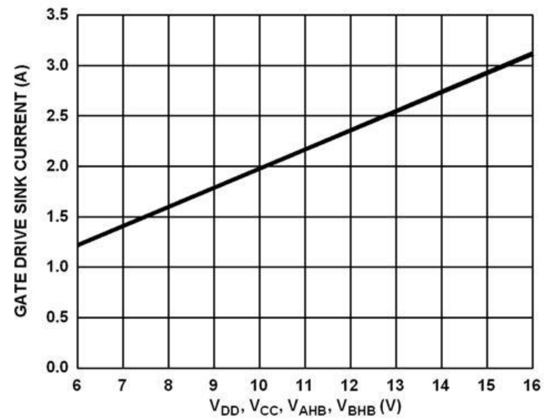


FIGURE 25. PEAK PULLDOWN CURRENT I_O vs BIAS SUPPLY VOLTAGE

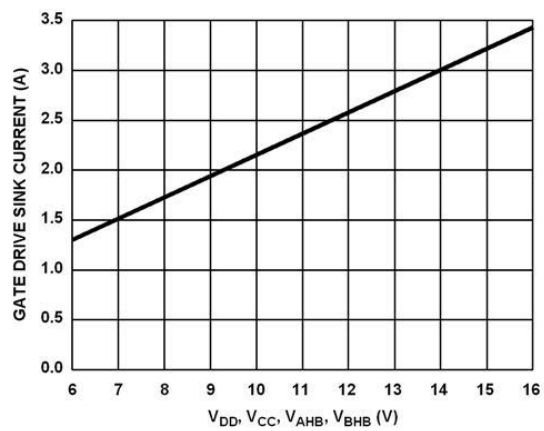


FIGURE 26. PEAK PULLUP CURRENT I_{O+} vs BIAS SUPPLY VOLTAGE

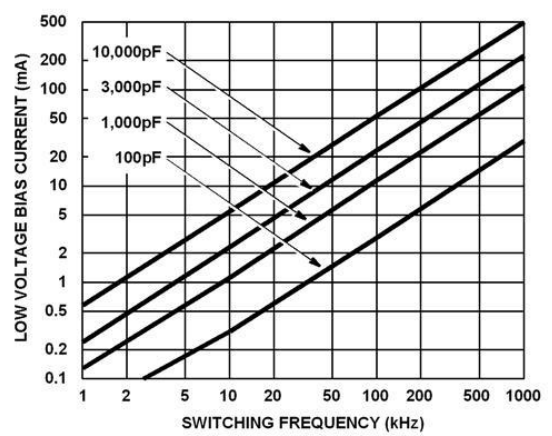


FIGURE 27. LOW VOLTAGE BIAS CURRENT I_{DD} (LESS QUIESCENT COMPONENT) vs FREQUENCY AND GATE LOAD CAPACITANCE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$ and $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

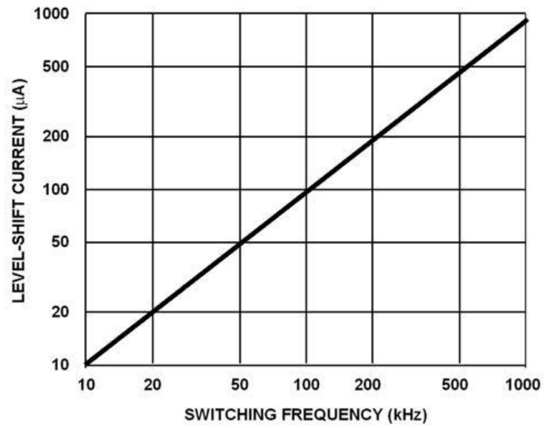


FIGURE 28. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

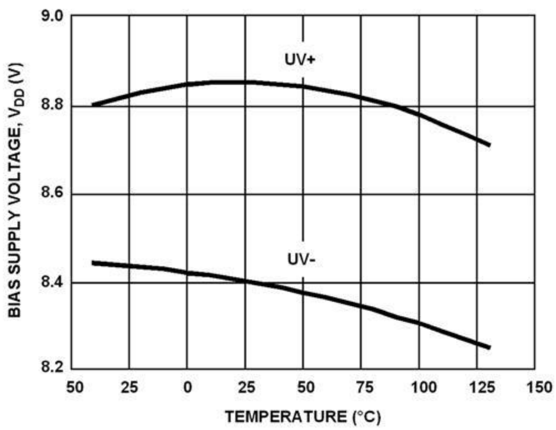


FIGURE 29. UNDERVOLTAGE LOCKOUT vs TEMPERATURE

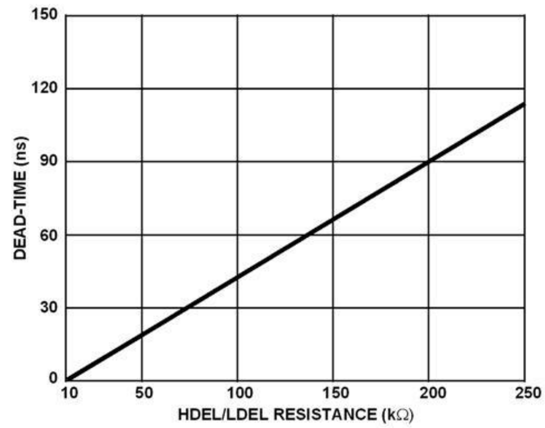
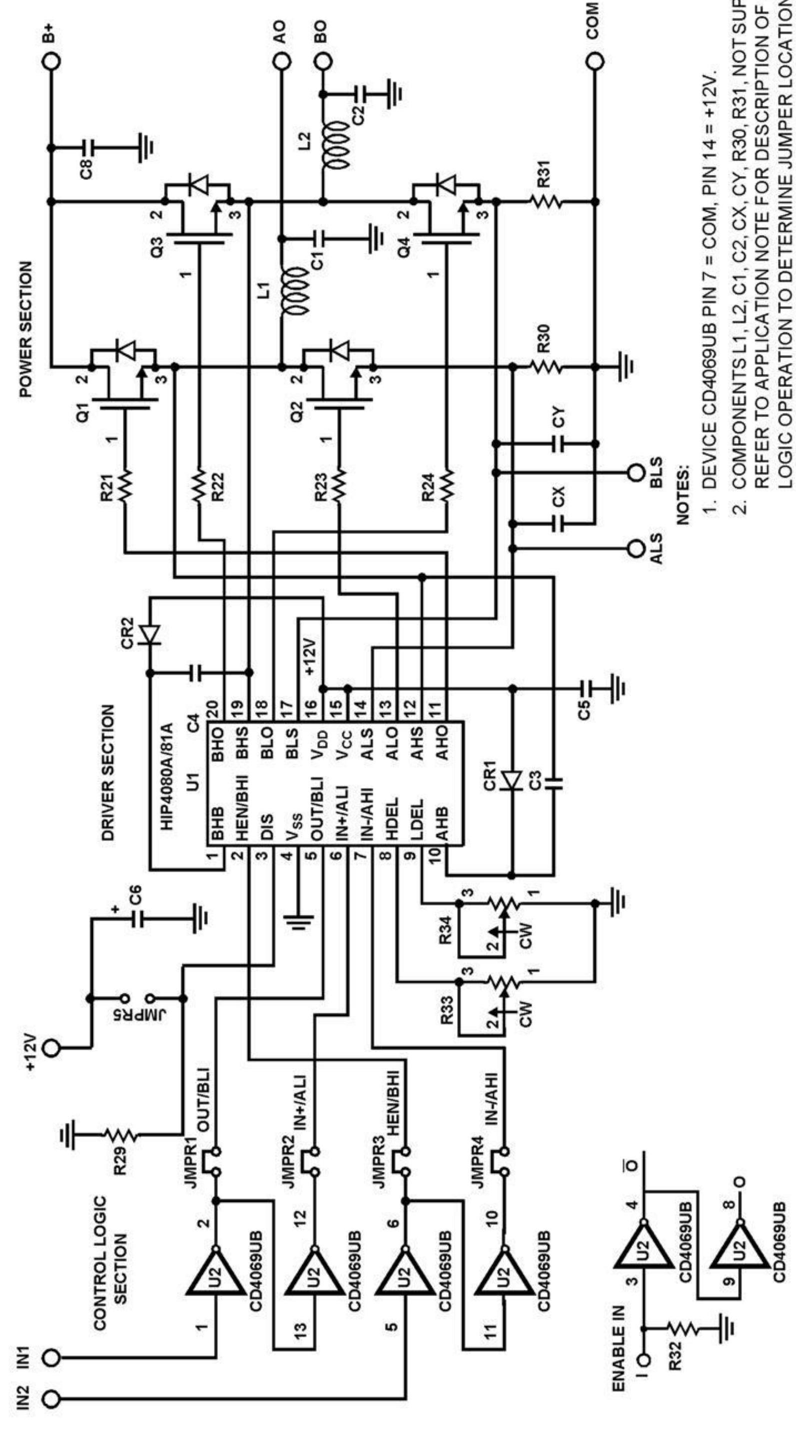


FIGURE 30. MINIMUM DEAD-TIME vs DEL RESISTANCE



NOTES:

1. DEVICE CD4069UB PIN 7 = COM, PIN 14 = +12V.
2. COMPONENTS L1, L2, C1, C2, CX, CY, R30, R31, NOT SUPPLIED. REFER TO APPLICATION NOTE FOR DESCRIPTION OF INPUT LOGIC OPERATION TO DETERMINE JUMPER LOCATIONS FOR JMPR1 - JMPR4.

FIGURE 31. HIP4081A EVALUATION PC BOARD SCHEMATIC

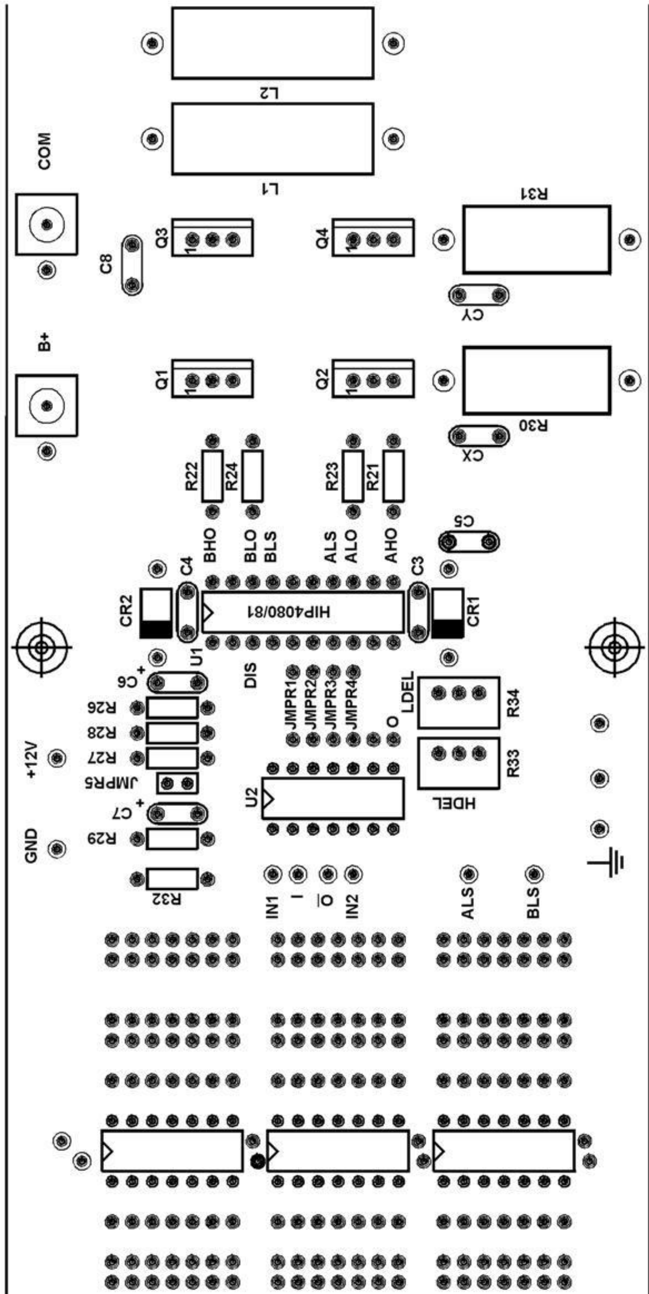
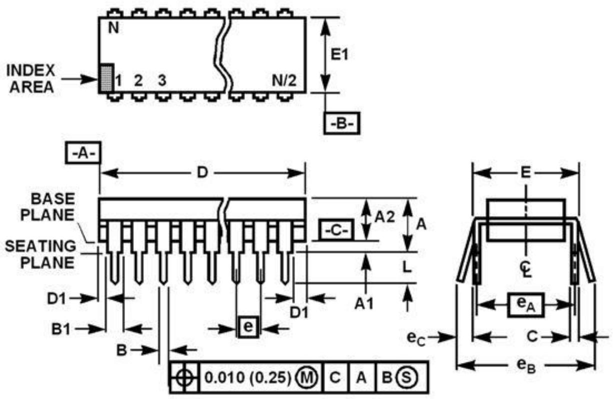


FIGURE 32. HIP4081A EVALUATION BOARD SILKSCREEN

Dual-In-Line Plastic Packages (PDIP)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

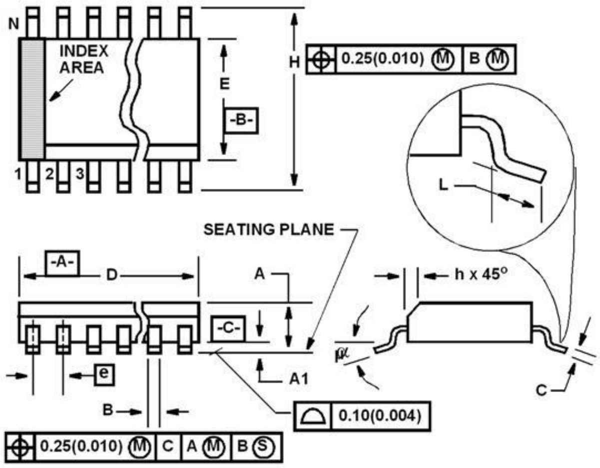
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.014	0.019	0.35	0.49	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 1 1/02

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation’s quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

ZXMN4A06G

40V N-CHANNEL ENHANCEMENT MODE MOSFET

SUMMARY

$V_{(BR)DSS}=40V$; $R_{DS(ON)}=0.05\Omega$; $I_D=7A$

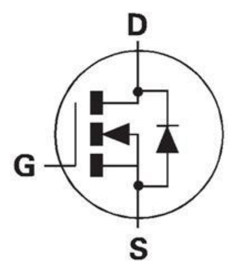
DESCRIPTION

This new generation of TRENCH MOSFETs from Zetex utilizes a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.

SOT223

FEATURES

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- SOT223 package

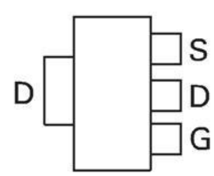


APPLICATIONS

- DC - DC Converters
- Audio Output Stages
- Relay and Solenoid driving
- Motor control

ORDERING INFORMATION

DEVICE	REEL SIZE	TAPE WIDTH	QUANTITY PER REEL
ZXMN4A06GTA	7″	12mm	1000 units
ZXMN4A06GTC	13″	12mm	4000 units



Top View

DEVICE MARKING

- ZXMN
  4A06

ZXMN4A06G

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DSS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current V_{GS}=10V; T_A=25°C(b) V_{GS}=10V; T_A=70°C(b) V_{GS}=10V; T_A=25°C(a)	I_D	7.0 5.6 5.0	A
Pulsed Drain Current (c)	I_{DM}	22	A
Continuous Source Current (Body Diode) (b)	I_S	5.4	A
Pulsed Source Current (Body Diode)(c)	I_{SM}	22	A
Power Dissipation at T_A=25°C (a) Linear Derating Factor	P_D	2.0 16	W mW/°C
Power Dissipation at T_A=25°C (b) Linear Derating Factor	P_D	3.9 31	W mW/°C
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient (a)	$R_{\theta JA}$	62.5	°C/W
Junction to Ambient (b)	$R_{\theta JA}$	32.2	°C/W

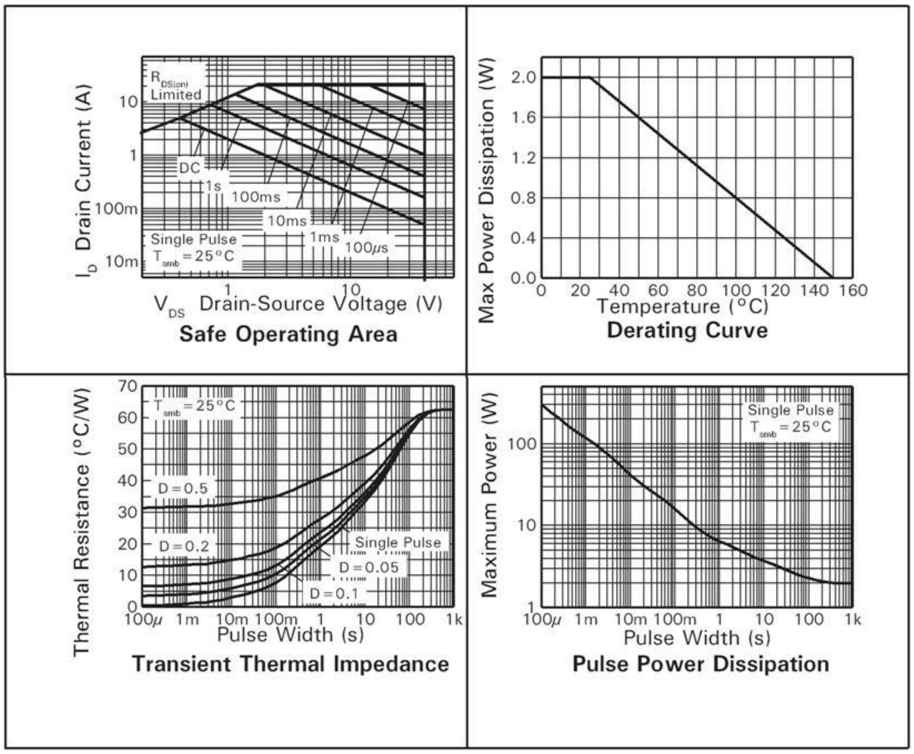
NOTES

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions

(b) For a device surface mounted on FR4 PCB measured at t≤5 secs.

(c) Repetitive rating 25mm x 25mm FRA PCB, D=0.05 pulse width =10µs - pulse width limited by maximum junction temperature.

CHARACTERISTICS



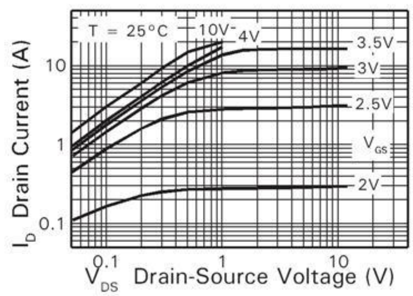
ZXMN4A06G

ELECTRICAL CHARACTERISTICS (at TA =25°C unless otherwise stated)

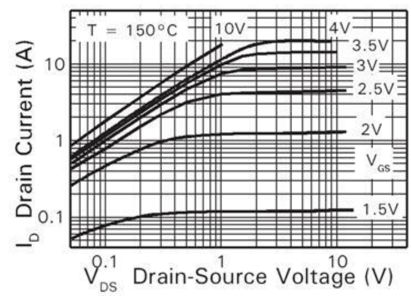
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	40			V	I_D=250μA, V_{GS}=0V
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS}=40V, V_{GS}=0V
Gate-Body Leakage	I_{GSS}			100	nA	V_{GS}=±20V, V_{DS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	1.0			V	I_D=250μA, V_{DS}=V_{GS}
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$			0.050 0.075	Ω Ω	V_{GS}=10V, I_D=4.5A V_{GS}=4.5V, I_D=3.2A
Forward Transconductance (3)	g_{fs}		8.7		S	V_{DS}=15V, I_D=2.5A
DYNAMIC (3)						
Input Capacitance	C_{iss}		770		pF	V_{DS}=40 V, V_{GS}=0V, f=1MHz
Output Capacitance	C_{oss}		92		pF	
Reverse Transfer Capacitance	C_{rss}		61		pF	
SWITCHING (2) (3)						
Turn-On Delay Time	$t_{d(on)}$		2.55		ns	V_{DD}=30V, I_D=2.5A R_G=6.0Ω, V_{GS}=10V (refer to test circuit)
Rise Time	t_r		4.45		ns	
Turn-Off Delay Time	$t_{d(off)}$		28.61		ns	
Fall Time	t_f		7.35		ns	
Total Gate Charge	Q_g		18.2		nC	V_{DS}=30V, V_{GS}=10V, I_D=2.5A (refer to test circuit)
Gate-Source Charge	Q_{gs}		2.1		nC	
Gate-Drain Charge	Q_{gd}		4.5		nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (1)	V_{SD}		0.8	0.95	V	T_J=25°C, I_S=2.5A, V_{GS}=0V
Reverse Recovery Time (3)	t_{rr}		19.86		ns	T_J=25°C, I_F=2.5A, di/dt=100A/μs
Reverse Recovery Charge (3)	Q_{rr}		16.36		nC	

NOTES
(1) Measured under pulsed conditions. Width≤300μs. Duty cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) For design aid only, not subject to production testing.

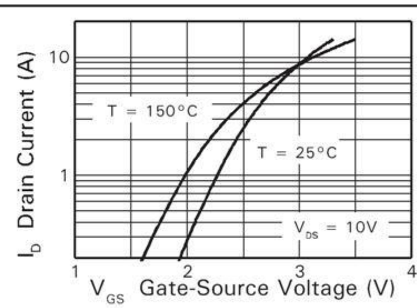
TYPICAL CHARACTERISTICS



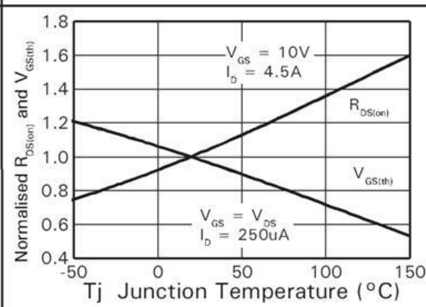
Output Characteristics



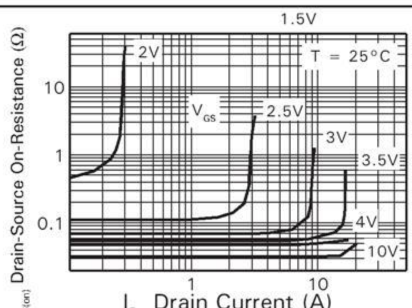
Output Characteristics



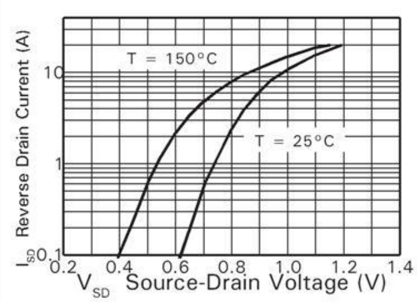
Typical Transfer Characteristics



Normalised Curves v Temperature

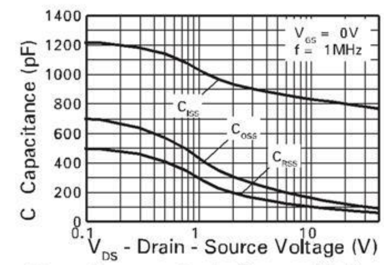


On-Resistance v Drain Current

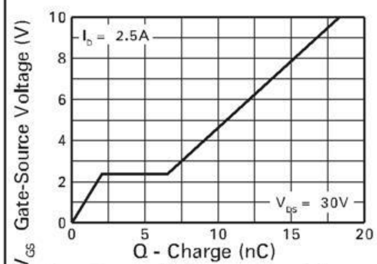


Source-Drain Diode Forward Voltage

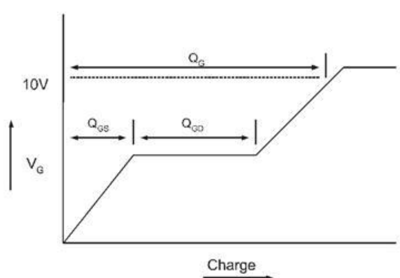
TYPICAL CHARACTERISTICS



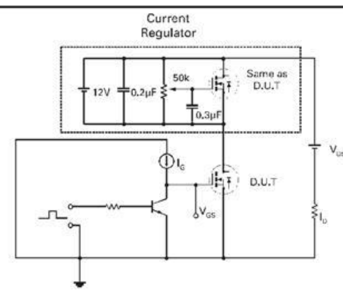
Capacitance v Drain-Source Voltage



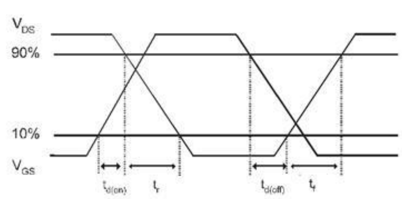
Gate-Source Voltage v Gate Charge



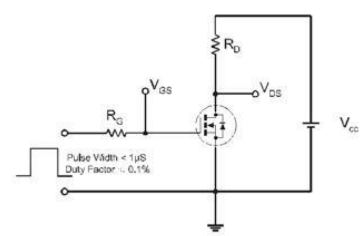
Basic Gate Charge Waveform



Gate Charge Test Circuit

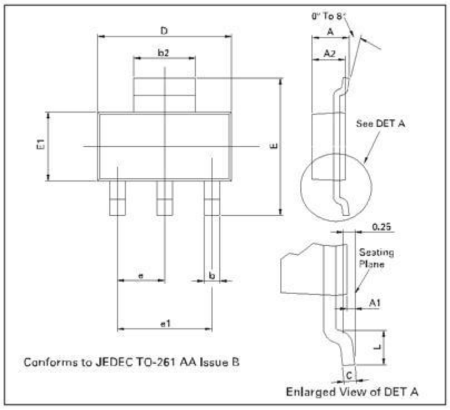


Switching Time Waveforms

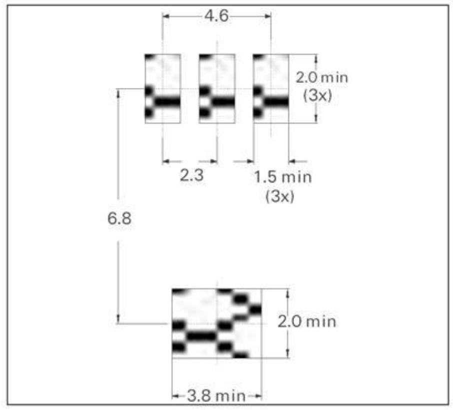


Switching Time Test Circuit

PACKAGE OUTLINE



PAD LAYOUT DETAILS



PACKAGE DIMENSIONS

DIM	MILLIMETRES		DIM	MILLIMETRES	
	MIN	MAX		MIN	MAX
A	—	1.80	D	6.30	6.70
A1	0.02	0.10	e	2.30 BASIC	
A2	1.55	1.65	e1	4.60 BASIC	
b	0.66	0.84	E	6.70	7.30
b2	2.90	3.10	E1	3.30	3.70
C	0.23	0.33	L	0.90	—

© Zetex plc 2002

Zetex plc
Fields New Road
Chadderton
Oldham, OL9 8NP
United Kingdom
Telephone (44) 161 622 4422
Fax: (44) 161 622 4420

Zetex GmbH
Streitfeldstraße 19
D-81673 München
Germany
Telefon: (49) 89 45 49 49 0
Fax: (49) 89 45 49 49 49

Zetex Inc
700 Veterans Memorial Hwy
Hauppauge, NY11788
USA
Telephone: (631) 360 2222
Fax: (631) 360 8222

Zetex (Asia) Ltd
3701-04 Metroplaza, Tower 1
Hing Fong Road
Kwai Fong
Hong Kong
Telephone: (852) 26100 611
Fax: (852) 24250 494

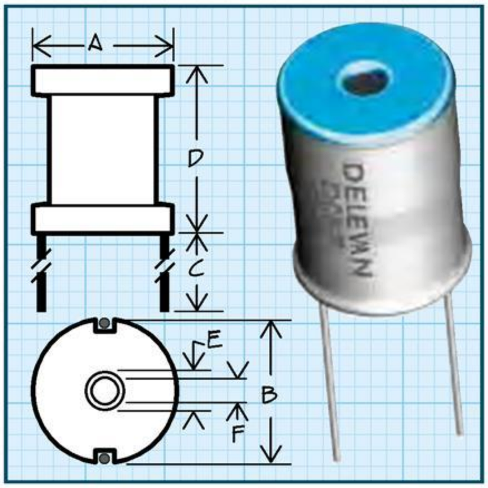
These offices are supported by agents and distributors in major countries world-wide.

This publication is issued to provide outline information only which (unless agreed by the Company in writing) may not be used, applied or reproduced for any purpose or form part of any order or contract or be regarded as a representation relating to the products or services concerned. The Company reserves the right to alter without notice the specification, design, price or conditions of supply of any product or service.

For the latest product information, log on to **www.zetex.com**

Series **DC630R** RoHS Compliant
DC630 Traditional First Quality

High Current Power Line Chokes



Physical Parameters

	Inches	Millimeters
A	0.630 ± 0.030	16.0 ± 0.762
B (C/L to C/L)	See Characteristics table	
C	0.750 Min.	19.05 Min.
D	0.810 ± 0.020	20.57 ±0.508
E (Ref. only)	0.195 Max.	4.95 Max.
F	Clearance Hole for 4/40 Screw	

Leads Tinned to within 1/16" of Body

Inductance
Measured @ 10 KHz, 25mAdc and 0 Adc @ 25°C

Mechanical Configuration Insulated Ferrite Bobbin protected with a flame retardant polyolefin sleeve; Center hole allows for mechanical mounting

Operating Temperature
–55°C to +125°C;
–55°C to +80°C @ full rated current

Current Rating at 80°C Ambient 45°C Rise

Incremental Current Minimum current which causes a 5% max. change in Inductance

Power Dissipation at 80°C 1.00 Watts Max.

Dielectric Withstanding Voltage 1000 V RMS Min.

Marking Parts printed with DELEVAN and API Part Number

Packaging Bulk only

DASH NUMBER*	NOMINAL INDUCTANCE (µH)	TOLERANCE	DC RESISTANCE MAX. (OHMS) @ 25°C	CURRENT RATING MAXIMUM (A DC)	INCREMENTAL CURRENT (A DC)	DIMENSION B (Approx. Inches)	LEAD DIAMETER (Inches)
SERIES DC630							
-102M	1.0	± 20%	0.003	14.00	68.0	0.490	0.051
-152M	1.5	± 20%	0.004	13.50	55.5	0.490	0.051
-222M	2.2	± 20%	0.005	12.80	46.0	0.490	0.051
-272M	2.7	± 20%	0.005	12.80	42.0	0.490	0.051
-332M	3.3	± 20%	0.005	12.80	38.0	0.490	0.051
-392M	3.9	± 20%	0.006	12.30	34.5	0.490	0.051
-472M	4.7	± 20%	0.007	11.70	31.5	0.490	0.051
-562M	5.6	± 20%	0.007	11.70	29.0	0.490	0.051
-682M	6.8	± 20%	0.008	10.50	26.0	0.490	0.051
-822M	8.2	± 20%	0.009	10.00	24.0	0.490	0.051
-103K	10.0	± 10%	0.010	9.50	21.5	0.490	0.051
-123K	12.0	± 10%	0.011	9.10	19.5	0.490	0.051
-153K	15.0	± 10%	0.015	8.09	17.5	0.470	0.045
-183K	18.0	± 10%	0.020	7.00	16.0	0.460	0.040
-223K	22.0	± 10%	0.025	6.26	14.5	0.460	0.040
-273K	27.0	± 10%	0.030	5.72	13.2	0.440	0.036
-333K	33.0	± 10%	0.040	4.95	11.9	0.430	0.032
-393K	39.0	± 10%	0.050	4.43	10.9	0.420	0.029
-473K	47.0	± 10%	0.062	3.98	10.0	0.480	0.029
-563K	56.0	± 10%	0.069	3.77	9.20	0.480	0.029
-683K	68.0	± 10%	0.077	3.57	8.30	0.480	0.029
-823K	82.0	± 10%	0.083	3.44	7.60	0.480	0.029
-104K	100	± 10%	0.095	3.21	6.80	0.480	0.029
-124K	120	± 10%	0.100	3.12	6.20	0.480	0.029
-154K	150	± 10%	0.111	2.97	5.60	0.480	0.029
-184K	180	± 10%	0.125	2.80	5.10	0.480	0.029
-224K	220	± 10%	0.168	2.42	4.60	0.470	0.025
-274K	270	± 10%	0.225	2.09	4.20	0.450	0.023
-334K	330	± 10%	0.315	1.72	3.80	0.450	0.020
-394K	390	± 10%	0.342	1.66	3.40	0.480	0.020
-474K	470	± 10%	0.377	1.58	3.10	0.480	0.020
-564K	560	± 10%	0.408	1.52	2.90	0.480	0.020
-684K	680	± 10%	0.468	1.42	2.60	0.480	0.020

***Complete part # must include series # PLUS the dash #**

For further surface finish information, refer to TECHNICAL section of this catalog.

POWER INDUCTORS

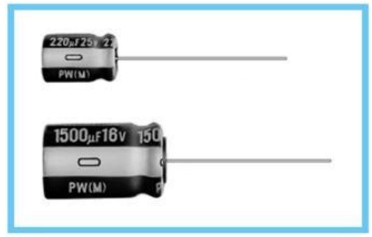
www.delevan.com E-mail: apisales@delevan.com
270 Quaker Rd., East Aurora NY 14052 • Phone 716-652-3600 • Fax 716-652-4814

API Delevan® American Precision Industries

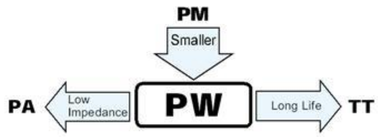
PW series

Miniature Sized, Low Impedance, High Reliability For Switching Power Supplies

Smaller | Low Impedance | Long Life | Anti-Solvent Feature (Through 100V only)



- Smaller case size and lower impedance than PM series.
- Low impedance and high reliability withstanding 2000 hours to 8000 hours.
- Capacitance ranges available based on the numerical values in E12 series under JIS.
- Adapted to the RoHS directive (2002/95/EC).



■Specifications

Item	Performance Characteristics
Category Temperature Range	−55 to +105°C (6.3 to 100V), −40 to + 105°C (160 to 400V), −25 to +105°C (450V)
Rated Voltage Range	6.3 to 450V
Rated Capacitance Range	0.47 to 15000μF
Capacitance Tolerance	±20% at 120Hz, 20°C
Leakage Current	see table below
tan δ	see table below
Stability at Low Temperature	see table below
Endurance	After an application of D.C. bias voltage plus the rated ripple current for 8000 hours (2000 hours for D = 4, 5 and 6.3, 3000 hours for D = 8, 5000 hours for D = 10, 7000 hours for D = 12.5) at 105°C the peak voltage shall not exceed the rated D.C.voltage, capacitors meet the characteristic requirements listed at right.
Shelf Life	After storing the capacitors under no load at 105°C for 1000 hours, and after performing voltage treatment based on JIS C 5101-4 clause 4.1 at 20°C, they will meet the specified value for endurance characteristics listed above.
Marking	Printed with white color letter on dark brown sleeve.

Leakage Current

Rated voltage (V)	6.3 to 100	160 to 450
Leakage current	After 1 minute's application of rated voltage, leakage current is not more than 0.03CV or 4 (μA), whichever is greater.	CV ≦ 1000 : I = 0.1CV+40 (μA) max. (1 minute's) CV > 1000 : I = 0.04CV+100 (μA) max. (1 minute's)

tan δ

For capacitance of more than 1000μF, add 0.02 for every increase of 1000μF. Measurement frequency : 120Hz, Temperature : 20°C

Rated voltage (V)	6.3	10	16	25	35	50	63	100	160 to 250	315 · 350	400 · 450
tan δ (MAX.)	0.22	0.19	0.16	0.14	0.12	0.10	0.09	0.08	0.15	0.20	0.25

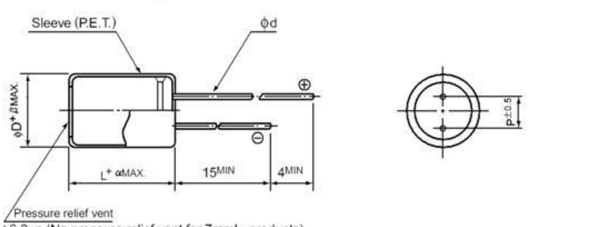
Stability at Low Temperature (120Hz)

Rated voltage (V)		6.3 · 10	16 · 25	35 · 50	63 · 100	160 · 200	250	315 · 350	400	450
Impedance ratio (MAX.)	Z−25°C / Z+20°C	—	—	—	—	3	3	4	6	15
	Z−40°C / Z+20°C	—	—	—	—	4	6	8	10	—
	Z−55°C / Z+20°C	3	3	3	3	—	—	—	—	—

Endurance

Capacitance change	Within ±20% of initial value
tan δ	200% or less of initial specified value
Leakage current	Initial specified value or less

■Radial Lead Type



ϕ6.3up (No pressure relief vent for 7mmL products)

α	
	(L = 7) 1.0
	(L < 20) 1.5
	(L ≥ 20) 2.0

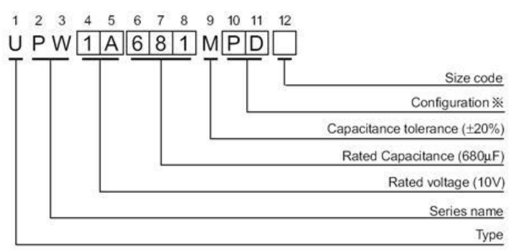
(mm)

ϕD	4	5	6.3	8	10	12.5	16	18	20	22	25
P	1.5	2.0	2.5	3.5	5.0	5.0	7.5	7.5	10.0	10.0	12.5
ϕd	0.45	0.5 (0.45)	0.5 (0.45)	0.6	0.6	0.6 ※0.8	0.8	0.8	1.0	1.0	1.0
β	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	1.0	1.0

※: Applied to L>25 products
( ): Applied to 7mmL products

• Please refer to page 20 about the end seal configulation.

Type numbering system (Example : 10V 680μF)



※ Configuration

ϕD	Pb-free leadwire Pb-free PET sleeve
4 · 5	DD
6.3	ED (7mm L : DD)
8 · 10	PD
12.5 to 18	HD
20 to 25	RD

●Frequency coefficient of rated ripple current

V	Cap. (μF) \ Frequency	50Hz	120Hz	300Hz	1kHz	10kHz or more
6.3 to 100	Less than 56	0.20	0.30	0.50	0.80	1.00
	68 to 330	0.55	0.65	0.75	0.85	1.00
	390 to 1000	0.70	0.75	0.80	0.90	1.00
	1200 to 15000	0.80	0.85	0.90	0.95	1.00
160 to 450	0.47 to 220	0.80	1.00	1.25	1.40	1.60
	330 to 470	0.90	1.00	1.10	1.13	1.15

Please refer to page 20, 21, 22 about the formed or taped product spec.
Please refer to page 4 for the minimum order quantity.
●Dimension table in next page.

PW series

■Standard ratings

Cap.(µF)	Code	6.3 (0J) Case size ϕD × L (mm)	6.3 (0J) Impedance (Ω) MAX. 20°C / 100kHz	6.3 (0J) Impedance (Ω) MAX. −10°C / 100kHz	6.3 (0J) Rated ripple (mArms) 105°C / 100kHz	10 (1A) Case size ϕD × L (mm)	10 (1A) Impedance (Ω) MAX. 20°C / 100kHz	10 (1A) Impedance (Ω) MAX. −10°C / 100kHz	10 (1A) Rated ripple (mArms) 105°C / 100kHz
22	220	5 × 11	0.60	1.20	180	5 × 11 ▲4 × 7	0.60 2.00	1.20 5.00	180 65
27	270	4 × 7	2.00	5.00	65				
33	330	5 × 11 ▲5 × 7	0.60 0.95	1.20 2.40	180 120	5 × 11 ▲5 × 7	0.60 0.95	1.20 2.40	180 120
39	390					5 × 7	0.95	2.40	120
47	470	5 × 11 ▲5 × 7	0.60 0.95	1.20 2.40	180 120	5 × 11 ▲4 × 11	0.60 1.30	1.20 2.60	180 120
56	560	5 × 7	0.95	2.40	120				
68	680	4 × 11	1.30	2.60	120				
82	820					5 × 11 ▲6.3 × 7	0.60 0.45	1.20 1.20	180 200
100	101	5 × 11	0.60	1.20	180	5 × 11 ▲5 × 15	0.60 0.50	1.20 1.00	180 235
120	121	6.3 × 7	0.45	1.20	200				
150	151	6.3 × 11 ▲5 × 15	0.25 0.50	0.50 1.00	290 235	6.3 × 11	0.25	0.50	290
180	181					6.3 × 11	0.25	0.50	290
220	221	6.3 × 11	0.25	0.50	290	6.3 × 11 ▲6.3 × 15	0.25 0.23	0.50 0.46	290 430
330	331	6.3 × 11 ▲6.3 × 15	0.25 0.23	0.50 0.46	290 430	8 × 11.5	0.117	0.234	555
470	471	8 × 11.5	0.117	0.234	555	8 × 11.5	0.117	0.234	555
560	561	8 × 11.5	0.117	0.234	555				
680	681	10 × 12.5	0.090	0.18	755	10 × 12.5 ▲8 × 15	0.090 0.085	0.18 0.17	760 730
820	821	8 × 15 ▲10 × 12.5	0.085 0.090	0.17 0.18	730 755				
1000	102	10 × 12.5	0.090	0.18	755	10 × 16 ▲8 × 20	0.068 0.065	0.136 0.13	1050 995
1200	122	8 × 20 ▲10 × 16	0.065 0.068	0.13 0.136	995 1050	10 × 20	0.052	0.104	1220
1500	152	10 × 20	0.052	0.104	1220	10 × 20 ▲10 × 25	0.052 0.045	0.104 0.090	1220 1440
2200	222	12.5 × 20 ▲10 × 25	0.038 0.045	0.076 0.090	1655 1440	12.5 × 20 ▲10 × 31.5	0.038 0.035	0.076 0.070	1655 1815
2700	272	10 × 31.5	0.035	0.070	1815	12.5 × 25	0.030	0.060	1945
3300	332	12.5 × 20	0.038	0.076	1655	12.5 × 25 ▲12.5 × 31.5	0.030 0.025	0.060 0.050	1950 2310
3900	392	12.5 × 25	0.030	0.060	1945	12.5 × 35.5 ▲16 × 20	0.022 0.029	0.044 0.058	2510 2210
4700	472	16 × 25 ▲12.5 × 31.5	0.022 0.025	0.044 0.050	2555 2310	16 × 25	0.022	0.044	2555
5600	562	12.5 × 35.5 ▲16 × 20	0.022 0.029	0.044 0.058	2510 2210	16 × 25 ▲18 × 20	0.022 0.028	0.044 0.056	2560 2490
6800	682	16 × 25 ▲18 × 20	0.022 0.028	0.044 0.056	2560 2490	16 × 31.5 ▲18 × 25	0.018 0.020	0.036 0.040	3010 2740
8200	822	16 × 31.5	0.018	0.036	3010	16 × 35.5 ▲18 × 31.5	0.016 0.016	0.032 0.032	3150 3635
10000	103	16 × 31.5 ▲18 × 25	0.016 0.020	0.032 0.040	3150 2740	18 × 35.5	0.015	0.030	3680
12000	123	18 × 31.5	0.016	0.032	3635				
15000	153	18 × 35.5	0.015	0.030	3680	18 × 40	0.014	0.028	3800

▲ : In this case, [6] will be put at 12th digit of type numbering system.

PW series

■Standard ratings

Cap. (μF)	Code	16 (1C) Case size φD × L (mm)	16 (1C) Impedance (Ω) MAX. 20°C / 100kHz	16 (1C) Impedance (Ω) MAX. −10°C / 100kHz	16 (1C) Rated ripple (mArms) 105°C / 100kHz	25 (1E) Case size φD × L (mm)	25 (1E) Impedance (Ω) MAX. 20°C / 100kHz	25 (1E) Impedance (Ω) MAX. −10°C / 100kHz	25 (1E) Rated ripple (mArms) 105°C / 100kHz
4.7	4R7					5 × 11	0.60	1.20	180
10	100	5 × 11	0.60	1.20	180	5 × 11	0.60	1.20	180
						▲4 × 7	2.00	5.00	65
15	150	4 × 7	2.00	5.00	65				
22	220	5 × 11	0.60	1.20	180	5 × 11	0.60	1.20	180
		▲5 × 7	0.95	2.40	120	▲5 × 7	0.95	2.40	120
27	270	5 × 7	0.95	2.40	120	4 × 11	1.30	2.60	120
33	330	5 × 11	0.60	1.20	180	5 × 11	0.60	1.20	180
		▲6.3 × 7	0.45	1.20	200				
39	390	4 × 11	1.30	2.60	120	5 × 11	0.60	1.20	180
						▲6.3 × 7	0.45	1.20	200
47	470	5 × 11	0.60	1.20	180	5 × 11	0.60	1.20	180
56	560	5 × 11	0.60	1.20	180	5 × 15	0.50	1.00	235
		▲6.3 × 7	0.45	1.20	200				
82	820	5 × 15	0.50	1.00	235	6.3 × 11	0.25	0.50	290
100	101	6.3 × 11	0.25	0.50	290	6.3 × 11	0.25	0.50	290
120	121	6.3 × 11	0.25	0.50	290	6.3 × 15	0.23	0.46	430
150	151	6.3 × 11	0.25	0.50	290	8 × 11.5	0.117	0.234	555
180	181	6.3 × 15	0.23	0.46	430				
220	221	8 × 11.5	0.117	0.234	555	8 × 11.5	0.117	0.234	555
330	331	8 × 11.5	0.117	0.234	555	10 × 12.5	0.090	0.18	760
						▲8 × 15	0.085	0.17	730
470	471	10 × 12.5	0.090	0.18	760	10 × 16	0.068	0.136	1050
		▲8 × 15	0.085	0.17	730	▲8 × 20	0.065	0.13	995
560	561					10 × 20	0.052	0.104	1220
680	681	10 × 16	0.068	0.136	1050	10 × 20	0.052	0.104	1220
		▲8 × 20	0.065	0.13	995				
820	821	10 × 20	0.052	0.104	1220	10 × 25	0.045	0.090	1440
1000	102	10 × 20	0.052	0.104	1220	12.5 × 20	0.038	0.076	1660
						▲10 × 31.5	0.035	0.070	1815
1200	122	10 × 25	0.045	0.090	1440				
1500	152	12.5 × 20	0.038	0.076	1655	16 × 25	0.022	0.044	2555
		▲10 × 31.5	0.035	0.070	1815	▲12.5 × 25	0.030	0.060	1950
1800	182					12.5 × 31.5	0.025	0.050	2310
						▲16 × 20	0.029	0.058	2210
2200	222	12.5 × 25	0.030	0.060	1945	16 × 25	0.022	0.044	2555
						▲18 × 20	0.028	0.056	2490
						※12.5 × 35.5	0.022	0.044	2510
2700	272	12.5 × 31.5	0.025	0.050	2310	16 × 25	0.022	0.044	2555
		▲16 × 20	0.029	0.058	2210				
3300	332	16 × 25	0.022	0.044	2555	16 × 31.5	0.018	0.036	3010
		▲12.5 × 35.5	0.022	0.044	2510	▲18 × 25	0.020	0.040	2740
3900	392	16 × 25	0.022	0.044	2560	16 × 35.5	0.016	0.032	3150
		▲18 × 20	0.028	0.056	2490	▲18 × 31.5	0.016	0.032	3635
4700	472	16 × 31.5	0.018	0.036	3010	18 × 35.5	0.015	0.030	3680
		▲18 × 25	0.020	0.040	2740				
5600	562	16 × 35.5	0.016	0.032	3150				
		▲18 × 31.5	0.016	0.032	3635				
6800	682	18 × 35.5	0.015	0.030	3680	18 × 40	0.014	0.028	3800
8200	822	18 × 35.5	0.015	0.030	3680				
10000	103	18 × 40	0.014	0.028	3800				

▲ : In this case, [6] will be put at 12th digit of type numbering system.
※ : In this case, [3] will be put at 12th digit of type numbering system.

PW series

■Standard ratings

Cap.(µF)	Code	35 (1V) Case size ϕD × L (mm)	35 (1V) Impedance (Ω) MAX. 20°C / 100kHz	35 (1V) Impedance (Ω) MAX. −10°C / 100kHz	35 (1V) Rated ripple (mArms) 105°C / 100kHz	50 (1H) Case size ϕD × L (mm)	50 (1H) Impedance (Ω) MAX. 20°C / 100kHz	50 (1H) Impedance (Ω) MAX. −10°C / 100kHz	50 (1H) Rated ripple (mArms) 105°C / 100kHz
0.47	R47					5 × 11	5.00	10.0	25
1	010					5 × 11	3.50	7.00	40
2.2	2R2					5 × 11	3.00	6.00	55
3.3	3R3					5 × 11	2.60	5.20	65
4.7	4R7	5 × 11	0.60	1.20	180	5 × 11	2.30	4.60	90
6.8	6R8	4 × 7	2.00	5.00	65				
10	100	5 × 11	0.60	1.20	180	5 × 11	1.40	2.80	120
		▲ 5 × 7	0.95	2.40	120	▲ 4 × 11	2.50	5.00	90
12	120	5 × 7	0.95	2.40	120				
18	180	4 × 11	1.30	2.60	120	5 × 11	1.30	2.60	155
22	220	5 × 11	0.60	1.20	180	5 × 11	1.20	2.40	170
27	270	5 × 11	0.60	1.20	180	5 × 15	0.90	1.80	215
		▲ 6.3 × 7	0.45	1.20	200				
33	330	5 × 11	0.60	1.20	180	6.3 × 11	0.43	0.86	300
39	390	5 × 15	0.50	1.00	235				
47	470	6.3 × 11	0.25	0.50	290	6.3 × 11	0.43	0.86	300
56	560	6.3 × 11	0.25	0.50	290	6.3 × 15	0.40	0.80	360
82	820	6.3 × 15	0.23	0.46	430	8 × 11.5	0.234	0.468	485
100	101	8 × 11.5	0.117	0.234	555	8 × 11.5	0.234	0.468	485
120	121					8 × 15	0.155	0.31	635
						▲ 10 × 12.5	0.162	0.324	620
150	151	8 × 11.5	0.117	0.234	555	10 × 12.5	0.162	0.324	615
180	181					8 × 20	0.120	0.240	860
						▲ 10 × 16	0.119	0.238	850
220	221	10 × 12.5	0.090	0.18	760	10 × 16	0.119	0.238	850
		▲ 8 × 15	0.085	0.17	730	▲ 10 × 20	0.090	0.18	1030
270	271					10 × 25	0.082	0.164	1200
330	331	10 × 16	0.068	0.136	1050	10 × 20	0.090	0.18	1030
		▲ 8 × 20	0.065	0.13	995	▲ 10 × 31.5	0.060	0.12	1610
390	391	10 × 20	0.052	0.104	1220	12.5 × 20	0.063	0.126	1480
470	471	10 × 20	0.052	0.104	1220	12.5 × 20	0.060	0.12	1500
560	561	10 × 25	0.045	0.090	1440	12.5 × 25	0.050	0.10	1832
680	681	12.5 × 20	0.038	0.076	1660	12.5 × 25	0.050	0.10	1840
		▲ 10 × 31.5	0.035	0.070	1815	▲ 16 × 20	0.048	0.096	1840
820	821					12.5 × 35.5	0.034	0.068	2290
						▲ 18 × 20	0.042	0.084	2420
1000	102	12.5 × 25	0.030	0.060	1950	16 × 25	0.034	0.068	2235
1200	122	12.5 × 31.5	0.025	0.050	2310	16 × 31.5	0.028	0.056	2700
		▲ 16 × 20	0.029	0.058	2210	▲ 18 × 25	0.029	0.058	2610
1500	152	16 × 25	0.022	0.044	2555	16 × 31.5	0.028	0.056	2700
		▲ 12.5 × 35.5	0.022	0.044	2510	▲ 16 × 35.5	0.025	0.050	2790
1800	182	16 × 25	0.022	0.044	2555	18 × 31.5	0.025	0.050	3000
		▲ 18 × 20	0.028	0.056	2490				
2200	222	16 × 31.5	0.018	0.036	3010	18 × 35.5	0.023	0.046	3100
		▲ 18 × 25	0.020	0.040	2740				
2700	272	16 × 35.5	0.016	0.032	3150				
		▲ 18 × 31.5	0.016	0.032	3635				
3300	332	18 × 35.5	0.015	0.030	3680				
4700	472	18 × 40	0.014	0.028	3800				

▲ : In this case, [6] will be put at 12th digit of type numbering system.

CAT.8100W

PW series

■Standard ratings

Cap(μF)	Code	63 (1J) Case size φD × L (mm)	63 (1J) Impedance (Ω) MAX. 20°C / 100kHz	63 (1J) Impedance (Ω) MAX. −10°C / 100kHz	63 (1J) Rated ripple (mArms) 105°C / 100kHz	100 (2A) Case size φD × L (mm)	100 (2A) Impedance (Ω) MAX. 20°C / 100kHz	100 (2A) Impedance (Ω) MAX. −10°C / 100kHz	100 (2A) Rated ripple (mArms) 105°C / 100kHz
0.47	R47					5 × 11	43.0	86.0	20
1	010					5 × 11	20.0	40.0	30
2.2	2R2					5 × 11	9.80	19.6	44
3.3	3R3					5 × 11	6.60	13.2	58
4.7	4R7	5 × 11	4.70	9.40	68	5 × 11	4.60	9.20	74
6.8	6R8	5 × 11 ▲4 × 11	2.50 3.50	5.00 7.00	95 80	5 × 11	3.50	7.00	95
10	100	5 × 11	2.10	4.20	110	6.3 × 11	1.80	3.60	130
12	120	5 × 11	2.00	4.00	145				
15	150	6.3 × 11	1.20	2.40	160	8 × 11.5	0.83	1.66	180
18	180	5 × 15	1.30	2.60	200	6.3 × 15	0.80	1.60	200
22	220	6.3 × 11	0.71	1.42	250	8 × 11.5	0.68	1.36	230
33	330	6.3 × 11	0.71	1.42	250	10 × 12.5 ▲8 × 15	0.46 0.45	0.92 0.90	320 360
39	390	6.3 × 15	0.70	1.40	330				
47	470	8 × 11.5	0.342	0.684	405	10 × 16 ▲8 × 20	0.37 0.37	0.74 0.74	420 420
68	680	8 × 11.5	0.342	0.684	405	10 × 20	0.30	0.60	490
82	820					10 × 25	0.25	0.50	540
100	101	10 × 12.5 ▲8 × 15	0.256 0.23	0.512 0.46	540 535	12.5 × 20	0.18	0.36	580
120	121	10 × 16	0.194	0.388	600				
150	151	10 × 16	0.194	0.388	660	12.5 × 25	0.13	0.26	710
180	181	10 × 20 ▲12.5 × 15	0.147 0.15	0.294 0.30	890 1020	12.5 × 31.5 ▲16 × 20	0.12 0.13	0.24 0.26	790 750
220	221	10 × 20 ▲10 × 25	0.147 0.13	0.294 0.26	885 1050	16 × 25 ▲18 × 20	0.10 0.11	0.20 0.22	890 850
270	271	16 × 15	0.090	0.18	1410				
330	331	12.5 × 20	0.085	0.17	1290	16 × 25	0.090	0.18	1080
390	391	12.5 × 25 ▲18 × 15	0.070 0.086	0.14 0.172	1720 1690	18 × 25	0.083	0.166	1260
470	471	12.5 × 25 ▲12.5 × 31.5 ※16 × 20	0.070 0.055 0.059	0.14 0.11 0.118	1720 2090 1770	16 × 31.5	0.076	0.152	1310
560	561					18 × 31.5	0.068	0.136	1370
680	681	16 × 25 ▲12.5 × 35.5 ※18 × 20	0.050 0.047 0.055	0.10 0.094 0.11	2160 2270 2290	16 × 35.5	0.064	0.128	1410
820	821	16 × 31.5 ▲18 × 25	0.043 0.043	0.086 0.086	2670 2590				
1000	102	16 × 31.5 ▲16 × 35.5	0.043 0.036	0.086 0.072	2770 2770	18 × 40	0.047	0.094	1520
1200	122	18 × 31.5	0.032	0.064	2950				
1500	152	18 × 35.5	0.030	0.060	3100				
2200	222	18 × 40	0.028	0.056	3200				

▲ : In this case, [6] will be put at 12th digit of type numbering system.
※ : In this case, [3] will be put at 12th digit of type numbering system.

Cap. (μF)	Code	160 (2C)		200 (2D)		250 (2E)		315 (2F)		350 (2V)		400 (2G)		450 (2W)	
0.47	R47	6.3 × 11	12	6.3 × 11	12	6.3 × 11	12	8 × 11.5	11	8 × 11.5	11				
1	010	6.3 × 11	17	6.3 × 11	17	6.3 × 11	17	8 × 11.5	16	10 × 12.5	17	10 × 12.5	16	10 × 12.5	18
2.2	2R2	6.3 × 11	25	6.3 × 11	25	8 × 11.5	29	10 × 12.5	28	10 × 16	31	10 × 16	27	10 × 20	29
3.3	3R3	8 × 11.5	36	8 × 11.5	36	10 × 12.5	42	10 × 12.5	34	10 × 16	38	10 × 20	36	12.5 × 20	41
4.7	4R7	8 × 11.5	43	10 × 12.5	50	10 × 12.5	50	10 × 16	45	10 × 20	49	10 × 20	43	12.5 × 20	49
10	100	10 × 12.5	70	10 × 16	80	10 × 20	88	10 × 20	72	12.5 × 20	82	12.5 × 25	72	16 × 25	75
22	220	10 × 20	130	10 × 20	140	12.5 × 25	155	12.5 × 25	120	16 × 25	130	16 × 25	110	16 × 31.5	115
33	330	12.5 × 20	180	12.5 × 25	190	12.5 × 25	190	16 × 25	155	16 × 31.5	160	16 × 31.5	140	•18 × 35.5	145
47	470	12.5 × 25	220	12.5 × 25	220	16 × 25	230	16 × 35.5	190	•18 × 35.5	200	•18 × 35.5	170	20 × 40	175
100	101	16 × 25	330	16 × 31.5	335	•18 × 35.5	340	Δ18 × 40	285	20 × 40	290	22 × 50	350	25 × 50	350
220	221	•18 × 35.5	500	Δ18 × 40	515	20 × 40	525	22 × 50	540	25 × 50	550				
330	331	20 × 40	900	22 × 40	1100	22 × 50	1150								
470	471	22 × 50	1200	22 × 50	1310	25 × 50	1350							Case size φD × L (mm)	※

※Rated Ripple (mArms) at 105°C 120Hz
Size 20 × 31 is available for capacitors marked "•"
Size 20 × 35 is available for capacitors marked "Δ"
In this case, [6] will be put at 12th digit of type numbering system.

CAT.8100W

Innovative Service Around the Globe **YAGEO**

DATA SHEET

GENERAL PURPOSE CHIP RESISTORS

RC1206 (Pb Free)

5%, 1%

Product specification – Sep 03, 2004 V.2

Phycomp

SCOPE

This specification describes RC1206 series chip resistors with lead-free terminations made by thick film process.

ORDERING INFORMATION

Part number is identified by the series, size, tolerance, packing type, temperature coefficient, taping reel and resistance value.

PHYCOMP ORDERING CODE

12NC CODE

2322 / 2350 XXX XXXXX L
(1) (2) (3) (4)

TYPE/ 1206	START IN [1]	TOL. (%)	RESISTANCE RANGE	PAPER / PE TAPE ON REEL (units) [2]		
				5,000	10,000/not preferred	20,000
RC01	2322	±5%	1 to 10 MΩ	711 61xxx	711 51xxx	711 81xxx
RC02	2322	±1%	1 to 10 MΩ	724 6xxxx	724 7xxxx	724 8xxxx
HRC01	2350	±5%	11 to 22 MΩ	520 10xxx	-	-
Jumper	2322	-	0 Ω	711 91032	711 91005	711 92004

(1) The resistors have a 12-digit ordering code starting with 2322/2350.

(2) The subsequent 4 or 5 digits indicate the resistor tolerance and packaging.

(3) The remaining 4 or 3 digits represent the resistance value with the last digit indicating the multiplier as shown in the table of "Last digit of 12NC".

(4) "L" means lead-free terminations.

Last digit of 12NC

Resistance decade [3]	Last digit
0.01 to 0.0976 Ω	0
0.1 to 0.976 Ω	7
1 to 9.76 Ω	8
10 to 97.6 Ω	9
100 to 976 Ω	1
1 to 9.76 kΩ	2
10 to 97.6 kΩ	3
100 to 976 kΩ	4
1 to 9.76 MΩ	5
10 to 97.6 MΩ	6

Example:			
	0.02 Ω	=	0200 or 200
	0.3 Ω	=	3007 or 307
	1 Ω	=	1008 or 108
	33 kΩ	=	3303 or 333
	10 MΩ	=	1006 or 106

ORDERING EXAMPLE

The ordering code of a RC02 resistor, value 56 Ω with ±1% tolerance, supplied in tape of 5,000 units per reel is: 232272465609L.

CTC CODE

RC1206 X X X XX XXXX L
(1) (2) (3) (4) (5) (6)

(1) TOLERANCE
- F = ±1%
- J = ±5%

(2) PACKAGING TYPE
- R = Paper/PE taping reel

(3) TEMPERATURE COEFFICIENT OF RESISTANCE
- – = Base on spec

(4) TAPING REEL
- 07 = 7 inch dia. Reel
- 10 = 10 inch dia. Reel (not preferred)
- 13 = 13 inch dia. Reel

(5) RESISTANCE VALUE
- 5R6, 56R, 560R, 5K6, 56K, 22M

(6) RESISTOR TERMINATIONS
- L = Lead free terminations (pure Tin)

ORDERING EXAMPLE

The ordering code of a RC1206 chip resistor, value 56 Ω with ±1% tolerance, supplied in 7-inch tape reel is: RC1206FR-0756RL.

NOTE

1. The "L" at the end of the code is only for ordering. On the reel label, the standard CTC or 12NC will be mentioned an additional stamp "LFP"= lead free production.
2. Products with lead in terminations fulfil the same requirements as mentioned in this datasheet.
3. Products with lead in terminations will be phased out in the coming months (before July 1st, 2006)

MARKING

RC1206

Fig. 1 Value=10 KΩ

E-24 series: 3 digits

First two digits for significant figure and 3rd digit for number of zeros

Fig. 2 Value=10 KΩ

Both E-24 and E-96 series: 4 digits

First three digits for significant figure and 4th digit for number of zeros

For marking codes, please see EIA-marking code rules in data sheet "Chip resistors instruction".

CONSTRUCTION

The resistors are constructed out of a high-grade ceramic body. Internal metal electrodes are added at each end and connected by a resistive paste. The composition of the paste is adjusted to give the approximate required resistance and laser cutting of this resistive layer that achieves tolerance trims the value. The resistive layer is covered with a protective coat and printed with the resistance value. Finally, the two external terminations (pure Tin) are added. See fig. 3.

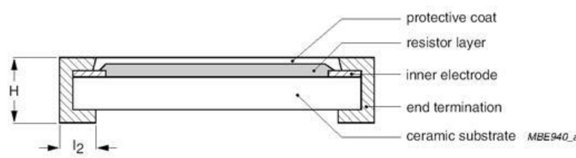


Fig. 3 Chip resistor construction

DIMENSIONS

Table 1

TYPE	RC1206
L (mm)	3.10 ±0.10
W (mm)	1.60 ±0.10
H (mm)	0.55 ±0.10
l_1 (mm)	0.45 ±0.20
l_2 (mm)	0.40 ±0.20

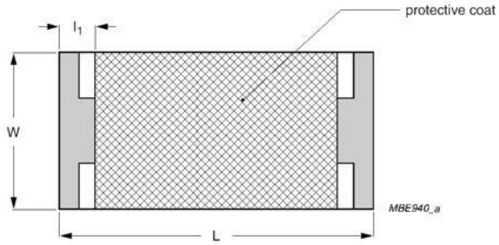


Fig. 4 Chip resistor dimension

For dimension see Table 1

ELECTRICAL CHARACTERISTICS

Table 2

CHARACTERISTICS		RC1206 1/4 W
Operating Temperature Range		–55 °C to +155 °C
Maximum Working Voltage		200 V
Maximum Overload Voltage		400 V
Dielectric Withstanding Voltage		500 V
Resistance Range	5% (E24)	1 Ω to 22 MΩ
	1% (E96)	1 Ω to 10 MΩ
		Zero Ohm Jumper < 0.05 Ω
Temperature Coefficient	10 Ω < R ≤ 10 MΩ	±100 ppm/°C
	R ≤ 10 Ω; R > 10 MΩ	±200 ppm/°C
Jumper Criteria	Rated Current	2.0 A
	Maximum Current	10.0 A

FOOTPRINT AND SOLDERING PROFILES

For recommended footprint and soldering profiles, please see the special data sheet "Chip resistors mounting".

ENVIRONMENTAL DATA

For material declaration information (IMDS-data) of the products, please see the separated info "Environmental data".

PACKING STYLE AND PACKAGING QUANTITY

Table 3 Packing style and packaging quantity

PRODUCT TYPE	PACKING STYLE	REEL DIMENSION	QUANTITY PER REEL
RC1206	Paper / PE Taping Reel (R)	7" (178 mm)	5,000 units
		10" (254 mm) / not preferred	10,000 units
		13" (330 mm)	20,000 units

NOTE

1. For Paper/PE tape and reel specification/dimensions, please see the special data sheet "Packing" document.

FUNCTIONAL DESCRIPTION

POWER RATING

RC1206 rated power at 70°C is 1/4 W

RATED VOLTAGE

The DC or AC (rms) continuous working voltage corresponding to the rated power is determined by the following formula:

$V=\sqrt{(P \times R)}$

Where

V=Continuous rated DC or AC (rms) working voltage (V)

P=Rated power (W)

R=Resistance value (Ω)

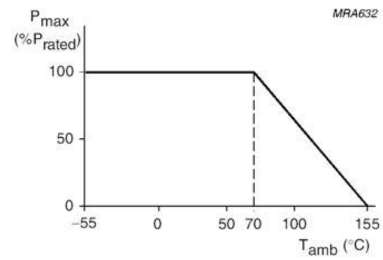


Fig. 5 Maximum dissipation (P_{max}) in percentage of rated power as a function of the operating ambient temperature (T_{amb})

PULSE LOADING CAPABILITIES

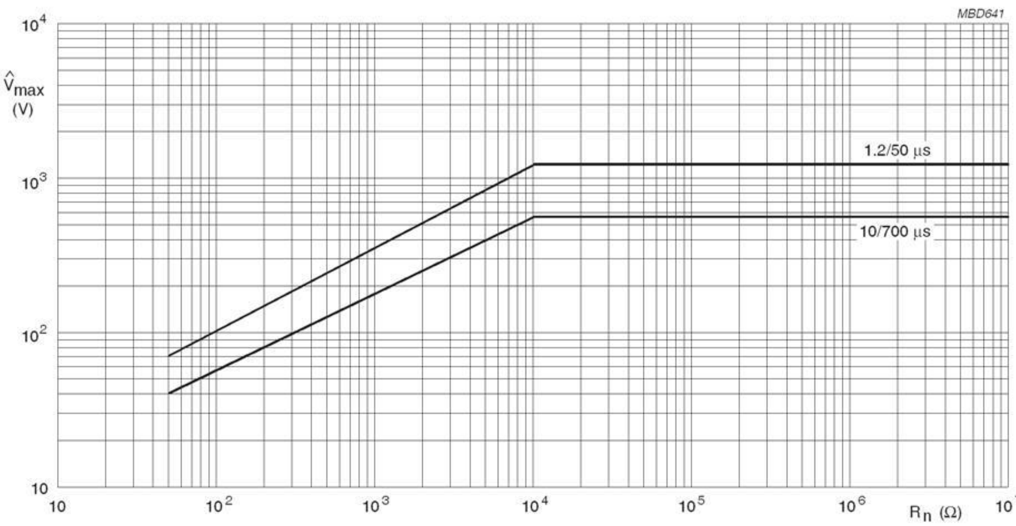


Fig. 6 Maximum permissible peak pulse voltage without failing to open circuit' in accordance with DIN IEC 60040 (CO) 533 for type: RC1206

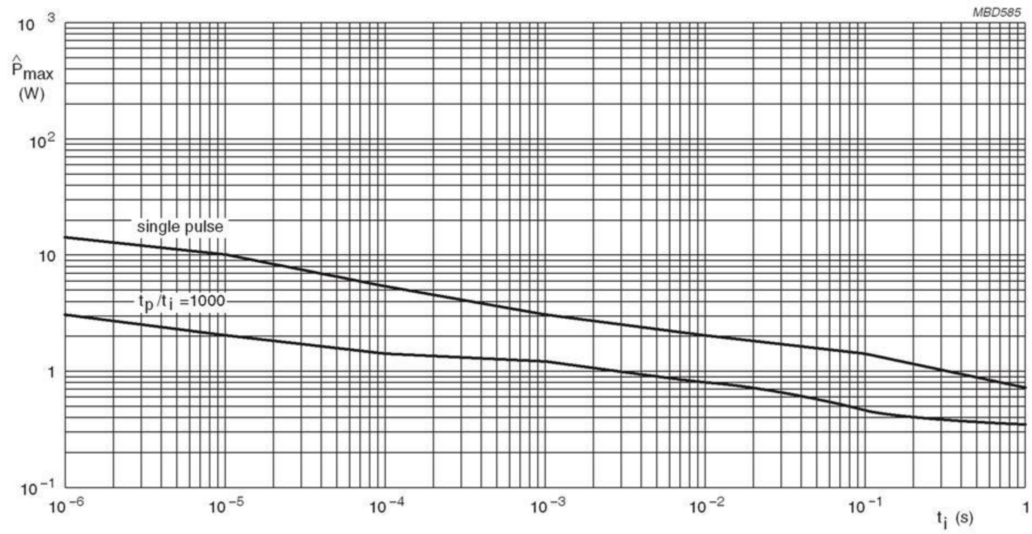


Fig. 7 Pulse on a regular basis for type: RC1206; maximum permissible peak pulse power as a function of pulse duration for single pulse and repetitive pulse tp/ti = 1000

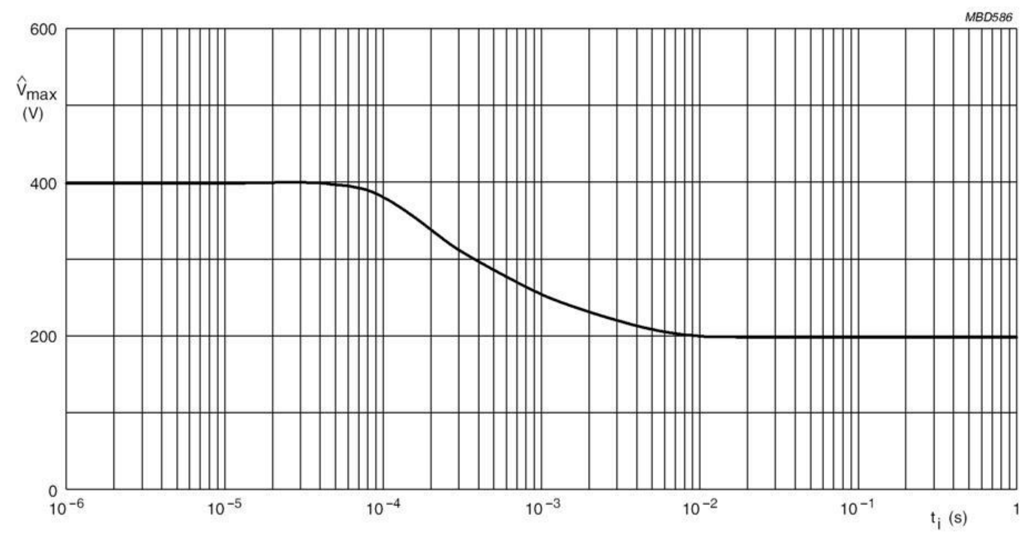


Fig. 8 Pulse on a regular basis for type: RC1206; maximum permissible peak pulse voltage as a function of pulse duration

TESTS AND REQUIREMENTS

Table 4 Test condition, procedure and requirements

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
Temperature Coefficient of Resistance (T.C.R.)	MIL-STD-202F-method 304; JIS C 5202-4.8	At +25/–55 °C and +25/+125 °C Formula: $T.C.R= \frac{R_2-R_1}{R_1(t_2-t_1)} \times 10^6$ (ppm/°C) Where t_1=+25 °C or specified room temperature t_2=–55 °C or +125 °C test temperature R_1=resistance at reference temperature in ohms R_2=resistance at test temperature in ohms	Refer to table 2
Thermal Shock	MIL-STD-202F-method 107G; IEC 60115-1 4.19	At –65 (+0/–10) °C for 2 minutes and at +155 (+10/–0) °C for 2 minutes; 25 cycles	±(0.5%+0.05 Ω) for 1% tol. ±(1.0%+0.05 Ω) for 5% tol.
Low Temperature Operation	MIL-R-55342D-Para 4.7.4	At –65 (+0/–5) °C for 1 hour; RCWV applied for 45 (+5/–0) minutes	±(0.5%+0.05 Ω) for 1% tol . ±(1.0%+0.05 Ω) for 5% tol. No visible damage
Short Time Overload	MIL-R-55342D-Para 4.7.5; IEC 60115-1 4.13	2.5 × RCWV applied for 5 seconds at room temperature	±(1.0%+0.05 Ω) for 1% tol. ±(2.0%+0.05 Ω) for 5% tol. No visible damage
Insulation Resistance	MIL-STD-202F-method 302; IEC 60115-1 4.6.1.1	RCOV for 1 minute Type: RC1206 Voltage (DC): 400 V	≥10 GΩ
Dielectric Withstand Voltage	MIL-STD-202F-method 301; IEC 60115-1 4.6.1.1	Maximun voltage (V_{rms}) applied for 1 minute Type: RC1206 Voltage (AC): 500 V_{rms}	No breakdown or flashover
Resistance to Soldering Heat	MIL-STD-202F-method 210C; IEC 60115-1 4.18	Unmounted chips; 260 ±5 °C for 10 ±1 seconds	±(0.5%+0.05 Ω) for 1% tol. ±(1.0%+0.05 Ω) for 5% tol. No visible damage
Life	MIL-STD-202F-method 108A; IEC 60115-1 4.25.1	At 70±2 °C for 1,000 hours; RCWV applied for 1.5 hours on and 0.5 hour off	±(1%+0.05 Ω) for 1% tol. ±(3%+0.05 Ω) for 5% tol.

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
Solderability	MIL-STD-202F-method 208A; IEC 60115-1 4.17	Solder bath at 245±3 °C Dipping time: 2±0.5 seconds	Well tinned (≥95% covered) No visible damage
Bending Strength	JIS C 5202.6.14; IEC 60115-1 4.15	Resistors mounted on a 90 mm glass epoxy resin PCB (FR4) Bending: 5 mm	±(1.0%+0.05 Ω) for 1% tol. ±(1.0%+0.05 Ω) for 5% tol. No visible damage
Resistance to Solvent	MIL-STD-202F-method 215; IEC 60115-1 4.29	Isopropylalcohol (C_3H_7OH) or dichloromethane (CH_2Cl_2) followed by brushing	No smeared
Noise	JIS C 5202 5.9; IEC 60115-1 4.12	Maximum voltage (V_{rms}) applied.	See table below
Humidity (steady state)	JIS C 5202 7.5; IEC 60115-8 4.24.8	1,000 hours; 40±2 °C; 93(+2/–3)% RH RCWV applied for 1.5 hours on and 0.5 hour off	±(0.5%+0.05 Ω) for 1% tol. ±(2.0%+0.05 Ω) for 5% tol.
Leaching	EIA/IS 4.13B; IEC 60115-8 4.18	Solder bath at 260±5 °C Dipping time: 30±1 seconds	No visible damage
Intermittent Overload	JIS C 5202 5.8	At room temperature; 2.5 × RCWV applied for 1 second on and 25 seconds off; total 10,000 cycles	±(1.0%+0.05 Ω) for 1% tol. ±(2.0%+0.05 Ω) for 5% tol.
Resistance to Vibration	On request	On request	
Moisture Resistance Heat	MIL-STD-202F-method 106F; IEC 60115-1 4.24.2	42 cycles; total 1,000 hours Shown as figure 9	±(0.5%+0.05Ω) for 1% tol. ±(2.0%+0.05Ω) for 5% tol. No visible damage

Noise requirements:

Resistors range	Value
R < 100 Ω	10 dB
100 Ω ≤ R < 1 KΩ	20 dB
1 KΩ ≤ R < 10 KΩ	30 dB
10 KΩ ≤ R < 100 KΩ	40 dB
100 KΩ ≤ R < 1 MΩ	46 dB
1 MΩ ≤ R ≤ 22 MΩ	48 dB

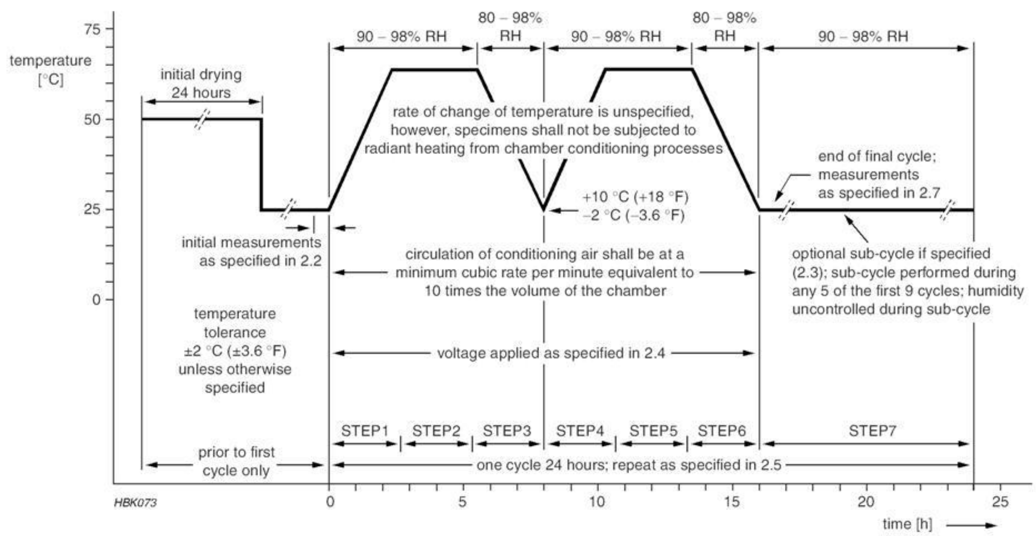


Fig. 9 Moisture resistance test requirements

REVISION HISTORY

REVISION	DATE	CHANGE NOTIFICATION	DESCRIPTION
Version 2	Sep 03, 2004	-	- New datasheet for 1206 thick film 1% and 5% with lead-free terminations - Replace the 1206 part of pdf files: RC01_11_21_31_5, RC02_12_22_32_10, and HRC01_5_4 - Test method and procedure updated - PE tape added (paper tape will be replaced by PE tape) - High ohmic products combined into standard products.

MICROCHIP

TC1426/TC1427/TC1428

1.2A Dual High-Speed MOSFET Drivers

Features:

- Low Cost
- Latch-Up Protected: Will Withstand 500 mA Reverse Output Current
- ESD Protected ±2kV
- High Peak Output Current: 1.2A
- Wide Operating Range:
  - 4.5V to 16V
- High Capacitive Load Drive Capability: 1000 pF in 38 nsec
- Low Delay Time: 75 nsec Max
- Logic Input Threshold Independent of Supply Voltage
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}
- Low Output Impedance: 8Ω

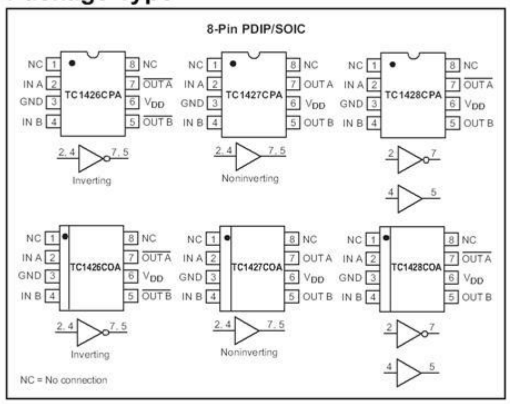
Applications:

- Power MOSFET Drivers
- Switched Mode Power Supplies
- Pulse Transformer Drive
- Small Motor Controls
- Print Head Drive

Device Selection Table

Part Number	Package	Temp. Range
TC1426COA	8-Pin SOIC	0°C to +70°C
TC1426CPA	8-Pin PDIP	0°C to +70°C
TC1427COA	8-Pin SOIC	0°C to +70°C
TC1427CPA	8-Pin PDIP	0°C to +70°C
TC1428COA	8-Pin SOIC	0°C to +70°C
TC1428CPA	8-Pin PDIP	0°C to +70°C

Package Type



General Description:

The TC1426/TC1427/TC1428 are a family of 1.2A dual high-speed drivers. CMOS fabrication is used for low-power consumption and high efficiency.

These devices are fabricated using an epitaxial layer to effectively short out the intrinsic parasitic transistor responsible for CMOS latch-up. They incorporate a number of other design and process refinements to increase their long-term reliability.

The TC1426 is compatible with the bipolar DS0026, but only draws 1/5 of the quiescent current. The TC1426/TC1427/TC1428 are also compatible with the TC426/TC427/TC428, but with 1.2A peak output current rather than the 1.5A of the TC426/TC427/TC428 devices.

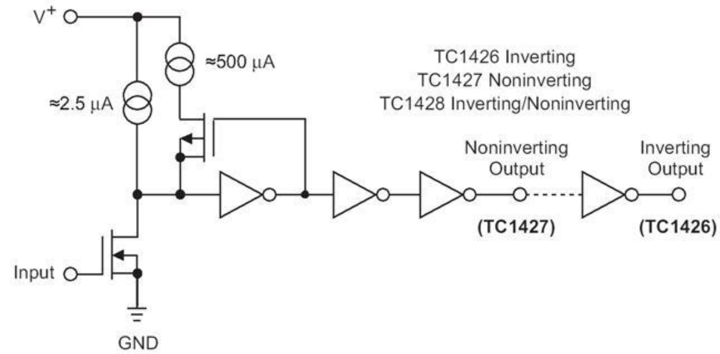
Other compatible drivers are the TC4426/TC4427/TC4428 and the TC4426A/TC4427A/TC4428A. The TC4426/TC4427/TC4428 have the added feature that the inputs can withstand negative voltage up to 5V with diode protection circuits. The TC4426A/TC4427A/TC4428A have matched input to output leading edge and falling edge delays, t_{D1} and t_{D2}, for processing short duration pulses in the 25 nanoseconds range. All of the above drivers are pin compatible.

The high-input impedance TC1426/TC1427/TC1428 drivers are CMOS/TTL input-compatible, do not require the speed-up needed by the bipolar devices, and can be directly driven by most PWM ICs.

This family of devices is available in inverting and non-inverting versions. Specifications have been optimized to achieve low-cost and high-performance devices, well-suited for the high-volume manufacturer.

© 2006 Microchip Technology Inc.

Functional Block Diagram



NOTE: TC1428 has one inverting and one noninverting driver.
Ground any unused driver input.

© 2006 Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage .... +18V
Input Voltage, Any Terminal
.... V_{DD} + 0.3V to GND – 0.3V
Power Dissipation ($T_A \leq 70°C$)
PDIP .... 730 mW
SOIC .... 470 mW
Derating Factor
PDIP .... 8 mW/°C
SOIC .... 4 mW/°C
Operating Temperature Range
C Version .... 0°C to +70°C
Storage Temperature Range .... -65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC1426/TC1427/TC1428 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 16V, unless otherwise noted.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input						
V_{IH}	Logic 1, High Input Voltage	3	—	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	—	0.8	V	
I_{IN}	Input Current	-1	—	1	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
V_{OH}	High Output Voltage	V_{DD} – 0.025	—	—	V	Figure 3-1, Figure 3-2
V_{OL}	Low Output Voltage	—	—	0.025	V	Figure 3-1, Figure 3-2
R_O	Output Resistance	— —	12 8	18 12	Ω	I_{OUT} = 10 mA, V_{DD} = 16V
I_{PK}	Peak Output Current	—	1.2	—	A	
I_{REV}	Latch-Up Current Withstand Reverse Current	—	>500	—	mA	
Switching Time (Note 1)						
t_R	Rise Time	—	—	35	nsec	Figure 3-1, Figure 3-2
t_F	Fall Time	—	—	25	nsec	Figure 3-1, Figure 3-2
t_{D1}	Delay Time	—	—	75	nsec	Figure 3-1, Figure 3-2
t_{D2}	Delay Time	—	—	75	nsec	Figure 3-1, Figure 3-2
Power Supply						
I_S	Power Supply Current	— —	— —	9 0.5	mA	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)

Note 1: Switching times ensured by design.

© 2006 Microchip Technology Inc.

TC1426/TC1427/TC1428 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Over operating temperature range with 4.5V $\le V_{DD} \le$ 16V, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
Input						
V_{IH}	Logic 1, High Input Voltage	3	—	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	—	0.8	V	
I_{IN}	Input Current	-10	—	10	µA	$0V \le V_{IN} \le V_{DD}$
Output						
V_{OH}	High Output Voltage	V_{DD} – 0.025	—	—	V	Figure 3-1, Figure 3-2
V_{OL}	Low Output Voltage	—	—	0.025	V	Figure 3-1, Figure 3-2
R_O	Output Resistance	— —	15 10	23 18	Ω	I_{OUT} = 10 mA, V_{DD} = 16V
I_{REV}	Latch-Up Current Withstand Reverse Current	—	>500	—	mA	
Switching Time (Note 1)						
t_R	Rise Time	—	—	60	nsec	Figure 3-1, Figure 3-2
t_F	Fall Time	—	—	40	nsec	Figure 3-1, Figure 3-2
t_{D1}	Delay Time	—	—	125	nsec	Figure 3-1, Figure 3-2
t_{D2}	Delay Time	—	—	125	nsec	Figure 3-1, Figure 3-2
Power Supply						
I_S	Power Supply Current	— —	— —	13 0.7	mA	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)

Note 1: Switching times ensured by design.

© 2006 Microchip Technology Inc.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, SOIC)	Symbol	Description
1	NC	No connection.
2	IN A	Control input A, TTL/CMOS compatible logic input.
3	GND	Ground.
4	IN B	Control input B, TTL/CMOS compatible logic input.
5	OUT B	Output B, CMOS totem-pole output.
6	V_{DD}	Supply input, 4.5V to 16V.
7	OUT A	Output A, CMOS totem-pole output.
8	NC	No connection.

© 2006 Microchip Technology Inc.

3.0 APPLICATIONS INFORMATION

3.1 SUPPLY BYPASSING

Large currents are required to charge and discharge capacitive loads quickly. For example, charging a 1000 pF load to 16V in 25 nsec requires a 0.8A current from the device's power supply.

To ensure low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (<0.5-in.) should be used. A 1.0 µF film capacitor in parallel with one or two 0.1 µF ceramic MLC capacitors normally provides adequate bypassing.

3.2 GROUNDING

The TC1426 and TC1428 contain inverting drivers. Individual ground returns for the input and output circuits or a ground plane should be used. This will reduce negative feedback that causes degradation in switching speed characteristics.

3.3 INPUT STAGE

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic '1' input, the maximum quiescent supply current is 9 mA. Logic '0' input level signals reduce quiescent current to 500 µA maximum. **Unused driver inputs must be connected to V_{DD} or GND.** Minimum power dissipation occurs for logic '0' inputs for the TC1426/TC1427/TC1428.

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making a logic '1' input any voltage greater than 1.5V up to V_{DD}. Input current is less than 1 µA over this range.

The TC1426/TC1427/TC1428 may be directly driven by the TL494, SG1526/27, TC38C42, TC170 and similar switch-mode power supply integrated circuits.

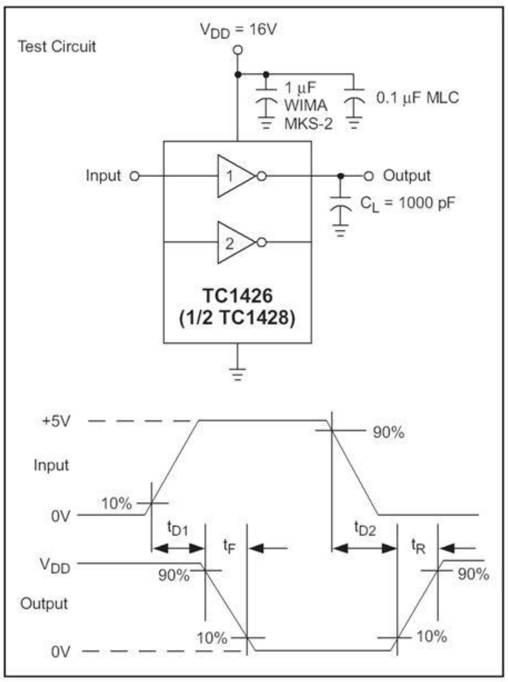


FIGURE 3-1: *Inverting Driver Switching Time*

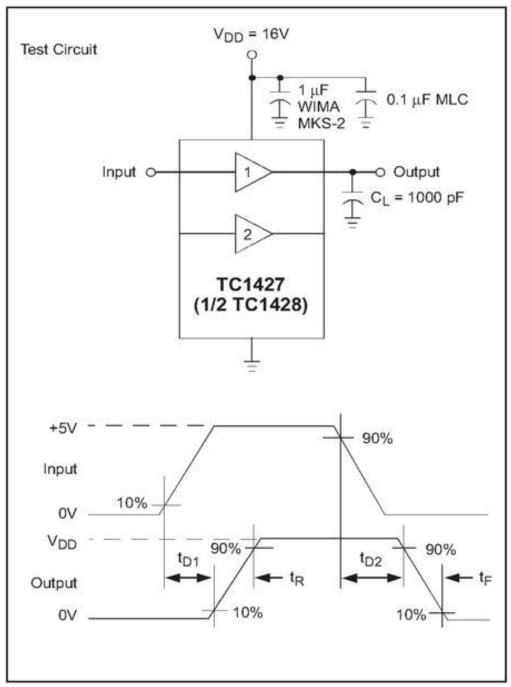


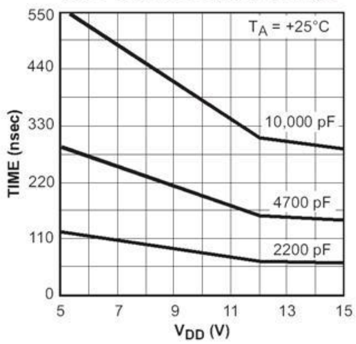
FIGURE 3-2: *Noninverting Driver Switching Time*

© 2006 Microchip Technology Inc.

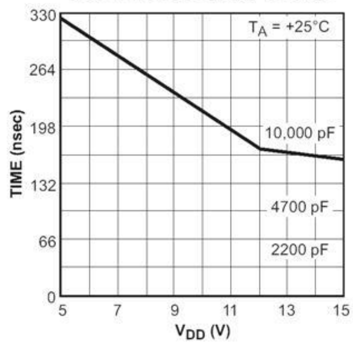
4.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

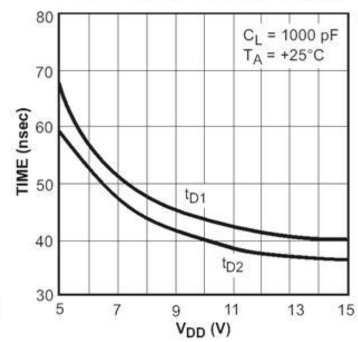
Rise Time vs. Supply Voltage



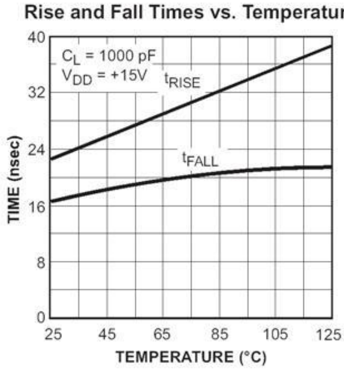
Fall Time vs. Supply Voltage



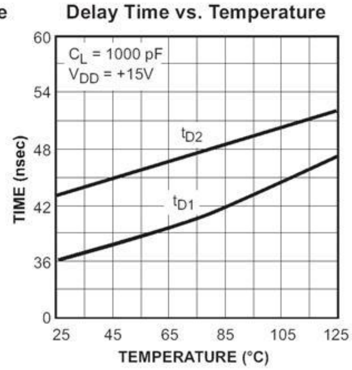
Delay Time vs. Supply Voltage



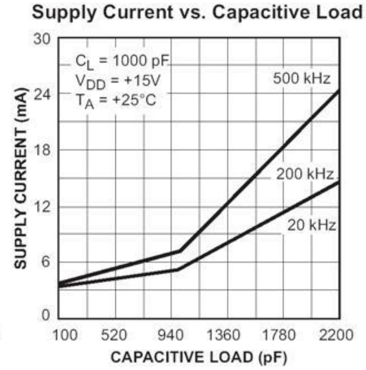
Rise and Fall Times vs. Temperature



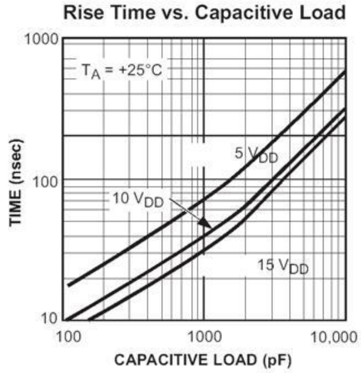
Delay Time vs. Temperature



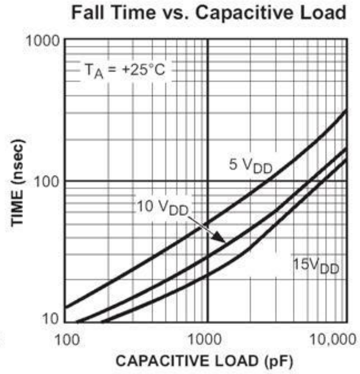
Supply Current vs. Capacitive Load



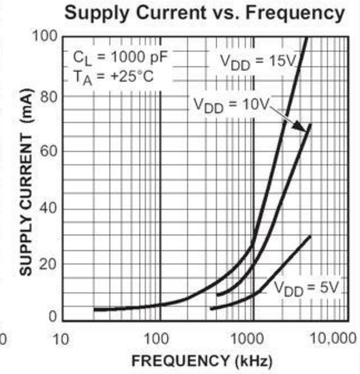
Rise Time vs. Capacitive Load



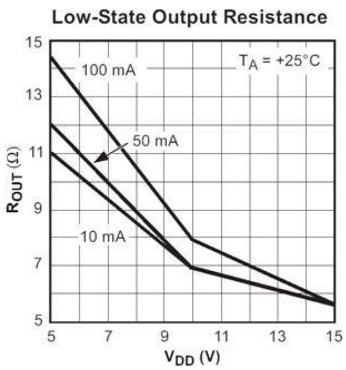
Fall Time vs. Capacitive Load

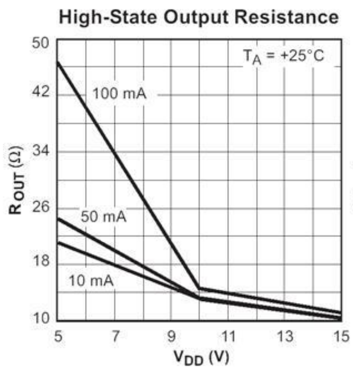


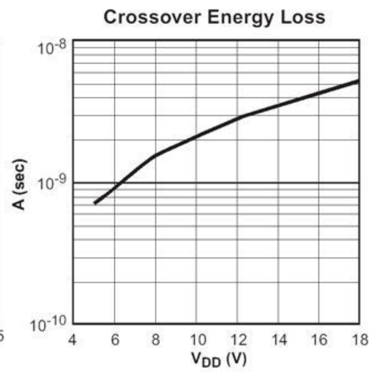
Supply Current vs. Frequency

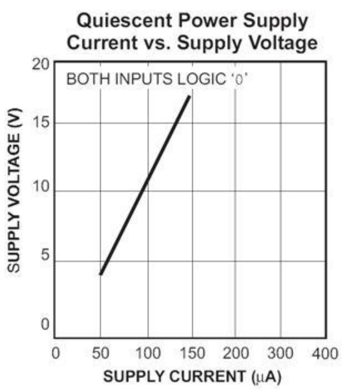


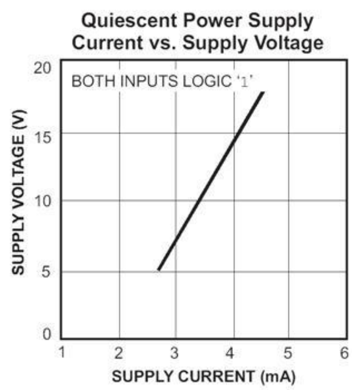
TYPICAL CHARACTERISTICS (CONTINUED)

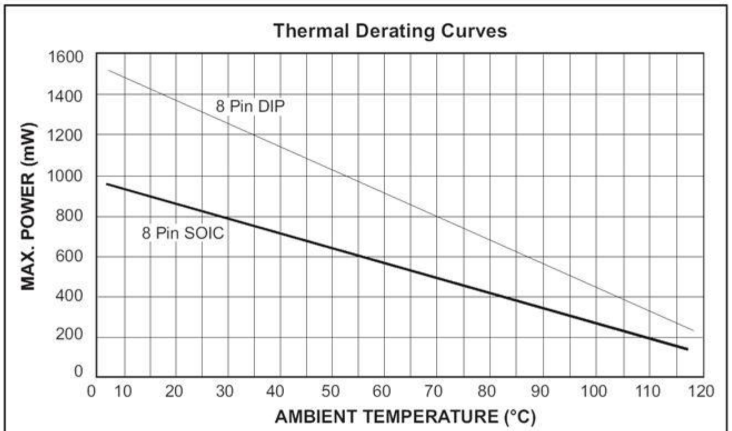












© 2006 Microchip Technology Inc.

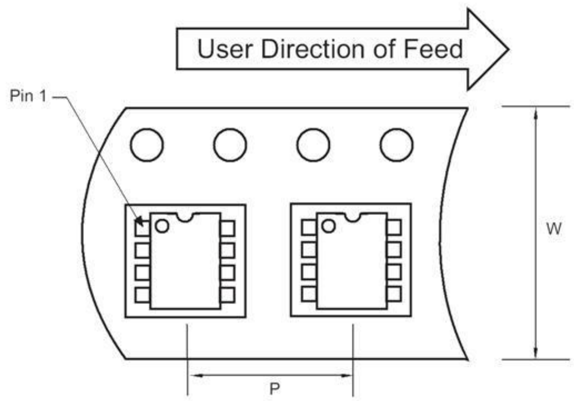
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package marking data not available at this time.

5.2 Taping Form

Component Taping Orientation for 8-Pin MSOP Devices

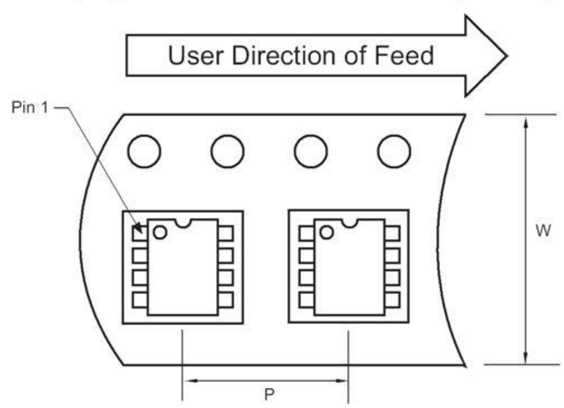


Standard Reel Component Orientation
for 713 Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin MSOP	12 mm	8 mm	2500	13 in

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



Standard Reel Component Orientation
for 713 Suffix Device

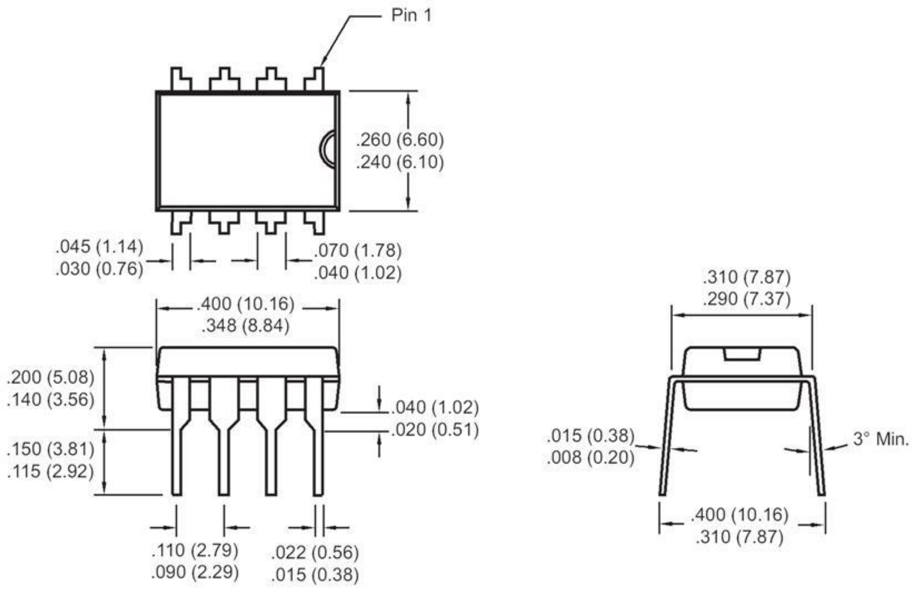
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

© 2006 Microchip Technology Inc.

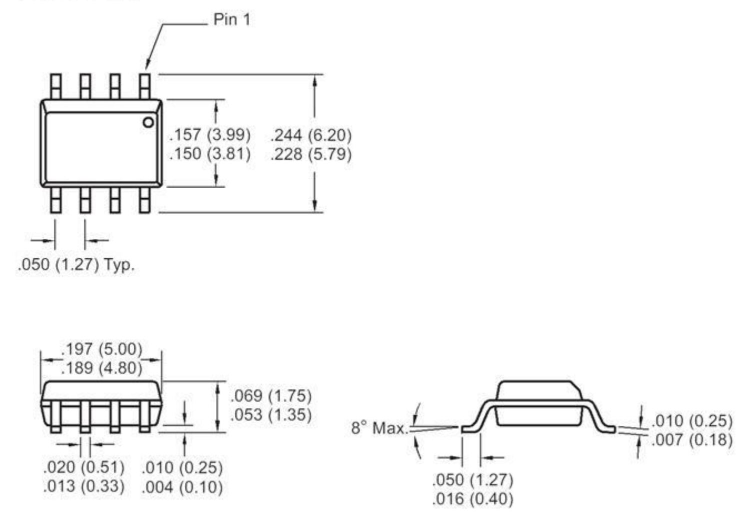
5.3 Package Dimensions

8-Pin Plastic DIP



Dimensions: inches (mm)

8-Pin SOIC



Dimensions: inches (mm)

© 2006 Microchip Technology Inc.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

© 2006 Microchip Technology Inc.

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager　　Total Pages Sent ________

RE: Reader Response

From: Name ______________________________

Company ______________________________

Address ______________________________

City / State / ZIP / Country ______________________________

Telephone: (_______) _________ - _________　　FAX: (______) _________ - _________

Application (optional):

Would you like a reply?___Y ___N

Device: TC1426/TC1427/TC1428　　Literature Number: DS21393C

Questions:

1. What are the best features of this document?

____

____

2. How does this document meet your hardware and software development needs?

____

____

3. Do you find the organization of this document easy to follow? If not, why?

____

____

4. What additions to the document do you think would enhance the structure and subject?

____

____

5. What deletions from the document could be made without affecting the overall usefulness?

____

____

6. Is there any incorrect or misleading information (what and where)?

____

____

7. How would you improve this document?

____

____

© 2006 Microchip Technology Inc.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rfPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AmpLab, FilterLab, Migratable Memory, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Linear Active Thermistor, Mindi, MiWi, MPASM, MPLIB, MPLINK, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rfLAB, rfPICDEM, Select Mode, Smart Serial, SmartTel, Total Endurance, UNI/O, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2006, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona, Gresham, Oregon and Mountain View, California. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

MICROCHIP

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Alpharetta, GA
Tel: 770-640-0034
Fax: 770-640-0307

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

San Jose
Mountain View, CA
Tel: 650-215-1444
Fax: 650-961-0286

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8676-6200
Fax: 86-28-8676-6599

China - Fuzhou
Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde
Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7250
Fax: 86-29-8833-7256

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi
Tel: 91-11-5160-8631
Fax: 91-11-5160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Gumi
Tel: 82-54-473-4301
Fax: 82-54-473-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Penang
Tel: 60-4-646-8870
Fax: 60-4-646-5086

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

02/16/06

© 2006 Microchip Technology Inc.

Features

- Multiturn / Cermet / Industrial / Sealed
- 5 terminal styles
- Tape and reel packaging available
- Chevron seal design
- Listed on the QPL for style RJ24 per MIL-R-22097 and RJR24 per High-Rel Mil-R-39035
- Mounting hardware available (H-117P)
- RoHS compliant* version available

3296 - 3/8 " Square Trimming Potentiometer

Electrical Characteristics

Standard Resistance Range ....10 ohms to 2 megohms (see standard resistance table)
Resistance Tolerance ....±10 % std. (tighter tolerance available)
Absolute Minimum Resistance ....1 % or 2 ohms max. (whichever is greater)
Contact Resistance Variation ....1.0 % or 3 ohms max. (whichever is greater)
Adjustability
Voltage.....................................±0.01 %
Resistance ....±0.05 %
Resolution....................................Infinite
Insulation Resistance ....500 vdc. 1,000 megohms min.
Dielectric Strength
Sea Level ....900 vac
70,000 Feet..............................350 vac
Effective Travel..................25 turns nom.

Environmental Characteristics

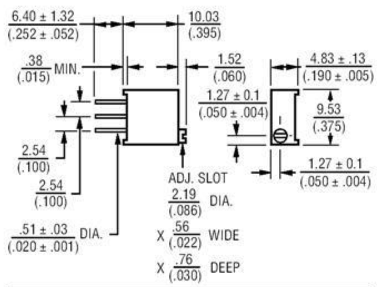
Power Rating (300 volts max.)
70 °C ....0.5 watt
125 °C ....0 watt
Temperature Range ....-55 °C to +150 °C
Temperature Coefficient ....±100 ppm/°C
Seal Test.......................85 °C Fluorinert†
Humidity........MIL-STD-202 Method 103 96 hours (2 % ΔTR, 10 Megohms IR)
Vibration.........20 G (1 % ΔTR; 1 % ΔVR)
Shock...........100 G (1 % ΔTR; 1 % ΔVR)
Load Life ....1,000 hours 0.5 watt @ 70 °C (3 % ΔTR; 3 % or 3 ohms, whichever is greater, CRV)
Rotational Life........................200 cycles (4 % ΔTR; 3 % or 3 ohms, whichever is greater, CRV)

Physical Characteristics

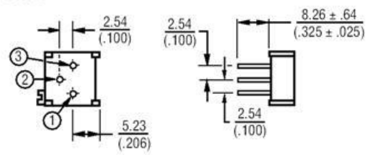
Torque ....3.0 oz-in. max.
Mechanical Stops.................Wiper idles
Terminals........................Solderable pins
Weight ....0.03 oz.
Marking ....Manufacturer's trademark, resistance code, wiring diagram, date code, manufacturer's model number and style
Wiper................50 % (Actual TR) ±10 %
Flammability ..........................U.L. 94V-0
Standard Packaging .....50 pcs. per tube
Adjustment Tool H-90

Product Dimensions

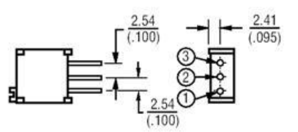
Common Dimensions



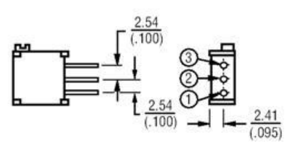
3296P



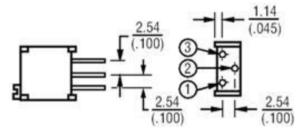
3296W



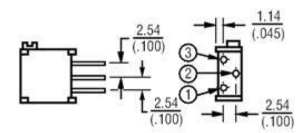
3296X

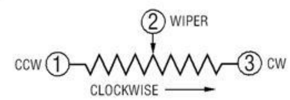


3296Y



3296Z





TOLERANCES: ± 0.25 (.010) EXCEPT WHERE NOTED

DIMENSIONS ARE: MM / (INCHES)

How to Order

3296 W - 1 - 103 __ LF

Model
Style
Standard or Modified Product Indicator
-1 = Standard Product
Resistance Code
Packaging Designator
Blank = Tube (Standard)
R = Tape and Reel (X and W Pin Styles Only)
A = Ammo Pack (X and W Pin Styles Only)
Terminations
LF = 100 % Tin-plated (RoHS compliant)
Blank = 90 % Tin / 10 % Lead-plated (Standard)

Consult factory for other available options.

Standard Resistance Table

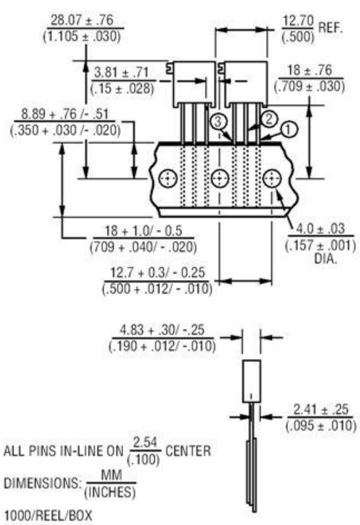
Resistance (Ohms)	Resistance Code
10	**100**
20	**200**
50	**500**
100	**101**
200	**201**
500	**501**
1,000	**102**
2,000	**202**
5,000	**502**
10,000	**103**
20,000	**203**
25,000	**253**
50,000	**503**
100,000	**104**
200,000	**204**
250,000	**254**
500,000	**504**
1,000,000	**105**
2,000,000	**205**

Popular values listed in boldface. Special resistances available.

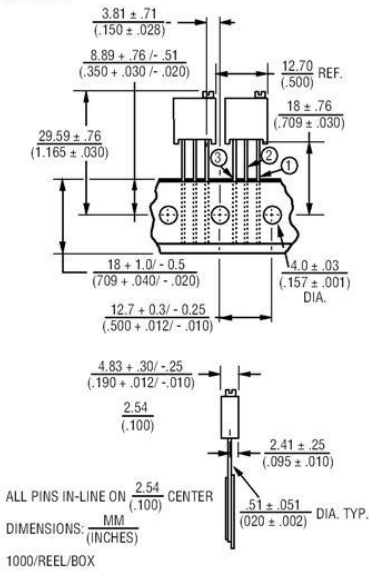
*RoHS Directive 2002/95/EC Jan 27 2003 including Annex.
†"Fluorinert" is a registered trademark of 3M Co.
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Packaging Specifications

SIDE ADJUST
3296X-1



TOP ADJUST
3296W-1

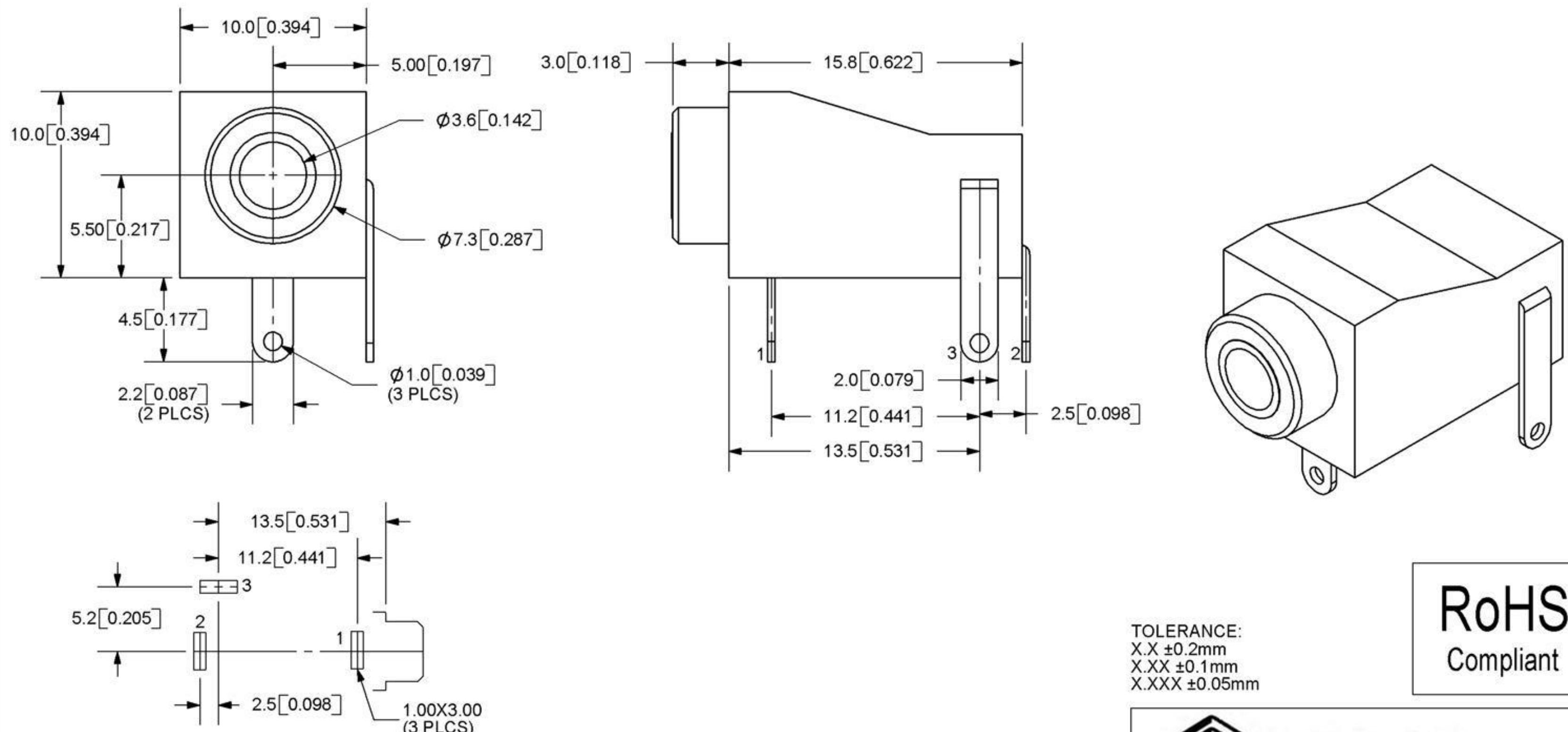


Meets EIA Specification 468.

REV. 10/05

Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

REV.	DESCRIPTION	DATE
A	NEW DRAWING	10/14/2005

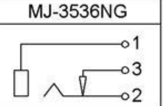


PCB LAYOUT
TOP VIEW
(SCALE 2:1)

TOLERANCE:
X.X ±0.2mm
X.XX ±0.1mm
X.XXX ±0.05mm

RoHS Compliant

SPECIFICATIONS:
RATING: 12V DC @ 1A
CONTACT RESISTANCE: 30m OHMS MAX
INSULATION RESISTANCE: 50M OHMS MIN: 100V DC
VOLTAGE WITHSTAND: 500V AC R.M.S. FOR 1 MINUTE
LIFE: 5,000 CYCLES

MODEL NO.	MJ-3536NG
SCHEMATIC	

	MATERIAL	PLATING
BUSHING	Brass	Nickel
TERMINAL 1	Brass	Tin
TERMINAL 2	Copper Alloy	Tin
TERMINAL 3	Brass	Tin
INSULATION CAP	PC	
HOUSING	PBT	

CUI INC
9615 SW Allen, Suite 103
Beaverton, OR 97005
Phone: (503) 643-4899
800-275-4899
Fax: (503) 372-1266
Website: www.cui.com

TITLE: 3.5mm AUDIO JACK-MONO		REV: A
PART NO. MJ-3536NG		UNITS: MM [INCHES]
DRAWN BY: ZRJ	APPROVED BY:	SCALE: 3:1

PC FILE NAME MJ-3536NG

COPYRIGHT 2005 BY CUI INC.

Innovative Service Around the Globe YAGEO

DATA SHEET

SURFACE-MOUNT CERAMIC MULTILAYER CAPACITORS

Class 2, X7R

16 V TO 500 V

Product Specification – Aug 17, 2005 V.9

Phycomp

Surface-mount ceramic multilayer capacitors

Class 2, X7R 16 V to 500 V

FEATURES

- Six standard sizes
- High capacitance per unit volume
- Supplied in tape on reel or in bulk case
- NiSn terminations.

APPLICATIONS

- Consumer electronics for example
  - Tuners
  - Television receivers
  - Video recorders
  - All types of cameras
- Telecommunications
- Automotive
- Data processing.

DESCRIPTION

The capacitor consists of a rectangular block of ceramic dielectric in which a number of interleaved nickel electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two copper terminations, coated with a barrier layer of plated nickel and finally covered with a layer of plated tin (NiSn). A cross section of the structure is shown in Fig.1.

QUICK REFERENCE DATA

DESCRIPTION	VALUE
Rated voltage U_R (DC)	16 V, 25 V, 50 V, 100 V, 200 V, 250 V and 500 V (IEC)
Capacitance range (E12 series):	
16 V	4.7 nF to 1 µF
25 V	3.3 nF to 1 µF
50 V	100 pF to 1 µF
100 V	220 pF to 560 nF
200 V	220 pF to 150 nF
250 V	220 pF to 33 nF
500 V	470 pF to 15 nF
Tolerance on capacitance	±10%; ±5%
Test voltage (DC) for 1 minute:	$2.5 \times U_r$
Sectional specifications	IEC 60384-10 second edition 1989-04; also based on CECC 32 100
Detailed specification	based on CECC 32 101-801
Climatic category (IEC 60 068)	55/125/56

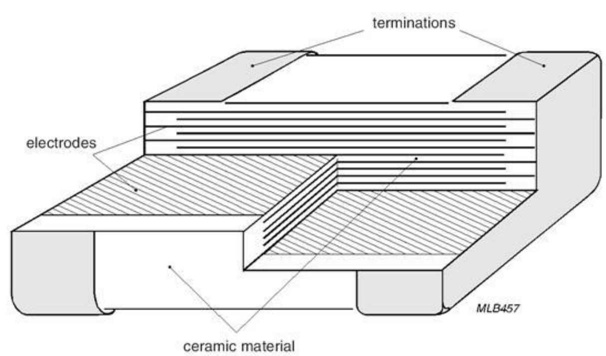
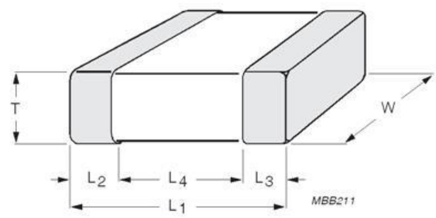


Fig.1 Construction of a ceramic multilayer capacitor.

MECHANICAL DATA



For dimensions see Table 1.

Fig.2. Component outline.

Physical dimensions

Table 1 Capacitor dimensions

CASE SIZE	L_1	W	T MIN.	T MAX.	L_2 and L_3 MIN.	L_2 and L_3 MAX.	L_4 MIN.
Dimensions in millimetres							
0402	1.0 ±0.05	0.5 ±0.05	0.45	0.55	0.20	0.30	0.40
0603	1.6 ±0.10	0.8 ±0.07	0.73	0.87	0.25	0.65	0.40
0805	2.0 ±0.10	1.25 ±0.10	0.50	1.35	0.25	0.75	0.55
1206	3.2 ±0.15	1.6 ±0.15	0.50	1.25	0.25	0.75	1.40
1210	3.2 ±0.20	2.5 ±0.20	0.50	2.10	0.25	0.75	1.40
1812	4.5 ±0.20	3.2 ±0.20	0.90	1.75	0.25	0.75	2.20
Dimensions in inches							
0402	0.040 ±0.002	0.020 ±0.002	0.018	0.022	0.008	0.012	0.016
0603	0.063 ±0.004	0.032 ±0.003	0.029	0.035	0.010	0.026	0.016
0805	0.079 ±0.004	0.049 ±0.004	0.020	0.053	0.010	0.030	0.022
1206	0.126 ±0.006	0.063 ±0.006	0.020	0.049	0.010	0.030	0.056
1210	0.126 ±0.008	0.098 ±0.008	0.020	0.083	0.010	0.030	0.056
1812	0.177 ±0.008	0.126 ±0.008	0.035	0.069	0.010	0.030	0.088

SELECTION CHART FOR 16 V

<table>
<tr><th rowspan="2">C
(nF)</th><th rowspan="2">LAST
TWO DIGITS
OF 12NC</th><th colspan="4">16 V</th></tr>
<tr><th>0402</th><th>0603</th><th>0805</th><th>1206</th></tr>
<tr><td>4.7</td><td>32</td><td rowspan="13">0.5 ±0.05</td><td></td><td></td><td></td></tr>
<tr><td>5.6</td><td>33</td><td></td><td></td><td></td></tr>
<tr><td>6.8</td><td>34</td><td></td><td></td><td></td></tr>
<tr><td>8.2</td><td>35</td><td></td><td></td><td></td></tr>
<tr><td>10</td><td>36</td><td></td><td></td><td></td></tr>
<tr><td>12</td><td>37</td><td></td><td></td><td></td></tr>
<tr><td>15</td><td>38</td><td></td><td></td><td></td></tr>
<tr><td>18</td><td>39</td><td></td><td></td><td></td></tr>
<tr><td>22</td><td>41</td><td rowspan="9">0.8 ±0.07</td><td></td><td></td></tr>
<tr><td>27</td><td>42</td><td></td><td></td></tr>
<tr><td>33</td><td>43</td><td></td><td></td></tr>
<tr><td>39</td><td>44</td><td></td><td></td></tr>
<tr><td>47</td><td>45</td><td rowspan="2">0.6 ±0.1</td><td></td></tr>
<tr><td>56</td><td>46</td><td></td><td></td></tr>
<tr><td>68</td><td>47</td><td></td><td rowspan="8">0.85 ±0.1</td><td></td></tr>
<tr><td>82</td><td>48</td><td></td><td></td></tr>
<tr><td>100</td><td>49</td><td></td><td></td></tr>
<tr><td>120</td><td>51</td><td></td><td></td><td></td></tr>
<tr><td>150</td><td>52</td><td></td><td></td><td></td></tr>
<tr><td>180</td><td>53</td><td></td><td></td><td></td></tr>
<tr><td>220</td><td>54</td><td></td><td></td><td rowspan="5">0.85 ±0.1</td></tr>
<tr><td>270</td><td>55</td><td></td><td></td></tr>
<tr><td>330</td><td>56</td><td></td><td></td><td rowspan="3">1.25 ±0.1</td></tr>
<tr><td>390</td><td>57</td><td></td><td></td></tr>
<tr><td>470</td><td>58</td><td></td><td></td></tr>
<tr><td>560</td><td>59</td><td></td><td></td><td></td><td rowspan="4">1.15 ±0.1</td></tr>
<tr><td>680</td><td>61</td><td></td><td></td><td></td></tr>
<tr><td>820</td><td>62</td><td></td><td></td><td></td></tr>
<tr><td>1 000</td><td>63</td><td></td><td></td><td></td></tr>
</table>

Note

1. Values in shaded cells indicate thickness class in mm.
2. Thickness classification and packing quantities refer to table 2.

SELECTION CHART FOR 25 V

C (nF)	LAST TWO DIGITS OF 12NC	25 V				
		0402	0603	0805	1206	1210
3.3	29					
3.9	31					
4.7	32					
5.6	33	0.5 ±0.05				
6.8	34					
8.2	35					
10	36					
12	37					
15	38					
18	39			0.6 ±0.1		
22	41					
27	42					
33	43		0.8 ±0.07			
39	44					
47	45					
56	46					
68	47			0.85 ±0.1		
82	48					
100	49					
120	51					
150	52				0.85 ±0.1	
180	53					
220	54					
270	55					
330	56				1.15 ±0.1	
390	57					
470	58					
560	59					1.15 ±0.1
680	61					
820	62					1.6 ±0.2
1 000	63					

Note

1. Values in shaded cells indicate thickness class in mm.
2. Thickness classification and packing quantities refer to table 2.

Thickness classification and packing quantities for 16 V to 500 V

Table 2 Quantities for all sizes and thickness

SIZE CODE	THICKNESS CLASSIFICATION (mm)	8 mm TAPE WIDTH QUANTITY PER REEL				12 mm TAPE WIDTH QUANTITY PER REEL	QUANTITY PER BULK CASE
		∅180 mm; 7"		∅330 mm; 13"		∅180 mm; 7"	
		Paper	Blister	Paper	Blister	Blister	
0402	0.5 ±0.05	10,000	–	50,000	–	–	50,000
0603	0.8 ±0.07	4,000	–	15,000		–	15,000
0805	0.6 ±0.1	4,000	–	20,000	–	–	10,000
	0.85 ±0.1	4,000	–	15,000	–	–	8,000
	1.25 ±0.1	–	3,000	–	10,000	–	5,000
1206	0.85 ±0.1	4,000	–	15,000	–	–	–
	1.15 ±0.1	–	3,000	–	10,000	–	–
1210	0.85 ±0.1	–	4,000	–	10,000	–	–
	1.15 ±0.1	–	3,000	–	10,000	–	–
	1.6 ±0.2	–	2,000	–	–	–	–
1812	1.15 ±0.1	–	–	–	–	1,500	–
	1.6 ±0.2	–	–	–	–	1,000	–

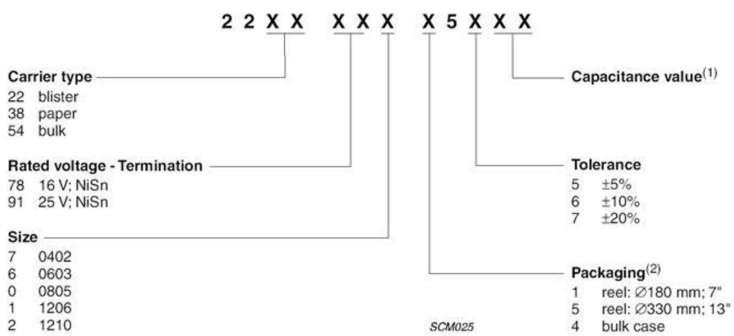
Surface-mount ceramic multilayer capacitors

Class 2, X7R 16 V to 500 V

ORDERING INFORMATION FOR 16 V AND 25 V

Components may be ordered by using either a Phycomp's unique 12NC or simple 15-digit clear text code.

Ordering code 12NC (preferred)



(1) Refer to chapters "Selection chart for 16 V" and "Selection chart for 25 V".

(2) Quantity on reel depends on thickness classification, see section "Thickness classification and packing quantities".

Clear text code

EXAMPLE: 08052R104K8BB0D

Size Code	Temp. Char.	Capacitance	Tol.	Vol.	Termination	Packing	Marking	Series
0402 0603 0805 1206 1210	2R = X7R	104 = 100000 pF; the third digit signifies the multiplying factor: 2 = × 100 3 = × 1000 4 = × 10 000 5 = × 100 000	J = ±5% K = ±10% M = ±20%	7 = 16 V 8 = 25 V	B = NiSn	2 = 180 mm; 7" paper 3 = 330 mm; 13" paper B = 180 mm; 7" blister F = 330 mm; 13" blister P = bulk case	0 = no marking	D = BME

SELECTION CHART FOR 50 V

C (pF)	LAST TWO DIGITS OF 12NC	50 V					
		0402	0603	0805	1206	1210	1812
100	09						
120	11						
150	12						
180	13						
220	14						
270	15						
330	16						
390	17						
470	18						
560	19						
680	21	0.5 ±0.05					
820	22						
1,000	23						
1,200	24		0.8 ±0.07				
1,500	25						
1,800	26			0.6 ±0.1			
2,200	27						
2,700	28				0.85 ±0.1		
3,300	29						
3,900	31						
4,700	32						
5,600	33						
6,800	34						
8,200	35						
10,000	36						
12,000	37						
15,000	38					0.85 ±0.1	
18,000	39						
22,000	41						

Note

1. Values in shaded cells indicate thickness class in mm.
2. Thickness classification and packing quantities refer to table 2.

SELECTION CHART FOR 50 V CONTINUED

<table>
<tr><th rowspan="2">C
(pF)</th><th rowspan="2">LAST
TWO DIGITS
OF 12NC</th><th colspan="6">50 V</th></tr>
<tr><th>0402</th><th>0603</th><th>0805</th><th>1206</th><th>1210</th><th>1812</th></tr>
<tr><td>27,000</td><td>42</td><td></td><td></td><td rowspan="8">0.85 ±0.1</td><td rowspan="9">0.85 ±0.1</td><td rowspan="8">0.85 ±0.1</td><td></td></tr>
<tr><td>33,000</td><td>43</td><td></td><td></td><td></td></tr>
<tr><td>39,000</td><td>44</td><td></td><td></td><td></td></tr>
<tr><td>47,000</td><td>45</td><td></td><td></td><td></td></tr>
<tr><td>56,000</td><td>46</td><td></td><td></td><td></td></tr>
<tr><td>68,000</td><td>47</td><td></td><td></td><td></td></tr>
<tr><td>82,000</td><td>48</td><td></td><td></td><td></td></tr>
<tr><td>100,000</td><td>49</td><td></td><td>0.8 ±0.07</td><td rowspan="10">1.15 ±0.1</td></tr>
<tr><td>120,000</td><td>51</td><td></td><td></td><td></td><td rowspan="6">1.15 ±0.1</td></tr>
<tr><td>150,000</td><td>52</td><td></td><td></td><td></td><td rowspan="3">1.15 ±0.1</td></tr>
<tr><td>180,000</td><td>53</td><td></td><td></td><td></td></tr>
<tr><td>220,000</td><td>54</td><td></td><td></td><td></td></tr>
<tr><td>270,000</td><td>55</td><td></td><td></td><td></td><td></td></tr>
<tr><td>330,000</td><td>56</td><td></td><td></td><td></td><td></td></tr>
<tr><td>390,000</td><td>57</td><td></td><td></td><td></td><td></td><td rowspan="2">1.6 ±0.2</td></tr>
<tr><td>470,000</td><td>58</td><td></td><td></td><td></td><td></td></tr>
<tr><td>560,000</td><td>59</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>680,000</td><td>61</td><td></td><td></td><td></td><td></td><td></td><td rowspan="3">1.6 ±0.2</td></tr>
<tr><td>820,000</td><td>62</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>1,000,000</td><td>63</td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

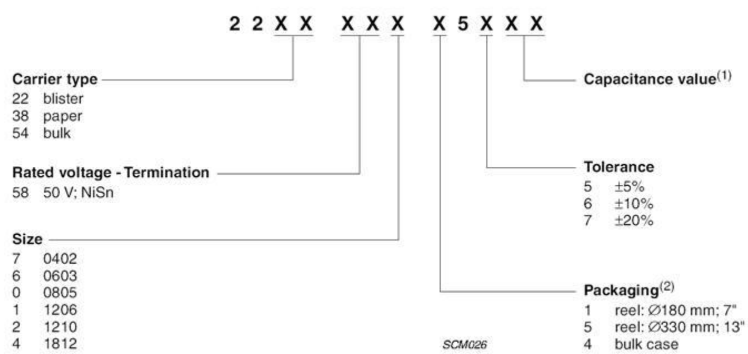
Note

1. Values in shaded cells indicate thickness class in mm.
2. Thickness classification and packing quantities refer to table 2.

ORDERING INFORMATION FOR 50 V

Components may be ordered by using either a Phycomp's unique 12NC or simple 15-digit clear text code.

Ordering code 12NC (preferred)



(1) Refer to chapter "Selection chart for 50 V".

(2) Quantity on reel depends on thickness classification, see section "Thickness classification and packing quantities".

Clear text code

EXAMPLE: 08052R104K9BB0D

Size Code	Temp. Char.	Capacitance	Tol.	Vol.	Termination	Packing	Marking	Series
0402 0603 0805 1206 1210 1812	2R = X7R	104 = 100000 pF; the third digit signifies the multiplying factor: 1 = × 10 2 = × 100 3 = × 1000 4 = × 10 000 5 = × 100 000	J = ±5% K = ±10% M = ±20%	9 = 50 V	B = NiSn	2 = 180 mm; 7" paper 3 = 330 mm; 13" paper B = 180 mm; 7" blister F = 330 mm; 13" blister P = bulk case	0 = no marking	D = BME

SELECTION CHART FOR 100 V

C (pF)	LAST TWO DIGITS OF 12NC	100 V			
		0805	1206	1210	1812
220	14				
270	15				
330	16				
390	17				
470	18				
560	19				
680	21				
820	22				
1,000	23				
1,200	24				
1,500	25	0.6 ±0.1	0.85 ±0.1		
1,800	26				
2,200	27				
2,700	28				
3,300	29				
3,900	31				
4,700	32				
5,600	33				
6,800	34				
8,200	35				
10,000	36				

Note

1. Values in shaded cells indicate thickness class in mm.
2. Thickness classification and packing quantities refer to table 2.

SELECTION CHART FOR 100 V CONTINUED

<table>
<tr><th rowspan="2">C
(pF)</th><th rowspan="2">LAST
TWO DIGITS
OF 12NC</th><th colspan="4">100 V</th></tr>
<tr><th>0805</th><th>1206</th><th>1210</th><th>1812</th></tr>
<tr><td>12,000</td><td>37</td><td rowspan="5">0.85 ±0.1</td><td rowspan="9">0.85 ±0.1</td><td></td><td></td></tr>
<tr><td>15,000</td><td>38</td><td></td><td></td></tr>
<tr><td>18,000</td><td>39</td><td></td><td></td></tr>
<tr><td>22,000</td><td>41</td><td></td><td></td></tr>
<tr><td>27,000</td><td>42</td><td></td><td></td></tr>
<tr><td>33,000</td><td>43</td><td></td><td></td><td></td></tr>
<tr><td>39,000</td><td>44</td><td></td><td></td><td></td></tr>
<tr><td>47,000</td><td>45</td><td></td><td rowspan="5">0.85 ±0.1</td><td></td></tr>
<tr><td>56,000</td><td>46</td><td></td><td></td></tr>
<tr><td>68,000</td><td>47</td><td></td><td rowspan="3">1.15 ±0.1</td><td></td></tr>
<tr><td>82,000</td><td>48</td><td></td><td></td></tr>
<tr><td>100,000</td><td>49</td><td></td><td rowspan="8">1.15 ±0.1</td></tr>
<tr><td>120,000</td><td>51</td><td></td><td></td><td rowspan="4">1.15 ±0.1</td></tr>
<tr><td>150,000</td><td>52</td><td></td><td></td></tr>
<tr><td>180,000</td><td>53</td><td></td><td></td></tr>
<tr><td>220,000</td><td>54</td><td></td><td></td></tr>
<tr><td>270,000</td><td>55</td><td></td><td></td><td></td></tr>
<tr><td>330,000</td><td>56</td><td></td><td></td><td></td></tr>
<tr><td>390,000</td><td>57</td><td></td><td></td><td></td><td rowspan="3">1.6 ±0.2</td></tr>
<tr><td>470,000</td><td>58</td><td></td><td></td><td></td></tr>
<tr><td>560,000</td><td>59</td><td></td><td></td><td></td></tr>
</table>

Note

1. Values in shaded cells indicate thickness class in mm.
2. Thickness classification and packing quantities refer to table 2.

SELECTION CHART FOR 200 V AND 250 V

<table>
<tr><th rowspan="2">C
(pF)</th><th rowspan="2">LAST
TWO DIGITS
OF 12NC</th><th colspan="4">200 V</th><th colspan="2">250 V</th></tr>
<tr><th>0805</th><th>1206</th><th>1210</th><th>1812</th><th>0805</th><th>1206</th></tr>
<tr><td>220</td><td>14</td><td rowspan="18">0.85 ±0.1</td><td></td><td></td><td></td><td rowspan="18">0.85 ±0.1</td><td></td></tr>
<tr><td>270</td><td>15</td><td></td><td></td><td></td><td></td></tr>
<tr><td>330</td><td>16</td><td></td><td></td><td></td><td></td></tr>
<tr><td>390</td><td>17</td><td></td><td></td><td></td><td></td></tr>
<tr><td>470</td><td>18</td><td rowspan="16">0.85 ±0.1</td><td></td><td></td><td rowspan="16">0.85 ±0.1</td></tr>
<tr><td>560</td><td>19</td><td></td><td></td></tr>
<tr><td>680</td><td>21</td><td></td><td></td></tr>
<tr><td>820</td><td>22</td><td></td><td></td></tr>
<tr><td>1,000</td><td>23</td><td></td><td></td></tr>
<tr><td>1,200</td><td>24</td><td></td><td></td></tr>
<tr><td>1,500</td><td>25</td><td></td><td></td></tr>
<tr><td>1,800</td><td>26</td><td></td><td></td></tr>
<tr><td>2,200</td><td>27</td><td></td><td></td></tr>
<tr><td>2,700</td><td>28</td><td></td><td></td></tr>
<tr><td>3,300</td><td>29</td><td></td><td></td></tr>
<tr><td>3,900</td><td>31</td><td></td><td></td></tr>
<tr><td>4,700</td><td>32</td><td></td><td></td></tr>
<tr><td>5,600</td><td>33</td><td></td><td></td></tr>
<tr><td>6,800</td><td>34</td><td rowspan="2">1.25 ±0.1</td><td></td><td></td><td rowspan="2">1.25 ±0.1</td></tr>
<tr><td>8,200</td><td>35</td><td></td><td></td></tr>
</table>

Note

1. Values in shaded cells indicate thickness class in mm.
2. Thickness classification and packing quantities refer to table 2.

SELECTION CHART FOR 200 V AND 250 V CONTINUED

C (pF)	LAST TWO DIGITS OF 12NC	200 V				250 V	
		0805	1206	1210	1812	0805	1206
10,000	36	1.25 ±0.1				1.25 ±0.1	
12,000	37		0.85 ±0.1	0.85 ±0.1			0.85 ±0.1
15,000	38						
18,000	39						
22,000	41		1.15 ±0.1				1.15 ±0.1
27,000	42						
33,000	43						
39,000	44			1.15 ±0.1			
47,000	45						
56,000	46						
68,000	47						
82,000	48				1.15 ±0.1		
100,000	49						
120,000	51						
150,000	52						

Note

1. Values in shaded cells indicate thickness class in mm.
2. Thickness classification and packing quantities refer to table 2.

SELECTION CHART FOR 500 V

C (pF)	LAST TWO DIGITS OF 12NC	500 V		
		1206	1210	1812
470	18			
560	19			
680	21			
820	22			
1,000	23	1.15 ±0.1		
1,200	24			
1,500	25			
1,800	26			
2,200	27			
2,700	28			
3,300	29			
3,900	31			
4,700	32		1.15 ±0.1	
5,600	33			0.85 ±0.1
6,800	34			
8,200	35			
10,000	36			
12,000	37			1.15 ±0.1
15,000	38			

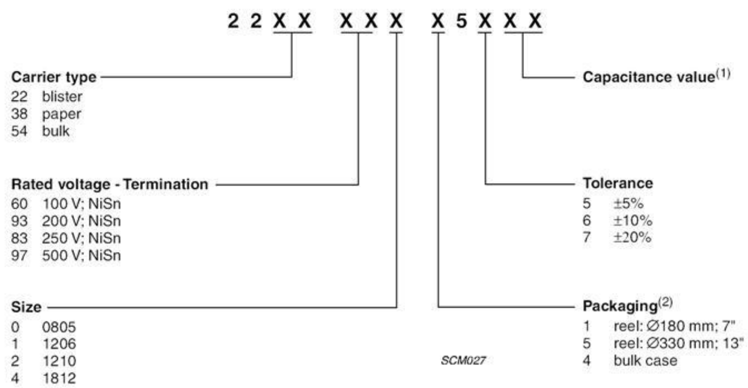
Note

1. Values in shaded cells indicate thickness class in mm.
2. Thickness classification and packing quantities refer to table 2.

ORDERING INFORMATION FOR 100 V, 200 V, 250 V AND 500 V

Components may be ordered by using either a Phycomp's unique 12NC or simple 15-digit clear text code.

Ordering code 12NC (preferred)



(1) Refer to chapters "Selection chart for 100 V" and "Selection chart for 200 V and 500 V".

(2) Quantity on reel depends on thickness classification, see section "Thickness classification and packing quantities".

Clear text code

EXAMPLE: 18122R104KBBB0D

Size Code	Temp. Char.	Capacitance	Tol.	Vol.	Termination	Packing	Marking	Series
0805 1206 1210 1812	2R = X7R	104 = 100000 pF; the third digit signifies the multiplying factor: 1 = × 10 2 = × 100 3 = × 1000 4 = × 10 000	J = ±5% K = ±10% M = ±20%	0 = 100 V B = 200 V C = 250 V D = 500 V	B = NiSn	2 = 180 mm; 7" paper 3 = 330 mm; 13" paper B = 180 mm; 7" blister F = 330 mm; 13" blister P = bulk case	0 = no marking	D = BME

ELECTRICAL CHARACTERISTICS

Class 2 capacitors; X7R dielectric; NiSn terminations

Unless otherwise stated all electrical values apply at an ambient temperature of 25 ±1 °C, an atmospheric pressure of 86 to 105 kPa, and a relative humidity of 63 to 67%.

DESCRIPTION	VALUE
Capacitance range; note 1	100 pF to 1μF
Capacitance tolerance	±20%, ±10%, ±5%
Dissipation factor (D.F.); note 1	≤2.5%; 16 V range ≤3.5%
Insulation resistance after 1 minute at U_r (DC)	$R_{ins} \geq 10$ GΩ or $R_{ins} \times C \geq 500$ seconds whichever is less
Maximum capacitance change as a function of temperature (Temperature characteristic/coefficient; for typical values see Fig.3)	±15%
Operation temperature range	−55 °C to +125 °C

Note

1 Measured at 1 V, 1 kHz, using a four-gauge method.

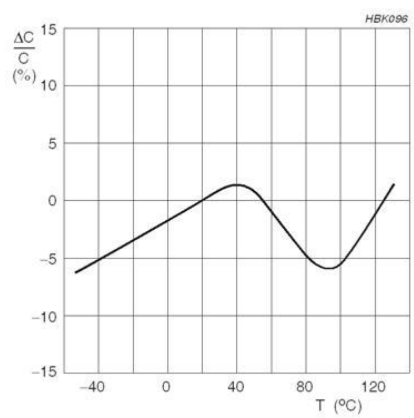
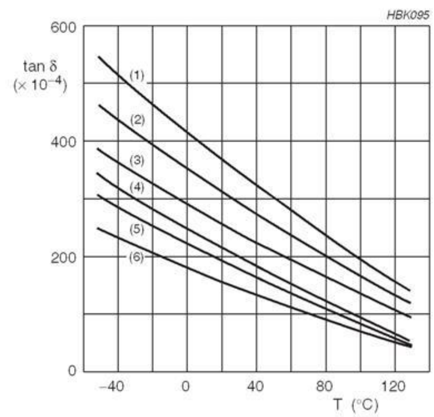


Fig.3 Typical capacitance change as a function of temperature.



Curve 1 = 16 V product.
Curve 2 = 25 V product.
Curve 3 = 50 V product.
Curve 4 = 100 V product.
Curve 5 = 200 V product.
Curve 6 = 500 V product.

Fig.4 Typical tan δ as a function of temperature.

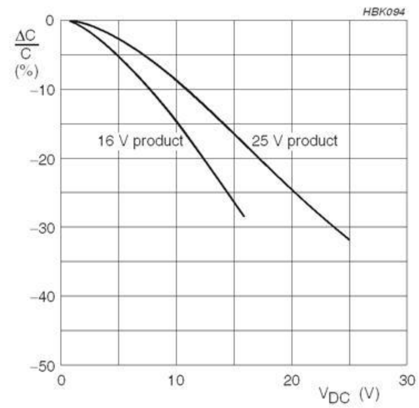


Fig.5 Typical capacitance change with respect to the capacitance at 1 V as a function of DC voltage at 20 °C.

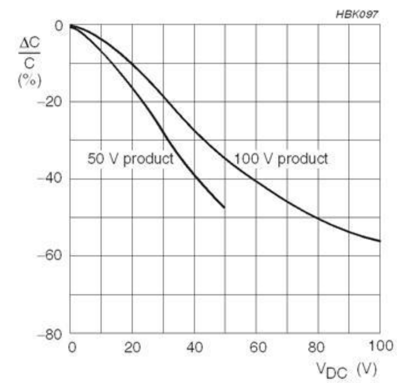


Fig.6 Typical capacitance change with respect to the capacitance at 1 V as a function of DC voltage at 20 °C.

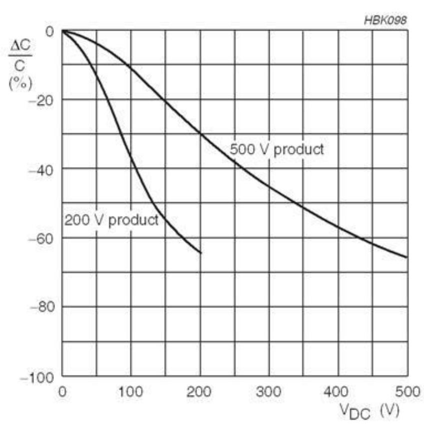


Fig.7 Typical capacitance change with respect to the capacitance at 1 V as a function of DC voltage at 20 °C.

REVISION HISTORY

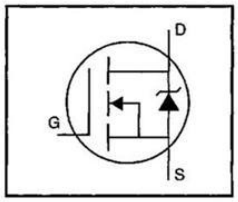
Revision	Date	Change Notification	Description
Rev.9	2005 Aug 17	-	- 0603 50V capacitance range extended to 100 nF
Rev.8	2004 Jul 30	-	- 0402 16V capacitance range extended to 47 nF
Rev.7	2004 Jan 09	-	- Revise for thickness and product range
Rev.6	2002 Aug 28	-	- Capacitance range changed from 2.2 nF
Rev.5	2002 Jul 15 2003 Jun 26	-	- Capacitance range changed from E6 into E12 - Capacitance range expanded to 4.7 µF - Figures 3 through 7 corrected - Updated company logo

PD- 95920

IRFD014PbF

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- For Automatic Insertion
- End Stackable
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free



$V_{DSS} = 60V$

$R_{DS(on)} = 0.20\Omega$

$I_D = 1.7A$

HD-1

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.

Absolute Maximum Ratings

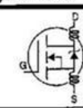
	Parameter	Max.	Units
I_D @ $T_C = 25°C$	Continuous Drain Current, V_{GS} @ 10 V	1.7	A
I_D @ $T_C = 100°C$	Continuous Drain Current, V_{GS} @ 10 V	1.2	
I_{DM}	Pulsed Drain Current ①	14	
P_D @ $T_C = 25°C$	Power Dissipation	1.3	W
	Linear Derating Factor	0.0083	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	130	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

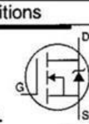
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	120	°C/W

10/27/04

Electrical Characteristics @ $T_J = 25°C$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.063	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.20	Ω	V_{GS}=10V, I_D=1.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	0.96	—	—	S	V_{DS}=25V, I_D=1.0A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=60V, V_{GS}=0V
		—	—	250		V_{DS}=48V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	11	nC	I_D=10A
Q_{gs}	Gate-to-Source Charge	—	—	3.1		V_{DS}=48V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	5.8		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	V_{DD}=30V
t_r	Rise Time	—	50	—		I_D=10A
$t_{d(off)}$	Turn-Off Delay Time	—	13	—		R_G=24Ω
t_f	Fall Time	—	19	—		R_D=2.7Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	6.0	—		
C_{iss}	Input Capacitance	—	310	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	160	—		V_{DS}= 25V
C_{rss}	Reverse Transfer Capacitance	—	37	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.7	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	14		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	T_J=25°C, I_S=1.7A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	70	140	ns	T_J=25°C, I_F=10A
Q_{rr}	Reverse Recovery Charge	—	0.20	0.40	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=25V, starting T_J=25°C, L=52mH R_G=25Ω, I_{AS}=1.7A (See Figure 12)

③ I_{SD}≤10A, di/dt≤90A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤175°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

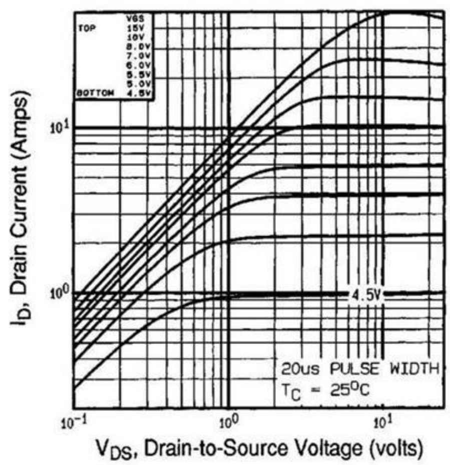


Fig 1. Typical Output Characteristics, TC=25°C

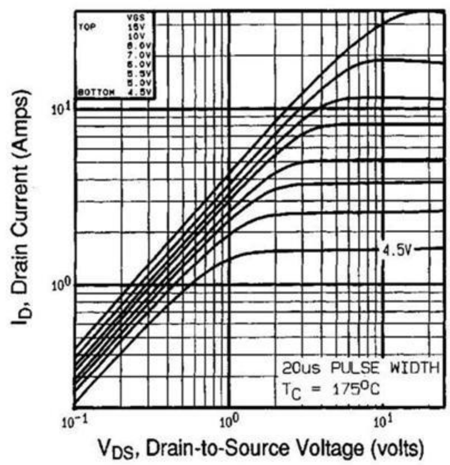


Fig 2. Typical Output Characteristics, TC=175°C

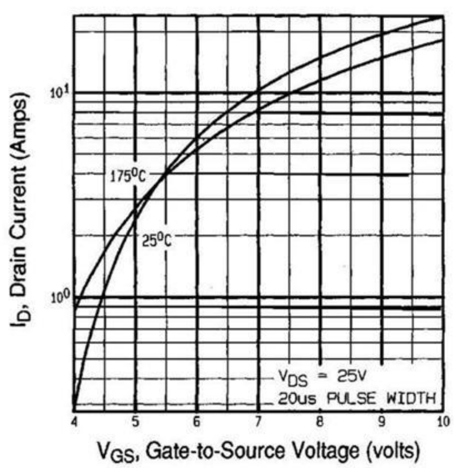


Fig 3. Typical Transfer Characteristics

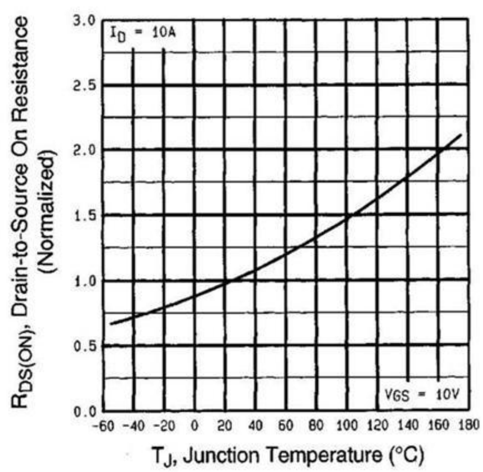


Fig 4. Normalized On-Resistance Vs. Temperature

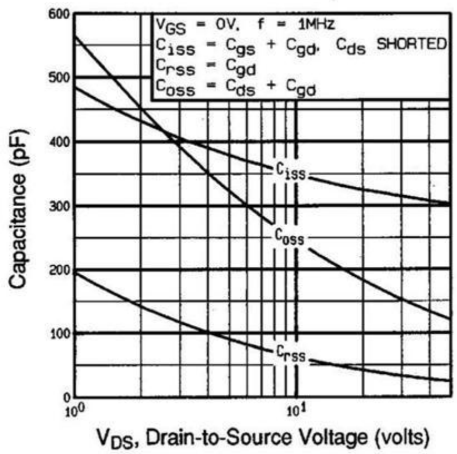


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

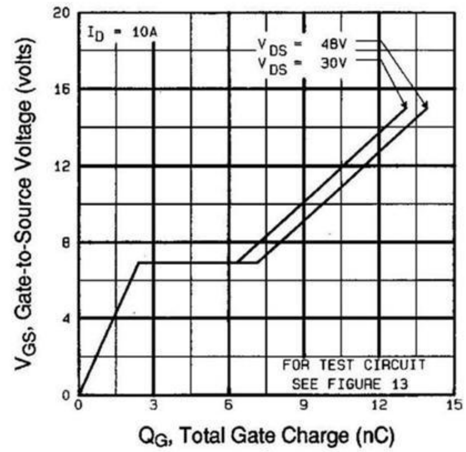


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

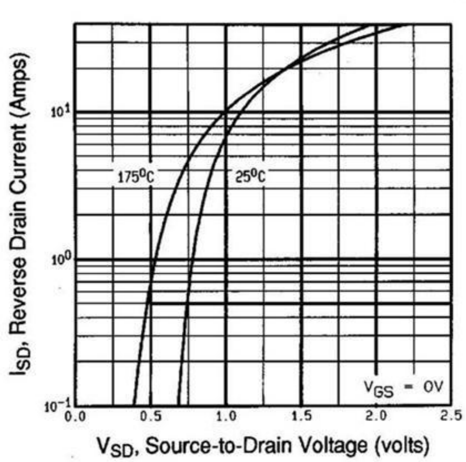


Fig 7. Typical Source-Drain Diode Forward Voltage

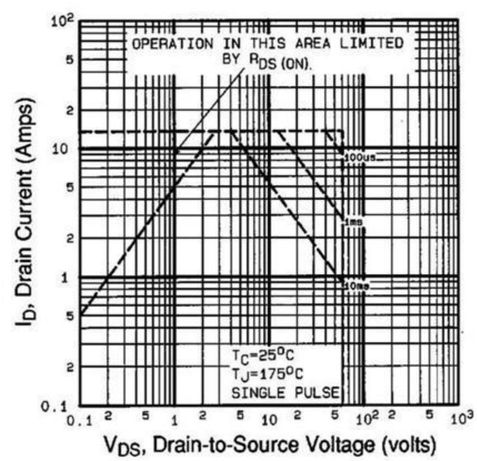


Fig 8. Maximum Safe Operating Area

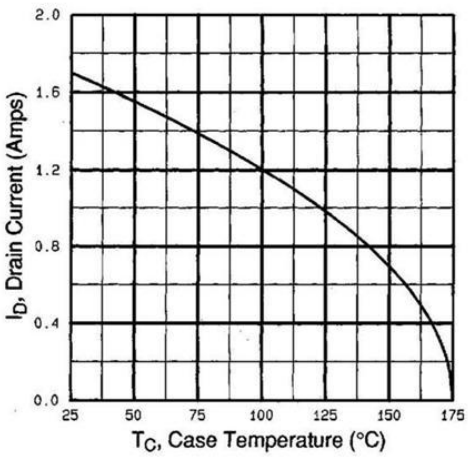


Fig 9. Maximum Drain Current Vs. Case Temperature

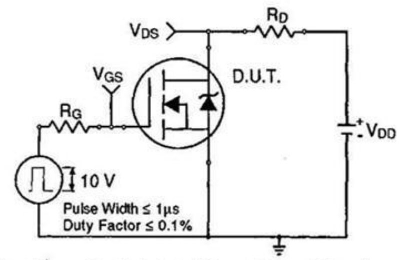


Fig 10a. Switching Time Test Circuit

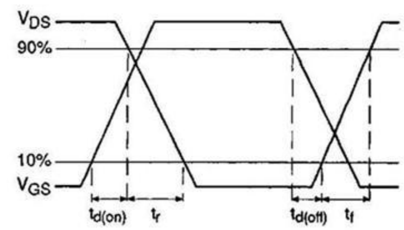


Fig 10b. Switching Time Waveforms

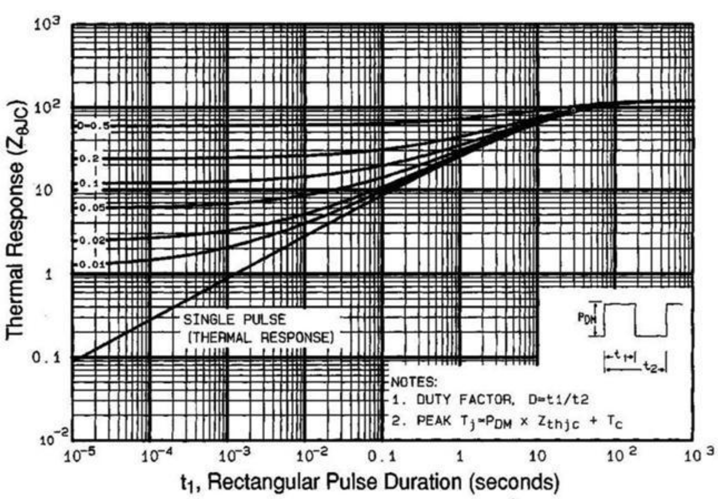


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

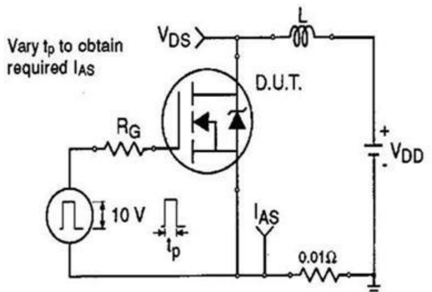


Fig 12a. Unclamped Inductive Test Circuit

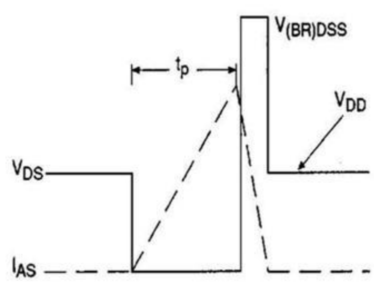


Fig 12b. Unclamped Inductive Waveforms

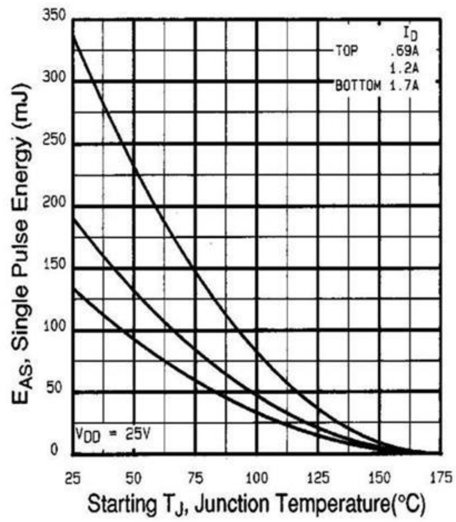


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

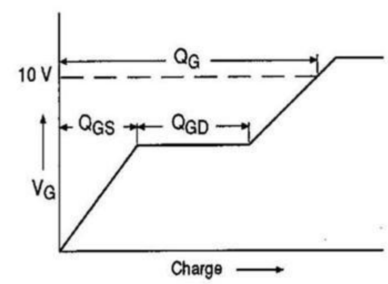


Fig 13a. Basic Gate Charge Waveform

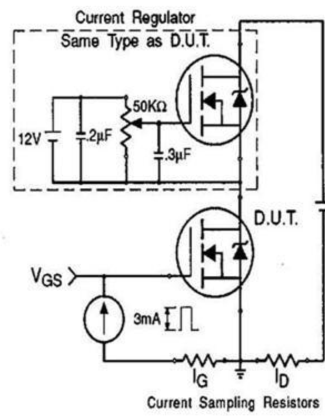
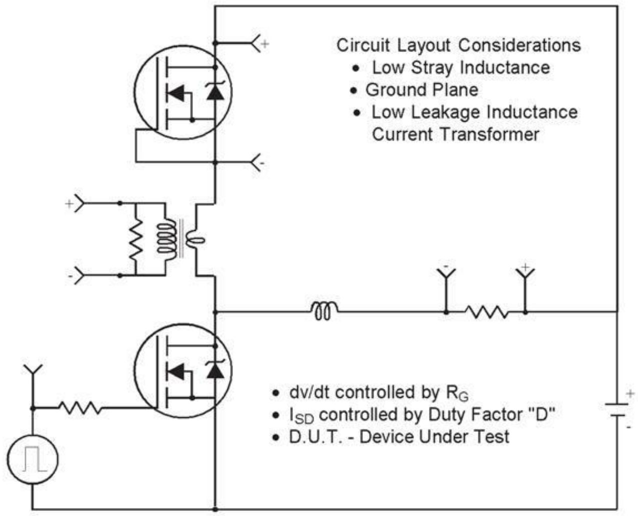
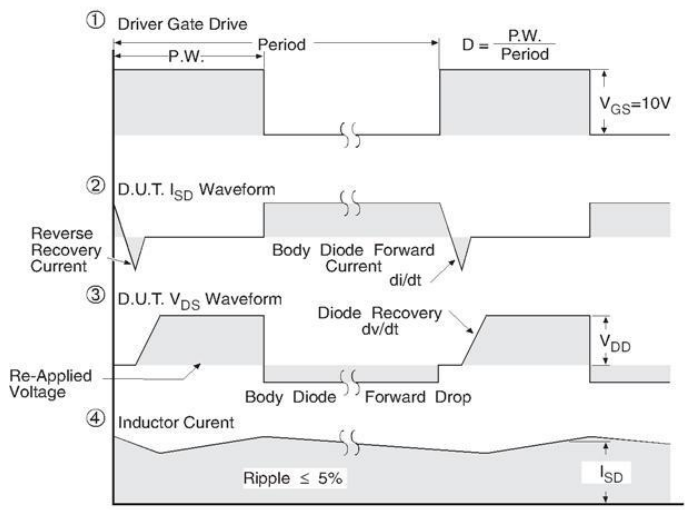


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel
** Use P-Channel Driver for P-Channel Measurements



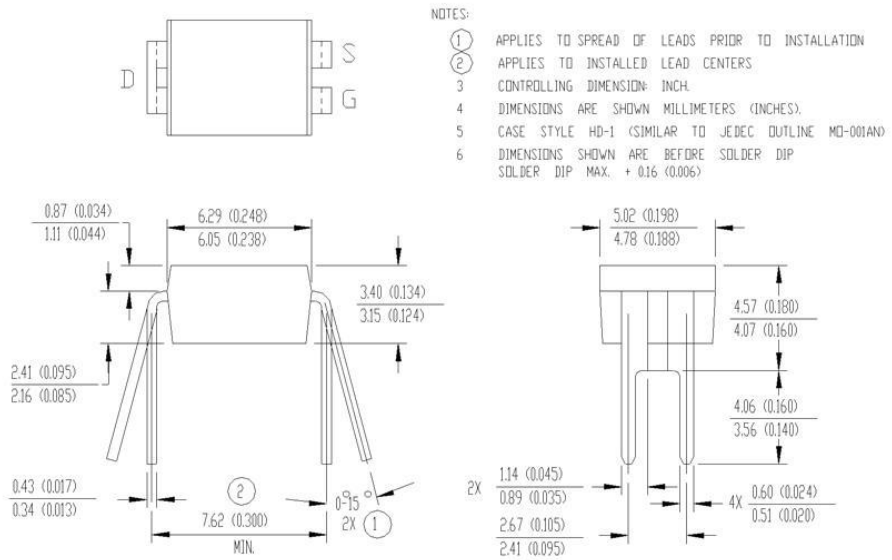
*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig -14 For N Channel HEXFETS

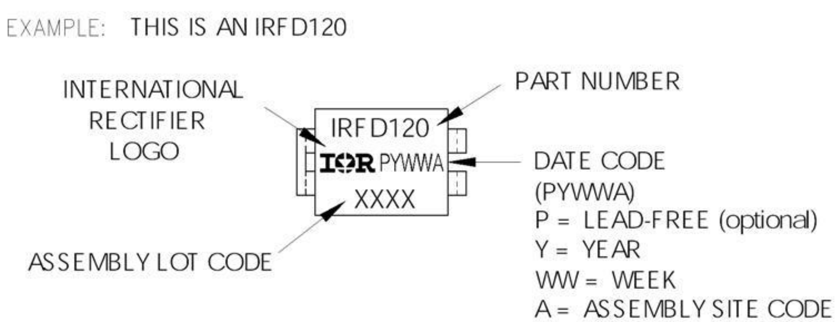
IRFD014PbF

Hexdip Package Outline

Dimensions are shown in millimeters (inches)



Hexdip Part Marking Information



Data and specifications subject to change without notice.

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
10/04

Notice

The products described herein were acquired by Vishay Intertechnology, Inc., as part of its acquisition of International Rectifier's Power Control Systems (PCS) business, which closed in April 2007. Specifications of the products displayed herein are pending review by Vishay and are subject to the terms and conditions shown below.

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

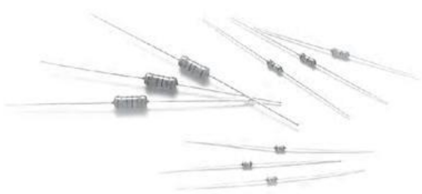
The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.

International Rectifier®, IR®, the IR logo, HEXFET®, HEXSense®, HEXDIP®, DOL®, INTERO®, and POWIRTRAIN® are registered trademarks of International Rectifier Corporation in the U.S. and other countries. All other product names noted herein may be trademarks of their respective owners.

Metal Film Resistors

MFR Type

Normal & Miniature Style [MFR Series]



INTRODUCTION

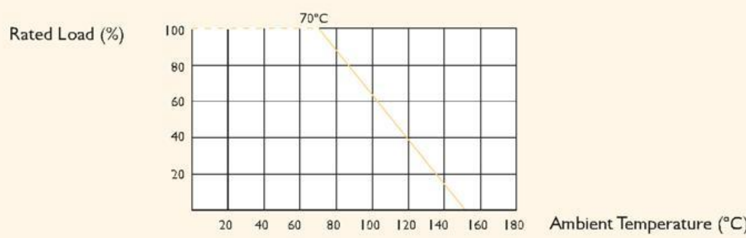
The MFR Series Metal Film Resistors are manufactured using vacuum sputtering system to deposit multiple layers of mixed metals alloy and passivative materials onto a carefully treated high grade ceramic substrate. After a helical groove has been cut in the resistive layer, tinned connecting leads of electrolytic copper are welded to the end-caps. The resistors are coated with layers of blue color lacquer.

FEATURES

Power Rating	1/6W, 1/4W, 1/2W, 1W, 2W, 3W
Resistance Tolerance	±0.5%, ±1%
T.C.R.	±15ppm/°C, ±25ppm/°C, ±50ppm/°C, ±100ppm/°C

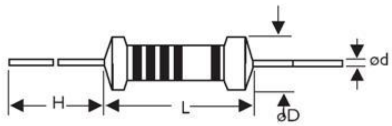
DERATING CURVE

For resistors operated in ambient temperatures above 70°C, power rating must be derated in accordance with the curve below.



DIMENSIONS

Unit : mm



STYLE		DIMENSION			
Normal	Miniature	L	øD	H	ød
MFR-12	MFR25S	3.4±0.3	1.9±0.2	28±2.0	0.45±0.05
MFR-25	MFR50S	6.3±0.5	2.4±0.2	28±2.0	0.55±0.05
MFR-50	MFR1WS	9.0±0.5	3.3±0.3	26±2.0	0.55±0.05
MFR100	MFR2WS	11.5±1.0	4.5±0.5	35±2.0	0.8±0.05
MFR200	MFR3WS	15.5±1.0	5.0±0.5	33±2.0	0.8±0.05

Note :

ELECTRICAL CHARACTERISTICS

STYLE	MFR-12	MFR25S	MFR-25	MFR50S	MFR-50	MFR1WS	MFR100	MFR2WS	MFR200	MFR3WS
Power Rating at 70°C	1/6W	1/4W		1/2W		1W		2W		3W
Maximum Working Voltage	200V		250V	300V	350V	400V	500V			
Maximum Overload Voltage	400V		500V	600V	700V	800V	1000V			
Dielectric Withstanding Voltage	300V	400V	500V			700V	1000V			
Resistance Range	1Ω ~ 10MΩ & 0Ω for E24 & E96 series value									
Operating Temp. Range	- 55°C to + 155°C									
Temperature Coefficient	±15ppm/°C, ±25ppm/°C, ±50ppm/°C, ±100ppm/°C									

* Below or over this resistance range on request.

ENVIRONMENTAL CHARACTERISTICS

PERFORMANCE TEST	TEST METHOD		APPRAISE
Short Time Overload	JIS-C-5202 5.5	2.5 Times RCWV for 5 Seconds	±(0.25%+0.05Ω)
Dielectric Withstanding Voltage	JIS-C-5202 5.7	in V-Block for 60 Seconds	by Type
Temperature Coefficient	JIS-C-5202 5.2	-55°C to +155°C	by Type
Insulation Resistance	JIS-C-5202 5.6	in V-Block	>10000MΩ
Solderability	JIS-C-5202 6.5	260°C ±5°C for 5 ±0.5 Seconds	95% Min. Coverage
Resistance to Solvent	JIS-C-5202 6.9	IPA for 1 Min. with Ultrasonic	No deterioration of Coatings and Markings
Terminal Strength	JIS-C-5202 6.1	Direct load for 10 Sec. In the Direction of the Terminal Leads	≧2.5kg (24.5N)
Pulse Overload	JIS-C-5202 5.8	4 Times RCWV 10000 Cycles (1 Sec. On, 25 Sec. off)	±1.0%+0.05Ω
Load Life in Humidity	JIS-C-5202 7.9	40±2°C, 90~95% RH at RCWV for 1,000 Hrs. (1.5 Hrs. on, 0.5 Hrs. off)	±1.5%+0.05Ω
Load Life	JIS-C-5202 7.10	70°C at RCWV for 1,000 Hrs. (1.5 Hrs. on 0.5 Hrs. off)	±1.5%+0.05Ω
Temperature Cycling	JIS-C-5202 7.4	-55°C→Room Temp.→+155°C→Room Temp. for 5 Cycles	±0.75%+0.05Ω
Resistance to Soldering Heat	JIS-C-5202 6.4	350°C ±10°C for 3±0.5 Seconds	±0.25%+0.05Ω

* Rated Continuous Working Voltage (RCWV)= $\sqrt{\text{Power Rating} \times \text{Resistance Value}}$

Metal Film Resistors

Type: **EROS2 (0.25 W)**
ERO25 (0.25 W)

■ Features

- ● Performance, Reliability······ Low T.C.R. and noise, high reliability
- ● Automatic insertion············· Taping style for automatic inserting machine
- ● Marking······························ 5 color code marking
- ● Reference Standards ········ IEC 60115-2, JIS C 5201-2

■ Explanation of Part Numbers

1	2	3	4	5	6	7	8	9	10	11	12
E	R	O	S	2	C	H	F	1	0	0	2

Product Code (1–3)

Product Code	
Metal Film Resistors	ERO

Power Rating at 70 °C Amb. (4–5)

S2	0.25 W
25	0.25 W

Special Feature and Cut & Formed Style (6)

C	Standard
P	Taped & Box (52 mm)
T	Taped & Box (26 mm)

Temperature Coefficient ×10⁻⁶/°C(ppm/°C) (7)

H	± 50

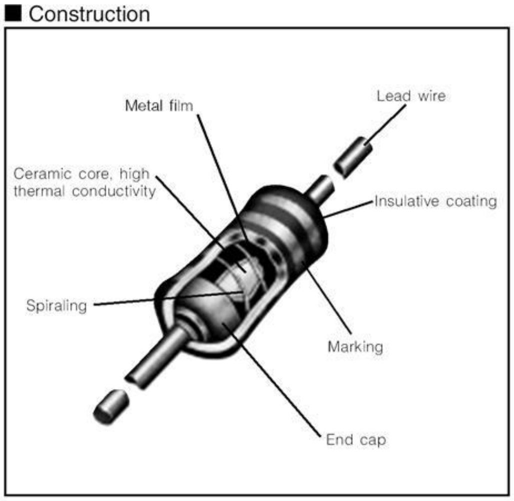
Resistance Tolerance (8)

D	± 0.5 %
F	± 1 %

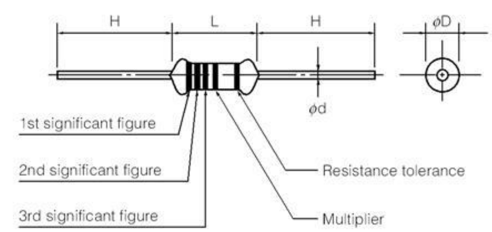
Resistance Value (9–12)

The first three digits are significant figures of resistance and the 4th digit denote number of zeros following.
Decimal point is expressed by R as 97.6 = 97R6.

■ Construction



■ Dimensions in mm (not to scale)



Standard Quantity : 2000 pcs.

Type	Dimensions (mm)				Mass (Weight) [mg/pc.]
	L	ϕD	ϕd	H	
EROS2C	$3.20^{\pm0.20}$	$1.70^{+0.20}_{-0.10}$	$0.45^{\pm0.05}$	$30^{\pm3}$	107
ERO25C	$6.30^{\pm0.50}$	$2.30^{\pm0.50}$	$0.60^{\pm0.05}$	$30^{\pm3}$	228

Design and specifications are each subject to change without notice. Ask factory for the current technical specifications before purchase and/or use.
Should a safety concern arise regarding this product, please be sure to contact us immediately.

Feb. 2006

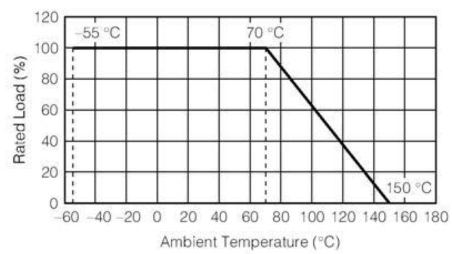
■ Ratings

Type	Power Rating at 70 °C (W)	Limiting Element Voltage (Maximum RCWV)(1) (V)	Maximum Overload Voltage(2) (V)	Dielectric Withstanding Voltage (VAC)	T.C.R. [×10^{-6}/°C (ppm/°C)]	Resistance Tolerance (%)	Resistance Range (Ω) min.	Resistance Range (Ω) max.	Resistance Value
EROS2	0.25	250	500	300	±50	F(±1) D(±0.5)	10	1 M	E24 E96
ERO25	0.25	250	500	500	±50	F(±1) D(±0.5)	10	1 M	E24 E96

(1) Rated Continuous Working Voltage (RCWV) shall be determined from RCWV=$\sqrt{\text{Power Rating}\times\text{Resistance Value}}$, or Limiting Element Voltage (maximum RCWV) listed above, whichever less.
(2) Overload (Short-time Overload) Test Voltage (SOTV) shall be determined from SOTV=2.5×Power Rating or max. Overload Voltage listed above whichever less.

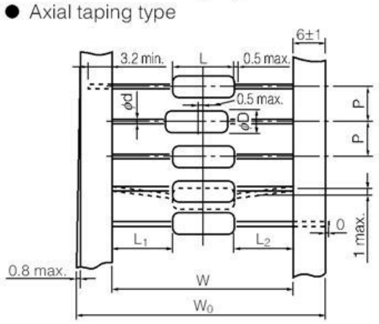
Power Derating Curve

For resistors operated in ambient temperatures above 70 °C, power rating shall be derated in accordance with the figure on the right.



■ Shape and Packaging

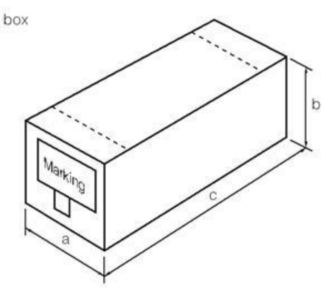
● Axial taping type



Shape	L max.	ϕD max.	ϕd	P ±0.3	W	W0
①	3.4	1.9	0.45	5.0	26^{+1}_{-0}	41.5max.
②	3.4	1.9	0.45	5.0	52±1	64.5±0.5
③	6.5	2.5	0.6	5.0	26^{+1}_{-0}	41.5max.
④	6.5	2.5	0.6	5.0	52±1	64.5±0.5

1 $|L_1-L_2| \leqq 1.0$
2 Cumulative 250±2mm by 50 pitch

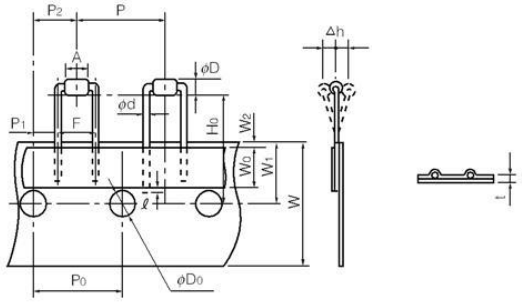
Flat box



Packaging	Shape	Type	Part Numbers	Std. Qty. (pcs./box)	Size of box a×b×c (mm)
26 mm Axial taping	①	Metal Film R	EROS2THO□□□□	5000	52×85×255
52 mm Axial taping	②	Metal Film R	EROS2PHO□□□□	5000	78×85×255
26 mm Axial taping	③	Metal Film R	ERO25THO□□□□	4000	52×95×255
52 mm Axial taping	④	Metal Film R	ERO25PHO□□□□	2000	78×58×255

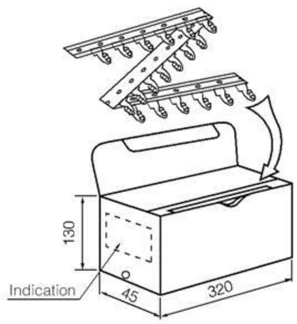
Design and specifications are each subject to change without notice. Ask factory for the current technical specifications before purchase and/or use.
Should a safety concern arise regarding this product, please be sure to contact us immediately.

● Radial Taping for small type



Type	Part Numbers	Std. Qty. (pcs.)
Metal Film R	EROS2GHO□□□□	2000

Dimensions (mm)		Dimensions (mm)		Dimensions (mm)	
P	12.7±1.0	W_0	5 min.	Δh	0±2
P_0	12.7±0.3	W_1	9.0±0.5	t	0.7±0.2
P_1	3.85±0.70	W_2	3 max.	A	3.2±0.2
P_2	6.35±1.00	H_0	$19.0^{+1.0}_{-0.5}$	ϕD	$1.7^{+0.2}_{-0.1}$
F	5.0±0.5	ϕD_0	4.0±0.2	ϕd	0.45±0.05
W	18.0±0.5	ℓ	0 max.		



⚠ Safety Precautions

The following are precautions for individual products. Please also refer to the precautions common to Fixed Resistors shown on page ER3 of this catalog.

1. Keep the rated power and ambient temperature within the specified derating curve.
   * When positioning and mounting Metal Film Resistors (hereafter called the resistors), make allowance for the effect of heat generated through close contact between the resistors and neighboring components and for the temperature rise of adjacent heat-generating components.
2. If a transient load (heavy load in a short time) like a pulse is expected to be applied, check and evaluate the operations of the resistors when installed in your products before use.
   When applying pulses to the resistors, keep the pulse peak within the rated voltage.
3. When the resistors' protective coatings are chipped, flawed, or removed, the characteristics of the resistors may be impaired. Take special care not to apply mechanical shock during automatic mounting or cause damage during handling of the boards with the resistors mounted.
4. Ultrasonic cleaning may cut the lead wire due to resonance. Try and check it before use.

Design and specifications are each subject to change without notice. Ask factory for the current technical specifications before purchase and/or use.
Should a safety concern arise regarding this product, please be sure to contact us immediately.

⚠ Safety Precautions
(Common precautions for Fixed Resistors)

- When using our products, no matter what sort of equipment they might be used for, be sure to make a written agreement on the specifications with us in advance. The design and specifications in this catalog are subject to change without prior notice.
- Do not use the products beyond the specifications described in this catalog.
- This catalog explains the quality and performance of the products as individual components. Before use, check and evaluate their operations when installed in your products.
- Install the following systems for a failsafe design to ensure safety if these products are to be used in equipment where a defect in these products may cause the loss of human life or other significant damage, such as damage to vehicles (automobile, train, vessel), traffic lights, medical equipment, aerospace equipment, electric heating appliances, combustion/gas equipment, rotating equipment, and disaster/crime prevention equipment.

✻ Systems equipped with a protection circuit and a protection device
✻ Systems equipped with a redundant circuit or other system to prevent an unsafe status in the event of a single fault

(1) Precautions for use

- These products are designed and manufactured for general and standard use in general electronic equipment (e.g. AV equipment, home electric appliances, office equipment, information and communication equipment)
- These products are not intended for use in the following special conditions. Before using the products, carefully check the effects on their quality and performance, and determine whether or not they can be used.
  1. In liquid, such as water, oil, chemicals, or organic solvent
  2. In direct sunlight, outdoors, or in dust
  3. In salty air or air with a high concentration of corrosive gas, such as Cl_2, H_2S, NH_3, SO_2, or NO_2
  4. Electric Static Discharge (ESD) Environment
     These components are sensitive to static electricity and can be damaged under static shock (ESD).
     Please take measures to avoid any of these environments.
     Smaller components are more sensitive to ESD environment.
  5. Electromagnetic Environment
     Avoid any environment where strong electromagnetic waves exist.
  6. In an environment where these products cause dew condensation
  7. Sealing or coating of these products or a printed circuit board on which these products are mounted, with resin or other materials
- These products generate Joule heat when energized. Carefully position these products so that their heat will not affect the other components.
- Carefully position these products so that their temperatures will not exceed the category temperature range due to the effects of neighboring heat-generating components. Do not mount or place heat-generating components or inflammables, such as vinyl-coated wires, near these products .
- Note that non-cleaning solder, halogen-based highly active flux, or water-soluble flux may deteriorate the performance or reliability of the products.
- Carefully select a flux cleaning agent for use after soldering. An unsuitable agent may deteriorate the performance or reliability. In particular, when using water or a water-soluble cleaning agent, be careful not to leave water residues. Otherwise, the insulation performance may be deteriorated.

(2) Precautions for storage

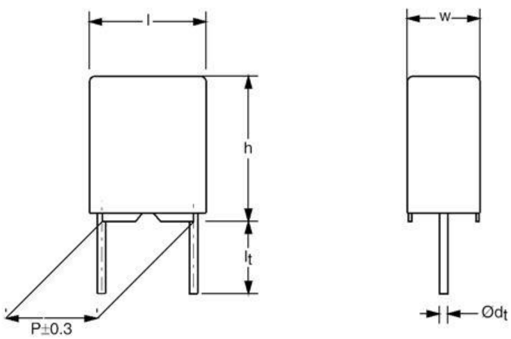
The performance of these products, including the solderability, is guaranteed for a year from the date of arrival at your company, provided that they remain packed as they were when delivered and stored at a temperature of 5 °C to 35 °C and a relative humidity of 45 % to 85 %.

Even within the above guarantee periods, do not store these products in the following conditions. Otherwise, their electrical performance and/or solderability may be deteriorated, and the packaging materials (e.g. taping materials) may be deformed or deteriorated, resulting in mounting failures.

1. In salty air or in air with a high concentration of corrosive gas, such as Cl_2, H_2S, NH_3, SO_2, or NO_2
2. In direct sunlight

<Package markings>
Package markings include the product number, quantity, and country of origin.
In principle, the country of origin should be indicated in English.

Metallized Polypropylene Film Capacitors
MKP Radial Potted Type



Dimensions in mm

FEATURES

5, 10 and 15 mm lead pitch. Supplied loose in box, in ammopack and taped on reel. Intermediate values are available of the E96 series

Lead (Pb)-free product

RoHS-compliant product

Pb-free

e3

RoHS COMPLIANT

APPLICATIONS

Low losses due to low contact resistance and low loss dielectric result in applications where high frequency occur or high stability is preferred. Their small dimensions make them suitable for circuits with high packaging density.

MARKING

C-value; rated voltage; tolerance; code for manufacturer; year and week of manufacture; manufacturers type designation

DIELECTRIC

Polypropylene film

ELECTRODES

Vacuum deposited aluminum

ENCAPSULATION

Flame retardant plastic case and epoxy resin (UL-class 94 V-0)

CONSTRUCTION

Wound mono construction

LEADS

Tinned wire

CAPACITANCE RANGE (E24 SERIES)

0.001 to 1.2 µF

CAPACITANCE TOLERANCE

± 5 %; ± 2 %

RATED (DC) VOLTAGE

63 V; 160 V; 250 V; 400 V; 630 V

RATED (AC) VOLTAGE

25 V; 63 V;100 V; 125 V; 160 V

RATED PEAK-TO-PEAK VOLTAGE

70 V; 180 V; 280 V; 350 V; 450 V

CLIMATIC CATEGORY

55/085/56

RATED TEMPERATURE (DC)

85 °C

RATED TEMPERATURE (AC)

85 °C

MAXIMUM APPLICATION TEMPERATURE

85 °C

REFERENCE SPECIFICATIONS

IEC 60384-16

PERFORMANCE GRADE

Grade 1 (long life)

STABILITY GRADE

Grade 1

DETAIL SPECIFICATION

For more detailed data and test requirements contact: filmcaps.roeselare@vishay.com

COMPOSITION OF CATALOG NUMBER

TYPE AND PITCHES	
416	5.0/10.0/15.0 mm
417	5.0/10.0/15.0 mm
418	5.0/10.0/15.0 mm
419	5.0/10.0/15.0 mm
420	5.0/10.0/15.0 mm

CAPACITANCE (numerically)

MULTIPLIER (nF)	
0.01	2
0.1	3
1	4

Example:
1004 = 100 x 1 = 100 nF

2222	4..	XX	XX	X
BFC2*	4..	XX	XX	X

* Use this partnumber for those with access to the Vishay's SAP system and Partners website within the Americas

TYPE	PACKAGING	PITCH (mm)	LEAD CONFIGURATION	PREFERRED TYPES					
				C-TOL	63 V	160 V	250 V	400 V	630 V
416	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 2 %	1				
	Loose in box	15	lead length 3.5 ± 0.3 mm	± 2 %	7				
417	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 2 %		1			
	Loose in box	15	lead length 3.5 ± 0.3 mm	± 2 %		7			
418	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 2 %			1		
	Loose in box	15	lead length 3.5 ± 0.3 mm	± 2 %			7		
419	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 2 %				1	
	Loose in box	15	lead length 3.5 ± 0.3 mm	± 2 %				7	
420	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 2 %					1
	Loose in box	15	lead length 3.5 ± 0.3 mm	± 2 %					7
				ON REQUEST					
416	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 5 %	0				
	Loose in box	5/10	lead length 4.0 + 1.0/– 0.5 mm	± 5 %	3				
				± 2 %	4				
		15	lead length 3.5 ± 0.3 mm	± 5 %	6				
417	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 5 %		0			
	Loose in box	5/10	lead length 4.0 + 1.0/– 0.5 mm	± 5 %		3			
				± 2 %		4			
		15	lead length 3.5 ± 0.3 mm	± 5 %		6			
418	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 5 %			0		
	Loose in box	5/10	lead length 4.0 + 1.0/– 0.5 mm	± 5 %			3		
				± 2 %			4		
		15	lead length 3.5 ± 0.3 mm	± 5 %			6		
419	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 5 %				0	
	Loose in box	5/10	lead length 4.0 + 1.0/– 0.5 mm	± 5 %				3	
				± 2 %				4	
		15	lead length 3.5 ± 0.3 mm	± 5 %				6	
420	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 5 %					0
	Loose in box	5/10	lead length 4.0 + 1.0/– 0.5 mm	± 5 %					3
				± 2 %					4
		15	lead length 3.5 ± 0.3 mm	± 5 %					6

Note:
Pitch = 5 and 10 mm: taped on ammopack
Pitch = 15 mm: taped on reel with diameter = 356 mm

SPECIFIC REFERENCE DATA

DESCRIPTION	VALUE	
Tangent of loss angle:	at 10 kHz	at 100 kHz
C ≤ 0.0091 μF	$\leq 5 \times 10^{-4}$	$\leq 10 \times 10^{-4}$
0.0091 μF < C ≤ 0.027 μF	$\leq 5 \times 10^{-4}$	$\leq 15 \times 10^{-4}$
0.027 μF < C ≤ 0.075 μF	$\leq 5 \times 10^{-4}$	$\leq 20 \times 10^{-4}$
0.075 μF < C ≤ 0.11 μF	$\leq 5 \times 10^{-4}$	$\leq 25 \times 10^{-4}$
0.11 μF < C ≤ 0.18 μF	$\leq 10 \times 10^{-4}$	$\leq 30 \times 10^{-4}$
0.18 μF < C ≤ 0.27 μF	$\leq 10 \times 10^{-4}$	$\leq 35 \times 10^{-4}$
0.27 μF < C ≤ 0.39 μF	$\leq 10 \times 10^{-4}$	$\leq 40 \times 10^{-4}$
0.39 μF < C ≤ 0.56 μF	$\leq 10 \times 10^{-4}$	$\leq 45 \times 10^{-4}$
0.56 μF < C ≤ 0.75 μF	$\leq 10 \times 10^{-4}$	$\leq 50 \times 10^{-4}$
0.75 μF < C ≤ 1.1 μF	$\leq 10 \times 10^{-4}$	$\leq 60 \times 10^{-4}$

DESCRIPTION	VALUE				
Rated voltage pulse slope $(dU/dt)_R$:	at 63 V (DC)	at 100 V (DC)	at 250 V (DC)	at 400 V (DC)	at 630 V (DC)
P = 5 mm	50 V/μs	50 V/μs	50 V/μs	50 V/μs	50 V/μs
P = 10 mm	20 V/μs	20 V/μs	20 V/μs	20 V/μs	50 V/μs
P = 15 mm	50 V/μs	50 V/μs	50 V/μs	50 V/μs	50 V/μs
R between leads, for C ≤ 0.33 μF:					
at 50 V; 1 minute	> 100000 MΩ				
at 100 V; 1 minute		> 100000 MΩ	> 100000 MΩ	> 100000 MΩ	> 100000 MΩ
RC between leads, for C > 0.33 μF at 10 V; 1 minute	> 30000 s	>30000 s	>30000 s	>30000 s	
R between interconnecting leads and casing; 50 V; 1 minute	> 100000 MΩ	> 100000 MΩ	> 100000 MΩ	> 100000 MΩ	> 100000 MΩ
Withstanding (DC) voltage (cut off current 10 mA); rise time 100 V/s	100 V; 1 minute	260 V; 1 minute	400 V; 1 minute	640 V; 1 minute	1000 V; 1 minute
Withstanding (DC) voltage between leads and case	2840 V; 1 minute	2840 V; 1 minute	2840 V; 1 minute	2840 V; 1 minute	1260 V; 1 minute

U_{Rdc} = 63 V; U_{Rac} = 25 V; U_{p-p} = 70 V

C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 416 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		It = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		It = 3.5 ± 0.3 mm	
			C-tol = ± 2 % last 5 digits of catalog number	SPQ	C-tol = ± 2 % last 5 digits of catalog number	SPQ	C-tol = ± 2 % last 5 digits of catalog number	SPQ	C-tol = ± 2 % last 5 digits of catalog number	SPQ
Pitch = 5.0 ± 0.3 mm; d_t = 0.50 ± 0.05 mm										
0.036	4.5 × 9.0 × 7.2	0.45	13603	1000	43603	2000				
0.039			13903		43903					
0.043			14303		44303					
0.047			14703		44703					
0.051	6.0 × 11.0 × 7.2	0.60	15103	750	45103	1500				
0.056			15603		45603					
0.062			16203		46203					
0.068			16803		46803					
0.075			17503		47503					
0.082			18203		48203					
0.091			19103		49103					
0.1			11004		41004					
0.11			11104		41104					
0.12			11204		41204					
Pitch = 10.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.13	5.0 × 11.0 × 12.5	0.85	11304	600	41304	1000				
0.15			11504		41504					
0.16	6.0 × 12.0 × 12.5	1.10	11604	500	41604	750				
0.18			11804		41804					
0.20			12004		42004					
0.22			12204		42204					
0.24			12404		42404					
0.27			12704		42704					
Pitch = 15.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.3	6.0 × 12.0 × 17.5	1.4					13004	900	73004	1000
0.33							13304		73304	
0.36							13604		73604	
0.39							13904		73904	
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm										
0.43	7.0 × 13.5 × 17.5	1.9					14304	800	74304	750
0.47							14704		74704	
0.51							15104		75104	
0.56							15604		75604	
0.62	8.5 × 15.0 × 17.5	2.6					16204	650	76204	750
0.68							16804		76804	
0.75							17504		77504	
0.82							18204		78204	
0.91	10.0 × 16.5 × 17.5	3.1					19104	600	79104	500
1.0							11005		71005	
1.1							11105		71105	

U_{Rdc} = 160 V; U_{Rac} = 63 V; U_{p-p} = 180 V

C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 417 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		It = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		It = 3.5 ± 0.3 mm	
			C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %	
			last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ
Pitch = 5.0 ± 0.3 mm; d_t = 0.50 ± 0.05 mm										
0.024	4.5 × 9.0 × 7.2	0.45	12403	1000	42403	2000				
0.027			12703		42703					
0.03			13003		43003					
0.033			13303		43303					
0.036	6.0 × 11.0 × 7.2	0.60	13603	750	43603	1500				
0.039			13903		43903					
0.043			14303		44303					
0.047			14703		44703					
0.051			15103		45103					
0.056			15603		45603					
0.062			16203		46203					
0.068			16803		46803					
Pitch = 10.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.075	4.0 × 10.0 × 12.5	0.60	17503	750	47503	1000				
0.082			18203		48203					
0.091			19103		49103					
0.1			11004		41004					
0.11	5.0 × 11.0 × 12.5	0.85	11104	600	41104	1000				
0.12			11204		41204					
0.13			11304		41304					
0.15			11504		41504					
0.16	6.0 × 12.0 × 12.5	1.10	11604	500	41604	750				
0.18			11804		41804					
0.20			12004		42004					
0.22			12204		42204					
0.24			12404		42404					
Pitch = 15.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.27	5.0 × 11.0 × 17.5	1.2					12704	1100	72704	1250
0.3	6.0 × 12.0 × 17.5	1.4					13004	900	73004	1000
0.33							13304		73304	
0.36							13604		73604	
0.39							13904		73904	
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm										
0.43	7.0 × 13.5 × 17.5	1.9					14304	800	74304	750
0.47							14704		74704	
0.51							15104		75104	
0.56							15604		75604	
0.62	8.5 × 15.0 × 17.5	2.6					16204	650	76204	750
0.68							16804		76804	
0.75							17504		77504	
0.82							18204		78204	
0.91	10.0 × 16.5 × 17.5	3.1					19104	600	79104	500
1.0							11005		71005	
1.1							11105		71105	

Metallized Polypropylene Film Capacitors
MKP Radial Potted Type

U_{Rdc} = 250 V; U_{Rac} = 25 V; U_{p-p} = 70 V

C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 418 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		It = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		It = 3.5 ± 0.3 mm	
			C-tol = ± 2 % last 5 digits of catalog number	SPQ	C-tol = ± 2 % last 5 digits of catalog number	SPQ	C-tol = ± 2 % last 5 digits of catalog number	SPQ	C-tol = ± 2 % last 5 digits of catalog number	SPQ
Pitch = 5.0 ± 0.3 mm; d_t = 0.50 ± 0.05 mm										
0.01	3.5 × 8.0 × 7.2	0.35	11003	1500	41003	3000				
0.011			11103		41103					
0.012			11203		41203					
0.013			11303		41303					
0.015			11503		41503					
0.016	4.5 × 9.0 × 7.2	0.45	11603	1000	41603	2000				
0.018			11803		41803					
0.02			12003		42003					
0.022			12203		42203					
0.024			12403		42403					
0.027	6.0 × 11.0 × 7.2	0.60	12703	750	42703	1500				
0.03			13003		43003					
0.033			13303		43303					
0.036			13603		43603					
0.039			13903		43903					
0.043			14303		44303					
Pitch = 10.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.047	4.0 × 10.0 × 12.5	0.60	14703	750	44703	1000				
0.051			15103		45103					
0.056			15603		45603					
0.062			16203		46203					
0.068			16803		46803					
0.075	5.0 × 11.0 × 12.5	0.85	17503	600	47503	1000				
0.082			18203		48203					
0.091			19103		49103					
0.1	6.0 × 12.0 × 12.5	1.10	11004	500	41004	750				
0.11			11104		41104					
0.12			11204		41204					
0.13			11304		41304					
Pitch = 15.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.15	5.0 × 11.0 × 17.5	1.2					11504	1100	71504	1250
0.16							11604		71604	
0.18	6.0 × 12.0 × 17.5	1.4					11804	900	71804	1000
0.2							12004		72004	
0.22							12204		72204	
0.24							12404		72404	
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm										
0.27	7.0 × 13.5 × 17.5	1.9					12704	800	72704	750
0.3							13004		73004	
0.33							13304		73304	
0.36							13604		73604	
0.39	8.5 × 15.0 × 17.5	2.6					13904	650	73904	750
0.43							14304		74304	
0.47							14704		74704	
0.51							15104		75104	
0.56	10.0 × 16.5 × 17.5	3.1					15604	600	75604	500
0.62							16204		76204	
0.68							16804		76804	

U_{Rdc} = 400 V; U_{Rac} = 125 V; U_{p-p} = 350 V

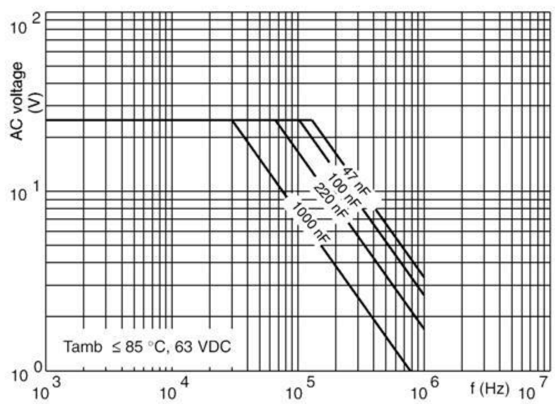
C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 419 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		It = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		It = 3.5 ± 0.3 mm	
			C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %	
			last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ
Pitch = 5.0 ± 0.3 mm; d_t = 0.50 ± 0.05 mm										
0.001	3.5 × 8.0 × 7.2	0.35	11002	1500	41002	3000				
0.0011			11102		41102					
0.0012			11202		41202					
0.0013			11302		41302					
0.0015			11502		41502					
0.0016			11602		41602					
0.0018			11802		41802					
0.002			12002		42002					
0.0022			12202		42202					
0.0024			12402		42402					
0.0027			12702		42702					
0.003			13002		43002					
0.0033			13302		43302					
0.0036			13602		43602					
0.0039			13902		43902					
0.0043	4.5 × 9.0 × 7.2	0.45	14302	1000	44302	2000				
0.0047			14702		44702					
0.0051			15102		45102					
0.0056			15602		45602					
0.0062			16202		46202					
0.0068			16802		46802					
0.0075			17502		47502					
0.0082			18202		48202					
0.0091			19102		49102					
0.01			11003		41003					
0.011			11103		41103					
0.012			11203		41203					
0.013	6.0 × 11.0 × 7.2	0.60	11303	750	41303	1500				
0.015			11503		41503					
0.016			11603		41603					
0.018			11803		41803					
0.02			12003		42003					
Pitch = 10.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.022	4.0 × 10.0 × 12.5	0.60	12203	750	42203	1000				
0.024			12403		42403					
0.027			12703		42703					
0.03			13003		43003					
0.033			13303		43303					
0.036	5.0 × 11.0 × 12.5	0.85	13603	600	43603	1000				
0.039			13903		43903					
0.043			14303		44303					

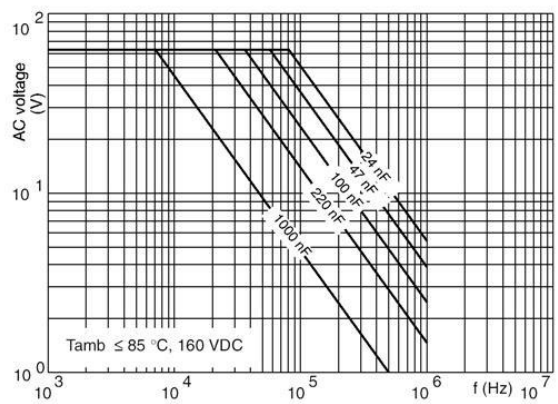
C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 419 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		lt = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		lt = 3.5 ± 0.3 mm	
			C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %	
			last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ
0.047			14703		44703					
0.051			15103		45103					
0.056	6.0 × 12.0 × 12.5	1.10	15603	500	45603	750				
0.062			16203		46203					
0.068			16803		46803					
Pitch = 15.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.075	5.0 × 11.0 × 17.5	1.2					17503	1100	77503	1250
0.082							18203		78203	
0.091							19103		79103	
0.1							11004		71004	
0.11	6.0 × 12.0 × 17.5	1.4					11104	900	71104	1000
0.12							11204		71204	
0.13							11304		71304	
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm										
0.15							11504		71504	
0.16	7.0 × 13.5 × 17.5	1.9					11604	800	71604	750
0.18							11804		71804	
0.2							12004		72004	
0.22	8.5 × 15.0 × 17.5	2.6					12204	650	72204	750
0.24							12404		72404	
0.27							12704		72704	
0.3							13004		73004	
0.33	10.0 × 16.5 × 17.5	3.1					13304	600	73304	500
0.36							13604		73604	

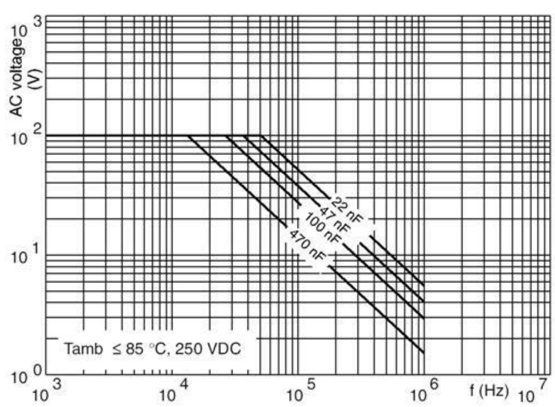
U_{Rdc} = 630 V; U_{Rac} = 160 V; U_{p-p} = 450 V

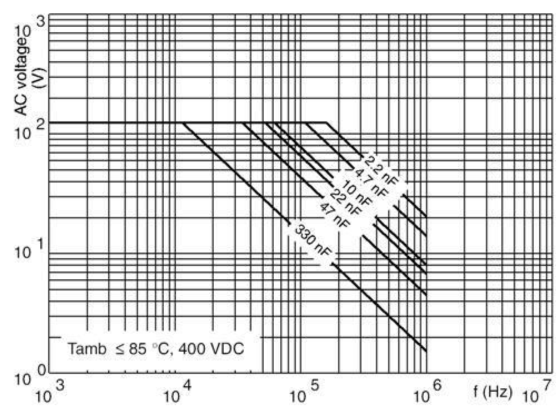
C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 420 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		It = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		It = 3.5 ± 0.3 mm	
			C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %	
			last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ
Pitch = 5.0 ± 0.3 mm; d_t = 0.50 ± 0.05 mm										
0.0015	3.5 × 8.0 × 7.2	0.35	11502	1500	41502	3000				
0.0016			11602		41602					
0.0018			11802		41802					
0.002			12002		42002					
0.0022			12202		42202					
0.0024			12402		42402					
0.0027			12702		42702					
0.003	4.5 × 9.0 × 7.2	0.45	13002	1000	43002	2000				
0.0033			13302		43302					
0.0036			13602		43602					
0.0039			13902		43902					
0.0043	6.0 × 11.0 × 7.2	0.60	14302	750	44302	1500				
0.0047			14702		44702					
0.0051			15102		45102					
0.0056			15602		45602					
0.0062			16202		46202					
0.0068			16802		46802					
Pitch = 10.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.01	4.0 × 10.0 × 12.5	0.60	11003	750	41003	1000				
0.011			11103		41103					
0.012			11203		41203					
0.013			11303		41303					
0.015			11503		41503					
0.016			11603		41603					
0.018	5.0 × 11.0 × 12.5	0.85	11803	600	41803	1000				
0.02			12003		42003					
0.022			12203		42203					
0.024			12403		42403					
0.027	6.0 × 12.0 × 12.5	1.10	12703	500	42703	750				
0.03			13003		43003					
0.033			13303		43303					
0.036			13603		43603					
0.039			13903		43903					
0.043			14303		44303					
0.047			14703		44703					
Pitch = 15.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.051	6.0 × 12.0 × 17.5	1.4					15103	900	75103	1000
0.056							15603		75603	
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm										
0.062	7.0 × 13.5 × 17.5	1.9					16203	800	76203	750
0.068							16803		76803	
0.075							17503		77503	
0.082							18203		78203	
0.091	8.5 × 15.0 × 17.5	2.6					19103	650	79103	750
0.1							11004		71004	
0.11							11104		71104	
0.12							11204		71204	
0.13	10.0 × 16.5 × 17.5	3.1					11304	600	71304	500
0.15							11504		71504	
0.16							11604		71604	

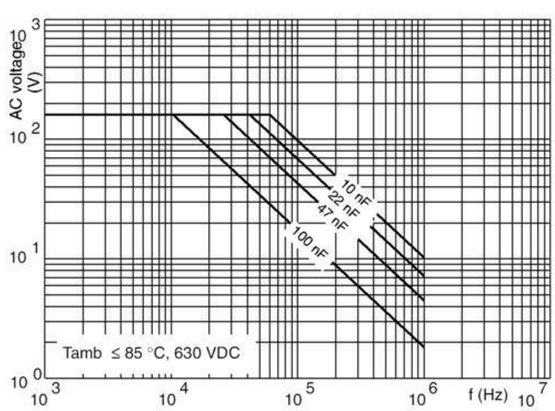
MAXIMUM RMS VOLTAGE (SINEWAVE) AS A FUNCTION OF FREQUENCY



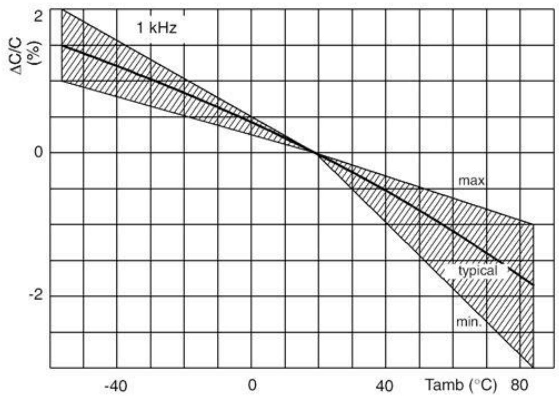




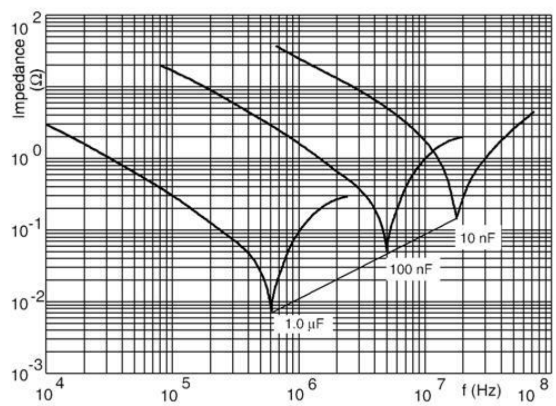




CAPACITANCE



IMPEDANCE

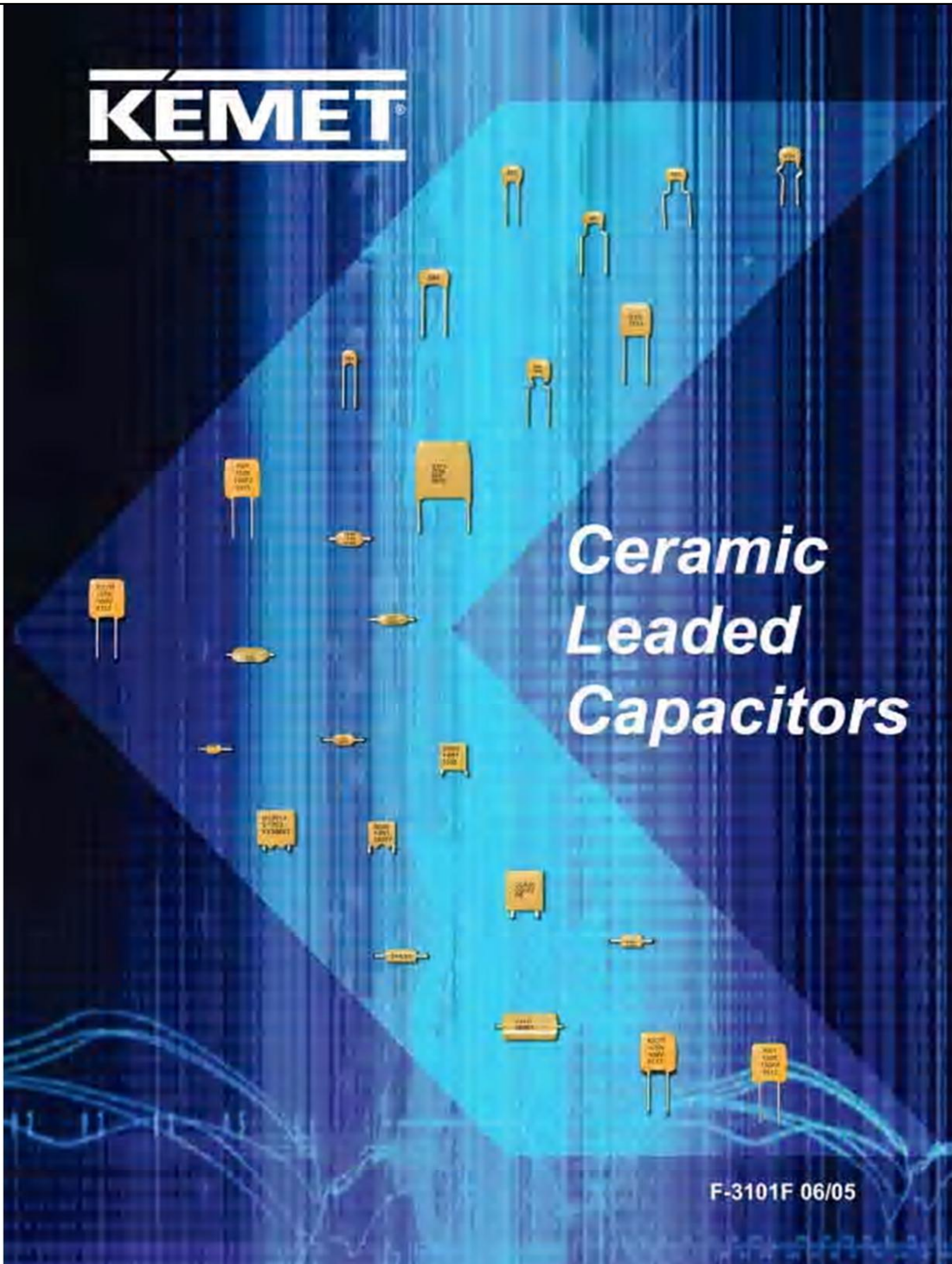


Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.


KEMET
Ceramic
Leaded
Capacitors
F-3101F 06/05

INDEX

NOTICE

Although the information in this catalog has been carefully checked for accuracy, and is believed to be correct and current, no warranty, either express or implied, is made as to either its applicability to, or its compatibility with, specific requirements; nor does KEMET Electronics Corporation assume any responsibility for correctness of this information, nor for damages consequent to its use. All design characteristics, specifications, tolerances, and the like are subject to change without notice.

Multilayer ceramic capacitors are available in a variety of physical sizes and configurations, including leaded devices and surface mounted chips. Leaded styles include molded and conformally coated parts with axial and radial leads. However, the basic capacitor element is similar for all styles. It is called a chip and consists of formulated dielectric materials which have been cast into thin layers, interspersed with metal electrodes alternately exposed on opposite edges of the laminated structure. The entire structure is fired at high temperature to produce a monolithic block which provides high capacitance values in a small physical volume. After firing, conductive terminations are applied to opposite ends of the chip to make contact with the exposed electrodes. Termination materials and methods vary depending on the intended use.

TEMPERATURE CHARACTERISTICS

Ceramic dielectric materials can be formulated with a wide range of characteristics. The EIA standard for ceramic dielectric capacitors (RS-198) divides ceramic dielectrics into the following classes:

Class I: Temperature compensating capacitors, suitable for resonant circuit application or other applications where high Q and stability of capacitance characteristics are required. Class I capacitors have predictable temperature coefficients and are not effected by voltage, frequency or time. They are made from materials which are not ferro-electric, yielding superior stability but low volumetric efficiency. Class I capacitors are the most stable type available, but have the lowest volumetric efficiency.

Class II: Stable capacitors, suitable for bypass or coupling applications or frequency discriminating circuits where Q and stability of capacitance characteristics are not of major importance. Class II capacitors have temperature characteristics of ± 15% or less. They are made from materials which are ferro-electric, yielding higher volumetric efficiency but less stability. Class II capacitors are affected by temperature, voltage, frequency and time.

Class III: General purpose capacitors, suitable for by-pass coupling or other applications in which dielectric losses, high insulation resistance and stability of capacitance characteristics are of little or no importance. Class III capacitors are similar to Class II capacitors except for temperature characteristics, which are greater than ± 15%. Class III capacitors have the highest volumetric efficiency and poorest stability of any type.

KEMET leaded ceramic capacitors are offered in the three most popular temperature characteristics:

C0G: Class I, with a temperature coefficient of 0 ± 30 ppm per degree C over an operating temperature range of - 55°C to + 125°C (Also known as “NP0”).

X7R: Class II, with a maximum capacitance change of ± 15% over an operating temperature range of - 55°C to + 125°C.

Z5U: Class III, with a maximum capacitance change of + 22% - 56% over an operating temperature range of + 10°C to + 85°C.

Specified electrical limits for these three temperature characteristics are shown in Table 1.

SPECIFIED ELECTRICAL LIMITS

PARAMETER	TEMPERATURE CHARACTERISTICS		
	C0G	X7R	Z5U
Dissipation Factor: Measured at following conditions: C0G — 1 kHz and 1 vrms if capacitance > 1000 pF 1 MHz and 1 vrms if capacitance ≤ 1000 pF X7R — 1 kHz and 1 vrms* or if extended cap range 0.5 vrms Z5U — 1 kHz and 0.5 vrms	0.15%	2.5%	4.0%
Dielectric Strength: 2.5 times rated DC voltage.	Pass Subsequent IR Test		
Insulation Resistance (IR): At rated DC voltage, whichever of the two is smaller	1,000 MΩ-μF or 100 GΩ	1,000 MΩ-μF or 100 GΩ	1,000 MΩ-μF or 10 GΩ
Temperature Characteristics: Range, °C Capacitance Change without DC voltage	-55 to +125 0 ± 30 ppm/°C	-55 to +125 ±15%	+10 to +85 +22%, -56%

* 1 MHz and 1 vrms if capacitance ≤ 100 pF on military product.

Table I

GENERAL SPECIFICATIONS

Working Voltage:

	Axial (WVDC)	Radial (WVDC)
C0G	50 & 100	50, 100, 200, 500, 1k, 1.5k, 2k, 2.5k, 3k
X7R	50 & 100	50, 100, 200, 500, 1k, 1.5k, 2k, 2.5k, 3k
Z5U	50 & 100	50 & 100

Temperature Characteristics:
C0G – 0 ± 30 PPM / °C from - 55°C to + 125°C (1)
X7R – ± 15% from - 55°C to + 125°C
Z5U – + 22% / -56% from + 10°C to + 85°C

Capacitance Tolerance:
C0G – ±0.5pF, ±1%, ±2%, ±5%, ±10%
X7R – ±10%, ±20%, +80% / -20%, +100% / -0%
Z5U – ±20%, +80% / -20%

Construction:
Epoxy encapsulated - meets flame test requirements of UL Standard 94V-0.
High-temperature solder - meets EIA RS-198, Method 302, Condition B (260°C for 10 seconds)

Lead Material:
100% matte tin (Sn) with nickel (Ni) underplate and steel core.

Solderability:
EIA RS-198, Method 301, Solder Temperature: 230°C ±5°C.
Dwell time in solder = 7 ± ½ seconds.

Terminal Strength:
EIA RS-198, Method 303, Condition A (2.2kg)

ELECTRICAL

Capacitance @ 25°C:
Within specified tolerance and following test conditions.
C0G – > 1000pF with 1.0 vrms @ 1 kHz
≤ 1000pF with 1.0 vrms @ 1 MHz
X7R – with 1.0 vrms @ 1 kHz
Z5U – with 1.0 vrms @ 1 kHz

Dissipation Factor @ 25°C:
Same test conditions as capacitance.
C0G – 0.15% maximum
X7R – 2.5% maximum
Z5U – 4.0% maximum

Insulation Resistance @ 25°C:
EIA RS-198, Method 104, Condition A <1kV
C0G – 100k Megohm or 1000 Megohm x µF, whichever is less.
≤500V test @ rated voltage, ≥1kV test @ 500V
X7R – 100k Megohm or 1000 Megohm x µF, whichever is less.
≤500V test @ rated voltage, ≥1kV test @ 500V
Z5U – 10k Megohm or 1000 Megohm x µF, whichever is less.

Dielectric Withstanding Voltage:
EIA RS-198, Method 103
≤200V test @ 250% of rated voltage for 5 seconds with current limited to 50mA.
500V test @ 150% of rated voltage for 5 seconds with current limited to 50mA.
≥1000V test @ 120% of rated voltage for 5 seconds with current limited to 50mA.

ENVIRONMENTAL

Vibration:
EIA RS-198, Method 304, Condition D (10-2000Hz; 20g)
Shock:
EIA RS-198, Method 305, Condition I (100g)

Life Test:
EIA RS-198, Method 201, Condition D.
≤ 200V
C0G – 200% of rated voltage @ +125°C
X7R – 200% of rated voltage @ +125°C
Z5U – 200% of rated voltage @ +85°C
≥ 500V
C0G – rated voltage @ +125°C
X7R – rated voltage @ +125°C

Post Test Limits @ 25°C are:
Capacitance Change:
C0G (≤ 200V) – +3% or 0.25pF, whichever is greater.
C0G (≥ 500V) – +3% or 0.50pF, whichever is greater.
X7R – + 20% of initial value (2)
Z5U – + 30% of initial value (2)
Dissipation Factor:
C0G – 0.15% maximum
X7R – 2.5% maximum
Z5U – 4.0% maximum
Insulation Resistance:
C0G – 10k Megohm or 100 Megohm x µF, whichever is less.
≥1kV tested @ 500V.
X7R – 10k Megohm or 100 Megohm x µF, whichever is less.
≥1kV tested @ 500V.
Z5U – 1k Megohm or 100 Megohm x µF, whichever is less.

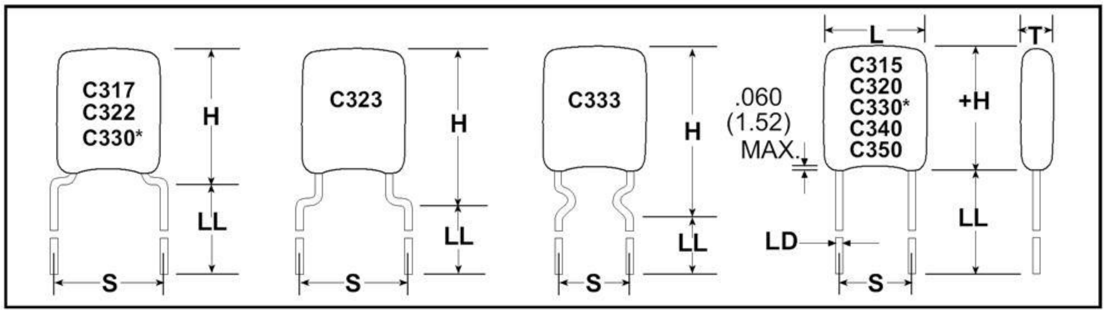
Moisture Resistance:
EIA RS-198, Method 204, Condition A (10 cycles without applied voltage.)
Post Test Limits @ 25°C are:
Capacitance Change:
C0G (≤ 200V) – +3% or 0.25pF, whichever is greater.
C0G (≥ 500V) – +3% or 0.50pF, whichever is greater.
X7R – + 20% of initial value (2)
Z5U – + 30% of initial value (2)
Dissipation Factor:
C0G – 0.25% maximum
X7R – 3.0% maximum
Z5U – 4.0% maximum
Insulation Resistance:
C0G – 10k Megohm or 100 Megohm x µF, whichever is less.
≤500V test @ rated voltage, ≥1kV test @ 500V.
X7R – 10k Megohm or 100 Megohm x µF, whichever is less.
≥500V test @ rated voltage, >1kV test @ 500V.
Z5U – 1k Megohm or 100 Megohm x µF, whichever is less.

Thermal Shock:
EIA RS-198, Method 202, Condition B (C0G & X7R: -55°C to +125°C); Condition A (Z5U: -55°C to 85°C)

(1) +53 PPM -30 PPM/ °C from +25°C to -55°C, + 60 PPM below 10pF.
(2) X7R and Z5U dielectrics exhibit aging characteristics; therefore, it is highly recommended that capacitors be deaged for 2 hours at 150°C and stabilized at room temperature for 48 hours before capacitance measurements are made.

 © KEMET Electronics Corporation, P.O. Box 5928, Greenville, S.C. 29606, (864) 963-6300

STANDARD LEAD CONFIGURATION – OUTLINE DRAWINGS



Drawings are not to scale. See table below for dimensions. + H dimension does not include meniscus.
* Lead configuration depends on capacitance value. See next page.

DIMENSIONS — INCHES & MILLIMETERS

Case Size	L Max. Inches (mm)	H. Max Inches (mm)	Standard T Max. Inches (mm)	High Voltage T Max. Inches (mm)	S(1) ±.030 (.78) Inches (mm)	LD +.004(.10) -.001(.025) Inches (mm)
C315	0.150 (3.81)	0.210 (5.33)	0.130 (3.30)	0.15 (3.81)	0.100 (2.54)	0.020 (.51)
C317	0.150 (3.81)	0.230 (5.84)	0.130 (3.30)	0.15 (3.81)	0.200 (5.08)	0.020 (.51)
C320	0.200 (5.08)	0.260 (6.60)	#0.150 (3.81)	0.200 (5.08)	0.100 (2.54)	0.020 (.51)
C322	0.200 (5.08)	0.260 (6.60)	0.150 (3.81)	0.200 (5.08)	0.200 (5.08)	0.020 (.51)
C323	0.200 (5.08)	0.320 (8.13)	0.150 (3.81)	0.200 (5.08)	0.200 (5.08)	0.020 (.51)
C330	0.300 (7.62)	0.360 (9.14)	0.200 (5.08)	0.250 (6.35)	0.200 (5.08)	0.020 (.51)
C333	0.300 (7.62)	0.390 (9.91)	0.200 (5.08)	0.250 (6.35)	0.200 (5.08)	0.020 (.51)
C340	0.400 (10.16)	0.460 (11.68)	0.200 (5.08)	0.270 (6.86)	0.200 (5.08)	0.020 (.51)
C350	0.500 (12.70)	0.560 (14.22)	0.250 (6.35)	0.270 (6.86)	0.400 (10.16)	0.025 (.64)

Note: 1 inch = 25.4mm.
Note (1): Measured at seating plane.
#0.160" (4.064mm) for 4.7 - 10.0µF

ORDERING INFORMATION

C 320 C 102 M 1 R 5 T A

CERAMIC (C)

CASE SIZE (320)
See Table Above

SPECIFICATION (C)
C – Standard

CAPACITANCE PICOFARAD CODE (102)
Expressed in picofarads (pF). First two digits represent significant figures. Third digit specifies number of zeros. Use 9 for 1.0 thru 9.9 pF. Example 2.2pF = 229

CAPACITANCE TOLERANCE (M)
C0G: D – ±0.5pF; F – ±1%; G – ±2%; J – ±5%, K – ±10%; M – ±20%
X7R: K – ±10%; M – ±20%; P – 0, -100%; Z – -20,+80%
Z5U: M – ±20%; P – 0, -100%; Z – -20,+80%

RATED VOLTAGE (DC) (1)

3 – 25	D – 1000
5 – 50	F – 1500
1 – 100	G – 2000
2 – 200	Z – 2500
A – 250	H – 3000
C – 500	

DIELECTRIC (R)
EIA Designation
G – C0G (NP0) - Ultra Stable
R – X7R - Stable
U – Z5U - General Purpose

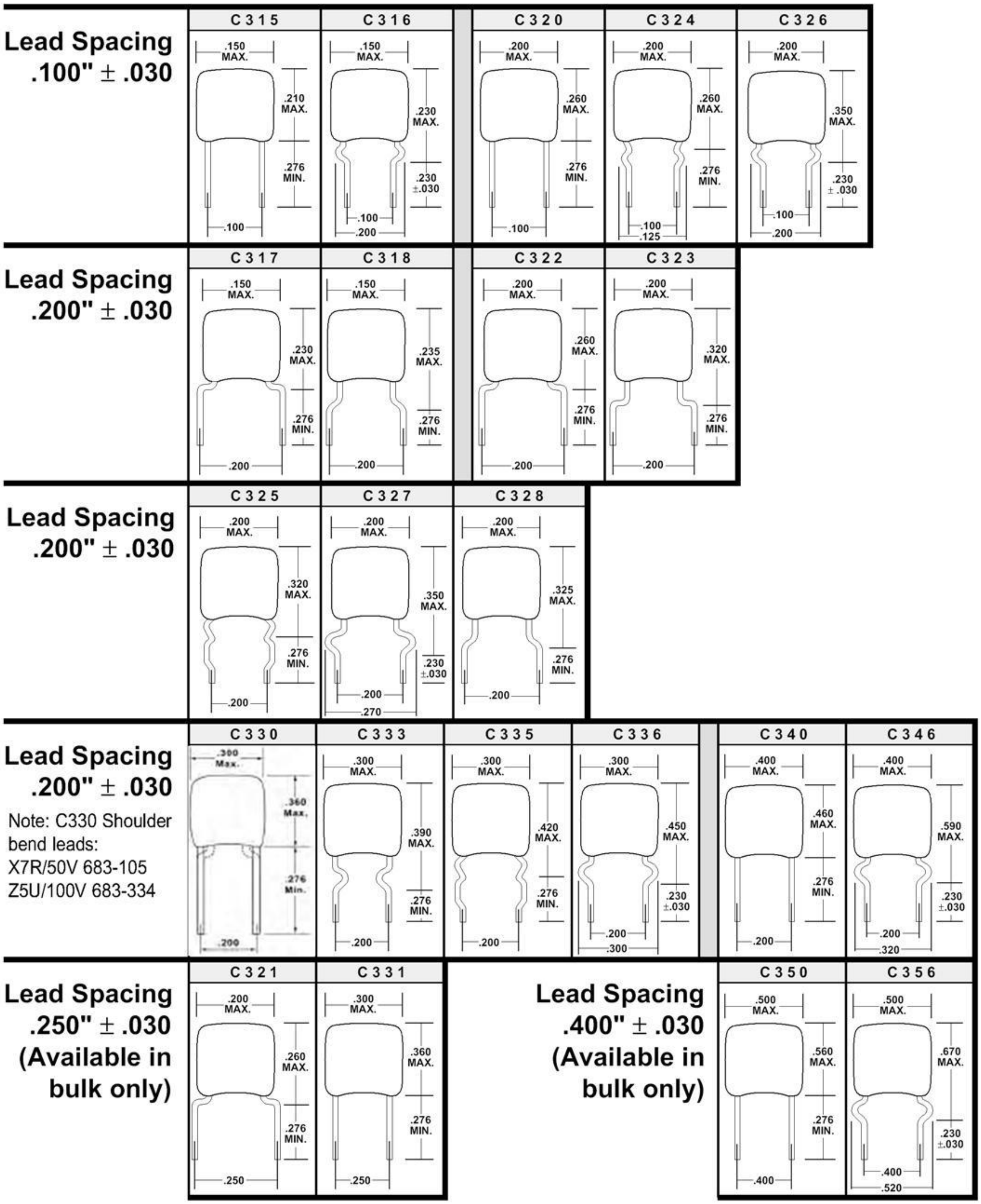
INTERNAL CONSTRUCTION (5)
5 – Multilayer

LEAD MATERIAL (T)
T – 100% Tin (Sn)
H – SnPb

FAILURE RATE (A)
A – Not Applicable

OPTIONAL CONFIGURATIONS BY LEAD SPACING

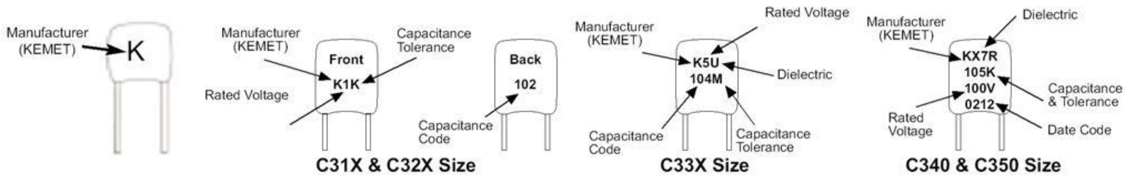
The preferred lead wire configurations are shown on previous page. However, additional configurations are available. All available options are shown below grouped by lead spacing.



Note: Non-standard lead lengths are available in bulk only.

© KEMET Electronics Corporation, P.O. Box 5928, Greenville, S.C. 29606, (864) 963-6300

CAPACITOR MARKINGS



RATINGS & PART NUMBER REFERENCE: ULTRA-STABLE TEMPERATURE CHARACTERISTICS – C0G/NPO

		Style	C31X					C32X							C33X									C34X							C35X						
Cap	Cap Code	Cap Tol	WVDC					WVDC							WVDC									WVDC							WVDC						
			50	100	200	500	1k	50	100	200	500	1k	1.5k	2k	50	100	200	500	1k	1.5k	2k	2.5k	3k	50	100	200	500	1k	2k	3k	50	100	200	500	1k	2k	3k
1.0pF	109	D																																			
1.1	119	D																																			
1.2	129	D																																			
1.3	139	D																																			
1.5	159	D																																			
1.6	169	D																																			
1.8	189	D																																			
2.0	209	D																																			
2.2	229	D																																			
2.4	249	D																																			
2.7	279	D																																			
3.0	309	D																																			
3.3	339	D																																			
3.6	369	D																																			
3.9	399	D																																			
4.3	439	D																																			
4.7	479	D																																			
5.1	519	D																																			
5.6	569	D																																			
6.2	629	D																																			
6.8	689	D																																			
7.5	759	D																																			
8.2	829	D																																			
9.1	919	D																																			
10	100	J,K																																			
11	110	J,K																																			
12	120	J,K																																			
13	130	J,K																																			
15	150	J,K																																			
16	160	J,K																																			
18	180	J,K																																			
20	200	J,K																																			
22	220	J,K																																			
24	240	G,J,K																																			
27	270	G,J,K																																			
30	300	G,J,K																																			
33	330	G,J,K																																			
36	360	G,J,K																																			
39	390	G,J,K																																			
43	430	G,J,K																																			
47	470	G,J,K																																			
51	510	G,J,K																																			
56	560	F,G,J																																			
62	620	F,G,J																																			
68	680	F,G,J																																			
75	750	F,G,J																																			
82	820	F,G,J																																			
91	910	F,G,J																																			

Golden Max

For packaging information, see pages 40 and 41.

RATINGS & PART NUMBER REFERENCE: ULTRA-STABLE TEMPERATURE CHARACTERISTICS — C0G/NPO CONT.

		Style	C31X					C32X							C33X									C34X							C35X						
Cap	Cap Code	Cap Tol	WVDC					WVDC							WVDC									WVDC							WVDC						
			50	100	200	500	1k	50	100	200	500	1k	1.5k	2k	50	100	200	500	1k	1.5k	2k	2.5k	3k	50	100	200	500	1k	2k	3k	50	100	200	500	1k	2k	3k
100	101	F,G,J																																			
110	111	F,G,J																																			
120	121	F,G,J																																			
130	131	F,G,J																																			
150	151	F,G,J																																			
160	161	F,G,J																																			
180	181	F,G,J																																			
200	201	F,G,J																																			
220	221	F,G,J																																			
240	241	F,G,J																																			
270	271	F,G,J																																			
300	301	F,G,J																																			
330	331	F,G,J																																			
360	361	F,G,J																																			
390	391	F,G,J																																			
430	431	F,G,J																																			
470	471	F,G,J																																			
510	511	F,G,J																																			
560	561	F,G,J																																			
620	621	F,G,J																																			
680	681	F,G,J																																			
750	751	F,G,J																																			
820	821	F,G,J																																			
910	911	F,G,J																																			
1000	102	F,G,J																																			
1100	112	F,G,J																																			
1200	122	F,G,J																																			
1300	132	F,G,J																																			
1500	152	F,G,J																																			
1600	162	F,G,J																																			
1800	182	F,G,J																																			
2000	202	F,G,J																																			
2200	222	F,G,J																																			
2400	242	F,G,J																																			
2700	272	F,G,J																																			
3000	302	F,G,J																																			
3300	332	F,G,J																																			
3600	362	F,G,J																																			
3900	392	F,G,J																																			
4300	432	F,G,J																																			
4700	472	F,G,J																																			
5100	512	F,G,J																																			
5600	562	F,G,J																																			
6200	622	F,G,J																																			
6800	682	F,G,J																																			
7500	752	F,G,J																																			
8200	822	F,G,J																																			
9100	912	F,G,J																																			
.010uF	103	F,G,J																																			
.015	123	F,G,J																																			
.015	153	F,G,J																																			
.018	183	F,G,J																																			
.022	223	F,G,J																																			
.027	273	F,G,J																																			
.033	333	F,G,J																																			
.039	393	F,G,J																																			
.047	473	F,G,J																																			
.056	563	F,G,J																																			
.068	683	F,G,J																																			
.082	823	F,G,J																																			
.10	104	F,G,J																																			
.12	124	F,G,J																																			

 © KEMET Electronics Corporation, P.O. Box 5928, Greenville, S.C. 29606, (864) 963-6300

RATINGS & PART NUMBER REFERENCE: STABLE TEMPERATURE CHARACTERISTICS — X7R

Golden Max Catalog Parts - X7R

		Style:	C31X							C32X									C33X								
			WVDC							WVDC									WVDC								
Cap	Cap Code	Cap Tol	25	50	100	200	250	500	1k	25	50	100	200	250	500	1k	1.5k	2k	25	50	100	200	250	500	1k	2k	3k
10pF	100	K,M,P,Z																									
12	120	K,M,P,Z																									
15	150	K,M,P,Z																									
18	180	K,M,P,Z																									
22	220	K,M,P,Z																									
27	270	K,M,P,Z																									
33	330	K,M,P,Z																									
39	390	K,M,P,Z																									
47	470	K,M,P,Z																									
56	560	K,M,P,Z																									
68	680	K,M,P,Z																									
82	820	K,M,P,Z																									
100	101	K,M,P,Z																									
120	121	K,M,P,Z																									
150	151	K,M,P,Z																									
180	181	K,M,P,Z																									
220	221	K,M,P,Z																									
270	271	K,M,P,Z																									
330	331	K,M,P,Z																									
390	391	K,M,P,Z																									
470	471	K,M,P,Z																									
560	561	K,M,P,Z																									
680	681	K,M,P,Z																									
820	821	K,M,P,Z																									
1000	102	K,M,P,Z																									
1200	122	K,M,P,Z																									
1500	152	K,M,P,Z																									
1800	182	K,M,P,Z																									
2200	222	K,M,P,Z																									
2700	272	K,M,P,Z																									
3300	332	K,M,P,Z																									
3900	392	K,M,P,Z																									
4700	472	K,M,P,Z																									
5600	562	K,M,P,Z																									
6800	682	K,M,P,Z																									
8200	822	K,M,P,Z																									
.010uF	103	K,M,P,Z																									
.012	123	K,M,P,Z																									
.015	153	K,M,P,Z																									
.018	183	K,M,P,Z																									
.022	223	K,M,P,Z																									
.027	273	K,M,P,Z																									
.033	333	K,M,P,Z																									
.039	393	K,M,P,Z																									
.047	473	K,M,P,Z																									
.056	563	K,M,P,Z																									
.068	683	K,M,P,Z																									
.082	823	K,M,P,Z																									
.10	104	K,M,P,Z																									
.12	124	K,M,P,Z																									
.15	154	K,M,P,Z																									
.18	184	K,M,P,Z																				2	2				
.22	224	K,M,P,Z																				2	2				
.27	274	K,M,P,Z																				2	2				
.33	334	K,M,P,Z																				2	2				
.39	394	K,M,P,Z																			2	2	2				
.47	474	K,M,P,Z																			2	2	2				
.56	564	K,M,P,Z																			2	2	2				
.68	684	K,M,P,Z																			2	2	2				
.82	824	K,M,P,Z																			2	2	2				
1.0	105	K,M,P,Z																			2	2	2				
1.2	125	K,M,P,Z																	2	2	2	2	2				
1.5	155	K,M,P,Z																	2	2							
1.8	185	K,M,P,Z																	2	2							
2.2	225	K,M,P,Z																	2	2							
2.7	275	K,M,P,Z																									
3.3	335	K,M,P,Z																									
3.9	395	K,M,P,Z																									
4.7	475	K,M,P,Z								1	1																
5.6	565	K,M,P,Z								1																	
6.8	685	K,M,P,Z								1																	
10	106	K,M,P,Z								1																	

Newly Released Parts

Currently in catalog

(1) Thickness max = 0.160" (4.06mm)

(2) Requires straight leads (all other C33X's require bent leads)

© KEMET Electronics Corporation, P.O. Box 5928, Greenville, S.C. 29606, (864) 963-6300

RATINGS & PART NUMBER REFERENCE: STABLE TEMPERATURE CHARACTERISTICS — X7R

Golden Max - X7R																				
		Style:	C34X									C35X								
	Cap	Cap	WVDC									WVDC								
Cap	Code	Tol	25	50	100	200	250	500	1k	2k	3k	25	50	100	200	250	500	1k	2k	3k
10pF	100	K,M,P,Z																		
12	120	K,M,P,Z																		
15	150	K,M,P,Z																		
18	180	K,M,P,Z																		
22	220	K,M,P,Z																		
27	270	K,M,P,Z																		
33	330	K,M,P,Z																		
39	390	K,M,P,Z																		
47	470	K,M,P,Z																		
56	560	K,M,P,Z																		
68	680	K,M,P,Z																		
82	820	K,M,P,Z																		
100	101	K,M,P,Z																		
120	121	K,M,P,Z																		
150	151	K,M,P,Z																		
180	181	K,M,P,Z																		
220	221	K,M,P,Z																		
270	271	K,M,P,Z																		
330	331	K,M,P,Z																		
390	391	K,M,P,Z																		
470	471	K,M,P,Z																		
560	561	K,M,P,Z																		
680	681	K,M,P,Z																		
820	821	K,M,P,Z																		
1000	102	K,M,P,Z																		
1200	122	K,M,P,Z																		
1500	152	K,M,P,Z																		
1800	182	K,M,P,Z																		
2200	222	K,M,P,Z																		
2700	272	K,M,P,Z																		
3300	332	K,M,P,Z																		
3900	392	K,M,P,Z																		
4700	472	K,M,P,Z																		
5600	562	K,M,P,Z																		
6800	682	K,M,P,Z																		
8200	822	K,M,P,Z																		
.010uF	103	K,M,P,Z																		
.012	123	K,M,P,Z																		
.015	153	K,M,P,Z																		
.018	183	K,M,P,Z																		
.022	223	K,M,P,Z																		
.027	273	K,M,P,Z																		
.033	333	K,M,P,Z																		
.039	393	K,M,P,Z																		
.047	473	K,M,P,Z																		
.056	563	K,M,P,Z																		
.068	683	K,M,P,Z																		
.082	823	K,M,P,Z																		
.10	104	K,M,P,Z																		
.12	124	K,M,P,Z																		
.15	154	K,M,P,Z																		
.18	184	K,M,P,Z																		
.22	224	K,M,P,Z																		
.27	274	K,M,P,Z																		
.33	334	K,M,P,Z																		
.39	394	K,M,P,Z																		
.47	474	K,M,P,Z																		
.56	564	K,M,P,Z																		
.68	684	K,M,P,Z																		
.82	824	K,M,P,Z																		
1.0	105	K,M,P,Z																		
1.2	125	K,M,P,Z																		
1.5	155	K,M,P,Z																		
1.8	185	K,M,P,Z																		
2.2	225	K,M,P,Z																		
2.7	275	K,M,P,Z																		
3.3	335	K,M,P,Z																		
3.9	395	K,M,P,Z																		
4.7	475	K,M,P,Z																		
5.6	565	K,M,P,Z																		
6.8	685	K,M,P,Z																		
10	106	K,M,P,Z																		

Newly Released Parts
Currently in catalog

RATINGS & PART NUMBER REFERENCE
GENERAL PURPOSE TEMPERATURE CHARACTERISTIC – Z5U

		Style	C31X			C32X			C33X			C34X			C35X		
Cap	Cap Code	Cap Tol	WWDC			WWDC			WWDC			WWDC			WWDC		
			50	100	200	50	100	200	50	100	200	50	100	200	50	100	200
1000pF	102	M,P,Z															
1200	122	M,P,Z															
1500	152	M,P,Z															
1800	182	M,P,Z															
2200	222	M,P,Z															
2700	272	M,P,Z															
3300	332	M,P,Z															
3900	392	M,P,Z															
4700	472	M,P,Z															
5600	562	M,P,Z															
6800	682	M,P,Z															
8200	822	M,P,Z															
.010uF	103	M,P,Z															
.012	123	M,P,Z															
.015	153	M,P,Z															
.018	183	M,P,Z															
.022	223	M,P,Z															
.027	273	M,P,Z															
.033	333	M,P,Z															
.039	393	M,P,Z															
.047	473	M,P,Z															
.056	563	M,P,Z															
.068	683	M,P,Z															
.082	823	M,P,Z															
.10	104	M,P,Z															
.12	124	M,P,Z															
.15	154	M,P,Z															
.18	184	M,P,Z															
.22	224	M,P,Z															
.27	274	M,P,Z															
.33	334	M,P,Z															
.39	394	M,P,Z															
.47	474	M,P,Z															
.56	564	M,P,Z															
.68	684	M,P,Z															
.82	824	M,P,Z															
1.0	105	M,P,Z															
1.2	125	M,P,Z															
1.5	155	M,P,Z															
1.8	185	M,P,Z															
2.2	225	M,P,Z															
2.7	275	M,P,Z															
3.3	335	M,P,Z															
3.9	395	M,P,Z															
4.7	475	M,P,Z															
5.6	565	M,P,Z															
6.8	685	M,P,Z															

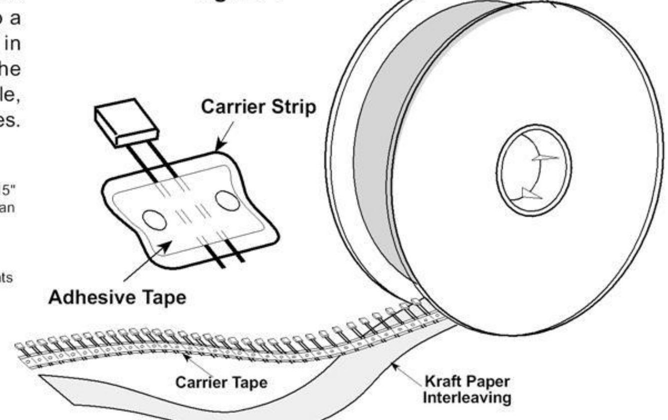
C330 shoulder bend lead configuration is standard for these cap codes.

For packaging information, see pages 40 and 41.

Ceramic Radial
Lead Tape and Reel Packaging

KEMET offers standard reeling of Molded and Conformally Coated Radial Leaded Ceramic Capacitors for automatic insertion per EIA specification RS-468. Parts are taped to a tagboard carrier strip, and wound on a reel as shown in Figure 1. Kraft paper interleaving is inserted between the layers of capacitors on the reel. Ammopack is also available, with the same lead tape configuration and package quantities.

Figure 1



(Note: Non-standard lead lengths available in bulk only.)

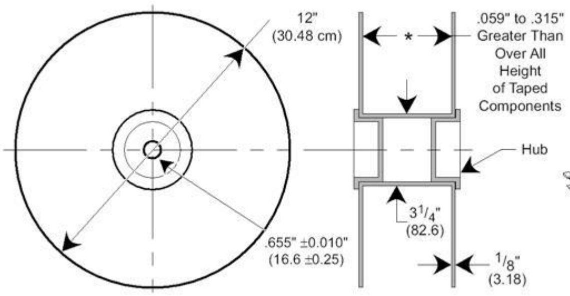


Figure 3: Standard Reel

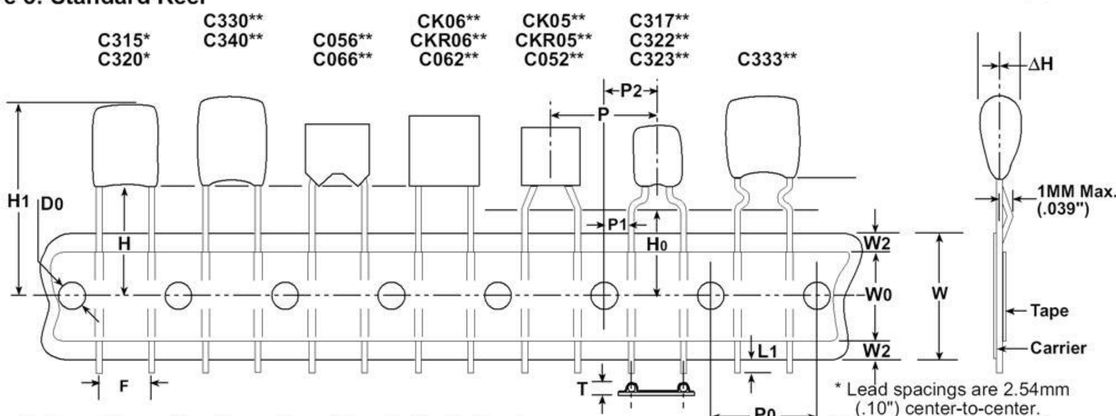


Figure 2: Lead Tape Configuration (See Table Below)

* Lead spacings are 2.54mm (.10") center-to-center.
** Lead spacings are 5.08mm (.20") center-to-center.
# See page 15 for exact lead configuration for Series.

Ceramic Radial Tape and Reel Dimensions in Millimeters & (Inches)

Dimension	Symbol	Nominal mm (inch)		Tolerance mm (inch)	
Sprocket Hole Diameter	Do	4.0 (.157)		± 0.2 (.008)	
Sprocket Hole Pitch	P0	12.7 (.500)		± 0.3 (.012)	
Component Pitch	P	12.7 (.500)		± 0.3 (.012)	
Lead Spacing (1)	F	5.08 (.20)	2.54 (.10)	+0.6 -0.2 (+.024 -.008)	
Sprocket Hole Center to Lead Center (1)	P1	3.81 (.150)	5.08 (.200)	± 0.7 (.028)	
Sprocket Hole Center to Component Center	P2	6.35 (.250)		± 1.3 (.051)	
Height to Seating Plane (straight leads) (2)	H	7301 16.0 (.630)	7303 18.0 (.709)	7301 ±0.5 (.020)	7303 Minimum
Component Height Above Tape Center	H1	32.2 (1.27)		Maximum	

Dimension	Symbol	Nominal mm (inch)		Tolerance mm (inch)	
Height to Seating Plane (formed leads) (2)	H0	7301 16.0 (.630)	7303 18.0 (.709)	7301 ±0.5 (.020)	7303 Minimum
Component Alignment	Δh	4.0 (.157)		±0.2 (.008)	
Lead Protrusion	L1	1.0 (.039)		Maximum	
Composite Tape Thickness	t	0.7 (.051)		±0.2 (.008)	
Overall Tape and Lead Thickness	T	1.5 (.059)		Maximum	
Carrier Tape Width	W	18.0 (.709)		+1.0 - 0.5 (+.039 -.020)	
Hold-Down Tape Width	W0	5.0 (.197)		Minimum	
Hold-Down Tape Location	W2	3.0 (.118)		Maximum	

(1) Measured at the egress from the carrier tape, on the component side.
(2) Determined by a 4 digit suffix placed at the end of the part number, as follows:
7301 = Recommended for parts with formed leads. Example: C322C104K5R5CA7301
7303 = Recommended for parts with straight leads. Example: C320C104K5R5CA7303

AXIMAX & GOLDMAX PACKAGING

KEMET Series	Military Style	Military Specification	Standard (1) Bulk Quantity	Ammo Pack Quantity Maximum	Maximum Reel Quantity	Reel Size
C31X			500/Bag	2500	2500	12"
C32X			500/Bag	2500	2500	12"
C33X			250/Bag	1500	1500	12"
C340			100/Bag	1000	1000	12"
C350			50/Bag	N/A	500	12"
C410			300/Box	4000	5000	12"
C412			200/Box	4000	5000	12"
C420			300/Box	4000	5000	12"
C430			200/Box	2000	2500	12"
C440			200/Box	2000	2500	12"

© KEMET Electronics Corporation, P.O. Box 5928, Greenville, S.C. 29606, (864) 963-6300