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Solar-Powered Handheld Bioinstrumentation

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Solar-Powered Handheld Bioinstrumentation

A Major Qualifying Project sponsored by NECAMSID

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Abstract

This project expands on a previous MQP with the objective of developing a low-cost, handheld bioinstrumentation demonstration board while meeting significantly stricter power, size and cost constraints than the previous project. Specifically, the device must operate using only power provided by a solar panel in indoor lighting conditions and be contained on a board the size of a standard business card. Our proposed solution measures electrocardiogram (ECG) signals taken from the fingertips and displays the user's heart rate on a liquid crystal display panel. We designed and built a functional prototype using this method, meeting the power and size requirements. An alternative method we investigated uses photoplethysmography (PPG), also measured at the fingertips, in place of the ECG signal to determine the user's heart rate. However, because of time and power constraints, we were not able to fully implement this design: recommendations for future work include implementation of the PPG design.

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Introduction

The purpose of this project is to demonstrate to prospective students what the WPI Electrical and Computer Engineering Department offers: education and technical training that would enable them to successfully complete design work in the electrical engineering field. Accordingly, our advisor proposed an interactive, low-cost device that could be given to and assembled by prospective students to generate interest in the department.

The goal for this design was to measure a biometric signal and communicate the result to the user. This project goal was based on a previous MQP, which developed a design to demonstrate the capability of an integrated chip manufactured by Analog Devices Inc. (Schwartz, Dagher, Thomson, & Walker, 2010). The previous design utilizes PPG to determine the user's heart rate and activate corresponding LEDs.

Our project added power, size and cost constraints to the previous project. While the previous design was powered by a battery, our design must operate using only power provided by a solar panel in indoor lighting conditions. Our design may occupy a board the size of a standard US business card (3.5 by 2 inches). A cost goal of one dollar per board was set, to allow the department to distribute large quantities to prospective students.

After researching several biometric signal options, we chose to measure ECG and PPG signals, and to use these to determine the user's heart rate. We researched key design components to determine key power, size and cost issues. We then designed and tested analog front-end circuits to measure the ECG and PPG signals, as well as circuit elements common to both designs. Digital signal processing algorithms for estimating the user's heart rate were investigated, implemented, tested and compared. Two printed circuit board (PCB) revisions were designed and fabricated for the ECG-based design. The project resulted in a final design that met both the power and size requirements with adequate accuracy for most subjects; however, the cost goal was exceeded significantly.

Background Research

We considered several biometric signal options for this project. Time, power and cost constraints allowed us to investigate only ECG and PPG signals in depth. This chapter includes initial background research and design considerations on the biometric signal alternatives we examined.

Survey

We performed an informal survey to select a measureable biometric signal that would be of interest to potential users (Table 1). The majority of the suggested signals could not be measured non-invasively from the user's hands, and so were dismissed.

Fertility	Body Temperature	Height
Heart Rate	EMG	Blood Alcohol Content
Blood Pressure	EEG	Life Expectancy
ECG	Abnormal Heart Rhythm	Intelligence Quotient
Panic Attacks	Stroke and Heart Attack	Hand Strength
Blood Composition	Stress	Dehydration
Blood Type	Hormone Levels	Bladder Level
Sweating	Weight	Gender
Sex Drive	Alertness	Eyesight

Table 1 - Biometric Signal Survey Results

Electroencephalogram (EEG)

Neural membranes transmit information through depolarization and repolarization. Neural activity in the brain generates detectable electric currents known as the Electroencephalogram (EEG). The EEG is typically detected with a large number of electrodes placed on the scalp. As each electrode is in close proximity to many neurons, the resulting signal represents the aggregate neural activity in the area of the brain near the electrode. The signal typically has amplitude from 1 to 100μV and frequency content from 0.5 to 40Hz.

EEG signals may be decomposed into several frequency bands of physiological significance. Delta rhythms (frequencies below 4 Hz) are associated with deep sleep or brain disease. Theta rhythms (4 to 7 Hz) are associated with drowsiness. Alpha rhythms (8 to 13 Hz) occur primarily in the occipital region in subjects who are awake and have closed their eyes. Beta rhythms (14 to 30 Hz) are typically observed in the frontal and central regions and are associated with an active cortex. Gamma rhythms (above 30 Hz) are related to active information processing (Sornmo & Laguna, 2005).

Clinical uses of EEG include the diagnosis of epilepsy and several sleep disorders. Common sources of noise include power line noise, motion artifacts, EMG, and Electrooculogram (signals caused by eye movement).As we intend to measure signals from the subject's hands, it is unlikely we would be able to record a clean EEG signal.

Electromyogram (EMG)

Prior to muscular contraction, a depolarization wave travels across the muscle's surface. This creates an electric current that may be detected with electrodes placed on the muscle's surface, called the Electromyogram (EMG). The EMG is a summation of the activity of many motor units firing during contraction. EMG may be used to diagnose neuromuscular disease and to estimate the force of the muscle's contraction, as a stronger contraction requires the recruitment of a larger number of motor units and results in an increased EMG amplitude. The EMG can have amplitudes up to 100 mV with frequency content up to 400 Hz (Sornmo & Laguna, 2005).

As we intend to measure signals from the subject's hands (where there are no large muscle groups) we would likely not be able to record a large or clean EMG signal. Furthermore, we would not be able to isolate which muscle groups are involved, as the electrodes would not be in close proximity to any large muscle groups.

Photoplethysmography (PPG)

Changes in blood volume and oxygenation level may be recorded using Photoplethysmography (PPG). Light in the visible red or infrared spectrum is directed through a capillary bed and detected on the other side. As the blood absorbs some of the light, changes in the volume of blood are seen as changes in the amount of light that is allowed to pass through. Oxygenated blood absorbs a higher proportion of red light than deoxygenated blood, while both absorb infrared light almost equally (Figure 1). For oxygenated hemoglobin, the wavelength with the highest absorption rate is 850 nm, which falls within the infrared spectrum. The oxygenation level may be determined through pulse oximetry, which measures the ratio of red to infrared light that passes through the capillary bed. The PPG signal has amplitude dependent on the light sources and sensors used. Typical noise sources include a large baseline from ambient light sources, as well as significant 120 Hz noise if the device is near artificial lighting (Webster, 2010).

A PPG signal may be taken conveniently from the finger, and provides pulse rate and blood oxygen level information. However, the necessary light sources (commonly LEDs) require significant power to produce sufficient light, presenting a challenge for our limited available power.
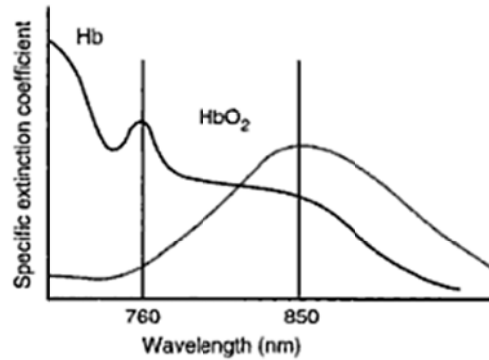
Figure 1 – Hemoglobin Light-Absorption Rate[1]

Electrocardiogram (ECG)

The standard clinical ECG uses 12 leads: three bipolar limb leads, three augmented limb leads, and six precordial leads. Of particular interest to this project is lead 1, which found by taking the voltage difference between the subject's left and right arms ($V_{LA} - V_{RA}$). The other eleven leads require electrodes on the subject's leg or chest to record. The characteristic lead 1 wave is shown below (Figure 2).
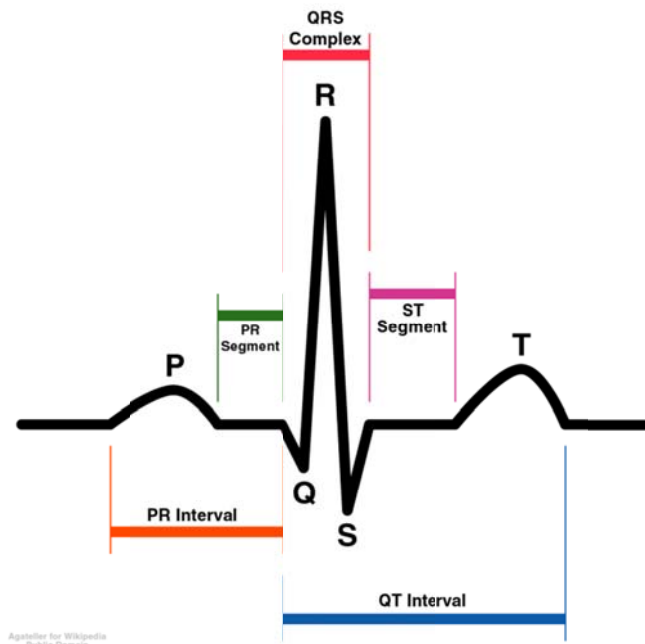
Figure 2 - Typical Lead 1 Waveform[2]

Lead 1 provides a large, clean R-wave, allowing us to detect R-R intervals fairly easily compared to other ECG leads. The signal is on the order of 1 to 3 mV, with the QRS complex lasting 70 to 110 milliseconds. The frequency content of the QRS wave ranges from about 10 to

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[1] Image taken from *Physiological Assessment of Human Fitness by Peter Maud and Carl Foster, page 173*

[2] Image taken from http://upload.wikimedia.org/wikipedia/commons/5/53/SinusRhythmLabels.png

50 Hz. The P wave is usually fairly small with frequency content below 15 Hz. The T wave can be larger, but has frequency content below 10 Hz. Heart rates can reach 220 beats per minute (bpm) in children, but this maximum heart rate decreases with age (Sornmo & Laguna, 2005).

Relevant noise sources include baseline wander, power-line noise, and motion artifact. Baseline wander is typical below 1 Hz, but can be significantly larger in amplitude than the ECG signal itself. Power line frequency is typically a 50 or 60 Hz sinusoid with amplitude dependent on proximity to sources of electromagnetic radiation, as well as the skin-electrode interface. Another consideration is the source impedance presented by the body, which is on the order of 200kΩ.

Skin Conductance (GSR)

Skin conductance, also called galvanic skin response (GSR), is believed to be a good physiological measure of the autonomic central nervous system activity (Healey, Seger, & Picard, 1999).The autonomic central system (ANS) operates on a subconscious level, affecting involuntary actions such as heart rate, perspiration and digestion. Since the ANS controls the sweat glands, the level of moisture on the skin may be an indication of ANS activity. The galvanic skin response is also linked to stress and physiological arousal.

There are two types of skin conductance: tonic and phasic (iWorx). The tonic skin conductance, also called skin conductance level (SCL), represents the baseline moisture level without any particular ANS event. The phasic skin conductance is the fluctuation in the SCL when there are ANS events occurring. Two methods commonly employed to measure GSR are injecting a current through the skin and observing the resulting voltage difference, or using the skin as a source of electrical activity (Fuller).

The typical tonic value of GSR can range from 10 to 50μS (iWorx). Phasic skin response takes place when there are events occurring, usually increasing the SCL for 10-20 seconds before falling back to the tonic level. Spontaneous GSR changes (not event-related) may happen in varying degrees depending on the individual. The typical frequency of spontaneous GSR changes is between one and three per minute.

The GSR is a useful tool in qualitatively indicating ANS activity. However, it has to be supported by other types of physiological measurements, such as EEG and heart rate, to draw a conclusion. Hence, the GSR is not an appropriate physiological signal to measure for this project.

Skin Temperature

Body temperature is widely accepted as a reliable measure for a person's overall health. Skin temperature is usually taken instead of internal temperature even though it is substantially lower than internal temperature. Average skin temperature is around 91˚F, while internal

temperature is 98.6° F. Core temperature is controlled by the hypothalamus, which is also a part of the ANS (Kimball).

Body temperature is typically held within a narrow range for a healthy person, despite the large difference in temperature between the body and its environment: "constant body temperature is achieved by perfect nervous regulation" (Hulin). The nervous system adjusts the metabolism rate, including digestion and respiration rates, to counteract heat loss.

Body temperature can be used to diagnose irregularities in the overall health. A body temperature of 1° or more over 98.6°F is technically a fever; and temperature of 103° or above is considered high fever and may indicate a serious condition (familydoctor.org).

Skin temperature offers a simple and quick measurement that can be easily interpreted; a desirable quality for this project. However, because of its relative simplicity, we decided to include it as an extra feature rather than as the primary biometric signal measurement.

Blood Pressure

The pressure exerted on the blood vessels every heartbeat is called blood pressure (BP). Blood pressure is a varying biometric signal, affected by diets, exercise and age for a single subject (MedicinePlus). Blood pressure may even change depending on where on the body the measurement is taken. Blood pressure is highest near the heart, which provides sufficient pressure to pump blood throughout the body, and rapidly decreases as the blood travels through veins and capillaries before returning to the heart.

Blood pressure is normally expressed as the ratio between the maximum pressure, systolic, and the minimum, diastolic (e.g., 120/80 mmHg).For healthy adults, systolic pressure should be less than 120 mmHg and diastolic less than 80 mmHg. Abnormal results may indicate high blood pressure (hypertension) or low blood pressure (hypotension). Hypertension increases the risk of heart illnesses, while hypotension may indicate a preexisting illness (Booth, 1977).

While blood pressure may be indicative of a person's health, it is not suitable for this project for several reasons. First, BP is likely to have decayed significantly at the fingertips, and would not necessarily represent pressure elsewhere in the body. Furthermore, methods for accurately measuring blood pressure would likely prove difficult to implement, given the project's cost constraint.

Summary

The background research we performed led us to believe that ECG and PPG were the two most plausible candidates for this project. These signals can be measured from the user's fingertips and provide meaningful results. We anticipated the power, size and cost constraints could be met, and that these signals offered appropriate implementation challenges for this project.

Main Component Research

Initial component research allowed us to determine that the solar panel and LCD were likely to have the greatest impact on our design's power, cost and size requirements. This chapter contains discussion on the criteria for selecting these main components. Discussion of all other component choices may be found in the related sections of the design chapter.

Solar Panel

The solar panel is the only component required for this project. The power limitation imposed by using an indoor solar panel source is perhaps the project's primary challenge. To increase the available power, both the size and cost of the solar panel must increase. As a result, we were left with relatively few available options.

Types of Solar Panel

The two primary types of solar panel commercially available are crystalline and silicon thin film. Crystalline cells may be further decomposed into two sub-groups: monocrystalline and polycrystalline. Monocrystalline panels are made of one contiguous piece of crystalline silicon, and offer an average power return rate of 14-18%. Polycrystalline panels are a collection of numerous smaller crystals and offer a slightly less efficient 12-14% return rate, but at a lower cost (SolarPanelCenter).

Silicon thin film solar cells are made by depositing thin layers of silicon over conductive metal on a glass substrate. These cells are far less efficient than either monocrystalline or polycrystalline cells, but are also significantly cheaper. Amorphous cells have an average return rate of 5-6%. At the time of this project, amorphous cells make up the majority of the commercially available solar cells.

Solar Cell Selection

The selected amorphous solar panel, Sanyo's AM-1819CA, has the following characteristics at 200 lux:

- Nominal open circuit voltage: 4.9V
- Nominal short circuit current: 7.5uA
- Dimensions: 31mm x 24mm x 1.3mm

This solar panel was selected for its availability, low cost, and ability to satisfy the design's power requirements.

V-I Characteristic

Even though the nominal short circuit current is very low, the available current under the indoor lighting conditions we considered was significantly higher (Figure 3).

AM-1819 Solar Cell V-I Characteristic
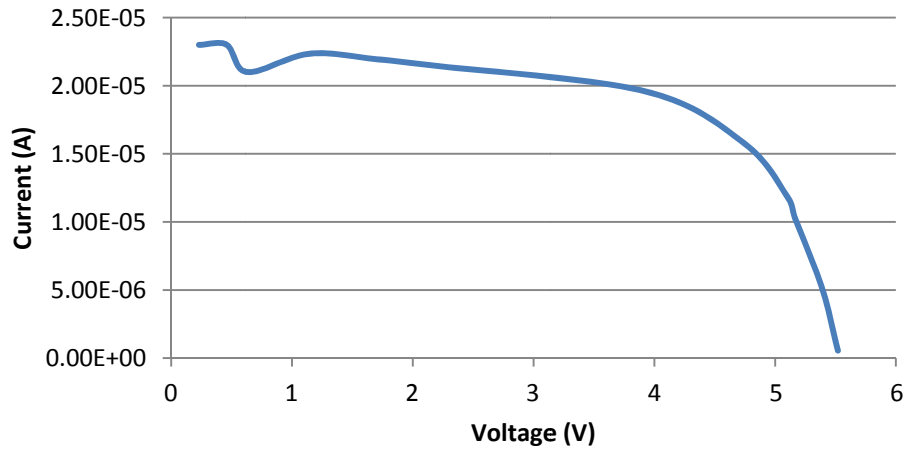
Figure 3 - AM-1819 VI Characteristic Curve

This V-I characteristic curve was experimentally determined by simply changing the load resistance and measuring the corresponding output voltage under fluorescent lighting. While operating at a higher voltage provides a larger available voltage swing for analog signals, there is a significant drop in the amount of generated power above four volts. Consequently, we considered an operating point of four volts and 20 µA for the design.

Under higher illumination levels (such as direct sunlight), the solar panel provides significantly higher voltage levels, potentially damaging any components rated for lower voltages used in the design (Figure 4). Furthermore, moving or tilting the panel may significantly affect the available power, and introduces a significant level of low-frequency noise.
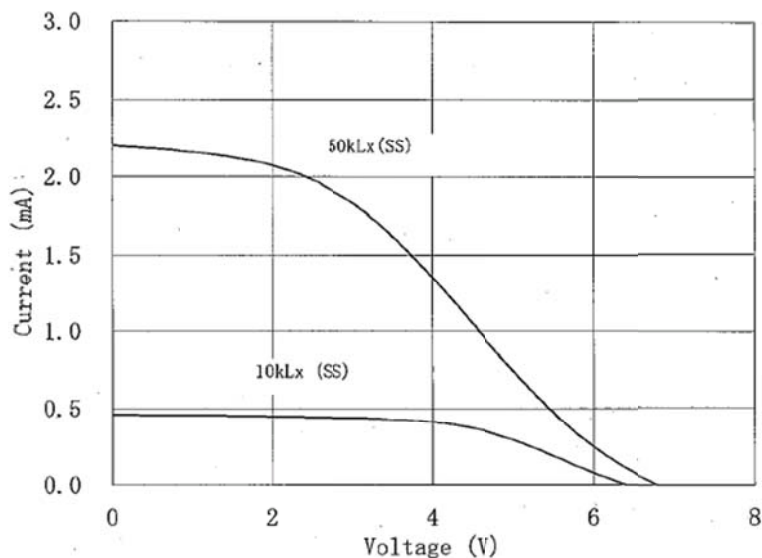
Figure 4 - AM-1819 High Illumination Characteristic Curve

LCD Display

Communicating with the user is a fundamental requirement of this project. Given the power constraints created by the solar panel, an LCD offered a practical user interface.

Display Comparison

We considered LED and LCD user interfaces. Though LED displays are relatively simple to implement, they require significantly more power (typically 20 milliamps at two volts) than was available from the solar panel. LCDs operate with very little current, though they require an AC driving voltage. LCDs were immediately recognized as a more practical method of transmitting information to the user, despite the increased complexity in driving the display. LCDs permit a cost-effective and power-efficient user interface.

LCD Background

There are three primary types of LCD displays currently available: reflective, transmissive, and transflective. The reflective display works by reflecting ambient light off a backing material. Segments are displayed by blocking the light, resulting in a low-cost, low-power passive display. Consequently, this display cannot be read without ambient light. Transmissive displays use an LED backlight in place of reflected ambient light. Hence, this is an active display, and may be read at any level of illumination. However, it also requires a significant amount of power to power the backlight. The transflective display combines the advantages of these two types by switching between reflective and transmissive mode depending on the level of illumination. While it is more versatile than the reflective display and more power efficient than the transmissive display, it is also the most expensive.

LCD Selection

We selected a reflective display for its low cost and power requirements. Because the solar panel will not operate in low levels of illumination, we decided that a backlight would be unnecessary. As we expected the solar panel to provide four volts, we only considered panels requiring four volts or less. To display the full range of normal heart rates, a display with at least 2.5 digits is necessary. We chose the Lumex S2X1C50TR, as it appeared to be the most aesthetically pleasing LCD meet these requirements. Key characteristics of the LCD are:

- Operating voltage: 3 – 5V(AC)
- Number of digits: 2.5
- Number of input pins: 16
- Dimensions: 30mm x 26mm x 3mm

This display operates with voltages provided by the solar panel and with very little current. It is capable of displaying a range of values (0 to 199) that covers the expected range of user heart rates. It is relatively inexpensive, easy to read, and does not require too much room on the card.

Design and Methods

This chapter contains the device design, including circuit elements common to both biometric signal circuits, as well as design components specific to the ECG and PPG circuits.

Common Circuit Elements

As the ECG and PPG circuits shared the same goals, the two designs shared many of the same elements. Specifically, both circuits required stable power supplies and an interface to the LCD, provided by a microcontroller. This section contains discussion on the component selection and design process involved in developing these shared circuit elements.

Voltage Regulator

The power provided by the solar panel introduced a high level of variability to the system. Depending on the user's proximity to a light source, the open-circuit voltage provided by the solar panel could vary from less than a volt to over six volts. Furthermore, the voltage could change suddenly with small changes in light intensity or solar panel angle. Many of the components considered were rated for less than six volts and portions of the design were sensitive to power-supply noise. Several means of regulating the supply voltage were considered.

To keep costs low, we investigated discrete-component solutions. We considered using a zener diode to prevent excessive voltages, coupled with a sufficiently-large capacitor to reduce supply noise (Figure 5).
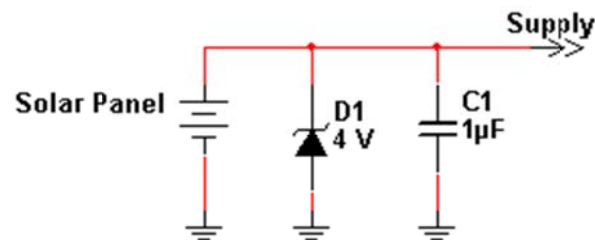
Figure 5 - Zener Diode Shunt Regulator Circuit

Because of the potential for a large discrepancy between the power available and the power necessary for operation, a zener diode with an extremely low equivalent series resistance was required. Furthermore, because of the low power levels involved, it was also necessary that the leakage current be very small. In full sun, the solar panel may generate over 20 µA at nearly 7V; under artificial fluorescent lighting it may generate only 10 µA. We were unable to find a zener diode with a sufficiently steep voltage-current characteristic.

We next considered adding a transistor for current gain (Figure 6).
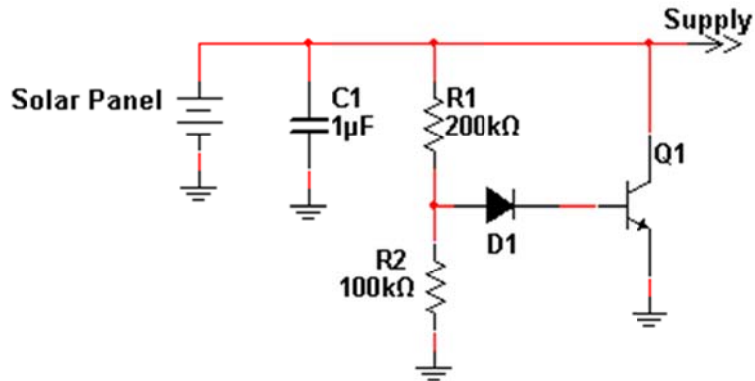
Figure 6 - Transistor Shunt Regulator Schematic

This would allow us to use a diode in the forward biased region, where the voltage-current characteristic curve is approximately exponential. The slope of this steeper curve is further increased by the transistor's gain. Unfortunately, any power beyond what is consumed is simply wasted under this approach. The circuit's performance was still significantly inferior to the integrated circuit regulators we found, and cost nearly as much.

Linear regulators are typically the cheaper than switching regulators, and provide comparable performance for this application. While switching regulators are often more efficient, this efficiency would mostly be lost in our design without a method of storing the power we weren't using. The first linear regulator we considered was the MCP1702, which has a low dropout voltage and quiescent current. The LCD display became significantly easier to read with a supply over three volts; we selected a 3.3 V regulator to allow for some variation in the LCD contrast. By selecting the lowest reasonable supply voltage, we minimized the luminance necessary to prevent large levels of power supply noise. If the solar panel is unable to provide a voltage greater than the regulator voltage, the linear regulator will be unable to function properly, effectively shorting the solar panel to the regulated output. Selecting a low voltage lowers the risk of this occurring and allows operation in environments with less light available. Large capacitors on the regulator input and output help to maintain a constant voltage despite fluctuations in the power supplied or the load. We use microfarad capacitors as they are large enough to reduce power-supply noise, but small enough to be relatively cheap.

During initial testing, we discovered that the MCP1702 briefly required over 20μA when turning on. As a result, significantly more light was necessary to turn the device on, which would likely be frustrating for the user. We switched to the Torex XC6218 regulator, which is very similar to the MCP1702 in performance and cost, but has a much smaller power-on transient. The final voltage-regulation circuit using this part costs approximately 41 cents in quantities of 100, uses a low level of power, and provides adequate power-supply regulation (Figure 7).
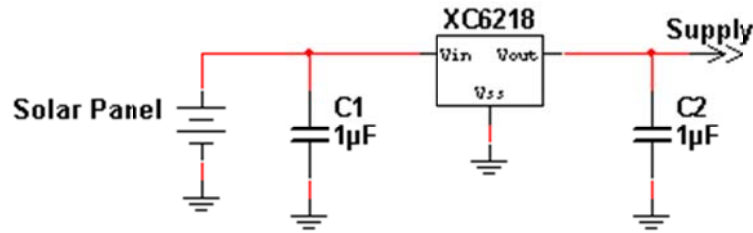
Figure 7 - XC6218 Linear Regulator Schematic

Microprocessor

Including a microprocessor in our design allows a fairly simple LCD driver implementation and adds digital signal processing capabilities. Low-cost, low-power microcontrollers are increasingly common, and often include necessary peripherals like timers and analog-to-digital converters. Available CPLDs we found for similar prices required significantly more power and were limited in functionality. It was clear almost immediately that a microprocessor would be central to our design.

Our first criterion in selecting a microcontroller was that it has at least 16 digital input-output pins to drive the LCD, in addition to any pins the remainder of our design might require. We also found that a microcontroller with an integrated analog-to-digital converter (ADC) would be significantly cheaper than using a separate chip. The microcontroller needed to be cheap and run on the little available power. We considered the following microcontrollers (Table 2-Microcontroller Comparison).

Manufacturer	Part Number	I/O Pins	ADC	Cost (100)
Freescale Semiconductor	MC9S08SE4CWL	24	10b	$0.99
STMicroelectronics	STM8S103K3T6C	28	10b	$1.05
Microchip Technology	PIC16LF722-I/SS	25	8b	$1.09
Texas Instruments	MSP430F2112IRHBR	24	10b	$1.65

Table 2- Microcontroller Comparison

We initially intended to use the MSP430 because we anticipated that our prior experience with it would lead to decreased development time. However, we selected the PIC for the final design as it provides similar performance at a greatly reduced cost. The PIC also has a fairly intuitive instruction set and is well-documented, so very little time was necessary to become familiar with the microcontroller. The initial development cost to purchase the programming hardware was also relatively small.

Clock Circuits

To accurately execute the digital signal processing algorithms of interest to us, an accurate, low frequency (60 Hz) timer was required. This timer is used to time ADC samples, as well as drive switching elements in both the ECG and PPG circuits. Error in this frequency

would shift the frequency response of any digital filter we implemented, and could decrease the signal-to-noise ratio in the ECG circuit by allowing more power-line noise through the analog circuit. To reduce cost, we considered using an external RC oscillator. However, to obtain the frequency necessary frequency tolerance, the resistor and capacitor would have to have extremely low tolerances (e.g., 0.001 % to achieve +/- 20 ppm). Components this precise would be very expensive (or unobtainable), and stray impedance from the circuit board would likely dominate the tolerances. The PIC has a built-in crystal-oscillator circuit, which we used for this purpose. The Abracon Corporation AB26TRB was the cheapest crystal oscillator we were able to find, a 32768Hz tuning fork crystal with +/- 20ppm frequency tolerance. The rated load capacitance is 12.5 pF; we used two 33 pF capacitors for a series combination of 16.5 pF. A 32768 Hz clock frequency is low enough that the PIC oscillator module uses very little current, but high enough to provide sufficient timing precision. We used a peripheral timer to divide the frequency by 546, resulting in a nominal timer frequency of 60.01 Hz. Using this crystal oscillator circuit we were able to obtain a frequency extremely close to the desired 60 Hz.

To conserve power, we decided to put the microcontroller in sleep mode while it was not performing any calculations between samples. As the PIC consumes very little power while in sleep mode, we attempted to maximize the amount of time it spends in that state. Though using higher clock frequencies results in higher power consumption, using a clock as slow as the 32768 Hz timer clock would cause the microcontroller to use much more power because it would spend very little time in sleep mode. A faster clock source was required. While the frequency tolerance for this fast clock was not particularly important, the length of time to enable and disable it was critical. The PIC's internal oscillator requires a long frequency-stabilization period when it is enabled. This would result in a large portion of time out of sleep mode without performing any operations. Instead, we decided to use an external RC timer. The RC timer is particularly well-suited for this application because it turns on immediately and is cheap given the wide allowable frequency tolerance. To conserve power, we used the largest recommended resistor value (10 kΩ). As the circuit is charging the capacitor through the resistor approximately half the time it is active, increasing the resistance reduces the average current. We also used a value close to the minimum recommended capacitance (33 pF) for a higher frequency. The resulting clock has a frequency close to 2 MHz, and is used as the main system clock when the microcontroller is not in sleep mode.

Analog to Digital Converter

Both the ECG and PPG circuit rely on the ADC to allow the microcontroller to process their respective analog signals. We believe eight-bit resolution is sufficient to capture most of the relevant information on both the ECG and PPG signals, provided they have amplitudes around half the full-scale range. We configured the ADC to perform conversions using the internal ADC clock to ensure that the clock frequency allows for accurate conversions while maintaining low power consumption.

LCD Driver

Though stand-alone logic to drive LCD displays exists, it did not prove to be cost-effective for our application. We decided to use dedicated microcontroller pins to drive the LCD, selecting these pins for the ease of printed circuit board layout and firmware efficiency. We attempted to lump LCD digits into single ports for more efficient code. PORTB drives the second digit, as well as the common pin; PORTC drives most of the third digit; and PORTA drives the first digit and one segment of the third digit. A simple look-up table with all the possible display values would require more indirectly accessible memory than is available on the PIC, but it would take many operations to update the LCD without any table. We found a compromise between these two options by creating lookup tables for the individual LCD digits. The individual digits to be displayed are first extracted in base ten. If the output value is greater than 100, the first digit is displayed and 100 subtracted from the value. The result is divided by ten to convert it to two binary-count-decimal (base ten) digits, with the quotient displayed on the second digit and the remainder displayed on the third digit. Lookup tables are used to determine which LCD segments are to be displayed based on the BCD digits. Though the division operation is relatively computationally expensive, dividing by a constant allows significant optimization for improved efficiency. Additionally, the number of operations to update the LCD is mitigated because it is only computed approximately once per second, depending on the detected heart rate.

Card-Edge Connector

To program the microcontroller, as well as test the system after assembly, it is necessary to communicate with the programming and test board. As header pins might prove aesthetically unpleasing, we decided that a card-edge connector would provide a reliable, convenient connection without detracting from the board's appearance. We selected the EDAC Inc. EDC305440 because it was relatively inexpensive and was the same length as the circuit board. To program the microcontroller, we added fingers for the VPP, ICSPDAT and ICSPCLK pins on the microcontroller, as well as the regulated voltage line. We use the grounded ECG pad to provide a connection to ground, and have access to the analog input through the other pad. For testing purposes, the output of the analog block and an additional microcontroller pin (to allow for serial communication with a DAC on the testing board) are also given fingers. In total, eight connection points are provided to the testing board. Because the fingers are only on one side of the board, no potentially harmful connections will be made if the board is inserted backwards.

ECG Analog Design

This section describes the component selection and design process for the ECG analog circuit.

ECG Model

We modeled the expected ECG signal, including predicted sources of noise, as shown below (Figure 8).

V1

V2

V3

Electrode1

2mVpk
60 Hz
0°
Powerline Noise

20mVpk
100mHz
0°
Baseline Wander

0 V 500uV
10msec 250msec
ECG Signal
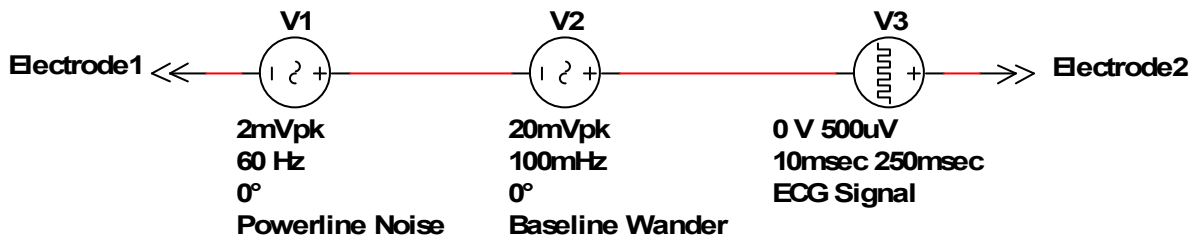
Electrode2

Figure 8 - ECG Model

We modeled powerline noise with a 2mV, 60 Hz AC voltage source. The amplitude is significantly larger than would be expected in most ECG applications because the available electrodes have a high-impedance connection to the skin, thus increasing the potential for a mismatch between the two electrodes and contributing to higher powerline noise. The value we chose, 2 mV, was based on measurements taken in the lab. Baseline wander was modeled with a 20 mV, 100 mHz AC voltage source, while the ECG signal itself was modeled by a 500 µV, 10 ms pulse to approximate the R-wave—these values were based on our background research.

Electrodes

Bio-potential electrodes are necessary to transduce the ECG signal carried by ions within the body to electric currents to be measured by our circuit. We decided to use exposed PCB patches out of cost and practical considerations; any conductive gel would have to be frequently replaced by the user, which would be cumbersome and costly. Though Ag-AgCl electrodes would provide a flatter frequency response and improved operation at lower frequencies, this material is not commonly used in PCB manufacturing processes. We chose instead to use a lead-free solder finish for its low cost. We modeled the electrodes using the following circuit (Figure 9).

R1
200kΩ
Electrode DC Resistance

V1

User

10mV
Half-Cell Potential

C1
800nF
Electrode Interface Capacitance

R2
200Ω
Electrode Series Resistance

Biocard
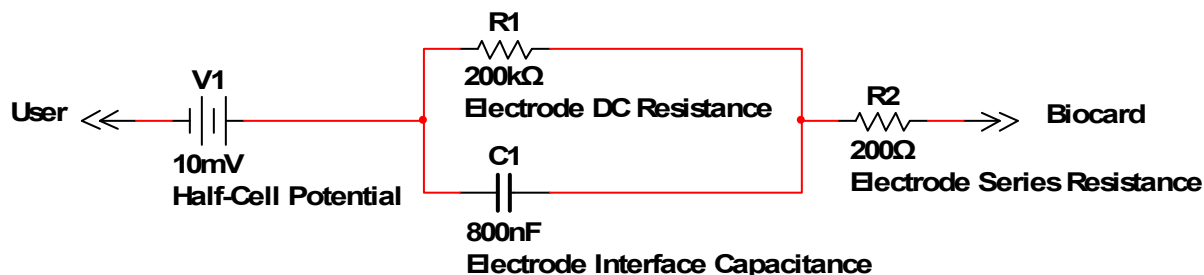
Figure 9 - ECG Electrode Model

We used a DC voltage source to model the half-cell potential expected across the electrode; this value is larger than typically observed values—our electrodes have fairly poor contact with the user's skin because of the lack of conductive gel. This high-impedance contact also resulted in a high DC resistance, which is again much larger than typical values, and is based on measurements taken in the lab. The electrode interface capacitance and series resistance were chosen to match the expected frequency response found during our background research.

Signal Biasing

To ensure the operational amplifier was functioning properly, it was necessary to bias the ECG signal from the electrodes. We chose a DC offset of approximately 1.65 V—midway between the regulated voltage supply and ground—to accommodate the maximum possible amplitude. Our first approach attempted to maximize the circuit's input impedance by biasing one electrode and recording the signal from the other (Figure 10).
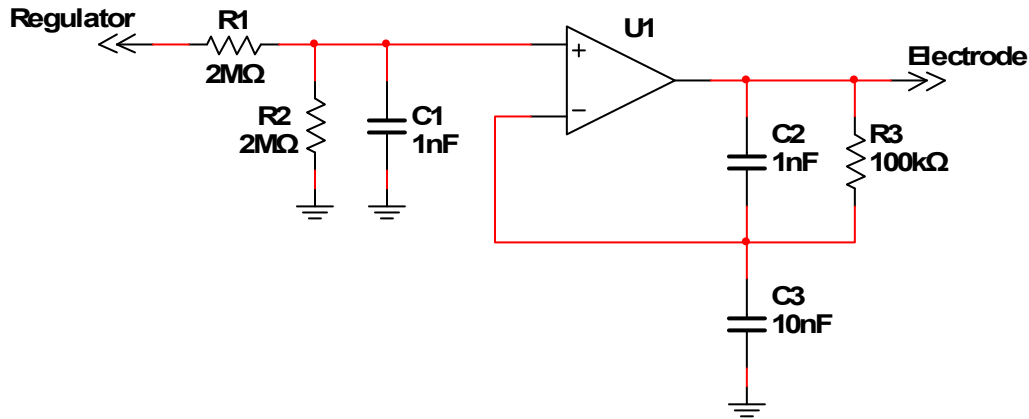
Figure 10 - Signal Bias Design 1

Resistors R1 and R2 were chosen to bias the operational-amplifier's non-inverting input at half the regulated power supply. Large resistance values decrease the circuit's power consumption, but expose the circuit to potential noise problems. To mitigate noise at the high-impedance non-inverting node, C1 was added to stabilize the voltage reference and reduce high-frequency noise. The feedback loop provides unity-gain at DC values, so the output provides a low-impedance voltage source equal to the reference voltage. C2 and C3 were added to allow the use of non-unity-gain-stable operational amplifiers by giving the circuit a gain of 11 at higher frequencies.

Using this circuit would allow the other electrode to be connected directly to the non-inverting input of another operational amplifier, resulting in the highest achievable input impedance and minimizing any signal reduction or filtering effects from the electrodes. The circuit would effectively bias the user between the power rails, so the other electrode would also have approximately the desired DC bias. However, this circuit requires an additional operational-amplifier or similar device to maintain a low-output-impedance DC voltage. To reduce the cost, we instead used the following circuit (Figure 11).
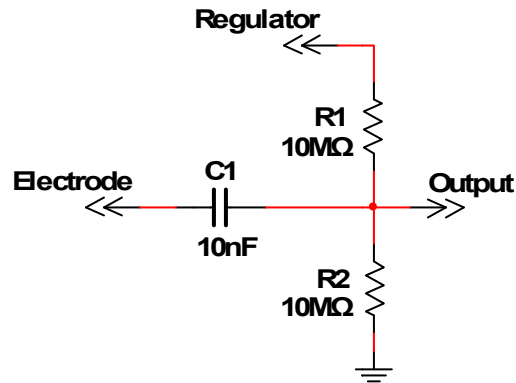
Figure 11 - Signal Bias Design 2

This circuit allows the electrodes to be biased at ground while keeping the operational amplifier's input well within its operating range. Resistors R1 and R2 provide a DC bias of half the regulated voltage supply, while C1 blocks the DC component of the signal from the electrodes with a high-pass corner frequency of about 3 Hz. The other electrode is grounded. The transfer function is shown below (Figure 12).
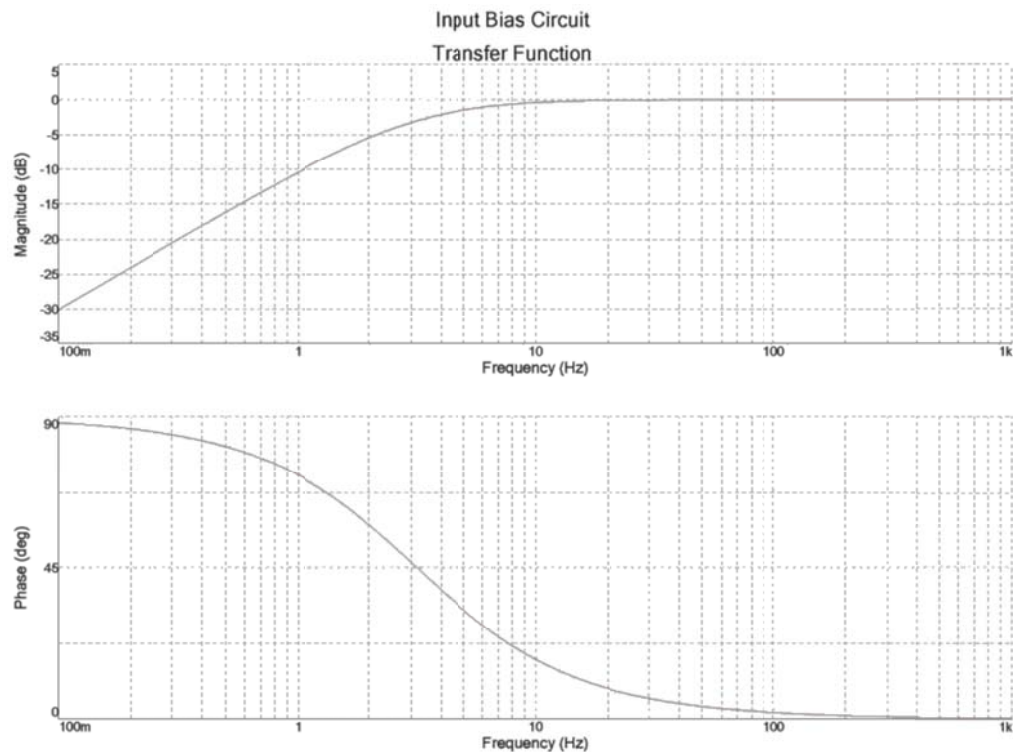
Figure 12 - Bias Circuit Transfer Function

While this circuit has lower input impedance and attenuates some ECG frequency components, it is significantly cheaper because it does not require any additional operational amplifiers or voltage regulators. The corner frequency is high enough to significantly attenuate

baseline wander, but low enough that most of the ECG signal content, particularly the higher-frequency R-wave, is preserved. High resistor values were chosen to reduce power consumption, as initial experiments showed that high-frequency noise at this node was not likely to be a large concern under normal operating conditions.

Gain Stage

To take advantage of the full scale range of the ADC it was necessary to amplify the ECG signal by a factor of over 1000. Because of the large variability in ECG amplitude between users, we chose a slightly smaller value than initial experiments suggested to prevent saturation under most expected circumstances. Our first design used a single operational amplifier, theMCP6141. This amplifier offers a gain-bandwidth product of 100 kHz, which would allow a gain of 1000 with a bandwidth of 100 Hz, a significantly wider bandwidth than necessary to capture most of the ECG signal. The MCP6141 is relatively cheap and uses very little power, but is not unity-gain-stable. We designed the following circuit (Figure 13).
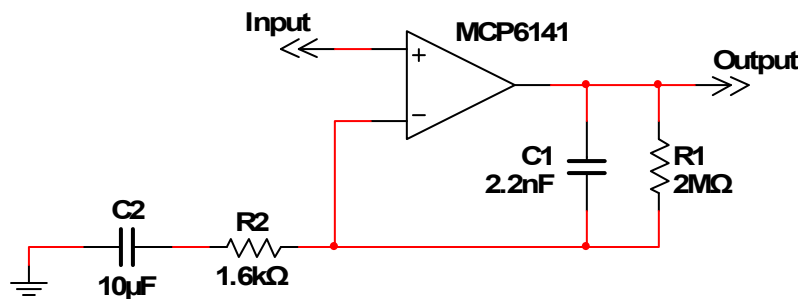
Figure 13 - Single Gain Stage Design

Resistors R1 and R2 provide a pass-band gain of approximately 1250, which we believed would sufficiently amplify the ECG signal. To avoid saturation, it was necessary to avoid amplifying the significant DC bias voltage we had previously added to the signal. The addition of C2 to the circuit ensures that the DC gain is unity, effectively re-biasing the amplified signal output at the same voltage as the input and allowing for the maximum signal amplitude without saturation. To slightly reduce powerline noise while maintaining stability, C1 was added. The resulting circuit has a band-pass characteristic with corner frequencies at 10 and 36 Hz, and a pass-band gain of over 1000 (Figure 14).
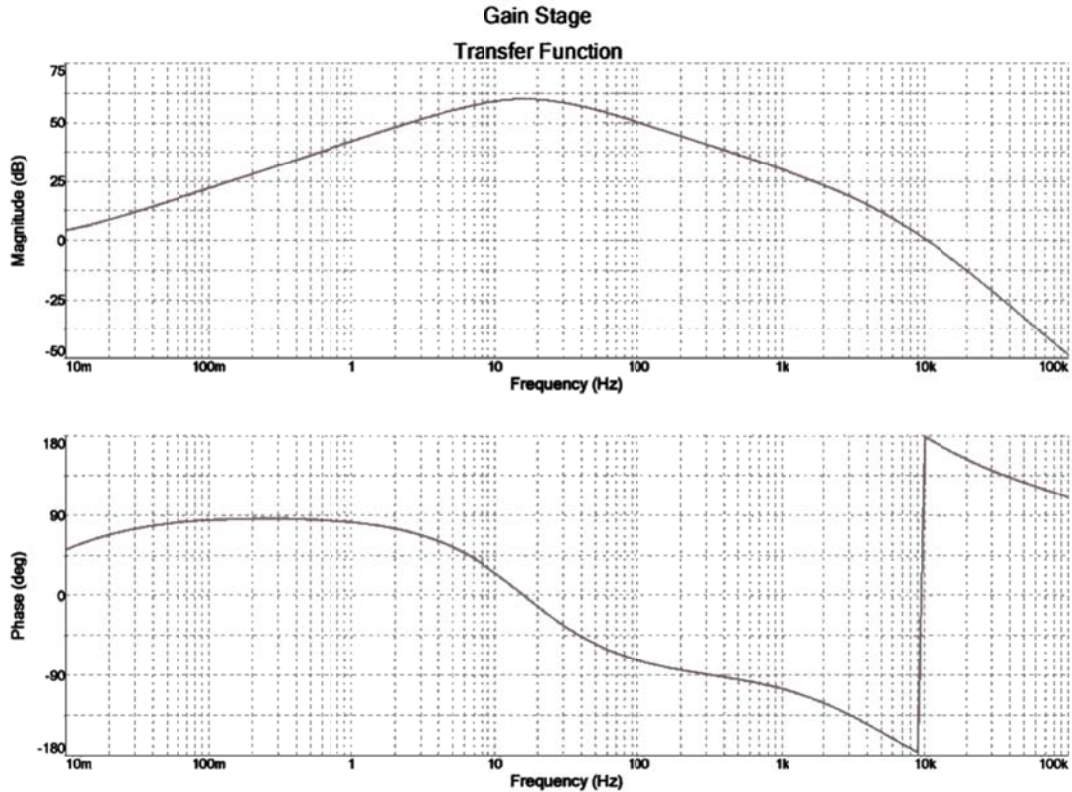
Figure 14 - Single Gain Stage Design Transfer Function

Though the circuit functioned properly, we discovered that powerline interference was significantly more prevalent than originally hypothesized. Measurements in the lab suggested that the 60 Hz noise was 10 to 20 times the amplitude of the ECG signal itself (Figure 15).
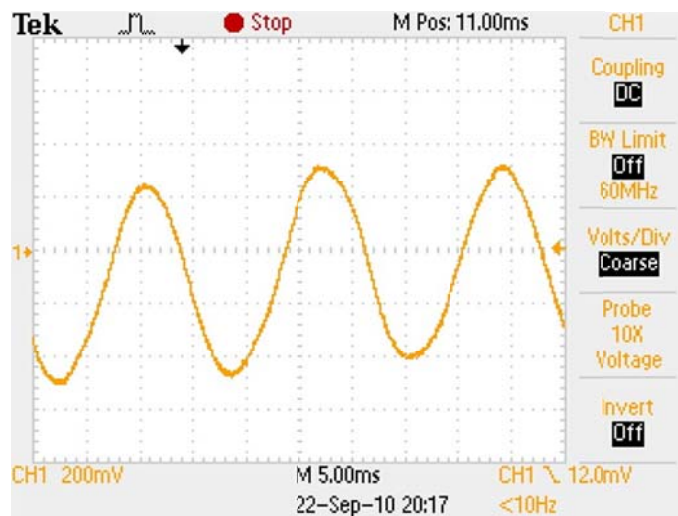
Figure 15 - ECG Signal with Powerline Noise

While we had originally intended to filter out all the 60 Hz noise digitally, it was clear that we would lose too much resolution with this approach; to avoid saturation, we could not amplify the signal enough with the analog circuit to prevent significant quantization error during sampling. Instead, the ECG signal would be only slightly larger than the quantization noise.

Switched Capacitor Circuit

To overcome this, we determined it would be necessary to filter out much more of the powerline noise in the analog circuit. We considered analog notch filters. Unfortunately, because the frequency under consideration is so low, LRC resonant filter circuits would require very large inductors and capacitors. Active filters, such as Sallen-Key or Biquad circuits, require additional operational amplifiers and achieve high Q values only with closely-matched components. We decided that using a 60 Hz timing signal generated by the microcontroller provided cheaper solutions to the problem. The first approach we considered, suggested by Professor McNeill, was to integrate over one 60 Hz cycle, then sample the signal and reset the integrator. We designed the following circuit (Figure 16).
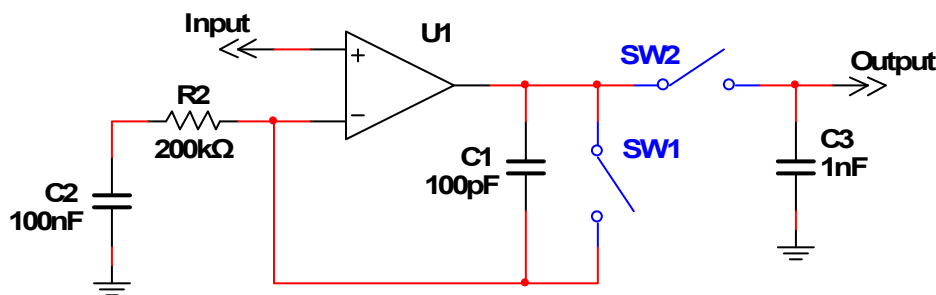
Figure 16 - Switched Capacitor Integrator Circuit

As the integral of a sinusoid over one period is zero, this integrator approach effectively cancels out sinusoidal noise at the switching frequency of analog switch SW1. We attempted to design the integrator itself, C1 and R2, with a large gain to amplify the ECG signal as much as possible while avoiding saturation. C2 was added to avoid integrating the signal's DC offset and bias the output at the same DC level as the input. SW2 and C3 act as a sample and hold circuit; SW2 is closed briefly before the integrator is reset each time, so most of the ECG signal below 30 Hz is allowed to pass without significant powerline noise reaching the output (Figure 17).
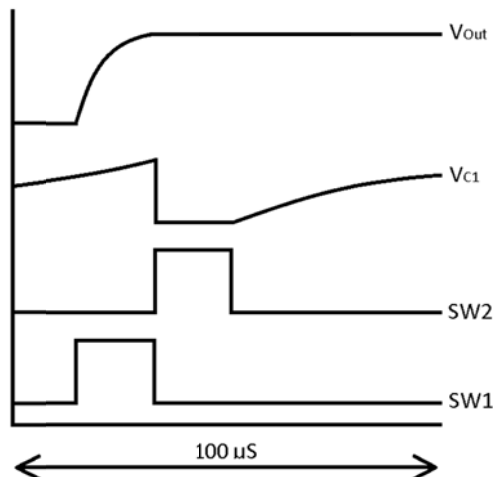
Figure 17 - Switched Capacitor Timing Diagram

While this circuit performed as expected, it requires two analog switches. We replaced SW1 with a large resistor (Figure 18).
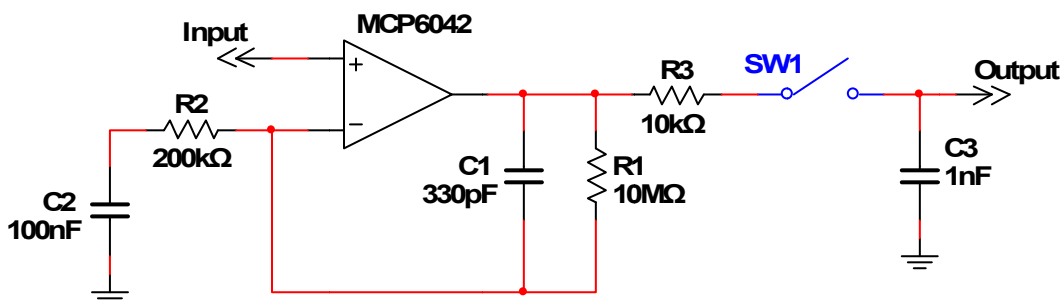
Figure 18 - Bandpass Gain Stage

This circuit has a similar response over the frequencies of interest, but requires only one analog switch, reducing the cost. The dual package MCP6042 operational amplifier was chosen for its low cost and low power operation. The gain-bandwidth product is 14 kHz, which is sufficient for this circuit's pass-band gain of about 33. R3 was added to ensure stability, as the amplifier is driving a capacitive load when the switch is closed. Sampling at 60 Hz causes the powerline noise to alias to DC, where it may be easily filtered out in the proceeding stage.

As the powerline noise is not removed until after the sample and hold stage, additional gain is required after this circuit to amplify the signal without noise saturation. We used another gain stage identical to the first gain stage as it satisfied the gain, frequency response, and power requirements. The transfer function for the individual gain stages is shown below (Figure 19).
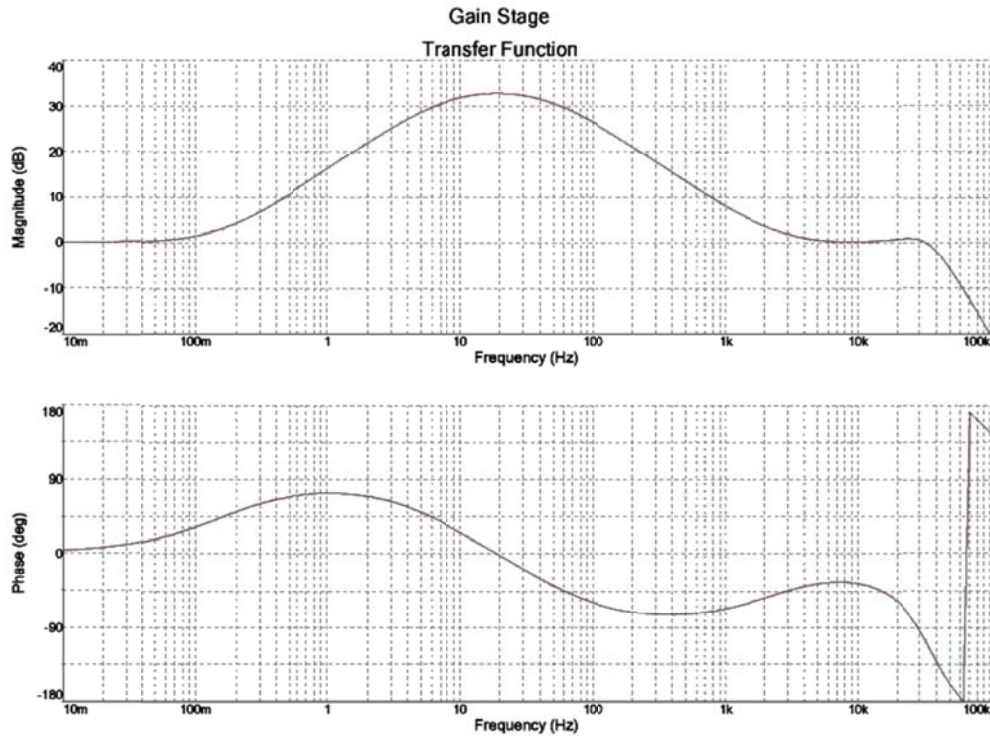
Figure 19 - Gain Stage Frequency Response

We chose the TI TS5A4594 analog switch for its low cost and power consumption, as well as its high off-impedance. The complete analog ECG circuit is shown below (Figure 20).
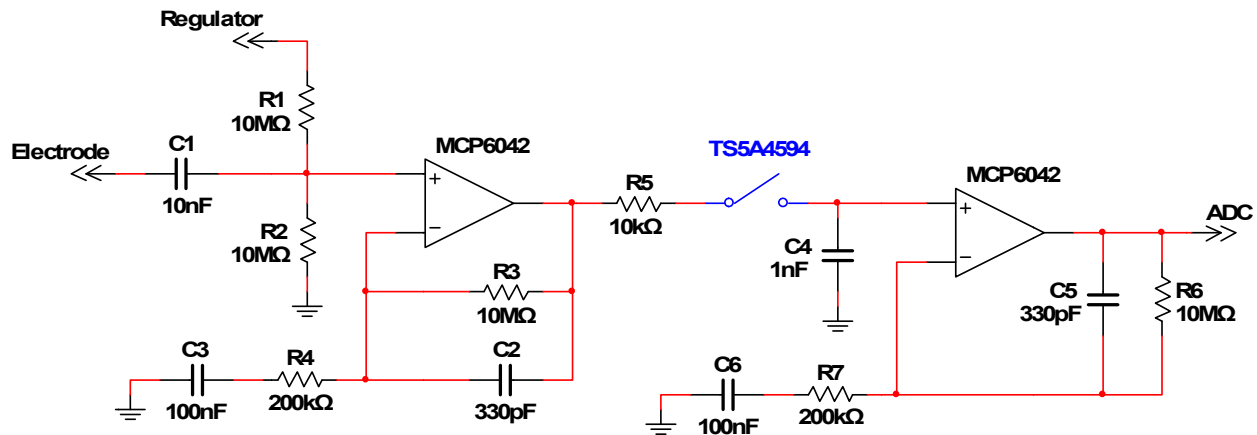
Figure 20 - Complete ECG Analog Circuit

This circuit biases the signal at half the regulated supply voltage, amplifies the signal by 30 dB, samples the signal at 60 Hz to remove powerline noise, and then amplifies the signal by another 30 dB (Figure 21). At this point, the signal is large enough to be quantized by the ADC.
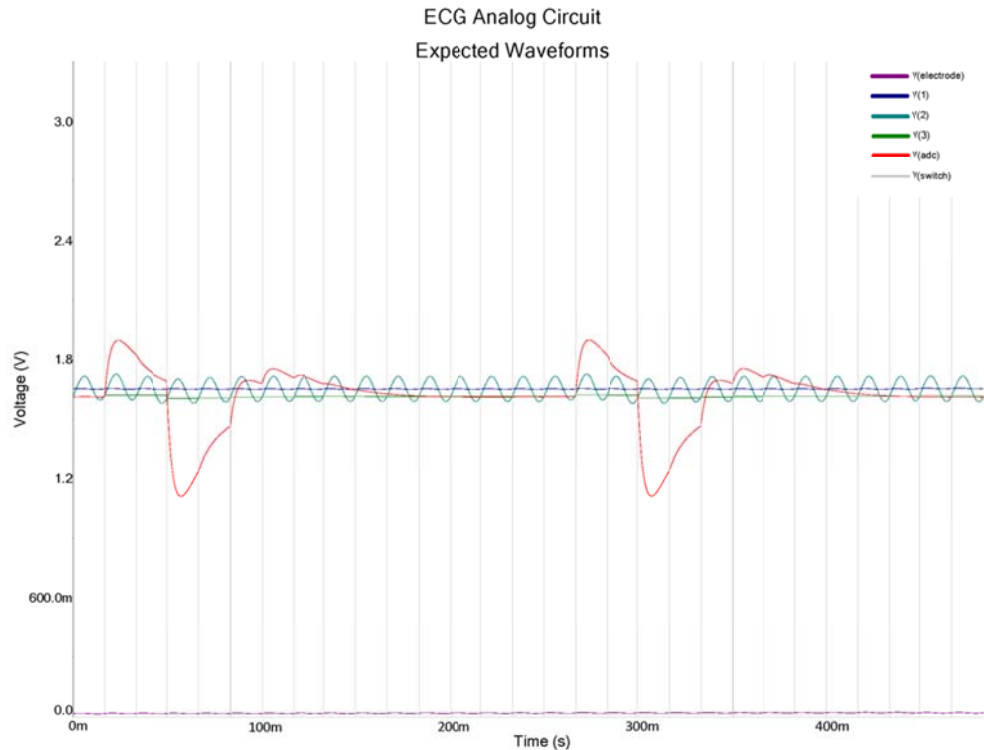
Figure 21 - ECG Analog Circuit Waveforms

ECG Digital Design

This section describes the component selection and design process for the ECG digital signal processing algorithm, including proposed methods for beat detection and heart rate estimation. The full PIC16LF722 assembly code implementation of the ECG digital design is contained in Appendix A.

Direct Estimation

One approach to estimating the user's heart rate we considered was direct estimation using a discrete Fourier transform. To achieve reasonable precision with this method, it would be necessary to use a large sample size, requiring a large number of multiplication operations. Because the PIC microcontroller we selected does not have a hardware multiplier, these calculations would be computationally expensive. We abandoned this approach because of the anticipated power requirement.

Beat Detection

We decided instead to detect heart beats and estimate the heart rate by timing the interval between beats. The detection approaches we considered involved conditioning the signal and comparing the result to a threshold value. To prevent spurious detections, we included a lockout timer; beats detected less than 20 samples (333 ms) after a previously detected beat were assumed to be noise and ignored. Consequently, the maximum detectable heart rate is 180 bpm. The lockout timer is reset each time a beat is detected, as well as when the signal nears the

minimum or maximum range of the ADC. This prevents the detection of large transients and saturation, which are likely caused by motion artifact or power supply noise. Conversely, if no beat is detected for 120 samples (2 s) the detector is assumed to have missed a beat, so the minimum detectable heart rate is 30 bpm.

One common beat detection procedure is to remove the signal offset and calculate a moving average of the signal's magnitude. To implement this approach, we designed a low-order high-pass FIR filter to remove the offset, and then calculated the absolute value of the filter's output. Our sampling rate is relatively low compared to most clinical ECG instrumentation; at the selected sampling frequency of 60 Hz, the entire ECG pulse typically occupies only three to four samples. Accordingly, we averaged over the expected signal duration of four samples. This result is then compared to a threshold value to determine whether a beat is present. This approach has several advantages: the detection algorithm has a relatively low computation requirement, and is capable of detecting both positive and negative beats (if, for instance, the user switches hands on the electrodes). However, the low number of available samples makes this approach somewhat sensitive to noise; this design tends to detect large noise spikes even if they do not resemble an ECG pulse.

To more effectively separate the signal from the noise, we considered applying a non-linear amplitude expansion function in place of the absolute value function. As the ECG spikes are typically larger than the noise, we hoped to isolate the signal by weighting more heavily large signal values. A common practice for this purpose is the square the signal before applying the moving average; in this way, larger amplitude spikes contribute more to the detector's result. However, the most efficient 8-bit multiplier we were able to implement in the PIC assembly code required over 50 operations. We attempted to reduce the number of operations by using a piecewise exponential function. This approach allowed similar functionality (by emphasizing larger signal values) using considerably fewer operations. However, testing indicated that adding these expansion functions actually hurt performance. This is likely because the level of noise present in our signal is much larger than in most clinical ECG signals. Thus, the noise was being amplified as much or more than the signal itself.

To reduce this issue, we instead considered median filtering. Calculating a moving signal median has a low-pass filtering effect with the advantage of high noise immunity. One approach to determine the signal median we considered involved sorting the previous signals. Unfortunately, the number of operations necessary to sort even lists of modest length (three or four values) is fairly large. This is because the PIC uses an accumulator-style architecture, where values must first be loaded into the working register before they can be moved or compared to other values. Furthermore, it is necessary to track the order in which the values arrived so that the oldest value can be discarded each time a new sample is added. As the goal was to increase noise immunity, we decided instead to discard only the sample with the largest magnitude, which is most likely to cause a false detection. We first found the signal's absolute value, summed the

previous four samples, then subtracted the largest value; this procedure required far less computation than the sorting method. However, this method also failed to perform well, because the ECG R-wave peak is typically only observed for one sample. Thus, this detection method removed the most prominent signal feature available.

As we had already taken steps to remove known sources of noise (powerline noise and large transients likely caused by motion artifact), we modeled the remaining noise as a Gaussian random process with constant covariance and time-varying variance. Gaussian noise seemed a reasonable approximation because the observed noise is likely a sum of many different random phenomena within the system; thus, the central limit theorem implies that this noise is likely to approximate the Gaussian distribution. Though the signal's covariance is likely to vary from user to user, much of it is also caused by the filtering in design's analog stage, which remains relatively consistent. The variance itself likely varies greatly between users based on skin impedance and proximity to sources of noise.

Based on this model, we attempted to develop an improved detector. For Gaussian noise, the optimal (highest probability of detection for a given probability of false alarm) detector is a matched filter with a pre-whitening phase (Kay, 1998). We took several seconds of training data that mimics expected user conditions. Within this data, we identified six ECG beats. Most of the signal power for these beats seemed to occur within five samples; accordingly, we aligned the beat signals and averaged them to produce a five-sample beat template (Figure 22).
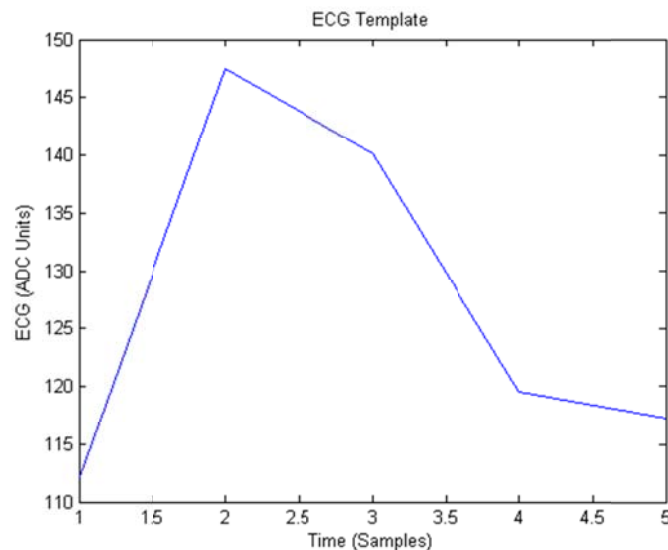
Figure 22 - ECG Template

We then estimated the noise covariance by calculating the covariance between each sample and the four samples preceding it; these covariance estimates for each point of training data were then averaged to produce a covariance estimate. We multiplied the beat template by the inverse of the estimated covariance matrix, and reversed the result to obtain whitening,

matched, finite impulse response (FIR) filter coefficients. We quantized these coefficients to four-bit, signed values; this provided reasonable performance while keeping the multiplication complexity low and preventing the result from become unmanageably large. The filter's frequency response peaks around 18 Hz, though it is fairly flat from 10 to 30 Hz where the QRS complex's signal power is larger than that of the noise. The filter does, however, block the signal's large DC component (Figure 23).
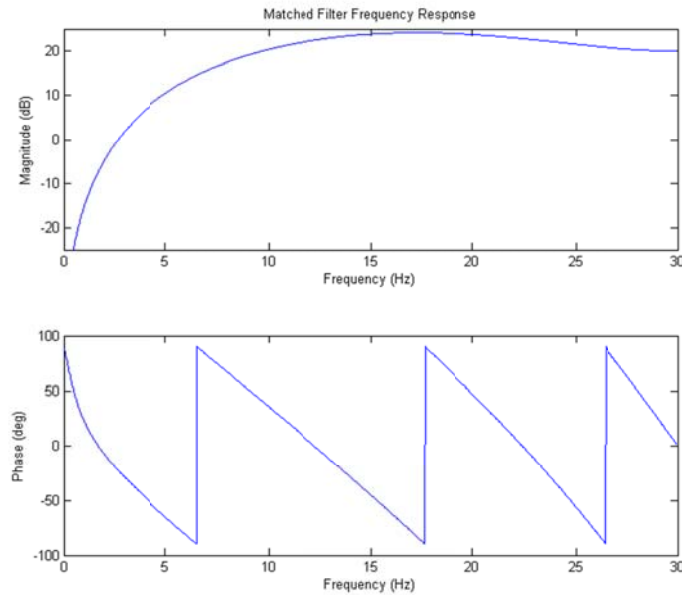
Figure 23 - Matched Filter Frequency Response

The following figure compares the original training signal with the filtered version of the signal, where the beats are much more distinguishable from the noise (Figure 24).
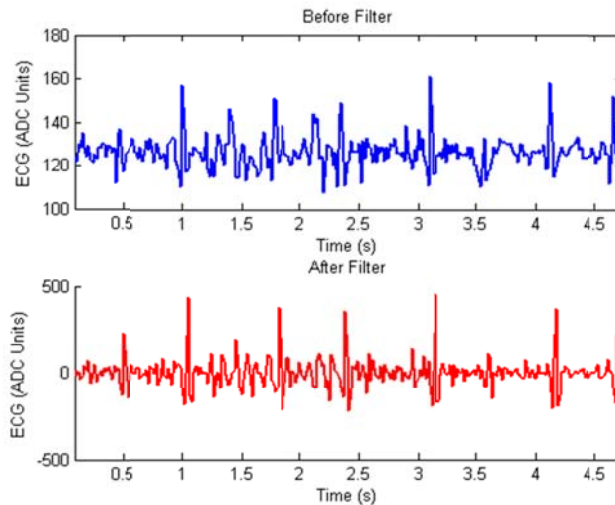
Figure 24 - ECG Matched Filter Performance

The matched filter has the FIR coefficients [-1, -3, 3, 8, -7]. This filter was implemented using shifting and adding to perform the multiplication operations, then updating the input samples by shifting the previous input memory locations. The result is stored using two bytes, required two registers.

The next step in detecting beats is to compare the processed signal to a threshold level; values above this threshold are determined to be beats (provided they do not violate the lockout timer). We first experimented with a fixed threshold, which has the advantage of requiring the least computation. Unfortunately, because of the wide variation in ECG amplitude and noise variance between users, finding a single fixed threshold that worked well for all users proved difficult. We decided instead to implement an adaptive threshold to allow remove the need for individual calibration. We first considered basing the threshold on the amplitude of previously detected beats. Each time a beat was detected, the threshold for the next beat would be set based on a fraction of the maximum observed signal. This threshold would then decay with time to prevent a particularly large spike from setting the threshold too high to detect future beats. This method proved difficult to implement effectively, as ECG amplitude and noise can vary considerably from one beat to the next. Furthermore, the rate of decay would have to be based on the heart rate to prevent the threshold from staying high for too long or decaying into the noise floor too quickly.

We decided instead to base the threshold on a noise estimate, setting the level just above the expected noise floor. By calculating a running estimate of the standard deviation of the noise, we were able to implement a Neyman-Pearson detection threshold. We began by noting that the standard deviation of a zero-mean, Gaussian process is well-approximated by a linear scaling (a factor of approximately 1.16) of the mean absolute value (Figure 25).
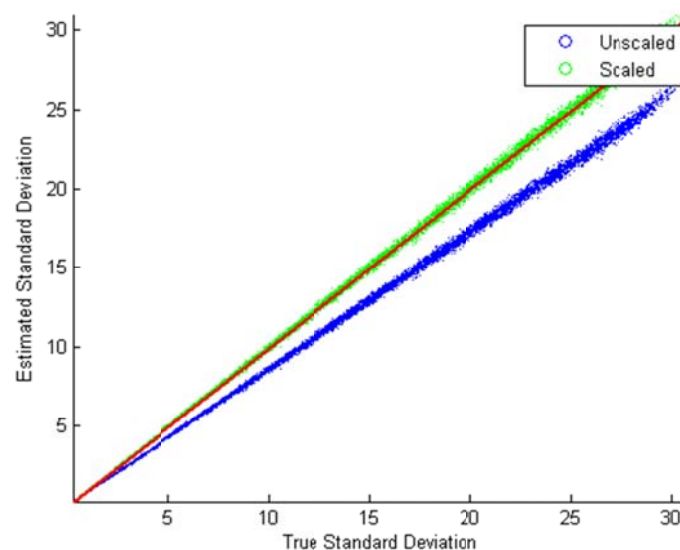
Figure 25 - Standard Deviation Estimator Performance

While calculating the true standard deviation requires computationally expensive squaring and square root operations, this approximation requires only absolute value, and as such is suitable for our low-power design. This method still requires a large running average; 256-sample averages were used to produce the results shown in the figure above. The computation involved in calculating this average directly may be reduced to only two arithmetic operations by using the previously calculated output in a cascaded integrator-comb topology. Each time the average is to be updated, the new sample is added to the previous output, and the oldest sample (the 256th sample) is subtracted from the result. However, this approach still requires sufficient memory to hold 255 previous samples, as well as computation to track the oldest sample and replace it with the newest. We decided instead to use an infinite impulse response (IIR) filter that mimics the behavior of this moving average. Each time the standard deviation estimate is updated, $1/256^{th}$ of the previous estimate is subtracted from itself. Then, the new value is added to the result. This process effectively functions as an IIR filter with the transfer function

$$H(z) = \frac{1}{1 - \frac{255}{256}z^{-1}}$$

The filter acts like an integrator, but is stable with a DC gain of 256. Thus, the output provides a reasonable approximation of the mean of the previous 256 values, resulting in an estimate of the signal's standard deviation. The result is stored using three bytes, requiring three registers.

Assuming Gaussian noise, a threshold of twice the estimated standard deviation (approximately 1.16 the true standard deviation) should result in a probability of false alarm below five percent. Furthermore, the matched whitening filter maximizes the probability of detection for this false alarm rate, though the rate of detection itself is based on the ECG amplitude.

Heart Rate Estimation

Once the beat is detected, we attempted to estimate the heart rate based on the period between beats. To improve immunity to noise caused by missed or extra beat detections, we implemented a combined median and averaging filter. Once a beat is detected, the newest period and seven previous periods are sorted. As the previous seven beats are already sorted in relation to each other, we use a binary search tree to remove the oldest sample from the previous sorted list, then another binary tree to insert the new value in the correct location. Once sorted, the median four values are summed to form a scaled estimate of the beat period. This effectively prevents the two highest and lowest values (which are most likely to be missed or extra beats) from affecting the result and improves resolution beyond what would be possible with single value and a 60 Hz sampling rate by summing four period measurements.

To calculate the heart rate, we implemented a lookup-table-based division algorithm. The estimated period is first scaled (with bit-shifting) to place it within the range of the 64-entry

table. The table contains the result of dividing 3600 by the input address; the output is therefore the heart rate in beats per minute. This result is then shifted again based on the pre-division scaling. This approach is significantly faster than a non-restoring division algorithm we originally used, though it has the drawback of using more than half of the available register memory. This output is then passed to the LCD driver module for display.

PPG Analog Design

This section contains component selection and design details for the PPG circuit, consisting of pulsing LED and integrator circuits. Circuit requirements, theory of operation and alternative topologies are also discussed.

Requirements

The PPG circuit requires the solar panel to power an LED to capture the user's pulse rate. The selected 850mm IR LED requires approximately 20mA to shine at nominal brightness. Obviously, the LED cannot be powered continuously by the solar panel, as it would require significantly more power than the solar panel produces under typical indoor conditions.

Block Diagram

The high-level block diagram of the proposed PPG circuit is shown below (Figure 26). Our proposed solution briefly powers an infrared LED, and then detects the modulated light level after it passes through the user's finger. Because this signal has a very short duration, an integrator circuit is used to hold the signal long enough to meet the operational amplifier slew rate. The signal is then band-pass filtered to eliminate the DC bias caused by ambient light and dark current, as well as to remove potential high-frequency noise, before ADC sampling. Though we were not able to implement digital heart rate estimation algorithms for the PPG, we propose a detection algorithm involving peak detection to estimate the beat period.
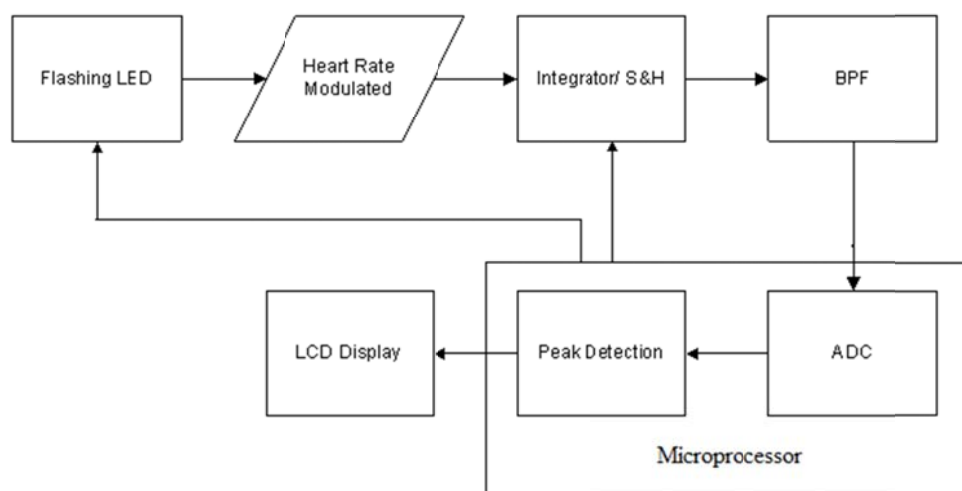
Figure 26 - PPG High Level Block Diagram

Pulsing LED Circuit

This section contains the description of the theory of operation of the selected pulsing LED topology along with a possible alternative. A comparison between the selected topology and the alternative is also included to show why the current topology was picked.

Theory of Operation

Figure 27 shows the selected pulsing LED topology for the PPG circuit. The topology makes use of the generated flyback current due to the inductor's collapsing EMF to power the LED efficiently. When the voltage across an inductive load is removed or reduced, current continues to flow through the inductor even if there is no path to ground; this current is called flyback current. Flyback current can potentially be dangerous if it reaches a sensitive part of a circuit. Normally, a freewheeling diode is used to dissipate the flyback current by feeding it back to the inductive load. This topology simply uses the IR LED as the freewheeling diode.
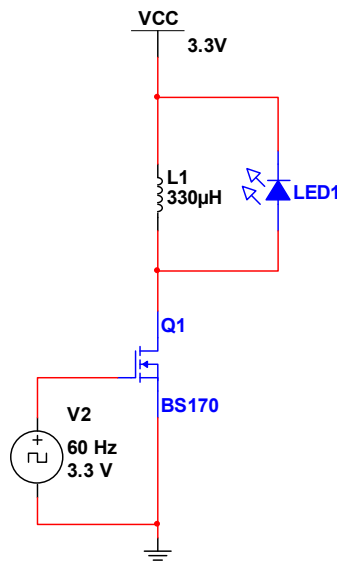
Figure 27 - Selected Topology for Pulsing LED

Recall that the equation for the voltage across an inductor is:

$$V(t) = L \frac{dI}{dt} \qquad (1)$$

Dividing both sides by the inductance yields:

$$\frac{dI}{dt} = \frac{V(t)}{L} \qquad (2)$$

Since V is constant and no current is initially flowing, we get the following equation:

$$I(t) = \frac{V}{L} t \qquad (3)$$

Equation 3 shows that the maximum current flow through the inductor can be controlled by the application and duration of voltage. More importantly, the current flow will increase linearly with time since the voltage is constant. This means the maximum current flow through the inductor can be easily controlled by the microcontroller.

Figure 28 is a graphical explanation of the previous statement. At time $t = 0$, the inductor current and the inductor voltage is zero. Between $t = t_1$ and $t = t_2$, the inductor current increases linearly with a slope of $\Delta I/\Delta t = V/L$, assuming that V is constant. Theoretically, when the voltage is reduced back to zero, the slope becomes zero and the inductor current stays at its maximum value. In realistic situations, however, the current flow through the inductor would be dissipated through some other paths.
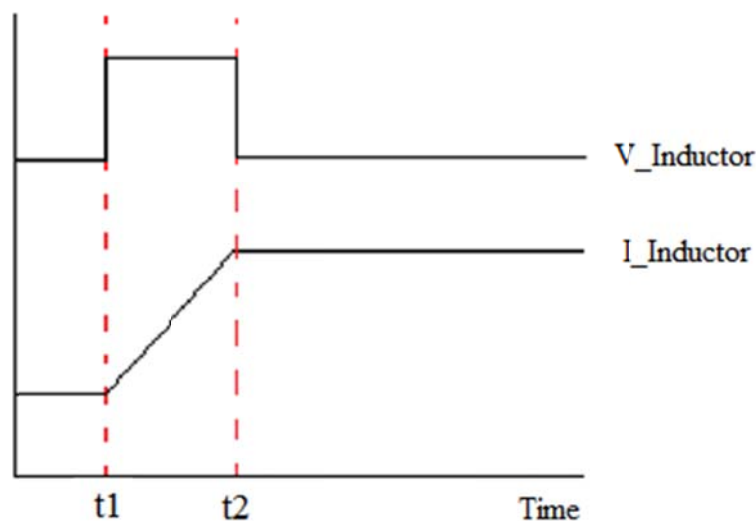
Figure 28 - Induction Current Timing Diagram

Figure 29 shows the timing of the events happening during the operation of the pulsing LED circuit in ideal conditions:

1. At 17 ms, the microcontroller's output pin goes high, pushing the MOSFET to its saturation region and causes current to flow from the positive voltage supply to ground through the inductor
2. After 4 µs, the microcontroller's output pin goes low, the MOSFET stops conducting, and the path to ground is cut off; no more current flow from the positive voltage supply
3. At the same time, the flyback current is fed back to the inductor and dissipated through the LED, causing a negative slope in the current flow through the inductor. During this time period, the LED lights up
4. After some amount of time, the current flow dissipates completely to zero
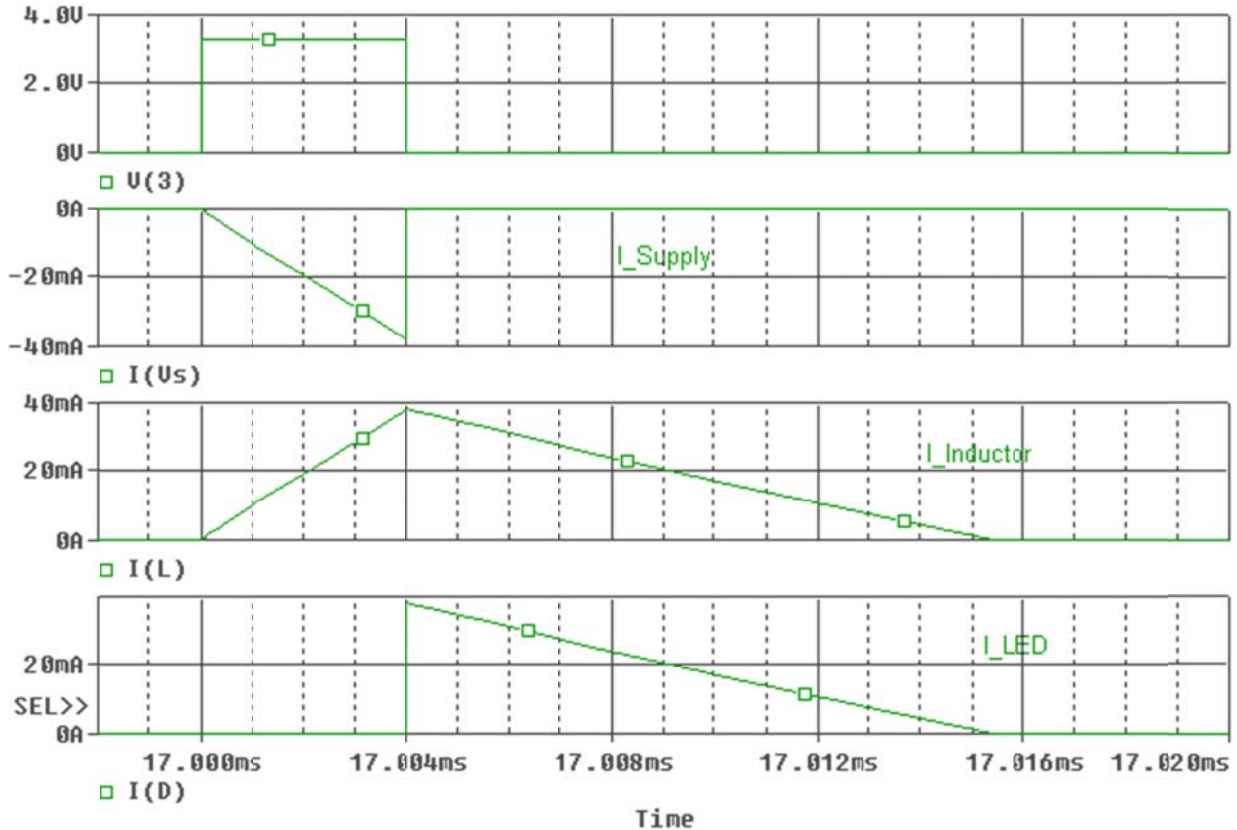
Figure 29 - Pulsing LED Timing Diagram

Component Values

The topology shown in Figure 27 was configured as follows:

- L = 330 µH – this value will be derived later in this section
- Pulse characteristic:
  - 0 to 3.3 V
  - Duration: 4 µs
  - Frequency: 60 Hz

Recall that the solar panel can only provide a maximum of 20 µA to maintain a 4 V output, for a total of 80 µW of available power. Since the LED is the most power consuming part of the device, half of the available current (10 µA) is reserved for powering it. According to the datasheet of the LED, a 20 mA current results in an approximately 1.2 V drop. This means 12 µW of the total available power is the maximum power allowable for the LED. The actual power being dissipated by the LED is approximately 6 µW as calculated later in the section.

A pulsing frequency of 60 Hz was chosen for three reasons:

1. The solar panel can support this pulsing frequency.
2. The pulse wave's frequency is below 20 Hz, so 60 Hz satisfies the Nyquist sampling theorem.
3. Power line noise at 60 Hz, as well as fluorescent light noise at 120 Hz, would be aliased down to DC, which is easy to filter out.

The second and third reasons are self-explanatory but the first reason requires some calculation. Referring back to Figure 29, the current flow through the inductor increases linearly and stops at its maximum value before being used by the LED. During this time when the current flow is increasing, the average current is approximately half the maximum value. The average current is calculated by finding the amount of electrical charge during the time duration that the current flow is increasing, and then dividing by the duration. The amount of charge is calculated by integrating the current flow with respect to time.

$$I_{avg} = \frac{1}{\Delta t}\int_0^{\Delta t} \frac{V}{L}t\ dt = \frac{1}{2}\frac{V}{L}\Delta t \qquad (4)$$

Since an average pulse current of 20 mA is desired, the maximum current flow across the inductor should be 40 mA, according to Equation 5. This average current is only applicable during the "active" state of the pulse. With a pulsing frequency of 60 Hz, the average constant current is calculated using a similar method:

$$I_{avg(DC)} = \frac{1}{T}\int_0^{\Delta t} I_{avg}dt = \frac{1}{T}I_{avg}\Delta t \qquad \text{where T} = \frac{1}{f} \qquad (5)$$

A maximum value of 10 µA was allocated for $I_{avg(DC)}$. The average DC current flow at 60 Hz is calculated to be approximately 5 µA, well within the capability of the solar panel.

The average amount of power dissipated by the LED is calculated as follow:

$$P_{avg\ LED} = I_{avg}V_{LED} = (5uA)(1.2V) = 6\ \mu W$$

Since a voltage regulator is used to power the device, there are only two levels of voltage available: 0 and 3.3V. Given that the voltage is constant for the duration of the pulse, and the desired slope of the current flow is 40 mA in 4 µs, the inductance is calculated as follow:

$$\frac{\Delta I}{\Delta t} = \frac{V}{L} \qquad (6)$$

$$L = V\frac{\Delta t}{\Delta I} \qquad (7)$$

Given that V = 3.3 V, Δt = 4 µs and ΔI = 40 mA; L is calculated to be 330 µH. Alternatively, Δt can be reduced to 2 µs and L reduced to 165 µH.

An alternative way to confirm the result is using the total amount of charge involved since charge is conserved in ideal condition. Since the average DC current is calculated to be 5 μA and the pulsing frequency is 60 Hz, the average amount of charge involved per pulse is:

$$\frac{5\ \mu A}{60\ Hz} = 80\ nC$$

In ideal conditions, this amount of charge has to be equal to the amount of charge supplied by the solar panel during the charging phase (shown in Figure 29) as shown below:

$$40\ mA * \frac{4\ \mu s}{2} = 80\ nC$$

The amount of time the LED lights up can be calculated since charge and energy have the relationship:

$$E = QV = IV\Delta t \qquad (8)$$

Since energy has to be conserved, the following equality can be used:

$$E = I_{LED}V_{LED}\Delta t = C_{solar\ panel}V_{solar\ panel} \quad (9)$$

$$\Delta t = \frac{C_{solar\ panel}V_{solar\ panel}}{I_{LED}V_{LED}} = \frac{(80\ nC)(3.3\ V)}{(20\ mA)(1.2\ V)} = 9\ \mu s$$

The result confirms that it is possible to provide an average of 20mA to the IR LED for 9 μs using a 4 μs pulse of the same average current, assuming 100% efficiency. Realistically, the efficiency of the circuit is closer to 80%.

Efficiency

It is often beneficial to calculate the efficiency of a topology, especially when given a strict power constraint. The efficiency is calculated as the ratio between "useful" energy and supplied energy. The "useful" energy is the amount of energy received by the LED to do useful work, such as lighting up. The supplied energy is the total amount of energy supplied by the solar panel. Energy is calculated by integrating the power with respect to time.

For this topology, the efficiency is calculated as follow:

$$E_{LED} = \int_{t_1}^{t_2+\Delta t} P_{LED}(t)\ dt \qquad (6)$$

$$E_{supply} = \int_{t_1}^{t_2+\Delta \tau} P_{supply}\ dt \qquad \text{Note that } \Delta\tau \neq \Delta t \qquad (7)$$

To clarify, $\Delta\tau$ is the time duration when current is actually flowing from the solar panel and Δt is the duration when LED is lighting up. The energy spent by the LED, and thus the efficiency, is determined by how long it takes for the current to dissipate.

Figure 30 shows the simulated power waveforms of the supply and the LED using PSPICE models. The efficiency of the topology is calculated to be approximately 80% using equations (6) and (7).
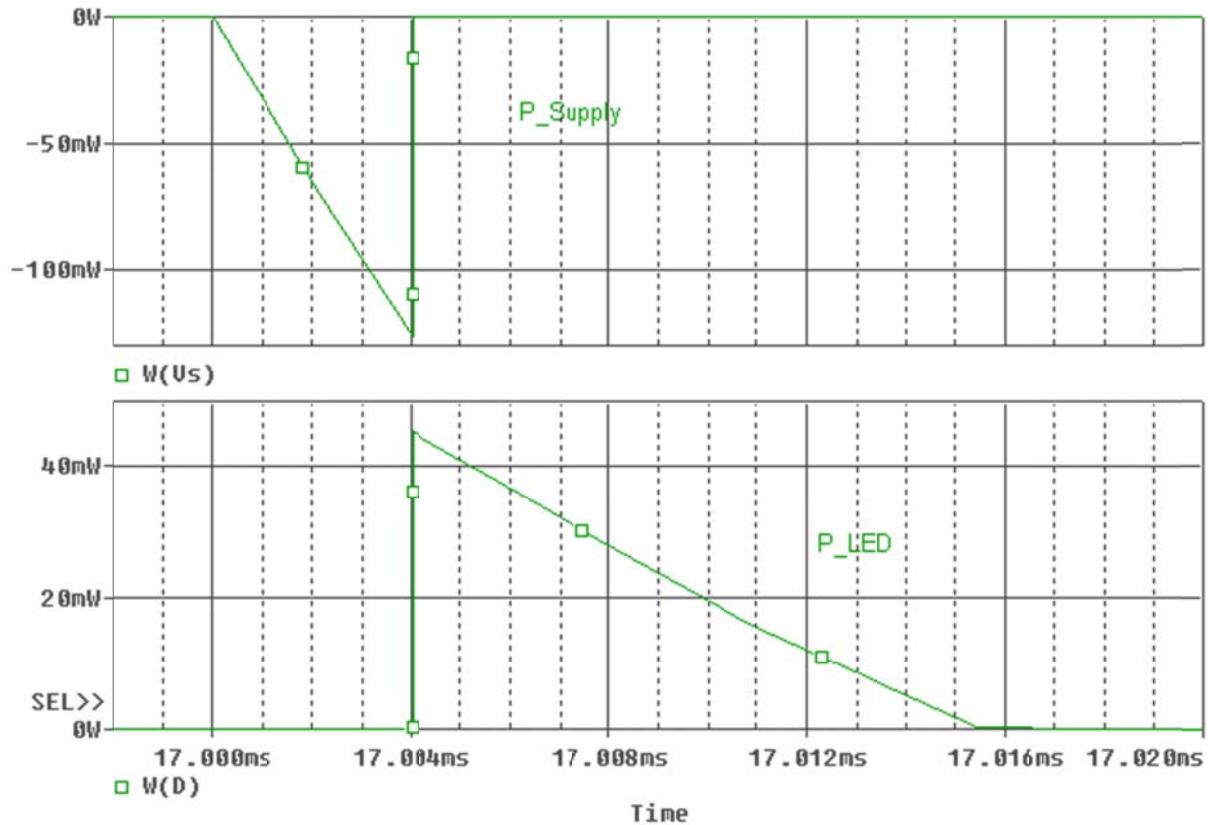
<p style="text-align:center">Figure 30 - Power Plot of Pulsing LED</p>

The calculations were done as shown below:

$$\text{E}_{LED} = \int_{t_1}^{t_2+\Delta t} P_{LED}(t)\, dt \approx \frac{1}{2}P_{LED\,peak}\Delta t = \frac{1}{2}(45\ mW)(11\ \mu s) = 247\ nJ$$

$$\text{E}_{supply} = \int_{t_1}^{t_2+\Delta t} P_{supply}(t)\, dt \approx \frac{1}{2}P_{supply\,peak}\Delta t = \frac{1}{2}(150\ mW)(11\ \mu s) = 300\ nJ$$

$$Efficiency = \frac{E_{LED}}{E_{supply}}100\% \approx 80\%$$

This fairly high level of efficiency is desirable for this project due to its severe constraints on power.

Experimental Result & Non-Idealities

       Figure 31 shows the experimental V-I characteristic of the LED and its best fit trend line. At 20 mA, the forward voltage drop is approximately 1.4 V instead of 1.2 V as stated in the datasheet.
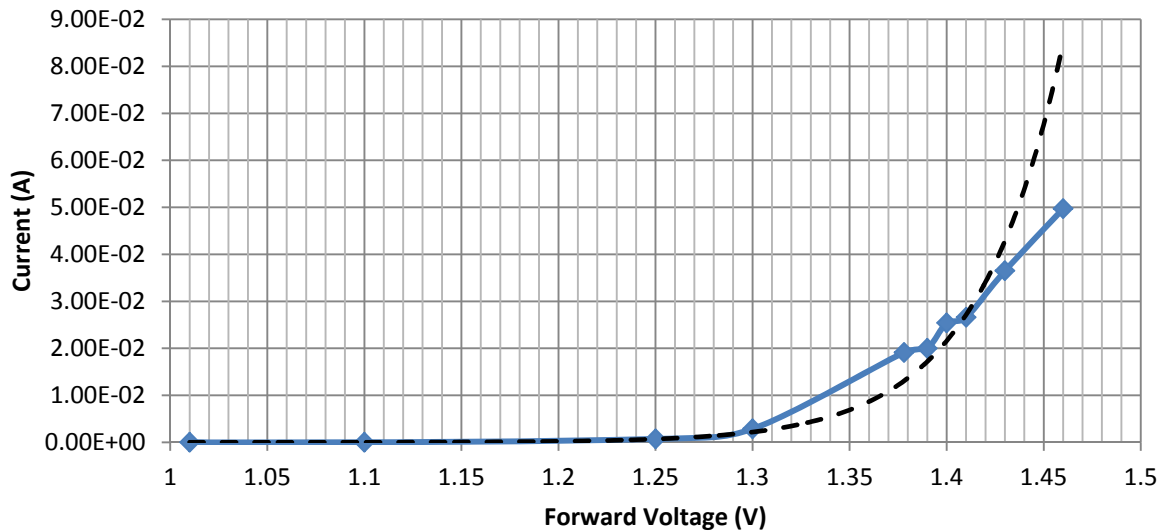
Figure 31 - IR LED Experimental VI Curve

Just like any real circuit, there are several non-idealities:

- Leakage current:
  - A small leakage current flow through the MOSFET even if it is in cut-off region
  - Small leakage current flowing through the LED
- Current flow error:
  - A small voltage drop of approximately 0.2 V appears across the MOSFET in its saturation region
  - Inductance value is not exactly its nominal value
  - Microcontroller pulses duration is not exactly the desired length
  - The forward voltage drop across the LED is closer to 1.4 V than 1.2 V at 20 mA
- There is a minimum requirement on current flow for the LED to light up

       Leakage current has some effect on the efficiency but has no effect on the operation of the topology. Since leakage current is not time variant, the voltage drop across the inductor is zero, which is the same as the ideal component assumption.

- According to the datasheet of the MOSFET, a maximum leakage current of 0.5 µA is expected for V_{DS} = 25 V. The leakage current would be much less at 3.3 V, but it is not listed in the datasheet, so the listed values are taken as maximum. This means there is a parasitic

resistance of approximately 50 MΩ.This equates to a maximum leakage current of 66 nA through the MOSFET in its "off" state.

- For the IR LED, a leakage current of 100 μA is expected for a reverse bias voltage of 5 V, equating to an approximately 20 MΩ parasitic resistance. Again, the leakage would be less at 3.3 V but it is not listed in the datasheet. A maximum leakage current of 165 nA is expected when the MOSFET is conducting.

Generally, a 5-10% of error in current flow has negligible effects on LED brightness:

- A voltage drop of 0.2 V across the MOSFET in its saturation region can be ignored because 0.2 V is only 6% of the voltage supply of 3.3 V. Since the current flow increases linearly, a 6% error equates to a 6% error in the current flow. According to the LED datasheet, 6% difference in current flow has a negligible effect on the brightness. However, this 6% voltage drop causes a 6% decrease in efficiency, which is a significant amount.
- A 5% error in the inductance value also has a negligible effect on the LED brightness since it equates to a 5% error in the current flow.
- The same reasoning applies to pulse duration and frequency.
- A slightly larger forward voltage drop across the LED has some effect on efficiency but none on the brightness

This topology uses the LED as a freewheeling diode to dissipate the flyback current from the inductor. However, the LED only conducts when a minimum amount of current is flowing. When the flyback current falls to a certain value (approximately 10 mA), the LED's requirement is not satisfied and it stops conducting.

At this point, the flyback current has no path to flow and starts to oscillate due to the parallel LC circuit formed by the inductor and the p-n junction capacitance in the LED. P-N junction capacitance occurs when there is a separation of charge across the depletion region while a voltage is applied across the diode. The separation of charge is due to the current flow not being high enough to forward bias the LED; this suddenly cuts off current flow.

The oscillation may potentially have a negative effect on the durability of the components. However, during performance evaluation, there are no noticeable adverse effects on the operation of the topology.

Alternative Topology

In addition to the selected topology, there is another alternative that was considered during the design process: serial induction.

Serial Induction Alternative

The serial induction topology is very similar to the selected topology since the same theory of operation applies. Figure 32 shows the alternative induction pulsing LED circuit.
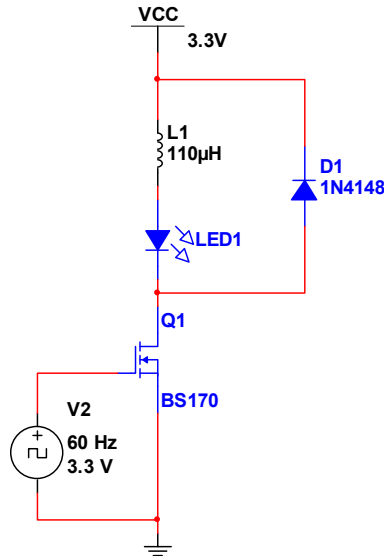
Figure 32 - Alternative Pulsing LED Topology

This alternative topology uses both the forward and flyback currents to power the LED. The LED is directly powered by the current flow through the inductor when the MOSFET conducts and the flyback current continues to power the LED after the MOSFET stops conducting.

Figure 33 shows the events timing of the serial induction topology. The main difference between this topology and the chosen topology is that the same current flows through both the LED and the inductor.

In terms of efficiency, the serial induction is slightly less efficient than the parallel induction topology, as shown in Figure 34.

Using equations (9) and (10), the efficiency of this topology is calculated to be approximately 69%, which is much lower than the 80% achieved in the other topology.

The inductance value is different because the forward voltage drop of the LED is approximately 1.4V for 20mA.This means there is only a voltage drop of $3.3 - 1.4 = 1.9$V across the inductor, resulting L = 190uH.

The advantage of this topology is that it uses slightly less energy to power the LED for a given amount of time (290 nJ instead of 300 nJ, based on simulation results). Plus, the inductance value is reduced by half, which could mean a reduction in physical dimension.

In term of efficiency, the serial induction topology is less efficient compared to the parallel induction topology. This is due to the added freewheeling diode dissipating power. Another drawback for this topology is the added cost of the diode.
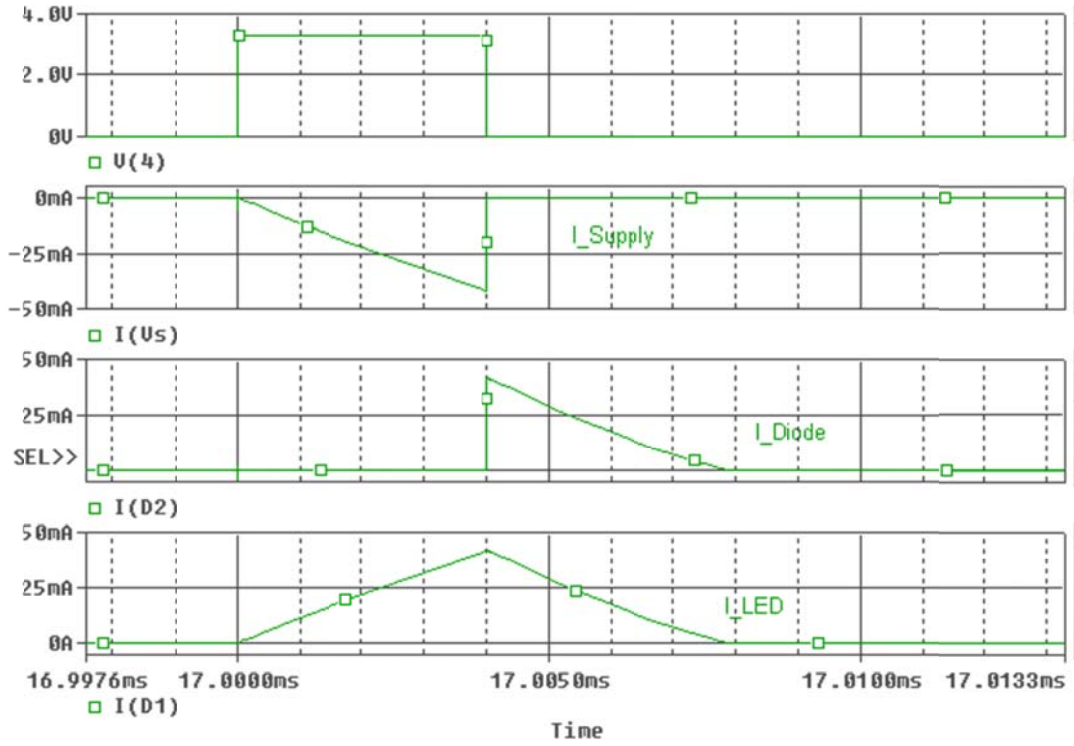
Figure 33 - Alternative Pulsing LED Timing Diagram
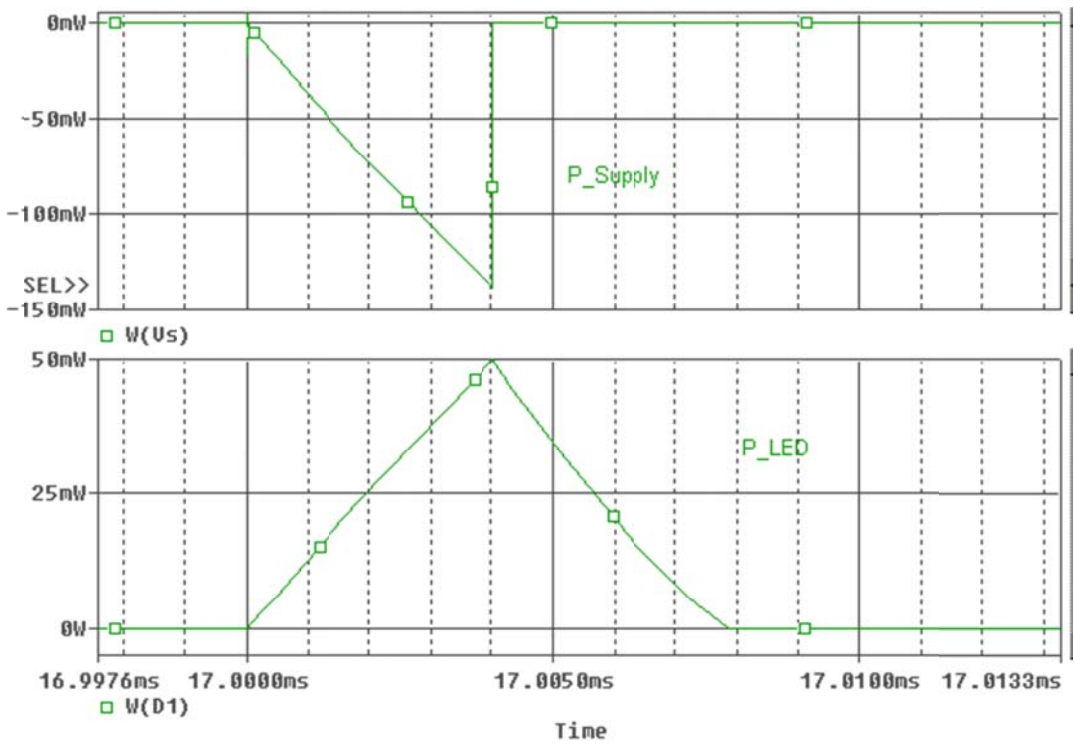
Figure 34 - Alternative Pulsing LED Power Plot

Integrator and Sample-and-Hold Circuit

This section contains the description of the theory of operation of the selected integrator and sample-and-hold (S&H) topology.

Theory of Operation

This topology uses a capacitor as a simple integrator to convert the current from the photodiode into voltage. The voltage is then band-pass filtered to amplify the frequency band that contains information corresponding to the pulse waveform. The output is then fed directly into the microcontroller's ADC. Figure 35 shows the selected topology for this part of the PPG circuit.
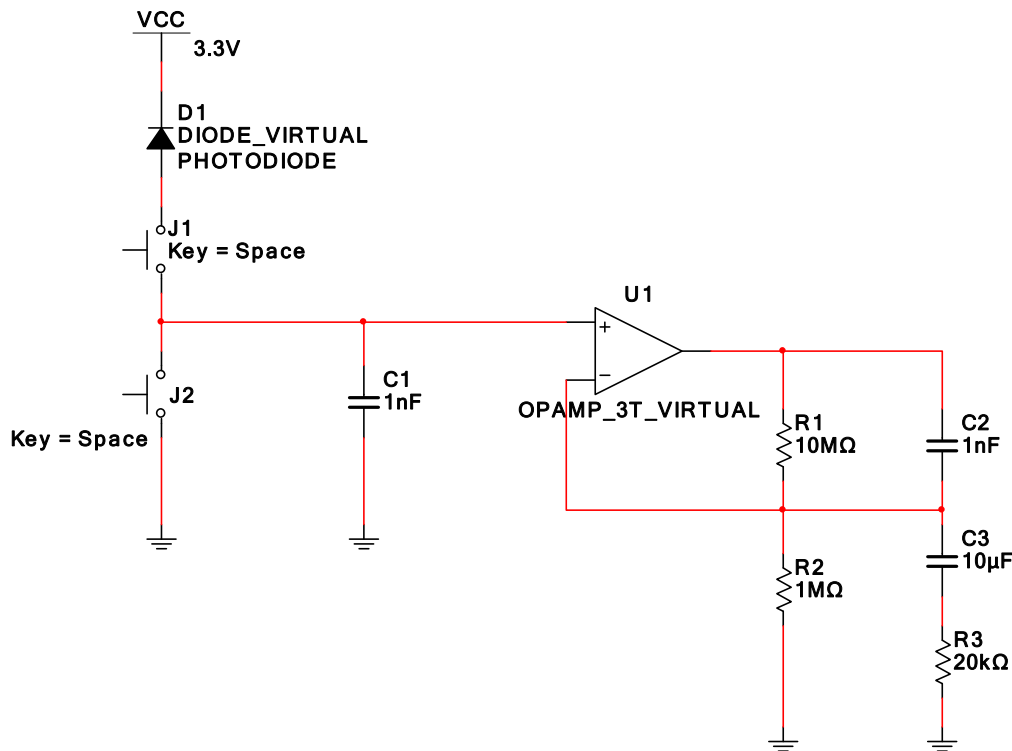
Figure 35 - Selected Integrator/S&H Topology

Recall that the equation for the current flowing into a capacitor is:

$$I(t) = C \frac{dV}{dt} \qquad (8)$$

Dividing both sides by the capacitance yields:

$$\frac{dV}{dt} = \frac{I(t)}{C} \qquad (9)$$

Solving for V, we get the following equation:

$$V(t) = \frac{I(t)}{C} t \qquad (10)$$

Equation 10 shows that the capacitor voltage varies directly with the amount and duration of the current flow. Since the LED can be easily controlled using the microcontroller, the time duration during which it lights up can be calculated, making the time duration t a fixed value. Therefore, the resulting voltage varies directly with the amount of current flow. Conveniently, the photodiode can be modeled as a time-variant current source with a DC component. When the photodiode detects IR light, reverse current flows into the capacitor and gets converted into voltage.

Equation 9 shows that if there is no current flow then the capacitor retains its maximum value. This is the sample-and-hold feature of this topology. The two analog switches control the current flow into and out of the capacitor. One analog switch resets the capacitor before the next LED pulse and the other controls the current flow from the photodiode.

The capacitor has to be reset; otherwise the charge will keep building up on every pulse of the LED. Eventually, the capacitor voltage will hit the 3.3 V supply and subsequent pulses will not be captured. Furthermore, the integrator should start at a known value (such as 0 V) to accurately capture the pulse rate.

Ambient light, 60 Hz noise and dark current are the main sources of "noise" for this circuit. Ambient light current may overpower the LED light and drastically reducing SNR. Dark current occurs when there is no light source, further reducing SNR.

The first analog switch (refer to Figure 35, switch labeled J1) is used to reduce the effects of these unwanted current sources. This task is achieved by allowing current to flow from the photodiode only when the LED lights up. Powerline noise from the user coupled to the photodiode is noticeable when the analog switch (J1) is connected between the power source and the photodiode; placing it between the photodiode and the capacitor prevents this effect.

Since the photodiode is allowed to conduct for only 4 μs, the effect of dark current is minimized. Furthermore, the ambient light is mostly eliminated because the user's finger will be covering the LED and the photodiode. There will still be some unwanted current flow due to ambient light, but the effect can be canceled as long as the capacitor is reset before the LED is pulsed.

Component Selections

This section contains a comparison between photodiode and phototransistor in the integrator and S&H circuit and discussion on how each component was chosen.

Photo sensors

Since the PPG circuit is based around capturing modulated light, the selection of the photo-sensor component is very important. There are two main types of photo-sensors considered: photodiodes and phototransistors. These photo-sensors work by producing photo-induced current. When photons with an adequate level of energy strike the sensitive region of the

sensor, a number of electrons are excited and make current flow. The main difference between photodiodes and phototransistors is sensitivity.

A phototransistor would be much more sensitive than a photodiode due to its physical characteristics. An ordinary BJT acts as a current amplifier, so it's expected that a phototransistor would also have a high current gain. High sensitivity is useful in detecting weak signals such as the heart rate. However, a phototransistor's advantage is also its disadvantage. Being so sensitive, the current flow caused by ambient light can easily overpower the actual signal. Leakage current would also become a bigger problem since the amount of dark current would be higher compared to a photodiode. Finally, the solar panel may not be able to support phototransistors since they can draw current in the range of milliamps instead of micro-amps like photodiodes.

Despite phototransistors' higher sensitivity, a photodiode was chosen for the PPG circuit instead. Since the photo-induced current does not have a closed form equation, it is simpler to measure the photodiode's sensitivity experimentally. Figure 36 shows how much current is expected for different DC LED current and Figure 37 shows the data for the current flow caused by the actual biometric signal.
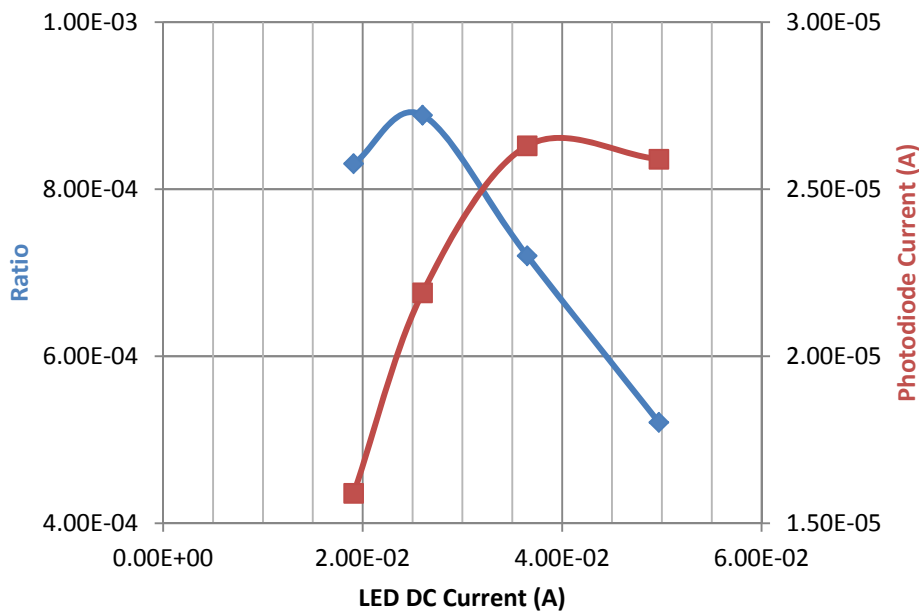
Figure 36 - Experimental Result of LED DC Current vs. Photodiode Induced Current
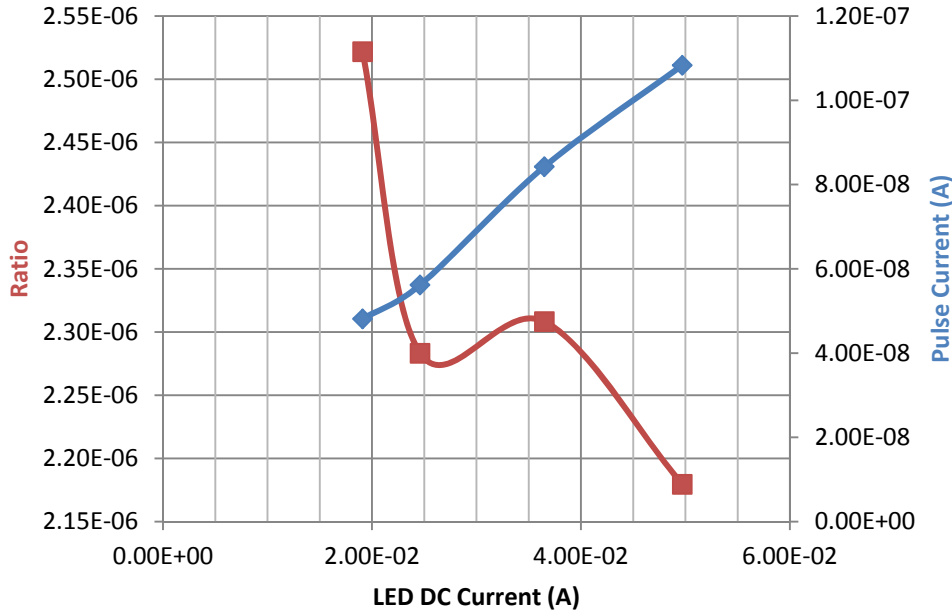
Figure 37 - Experimental Result of LED DC Current vs. Photodiode Signal Current

The ratio between the photo-induced current and the LED current is an indication of how "efficient" the chosen LED current is. A large value means more photo-induced current is achieved for a given LED current. Figure 36 shows that for the DC current of 20 mA, the circuit is not efficient in capturing the DC level of the LED. However, Figure 37 shows that the circuit is very efficient in capturing the heart rate induced current. It is desirable to efficiently capture the heart rate rather than the DC level; this is why the LED is designed to operate at an average current of 20 mA.

Integrator/S&H circuit

The capacitor value is picked experimentally by determining how much current is expected for different DC current flow through the LED (shown in Figure 36).According to the data, approximately 16 μA is expected from the photodiode. In addition to this DC current, a relatively small amount of current due to the actual signal is also expected (shown in Figure 37).

Using equation (10) to calculate the maximum DC voltage expected:

$$V(t) = \frac{I(t)}{C}t = \frac{16\ \mu A}{1\ nF} * 8\ \mu s = 128\ mV$$

A DC gain of 11 sets the bias level at 1.4 V

According to Figure 37, the expected current from the pulse signal is approximately 50nA.Using the same equation to calculate the maximum voltage expected from the actual pulse signal:

$$V(t) = \frac{I(t)}{C}t = \frac{50\ nA}{1\ nF} * 8\ \mu s = 400\ \mu V_{peak}$$

A mid-band gain of 500 equates to amplitude of 200 mV assuming that the current flow caused by the signal is constant.

Band-pass Filter

The voltage is then fed into the band-pass filter with the following transfer function:

$$V_{out} = 1 + \frac{R_1||Z_{C_2}}{R_2||(R_3 + Z_3)}V_{in} = 1 + \frac{R_1}{R_2}\frac{(1 + s(R_2 + R_3)C_3)}{(1 + sR_3C_3)(1 + sR_1C_2)}V_{in}$$

Using the following resistance and capacitance values (shown in Figure 35):

- R_1 = 10MΩ
- R_2 = 1MΩ
- R_3 = 20kΩ
- C_2 = 1nF
- C_3 = 10μF

This filter has the following characteristics:

- DC gain = $1 + \frac{R_1}{R_2}$ = 11
- Mid-band gain = $\frac{R_1}{R_2||R_3}$ = 500
- Zero at $\frac{1}{2\pi(R_2+R_3)C_3}$ = 1.6e-7 Hz
- Poles at $\frac{1}{2\pi R_3 C_3}$ = 0.8 Hz and $\frac{1}{2\pi R_1 C_2}$ = 16 Hz

Since the desired signal frequency is less than 20 Hz, the cut-off frequency is set to be 16 Hz. Also, the 60 Hz power transmission noise and the 120 Hz fluorescent light noise are aliased down to DC so it is undesirable to have high gain at DC. That is why the zero is set to be very small but not DC. A DC gain of 11 sets the bias for the amplified signal. Figure 38 shows the Bode plot of the BPF's frequency response:
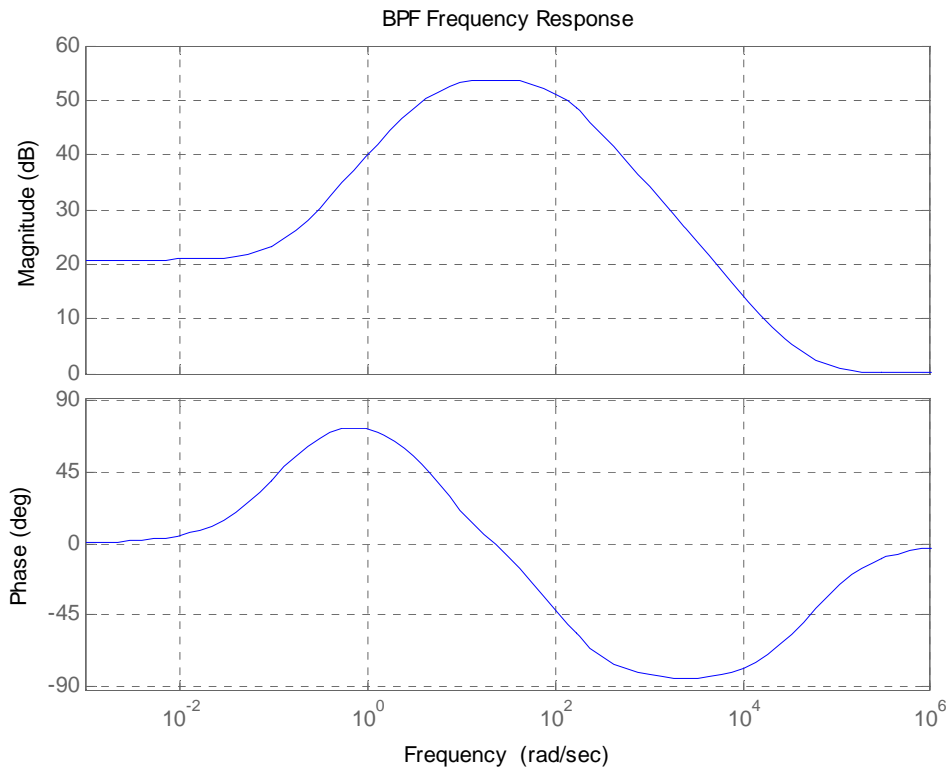
Figure 38 - Frequency Response of the BPF

Future Recommendations

In future projects, it is recommended to improve and implement the PPG circuit due to its superior signal quality, compared to the ECG circuit. Currently, the PPG circuit functions with adequately. Figure 39 shows the well-defined pulse waveform captured using the PPG circuit.
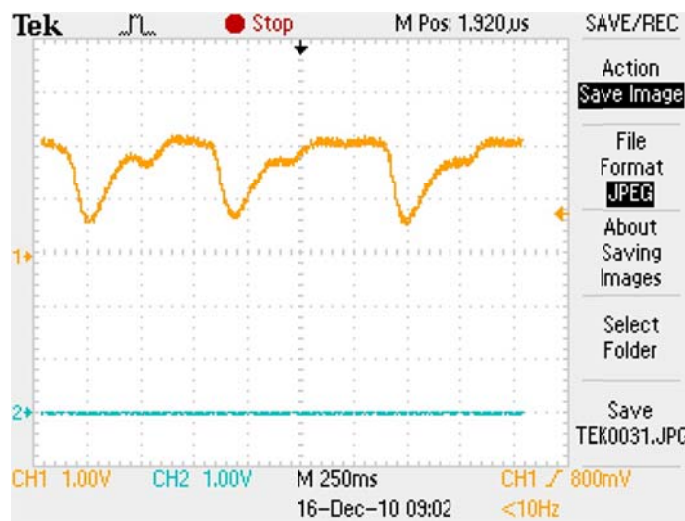
Figure 39 - Measured PPG Signal

This waveform represents the highest quality signal we observed using the PPG circuit. The quality of the signal varies with the finger pressure of the user. More pressure forms a better seal, blocks out ambient light and results in a clean waveform. However, too much pressure prevents blood from reaching the capillaries in the finger tip with each heart beat, which is the basis of operation for the PPG circuit.

It is desirable to keep the output signal power level constant for varying input amplitude levels to minimize quantization errors, thus ensuring high performance from the digital detection algorithm. One possible way to is to use an automatic gain control (AGC) circuit to regulate the power level of the signal.

Automatic Gain Control Proposal

An AGC circuit employs a feedback loop to make correction in the amplifying phase of the PPG circuit. There are two options for the implementation of the feedback loop: digital and analog. Due to the limitation of the PIC microcontroller used in this project (i.e. lack of a DAC), it is not a viable option to use a digital feedback system. Some headway could be made using PWM as a makeshift DAC, but due to the time constraint of this project, this option was not investigated further. With fewer constraints on power and cost, the digital feedback loop would be a better choice than the analog loop due to its robustness and ease of implementation.

An analog feedback loop is investigated and a proposed circuit layout is shown in Figure 40.
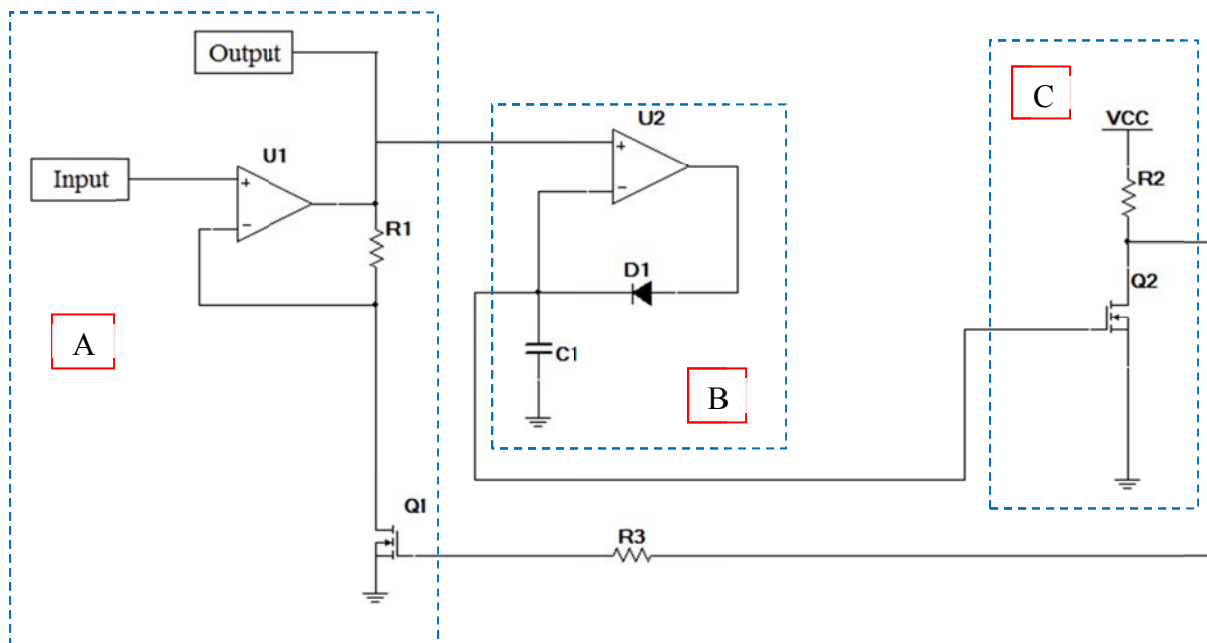
Figure 40 - Automatic Gain Control Schematic

There are three components in the proposed analog feedback AGC system: the variable non-inverting amplifier, the peak detector and the voltage controller.

Component A, the variable amplifier, is the main component responsible for keeping the power level of the output signal constant. This component requires a control voltage to change the closed-loop gain. The closed-loop gain is expressed as:

$$A = 1 + \frac{R_1}{r_{ds}}, \text{ where } r_{ds} \text{ is the drain-source resistance of the transistor}$$

This amplifier varies its gain by controlling r_{ds} using the control voltage. The equation for r_{ds} of a MOSFET in triode region is given as:

$$r_{ds} = \frac{1}{k_n'(\frac{W}{L})(V_{GS} - V_{TH})}$$

The gain of the amplifier in terms of V_{GS} becomes:

$$A(V_{GS}) = 1 + k_n'(\frac{W}{L})R_1 V_{OD} = 1 - k_n'(\frac{W}{L})R_1 V_{TH} + k_n'(\frac{W}{L})R_1 V_{GS}$$

The equation above shows that the gain varies linearly with the control voltage, which is desirable because the signal is not distorted. Finally, in order to keep the MOSFET in triode region, V_{DS} has to be smaller than the overdrive voltage $V_{OD} = V_{GS} - V_{TH}$

Component B is a peak detector circuit. This topology is essentially a voltage follower, driving the voltage drop across the capacitor to be the same as the input. Current flows into the capacitor only when the input is increasing. When the input decreases, the diode prevents current from flowing out of the capacitor, keeping the maximum value of the input minus the 0.7 V drop across the diode. The value of the capacitor affects charge retention, as well as the stability of the feedback loop.

Even though this topology is proposed, it is not the best choice for the design. The PPG circuit only uses one op-amp of the dual package, so it is desirable to design the AGC using only one op-amp. There are many examples of peak detector circuit without using op-amps, but they require either a constant current source or a negative supply voltage. Neither is supported by the solar panel. One way to work around this limitation is to create a virtual ground, but that will require even more op-amp.

Component C is a simple common source amplifier, which has a negative gain. An increase in the input voltage means a decrease in the output. The gain of the common source amplifier is given as:

$$A = -g_m(R_D||r_o) \approx -g_m R_D$$

Since the solar panel cannot supply negative voltage, the amplifier has to be biased. The bias plus the largest voltage swing has to be larger than V_{TH} but small enough to keep the MOSFET in component A in triode region.

There are many variables that have to be taken into account when designing the proposed circuit, the most important one being the range of the input signal voltage. For this project, the signal amplitude is measured using DC LED current (refer back to Figure 36 in the PPG circuit description section), which gives an approximation of what the signal amplitude would be when pulsed current is used.

Note that finger pressure plays a major role on the quality and amplitude of the signal. At the time of this project, there is no quantitative way to effectively measure finger pressure without using a pressure scale. Future projects that want to implement this design have to overcome this challenge.

Physical Alternative

Another way to minimize the effect of finger pressure on the quality of the signal is simply using a physical device to apply constant pressure on the user's finger. This method is widely used to measure blood oxygen level in medical offices. It is also the most effective and simplest way to ensure the quality of the signal. However, due to cost and PCB prototyping technology constraints at the time of this project, this alternative is not a viable option.

Printed Circuit Board Design

This section contains design details for the ECG printed circuit board (PCB) revisions.

Revision One

The primary design considerations involved in the PCB design concern the area constraint: the board must be the size of a business card (3550 by 1970 mil). The solar panel and LCD have rigid dimensions (unlike the electrodes), and occupy much of the available area, so the placement of these components was considered first. In the earliest revision, the solar panel and LCD were placed in the center-North and center-South sections of the board, respectively. Electrodes occupied the East and West sides of the board, and the remaining components were relegated to the underside. The microcontroller was placed directly beneath the LCD to allow efficient routing of the LCD driver pins. Because the analog portion of the ECG circuit contains several high-impedance nodes, the analog section was located as far as possible from the digital traces to reduce the possibility of noise coupling, and close to the ungrounded electrode. Placement of power planes on both the top and bottom sides of the board helped to further reduce the chance of noise coupling. Because the available power is low, we chose to ground both power planes (rather than wire one to the regulated power supply) to reduce the risk of the user accidentally introducing a path from the regulated supply directly to ground simply by holding the board.
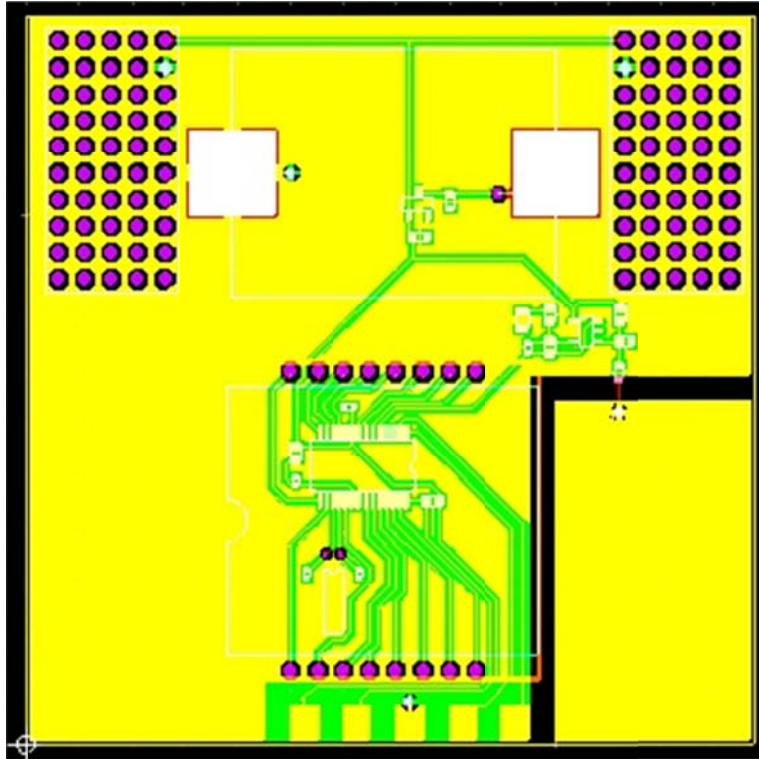
Figure 41 - PCB Revision 1

All component packages were surface-mount except for the LCD and oscillator, which were not available in surface-mount packages. All footprints were designed using Ultiboard's Part Wizard tool, and were based on mechanical specifications in the component datasheets. Passive components were from selected based on price, and so were from several different manufactures and in different packages. Trace width and clearance was set at 10mil, and vias were 24mil in diameter; these values are large enough to ensure reasonable trace impedance and manufacturability. Because of the solar panel and LCD placement, this design exceeded the acceptable dimensions. Additionally, Professor McNeill suggested that the components be located on the top of the board; making the components easily visible should promote user interest in electrical engineering, one of the fundamental project goals.

Revision Two

To fit the solar panel and LCD within the acceptable boundaries, the layout was changed to put them next to each other, in the North-West and North-East corners. This left room for electrodes on either side directly below these components, and space in the center of the board for the remaining components. All components were placed on the top layer. Again, the high-impedance analog nodes were kept as far as possible from potential noise sources. As this revision of the board was the first to be fabricated, we added a large debugging area with space for through-hole components. Passive components were selected to use common footprints (0402 pads for capacitors and 0603 pads for resistors).Pads were added in the operational amplifier

circuit feedback loops to allow different circuit configurations to be implemented, if necessary. We also inserted spaces for zero-ohm resistors in many of the traces to allow blocks of the board to be isolated and operated independently.
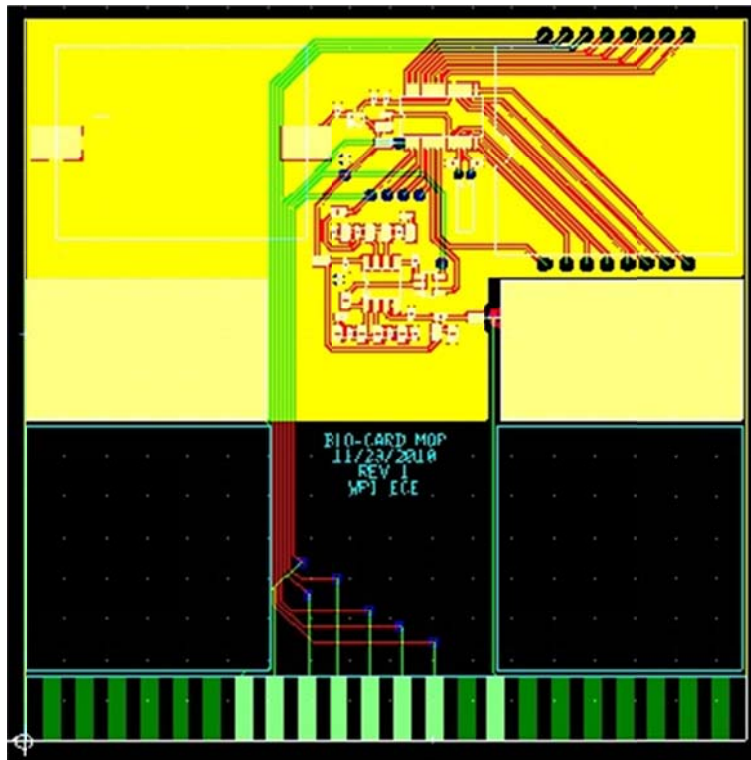
Figure 42 - PCB Revision 2

This revision introduced the card-edge connector pads, which were intended to be between the two electrodes; however, they were instead placed below the debugging area, so as to be on the board's edge. Sufficient room was left where they would be placed in the final revision. Time constraints prevented us from adding circuitry for the PPG design. To reduce costs and decrease manufacturing time, we specified a lead-free hot air solder leveling (HASL) finish, as it was likely to serve adequately as an ECG electrode surface. Solder mask was applied to both the top and bottom to minimize accidental power loss caused by contact with the user.

Revision Three

Having debugged the design on the previous revision, several changes were made to component footprints. To increase the ease of soldering, the capacitor pads were changed to larger 0603 pads. The voltage regulator pads were made larger, as the original footprint did not extend beyond the pins, making a reliable solder joint difficult to achieve. The hole size for the crystal oscillator pins was increased, as the original holes barely allowed the pins in. Despite thermal reliefs, the solar panel pads proved too large to solder easily (as it was difficult to sufficient heat such a large area), so we reduced the pad area. Reference designators were added for all components were added to the silkscreen to allow easier assembly. Finally, we removed the unused and zero-ohm-resistor component pads, as well as the debugging section, and

properly placed the card-edge connector pads. The completed ECG PCB design is shown below (Figure 43).
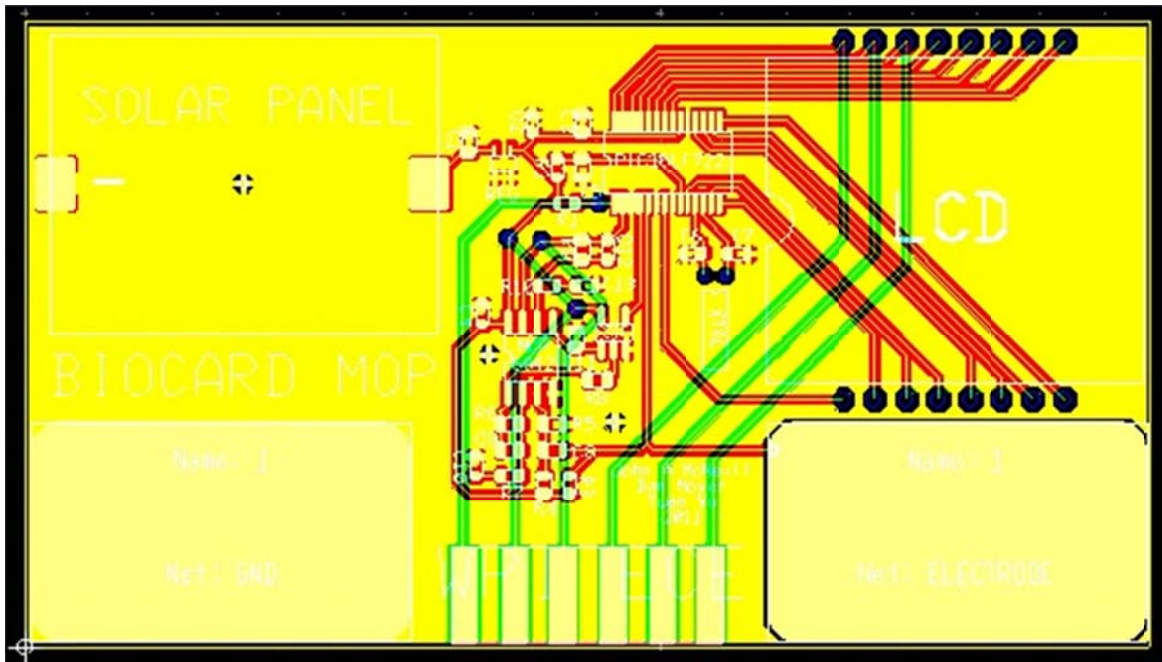
Figure 43 - PCB Final Revision

Results

This chapter summarizes the performance of the fully-implemented ECG design and the investigated PPG design.

Power Consumption

To measure the power consumption, the solar panel was replaced by a voltage supply with a 10kΩ series resistor. Voltage across this resistor was used to determine the operating current as component blocks were added to the board. The following table illustrates the power used by each component.

Part	Current Drawn
Voltage Regulator	1.35 µA
Analog Stage 1	1.28 µA
Switch	0.2 µA
Analog Stage 2	0.3 µA
Microcontroller (60 cycles)	2.6 µA
LCD	1.2 µA
Full System	7 µA

Table 3 - ECG Power Consumption

The test board draws significantly more power when an input large enough to result in operational amplifier saturation was applied. We noted that powerline noise does not typically reach this level unless the board is well-grounded and the user contacts only the ungrounded electrode. When the board is not grounded (i.e., under normal operation when the board is not attached to a power supply or oscilloscope), the noise level does not reach a large enough amplitude to cause this issue.

We also noted that the microcontroller draws significantly more power if an analog signal is applied to a pin configured for digital input, even if the tri-state buffer is enabled. The effective resistance to ground in this situation is approximately 200 kΩ, drawing enough current to prevent proper operation.

The solar panel should provide 16 to 20 µA under moderate indoor lighting, which is sufficient to meet the 7 µA current demand. The device operates properly under reasonable indoor lighting conditions, including the fluorescent lighting present in the lab.

Heart Rate Estimation Performance

Standing heart rates of six subjects were measured by counting pulses felt at each subject's wrist for 15 seconds. The subject's heart rate was simultaneously measured using the device, under indoor lighting conditions. The device provided an accurate (within 5 bpm) estimate of five of the subjects' heart rates. The device's failure to achieve an accurate estimate of the remaining subject was likely because of the subject's high skin resistance (which was

measured to be over 1 MΩ). This would have the effect of increasing the level of noise while simultaneously reducing the ECG amplitude, resulting in poor performance.

PPG Performance

In summary, the PPG analog circuitry is capable of capturing fluctuation of the light absorption in the user's capillaries; which correspond to the user's heart beat. The output voltage is scale appropriately to fully utilize the 3.3V dynamic range of the ADC. The most power consuming component of the circuit is the flashing LED, which consumes an average current of 5µA and achieving an efficiency of up to 80%.

Although a dedicated digital signal path was not developed for the PPG circuit, the peak detection algorithm used in the ECG can easily detect the heart beat in the PPG signal. This is due to the limited number of noise sources for PPG: 60Hz noise and fluorescent light noise; both of which can be easily removed using a high pass filter.

As discussed in the PPG circuit description, the analog circuitry is fully functional but not robust to users' actions. Specifically, the amount of finger pressure that the user applies to the device causes this unreliability. Too much pressure and the blood cannot reach the capillaries, which is the basis of operation for PPG; too little pressure and the signal will be drown out by ambient light.

A proposed method for increasing the reliability of the PPG circuitry can be found in the Future Recommendation chapter. Additionally, a more detailed discussion of the PPG circuit performance is included in the PPG circuit description chapter.

Cost and Bill of Materials

The ECG circuit bill of materials is summarized below (Table 4). Prices are listed for quantities of 100 from Digikey.

Part Number	Digikey Number	Description	Value	Reference Designators	Quantity	Unit Price (100)	Total Price (100)
AM-1819CA	869-1006-ND	Solar Cell	4 V, 20 µA	SOLAR PANEL	1	207	207
LCD-S2X1C50TR	67-1787-ND	LCD	2.5 Digit	LCD	1	178	178
PIC16LF722-I/SS	PIC16LF722-I/SS-ND	Microcontroller	8-bit ADC	PIC16LF722	1	109	109
MCP6042-I/SN	MCP6042-I/SN-ND	Op Amp	14 kHz GBW	MCP6042	1	60	60
XC6218P332NR	893-1087-1-ND	Linear Regulator	3.3 V	REG	1	36.6	36.6
TS5A4594DBVR	296-17705-1-ND	Switch	NO	SW	1	29.7	29.7
AB26T-32.768KHZ	535-9032-ND	Crystal	32768 Hz	XTAL	1	14	14

GRM188R61A105KA61D	490-1543-1-ND	Capacitor	1 uF	C1, C2	2	2.24	4.48
GRM188R71C104KA01D	490-1532-1-ND	Capacitor	100 nF	C3, C4, C10, C13	4	1.04	4.16
GRM188R71H103KA01D	490-1512-1-ND	Capacitor	10 nF	C8	1	1.01	1.01
GRM188R71H102KA01D	490-1494-1-ND	Capacitor	1 nF	C11	1	1.11	1.11
GRM1885C1H331JA01D	490-1439-1-ND	Capacitor	330 pF	C9, C12	2	2.8	5.6
GRM1885C1H330JA01D	490-1415-1-ND	Capacitor	33 pF	C5, C6, C7	3	1.56	4.68
ERJ-3GEYJ106V	P10MGCT-ND	Resistor	10 MΩ	R3, R4, R5, R6, R9	5	0.79	3.95
ERJ-3GEYJ204V	P200KGCT-ND	Resistor	200 kΩ	R7, R10	2	0.79	1.58
ERJ-3GEYJ103V	P10KGCT-ND	Resistor	10 kΩ	R1, R2, R8	3	0.79	2.37

Table 4 - ECG Bill of Materials

The total estimated component cost for 100 boards is $663.24, or approximately $6.63 per board. A quote for 100 PCBs from Advanced Circuits was $460, or $4.60 per board. The total cost for quantities of 100 is $1123.24, or $11.23 per board. This is significantly more than our $1 per board goal, despite our best efforts to use only low-cost components. Both the solar panel and the LCD, components considered vital to the project, each cost more than a dollar alone. The $1 goal will therefore not be feasible under the cost of these components deceases dramatically.

Conclusion

We were able to design and fabricate functioning, solar-powered, portable bioinstrumentation. The final ECG board meets the assigned size and power constraints, though we were unable to meet the cost goal. Our design addresses typical sources of noise for ECG and uses matched filtering with an adaptive Neyman-Pearson threshold to provide accurate heart rate estimates for most of our test subjects.

We were also able to design and test a proof-of-concept prototype for the PPG approach. Because the solar panel provides very little power, our PPG design faced significant challenges compared to the lower-power ECG approach. However, we were able to provide sufficient power to pulse an LED and measure the reflected short-duration signal. The PPG offers promising future work, as the conditioned signal typically exhibits a lower level of noise than the ECG circuit, with the potential to provide increased beat detection performance.

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Appendix A – ECG Digital Algorithm

This appendix contains the PIC16LF722 assembly code implementation of the ECG digital design.

```
;-------------------------------------------------------------------------------
; ECG Heart Rate Monitor
; Biocard MQP
; WPI ECE
; Dan Moyer
; 3/1/2011
;-------------------------------------------------------------------------------


;-------------------------------------------------------------------------------
; Processor Declaration
;-------------------------------------------------------------------------------
LIST          p=16LF722
#INCLUDE      <P16LF722.INC>


;-------------------------------------------------------------------------------
; Configuration Setup
;-------------------------------------------------------------------------------
__CONFIG      _CONFIG1, _DEBUG_OFF & _PLL_DIS & _BORV_1_9 & _BOR_OFF & _CP_OFF &
_MCLR_EN & _PWRT_EN & _WDT_OFF & _EXTRCIO
__CONFIG      _CONFIG2, _VCAP_DIS


;-------------------------------------------------------------------------------
; Configuration Definitions
;-------------------------------------------------------------------------------
#DEFINE               TRISA_CONFIG 0x9B  ; PORTA TRIS Configuration
#DEFINE               TRISC_CONFIG 0x03  ; PORTC TRIS Configuration
#DEFINE               ANSELA_CONFIG 0x1B ; PORTA ANSEL Configuration
#DEFINE               INTCON_CONFIG 0x40 ; INTCON Configuration
#DEFINE               PIE1_CONFIG        0x41  ; PIE1 Configuration
#DEFINE               T1CON_CONFIG 0x9C  ; Timer1 Configuration
#DEFINE               ADCON1_CONFIG 0x30 ; ADC Control Register 1 Configuration
#DEFINE               ADCON0_CH3         0x0D  ; ADC CH3 Configuration


;-------------------------------------------------------------------------------
; Memory Allocation
;-------------------------------------------------------------------------------
#DEFINE               DIV_TABLE          0x20  ; Division Lookup Table
#DEFINE               T_MEM              0x60  ; Previous 8 Periods
#DEFINE               LCD1_TABLE         0xA0  ; LCD Lookup Table for Port B (Digit 2,
COM)
#DEFINE               LCD2_TABLE         0xAA  ; LCD Lookup Table for Ports A, C
(Digit 1, 3)

S0                    EQU 0x68                                ; Sorted Periods
S1                    EQU 0x69                                ;
S2                    EQU 0x6A                                ;
S3                    EQU 0x6B                                ;
S4                    EQU 0x6C                                ;
S5                    EQU 0x6D                                ;
S6                    EQU 0x6E                                ;
S7                    EQU 0x6F                                ;

X1                    EQU   0x71                              ; Previous Samples
X2                    EQU 0x72                                ;
X3                    EQU   0x73                              ;
X4                    EQU 0x74                                ;
```

```
YL                    EQU   0x75                          ; Filter Output
YH                    EQU 0x76                            ;

ZL                    EQU 0x77                            ; Standard Deviation Estimate
ZM                    EQU 0x78                            ;
ZH                    EQU 0x79                            ;

PERIOD      EQU   0x7A                        ; Current Period
LOCKOUT               EQU   0x7B                          ; Lockout Timer
T                     EQU 0x7C                            ; Pointer to New Period
LCDA        EQU   0x7D                        ; Value Written to PORTA
LCDB        EQU   0x7E                        ; Value Written to PORTB
LCDC        EQU   0x7F                        ; Value Written to PORTC


;------------------------------------------------------------------------------
; Reset Vector
;------------------------------------------------------------------------------
RESET
      ORG    0x0000                    ; Reset Vector
      GOTO   initialize_         ;


;------------------------------------------------------------------------------
; Interrupt Vector
;------------------------------------------------------------------------------
ISR
      ORG    0x0004                    ; Interrupt Vector Location
      GOTO   initialize_         ;


;------------------------------------------------------------------------------
; Initialize
;
; Initializes Timer, Interrupts, ADC,
; Division Table, LCD Tables and Ports
;------------------------------------------------------------------------------
initialize_
      CLRF   STATUS                    ; Configure Bank 0
      MOVLW  T1CON_CONFIG         ; Timer1
      MOVWF  T1CON                     ;
      MOVLW  INTCON_CONFIG        ; Global Interrupts
      MOVWF  INTCON                    ;
      CLRF   PORTA                     ; Clear Port Values
      CLRF   PORTB                     ;
      CLRF   PORTC                     ;
      BSF            STATUS, 5                ; Configure Bank 1
      MOVLW  PIE1_CONFIG          ; Interrupts
      MOVWF  PIE1                      ;
      MOVLW  ADCON1_CONFIG        ; ADC
      MOVWF  ADCON1                    ;
      MOVLW  TRISA_CONFIG         ; Port Tri-State Buffers
      MOVWF  TRISA                     ;
      CLRF   TRISB                     ;
      MOVLW  TRISC_CONFIG         ;
      MOVWF  TRISC                     ;
      BSF            STATUS, 6                ; Configure Bank 3
      MOVLW  ANSELA_CONFIG        ; Port Analog Select
      MOVWF  ANSELA                    ;
      CLRF   ANSELB                    ;

      CLRF   STATUS                    ; Initialize Division Table
      MOVLW  0xE1                      ;
      MOVWF  (DIV_TABLE + 0x00)  ;
      MOVLW  0xDD                      ;
      MOVWF  (DIV_TABLE + 0x01)  ;
```

```
MOVLW  0xDA                          ;
MOVWF  (DIV_TABLE + 0x02) ;
MOVLW  0xD6                          ;
MOVWF  (DIV_TABLE + 0x03) ;
MOVLW  0xD3                          ;
MOVWF  (DIV_TABLE + 0x04) ;
MOVLW  0xD0                          ;
MOVWF  (DIV_TABLE + 0x05) ;
MOVLW  0xCD                          ;
MOVWF  (DIV_TABLE + 0x06) ;
MOVLW  0xCA                          ;
MOVWF  (DIV_TABLE + 0x07) ;
MOVLW  0xC8                          ;
MOVWF  (DIV_TABLE + 0x08) ;
MOVLW  0xC5                          ;
MOVWF  (DIV_TABLE + 0x09) ;
MOVLW  0xC2                          ;
MOVWF  (DIV_TABLE + 0x0A) ;
MOVLW  0xC0                          ;
MOVWF  (DIV_TABLE + 0x0B) ;
MOVLW  0xBD                          ;
MOVWF  (DIV_TABLE + 0x0C) ;
MOVLW  0xBB                          ;
MOVWF  (DIV_TABLE + 0x0D) ;
MOVLW  0xB8                          ;
MOVWF  (DIV_TABLE + 0x0E) ;
MOVLW  0xB6                          ;
MOVWF  (DIV_TABLE + 0x0F) ;
MOVLW  0xB4                          ;
MOVWF  (DIV_TABLE + 0x10) ;
MOVLW  0xB1                          ;
MOVWF  (DIV_TABLE + 0x11) ;
MOVLW  0xAF                          ;
MOVWF  (DIV_TABLE + 0x12) ;
MOVLW  0xAD                          ;
MOVWF  (DIV_TABLE + 0x13) ;
MOVLW  0xAB                          ;
MOVWF  (DIV_TABLE + 0x14) ;
MOVLW  0xA9                          ;
MOVWF  (DIV_TABLE + 0x15) ;
MOVLW  0xA7                          ;
MOVWF  (DIV_TABLE + 0x16) ;
MOVLW  0xA5                          ;
MOVWF  (DIV_TABLE + 0x17) ;
MOVLW  0xA3                          ;
MOVWF  (DIV_TABLE + 0x18) ;
MOVLW  0xA1                          ;
MOVWF  (DIV_TABLE + 0x19) ;
MOVLW  0xA0                          ;
MOVWF  (DIV_TABLE + 0x1A) ;
MOVLW  0x9E                          ;
MOVWF  (DIV_TABLE + 0x1B) ;
MOVLW  0x9C                          ;
MOVWF  (DIV_TABLE + 0x1C) ;
MOVLW  0x9A                          ;
MOVWF  (DIV_TABLE + 0x1D) ;
MOVLW  0x99                          ;
MOVWF  (DIV_TABLE + 0x1E) ;
MOVLW  0x97                          ;
MOVWF  (DIV_TABLE + 0x1F) ;
MOVLW  0x96                          ;
MOVWF  (DIV_TABLE + 0x20) ;
MOVLW  0x94                          ;
```

```
MOVWF   (DIV_TABLE + 0x21)   ;
MOVLW   0x92                         ;
MOVWF   (DIV_TABLE + 0x22)   ;
MOVLW   0x91                         ;
MOVWF   (DIV_TABLE + 0x23)   ;
MOVLW   0x90                         ;
MOVWF   (DIV_TABLE + 0x24)   ;
MOVLW   0x8E                         ;
MOVWF   (DIV_TABLE + 0x25)   ;
MOVLW   0x8D                         ;
MOVWF   (DIV_TABLE + 0x26)   ;
MOVLW   0x8B                         ;
MOVWF   (DIV_TABLE + 0x27)   ;
MOVLW   0x8A                         ;
MOVWF   (DIV_TABLE + 0x28)   ;
MOVLW   0x89                         ;
MOVWF   (DIV_TABLE + 0x29)   ;
MOVLW   0x87                         ;
MOVWF   (DIV_TABLE + 0x2A)   ;
MOVLW   0x86                         ;
MOVWF   (DIV_TABLE + 0x2B)   ;
MOVLW   0x85                         ;
MOVWF   (DIV_TABLE + 0x2C)   ;
MOVLW   0x84                         ;
MOVWF   (DIV_TABLE + 0x2D)   ;
MOVLW   0x82                         ;
MOVWF   (DIV_TABLE + 0x2E)   ;
MOVLW   0x81                         ;
MOVWF   (DIV_TABLE + 0x2F)   ;
MOVLW   0x80                         ;
MOVWF   (DIV_TABLE + 0x30)   ;
MOVLW   0x7F                         ;
MOVWF   (DIV_TABLE + 0x31)   ;
MOVLW   0x7E                         ;
MOVWF   (DIV_TABLE + 0x32)   ;
MOVLW   0x7D                         ;
MOVWF   (DIV_TABLE + 0x33)   ;
MOVLW   0x7C                         ;
MOVWF   (DIV_TABLE + 0x34)   ;
MOVLW   0x7B                         ;
MOVWF   (DIV_TABLE + 0x35)   ;
MOVLW   0x7A                         ;
MOVWF   (DIV_TABLE + 0x36)   ;
MOVLW   0x79                         ;
MOVWF   (DIV_TABLE + 0x37)   ;
MOVLW   0x78                         ;
MOVWF   (DIV_TABLE + 0x38)   ;
MOVLW   0x77                         ;
MOVWF   (DIV_TABLE + 0x39)   ;
MOVLW   0x76                         ;
MOVWF   (DIV_TABLE + 0x3A)   ;
MOVLW   0x75                         ;
MOVWF   (DIV_TABLE + 0x3B)   ;
MOVLW   0x74                         ;
MOVWF   (DIV_TABLE + 0x3C)   ;
MOVLW   0x73                         ;
MOVWF   (DIV_TABLE + 0x3D)   ;
MOVLW   0x72                         ;
MOVWF   (DIV_TABLE + 0x3E)   ;
MOVLW   0x71                         ;
MOVWF   (DIV_TABLE + 0x3F)   ;

BSF         STATUS, 5                    ; Initialize LCD Tables
```

```
        MOVLW  0x6F                        ;
        MOVWF  (LCD1_TABLE + 0)    ;
        MOVLW  0x03                        ;
        MOVWF  (LCD1_TABLE + 1)    ;
        MOVLW  0x76                        ;
        MOVWF  (LCD1_TABLE + 2)    ;
        MOVLW  0x57                        ;
        MOVWF  (LCD1_TABLE + 3)    ;
        MOVLW  0x1B                        ;
        MOVWF  (LCD1_TABLE + 4)    ;
        MOVLW  0x5D                        ;
        MOVWF  (LCD1_TABLE + 5)    ;
        MOVLW  0x7D                        ;
        MOVWF  (LCD1_TABLE + 6)    ;
        MOVLW  0x07                        ;
        MOVWF  (LCD1_TABLE + 7)    ;
        MOVLW  0x7F                        ;
        MOVWF  (LCD1_TABLE + 8)    ;
        MOVLW  0x5F                        ;
        MOVWF  (LCD1_TABLE + 9)    ;
MOVLW        0xFA                          ;
        MOVWF  (LCD2_TABLE + 0)    ;
        MOVLW  0x60                        ;
        MOVWF  (LCD2_TABLE + 1)    ;
        MOVLW  0xB6                        ;
        MOVWF  (LCD2_TABLE + 2)    ;
        MOVLW  0xF4                        ;
        MOVWF  (LCD2_TABLE + 3)    ;
        MOVLW  0x6C                        ;
        MOVWF  (LCD2_TABLE + 4)    ;
        MOVLW  0xDC                        ;
        MOVWF  (LCD2_TABLE + 5)    ;
        MOVLW  0xDE                        ;
        MOVWF  (LCD2_TABLE + 6)    ;
        MOVLW  0x70                        ;
        MOVWF  (LCD2_TABLE + 7)    ;
        MOVLW  0xFE                        ;
        MOVWF  (LCD2_TABLE + 8)    ;
        MOVLW  0xFC                        ;
        MOVWF  (LCD2_TABLE + 9)    ;
        CLRF   STATUS                      ;

        CLRF   LCDA                        ; Clear LCD
        CLRF   LCDB                        ;
        BSF          LCDB, 4                           ;
        CLRF   LCDC                        ;
        BSF          LCDC, 2                           ;

        MOVLW  0x40                        ; Clear Period List
        MOVWF  (T_MEM + 0)         ;
        MOVWF  (T_MEM + 1)         ;
        MOVWF  (T_MEM + 2)         ;
        MOVWF  (T_MEM + 3)         ;
        MOVWF  (T_MEM + 4)         ;
        MOVWF  (T_MEM + 5)         ;
        MOVWF  (T_MEM + 6)         ;
        MOVWF  (T_MEM + 7)         ;
        MOVWF  S0                          ; Clear Sorted List
        MOVWF  S1                          ;
        MOVWF  S2                          ;
        MOVWF  S3                          ;
        MOVWF  S4                          ;
        MOVWF  S5                          ;
```

```
        MOVWF  S6                                      ;
        MOVWF  S7                                      ;

        MOVLW  0x78                     ; Initialize Period
        MOVWF  PERIOD                   ;
        MOVLW  0x14                     ; Initialize Lockout
        MOVWF  LOCKOUT                           ;
        CLRF   T                                ; Initialize Period Pointer

        CLRF   ZH                               ; Initialize Standard
        MOVLW  0x78                     ; Deviation Estimate
        MOVWF  ZM                               ;
        CLRF   ZL                               ;

        MOVLW  0xFE                     ; Initialize Timer
        MOVWF  TMR1H                    ;
        MOVLW  0xEF                     ;
        MOVWF  TMR1L                    ;
        BSF          T1CON, 0                   ; Start Timer

;-------------------------------------------------------------------------------
; Drive LCD
;-------------------------------------------------------------------------------
driveLCD_
        MOVF   LCDA, 0                          ;
        MOVWF  PORTA                    ;
        MOVF   LCDB, 0                          ;
        MOVWF  PORTB                    ;
        MOVF   LCDC, 0                          ;
        MOVWF  PORTC                    ;
        COMF   LCDA, 1                          ;
        COMF   LCDB, 1                          ;
        COMF   LCDC, 1                          ;
        BCF          LCDA, 2                            ;

;-------------------------------------------------------------------------------
; Sample
; 60 Hz sampling rate
;-------------------------------------------------------------------------------
sample_
        SLEEP                                   ;
        BSF          ADCON0, 0                  ; Turn on ADC
        BCF          T1CON, 0                   ; Stop Timer1
        MOVLW  0xFE                     ; Reset Timer1
        MOVWF  TMR1H                    ;
        MOVLW  0xEF                     ;
        MOVWF  TMR1L                    ;
        BCF          PIR1, 0                            ; Clear Timer Interrupt
        BSF          T1CON, 0                   ; Start Timer1
        BSF          ADCON0, 1                  ; Start ADC
        SLEEP                                   ;
        BCF          ADCON0, 0                  ; Disable ADC
        BCF          PIR1, 6                            ; Clear ADC Interrupt

        BSF          PORTA, 2                   ; Sample

;-------------------------------------------------------------------------------
; Matched Whitening Filter
; FIR [-1, -3, 3, 8, -7]
;-------------------------------------------------------------------------------
        CLRF   YH                               ;
        MOVF   X4, 0                    ;
        SUBWF  X3, 0                    ;
```

```
        MOVWF   YL                                      ;
        BTFSS   STATUS, 0                       ;
        DECF    YH, 1                           ;
        BCF             STATUS, 0                       ;
        RLF             YL, 1                           ;
        RLF             YH, 1                           ;
        BCF             STATUS, 0                       ;
        RLF             YL, 1                           ;
        RLF             YH, 1                           ;
        MOVF    X2, 0                           ;
        ADDWF   YL, 1                           ;
        BTFSC   STATUS, 0                       ;
        INCF    YH, 1                           ;
        MOVF    X1, 0                           ;
        SUBWF   YL, 1                           ;
        BTFSS   STATUS, 0                       ;
        DECF    YH, 1                           ;
        BCF             STATUS, 0                       ;
        RLF             YL, 1                           ;
        RLF             YH, 1                           ;
        MOVF    X4, 0                           ;
        ADDWF   YL, 1                           ;
        BTFSC   STATUS, 0                       ;
        INCF    YH, 1                           ;
        MOVF    X3, 0                           ;
        MOVWF   X4                                      ;
        MOVF    X2, 0                           ;
        ADDWF   YL, 1                           ;
        BTFSC   STATUS, 0                       ;
        INCF    YH, 1                           ;
        MOVWF   X3                                      ;
        MOVF    X1, 0                           ;
        SUBWF   YL, 1                           ;
        BTFSS   STATUS, 0                       ;
        DECF    YH, 1                           ;
        MOVWF   X2                                      ;
        MOVF    ADRES, 0                        ;
        SUBWF   YL, 1                           ;
        BTFSS   STATUS, 0                       ;
        DECF    YH, 1                           ;
        MOVWF   X1                                      ;

;-------------------------------------------------------------------------------
; Standard Deviation Estimate
; Absolute Value
; IIR [255/256, 1]
;-------------------------------------------------------------------------------
        MOVF    ZM, 0                           ; Filter
        SUBWF   ZL, 1                           ;
        BTFSS   STATUS, 0                       ;
        DECF    ZM, 1                           ;
        MOVF    ZH, 0                           ;
        SUBWF   ZM, 1                           ;
        BTFSS   STATUS, 0                       ;
        DECF    ZH, 1                           ;

        MOVF    YL, 0                           ; Absolute Value
        BTFSC   YH, 7                           ;
        GOTO    abs1_                           ;
        ADDWF   ZL, 1                           ;
        CLRW                                            ;
        BTFSC   STATUS, 0                       ;
        MOVLW   0x01                            ;
```

```
        ADDWF  ZM, 1                        ;
        BTFSC  STATUS, 0                     ;
        INCF   ZH, 1                        ;
        MOVF   YH, 0                        ;
        ADDWF  ZM, 1                        ;
        BTFSC  STATUS, 0                     ;
        INCF   ZH, 1                        ;
        GOTO   abs2_                        ;
abs1_
        SUBWF  ZL, 1                        ;
        CLRW                                          ;
        BTFSC  STATUS, 0                     ;
        MOVLW  0x01                         ;
        ADDWF  ZM, 1                        ;
        BTFSC  STATUS, 0                     ;
        INCF   ZH, 1                        ;
        COMF   YH, 0                        ;
        ADDWF  ZM, 1                        ;
        BTFSC  STATUS, 0                     ;
        INCF   ZH, 1                        ;
abs2_


;-------------------------------------------------------------------------------
; Saturation
; Resets lockout when input is within 1/8 ADC FSC of power rails
;-------------------------------------------------------------------------------
        MOVF   ADRES, 0                     ;
        ADDLW  0x20                         ;
        ADDLW  0xC0                         ;
        MOVF   LOCKOUT, 0                   ;
        BTFSS  STATUS, 0                     ;
        MOVLW  0x1E                         ;
        MOVWF  LOCKOUT                              ;


;-------------------------------------------------------------------------------
; Detect
; Detects beat if 2 seconds have elapsed or if the lockout
; timer has expired and the input exceeds the threshold value
;-------------------------------------------------------------------------------
        BCF           PORTA, 2               ; Hold

        DECF   PERIOD, 1                ; Period
        BTFSC  STATUS, 2                ;
        GOTO   standby_                 ;

        DECFSZ LOCKOUT, 1               ; Lockout
        GOTO   driveLCD_               ;
        INCF   LOCKOUT, 1              ;

        RLF           ZL, 0                   ; Threshold
        RLF           ZM, 0                   ; 2 Standard Deviations
        SUBWF  YL, 1                    ;
        BTFSS  STATUS, 0                ;
        DECF   YH, 1                    ;
        RLF           ZM, 0                    ;
        RLF           ZH, 0                    ;
        SUBWF  YH, 1                    ;
        BTFSC  YH, 7                    ;
        GOTO   driveLCD_               ;


;-------------------------------------------------------------------------------
; Standby
; Checks for user each time a beat is detected
```

```
;-------------------------------------------------------------------------------
standby_
        MOVLW  ADCON0_CH3                      ; Configure ADC
        MOVWF  ADCON0                          ;
        BSF           ADCON0, 1                        ; Start ADC
        SLEEP                                           ;
        CLRF   ADCON0                          ; Disable ADC
        BCF           PIR1, 6                                   ; Clear ADC Interrupt
        MOVLW  0x20                            ; Check for User
        SUBWF  ADRES, 0                        ;
        BTFSS  STATUS, 0                       ;
        GOTO   updatePeriod_           ;
        CLRF   LCDA                            ; Clear LCD
        CLRF   LCDB                            ;
        BSF           LCDB, 4                                   ;
        CLRF   LCDC                            ;
        BSF           LCDC, 2                                   ;
        GOTO   driveLCD_                       ;


;-------------------------------------------------------------------------------
; Update Period
;-------------------------------------------------------------------------------
updatePeriod_
        INCF   T, 1                            ; Update T
        BTFSC  T, 3                            ;
        CLRF   T                                        ;
        MOVLW  T_MEM                           ; Update list
        ADDWF  T, 0                            ;
        MOVWF  FSR                                      ;


;-------------------------------------------------------------------------------
; Remove Old Period
;-------------------------------------------------------------------------------
search3_
        MOVF   INDF, 0                                  ;
        SUBWF  S3, 0                           ;
        BTFSS  STATUS, 0                       ;
        GOTO   search5_                        ;
search1_
        MOVF   INDF, 0                                  ;
        SUBWF  S1, 0                           ;
        BTFSS  STATUS, 0                       ;
        GOTO   search2_                        ;
search0_
        MOVF   INDF, 0                                  ;
        SUBWF  S0, 0                           ;
        BTFSC  STATUS, 0                       ;
        GOTO   shift0_                                  ;
        GOTO   shift1_                                  ;
search2_
        MOVF   INDF, 0                                  ;
        SUBWF  S2, 0                           ;
        BTFSC  STATUS, 0                       ;
        GOTO   shift2_                                  ;
        GOTO   shift3_                                  ;
search5_
        MOVF   INDF, 0                                  ;
        SUBWF  S5, 0                           ;
        BTFSS  STATUS, 0                       ;
        GOTO   search6_                        ;
search4_
        MOVF   INDF, 0                                  ;
        SUBWF  S4, 0                           ;
```

```
        BTFSC  STATUS, 0                     ;
        GOTO   shift4_                               ;
        GOTO   shift5_                               ;
search6_
        MOVF   INDF, 0                               ;
        SUBWF  S6, 0                         ;
        BTFSC  STATUS, 0                     ;
        GOTO   shift6_                               ;
        GOTO   shift7_                               ;
shift0_
        MOVF   S1, 0                         ;
        MOVWF  S0                                    ;
shift1_
        MOVF   S2, 0                         ;
        MOVWF  S1                                    ;
shift2_
        MOVF   S3, 0                         ;
        MOVWF  S2                                    ;
shift3_
        MOVF   S4, 0                         ;
        MOVWF  S3                                    ;
shift4_
        MOVF   S5, 0                         ;
        MOVWF  S4                                    ;
shift5_
        MOVF   S6, 0                         ;
        MOVWF  S5                                    ;
shift6_
        MOVF   S7, 0                         ;
        MOVWF  S6                                    ;
shift7_


;-----------------------------------------------------------------------------
; Insert New Period
;-----------------------------------------------------------------------------
        MOVF   PERIOD, 0                     ;
        SUBLW  0x78                          ;
        MOVWF  INDF                          ;
compare3_
        SUBWF  S3, 0                         ;
        BTFSS  STATUS, 0                     ;
        GOTO   compare5_                     ;
compare1_
        MOVF   INDF, 0                               ;
        SUBWF  S1, 0                         ;
        BTFSS  STATUS, 0                     ;
        GOTO   compare2_                     ;
compare0_
        MOVF   INDF, 0                               ;
        SUBWF  S0, 0                         ;
        BTFSC  STATUS, 0                     ;
        GOTO   insert0_                      ;
        GOTO   insert1_                      ;
compare2_
        MOVF   INDF, 0                               ;
        SUBWF  S2, 0                         ;
        BTFSC  STATUS, 0                     ;
        GOTO   insert2_                      ;
        GOTO   insert3_                      ;
compare5_
        MOVF   INDF, 0                               ;
        SUBWF  S5, 0                         ;
        BTFSS  STATUS, 0                     ;
```

```
        GOTO    compare6_                       ;
compare4_
        MOVF    INDF, 0                                 ;
        SUBWF   S4, 0                           ;
        BTFSC   STATUS, 0                       ;
        GOTO    insert4_                        ;
        GOTO    insert5_                        ;
compare6_
        MOVF    INDF, 0                                 ;
        SUBWF   S6, 0                           ;
        BTFSC   STATUS, 0                       ;
        GOTO    insert6_                        ;
        GOTO    insert7_                        ;
insert0_
        MOVF    S6, 0                           ;
        MOVWF   S7                                      ;
        MOVF    S5, 0                           ;
        MOVWF   S6                                      ;
        MOVF    S4, 0                           ;
        MOVWF   S5                                      ;
        MOVF    S3, 0                           ;
        MOVWF   S4                                      ;
        MOVF    S2, 0                           ;
        MOVWF   S3                                      ;
        MOVF    S1, 0                           ;
        MOVWF   S2                                      ;
        MOVF    S0, 0                           ;
        MOVWF   S1                                      ;
        MOVF    INDF, 0                                 ;
        MOVWF   S0                                      ;
        GOTO    sum_                            ;
insert1_
        MOVF    S6, 0                           ;
        MOVWF   S7                                      ;
        MOVF    S5, 0                           ;
        MOVWF   S6                                      ;
        MOVF    S4, 0                           ;
        MOVWF   S5                                      ;
        MOVF    S3, 0                           ;
        MOVWF   S4                                      ;
        MOVF    S2, 0                           ;
        MOVWF   S3                                      ;
        MOVF    S1, 0                           ;
        MOVWF   S2                                      ;
        MOVF    INDF, 0                                 ;
        MOVWF   S1                                      ;
        GOTO    sum_                            ;
insert2_
        MOVF    S6, 0                           ;
        MOVWF   S7                                      ;
        MOVF    S5, 0                           ;
        MOVWF   S6                                      ;
        MOVF    S4, 0                           ;
        MOVWF   S5                                      ;
        MOVF    S3, 0                           ;
        MOVWF   S4                                      ;
        MOVF    S2, 0                           ;
        MOVWF   S3                                      ;
        MOVF    INDF, 0                                 ;
        MOVWF   S2                                      ;
        GOTO    sum_                            ;
insert3_
        MOVF    S6, 0                           ;
```

```
        MOVWF  S7                              ;
        MOVF   S5, 0                    ;
        MOVWF  S6                              ;
        MOVF   S4, 0                    ;
        MOVWF  S5                              ;
        MOVF   S3, 0                    ;
        MOVWF  S4                              ;
        MOVF   INDF, 0                          ;
        MOVWF  S3                              ;
        GOTO   sum_                     ;
insert4_
        MOVF   S6, 0                    ;
        MOVWF  S7                              ;
        MOVF   S5, 0                    ;
        MOVWF  S6                              ;
        MOVF   S4, 0                    ;
        MOVWF  S5                              ;
        MOVF   INDF, 0                          ;
        MOVWF  S4                              ;
        GOTO   sum_                     ;
insert5_
        MOVF   S6, 0                    ;
        MOVWF  S7                              ;
        MOVF   S5, 0                    ;
        MOVWF  S6                              ;
        MOVF   INDF, 0                          ;
        MOVWF  S5                              ;
        GOTO   sum_                     ;
insert6_
        MOVF   S6, 0                    ;
        MOVWF  S7                              ;
        MOVF   INDF, 0                          ;
        MOVWF  S6                              ;
        GOTO   sum_                     ;
insert7_
        MOVF   INDF, 0                          ;
        MOVWF  S7                              ;


;------------------------------------------------------------------------------
; Sum Periods
;------------------------------------------------------------------------------
sum_
        MOVF   S2, 0                    ;
        ADDWF  S3, 0                    ;
        MOVWF  PERIOD                   ;
        MOVF   S4, 0                    ;
        ADDWF  S5, 0                    ;
        ADDWF  PERIOD, 1                ;


;------------------------------------------------------------------------------
; Divide
; Period must be between 64 and 511 (including carry)
;------------------------------------------------------------------------------
        CLRF   LOCKOUT                          ;
        BTFSC  STATUS, 0                 ;
        BSF           LOCKOUT, 0                 ;
        BTFSC  LOCKOUT, 0                 ;
        RRF           PERIOD, 1                  ;
        BTFSC  PERIOD, 7                 ;
        BSF           LOCKOUT, 1                 ;
        BTFSC  LOCKOUT, 1                 ;
        RRF           PERIOD, 1                  ;
        BCF           PERIOD, 7                  ;
```

```
        MOVF    PERIOD, 0               ;
        ADDLW   (DIV_TABLE - 0x40)  ;
        MOVWF   FSR                             ;
        MOVF    INDF, 0                         ;
        MOVWF   PERIOD                  ;
        BCF             STATUS, 0               ;
        BTFSC   LOCKOUT, 0              ;
        RRF             PERIOD, 1               ;
        BCF             STATUS, 0               ;
        BTFSC   LOCKOUT, 1              ;
        RRF             PERIOD, 1               ;
        MOVF    PERIOD, 0               ;


;-------------------------------------------------------------------------------
; Update LCD
; W must be between 0 and 199
;-------------------------------------------------------------------------------
        BSF             STATUS, 5               ;
        CLRF    LCDA                    ;
        CLRF    LCDB                    ;
        ADDLW   0x9C                    ;
        BTFSC   STATUS, 0               ;
        BSF             LCDA, 5                         ;
        BTFSS   LCDA, 5                         ;
        ADDLW   0x64                    ;
        ADDLW   0xB0                    ;
        BTFSC   STATUS, 0               ;
        BSF             LCDB, 3                         ;
        BTFSS   LCDB, 3                         ;
        ADDLW   0x50                    ;
        ADDLW   0xD8                    ;
        BTFSC   STATUS, 0               ;
        BSF             LCDB, 2                         ;
        BTFSS   LCDB, 2                         ;
        ADDLW   0x28                    ;
        ADDLW   0xEC                    ;
        BTFSC   STATUS, 0               ;
        BSF             LCDB, 1                         ;
        BTFSS   LCDB, 1                         ;
        ADDLW   0x14                    ;
        ADDLW   0xF6                    ;
        BTFSC   STATUS, 0               ;
        BSF             LCDB, 0                         ;
        BTFSS   LCDB, 0                         ;
        ADDLW   0x0A                    ;
        ADDLW   LCD2_TABLE              ;
        MOVWF   FSR                             ;
        MOVF    INDF, 0                         ;
        MOVWF   LCDC                    ;
        MOVF    LCDB, 0                         ;
        ADDLW   LCD1_TABLE              ;
        MOVWF   FSR                             ;
        MOVF    INDF, 0                         ;
        MOVWF   LCDB                    ;
        BTFSC   LCDC, 1                         ;
        BSF             LCDA, 6                         ;
        CLRF    STATUS                  ;


;-------------------------------------------------------------------------------
; Reset
;-------------------------------------------------------------------------------
        MOVLW   0x78                    ; Reset Period
        MOVWF   PERIOD                  ;
```

```
        MOVLW   0x14                        ; Reset Lockout
        MOVWF   LOCKOUT                             ;
        CLRF    PORTA                       ; Clear LCD
        CLRF    PORTB                               ;
        CLRF    PORTC                               ;
        GOTO    sample_                              ;

;------------------------------------------------------------------------
; End of Program
;------------------------------------------------------------------------
        NOP                                         ;
        END                                         ;
```