RF Switch Design

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Abstract

For this project, we created a simulation platform in order to optimize the silicon-on-insulator (SOI), field effect transistor (FET) switch technology. There are many alterations that could make these switches more efficient. However, such alterations are infrequently attempted due to the time-intensive nature of common circuit simulators. The goal was to create a faster way to test design ideas early in the design process. Our platform included a switch model, a transistor model, and a finite element analysis capacitance model.

1 Introduction

RF switches are commonplace in the mobile electronics industry, having the ability to create multiple possible signal paths. There are various technologies and topologies that can be employed to achieve the desired performance. Two standards in use today are electromechanical and solid state. RF switches provide easy and efficient flexibility for various signal paths [1]. Although there are a variety of technologies employed in RF switches, field effect transistor (FET) switches are more common in cellular applications.

1.1 RF Switch Purpose and Cellular Applications

RF switches are vital in alternating between various RF signal paths, an action required due to the wide variety of possible signal frequencies. Their function is not limited to mobile phones; they are also used in Bluetooth accessories, remote keyless entry systems, WLAN, and GPS navigation systems.

RF switches can be found in the front end signal chain, along with filters, amplifiers, matching networks, and mixers/local oscillators. The general structure of the RF receiver begins at the antenna. From there the signal usually enters a bandpass filter before passing through a low noise amplifier (LNA) and on through another filter. It then moves on to a mixer, with a local oscillator of variable frequency. This lowers the frequency to allow for easier demodulation into a binary signal. The switches are usually needed to select which filters are necessary, while still using common amplifiers, antennas and mixers, as shown in Figure 1.1.

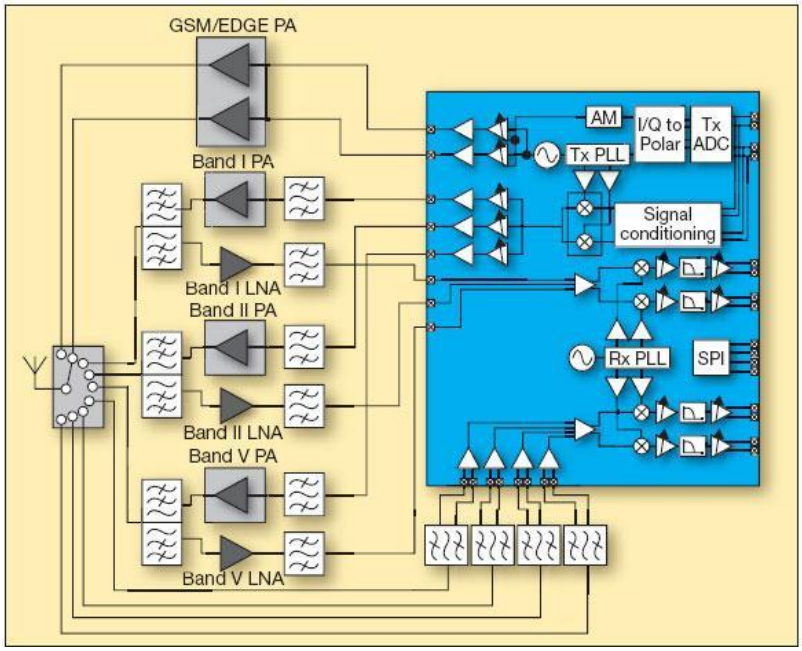


Figure 1.1. A typical cellular RF frontend showing a 9 throw switch from a common antenna. *Modern devices have multiple antennas permitting the use of multiple functions at once* **[2]**.

The transmitter signal path begins at the baseband (low frequency) circuitry. This low frequency signal contains the information to be transmitted. It is then mixed with a local oscillator in order to obtain the radio frequency signal. The RF signal generated by the mixer passes through a power amplifier and one or more filters before entering the antenna. Additionally, there is usually a matching network between the antenna and other circuitry for maximum power transfer. A receiver is essentially the transmitter signal path in reverse. Switches are used in order to create multiple transmitter/receiver signal paths without needing different antennas and amplifiers for each one.

Further complicating the circuitry in cellular applications is the wide variety of frequency bands used. Modern handsets like the one displayed in Figure 1.1 need to access several different cellular phone and data platforms as well as wireless LAN networks and global positioning satellites. Different frequencies and modulation/demodulation schemes are required in different locations and by different providers. Specific devices may only support a fraction of these frequency bands, but even this necessitates many different possible signal paths. In a typical cellular frontend, it is not uncommon to see switches with twelve to fourteen possible signal paths. It is important, therefore, that these switches are small, efficient, and fast.

1.2 Design Challenges in Mobile Systems

Mobile phones and other communications devices present several stringent design requirements including size, cost and efficiency. Devices such as cellular telephones must be efficient in order to extend battery lifespan and make them competitive in the rapidly growing cellular industry. The wide array of hardware that is now considered standard in cell phones demands extremely compact circuitry [3]

1.2.1 FET Breakdown Restrictions

To meet the specific needs of various cellular applications, MOSFETs are usually employed. Since RF voltages can be on the order of twenty volts, these FETs must be stacked, the drain of one being the source of the next. This ensures that the relatively high voltage is spread out among the transistors, reducing the voltage across each individual one, preventing breakdown. This is critical because the drain-to-source breakdown voltage of a single FET in the Skyworks process technology is on the order of 2 to 4 volts, significantly smaller than normal RF voltages.

This technology also creates another design problem. Due to the insulator between the drain and the ground plane, a drain-to-ground capacitance is always present. This capacitance array is shown in Figure 1.2. Because of the extra capacitance, the distribution of the voltage across the transistors is not even. The top transistor tends to have a significantly larger, drain-to-source voltage across its channel than the others. Unfortunately, if this voltage becomes large enough, the device could be sent into breakdown, potentially causing critical failure. Companies like Skyworks use different metallization schemes in order to add capacitance to the lower FETs in an effort to more evenly distribute the voltage. Our project produced a set of recommendations to ensure that each FET is optimized to have an even voltage.

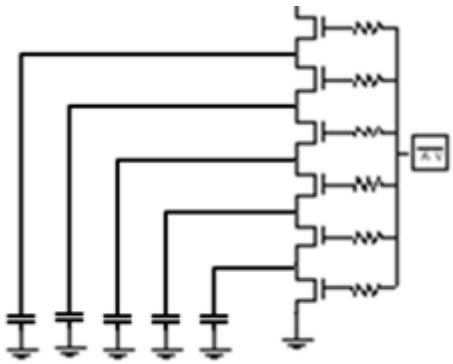


Figure 1.2. Shunt Stac. *Shows shunt stack of FETs, including the ground capacitance* **[4]**.

1.2.2 Time Limitation of Finite Element Analysis

Due to their significant complexities, full, three-dimensional, finite element analysis simulations of RF switches are quite time consuming. Typical numerical computations require mesh configurations in excess of one million elements. This presents a problem when attempting to improve switch performance, as simulation times for a single analysis could be on the order of hours, days, or weeks. Because of this limitation, full simulations are infrequently performed in industry. Instead, simpler models are used to yield reasonably accurate approximations in less time. This project created simpler models in an effort to reduce simulation runtime and thereby enabling rapid design and prototyping.

2 Background

There exists a wide variety of switch topologies. This project focuses on the optimization of FET switches due to their widespread use in cellular applications. In order to optimize switch performance, it is important to consider their characteristics and performance metrics. This chapter discusses critical switch terminology, topology considerations, and performance metrics.

2.1 FET-based RF switch designs

There exist three major FET switch topologies: series, shunt, and combinational. Combinational switches are common in cellular applications, as they tend to be less lossy than the alternatives. In Figure 2.1, a combinational switch is shown. When a control voltage is held high, the series FET for its corresponding port allows signals to pass through it and the shunt FET for the alternative port directs signals to ground. When held low, the series FET of the port prevents anything from passing through it, as does the shunt FET for the opposite port [5].

In Figure 2.1, only four FETs are shown. For many commercial switches, however, each of these FETs would represent a stack of at least twelve devices in series. Stacking the devices in this manner is often necessary since each individual FET has a relatively low breakdown voltage, as previously discussed. By stacking the FETs, the relatively high voltage typically used in most RF frontends is dispersed over several devices, so that the voltage across any one device is relatively small and unlikely to result in breakdown. Ideally, all the FETs in the stack should have identical drain-to-source voltages.

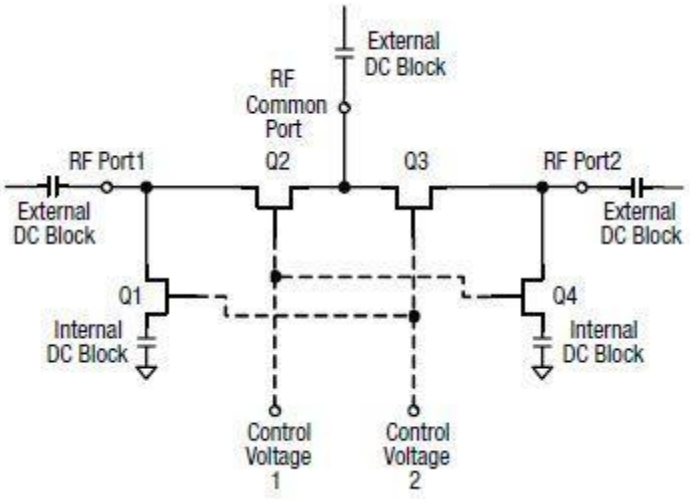
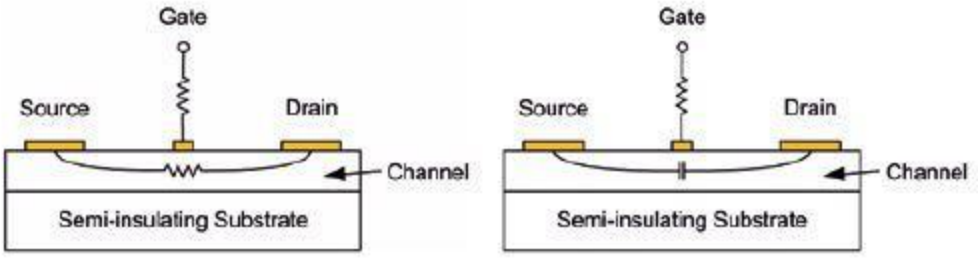


Figure 2.1. Combination Series-Shunt FET Switch. *When a control voltage is held high, it enables the series FET for one port and the shunt FET for another. When it is held low, it disables both of these FETs. The series FETs pass signals when they are enabled and block signals when disabled. The shunt FETs do the opposite. When enabled, they block the signal by sending it to ground. When disabled, they prevent the signal from going to ground, effectively passing it. The control voltages must be set at opposite levels for the switch to work. When control voltage 1 is enabled, it causes the series FET at port 1 to pass signals and the shunt FET at port 2 to block the signals to ground. If control voltage 2 is disabled while this occurs, it disables the shunt FET for port 1 and the series FET for port 2, passing signals for port 1 and blocking for port 2* **[5]**.

FETs are three terminal devices and are typically fabricated with either silicon or gallium arsenide. The basic function of a FET is shown in Figure 2.2. When the gate is biased positively against the source, a channel forms under the gate terminal, decreasing the resistance of the device and allowing current to pass through when a drain-to-source voltage is applied (Figure 2.2(a)). If, however, the gate voltage is equal to or below that of the source, a channel will not form, resistance will remain relatively high, and current will not flow through the device (Figure 2.2(b)).



(a) *(b)*

Figure 2.2. Basic functionality of FET device. *(a) When the gate voltage is high, a FET behaves like a resistor. (b) When the gate voltage is low, a FET behaves like a capacitor* **[6]**.

2.1.1 Switch metrics and Benefits of FET Technology

As summarized in Table 2.1, each switch technology has its advantages and disadvantages. This section will attempt to justify the choice of FET technology over PIN diode and MEMS. FET switches in the shunt-series configuration are used in cellular technology not only for their performance merits, but also for their manufacturability and low cost. Table 2.1 outlines key performance metrics for the different switch topologies.

Table 2.1. Comparison of different designs. *Figures of merit which are important in cellular devices include insertion loss, isolation and DC power. FET switches are widely used because of their superior performance* **[6]**.

	Solid state switches			Electromechanical switches
	Pin diode	FET	Hybrid	
Frequency range	from MHz	from DC	from kHz	from DC
Insertion loss	Medium (Roll off at low frequencies)	High (Roll off at high frequencies)	High (Roll off at high frequencies)	Low
Isolation	Good at high frequencies	Good at low frequencies	Good at high frequencies	Good across broad frequency range
Repeatability	Excellent	Excellent	Excellent	Good
Switching speed	Fast	Average	Average	Slow
Power handling	Low	Low	Low	High
Operating life	High	High	High	Medium
Power consumption	High	Low	Moderate	Current interrupt feature reduces current consumption
Sensitive to	RF power overstress, temperature	RF power overstress, temperature	RF power overstress, temperature	Vibration

Although PIN diodes can offer better insertion losses at high frequencies, they require a constant operating current which would quickly drain the battery on cellular devices. Electromechanical/MEMS switches suffer from a similar problem. Additionally, the current MEMS technology is limited in durability, being subject to mechanical deterioration.

In general, RF devices are characterized by their "S-Parameters" a set of voltage wave ratios which characterize the transmission through a path or reflection from a port of the device. For RF switches, there

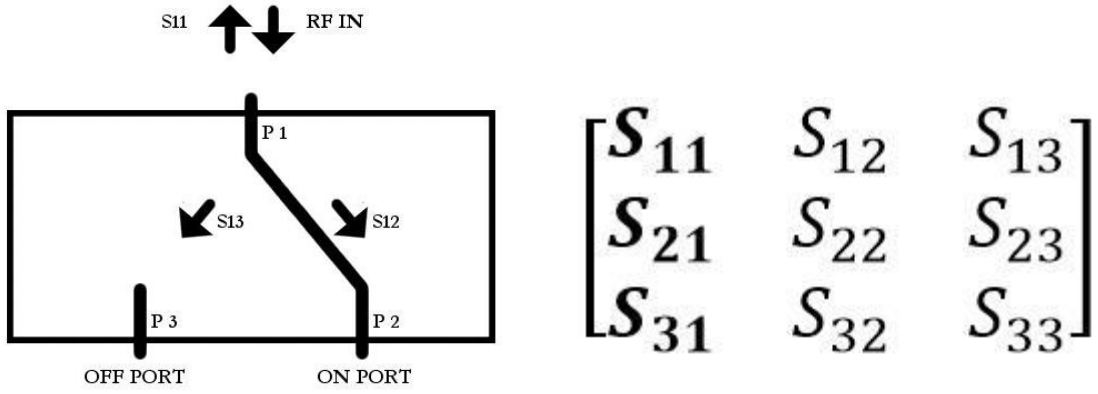
are three S-parameters of significant importance to this project: S11, S21, and S31. These are also known as the reflection coefficient, insertion loss, and isolation, respectively.

S11 is the input reflection coefficient, or the voltage ratio of the reflected wave on the input port to the original incident wave. It can be used to determine the input voltage standing wave ratio (VSWR) and the return loss. The return loss represents power loss from impedance mismatches. The VSWR also measures mismatch. A low (preferably zero) reflection coefficient is desired so that all of the power is transmitted through the switch [7]. All of the aforementioned technologies can be tuned for a low return loss.

S21 represents the forward voltage gain or, as in the case of most switches and other passive devices, loss. The insertion loss can be determined from this parameter. A low insertion loss between the source and an active (on) arm is desirable to increase switch efficiency.

Another important switch parameter is the isolation of the switch. Assuming a three-port network where port 2 is on and port 3 is off, this is the transmission coefficient (S31) from the source to an off arm. It is usually displayed in dB below the input signal (a negative value). It is an important parameter because it determines how much power is wasted due to "leakage" through the off arms. These parameters, S11, S21, and S13 are demonstrated in Figure 2.3(a). FET devices tend to have better isolation at low frequencies [5].

For a device with an arbitrary number of ports, n, there exist n^2 S-parameters, one for each possible signal path through the device. S11, S21, and S31 are the only ones discussed because they are of the most importance to RF switch behavior. The full S parameter matrix for a 3 port system can be seen in Figure 2.3(b).



(a) (b)

Figure 2.3. S-Parameters in a single pole dual throw switch. *(a)Diagram of relevant S-parameters in a single pole dual throw switch. The input RF power is the power from the source fed into port 1. S11 is the wave reflected back towards the generator. S21 is the wave transmitted through to the on port, port 2 in this case. S31 is the wave unintentionally leaked through to the off switch arm. (b) A 3 port S parameter matrix illustrates all of the possible voltage gains from port to port. Important switch parameters are in bold. S11, the reflection coefficient, S21, the insertion loss, and S31 the isolation to the third port are all also demonstrated in the left diagram.*

There are other parameters applicable to RF switches which are also important. Maximum absolute power is one of these parameters. It is measured in dBm, where 0 dBm is equivalent to 1mW of RF power. This is simply the maximum power that the device can bear without degrading.

The third order intercept point (IP3) is a measure of the linearity of a device. It measures a phenomenon known as intermodulation distortion. Intermodulation distortion is a result of the non-linearities in devices. The third order intercept point is the level at which a third order signal would equal the input level if two input signals of different frequencies were input [4].

Other important switch metrics include the DC current required to switch between ports, the speed at which they can be switched and manufacturability. The switching speed can affect the data rate and a high DC current is inefficient. These characteristics, along with manufacturability are very important to the cellular industry. Since FET's are voltage controlled devices, they require no quiescent current, making them very desirable in terms of efficiency.

2.1.2 Many-throw Topologies and Switch Nomenclature

Switches are categorized by their numbers of poles, or common ports, and throws, or switchable ports. For instance a single pole double throw (SPDT) switch is capable of sending a signal to port 1 (the pole) from two other ports (throws 2 and 3). Switches consisting of many poles and throws are often employed in more complicated frontends. The downside to multi-throwed switches is that loss will increase due to signal leakage through the off throws. This loss is small though, in comparison to the benefits in size and complexity attained by using multi-throwed switches [4].This project focuses on simulating a single-pole, twelve-throw (SP12T) switch, a common configuration found in mobile technologies. The models used, however, may be applied to a switch of any configuration.

2.2 FET Switch Construction

As this project involves the optimization of physical characteristics, it is important to discuss how the transistors are constructed. This section covers some techniques used in silicon-on-insulator technology, a technology employed to prevent substrate current, a common cause of significant losses [4].

2.2.1 Physical Layout and Equivalent Circuit

Since the transistors in RF switches are expected to sustain a sizable amount of current, they are distributed over the area of the wafer in a multi-fingered layout (Figure 2.4). Each finger is connected to either the source or the drain, the specific terminal being determined on an alternating basis. Essentially, such a transistor is a set of many smaller transistors in parallel. This results in an effective transistor width that is much greater than its length.

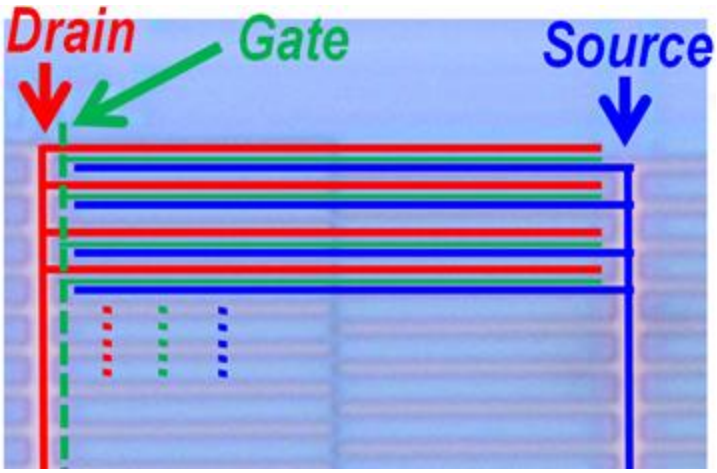


Figure 2.4. Top down perspective of a multi-fingered RF transistor. [4].

The vertical perspective of the FET must also be considered. Figure 2.5 shows a vertical cutaway of the FET between two fingers. The drain and source are connected to metal layers by conducting rods, known as vias. These are typically made out of tungsten, while the metal layers are made of copper or other high conductivity metals. A three-dimensional representation is shown in Figure 2.6.

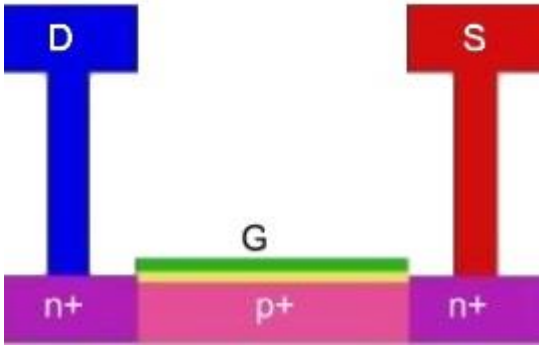


Figure 2.5. Cutaway of transistor.

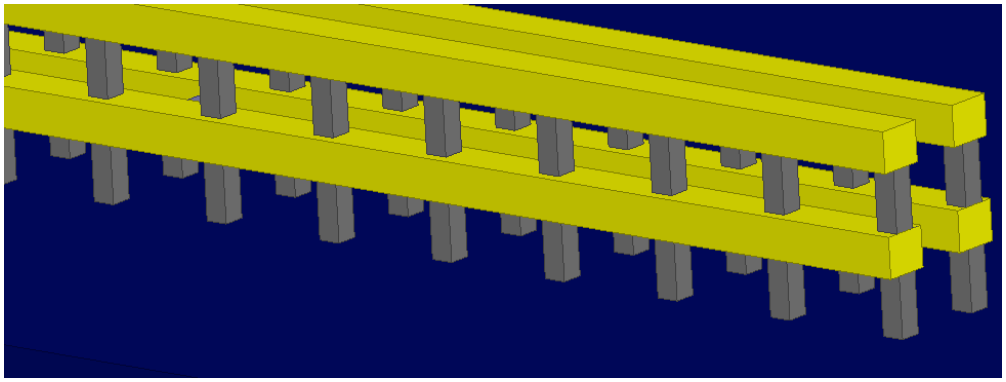


Figure 2.6. One drain and one source in three dimensions. *The vias (gray) are the vertical rods that run from the silicon base to the conductors (yellow). This image only shows one source and one drain in order to better show the via conductor layout. The spacing between the drain and source is about 1 um. The height of this double stack stands at about 1.5 um.*

For higher level simulation and optimization, a circuit model has to be constructed. This circuit can vary in complexity. The model used in this project was significantly idealized (Figure 2.7). Individual transistors were simulated as either capacitors or resistors. These represented the states of not conducting (off) and conducting (on), respectively. The substrate capacitance was also included. A complicated circuit model could have included the parasitic inductances of the source and drain, but this was deemed too complex for the simple, time-efficient goal of this project.

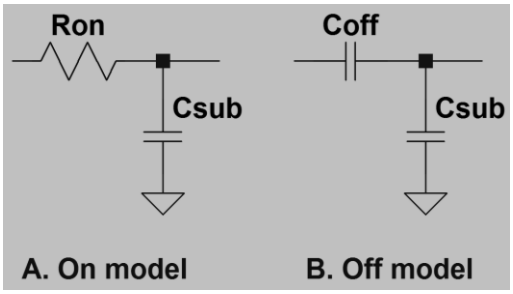


Figure 2.7. The circuit model used in this project's higher level simulations. *Typical values for the on resistance may be in the tenths of an ohm. The off capacitance can range from about 200 to 600 femto farads. The substrate capacitance is much less (but still not negligible) in the range of 1-5 femto farads.*

2.2.2 Silicon-On-Insulator Technology and Substrate Capacitance

Silicon-On-Insulator (SOI) is a technology that involves the placement of an insulation layer underneath the FET channel, limiting the space of the channel (Figure 2.8) [4].This insulator is placed below the channel in order to limit any current flow around the depletion region when the transistor is off. The

insulator restricts the current to the space directly between the drain and source wells. This allows for an extremely high off-resistance when compared to regular FET technology. This increases isolation, reducing overall loss.

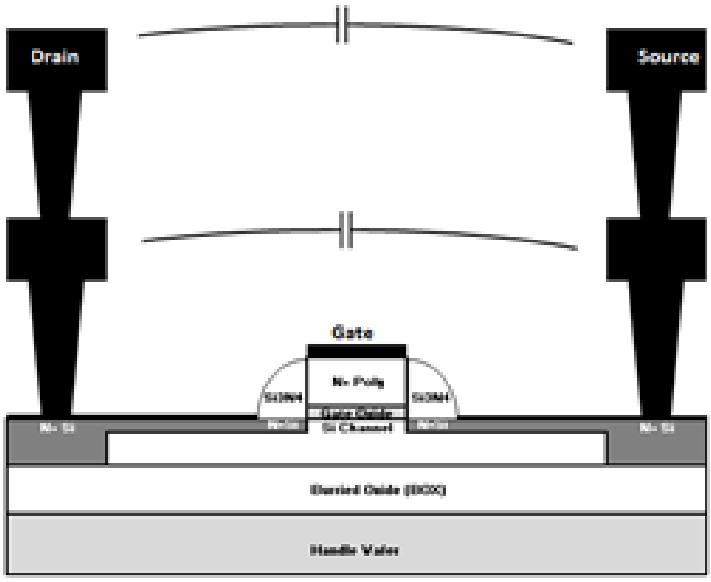


Figure 2.8. Cutaway of SOI transistor. *Also shown are the drain source capacitances between the metal conductors. They may be adjusted by varying the number and configuration of these conductors. The insulator made from silicon dioxide separates the channel from the main wafer* **[4]**.

Silicon-on-insulator technology has many advantages. However, it is still subject to substrate capacitance between the drain/source wells and the ground plane. This capacitance can be limited by increasing the thickness of the insulator. Unfortunately, this would also increase the voltage required to create the depletion region. Instead, designers strive to accommodate for ground capacitance by varying the drain-to-source capacitances so as to evenly distribute the drain-to-source voltages. The optimization of this method is one of the primary purposes of this project.

2.3 Potential tools to decrease simulation time

This project focuses primarily on simulation as the goal is ultimately to decrease simulation time and therefore enable the rapid testing of novel circuit design ideas. Three programs were used to create these rapid simulations: ADS, Excel, and HFSS.

2.3.1 Advanced Design System (ADS) for high level Optimization

Advanced Design System, or ADS, uses SPICE based circuit simulation and behavioral models to simulate a wide variety of circuits, from simple designs to complex RF systems. It is widely used in the industry, particularly for RF applications. This program was used to create and optimize the full switch model. One aspect of this program that was particularly useful to this project was the optimization functionality [8].

2.3.2 Microsoft Excel for nodal analysis with circular dependencies

In order to model the on-resistance of a single FET, Excel was utilized. Excel has many benefits, in particular its ability to evaluate circular dependencies iteratively. It is also widely available, significantly less expensive than many alternatives, and has options for the creation of an intuitive user interface.

2.3.3 Ansoft High Frequency Structure Simulator (HFSS) based equations

The drain-to-source capacitance of a single FET presented another challenge. Due to the complex geometries involved in each FET, it became clear that finite element analysis software would be necessary. For this purpose, Ansoft's HFSS and Maxwell were chosen. These are industry standards for high frequency and low frequency finite element analysis, respectively. Since the goal of this project was to create simpler, faster analysis tools, it was desired to avoid using these computationally intensive numerical software packages. Thus, new, faster analytical models and equations were created for this project, with their results being compared to the more complex software.

3 Project Purpose/Goals

The goal of this project was to create a simulation platform in order to optimize the SOI FET switch technology developed and used by the sponsor Skyworks, Inc. These switches can be altered in multiple ways such as changing transistor size and modifying the metal layer geometry in order to make the design more efficient. There were obstacles, however, to this improvement. This project focused specifically on simulation time. Due to the complexity of RF systems, simulations have become incredibly time-intensive. Unfortunately, this can discourage attempts at switch optimization. If a new design does not perform well, a significant amount of time may have been wasted. This means that it is sometimes more appealing to stick with an inefficient design then to attempt a new one and risk losing several hours (or days) of potential work time. This project created an optimization tool that is faster than the current simulation techniques. It was, out of necessity, significantly less complex, therefore limiting its application. The intent of this project was to create a fast and simple way for the design engineers at Skyworks to test their ideas before implementing them in their designs and using the more time-consuming simulations.

4 Approach

In order to achieve the desired degree of accuracy and flexibility for this project, the switch design was modeled on both the circuit level and the physical level. The circuit level model that was created simulates the entire switch while the physical level model simulates a single transistor. The purpose of the dual model method is to allow for inclusion of both the overall design of the switch, as well the geometric attributes of each transistor.

4.1 Using ADS to create a full switch model

Keysight's Advanced Design System (ADS) was used to construct a model of a full switch array. This model was us deployed to predict the linear characteristics of switch performance and to optimize for equal voltage distribution across each transistor. The individual transistors were modeled as resistances and capacitances, both with a substrate capacitance to ground, as shown previously. The optimization for a voltage distribution was done using the built-in optimizer. The effect of this optimization on the insertion and return loss of the overall switch could then be tested. There are three major components to the ADS model: the optimizer, S-parameter tester, and sensitivity analysis.

4.1.1 Using lumped-component circuit approximation

The circuit-level simulation used a simple resistor-capacitor approximation for each transistor. There already exist many behavioral and SPICE based models which could provide more accurate results but would require much longer simulation times due to their complexity. These models are based upon lookup tables or complex equations, and are useful for many large-signal applications, such as determining transistor biasing points. For this project, the main concern was small-signal performance so a linear approximation was employed. A relatively simple linear model was used because of the inherent linearity of the SOI technology, as shown in Figure 4.1. This simplification allows us to use the simple RC model for a FET.

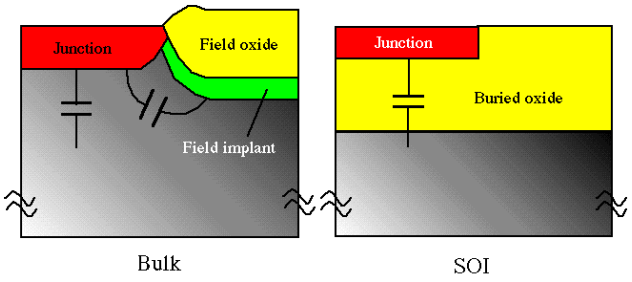


Figure 4.1. Lack of parasitic capacitances in SOI. *This cross-section illustrates the lack of parasitic capacitances between junction and field implant as well as reduction of parasitic capacitance into bulk. The lack of these parasitics allows for the easy simplification of the model to that shown in Figure 2.7* **[9]**.

Each arm of a switch was modeled as two stacks, series and shunt, of twelve FETs (Figure 4.2). An enabled FET was modeled by its on resistance along with its substrate capacitance. A disabled FET was modeled using its off capacitance and the same substrate capacitance.

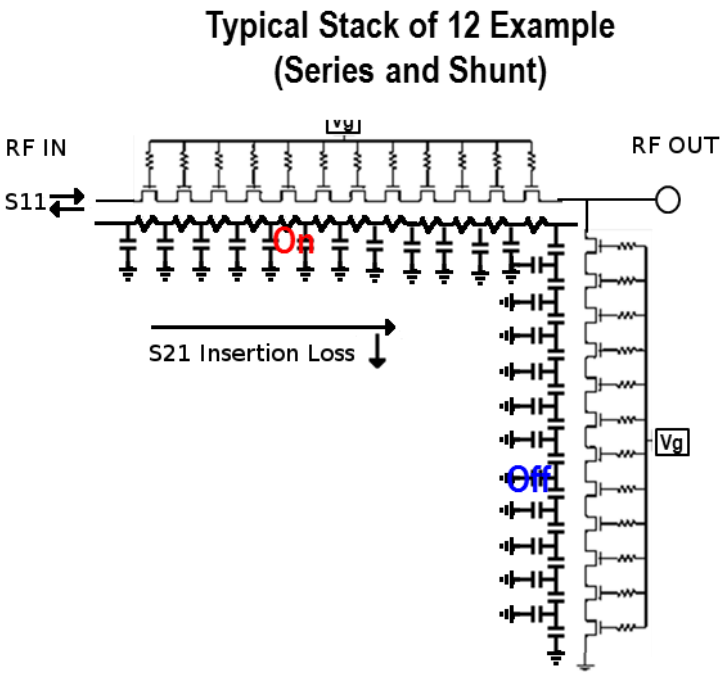


Figure 4.2. Switch arm juxtaposed with its representative model circuit. *This arm is active. The series transistors are modeled by resistances and substrate capacitances. The shunt transistors are modeled by capacitances and substrate capacitances* **[4]**.

4.1.2 Using the optimizer for capacitance optimization

The voltage optimizer was the first component of the circuit-level simulation. This optimizer was intended to find values of capacitance in such a way as to evenly distribute the voltage across all of the transistors. This is the most important part of the ADS simulation. If the voltage is not distributed evenly, the voltage across the first transistor could rise high enough to induce breakdown, causing catastrophic failure in the device. The optimizer uses AC analysis to find voltages at each FET. It simulates a single arm of the switch and optimizes the capacitance values such that there is an even voltage distribution across the transistor stack. The optimizer accepts the series resistance, substrate capacitances, and the range of capacitance that is possible. This optimizer is set up for a single active arm of the switch. In order to optimize for an inactive arm, the values for resistances and capacitances can simply be switched. Figure 4.3 shows the setup for this simulation and optimization.

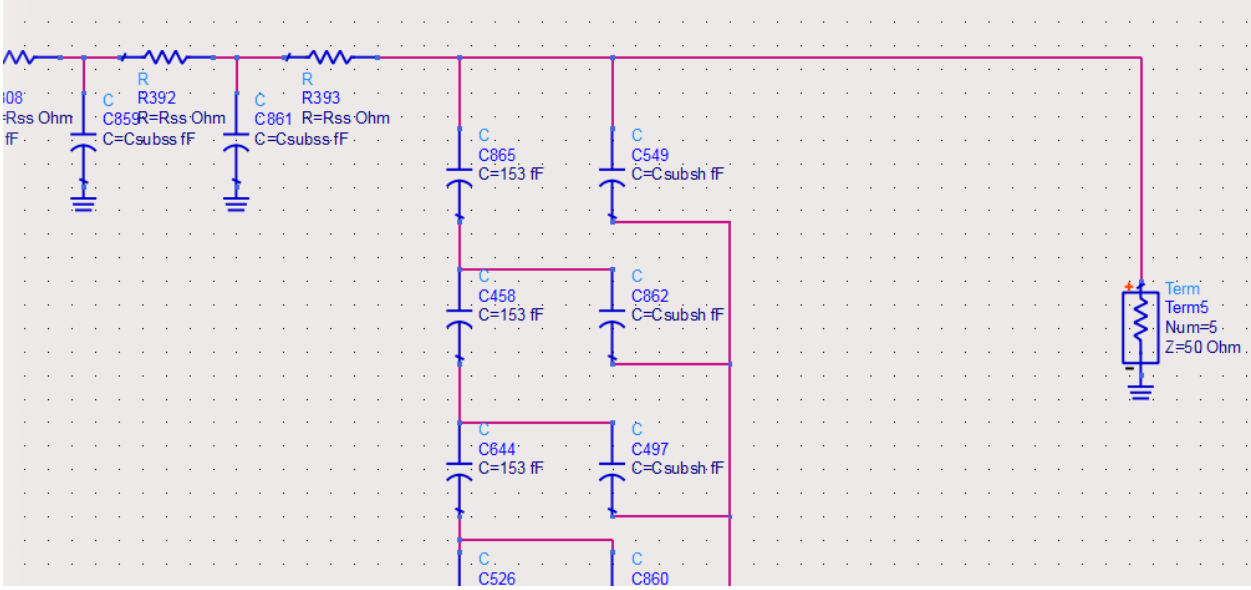


Figure 4.3. ADS simulation model of an on arm (close up view). *The resistors at the top represent the on resistance of the series FETs and the capacitors at bottom represent the off shunt FETs. The capacitors to ground in both cases are the substrate capacitances of each FET. These are assumed to be uniform. The resistor at right represents the transmission line load. The capacitors/resistors continue on to represent all twelve FETs in this model.*

The AC analysis tool ensures only that the transistors are at the same voltage. It does not simulate or attempt to minimize RF losses. This is accomplished in later simulations involving the S-parameters and the RC constant optimizer. Figure 4.4 shows the inputs of the optimizer and a full arm.

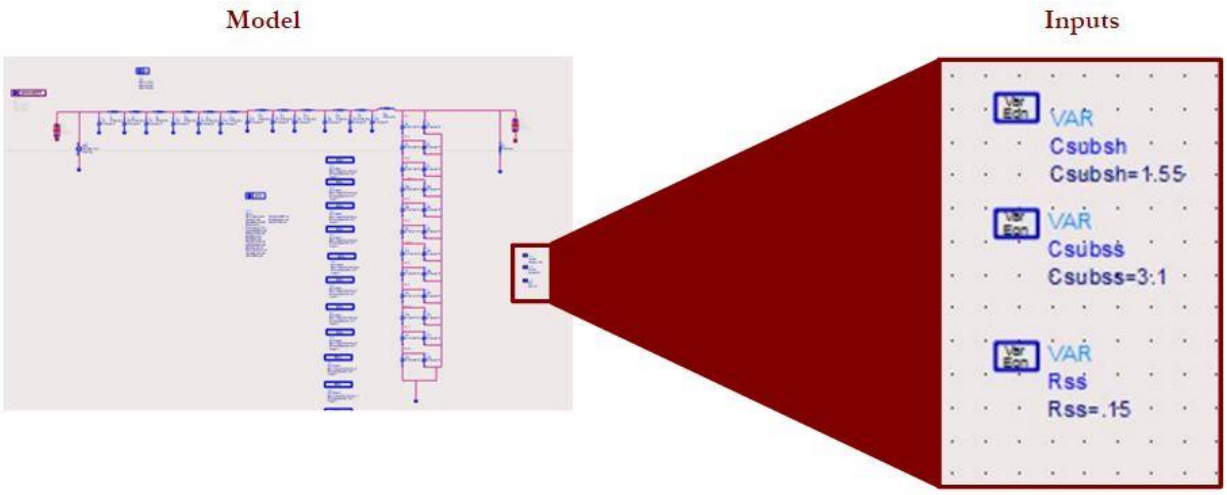


Figure 4.4. Full active arm of a switch used in the capacitance optimization simulation. *At left the full arm can be seen. The inset displays common inputs which are stowed as variables in ADS. Other inputs which are not common among all FETs must be adjusted manually for each one.*

4.1.3 Modeling switch metrics

The S-parameter test schematic is designed to test the return loss, insertion loss, and isolation of a sample 12 pole switch. This is accomplished using the capacitance and resistance values from the previous optimizer. The S-parameters are tested with the original values and post-optimization values.

The S-parameter simulation output graphs the insertion loss, return loss, and isolation before and after optimization. The two traces are plotted on the same axes so that the difference may be clearly seen. Thus, the designer may make an optimization and then clearly see the resulting changes in the RF metrics. If the losses are higher than desired, the designer can return to the optimizer, re-optimize for different conditions, and simulate again. This can be repeated until acceptable results are obtained.

An additional component to the ADS simulation is the sensitivity analysis tool. This tool allows the user to view the sensitivity of the S-parameters to variation in the resistances and capacitances of every component. It obtains a result by simulating a system then changing some value by a very small amount. It then re-simulates the system to obtain a new result. The difference between outputs is then divided by the difference in the input. This value is known as the sensitivity of this result to the input value. For instance, if the sensitivity of the insertion loss to a change in one of the on resistances is measured, the result would be in

units of dB/Ohm. This value is usually normalized for ease of use. With this tool, the user can see which values could be changed without significantly decreasing performance.

4.1.4 Optimizing RF Performance utilizing Constant Ron-Coff Model

Additionally, a constant Ron-Coff optimizer was created. True to its name, this assumed that each transistor had a constant value for the product of the on resistance and off capacitance (Ron-Coff constant). This is a common figure of merit for a switch design process because, assuming drain-to-source pitch and via pitch are equal, adding further stacked conductors both increases capacitance and decreases resistance proportionately, leaving their Ron-Coff constant unchanged.

This tool allows the circuit designer to find an RC constant for a particular configuration and then use that to obtain reasonable values for the capacitances of all transistors in the switch. This also allows the optimizer to find values that results in an even voltage distribution without compromising RF performance.

4.2 Using Excel to create a transistor resistance calculator

The Excel model was created to allow for the time-efficient exploration of the effect of the physical dimensions and parameters of a RF transistor on its total resistance. This is done by performing a complex nodal analysis, relying on Excel's ability to evaluate circular dependencies to do so. The user primarily interfaces with the program through a form, designed to facilitate the experience.

4.2.1 The three-dimensional transistor equivalent circuit

This program seeks to model the multi-finger, multi-via, multi-layer RF transistor, shown in Figure 4.5(a). For the purposes of this project, a three-dimensional equivalent circuit was developed; it is shown in Figure 4.5(b).

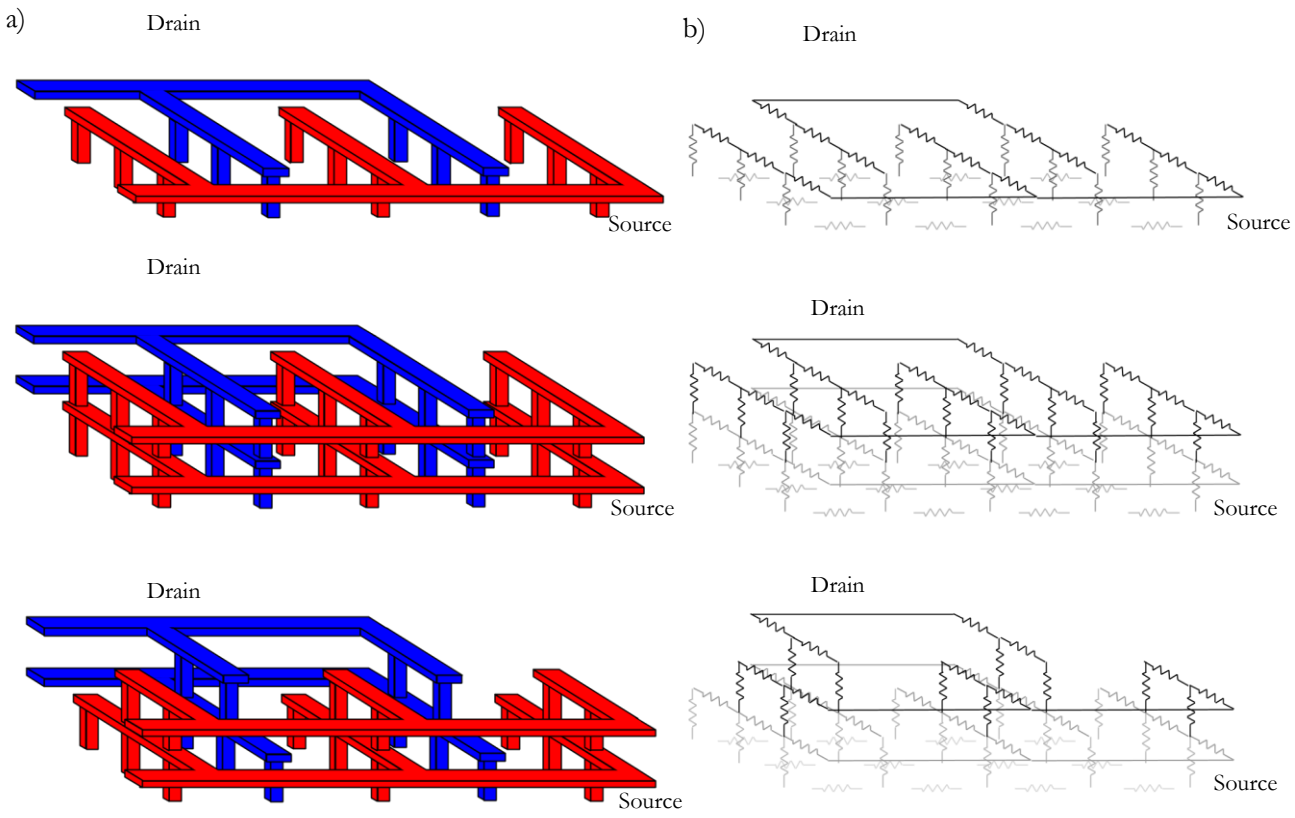


Figure 4.5. Transistor layout and circuit. *(a) Physical layouts of multi-finger, multi-via transistor. The first structure consists of a transistor with only one metal layer. The second consists of a transistor with two metal layers of the same size. The third represents a transistor with two metal layers of different sizes. (b) Lumped-component equivalent circuit corresponding to each physical layout in (a).*

4.2.2 Using Excel's circular dependency evaluation to perform nodal analysis

Nodal analysis is performed by approaching a circuit as a system of nodes. The main premise is that the current flowing into a node has to be equal to the current flowing out of that same node. The nodal method is both simple and versatile. However, in this case, it creates circular dependencies. These occur when one variable depends on the value of another variable which in turn depends on the initial variable. This relationship can be direct, as seen in Figure 4.6(a), or indirect, as depicted in (Figure 4.6(b)).

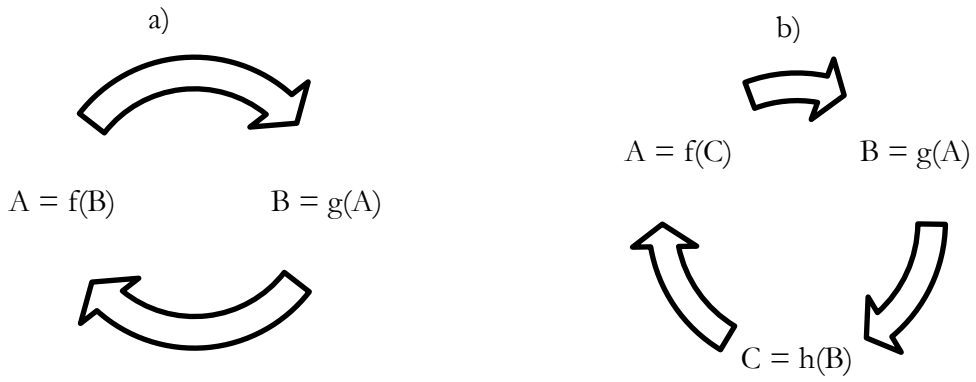


Figure 4.6. Circular Dependencies. *a) Shows a direct circular relationship. b) Shows an indirect circular relationship.*

For a time-efficient approach, this means that some form of numerical method must be used, making the results inherently an approximation. Having options for the iterative evaluation of circular dependencies, Excel is an ideal program for the implementation of this model. These options are variable and can be used to increase or decrease both accuracy and runtime of the program.

The circular dependency evaluation options in Excel include enabling/disabling the evaluation, setting the maximum number of iterations allowed in an evaluation, and setting the maximum difference between the previous value and the current value allowed before an evaluation can stop. This allows one to adjust the speed and accuracy of the resistance calculation. Specifically, decreasing the maximum difference will increase accuracy but reduce speed, while increasing it will do the opposite. The number of iterations has the opposite relationship with accuracy and speed. However, it was found to have less of an impact than the maximum difference.

Once the submit button is pressed on the form, the program begins by clearing all cells. The physical parameters are then transformed into the via number and the lumped resistance values for the equivalent circuit. The program then iterates through each layer of the device. For each layer, the program then iterates through each node. The number of nodes for a layer is equivalent to its number of vias.

While on the transistor layer, the via number is equal to that of the first metal layer. For each node, the relative locations of any nodes that are directly connected to it through a single, lumped resistance are determined. This is incorporated into the voltage equation for that node. The full voltage formula for these

nodes also includes a connection through a via resistance to the first metal layer as well as connections to other nodes in the transistor layer.

For metal layers, several string variables are assigned values specific to that node during its iteration. These variables are eventually strung together to form the cell formula that defines the relationship of the voltage of that node with the rest of the nodes in the circuit. This system is designed around a standard equation. This equation includes all of the different potential nodal relationships that could show up in the equation for any single node. Each relationship is then multiplied by either 1 or 0, depending on whether it is valid for the node under consideration. *Equation* ***4.1*** is the general equation.

$$voltage\ of\ node = \frac{a}{b} \qquad \textit{Equation 4.1}$$

The variables a and b are given in *Equation* ***4.2*** and *Equation* ***4.3***, respectively. The variables c through g have a value of either 0 or 1.

$$\begin{aligned} a = {} & (voltage\ of\ next\ node\ of\ layer) * \frac{c}{Rx\ of\ layer} \\ & + (voltage\ of\ node\ directly\ below\ in\ previous\ layer) * \frac{1}{Rv\ of\ layer} \\ & + (voltage\ of\ previous\ node\ of\ \ layer) * \frac{d}{Rx\ of\ layer} \\ & + (voltage\ of\ node\ directly\ above\ in\ next\ layer) * \frac{e}{Rv\ of\ next\ layer} \\ & + Vss * \frac{f}{Rm\ of\ layer} \\ & + Vcc * \frac{g}{Rm\ of\ layer} \end{aligned} \qquad \textit{Equation 4.2}$$

$$\begin{aligned} b = {} & \frac{c}{Rx\ of\ layer} + \frac{1}{Rv\ of\ layer} + \frac{d}{Rx\ of\ layer} \\ & + \frac{e}{Rv\ of\ next\ layer} + \frac{f}{Rm\ of\ layer} + \frac{g}{Rm\ of\ layer} \end{aligned} \qquad \textit{Equation 4.3}$$

For these equations the following is true:

c equals 1 if there exists a node directly following the current node in the current finger.

d equals 1 if the current node is connected to neither the drain nor the source.

e equals 1 if the current node has a node (in the next metal layer) directly above it.

f equals 1 if the current node is connected to the source.

g equals 1 if the current node is connected to the drain.

Rx is the resistance between vias.

Rv is the resistance of a via.

Rm is the resistance between start of finger and either the drain or the source.

If a metal layer node is connected to either the source or the drain, the current flowing into that node from the terminal is calculated and recorded in one of two columns, depending on the terminal. The total drain and source currents are calculated from these recorded currents. The drain current is then used to determine the approximate resistance of the full transistor.

4.2.3 Creating a workable form and adding physical parameters

The main functionality of this program will be covered in this section. There are two pages in the form: General and Metal Layers. There three changeable physical parameters for standard use on the General page of the form (Figure 4.7): number of fingers, drain-to-source pitch, and number of metal layers. These parameters are general and not specific to a specific metal layer.

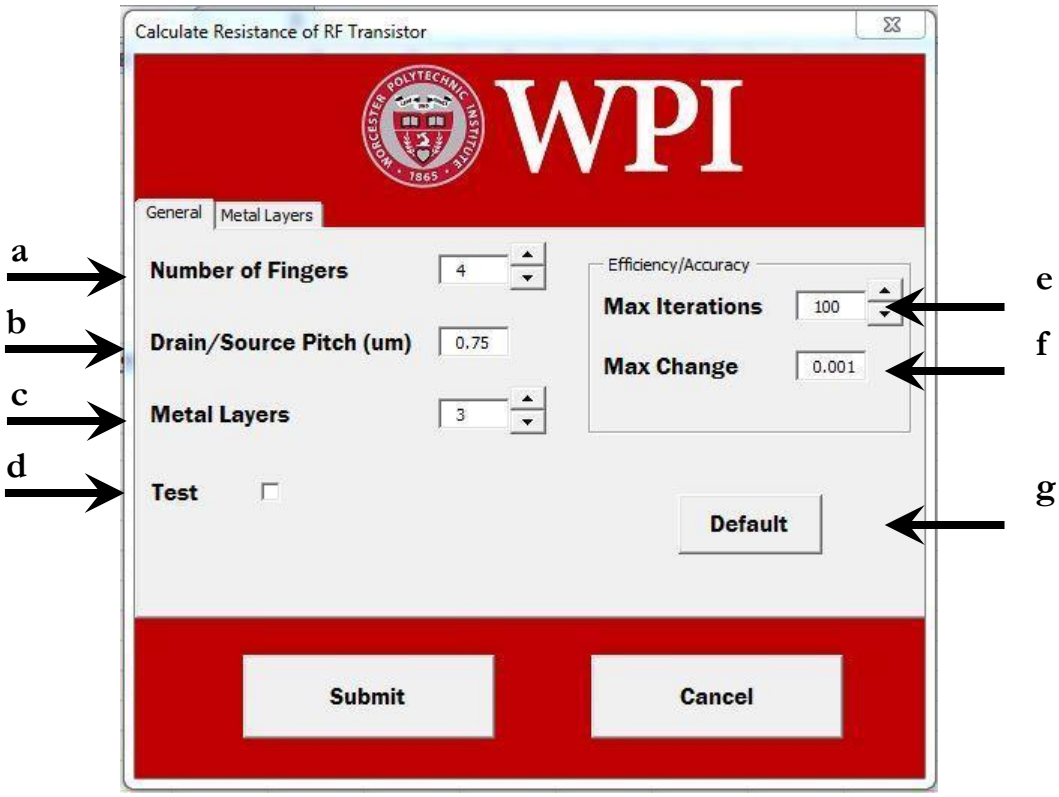


Figure 4.7. The General Page of the Form. *This page has the options that are independent of the specific metal layers. (a) Indicates the number of fingers of the device. This value cannot go below one. (b) Indicates the drain to source pitch, i.e. the distance between any two fingers, one representing the source and the other, the drain. (c) Specifies the number of metal layers used in this device. This value cannot go below one. (d) This option allows for the program to be tested against a circuit simulator. It will be discussed in more detail in a further section. (e) This value specifies the maximum number of iterations allowable in a circular dependency evaluation. (f) This value specifies the maximum difference between the previous approximated value and the current approximate value in a circular dependency evaluation that is allowed for the evaluation to stop, provided it hasn't run out of iterations. (g) This button sets all of the values back to their defaults. The default values are based on an example provided by Skyworks, with the exception of the number of fingers which was significantly decreased.*

There are eight changeable physical parameters for standard use on the Metal Layers page of the form (Figure 4.8): metal length for each layer, metal height for each layer, metal conductivity for each layer, finger width for each layer, via height for each layer, via width for each layer, via conductivity for each layer, and via pitch. With the exception of via pitch, all of these parameters are specified for the specific metal layer, whose tab is selected at any given moment. Via pitch is independent of a specific metal layer. However, since it changes the number of vias a metal layer may have, it was placed on this page to allow the user to more easily see how changes in via pitch will affect the number of vias.

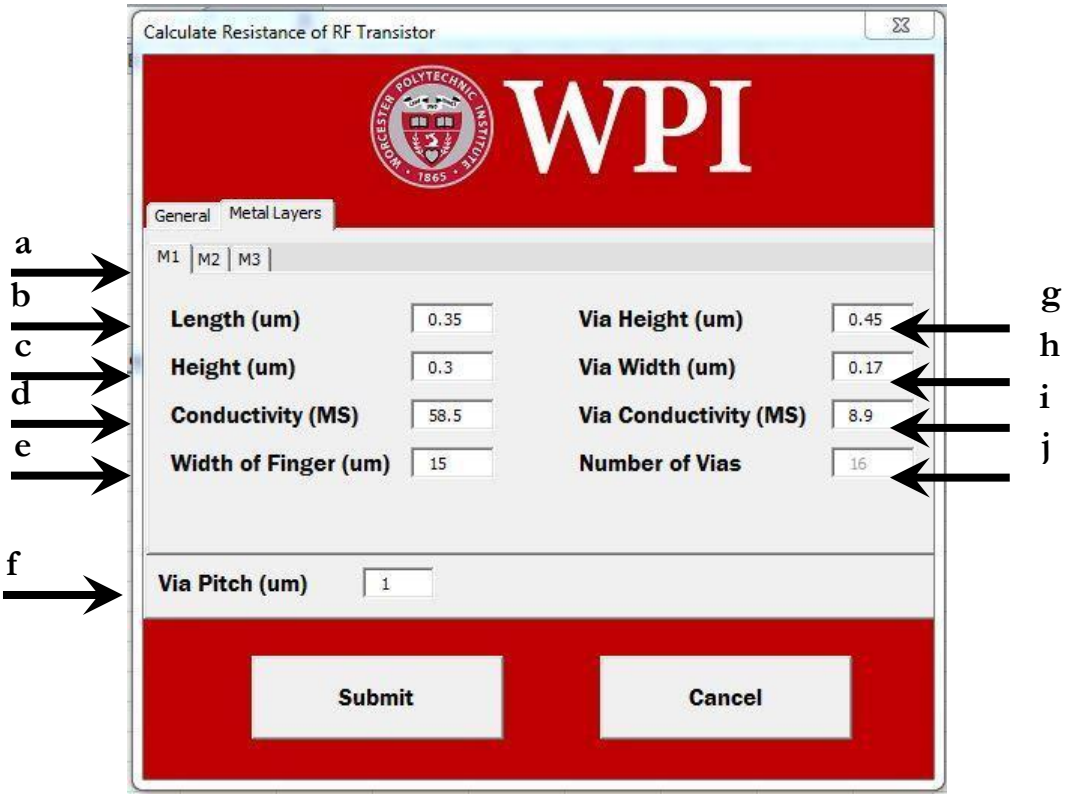


Figure 4.8. The Metal Layers Page of the Form. *This page includes the options directly related to the metal layers. (a) Allows for the selection of a metal layer for which the values are being viewed or edited. (b) Indicates the length in microns of the selected metal layer. (c) Specifies the height in microns of the selected metal layer. (d) Indicates the conductivity in Siemens * 10^6 of the selected metal layer. (e) Specifies the width of the finger of the selected metal layer. This value can be neither larger than the layer below it nor smaller than the layer above it. (f) This specifies the pitch of or distance between two vias. This is independent of a selected metal layer but affects the number of vias. (g) This specifies the height of the vias of the selected metal layer. (h) Specifies the width (which is also the length) of the vias of the selected metal layer. (i) Indicates the conductivity of the selected metal layer. (j) Shows the number of vias, which is based on the finger width as well as the via pitch.*

4.3 Using HFSS to determine transistor capacitance

In order to realize the drain-to-source capacitance values from the ADS simulation, a sufficiently accurate model for the capacitance of an individual transistor was required. If this model could be suitably fast, it would lead to faster transistor design.

4.3.1 Attempt at Closed Form Capacitance Model

Initially, a closed form model was attempted. The capacitance equation for two wires in parallel was chosen. This model would treat the copper conductor bars and the vias as wires of finite thickness. Using the

equation, it would find the capacitances between neighboring vias. Summing many of these capacitances would yield the total capacitance of the transistor.

There are several sources of error in this model. One is the assumption that the conductors are surrounded by a uniform dielectric constant. In the devices modeled for this project, some of the electric field exists in the silicon and some is dispersed through the insulator above the silicon. This insulator has a different dielectric constant than the silicon, resulting in the error. Another error arises from the assumption that the rectangular vias and conductors can be approximated as circular cross-sections.

The most significant problem with this approach, however, was the effect of the fringing field. The capacitance equation for two parallel wires does not account for fringing. Since the vias are short in comparison to their spacing, much of the energy stored in the electric field is found in fringe fields.

A small test was carried out in order to observe the accuracy of this approximation. An HFSS model of two vias in close proximity was constructed (Figure 4.9). A closed form equation was used to calculate the capacitance between the same two vias.

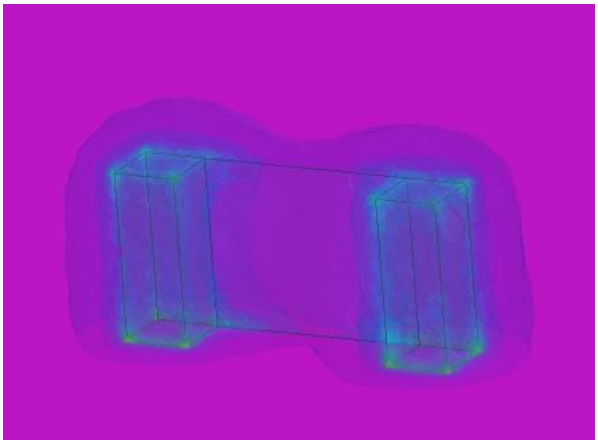


Figure 4.9. HFSS simulation of the two vias. *The effect of parasitic capacitances can be seen in the magnitude of the electric field as shown in this overlay.*

The results were very different. HFSS reported a capacitance of 73 aF, whereas the equation resulted in a capacitance of only 23 aF. This results in an error of 68%, an unacceptable value for any tolerance. It soon became obvious that the closed-form approach was not appropriate for this project.

4.3.2 Creating HFSS based equations for capacitance

A capacitance model was thus created using HFSS. This portion of the project modeled a small segment of a transistor. This segment was modified in various ways, including varying the drain-to-source pitch, via pitch and the number of conductor layers. For each of these variables, multiple simulations were run to obtain a representative curve of the effect they had on the drain-to-source capacitance. The results were used to formulate an approximate equation for the capacitance of a transistor based on certain physical parameters. The model was further complicated by the fact that some of the parameters depended on each other. For instance, the effect of via offsetting is influenced by via density. The parameters that were varied are shown in Figure 4.10.

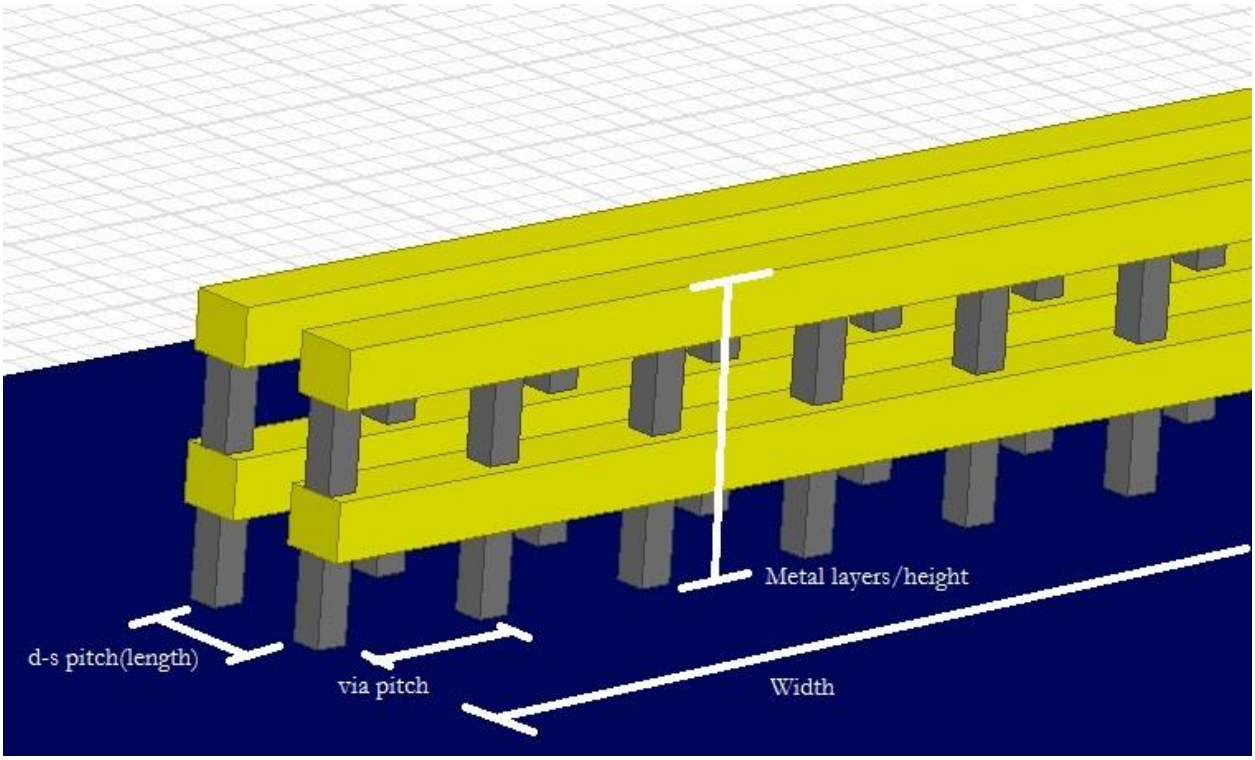


Figure 4.10. The parameters included in the simulations and model. *The drain-to-source pitch is the distance between the drain and source (about 1 um in this simulation), also known as transistor length. Via pitch is the distance between each via in any given finger. The number of metal layers stacked vertically was another parameter which was varied. The total width of the transistor was also considered.*

Another method considered in the model was via staggering. This technique lowers transistor capacitance without increasing resistance. In it, vias are staggered, with each via of a finger being placed across from the space between two vias in an opposing finger (Figure 4.11). The capacitance between the vias

on the source and drain is decreased because they are further apart. Since the conduction layer is not removed, the on resistance remains does not change. In this way, a transistor can have a lower Ron*Coff constant, and therefore less loss at high frequencies.

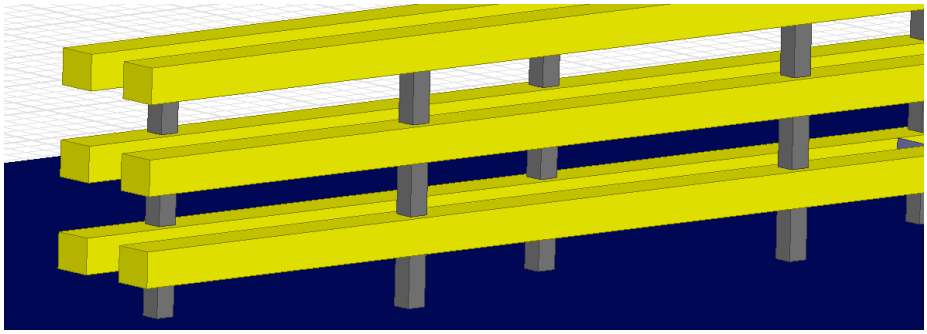


Figure 4.11. Example of FET layout with staggered vias. *Note that the vias are not directly across from each other. The via pitch has been greatly increased from that shown in* **Figure 4.10**. *Via staggering in most effective if the via pitch is high.*

4.4 Guideline for Simulation Usage and Interaction

Standing alone, each of these models is not very helpful to the designer. However, when they are used in combination, they become quite useful. The circuit-level model is meant to be used with the physical model in a circular process until an acceptable design is reached. The design starts with the circuit-level simulation. The switch topology is built, including the number of FETs stacked in series and the number of throws. Transistor width may be determined by the power requirements of the design, which will create a starting point for the off capacitances and on resistances.

The values for the off capacitances are then optimized with ADS in order to provide an even voltage load. If the RF losses are not greatly increased by this optimization, then the physical model can be used in an attempt to realize these capacitances. If the capacitances cannot be realized, the designer may need to return to the optimizer and readjust the limits of the optimization. This process can be cycled through many times until a suitably performing switch is found. This process is visualized in Figure 4.12.

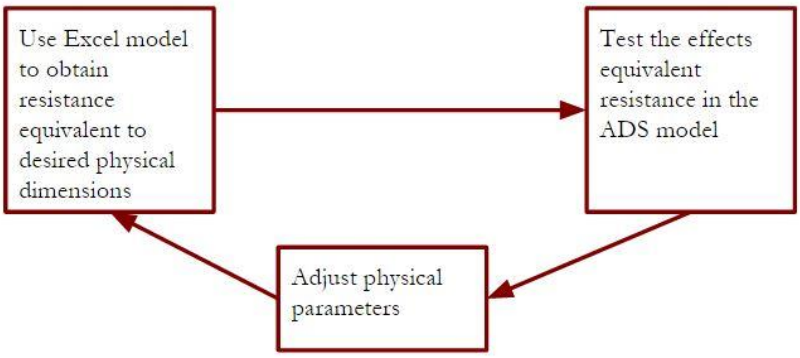


Figure 4.12. The circular design cycle for these models.

4.5 Gaining familiarity with the real-world technology

In order to gain familiarity with the technology, testing was done on the SKYA21013, a CMOS SOI switch manufactured by Skyworks Inc. This switch is used in such applications as GPS/Navigation systems, automated toll systems, remote keyless entry, telematics, and WLAN, to name a few. It is single-pole, double-throw band switch, with a high linearity, a low insertion loss, and a broadband frequency usage range between 0.1 GHz and 6.0 GHz [10]. A functional representation of this device is shown in Figure 4.13.

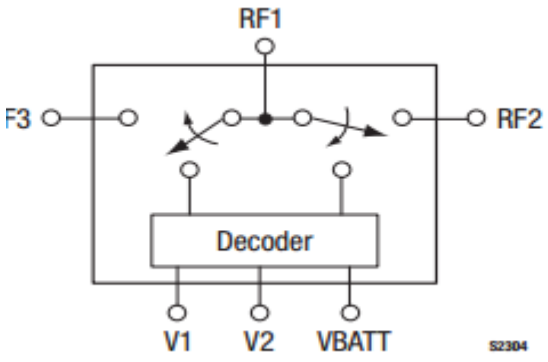


Figure 4.13. SKYA21013 Block Diagram. *Switching is controlled by two control voltage inputs (V1 and V2). Depending on the logic voltage level applied to these pins, the RF1 pin is connected to one of two switched RF outputs (RF2 or RF3) using a low insertion loss path, while the path between the RF1 pin and the other RF path is in a high isolation state)* **[10]**.

4.5.1 Initial testing was not viable

Initially, construction of the board was attempted independently of Skyworks Inc. A Skyworks RF switch was selected and several were ordered. A PCB board was designed around this switch, using DesignSpark software [11], and several prototypes were ordered from OSH Park [12]. This was not optimal, as these types of boards are not typically made for RF applications. However, at this point in the project, it was the only option. Several attempts were made to correctly solder the switch and the various other necessary components with multiple boards. This was difficult due to the limited availability of precision soldering tools. The standard tools used for soldering the type of chip ordered were not available, greatly hindering success. Thus, due either to flaws in the design (possibly related to the non-ideal nature of the PCB products for RF circuitry) or to issues with soldering, all testing attempts with the hand-soldered boards failed. A second option then came into view that was significantly more promising: testing through Skyworks.

4.5.2 Testing through Skyworks

After initial attempts at testing failed, a PCB Demo Board was requested from Skyworks Inc. in an attempt to create a viable test setup. This board was professionally manufactured and thus did not suffer from the same problems as the previous board attempts. Insertion loss and isolation were tested using an Agilent network analyzer available at WPI.

5 Results and Deliverables

The simulation package was implemented in Keysight's Advanced Design System (ADS). This included schematic layouts and simulations of the many-throwed switch topology. The single transistor model was implemented in a Microsoft Office Excel. The results of these implementations are covered in this section.

5.1 ADS Simulation and Optimization results/implications

The ADS switch model can optimize and simulate a number of different parameters in a given switch. After creating the optimizer and simulator mentioned above, tests were done on a series of switches to demonstrate its capability. This tool performed as expected in all cases, proving its usefulness.

5.1.1 Optimization results

Some sample results are shown in Figure 5.1. Before the optimizer was run, all drain-to-source capacitances were equal. It can be seen that the voltage across each FET ranged from about 0.65 volts to about 1.05 volts, an unacceptable variance. After the optimizer was run, the voltage loads were all approximately equal, at about 0.82 volts. Optimization times were not exorbitant, the longest being around four and a half minutes. This seems reasonable even if a designer needs to run this program many times in the course of the design process.

The constant Ron-Coff optimizer took slightly longer. This was probably due to the higher number of goals it had, leading to more stringent requirements. This optimizer did not take long either, however, with simulation times in the range of six to eight minutes.

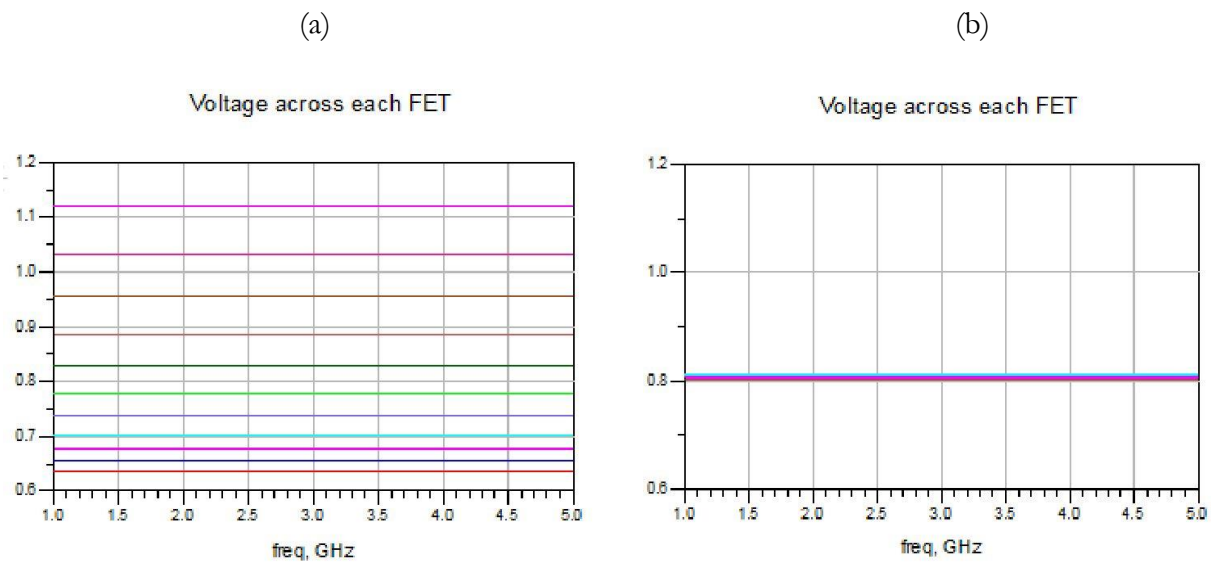
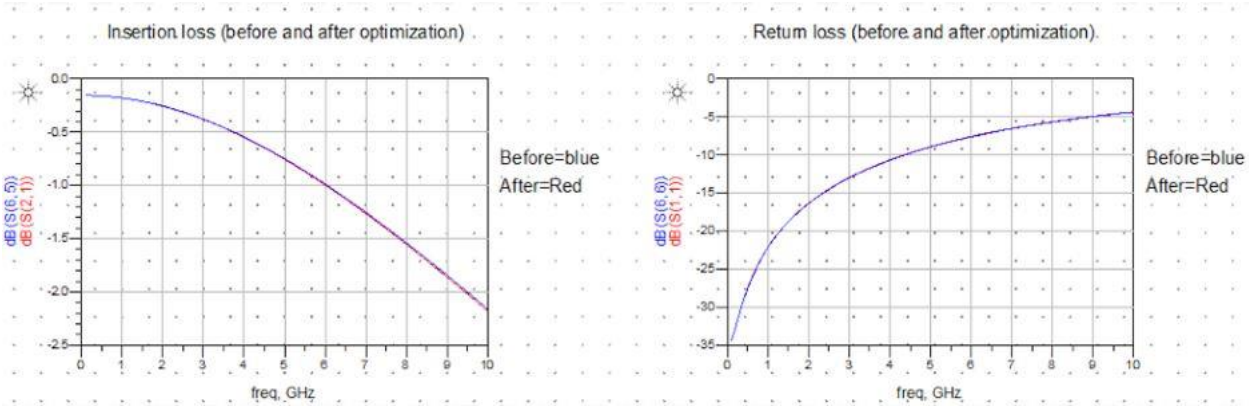


Figure 5.1. Optimization results from standard ADS model. *(a) Before optimization. (b) After optimization. The x-axis represents frequency. The y-axis is voltage load for each FET.*

5.1.2 S-Parameter Prediction

The ADS model was also used to evaluate the effect of the previous optimization on small-signal RF losses. This was needed to ensure that the optimizer had not grossly increased the losses of the switch. The ADS model automatically tests the insertion loss, return loss, and isolation, both before and after the optimization, and displays the results. An example of this functionality is shown in Figure 5.2.

(a) (b)



(c)

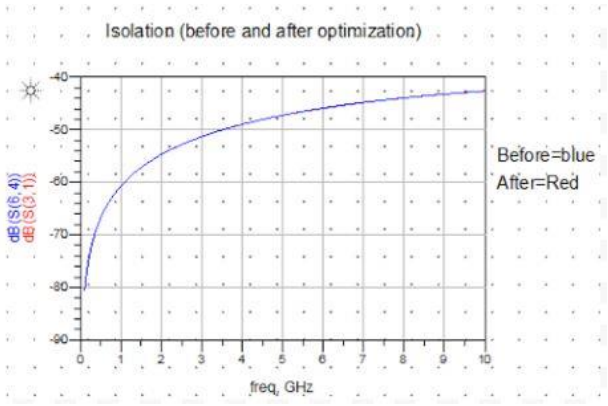


Figure 5.2. S-Parameter Results. *RF losses in dB, plotted are the (a) Insertion loss, (b) Return loss, and (c) Isolation of a SP12T (single pole 12 throws) switch. The parameters before optimization are shown in blue and the post optimization results are shown in red. It can be seen that in this particular example, there was very little effect on RF losses from the optimization. This is not necessarily true for every example.*

5.1.3 Sensitivity analysis information

Due to the speed of each simulation, the sensitivity analysis tool allowed the team to find the sensitivity of many values. Of particular interest was the sensitivity of the output insertion loss, return loss, and isolation to changes in on resistance and off capacitance. There was a desire to determine if there was a major difference between the switch performance before optimization and after optimization. It was found that there was not.

It was found that the on resistance of the active arm had the most effect on the insertion loss, with each series resistance having approximately the same sensitivity. This was expected, as the on resistance is the

primary source of loss in the system. Further, the return loss was greatly affected by the series off capacitances of the inactive arms, with the capacitance closest to the common port having the most effect. This was also not a surprise. Assuming constant line impedance, the return loss is solely a function of the input impedance. Since this switch had twelve throws, changing the off capacitance for all the inactive arms is eleven times more effective at influencing the input impedance than changing anything in the active arm.

The on resistances and off capacitances in the inactive arms had the greatest influence on the isolation between active and inactive arms. This is due to the fact that the isolation is essentially the insertion loss of the inactive arms. In order to improve isolation, the designer should decrease the off capacitance of the series FETs. This creates an engineering tradeoff between isolation and insertion loss. To decrease the series off capacitances, metallization is removed. This increases the series resistances, which increases the insertion loss.

5.2 HFSS Results and implications

Our finite element analysis models were constructed and run in ANSYS HFSS. We assumed that with enough cycles, the results from HFSS would approach the actual physical values. To find the appropriate number of cycles, the team repeatedly simulated a sample FET, constantly increasing the number of cycles until the variance between capacitance values was undetectable. In the end, HFSS required 15 iterations in order to obtain sufficiently accurate results. We considered a variance of 0.5% between iterations to be sufficiently accurate. Since there was no means of actually testing capacitances, the HFSS results were used as quasi-real values.

Simulation times varied from fifteen minutes and to two hours, due to the varying complexity of our models. A 15 um finger was modeled. In order to find the capacitance of an entire FET, this result was multiplied by the number of fingers. Metallization schemes with more metal layers and more vias took much longer to compute than did simpler models. The simulations were run on a Dell Optiplex 7010 running an i7-3770 at 3.4 Ghz with 8 GB of RAM.

5.2.1 Capacitance Results ad Equations

A total of forty-three tests were run in HFSS to acquire a pool of capacitance values large enough to create a generalized equation for transistor capacitance. Six parameters of the FET were varied, including the number of metal layers, via pitch, the drain-to-source pitch, via offset, the number of fingers, and the length of each finger. The large number of tests was necessary because of the interdependencies between the parameters and the non-linear effect that some of them had on the capacitance.

Many of the parameters affected each other. For instance, the effect of offsetting the vias depended upon both the via pitch and the drain-to-source pitch. This meant that via offsetting had to be tested under many different conditions. The number of metal layers and the via pitch were also interdependent.

Many of the parameters had nonlinear effects on the capacitance. An example of this is via pitch. As the pitch decreases, the spacing between vias decreases. The vias start to act like a metal plate and the effect of adding more vias results in limiting returns. This also happens if vias are removed. As the via pitch increases, the vias become sparse. The effect they have on the capacitance of the system is vastly overshadowed by that of the conductors. Thus, the effect of via pitch on capacitance has a logistic curve. Similarly, the via offset had a nonlinear effect on the capacitance which was dependent upon the via pitch.

These problems led to inaccuracies in our final model. Usually this model was accurate to within five or ten percent of the actual capacitance. However, if the vias were offset or the drain-to-source pitch was not 1μm, the error sometimes reached close to twenty percent. This error makes this model not useful for final designs. However, it could still reasonably be used in the preliminary stages of the design process. Figure 5.3 shows the final model.

		val/modifier
metal layers	1	0.10175
pitch(between vias in u)	2	0.831394998
d-s pitch	1	1.818181818
ofsetting of vias (1 for yes, 0 for no), **0 if d-s pitch is not between 1 and 6**	0	1
# of fingers	133	133
finger length(in u)	15	15
Total Capacitance in fempto======		306.8471088

Figure 5.3. HFSS Results. *Shows a final test run of our model. Input are the number of metal layers, via pitch, drain-to-source pitch, via offsetting parameter (either 0 or 1), the number of fingers, and the length of each finger. The result is shown to be 306 fF in this case. This compares favorably to the HFSS value of 321 fF, yielding an error of only 4%.*

5.3 Excel Resistance Model

The Excel resistance model required testing to determine if it was in line with our project goals. First, its results were compared to the results of other circuit simulators. Second, several simulations done using it were timed. These tests were done to ensure the sufficient accuracy and speed required for the project.

5.3.1 Comparison to circuit simulator calculations

In order to ensure that the algorithm was accurate to the lumped-component model, it was tested against two simulations: a circuit simulator applet and an LTSpice simulation. Each test and its resulting drain currents are shown in Table 5.1. The devices used for these tests are quite small in order to facilitate creating the circuit simulations. Normal device sizes are prohibitively large for this type of testing. Each simulation was run with the drain connected to 5 volts and the source connected to ground. The results in Table 5.1 demonstrate that the Excel model is consistent with the circuit simulators.

Table 5.1. Comparing Excel model to circuit simulator results.

Number of Fingers	Metal Layers	Transist Resist	Number of Vias	Via Resist	Resist between vias	Circuit Sim Applet (mA)	LTSpice (mA)	Excel Model (mA)
4	1	100	3	100	100	24.61	24.6072	24.608
4	2	100	M1: 3 M2: 3	M1: 100 M2: 100	M1: 100 M2: 100	37.58	37.5803	37.583
4	1	200	3	50	100	25.01	25.0149	25.016
4	2	200	M1: 3 M2: 3	M1: 50 M2: 60	M1: 100 M2: 150	35.62	35.6184	35.622
3	2	200	M1: 3 M2: 3	M1: 50 M2: 60	M1: 100 M2: 150	24.95	24.9474	24.949
3	1	200	4	50	100	16.02	16.021	16.022
3	2	200	M1: 4 M2: 3	M1: 50 M2: 60	M1: 100 M2: 150	23.11	23.1121	23.114

5.3.2 Runtime Comparison

In order to verify that the Excel model met the time-efficiency goal, several test simulations were timed. The results of these tests are shown in Table 5.2. The range of parameters for the tests was chosen to display a range of potential simulation times, from the least to most time-intensive. As can be seen, even the most time-intensive simulation is only a little over an hour, significantly less than the more intensive simulations typically used.

Table 5.2. Timing results for Excel model simulation.

Number of Fingers	Number of Vias	Number of Layers	Max Iterations	Max Change	Runtime (hh:mm:ss)
4	16	1	100	0.001	0:00:04
4	16	4	100	0.001	0:00:19
4	32	1	100	0.001	0:00:06
133	16	1	100	0.001	0:04:53
4	16	1	500	0.001	0:00:04
4	16	1	100	0.00001	0:00:08
133	16	3	100	0.001	0:20:45
133	32	4	500	0.00001	1:13:53

5.4 Production Switch Testing Results

Using the network analyzer, two tests were performed. These tests included the insertion loss (IL) of each switch channel and the isolation to an inactive arm. The first experiment was conducted to examine the isolation of the SKY13370-374, followed by the insertion loss. The new demo board performed as specified in its data sheet and as the team intended. The switch was found to be very efficient and had hardly any losses. The results for insertion loss and isolation from the network analyzer are shown in Figure 5.4 and Figure 5.5, respectively.

Figure 5.4. Isolation results of the test switch. *Frequency was swept from 300 kHz to 3 GHz.*

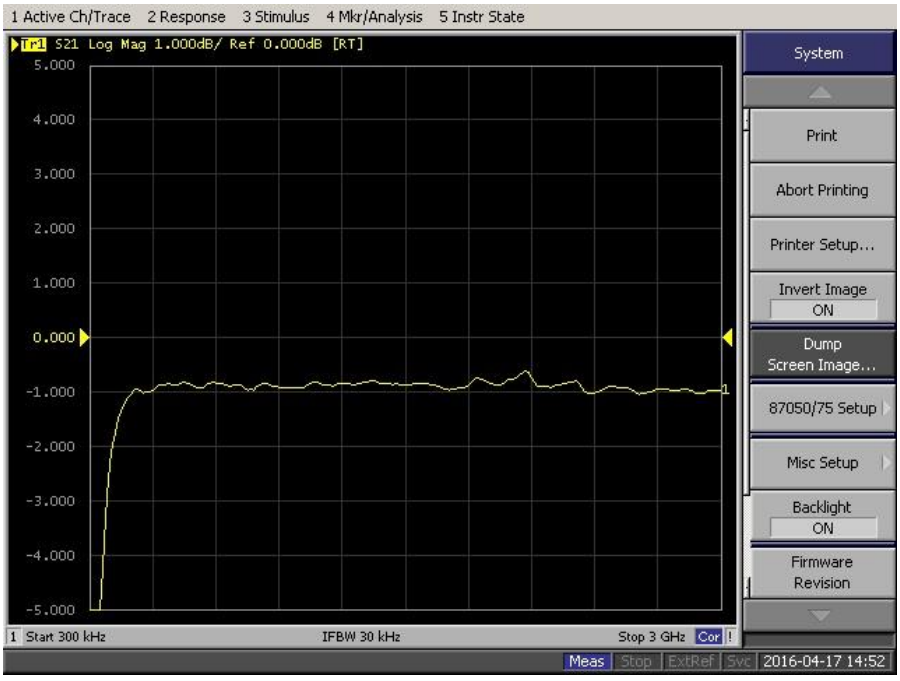


Figure 5.5. Insertion loss of the test switch. *Frequency was swept from 300 kHz to 3 GHz. For most of the range, only 1dB of loss was detected.*

6 Conclusion

This project created faster models for and investigated the optimization of SOI FET RF switches. The many frequency bands used in the cellular industry necessitate fast and efficient RF switches. These switches can be altered in multiple ways in order to make the design more efficient. However, such alterations are infrequently attempted due to the long runtimes of the simulations involved. As a result, our focus in this project concentrated on creating models that decreased early design simulation runtimes. Since the tools were already being developed as part of this project, there was also a push to use these new models to develop a set of design recommendations.

To do so, our research delivered a simulation package to Skyworks Inc. This package included three major tools: the full switch ADS model, the transistor resistance Excel model, and the capacitance HFSS model. The full switch model consisted of a simulation of a many-throw switch model in Keysight's Advanced Design System (ADS) and a behavioral using lumped element approximation for the FETs. The key functions of this tool included the abilities to provide Ron-Coff parameter values for optimal performance, to simulate and optimize for insertion loss, isolation, return loss, and equal voltage distribution, and to provide sensitivity analysis to show which parameters on which FET in the stacks have the most influence on Insertion Loss. The transistor resistance model was a single FET model, implemented in Excel and designed to calculate the total resistance of the FET in question based on several physical parameters. The capacitance model provided a simple and fast way to calculate the approximate capacitance of a RF transistor. This model and the full switch model were used to provide recommendations for improved switch design.

There are many aspects of this subject matter that were not encompassed by this project. Consequently, there are many possibilities for future research. More complex, lumped-component approximations of the active and inactive transistor could be implemented in a similar full switch model. This could provide more accurate simulations and may not require too much extra compute time. The Excel model certainly offers many options for further development, including alterations to the lump-circuit

approximation in order to increase its accuracy. There also is room for creating a model that can be tested reasonably well in comparison to a real-world switch. This project covered a small area of RF switch simulation and optimization. Given the ever-growing nature of the cellular industry, the potential opportunities to advance our modeling environment will only grow.

7 References

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