April 2009

Smart Recloser Breaker

Andre R. Campbell
Worcester Polytechnic Institute

Kerron Dwight Brown
Worcester Polytechnic Institute

Yusuf Ziya Aydin
Worcester Polytechnic Institute

Project Number: AEE

Smart Recloser Circuit Breaker

A Major Qualifying Project Report:

Submitted to the Faculty

Of the

WORCESTER POLYTECHNIC INSTITUTE

In partial fulfillment of the requirements for the

Degree of Bachelor of Science

By

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Yusuf Ziya Aydin

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Kerron Brown

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Andre Campbell

4/28/2009

Approved:

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Professor Alexander Emanuel, Advisor

Abstract

This project explores a method for protecting electric power distribution systems against persistent faults. We designed and implemented a device that we called “Smart Recloser Breaker” to provide the necessary protection for a power distribution system. The “Smart Recloser Breaker” is to open when there is a fault on the main line and close only when the fault is removed or cleared. The device functionality was tested and demonstrated using theoretical and actual simulations.

Acknowledgements

We would like to take this opportunity to show our gratitude to our Advisor, Prof. Alexander Emanuel for the help he administered to us during the course of this project. We would also like to thank the Professors of the ECE department for the advice they gave us. And last but not least we would like to thank our parents and friends for their love and support. Without the help of the people we have mentioned, this project would have never been possible.

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1. Introduction

In the world we live in today electricity is vital for the day to day activity of almost everyone in the world, if there was no electricity in the world we might as well be living in the 19th century. Therefore it can be said that it is of outmost importance that we preserve and protect our electrical power system. Although there are three main components in an electrical power system, the protection of the distribution system is of great importance due to the fact that major parts of the system is exposed to things like weather elements, vehicles and animals. These factors can cause what is known as an electrical fault, which in turn can cause damage to the distribution system and affect the customers through surges and blackouts. And because of electrical faults utility companies has put preventative and detection measures in order to reduce the damages that faults may cause.

In almost every fault protection system, one can find a circuit breaker, which is an electro-mechanical device that disconnects the distribution circuit when there is a fault and when the fault is removed it is manually reclosed in order to reconnect the circuit. Another type of breaker that has the ability to reclose automatically was designed and is called the recloser circuit breaker. The recloser breaker is ideal in 90% of fault situation which are transitory or temporary, while the breaker is non-ideal for persistent faults mainly because it has preprogrammed amount of attempt and after that it remains open.

This project outlines the research, design and implementation of a “smart” recloser breaker, which will be suitable for use when there is a persistent or permanent fault. The design of this breaker is primarily based on the comparison of voltage levels in a power line; comparing them in order to make a decision on where or not there is a fault present in the line. And based on the results of the comparison a decision is then made to either keep the line connected or to disconnect it.

2. Background

This section covers the systems, concepts and devices which are relevant for the understanding of the design, discussions and solutions that are found in later chapters. A general background of electrical power distribution system is provided, followed by an overview of distribution lines which are important for the comprehension of how faults occur. Then there are descriptions of what a fault is and what a typical fault protection system is comprised of. And the remaining sections deals with breakers and recloser breakers.

2.1. Power Distribution System

In the breakdown of an electrical power system one will find three basic subsystems which are; a generation system, a transmission system and a distribution system. This section will discuss a typical distribution system and its layout. Electric power distribution is the section of the electrical power system that takes the electricity from highly meshed, high voltage transmission circuit and delivers it to customers. At the distribution station, a substation transformer takes the incoming transmission voltage, which is about 35 to 230kV and steps it down to about 600V to 35kV (Short, 2004).

From the distribution substation primary distribution lines takes the voltage from the distribution station to a distribution transformer which then steps down the voltage again to low voltage secondary distribution lines typically 120/240 V. From the distribution transformer the secondary distribution connects to the end user whether commercial, industrial or residential. A figure of a typical electrical power system is shown in Figure 1.

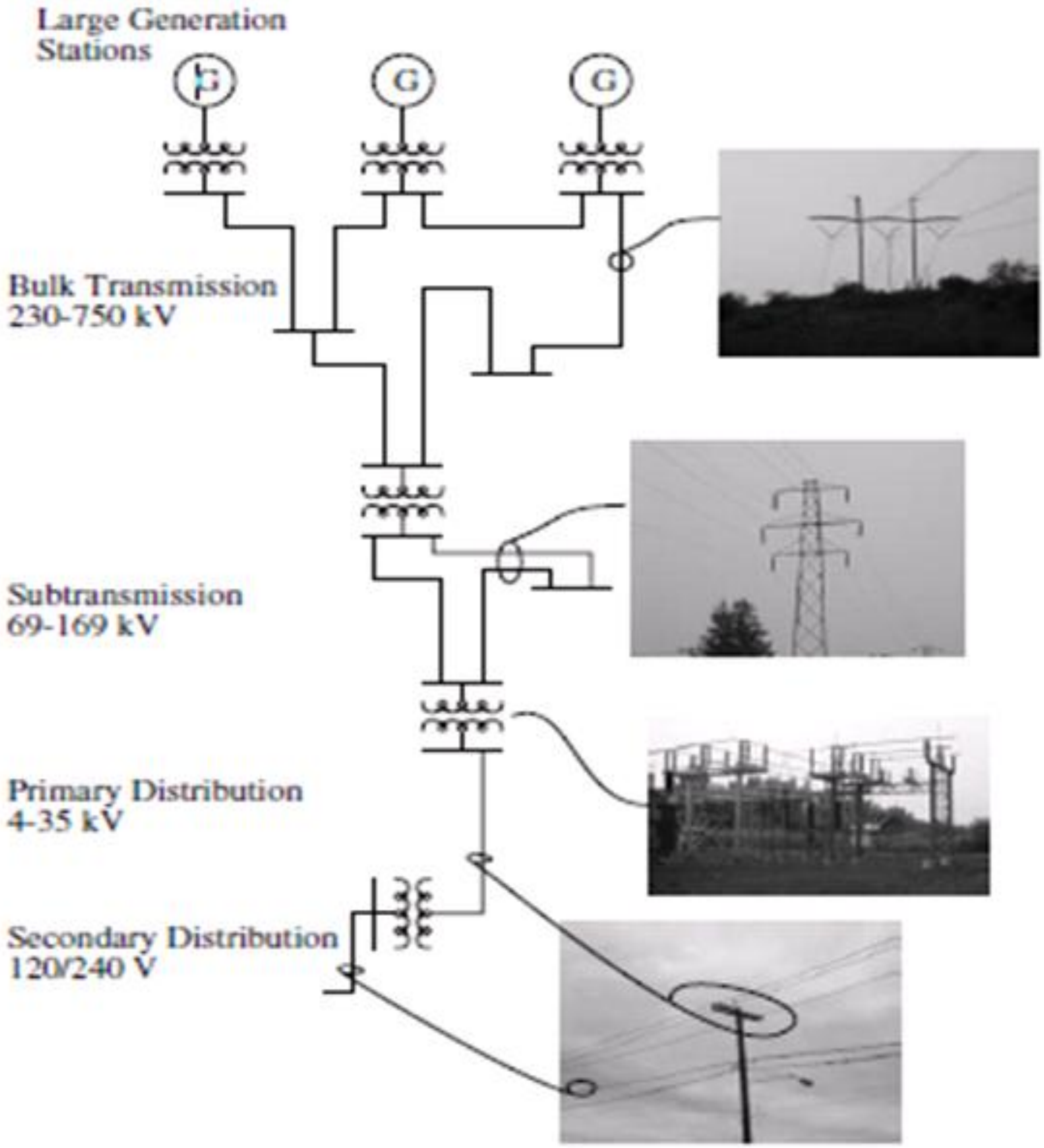


Figure 1 - Typical Layout of an Electrical Power System

2.2. Distribution Lines

In order to link the power generated from power plants to the customers who require it, power lines are utilized. There are two types of power lines transmission lines and distribution lines (Inc.). Distribution lines are those that carry electricity from substations to residential neighborhoods, industrial areas and commercial districts everywhere. There are two types of distribution lines, namely overhead lines and underground lines. We will concentrate on overhead distribution lines in this section due to its relevance to our project. Distribution Lines are those that link the power from substations to end-use customers; they can be three phase or single phase (Gonen, 2008).

Distribution lines are normally smaller in size in comparison to transmission lines and are rated for smaller voltage typically in the range of less than 69,000V. Because overhead lines are exposed to such things as trees, animals, wind, lightening, cars and kites which induces problems that can damage the distribution lines and system. A picture of single phase distribution lines can be seen in Figure 2.

Figure 2 - A picture of single phased distribution lines

2.3. Fault and Fault Protection

In general faults that occur in distribution lines are short circuits. Faults can be caused by a falling tree branch, lightening or even an animal running on the line. Faults are normally accompanied by a spike in current levels, which affects power quality illustrated through such things as surges and blackouts. There are four types of faults namely: phase to ground (most popular), two phases to ground, three phase to ground and phase to phase. The ground to phase fault occurs when there is an electrical path between the ground and any of the distribution lines (Williams). Typically Power utility companies spend a great deal of time and money for fault detection and protections, in order to prevent further damaged to their distribution system and their customers. Typical fault detection and protective system would normally include circuit breakers or reclosers, control devices, measuring devices and protective relays.

2.4. Circuit Breakers and Reclosers

Circuit breakers are automatic electric switch that are designed to protect electrical circuits from current overload and short circuits. Although there are several different types of circuit breaker, they all have the same operational concept (just different mechanisms) in that they all must detect a fault and then their contacts open in order to discontinue the circuit. There are three types of circuit breakers, low voltage breakers, medium voltage breakers and high voltage breakers. The breakers that are typically used in distribution systems are the medium voltage breakers. There are two types of medium voltage circuit breaker, the vacuum circuit breaker and the air circuit breaker and they both fall in the range of 1 to 72kV for their voltage rating (Chen, 2005).

A recloser is a special type of circuit breaker that automatically recloses after a fault has occurred in overhead power lines. When a fault occurs in a overhead power line a typical circuit breaker will disconnect its contacts disabling the line while with a recloser the contacts are disconnected during fault occurs but instead of being permanently disconnected the recloser makes several attempts to reclose, doing so permanently when the fault is cleared (Grigsby, 2000). Most faults are temporary or transitory and the reclosers are perfect for these type of situation, but if the permanent of persistent the recloser will exhaust its pre-programmed attempts and remain open.

3. Problem Statement

In the power utility business, protection of distribution lines is essential and a critical part of the protection system is the recloser breaker. The recloser breaker is perfect for faults that are transitory but non-ideal for persistent faults. Our task is to design and implement a recloser breaker that is ideal for both transitory and persistent faults.

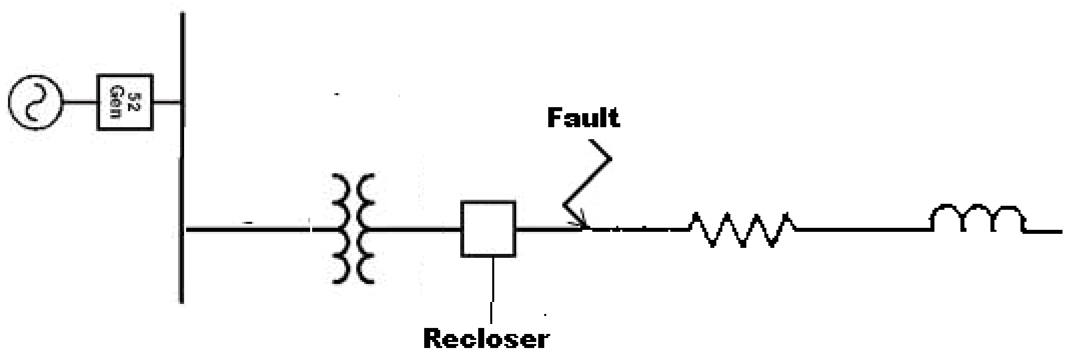


Figure 3 - Schematic

4. Design Approach and Simulations

This section describes the design process for the "smart" recloser circuit breaker. A basic system block diagram is shown below in Figure 4. What follows is an overview of each block followed by a detailed design description. The next section looks at the overall design of our project, which provides an understanding of how the individual components come together.

4.1. Overall Design

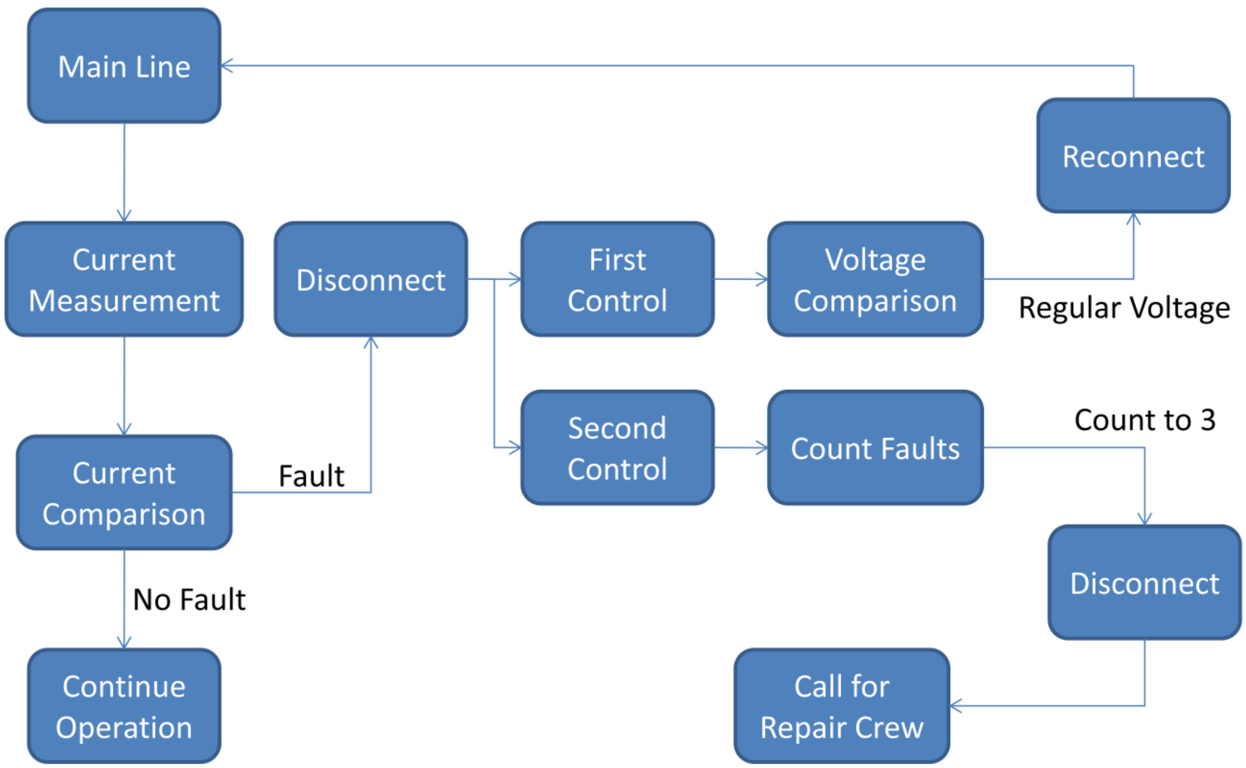


Figure 4 - Block Diagram

4.1.1. Main Line

In order to test the smart recloser circuit breaker, it has to be connected to a distribution line. Since power distribution lines are inaccessible, a main line was designed within the constraints of WPI's laboratory environment. A potentiometer and a variable voltage source from the MQP laboratory were used to mimic the power generation site and the load. The voltage supply remained constant and produced a fault by short circuiting the load.

4.1.2. Circuit Breaker

As long as there is current flowing through the main line, the circuit breaker will measure the current through the line, compare it to a threshold that it shouldn't exceed and disconnects the main line if needed.

4.1.3. 1st Control System

For the circuit breaker to have its reclosing functionality there has to be a control system that checks if the fault is still present or if it is cleared, which is the 1st Control System .The 1st Control System is designed to monitor the main line even when it is disconnected. This is done by connecting a large resistor in parallel with the switch from the circuit breaker that disconnects the line. The large resistor doesn't affect the circuit under normal conditions, but it allows us to measure the voltage level during a fault. If the voltage is at the desired level, the 1st control circuit resets the disconnection that was caused by the circuit breaker and this causes the main line to resume operation. This avoids the need of a technician being sent to the site if the fault is only temporary.

4.1.4. 2nd Control System

A 2nd Control System was designed in order disconnect the main line permanently after the fault has happened after a pre-programmed number of times. It includes a counter which counts the number of times a fault occurs. If the fault occurs three times, then it disconnects the main line until a technician arrives on site and resets the breaker.

4.2. Detailed Circuit Design and Simulations

4.2.1. Main Line

The main line represents a power generator and a load. The role of the main line can be better understood by looking at Figure 3. For testing purposes, designing a main line at a smaller scale was required; a schematic of our design can be seen in figure 5. Nodes 2 and 4 are the connections to the recloser circuit breaker.

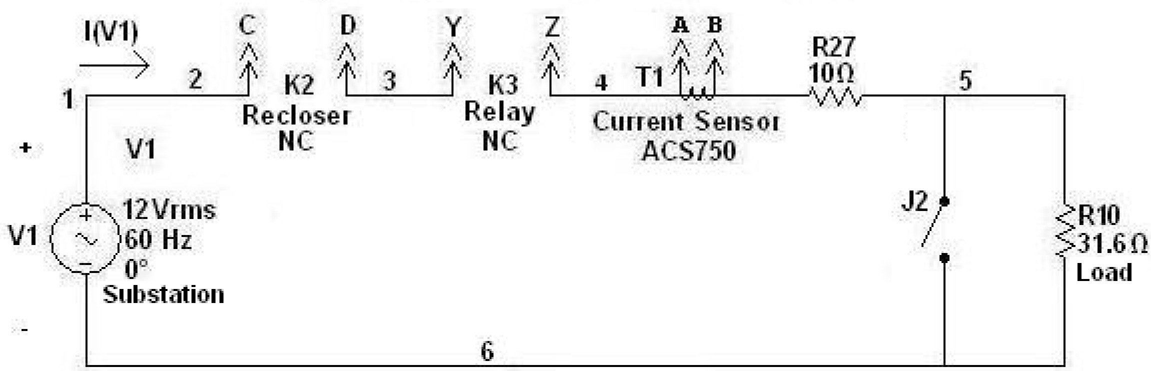


Figure 5 – Main Line

The voltage source V1 represents the power generation system and R10 represents the load. Switch J2 is placed between nodes 4 and 5 in order to create a short circuit and increase the current through the main line. Under laboratory conditions, a sinusoidal voltage source of $12V_{rms}$ was used to supply a 41.6Ω load under regular operation. During a fault (when J2 is closed) the load drops to 10Ω which results in current I(V1) to increase. The peak current through the main line will be:

Regular operation: $I(V1) = \frac{12\times\sqrt{2}}{41.6} = 0.408A$

During fault: $I(V1) = \frac{12\times\sqrt{2}}{10} = 1.69A$

Figures 6 and 7 illustrate the main line's current and voltage simulations during regular operation and during fault.

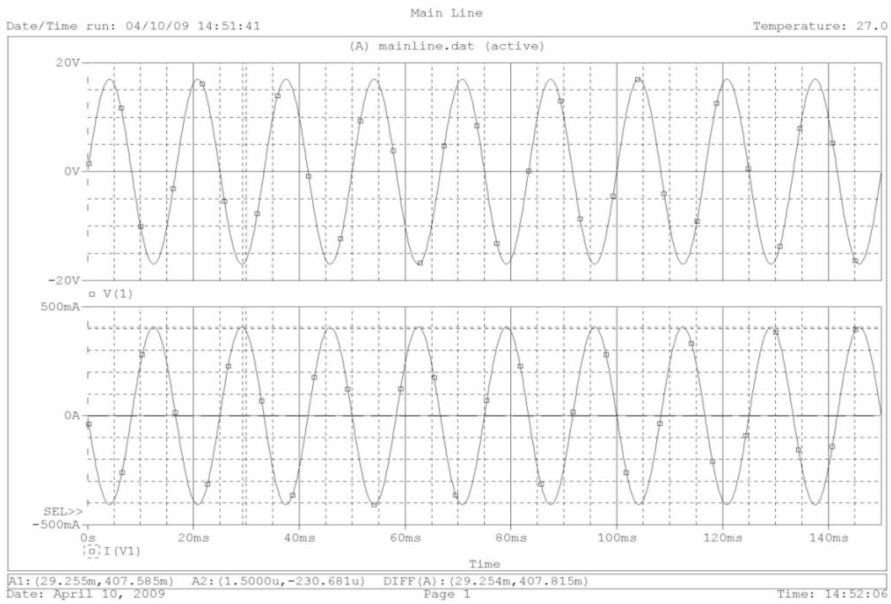


Figure 6 – Substation voltage V(1) and current through the main line I(V1) during normal operating conditions

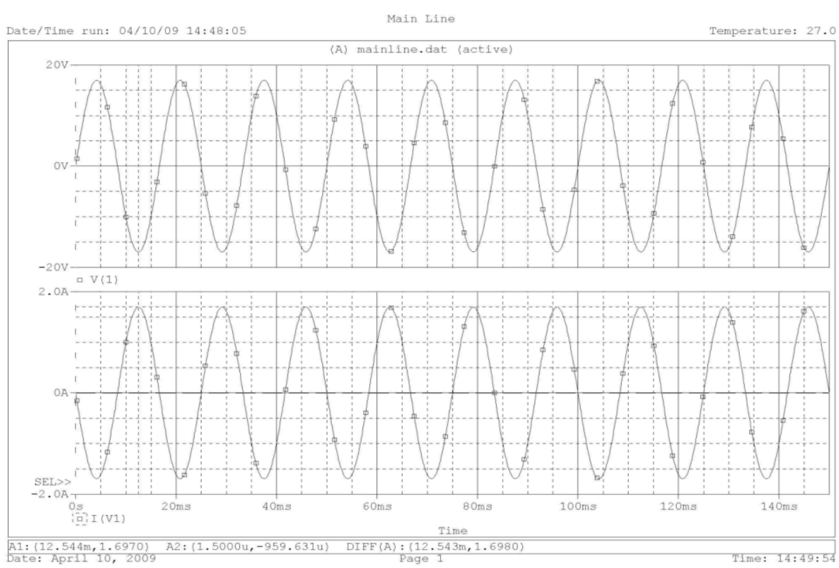


Figure 7 - Substation voltage V(1) and current through the main line I(V1) during fault

4.2.2. Circuit Breaker

As mentioned earlier, the current sensor of the circuit breaker measures the current on the main line and the circuit breaker will open based on this current level. Next, the circuit breaker will be divided into two parts, the current measurement section and the current comparison section. Each part and the components used will be described in detail.

4.2.2.1. Measuring Current

The first part of the circuit breaker measures the current flowing through the main line. For that purpose, a hall-effect current sensor, an AC coupling circuit and an operational amplifier circuit is designed to feed the measured current to the current comparison circuit.

Hall Effect Sensor

The first stage of the current measurement process is an AllegroACS750SCA-100 Hall Effect Current Sensor which is shown on Figure 8.[1] The current drawn from the voltage source on the main line will go through this device, and a voltage proportional to the instantaneous current is produced at the

Figure 8 – Allegro ACS750SCA-100

output terminal. This sensor requires a single 5v supply, and the output rides on a 2.5V offset. Table 1, shown below, provides relevant data from the ACS750 data sheet. The device requires at least 4.5 volts, which is different than the supply voltage we used at other parts of the circuit. This

[1] http://www.allegromicro.com/en/Products/Part_Numbers/0750/0750-100.pdf

necessitates two different DC voltages from the power supply. The small primary conductor resistance ensures that the device will have no significant interference on the actual current, and since the output resistance of the device is small, we don't need to be concerned with the input impedance of the next stage of the module. Since the bandwidth of the device (13kHz) is much greater than our operating frequency (60Hz), we can be sure that no loss of signal will occur due to frequency limitations. With the device sensitivity of 20mv/A, we see that we will produce only 20mV per 1A current. This indicates the need of amplification in order to be able to be more sensitive to current changes. However, we need to get rid of the 2.5V DC offset voltage which tends to hide the AC Signal due to the difference in values. Figure 9 illustrates how the current sensor is set up according to the suggestions from the Allegro website to connect a bypass capacitor.

Supply voltage range	4.5v - 5.5v
Primary Conductor Resistance	130uA
Output Resistance	1-2Ω
Bandwidth	13kHz
Sensitivity	18.75-20.75mv/A

Table 1 - Current Sensor Characteristics[1]

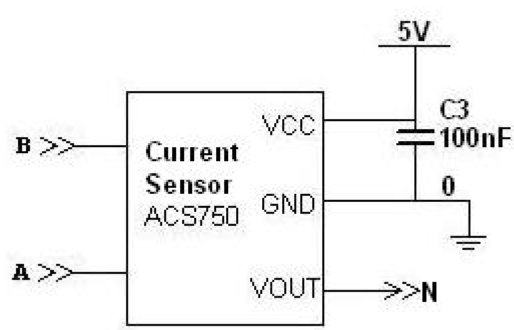


Figure 9 - Current Sensor

During normal operation, there will be 0.408A current through the main line as calculated before. This will increase to 1.69A during fault. According to these current values, the output of the current sensor will be:

Regular operation:

$$Voltage\ Output_{pk} = Current \times Sensitivity = 0.408A \times \frac{19.75mV}{A} = 8.06mV$$

During fault:

$$Voltage\ Output_{pk} = Current \times Sensitivity = 1.69A \times \frac{19.75mV}{A} = 33.37mV$$

AC Coupling

Because we need to separate the AC portion of the signal from the DC component, an AC coupling circuit is utilized. AC coupling rejects the DC component in the signal which is needed to condition the output of the current sensor which is riding on a 2.5V offset. Figure 10 shows the circuit that is used to reject the DC offset and keep the AC signal. The capacitor C2 is used to filter the DC component.

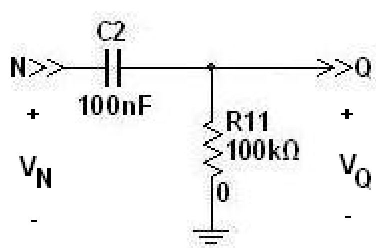


Figure 10 - AC Coupling

In order to verify the operation of the AC coupling circuit, we ran a simulation in PSPICE by supplying V_N with the output voltage of the current sensor during regular operation. The simulation gave the following results on Figure 11. The waveform labeled V_N is the approximated output of the current sensor by the calculations before. The next waveform labeled V_Q is the result of AC coupling. It can be seen from the waveforms that the AC coupling circuit achieved its objective successfully as the output V_Q of the same magnitude is centered at 0V.

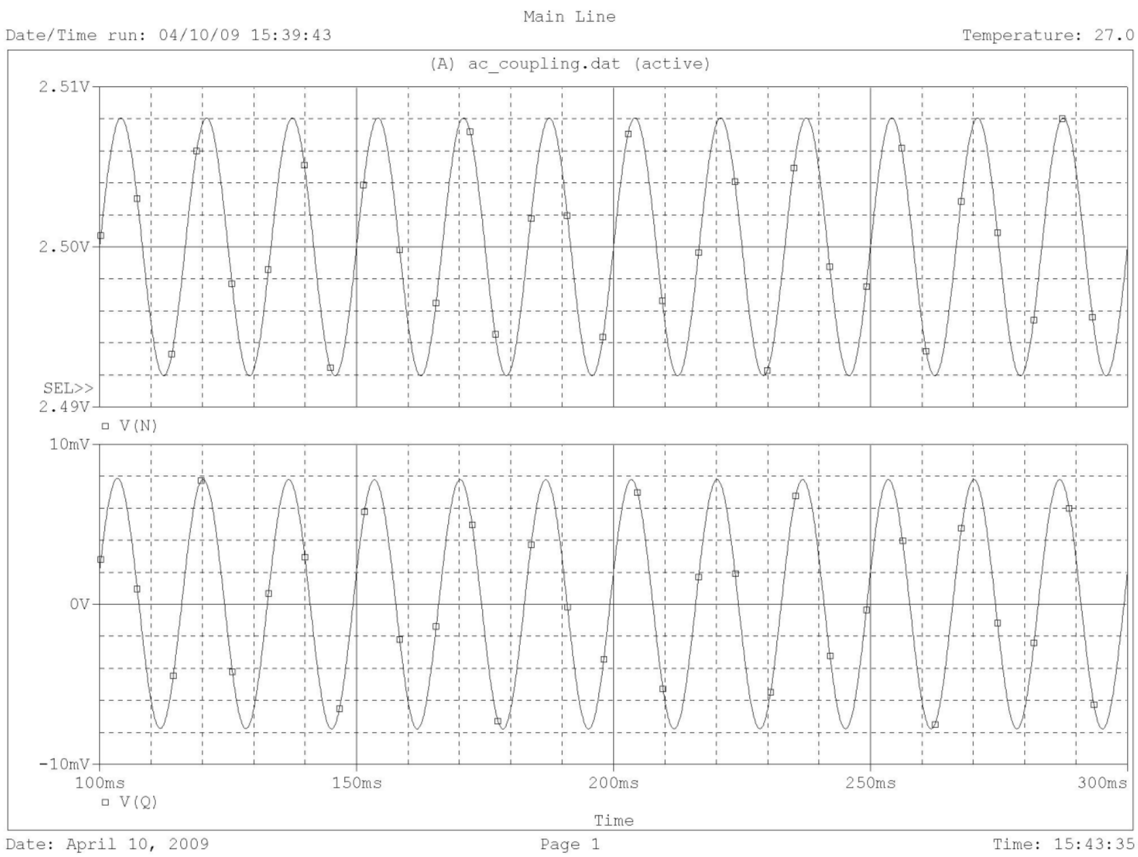


Figure 11 - Simulation for AC Coupling

Amplifier

After the output of the current sensor is conditioned by the AC coupling circuit, the signal has to be amplified in order to achieve enough sensitivity for comparison. To amplify the signal, we used an op-amp with non-inverting amplifier configuration. Figure 12 illustrates the non-inverting operational amplifier configuration used to increase the magnitude of the output from AC coupling circuit. In the non-inverting configuration R12 and R13 (on Figure 12) acts as a voltage divider. In order to keep the two input voltages of the amplifier the same, the output voltage at node 6 with reference to ground must be set to make the feedback voltage to the negative input match the positive input.

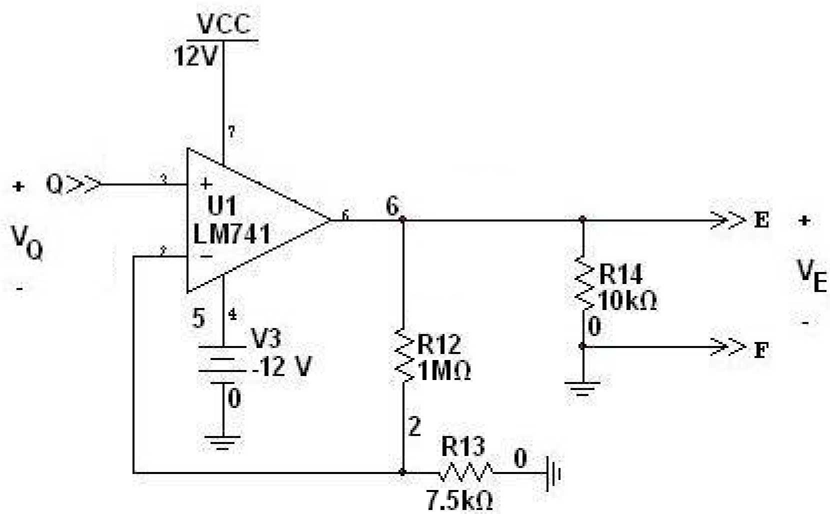


Figure 12 – Amplifier

This configuration follows the equation:

$$V_{OUT} = \frac{R13 + R12}{R13} V_{IN}$$

For our design,

Regular operation: $V_{OUT} = \frac{7.5k+1M}{7.5k} V_{IN} = 134.33 \times 8.06mV = 1.08V$

During fault: $V_{OUT} = \frac{7.5k+1M}{7.5k} V_{IN} = 134.33 \times 33.37mV = 4.48V$

To see if the amplifier design will work, a simulation of the circuit in Multisim was done and can be seen in the appendix. The waveforms are taken at V_E on Figure 12. However, the results were not similar to the calculations. These resulting waveforms can be seen on Figure 13 and Figure 14. By looking at the magnitude of the waveforms, it can be seen that the amplifier achieved its objective. Therefore, one can deduce that the difference between the calculations and the simulations is because of ignoring the effects of AC coupling.

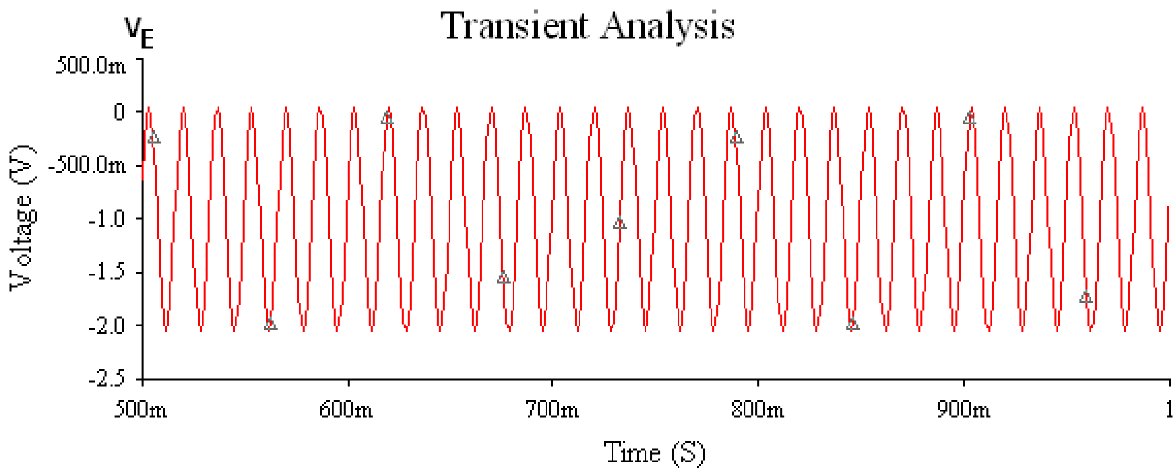


Figure 13 - Measuring current output simulation during regular operation

Comparing the scales of the waveforms in Figure 13 and Figure 14, it is obvious how the measured current increases during fault.

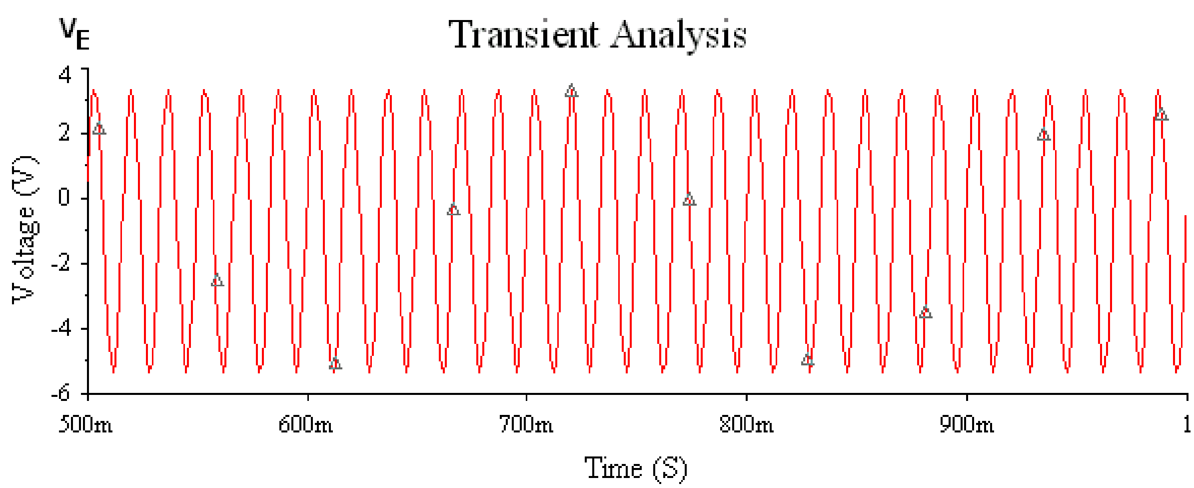


Figure 14 - Measuring current output simulation during fault

The schematic in Figure 15 shows the complete measuring current section of the circuit breaker design. The off page connections A and B are connected to the main line and the output V_E is used in the next section which is current comparison. As it is calculated step by step in the earlier sections, the measuring current circuit is supposed to output 1.08V during regular operation and 4.48V during fault.

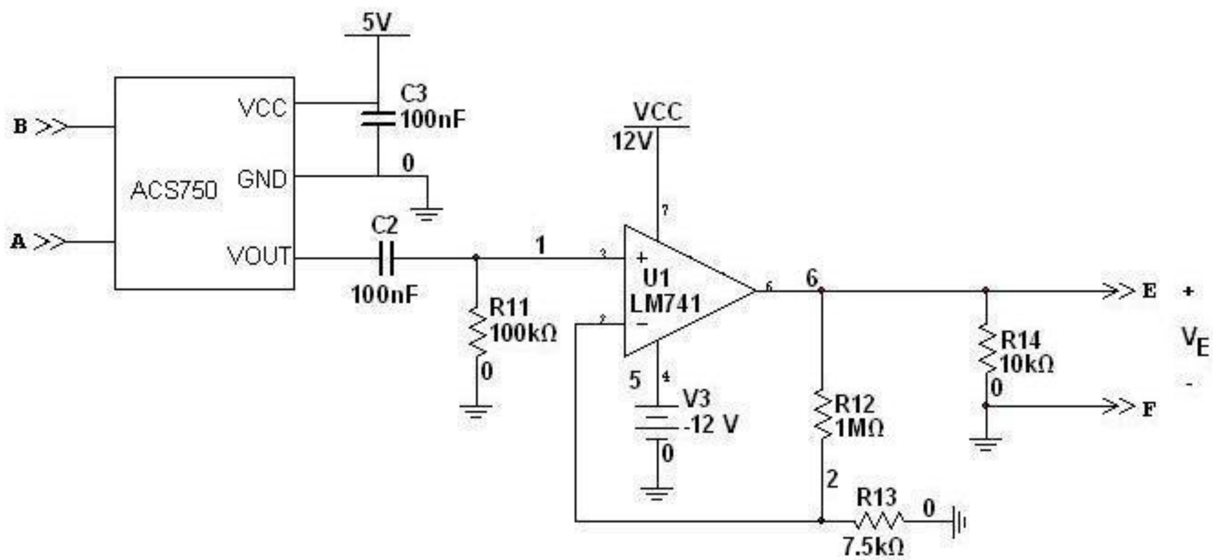


Figure 15 - Measuring Current

4.2.2.2. Current Comparison

The second part of the circuit breaker is called current comparison. The objective of this part is to decide if the current on the main line is under a desirable level and disconnect the main line if otherwise. In order to accomplish this objective, an AC-DC conversion circuit, a voltage comparator and a circuit that feedbacks the output of the comparator to the main line is designed.

AC-DC Conversion

The AC-DC conversion part takes the output V_E of the measuring current part as an input and converts it to a DC signal which can be used by a comparator. The voltage V_E goes through a rectifier labeled D1 and is then filtered by a filter producing a DC voltage.

The first step taken in converting the voltage V_E from AC to DC, is rectifying it. In order to rectifier V_E a RB154 bridge rectifier was used, which can be seen in Figure 16. The RB154 has a max input voltage of 280 volts (rms) and maximum output current of 1.5A

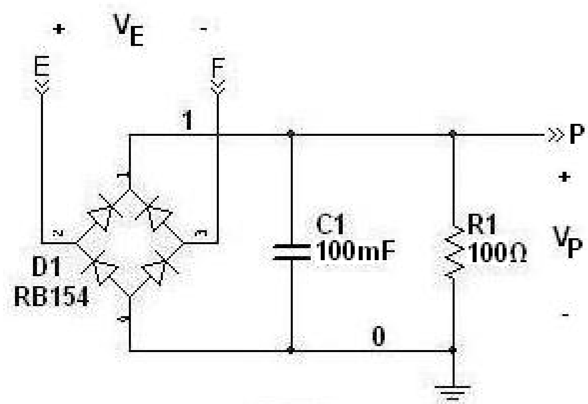


Figure 16 - AC-DC Conversion Circuit

After the V_E is rectified, it is then passed through a low pass filter which comprised of a 100mF capacitor C1 and a 100Ω resistor R1.

When the circuit seen in Figure 16 was simulated using Multisim under regular operating conditions, V_P appears to be negative at all times at very low voltages since the current on the main line is very small. The results of this simulation can be seen in Figure 17.

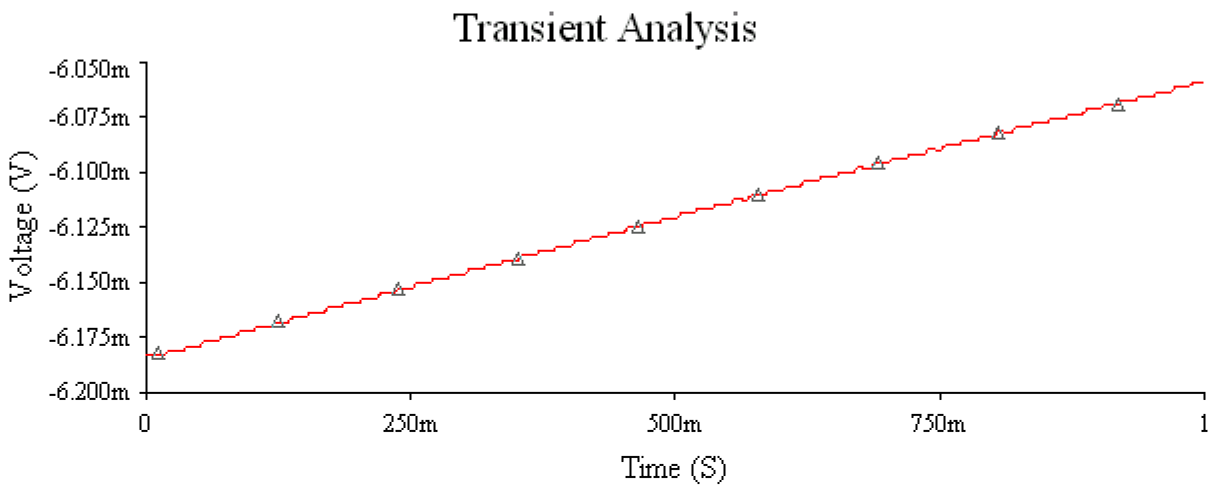


Figure 17 - AC-DC Conversion Output during regular operation

When the fault appears (when fault condition values are used in the simulation) the resulting waveform of V_P is shown in Figure 18. As it can be seen, the voltage is at significantly higher levels compared to the previous case in Figure 17. While the shape of the waveform in Figure 18 is exactly how it would be expected from an AC-DC conversion circuit, Figure 17 has a linear shape due to the small values at V_E.

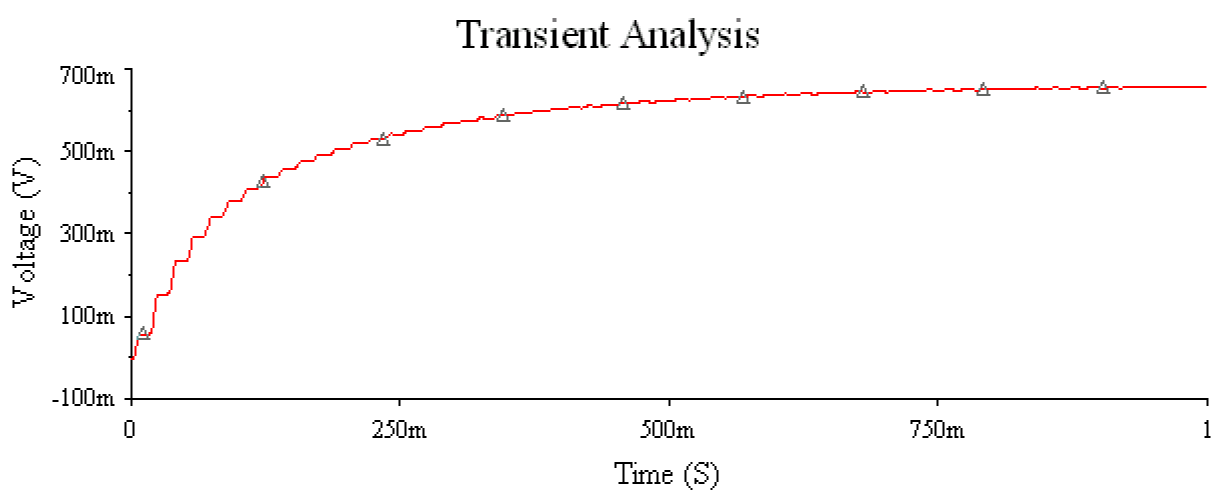


Figure 18 - AC-DC Conversion Output during fault

Voltage Comparator

After the voltage from the main line is rectified and filtered producing a DC voltage, it is compared with a threshold voltage in order to check if there is a fault or not. The threshold voltage used for this circuit is:

$$12V \times \frac{1k}{51k + 1k} = 230.77mV$$

The schematic for the voltage comparator circuit is shown in Figure 19. The circuit utilizes the general operational amplifier LM741 which was configured as a comparator. At point P the voltage that we want to compare enters the op amp which compares it to the threshold voltage of 230mV, if the voltage is higher than the threshold then the op amp produces a positive value and a negative value when the voltage V_p is lower than the threshold.

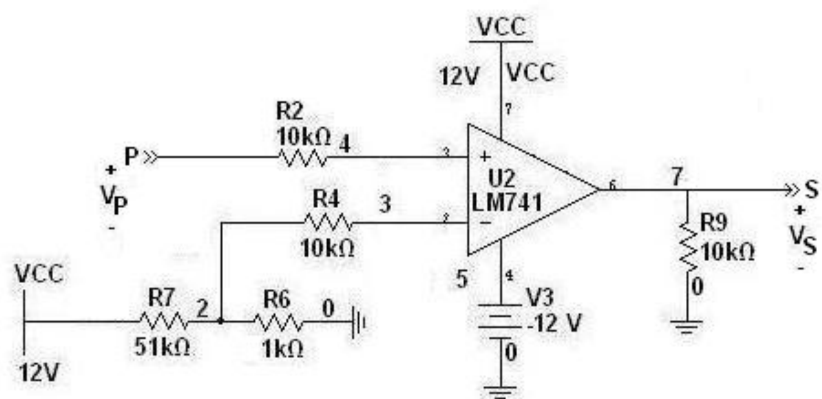


Figure 19 - Voltage Comparison Circuit

When the circuit in Figure 19 was simulated using Multisim, the output when the voltage V_p is lower than the threshold voltage can be seen in Figure 20. The graph in Figure 20 shows that the voltage is negative when the voltage is below the threshold. The graph in Figure 21 represents the output voltage of the voltage comparator when the V_p is higher than the threshold, the voltage in the graph is shown to be positive. Based on the results of the simulation, it was deduced that the design that was used for the voltage comparator in Figure 19 will work.

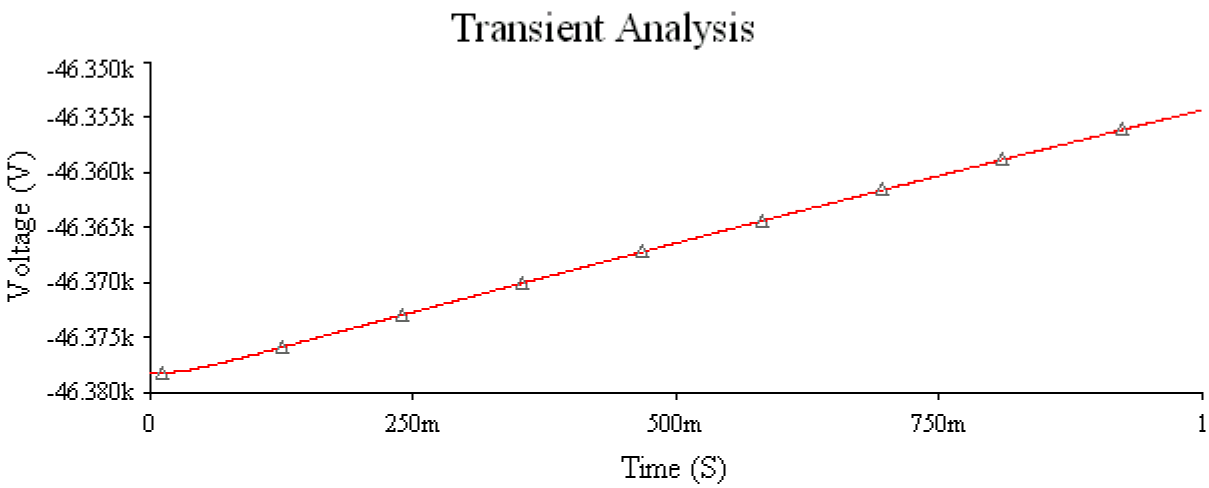


Figure 20 - Comparator output simulation during regular operation

As expected, the output of the op-amp becomes positive during a fault and it stays negative otherwise.

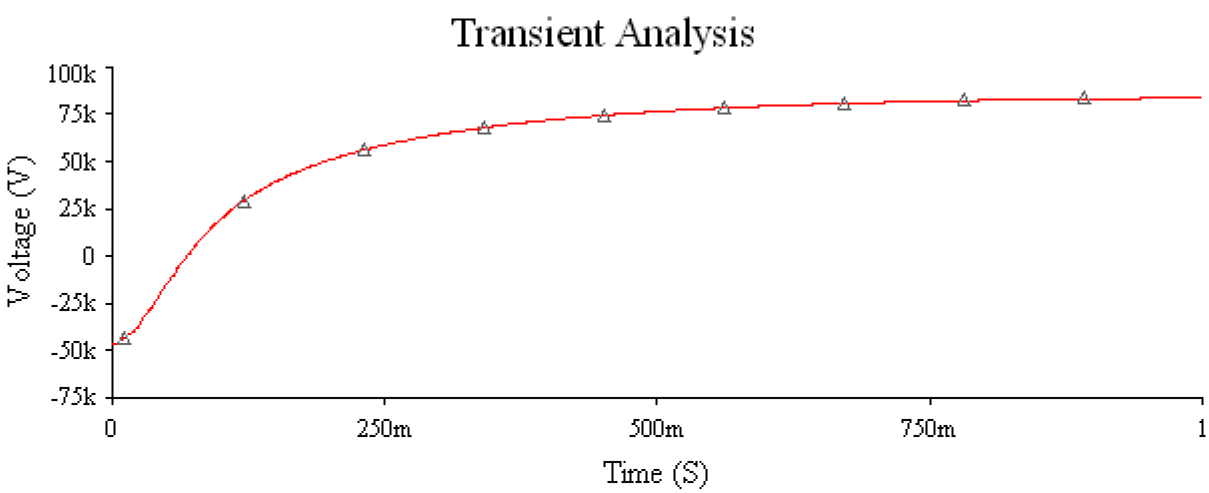


Figure 21 - Comparator output simulation during fault

Feedback to Main Line and 2nd Control System

After the current from the main is measured and compared, a feedback system was designed in order to pass the results that followed after the comparison to the main line. The circuit that was designed can be seen in Figure 23. The voltage from the voltage comparator block V_s enters the point S of the Feedback circuit. It first enters a device called a SCR labeled as D2 in Figure 23. A SCR (Silicon Controlled Rectifier) is a type of thyristor that controls current; it acts like a bistable switch when the gate receives a current pulse. The SCR will continue to conduct until the voltage across it is not reverse, the symbol used for a SCR can be seen in Figure 22.

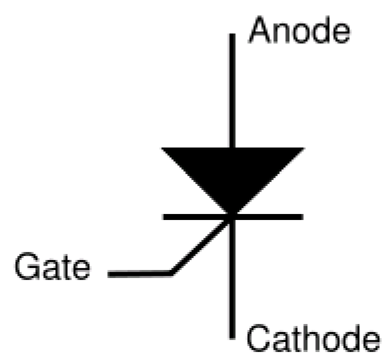


Figure 22-Circuit Symbol for a SCR

The particular SCR that was used in the circuit was the S8008L, which requires a gate voltage of 12v to be switched on. Therefore when there is a fault and the voltage coming from the voltage comparator block labeled V_s will be both positive and more than sufficient to turn the SCR on as shown in the graph in Figure 21. When the SCR is turned on the relay labeled K2 in Figure 23 will be energized causing the normally closed switch between points C and M to open which disconnects the main line. The normally open switch between points L and M will be closed connecting the circuit to the 2nd control circuit which will be discussed in a later section. The connection to the 1st control circuit between points H and G will be disconnected due to the current flowing through the normally closed relay and this will also be discussed in more details in a later section. The current through the Feedback circuit will continue to flow as long as there is voltage coming from the voltage comparator circuit.

When the main line is operating under normal conditions and then the voltage coming from the voltage comparator block will be negative as seen in the graph in Figure 20, this voltage is not sufficient to turn the SCR on and hence current does not flow through the feedback circuit leaving it in its initial state.

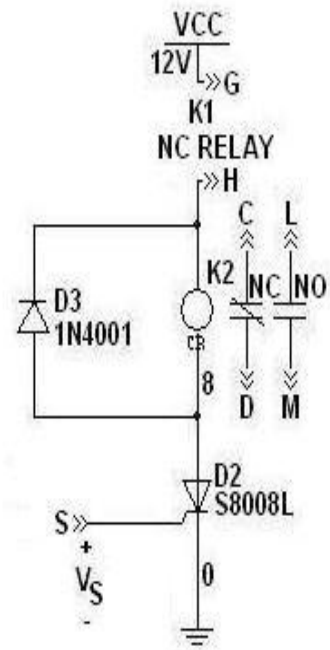


Figure 23 - Feedback to main line and second control system

Figure 24 shown below is a schematic of the entire Current Comparison Circuit. The overall job for this block of the circuit breaker is to compare the current coming from the main and based on whether the current indicates fault conditions or not it will it send feed back to the main line regarding if the main line should remain connected or if it should be disconnected. This block also provides both control circuits with information on the state of the main line (whether it is operating under normal conditions or if there is a fault occurring).

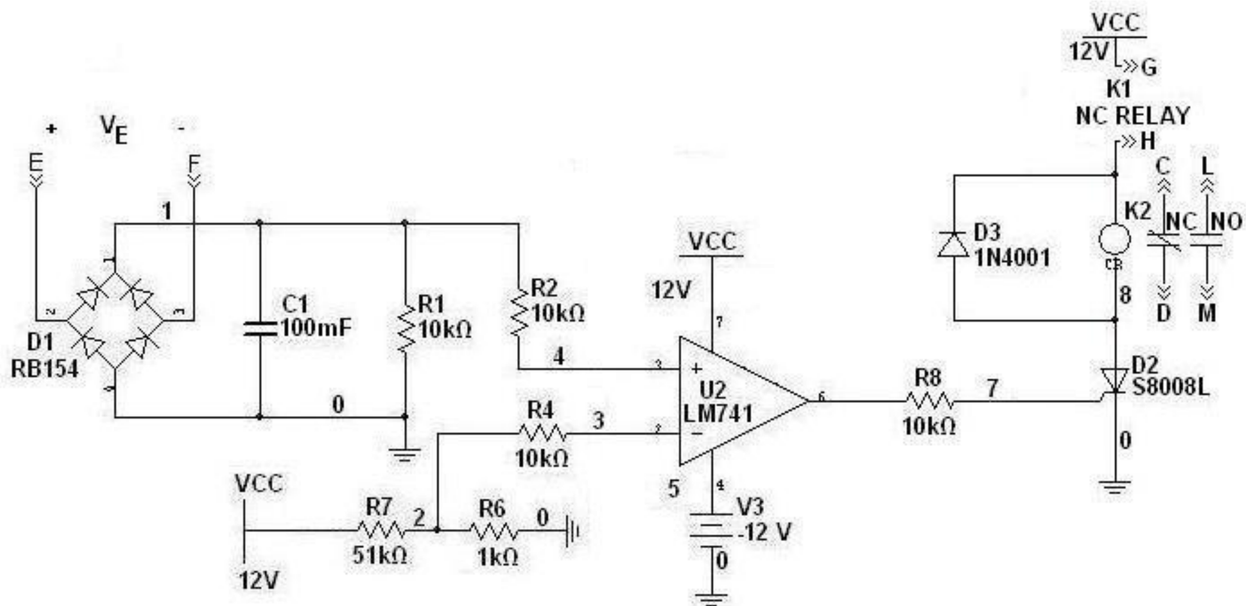


Figure 24 - Current Comparison Circuit

4.2.3. 1st Control Circuit

The next module of the 'smart' recloser breaker is the 1st control system. The system has several different parts namely; the AC-DC Conversion, the Voltage Comparator and the feedback circuit to the main line. Each part is discussed in details in the sections below.

AC-DC Conversion

The main task of the first control circuit is to monitor the voltage in the main line and make sure that the fault is cleared before reclosing the circuit breaker and hence reconnecting the main line. In order to the check if the fault is still present in the main line the control circuit will have to make sure that the voltage is below a threshold voltage and to do this the mainline voltage will have to be converted from AC voltage to DC voltage. The voltage from the main line V_R enters the control circuit from points C and D as seen in Figure 25, the resistor R5 and R8 were placed in the circuit in order to prevent a large amount of current to flow to the circuit. Then the current is rectified by the bridge rectifier D4 in Figure

25, after it is rectified the voltage is then filtered using a lower pass filter. The low pass filter is comprised of a 100µF capacitor C4 and a 10KΩ resistor R16 seen in Figure 25 below.

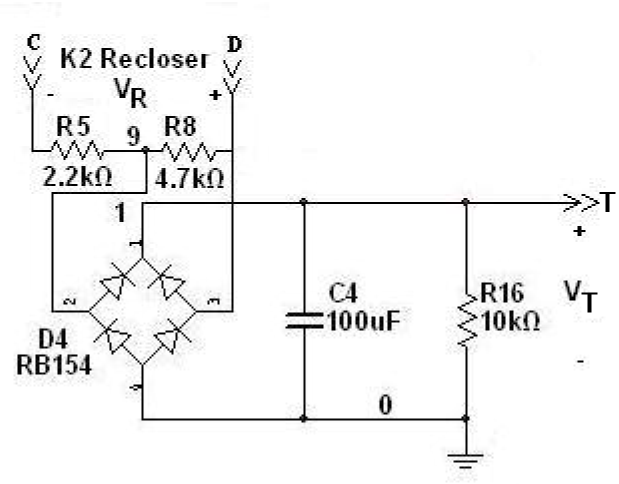


Figure 25 - AC-DC Conversion Circuit

The resulting voltage V_T after conversion, during a fault occurrence can be seen in Figure 26, the graph shows a steady DC voltage at approximately 7V.

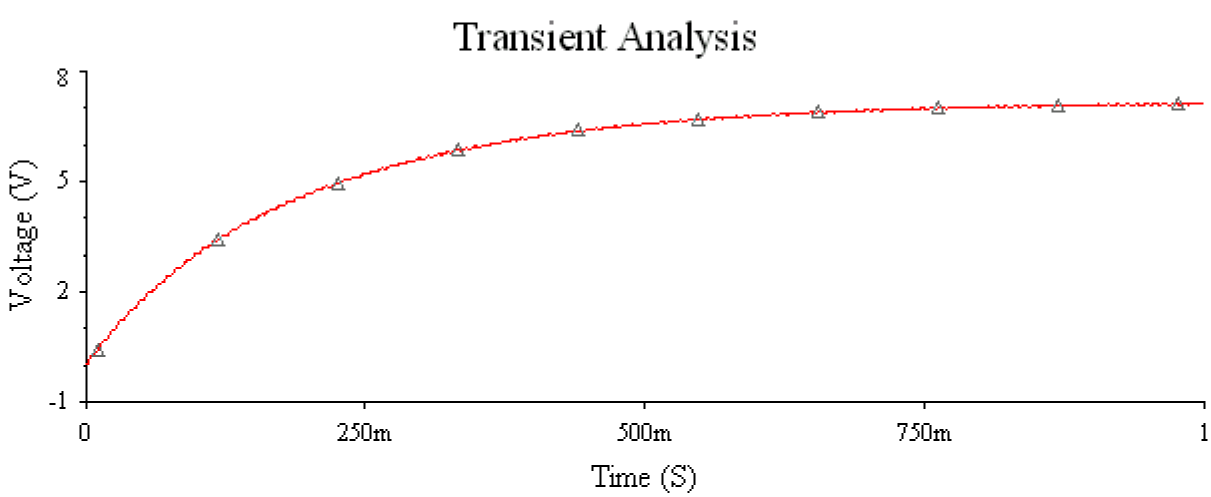


Figure 26 - AC-DC Conversion Output during fault

Voltage Comparator

After the voltage is rectified it is now ready to be compared to the threshold voltage. To compare the voltage a general purpose operational amplifier U3 in Figure 27 was configured to be a voltage comparator. A threshold voltage of 12 V was used as the voltage across the main line is approximately 7V and should not exceed 12V under normal operating conditions. Therefore if the voltage connected the inverting input is higher that the threshold voltage to the non-inverting input the op-amp will have an output that is low and if it is lower than the threshold voltage a high output is produced.

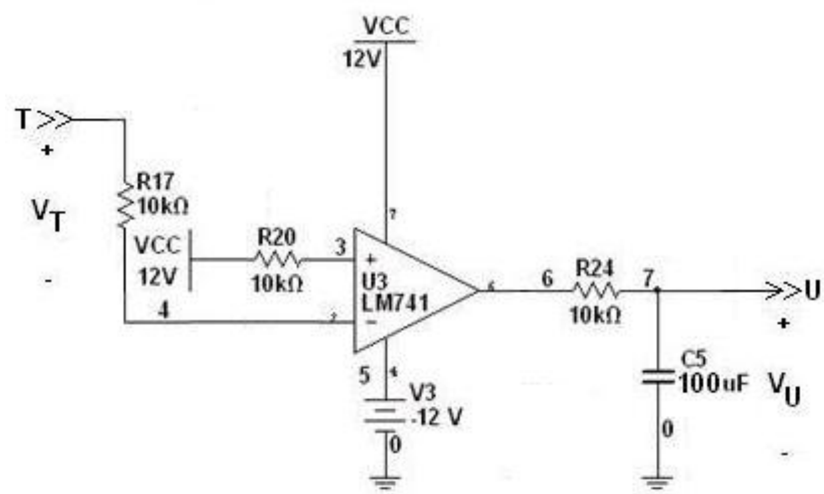


Figure 27 – Voltage Comparator of the First Control System

Feedback to Circuit Breaker

When the voltage V_U leaves the Voltage Comparator circuit shown in Figure 27 it then enters the a feedback circuit shown in Figure 28. The purpose of the feedback circuit is to relay the information received from the comparison circuit to the mainline which then dictates whether it is reconnected or not. When V_u enters the point U in the circuit shown in Figure 28 it enters the base of a NPN Bipolar Junction Transistor that acts like a switch. A BJT is a three terminal semiconductor transistor that is commonly used for amplification and switching applications.

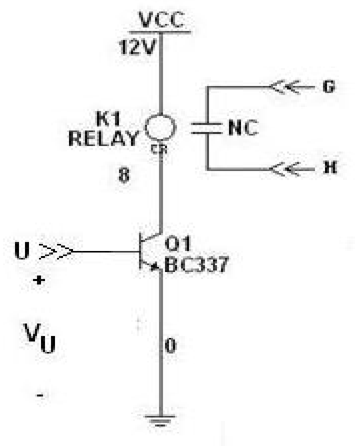


Figure 28 – Feedback to Circuit Breaker Circuit

Therefore when the voltage coming from the Voltage Comparator block is high the BJT is turned on and the circuit starts conducting energizing the relay K1 which opens the normally closed connection of the relay contacts. When the contacts of the relay K1 is opened it will interrupt the current going through the feedback portion of the circuit breaker causing the normally closed contacts of the relay K2 shown in Figure 24 to close and reconnecting the main line. If the voltage from the voltage comparator block is low the BJT will not turn on resulting in the main line remaining disconnected.

Figure 29 below shows the complete schematic for the first control circuit starting from the connection to the main line until the feedback to the circuit breaker system.

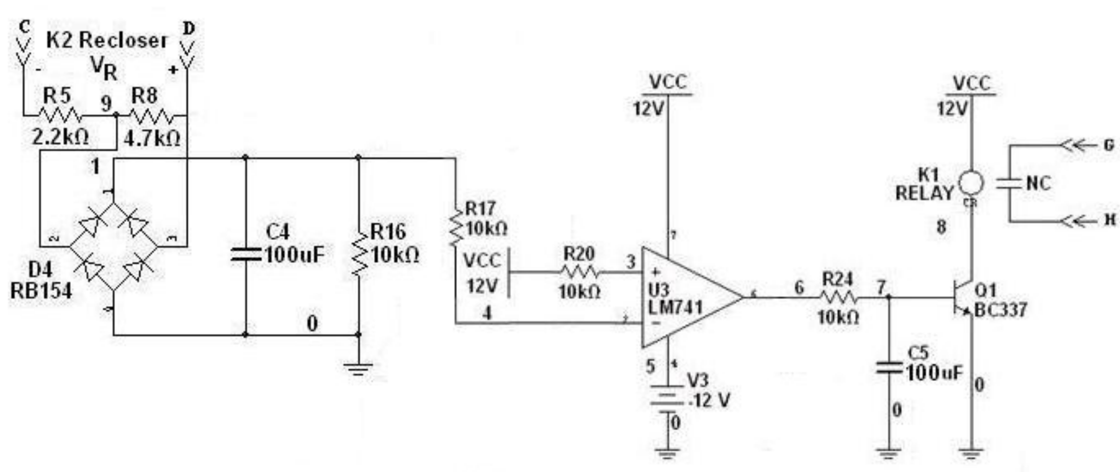


Figure 29 - First Control System

4.2.4. 2nd Control Circuit

The Second Control System was designed to decide if a fault is persistent. It basically counts the times a fault occurs, and disconnects the main line after three faults. Then a technician is needed to reset the system. The second control system consists of three parts which are a switch debouncer, a counter and a feedback to the main line.

Switch Debouncing

The counter is designed to count the number of times that a fault occurs; therefore it needs to use the input from the circuit breaker. However, since that input is from the switching of a mechanical relay, it will not provide a defined edge. When this signal is used in a digital counter as the one in the "smart" recloser circuit breaker, the counter will count multiple times when it was expected to count only once. To avoid this situation, a circuit called switch debouncer is needed to condition the output from the K2 relay at the end of the circuit breaker system. The schematic of this circuit is illustrated in Figure 30. When the contacts of K2 relay which are labeled L and M are disconnected (during regular operation) capacitor C6 will charge via resistor R25. Voltage across C6 will reach VCC in time and the Schmitt Trigger's Nand gate U4 will output a logic low signal. When L and M get connected during a fault, the capacitor C6 will discharge reaching 0V. Therefore U4 will output a logic high signal.

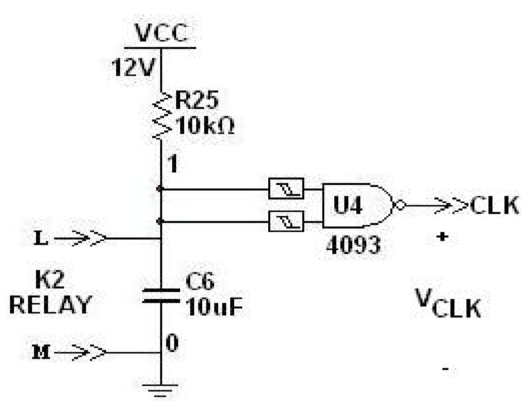


Figure 30 - Switch Debouncer Circuit

Counter

This part uses the output from the switch debouncer circuit and counts the times that a fault occurs. For this purpose a 74161 synchronous 4-bit counter with standard reset is used. Figure 31 shows the 74161 IC and how the connections are made. The count advances as the clock input becomes high (on the rising edge). The 4-bit counter is able to count from 0 to 15, but since this system was designed to allow the fault to occur only three times, an AND gate is connected that uses the two least significant bits as inputs. When the counter counts up to 3, the outputs at Q_A and Q_B both become 1 which sends a logic high signal to V_X. For normal operation, the reset input is connected to VCC through a switch. The switch is placed so that when there is a persistent fault and a technician corrects it, he can reset the counter and reconnect the main line.

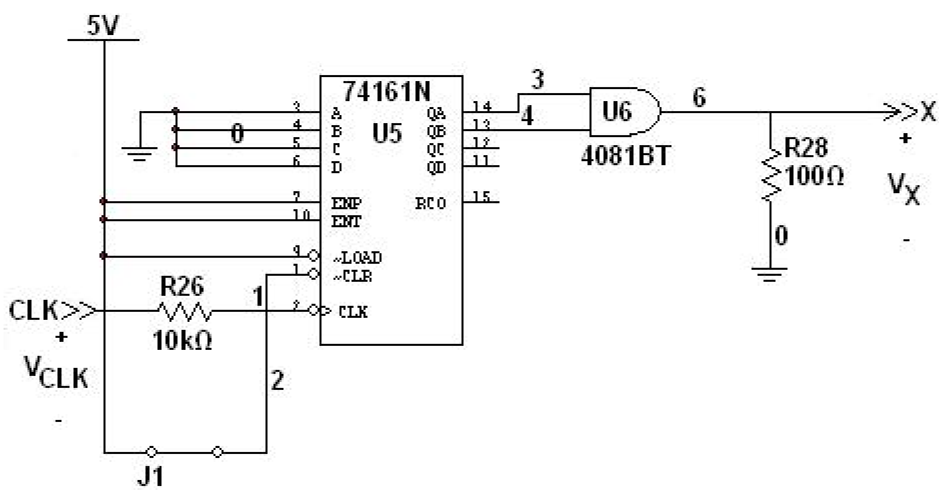


Figure 31 – Counter

In order to prove the operation of the counter, a simulation in Multisim was used. The simulation circuit can be found in the Appendix and the results are displayed in Figure 32. For simulation purposes, a pulse signal was used as the input to the clock. The simulation results show how the outputs change at the two least significant bits (Q_A and Q_B) and how the output V_X changes accordingly.

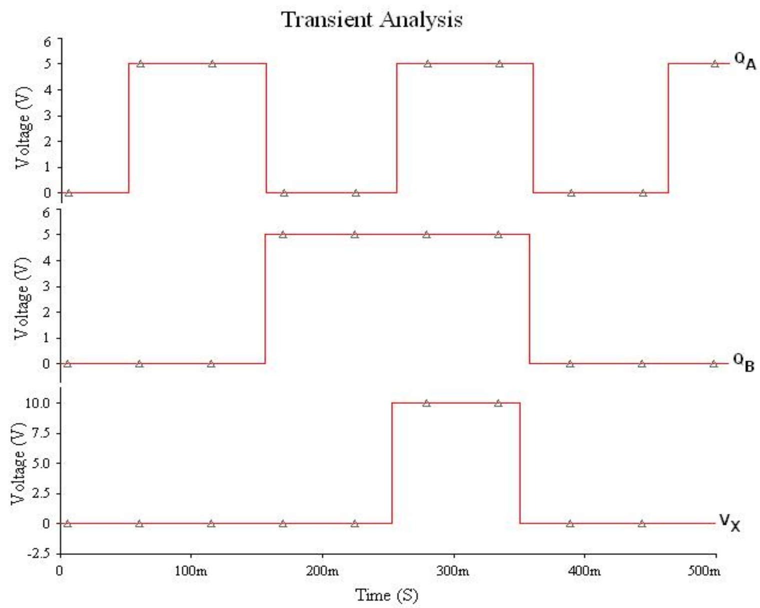


Figure 32 - Counter Simulation

Feedback from Counter

After the counter counts up to three and produces a logic high signal at V_X, a system was needed to use that input to disconnect the main line until a technician arrives at the site. This system is shown in Figure 33. It consists of a transistor (Q2) that conducts when the V_X signal becomes high and a relay (K3) that gets energized when the transistor starts conducting. When the relay gets energized, the normally closed connections to the main line which are labeled Y and Z get disconnected.

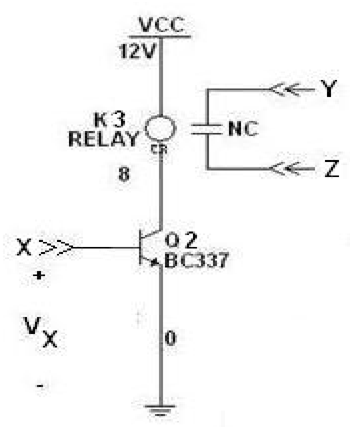


Figure 33 - Feedback from Counter

Figure 34 illustrates the complete second control system starting from the input from K2 relay until the output at the relay K3.

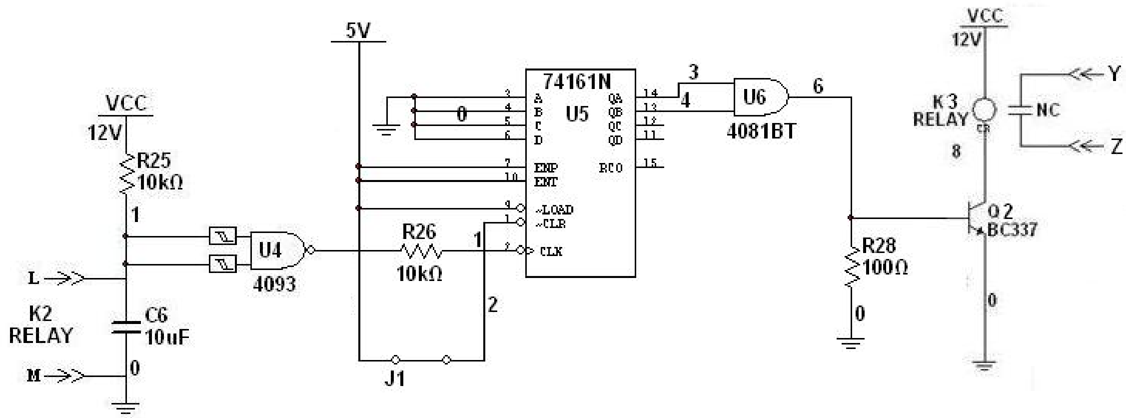


Figure 34 - Second Control System

5. Results

This section of the report discusses the resulting computer simulation of the whole smart circuit breaker system. The circuitry that is used for this section is not exactly the same as the implementation design, but it is a representation of it in PSPICE. The code that is used can be found in the Appendix as a whole, but for detailed description, the system will be broken into parts for ease of understanding.

The first circuit is the representation of the main line. The schematic of the simulation of this part can be seen in Figure 35.

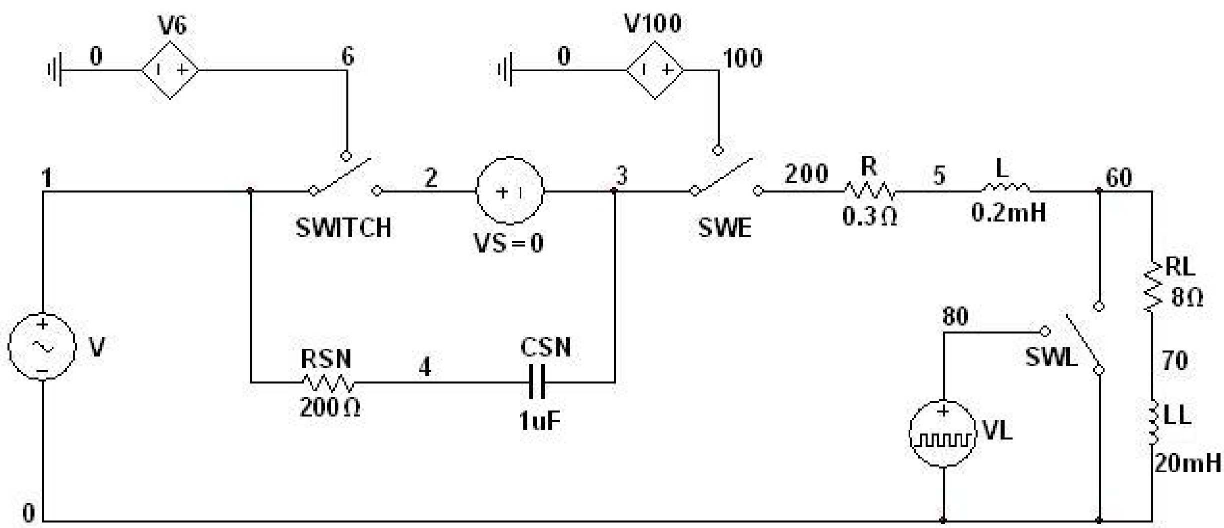


Figure 35 - PSPICE Simulation Circuit of Main Line

The voltage source "V" is an AC source at 60Hz with 100V peak. The circuit has 2 resistors (R and RL) and 2 inductors (L and LL). In order to create a fault, the voltage controlled switch "SWL" gets connected by the pulse that is created by "VL" at node 80. The pulse has 75ms delay and in order to keep the fault consistent it has a high output of 10V throughout its period which is 600ms. Figure 36 shows the waveforms of the voltage at node 80 which represents when the fault occurs and the current through the resistor "R". It can be clearly seen that the fault creates a significant increase in the current through the resistor. In order to generate this simulation, the switches that disconnect the main line has been neglected.

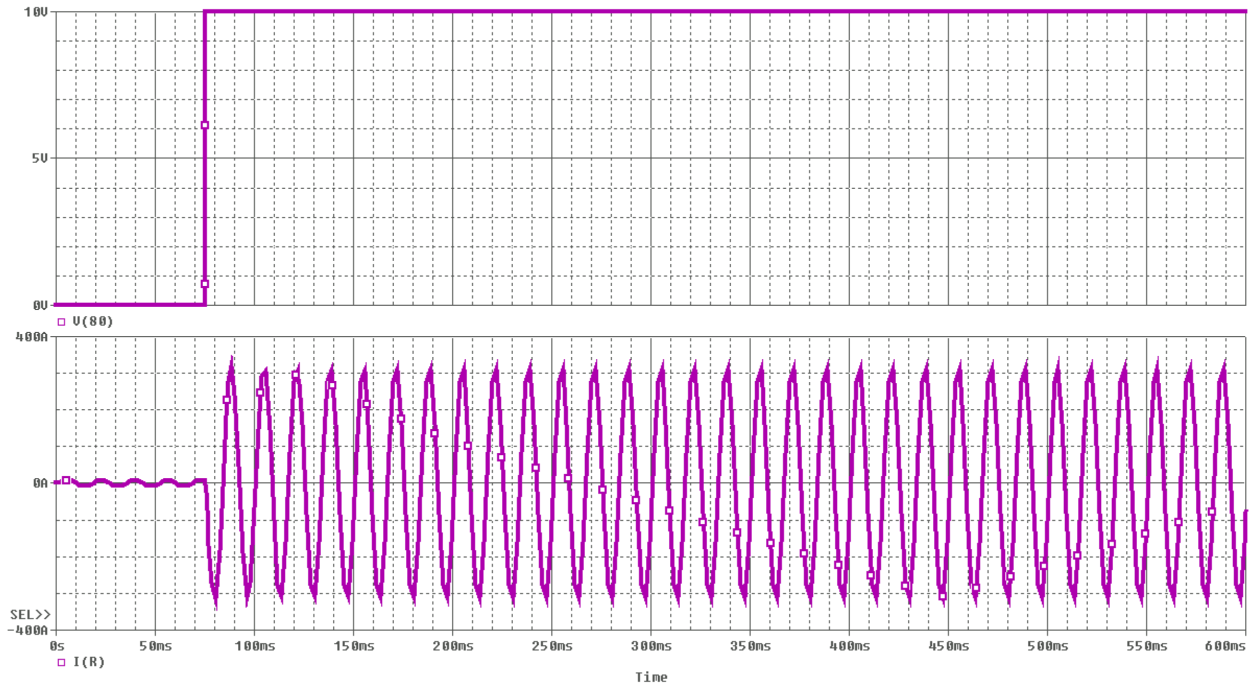


Figure 36 - Current through the Resistor "R" During Regular Operation and Fault

The representation of the current measuring circuit has been done by using a voltage source that equals to the absolute value of the current through the main line. The voltage source "EC" between nodes A and 0 has been integrated by the resistor REC and capacitor CEC to achieve the DC voltage representation of the current. The schematic of this part can be seen in Figure 37.

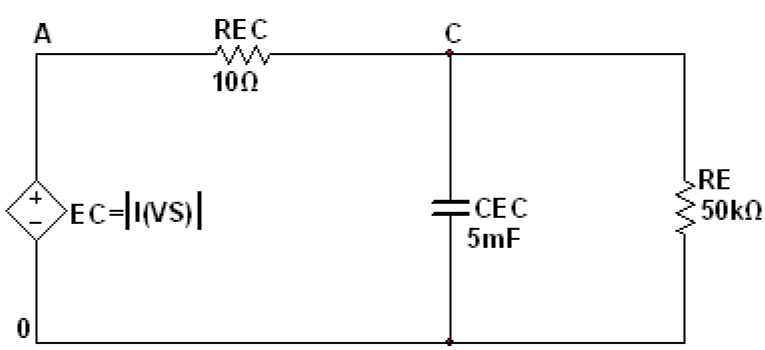


Figure 37 - PSPICE Simulation Circuit of Current Measurement Part.

Figure 38 illustrates V (80) which represents the fault and how V(C) changes accordingly. V(C) is the voltage that is outputted when the voltage that represents the current on the main line is rectified and filtered. As expected V(C) increases significantly when the fault occurs.

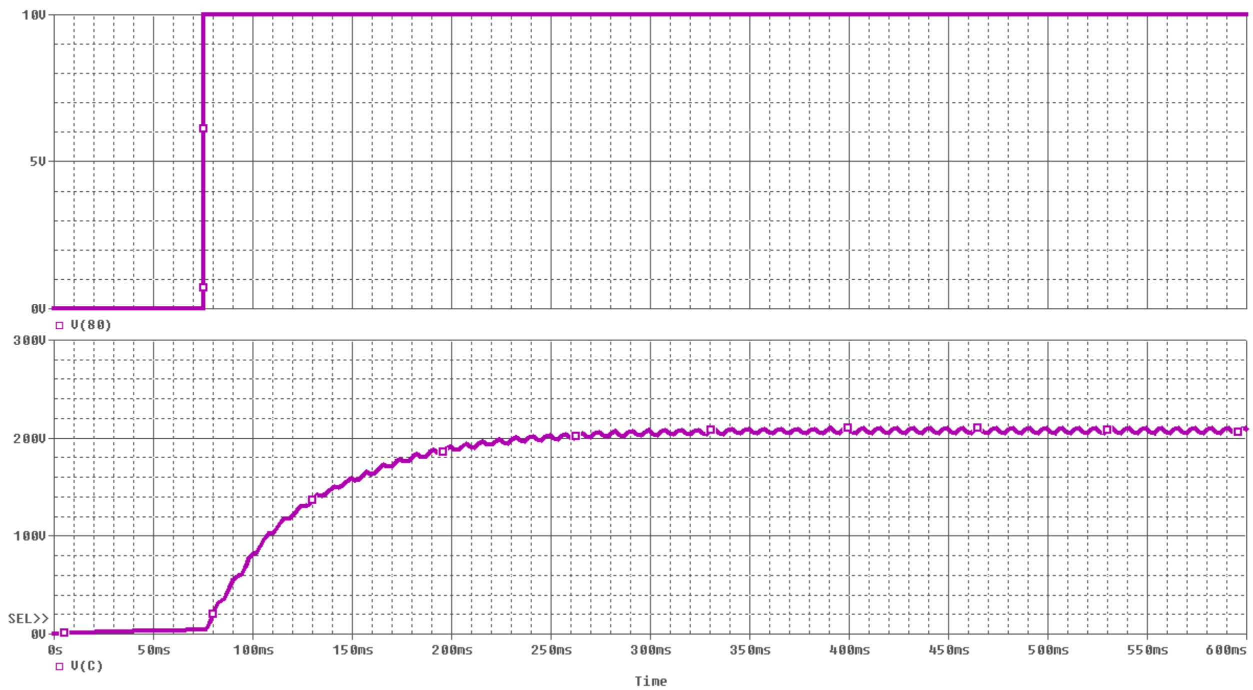


Figure 38 - Voltage across Node C and Ground

In the next part, V(C) is used in a comparison system. In order to simulate a comparator, the voltage source “ET” which is equal to the voltage across nodes C and 0, is subtracted from a constant 10V voltage source labeled as “VGATE”. Figure 39 shows the circuit that represents a voltage comparator.

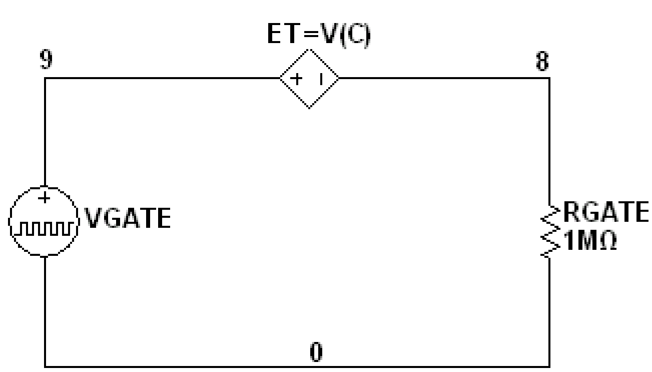


Figure 39 - PSPICE Simulation Circuit of Current Comparison Part

Figure 40 shows the simulated waveforms of this part. V(C) as can be remembered from the previous set of waveforms increases when the fault occurs. Meanwhile, V(8) decreases when the fault occurs since it equals V(C) subtracted from "VGATE".

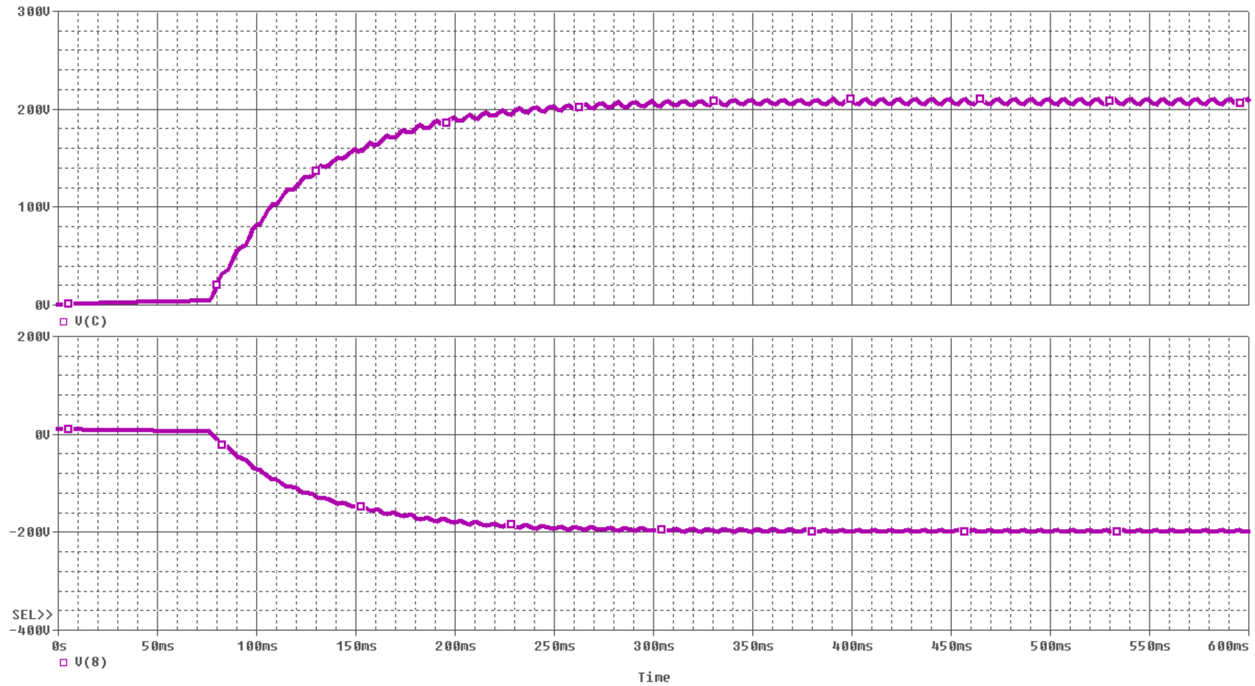


Figure 40 - Voltages across Node C and Ground, Node 8 and Ground

After the comparison was done, a system was needed to use this comparison as an input and disconnect the main line if necessary. The switch that uses the output from this part can be seen in Figure 35. It is labeled as "SWITCH". It is a voltage controlled switch that is controlled by the voltage across nodes 6 and 0. It is closed when that voltage is high and open otherwise. Figure 41 shows the circuit that was used to represent the feedback from the comparator to the main line.

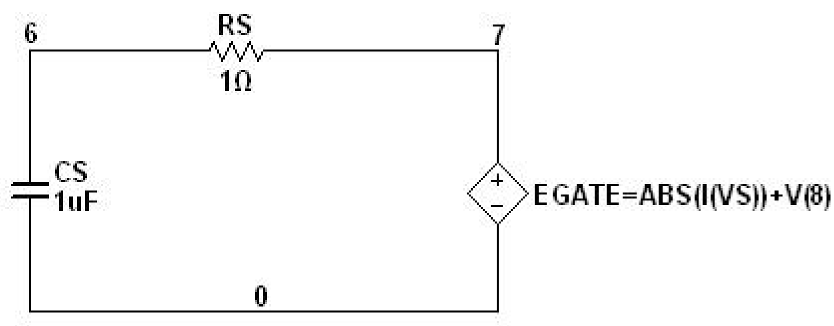


Figure 41 - PSPICE Simulation Circuit of Feedback to Main Line

The voltage source labeled "EGATE" is equal to absolute value of the current on the main line plus the voltage across nodes 8 and 0 (V(8)). The value of "EGATE" is entered in the PSPICE code as a table which follows the graph in Figure 42. In short, V (7) will be 1V when (ABS (I (VS)) +V (8)) is positive and 0V otherwise. This behavior provides the voltage controlled switch labeled "SWITCH" with a clean pulse to operate by. In the beginning, the current on the line will be 0, but V(8) will be 10V since there is no current and 0V on "ET" that can be subtracted from "VGATE". In this case, the switch will be connected. When a fault occurs, the current on the main line increases, but so does V(C). When V(C) increases, V(8) decreases significantly and "EGATE" becomes negative which creates 0V across nodes 7 and 0. This causes the disconnection of the circuit.

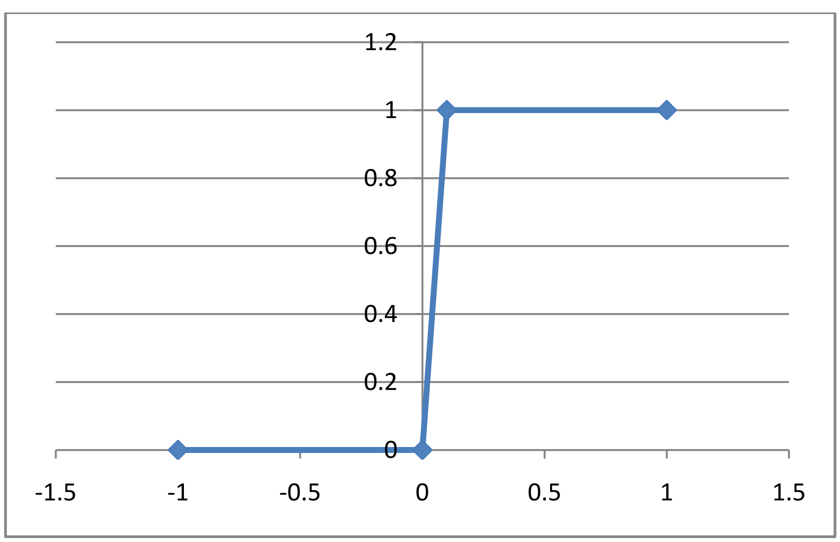


Figure 42 - Behavior of "EGATE"

When the main line gets disconnected, the current decreases to 0A. When current decreases, V(C) decreases accordingly, which increases V(8). The increase in V(8) and the decrease in the current cause the voltage value of "EGATE" to reach above 0 again. In this case, from the graph in Figure 42, V (7) becomes 1 and it tries to reconnect the circuit. If the fault is persistent, the circuit goes back to the disconnection state. **Error! Reference source not found.** displays the behavior of the circuit during a

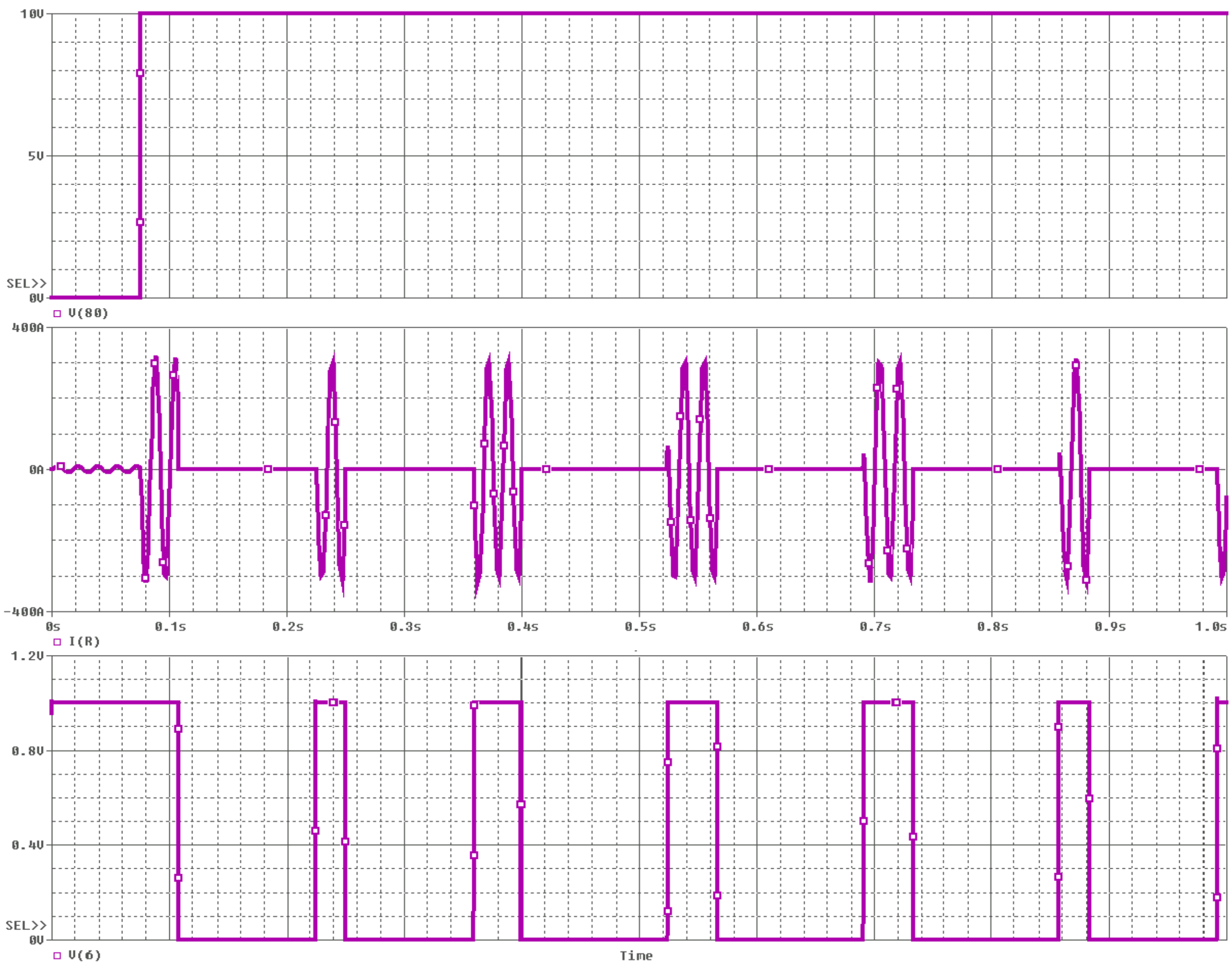


Figure 43 - V(80), Fault Creation - I(R), Current on the Main Line - V(6), Voltage across Nodes 6 and 0 that controls "SWITCH"

fault. As we can see, the current on the main line increases as the fault occurs. Then the main line gets disconnected. It gets connected again due to the voltage across nodes 6 and 0 which closes the "SWITCH". Since the fault is persistent, the main line gets disconnected again and this connection – disconnection can keep on going forever. In order to prevent this, the next part is the representation of the counter circuit on PSPICE which hard disconnects the main line after the third fault. Figure 44 illustrates the circuit that is used to invert V (7). The voltage source labeled “Ecount” is connected in opposite direction and V(10) across nodes 10 and 0 appears to be the inverse of V(7). This is done to achieve the rising edges at each fault. In other words, V (10) is normally low and it becomes high when there is a fault.

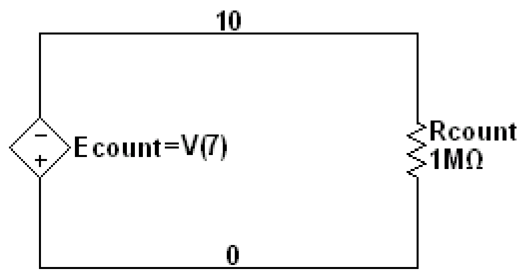


Figure 44 - Inversion of V(7)

The next part of the system is the representation of the counter. An indirect path is taken to simulate the counter. V(10), which represents the clock input to a counter, is used as a constant current source. That constant current source, which equals V(10), is used to charge the capacitor labeled as “Ccon”. When a constant current source is used to charge a capacitor, the voltage across the capacitor increases linearly. The circuit that is used for this part can be found in Figure 45.

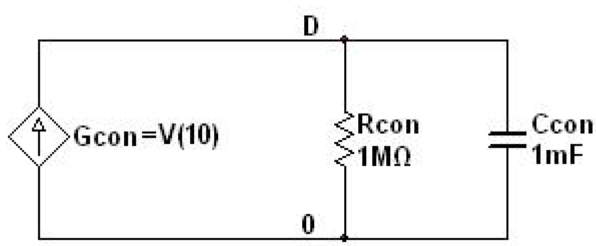


Figure 45 - PSPICE Simulation Circuit of the Counter

Every time the circuit breaker recloses due to a fault, it creates a high voltage at V(10) and by the circuit shown in Figure 45, “Ccon” gets charged more at every reconnection. Figure 46 displays V(10) as the clock input to the counter and V(D) as the charge on the capacitor "Ccon". As it can be seen from the waveforms, V(D) increases linearly at each reconnection.

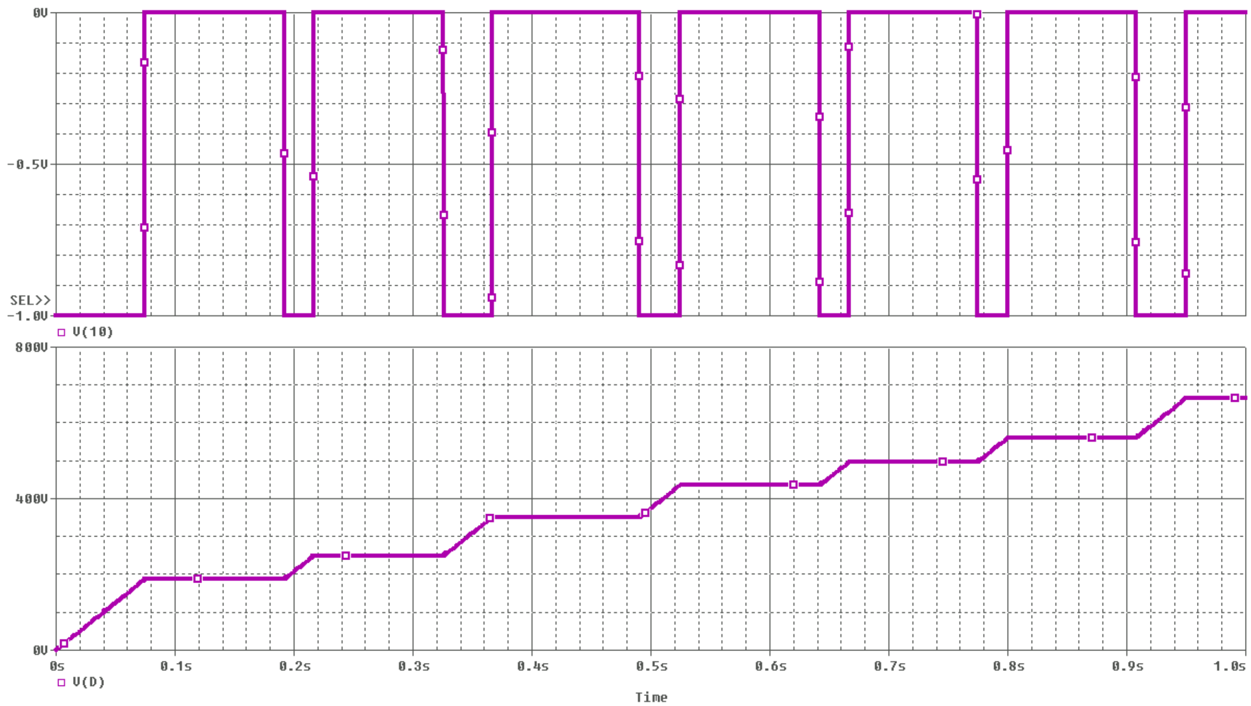


Figure 46 - Reclosing (Clock Input to Counter) and Capacitor Charging (Counter Representation)

In order to complete the representation of the counter system, a circuit is simulated to use V(D) in comparison with a threshold which corresponds to the charge on "Ccon" after third disconnection. That circuit can be seen in Figure 47.

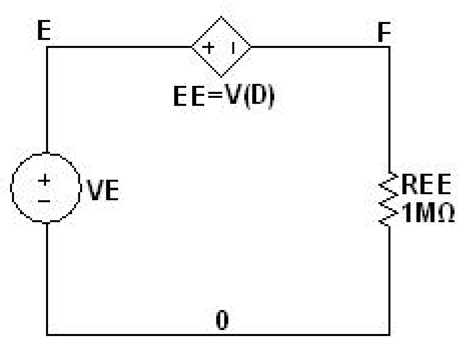


Figure 47 - Pspice Simulation for Recognizing Third Disconnection

This part of the system follows the same method as the circuit in current comparison. V(D) which increases after every disconnection is subtracted from the 415V constant voltage source "VE". Therefore V(F) which was at 415V in the beginning reaches below 0 after 3 disconnections. These waveforms can be seen in Figure 48. After three disconnections, V(D) reaches above V(E) and V(F) becomes negative.

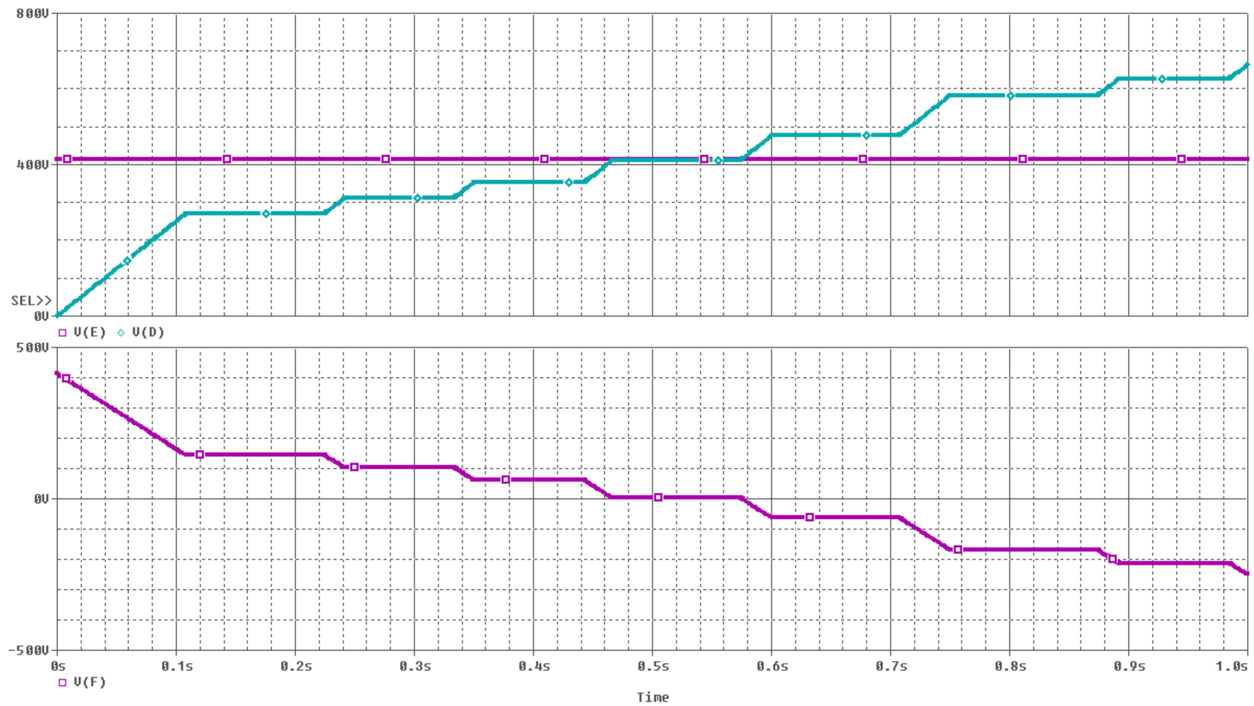


Figure 48 - Voltages V(E), V(D) and V(F) - Notification of the Third Disconnection

V(F) that reaches below 0V after the third disconnection is used in the same way that "EGATE" was used. The voltage source "EconE" equals to V(F) and it also has the characteristic which was shown in Figure 42. V(101) is 1V when V(F) is positive and it becomes 0V when V(F) becomes negative. In summary, V(101) is 1V in the beginning and it drops to 0V after the third disconnection. The circuit that is simulated in this part can be seen in Figure 49.

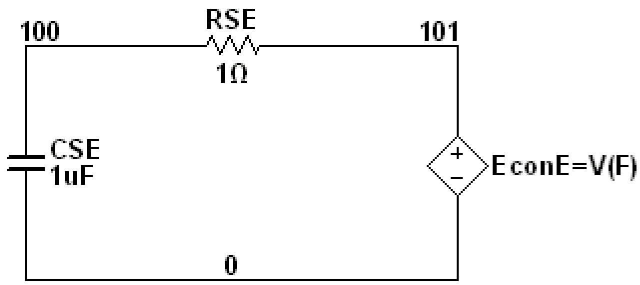


Figure 49 - PSPICE Simulation of the Feedback from the Second Control Circuit to the Main Line

The voltage controlled switch labeled as “SWE” completes the second control system. “SWE” is controlled by V(100). It keeps connected as long as V(100) is 1V and gets disconnected when V(100)drops to 0V.This disconnection occurs after the third reconnection. When “SWE” gets disconnected, it means that the hard disconnection has occurred and the main line keeps disconnected until it is manually reset.

Figure 50 illustrates the final simulation of the whole system. V(80) which represents the fault becomes 10V after 75ms. This means that the fault has occurred and it is persistent. The current on the main line increases. It gets disconnected and tries to reconnect three times. These tries are not successful due to the fact that the fault is still there. After three tries, hard disconnection occurs and the main line keeps disconnected.

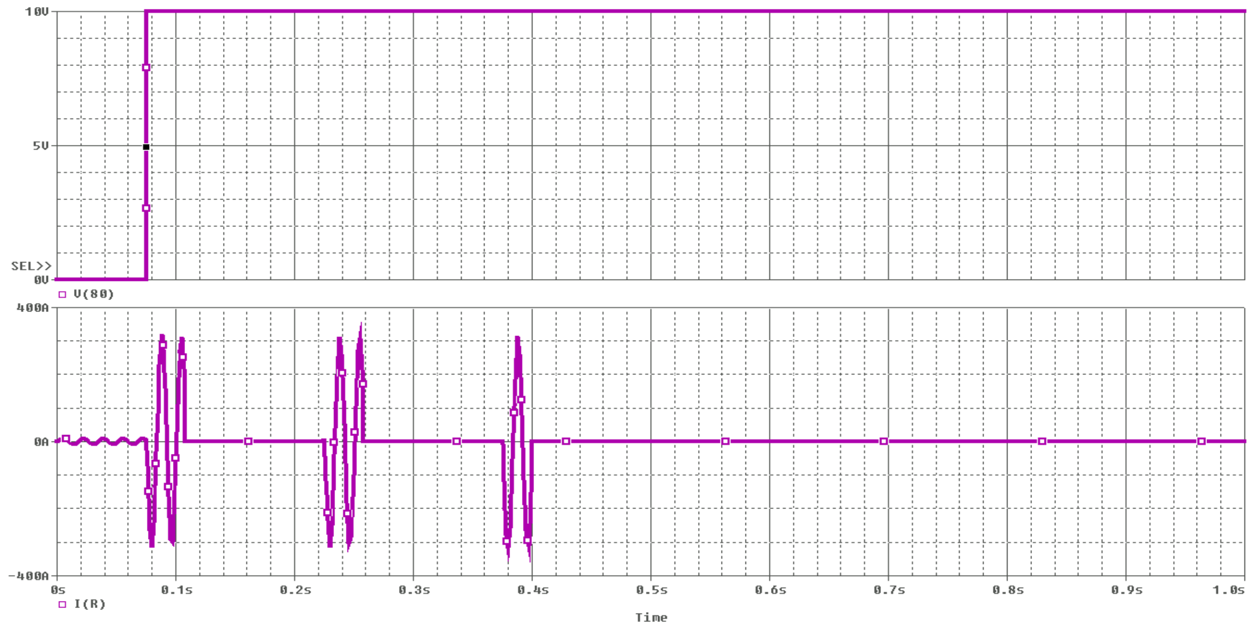


Figure 50 - Final Simulation

Appendix

PSPICE Simulation Codes

Main Line

Main Line Regular Operation

```
V1 1 0 SIN(0 16.97 60)
R1 1 0 41.6
.PROBE
.TRAN 300m 300m 0 150u UIC
.END
```

Main Line During Fault

```
V1 1 0 SIN(0 16.97 60)
R1 1 0 10
.PROBE
.TRAN 300m 300m 0 150u UIC
.END
```

AC Coupling

AC Coupling

```
V1 N 0 SIN(2.5 8.06m 60)
C2 N Q 100n IC=0
R11 Q 0 100k
.PROBE
.TRAN 300m 300m 0 150u UIC
.END
```

PSPICE Representation of the Whole System

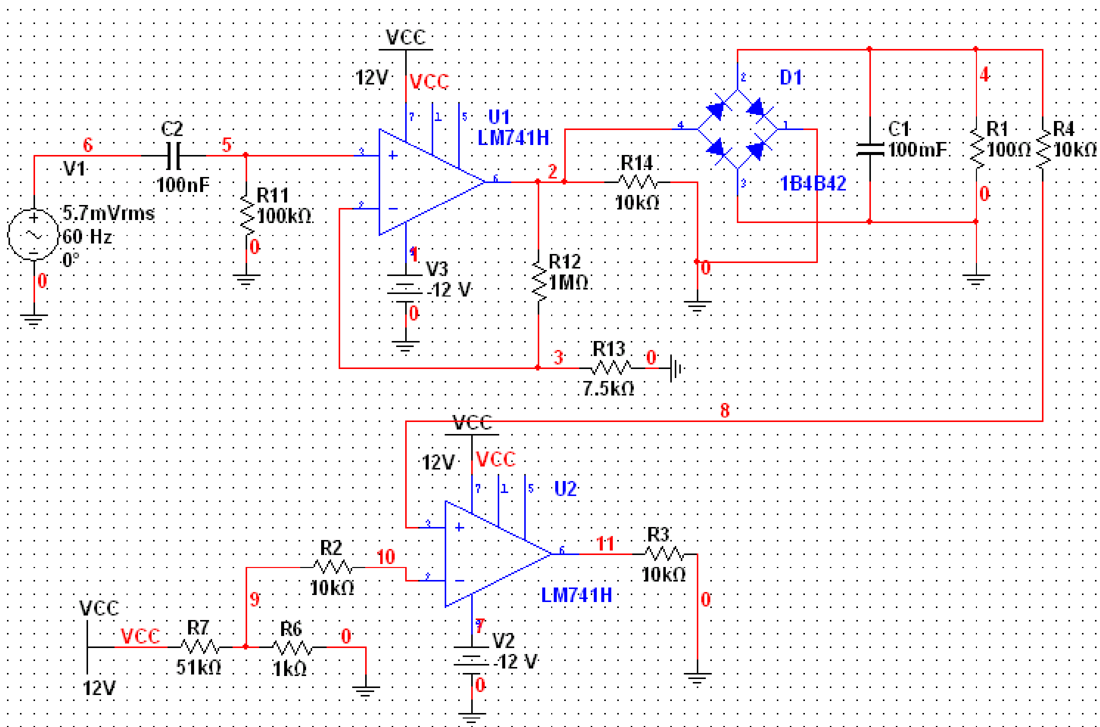
SMART RECLOSER CIRCUIT BREAKER

```
V   1 0 SIN(0 100 60)
VS  2 3 0
R  200 5 0.3
L  5 60 0.2m IC=0
RL 60 70 8
LL 70 0 20m IC=0
SWL  60 0 80 0 SWL
```

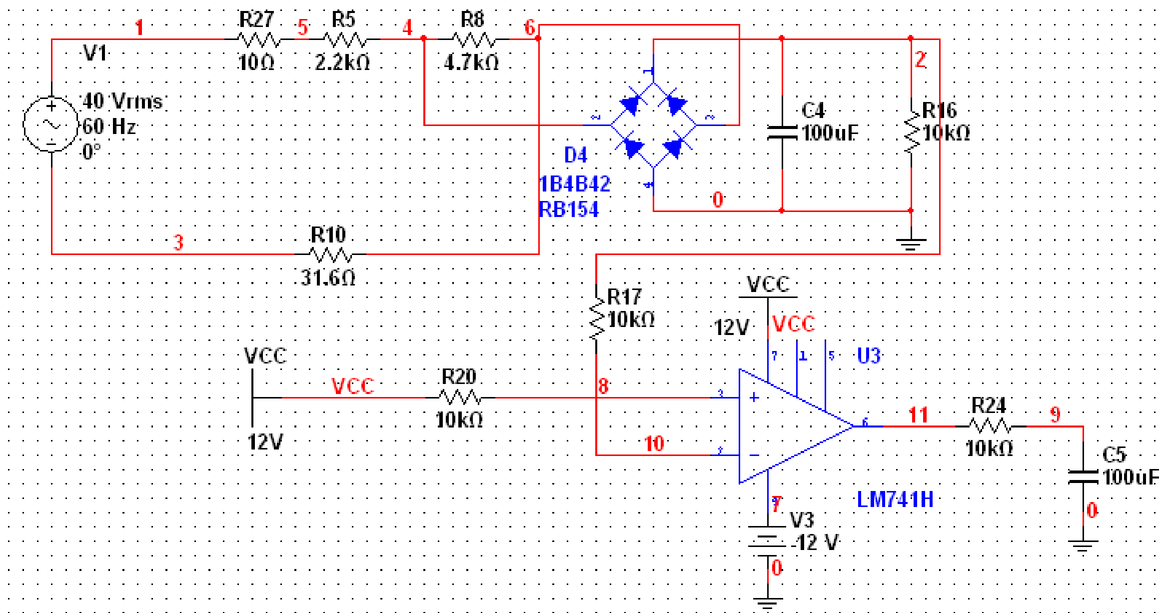
```
VL 80 0 PULSE(0 10 75m 1u 1u 600m 600m)
EC A 0 VALUE={ABS(I(VS))}
REC A C 10
CEC C 0 5m IC=0
RE C 0 50k
VGATE 9 0 10
ET 9 8 VALUE={V(C)}
RGATE 8 0 1MEG
CS 6 0 1u IC=0
RS 6 7 1
EGATE 7 0 TABLE {ABS(I(VS))+V(8)} = -1,0 0,0 0.1,1 1,1
SW  1 2 6 0 SWITCH
RSN 1 4 200
CSN 4 3 1u IC=0
Ecount 0 10 VALUE={V(7)}
Rcount 10 0 1MEG
Gcon D 0 10 0 2.5
Rcon D 0 1MEG
Ccon D 0 1m IC=0
VE E 0 415
EE E F VALUE={V(D)}
REE F 0 1MEG
CSE 100 0 1u IC=0
RSE 100 101 1
EconE 101 0 TABLE {V(F)} = -1,0 0,0 0.1,1 1,1
SWE 3 200 100 0 SWE
.MODEL SWITCH VSWITCH(RON=1m ROFF=1MEG)`
.MODEL SWL VSWITCH(RON=1m ROFF=1MEG)
.MODEL SWE VSWITCH(RON=1m ROFF=1MEG)`
.PROBE
.TRAN 1000m 1000m 0 10m UIC
.END
```

Multisim Simulation Circuits

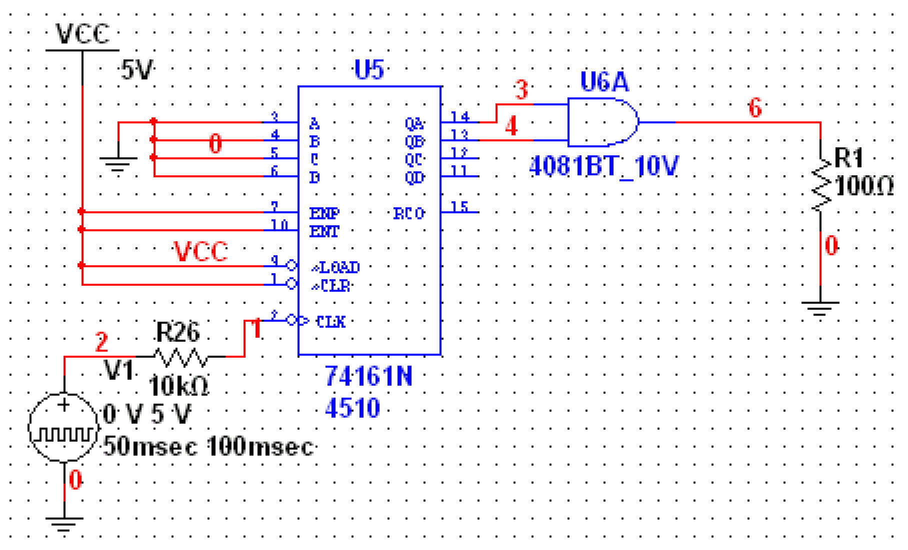
Simulation of the circuit breaker system: amplification of current sensor output, conversion to DC and comparison with a threshold



Simulation of the first control system: AC-DC Conversion and comparison to a threshold



Simulation of the second control system: counter circuit



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