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FLORIDA INTERNATIONAL UNIVERSITY

Miami, Florida

LOW COST SCANNING ARRAYS

A dissertation submitted in partial fulfillment of

the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

ELECTRICAL AND COMPUTER ENGINEERING

by

Matilda Livadaru

2018

To: Dean John Volakis College of Engineering and Computing

This dissertation, written by Matilda Livadaru, and entitled Low Cost Scanning Arrays, having been approved in respect to style and intellectual content, is referred to you for judgment.

We have read this dissertation and recommend that it be approved.

Elias Alwan

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John L. Volakis Major Professor

Date of Defense: June 22, 2018

The dissertation of Matilda Livadaru is approved.

Dean John L. Volakis College of Engineering and Computing

Andrés G. Gil Vice President for Research and Economic Development and Dean of the University Graduate School

Florida International University, 2018

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DEDICATION

To Julia 🕈

ACKNOWLEDGMENTS

I am immensely grateful to have had the opportunity to work with Professor John Volakis. His guidance and mentorship for these past years improved my understanding of antennas and electromagnetism. I am also thankful for his thought-provoking questions regarding this work, which I enjoyed exploring and opened many more avenues to continue on this topic. Likewise, thanks to my graduate committee, for their time and feedback on this research.

I want to extend my gratitude to the passionate group of people from which I learned a lot about phased arrays, and the leadership at RC, whose support allowed me to further my understanding on this topic. In particular, Lee, whose encouragement and optimism for research were energizing whenever the work hit a roadblock. He graciously offered context for this work, provided meaningful insight about all things arrays, and let me to talk about balancing work and graduate studies. Thanks to Jeremiah, whose friendship and collaboration meant a great deal to me in these past years. Thanks to Chris for our conversations on PCBs, Jim, Ted, Dana, and Andy for their support.

Thanks to Randall for the time allowance to finish writing this work.

I am particularly grateful to my family, Julia and Razvan, for their unlimited patience, and unconditional love throughout these past years. Without their support, this work would not have been possible.

ABSTRACT OF THE DISSERTATION

LOW COST SCANNING ARRAYS

by

Matilda Livadaru

Florida International University, 2018

Miami, Florida

Professor John L. Volakis, Major Professor

Over the past decades, phased arrays have played a significant role in the development of modern radar and communication systems. The availability of printed circuit technology and ease of integration with microwave components, as well as the development of low profile and low weight approaches, have also played an important role in their conformal adaptation. However, fabrication costs remain prohibitive for many emergent platforms, including 5G base stations and autonomous vehicles, when compared to a conventional mechanically steered passive array. Therefore, cost reductions in the fabrication and integration of modern phased arrays are essential to their adaptation for many upcoming commercial applications.

Indeed, although phased array design methods are well-understood, even for wideband and wide-angle scanning applications, their fabrication is still based on highcost, low-yield printed circuit technology. With this in mind, this dissertation focuses on a new planar aperture topology and low-cost techniques for phased array methodologies. The first part of the thesis presents new fabrication advancements using commercially available multi-layered printed circuit technologies. We discuss methods for low cost fabrication while still maintaining performance and design constraints for planar array apertures. The second part of the dissertation presents a novel Integrated Planar Array (*IPA*) at S-Band and discusses dramatic cost reductions for multi-function radar applications. Performance and cost benefits are presented, and fabrication techniques to exploit an emerging class of high-speed digital laminates are discussed. These are compatible with high-volume, highyield production, while reducing aperture cost by 75% when compared to conventional approaches. Performance of a planar array employing a pin-fed dual-polarized antenna element with active VSWR<3.2, while scanning to $\pm 45^{\circ}$ in all planes is presented.

Further, to enhance scanning volume, we introduce an aperture-fed dual-polarized element with -40dB isolation at broadside, active VSWR<2.2 while scanning to $\pm 50^{\circ}$ in all planes, scan blindness-free operation, and high aperture efficiency over the band. We present measured beam patterns when scanning to $\pm 70^{\circ}$ from broadside for an 8x8 array demonstrator, showing excellent agreement with simulations.

Overall, this dissertation addresses several manufacturing and performance challenges in realizing affordable planar phased arrays using low cost fabrication without performance compromise. As commercial interest in phased array technology is anticipated to grow, the proposed approaches for phased array design and fabrication will enable quick turnaround times for mainstream adoption.

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Chapter 1: Introduction to Modern Phased Arrays

Market needs and platform specific requirements stimulated the evolution of phased arrays. In its early developments, fixed ground installations of phased arrays delivered more power and aperture gain for government operations such as longer ranges for satellite surveillance [1]. Over time, low-visibility apertures for airborne platforms and on-themove missions pushed the array technology to lower profile and lower weight arrays. Concurrently, progress in solid state physics, specifically in integrated circuits and advanced technology nodes [2], enabled the adoption of high performance, "one-of-a-kind" phased array on military platforms to deliver tactically relevant information and spectrum awareness functionality. However, on this vastly accelerated timeline, from early developments of passive arrays to digital arrays of today (see Figure 1-1 on page 1), performance requirements surpassed the need of developing cost-effective phased array technologies.



Figure 1-1: Timeline of phased array technology through government funding showing an evolution from passive arrays to digital arrays at elemental level. Taken from Herd et. all [2], with the addition of the latest thrust in millimeter wave phased array integration ©IEEE 2015.

More recently, the growing demand for high-data and high-throughput systems [3] has shifted the attention of commercial markets toward a low cost phased array technology solution because of its inherent benefits such as rapidly scanned electronic beams, low profile, low weight and resilience to failure modes. The application spaces are particularly focusing on emerging 5G standards, Internet of Things (IoT) or satellite communication (SATCOM) uses because of spectrum availability and increased capacity (see Figure 1-2 on page 2 for an illustration on the allocation of frequency bands [4, 5]). Existing SATCOM systems are based on gimbaled antennas [6], that are bulky, with slow update times and mechanically steered beams. This outdated technology does not meet the current needs of the consumer market, such as internet on the move or internet availability in remote locations. To this end, enabling emerging phased array technologies and satellite constellations are proposed [7] to meet the demands of the consumer market for higher speeds and more bandwidth. Similarly, 5G technology [8] proposes a new infrastructure for consumer terminals and new base stations to meet the exponential growth of data consumption, increased capacity and low latency.



Figure 1-2: Spectrum allocation for commercial communication and radar links.

This is a consequence of Shannon-Hartley's [9] theorem that sets the system capacity of a channel, C [bits/s], as a function of the channel bandwidth, W [Hz], and the received average signal-to-noise power ratio, SNR (S/N [Watts/Watts]):

$$C = W \log_2 \left(1 + \frac{S}{N} \right) \tag{1-1}$$

Further, with constant envelope signaling, the equivalent relation relates the received power, P_r [Watts], and noise power to *SNR*:

$${}^{P_r}/_N \equiv {}^{S}/_N \tag{1-2}$$

The range equation [10] correlates the ratio of the received power P_r , transmitted power P_t , path loss proportional to the wavelength λ , and the aperture gain of the receiver G_r and transmitter G_t , respectively:

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi d)^2} \tag{1-3}$$

These equations fundamentally limit the degrees of freedom in the system to enable high directional links and increased capacity. For 5G and SATCOM applications, the degrees of freedom are a function of the aperture power gain, and available channel bandwidth.

Additionally, communication applications require modest fractional bandwidth requirements of less than 30%. For 5G, phased arrays in proposed base-stations enable directional links for spatial diversity, whereas, for SATCOM, a new constellation of Low Earth Orbit (LEO) satellites provide high capacity, high bandwidth links, and rely on the received aperture gain. Furthermore, SATCOM applications benefit from the capabilities of phased arrays with rapidly electronically scanned beams for frequent satellite handovers that occur in these proposed constellations. Consequently, phased arrays become a critical enabler for these applications.

Additionally, these communication applications respond to the exponential growth of consumer demand for data consumption and electronics. Of particular interest is the growth of consumer electronics [11], see Figure 1-3 on page 4. Consumer electronics leverage

low-cost packaging techniques, integration, monolithic microwave integrated circuits (MMICs), automated electronics manufacturing and assembly processes driven by high volume production. These advances in high volume manufacturing and integration stimulate the development of more affordable phased array approaches. Altogether, thanks to an increase in transistor density, packaging of MMICs, and tight integration of components on printed circuit boards, the cost boundary in phased arrays has been under pressure to meet the needs of a low-cost consumer market.



Figure 1-3: Exponential growth of consumer units for Internet of Things. Commercial research and development is driving low cost, high volume manufacturing, smaller technology nodes in integrated circuits, packaging and integration in very small form factors.

The pursuit for affordability in phased arrays is not unique to consumer markets. Similarly, in government applications, aging ground-based mechanically steered and passive weather radars need increasing maintenance costs [12]. Combined with a need to reallocate part of the RF spectrum in L-band for government applications [13], an electronically scanned array (ESA) emerged as an option capable to combine multifunction missions needs for weather observations, air traffic control, and Department of Defense (DoD) missions (Figure 1-4 on page 5) with reduced number of deployed systems and lower operational long-term costs [14]. However, a feasible phased array replacement to aging mechanically steered radars must ensure that the price point of the system remains neutral. Despite the fact that planar element topologies have not changed much in the past decades, progress toward lower cost, higher density circuitry and automated assembly is ongoing. However, opportunities to further reduce cost of phased arrays still exist.



Figure 1-4: Operational view of SENSR showing a multi-faceted electronically steered array enabling multiple missions for DoD, FAA, DHS and NOAA. Figure from [14]

With the theme of affordability in mind, one goal of this dissertation is to develop a novel dual-polarized Integrated Planar Array (IPA) for use in S-Band phased array radar application using modern computational resources, and validate our approach through a full set of measurements. Moreover, by exploiting multi-layer printed circuit board (PCB)

technology, we quantify the relative cost reduction and performance objectives achieved in comparison with traditionally built planar apertures. Furthermore, a departure from a traditional aperture design approach asks for a discussion on methods to enhance the scan volume, bandwidth, and mitigate scan blindness for this particular demonstrator.

In the subsequent sections, we briefly introduce modern applications for phased array technology for communication and radar, and associated planar aperture developments to enable these applications.

1.1 Survey of Planar Apertures for Phased Arrays in Communications and Radars

The microstrip patch antenna is a narrowband resonator. It is perhaps one of the most pervasive elements found in radar and communication because of ease of fabrication and modest fractional bandwidth specifications in these types of systems. Munson [15] introduced microstrip patch radiators in literature, initially as a conformal radiator printed on a two-layer board for a telemetry application. He emphasized the benefits of a low-cost, low profile and ease of integration in phased arrays systems, while he recognized the challenges to extend the bandwidth of these radiators.

The advent of the patch led to decades of numerous contributions from research laboratories, industry and academia to achieve moderate bandwidths, polarization, good efficiency and radiation characteristics. In 2001, Waterhouse [16] proposed a linearly polarized stacked patch element design by employing two printed metal layers on a low dielectric material (ε_r =2.2), separated from the ground plane with a layer of foam (ε_r =1.07), referred to as a *lo-lo* construction. The radiator showed 64% fractional

bandwidth. Similarly, in [17], with a combination of a high-dielectric material ($\varepsilon_r = 10.2$), and low-dielectric layer foam material (*hi-lo*), a linearly polarized element showed a fractional bandwidth of 27%. These two methods for bandwidth enhancement have become standard in the design of patch radiators for phased arrays, as seen in the timeline from Table 1-1 on page 6. The timeline for antenna elements in phased array applications spans the last 17 years. We note there is a wealth of information on isolated patch radiators. This table summarizes open literature designs in phased arrays development with a meaningful impact in the planar array development.

Unfortunately, there is scarce information regarding measured performance or affordability of phased array systems realized using planar elements in the open literature. Rather, most of the designs report scanning range based on active VSWR and limited data on scanning performance. Throughout this work, the relative cost of these apertures is derived from PCB vendor conversations based on substrate materials and printed circuit board construction, when it was provided. However, for this work's goals, these designs summarized here use the same construction methodology, thus, they provide meaningful insight for our analysis.

Returning to the timeline, a closer inspection reveals that patch bandwidth enhancement methods rely on a hybrid construction of high/low dielectric materials, or very low dielectric to mitigate surface waves [18]. We note that there are inherent limitations in the fractional bandwidth of these radiators. The limited bandwidth is a consequence of the reduced height from the ground plane to the aperture [19]. The aperture is lower frequency bounded by the proximity of the ground plane reactance, which shunts the free space load, and at the higher frequency by the onset of the grating lobes. Another interesting observation from this table is that there are competing figures of merit that determine the overall performance of the radiating element. In general, the performance of a good radiator design is summarized in terms of the element effective area, scanning volume, scan blindness-free and grating lobe-free operation, polarization diversity, bandwidth and high efficiency across the band. Obviously, the specific application requirements drive the significant performance metrics.

We contrast the performance of a radiating element as a function of the scanning capabilities and the area of the radiating element. We take the physical unit cell size (e.g. area of the element) normalized to the highest frequency of operation (f_{high}) and the scan volume coverage of the array. Intuitively, the smallest element size and lowest gain will have the largest half-power beamwidth (HPBW) that, in turn, extends the scanning range of the overall array. Indeed, a linearly polarized element achieves $\pm 55^{\circ}$ scanning [20], albeit with an element that has a normalized area $0.21\lambda_{high}^2$.

					Scanning range		Fractional	Aperture	Normalized	
		Year	Ref	Polarization	E-Plane (±deg)	H-Plane (±deg)	BW	Construction	Unit Cell Area	Application
		2001	[16]	LP	45	55	64%	Foam/Teflon	$0.18\lambda_{high}^2$	-
ine		2002	[17]	LP	45	45	27%	Foam/High Dielectric Constant	$0.18\lambda_{high}^2$	not known
me		2005	[21]	LP	45	45	58%	Foam/Teflon	$0.2\lambda_{high}^2$	-
Tir		2010	[22]	СР	5	0	2.5%	Air cavity/LTCC	$0.25\lambda_{high}^2$	SATCOM
		2014	[20]	LP	55	56	6%	Foam/Teflon	$0.21\lambda_{high}^2$	-
		2017	[23]	DP	40	50	13%	Air cavity/Low Dielectric Constant	$0.25\lambda_{high}^2$	5G
	•	2018	[24]	DP	45	45	7%	Teflon	$0.25\lambda_{high}^2$	MPAR

Table 1-1: Open literature survey of planar apertures for communication and radar applications.

Consequently, it is most desirable for a phased array element to have an "omnidirectional-looking" pattern (cosine-pattern) in the steering direction to enable wide scanning capabilities, free of grating lobes or surface waves. However, a small unit cell size has low aperture gain, and it is impractical in many applications. Particularly at higher frequencies, such as 5G applications, the physical unit cell size needs to accommodate transceiver circuitry in a compact phased array system. To put dimensions in context, a 5G rectangular planar phased array operating at maximum 60GHz, has an edge length of less than 2.5mm, which is about the average length of a ladybug. Moreover, to truly benefit from aperture and power gain of the array, a design goal is to maximize the area of the element, in the limit of the onset of grating lobes ($0.25\lambda_{hi}^2$) to reduce the number of circuitry required to drive individual elements, with wide scan volume coverage.

1.2 On the Affordability of Phased Array Systems for Communication and Radar Applications

A critical enabler for phased arrays in modern applications remains affordability of these systems. In 1997, Loomis [25] remarks "perhaps the single most significant barrier to ubiquitous radar deployment is their cost." In this section, we investigate the subsystem components and their associated cost, as published in open literature.



Figure 1-5: Exemplary phased array systems showing sub-system hardware components.

A high-level hardware subsystem distribution for an analog active phased array consists of the aperture elements, the microwave circuits that make the transmit and receive modules (T/R), a manifold layer that combines the Radio Frequency (RF) signals, downconverters, and a radar processing unit (see Figure 1-5 on page 10). A breakdown of the relative cost [25] showing the contribution from each sub-system reveals that the RF layers that include the aperture and T/R modules contain almost 75% of the full system cost (see Figure 1-6 on page 10).



Analog Active Phased Array Cost Breakdown

Figure 1-6: Cost distribution of hardware layers in analog active phased arrays. The chart aggregates data from radar houses. From [25].

A decade later, US Army CERDEC and Space and Terrestrial Communications Directorate (S&TCD) publish their developments in phased arrays systems to enable communications on the move [26]. An overarching need for affordability is present in these developments. Research in this area made significant cost improvements at component level, from low-noise amplifiers, power amplifiers, and thereby reducing their cost by 99%, and cost-efficient liquid cooling techniques. However, the aperture developments stalled at adjustments of foam-based patch radiators with no cost reduction benefits.

In one CERDEC development for a SATCOM system, a microstrip patch radiator uses a combination of foam and dielectric (see Figure 1-7 on page 12) to provide dual polarization capability and cross-polarization levels of -20dB at broadside. Furthermore, the axial ratio degradation over the scanning volume led to another year of research in alternative types of elements: crossed dipoles and helical elements. These two elements resulted in costly fabrication because of the touch-labor assembly or poor axial-ratio performance, respectively. With this information, a redesigned stacked patch element provided $\pm 45^{\circ}$ scan volume, with 5dB axial ratio, with somewhat improved performance over the previous design. Therefore, it quickly becomes apparent that highly-integrated planar aperture elements with good performance (i.e. scan volume, dual polarization, and enhanced cross-polarization characteristics) are in demand to further reduce cost by leveraging advancements in automated assembly and fabrication techniques.



Figure 1-7: Microstrip patch element for a SATCOM application. CERDEC study [26]. Left: Phased array system showing hybrid beam control. Right: The microstrip radiator.

In another effort, MIT Lincoln Laboratory and NOAA collaborated on a feasibility study, Multi-Function Phased Array Radar (MPAR), on the affordability and performance enhancements of a phased array system for weather observation to replace aging ground based radars [27]. Aggressive cost targets were set for the emerging phased array replacement. It has now converged in Spectrum Efficient National Surveillance Radar (SENSR) program. SENSR [28] combines multi-function missions for four federal agencies to monitor weather, aircraft surveillance and other government missions at S-Band. By 2025, SENSR seeks to replace approximately 550 mechanically steered radars with approximately 365 phased array radars [14] to enable unprecedented capabilities afforded by phased array technology. Therefore, with a scheduled deployment of a large number of replacement radars, cost and performance become the drivers in this effort. Additionally, affordability needs to be on par with traditional mechanically steered arrays.



Figure 1-8: MIT Lincoln Lab MPAR Panel Sub-Assembly Components showing the Aperture PCB panel, the T/R modules with integrated thermal solution, and the digital backplane PCB.

The outcome of the study provided meaningful insight into the cost distribution of a phased array system at sub-component level. We note the phased array system for the feasibility study leveraged automated assembly and commercially available PCB technology to reduce cost of the array components. An overview of the sub-assemblies [29] shows close integration (see Figure 1-8 on page 13) of one array panel that combines the aperture PCB, T/R modules, signal distribution, thermal solution, and the digital backplane PCB. It turns out that the aperture PCB takes 41% of the cost in volume manufacturing of a phased array system (see Figure 1-9 on page 14), while the driving circuitry, integration, thermal cooling, and digital interconnect take up the remainder. It is interesting to note that the aperture PCB costs have not moved significantly during the >8-year duration of the study. We note that the radiating aperture employs a dual-polarized, foam-based stacked patch operating at S-Band, and achieves $\pm 45^{\circ}$ scan volume in all planes. Clearly, there is a need for affordable planar phased arrays.



Figure 1-9: Cost distribution for the MPAR Panel (2012). Cost percentages shown for volume manufacturing. [29].

1.3 Enablers for Affordable Phased Arrays in Radar and Communication Systems

As we have seen in Section 1.2, affordability is still the biggest challenge in the adoption of phased arrays technology across many platforms and many applications. We looked at sub-systems costs; in particular, heritage T/R modules built in low-yield, high-cost, Gallium Arsenide (GaAs) or Gallium Nitride (GaN) [30] provided low noise amplifiers (LNAs), power amplifiers (PAs) and beamforming functions. More recently, to address the cost of these modules, integrated circuit designers achieved unprecedented capabilities in high-yield, low-cost Silicon Germanium (SiGe) [31] and complementary metal–oxide–semiconductor (CMOS) beamformers by leveraging advancements in the wireless industry and an increase in foundries' capabilities. However, the largest cost driver in these systems remains in the aperture PCB. In order to accelerate the development of affordable phased arrays, the aperture PCB must address several key challenges.

Integrated Planar Apertures

As we have seen in Section 1.1, the cost of planar apertures has not changed much in the past two decades. While the patch radiator was revolutionary at the time with its ease of integration in narrowband systems, it is based on outdated PCB technology that employs a hybrid planar construction to mitigate surface waves or small element aperture area to enhance the scanning volume of the array. The hybrid method employs a foam layer sandwiched between the antenna ground plane and the radiating surface. The drawback to this approach is that the hybrid construction requires manual panel processing and accurate layer-to-layer resolution for the finished aperture PCB, driving up the cost. Often times, the radiating layer is the final step in the phased array PCB assembly as the foam is not suitable for further processing.

Alternatively, a patch radiator based on Teflon materials [24] takes advantage of automated processing steps. However, it adds significant cost to the aperture board, as Teflon is malleable, and restricts the number of layers in multi-layer PCB construction [32]. Additionally, it requires specialized printed circuit board shops to process these boards because copper¹ layers do not stick well to the base laminate, and yield is typically low.

To assess the cost of these common elements found in the literature, we surveyed the printed circuit board processing vendors for the relative cost, \tilde{C} , of the hybrid construction

¹ Nothing sticks to Teflon

and Teflon and compared it to FR-4 type materials found in modern high-speed digital boards.

Table 1-2: Relative PCB laminate cost compared to FR-4

Material	Relative Cost \tilde{C} to FR4
FR-4 High Speed Digital	1x
Rogers, Teflon, or Hybrid Construction	3x
Low Temperature Co-Fired Ceramic (LTCC)	4x

Consequently, to compare the cost and performance of the elements, we introduce a normalization fill area factor, defined as the ratio between the number of elements, N_{elem} , required to fill an equivalent area λ_{hi}^2 , where λ_{hi} is the wavelength at the highest frequency of operation, with maximum of 4 elements in the limit of grating lobe onset. The fill area factor, thus, takes into consideration the element effective area.

Fill Area Factor =
$$4N_{elem}/\lambda_{hi}^2$$
 (1-4)

The number of elements follows from the normalized unit cell area defined as the ratio between the area of the antenna element expressed as a function of the wavelength and a theoretical maximum of $0.25\lambda_{hi}^2$:

$$N_{elem} = \frac{1}{A_{unit \ cell \ norm} / \lambda_{hi}^2} \tag{1-5}$$

We express the weighted aperture cost for λ_{hi}^2 fill area factor as:

Weighted Aperture Cost =
$$N_{elem} \tilde{C}$$
 (1-6)

For the radiating elements in Table 1-1 on page 8, we plot the relative cost per area versus the scan volume capability of the element. We see in Figure 1-10 (page 17), a lower cost, high-performance aperture PCB construction must exploit FR-4 type laminates to broaden the manufacturing base options and eliminate touch labor assembly.



Figure 1-10: Normalized Cost per Unit Area relative to the Scan Performance of Planar Elements.

Commercial PCB Manufacturing and Multi-Layer Circuit Boards

A modern affordable integrated planar aperture PCB must parallel the developments in high-speed digital printed circuit boards. In this work, we exploit an emergent class of high-speed digital laminates with a high dielectric constant for the aperture PCB to enable cost reduction techniques in automated processing, broaden the manufacturing base and allow for multi-layer board construction with no touch labor. Additionally, we address the performance challenges associated with the development of the dual-polarized planar element using the fabrication and integration methods outlined here.

Array Integration

Close integration of the aperture PCB on FR-4 type materials with the surface mount transceiver circuitry provides cost and performance enhancements because of a multi-layer construction that reduces interconnect loss by eliminating expensive connectorized interfaces and ease of routing. From an automated integration perspective, for narrowband phased arrays, a fully-integrated circuit card array results in the lowest costs (see Figure 1-11 on page 18).



Figure 1-11: Aperture integration within the array impacts cost of the phased array system.

Circuit Card Architecture integrates all the radiating elements for the phased array and supporting circuitry within a monolithic printed circuit board. This architecture leverages automated assembly. In particular, 5G phased arrays are marching toward this architecture.

Tile Card Architecture integrates building blocks, or tiles, comprised of radiating elements and supporting circuitry. Within this architecture, the elements may be planar or card based. This approach is common in large phased arrays with high element count.

Brick (Slate) Architecture integrates vertical building blocks comprised of radiating elements and supporting circuitry. This architecture is typical for wideband arrays with vertical printed elements.

1.4 Contributions and Organization of this Dissertation

The goal of this dissertation is to address the cost of the aperture PCB through the development of a novel IPA design and methods. In particular, we emphasize 1) a departure from traditional specialized RF-laminates in the aperture design, 2) we propose an integrated planar aperture with dual-polarization, improved cross-polarization levels, wide scan-volume, free of scan blindness, and lower cost, and 3) performance enhancements of the radiating element through surface wave mitigation and feeding techniques.

In Chapter 2, we discuss the design approach for a low cost planar array design operating at S-Band. We contrast two feeding methods for the antenna element, a pinfeeding technique and an aperture coupled design. We note these techniques are applicable to a wide range of frequency bands. Moreover, we develop two elements based on these feeding techniques and discuss manufacturing constraints and practical implementations. Chapter 3 presents the infinite and finite array performance in the simulation environment and discuss the performance metrics regarding field of view and bandwidth of the radiating aperture.

Chapter 4 presents the measured results for an 8x8 dual polarized aperture. This dualpolarized design, which we refer as integrated planar aperture (IPA) yields $\pm 70^{\circ}$ scanning range, in all planes, and scan blindness-free operation.

Chapter 5 summarizes our conclusions and opportunities for improvements, as well as suggestions for IPA high frequency extensions.
Chapter 2: Low Cost Integrated Planar Array (IPA) Considerations

This chapter presents preliminary considerations for the radiating element to enable integrated planar apertures for radar and communication systems at an affordable price point. In particular, we demonstrate two radiating elements for operation at S-Band to address the multi-function phased array radar (MPAR) because of the availability of performance metrics and cost target for this particular application. We summarize the aperture requirements in Table 2-1. The dual-polarized element in a rectangular grid needs to cover 2.7-2.9GHz frequency, $\pm 45^{\circ}$ scan volume coverage off broadside in all planes, cross-polarization isolation of at least -20dB, and simple 50 Ω feeding structure. We remark that we provide comparative relative cost numbers for the aperture PCB and existing designs in Section 5.1.

Requirement	Objective
Antenna Element Lattice	Rectangular grid
Polarization	Dual (horizontal and vertical)
Frequency of operation	2.7 -2.9GHz
Scan Volume	$\pm 45^{\circ}$ off broadside
Cross-Pol Isolation	-20dB
Feed	50Ω

Table 2-1: Performance requirements for the S-Band Aperture

The dual polarization of the element is a requirement for the weather monitoring application because both polarizations need to capture the aspect ratio (or geometry) of the target (i.e. rain droplets). Polarization diversity sorts out the shape of the rain drop [33]. Additionally, for a precise discrimination of the rain drop distortion, the horizontal and vertical patterns need to have similar beam shapes with high cross-pol isolation, which is

challenging for printed planar antennas. For a small target, such as a rain drop, weather observations rely on a pencil beam with 1° 3-dB beamwidth [34]. It turns out that 1° beamwidth requires an array length L of ~7.1m or approximately 20,000 total elements (see Figure 2-1 on page 23) for a square aperture. With such a large number of elements required for the full system, it becomes apparent that cost of the system needs to remain affordable. Notably, we can write the half-power beamwidth [35] in the direction of the scan angle as:

$$\theta_{3dB} = \frac{k\lambda}{Nd\,\cos\theta_{scan}}\tag{2-1}$$

In this equation, the *k*-factor is a function of the aperture illumination. For uniform amplitude illumination, k = 0.886. Additionally, the 3-dB beamwidth is a function of the frequency of operation, and inversely proportional with the physical length of the array expressed as the inter-element spacing *d* and the number of elements *N* along one axis,

$$L = Nd \tag{2-2}$$

and the steering angle θ_{scan} . Equation also accounts for the beam broadening as a function of the steering angle (1/cos θ_{scan}).

Furthermore, in this chapter we discuss key PCB manufacturing challenges to enable future integration with surface mount T/R modules and reduce cost of the system. We also consider two feeding methods for the radiating element for dual-polarization capability and discuss the PCB implementation of the radiating planar elements.



Figure 2-1: Beamwidth of a scanning array with uniform illumination as a function of the scan angle θ_0 . For a pencil beam in both azimuth and elevation planes, an array requires 20,000 total radiating elements.

2.1 Considerations for Manufacturing Integrated Planar Arrays

We start the initial design approach with considerations for multi-layer planar arrays to ensure compatibility with standard manufacturing processes. As described in Section 1.3, an affordable planar aperture exploits standard commercial PCB processes and a new class of materials used in high-speed digital boards to enable automated processing. Moreover, aperture designs require close knowledge of manufacturing, fabrication constraints and materials to achieve predictable measured results and good agreement with the simulation model. We cover in this section high-level considerations for aperture thickness and size that determines the array integration approach.

Standard Panel Sizes and PCB Thickness

Among printed circuit board vendors, a common standard of manufacturing exists that establishes the maximum size of the printed circuit board, thickness and smallest feature sizes for a *multi-layer* (20+ layers) construction [32, 36]. We note that we frame the development of the aperture design in terms of the capabilities of current printed circuit technology manufacturing. Using this normative, we glean meaningful insight to drive our design variable space. Commercial PCB shops standardized on these sizes for their laminate processing equipment. The overall finished thickness (*t*) of a multi-layer printed circuit board compatible with standard processing equipment (see Figure 1-11 on page 18) must not exceed t = 0.35", while the overall panel size (*xy*) must be within 18" x 24" or 21" x 24" for standard laminate panels².



Figure 2-2: Standard Printed Circuit Board Size and Maximum Finished Thickness

 $^{^{2}}$ We make the distinction between available standard panel sizes through the manufacturers. There are a variety of panel sizes through the manufacturers. However, our focus is on standards of processing these panels through widely available board shops.



Figure 2-3: Optimum number of planar antenna elements within a standard 18" x 24" panel. The fill factor of the panel is set at 90% to allow for PCB test coupons.

For a planar aperture, these considerations translate into a lower frequency bound for a realizable, printed planar aperture using standard PCB processes. We observe that with increasing frequency, the number of antenna elements in a rectangular arrangement at the optimum separation $\lambda_{hi}/2$ printed on a panel increases (see Figure 2-3 on page 25). This has the added benefit to reduce the cost per radiating element at higher frequencies. In addition, a practical lower physical limitation for the frequency of operation is evident. For example, at a maximum operation frequency of 7GHz, a planar array allows for a total of 400 elements, while at 1GHz, only 8 elements can fit within an 18" x 24" panel, which makes an affordable planar array solution impractical for frequencies of operation lower than ~2GHz.

For S-Band operation, the maximum number of allowed elements is 74. However, as discussed in Section 2.1, the full system requires 20,000 radiating elements. Observation

leads to a rectangular arrangement³ of elements in a sub-array panel because it favors a tiling architecture of sub-array panels to achieve array systems with a large element count.



Figure 2-4: Panel thickness for standard PCB processing equipment

For the printed elements in this dissertation, the physical PCB thickness of the overall panel also enforces bandwidth limitations of the antenna because of the proximity of the consider thickness [19]. We overall ground plane an panel of t = $[0.05; 0.1; 0.15, 0.2] \lambda_{low}$ and illustrate overall physical thickness of the panel in Figure 2-4 on page 26. We observe that for S-Band operation, the aperture panel has a limited set of allowed thicknesses that results in a reduced bandwidth for the radiator. In contrast to

³ A triangular element arrangement reduces by ~13% the number of antenna elements required to fill the same aperture area with elements in a rectangular arrangement. In a triangular grid, the element area is slightly larger than $0.25\lambda_{hi}^2$. Moreover, the triangular grid pushes the grating lobes in various regions of the visible space. For a comprehensive discussion, refer to [51].

low frequencies, at higher frequencies, a variety of allowed thicknesses is realizable in modern printed circuit technology.

Multi-Layer Printed Circuit Board Technology

Current practices in the construction of multi-layer printed circuit board technology enable a dynamic design and optimization space regarding the number of layers in the integrated aperture. Multi-layer printed circuit boards use core laminates and prepreg (the glue between core layers). Additionally, they are based on glass and resin composites with a typical high dielectric constant ($\varepsilon_r \ge 3$) and very low loss ($tan\delta < 0.006$) to enable high-speed data transfer. A variety of materials in different thicknesses and dielectric constants are available from PCB suppliers. These materials form a building block in a PCB stackup to enable a multi-layer construction for the integrated planar aperture and allow optimization of the radiator performance.

We incorporate this new class of materials in the aperture, and we enforce a circuit card architecture compatible with a tile integration for large arrays. A circuit card architecture potentially enables the digital, power, manifold and routing functions as required by an active array to reside within a monolithic board. These added functionalities serving digital, power, and signal distributions do not require specialized RF-based laminates. Therefore, a homogenous substrate approach for planar array is straightforward. This approach enables a robust and environmentally hardened construction, while it avoids the mismatch of the coefficient of thermal expansion (CTE) between layers.

2.2 Feeding Methods for an Integrated Planar Aperture

Several methods exist to route an RF signal line and excite a printed planar antenna. These methods (see Figure 2-5 on page 28) include direct feeding, and non-contact excitation [37]. Selecting the type of excitation depends on the particular application. We review some of the methods and contrast benefits and disadvantages of each.



Figure 2-5: Feeding techniques for a printed antenna element include aperture coupling excitation, transmission line (T-Line) edge feeding, proximity coupling, and probe coupling.

Direct feeding methods are inductive in nature because of the length of the signal path in series with antenna impedance. For t-line edge excitation, a microstrip feed line has a characteristic impedance Zo (typically set at 50 Ω) expressed using the lumped element circuit model for a lossy line and in absence of coupling as [38]:

$$Z_0 = \frac{\sqrt{R + j\omega L}}{\sqrt{G + j\omega C}} \simeq \sqrt{\frac{L}{C}}$$
(2-3)

Here, R is the series resistance, L is the series inductance, G is the shunt conductance and C is the capacitance per unit length, respectively (see Figure 2-6 on page 29). Similar

argument holds for the probe-feeding technique. With regard to the lumped circuit model for a transmission line, it is convenient to model the feed path as a two-port network because the TEM-mode or a quasi-TEM mode (for the microstrip line) require two conductors, namely, the feed line and the ground reference plane. For the edge feeding method, the signal line is in contact with the edge of the patch. The antenna impedance response is a function of the contact point location between the feed line and the edge of the patch. One disadvantage with this type of feeding in planar arrays is the spurious radiation of the feed lines, that reduces the efficiency of the aperture. To overcome this shortcoming, the probe coupled patch uses a pin (via or coax) to route the signal with minimum spurious radiation from the feed lines to the aperture element. Similarly, the location of the pin on the driven layer determines the antenna impedance response. For integrated planar arrays, the pin-feeding method provides better radiation efficiency and ease of routing to the individual antenna elements than edge-feeding at the expense of adding vias in the substrate.



Figure 2-6: Lumped-Element Circuit Model for a Transmission Line Feed

The *non-direct excitation* relies on capacitive coupling of the feed line to the radiating element. The feed is a transmission line terminated in an open circuit with a stub for additional matching optimization control. The proximity coupled method uses a feed line

directly underneath the radiator, in which power couples to the radiator through a thin substrate that inherently limits the bandwidth, and has poor radiation efficiency. Conversely, the aperture coupling method, initially introduced by Pozar [39], separates the feed structure from the radiator through an antenna ground plane. In an integrated aperture, a stripline feed couples the RF power to the radiator through a slot (sometimes referred as aperture slot) in the ground plane. This mechanism achieves high cross-polarization isolation because the ground plane shields the spurious radiation of the feed line. We note the shape and size of the slot, and substrate height between the radiator and the slot determine the strength of RF coupling. Moreover, the slot coupling mechanism provides additional degrees of freedom in the optimization and matching the response of the radiator through the feeding structure, open stub termination, and the shape and size of the slot. Drawbacks to this approach are an extra layer required for a stripline feed and expensive computational time.

2.3 Dual Polarization Feeding Techniques

To illustrate dual-polarization feeding techniques for planar elements, we consider a probe-fed and aperture coupled radiating elements because of their compatibility with a circuit card array assembly (see Figure 2-7 on page 31) and enhanced antenna radiation characteristics.

The probe feeding technique for an integrated array uses vias in the PCB for direct contact between the signal layer and the radiating element. For dual linear polarization synthesis, horizontal (H-Pol) and vertical (V-Pol), respectively, we place the vias

orthogonally from the geometrical center of the radiating element to generate orthogonal electric fields.

Conversely, the slot coupling method uses 50Ω striplines to route the signals to the radiating element. Similar to the probe coupling case, the two slots are rotated 90° from each other with respect with the geometrical center of the unit cell.



Figure 2-7: Dual-polarization feeding method for the integrated planar. Left: Probe-feeding for dual linear polarization within a unit cell. Right: Aperture coupled feeding within a unit cell to enable dual-polarization for IPA.

2.4 PCB Stackup for Integrated Planar Antenna Design with Probe Feeding

With these manufacturing considerations, we investigate the probe-feeding method and PCB integration for the antenna element. As we have seen, one key challenge at low frequencies for the printed aperture realization is the physical thickness of the board. We

choose Panasonic Megtron6 substrate as the baseline for the construction of the antenna ($\varepsilon_r = 3.64$ and $tan\delta = 0.003$). A preliminary PCB stackup for the antenna (see Figure 2-8 on page 32) incorporates six metallization layers. We require discrete RF connectors to each of the antenna feeds to fully characterize the RF performance of the antenna panel, in absence of any RF combiners or transceiver circuitry. Two additional layers (Layer 1 to Layer 3) route the signal from the two RF connectors to the feed points within one unit cell. The RF surface mount connector is a micro-mini connector (MMCX) [40] that has acceptable RF performance up to 6GHz with a small footprint of only 0.136 x 0.136". The connector routes a microstrip feed line (red line in Figure 2-8 on page 32) from Layer 1, through a signal via from L1 to L3. The radiator layers feature one ground layer (Layer 3), and three stratified dielectrics with metallization on Layer 4, and Layer 5, while Layer 6 acts as a dielectric superstrate to enhance the scan volume. We require ground shielding vias between L1-L3 to form a 50 Ω coax feed. In the PCB, a controlled depth drilling technique (back drill) removes the unwanted stub between L4 to L3, while eliminating one lamination step reducing the overall fabrication cost of the panel.



Figure 2-8: Preliminary PCB stackup for the probe-feed integrated antenna element

A cross-section of the antenna unit cell (see Figure 2-9 on page 33) shows the electromagnetic model implementation with the dual-feeds in the antenna unit cell and a simplified layer stackup.



Figure 2-9: Electromagnetic implementation of the probe-feed unit cell design. Left: Crosssection of the unit cell. Right: Bird-eye view of the first routing layer to the antenna feeds.

Table 2-2 shows preliminary substrate thicknesses required for the pin-fed radiating element. However, the baseline dielectric thicknesses are not standard, and because of the physical thickness of the board, an accurate PCB stackup uses a combination of available standard cores and prepreg to reach the baseline thicknesses (see Figure 2-10 page 34). The baseline for the aperture layers are 0.25" thick ($\sim 0.06\lambda_{2.9GHz}$), with an overall panel thickness of 0.32", well within manufacturing capabilities. In the PCB implementation, the aperture panel requires a combination of 19 standard cores and prepreg layers (see Figure 2-10 on page 34), and their overall thickness given in Table 2-2 (page 34). Because the PCB stackup uses a homogenous material construction, in the electromagnetic model we use the simplified layer stack.

	Baseline	Baseline	PCB Actual	Unit
	Thickness	Value	Thickness	
Layer 1 – Layer 2	h1	30	29.5	
Layer 2 – Layer 3	h2	30	30	
Layer 3 – Layer 4	h3	120	117.5	mil
Layer 4 – Layer 5	h4	120	117	
Layer 5 – Layer 6	h5	30	29.5	

Table 2-2: PCB Thickness for the Probe Feed Antenna Element



Figure 2-10: PCB Stackup Implementation for the Probe-Feed Integrated Planar Aperture

2.5 PCB Stackup for Integrated Planar Antenna Design with Slot Coupling

The slot-coupled radiating element requires a stripline layer to route the signal to the antenna feed slots. For the demonstrator panel, we use RF connectors (SMPM) [41] to route the signal via a microstrip trace on Layer 1 to the 50 Ω stripline antenna feed (see Figure 2-11 on page 35). To eliminate one lamination step, the signal via has a back drill to remove the stub between Layer 3 to Layer 4. To enhance the isolation between the two stripline feeds within the unit cell, we use ground shield vias from Layer 1 to Layer 3. Layer 4 through Layer 6 are the aperture layers, and we add a dielectric superstrate cover.

The preliminary stack for the slot-coupled element employs Megtron6 as the dielectric substrate.



Figure 2-11: Preliminary PCB Stackup for the Slot-Coupled Radiating Element

Similar to the probe-coupled element, the electromagnetic model for the slot-coupled (see Figure 2-12 on page 35) uses a simplified PCB stack.



Figure 2-12: Electromagnetic model implementation of the slot-fed unit cell design. Left: Cross-section of the unit cell. Right: Bird-eye view of the first routing layer to the antenna stripline feeds (ground via shields removed for clarity).

	Baseline Thickness	Baseline Value	PCB Thickness	Unit
Layer 1 – Layer 2	h1	6	5.9	
Layer 2 – Layer 3	h2	30	28.8	
Layer 3 – Layer 4	h3	30	29.5	mil
Layer 4 – Layer 5	h4	100	99.8	
Layer 5 – Layer 6	h5	100	108.7	
Layer 6 - Cover	h6	20	17.6	

Table 2-3: PCB Thickness for the Slot-Coupled Antenna Element

The PCB implementation of the panel includes a combination of 19 prepreg layers and laminate cores to realize the physical thickness required. We remark that the aperture height is 0.22", at ~0.05 $\lambda_{2.9GHz}$, slightly lower than the probe-fed aperture, and the panel has an overall thickness of 0.29", well within manufacturing capabilities, with opportunities to add more layers for digital, RF manifold or power routing.



Figure 2-13 PCB Stackup Implementation for the Slot-Fed Integrated Planar Aperture

In the next chapter, we discuss two designs of the integrated planar aperture, using the feeding techniques we highlighted here based on pin-feeding and slot-coupling. We incorporate the actual PCB thicknesses for the radiating elements to reduce the number of iterations in the electromagnetic simulations.

Chapter 3: Array Performance in a Simulation Environment

As described in the previous section, we include the PCB manufacturing constraints in the design of the radiating elements and optimize their scan impedance over the desired angles of incidence and frequency. In this chapter, we detail the design of the two elements, and analyze the simulated performance in an infinite and finite array environment for operation at S-Band. Particularly, we use Frequency Selective Surfaces (FSS) [42] as an active phased array (i.e. voltage sources connected to each radiator) because of their wellknown stability in the scan impedance with varying frequency, and we employ feeding methods used in the patch radiators. We refer to this array as the *Integrated Planar Aperture* (IPA).

3.1 Design of the Pin-Fed Integrated Planar Aperture

We begin with the pin-fed dual-polarized unit cell implementation. The unit cell shown (see Figure 3-3 on page 43) contains two radiating layers above a ground plane. The first radiating layer closest to the antenna ground plane has two driven monopoles for each polarization. Each printed monopole has an unbalanced 50 Ω feed realized using a signal via in the printed circuit board. The additional parasitic patches surrounding the driven monopoles act as impedance matching (see Figure 3-2 on page 41). A top metallization layer and a dielectric superstrate provide additional impedance matching over the scanning volume. Indeed, the stratified dielectric layers and aperture layers act as impedance

transformers from the 50 Ω coax to the characteristic Floquet fundamental port impedances, namely TE_{00} and TM_{00} , that modulate with the scan angle [43] according to the equations:

$$Z_{\theta}^{TM} = \frac{1}{\cos\theta} \sqrt{\frac{\mu_0}{\varepsilon_0}}$$
(3-1)

and

$$Z_{\theta}^{TE} = \cos\theta \sqrt{\frac{\mu_0}{\varepsilon_0}}$$
(3-2)

Here, μ_0 , ε_0 are the constitutive parameters of free space, and θ is the scan angle measured from broadside (from the *z*- axis orthogonal to the plane of the array, *xy*). These equations show that the planar element needs to transform the system impedance of $Z_0 = 50\Omega$ to a broad impedance range over the scanning range (see Figure 3-1 on page 39). For E- and H- plane scanning this constitutes a challenge to the designer because with very wide angles of incidence, the free space impedance rapidly diverges from the nominal free space impedance of ~377 Ω .



Figure 3-1: Fundamental Floquet mode impedances over varying angles of incidence.

To illustrate the additional matching provided by the parasitic metallization we look at the driven monopole response at broadside with periodic boundary conditions, in absence of the parasitic patches (see Figure 3-2 on page 41) in the stratified dielectric media. We note the tuning response and bandwidth extension (2.66GHz to 3.44GHz) observed with the addition of parasitic metallic patches. However, for the radiating element, the onset of grating lobes limits the upper operational frequency at 3GHz. From an equivalent circuit perspective, the parasitic patches have an inherent inductance due to their length in series with a coupling capacitance due to the proximity of the neighboring elements.

We simulate the periodic unit cell in Ansys Electronics Desktop 19 [44], and we use the optimized values given in Table 1-1 on page 8. The broadside return loss for H- and V-polarization and the Smith Chart response is given in Figure 3-4 (page 44). At broadside, the element shows a return loss of -8.6dB at 2.7GHz and -15.3dB at 2.9GHz. The horizontal polarization and vertical polarization have similar impedance responses because of the symmetry of the element for each polarization. The port to port isolation within the unit cell shows degraded performance of -16dB at the low end of the band. This result is consistent with the initial simulation of the "probe-only" (see Figure 3-2 on page 41).

We remark that the Smith Chart response is critical to track for narrowband phased arrays systems. It is well known that the impedance antenna response changes over the scanning volume. For the probe coupled element, the impedance response at broadside is matched to a lower source impedance. However, with varying angles of incidence, the Floquet mode impedance changes, and the antenna impedance locus moves from the broadside response. Ideally, the impedance locus does not change too abruptly over the scanning volume. Indeed, a tight impedance locus in the active impedance allows direct integration with T/R modules. In particular, the antenna impedance response over scan becomes both the load impedance for the PA, and the impedance seen by the LNA, in absence of circulators.



Figure 3-2: Simulated return loss the driven monopole-only fed by a 50Ω via-probe in a periodic unit cell. Solid line shows the de-tuned impedance response at broadside of the monopole. The dashed lines show the tuning impedance response of the unit cell with the addition of the parasitic patches.

Parameter	Value	Units
al	24	
a2	265	
a3	208	
a4	96	
b1	174	mil
b2	360	
b4	380	
b5	855.5	
b6	639	
dx	2	
dy	2	in
h3	117.5	
h4	117	mil
h5	29.5	

Table 3-1: Optimized parameter values for the probe-fed unit cell



Figure 3-3: Periodic unit cell model for the probe-fed IPA element, showing first and second aperture layers, and 50Ω via probes to the driven monopoles. For dimensions, see Table 3-1 (page 42).



Figure 3-4: Simulated broadside response for the probe-fed radiating element for both polarizations. Left: Return Loss and H-V port isolation. Right: Smith Chart response.

The simulated active VSWR for the pin-fed square unit cell (see Figure 3-5 on page 45) shows scanning capability up to $\pm 45^{\circ}$, in $\theta_{scan} = 15^{\circ}$ increments, for both polarizations (H- and V-, respectively) in the TM-mode (E-plane), TE-mode (H-plane) and Diagonal (D-plane) with an active VSWR <3.1 over the scanning volume. We note that the antenna element has a simulated radiation efficiency of 95% across the band calculated from the ratio of radiated power to the accepted power (we exclude the feed mismatch).



Figure 3-5: Simulated VSWR of the infinite array with probe-feeding. The array has VSWR<2.1 at broadside, with scanning capability in E-, D-, and H- plane to 45° and VSWR <3.2.

However, the probe-fed element suffers from a fatal deficiency for the S-Band application. Although we took steps to spatially separate the two coaxial probes to improve isolation, the response (see Figure 3-6 on page 46) shows -15dB coupling at broadside, and degraded performance over the scanning volume.

Nevertheless, the probe feeding implementation for IPA reduces the complexity of the printed circuit board by eliminating one lamination step. Moreover, through the use of FR-

4 based laminates, wide scan volume up to $\pm 45^{\circ}$ in all planes, and high radiation efficiency, the dual-polarized IPA array provides a significant low-cost alternative to stacked patch apertures.



Figure 3-6: Right: H-to-V Coupling for the probe-fed radiating element in an infinite array environment. Left: Simulated radiation efficiency of the probe-fed element defined as the ratio of radiated power to the accepted power.

For some applications, where only linear polarization is desired, such as a communication system with vertical polarization requirements, a modified probe-fed IPA array design is attractive. In Section 3.2, we present a new design a dual-polarized IPA and improve the scan volume of the radiating aperture, and address the challenge of cross-polarization isolation for planar apertures.

3.2 Design of Slot-Coupled Integrated Planar Array with Enhanced Isolation

In this section, we detail the design for a dual-polarized phased array with enhanced cross-polarization levels and wide-scanning volume. Indeed, for our particular application, the planar aperture needs to exhibit high cross-polarization isolation to enable weather target discrimination. As discussed previously, a common way to achieve enhanced polarization purity in patch arrays is through a slot-coupled feeding method because it isolates the spurious radiated fields of the feed line from the radiation of the patch. However, a dual-fed patch radiator supports more than one orthogonal sense of polarization when scanning away from the principal planes which counteracts the potential improvement in isolation. To overcome this critical flaw of patches, we look at synthesizing dual polarization through means of a novel printed antenna geometry.

Consider a descriptive way of polarization synthesis through an analogy to a wire grid polarizer. A spatial filter, or the polarizer, transmits the \vec{E} -field aligned with length of the wires, and absorbs or reflects the undesired polarizations in the specular direction. While it makes an imperfect analogy because our goal is to synthesize dual polarization without the typical polarizer loss, this meaningful insight provides guidance in the choice of the radiating geometry. In addition, Munk [42] suggested the use of an arrangement of dipoles as a FSS passive structure because they can handle only the co-polarized \vec{E} -field along the conducting dipoles. This is accomplished in a "gangbuster" FSS geometry, with two layers of printed dipoles in an orthogonal arrangement. We also note in [45], a linearly polarized, single-layer dipole geometry is proposed as an isolated element, rather than a patch. We use these starting points to shift from a patch geometry to a dipole-like based geometry to synthesize dual polarization within the unit cell.

Parameter	Value	Units
al	20	
a2	210	
a3	170	
a4	210	
a5	360	
аб	480	
a7	190	
b1	213	
b2	120	mil
b3	400	
b4	190	
c1	54	
c2	180	
c3	650	
c4	506	
dx	2	
dy	2	in
h4	99.8	
h5	108.7	mil
h6	17.6	

Table 3-2: Optimized parameter values for the slot-fed dual polarized unit cell



Figure 3-7: Periodic unit cell model for the slot-fed dual polarized IPA element, showing first and second aperture layers. Two separate 50Ω stripline couple into the H-polarized and V-polarized elemental geometry. For dimensions see Table 3-2 on page 48.



Figure 3-8: Simulated broadside performance for the slot-coupled dual-polarized element. Left: Return loss for the horizontal and vertical polarization. Better than -40dB port to port isolation at broadside. Left: Impedance on the Smith Chart at broadside for H- and V-Polarizations.



Figure 3-9: Active antenna impedance in an infinite array environment showing stability with the angle of incidence. Black lines represent the broadside response. Left: Active impedance for the horizontal polarization. Right: Active impedance for the vertical polarization.



Figure 3-10: Simulated active antenna response for the dual-polarized element in Figure 3-7 (page 49) in an infinite array environment. The input system impedance is 50Ω . Black line represents the broadside response. Left: Smith Chart response for the element scanning to $\pm 50^{\circ}$ from broadside. Solid black line represents the response at broadside. Right: Active VSWR for the infinite array with <2.2 in all planes for both polarizations.



Figure 3-11: Simulated horizontal to vertical coupling for $\theta_{scan} = [0 - 50]^{\circ}$ in 10° increments in an infinite array environment shows better than 20dB isolation across ±50° scan volume in all planes. Solid black line represents the broadside response.

To this end, we detail here the development of a dual-polarized planar element for use in an active phased array with wide scanning capability and affordable PCB construction.

The radiating element geometry requires 5 metallization layers. The feed layer has one 50Ω stripline for each polarization terminated in an open stub for impedance matching to the antenna impedance. Additionally, a slotted RF ground has two orthogonal slots for each polarization. The shape and size of the slot, and the stub terminations are part of the optimization variable space. Between the ground layers, we add a wall of ground vias for each stripline to eliminate parallel waveguide modes and enhance isolation between the feed lines. The aperture has two metallization layers with printed dipoles. A dielectric cover provides further impedance matching to the free space impedance. We note that due to the particular arrangement of the dipole geometry, we only maintain an axis of symmetry in

the H-Plane for each polarization to reduce the number of optimization variables. However, this will result in slight impedance variations between the H- and V-polarizations, as we will see in the simulation results.

We simulate the performance of the periodic unit cell in Figure 3-7 (on page 49) with the optimized values (see Table 3-2 on page 48). The simulated broadside return loss and impedance on the Smith Chart, active VSWR, active scanning impedance, and port-to-port coupling is given in Figure 3-8 through Figure 3-11. At broadside, the element shows better than -9dB return loss for the horizontal polarization and -11dB for the vertical polarization at the low end of the band, and ~-20dB return loss at 2.9GHz for both polarizations. Notably, simulated port-to-port isolation is better than -45dB at broadside because of the stripline feed shielding and low cross-polarization susceptibility level of the radiating geometry.

The radiating element exhibits an active VSWR<2.1 for angles of incidence of up to $\pm 50^{\circ}$ for both polarization in $\theta_{scan} = 10^{\circ}$ increment (see Figure 3-10 on page 51). We note the port-to-port isolation of better than 20dB in the scanning range, in the E-, H- and the cardinal planes. The impedance on the Smith Chart shows that at broadside the element is matched to lower system impedance. However, as the angles of incidence change, the impedance locus shifts from the broadside response toward the center of the Smith Chart. As mentioned, the smooth variation of the scan impedance and the location of the active VSWR for both polarizations provide additional benefits from an array T/R integration perspective in a circulator-free architecture. The element shows remarkable active impedance stability over the scanning range for both polarizations in all planes (see Figure 3-10 on page 51).

We illustrate the effect of the incident \vec{E} - field coupling into the radiating layers (see Figure 3-12 on page 54 and Figure 3-13 on page 54), and observe that the magnitude of the electric field is more pronounced for the geometry co-polarized with the incident \vec{E} -field.



Figure 3-12: Visualization of the electric field coupling into the first layer at broadside. Left: Coupling through the slot and the V-polarized geometry. Right: Coupling to the H-polarized geometry within the periodic unit cell.



V-Pol Excitation

H-Pol Excitation

Figure 3-13: Visualization of the electric field coupling into the second layer at broadside. Left: Coupling through the slot and the V-polarized geometry. Right: Coupling to the H-polarized geometry within the periodic unit cell.

3.3 Considerations for Finite Array Fabrication

The infinite array simulation provides a limited understanding of the active performance of the phased array system. It is well known [42] that in an infinite array environment Floquet currents have an equal magnitude and phase matching to that of the incident wave. The validity of this statement does not hold for finite arrays, where the array may excite currents with different magnitudes from the Floquet currents. Another reason that may alter the performance of the aperture is the truncation effect and the excitation of edge currents. While the infinite array model approximates the performance of elements in the center of very large arrays with uniform excitation, for a small finite array, the element performance may depart quite severely from the ideal response.

For the slot-coupled radiating element, the finite array poses a key challenge. At S-Band, manufacturing limitations preclude a finite array with more than 8x8 elements (64 dual polarized elements) due to panel size commercial limitations. Indeed, the rectangular grid for the element is set at 2" that translates into a 16"x 16" physical size. However, the IPA dual polarized aperture has low element to element coupling, as we will show in Chapter 4, that partially mitigates the truncation effects.

For finite array characterization, we place RF connectors behind each polarization for all elements. A surface mount connector carries the RF through a grounded coplanar waveguide on layer 1 through a via between layers 1 and 3 to the stripline antenna feed (Figure 3-14 on page 56). We maintain isolation between the antenna feeds through a cage ground via shield as shown between layer 1 through 3. The return loss is -15dB across the band of interest.



Figure 3-14: RF transition from the surface mount connector to the antenna stripline feed.



Figure 3-15: 5x5 finite array geometry for embedded element pattern. Left: Unit cell (shown here the first radiating layer). Right: 5x5 finite array simulation.
We simulate a 5x5 finite array in CST [46] using the Finite Different Time-Domain (FDTD) solver to investigate any anomalies in the embedded element pattern in all planes. Any anomalies may be indicative of surface waves excited in the substrate. At this point, we also add ground shield vias between each element to mitigate cavity resonances generated by the wall of vias introduced for stripline feed isolation.

We remark that the finite array simulation is limited to a 5x5 size because of the availability of computing resources. It is anticipated that better computing resources and more efficient numerical codes will lead to a better approximation of the behavior of the radiating element in a finite array environment.

We illustrate the simulated normalized element pattern in Figure 3-16 (page 56). In this simulation, only one element is excited, and a matched impedance terminates all other ports. There are no ground plane extensions to mitigate finite array effects. Notably, the element excited to the center of the array has at least one adjacent unit cell. The E-Plane patterns show a ripple in the finite array for both horizontal and vertical polarized elements, caused the by edge currents travelling along the dipoles on the aperture. The H-Plane patterns for both polarizations remains smooth.

The finite array simulation, where all elements uniformly excited, provides good correlation between simulation and measured data, as we will show in the next chapter.



Figure 3-16: Simulated normalized element patterns in a 5x5 array. Left: E-plane scanning for H- and V-Pol. Right: H-Plane element pattern for H- and V-Polarization.

After the finite array validation in a simulation environment, we fabricate the design using a commercial PCB vendor. In the following chapter we show the measured array performance.

Chapter 4: Measured Array Performance and Detailed Discussion

The slot-fed dual-polarized design operating from 2.7-2.9GHz from Section 3.2 is fabricated by a commercial PCB vendor. One of the main advantages of Integrated Planar Arrays is that fabrication is fully automated, requiring to send in the design files to the PCB house, wait for fabrication, and then receive the full array panel. For the S-Band radiator, a standard panel size of 18" x 24" is used. The PCB vendors want a perimeter clearance, typically around 1" inward from the panel, leaving a usable PCB area of 16" x 22". The rectangular antenna element is 2" on the side, for an effective aperture area of 16" x 16". Test structures for measurements are added in the remaining area, as we will show in Section 4.2 (see Figure 4-1 on page 59).

Moreover, the integrated planar aperture uses common substrate materials, namely Megtron6, broadening the vendor options for fabrication of the array. As such, with a wide range of options for manufacturing this aperture, we achieve a 75% cost reduction compared with a traditional planar array built on specialized RF laminates (see Figure 4-2 on page 60).



Figure 4-1: Panel footprint of the aperture PCB and with test structures.



Figure 4-2: Relative cost of the Integrated Planar Aperture (IPA) contrasted with a traditional patch radiator approach.

4.1 Finite Array Demonstrator for the Dual-Polarized Integrated Aperture

The 8 x 8 demonstrator has an area of 18" x 16", that includes the aperture (active) area of 16" x 16". It is 0.29" thick and has a weight of ~6.1 lbs. The active area has a 1" blank border at the edges of the array. The border has non-plated holes for a mechanical mounting fixture for pattern measurements in the indoor chamber (see Figure 4-4 on page 62). We remark that the demonstrator does not have any guard elements to mitigate any edge effects. The fabricated panel is mechanically and environmentally robust, with an integrated dielectric cover that protects the top metallization radiating layer. There is no warpage observed in the panel because of our choice in materials and proper balancing of copper percentages in the PCB stackup. This is contrary to the traditional foam-stacked radiators that have an unbalanced board construction. Moreover, with our monolithic dielectric construction, the aperture panel is compatible with automated pick and place processing of surface mount components and reflow.

We add surface mount SMPM connectors to the backside of the panel to access all elements of the array (see Figure 4-4 on page 62), and to characterize the RF performance of the elements. We note that at S-Band the footprint of the element is quite generous, and other families of RF connectors with a lower cutoff frequency can easily be considered for finite array characterization. However, in-house availability of discrete 50 Ω loads determined the choice of connector for this particular demonstrator. The 8 x 8 dual polarized panel requires 128 connectors for each antenna element port (see Figure 4-3 on page 61). We anticipate that in a fully integrated phased array system, the RF connectors will be replaced with surface mount T/R modules attached to the backside of the aperture panel.

	1	2	3	4	5	6	7	8
Legend Unit Cell J (purple) H- Pol J (orange)V- Pol	J1	J4	J6	J8	J10	J12	J14	J16
	J50	J5	J7	19	J11	J13	J15	J17
	9	10	11	12	13	14	15	16
	J32	J33	J35	J37	J39	J41	J43	J45
	J47	J34	J36	J38	J40	J42	J44	J46
	J48 ¹⁷	18 J49	19 J52	J54 ²⁰	J56 ²¹	J58 ²²	J60 23	J62 24
	J64	J51	J53	J55	J57	J59	J61	J63
	25 J65	26 J66	27 J68	J70 ²⁸	29 J72	30 J74	J 76 31	J78 32
	J80	J67	J69	J71	J73	J75	J77	J79
	33 J81 J96	34 J82 J83	35 J84 J85	36 J86 J87	37 J88 J89	38 J90 J91	39 J92 J93	40 J94 J95
	J97 41 J112	42 198 ا	J100 ⁴³ J101	44 J102 J103	45 J104 J105	46 J106	47 J108 J109	48 J110
	49	50	51	52	53	54	55	56
	J113	J114	J116	J118	J120	J122	J124	J126
	J128	J115	J117	J119	J121	J123	J125	J127
	57 J2 J31	58 J3 J18	59 J19 J20	60 J21 J22	61 J23 J24	62 J25 J26	63 J27 J28	64 J29 J30

Figure 4-3: Port designation for the aperture panel. Element #37 is chosen for the central element. Horizontal polarization is on port J88, and vertical polarization is on port J89.



Figure 4-4: Pictures of the 8x8 Dual-Polarized Integrated Planar Aperture. The finite array measures 18" x 16" with an active area of 16" x 16". Top: Aperture side of the panel. Bottom: RF connectors on the backside to enable full characterization of the planar aperture.

4.2 Considerations for Impedance Measurements

In order to validate the performance characteristics of the S-Band planar array, we begin with impedance measurements. For accurate impedance measurements, we employ a custom PCB thru-reflect-line (TRL) calibration kit [38]. This method does not use off-the-shelf, expensive coaxial short-open-load-thru calibration standards (SOLT), but rather it uses PCB transmission lines printed on the same aperture panel.

TRL is an effective method to remove systematic errors associated with imperfections in the equipment such connectors and cables. TRL calibration involves a two-port measurement that mathematically sets the reference measurement plane of the device under test (DUT). A simplified block diagram (see Figure 4-5 on page 63) shows the measurement setup on the network analyzer. After some mathematical manipulations [38], the *ABCD*-parameters for the DUT are:

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} \begin{bmatrix} A^m & B^m \\ C^m & D^m \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix}$$
(4-1)



Figure 4-5: TRL calibration kit for the network analyzer.

Using a TRL calibration procedure, the network analyzer automatically computes the DUT S-Parameters. Specifically, the TRL calibration method consists of a "thru" line, or a transmission line, a reflect standard (open or short), and a line with an electrical length of that sets the center frequency of the TRL defined as:

$$2\beta l_{phys} = \pi \tag{4-2}$$

where β is the propagation constant in the medium, and l_{phys} is the physical length. The operation bandwidth for the calibration kit is then:

$$[f_{low}; f_{high}] = \frac{c_0[l_{e-low}; l_{e-high}]}{2\pi\sqrt{\varepsilon_r}l_{phys}}$$
(4-3)

where $[l_{e-low}; l_{e-high}]$ are the electrical lengths corresponding to the frequency range $[f_{low}; f_{high}]$ of operation for the TRL calibration kit. The electrical length range is chosen between $[20^{\circ}-120^{\circ}]$. The other parameters in this equation are the speed of light, c_0 , and the effective permittivity of the medium, ε_r .

The PCB implementation of a TRL calibration method can be easily designed in three steps as follows:

- The thru-standard consists connects two transmission lines. For the S-Band panel, the RF path includes the connector, and the connector RF transition to the stripline antenna feed.
- 2. The line length is computed using equation 4-2 and the calibration kit is valid across the frequency bands defined in equation 4-3.
- 3. The reflect standard is either an open or a short (accomplished with a via to the RF ground).

Another advantage provided by this method is that typical dielectric thickness variations expected in fabrication is partially accounted in the calibration process. The TRL calibration kit effectively removes the effects of the RF connector, and the RF transition to the stripline. For the aperture panel, our TRL calibration kit sets the reference plane to the stripline feed that matches our reference plane in the electromagnetic simulations. This provides good confidence in the measurement to simulation correlation.

The TRL calibration kit for the aperture (see Figure 4-6 on page 65) has an operational frequency of 0.6GHz to 5GHz, with a center frequency set at 2.8GHz.



Figure 4-6: Fabricated TRL calibration kit for the aperture panel.

An additional test vehicle was added next to the aperture panel that contains a 5" long stripline to measure the line loss within the printed circuit board (see Figure 4-7 on page 65).



Figure 4-7: Test structure for line loss measurement.

After the calibration procedure outlined previously, the stripline loss was measured to be -0.1dB/inch at 3GHz using the test structure built (see Figure 4-8 on page 66). The stripline loss can be accounted in the pattern measurements of the antenna array.



Figure 4-8: Measured 5" stripline loss in Megtron6 substrate.

4.3 Impedance Measurements for the S-Band Aperture

In our investigation of the aperture RF performance, we first measure the passive return loss for a central element in the array. With the 2-port VNA calibration already done, mutual coupling measurements to all elements in the aperture are carried out. At any given time, two elements are excited in the aperture and all other elements are load-terminated in a 50 Ω . Because the panel has an even number of elements (8x8), there is no well-defined central element. We pick the ports J88/J89 as the central element 37 (see Figure 4-3 on page 61).

Passive Impedance Measurements

For the *H-polarized* element, the measured passive return loss is shown in Figure 4-9 on page 67. At 2.7GHz, the measured passive return loss for the central element is ~-19dB, and at the high end of the band is ~-9.5dB. We observe that the return loss is remarkably similar across the face of the array. In particular, even as we move toward the edge of the array, the passive return loss is not much different from the measured passive return loss of the central element (port J88 on element #37). This suggests that mutual coupling is low between the elements.



Figure 4-9: Measured passive return loss for the horizontally polarized elements across the face of the aperture. Blue solid line represents the measured passive impedance of the H-pol central element.

For the *V-polarized* element, a similar remarkable behavior in passive return loss is observed (see Figure 4-10 on page 68). At 2.7GHz, the measured passive return loss is ~-14dB, and at 2.9GHz, we return loss is -8.7dB for the central element (port J89 on element #37). Further, all vertical polarized elements show strong similarities in passive return loss with the central element.



Figure 4-10: Measured passive return loss V-polarized elements across the face of the array. Blue solid line represents the measured passive impedance of the V-pol central element.



Figure 4-11: Measured passive VSWR for the horizontally and vertically polarized elements across the face of the array. Passive VSWR measurements show stability of the element impedance versus the location of the element in the array.

As mentioned above, the elements exhibit stability of the passive impedance measurements across the face of array, as seen in the passive VSWR for all elements and for H- and V-polarizations in Figure 4-11 on page 69. Moreover, the measurements are repeatable. We observe there is good convergence of the passive impedance across the face of the array. That is, there is no impact of moving from the central element to the edge elements.

We also measure the mutual coupling relationship between the central element (#37) and all other elements, see Figure 4-12 on page 71 and Figure 4-13 on page 72. One port of the vector analyzer was connected to the central element, while the second port was moved from element to element across the face of the array. In total, 256 measurements were carried out to record the impedance response for each polarization. At all times, the elements not used in the measurement were load-matched. As expected, mutual coupling between elements is very low, with -10dB being the highest measured value for coupling, and all other measured coupling values were below a remarkable -20dB threshold.

During the mutual coupling measurements, an interesting relationship between the element under test and all elements in the aperture is observed. Mutual coupling is somewhat stronger between the central element and the first ring of surrounding elements This behavior is observed in the *E*-plane for the co-polarized ports, while stronger mutual coupling is observed for the cross-polarized ports, as expected.



Figure 4-12: Measured mutual element coupling for the H-polarized element (#37) in the center of the array and all other elements. Left: H-to-H port coupling. Right: H-to-V coupling.



Figure 4-13: Measured mutual element coupling for the V-polarized element (#37) in the center of the array and all other elements. Left: V-to-V port coupling. Right: V-to-H port coupling.



Figure 4-14: Passive return loss comparison between the 5x5 finite array simulation model and measurements.

The passive impedance measurements are our first step in the measurement to simulation correlation. This approach helps validate our design approach, simulation model, calibration method, and impedance measurements. As such, we plot the measured passive impedance measurement and compare it with the 5x5 finite array simulation employed in CST (see Figure 4-14 on page 73). The correlation shows excellent agreement between the 5x5 finite array simulation and actual measurements. The passive return loss referenced to the central element for both polarizations is remarkably similar.

Active Impedance Calculations

With the full passive impedance characterization for the dual-polarization panel, we can now compute an active reflection coefficient at broadside given by a summation of all mutual coupling coefficients seen by the excited element given by the:

$$S_{nn}^{active} = S_{nn} + \sum_{m=1}^{N} Smn$$
(4-1)

Here, the computed active return loss at broadside represents a summation between the coupling of adjacent elements in the array (m = 1 to N, $m \neq n$, and N is the total number of elements in the array) to the element under test and the self-impedance.

We compute the active return loss for the central element (#37). A comparison (see Figure 4-15 on page 75) to the simulation results of the unit cell in an infinite array environment is given. The computed active return loss for the horizontally polarized element shows better than -11dB and -13dB for the vertical polarization. Good agreement between simulation and measurement is observed due to low mutual element coupling (see Figure 4-16 on page 76).



Figure 4-15: Comparison with the simulation of the unit cell in HFSS and calculated from measurements active return loss for both polarization at broadside. Top: H-polarized element. Bottom: V-Polarized element.



Figure 4-16: Smith Chart of H- and V-pol calculated from measurement and simulated unit cell at broadside. Measurements are for a central element in the array. Top: H-pol results. Bottom: V-Pol results.



Figure 4-17: Computed broadside active impedance from measurements with the finite 5x5 finite array in CST for the central element. Top: Horizontally polarized radiating element. Bottom: Vertically polarized radiating element.

Moreover, computed active return loss at broadside and simulated active return loss in the 5x5 finite array environment (see Figure 4-17 on page 77). As with the unit cell in an infinite array environment from HFSS, excellent agreement is observed between measured and simulated data.



Figure 4-18: Comparison between measured H-V Coupling and simulated isolation in finite and infinite array environments.

Another interesting data point is the good agreement of the H-to-V port-to-port coupling in measurement and simulation. Coupling between H-V ports for the central element is -30dB or better across the band of interest.

To summarize our investigation in the impedance measurements, we show the computed active VSWR of the central element (Figure 4-23 on page 83). The computed active VSWR at broadside is < 2 for S-Band operation. Additionally, the mutual coupling

is very element, with somewhat more pronounced effect in the first adjacent ring of elements.



Figure 4-19: Computed active VSWR at broadside for H-pol and V-pol for the central element.

4.4 Measured Radiation Patterns for the S-Band Aperture

Having completed the full set of impedance measurements, we need to characterize the radiation characteristics of the S-Band aperture panel. In the first measurement, we add absorbing foam around the edges to mitigate any reflections from the metal mounting fixture attached to the backside of the array. There is no large metallic ground plane behind the array. We only had absorbing foam rated for X-band operation; however, we proceed with the embedded element patterns. For the array pattern measurements, the definition of the principal planes of the dual-polarized element is shown in Figure 4-20 on page 80. The array is in receive mode.



Figure 4-20: Definition of the principal planes for embedded element pattern measurements for the dual-polarized aperture at S-Band. Photograph of the aperture panel mounted in the indoor range.



Figure 4-21: Measured embedded element gain for the central element of the array. There is no extended metallic ground plane.

The E-Plane and H-Plane planes for the co-polarized and cross-polarized measurements are shown in Figure 4-21 on page 81. The measured co-polarized embedded

element patterns provide superb wide-angle coverage for the full bandwidth of interest. Both the horizontal and vertical element patterns are very similar, suggesting the element performs as predicted in simulations. Moreover, we maintain more than -25dB of crosspol isolation for the scan volume of interest. The radiating element performs as expected, with no noticeable ripples in the pattern, free of surface waves and no grating lobes and greater than 95-97% aperture efficiency, despite the small finite array size.

We plot (see Figure 4-22 on page 82) the measured peak gain against the directivity of the element to determine the aperture efficiency. The element directivity is commonly expressed in terms of the element effective physical area, A_{elem} , and the wavelength at the operational frequency λ_{op} as:

$$D_0 = \frac{4\pi A_{elem}}{\lambda_{op}^2} \tag{4-2}$$

Fortunately, at S-Band the mismatch losses are small, and we account here for all the losses, including the connector mismatch. The aperture efficiency approaches **95-97%**, accounting for error measurement.



Figure 4-22: Comparison between the measured peak gain and theory.



Figure 4-23: Measured embedded element pattern with extended metallic ground plane.

Another set of measurements (see Figure 4-23 on page 83) was carried out; this time with an extended metallic ground plane and absorbing foam around the edges of the panel in an attempt to quantify any differences in the cross-polarization patterns. We note, the foam was rated for operation at S-Band. The E-plane embedded element patterns are quite similar to the first set of measurements. However, we notice slight pattern ripples in the co-polarized patterns. Moreover, no noticeable differences are observed in the magnitude of the cross-polarized pattern measurements.

An insightful relationship can be derived between the scan loss and the embedded element patterns. Scan loss is a figure of merit commonly used by system engineers that aggregates all mismatch losses due to the variation of scan impedance with the pointing angle. A common expression for the element gain $g(\theta, \varphi)$, and the scan loss, *n*, is [35]:

$$g(\theta, \varphi) = \frac{4\pi A_{eff}}{\lambda_{op}^2} \cos^n(\theta)$$
(4-3)

The co-polarized gain patterns were plotted against an ideal cosine curve (see Figure 4-24 on page 85), with a scan loss of n = 1.3, for $f_{op} = 2.7$, 2.8 and 2.9GHz. As expected, the element has an impressive scanning capability up to $\pm 60^{\circ}$ from broadside. This is particularly important in a phased array system, as the aperture does not introduce an excessive amount of front-end losses.



Figure 4-24: Computed scan loss from measured embedded element pattern.

A common way to analyze array beam patterns is to apply the rule of pattern multiplication $[35]^4$. The embedded element pattern is multiplied with the array factor (*AF*). The AF [10] is a function of the steering angle, and for a linear array with uniform illumination is expressed as:

$$AF = \sum_{n=1}^{N} e^{j(n-1)\psi}$$
(4-4)

The phase shift between elements is $\psi = kd\cos\theta + \beta$. Here, k is the wave number, d is the separation between elements, and θ is the steering angle, and β is the progressive phase shift between elements. With this convention, we can compute the beam patterns for

⁴ The pattern multiplication rule is generally applicable to very large arrays, in which the measured embedded element pattern for the central element approximates the majority of elements in the array [35]. In [56], a small 7x7 array is shown to approximate a large array scan-blindness behavior.

an 8-element linear S-Band array (see Figure 4-25 on page 86). The computed beam patterns show three frequencies of interest at 2.7, 2.8 and 2.9GHz, and a theoretical element pattern ($\cos^{1.3} \theta$), where scan loss, *n*, is 1.3.



Figure 4-25: Computed beam patterns from the embedded element pattern for both polarizations in principal planes.

However, with analytically derived array beam patterns from the measured embedded element pattern (EP), there is little insight in how the planar aperture performs in an actual array environment. In particular, the pattern multiplication rule commonly applies to large element count arrays [35], where EP is stable across the center of the array. Fortunately, the team at Rockwell Collins developed a digital beamforming module under DARPA ACT program [47] that was available to test active beam patterns of the S-Band panel. 8 linearly polarized antenna elements from the S-Band panel were connected to the digital beamformer, with all other elements in the panel terminated in a matched load (see Figure 4-26 on page 87). Active array beam patterns were measured at 2.8GHz for the 8-element linear array. Here, we reproduce a set of the beamforming results reported in [48].



Figure 4-26: S-Band Array connected to ACT Common Module Development Kit in Rockwell Collins' far-field range. Reproduced from [48] ©2018 IEEE.



Figure 4-27: S-Band Panel active pattern measurements. Co-polarized beamforming measurements for horizontal and vertical polarization in receive mode when scanning from broadside to 70° in 10° increments. Reproduced from [48] © 2018 IEEE.

The normalized co-polarized beam patterns are shown in Figure 4-27 (page 88). The steering angle for this set of measurements is between $[0^{\circ} -70^{\circ}]$ in 10° steps, with a uniform amplitude taper. For the H-polarized element, the array beam patterns represent an E-plane cut. The V-polarized element, the H-plane beam patterns are illustrated. We note the remarkable similarity in both sidelobe levels and main beam performance for both polarizations, which is a requirement for the S-Band application and the main focus of this work.

4.5 Surface Waves and Grating Lobes in Integrated Planar Apertures

We have not addressed the topic of surface waves in planar arrays and the onset of grating lobes. These conditions occur when at least one higher order mode propagates in a periodic structure [43]. This section does not present new concepts; however, the intent is to apply a certain set of fundamental concepts to guide the initial design considerations for integrated planar arrays. For a rigorous discussion on surface waves and grating lobes, many excellent resources are available [42, 18, 38, 35, 49]. Specifically, we are interested in the relationship between the substrate thickness, dielectric constant and the unit cell size for an integrated planar array. A planar array on a grounded dielectric substrate supports a number of surface waves that may result in total reflection under certain scan conditions. This is a classical manifestation of scan blindness in a phased array. By contrast, grating lobes correspond to secondary beams that radiate in the visible space with the same intensity as the main beam.



Figure 4-28: Illustration of the array coordinate system and the 2-D element location for a planar array. The periodic planar aperture has a grounded dielectric substrate. The scanned

beam direction is (θ_0, ϕ_0) . Left: Spherical coordinate system. Right: 2-D grid for a periodic array in xy-plane.

Consider the planar array in the angle-space as shown in Figure 4-28 (page 89). We write the following spherical coordinate transformation in the (u-v) space as:

$$u = \sin \theta \cos \phi \qquad (4-5)$$
$$v = \sin \theta \sin \phi$$
$$z = \cos \theta$$

Because the main beam of the planar array scans in (θ_0, ϕ_0) direction, then the visible space of the array in *u*-*v* space is commonly expressed as:

$$\theta_{0} = (-90,90)^{\circ} \qquad \stackrel{def}{\longleftrightarrow} \qquad u_{0} = (-1,1) \qquad (4-6)$$

$$\phi_{0} = (-180,180)^{\circ} \qquad \stackrel{def}{\longleftrightarrow} \qquad v_{0} = (-1,1)$$

As such, the coordinate transformation projects the hemispherical scan volume of the array into a 2-D plane.

The spectrum of grating lobes as a function of the inter-element spacing [35] in the u-v space is given by an infinite summation of (m,n) modes:

$$u_{p} = u_{0} + \frac{p\lambda}{dx}, \qquad p = 0, \pm 1, \pm 2, \dots$$

$$u_{q} = v_{0} + \frac{q\lambda}{dy}, \qquad q = 0, \pm 1, \pm 2, \dots$$
(4-7)

Clearly, grating lobes enter the visible space when the inter-element spacing is larger than $\lambda_{hi}/2$. For the S-Band planar aperture array, the unit cell size is dx = dy = 2" in a rectangular grid. The unit cell size is set at $0.241\lambda_{2.9GHz}$, maximizing the available area of the unit cell for S-Band operation.

A typical a graphical representation of the interaction of the grating lobes with the visible space (u, v) = (-1, 1) is the grating lobe diagram. Moreover, we employ a combined grating lobe – surface wave (GL- SW) diagram to simultaneously determine the unit cell size and capture the interaction of surface waves with the propagating fundamental modes. In particular, a first order approximation for the excitation of surface wave in a planar array can be stated using well-known analytical expressions for surface waves excitation in a grounded dielectric slab [18, 38]. For the surface wave, the total reflection condition occurs when the propagation constant in an unbounded medium, β_0 , equals the propagation constant of the surface wave, β_{sw} . The surface wave couples into the fundamental propagation mode of the radiating element causing scan blindness when the following condition is satisfied:

$$\left(\frac{\beta_{sw}}{\beta_0}\right)^2 = \left(u_0 + \frac{p\lambda}{dx}\right)^2 + \left(v_0 + \frac{q\lambda}{dy}\right)^2 \tag{4-8}$$

Here, β_{sw} is extracted numerically from the transcendental equations of the transverse magnetic (*TM*) and transverse electric (*TE*) fields [18]. Furthermore, from (4-8), it is observed that for a grounded dielectric medium of a given thickness and dielectric constant, the propagation constant for a surface wave corresponds to a unit circle in the grating lobe diagram with a radius equal to the normalized propagation velocity of the surface wave to that of free space. We note that higher order surface wave modes may exist with increasing substrate thickness as shown in Figure 4-29 (page 92).

A study of the combined grating lobes and the surface wave diagram for different types of substrates, $\varepsilon_r = [2.2;3.65;10.2]$, corresponding to Teflon, Megtron6, and Rogers specialized RF laminate, respectively, is carried out (see Figure 4-30 on page 93) for the S-Band aperture with a substrate thickness $h_{sub} = 226.1 \ mil$ to obtain: $\beta_{sw}/\beta_0 = [1.018; 1.037; 1.119]$



Figure 4-29: Normalized surface propagation constant for higher order modes on a grounded dielectric medium as a function of substrate thickness. a) $\varepsilon_r = 2.2$, b) $\varepsilon_r = 3.65$, and c) $\varepsilon_r = 10.2$.


Figure 4-30: Grating lobe and surface wave diagram for the S-band element at 2.9GHz. The propagation constants of TM_0 surface wave mode for a dielectric constant, $\varepsilon_r = [2.2; 3.65, 10.2]$ is solved numerically. The main beam is scanned to $[\theta_0 = 60^\circ, \Phi_0 = 0^\circ]$.

For a substrate with $\mathcal{E}_r = 10.2$, the intersection of the TM_0 unit circle with the visible space indicates a resonance in the *E*-Plane for both polarizations. We note a range of resonances off-the principal planes are also possible. However, for the S-Band with an aperture height $0.055\lambda_{hi}$, where λ_{hi} is the wavelength in free space at 2.9GHz, only the fundamental TM_0 mode is supported. This leads to an initial variable design space for the radiating element to set the unit cell size, substrate material and overall thickness to avoid resonances of the surface waves and the propagating modes. We emphasize that this simple procedure makes no assumption on material loading in the stratified dielectric media for the planar array.

Finally, a compliance matrix for the objectives set for the aperture PCB is given in Table 4-1.

Requirement	Objective	Status
Antenna Element Lattice	Rectangular grid	Met
Polarization	Dual polarization	Met
Frequency	2.7 -2.9GHz	Met
Scan Volume	±45° off broadside	Exceed
Cross-Pol Isolation	-20dB	Exceed
Feed	50Ω	Met
Cost Objective / Element	\$\$	Exceed

Table 4-1: Compliance Matrix for the S-Band Aperture PCB

Chapter 5: Conclusions and Future Directions

5.1 Summary of this work

Three goals were set for this work. The first goal was to quantify the cost of current planar aperture technology. The second goal was to develop a reasonable set of fabrication guidelines for multi-layer planar apertures based on widely available dielectric materials. Lastly, two new dual-polarized planar antenna topologies are proposed to exploit commercial printed circuit board fabrication techniques and address cost and performance objectives.

Since its inception in 1973, the microstrip patch radiator has made a significant impact in the development of narrowband phased arrays. An extensive literature exists on the design and simulated performance of patch radiating elements. However, very few published works present the actual performance of the designed element in an array environment. Clearly, as most of the phased array designs were tailored to meet the needs for government applications. More significantly, less transparency is on the cost of the subsystem components, including the planar aperture developments. Recently, the exponential growth of commercial applications demanding phased array systems stimulated the development of more affordable sub-components for array systems, from IC developments and multi-layer printed circuit technology advancements. Less attention has been given to the aperture itself, rather, PCB apertures in today's phased array systems are still rooted on outdated aperture design methodologies.

An intention of this work has been to investigate the applicability of current PCB technologies in aperture development, cost reduction practices and performance challenges. To this end, a complete aperture design methodology and measurements set for

the fabricated panel are presented. It is the belief of this author that opportunities for aperture performance improvements still exists.

To complete our analysis, an overview of the chapters is presented here.

Chapter 1 presented a historical overview of phased array technologies for radar and communication systems from an aperture perspective. As discussed, many literature examples focus on the performance of the elements. Few works address the affordability aspect of the aperture.

Chapter 2 investigated current manufacturing practices and the applicability of current trends in printed circuit technology for aperture design. We also presented relevant feeding techniques for an integrated planar element. We developed a fairly simple set of design guidelines for planar aperture development based on manufacturing constraints with a focus on lower frequencies. We introduced the printed circuit board stackups for the proof of concept developments presented in the subsequent chapter.

Chapter 3 presented the design of two novel aperture designs, which we refer as Integrated Planar Apertures (IPAs). The first design is a pin-fed coupled dual-polarized element with VSWR<3.1 and scanning capability up to $\pm 45^{\circ}$ in all planes, but poor port-to-port isolation. We then focused on the development of a new dual-polarized radiating element employing a slot-feed technique. The element achieved VSWR<2.1, enhanced port to port isolation of -40dB at broadside and enhanced scanning capability to $\pm 50^{\circ}$ in all planes. The radiating element leveraged conventional manufacturing techniques. Notably, the substrate material for the aperture leverages FR-4 type materials, which is compatible with modern printed circuit technology processing and assembly. This broadens the manufacturing base for the aperture PCBs, reducing the cost of the aperture. We anticipate

as we march toward smaller and more integrated systems, an increase in the demand of an affordable integrated aperture approach with no performance compromise.

Chapter 4 presented the measurements of the fabricated 8x8 aperture demonstrator. We illustrate a calibration technique for the integrated planar aperture (IPA). This includes fabrication of a custom TRL kit on the aperture panel for antenna impedance measurements and correlation to simulation data. Embedded element patterns are presented for the finite array, with a quantitative measurement comparison between the aperture with an extended metallic ground plane and without an additional ground plane. Moreover, we provided active beam patterns for the aperture panel with a digital beamformer to fully validate our aperture. A cost comparison and scanning performance achieved with our approach is given in Figure 5-1.



Figure 5-1: Scanning volume of current planar narrowband apertures and their relative cost.

5.2 Future Work

Several opportunities for continuing the development of integrated planar apertures exist:

- Moderate bandwidth extensions are achievable. The main requirements for this work were to maximize scanning range, aperture efficiency, cross-pol isolation, and to minimize cost for the S-Band application. However, the pin-fed design showed 25.5% fractional bandwidth potential. Further work should be taken to maximize the bandwidth for this design and improve isolation. It is also envisioned that linearly polarized applications with moderate bandwidth requirements may benefit from this extension.
- High frequency extensions for this work are possible in the realm of current printed circuit technology, especially for 5G developments. Proposed spectrum allocations for 5G suggest a narrowband IPA design will be well suited for integration in these system.
- 3. Coupled element extensions may also be possible to extend the bandwidth of the element. It is well known that mutual coupling is in fact beneficial for UWB antenna topologies. This effect has not been studied for these designs.
- 4. Finally, an optimization algorithm for the element needs to be developed. The topic of an equivalent circuit for IPA has been ignored in this work, as the geometry of the element does not permit a quick extraction of an equivalent circuit topology. It is possible that a generalized scattering matrix approach may work well for this extension.

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