ABSTRACT

Title of Dissertation: EFFECTS OF GLASS/EPOXY INTERPHASES ON ELECTRO-CHEMICAL FAILURES IN PRINTED CIRCUIT BOARDS

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Reduction in printed circuit board line spacing and via diameters and the increased density of vias with higher aspect ratios (ratio between the thickness of the board and the size of the drilled hole before plating) are making electronic products increasingly more susceptible to material and manufacturing defects. One failure mechanism of particular concern is conductive anodic filament formation, which typically occurs in two steps: degradation of the resin/glass fiber bond followed by an electrochemical reaction. The glass-resin bond degradation provides a path along which electrodeposition occurs due to electrochemical reactions. Once a path is formed, an aqueous layer, which enables the electrochemical reactions to take place, can develop through the adsorption, absorption, and capillary action of

moisture at the resin/fiber interphase. This study describes the experimental and analytical work undertaken to understand the glass-resin delamination and the methods used for analyzing this critical interphase.

This study shows that a smaller conductor spacing in reduces the time to failure due to conductive anodic filament formation and that the plated-through-hole to plated-through-hole conductor geometry is more susceptible to conductive anodic filament-induced failures than plated through hole to plane geometries. The results also show that laminates with similar materials and geometries with a 45-degree angle of weave demonstrate a higher resistance to conductive anodic filament formation compared with a 90-degree angle of weave.

The study is the first of its kind conducted on FR-4 printed circuit board materials where the pathway formation due to breakage of the organosilane bonds at the glass/resin interphase was evaluated. Using techniques such as force spectroscopy, micro-Fourier transform infrared spectroscopy, scanning quantum interface device microscopy and focused ion beam, evidence of bond breakage and a pathway formation was revealed, poor glass treatment, hydrolysis of the silane glass finish (adsorption of water at the glass fiber/epoxy resin interphase) or repeated thermal cycling contribute to the bond breakage. The technique of applying in-situ resistance measurements during cross-sectioning analysis of printed circuit boards suspected of conductive anodic filament is the first time this method is described in the open literature. This solution addresses the potential problem in destructive physical analysis of grinding away the evidence of the CAF filament and ultimately loosing evidence at the failure site.

By applying a subset of the evaluation criteria described in this research, an upfront evaluation of printed circuit board materials can be performed for susceptibility to electro-chemical migration and other failure causes in PCBs that are attributable to the glass/resin interfacial adhesion. Manufacturers can identify board suppliers based on answers to and validation of a series of questions. These questions focus on the necessary requirements of reliable board material manufacturing and are independent of the specifications of the product.

EFFECTS OF GLASS/EPOXY INTERPHASES ON ELECTRO-CHEMICAL FAILURES IN PRINTED CIRCUIT BOARDS

by

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2018

Dedication

I dedicate this thesis to my wife Reena, and my children Zoya and Yuvaan. Thank you Reena for believing in me, you are a constant source of support and encouragement. I am truly thankful for having you in my life.

A special feeling of gratitude to my loving parents, Mrs. and Col. Bhupender Kumar Sood and my sister Bhawna whose words of encouragement and push for tenacity ring in my ears.

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In many ways, this dissertation reflects the culmination of the last fourteen years of my time spent at the University of Maryland as a staff member, as CALCE Laboratory Director and as a student. I would be remiss not to thank those who have provided guidance and have helped shape me into the person I am today. Without question, I would like to start by acknowledging the support and guidance provided to me by my advisor, Professor Michael Pecht, for helping me with his technical acumen, challenging me and constantly providing new perspectives. I would like to thank my committee members, Professor Bongtae Han for his encouragement, Professor Patrick McCluskey, Professor Peter Sandborn, Professor Lourdes Salamanca-Riba and Dr. David McElfresh for their valuable guidance and agreeing to become my dissertation committee members.

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Chapter 1: Introduction

1.1. Printed Circuit Boards

Printed circuit boards (PCBs) are the baseline for electronic packaging upon which electronic components are formed into electronic systems. PCBs are used in a variety of electronic circuits from simple one-transistor amplifiers to large super computers. A PCB serves three main functions:

1) it provides the necessary mechanical support for the components in the circuit

2) it provides the necessary electrical interconnections, and

3) it bears some form of legend that identifies the components it carries.

Printed circuit boards can be classified into three categories based on their construction and physical characteristics, namely rigid, flexible and rigid-flex boards. Rigid circuit boards are basically a composite layered structure in which solid copper sheets are laid down and separated with a dielectric material, which is commonly an epoxy resin system. Rigid boards represent the most widely used category and they can be built from different materials systems. Flexible printed circuits consist of thin copper foil bonded to a thin plastic base. The base material most frequently used is polyester film. This type of board is usually limited to a single- or double-sided board and only for very small components. The third category is the rigid-flexible boards which is a combination of rigid and flexible

boards bonded together. The rigid portion supports the components while the flex portion allows the structure to be folded. Attention will be given to the rigid printed circuit boards since they represent the highest volume and it is within this category that the major challenges in terms of fabrication, materials, and applications are encountered.

Rigid printed circuit boards can be further categorized in terms of circuit complexity and base materials. Circuit density can force the design to be single-sided, double-sided, or multi-layer. A single sided board has circuit layout on one side only, while the double sided board has artwork on both sides. On double sided boards, connections between the two layers are made with small conductive holes called "vias". A multilayer board has artwork on one or more internal layers in addition to the top and bottom. Schematic drawings of the three types of boards are shown in

Figure 1.

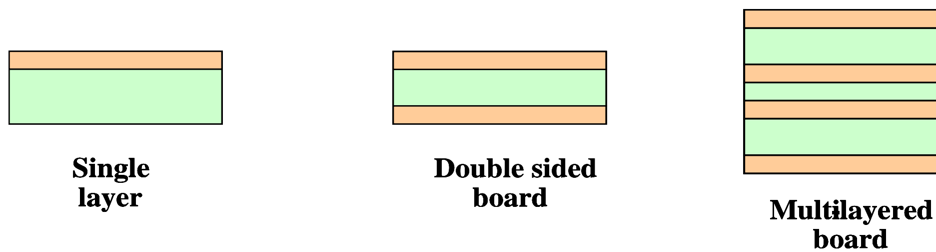


Figure 1 Schematic representation of single, double, and multi layer boards.

1.2. Materials and Processes

Rigid printed circuit boards can be made up of different base materials combinations. Each material group provides key characteristic parameters and important advantages for different applications. Ceramic materials such as aluminum oxide, aluminum nitride, and glass ceramic are used as substrates and metal circuit traces are screen printed on top of the substrate. The whole system is then fired to obtain a single monolithic ceramic circuit board. Boards with silicone resin based substrates are used mainly when low characteristic impedance is required at high frequencies, for example in transmission lines, filters, and oscillator circuits. The third type of base material used for PCB fabrication is from the organic family, where the low cost phenolic resin reinforced with paper is used for low end applications and epoxy resin reinforced with woven glass cloth is used for mid and high end applications.

The epoxy glass composite is manufactured by impregnating rolls of woven glass cloth with resin, and then laying up the necessary number of layers of impregnated cloth between sheets of copper foil and pressing in hydraulic presses. In today's electronics, glass based materials are generally used. These are covered by NEMA (National Electrical Manufacturers Association) specifications and summarized in Table 1: G_2, G_3 (Phenolic resins), G_5(Melamine), G_{10}(Epoxy), G_{11}(heat resistant epoxy), FR4 and FR5 which are flame retardant versions of G_{10} and G_{11}

respectively. The most common material system is the FR4 which gives the best balance of electrical and mechanical properties, with the best bond between the resin and the glass fibers and between the resin and copper cladding [1].

Table 1 Basic NEMA classification for commonly used materials [2].

XXXP	Phenolic / Paper
XXXPC	Phenolic / Paper, cold punching
FR_2	Phenolic / Paper, flame resistant
FR_3	Epoxy / Paper, flame resistant
G_{10}	Epoxy / Glass, general purpose
G_{11}	Epoxy / Glass, temperature resistance
FR_4	Epoxy / Glass, general purpose, flame resistant
FR_5	Epoxy / Glass, general purpose, temperature and flame resistant

FR-4 is a composite of epoxy resin with woven fiberglass reinforcement and is the most commonly used PCB laminate material type. The typical constituents of a FR-4 laminate is given in Table 2. In addition to these constituents, copper is generally used as the conductor material in a built up circuit board. The steps involved in FR-4 laminate fabrication are shown in Figure 2 [3]. Glass fibers are made out of glass raw materials and a coupling agent is coated onto them prior to weaving the glass fabric. A single ply of glass cloth when impregnated with the semi-cured resin is called prepreg. Multiple prepregs are thermally pressed to obtain a core or laminate.

Copper foil is then electrodeposited to obtain a copper clad laminate. The laminate is further processed with solder mask and design data to obtain a single or a double layered PCB. Several prepregs and cores are stacked together under temperature and pressure conditions prescribed by laminate manufacturer to obtain a multi-layered PCB [4].

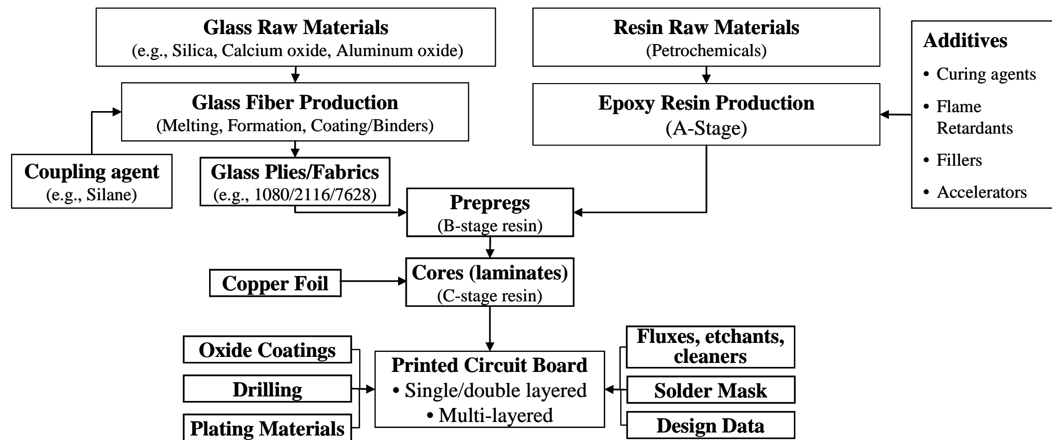


Figure 2: FR-4 Laminate Fabrication [69]

Table 2: Typical constituents of FR-4 laminates [69].

Constituents	Major Function(s)	Example Material(s)
Reinforcement	Provides mechanical strength	Woven glass (E, S, A or C grade) fiber
Resin	Acts as a binder and load transferring agent	Epoxy (DGEBA)
Curing Agent	Enhances linear/cross polymerization between the resin and reinforcement	e.g., Dicyandiamide, Phenol novlac, Xylok
Coupling Agent	Bonds inorganic glass with organic resin and transfers stresses across the matrix	e.g.,Organo silanes $Y\text{-}(CH_2)_n\text{-}Si\ (OX)_3$ (Y-organo functional group; OX- silicon functional group)
Flame Retardant	Reduces flammability of the material	Halogenated (TBBPA) or Halogen-free (Phosphorous compounds)
Fillers	Reduces thermal expansion, increases flame retardancy	e.g., Aluminum silicate, Mica
Accelerators	Increases reaction rate, reduces curing temperature, controls cross-link density	e.g., Organophosphine, Imidazole, BF3 amine complex

1.3. Constituents

The constituents of FR-4 laminates are discussed below. Each of these constituents are important in its own, and in combination they determine the properties of the laminates.

1.3.1. Glass Reinforcements

Glass fibers are widely used in reinforced PCBs because they are inexpensive to produce and have relatively good strength to weight characteristics. In addition, glass fibers also exhibit good chemical and fire resistance. Electrical (E) glass, a low-alkali composition which exhibits an excellent balance of electrical insulation

properties and good resistance to water, is the most widely used reinforcement material for cost effective electronic applications (see Table 3 for typical composition of e-glass).

Table 3: Typical composition of E-grade glass

Constituent	Composition (%)
Silicon dioxide (SiO_2)	52-56
Calcium oxide (CaO_2)	16-25
Aluminum oxide (Al_2O_3)	12-16
Boron oxide (B_2O_3)	5-10
Sodium oxide (Na_2O) + Potassium oxide (K_2O)	0-2
Magnesium oxide (MgO)	0-5
Iron oxide (Fe_2O_3)	0.05-0.4
Titanium oxide (TiO_2)	0-0.8
Flourides	0-1

Manufacturing of glass fiber begins with the dry mixing of silicas, limestone, clay, and boric acid in appropriate proportions. A homogeneous melt composition with negligible impurities is necessary for the successful manufacture of glass fibers. Solid inclusions of even sub-micron dimensions can act as stress concentrators that reduce the fiber strength.

After the molten glass is poured into the bushing, glass fibers are produced by drawing a solidified filament of glass from a molten drop. The diameter of a glass fiber is typically between 5 and 25 microns. During drawing, any seeds present will become attenuated and elongated, forming capillaries several meters long in the glass filaments and effectively creating hollow fibers. These hollow fibers provide

a path for conductive anodic filament formation [3][59]. A schematic of the glass fiber fabrication steps in shown in Figure 3. Sizing agents, which are applied to the individual glass fibers after they are formed (binder formulations) are discussed later in this chapter.

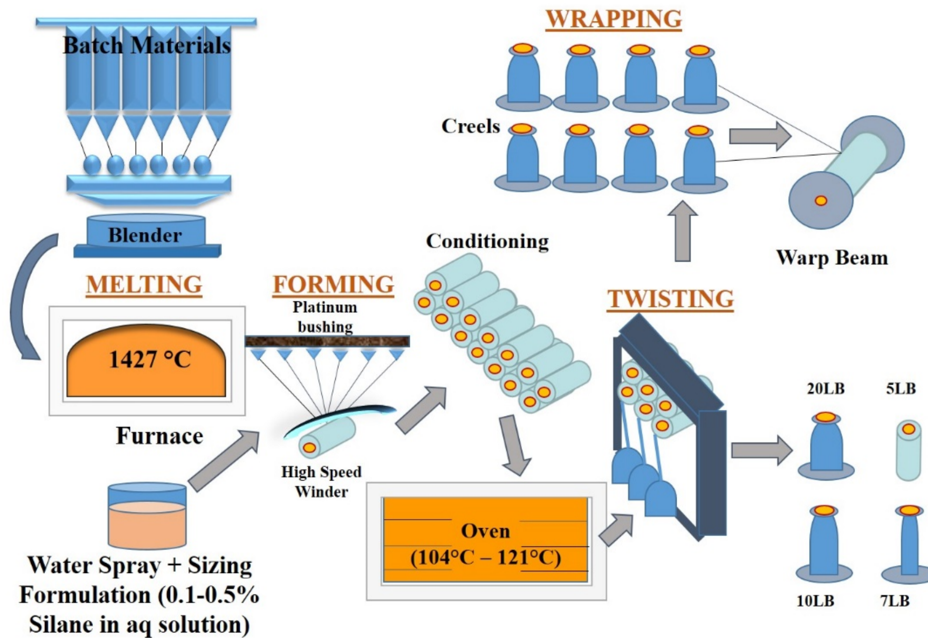


Figure 3 Schematic showing the glass fiber fabrication steps [8][9].

Glass fabric consists of two sets of fiber bundles, warp bundles are the initial set of parallel fiber bundles and fill bundles are woven through the first set to form a fabric. Changes in the tension and spacing of these bundles during weaving result in varying degrees of crimp (waviness) and hence different properties along both directions. Parameters such as glass fiber bundle diameter, number of fiber bundles

used and linear density of the fabric define the type of glass-weave style. Typical glass-weave style numbers used in PCBs are 1080, 2116 and 7628. The difference in their fabric styles is represented in Figure 4.

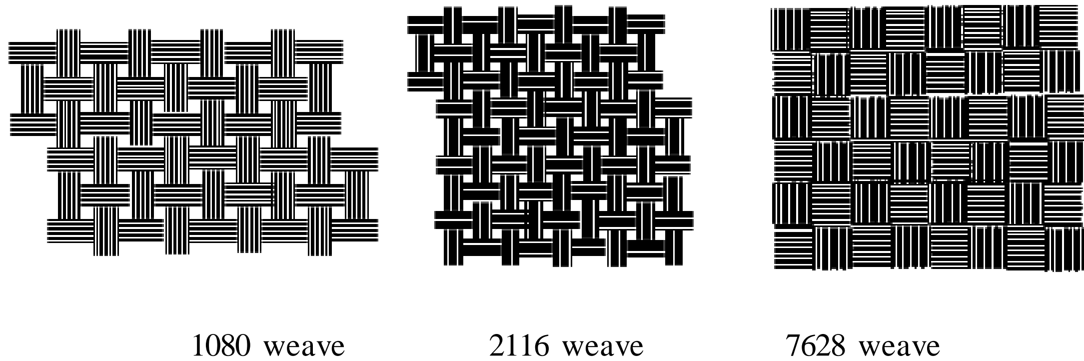


Figure 4: Typical glass-weave styles

1.3.2. Resin System

The function of a resin system in a laminate is to hold the fibers in place, bind the fibers, provide thermal stability to the composite structures and provide interlaminar toughness. The resin system used in FR-4 laminates primarily consist of bi, tetra or multi-functional epoxy groups. The resin is derived from the reaction of Bisphenol-A with Epichlorohydrin which creates a "Diglycidyl Ether of Bisphenol A" called DGEBA. It is also referred to as an oxirane (shown in Figure 5).

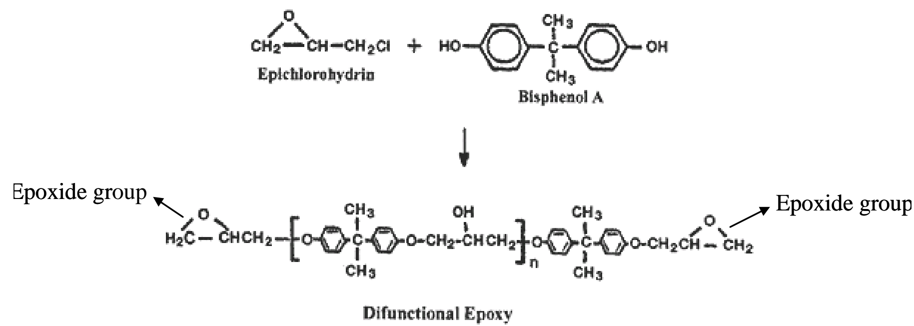


Figure 5: Formation of DGEBA

The epoxy groups present in DGEBA react in subsequent resin polymerization and result in curing of the resin system [3]. Higher cross-linking in the cured system is achieved by the use of epoxy monomers with more than two epoxy functional groups per molecule (shown in

Figure 6). Additives such as curing agents, flame retardants and fillers are added to the resin system to improve the performance of the laminate.

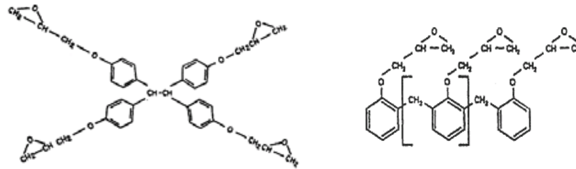


Figure 6: Tetra-functional and multi-functional epoxy monomers.

1.3.3. Interphases Between Resin and Glass

The interphase between the glass and resin is a three-dimensional region between the bulk fiber and bulk resin. It includes not only the area of contact (interface)

between the fiber and the matrix, but also a region of some finite thickness extending on both sides of the interface in both the fiber and resin matrix (interphase) [4]. A schematic illustration of the glass-resin interphase is shown in Figure 7 with a cross-section of PCB shown on left and a detail of the region at the fiber surface shown on the right.

The interphase comprises the functional interlayer and the part of the epoxy resin affected by the presence of the silane coated fiber. The coated interlayer improves compatibility between the glass fiber and the resin matrix by forming a strong but tough link between both phases. This interphase will be the subject of further discussion in chapters 2, 3, 4 and 5.

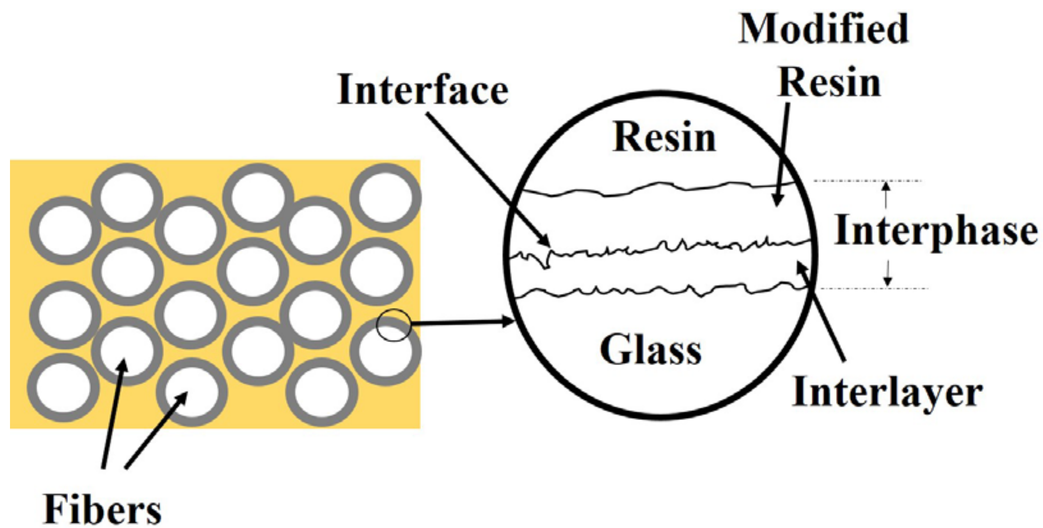


Figure 7 Schematic illustration of the glass-resin interphase.

Various types of interphases can exist such as mechanical, chemical or physical. A mechanical interphase between the glass and resin matrix comprises of a lock and key (based on the surface morphology) mechanism which is dictated by surface roughness, porosity, resin viscosity etc. For example in a physical interphase, phenomenon such as interdiffusion entanglement, electrostatic energy, polar and Van-der-Waal bonding can act on the surface of the fibers.

Glass fiber to resin matrix adhesion quality will vary for different systems. The surfaces of the glass fibers can be roughened which improves adhesion and improves friction with the resin matrix. The roughening can be done by methods such as chemical etching, which produces microscopic and macroscopic features that enhance adhesion with the resin matrix. Other treatments include argon induced roughening, and oxygen plasma based cleaning of the glass fiber surfaces.

The glass resin adhesion is necessary because this interphase dictates transverse mechanical properties of the PCB laminate, its through thickness or bulk properties including delamination resistance, fatigue resistance, resistance against CAF. Sources of residual stresses along the glass resin interphase are the thermal mismatches that exist along the interphase, glass with a smaller coefficient of thermal expansion (CTE) is subject to compressive residual stresses and resin which has a larger CTE is subject to tensile residual stresses.

Glass fiber treatments tend to be geared towards the removal of weak fiber boundaries, removal of contaminants and offer to moderate the excessively high interphase stresses. The coatings can add an intermediate modulus layer or add an elastomer layer. Treatments of the glass can also provide variations in the surface topography or mechanical locking. Wettability of the surface is important, in case the glass fiber surface is wettable, the matrix angle Θ is less than 90°, when the matrix angle Θ is greater than 90°, the fiber to matrix adhesion is poor.

Resin to glass interactions include molecular adsorption into the matrix, penetration into the matrix, fiber catalytic effects and fiber surface induced crystallization of the resin matrix.

1.3.4. Sizing Agents

The sizings are a multifunctional coating applied to perform a number of functions. The application process of the sizings consists of creating a form of a suspension in an aqueous solution and this mix limits the constituents that can be mixed in with the sizing agents. A schematic showing the glass fibers that are being drawn from the forming bushings into the sizing applicator roll for processing is shown in Figure 8. Within a few seconds after the glass fibers are formed and drawn out of the platinum bushings, water is sprayed on the glass fibers. Water is preferred as it wets glass easily and fast yielding a good dispersion of the sizing [5].

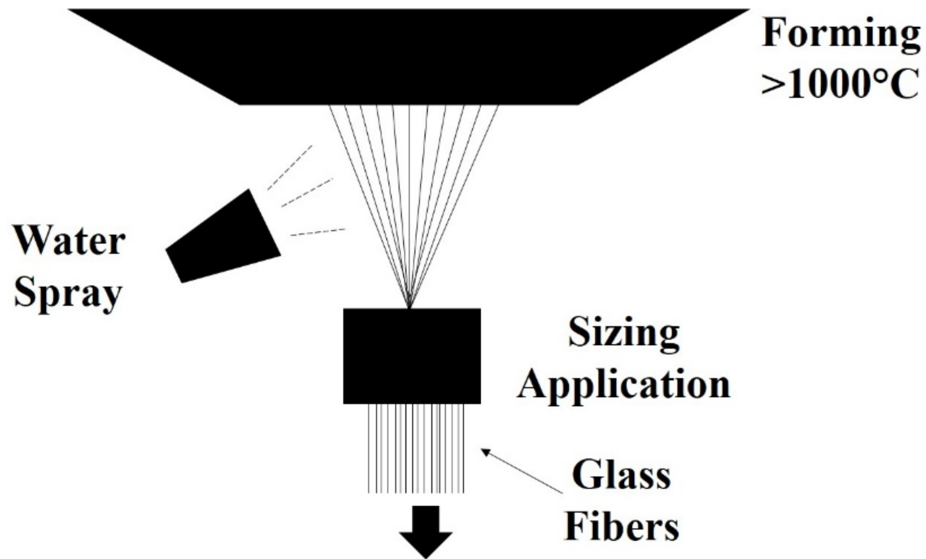


Figure 8 Schematic showing the glass fibers being drawn from the forming bushings (top) into the sizing applicator roll (bottom) and further for processing [5].

The primary function of the sizing is to protect the glass fiber surface against damage due to fiber-fiber contact when the glass is wound into a strand in order to continue the processing and handling, other attributes include reduction in fuzz during handling, provide good wetting during laminate manufacture with a low void content as a result, facilitate high fiber matrix interaction for successful stress transfer and low cost [6] [7]. While the exact recipes of the sizing agents are proprietary within individual companies, the types can broadly be classified as follows:

- Aminosilanes
- Epoxy Silanes

- Vinyl Silanes
- Methacryl Silanes
- Alkylsilane
- Phenyl Silane
- Chlorosilane

Most sizing consists as a minimum of a film former and a coupling agent, but often many more components. The film former protects against fiber-fiber damage and protects the whole fabric during production. A sizing is often chosen to be similar to the PCB epoxy matrix in order to obtain a good wetting. Anti-static agents, emulsifiers and lubricants are added to reduce fuzziness, to stabilize insoluble components in the suspension and to further improve the dispersion and protect the fibers. When the reaction of this sizing and the glass takes place, a covalent bond is formed between the silane coupling agent to the fiber surface.

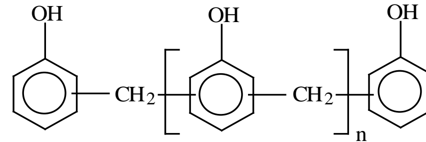
It is known that the process of pre-curing the sizing agent further condenses the Si-OH groups of the coupling agent to Si-O-Si linkages [73]. The results of the above reactions between the coupling agent and the epoxy resin indicate that the physical state and processing conditions of the coupling agent can drastically effect the reaction. First, the coupling agent should not be pre-heated before the epoxy resin is added [74] . Pre- heating only further condenses the coupling agent interphase

reducing the penetration of the resin into the coupling agent interphase. Second, the reaction temperature must be kept under 115°C or some of the primary amines of the coupling agent will be oxidized to imine groups [74]. Third, as a corollary of the first two, penetration of the resin into the silane interphase along with the chemical reaction is important and these two processes must be optimized to improve the mechanical properties of the composite materials.

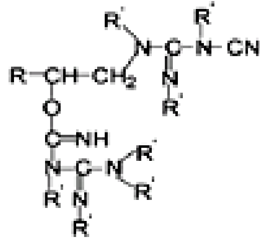
1.3.5. Curing Agents

Curing agents are added into the resin matrix to enhance cross-linking thereby thermosetting the composite structure [3]. They are usually aliphatic or cycloaliphatic amines and polyamines or amides. The most widely used curing agents in the PCB industry are dicyandiamide (commonly known as dicy) and phenol novolac (phenolic). The chemical formulae of dicy and phenolic curing agents and typical molecular structures of the cured resin systems are shown in Figure 9.

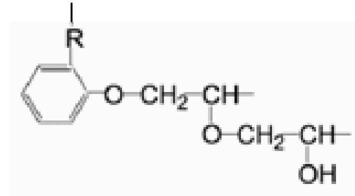
Dicyandiamide (DICY)



Phenolnovolac (Phenolic)



Dicy cured resin



Phenolic cured resin

Figure 9: Typical structure of dicy and phenolic cured systems.

The properties of dicy and phenolic cured systems differ because of the nature of their molecular structures. Dicy and its cured resin systems are linear aliphatic molecules compared to the aromatic structure of phenolic and its cured epoxy systems. This makes the phenolic cured systems more thermally stable than dicy cured systems. Dicy cured systems are more hygroscopic than phenolic cured systems due to the presence of highly polar carbamidine-carbamide bond in their chemical structure. At higher temperatures the strong polar nitrogen atom present in the dicy cured system can destabilize the brominated epoxy resin resulting in the production of corrosive bromide ions [11]. Overall, phenolic cured resin systems offer better thermal resistance, chemical and humidity resistance as well as, improved mechanical properties but poor processability (e.g., drilling) when compared to dicy cured systems.

1.3.6. Flame Retardants

Flame retardants are added into the epoxy matrix to reduce flammability of the laminate material. Tetrabromobisphenol A (TBBPA) (Figure 10) is the most commonly used halogenated flame retardant for epoxy resin systems. Bond energies of the various bonds in the polymer matrix are as shown i

Table 4.

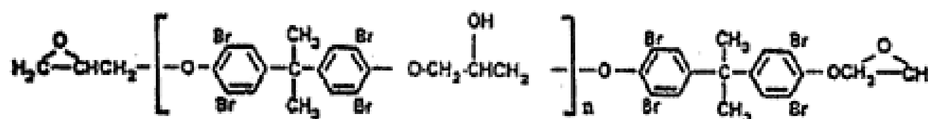


Figure 10 Tetrabromobisphenol A (TBBPA).

Table 4: Typical bond energies

Bond	**Bond energy (kJ/mol)**	**Temperature above which degradation starts (°C)**
C_{arom} – Br	335	360
C_{aliph} – C_{aliph}	340-370	400
C_{aliph} – H	390-436	>500
C_{arom} – H	469	>500

Brominated flame retardants (BFRs) are halogenated flame retardants that break down and releases bromine radicals (Br•) because of the lower C-Br bond energy

compared to other bonds [15][16]. These radicals react with the surrounding polymeric material (RH) and the resulting reaction releases hydrogen (H) from the functional group (R•) to form hydrogen bromide (HBr). Hydrogen bromide (HBr) in turn interferes with the radical chain mechanism by reacting with the high energy H• and OH• radicals. Highly reactive H• and OH• radicals are trapped and chain reaction leading to combustion is stopped. Thus, BFRs decompose during ignition, and retard combustion by trapping radicals generated from resins and by forming gas-phase barriers against oxygen [14].

Halogen-free flame retardant epoxy systems are gaining importance because of the environmental concerns involved with halogenated flame retardants. Phosphorous compounds (organophosphate esters or inorganic red phosphorous) and metal hydroxides (hydroxides of aluminum and magnesium) are some of the commonly used halogen-free flame retardants. Organophosphate esters works by forming flame retarding glass-like barriers on the resin surface during ignition thereby cutting off oxygen necessary for combustion. Metal hydroxides retard flames by absorbing the heat during ignition.

Fillers are added in the laminate systems for specific performance requirements such as reducing out-of-plane coeffecient of thermal expansion (CTE) and to prevent barrel cracks in plated through holes. Fillers are also added to enhance the

flame retardancy to meet UL 94V-0 flammability rating and to reduce material costs (as they replace resin) [19].

1.4. Lamination Process

The weave fabric is impregnated with epoxy to form a laminate. Environmental scanning electron microscope (ESEM) micrograph of a 6 ply 7628 glass weave laminate is shown in Figure 11. During the lamination process the thin-core inner-layers are subjected to heat and pressure and compressed into a laminated panel. Sheets of material consisting of glass fibers impregnated with epoxy resin, known as pre-preg or b-stage, are slipped between the layers and bond the layers together. Pre-preg is available in different styles with varying ratios of resin to glass fibers. This choice of differing epoxy resin to fiber glass ratios allows the manufacturer to control the thickness between layers and to provide the appropriate amount of resin flow between circuitry. Lamination steps are fairly consistent among manufacturers. In lamination, the pressing parameters must closely match what the laminator recommends. If the heat rise of the pressed book is not maintained as per manufacturer's specifications, the resin will not have enough time to properly wet-out the cores that are being pressed [1]. Laminate voids or other lamination defects may occur as a result.

One lamination process is a Standard Hydraulic Lamination. Steam press, hot oil press, or electrical resistance heaters are common elements used in this process to

provide heat to the stack. Using the steam and hot oil method allows for a higher heat rate to be achieved but the maximum temperature reached is relatively low. A caution for the steam press is the lamination temperature may not be met during a typical lamination process.

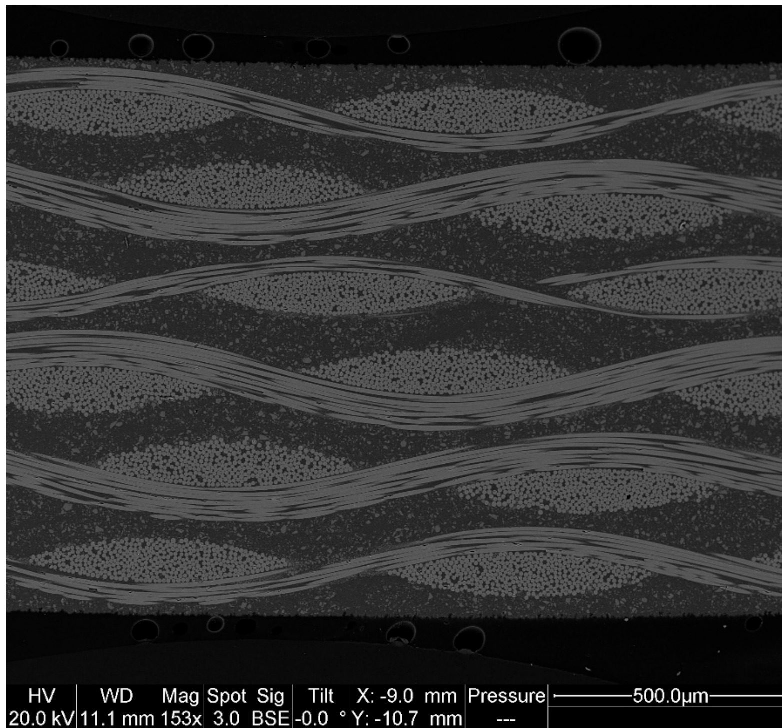


Figure 11 Typical 6-ply 7628 weave stack up.

The second process is Vacuum-Assisted Hydraulic Lamination (VAHL). This is the most widely accepted process practice in the industry today. Before the lamination process occurs a vacuum cycle 15 to 60 minutes occurs where moisture, air, and other volatiles are pulled out from the PCB stack. Note that this is very different from a pushing out method as utilizing a pushing out method can still

cause volatiles to be trapped in the finished PCB. Then follows a typical Hydraulic Lamination process. An overview of the time, temperature and pressure relationship used during the lamination process is shown in Figure 12. The vacuum cycle helps lower the pressure need for lamination. A lower pressures can help reduce the effect of misregistration by roughly a thousandth to two thousandth of an inch. In the world of electronic packing this is very substantial and can allows even smaller traces to be created and increase the amount of signals in a layer on a board.

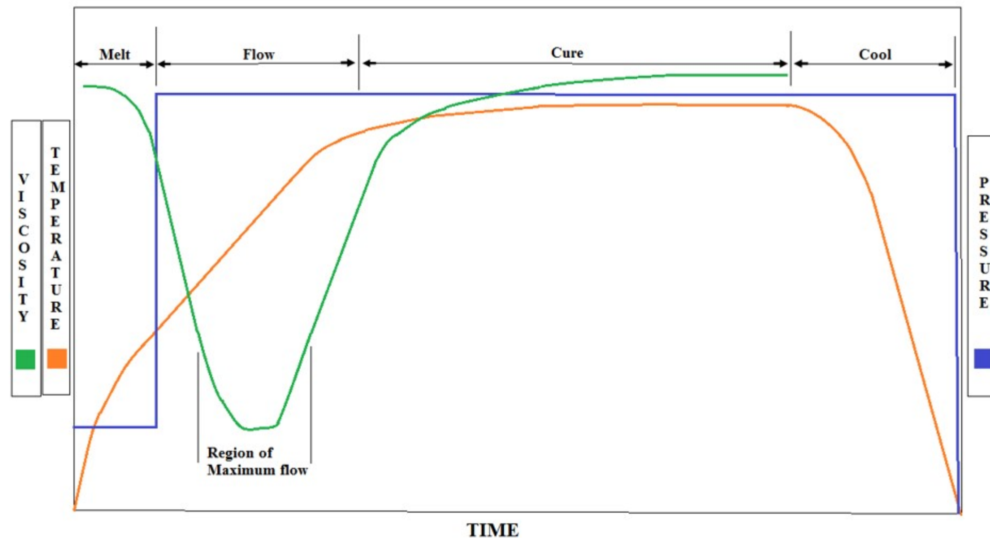


Figure 12 An overview of the time, temperature and pressure relationship used during the lamination process [9] [10].

The third process is an Autoclave Lamination. The PCB is sealed in a vacuum chamber with high pressure heated gas. This creates a uniform hydrostatic pressure

force. The downfall to this process is the pre-vacuum cycle will take much more time than a VAHL and the heat up rate is slower compared to the other lamination process.

1.5. PCB Fabrication Process

Rigid PCBs can be categorized as single-sided, double-sided, or multilayer depending on the circuit complexity. Different process steps are required for each of these technologies, with single-sided having the simplest process and multilayer the most complex and costly process.

1.5.1. Single Sided Boards

The basic steps for manufacturing single sided boards is presented along with the critical parameters [9]. More complex technologies use these steps as the base for constructing the more sophisticated structures.

A screen printing process step creates the master pattern from which the traces on the board are derived. The image is screen printed using a fine silk screen or a stainless steel wire mesh. The precision of the screen printed image depends on the mesh and the viscosity of the used ink.

In the photo resist step the board is coated with a thin uniform layer of photoresist material. The master created in the first step is then placed over the board and exposed to UV light. The resist is then developed and leaves the tracked pattern coated with the resist material; the remainder uncured resist material is washed

away. A rigorous inspection is required to detect "pin holes" in the ink or photoresist to avoid unwanted etching of the protected material, failure in this stage can result in out of specification traces or even an open trace line. Process mistakes at this step can potentially impact the reliability of the board causing an instantaneous failure or affecting then the performance over time. Once this stage is completed, the board can be etched.

During the etching process, all the unwanted copper that is unprotected by the photoresist material is attacked and removed, leaving only the metal traces and contact pads. There are three commonly used etching fluids used in PCB fabrication: ferric chloride, ammonium persulphate, and chromic acid. The etching operation is followed by a washing and subsequent a drying operation. The board is then inspected and the ink or resist is removed from the just created traces.

In the solder mask application process, the exposed copper traces are protected and electrically isolated with a dielectric coating known as solder mask. The solder mask protects the traces from mechanical damage and provides protection during the metallization and soldering processes.

Exposed board features such as pads, through holes, and any other specified contact points are now plated with a metal system (specified in the drawings) by any of the available metallization process. This metal finish will provide an oxidation barrier to the copper base metal. It will also serve as an interdiffusion barrier, and will

provide the metallurgical base to form a sound interconnection. The most common metallization materials for PCBs are gold over nickel, tin-lead, tin, silver, nickel, and bare copper protected with an organic preservative coating (such as Organic Surface Protect or Organic Copper Coating). The ultimate usage, criticality of the product, and cost must be considered when selecting the material and the method. The most common plating methods are electroless plating, electrolytic plating, immersion, and hot air surface leveling (HASL).

1.5.2. Multilayer Boards

Multilayer boards are made by a combination of the processes used for single sided boards and double sided boards with plated through holes. The individual internal layers, which may be single or double sided, are first etched in the same manner as single boards (after being punched and drilled for locating dowels), and then the layers are bonded together. The layers are laid up with a prepreg between the etched layers on the alignment dowels and the assembly is placed in a powerful press to obtain a blank. This sequence is known as inner layer fabrication and is illustrated in Figure 13.

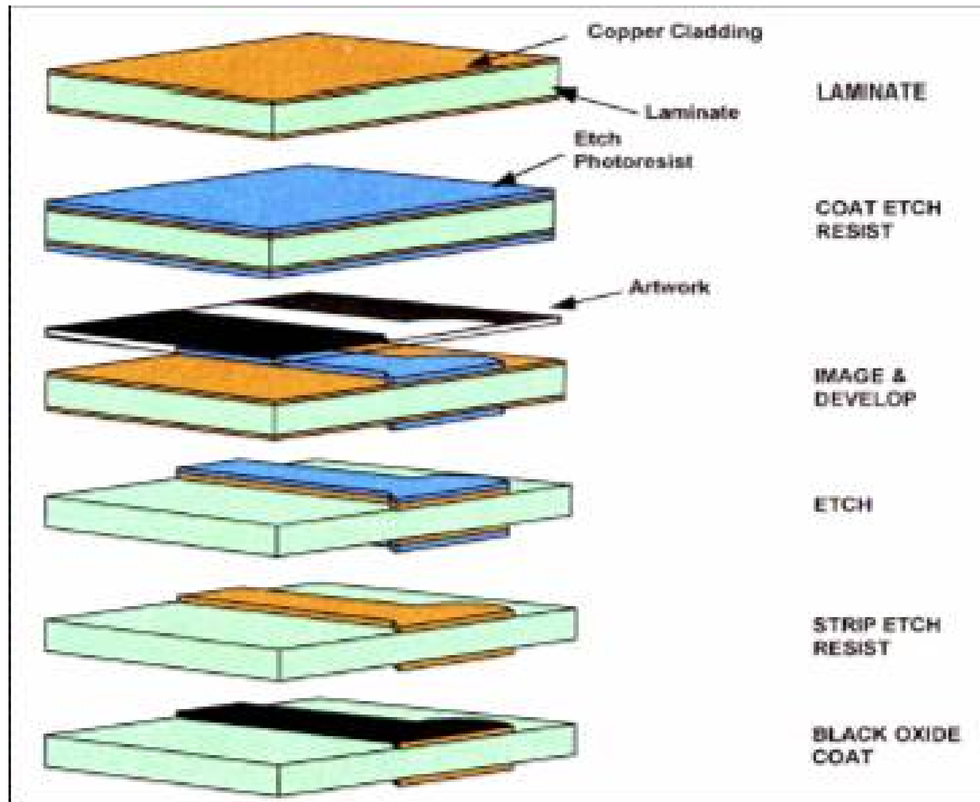


Figure 13 Inner layer process steps for multi layer boards [55].

Initially a light pressure is applied to close the layers together, and then the system is heated up. The full bonding pressure is applied and the resin is cured at elevated temperature. Once this stage is complete, the blank is ready for the outer layer process that can be seen in Figure 14.

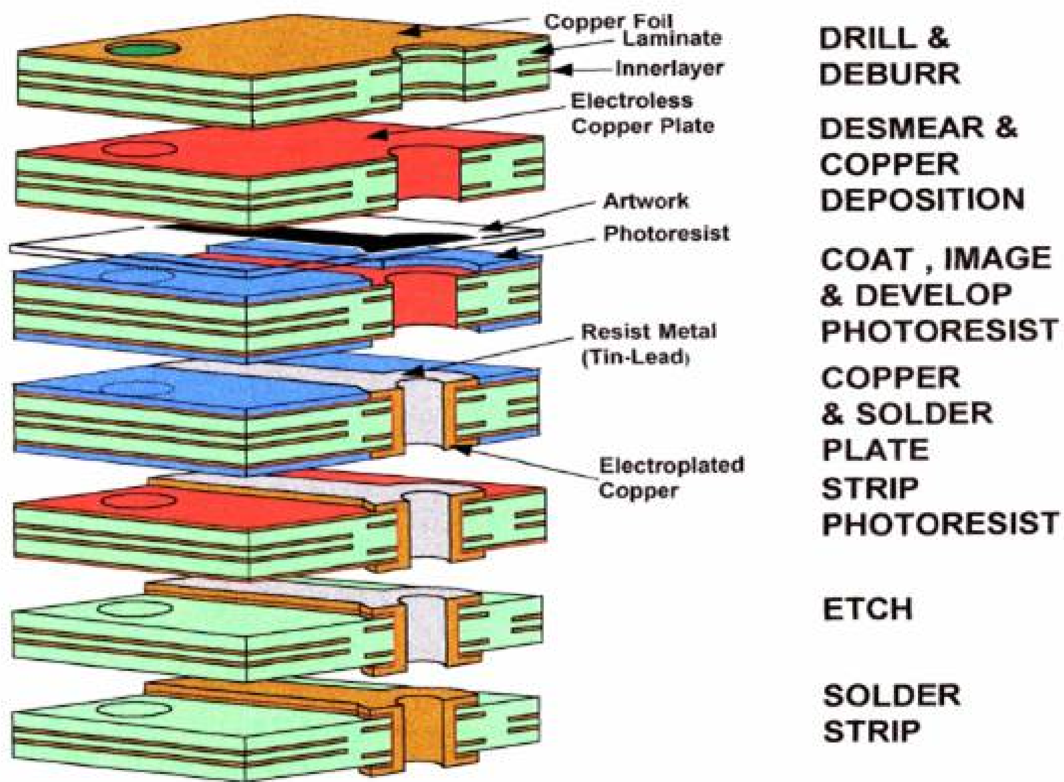


Figure 14 Outer layer process steps for multilayer boards [55].

1.6. Process Control and Inspections

Some PCB manufacturers use a special control pattern that is outside the finish board area to monitor all the processes. Microsections for characterization are taken from this area. Other suppliers make an extra boards or coupons on each lot, and this is used for process monitoring purposes and cross-sectional analysis. The inspection procedures normally applied throughout the process include visual inspections at every stage with "touch up" operations whenever necessary.

Regular analysis of all plating and etching baths form an important part of inspection procedures. Quantitative chemical analysis is obtained from the laboratory and compared to the standards. Plating thickness and undercutting are usually monitored on a batch basis by cross-sectioning or XRF techniques to inspect plating composition. Diameters of selected number of holes on each board are checked with pin gauges. Pad diameters, trace widths, and clearances are verified with an optical microscope. Electrical continuity testing for all PTHs should be applied. This test indicates whether a hole is an open circuit or not. It can not detect poor plating, roughness, or porosity, which would only be detected by visual inspection or destructive testing [16].

The inspection of multi-layer boards follows the same pattern of simpler boards, but as there are more process steps, more inspection is required. Electrical testing for internal short circuits and continuity is conducted. The boards are also inspected in x-ray to check for internal trace integrity. Thermographic testing can be used to locate short circuits between layers, which may be due to a single metal flake trapped between two layers, that had penetrated the B-stage on the bonding process.

1.7. Faults in Multi-layer Manufacturing Process

Wider tolerances are usually preferred for multilayer boards to allow for the extra processes involved and the misregistration problems that are encountered. A drilled hole that is out of the capture pad in the outer layer is a detectable problem, but on

an inner layer it could leave a hairline gap in which the plating material may induce an internal short. The risk of material movement is also increased in multilayer boards. This means that larger pads are used to guarantee that the hole will be within the pad area of all the stacked layers. To avoid the risk of board distortion, the lay-up at the board should be symmetrical, i.e. the stacking sequence must be a mirror image with respect to the middle layer [1].

The biggest problem in the manufacture of multilayer boards is the possibility of material movement during processing. A slight lack of balance in the lay-up can result in a locked-in stress which will cause the board to bow or warp. The pressure involved in laminating may cause an inner layer trace to slip sideways. This condition should not happen if the layout is uniform and the initial light pressure is properly applied. If there is a slight fault in the process and a trace moves over to bridge a narrow clearance, the whole board is lost.

1.8. Cost of Multi-layered Boards

The biggest disadvantage to multilayer boards, when compared to double sided boards of comparable size, is the high cost. After being bonded, the multilayer goes through the same processes as does a double-sided board, in addition to the etch back of the base material. Each inner layer has to have its traces pattern etched, with all the cleaning and intermediate inspection involved. Then the layers must be stacked carefully on the dowels and bonded together. Due to the incremental

number of process steps and the more rigorous inspection, the cost of multilayer boards goes up dramatically as the number of layers and drill count goes up. The following table provides a cost comparison in cents per hole.

Table 5 Cost Comparison for PCB (Approx. Cents per Hole) [13]

Board Type	Process	Cost
Single-sided	Punched	1.0
Double-sided	Punched	2.5
Double-sided	Drilled	5.2
Multilayer		
4 layers	Drilled	22.0
10 layers	Drilled	120.0
>10 layers	Drilled	380.0

1.9. Printed Circuit Board Failure Modes and Causes

The failure modes on the PCBs can be categorized in a hierarchical structure, in which the mechanisms and causes are site or location dependent. In this section, the most critical failures modes will be presented along with possible causes, in order to provide a synthesized analysis. A fish bone diagram is used.

1.9.1. Open Circuit

The electric path of a signal is defined on a PCB by the circuit traces. The continuity of these paths is critical for the functionality and reliability of circuit boards. An open circuit is defined as an electrical discontinuity, and will adversely affect the functionality of the board. This well known failure mode can be induced by multiple causes, and the physical processes by which the causes transforms into the

observed effect (mechanism) will depend on the life cycle conditions as well as the location (site) on the PCB. Figure 15 provides a detailed cause and effect diagram for the Open Circuit defect. On this diagram the main categories are divided in materials, design, equipment, method, man, and assembly process. For the equipment, man, and method sections, the analysis focuses on the practices on the manufacturing floor for the printed circuit board as well as on the circuit assembly manufacturing site. Materials, design, and assembly process represent the areas in which engineering knowledge along with failure analysis can provide the biggest contribution. Materials' compatibility with the environmental conditions as well as with the other materials used has been identified as a key element in product reliability. This is especially true in applications above ambient temperature where CTE mismatches are the cause for internal residual stresses, which could cause delamination resulting in an open circuit. Figure 15 provides a visual aid for the complexity and interrelated nature of the failure analysis.

Depending on the site, open circuits can be observed by visual inspection, non destructive x-ray analysis, or destructive cross section. The industry standard responsible for providing the acceptability guidelines for PCBs is the IPC-A-600G, where the different conditions are presented and evaluated based on the criticality of the product.

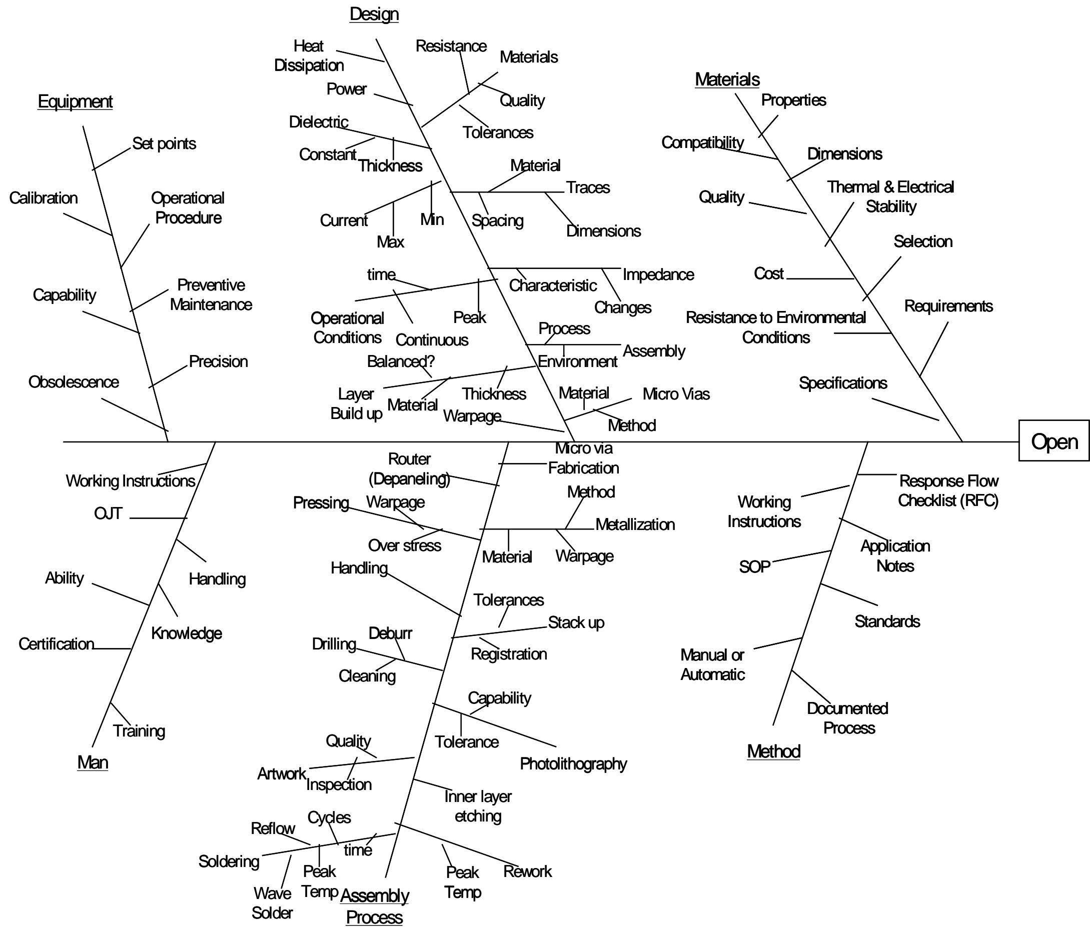


Figure 15 Cause and effect diagram for open circuit on a PCB [55].

1.9.2. Short Circuit

A short circuit will occur whenever a low resistance path is formed between conductors in the presence of a voltage potential. This can sometimes result in catastrophic damage to the PCB or the whole system with fire or explosion in the worst case. This type of defect is also known to cause intermittent failures in electronic devices, which can be tedious to troubleshoot. A short circuit can be the

start of a propagating fault that will burn or melt the PCB material leaving no evidence of the root cause.

As can be observed from Figure 16, there are multiple causes for its formation and there are multiple causes for its formations. Thre are also a whole range of failure mechanisms that are activated by different factors occurring throughout the life cycle environment of the product. A short circuit is the observed effect or failure mode, but there are multiple possible causes for this to happen and a variety of associated failure mechanisms. Figure 16 provides a cause and effect diagram for the short circuit problem.

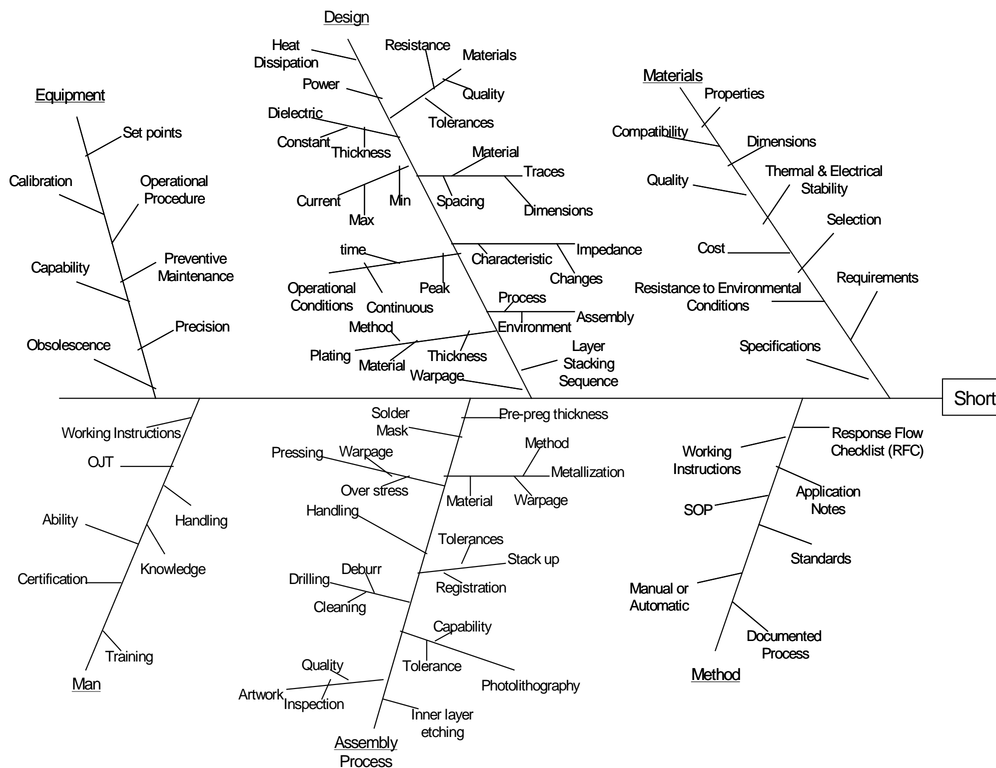


Figure 16 Cause and Effect Diagram for Short Circuit on a PCB [55].

Three categories on the above cause and effect diagram namely, Man, Method, and Equipment are mainly associated with the quality of manufacturing practices on the shop floor. Areas such as Materials are associated with the design practices. The assembly process can be associated with both quality and design issues, and deficiencies in these areas could have a detrimental effect on the product. The assembly process can be associated with both quality and design issues, and deficiencies in these areas could have a detrimental effect on the product.

1.9.3. Delamination

As previously discussed, multi-layer boards are basically a stack-up composite system in which a series of laminates are bonded together by means of a pre-preg dielectric layer impregnated with semi-cured epoxy-resin. The bonding strength of all of these interlayers depends on the strength of the thermo set material, which in turn is a function of thermo-mechanical properties such as glass transition temperature, CTE, and stiffness of the epoxy. The bonding capacity of these materials will also depend upon the curing time and temperature as well as the presence and efficiency of the accelerators, binders, and catalysts in the epoxy system. Failure to hold the stacked layers in the out of plane "z" direction will result in a failure mode known as delamination, which is a non- acceptable condition on PCB integrity. Figure 17 provides a cause and effect diagram for this

failure mode, where the main categories can be listed as Assembly Process/Method, Materials, Man, and Design.

Causes related to human behavior during the manufacturing process must be controlled in order to reduce the probability of occurrence. Materials, specifically the properties and cross compatibility among them, along with the resistance to environmental conditions are the most critical factors. The assembly process/methods are basically the source for energy, which is required for the failure mechanism to activate.

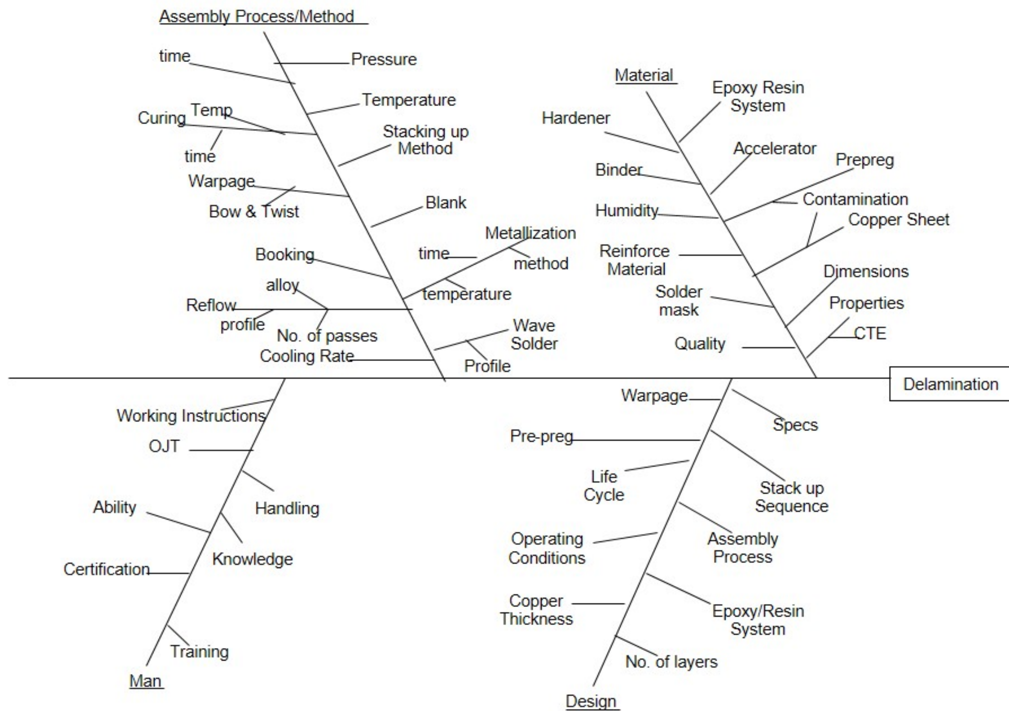


Figure 17 Cause and Effect Diagram for Delamination [55] [20][21][22].

Delamination has been historically attributed to high levels of humidity absorbed in the dielectric material. Investigations which were part of this research have shown that the increased build up of humidity was caused by under curing of the epoxy resin. It was observed that delamination occurred in samples where the epoxy was not fully polymerized.

1.10. Lead-Free Solder and Effects on PCBs

With the European Union's ban of lead from electronic devices, manufacturers of PCBs have developed new formulations of resin systems to withstand the increased thermal load on the laminate materials when using lead-free solders. Factors that are taken into account include risk to functionality, changes in processing techniques, material changes, and effects on the applicability of the new PCBs [3] [12] [51].

The functionality of new lead-free compatible PCBs is to withstand the increase temperatures produced during a lead-free soldering process (which is roughly a 30°C temperature increase). They have to be able to retain the same structural integrity as PCBs manufactured for lead-based soldering. The newer boards must be able to withstand the delaminating of the glass and epoxy used in FR-type boards. Also, warpage of the board must be kept to a minimum to reduce the risk of connection failure on the surface-mounted components during the PCB assembly process. Another function of a lead-free compatible PCB is to maintain proper

structural integrity for a longer soldering and reflow period, which is about 2 minutes longer overall and 30 seconds more in the reflow process compared to the conventional lead-based soldering process.

Most PCB manufacturers have already developed modified FR-4-type PCBs that are capable of withstanding the increased temperatures of the lead-free soldering processes. The key to the successful replacement of traditional FR-4 boards with new modified boards is that the same assembly process techniques can still be used on the new boards, thereby reducing the risk of increased cost from development of new assembly process techniques.

The materials that are used for the production of lead-free compatible FR-4 type PCBs are formulated with the addition of new polymers and epoxy resins with higher glass transition temperatures than conventional epoxy resins. One such example of a higher Tg epoxy resin is bismaleimide triazine, with a glass transition temperature of 205°C, which is close to the maximum reflow temperature of a tin-copper-silver solder (244°C) to prevent significant damage to the new lead-free compatible modified FR-4.

The new lead-free compatible PCBs can still be applied in exactly the same manner as current lead-based compatible boards. These applications are in the consumer, military, communication, and aerospace electronics fields to name a few.

1.11. Summary

Material makeup and fabrication of PCBs was discussed, along with the manufacturing processes for different types of boards. Process control and inspection techniques used for PCB fabrication along with an overview of common failure modes and causes were also covered. An overview of cost structure was provided, and overall impact of introduction of lead-free processing conditions was discussed.

Chapter 2: Conductive Anodic Filaments in Printed Circuit Boards

2.1 Introduction

Conductive anodic filament formation, a major cause of failures in printed circuit boards, is an electrochemical process that involves the transport of a metal through or across a nonmetallic medium under the influence of an applied electric field. With an increasing potential to market "green" electronics, environmental and health legislations, and the advent of lead-free and halogen-free initiatives, newer types of printed circuit board materials are being exposed to ever higher temperatures during solder assembly. The higher temperatures can weaken the glass-fiber bonding, thus enhancing conductive anodic filament formation. The effects of the inclusion of halogen-free flame retardants on conductive anodic filament formation in printed circuit boards are not completely understood. Previous studies, along with analysis and examinations conducted on printed circuit boards with failure sites that were due to conductive anodic filament, have shown that the conductive path is typically formed along the delaminated fiber glass and epoxy resin interphases.

The spacing between plated-through-hole edges is estimated to approach 2 mil and even closer. With increases in design density and tighter spacing between

conductors, the possibility of CAF failure in PCB electronic assemblies has also increased. CAF is a failure observed within glass-reinforced epoxy PCB laminates that is caused by an electrochemical process involving the ionic transport of a metal through or across a non-metallic medium under the influence of an applied electric field [24].

Failures in PCBs account for a significant percentage of field returns in electronic products and systems. The occurrence of CAF deep within the PWB can easily be diagnosed as "Failure Unknown." The Test Services and Failure Analysis Laboratory at CALCE has examined numerous electronic assembly failures due to permanent and intermittent PWB shorts [46] [47] [54]. Many of these failures in assemblies that were sent back after customer complaints could only be duplicated in a relatively high humidity environment since moisture was required to complete the electrical path. CAF is difficult to detect in the field because, once it occurs, sufficient heat is generated to "vaporize" the conductive anodic filament and "clear" the failure. Furthermore, observation of a partial filament formation requires destructive analysis. The growth of the metallic filament is a function of temperature, humidity, voltage, laminate materials, manufacturing processes, and the geometry and spacing of the conductors [25]. The growth of these filaments can cause an abrupt loss of insulation resistance between the conductors under a DC voltage bias.

Studies on CAF have found that path formation in a PCB is often along the glass fiber to epoxy matrix interphase (Figure 19). Delamination along the fiber/resin interphase can occur as a result of stresses generated under thermal cycling due to coefficient of thermal expansion (CTE) mismatch between the glass fiber (CTE~5.5 ppm/°C) and the epoxy resin (CTE~65 ppm/°C) (Figure 20). CAF can take place in the plated-through-hole to plated-through-hole (PTH-PTH), PTH-plane, and trace-trace geometries.

It is also important to differentiate between CAF, which occurs inside of a printed circuit board, and dendritic formation, a phenomenon that occurs on the surface of a printed circuit board, as shown in Figure 18.

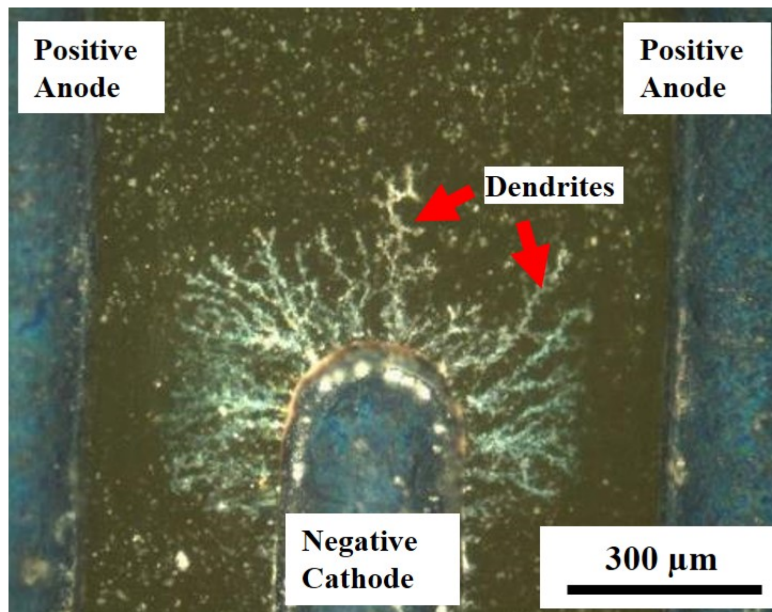


Figure 18 Photograph showing the phenomenon of dendritic growth, which occurs on the surfaces of a PCB.

A key characteristic of CAF is that it grows from the positively biased electrode to the negatively biased one inside the circuit board. In contrast, the dendrites from electrochemical reactions grow from the negative to the positively biased electrode. The phenomenon of dendritic formation, which is outside the scope of this research, is often confused with CAF and the terms are used interchangeably. It should be stressed that the growth of surface dendrites is promoted by the presence of contaminants on the board surface, the sources of such contaminants include residues from the PCB fabrication, solder mask application or from the printed circuit board assembly processes, such as the presence of flux residues which are not completely activated.

2.2 Literature Review

The following section provides a review of past research in the area of CAF, including substantive findings and contributions to the understanding of CAF.

Tests to characterize CAF conducted by Lahti and Lando in 1979 showed that there is little or no degradation in insulation resistance up to the point of failure [24][25]. That is, prior to failure, it is difficult to anticipate or predict failure by examining or monitoring insulation resistance. They also observed that one of the mechanisms

responsible for CAF failures involves the penetration of the glass/epoxy interphase by a conductive copper compound generated by electrochemical activity at the biased conductors (at the anode). The researchers observed that failure times dropped drastically at spacing less than 5 mil.

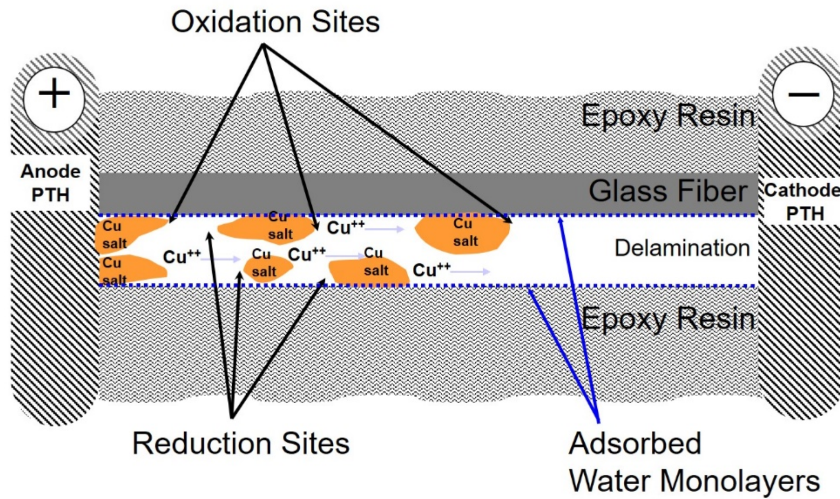


Figure 19: Schematic describing CAF growth.

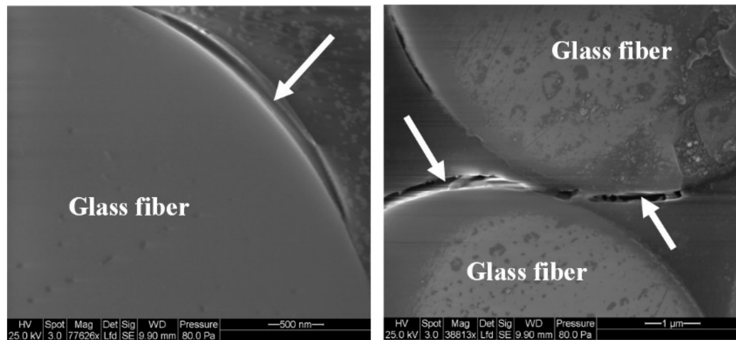
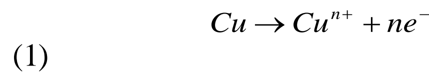


Figure 20: CAF growth along the fiber/resin interphase.

A two-step model was proposed to explain the growth of the conductive anodic filaments occurring at the resin-glass interphase in PCBs. Degradation of the resin-

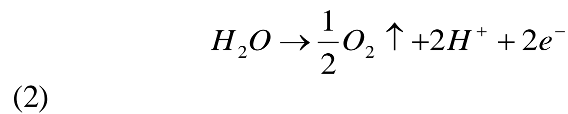
glass interfacial bond takes place in the first step, followed by the electrochemical reaction. According to Lando's hypothesis, the path required for the transportation of metal ions formed by the degradation of the resin-glass interfacial bond may result from mechanical release of stresses, poor glass treatment, hydrolysis of the silane glass finish, or stresses resulting from moisture-induced swelling of the epoxy resin. The path formation was reported to be independent of bias; however, it was observed that humidity could be a contributing factor in the case of chemical degradation. After path formation, the PCB may be viewed as an electrochemical cell. In this cell, the copper conductors are the electrodes, the absorbed water is the electrolyte, and the driving potential for the electrochemistry is the operating or test potential of the circuit. The electrode reactions proposed for the metal migration were:

At the anode



$$Cu \rightarrow Cu^{n+} + ne^{-}$$

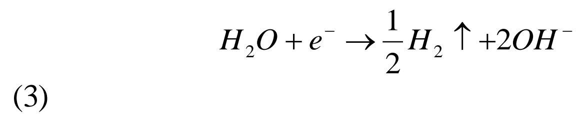
(1)



$$H_2O \rightarrow \frac{1}{2}O_2 \uparrow + 2H^{+} + 2e^{-}$$

(2)

At the cathode



$$H_2O + e^{-} \rightarrow \frac{1}{2}H_2 \uparrow + 2OH^{-}$$

(3)

The electrolysis of water creates a pH gradient between the electrodes, since hydronium ions are produced at the anode while hydroxide ions are produced at the

cathode. Using a simplified Pourbaix diagram for copper, a drop in pH at the anode allows copper corrosion products to be soluble until reaching a neutral region where they will be insoluble; thus, deposition along the epoxy-glass interphase was explained.

The materials tested in this study [25] included standard FR-4 materials from six suppliers using barrier coatings of resin (1–4 mils thick) in addition to various glass treatments. G-10, polyimide, and triazine, all with woven glass, along with polyester (woven and chopped glass), and epoxy with woven Kevlar were tested. The parameters of the tests were a continuous DC bias ranging from 200–400 V, 80% RH, 85°C, line-line, hole-hole, and hole-line conductor test patterns with and without surface coating. Lando [25] concluded that the susceptibility to CAF growth may depend on conductor configuration in decreasing order of susceptibility: hole-hole > hole-line > line-line. Mitigation strategies proposed by Lando included separating the resin/glass from the conductors by resin-rich areas, using traizine laminates, and improving the glass finish to allow stronger interfacial bonding at the glass fiber-epoxy resin interphase.

Researchers from Bell Laboratories in 1955 observed that silver in contact with insulating materials under an applied electrical bias can be ionically removed from its initial location at an anode and be re-deposited as metal at a different location at a cathode [26]. A major requirement for the process is the adsorption of water on

the insulating surface to act as the electrolyte. Examination of the metal re-deposited at the cathode revealed a dendritic structure, while the deposits at the anode appeared brownish and colloidal. Since silver was the only metal at that time to cause a potential hazard, the process was called silver migration. Parameters that were identified as affecting the silver migration rate included the properties of the insulating material, the DC voltage, time of the voltage application, and the percent relative humidity. Phenol fabric—the insulating material between the metals—was found to be susceptible to silver migration. The rate of the migration was observed to increase with voltage and relative humidity. Mitigation techniques that were suggested included resin impregnation to more effectively isolate fibers, pretreatments of fibrous surfaces with water repellant agents, and the use of silver precipitating agents to capture free silver ions.

In 1979, Lahti et al. [24] conducted experiments on configurations of single-sided, double-sided, and multilayered rigid PCBs with and without plated-through-holes (PTHs) with conductor spacings ranging from 5 mils to 50 mils, temperatures from 23°C to 95°C, relative humidities from 2% to 95%, and test voltages ranging from 10V to 600V. The authors observed while monitoring CAF failures that there is little or no degradation in insulation resistance up to the point of failure. Hence, prior to failure, it is difficult to anticipate or predict failure by examining or monitoring insulation resistance. Also seen was that the mechanism responsible for CAF failures involves the penetration of the glass/epoxy interphase by a conductive

copper compound generated by electrochemical activity at the anodically biased conductors.

The first indication that the mechanism has initiated is the visual enhancement of the glass reinforcement around the anodes due to the physical separation at the glass/epoxy interphase. Dark copper-bearing material then begins to fill the articulated regions, growing away from the anodes. The growth of the copper-bearing material follows the reinforcement in many directions, but ultimately migrates preferentially towards the cathodically biased conductors. The researchers observed that at spacings less than 5 mils, failure times dropped drastically. Lot to lot variability in the CAF resistance of the epoxy-glass printed wiring boards was also noted; one lot may perform better at 400V than another set at 45V.

Among the variables observed to affect the susceptibility of a PCB to CAF, the most important appeared to be raw materials. Processing factors such as process chemistry and lamination parameters, in addition to assembly parameters such as fluxing, soldering, cleaning, and baking, were shown to influence the propensity of a PCB to CAF failure. From the tests, it was concluded that the CAF failure mechanism is voltage sensitive, but not highly so; the dependence was not found to be greater than the inverse of voltage. In this study, failures occurred first on the most deeply buried layers and later in the layers closer to the board surface.

In 1980, Welsher and other researchers at Bell Laboratories [27] conducted extensive tests on triazine-glass, a CAF resistant material. The test boards were fabricated with a hole-hole grid test pattern with 42 mil diameter PTHs on 75 mil centers, with a minimum conductor spacing of 35 mils. Welsher proposed a two-step model consistent with that proposed by Lando in 1979 [25]. The tests showed that the exposure of a PCB to thermal transients such as thermal shock or during multiple soldering steps could significantly reduce its CAF resistance. The application of an intense thermal transient accelerates debonding of the fiber-epoxy matrix interphase due to the coefficient of thermal expansion (CTE) mismatch between the fiber and epoxy. A delayed application of the DC bias test showed that delaying the application of the DC bias does not significantly affect the time to CAF failure of the boards.

This confirmed the two-step sequential process proposed for CAF formation rather than the parallel process. It was also shown that the mean time to failure due to CAF might not be sensitive to the continuous or intermittent nature of the applied DC bias. Accelerated tests comparing the resistance of FR-4 and triazine to CAF failures demonstrated that boards manufactured with triazine can exhibit a life at least 20 to 30 times that of the FR-4s tested.

Mitchel and Welsher in 1981 [28] observed that failures due to filament formation showed an Arrhenius temperature dependence over the temperature range of 50°C

to 100°C. Analysis of the delayed bias tests in [28] showed that CAF growth takes place in two sequential steps, where mean time to failure is equal to the time for step 1 (path formation) plus the time for step 2 (electrochemical reaction), and that the time required for path formation is much greater than that required for the electrochemical reaction.

It was also observed that during the first stage of the failure process, an applied voltage is not necessary. In another pair of experiments, the reversibility of the two sequential steps was studied. In the first experiment, two sets of FR-4 samples were exposed to 85°C/80% RH; the first set for 240 hours, the second set for 168 hours. The second set was dried at 85°C for 72 hours. Both sets were then tested at 85°C/80% RH/200V. All samples in the first set failed within four hours, while the mean time to failure of the second set of samples was 122 hours.

From this study, it was concluded that step 1, the interfacial degradation, is essentially reversible, in agreement with studies on hydrolysis of glass-polymer coupling agents. To test the reversibility of the second step, electrochemical migration, several samples after failing at 70°C/85% RH/200V were dried at 70°C for 330 hours and then retested again at 70°C/85% RH/200V. The MTF before the drying was 292 hours while the MTF after the drying was 54 hours. It was thus concluded that once a filament has formed, it is permanent. In addition, several PCB materials were studied to determine their susceptibility to CAF growth. From

this study, woven glass laminates with resins of triazine, bismaleimide triazine, and polyimide were observed to offer the best hole-hole CAF resistance.

Augis et al. [29] in 1989 indicated that there is a threshold in relative humidity below which CAF would not occur. It was important to identify this threshold since linear acceleration factor models used for extrapolating reliability had broken down (i.e., a material that performed poorly under highly accelerated conditions could have acceptable characteristics under normal operating conditions). Tests showed that newly manufactured boards compared to aged boards showed no difference in CAF resistance during accelerated tests. Step stress tests run over a long period of time showed that above certain humidity levels the percentage of CAF failures increased rapidly. Hence, it was concluded that in humidity-controlled environments, CAF failures might not be a threat. Elemental analysis of the conductive anodic filaments in the study always showed elemental copper and sometimes either chlorine or sulfur associated with the filament. The chlorine and sulfur were believed to be from the fabrication processes.

It was speculated that the filament grows from the anode to the cathode, and the degradation mechanism most likely involves these four steps:

- Diffusion of water into the epoxy
- Migration of ions (Cu^{++}, Cl^{-})
- Corrosion ($Cu \rightarrow Cu^{++}$)

- Chemical reactions, such as breaking of the silane bonds at the fiber/epoxy interphase (may be due to hydrolysis)

A wide variability in median time to failure under the same environments using different lots of material was also observed.

Rudra et al. [31] in 1994 conducted experiments at CALCE using three PCB materials (FR-4, bismaleimide triazine (BT) and cynate ester (CE)), two humidity levels (70% and 85% RH), two temperatures (70°C and 85°C), and two DC voltages (300 and 800 volts). Each test board had six layers, ten different spacings, and six conductor geometries. The conductor geometries were PTH-to-plane, line-to-line, line-to-PTH, corner-to-PTH, PTH-to-PTH, and non-plated through-hole-to-line. The conductor spacings varied from 5 mils to 65 mils. Six different surface coatings were also tested.

From this study, it was concluded that BT and CE PCB materials are more resistant to CAF than FR-4 boards. BT and CE also had lower moisture absorption percentages. The presence of a post coat (a type of conformal coating) increased the time-to-failure due to CAF, while a solder mask in addition to the post coat offered the highest resistance to filament formation. For the various conductor geometries tested, PTH-to-PTH was the most susceptible failure site, followed by line-to-PTH and then line-to-line. It was observed that geometries on the surface layer tend to fail faster than the geometries on the inner layers. An empirical model

based on the failure data from the FR-4 laminates was developed to assess the time to failure due to conductive anodic filament formation. In this model temperature and humidity were combined into a threshold moisture content based on Augis' findings.

Ready et al. [32] in 1996 postulated that elevated bromide levels detected by EDX analysis in the area of a CAF failure may not have come from the board itself, but rather from a processing step. The presence of HBr in the soldering flux used during the problematic period suggests that this may be the source of the bromide. In this case, the bromide is speculated to have diffused through several layers of a 14-layered board during the soldering process at temperatures above 200°C. It was observed that substrates processed with fluxes containing certain polyglycols seem to exhibit an affinity for CAF formation. It appears that these polyglycols can also increase the moisture absorption of the laminate.

Turbini et al. [33] in 2000 examined the effect of certain water-soluble flux vehicles, both with and without halide activators, at processing temperatures of 201°C and 240°C in enhancing CAF formation. These two temperatures were selected to reflect both the expected peak temperature in wave soldering for traditional eutectic solder and for a typical lead-free solder. Using standard IPC-B-24 test coupons, it was observed that at the higher processing temperature, the occurrences of CAF failures greatly increased. It was speculated that this increase

in CAF failures at the higher temperature was due to the enhanced diffusion of polyglycols into the boards during the wave soldering. Since the diffusion process follows an Arrhenius behavior, the length of time during reflow that the board is above its glass transition temperature will have an effect on the amount of polyglycol absorbed into the epoxy. Higher reflow temperatures also lead to greater thermal strains due to the CTE mismatches between the glass fibers and the epoxy resin. Augis et al.[30] noted that the filaments always contain copper and sometimes contain chlorine or sulfur. Research by Ready [32] indicated that CAFs generally contain copper and chloride but may also contain bromide. Ready [30] reported that SEM/EDS data show that the CAF observed is copper and chlorine containing. In TEM analysis to determine the exact crystalline composition of copper-bearing CAF, the diffraction data showed good correspondence to that of synthetic atacamite ($2CuCl_2 \cdot 5Cu(OH)_2\ H_2O$). They further stated that present in nature, atacamite is transparent to translucent and deep green in color. It displays a slender, striated, and acicular to fibrous rhombic or orthorhombic crystal structure.

In 2002, Sauter [35] from Sun Microsystems described the testing parameters and design features that CAF test boards should incorporate to effectively assess CAF vulnerability in today's electronics. Some CAF test boards/coupons have been designed with only twenty PTHs and a few layers, which is not representative of today's higher layer count boards with thinner dielectrics. Sun Microsystems developed a ten-layer board with 168 potential in-line PTH-PTH failures per

spacing/test daisy chain and 312 potential diagonal PTH-PTH failures per spacing/test daisy chain. The data analysis techniques require 25 or more boards to be run per sample lot per bias level, giving 4,200 potential in-line hole-hole failure sites and 7,800 potential diagonal hole-hole failure sites per sample lot. This design has been made available to IPC (Institute for Interconnecting and Packaging Electronic Circuits) for industry use. Telcordia uses a 1,000-hour test while Sun uses a 500-hour duration period.

Sauter also recommends that a temperature of 65°C be used instead of 85°C to reduce the risk of sublimation, which can artificially reduce the activity of flux residues or other residues that may remain when certain board finishes are used, resulting in an erroneous assessment of CAF reliability risk. Sauter has found that some laminates that offer significantly more CAF resistance at larger spacings could perform poorly at smaller spacings. It was shown that although the Bell Labs and CALCE CAF prediction models appear to be quite different, the Bell Labs model and the adjusted CALCE model both predict a similar 8X increase in CAF failure risk for the same decrease in conductor spacing. The modification to the CALCE model was made to include the readily conductive region around the PTHs. From test failure data, Sauter concluded that some high T_g (glass transition temperature) FR-4 laminate materials for some PCB manufacturers show less resistance to CAF than standard T_g FR-4 materials. Since the combination of the PCB board finish and glass weave direction has a significant impact on CAF testing

results, the most vulnerable combination, HASL-finished boards tested in the machine direction, is recommended for evaluating the CAF susceptibility of a PCB.

In 2004, research scientists at the National Physical Laboratory [35] conducted two phases of accelerated tests to characterize conductive anodic filamentation. The first phase was aimed at understanding the effects of PTH geometries, voltage levels, and thermal effects, such as thermal shock and lead-free reflow, on a typical FR-4 laminate. Phase 2 incorporated improvements of the test board design based on lessons learned from phase 1. Phase 2 also compared different laminate types, glass reinforcements, drill feed speeds, and other laminate manufacturing variables.

In phase 1, standard T_g non-CAF resistant FR-4 boards with an electroless nickel immersion gold finish and no solder mask were tested. Each board had ten layers and more than 6,000 PTHs. The test voltages used ranged from 5 volts to 500 volts, while the conductor spacings ranged from 300μm to 800μm (in-line and staggered PTHs), and from 100μm to 200μm (anti-pad annulus). The parameters of the thermal shock were -15°C to +120°C and a cycle time of 14 minutes with a 5-minute dwell in each bath. Selected samples were exposed to 250 thermal shock cycles. The peak temperature used for the lead-free reflow was 250°C, and the boards were exposed three times. The testing was conducted at 85°C /85% RH for a duration of 1000 hours.

The findings from phase 1 were as follows: lead-free reflow increased CAF susceptibility while thermal shock had a negligible effect; MTF for in-line PTHs < staggered PTHs ≈ anti-pad; CAF occurs faster at higher voltages; CAF occurs faster at smaller spacings; and MTF is not strongly dependent on anti-pad gap spacing. NPL also determined that the relatively fast initial filament growth slows as it moves further away from the anode.

Phase 2 compared the CAF resistance of two manufacturers, both with CAF resistance and non-CAF resistance, and high and low T_g laminates. The effect of different drill feed speeds and surface finishes (electroless nickel immersion gold, silver, hot air solder level, and organic solderability preservative) on the time to failure for CAF were also examined. Two reflow peak temperatures were used: 210°C and 250°C.

The test results from phase 2 indicated that a higher reflow temperature promotes faster CAF growth. This, in conjunction with the negligible thermal shock effect, implies that perhaps the mechanism for damage in the laminate is not based on CTE mismatches between the materials, but rather a chemical or physical breakdown above a certain critical temperature. It was observed that in the anti-pads, failure occurs faster if the PTH is positively biased and the plane is negatively biased, and slower if the PTH is negatively biased and the plane is positively biased. It was also observed that PTHs closer together fail faster, even for the same electric field. In

all laminates tested, the CAF resistance laminates offered extended life of different percentages compared to their non-CAF resistant counterparts. The CAF resistant laminates delayed the time to failure due to CAF, but did not prevent it. CAF failures occur faster along the fabric weave in the machine direction. Identical laminates from different board manufacturers can have significantly different resistances to CAF. The tendency for failure to occur in a specific fabric glass style within the laminate weave-stack-up can vary from manufacturer to manufacturer. The parameters that had the most significant impact on CAF resistance were firstly the manufacturer (manufacturing process) and secondly the materials. The parameters that had negligible effects on the time to failure due to CAF were surface finishes, high or low T_g designation, and drill feed speed.

Rogers et al. [36][37] showed that laminates containing hollow fibers posed a threat to the reliability of electronic systems in that they provided a convenient open path for CAF. A method to detect hollow fibers in PCB laminates is discussed in detail. Based on CALCE's recommendations, hollow fiber assessment has now become a standard screen by which hollow fiber content ratios may be determined. This screen allows board fabricators and contract assemblers to qualify suppliers and discard lots with hollow fiber concentrations above specifications.

Chapter 3: Experiments to Characterize CAF Behavior in Laminated PCBs

3.1 Introduction and Experimental Procedure

In order to characterize the CAF failure behavior in laminated PCBs, accelerated tests were conducted under high temperature and high humidity environments. Four laminate types, three conductor spacings, and voltages ranging from 1 to 100VDC were included in the design of experiments [34]. The test boards were manufactured by Gold Circuit Electronics in Taiwan.

The test board designs and parameters for the test coupons were selected based on IPC-TM-650 2.6.25 (2003), Telcordia GR-78 (GR-78-CORE, 13.1.4, Electro-migration Resistance Test) and Sun Microsystems [35] CAF Test Board Specifications. The design of the test boards, as shown in Figure 21, contained 600 in-line PTH-PTH and 100 PTH-plane conductors, with PTH-PTH spacings and PTH-internal plane spacings based on current technology and manufacturing limitations using mechanical drilling (Figure 22). The three feature sizes in both PTH-PTH and PTH-plane conductor geometries were selected to be representative of nominal, advanced, and next generation (XG) feature sizes in electronics. The nomenclature of the three designs and conductor feature sizes were:

- Nominal feature (NF): PTH-to-PTH: 6 mil; PTH–plane: 8 mil

- Advanced feature (AF): PTH-to-PTH: 4 mil; PTH–plane: 6 mil
- XG: PTH-to-PTH: 3 mil; PTH–plane: 3 mil

The allowed drill wander for all features was ± 1 mil.

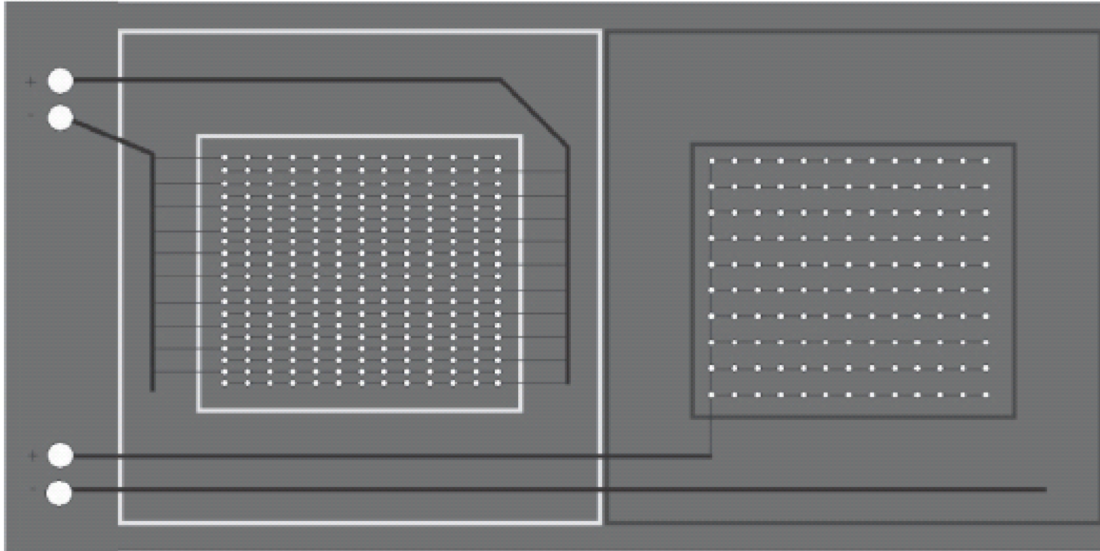


Figure 21: Test board design.

3.2 Test Sample Fabrication

Four different laminate types from two laminate suppliers were used for the fabrication of the 71-mil thick, 8-layer board (six internal planes). Since CAF susceptibility can be affected by fabric weave direction, features were placed on the board in such a way that the failure site opportunity with respect to weave orientation was either parallel to machine direction (warp direction) or at 45 degrees to machine direction. Figure 23 shows the placement of the features with respect to the fabric weaves.

The four laminate types from the two suppliers, along with the glass transition temperatures (T_g) were:

- Supplier A, T_g 180°C
- Supplier A, T_g 170°C
- Supplier B, T_g 170°C
- Supplier B (Halogen-free), T_g 150°C

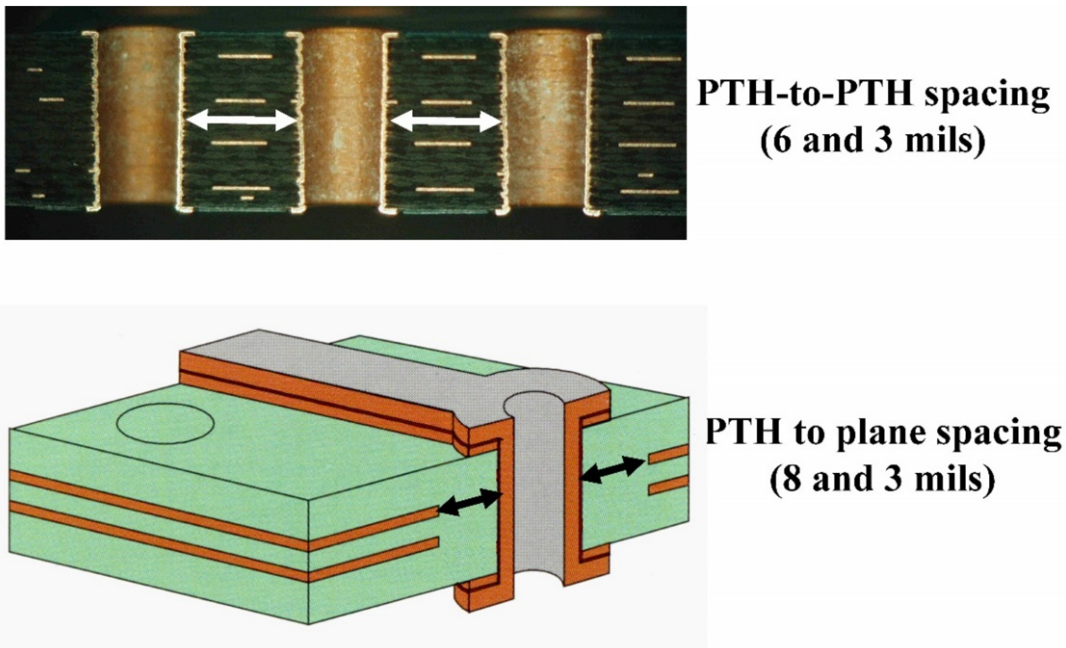


Figure 22: Conductor spacing in the test samples.

Five samples were tested for each spacing design and laminate type for a total of 20 samples per test.

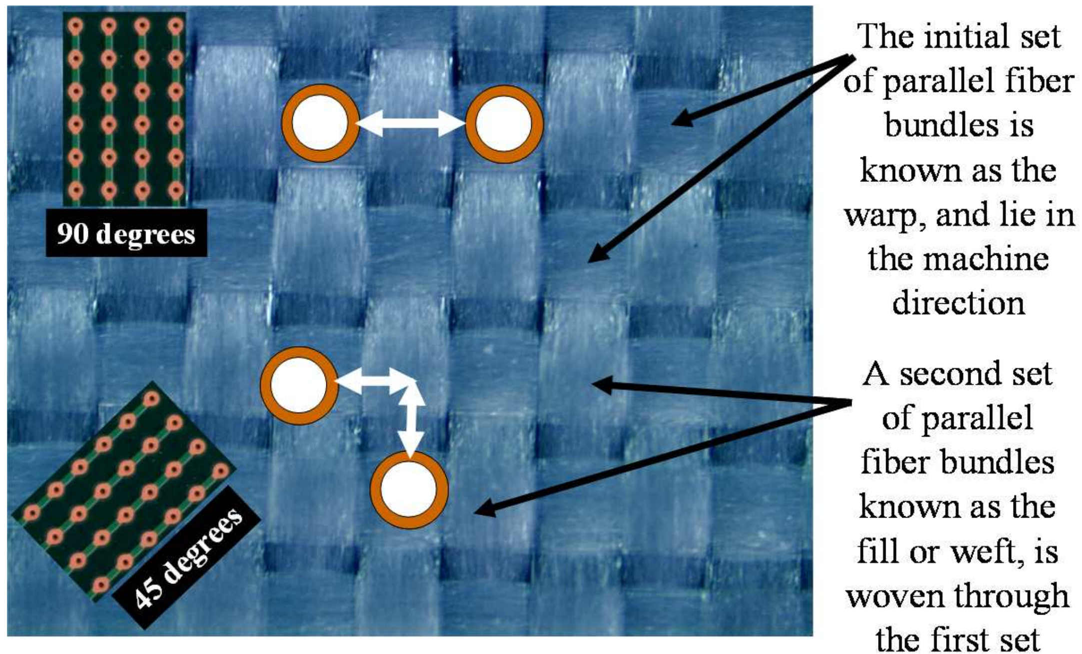


Figure 23: Fabric weave orientations.

Cross-sectional measurements of the internal conductor spacings and optical inspection revealed that the conductor spacing were within the specified tolerances. Copper wicking was found to be less than 1 mil (5, 4, and 3 mil are acceptable per IPC A-600F for class 1, 2, and 3 electronic assemblies, respectively). No plating voids or plating cracks were observed in the cross-sections. The average solder mask thickness was 0.5 and 0.2 mil measured over a masked trace and the edge of a masked trace, respectively. The maximum measured misregistration was less than 0.5 mil. Ion chromatography analysis of the boards revealed that the ionic contamination was less than 1 mg of NaCl per square inch (IPC recommends no more than 10 mg of total ionics per square inch).

3.3 Sample Preconditioning and Testing

The boards were tested in accordance with IPC-TM-650 2.6.25, Conductive Anodic Filament (CAF) Resistance Test: X-Y Axis [53]. Each board was uniquely identified. The test boards were handled by the edges only using non-contaminating gloves. Each of the two circuits in each test board was prescreened for short circuits by performing an as-received insulation resistance measurement check.

The boards were baked for 6 hours (h) at 105°C prior to each test to dry out the samples. After baking, the samples were preconditioned for 24 h at 23°C and 50% RH. The insulation resistances were again measured prior to a 96-h stabilization period with no applied bias at 85°C/85% RH. After this stabilization period, a bias was applied and insulation resistance measurements were started. An Agilent 4349B high resistance meter was used to monitor the insulation resistance of the 20 boards as they were subjected to humidity/temperature/bias testing. The insulation resistance monitoring setup is shown in Figure 24. A 1 MΩ current limiting resistor was placed in series with the current path to prevent "blow-out" of the fragile filaments when shorting occurred. Prior to the biased test, insulation resistance readings for each of the circuits were measured to be greater than 500 MΩ. Every channel used for resistance monitoring was scanned once every 48 seconds. This monitoring regime was more stringent than the IPC requirements of 24 to 100 hours.

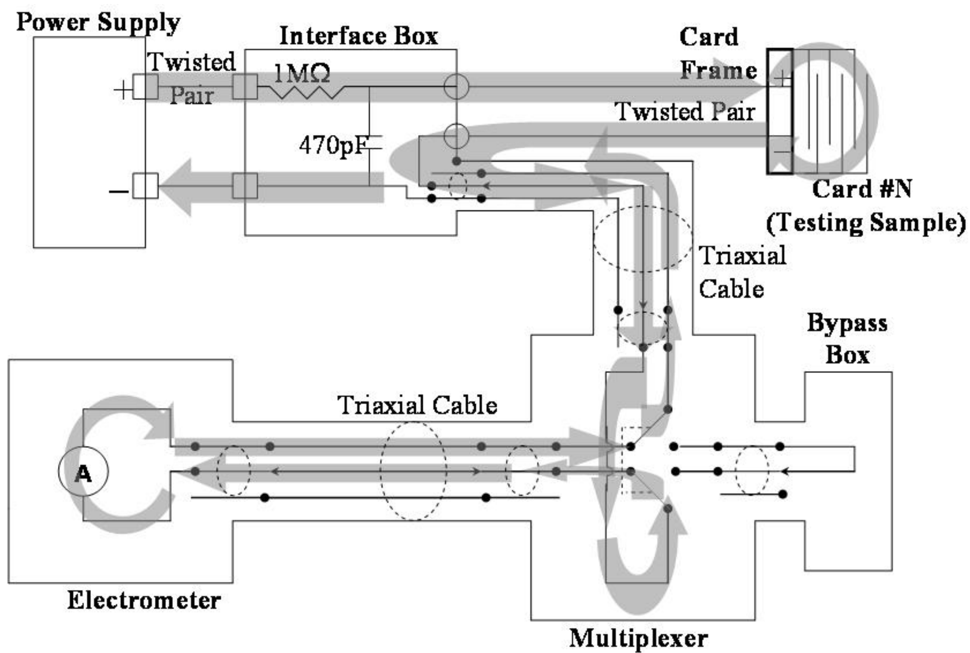


Figure 24: Schematic of setup used for measuring insulation resistance.

One set of 20 boards were subjected to reflow conditions prior to the test exposures. In test 4, from each of the four groups of five samples each, two samples (a total of 8) were exposed to three times (3x) eutectic reflow and three samples (a total of 12) to 3x lead-free reflow. A typical lead-free reflow profile is shown in Figure 25. All samples were exposed to 3x reflow cycles. The samples were subsequently exposed to 85°C and 85% RH conditions at 10V DC bias conditions as outlined in the test matrix. A summary of the test conditions is shown in Table 6.

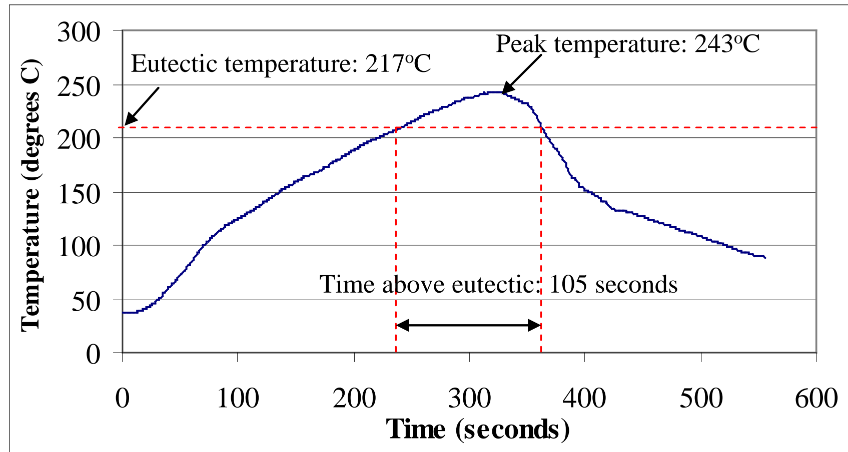


Figure 25: A typical lead-free reflow profile.

Table 6: Test Conditions

Test	Number of Boards	Spacing (mil)		Pre-exposure	Test Environment (°C, %RH)	Voltage Bias (VDC)
		PTH-PTH	PTH-Plane			
1	20	6	8	None	85, 85	10
2	20	3	3	None	85, 85	2
3	20	3	3	None	65, 85	2
4	8	6	8	Eutectic reflow *	85, 85	10
	12	6	8	Lead-free reflow *	85, 85	
5	20	6	8	None	85, 85	10

*- From each of the four groups of five samples each, two samples were exposed to eutectic reflow and three to lead-free reflow.

3.4 Results and Discussion

For the largest spacing (PTH-to-PTH 6 mil and PTH-plane 8 mil), a typical plot of the insulation resistance changes for three samples (two Supplier B 170°C T_g and one Supplier B halogen-free 150°C T_g) monitored over the 500-h duration of the test for the PTH-PTH conductor geometry is shown in Figure 26.

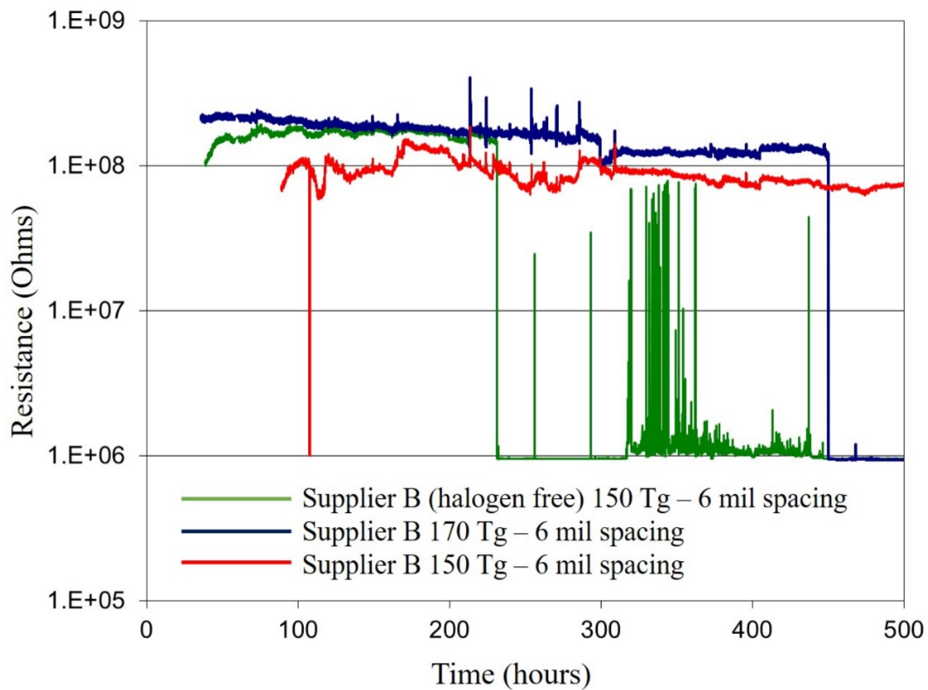


Figure 26: Plot showing PTH-PTH insulation resistance monitored at 10V for three of the Supplier B samples.

Figure 26 shows the intermittent nature of the CAF failures. Here, the insulation resistance value instantaneously drops to $1\times10^6\Omega$, which is the value of the in-series protection resistor, and then recovers back to normal. At the 10V bias level in test

1, there were seventeen failures in the PTH-PTH geometries and no failures in the PTH-plane geometries. After the duration of the 500-h test, some of the samples had not failed.

When the AF spacing (PTH-to-PTH 3 mil, PTH-plane 3 mil) was subjected to the same environmental test conditions after the application of the voltage bias (10V) and after the required presoak (96 h at 85°C/85% RH per IPC-TM-650 2.6.25, CAF Resistance Test: X-Y Axis Specifications), all PTH-PTH insulation resistances immediately dropped to 1MΩ, which was the resistance of the in-series protection resistor. This suggests that there were locations where the insulation resistance significantly decreased (by two orders of magnitude) in these samples prior to the biased exposure. All of the samples failed prior to 40 h, some within 1 min. There were also four PTH-plane failures in test 2. Similar behavior was observed for test 3 where the spacing was the same (PTH-to-PTH: 3 mil; PTH-plane: 3 mil), but the exposure conditions were 65°C/85% RH at 2V bias. All the PTH-PTH geometries failed during the 500-h test. No failures were observed in the PTH-plane geometries.

There were failures in the test samples exposed to eutectic and lead-free reflow conditions. For PTH-PTH geometries with 6 mil spacing exposed to eutectic reflow conditions, five out of the eight boards failed. On the other hand, for PTH-PTH geometries (6 mil spacing) exposed to lead-free reflow conditions, nine of the

twelve boards failed. Slightly higher failures were seen in the test samples exposed to 3X lead-free conditions as compared to samples exposed to 3X eutectic reflow conditions. There were no failures observed in the PTH-plane geometries with 8 mil spacings exposed to eutectic reflow conditions, but the test samples that were exposed to lead-free reflow conditions had three failures out of the eight samples.

In the 6 mil spacing PTH-PTH test samples exposed to 85°C and 85% RH, where features were placed at a 45- degree angle to the machine direction, there was only one failure. There were no failures in the 8 mil spacing PTH-plane geometries. A compilation of the experimental results are shown in Table 7.

Table 7: Experimental Results

<table>
<tr><th rowspan="2">Test</th><th rowspan="2">Weave</th><th colspan="2">Spacing (mil)</th><th rowspan="2">Pre-exposure</th><th rowspan="2">Voltage Bias
(VDC)</th><th rowspan="2">Test Environment
(°C, % RH)</th><th colspan="2">Number of Boards Showing Failures/Total Boards</th></tr>
<tr><th>PTH-PTH</th><th>PTH-Plane</th><th>PTH-PTH</th><th>PTH-Plane</th></tr>
<tr><td>1</td><td>90°</td><td>6</td><td>8</td><td>None</td><td>10</td><td>85, 85</td><td>17/20</td><td>0/20</td></tr>
<tr><td>2</td><td>90°</td><td>3</td><td>3</td><td>None</td><td>2</td><td>85, 85</td><td>20/20</td><td>4/20</td></tr>
<tr><td>3</td><td>90°</td><td>3</td><td>3</td><td>None</td><td>2</td><td>65, 85</td><td>20/20</td><td>0/20</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">90°</td><td>6</td><td>8</td><td>Eutectic reflow</td><td rowspan="2">10</td><td rowspan="2">85, 85</td><td>5/8</td><td>0/8</td></tr>
<tr><td>6</td><td>8</td><td>Lead-free reflow</td><td>9/12</td><td>3/12</td></tr>
<tr><td>5</td><td>45°</td><td>6</td><td>8</td><td>None</td><td>10</td><td>85, 85</td><td>1/20</td><td>0/20</td></tr>
</table>

The result of reflow exposure to CAF formation also varied with the laminate material type. The effect of reflow was seen clearly in the case of Supplier B T_g 170°C and Supplier B halogen-free materials where all of the samples exposed to any kind of reflow (both eutectic and lead-free) failed during testing. Test samples that were constructed out of the same two laminate materials but were not exposed to any soldering showed a fewer number of failures after testing. All the test samples constructed with Supplier B halogen-free material and tested after no reflow, eutectic reflow, or lead-free conditions failed. Test samples constructed with the halogen-free flame retarding material were the only cases where all samples had failed during testing. The test samples from Supplier A that were exposed to lead-free or eutectic reflow conditions showed a lower number of failures compared to samples that were not exposed to any reflow conditions. A summary of the effect of reflow on various laminate materials is provided in Table 8.

After the insulation resistance dropped to 1 MΩ (the resistance of the in-series protection resistor), selected samples were removed from the test chamber and analyzed with a scanning quantum interference device (SQUID). SQUID-based microscopy is able to image buried current-carrying wires by sensing and measuring magnetic fields produced by the currents (see Appendix B). By mapping the current, short circuits can be localized and failure sites determined. Figure 27

shows the SQUID output for the selected failed samples, locating the shorted sites in the board in a PTH-PTH conductor geometry.

Table 8: Effect of Reflow on CAF Failures in PTH-PTH Geometries for Various Laminate Types.

Laminates	**Number of Boards Showing Failures**		
	No Reflow	**Eutectic Reflow**	**Lead-free Reflow**
Supplier A, T_g 180°C	5/5	0/2	2/3
Supplier A, T_g 170°C	5/5	1/2	1/3
Supplier B, T_g 170°C	3/5	2/2	3/3
Supplier B (Halogen Free), T_g 150°C	4/5	2/2	3/3

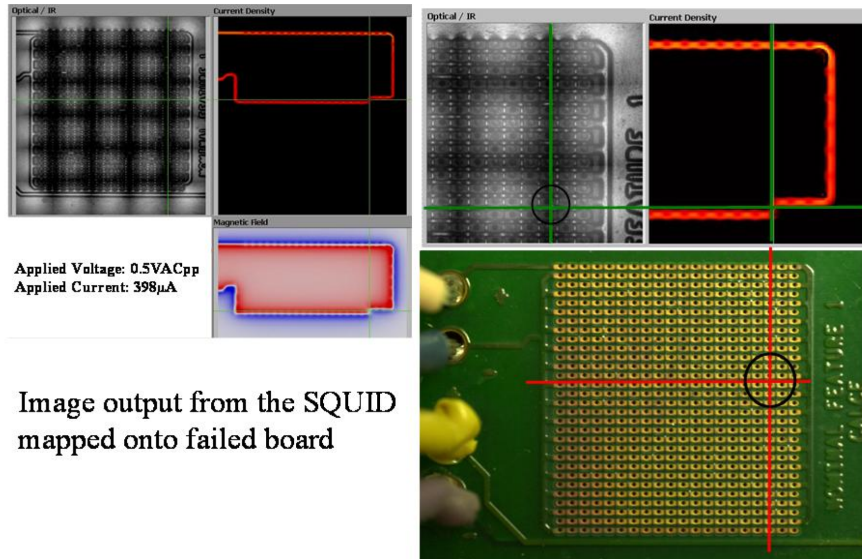


Figure 27: Overlaying the shorted site as predicted by the SQUID current mapping images, the respective conductor locations on the test boards were identified for cross-sectioning.

Cross-sectioning was performed on the failed samples in order to reveal the failure site and to inspect the CAF. The site isolation was performed in the failed samples by the SQUID, which revealed the leakage pathways.

First, using high speed rotary cutting tool with a diamond-tipped steel blade, the part of the test sample which was identified as containing the short location in SQUID microscopy was sectioned. Once sectioned, the sample was mounted using a two-part epoxy. The initial sectioning step consisted of grinding in the device under test sample using 600-grit silicon carbide paper; this grit size is used to remove layers from samples while maintaining the PTH in an as-received condition. Once the edges of the copper pads on the PTHs were reached, a switch to 800-grit silicon carbide paper was made. To ensure an even sectioning and to monitor the progress towards the sectioning plane, periodic X-ray inspection was performed to monitor the progress of the cross-sectioning plane into the samples. The grinding process continued with the 800-grit size abrasive paper until a CAF pathway was observed in the microscope. In optical inspection, copper-colored material was observed in the region between the plated through holes, revealed conductive anodic filaments in PTH-PTH conductor geometry when optically examined. Figure 28 shows optical images of a filament formed between two PTHs.

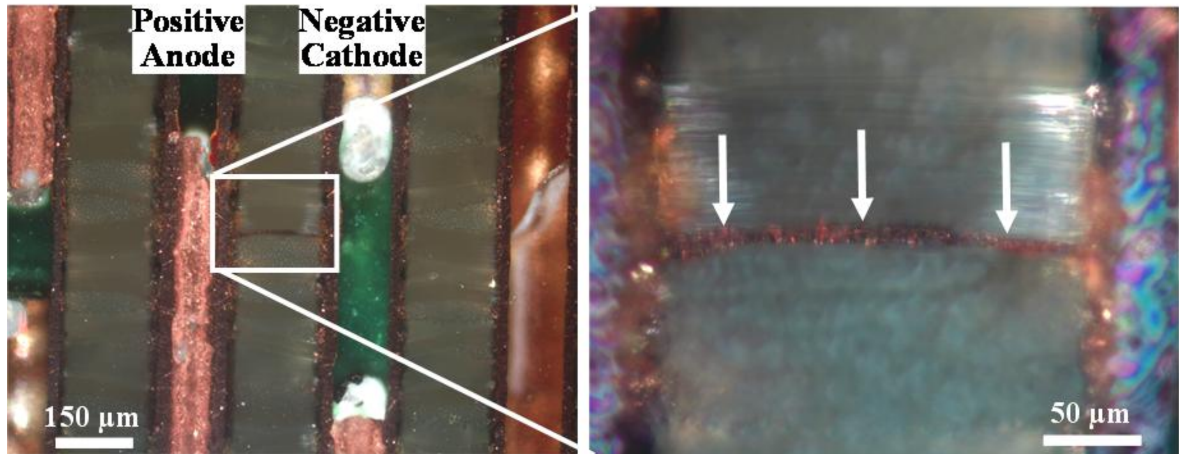


Figure 28: Filament formation in the PTH-PTH geometry.

3.5 Summary

The drive to increase circuit density with smaller printed circuit board geometries, higher layer counts, and the increasing use of electronics in environmentally uncontrolled applications, have made short circuiting due to conductive anodic filaments between biased conductors a major concern. In addition, higher temperatures in lead-free processing and new flame retardant materials affect laminate stability and increase the potential for conductive anodic filament formation failures. This shows that smaller conductor spacing reduces the time to failure due to conductive anodic filament formation and that the plated-through-hole to plated-through-hole (PTH-PTH) conductor geometry is more susceptible to conductive anodic filament-induced failures than PTH-plane geometries. The results in this chapter also show that laminates with similar materials and

geometries with a 45-degree angle of weave demonstrate a higher resistance to conductive anodic filament formation compared with a 90-degree angle of weave.

To mitigate catastrophic failures, it is necessary to understand the roles and synergistic effects of environmental conditions, material properties, and manufacturing quality in accelerating the pathways necessary for the initiation of conductive anodic filament formation. Some proactive companies have already begun to invest in this area and are funding research to deter conductive anodic filament formation-related failures.

Chapter 4: Experiments to Characterize the Effect of Epoxy/Glass Interphases on CAF Failures in Printed Circuit Boards

4.1 Introduction and Experimental Procedure

Experiments that highlight the problems that arose on a telecommunications circuit board and the systematic evaluation to reveal the root causes are discussed in this chapter [54].

Three test printed circuit board assemblies were biased during a 28-day temperature-humidity test. This test is part of a suite of internal tests that a telecommunications provider uses to understand the long-term effects of humidity and bias on their electronics products.

Three PCBs (device under test samples #9, #7, and #11) were exposed to a 28-day test at 52°C and 95% relative humidity (RH) in a temperature humidity chamber. A bias voltage of 2.4VDC was applied to pins that were at a location which corresponds to the mounting site of through hole male connector. The nominal center to center pitch of the plated through holes in which the connector pins are mounted is 1.3mm. Resistances between pin pairs were measured every twenty four hours by removing the samples from the temperature humidity chamber. Although, due to the rapid loss of moisture from the outer surfaces of the PCB samples when

removed from the temperature/humidity chamber, it is desirable to conduct in-situ insulation resistance measurements while the samples are placed in the temperature/humidity chamber, diffusion modelling and experiments have shown [57][58] that a bulk of moisture is carried by the PTH features within the PCB design and facilitate the diffusion of moisture into and out of the PCB. The insulation resistances are measured using a digital multimeter. The initial, time zero, insulation resistances of the three PCB samples #9, #7 and #11 were in the 10GΩ or higher range. The initial measurements confirmed that the tested features in the PCB were free of electrical leakage pathways at time zero.

After 14 days in test, the resistance between connector P401 on device under test sample #9 pins 2–3 measured 200 Ω and the resistance for pins 7–8 measured 435 Ω. The telecommunications provider reported that manual resistance monitoring of sample #9 did not show a change in IR up until the 13th day of testing. The drop on the 14th day to 200Ω was first observed on that day. After the failures were observed, certain resistor reference designators located on layer 1 of the assembly were removed to isolate pins 2–3 and 7–8 from the rest of the circuit. No change in resistance was observed after removal of the components. The plastic shell on connector P401 located on layer 6 was mechanically removed to expose its pins and the area beneath the connector. Each pin has a trace extending a short distance to a test point. These traces were cut near both pins to further isolate pins 2–3 and 7–8. No change in resistance was observed at pin pairs 2–3 and 7–8. The area

beneath the connector on layer 6 appeared to be clean, with no signs of dendrite growth between pins. A groove was cut in the circuit board between pins 2–3 and 7–8 on layer 6 to eliminate surface leakage as a possible source. The resistance between pins 2–3 and 6–7 remained unchanged. Visual inspection of the area between pins 2–3 and 7–8 on layer 1 revealed no dendrite growth between pins. A groove was cut between pins 2–3 and 7–8 on layer 1 to eliminate surface leakage as a possible source. No change in resistance between pin pairs 2–3 and 7–8 was observed. At this point, it was believed that the low-resistance path was internal to the PCB at both locations.

After an additional 5 days in test, the resistance measured at pins 2–3 dropped to 30 Ω and to 40 Ω for pins 7–8. These resistance measurements were repeated using an Agilent 4155C semiconductor parameter analyzer. Current-voltage (*I-V*) sweep characterization testing was performed on all PTHs: first (initial stage of testing) as a general characterization of the resistance measurement in between each PTH and later at known locations (known shorts). In some cases, high resistance values that were in the kiloOhms were observed; in other samples (known shorts) low resistance measurements (mΩ) were recorded. One source monitoring unit (SMU) of the 4155C semiconductor parameter analyzer was used to sweep a 0–1 volt DC (VDC) through each pin pair; voltage was injected through the force terminal and the current measured at the sense terminal. A total of 101 steps were measured, and

the compliance current was set at 10 mA. The resulting *I-V* curves obtained from DUT#9 pins 2–3 and 7–8 are shown in Figure 29 and Figure 30.

Similar resistive behaviors were also observed in DUTs #7 and #11. After 11 days in test, the resistance between connector P401 of DUT#7 pins 5–6 measured 182 Ω. Reference designator resistors located on layer 1 of the assembly were mechanically removed to isolate pins 5–6 from the rest of the circuit. No change in resistance was observed after removal of the components. The plastic shell on connector P401 located on layer 6 was mechanically removed to expose its pins and the area beneath the connector. Each pin has a trace extending a short distance to a test point. White and yellow leads were soldered to the test points to monitor the resistance. No change in resistance was observed at pins 5–6. The area beneath the connector on layer 6 appeared to be clean; no signs of dendrite growth between pins were observed. A groove was cut in the circuit board between pins 5 and 6 on layer 6 to eliminate surface leakage as a possible source. The resistance between pins 5 and 6 remained unchanged. Visual inspection of the area between pins 5-6 on layer 1 revealed no dendrite growth between pins. A groove was cut between pins 5 and 6 and between test points on layer 1 to eliminate surface leakage as a possible source. No change in resistance between pins 5 and 6 was observed. After storage for two weeks in ambient conditions, the assembly measured an electrical open and it appeared that the low resistance pathway had recovered. Upon replacement into the humidity chamber at 52°C and 95% RH and supplied 2.4 VDC

to the assembly limiting the current to 1 mA, after 12 h in test, there was a 40 kΩ resistance between the pins.

For device under test sample #11, after 21 days in test, the resistance between connector P401 pins 6 and 7 measured 430 Ω. Resistors R421 and R422 located on layer 1 of the assembly were mechanically removed to isolate pins 6–7 from the rest of the circuit. No change in resistance was observed after removal of the components. The plastic shell on connector P401 located on layer 6 was mechanically removed to expose its pins and the area beneath the connector. Each pin has a trace extending a short distance to a test point. The trace was cut near both pins to further isolate pins 6–7. No change in resistance was observed at pins 6–7. The area beneath the connector on layer 6 appeared to be clean, with no signs of dendrite growth between pins. A groove was cut in the circuit board between pins 6 and 7 on layer 6 to eliminate surface leakage as a possible source. The resistance between pins 6 and 7 remained unchanged at 430 Ω. Visual inspection of the area between pins 6 and 7 on layer 1 revealed no dendrite growth between pins. A groove was cut between pins 6 and 7 on layer 1 to eliminate surface leakage as a possible source. No change in resistance between pins 6 and 7 was observed. After storage for two weeks in ambient conditions, the assembly measured an electrical open. Leads were soldered to the connector side of resistors R421 and R422, and the board was placed back into the humidity chamber at 52°C and 95% RH and

supplied 2.4 V to the assembly limiting the current to 1 mA. After 12 h in test, 860 Ω was measured between pins.

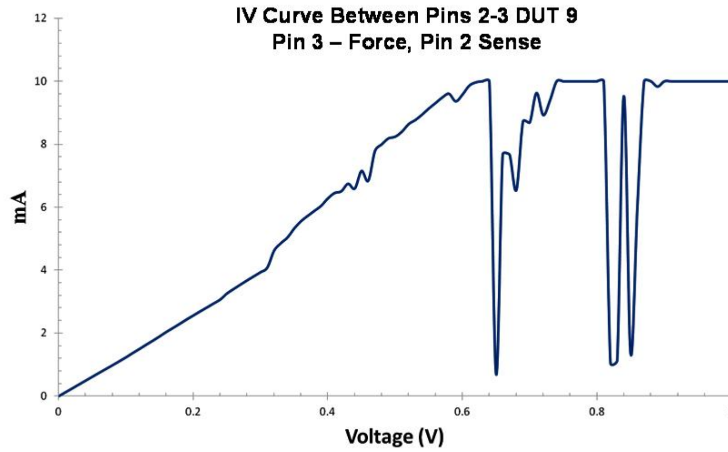


Figure 29 Current-voltage relationship between pins 2 and 3 of device under test sample #9.

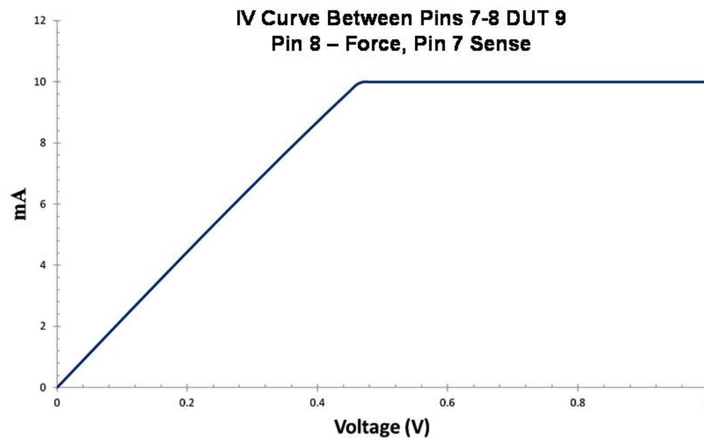


Figure 30 Current-voltage relationship between pins 7 and 8 of device under test sample #9.

The device under test sample #9 to be cross-sectioned and inspected for inner-layer shorts and CAF was selected based on findings from electrical testing. For sample 7 and 11, even though an open (or high) resistance between pin pairs 5 and 6 (sample7) 6 and 7 (sample 11) was observed after storage for two weeks in ambient conditions, the repeat 52°C and 95% RH with 2.4 V produced a 40kΩ and 860 Ω between pins after a 12 hour period, these samples were not selected as candidates for further destructive analysis due to the intermittent nature of the leakage pathways. In order to monitor the resistance in between the PTH pin pairs 7–8 and 2–3 of device under test sample #9 while sectioning, leads were soldered to pins. These pins are soldered into the PTHs that had the shorts. The technique of using in-situ resistance measurements during destructive physical analysis to confirm one has reached CAF filaments during cross-sectioning is the first time this is described in the open literature. This solution addresses the potential problem in destructive physical analysis of grinding away the evidence of the CAF filament and ultimately losing evidence at the failure site.

Using a high speed rotary cutting tool with a diamond-tipped steel blade, the part of the PCB assembly with the PTH was sectioned. Once sectioned, the PCB section was mounted using a two-part epoxy. The previously soldered cables were then connected to an Agilent 34410A digital multimeter to monitor the change in resistance while sectioning. An optical photo of the section with soldered leads is shown in Figure 31.

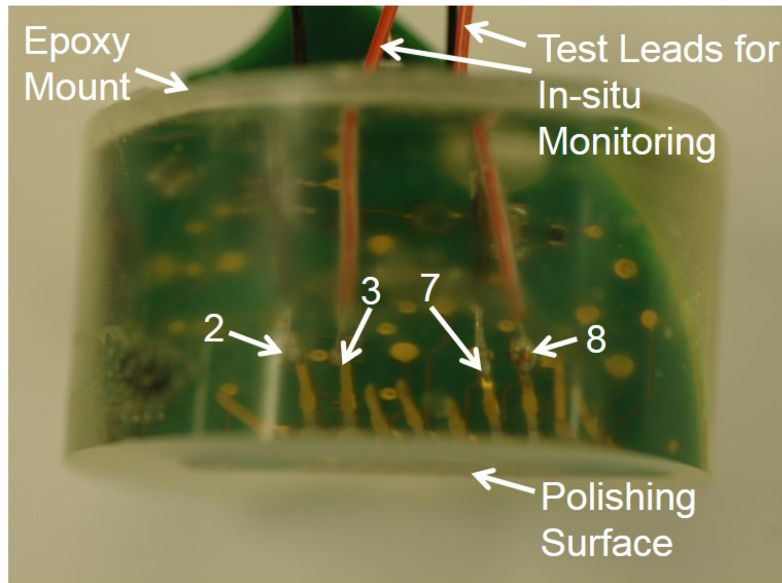


Figure 31 Photo of the potted section of device under test sample #9 with soldered leads.

The initial sectioning step consisted of grinding in the device under test sample using 600-grit silicon carbide paper; this grit size is used to remove layers from samples while maintaining the PTH in an as-received condition. Once the edges of the copper pads on the PTHs were reached, a switch to 800-grit silicon carbide paper was made. To ensure an even sectioning and to monitor the progress towards the sectioning plane, periodic X-ray inspection was performed to monitor the progress of the cross-sectioning plane into the samples. A sample X-ray radiograph obtained during the grinding with 800-grit paper is shown in Figure 32. The grinding process continued with the 800-grit size abrasive paper until a fluctuation in the resistance value was observed.

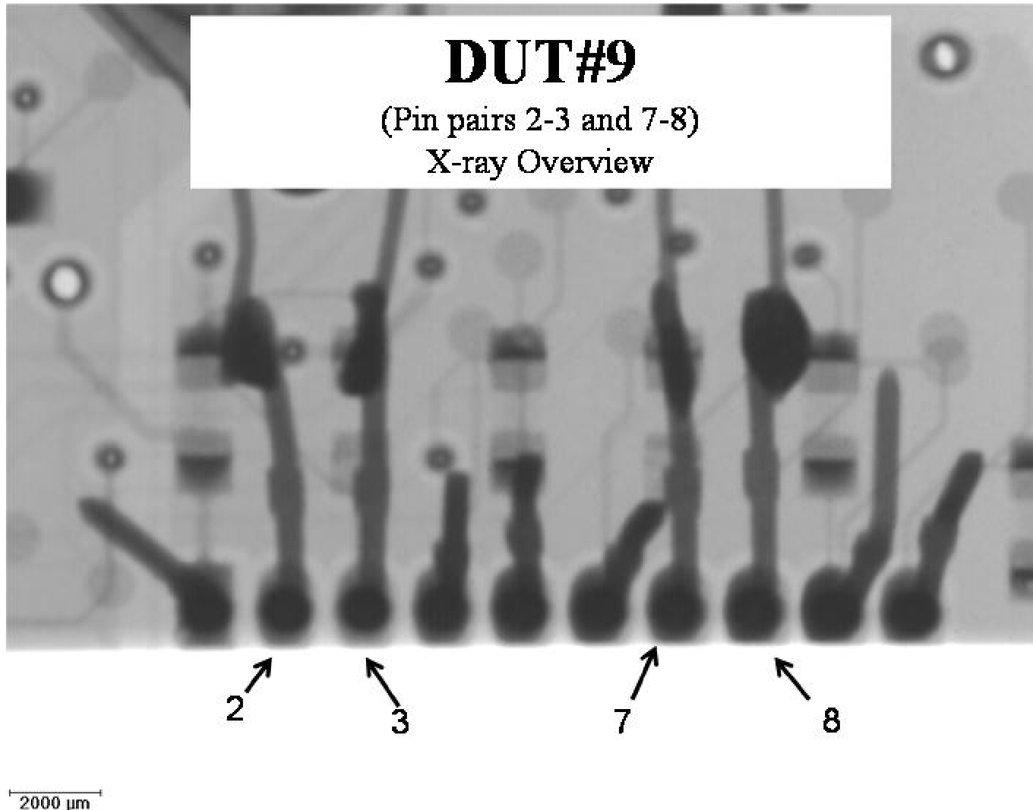


Figure 32 X-ray radiograph obtained during the grinding with 800-grit abrasive paper.

The observation of CAF in device under test sample #9 between pins 2 and 3 was accompanied by a wide fluctuation in the electrical resistance values that were being monitored in an in-site fashion. Formation of conductive anodic filaments was confirmed for device under test sample #9. In optical inspection, copper-colored material was observed at the interphase of glass fibers and epoxy resin in the region between PTHs 2 and 3. An optical image obtained at this sectioning plane is shown in Figure 33 and Figure 34. A corresponding SEM image is shown

in Figure 35. Note in Figure 35, as opposed to the optical viewgraphs in Figure 33 and Figure 34, the SEM image shows a fragmented pathway along with glass/epoxy interphase. The brightfield optical viewgraph in Figure 33and Figure 34, due to the higher depth of field, captures details from the focal planes that are beyond the viewing range with the SEM. A corresponding energy dispersive spectroscopy (EDS) spectrum taken over the region shown in Figure 35(a) is shown in Figure 35(b). The EDS spectrum shows presence of elements such as copper and bromine along with magnesium calcium, aluminum and oxygen. While the magnesium, calcium, aluminum and oxygen are components of e-glass and the bromine likely originated from laminate material which surrounds the glass fibers [54], copper does not belong in this region. The copper is a component of the CAF that originated at the anode, pin 2 and was electrochemically migrated towards the cathode, pin 3. The EDS spectrum only shows a weak peak for copper at 8.04keV, the chlorine peaks are likely weak and not discernable in the EDS spectrum shown in Figure 35(b). The inability of the EDS tool to resolve the chlorine at this SEM viewing area and magnification or the relative non-abundance of chlorine at the EDS spectrum acquisition location could be other reasons why the chlorine was not discernable at 2.62keV, and copper was not a very strong signal at 8.04keV. The method of in-situ electrical resistance measurements during the grinding process enables precise isolation of the CAF by monitoring the change in resistance between the PTHs (2 and 3) while cross-sectioning. Note that in Figure 33 and

Figure 34, the surface of the mount appears rough and striated. The striations result from the polishing process, however, once the resistance fluctuations are observed, any further grinding or polishing (performed in order to remove the surface striations) will extract the CAF residual materials and can result in recovery of the impedance pathway.

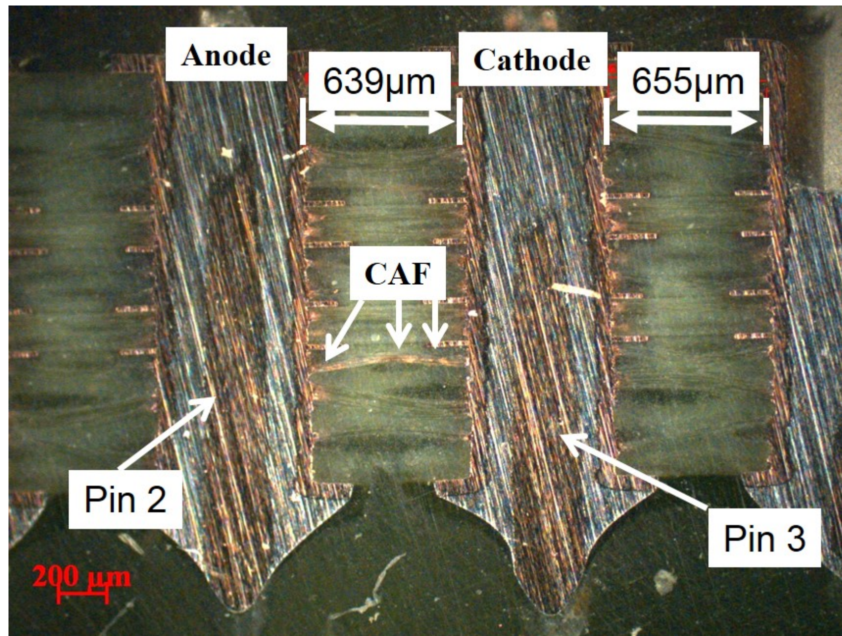


Figure 33 Formation of CAF on device under test sample #9 between pins 2 and 3. Note that the surface of the mount appears rough and striated. Once the resistance fluctuations are observed, any further grinding or polishing will extract the residual materials and result in recovery of the low impedance pathway.

Scanning electron microscopy and energy dispersive spectroscopy (EDS) analysis was conducted on the site revealed by the cross-section with in-situ monitoring. EDS analysis showed that the material observed between pins 2 and 3 of device under test sample #9 was copper. In addition to copper, elements such as oxygen,

aluminum, silicon, and calcium were identified. Scanning electron micrographs also showed separation between the glass fiber and the epoxy resin matrix. The presence of this delamination indicates that monolayers of moisture could form along this separation. If electrolyte and ions are present, they form an electrochemical cell. Oxidation and reduction reactions occur at the conductor, forming copper ions. Since CAF is a corrosion-based process, it is influenced by parameters such as drill damage, stability of the metal, the presence of moisture, and electrical bias levels.

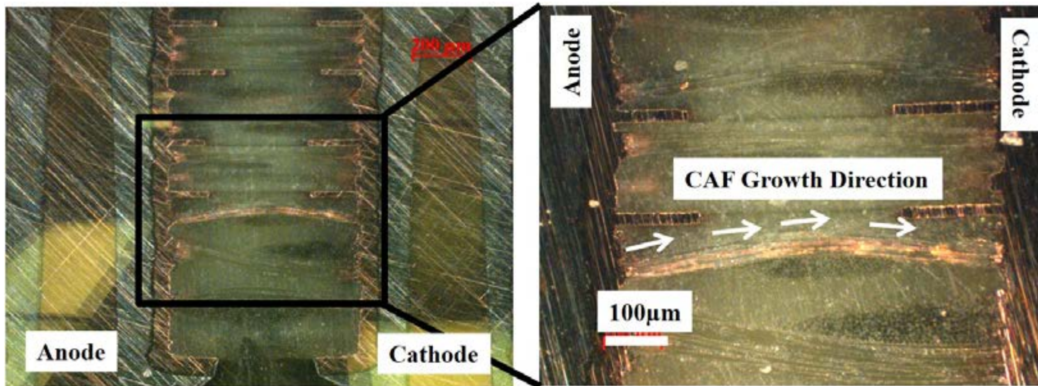


Figure 34 Optical micrographs of CAF observed between the glass fibers and the epoxy resin. Note the surface of the mount appears rough and striated. Once the resistance fluctuations are observed, any further grinding or polishing will extract the residual materials and result in recovery of the low impedance pathway.

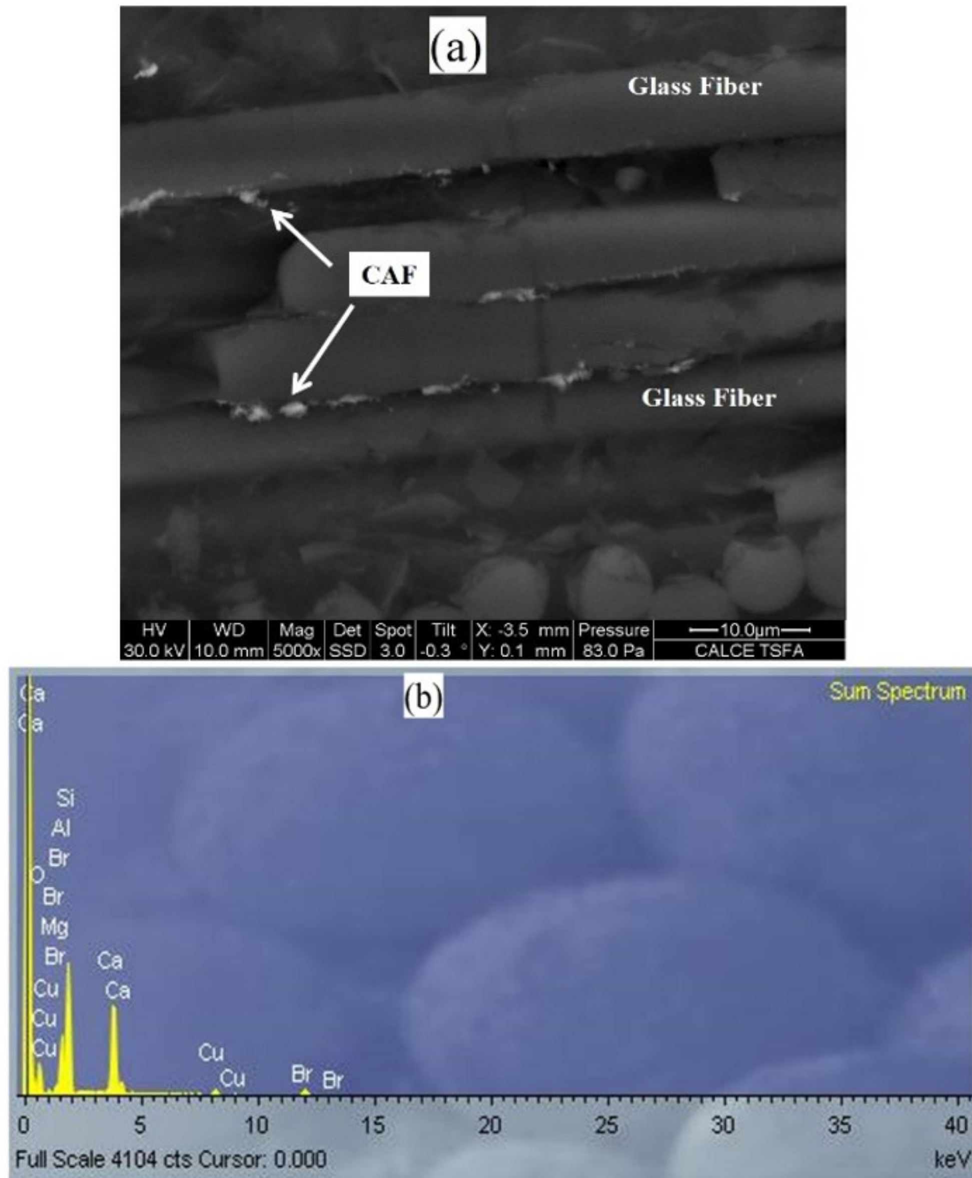


Figure 35 (a) Scanning electron microscope image of CAF observed between the glass fibers and the epoxy resin. Note, as opposed to the optical viewgraph, the SEM images show a fragmented pathway. The brightfield optical viewgraph, due to the higher depth of field, captures details from the focal planes that are beyond the viewing range with the SEM; (b) an EDS area elemental scan of the region shown in (a). Spectrum shows presence of elements such as copper, bromine and magnesium along with calcium, aluminum and oxygen.

4.2 Nano-indentation Study

In order to characterize the interphase between the glass fibers and the surrounding epoxy matrix, a nano-indentation study was conducted on the device under test sample #9 cross-section with the planes of PTHs 2 and 3 revealed. A similar, non-failed PCBA manufactured from a different lot of the same ISOLA 370HR circuit board base material was incorporated into the comparative study for comparison with the mechanical properties. An Agilent G200 nano-indenter was used for the comparative characterization. Nano-indentation allows the measurement of material properties such as hardness, modulus, and creep. Mechanical properties are measured as a function of indentation depth. In order to prepare the samples for nano-indentation, the non-failing PCBA samples were sectioned from the assembly and taken through the grinding and polishing steps in a similar method as the device under test sample #9.

After the non-failing sample was prepared, it was inspected by using a nano-indenter. A scratch test was conducted on the two samples. After the scratch tests were performed, the regions on the two surfaces were inspected by using a scanning electron microscope. Two micrographs in Figure 36 show the relative state of the surfaces after the nano-indentation was performed. A higher amount of debris is seen on the failed specimen. The wipe and accumulation seen in the failed specimen is not observed on the non-failed specimen. On the failed specimen, the glass fibers

appear to be splintered, whereas in the non-failed specimen, a small portion of the fibers appears to be sheared. The composition of the two glass fiber bundles was analyzed in EDS and was found to be similar.

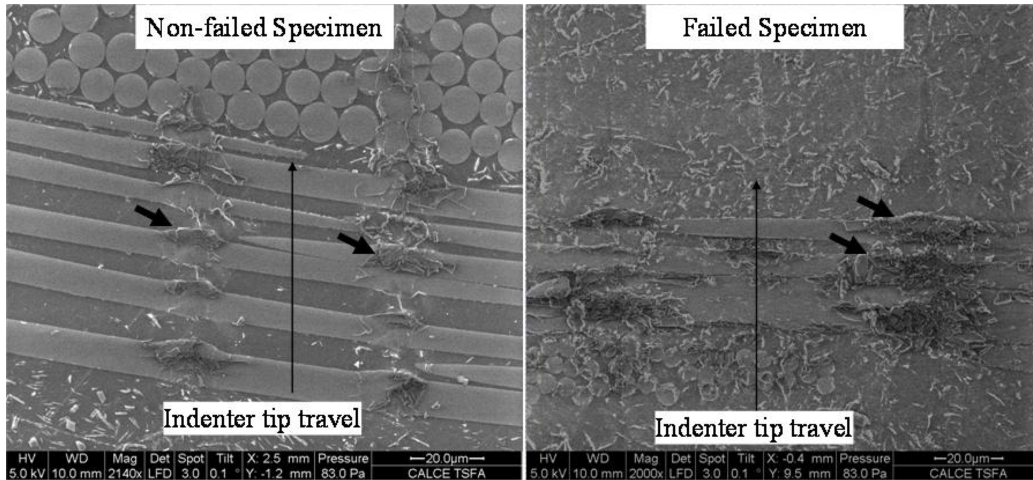


Figure 36 Wipe and accumulation seen in the non-failed specimen (left) is not observed on the failed specimen (right).

The nano-indentation results have shown that accumulation along the scratch is observed with the failed specimen, however, this behavior is not observed along the scratch induced on the non-failed specimen. The splintering of the glass fibers in the failed sample appears to suggest that the glass fibers are poorly adhering to the epoxy matrix which causes these to be pulled and splintered, whereas in the non-failed specimen, only a small portion of the fibers appears to be sheared suggesting that the glass bundles are better adhering to the matrix. The wipe and accumulation on either samples away from the glass fibers is similar, suggesting

that the region around the glass and the glass fibers themselves are behaving differently. As a follow-up and to determine whether the composition of the glass fibers was contributing to the behavior observed in nano-indentation, energy dispersive spectroscopy (EDS) was performed. The composition of the two glass fiber bundles was analyzed in EDS and was found to be identical.

The nano-indentation study has demonstrated that the interphase region demonstrates material properties that are distinct from those of the bulk epoxy. The study further shows that the moisture uptake can affect the interphase region, but the study is not able to drive a correlation between the expansion rate or the subsequent width of the IPN interphase to moisture content in the epoxy. The technique is not able to capture the viscoelastic properties of the PCB materials. The geometry of the indenter tip may also have to be better matched with IPN interphase geometry and do constituents of the PCB laminate such as fillers, flame retardants, interact with the nano-indenter tip. It is necessary to establish material properties of the interphase region in order to obtain the evolution of properties at the resin-glass interphases.

4.3 Results and Discussion

Conductive anodic filament formation is an electrochemical process that requires the transport of a metal through or across a nonmetallic medium under the influence of an applied electric field. Previous studies, along with analysis and examinations

conducted on failure sites in PCBs due to CAF, have shown that the conductive path is typically formed along delaminated or debonded glass fiber and epoxy resin interphases.

The filament formation typically takes place in two steps: a degradation of the resin/glass interphase followed by an electrochemical reaction. The two-step process of CAF includes the resin/glass fiber bond degradation and pathway formation, followed by an electrochemical reaction between the conductors. One method by which the pathway forms is due to breakage of the organosilane bonds at the glass/resin interphase. Bond degradation provides a path along which electrodeposition may occur due to electrochemical reaction. The path may result from poor glass treatment, hydrolysis of the silane glass finish, and mechanical stresses. Once the path is formed, an aqueous medium will develop through the adsorption, absorption, and capillary action of water. This breakage occurs by hydrolysis (adsorption of water at the glass fiber/epoxy resin interphase) or by repeated thermal cycling, which induces stresses at the interphase due to thermal expansion mismatches.

This chapter reviewed the organosilane-resin bonding process and summarized the processing and environmental phenomena that can result in breakage of the bonds. The technique of using in-situ resistance measurements during destructive physical analysis to confirm one has reached CAF filaments during cross-sectioning is the

first time this is described in the open literature. This solution addresses the potential problem in destructive physical analysis of grinding away the evidence of the CAF filament and ultimately loosing evidence at the failure site. The nano-indentation test and analysis at the glass-resin interphase suggests that this interphase undergoes degradation due to environmental factors. As a result of the failure analysis and subsequent investigations, the author recommends that systematic evaluation of mechanical properties at the glass/resin interphase be required at the OEM and PCB supplier level. The strength of the glass/resin interphase is influenced by physio-chemical stresses such as moisture and pH. By applying evaluation criteria, such as nano-indentation scratch tests, PCB material can be assessed for susceptibility to CAF and other failure causes in PCBs that are attributable to the glass/resin interfacial adhesion. OEMs can identify board suppliers based on answers to and validation of a series of questions. These questions focus on the necessary requirements of reliable board material manufacturing and are independent of the specifications of the product. The end deliverable is the identification of manufacturers who will provide reliable PCBs on a timely basis.

An upfront evaluation of PCB suppliers and manufacturers based on their ability to meet reliability requirements is critical for the PCB industry as most OEMs outsource board manufacturing capabilities. It is also needed because today's designs are much more complex and dense and call for a tighter process window

during the PCB material and manufacturing processes. Furthermore, as noted in the paper, an increasing number of electronic systems are failing due to problems traced back to the PCB. Failure in the field leads to increased costs and decreased customer confidence.

Chapter 5: Experiments to Inspect Epoxy/Glass Interphases Using FT-IT and AFM Atomic Force Spectroscopy

5.1 Introduction and Experimental Procedure

In order to assess the quality of glass to resin adhesion of commercially available printed circuit boards, experiments were performed. Samples consisted of two different laminate materials, a prepreg with two glass bundles of 2116 glass type and a core with also two glass bundles with a glass type 3113. The second core sample was thermally degraded at 530 ℃ to remove all epoxy material and also the coupling agents, this method was adapted from previous work done by Rogers [29]. Figure 37 shows the bare glass bundle from top view, this glass bundle sample was mounted using a two part epoxy. After the two part epoxy was cured, the sample was cross sectioned and polished. Cross section view was used for observation using optical microscopy, FTIR microscopy, and atomic force microscopy. The sample which was prepare by removing the epoxy with the 530 ℃ thermal degradation was designated "uncoated" and the prepreg samples are designated as "coated". This nomenclature was selected to ease in distinction between samples. Samples were baked in an oven until the weight loss due to the egress of moisture had stabilized. These samples are labeled as dried. Later these samples were exposed to 85 ℃ and 85% RH. These samples are labeled as humidified.

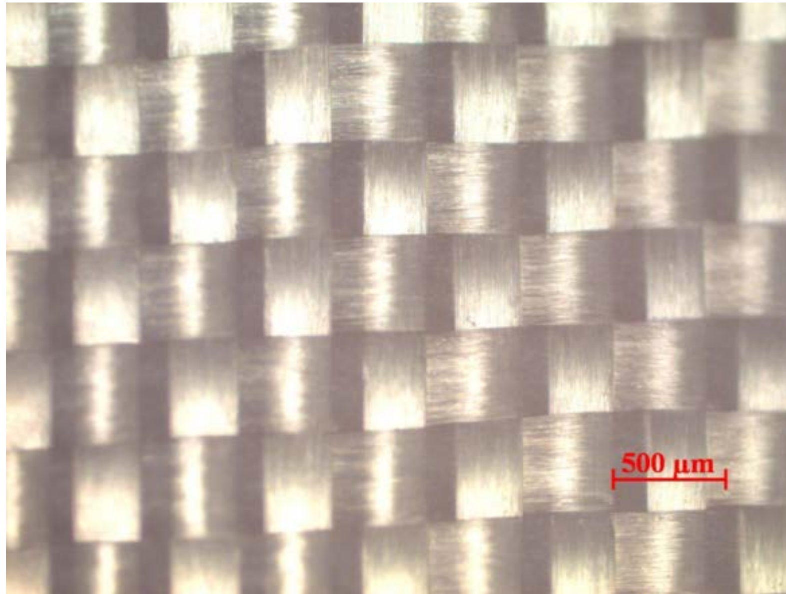


Figure 37 Laminate material thermally etched at 530 °C. Only glass bundle remained. The epoxy and the coupling agent were removed.

5.2 Fourier Transform Infrared (FTIR) spectroscopy Analysis

One of the most useful techniques for obtaining molecular structure information is FT-IR spectroscopy analysis. Since several components may be present at the resin to glass interphase: the glass fiber, coupling agents, curing agents, resin matrix and a hardener. All of these components must be characterized in order to perform meaningful subtractions to determine the reactions occurring at the silane interphase with the resin matrix. FT-IR has been used to characterize the reaction between silane coupling agents and epoxy resins [71] [72]. In the processing of reinforced composites the silane coupling agents are adsorbed/deposited on the

reinforcement material before the resin matrix is added. Often, the silane is thermally pre-cured on the surface of the reinforcement material.

In order to analyze the chemical changes after high temperature/high humidity test a FTIR spectrometer and a FTIR microscope with a 32 by 32 focal plane array (FPA) detector were used to acquire the FTIR spectra, and also to map images that contain 1064 microspectra Each scan area represents 70 by 70 microns. Images were generated using a 15X Optical/IR objective lens. FTIR microscopy was selected as a tool for this analysis because it can accurately acquire spectra from a small sample region, providing spatial and spectral information. Images were analyzed and the identification of the functional groups was made, Si-O bonds were identified in the coated and uncoated samples due to the presence of silicon atoms in the glass fiber samples. Vibrations between atoms in Si-O molecules excited by infrared radiation could be either absorb or transmit. Figure 38 a) is an optical image of the cross section of a dried coated sample, the glass bundle and the epoxy are highlighted with arrows. Figure 38 b) is the IR mapping image, lighter colors are related to the Si-O molecules. The IR spectrum showed in Figure 39 corresponds to the signal acquired from the glass bundle, the Si-OH and OH functional groups were detected.

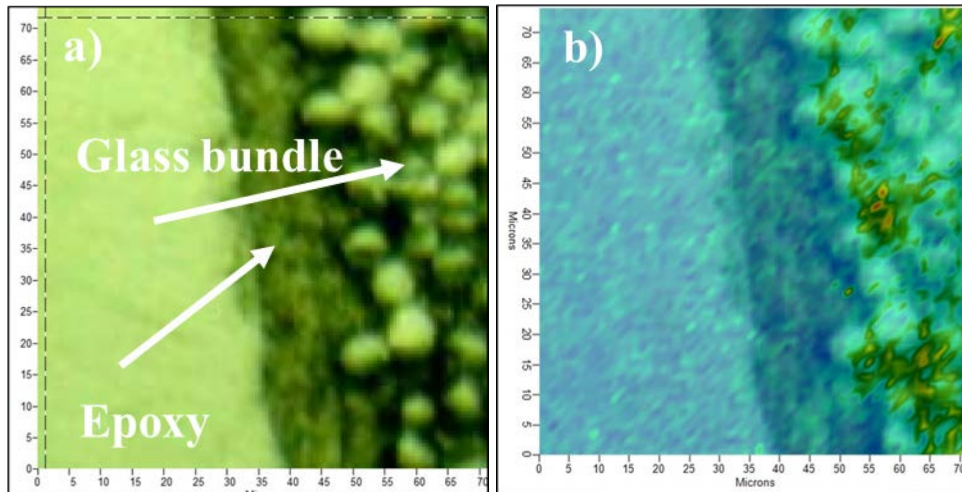


Figure 38 a) Optical image and b) IR image of cross section view of non-coated siloxane sample.

The organic functional group detected by the FTIR in the dried uncoated sample was the Si-O, which were located at 1038 cm^{-1}, shown in Figure 39. In Figure 40, after the sample was exposed to humidity test, the hydroxyl group around 3200 cm^{-1} are present. There is an evidence of water absorption and also it can be noticed that there are new peaks associated to Si-OH functional groups.

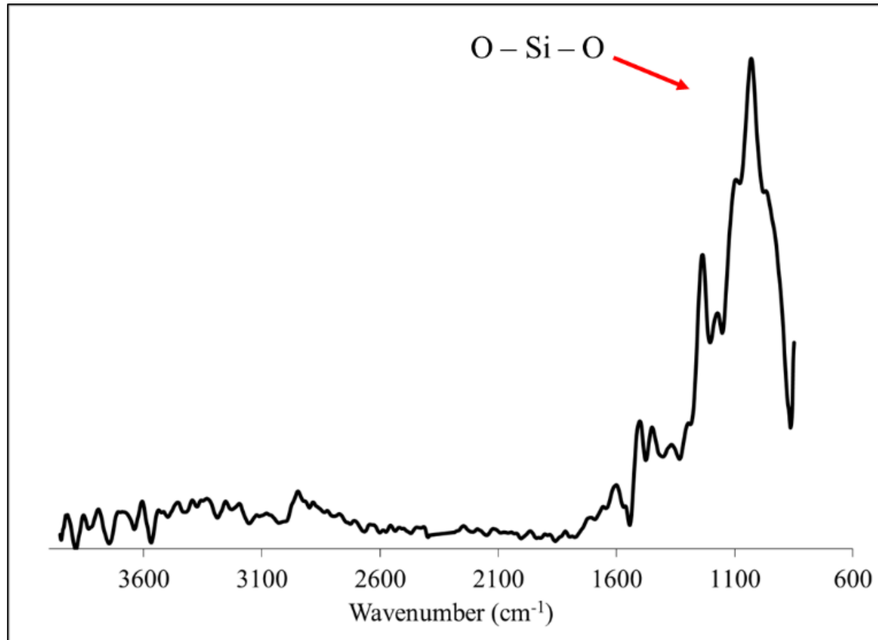


Figure 39 IR spectrum of dried uncoated sample. Evidencing the presence of Si-O bonds from the glass fiber.

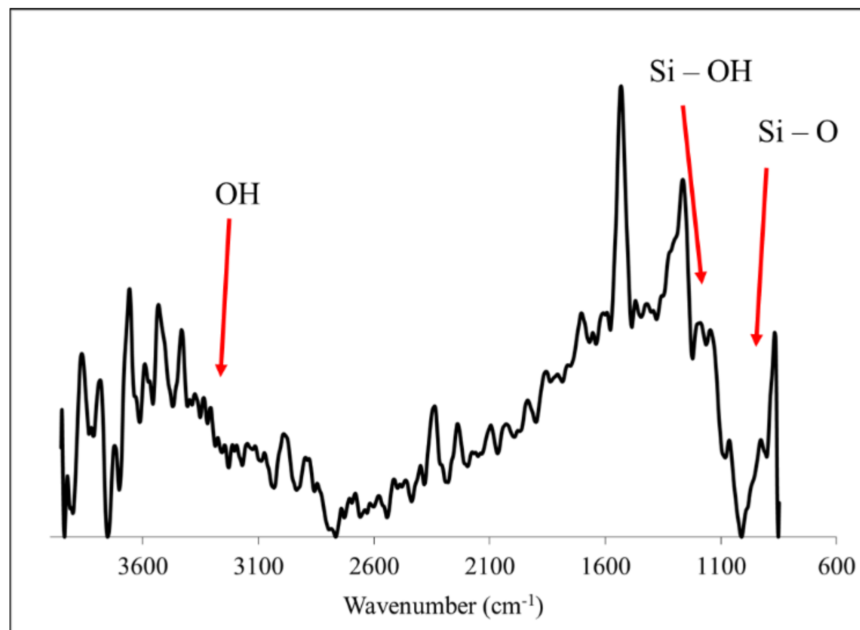
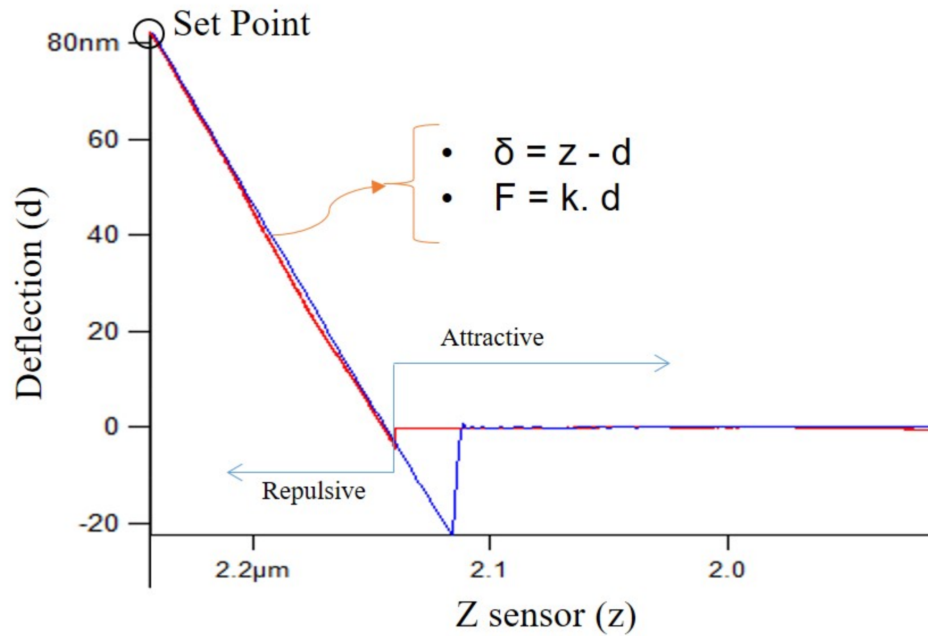


Figure 40 IR spectrum of uncoated sample after humidity test.

FT-IR can be used to follow the reaction process but this yields no information on the mechanical properties of the composite. Mechanical property tests are needed to determine if increasing the penetration of the resin into the silane interphase and the extent of the reaction have a positive effect on improving the mechanical properties.

5.3 AFM Force Spectroscopy Analysis

Since epoxy materials that are used in the fabrication of laminate materials in PCB are viscoelastic, the technique that was selected for this analysis was based on atomic force microscopy (AFM) static force spectroscopy (SFS), shown in Figure 41.



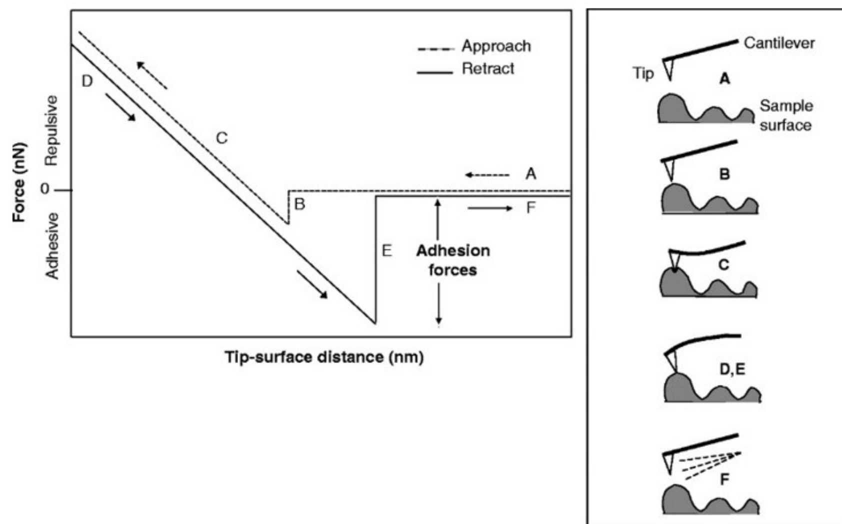


Figure 41 Schematic illustration of the static force spectroscopy principle [75].

SFS is based on the interaction between the cantilever tip and the glass/epoxy interphase on dried and humidified samples [75]. Figure 41, shows an idealized

force-distance curve describing a single approach-retract cycle of the AFM tip [74], which is continuously repeated during surface scanning. The AFM tip is approaching the sample surface (A). The initial contact between the tip and the surface is mediated by the attractive van der Waals forces (contact) that lead to an attraction of the tip toward the surface (B). Hence, the tip applies a constant and default force upon the surface that leads to sample indentation and cantilever deflection (C). Subsequently, the tip tries to retract and to break loose from the surface (D). Various adhesive forces between the sample and the AFM tip, however, hamper tip retraction. These adhesive forces can be taken directly from the force-distance curve (E). The tip withdraws and looses contact to the surface upon overcoming of the adhesive forces (F).

For the present analysis the cantilever approaches the interphase between the glass fibers and the resin matrix at different velocities, a schematic illustration of the AFM cantilever on the cross-sectioned PCB sample is shown in Figure 42 Schematic illustration of the AFM cantilever on the cross-sectioned PCB sample.. The aim of this analysis is to obtain information about the viscoelastic behavior of the glass-resin interphase. In the analysis of AFM as shown in Figure 43, Figure 44 and Figure 45, it was found that the slope of the curves for humidified samples are higher.

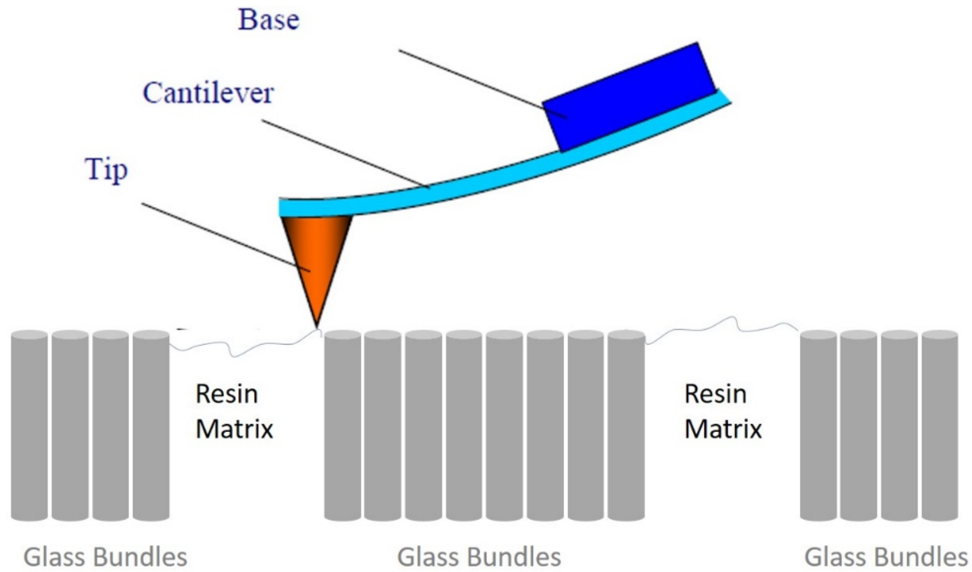


Figure 42 Schematic illustration of the AFM cantilever on the cross-sectioned PCB sample.

Higher slope refers to higher compliance / less stiff material. However the dry sample is more viscoelastic and has higher dissipation behavior. The analysis shows that the slope for humidified sample is higher, in other words, a higher compliance or a softer material – which means that as the samples absorb moisture, the interphase between the glass and resin becomes softer. However the dry sample includes both viscous and elastic behaviors because a dry sample has higher dissipation behavior. Additionally, the analysis also shows that all samples show a velocity dependency. The analysis was performed in contact mode, there was no vibration involved in the measurement, and the test was repeated a 100 times at the same location.

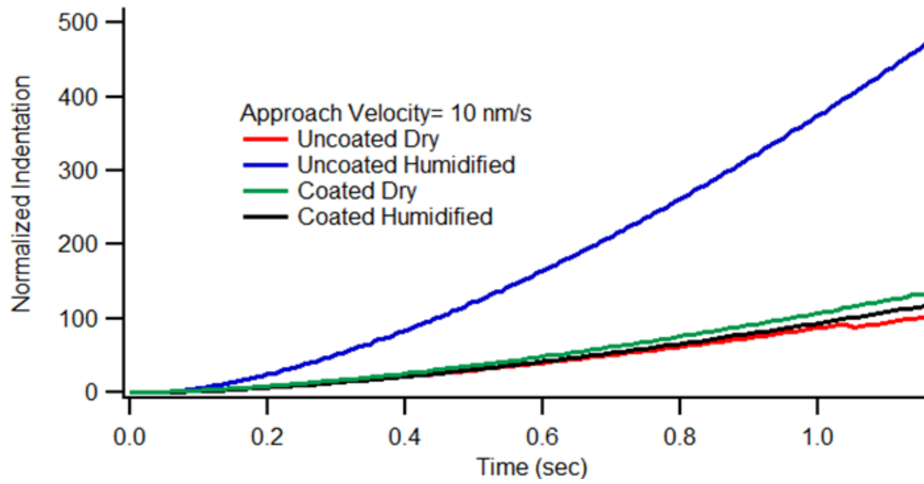


Figure 43 Comparison between the normalized indentation of dried and humidified samples at 10nm/s

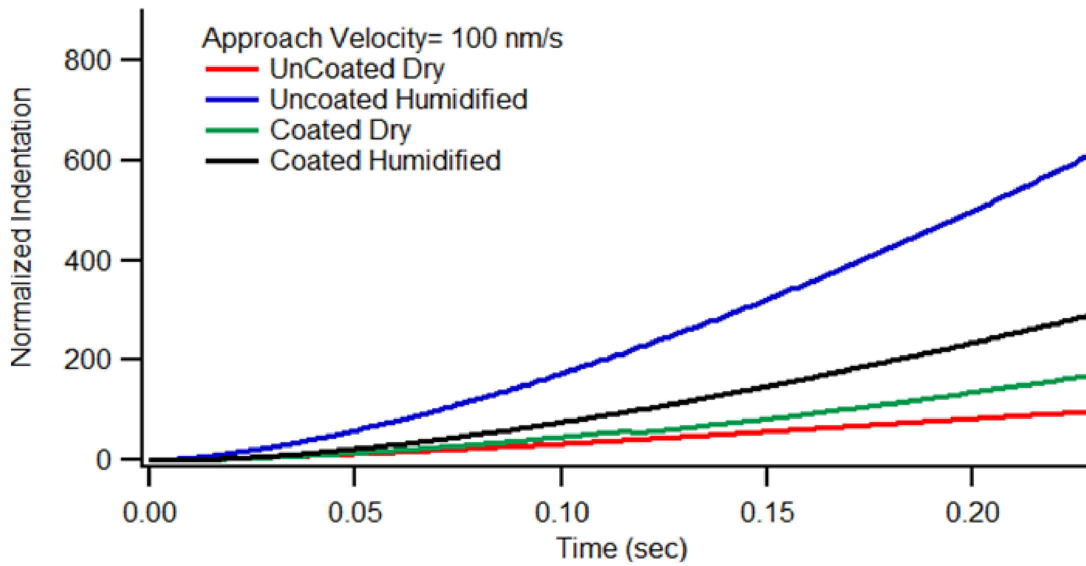


Figure 44 Comparison between the normalized indentation of dried and humidified samples at 100nm/s

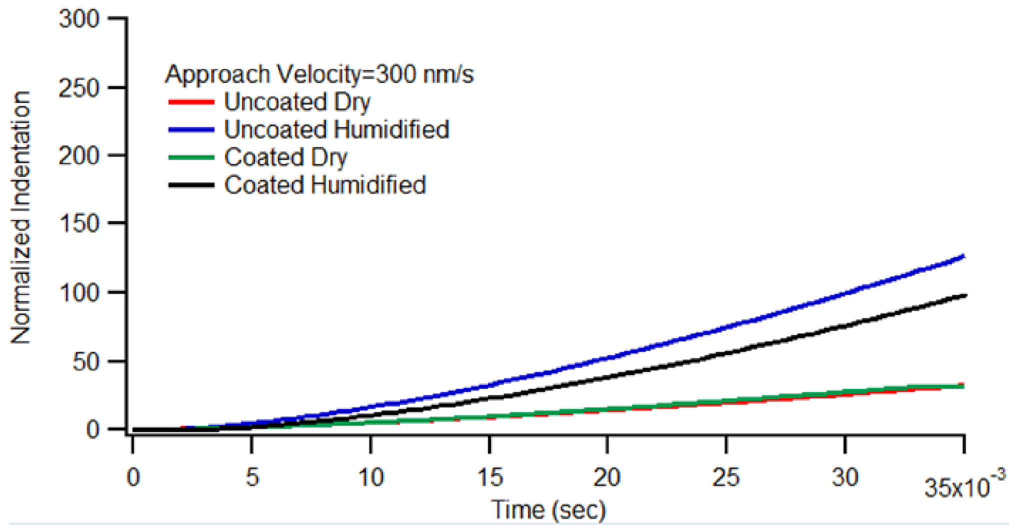


Figure 45 Comparison between the normalized indentation of dried and humidified samples at 300nm/s

5.4 Summary of FT-IR and AFM Studies

Analytical techniques such as AFM atomic force spectroscopy have the advantage of providing a rapid evaluation of the critical interphases that can contribute to overall PCB reliability and quality. There are many printed circuit board laminate manufacturing steps, each of which can install an unrepairable defect into the board. PCBs are an integrated item which cannot be disassembled for repair. Most PCB defects cannot be repaired, and PCBs are not made in production lots but are instead made in panels. For understanding CAF type of electrical shorts in printed circuit boards, the behavior of the glass-resin interphase in “off-the-shelf” PCB materials is key. AFM atomic force spectroscopy experiments were shown to target the changes to viscoelastic properties of the glass-resin interphase in FR4 materials.

Process variations can occur from panel-to-panel and across a single panel. With few exceptions (e.g. electrical test, external visual), groups of boards cannot be screened for defects, instead, destructive quality conformance inspection such as the ones described here can be performed on a representative sample of each manufacturing lot.

This chapter showed a unique approach where PCB laminate materials are chemically and mechanically analyzed at a microscopic level using an AFM atomic force spectroscopy technique Microscopic examination has previously shown that conductive anodic filaments can be formed along debonded or delaminated fiber glass and epoxy resin interphases. The debonding between the glass and epoxy is largely attributed to the breaking of the organosilane bonds. The organosilane bonds can be chemically degraded by hydrolysis (adsorption of water at the fiber glass/epoxy resin interphase) or by repeated thermal cycling, which induces stresses at the interphase due to coefficient of thermal expansion mismatches.

To determine the feasibility of analysis and detection of silicon functional groups and moisture ingression in printed circuit boards, coupons were made of laminate materials, with and without siloxane coatings and exposed to 85ºC and 85% RH, it was possible to detect functional groups associated to silicon and moisture absorption using FT-IR. Regarding the mechanical behavior after temperature and moisture exposure, samples presented a more elastic response to an AFM cantilever

tip approach. Original equipment manufacturers and researchers can use the methodology developed in this work as an alternative to characterize and screen laminate materials..

Chapter 6: Focused Ion Beam Inspection of Glass-Resin Interphases

6.1 Introduction

A printed circuit board assembly in the form of a module was analyzed for a suspect circuit node with a reported intermittent fault, an overview of the suspect region of the module is shown in Figure 46 and a closer view in Figure 47. The assembly module was submitted for electrical testing of the suspect nodes (named KCP+ and RST_DRV in the module) which did not reveal any leakage (0.0µA@ 3.3V) another node when monitored with a curve tracer for intermittent leakage. No electrical leakage currents were measured after an overnight continuous bias.

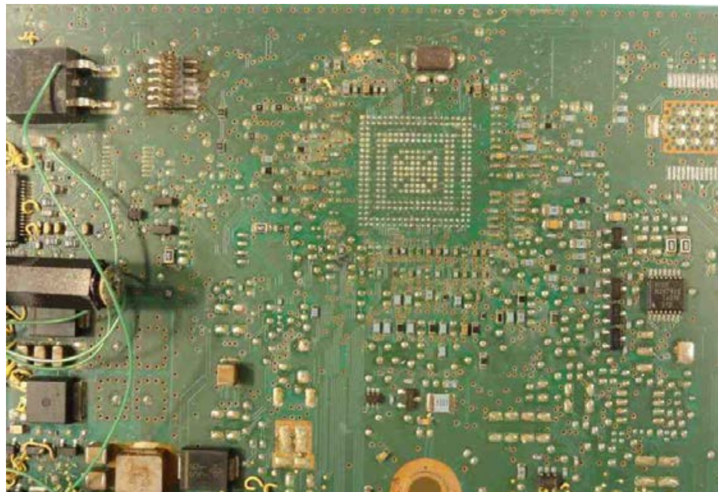


Figure 46 Overview of front side of a PCB module showing the region which contains the suspect nodes KCP+ and RST_DRV. Note: the microprocessor was removed for the purpose of this experiment.

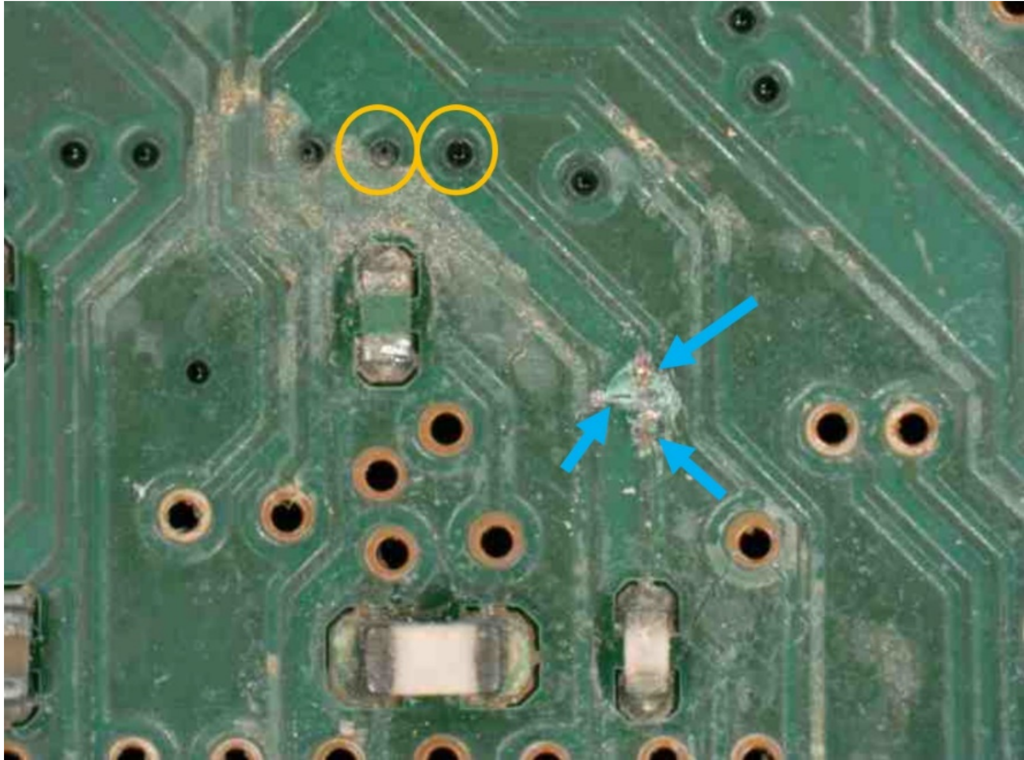


Figure 47 Closer view of suspect KCP+ node via and trace which was cut for the purpose of fault isolation. Blue arrows indicate the locations for electrical probing while monitoring with curve tracer. No leakage was observed between the vias, circled in yellow.

The module was prepared for planar cross-sectional analysis of the two adjacent vias for KCP+ and RST_DRV. Optical inspection has revealed crazing along a row of vias containing vias for KCP+ and RST_DRV. Figure 48 shows bottom side (microprocessor side) view of PCB during preparation for planar sectioning. Copper layer #4 was removed to allow backside lighting. This exposed suspect vias RST_DRV and CKP+ inspection and measurements. A line of glass fiber to epoxy

delamination was observed along this row of vias, highlighted by blue arrows as shown in Figure 49. A closer view is shown in Figure 50.

Figure 48 Bottom side (microprocessor side) view of PCB during preparation for planar sectioning. Copper layer #4 was removed to allow backside lighting. This exposed suspect vias RST_DRV and CKP+ for measurement of the drill size and via spacing.

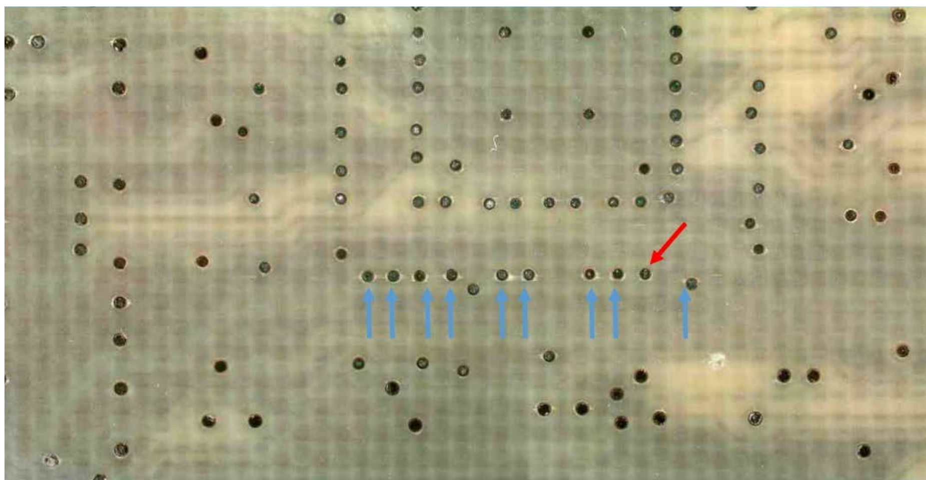


Figure 49 Overall top down view of the laminate after removal of copper layer number 4. Suspect KCP+ via is highlighted by red arrow. A line of glass fiber to epoxy delamination was observed along this row of vias, highlighted by blue arrows.

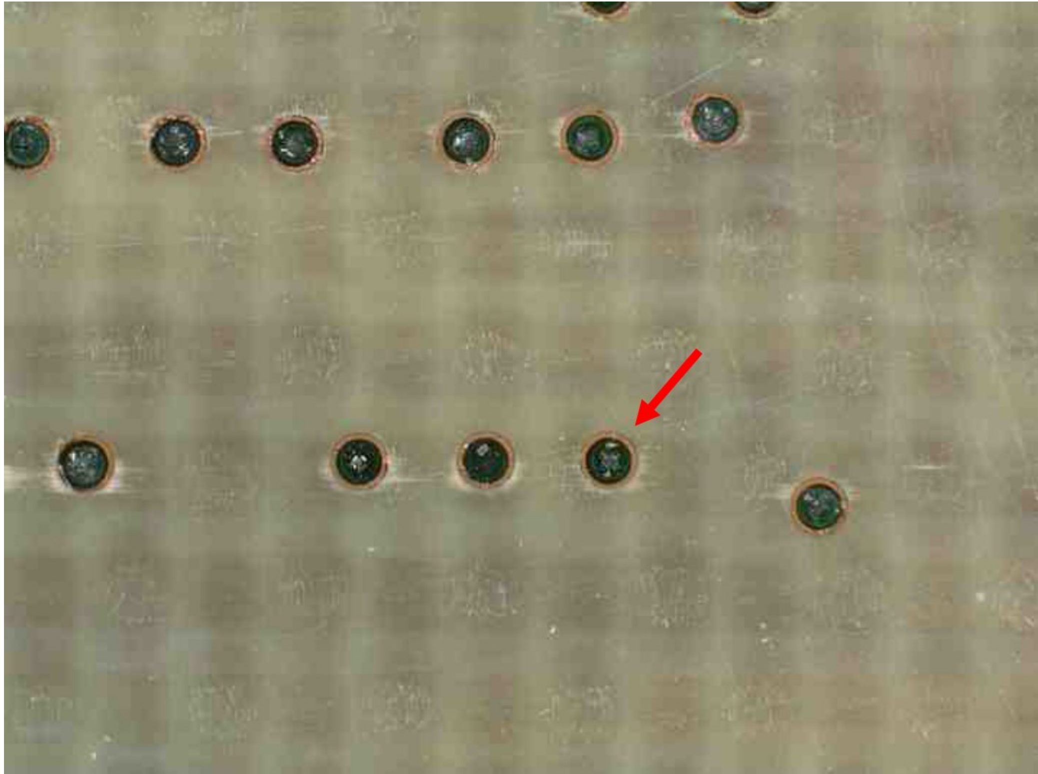


Figure 50 Closer view laminate after removal of copper layer #1 with suspect KCP+ via highlighted by red arrow.

6.2 Focused Ion beam (FIB) Inspection

Focused ion beam (FIB) was further performed on this section to inspect the quality of the glass to fiber interphase. FIB is selected because it enables selecting removal of material from the surface to expose the interphase of interest. The equipment used to make the final cross section cut is an early model FEI dual beam system. The system consists of a SEM column and a FIB column configured on the same chamber with an angle of about 53 degrees between the two beam lines. A stage with motorized translation and rotation and manual tilt

and height control allows the features of interest on the sample to be positioned precisely at the intersection of the two beams. The advantage of this sample preparation is that the wall of a box cut being made by the focused ion beam is typically in clear view of the SEM allowing a visual guide.

This sample having already been cross-sectioned with conventional mechanical methods is mounted so the ion beam impinges at a glancing angle (<15 degrees) with the face of the existing cut. Closer view of RST_DRV and CKP+ vias with selected measurements of suspect paths are shown in Figure 51. The green box indicates the location of the FIB cutting, with the blue arrow indicating viewing orientation The first ion beam cut uses the largest current (11 nanoamps) in a thin and wide box (~20 by 100 microns). Figure 52 shows a rotated and angled SEM view of RST_DRV and CKP+ vias with suspect gap highlighted by arrow within the FIB cut.

Figure 51 Closer view of RST_DRV and CKP+ vias with selected measurements of suspect paths. The green box indicates the location of the FIB cutting, with the blue arrow indicating viewing orientation.

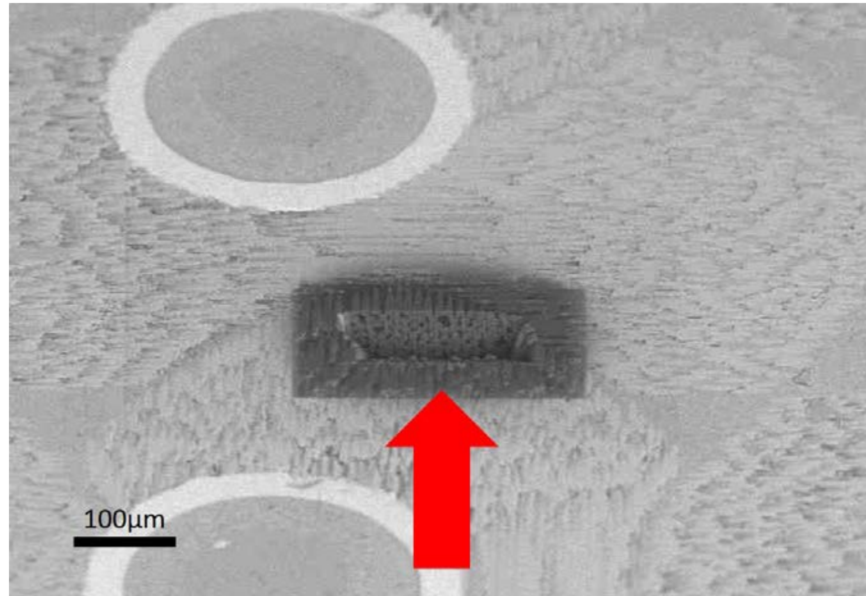


Figure 52 Rotated and angled SEM view of RST_DRV and CKP+ vias with suspect gap highlighted by arrow within the FIB cut.

FIB removes the glass fibers selectively from the earlier mechanical micro-section. Beams with successively lower currents are then used to trim the face of the cut until the interphases of interest are clearly imaged in the SEM. Slight adjustments in the position of each trim cut are made based on observation of the progress as indicated in SEM image. The shallow angle of the cut makes it difficult to follow the more common method of using ion beam images for positioning the trim cuts. However, the shallow angle made it possible to create a larger exposed face in a shorter time. FIB sectioning has confirmed the presence of separation between a

glass fiber and the epoxy in the prepreg laminate, as shown in Figure 53 and between copper layers #1 and #2.

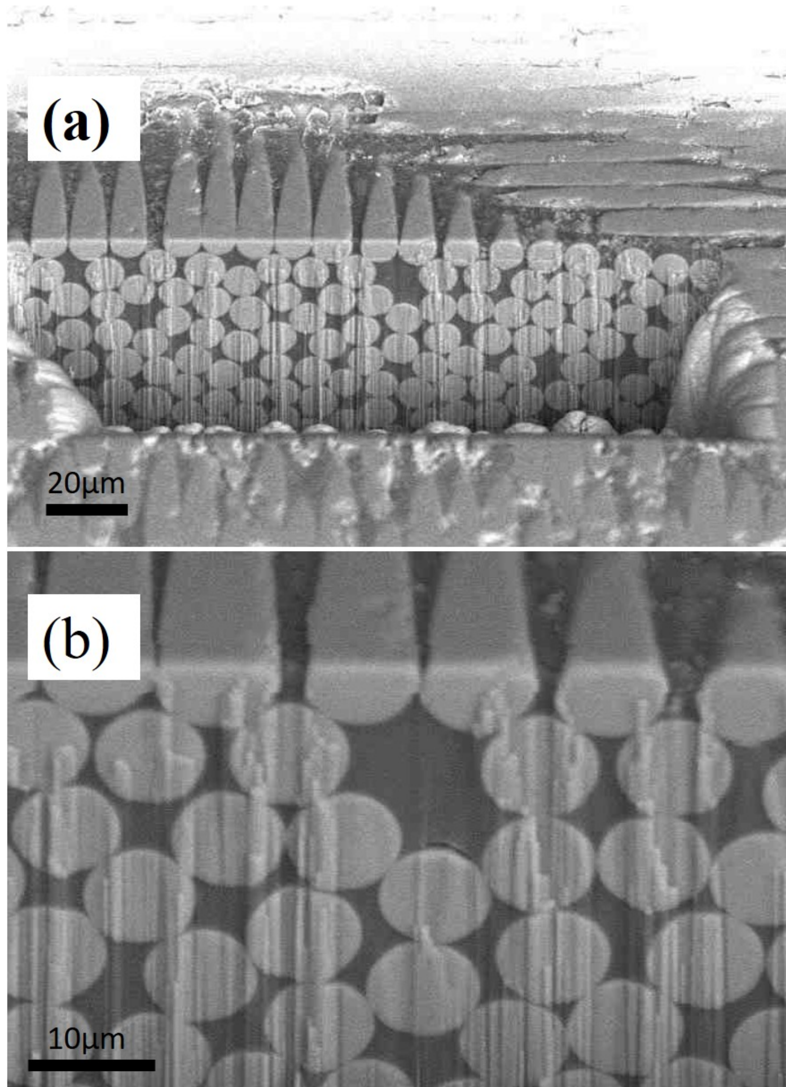


Figure 53 Closer view of suspect glass fiber bundle.

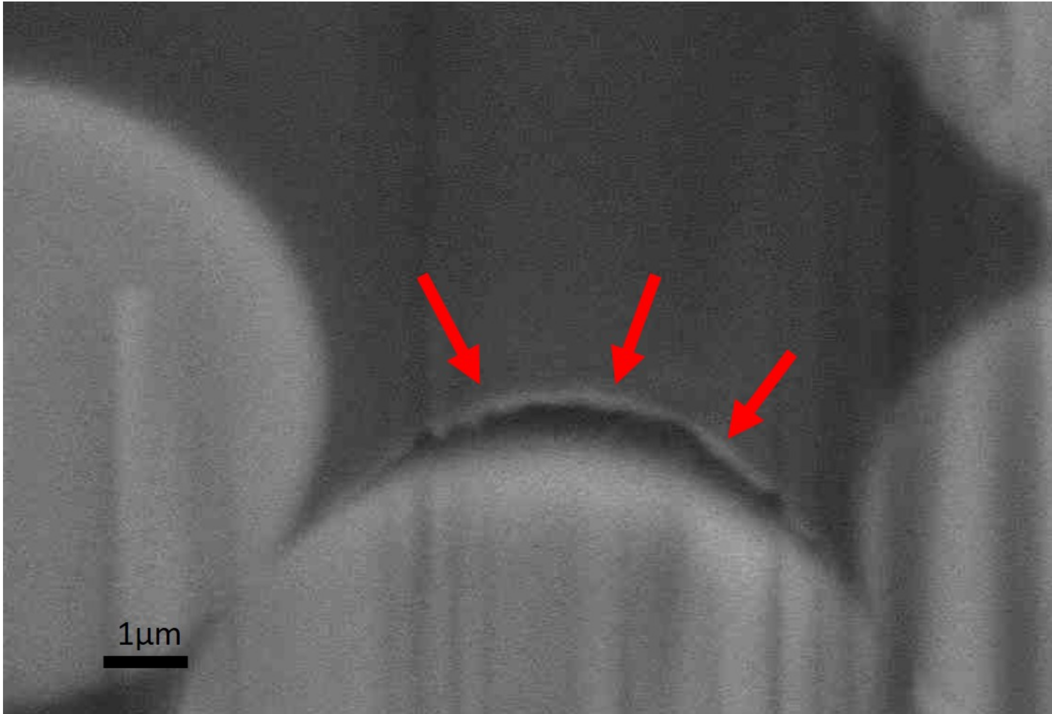


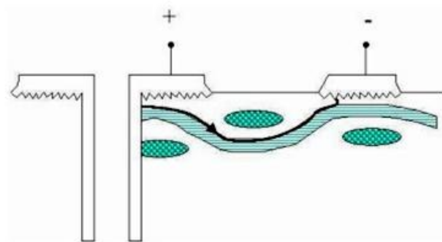
Figure 54 Closer SEM view of the separation between a single fiber and the epoxy.

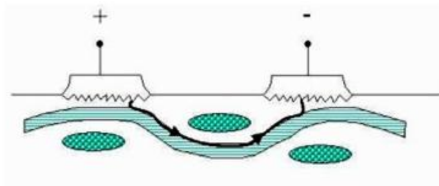
SEM inspections and Energy Dispersive X-Ray Spectroscopy (EDS) elemental analysis confirmed the presence of copper within the glass to resin separation within this layer. The glass to resin separation within the core laminate layer provided a path between the suspect vias with copper being observed at many locations within the laminate cracking.

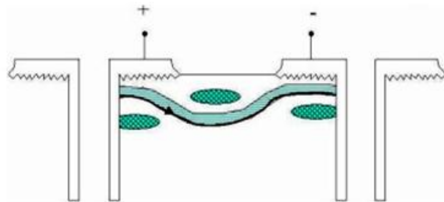
Chapter 7: Path Formation in CAF

Prior to or simultaneously with the formation of the filament, a pathway connecting the oppositely biased conductors must be formed. Three of the common pathways (PTH/PTH, PTH/plane and plane/plane) in addition to vertical filament formation are observed. In the case of vertical filament formation, the PCBs experience a drop in insulation resistance by shorted internal planes, which was verified after physical identification of a hydrolyzed Cab-o-sil particle at a failure site [56]. Other path configurations include formation between PTHs and power/ground planes, between internal traces, between an internal trace and a PTH, and between internal and surface traces. It is hypothesized that path formation, proposed to be voltage-independent, is the rate-limiting step in CAF. In other words, it takes a much longer time for the pathway to form than for the metal migration and formation of the conductive anodic filament to bridge and short the two conductors. The rate-limiting step of CAF induced failure is the creation of the path. Hollow fibers, discussed previously [36], can also contribute to CAF by creating an open path between biased conductors. The common pathways are show in Figure 55. Other path configurations include formation between PTHs and power/ground planes, between internal traces, between an internal trace and a PTH, and between internal and surface traces. Figure 56 shows an actual CAF failure between two adjacent PTHs.

It is hypothesized that path formation, proposed to be voltage independent, is the rate-limiting step in CAF. In other words, it takes a significantly longer time for the pathway to be formed than for the metal migration and formation of the conductive anodic filament bridging and the shorting of the two conductors [37].







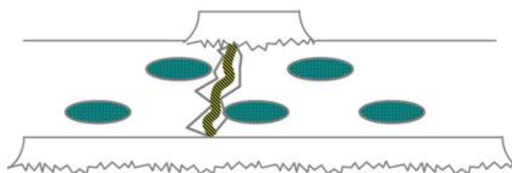


Figure 55: Common CAF pathway configurations are shown. Hollow fibers can also contribute to CAF by allowing an open pathway [37].

7.1 Path Caused by Mechanical Degradation

Mechanical degradation or physical delamination can occur at the interphases of the glass fibers and epoxy resin matrix (see Figure 57). Mechanical stress can arise due to the coefficient of thermal expansion (CTE) mismatches in the properties of the epoxy resin and the glass fibers. CTE values for cured un-reinforced epoxy resin can range from 50 to 65 ppm/^{o}C (depending on the amount of diluents), while that of the glass fibers in the radial direction is approximately 5 ppm/^{o}C [38]. Studies by Li et al. [39] show that this mismatch can lead to interfacial stresses and de-bonding at the fiber-resin interphase during thermal cycling. Manufacturing defects can accelerate and help to initiate the formation of this pathway.

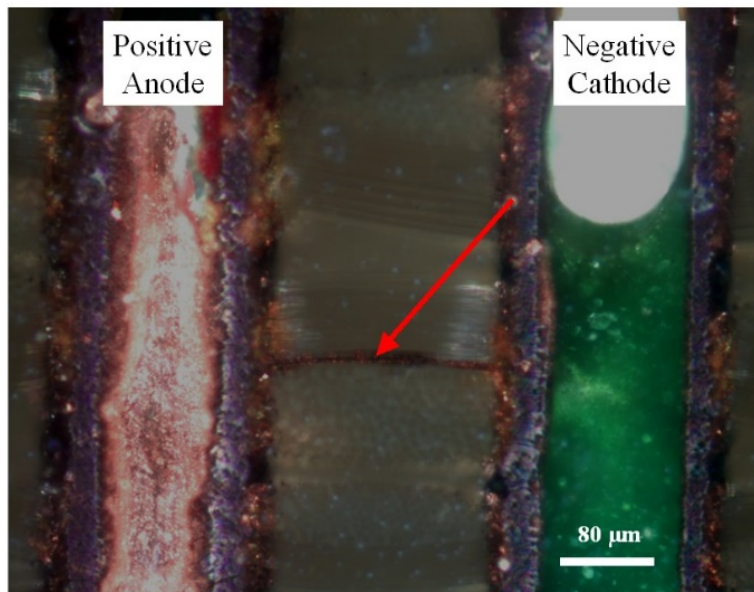
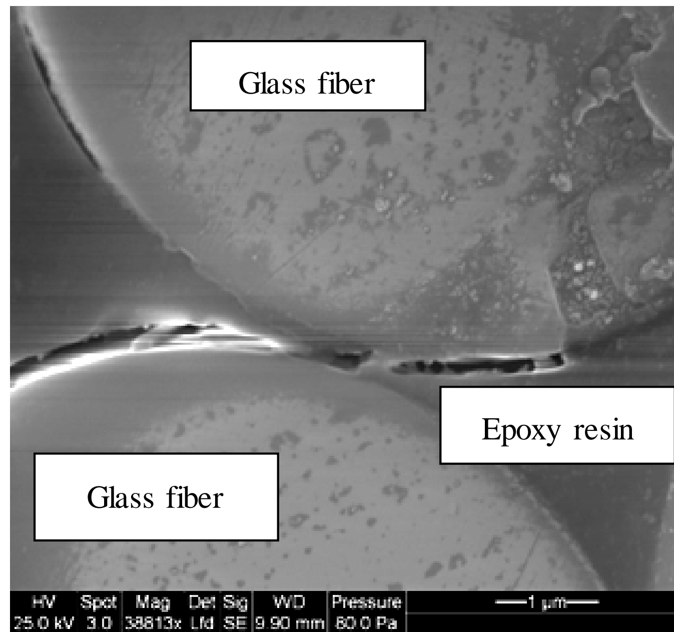


Figure 56. This optical darkfield photo shows a conductive anodic filament close to but under the polished cross-sectional resin plane, connecting and electrically shorting two adjacent PTHs.



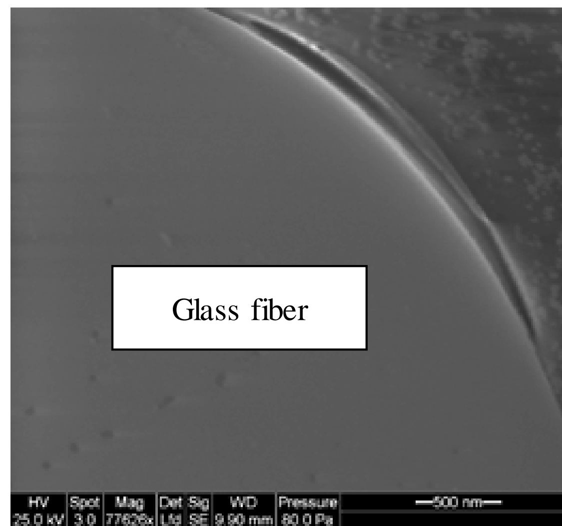


Figure 57. These E-SEM photos show physical delamination at the interphases of the glass fibers and epoxy resin matrix. De-bonding can occur due to mechanical stresses arising due to the coefficient of thermal expansion (CTE) mismatches in the properties of the epoxy resin and the glass fibers during thermal cycling. [54]

The difference in the moisture absorption of glass fibers and epoxy resin can also lead to interfacial stresses. During thermal-humidity cycling, the swelling and shrinking of the epoxy has been shown to induce physical de-bonding at the fiber glass/epoxy resin interphase, in addition to micro-cracking in the resin [39]. The absorption of moisture can also reduce the T_g of the laminate, allowing excess thermal stress to cause more damage [40], [41]. Path formation, where there is a physical, mechanical separation at the fiber glass/epoxy resin interphase or micro-cracking due to thermal cycling and thermal-humidity cycling, may not be reversible.

7.2 Path Caused by Hollow Fibers

During the manufacture of glass fibers, a homogeneous melt composition with negligible impurities is necessary to prevent the decomposition of raw materials. The sublimation of these organics can lead to trapped gases. Depending on the viscosity of the glass mixture and various manufacturing processes, these gases can get trapped as bubbles, called seeds. Seeds are a naturally occurring part of the process and thus methods to remove them are necessary. If the molten glass contains a sufficient level of impurities, air bubbles may become trapped inside the fibers while being drawn through the bushing. These air bubbles, unless very large, do not cause fiber breakage but end up as capillaries in the glass fibers, otherwise

known as hollow fibers (see Figure 58). These hollow glass fibers increase the opportunity for failure between close conductors because the capillary provides a convenient path for the formation of conductive anodic filaments [43]-[47]. Hollow fibers pose a serious reliability threat because with hollow fibers the rate limiting step, T_1, is eliminated from the two-step sequential process. T_1 consists of path formation, followed by T_2, which is the electrochemical reaction, where $T_1 >> T_2$ [28].

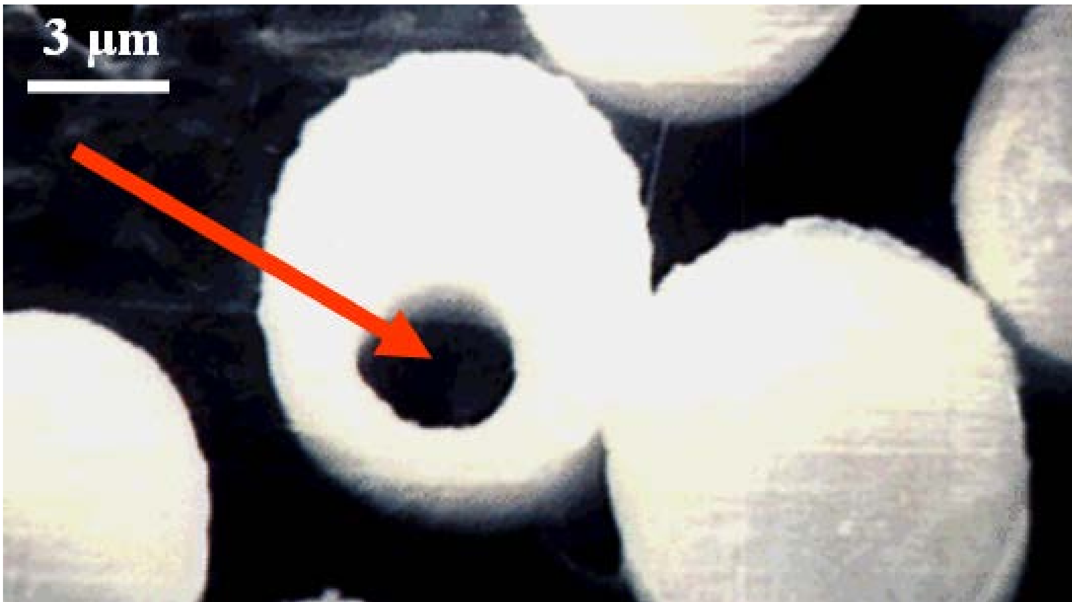


Figure 58. Image of a hollow fiber (red arrow) [36].

7.3 Path Caused by Cracks in Resin Filler Particles

In a set of PCBs failing by shorted internal planes, the root cause was determined to be conductive anodic filament formation in the vertical direction via cracked

Cabosil (fused silica) particles [29]. This determination required actual physical identification of a hydrolyzed Cabosil particle at a failure site (see Figure 59 and Figure 60). Unfortunately, this was made difficult by the large area covered by the power and ground planes, which made identification of the failure site using functional or parametric testing impossible.

Due to the particles being larger than the vertical spacing between the power and ground planes, during lamination of the boards, larger particles are trapped in the vertical gap between the power and ground planes and cracking. In humid environments during testing and operation, these internal cracks in the Cabosil allow moisture to ingress into the existing path, leading to conductive anodic filament growths.

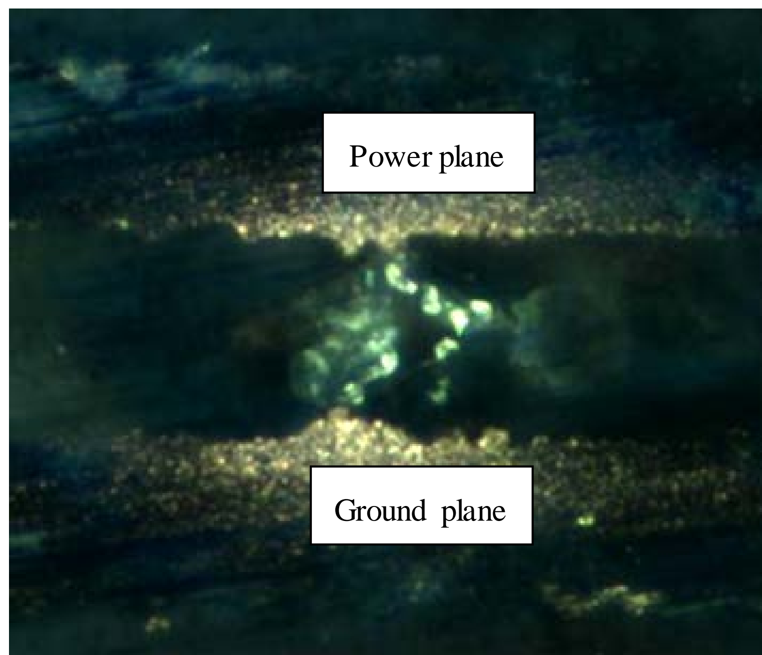


Figure 59. Optical photo of conductive filament formed in the vertical direction between cracked Cabosil filler particles [29].

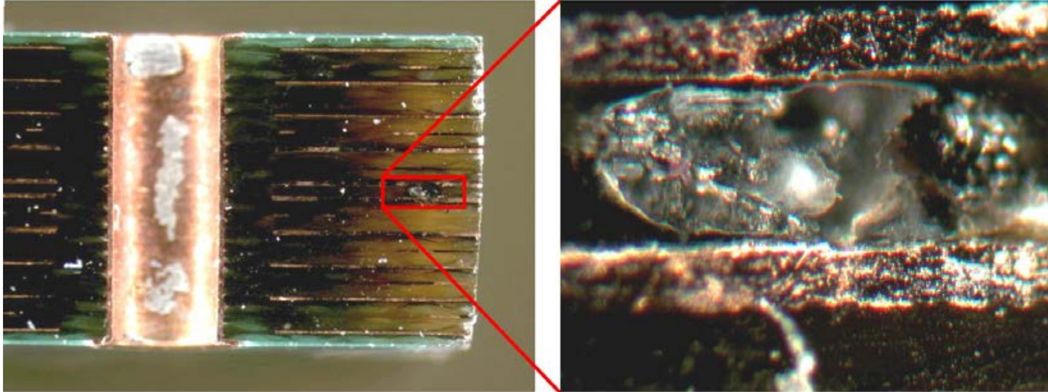


Figure 60. Optical photos show a charred burnt area between the power and ground plane in a printed wiring board due to vertical filament formation [29].

7.4 Path Caused by Chemical Degradation

A pathway between conductors may be formed by chemical hydrolysis of the silane glass finish or coupling agent. Studies indicate that the glass epoxy interphase absorbs 5 to 7 times more moisture than the bulk epoxy [42]. The most common cross-linking agent used in FR-4 and many other epoxy-based laminated systems is dicyandiamide (dicy). Dicy is hydrophilic and, to some extent, so is the glass surface. This combination of a hydrophilic surface and a hydrophilic cross-linking agent appears to be one of the factors responsible for the mechanism whereby chemical degradation of the glass fiber/epoxy resin interphase due to hydrolysis occurs. Williams et al. [41] have shown that PCBs manufactured with non-dicy

cross-linked epoxy resins exhibit much more resistance to CAF failures compared to PCBs manufactured with dicy cross-linked epoxy resins. Research by Mitchell et al. [28] demonstrated that this type of chemical degradation may be reversible.

One manner in which the pathway between conductors is formed in PCBs is chemical hydrolysis of the silane glass finish or coupling agent. Past work has shown that the glass epoxy interphase absorbs 5 to 7 times more moisture than the bulk epoxy [61]. A common cross-linking agent used in FR-4 and many other epoxy-based laminated systems is DICY. DICY and glass surfaces are both hydrophilic. This combination of a hydrophilic surface and a hydrophilic cross-linking agent is one of the factors responsible for degradation of the glass fiber/epoxy resin interphase due to hydrolysis. Williams [62] has shown that PCBs manufactured with non-DICY cross-linked epoxy resins are more resistant to CAF failures than PCBs manufactured with DICY cross-linked epoxy resins.

Organosilanes are bifunctional molecules that act as adhesion promoters, cross-link agents, and moisture scavengers in adhesive and sealant products [63]. Silane adhesion promoters act as molecular bridges between two chemically different materials and have been shown to dramatically improve the adhesion of polymeric resins to substrates such as glass, silica, alumina, or active metals [64].

Figure 61 illustrates a typical alkoxysilane coupling agent and its hydrolysis reaction. Typically, the silane is functional at both ends. R is an active chemical

group, such as amino (NH_2), mercapto (SH), or isocyanato (NCO). This functionality reacts with functional groups in an industrial resin or biomolecule such as DNA fragments. The other end consists of a halo (most often chloro) or alkoxy (most often methoxy or ethoxy) silane [29]. This functionality is converted to active groups on hydrolysis called silanols. The silanols can further react with themselves, generating oligomeric variations. All silanol variations can react with active surfaces that contain hydroxyl (OH) groups. A pathway between conductors may also be formed by chemical hydrolysis of the silane glass finish or coupling agent. Research has demonstrated that this type of chemical degradation might be reversible [66] [67].

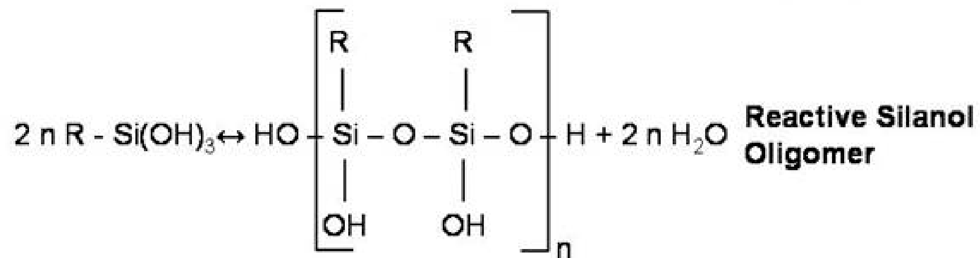


Figure 61 Alkoxysilane coupling agent and its hydrolysis reaction.

The three main classes of silanes are chloro-, methoxy-, and ethoxysilanes. Chlorosilanes are the most reactive, but evolve into corrosive hydrogen chloride on

hydrolysis; methoxysilanes are of intermediate reactivity; ethoxy-silanes are the least reactive and evolve into nontoxic ethanol . The difference in reactivity between methoxy- and ethoxysilanes is small; at typical hydrolysis pH (acidic ~5, basic ~–9), both versions hydrolyze in under 15 min at 2% silane concentrations.

The bifunctional silane molecules act as a link between the glass fiber and resin by forming a chemical bond with the glass surface through a siloxane bridge, and the organofunctional group bonds to the polymeric resin [29]. This allows silanes to function as surface-treating or "coupling" agents. The formation of an interpenetrating network (IPN) through interdiffusion is the next step in the process. Figure 62 shows a schematic for interdiffusion and creation of an IPN in a silane-treated glass fiber [66]. Interdiffusion and intermixing take place in the coupling agent/polymer resin interphase region due to penetration of resin into the chemisorbed silane layer and migration of the physisorbed silane molecules into the resin phase. The migration and intermixing of silane and other sizing ingredients with polymer resin create an interphase of substantial thickness.

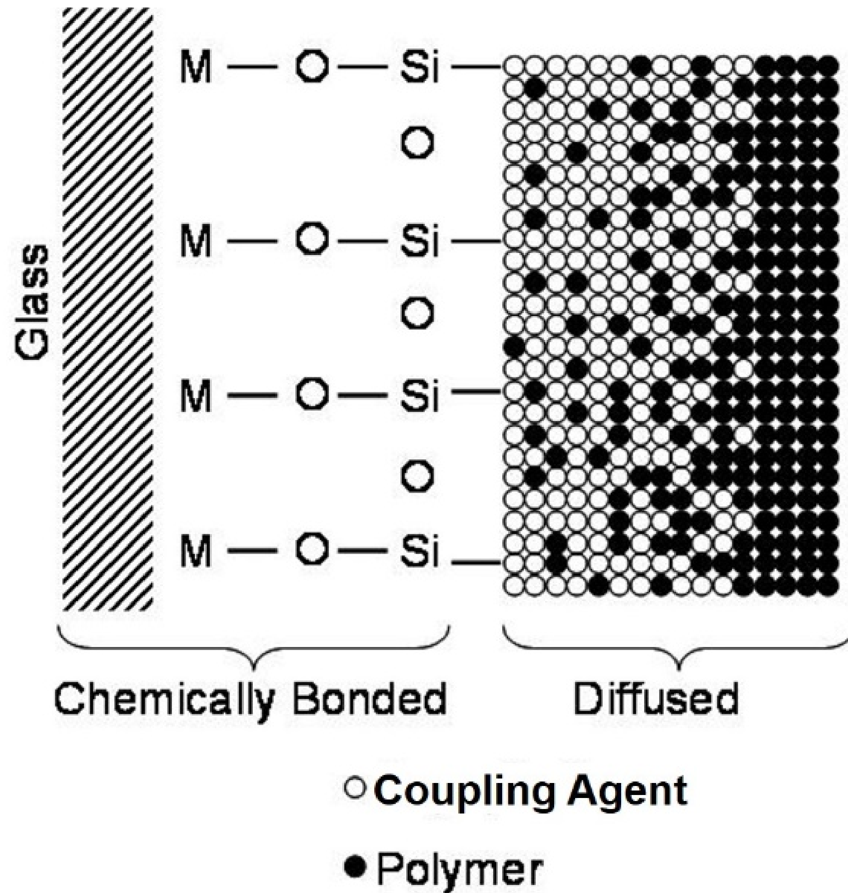


Figure 62 Schematic for conventional interdiffusion and IPN [54] [66] [67].

A single layer of silane may be sufficient to bond with the glass surface; however, to ensure uniform coverage, more than one layer of silane is usually applied by the glass manufacturers. This results in a tight siloxane polymeric network close to the inorganic surface that diffuses into subsequent overlays. The siloxane remains in high concentration at the glass/epoxy interphase and may be dissolved into the matrix during curing of the matrix resin, as shown in Figure 63. Coupling to the organic matrix is a complex phenomenon. The reactivity of a thermoset polymer is

matched to its reactivity with the silane. For example, an epoxysilane or aminosilane will bond to an epoxy resin; an aminosilane will bond to a phenolic resin; and a methacrylate silane will bond through styrene cross-linking to an unsaturated polyester resin. The large differences in composition and chemical characteristics of the individual components, such as antistats on the glass, lubricants, surfactants, and film formers, further complicate the formation of this interphase with different formulations. While the silane chemistry and its interactions with the glass surface and the polymer have been extensively studied, relatively little information is available about the influence of these sizing components on the formation of the interphase. The interphase is the region where stress transfer occurs between the two composite constituents, but its material properties and effective thickness are not well studied for FR-4 PCB laminates. Investigation of the mechanical properties of the interphase presents a challenge to probing into materials in extremely thin thicknesses.

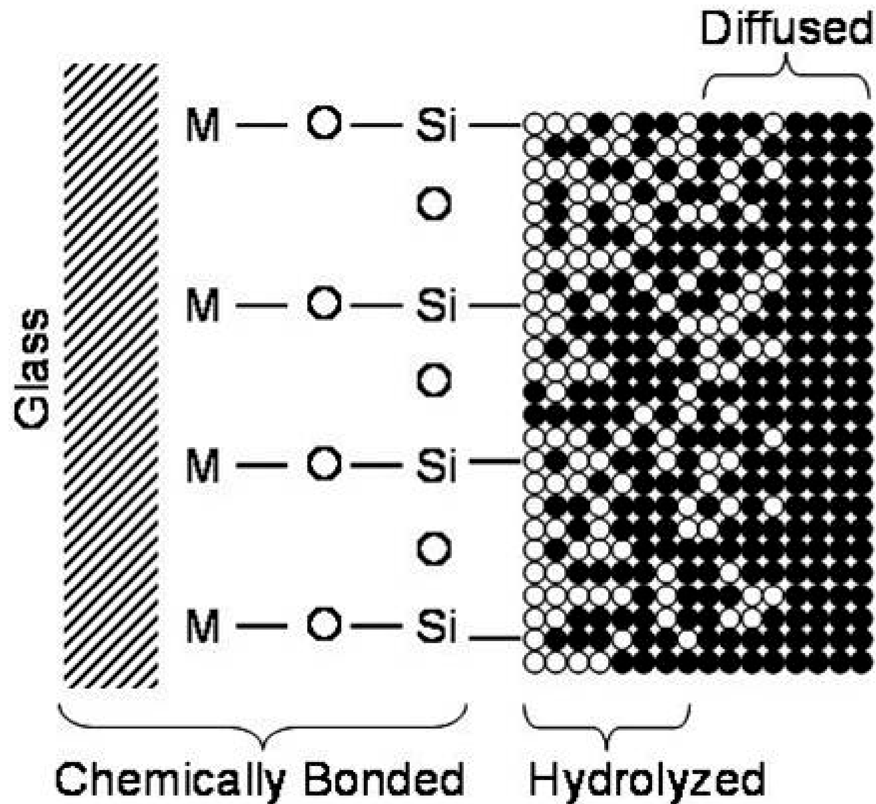


Figure 63 Schematic for hydrolyzed diffused interphase after aging in water in a silane-treated glass fiber [66][67].

The silicon atoms in the silanes are bonded to the silicon atoms in the glass through oxygen atoms, and the silicon atoms in the glass are bonded to each other. If the water produced in the forward reaction is continuously removed (e.g., by evaporation), then the bonding of silane to glass will continue until either there is no more silane or no more attachment sites on the glass surface. Conversely, if water is added to the silane bonded to glass, the reverse reaction can debond the silane from the glass. The rate of hydrolysis is influenced by the pH.

Instrumented indentation or atomic force microscopy testing is an appropriate method to characterize the degradation in the glass/resin interphase. Indentation is a technique for measuring the mechanical properties of materials and was developed from traditional hardness tests such as Brinell, Rockwell, Vickers, and Knoop. Instrumented indentation testing is similar to traditional hardness testing in that a hard indenter, usually a diamond, is pressed into contact with the test material. However, traditional hardness testing yields only one measure of deformation at one applied force, whereas during an instrumented indentation test, force and penetration are measured for the entire time that the indenter is in contact with the material. Nearly all of the advantages of instrumented indentation derive from this continuous measurement of force. Instrumented indentation is particularly well suited for testing small volumes of material such as thin films, particles, or other small features. Even for larger volumes of material that could be tested in a tensile configuration, instrumented indentation is often preferred for its speed and simplicity; sample preparation is relatively easy, and many tests can be performed on a single sample.

7.4.1 Halogen-free and Lead-free

Flame-retardant (FR) chemicals are added to PCBs during or after manufacture to inhibit or suppress combustion. FRs interfere with combustion at various stages of

the process, such as during heating, decomposition, ignition, or flame spread. One goal is to prevent the spread of fires or delay the time of flashover.

There are various kinds of FRs, such as halogenated, chlorinated, phosphorous-based, nitrogen-based, and inorganic. Different types of FRs are better suited for different applications. Their suitability depends on compatibility with the material to be flame-retarded, the fire safety standards with which the product must comply, reliability, and cost considerations. Halogens are the chemical elements fluorine, chlorine, bromine, iodine, and astatine. For plastic PCBs, brominated flame-retardants (BFRs) are the most effective flame retardant when both performance and cost are considered. BFRs have a unique chemical interaction with the combustion process because bromine is more effective than most of the alternatives, meaning that a much lower quantity of flame retardant achieves the highest fire resistance.

There are different types of BFRs [48], such as PBBs (polybrominated biphenyls), PBDEs (polybrominated diphenyl ethers), TBBPA (tetrabromobisphenol–A), and HBCD (hexabromocyclododecane). Each of these BFRs has very different properties.

Humans and the environment can be exposed to PBBs released during recycling of materials or after disposal in landfills. BFRs, and especially PBBs and PBDEs, are considered hazardous due to the formation of polybrominated dibenzodioxins and

furans (PBDD/F) during combustion of both the BFRs themselves and flame-retarded materials such as PCBs. Analyses of the principal halogen-containing component of printed circuit boards, TBBPA, have not shown that TBBPA is a source of human dioxin exposure [49]. According to an IPC white paper, the major driver for halogen-free flame substitutes for TBBPA in printed circuit boards is marketing, and there are no significant health concerns.

The main applications of lead in electrical and electronic equipment (EEE) include the solder joints of components mounted onto PCBs and board finishes [50]. Typically, reflow and wave soldering involve exposing the components and circuit boards to processing conditions sufficiently hot to melt the soldering alloys, which then form acceptable solder joints. The drive towards lead-free electronics has resulted in the use of lead-free solders in PCB assemblies. Common lead-free solder alloys such as Sn/Ag/Cu and Sn/Ag typically require a peak reflow temperature increase of approximately 40°C compared to traditional eutectic Sn/Pb reflow soldering conditions [50]. The temperature and process time required to flow the lead-free solders have posed a significant issue in tin-lead replacement. The melting point of tin-lead solder is 183°C, which typically corresponds to maximum reflow temperatures in the region of 220–230°C. The primary lead-free alloys have melting points in the 217–220°C range with corresponding processing temperatures of approximately 240–260°C. Such an increase in processing temperature raises

concerns for boards and components initially designed for tin-lead processing, but which now must withstand a 34°C heating differential.

A particular concern is the reaction of components and PCBs that may crack or delaminate due to trapped moisture or board warpage. Significant deformation of moisture-laden packages versus dry packages starts to increase at around 90°C. Increased rates of deformation occur beyond 138°C [51][52]

7.5 Path Formation – Summary

The two-step process of CAF includes the resin/glass fiber bond degradation and pathway formation, followed by an electrochemical reaction between the conductors. One method by which the pathway forms is due to breakage of the organosilane bonds at the glass/resin interphase. This breakage occurs by hydrolysis (adsorption of water at the glass fiber/epoxy resin interphase) or by repeated thermal cycling, which induces stresses at the interphase due to thermal expansion mismatches.

This section reviewed the organosilane-resin bonding process and summarizes the processing and environmental phenomena that can result in breakage of the bonds. The technique of using in-situ resistance measurements during destructive physical analysis to confirm one has reached CAF filaments during cross-sectioning is the first time this is described in the open literature. This solution addresses the potential problem in destructive physical analysis of grinding away the evidence of

the CAF filament and ultimately loosing evidence at the failure site. The nano-indentation test and analysis at the glass-resin interphase suggests that this interphase undergoes degradation due to environmental factors. As a result of the failure analysis and subsequent investigations, we recommend that systematic evaluation of mechanical properties at the glass/resin interphase be required at the OEM and PCB supplier level. The strength of the glass/resin interphase is influenced by physio-chemical stresses such as moisture and pH. By applying evaluation criteria, such as nano-indentation scratch tests, PCB material can be assessed for susceptibility to CAF and other failure causes in PCBs that are attributable to the glass/resin interfacial adhesion. OEMs can identify board suppliers based on answers to and validation of a series of questions. These questions focus on the necessary requirements of reliable board material manufacturing and are independent of the specifications of the product. The end deliverable is the identification of manufacturers who will provide reliable PCBs on a timely basis.

An upfront evaluation of PCB suppliers and manufacturers based on their ability to meet reliability requirements is critical for the PCB industry as most OEMs outsource board manufacturing capabilities. It is also needed because today's designs are much more complex and dense and call for a tighter process window during the PCB material and manufacturing processes. Furthermore, as noted in the section, an increasing number of electronic systems are failing due to problems

traced back to the PCB. Failure in the field leads to increased costs and decreased customer confidence.

7.6 Influence of Path Formation on CAF Time-to-Failure

Prior to formation of the filament, consistent with the published literature, a pathway connecting the oppositely biased conductors must be formed. It is hypothesized that path formation, which is proposed to be voltage independent, is the rate-limiting step in conductive anodic filament formation. In other words, it takes a much longer time for the pathway to be formed than for the metal migration and formation of the conductive anodic filament bridging and shorting the two conductors.

Hence, to deter failures due to the growth of conductive anodic filaments, it is necessary to control the rate limiting step (path formation) by characterizing the different path formation modes and mechanisms. Attempts to mitigate CAF failures include:

- Upfront assessment of the glass to resin interphase region
- Investigating into CAF resistant laminates by PCB laminate suppliers
- Use of moisture barriers to retard moisture ingress
- Use of non-woven fibers
- Use of staggered (non-inline) PTHs
- PTHs drilled at 45 degrees to the weave of the glass fabric.

Chapter 8: Conclusions

The two-step process of CAF includes the resin/glass fiber bond degradation and pathway formation, followed by an electrochemical reaction between the conductors. One method by which the pathway forms is due to breakage of the organosilane bonds at the glass/resin interphase. This breakage occurs by hydrolysis (adsorption of water at the glass fiber/epoxy resin interphase) or by repeated thermal cycling, which induces stresses at the interphase due to thermal expansion mismatches.

This research investigated the organosilane-resin interphase and summarizes the processing and environmental phenomena that can result in breakage of the bonds. The technique of using in-situ resistance measurements during destructive physical analysis to confirm one has reached CAF filaments during cross-sectioning is the first time this is described in the open literature. This solution addresses the potential problem in destructive physical analysis of grinding away the evidence of the CAF filament and ultimately loosing evidence at the failure site. The nano-indentation, AFM Force Spectroscopy and μFT-IR tests and analysis at the glass-resin interphase suggests that this interphase undergoes degradation due to environmental factors such as moisture absorption. As a result of the failure analysis and subsequent investigations, this research provides a recommendation that systematic evaluation of mechanical properties at the glass/resin interphase be

required at the original equipment manufacturers and at the circuit board laminate supplier level. The strength of the glass/resin interphase is influenced by physio-chemical stresses such as moisture and pH. By applying evaluation criteria, such as force spectroscopy and μFT-IR, PCB material can be assessed for susceptibility to CAF and other failure causes in PCBs that are attributable to the glass/resin interfacial adhesion. Electronics manufacturers can identify board suppliers based on answers to and validation of a series of questions. These questions focus on the necessary requirements of reliable board material manufacturing and are independent of the specifications of the product. The end deliverable is the identification of manufacturers who will provide reliable PCBs on a timely basis.

An upfront evaluation of PCB suppliers and manufacturers based on their ability to meet reliability requirements is critical for the PCB industry as most OEMs outsource board manufacturing capabilities. The evaluation is also needed because today's designs are much more complex and dense and call for a tighter process window during the PCB material and manufacturing processes. Furthermore, as noted in this research, an increasing number of electronic systems are failing due to problems traced back to the PCB. Failure in the field leads to increased costs and decreased customer confidence.

Chapter 9: Contributions

This research advances the understanding into CAF failures in printed circuit boards and their relationship to the degradation at the glass and resin interphase.

- Through the application of laboratory analytical techniques, tracked the evolution of glass/epoxy interphase with aging of the printed circuit board materials when subjected to different environments and aging mechanisms,
- Related mechanical changes at the glass interphase to chemical variations.
- Developed a basis for the rapid assessment tests for printed circuit board quality examination.
- Formed the basis to develop a Standard test method targeted to the testing of the glass-resin interphase using analytical techniques. The method will be applied without the need for fabrication of specialized test coupons, and failure criteria would be based upon comparison of interfacial performance using previously developed acceptance data.

Chapter 10: Future Work

10.1 Further Studies on Quantifying the Reduction in Modulus

For CAF, the isolation of the glass-resin interphase in "off-the-shelf" PCB materials is critical. A reduction in the modulus and the composition at the glass to resin interphase was measured using AFM force spectroscopy and μFT-IR experiments. It is shown that as the PCB samples absorb moisture, the interphase between the glass and resin becomes softer, which makes it more prone to separation. To further quantify the reduction in modulus and relate it to specific glass and epoxy types supplied by different manufacturers, analysis should be performed using PCB samples sourced from various laminate suppliers.

10.2 In-situ Humidity Exposures

The properties of PCB materials and their CAF susceptibility at as-received state and their evolution under humid service conditions are highly influenced by the interphase or interphase created between the resin matrix and the glass reinforcement. In-situ humidity exposure to PCB materials (along with AFM force spectroscopy) will help to track the evolution of the glass-resin interphase while hydrolysis acts to weaken this interphase. Changes in the mechanical properties, moisture diffusivity constants and stiffness reduction of glass/epoxy interphase as the PCB samples absorb moisture will be critical in tracking the degradation at this

interphase and for developing critical moisture content, control plans and guidelines.

10.3 Variations in Glass Transition Temperature of the Interphase

At the glass to resin interphase, it is shown that as the PCB samples absorb moisture, the interphase between the glass and resin becomes softer, however, this interphase may also have a glass transition temperature (Tg) much different than the bulk PCB Tg as reported by the PCB laminate suppliers.

Appendix A: Controlling Moisture in Printed Circuit Boards

(Adapted from *Sood, Bhanu, and Michael Pecht. "Controlling moisture in printed circuit boards." IPC Apex EXPO Proceedings (2010).*)

Introduction

Moisture can accelerate various failure mechanisms in printed circuit board assemblies. Moisture can be initially present in the epoxy glass prepreg, absorbed during the wet processes in printed circuit board manufacturing, or diffuse into the printed circuit board during storage. Moisture can reside in the resin, resin/glass interphases, and micro-cracks or voids due to defects. Higher reflow temperatures associated with lead-free processing increase the vapor pressure, which can lead to higher amounts of moisture uptake compared to eutectic tin-lead reflow processes. In addition to cohesive or adhesive failures within the printed circuit board that lead to cracking and delamination, moisture can also lead to the creation of low impedance paths due to metal migration, interfacial degradation resulting in conductive anodic filament formation, and changes in dimensional stability. Studies have shown that moisture can also reduce the glass-transition temperature and increase the dielectric constant, leading to a reduction in circuit switching speeds and an increase in propagation delay times. This section provides an overview of printed circuit board fabrication, followed by a brief discussion of moisture diffusion processes, governing models, and dependent variables. We then

present guidelines for printed circuit board handling and storage during various stages of production and fabrication so as to mitigate moisture-induced failures.

Effects of Moisture in PCBs

Moisture can reduce the quality of lamination, metallization, solder mask, and manufacturing steps associated with board fabrication and assembly. Moisture reduces the glass-transition temperature (T_g) so that excess thermal stresses can cause damage [86], [87]. Moisture also increases the dielectric constant, leading to a reduction in circuit switching speeds and an increase in propagation delay times [88], [89], [90]. Moisture ingress can also facilitate ionic corrosion, leading to both open and short circuits. Additionally, moisture that accumulates at the interphases of the resin and fiberglass can cause interfacial degradation, resulting in conductive anodic filament formation [91], [92], [93], [94], [95]. The common failure mechanisms attributed to moisture absorption in PCBs are listed below. Familiarity with these mechanisms is an essential input in selecting the most appropriate strategy for reducing moisture in PCBs:

- Entrapped moisture can cause blistering or inner layer delamination [17], [70].
- Excessive moisture increases dielectric constant (D_k) and dissipation factor (D_f), leading to changes in circuit switching speed [71].

- Since moisture acts as a plasticizer, it reduces the glass-transition temperature (T_g), which in turn increases stresses on PCB features such as plated through-holes [68], [69].
- Oxidation of copper surfaces leading to poor wettability of finishes and solder [77].
- Ionic corrosion causes electrical opens or shorts [77].
- Interfacial degradation can result in a reduced time to failure due to conductive anodic filament formation (CAF) [92], [93], [94], [95].

Mechanisms of Moisture Transport

Bulk diffusion within the epoxy matrix is the result of the motion of molecules along a concentration gradient (high concentration to low concentration). Surface topology and resin polarity are the primary aspects that affect the equilibrium moisture content [83]

The concept of capillary action is similar to wicking, but a distinction lies in that wicking is used to describe enhanced moisture absorption due to voids or cracks at the interphase, while capillary action is generally used to describe enhanced moisture absorption due to voids or cracks present inside the bulk. The sites for wicking and capillary action are present in the form of voids or cracks that may form by the addition of fillers.

For many polymeric resin systems, bulk diffusion is the dominant form of moisture transport. Bulk diffusion can be classified as Fickian [78], [79], [80], [81]. For Fickian diffusion in a plane sheet with thickness l exposed on both sides to the same environment (Figure 64), the moisture content, M_t, at time t, is given by equation 1.

$$\frac{M_t}{M_\infty} = 1 - \sum_{n=0}^{\infty} \frac{8}{(2n+1)^2 \pi^2} \exp\left(\frac{-D(2n+1)^2 \pi^2 t}{4l^2} \right) \tag{1}$$

where M_∞ is the equilibrium moisture content, and D is the diffusion coefficient, or diffusivity, given in $(\text{length})^2(\text{time})^{-1}$. By using this relationship, one assumes that diffusion is one-dimensional, i.e., diffusion through the laminates' edges is negligible, and the laminate surfaces instantaneously reach the equilibrium moisture content.

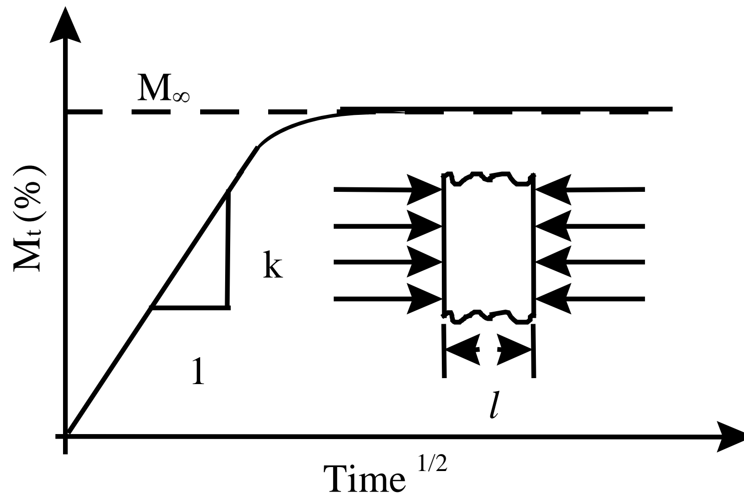


Figure 64: Fickian sorption by a plane sheet exposed on both sides to the same environment.

The initial stage of diffusion can be expressed by a reduced form of equation 1:

$$\frac{M_t}{M_\infty} = \frac{4}{l}\left(\frac{Dt}{\pi}\right)^{1/2} \tag{2}$$

By rearranging equation 2, the diffusion coefficient is:

$$D = \pi\left(\frac{kl}{4M_\infty}\right)^2 \tag{3}$$

where k is the slope of the initial linear portion in Figure 64.

Sorption tests were conducted [82] on seven different materials to determine the diffusion coefficient of each laminate. Two dry-baked coupons were used in each test at four environmental conditions: 50°C/50% RH, 50°C/85% RH, 85°C/50% RH, and 85°C/85% RH. The coupons were removed to assess their mass gain at increasing time intervals, i.e., the first interval lasted 15–20 minutes while the last one went up to a few days. The experiment ended once the gravimetric measurements indicated a constant mass within the scale's resolution.

Figure 65 shows typical diffusion curves for the CE-A laminates at 50°C/85% RH. Moisture content is plotted as a function of the square root of time to facilitate evaluation of the diffusion coefficient. The diffusion coefficients for thin and thick samples were calculated and averaged to form an average D (independent of thickness) for each environmental condition (Table 9).

The diffusion coefficients for each environmental condition along with the average percentage equilibrium moisture contents (independent of thickness) were introduced into equation 3 for thin and thick laminates to solve for the theoretical percentage moisture content, $M_t\%$, which was then superimposed onto the experimental data (Figure 65).

Table 9: Diffusion Coefficients (cm²/s)

Laminate	Average D ($\times 10^{-8}$)			
	@50ºC/ 50%RH	@50ºC/ 85%RH	@85ºC/ 50%RH	@85ºC/ 85%RH
FR-4 A	0.74	0.99	3.22	2.27
FR-4 B	0.82	1.23	2.74	0.93
HTFR-4 A	0.64	0.97	1.06	1.02
PI A	3.30	1.64	8.17	4.65
PI B	1.24	1.24	4.33	2.74
CE A	3.44	2.91	11.17	5.75
BT A	1.22	1.65	4.75	3.03

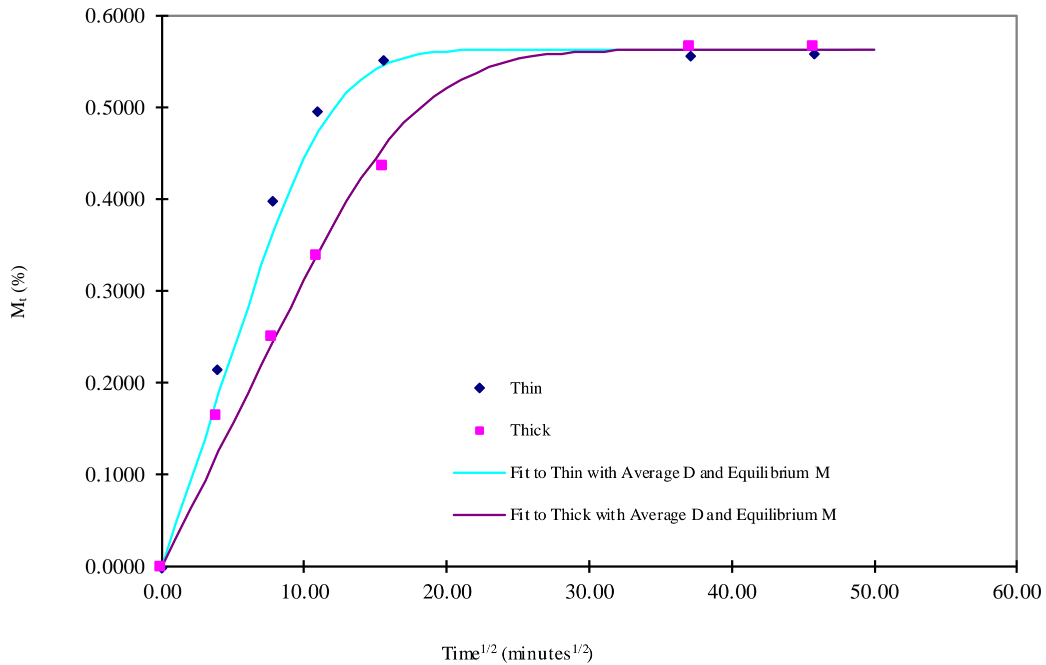


Figure 65: Diffusion curves with theoretical fit (CE-A laminates at 50ºC/85% RH).

Guidelines for Preventing Excessive Moisture Intake

Rigid PCBs can be categorized as single-sided, double-sided, or multilayer depending on the circuit complexity. Different process steps are required for each of these technologies, with single-sided having the simplest process and multilayer the most complex and costly process. Fabrication techniques and processes are common to the different technologies with special and more sophisticated steps required for complex multilayer boards. Many steps involved in the PCB fabrication are wet processes and some measures are required in order to remove residual moisture. Multi-layered laminate manufacturing is a process consisting of

encapsulating a ply (or several plies) of glass fabric within a polymeric resin. The fabric–resin combination provides dielectric as well as mechanical and thermo-mechanical properties. However, since the resins used in laminates are hydrophilic, the assembly can be susceptible to degradation and performance failure mechanisms driven by environmental moisture. Materials used in PCB manufacturing should be protected from stresses induced during fabrication, handling, or storage. Laminators, fabricators, and end users are responsible for the protection of PCBs from excessive moisture. Parties should ensure that effective process controls are implemented. The following section provides controls and guidelines on the treatment of PCBs and raw materials during various steps of the fabrication process.

Controls Implemented During Lamination

It should be noted that the PCB lamination process in itself is a dehydrating step. In this process, the prepregs and cores are stacked together and placed into a large press which bonds all the layers into the final laminate. During lamination, the heating rate, cure temperature and cure time are controlled. In many cases, a low temperature, vacuum (low pressure) step is introduced to minimize the occurrence of internal voids, which are a preferential site for moisture entrapment. During the lamination process, the prepregs should only be handled by the edges using clean latex or nitrile gloves to prevent damage and scratching, and to also prevent cross-

contamination of different epoxy resin types. It is also advisable to not reuse gloves to prevent cross-contamination. To prevent prolonged exposure to the remaining unused prepregs in a moisture barrier bag (MBB), the MBB housing the prepregs should be promptly resealed and should be stored flat (horizontally) in a in a cool, dry environment (such as a dry cabinet—typically at 23°C or lower and 50% RH or lower). MBB should have a water vapor transmission rate (WVTR) of less than or equal to 0.002/gm/100 in^2 (WVTR≤ 0.002/gm/100 in^2) in 24 hrs at 40°. Ensure an adequate seal width on the MBB.

Desiccant materials should be non-contaminating and dustless. During selection, the environmental conditions during shipping and storage should be factored in. Humidity indicator cards (HIC) should be non-corroding and should have an adequate number of divisions to resolve varying humidity levels. Once the prepregs have been removed from the MBB that was previously stored at low temperature, sufficient time should be provided for the prepreg to acclimate to ambient conditions prior to layup. The acclimatization should be conducted by keeping the prepreg in the MBB during the stabilization period to prevent moisture condensation. Bare, uncoated laminates also have higher moisture absorb rate as compared to a board covered with a solder mask. The number and duration of wash cycles also affects the moisture uptake. However, short duration wash cycles of laminates that are stored in controlled environment are not normally an issue if subsequent process steps are closely spaced in time.

It has been the practice with many PCB fabricators to bake prepregs prior to lamination. The theory behind the bake is to reduce excessive shrinkage during the lamination process and prevent formation of pockets for moisture to aggregate and cause blisters. The bake may be justified if the prepregs have been stored in uncontrolled environments for extended periods of time; however, in most cases, this bake step is unnecessary.

Controls Implemented During Inner Layer Production and After Lamination

PCBs typically experience higher moisture absorption rates after the photo imaging, etching, and drilling steps. Moisture may also get entrapped inside PCB features during the wet processes. However, steps such as solder mask bake and silkscreen cure are dehydrating and relieve the PCB of some entrapped moisture. Most solder masks require a cure in the range of 150°C to complete the soldermask. Silkscreen adds an additional bake step. Many fabricators rely on these additional bake steps to address incomplete cure in the lamination cycle.

During production, process flow should be designed in such a way that it minimizes the hold times between steps. Controlling storage conditions also helps in reducing moisture uptake. Once fabricated, PCBs should be placed in MBBs to ensure that no moisture is absorbed during transit. To ensure that the PCBs are sufficiently dry when they are received at the assembly location, adequate process control measures should be adopted to protect them from moisture uptake. This should also help in

preventing additional bake steps before assembly. Many PCB fabricators may bake the boards after the lamination step. This step is undertaken to complete the epoxy cure and eliminate any subsequent warpage resulting from uneven stress distributions. However, a properly run lamination cycle based on the guidelines of the PCB material manufacturer, accompanied by controlled cooling, should be able to produce warp-free and fully cured PCBs. This baking step may, in many cases, thermally degrade the PCB materials.

A few PCB fabricators bake after the drill step. This bake is primarily conducted in order to remove a phenomenon called "Pink Ring" [96], [97]. Pink ring is caused by a chemical attack on the inner layer surfaces that are exposed by cracks introduced at the drill step. It is believed that the bake step "relaxes" the epoxy enough to close the crack, but does not reseal the crack; thus this bake step is considered a cosmetic fix. Additionally, the bake hardens the epoxy smear and makes it difficult to remove in subsequent steps. A preferred solution to Pink Ring should be to use a good inner layer surface treatment that prevents cracking during drilling. Baking prior to hot air solder leveling is performed in order to remove residual moisture in PCBs and is another practice prevalent among many PCB fabricators. Again, if the solder mask cure step is performed as per manufacturer's specification and there is a minimum time delay between that step and HASL, the additional bake before hot air solder leveling is unnecessary.

Controls Implemented During PCB Assembly

After receipt of the PCBs at the assembly location, start by inspecting the condition of the MBB and humidity indicator cards (HIC). Check for tears or other damage to the MBB during transit. The HIC should always be read at room temperature (23 +/– 5°C) conditions. In a typical HIC, a pink dot indicates greater than 10% humidity. If the HIC indicates that exposure time or humidity limits have been exceeded, a bake may be necessary in order to ensure dryness prior to usage. Any non-conformance should be recorded and communicated to the board laminator. If possible, the PCBs should be placed in quarantine to prevent use. If the condition of the shipment is acceptable and the HIC indicator is acceptable and if the assembly is not scheduled immediately after receipt of the PCBs, the MBBs should be resealed promptly for PCB storage. Once PCB assembly has been scheduled, it is recommended to open the MBB just prior to assembly. Limit the "out-of-bag" exposure times during production.

As discussed earlier, the moisture absorption characteristics and sensitivity of any PCB will depend on the resin system used, design, construction, the type of assembly process, the number of steps in the assembly process, and many other factors. IPC-1601 [84] suggests that for most PCB designs, the maximum allowable moisture content will be between 0.1% to 0.5% of moisture weight to the total weight. The moisture content in a PCB may be determined by using the gravimetric

procedure described in IPC-TM-650, Method 2.6.28 [85]. If tests reveal that the moisture content exceeds the specified limits, both the PCB manufacturers and the assembly house should review the practices and identify areas for improvement. Regular audits of the warehouse, staging area, and production floor should be conducted to check for variations in parameters such as temperature, humidity, and handling controls. If the measured moisture content exceeds the limit, baking may be required. The baking step is required to remove the moisture that can be absorbed into the PCB due to the mechanisms discussed earlier.

Guidelines for Baking

Always set the baking oven temperature below the maximum operating temperature (MOT) and glass transition (Tg) temperature of the PCB material. However, the temperature should be always set above 100°C, which is the boiling point of water. The baking time should be selected on the basis of the measured moisture content, the desired content, and factors such as PCB complexity, overall thickness, and PCB finish. It is recommended that baking be performed in a forced air recirculating oven, but vacuum or nitrogen atmospheres are also effective. While placing the PCBs inside the baking oven, it is important to ensure proper venting and cleanliness of the oven and sufficient gaps between the PCBs for proper circulation. The PCBs should never be stacked inside the baking oven. The oven used for baking the PCBs should be dedicated for this purpose only and should not

be used for any other application. Potential cross-contamination and surface finish anomalies can occur if residues from other processes are deposited inside the oven and are consequently deposited on the PCBs.

Prior to establishing a baking profile, the laminate suppliers should be consulted in order to establish the baking limits. Additionally, the PCB fabricator and PCB finish supplier may have their own recommendations regarding temperature sensitivity of the PCB materials and surface finishes. The first step in establishing a bake profile is to test the moisture content of the PCB as described in IPC-TM-650, Method 2.6.28. It is recommended to first establish a baseline dry weight of the PCB by means of a bake. The sample can then be exposed to an elevated temperature and humidity environment, as described in section 0, in order to allow it to absorb known amounts of moisture. The moisture absorption rate measurement was also described earlier. Further, to determine the rate of moisture loss at a given bake temperature, the PCB sample should be placed in an oven and then taken out at periodic intervals for weight measurements. The duration at which the desired maximum allowable moisture content is reached should be recorded, and this bake time should be used for subsequent baking of PCBs with similar construction, geometry resin type, and PCB finish. Any time these PCB parameters are changed, the experiment should be repeated to establish a new baking profile and duration. Organizations can also create a library of such profiles and document the moisture uptake and release rates for specific PCB materials types.

Adverse Effects of Baking

It is possible to degrade the PCBs at certain bake temperatures that are below MOT and T_g. Degradation may also be caused by selecting a baking duration that is too long. Examples of degradation include damage to the board finish, solder mask, or laminate. IPC-1601 provides guidelines on baking and lists the adverse effects of baking, including the effects on individual PCB finishes. In addition to the potential for PCB degradation, baking also increases cost and cycle time.

Recommendations for Packaging, Shipment and Storage

After assembly, the test and inspection steps should be conducted in such a way as to reduce excessive moisture uptake. Steps such as radiological inspection (X-ray) may be conducted after the assemblies are packaged in appropriate packaging. Criteria for selection of appropriate packaging should include evaluation of moisture control during PCB fabrication process, complexity of the assembly, and the expected storage period prior to use. At a minimum, the packaging materials should fully protect the PCB during shipment and storage.

The use of a laminate witness coupon (LWC) [84] is also gaining popularity. LWCs can be used as indicators to evaluate the relative moisture absorption and condition of the PCBs and packaging materials during the various stages of the assembly process. The weight of the LWC should be measured and recorded prior to placing them in the MBB along with the PCBs. The LWC should always be placed on top

of the PCBs. Soon after receipt, the LWC should be evaluated for moisture uptake by weighing the coupon using an analytical balance, and the result compared to the initial recorded value. If the moisture uptake value exceeds the specified limits, the LWC should be baked until dry to validate the result. The user should also inform the PCB fabricator when the values exceed agreed-upon limits to determine the appropriate next steps.

Summary - Controlling Moisture in Printed Circuit Boards

Printed circuit boards have come a long way since the time when they existed mainly as a platform for connecting components. Boards are now part of the design, as features and even components are built into layers. The electrical and thermal properties of printed circuit boards are becoming critical factors in system designs. Many board developers do not realize that moisture in boards can significantly alter board performance. Moisture can negatively affect the integrity and reliability of printed circuit boards. The presence of moisture in a printed circuit board alters its quality, functionality, thermal performance, and thermo-mechanical properties, thereby affecting overall performance. Moisture content can vary widely depending on how boards are handled. Regardless of how much protection is used, some moisture will be absorbed. Parameters will be changed, even if boards are baked to dry them before they are used; this can alter performance from the specification sheet listings. This appendix summarizes moisture-related issues and provides

guidelines to reduce the impact of moisture on the reliability of printed circuitry boards. The controls and guidelines provided in the section can be implemented at different stages of PCB production.

Appendix B: Use of SQUID Microscopy for CAF Site Isolation

(Adapted from: ***Sood, Bhanu, and Michael Pecht. "Conductive filament formation in printed circuit boards: effects of reflow conditions and flame retardants." Journal of Materials Science: Materials in Electronics 22.10 (2011): 1602.*****)**

Introduction

Superconducting Quantum Interference Device (SQUID) microscopy is a technique used to map current flow, since current generates a magnetic field which is detectable by the SQUID sensor. A current of a few nanoamps is sufficient to be detectable. The scanning SQUID microscope transforms the magnetic fields into a current image using a Fast Fourier Transform back -evolution technique. The output is displayed as a false -color image of current density versus location on the sample, from which a short circuit or leakage current can be visually identified. The microscope is a sensitive near-field imaging system for the measurement of weak magnetic fields by moving a SQUID head across an area. The microscope can map out buried current-carrying wires by measuring the magnetic fields produced by the currents, or can be used to image fields produced by magnetic materials. By mapping out the current in an integrated circuit or a package, short circuits can be

localized and chip designs can be verified to see that current is flowing where expected. Scanning SQUID microscopy is a non -contact and non - destructive approach. A device can be tested at room temperature and atmospheric pressure, even though the sensor is cooled below 80K and in vacuum. A scanning SQUID microscope can achieve a spatial resolution of 20 µm, while magnetic shielding is not necessary because the SQUID can map out the background magnetic field.

Test Setup

A MAGMA -C10 scanning SQUID Microscope, was used to localize the CAF shorts in printed circuit boards. An image of the system is shown in

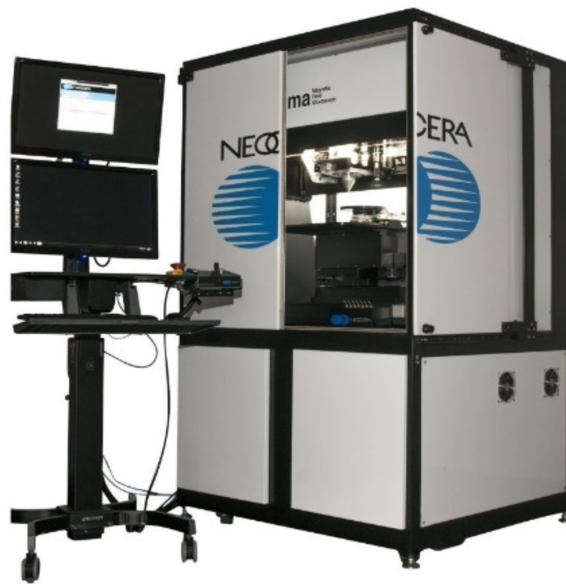


Figure 66 MAGMA -C10 scanning SQUID Microscope.

This is a DC SQUID, which has a measurement sensitivity to current of 600 nanoamps at a 100µm working distance (from SQUID sensor head to the surface of the PCB under test), with 30 ms averaging, without magnetic shielding.

shows the schematic of the test station of the scanning SQUID microscope system used in this study. A stage which can move in X, Y, Z axis and rotate about Z axis was used to hold the PCB under test. The SQUID sensor head, an optical camera, and needle probe were mounted on a track above the stage and the test specimen.

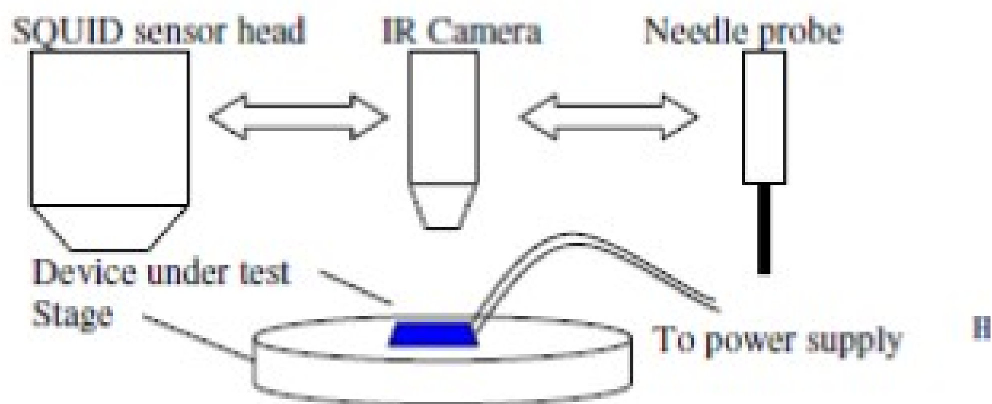


Figure 67 Schematic of scanning SQUID microscope test station.

The needle probe was used to define the target plane, which was a portion of top surface of the CAF containing PCB. With the needle probe engaged, the specimen was moved to detect the four corners of the target plane. The optical camera was used to take an external picture of the PCB. The SQUID sensor head

detects the magnetic field over the PCB under test when a current is passing through the test specimen. After the SQUID sensor head scans through the test zone, a magnetic fiel d mapping is generated . This magnetic field is then converted to a current density image as shown in .

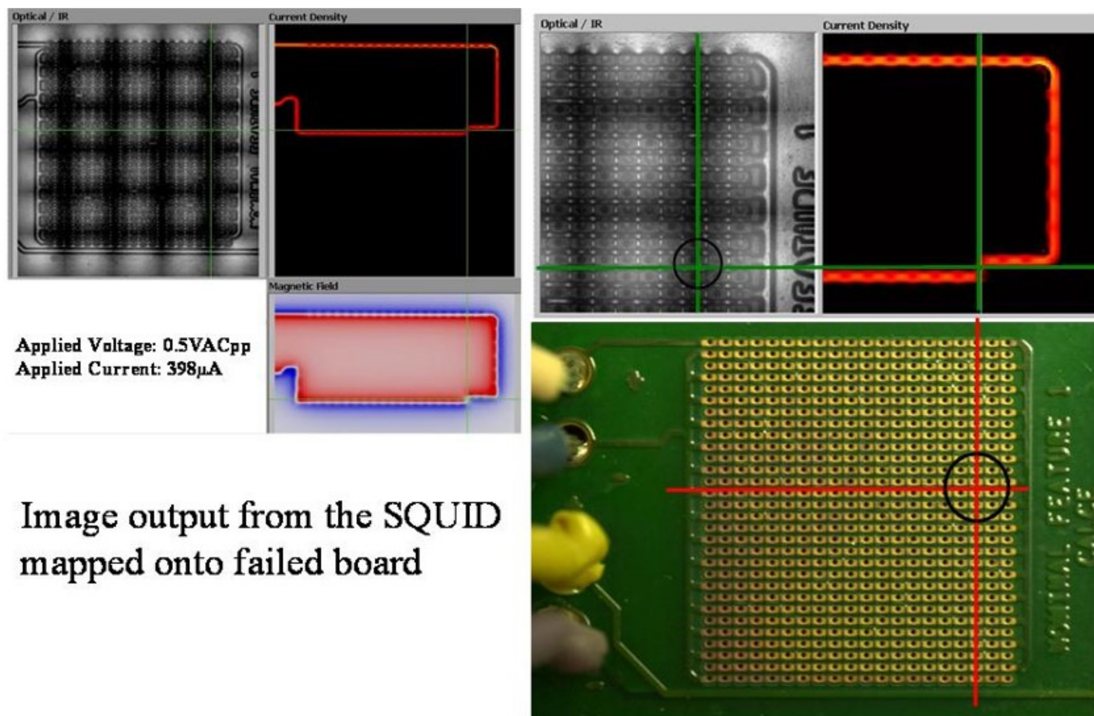


Figure 68 Overlaying the shorted site as predicted by the SQUID current mapping images, the respective conductor locations on the test boards were identified for cross-sectioning.

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