ABSTRACT

Title of Dissertation: MESOSCALE MICROSTRUCTURE EVOLUTION, RELIABILITY AND FAILURE ANALYSIS OF HIGH TEMPERATURE TRANSIENT LIQUID PHASE SINTERING JOINTS

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The continuous increase in application temperature of power electronic devices, due to the growing power density, miniaturization, and functionality in military and commercial applications, requires new packaging technologies with high temperature and reliability capabilities. Currently, the traditional maximum allowable temperature of power electronics (125°C) is a limiting factor for high temperature applications, such as space exploration, drilling, avionics, and electronic vehicles. Substitution of Silicon devices with wide bandgap (e.g., SiC) devices has extended the maximum allowable temperatures to 475℃. However, this created the need for robust high temperature packaging materials, especially interconnects and attachments. High temperature solders are often too expensive, too brittle, or environmentally toxic to be used, leading to increased study of low temperature joining techniques, such as solid phase sintering

and Transient Liquid Phase Sintering (TLPS), for producing high temperature stable attachments. TLPS is an emerging electronic interconnect technology enabling the formation of high temperature robust joints between metallic surfaces at low temperatures by the consumption of a transient, low temperature, liquid phase to form high temperature stable intermetallic compounds (IMCs).

The performance and durability of these materials strongly depend on their microstructure, which is determined by their processing. The complicated process of IMC formation through eutectic solidification and the extensive number of parameters affecting the final microstructure make it impractical to experimentally study the effect of each factor. In this work, phase field modeling of the microstructure of TLPS materials fabricated by different processing methods will be conducted. Phase-field modeling (PFM) is a powerful thermodynamic consistent method in mesoscale modeling that simulates the evolution of intermetallic compounds during the solidification process, providing insight into the final microstructure. Application of this method facilitates the optimization of influential processing factors. Efforts will also be conducted to identify failure modes and mechanisms experimentally under dynamic, power and thermal cycling loads as a function of critical microstructural features, facilitating the optimization of joining parameters to obtain higher durability TLPS interconnections.

The objective of this dissertation is to provide an insight into the processing of a reliable high temperature TLPS and facilitate their application in power electronic industries.

MESOSCALE MICROSTRUCTURE EVOLUTION, RELIABILITY AND FAILURE ANALYSIS OF HIGH TEMPERATURE TRANSIENT LIQUID PHASE SINTERING JOINTS

by

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Dedicated

To my wonderful family

Ata, Azar, Azita, Rozita, Reza

and the love of my life,

Mahshid

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Ali Moeini, Sep 2017

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Chapter 1 : High temperature interconnections

The maximum application temperature of power electronic packages is continuously growing due to the increase in their power density, miniaturization and functionality. This is motivated and driven by industrial and commercial applications, such as avionics, space exploration, drilling, and electric vehicles. The traditional application temperature of 125˚C [1], [2] for current power electronic devices is a barrier to progress of the aforementioned applications. Thus, new components and technologies with higher application and threshold temperatures are required to produce future generations of power electronics. In recent decades, the move from traditional silicon semiconductor devices with application temperature below 175˚C to wide bandgap (WBG) devices increased the limits on the semiconductor device to 475˚C [3], [4]. Similar trends are observed for other packaging components, such as substrates and interconnections. New types of power substrates made of AlN and Si_3N_4 are proposed to improve the reliability of power packages at high temperature applications [5]. The need for high temperature interconnection materials in power packages resulted in a sharp increase in application of high lead containing solders with melting temperatures above 186˚C. However, the search for an alternative is essential due to the expanding ban on the application of lead containing materials in electronics because of their hazardous effects on human health.

Currently, some regulations, such as the Restriction of Hazardous Substances (ROHS) 2002/95/EC, End of Life Vehicle (ELV), and Waste Electrical and Electronic Equipment (WEEE) 2002/96/EC restrict the use of lead containing materials in electronic applications aimed at eventually prohibiting their use completely [6]. Power

electronics which use high lead solders are currently exempted due to the lack of a reliable non-hazardous replacement. Different alternatives, such as lead-free tin/gold based solders and sintering based interconnections, were proposed to replace the lead containing solders and deliver a similar performance. A review of the state of the art high temperature interconnection technologies and materials proposed as alternative replacement is provided in the following sections to introduce their potentials and defects for power electronic applications. The rest of this dissertation is focused on developing, processing, screening, and qualifying TLPS for high temperature applications.

Lead-free solders

High operating temperature is the first factor in the selection of a material for high temperature applications. Eutectic tin-lead alloy as the predominant solder material in classical electronic devices has a melting temperature of 183˚C. This melting temperature can increase to higher values by increasing the fraction of lead in the solder composition, to even 312˚C, for extreme temperature application [7]. High melting temperature for a solder has a twofold effect: first, it increases the allowable operating temperature of the package; second, it improves the mechanical properties of the interconnection by decreasing the homologous temperature, T_h (the ratio of operating temperature over the melting temperature, both expressed in Kelvin). Higher values of this ratio result in poor mechanical properties, such as creep resistance of the solder during performance. For high temperature applications, homologous temperatures lesser than 0.67 are favorable; however, values around 0.85 are not uncommon. Contrary to favorable effects of high melting temperature is the increase in process

temperature. It may damage the other packaging components or result in higher residual stresses due to large temperature differences. Generally, die-attach materials with a processing temperature lower than 300˚C are more favorable.

The above factors are considered as parts of the broad category of attach manufacturability. Furthermore, performance/reliability issues are the other essential factors in the selection of interconnection materials. Table 1 shows the properties related to manufacturing and reliability/performance of the solder alloys. Material composition is a major element in defining these properties. The base materials for most of the lead-free solders are Sn, Au, or Bi. Other alloying components are In, Zn, Ag, Sb, Cu, and Mg. Properties of some of the solders made of these materials are presented in the following sections.

Table 1 Properties relevant to manufacturing and reliability/performance of the solder materials [8]

Manufacturing	Reliability and performance
Melting/liquidus temperature	Electrical conductivity
Wettability (of copper)	Thermal conductivity
Cost	Coefficient of thermal expansion
Environmental friendliness	Shear properties
Availability and number of suppliers	Tensile properties
Manufacturability using current processes	Creep resistance
Ability to be made into balls	Fatigue properties
Copper pick-up rate	Corrosion and oxidation resistance
Recyclability	Intermetallic compound formation
Ability to be made into paste	

Sn-based alloys

Tin is the base material for a relatively large number of lead-free interconnections. A combination of different properties makes tin an attractive candidate for high temperature applications. The melting temperature of tin is 231˚C which is above the

current maximum allowable temperature of power electronic devices and low enough to facilitate the manufacturing process. The ability of tin in wetting different substrates is another advantageous parameter in its application for joint technologies. However, the disadvantageous factors, such as tin pest and tin whiskers, should be considered in application of Sn-based alloys.

Tin pest occurs when a tin crystal structure transforms from one thermodynamically stable condition (β-phase) to the other (α-phase) with respect to temperature change. Tin has two different crystal structures in the solid state: white tin (β-phase) which has a body-centered tetragonal (BCT) structure and gray tin (α-phase) which has a diamond cubic crystal structure. The BCT structure is stable at room temperature while the other is thermodynamically stable below 13˚C. Therefore, when the temperature falls below the transition temperature the β-phase transforms to lower density α-phase. This results in large increases in the volume which can result in cracking the structure [8]. The addition of alloy agents showed an effective influence in preventing this phase transformation and its undesirable consequences.

Another limitation is the possibility of whisker growth in the high content tin compositions. Single crystal whiskers can grow, similar to fine wires, up to 0.64 mm high (more rapidly ~51˚C). Whiskers do not deteriorate tin solderability. However, they can cause electrical shorts in circuits. Lead has a substantial effect in suppressing tin whisker growth [9]. Here some of the common Sn-based lead-free solders are introduced and their properties discussed.

Sn-Ag

The phase diagram for the Sn-Ag system has a eutectic point of 221˚C at Sn3.5Ag composition, Figure 1-1. This temperature is in appropriate range for the manufacturing purposes of high temperature packages; however, it does not increase the maximum allowable and homologous temperatures significantly. The microstructure of joints prepared from eutectic solidification of Sn3.5Ag is described as dispersed Ag_3Sn percipitates within β-phase tin matrix [10]. Addition of 1% Zn improves the microstructure by introduction of a finer two phase distribution throughout the joint [11]. This alloy may be prone to whisker growth due to its high tin content.

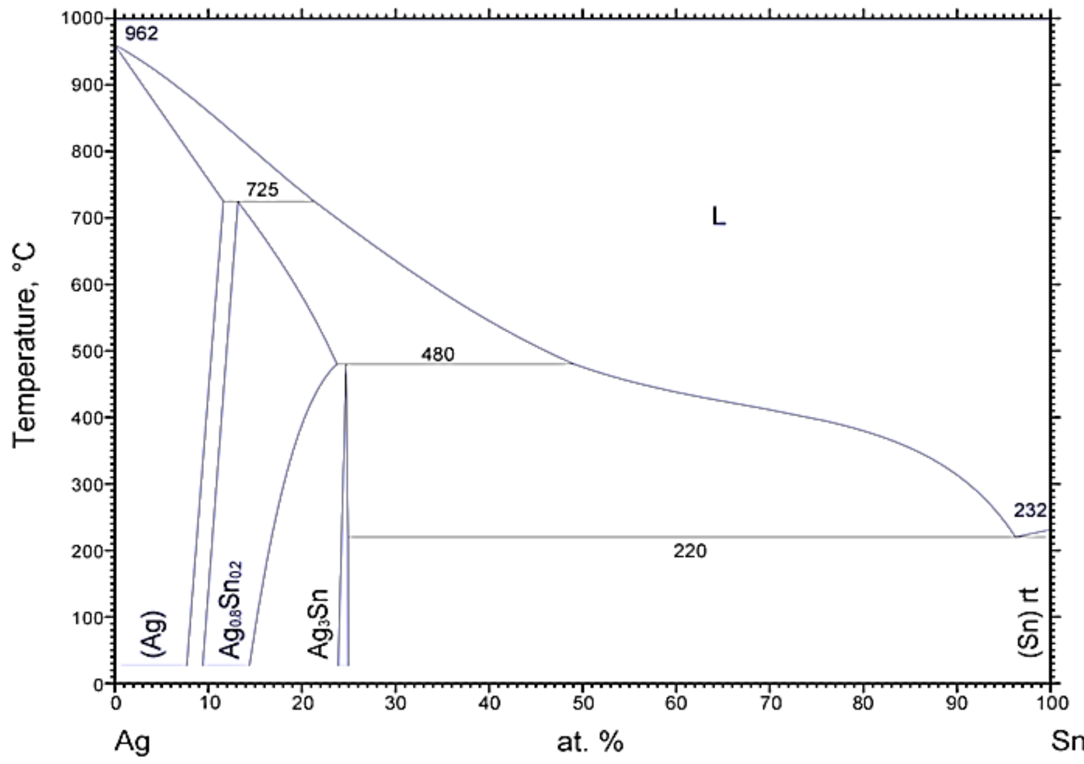

Figure 1-1: Ag-Sn phase diagram [12]

Sn-Ag-Cu

The Sn-Ag-Cu (SAC) alloys are the most widely accepted type of lead-free solders. Near eutectic SAC alloy (with 3-4% Ag and 0.5-1.0% Cu) is the most popular type of these alloys, Figure 1-2. Its melting point is 217˚C which is close to binary Sn3.5Ag alloy. The addition of Cu improved the wettability and reduced the melting point of near eutectic alloy [13]. The microstructure properties of SAC alloys are affected by the formation of IMC between three constituents. The possible IMC compositions are: Ag_3Sn, Cu_6Sn_5, and Cu_3Sn. The reaction between Ag and Cu only results in Ag-rich α-phase and Cu-rich β-phase and without formation of any IMCs [14]. The fine IMCs can strengthen the alloy and improve the fatigue life of the solders. Fatigue life of 3-4 times higher than Pb-Sn eutectic solders are reported for SAC solders [15].

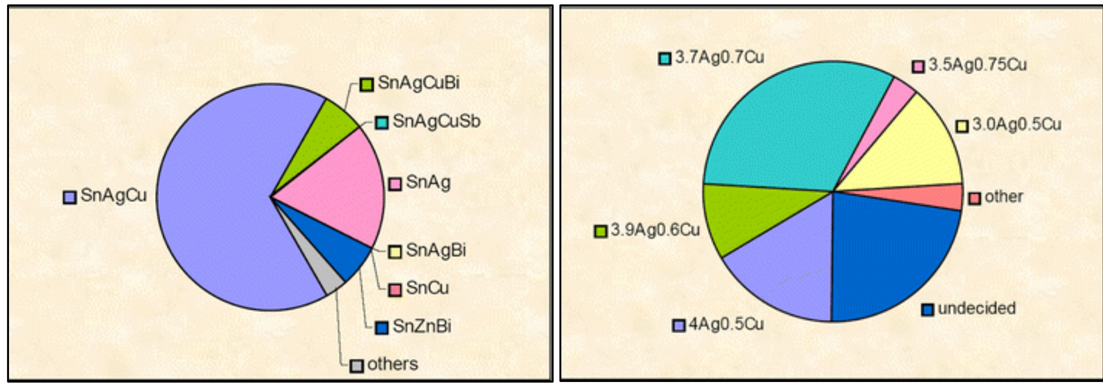

Figure 1-2: Left) The market share of different lead-free solders; Right) Survey of the market share of different types of SAC alloys [16]

The low melting temperature of some of the other Sn-based alloys, such as Sn-Bi (139˚C) and Sn-In (117˚C), makes them incompatible for high temperature applications. Therefore, they are not considered in this section.

Au based alloys

Au-Sn

There are several binary eutectic points in the Au-Sn phase diagram, Figure 1-3. Different types of stable IMCs form during the soldering process. The Au-rich solder (Au20wt%Sn) has a eutectic temperature of 280˚C which is compatible for high temperature processing requirements. Also, the fluxless bonding process in addition to high fatigue and creep resistance makes this solder a superior choice for electronic and optoelectronic packages [17]. There are two application limitations: first, high cost of gold; second, the transformation in IMCs phases near 190˚C which can induce cracks and decrease joint reliability [18]. Au-rich solders are considered as hard solders due to the existence of the brittle Au_5Sn IMCs [5].

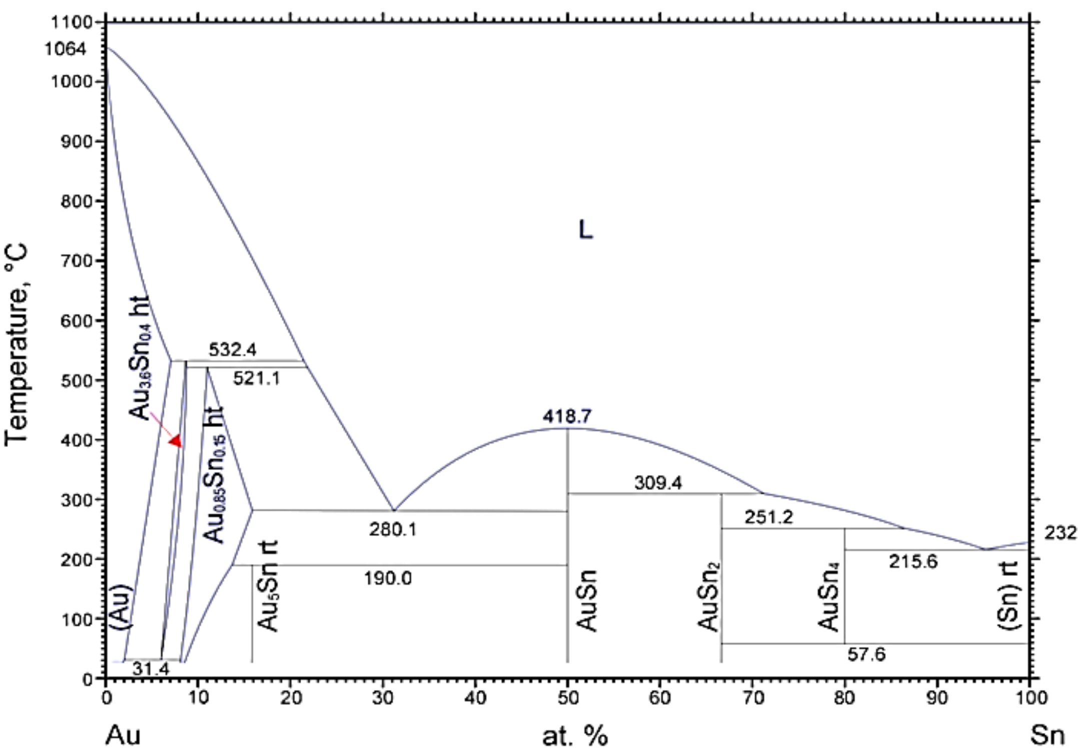

Figure 1-3: Au-Sn phase diagram [12]

Off-eutectic Au-Sn

The off-eutectic Au-Sn alloy has a high melting temperature of 400˚C and shows excellent performance at high temperature, corrosion resistance, and high electrical and thermal conductivities. Also, the fluxless bonding process makes it an excellent choice for optoelectronic, biomedical and micro-electro-mechanical systems (MEMS) applications. On the other hand, the processing temperature for this type of interconnection is very high and requires specific considerations during manufacturing [19].

Au-Ge

Au-Ge similar to the Pb-Sn system has no IMC phases. The eutectic (Au28at%Ge) melting temperature of 360˚C and decent ductility makes this material an excellent die-attach material for very high temperature applications. The high ductility solder material makes it an excellent choice for die-attach applications due to its great ability to relax under high thermomechanical stresses. The addition of Sb to this solder decreases the melting temperature and increases the ductility considerably which makes it more appropriate for manufacturing processes [17]. Like all other Au-based solders, the high cost of raw materials is a huge hindrance in its widespread industrial applications.

Zn-based alloys

Zn-Al

Zn6wt%Al has a eutectic melting point of 381˚C. The eutectic solidification does not create any IMCs throughout the microstructure. The advantage of using Zn-Al eutectic alloy is the low cost of raw material. In contrast, the corrosive behavior of Zn and poor

wettability of Al and Zn, due to their high oxygen affinity, are the drawbacks of using Zn-Al alloys. Also, this alloy is considered as a hard alloy compared to high lead solders [5].

Zn-Sn

Different alloys of Zn-Sn were proposed as high temperature solders (Zn20wt%Sn, Zn30wt%Sn, and Zn40wt%Sn). They have several desirable properties, such as: decent melting temperature (199˚C), no IMCs at the equilibrium state, good ductility, excellent electrical properties, superior thermal conductivity (100-106 W/m-K) and oxidation resistance [20], [21]. On Cu substrates, the Zn forms $CuZn_5$ and Cu_5Zn_8 IMCs with Cu. This results in increased hardness of Zn-Sn alloy which provides higher strength at high temperatures. The main drawback of this alloy, like Zn-Al, is its low corrosion resistance.

Bi-based

Bismuth has a melting temperature of 270˚C which makes it a potential candidate for high temperature applications. Meanwhile, the brittle nature of its microstructure, and its poor bonding strength makes it less attractive for high reliability applications. Alloying bismuth with other elements, such as Ag, Al, Mn, and Cu is considered to improve its performance. Here, Bi-Ag and Bi-Cu-Al-Mn systems are considered and discussed to elaborate their advantages and defects for high temperature power electronic applications.

Bi-Ag

The favorable eutectic melting temperature (shown in Figure 1-4) and good workability of the Bi2.6Ag alloy makes it a decent candidate for high temperature applications.

However, its poor thermal conductivity and wetting behavior on Cu substrates are shortcomings of this material [22]. Bi-(11-12)Ag is another system considered to improve some of the shortcomings of Bi-2.6Ag. The higher amount of silver slightly improves the thermal conductivity, seen in Table 2, and the electrical resistance considerably decreases from 116.5 $\mu\Omega.cm$ for Bi-2.5Ag to 86.5 $\mu\Omega.cm$ for Bi-11Ag [23]. Also, the higher content of silver makes strain localization and crack growth harder in the Bi-11Ag systems [24]. Development of this solder system is still in progress to improve the inferior workability, thermal conductivity, and electrical conductivity. Currently, the addition of rare earth metals is considered as a method to improve the wettability and shear strength of the solders [25].

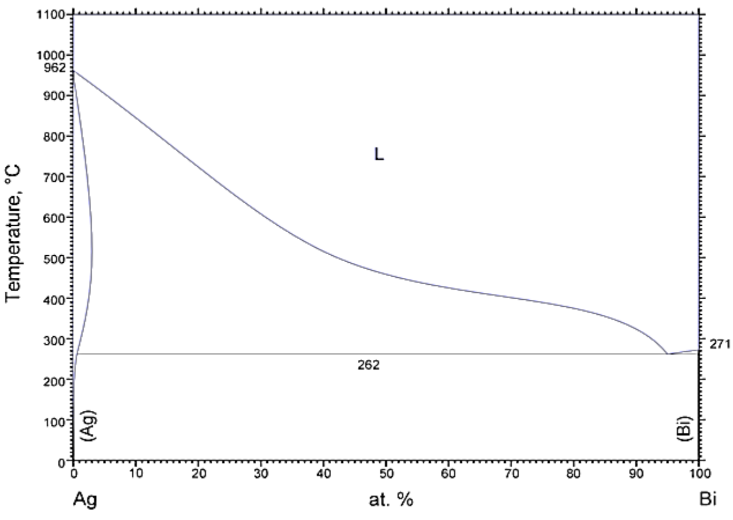

Figure 1-4: Silver-bismuth phase diagram [12]

Table 2: Thermal conductivity of solder systems [22]

Alloy	Thermal conductivity (W/m-K)
Sn-25Ag-10Sb	55
Bi-2.6Ag	7
Bi-12Ag	11
Pb-2Sn-2.5Ag	53

Up to this point some of the high temperature lead-free solders which can be used as die-attach interconnections in power electronic packages were introduced. In the following sections, some of the materials and interconnection technologies specifically designed as die-attach materials will be discussed.

Epoxy adhesives

Epoxy adhesives is the general term for die-attach materials prepared by the suspension of metal particles or flakes in an epoxy carrier. The metal content provides electrical and thermal paths in the component while the epoxy matrix creates a strong bonding between the components. There are two challenges in the application of adhesive components: first, the maximum allowable temperature with respect to melting temperature of the conductive adhesive; and second, poor thermal and electrical conductivity due to poor connections between metal particles or flakes. Thermal and mechanical properties of some commercial epoxy adhesives are listed in Table 3.

Silver filled adhesives are high temperature die-attach materials with a decent ability to lower stress concentrations on the die. The main concern in the application of these types of adhesives is the dispersion of silver fillers in the epoxy and inability of the die-attach to provide appropriate thermal and electrical paths for the high temperature applications [25]. Also, the reliability issues, such as die-attach delamination and "popcorn" cracking, become more serious with increasing chip sizes [26]. The popcorn cracking occurs when the moisture absorbed in the polymer evaporates during the surface mounting process and cracks the plastic package or the semiconductor die. Efforts are underway to improve the polymers used in the manufacturing of epoxy

adhesives to assure high performance and reliability during high temperature applications.

Table 3: Thermal and mechanical properties of selected die-attach materials [27]

Material	$T_{m\,(^{\circ}C)}$	$T_{max\,(^{\circ}C)}$	K (W/m K)	CTE (10-6/˚C)	G (GPa)
P-1011[1]	-	350	1.29	37	-
H20E-HC[1]	-	300	3.5	26	-
H20E-HC[1]	-	200	9.96	53	-
QMI-3555R[2]	~400	300	80	16	11.5
FO-3, FO-13[3]	450	300	~60	25	-
Tap 3M[4]	-	250	-	-	0.1

Sintering technologies

The sintering process is densification and growth of the initial grains by application of thermal energy. The driving force for this process is reduction of interfacial energies [28]. Different classifications based on the state of the constituents or process parameters can be considered for categorizing the sintering processes, such as pressureless and pressure-assisted processes or solid-state sintering and liquid phase sintering. The latter is the most common type for dividing sintering processes and indicates the state of the constituent during the sintering process.

In solid-state sintering, all the components are in solid state. This method is mostly used in power metallurgy in which the metal particles/flakes are mixed and processed under temperature and pressure. In solid-state sintering, the process temperature is lower than the melting temperature of all the paste constituents.

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[1] Adhesive made by Epoxy Technology
[2] Silver filled glass made by Loctite
[3] Silver filled glass made by ITME, Poland.
[4] Thermally conductive tape made by 3M

In liquid phase sintering, at least one of the components melts during the sintering. The processing temperature for liquid phase sintering is above the melting temperature of at least one of the paste ingredients. There are different types of liquid sintering, such as viscous flow sintering and transient liquid phase sintering. The viscous flow sintering occurs when the volume of the liquid phase is large enough to completely mix with solid particles. During this process, the shape of the grains does not change. In the transient liquid phase sintering process, the liquid phase only exists in the early stages of sintering and the sintering completes by solid-state sintering [28].

The low process temperature of sintering technology in contrast with the high application temperature makes them a potential candidate for high temperature applications. For example, the solid-state sintered silver joints can be processed at low temperatures near or less than 300˚C and they are stable up to 960˚C, which is the melting temperature of silver. Different aspects of utilization of sintering technologies in power electronic applications and the important parameters in their preparation, such as binder, and particle sizes, in addition to process parameters, such as temperature and pressure are discussed in the following chapters.

Research gap and problem statement

There is a growing demand for power electronics with higher application temperature due to continuous increase in power density, functionality, and miniaturization. This has inspired more advanced and new packaging technologies. Additionally, the expanding ban on application of lead-containing solders, as the conventional high-temperature power electronics die-attach material, necessitates a new nonhazardous alternative.

In this chapter, the current state of the art interconnection materials and their processing conditions have been introduced. The options can be classified into three broad categories: lead-free solders, epoxy adhesives, and sintered joints. The first group can be used either as solder or die-attach material; however, the other two are specifically designed for die-attach applications. The advantages of different options from processing, and mechanical, electrical, and thermal features, in addition to their shortcomings, which prevented them from completely replacing lead-containing solders were discussed.

One of the introduced technologies with considerable potential for industrial applications is sintering. Sintering provides the feasibility of processing high melting temperature materials at alternatively low processing temperature[1]. Also, it is possible to use different types of sintering methods based on the processing requirement. Sintering can be done fully in solid-state or solid-liquid interaction. Also, it is possible to have only a single material or a combination of different materials. These features provide great controllability over processing and final properties; however, the inadequate reliability information, complicated processing procedure, and poor modeling approaches limit their potential. The main goal of this dissertation is to provide improvement in processing, modeling, and reliability testing of TLPS joints through experimental, analytical, and simulation approaches. Therefore, the following objectives were considered:

1) Creating a simple and repeatable TLPS processing approach which does not require specific operator training or any specific environment

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[1] The processing temperature is considerably lower than melting temperature of sintered interconnection

2) Creating an accurate joint screening and composition monitoring approaches to evaluate the quality of processed interconnections
3) Increasing the application of TLPS joints to large size areas
4) Introducing a new phase field modeling method to simulate microstructure evolution during TLPS processes
5) Comparing different processing methods by phase filed modeling (PFM) simulation to find the one with better potential for industrial applications
6) Evaluating performance of TLPS joints under dynamic loads (drop-shock) and compare with competition
7) Evaluating performance of TLPS joints under power and thermal cycling loads and compare with other interconnection technologies
8) Introducing an innovative and novel approach to improve conventional TLPS interconnections

Based on these objectives the following outline is considered for this dissertation:

Outline

In Chapter 2, different aspects of solid-state and liquid-state sintering from the fabrication and processing point of view are introduced and analyzed. The effects of different factors in paste preparation, such as paste ingredients, and processing factors, like temperature and sintering environment, are evaluated. Then, common processing methods used in the literature are introduced and their shortcomings in becoming an industrial prevalent method are discussed. Finally, a new one-step TLPS processing method is introduced. The one-step TLPS processing procedure does not require extensive operator training or special sintering environment or chamber and creates high quality joints. Furthermore, unlike conventional methods, it can create low voiding large area joints. Additionally, tertiary elements can be integrated in the joint without any change in processing.

Chapter 3 introduces common solutions to solid-liquid interaction problems. Two methods of sharp-interface problem and PFM are introduced. PFM has great potential for application, such as eutectic solidification and TLPS. The fundamentals of this method are presented and a new approach is introduced by the author to improve its application to TLPS modeling. Finally, copper-tin joints which are processed with two-step and one-step processing methods are modeled with PFM and the microstructure evolution results are presented. This provides significant insight in process completion and selection of appropriate processing methods.

Chapter 4 includes screening and reliability testing methods specifically designed for die-attach interconnections. First, a joint quality screening method using image processing is introduced and later, this is extended to application of machine-learning methods to accurately define joint material composition. Then, different reliability tests, such drop-shock, and power and thermal cycling are considered for evaluating the performance of TLPS interconnections. For each test, a specific procedure is designed and applied. The samples are cross-sectioned and examined at the end of the process to define failure mechanism and its root cause.

Chapter 5 introduces a novel TLPS interconnection method and material involving copper and tin micro-particles embedded in wood carbon channels. This provides a high-conductivity material with comparable mechanical properties to common TLPS joints. The processing method is explained comprehensively and the mechanical integrity is tested by shear strength test at room and high temperature.

Finally, Chapter 6 summarizes the contributions and findings of this dissertation. Also, potential future works to further improve the current state of the art based on the results of this dissertation are discussed.

Chapter 2 : Sintered joints, fundamentals, processing and development

Introduction

The advent of wide band-gap devices (GaN, SiC) has made high operating temperatures more achievable in power electronic components. This creates the opportunity to have higher power densities, better functionality and miniaturization. However, this demands compatible packaging components which work efficiently under the new conditions. In the case of interconnections, the expanding ban on the application of high-lead solders, which are the conventional high-temperature interconnection in power electronic applications, have increased the priority of finding a reliable and environmentally friendly high temperature interconnects.

In the previous chapter, the current state-of-the-art alternatives for high-lead solders were introduced. The options were categorized into three classes of lead-free solders, epoxy adhesives and sintering technologies [29], [30]. These are still in the development and qualification research phases to potentially fully substitute high-lead solders and even grow the application limits beyond current power electronics. In this chapter, the focus will be on sintering technologies. First, the two major types of sintering, solid-state and liquid-solid inter-diffusion sintering will be introduced and then, the paste constituents, processing factors, and their effect on the joint quality will be discussed.

Finally, a novel method of processing will be introduced to fabricate high quality transient liquid phased sintered joints. The method is designed based on two factors:

simplicity and repeatability. A major issue with most sintering systems is the complicated processing which requires detailed attention to many factors. A minor change in one of these factors results in an unacceptable decrease in the quality of joint microstructure. This generally depicts an increase in pore content of the joint or high amount of reactants in the final products. The main objective is to design a simple processing, like solders that creates repeatable results. Also, this method provides the potential to involve a more diverse range of reactants or passive elements.

Solid-state Sintering

Reduction in interfacial energy is the main driving force behind a sintering process [28]. Solid particles, generally from one phase, start forming solid bonds when heated. The sintering temperature is below the melting point of the reactant material. The final product will have a melting temperature equal to the reactant. For the case of silver sintering, the melting temperature is 960℃ while the sintering temperature is ~300℃. The process includes two simultaneous steps of densification and coarsening as shown in Figure 2-1. Densification is the process of increasing joint density by reducing the pores. Coarsening or grain growth is the process of increasing average grain size by boundary motion or Oswald ripening. Smaller size particles and application of pressure during processing expedites these processes and decreases the required heat. Most of the sintering studies were performed on ceramic, but in recent decades silver (and copper) sintering became of interest for interconnection applications.

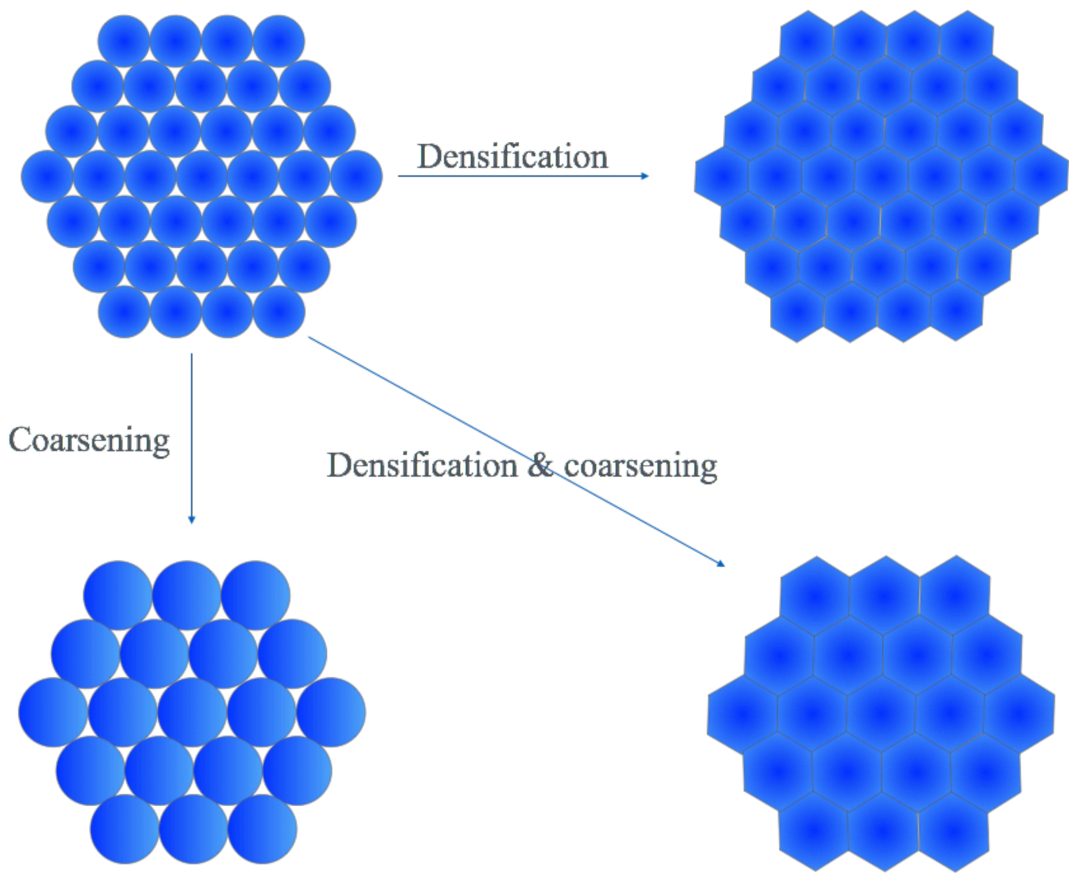


Figure 2-1: Solid-state sintering stages

Silver solid-state sintering methods developed a long time ago, but due to the advent of nanoparticles they became more and more of interest for electronic applications. In the following sections the evolution of solid-state sintering and its application in electronics packaging is analyzed. Many concepts, such as paste preparation, and effective factors can be easily applied to solid-liquid sintering.

Microscale Silver Sintering

In the late 1980s, a die-bonding technique based on solid diffusion of metals was introduced for fabrication of power electronic components [31]. This method was initially termed the Low Temperature Joining Technology (LTJT). In this method, microscale metal (silver) flakes are sintered under uniaxial or hydrostatic pressure at

temperature levels generally lower than 300˚C. The application of this method in attachment of Molybdenum disks to silicon wafers was first introduced by Schwarzbauer and Kuhnert [32], [33] as a four-step process. First, the joining paste was prepared through the dispersal of silver flakes (20-30 um) in an organic binder. Second, the produced paste was screen or stencil printed on the molybdenum disk surface. Third, the paste was dried in open air at 250˚C. Lastly, the silicon wafer was mounted on the dried paste and sintered under 10-40MPa at 200-250˚C until bonding had occurred. The fabricated joints showed acceptable mechanical stability and shear strength up to 100 MPa. It is demonstrated that thermomechanical stresses between the molybdenum disk and the Silicon wafer could be avoided by controlling the process temperature. This minimizes the bowing in the final product [34].

Successful application of silver flakes in the fabrication of power components inspired the utilization of LTJT in the attachment of power electronic devices. Various advantages were mentioned in the literature [35] for sintered joints in power electronic applications, such as:

1. Acceptable wetting
2. Movement control of chips (no swimming)
3. High thermal-conductivity
4. High reliability
5. Low microscopic void content

Properties of microscale sintered joints were evaluated and compared with $Sn63Pb37$ from thermal, mechanical, and electrical aspects. The results showed promising properties and potential for industrial applications [36]. In a study, the two main failure mechanisms of interconnections, joint detachment and wire-bond lift off were studied

in single- and double-sided sintered diode chips [37]. In the double-sided case, two 1 mm silver bands with 100 µm thickness replaced the Al wire bond. The results indicate that bond-wire lift-off and aluminum reconstruction are the main failure mechanisms of single-sided sintered assemblies under power cycling conditions. The life of double-sided LTJT assemblies is reported to be nearly double that of single-sided assemblies; however, the main failure mechanism of the double-sided assemblies is not addressed by the authors. The high caliber mechanical and thermal performance of LTJT joints showed potential for high temperature electronic applications. Numerous research projects were conducted to improve the manufacturability and reliability of LTJT joints. A major improvement was shown with the application of nanoscale silver particles mixed with or applied instead of microscale silver particles.

Nanoscale Silver Sintering

The advent of nanoscale silver particles boosted solid-state sintering and their application in power electronics industry. The use of nanoscale silver particles in LTJT significantly improves the sintering conditions required to process a high-quality joint. Decreasing particle sizes creates an opportunity to revise other influential factors, such as processing pressure and temperature. In a case study, Lu et al. [38] assessed the dependency of joint density on influential factors, such as pressure and kinetic factors. Two types of sintering strategies were considered: first, microscale (1-3µm) silver particles were sintered at a low temperature (240˚C) under 40 MPa; and second, processing nanoscale (10-30 nm) silver particles at 280˚C without pressure. Both joints showed acceptable density and high thermal-conductivity. They concluded that utilization of smaller particles results in similar density with lower or no pressure

during processing. Extensive research in processing and optimization of sintered joints is ongoing; recently, several sintering pastes have been commercialized [39].

The following sections concentrate on silver sintering, its requirements, and properties; however, alternative materials (such as Cu) are discussed separately at the end of this section to evaluate the progress in their manufacturability, as well as their relative advantages and disadvantages over silver particles. The "sintering" described in the first part of this article indicates "silver sintering" unless otherwise mentioned.

Liquid Sintering

In liquid phase sintered joints, at least two materials with high inter-diffusion coefficients are placed in contact. Usually, one of the materials has a significantly lower melting point; the liquid phase sintering process starts above this temperature. The now molten material diffuses into and reacts with the solid material in a process called isothermal solidification. Preferably, all the molten material should react with the solid material to form IMCs. These IMCs have a higher melting point than the low temperature melting ingredient [40]; so, liquid phase sintering provides the ability to process high temperature joints at low temperature conditions. For example, Ni-Sn liquid phase sintered joints will form Ni_3Sn_4 IMCs and can have melting temperatures >700˚C while the processing temperature is ~245˚C [41], [42]. Processing at low temperatures prevents possible damage to the other packaging components and provides lower thermomechanical stresses due to coefficient of thermal expansion (CTE) mismatch during fabrication.

Considering their unique processing, liquid phase sintered joints demonstrate decent potential for application in high temperature power electronic devices as a die attach.

As an alternative to silver sintered joints, liquid phase joints are fabricated from a diverse range of materials, mostly less expensive materials, with prospects of solving creep and electro-migration issues seen in silver. Two primary methods are utilized in the fabrication of liquid phase sintered joints: 1) foil or layer deposition and sintering on contact sheets of raw materials; 2) powder paste sintering. This latter method is fundamentally similar to the former but utilizes a raw material in powder form mixed prior to sintering. Application of layered sintering in power electronics is a long-established practice.

Figure 2-2 shows the common thermal profile for transient liquid phase sintering. The paste used in this process is presented in Figure 2-3; it is a mixture of high melting point (HMP) and low melting point (LMP) particles in an organic vehicle, a combination of binder, surfactant and thinner. First, the paste goes through an optional drying stage to evaporate the binder solvent and reduce the pores. Then, the heating continues until the flux burns and reduces particle oxides. At the processing temperature, the molten LMP surrounds HMP particles, and IMC grains start growing on HMP particles. During processing dwell time, based on the ratio of initial materials, it is expected that some of either the LMP or HMP phases exist unreacted at the end of the process. Having unreacted LMP phase decreases the joint stability at high temperature; while having unreacted HMP particles improves the mechanical properties due to better ductility of pure materials compared to IMCs. The relationships of processing temperature, melting points of the constituents, and the final product are presented in equations (2-1) and (2-2).

$$T_P > T_{LMP}; T_p\text{: processing temperature} \quad (2\text{-}1)$$

$$T_{HMP} > T_{IMC} > T_{LMP} \tag{2-2}$$

Different combinations of metals are used in preparing and processing TLPS joints, such as Cu-Sn, Ni-Sn, Ag-Sn, Au-In. The popular HMP materials for this process are Cu, Ni, Ag, and Au, and the most common LMP materials are Sn, and In. The processing requirements and joints properties for these systems are presented in Appendix I. In subsequent sections, different mechanical, electrical, and thermal properties are compared to identify the possibility of their application as an alternative to high lead solders.

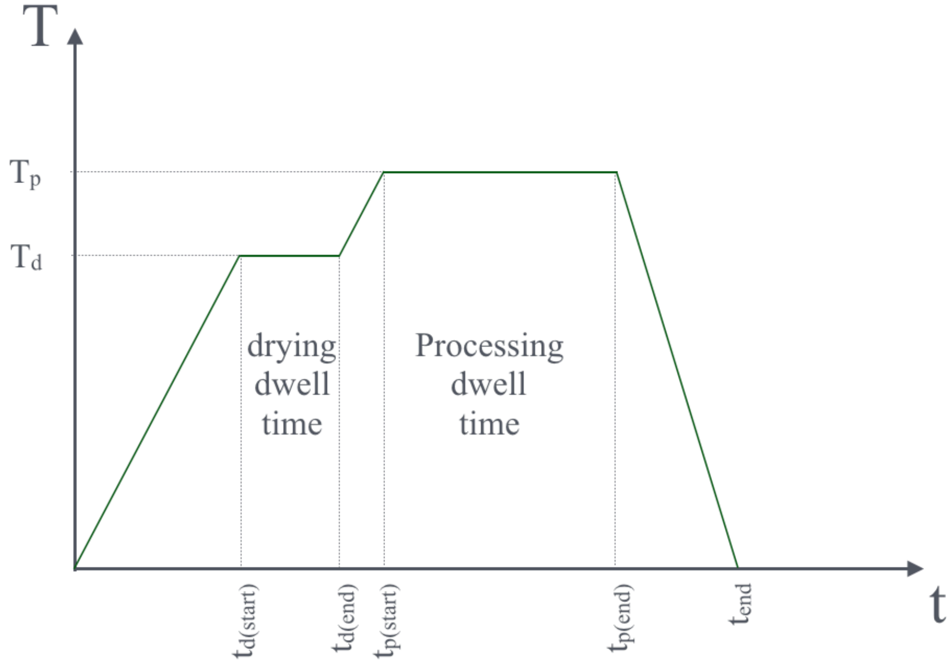


Figure 2-2: Processing thermal profile

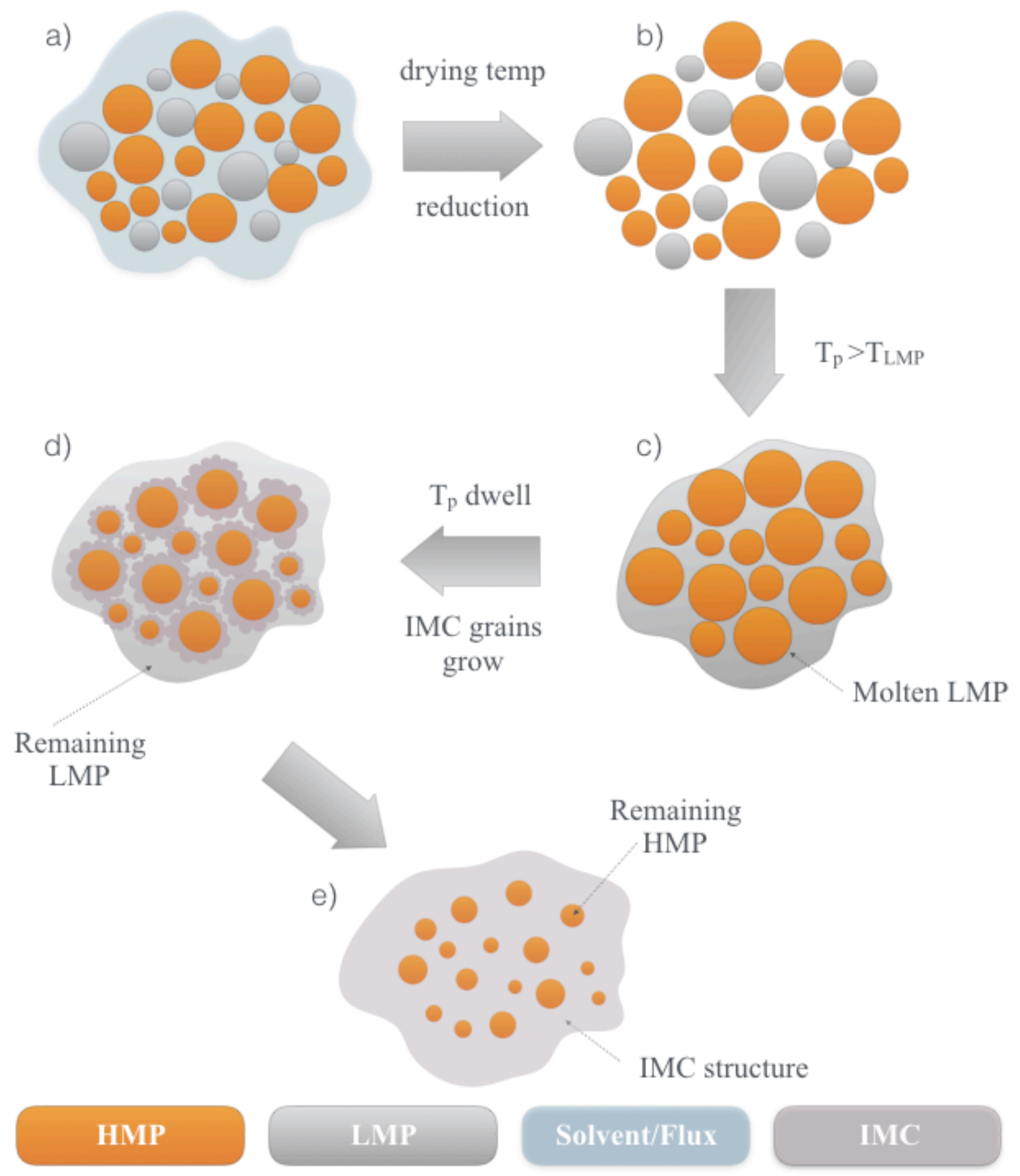


Figure 2-3: TLPS processing stages: a) HMP and LMP particles mixed in binder, b) Reduced particles at drying temperature, c) LMP phase melts and diffuse into HMP phase matrix, d) IMC grains start growing on HMP particles, e) An IMC matrix forms around the remaining unreacted HMP particles

Paste Constituents and Preparation

Organic Vehicle

The sintering process involves three diffusion mechanisms: surface, grain boundary, and lattice [38], [43]. Surface diffusion is the main mechanism employed in low temperature systems. This process results in clusters of particles which have lower potential for high temperature grain boundary and lattice diffusion processes. Necking increases the grain boundaries formed during surface diffusion; however, this is not accompanied with densification [44], [45]. Therefore, it is desirable to prevent surface diffusion while increasing the temperature to activate grain boundary and lattice diffusion. Bai et al. [43] showed that using a high burn-out (300-450˚C) temperature "binder" results in denser sintered joints. These "binders" are organic vehicles of different compositions used to maintain the physical and chemical properties of the sintering paste.

Prevention of low temperature sintering is the main objective of an organic vehicle; however, the surfactant, binder and thinner materials found in the organic vehicle have additional advantageous effects. The surfactant attaches chemically to the metal particles to prevent agglomeration [46]. The binder provides the integrity of the paste and keeps the sintering paste together after printing; the long hydrocarbon chains hold the particles in a way which prevents cracking during preheating or drying stages. The thinner controls the viscosity and further improves the printing potential. The mixture of these components is usually dissolved in an organic solvent, such as acetone or alcohol [47] to prepare the organic bed for solid particles. Then, the particles are added to this solution while mechanically stirred and agitated by ultrasonic waves [47],

preventing agglomeration and clustering [6]. Due to the addition of this organic combination in the paste a preheating step is required to evaporate and burn the solvent and organic vehicle. Sintering temperature and preheating duration are selected based on the materials used in the organic vehicle and their weight fraction. Generally, thermo-gravimetric analysis (TGA) and differential calorimetry (DSC) are used to define these characteristics.

Metal Particles

The literature presented in this section is mainly based on silver sintering, but it could be comparably applied to the other materials, such as copper. Joints prepared during the original applications of the LTJT method contained 20-30 μm silver flakes [33] and displayed decent mechanical and thermal properties. However, the use of microscale silver flakes requires pressure up to 40 MPa to provide the high density and low micro-void content needed to be considered a viable high temperature joining technology. Currently, nanosilver particles are utilized for sintering purposes; the most common sizes are between 10-30 nm [38], [43], [47]–[52]. Other silver particle sizes ranging from 1 μm to 30 μm [33], [38] have been tested and proved the possibility of producing acceptable mechanical, thermal and electrical properties. Smaller particle sizes provide higher surface energy and require less activation energy to diffuse; therefore, the sintering process can be completed at lower temperatures. Bai et al. [48] compared two joints produced by microscale and nanoscale pastes sintered at 280˚C. It was observed that the sintering process in the microscale joint restarts at 500˚C and the properties, such as electrical conductivity, were altered. Another study conducted by the authors

compared the densities of joints prepared from 30 nm and 100 nm particles. As expected, the smaller particles resulted in denser joints [43].

Hybridization is a popular method to maintain the density and strength of sintered joints while decreasing material costs [53], [54]. In this method, microscale particles are mixed with nanoscale particles during preparation of the sintering paste. Thus, the cost of production and the amount of required nanomaterial decreases. The density and other properties of sintered joints are determined by both the materials used in the paste and processing conditions, making it possible to obtain varying properties out of a paste by altering the paste composition or sintering conditions, such as pressure and temperature.

Paste Placement

Solid-state sintering

The most common method of placing the sintering paste between the die and substrate is stencil printing. In this method, the stencil is placed on top of the substrate and the sintering paste is spread on the substrate with a squeegee. Stencil printing is inexpensive and various joint thicknesses can be achieved with application of different sized stencils. The main constraint is that stencil thickness should be greater than the particle size. Screen printing is an alternative method for placing the sintering paste during which the paste is printed on a carrier film and then placed on top of the substrate by the carrier film. Selection of the proper organic vehicle influences the screen printing process significantly.

While screen and stencil printing are the most common techniques employed in placing sintering pastes, printing methods are not just limited to them. Mertens et al. [55] used a paste dispenser to print sintering paste dots as small as 150 µm in diameter and 15 µm in height, a technique known as dot printing. An array of sintering dots was prepared and a dummy die was placed on top of this array at 230˚C and 30 MPa for 10 s. The resulting joints showed shear strength of 20 MPa at 300˚C with the failure site analysis pinpointing joint fracture occurrence at the top of the sintering dots. Joint porosity was lower at the top interface due to the dot-printing mechanism. Thus, joints manufactured using this technique are more prone to fail under shear stress at the joint-top device interface.

Another method for placement of sintering paste was introduced by Kahler et al. [56], [57]. The sintering paste was transferred and placed on the substrate via power device, similar to flip-chip technology. In [56] the sintering paste was printed on a commercial InGaN-LED with Ti/TiN/Au metallization and then picked by a fine placer vacuum. The LED was placed on the substrate and sintered under 40 MPa at 250˚C for two minutes. In their recent article [57], the authors first printed the sintering paste on a carrier foil and heated it to 140˚C. Then, a pick and place device was used to locate the power device on the paste. The paste was detached from the foil and transferred to the top surface of the substrate. Finally, the sintering process was completed under pressure of the placer stamp. The sintered joints prepared by pick and place methods showed decent shear strength, however these methods are more appropriate for small area power devices which require high resolution manufacturing processes, such as micro-opto-electro-mechanical sensors [56].

Liquid phase sintering

Material placement for transient liquid phase sintering is categorized into two major classes: layer-based or particle-based. In layer based liquid sintering, a thin layer of LMP phase is sandwiched between two layers of HMP. During processing the LMP phase melts and IMCs start growing from top and bottom interfaces, Figure 2-4. The required processing time to complete sintering depends on the thickness of the LMP layer. For Cu-Sn system, micro-joints with full IMC structure were processed in 15 min by using a 5 μm [58]. Increasing joint thickness results in considerable increase in processing time and possibility of unreacted LMP inside the joint.

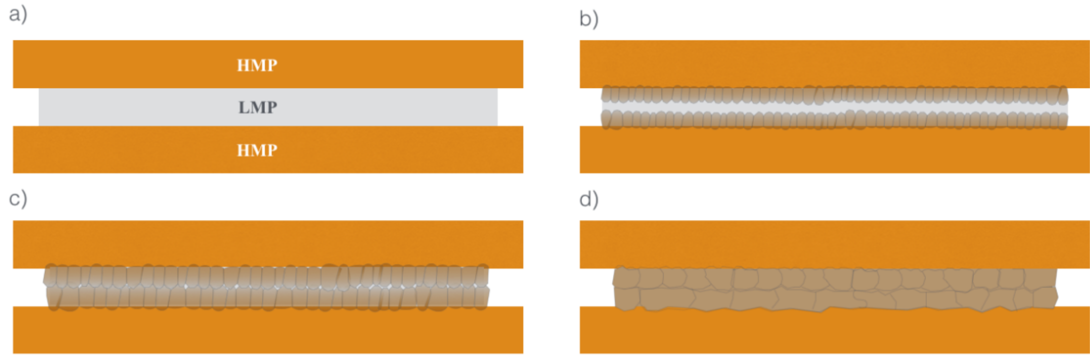


Figure 2-4: Layer-based TLPS processing a) Material placement, b) IMCs start growing c) Small amount of unreacted LMP phase d) Full IMC joint

Particle-based transient liquid phase sintering method provides a decent solution to long processing time in layer-based approach. Using particles increases the surface energy of the system and provides more interfaces regions to induce the IMC growth reaction. This expedites the sintering process and creates the possibility of having joints with different thicknesses. Just like solid-state paste placement, stencil printing is the most common particle-based TLPS paste placement method. The only consideration is diffusion of LMP material through the HMP matrix. One common method is printing a paste made of only HMP or a mixture of high HMP and low LMP contents. After

placing the semiconductor die, an LMP paste is injected around the printing area. Another approach is placing a chunk of solid LMP near the printing region and processing in a reducing environment [59].

Sintering Process

The sintering process is the single most important part of preparing a feasible high temperature die-attach. There are different combinations of parameters which can affect the quality of the final product. The sintering paste is the most important factor in the selection of these parameters. The effect of changing pressure, temperature, and sintering duration, as the most controllable factors, are considered in the subsequent sections. Other parameters, such as shrinkage and weight loss, were added to this list to enhance the understanding of the sintering process and increase its commercial and industrial applicability.

Pressure

The advent of low temperature joining technique is based on the application of uniaxial pressure during the sintering process instead of sintering at high temperature levels [31], [33]. Common pressure level is around 40 MPa to achieve acceptable joint quality at sintering temperatures in the range of 200-280˚C for microscale silver sintering, [35], [38], [55], [60]; however, this pressure level is detrimental to the semiconductor wafer in the package. Application of nanosilver particles provided an alternative to high pressure levels and produced high quality pressure-less joints at low temperatures [38], yet further research showed the advantages of applying pressure on nanoscale systems [56], [57], [61]–[64]. Pressing the paste during the drying stage before sintering also

improves the quality of final product [65]. Moreover, it could lead to preparing sintered preforms outside the package under very high pressure and then use them in packaging under low [66]. Generally, application of pressure develops sintered joints with higher strength and density and improves the electrical and thermal properties of sintered bonds. It is also reported that it is not possible to achieve acceptable sintered bonds over large areas without application of at least 1-5 MPa pressure [61].

Temperature

Sintering processes can be conducted at temperatures considerably lower than the melting temperature of the HMP material. In micron/nano-scale silver sintering, processing occurs at temperatures ranging from 200-350˚C depending on the pressure applied and time duration; however, the resulting joints will share silver's melting temperature (961˚C), improving the range of operability of sintered silver. In transient liquid phase sintering, the processing temperature depends on the melting point of LMP phase. For example, in systems containing tin or indium, the processing temperature should be above 232℃ and 156℃.

Other common high temperature interconnect materials require high temperature processing, or are limited to operation at low temperatures. Sn-based high temperature solders are processed at temperatures lower than 260˚C but operation temperature is limited to 225˚C. Similarly, Pb-Sn solders can be processed at 217˚C but should not be used in temperatures exceeding 183˚C [67]. Au-based high temperature solders can operate up to 280˚C but require high processing temperatures (~310) [67]. Technologies like silver epoxy process at temperatures less than 200˚C but only operate at temperatures less than 200˚C [67]. On the other hand, sintered joints survive up to

extremely high temperatures while their processing temperature does not exceed the semiconductor packages thermal limits.

As mentioned in previous sections, the appropriate sintering temperature should be selected based on the properties of the sintering paste and other processing factors, such as pressure. While increasing the pressure can decrease the sintering temperature, it should be considered that the lower bound of the sintering temperature is set by the organic vehicle in the paste; sintering temperature should exceed the organic binder burnout temperature. The trade-off between the burnout temperature of organic vehicle and sintering temperature is an important contributing factor in initiation of sintering. Selecting temperatures close to or lower than the organic binder burnout temperature results in high porosity, low quality joints [43]. Another important consideration in selection of the sintering temperature is the energy required to activate the grain boundary and lattice diffusion processes. As previously discussed, at low temperatures the sintering is mainly driven by surface diffusion while grain boundary and lattice diffusion occur at higher temperatures [38]. These high temperature diffusion processes are necessary to achieve a high density sintered joint [43]–[45]. Temperature range 200-350˚C is sufficient to activate the high temperature diffusion processes while protecting the semiconductor from unfavorable high temperature effects.

Ambient

The sintering ambient is another influential factor in the sintering process and consequently, joint quality. Two types of environments can be utilized as sintering ambient: open air and inert gas. Open air sintering is popular due to its simplicity and low procurement. On the other hand, inert atmosphere offers lower possibility of

oxidation. Knoerr et al. [63] sintered nanosilver pastes with diameter <50nm under nitrogen and open air. Densities of sintered joints were evaluated, and it is reported that joints sintered under open air show higher density. The authors also indicated that 60s of sintering under 5 MPa pressure at temperature 200-300˚C resulted in necking of silver particles under nitrogen ambient, while bulky grains (>1µm) were obtained during that time in air. Thus, it can be stated that air provides the required oxygen for burnout of the organic material inside the paste, while in nitrogen ambient the silver particles are trapped inside the organic binder at sintering temperature. This prevents the high temperature diffusion processes and results in low quality joints. The best density results were produced by open surface sintering of paste under open air [63]. The open surface provides enough area for organic binder evaporation to occur before completion of the sintering process. Similar results were reported for microscale silver sintering (25-50µm) under nitrogen and open air [68]. The authors investigated shrinkage and weight loss of the paste during sintering. The results from uncovered samples indicate that under open air the samples reach a stable weight, ~80% of the initial weight, at 238˚C while weight loss continues up to 318˚C under nitrogen.

Recently, two step transient liquid phase sintering became of interest, in the first step the mixed particles will be processed in open air and a high porosity joint will form [69], [70]. Then, LMP paste will be injected around this joint and under a reducing environment, the assembly will be heated to sintering temperature. Another option is using extra flux in the LMP paste and process the joint in the open air. The reducing environment or extra flux removes the oxides and provides clean surfaces for IMC growth.

Shrinkage and Weight Loss

The evaporation and burn out of the organic content in weight loss and shrinkage of the sintering paste. Densification and diffusion of metal particles are the other causes of increased shrinkage in sintered joints. Most of the common sintering pastes are composed of 10-20wt% organic content and 80-90wt% metal particles. This organic binder will evaporate and burn during sintering at temperatures generally lower than 175˚C. Thus, it is expected to see ~20% weight loss during the sintering process. Lu et al. [61] studied the shrinkage and weight loss of nanosilver sintering paste during processing using an optical method similar to [71]. In this method, the sintering paste is printed on a horizontal substrate and another substrate is placed on top of the paste. A polished alumina piece is placed on substrate from the edge while its other edge is pivoted to a fixed location. The change in thickness of the sintering paste/joint results in moving of the alumina piece. A He-Ne laser beam emits on the alumina piece and the reflected beam is collected by a detector. The collected beam is analyzed to define the angle of alumina piece and consequently the thickness of the joint. Lu et al. [61] evaluated the shrinkage of the paste printed with small ($<3 \times 3$ mm^2) and large ($>10 \times 10$ mm^2) printing areas and chips. The authors mentioned the use of 1-5 MPa pressure during heating of large area samples to achieve acceptable joint quality. 17.5% weight loss and 55% decrease in thickness are reported. This large proportion of shrinkage to weight loss confirms high densification in the paste during sintering.

Wang et al. [68] conducted a similar study to [61] and monitored weight loss and thickness shrinkage of sintering pastes with 1, 9, and 25 mm^2 area. Sintering pastes (20wt.% organic content: 80wt.% metal particles) were stencil printed on an alumina

or silicon substrate and heated uncovered up to sintering temperature. This same method was applied to another set of samples, but with a similar substrate used to cover the top surface. The uncovered samples' weight stabled at 80% initial weight at 238˚C; the covered samples did not reach a stable condition up to 275˚C. It is noted that weight loss by percentage decreases with increasing sample size. Therefore, it is concluded that residual burnt organic binders remained in the joints. The authors suggested pre-drying the pastes before covering them with another substrate to decrease the amount of binder prior to sintering. Their proposed maximum drying temperature is 150˚C to prevent premature necking and sintering of the particles at low temperatures.

A similar technique to [71] was used to measure the thickness shrinkage of covered samples. The results show that during the heating of larger area samples (5 × 5 mm^2), the thickness increases in some temperature ranges. This is mainly due to the accumulation of gasses caused by binder evaporation below the top surface. This can result in delamination of the joint at interfaces. Furthermore, the authors showed the effects of constant-rate and ramp-soak heating profiles on joint quality in large area (5 × 5 mm^2) samples. The higher rate heating resulted in delamination of the substrate and sintered film while in ramp-soak heating only longitudinal cracks at the interface were reported. The authors suggest the use of low pressure levels to overcome this problem, similar to [64].

Pre-drying

Pre-drying sinter paste before the sintering process is an effective method of improving joint strength and quality. Especially in large area joints, gasses produced by organic content burnout accumulate underneath the top substrate and result in bowing or loose

bonding. Pre-drying provides a step to remove the remaining binder burnout and accumulated gasses from the paste and start the high temperature diffusion process. The nature of the pre-drying method is selected based on the organic materials used in the paste and the temperature limits. The most common pre-drying technique is heating uncovered printed sintering paste on a standard heat plate under air up to temperatures ≤180˚C. The top surface (power device or substrate) is then placed on the pre-dried paste and heated to sintering temperatures in a thermal chamber or on a heat plate.

Nowadays, pre-drying is an integral part of the sintering process. Control over the effects of organic content on the final sintered joint as well as higher joint quality are the main reasons to consider the addition of a preheating step before sintering. The pre-drying process is generally performed in three or four steps using the heat soaking approach [61], [67], [72], [73]. For example, Chen et al. pre-dried sintering paste in three steps: 20 min at 50˚C, 20 min at 100˚C, then 5 min at 175˚C [72]. Because the preheating stage provides the capability to monitor the paste at temperatures close to sintering, it is possible to calculate the correct percentage of organic content required to prevent cracking during pre-drying [47]. Other researchers reported the positive influence of increased pre-drying time on shear strength of sintered joints [51]. The desirable effects of pressing the sintering paste during pre-drying are reported by Xiao et al. [65]. The authors showed that using the double-print method and applying pressure during the pre-drying stage provides strong joints with die-shear strength >30MPa. The increase of pressure during drying stage produces joints with >98% relative density.

Surface Metallization

Surface metallization influences bonding and sintering characteristics. Bond strength is directly affected by the surface metallization; sintering factors, such as temperature, pressure, and duration should be modified based on the surface metallization implemented. It is generally known that plain silicon wafers do not directly attach to sintered silver and therefore metal-plated silicon wafers must be used for sintering. Actually, this property can be used to sinter the paste under cover of plain silicon wafer, and the cover detached afterwards to study the sintered joint surface [63]. Noble metal plating used with other materials as diffusion barriers (Ti/Ni) underneath are very common in silver sintering [56], [74]. Among the noble materials, gold and silver are the best candidates for plating of substrates. Sintering on silver plates is easier and faster due to a higher self-diffusion coefficient of silver particles compared to the gold-silver inter-diffusion coefficient [44]. Lu et al. [67] conducted nanosilver sintering on two types of plating, silver and gold, and showed that under similar conditions the sintering temperature is 275˚C and 325˚C, respectively. Buttay et al. [75] used nanosilver particles (8-12 nm) to sinter SiC and silicon chips with silver backsides to Al_2O_3 substrates with copper plating. Various surface finishes and plating were used to prepare the samples, Table 4. The authors indicated that surface roughness affects joint shear strength significantly; however, the effects of surface finish and paste thickness were not significant. Furthermore, it is mentioned that sintering on bare copper finishes resulted in high oxidation of the copper on the surfaces, regardless of die size. It should be noted that the nanosilver particles used in this experiment were extremely small; this increases the effects of surface roughness on the final joint strength.

Table 4: Substrate metallization and plating [26]

Thickness (μm)	Substrate	Pressure (MPa)	Remarks
50	Raw DBC	6	
50	Raw DBC	6	
50	Au-finished DBC	6	Manual scrubbing to get good die-paste contact
50	Au-finished Si_3N_4	6	
50	PolishedDBC	6	
100	Raw DBC	6	
50	Raw DBC	0.7	
50+50	Polished DBC	6	Two-step screen printing
50+50	Raw DBC	6	Two-step screen printing

Alternative methods to facilitate the sintering process without silver or gold metallization are of interest. Mei et al. [51] reported that the Current Assisted Sintering Technology (CAST) demonstrates suitable potential to fabricate dense sintered joints with high shear strength in short time durations, even without silver electroplating of components. On the other hand, Kahler et al. [76] proposed sintering of Cu particles to avoid the need for surface metallization. Transient liquid phase sintered joints have a great advantage in this sense compared to silver sintering. The significant potential of LMP phases, such as tin, in wetting different surfaces and form IMCs with different substrate materials provides a substantial opportunity to process them on a wide range of power substrates.

Experiment:

There is at least a high and low melting point constituent in a TLPS. In this dissertation, tin is considered as the LMP phase, and either nickel or copper as the HMP. Considering Cu-Sn phase diagram, the Cu and Sn melting points are 1085°C and 232°C, respectively. At temperatures above 232°C, Sn melts and diffuses through Cu particles and gradually forms Cu_6Sn_5 with melting point of ~415°C [77]. As the

process continues and the liquid Sn decreases, another type of IMC with lower Sn content will form Cu_3Sn, which has a melting point of 675°C. Thus, an interconnection made of Cu-Sn IMCs has a great potential to support the current move toward application of wide bandgap semiconductors and increase in application temperature of power electronics.

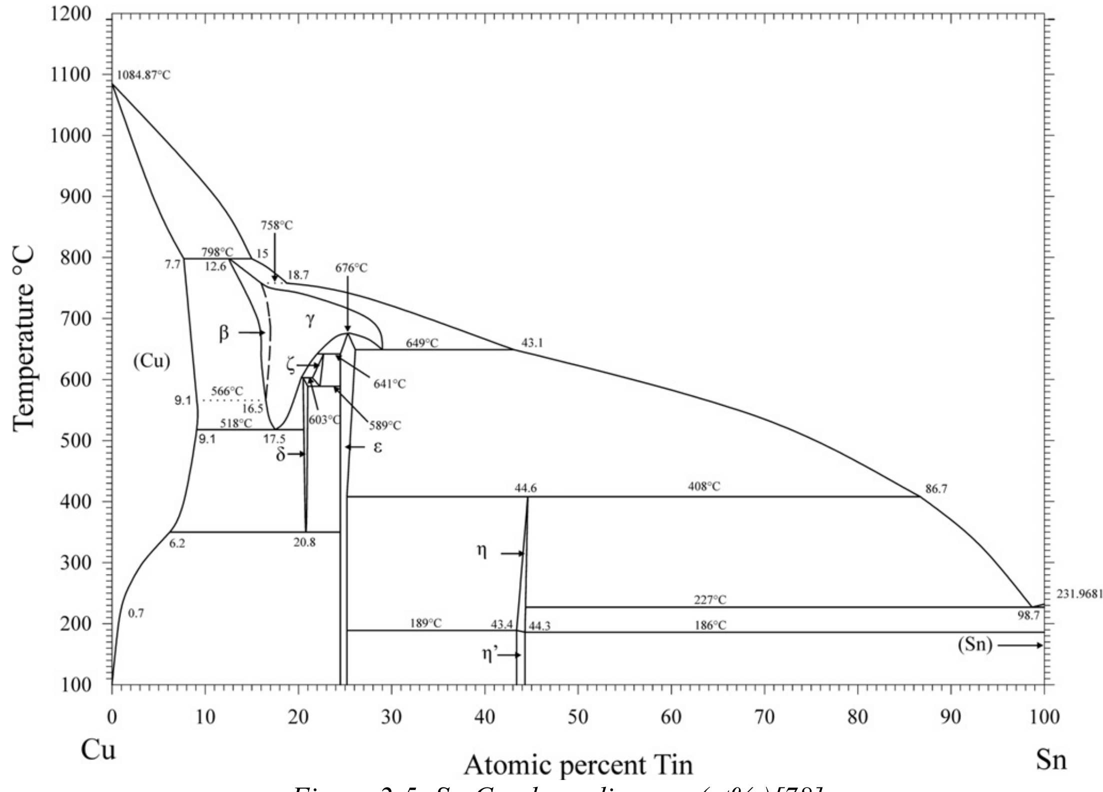


Figure 2-5: Sn-Cu phase diagram (at%)[78]

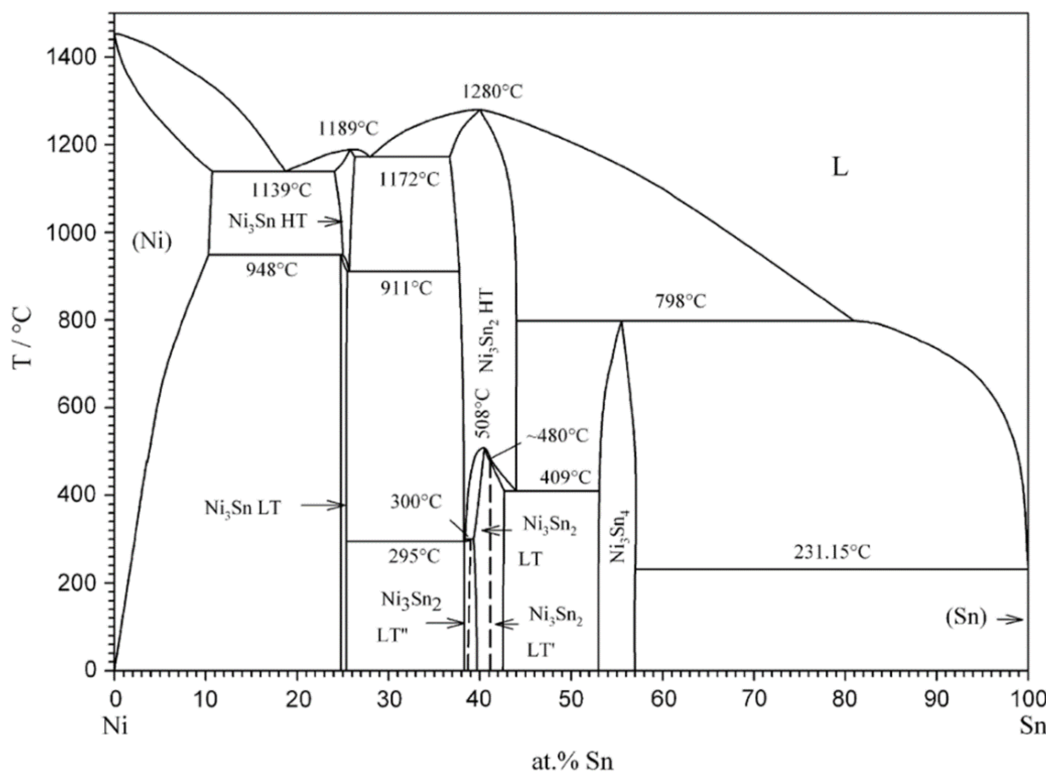


Figure 2-6: Ni-Sn phase diagram (at%) [79]

Another important part of TLPS pastes is binder (generally, an organic vehicle). It provides the capability to mix the metal particles while creating the integrity to stencil-print the paste. Here, the two constituents, Cu and Sn particles, were mixed together with TACFlux026 from Indium Corporation. This provides a good binding between the constituents at room temperature, and removes the oxide layers from particles at high temperature, just before processing temperature. The high viscosity of TACFlux026 creates a good integrity to keep different packaging components in place; however, a slight pressure of 0.5 MPa on the semiconductor die during processing prevents die misalignment or moving due to flux evaporation. Moreover, the activation temperature near 180℃ cleans the oxides before tin melts and provides the buffer time to evaporate and leave the joint area before sintering starts.

The ideal amount of HMP and LMP particles are based on their weight percentage fraction in the target IMCs. For example, for Cu_6Sn_5, and Cu_3Sn the proportion of Cu to Sn should be $62wt.\%$, and $39wt.\%$ respectively, equations (2-3) and (2-4). However, this condition could be exempted by application of two-step processing.

$$w\%(Cu) = \frac{6\, m_A(Cu)}{6\, m_A(Cu) + 5\, m_A(Sn)} \simeq 62\%; for\ Cu_6Sn_5 \tag{2-3}$$

$$w\%(Cu) = \frac{3\, m_A(Cu)}{3\, m_A(Cu) + m_A(Sn)} \simeq 39\%; for\ Cu_3Sn \tag{2-4}$$

In two-step processing, the paste is mainly made of the HMP particles and some binder. For this purpose, Cu (85wt.%) and Sn (3wt.%) particles were soaked in IPA (separately in two glass containers) and put in an ultrasonic cleaner for five minutes to break down the clusters. The wet particles were left under vacuum to dry and were immediately mixed in the binder (12wt.%). Figure 2-7 shows Cu particles right after ultrasonic cleaning. The particles were separated and no low temperature sintering was detected. The mixing was done manually for three minutes to obtain a uniform paste. The paste was vacuumed for two minutes to remove the air bubbles. This increases the density of the paste and results in higher amount of metal particles in stencil-printing region. Then, the paste is stencil-printed on the substrate.

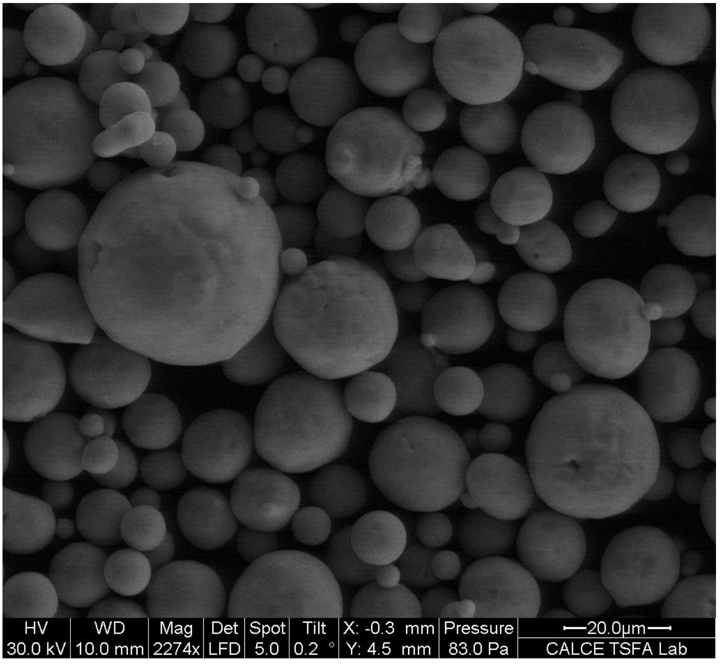


Figure 2-7: Cu particles after ultrasonic cleaning at room temperature

Then, the assembly was put in a vacuum chamber for two minutes to remove the created air bubbles during screen printing. This prevents the air voids with high potential to accumulate burn-out gasses and residual flux during the processing and consequently, deliver a higher density interconnection. A thermal drying profile at this step increases the print stability and prevents the particles from spreading on the surface. This step is important to prevent the moving of particles out of the joint area during the processing and forming IMCs out of the interconnection region around the edges. The assembly was placed in the chamber and heated slowly to 120°C with 5 min dwell time at 100°C and 120°C to dry the paste and create a more stable structure. Surface energy is the main thermodynamic cause of the sintering process. Thus, it is not favorable to lose the surface energy through low temperature sintering between the particles during drying. This is a major factor in sintering of nano-sized particles due to higher tendency to decrease their free energy through joining other particles. Here, due to the large size

Cu particles (compared to nano-levels), low temperature sintering will be limited during drying process. To further investigate this effect, Cu particles were heated up to 500°C and held for 30 minutes. It was observed that small particles (<5μm) form bridges between large particles, Figure 2-8. However, without pressure and liquid phase to improve the sintering process, no major connection was formed between the particles. Another important observation in this image is the arrangement of the different sized Cu particles. The connected channels between the particles provide enough room for the liquid Sn to move through the center of the joint and fill all the gaps.

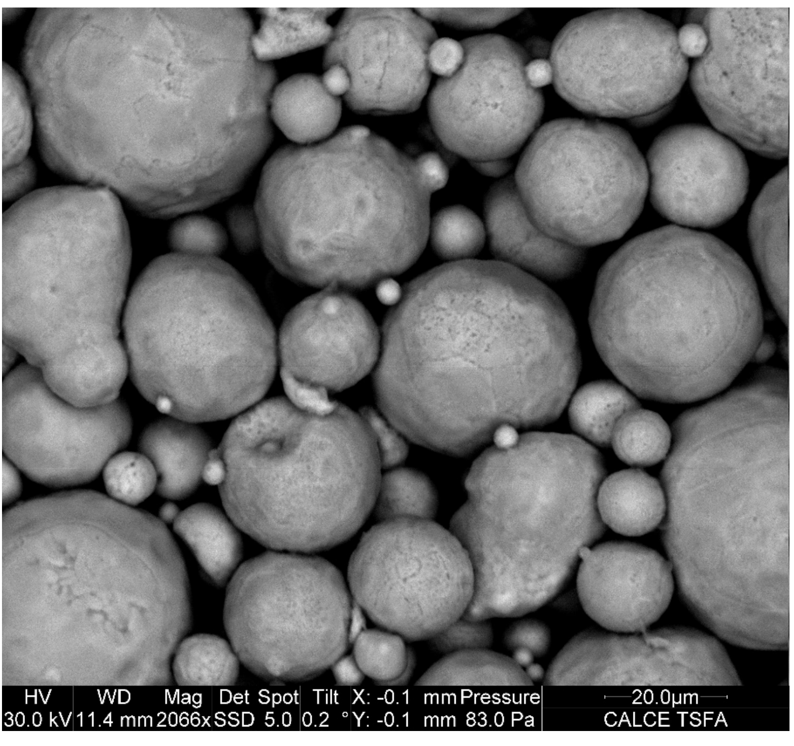


Figure 2-8: Cu particles after drying at 500°C

After the drying, the semiconductor die was mounted on the paste and a combination of LMP phase and binder was injected around the assembly, Figure 2-9. The sample was placed in the vacuum chamber (for 3 minutes) to remove the air bubbles from the

LMP paste and die/paste interface. Since the die-attach material should cover a large surface (~5×5 mm^2), the wetting capability of the LMP paste, in addition to the particle size of HMP phases, was considered as a decisive factor in paste processing. The acceptable combination of particle sizes and amount of LMP paste around the assembly was determined to iterative try and error process. Joints made of different particle sizes of Cu and Sn were made, cross-sectioned, and the fraction of voids to joining cross-section area was considered as the joint quality indicator. Finally, Cu particles with -325 mesh size (44 μm) were considered as the main part of the HMP TLPS paste with 85% of weight fraction. The rest of the paste was 12% TACFlux026 and 3% Sn particles with -140 mesh size ($105\ \mu m$). For the LMP paste, 85% Sn particles ($< 105\ \mu m$) with 15% TACFlux026 was used. In the next step, the processing environment and thermal profile will be discussed.

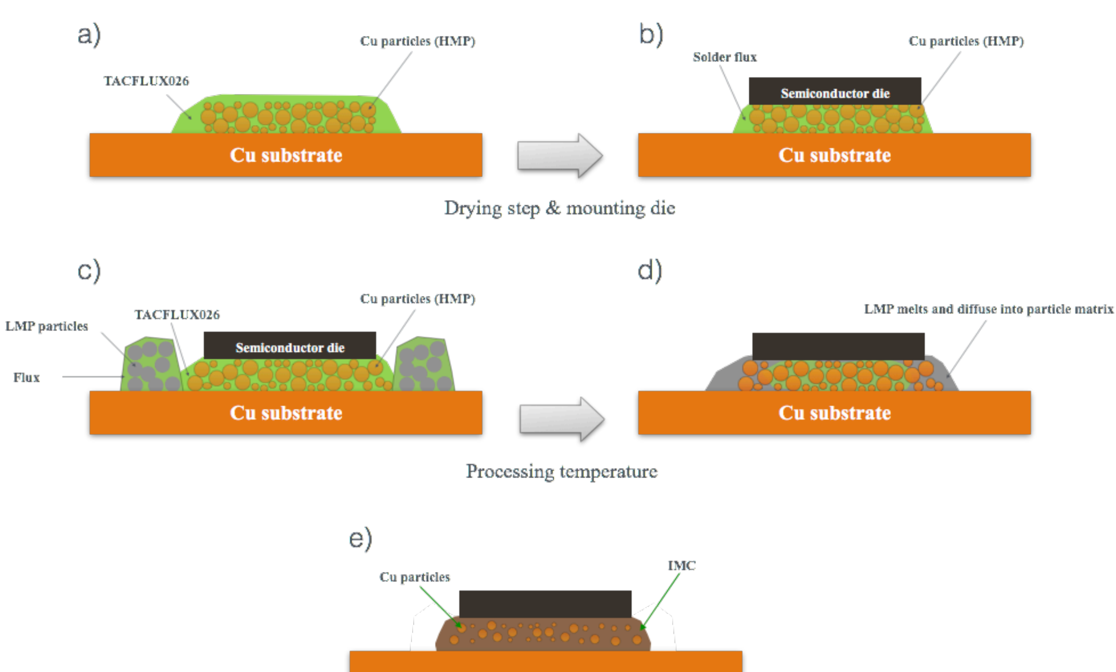


Figure 2-9: Two-step processing: a) HMP paste was stencil-printed on the substrate, b) Semiconductor die was mounted on the paste, c) LMP phase was injected around the assembly d) At processing temperature, the LMP phase melts and diffuses through the interconnection region

The samples prepared in the previous step were placed in the thermal chamber and heated to 190°C with a dwell time of 5 minutes. At this temperature, the TACFlux will evaporate. The dwell step provides the time-window for fumes to move out of the joint area before solder diffusion. Then, the temperature increases to 325°C with a 30 minutes dwell to complete the sintering process, Figure 2-10. The dwell time is a significant factor in complete processing of TLPS interconnection since IMC formation is a time-consuming process.

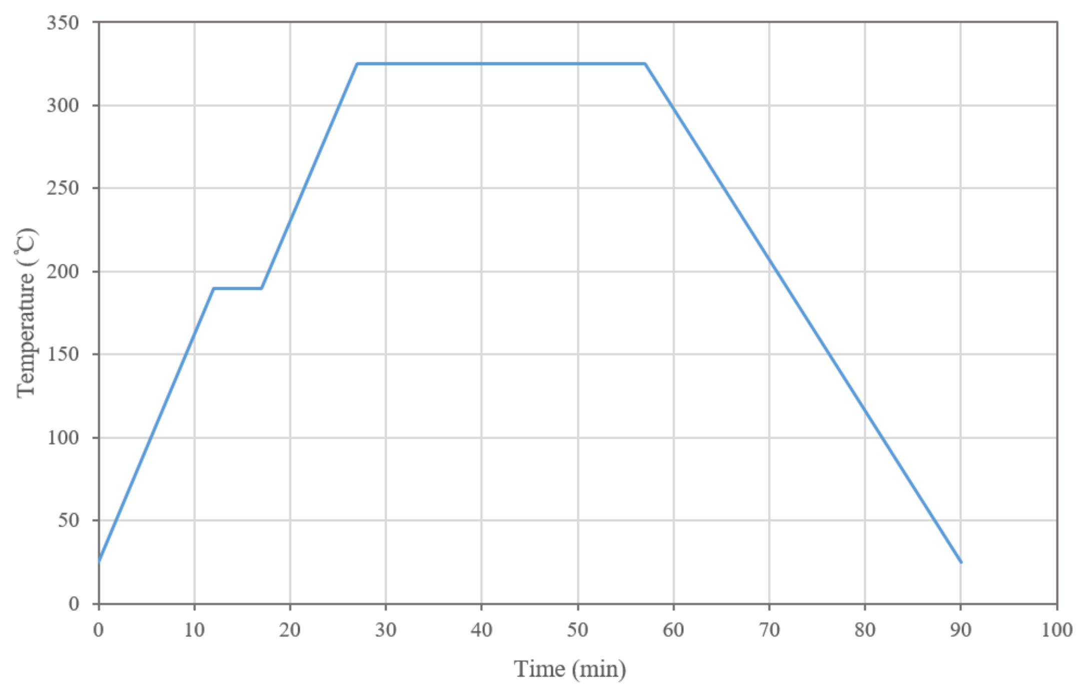


Figure 2-10: Cu-Sn two-step sintering thermal profile

Figure 2-11shows the top surface of a TLPS interconnection after processing at 325°C for 2 and 5 minutes. Instead of metal layered power device/metallic dummy die, a silicon wafer was placed on the top of the paste. After processing, the silicon was removed and the samples were investigated under environmental scanning electron microscope (ESEM). The short dwell step (2 minutes) did not provide enough time to grow enough IMCs to keep the integrity of joint during the cooling step. The longer

dwell step (5 minutes) provided a better quality joint and kept its integrity after processing.

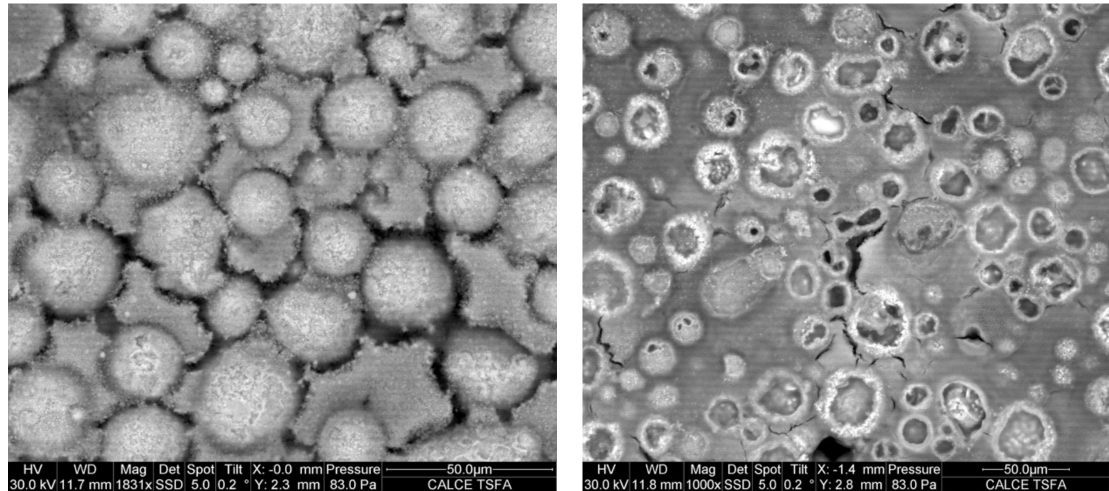


Figure 2-11: Considering the effect of dwell time on formation of TLPS joints: dwell for 2 minutes (left image), and 5 minutes (right image) at 325°C

For short dwell time (2min), the existence of extra LMP phase between the particles and separation of this phase from IMCs forms on the surface of the particles. Lack of a joining surface and pressure on top of the particles provided enough room for the molten material and particles to move and break easily. In the following sections, a similar test with a joining surface (Cu dummy die) on top of the paste was performed and a less destructive interaction between the phases was observed. The thorough analysis of effects of sintering time and temperature on the quality of TLPS joints is a challenging problem which is out of the scope of this work.

Figure 2-12 shows the cross-section of a fully processed Cu-Sn TLPS joint under environmental scanning electron microscope (ESEM). Obviously, the liquid Sn could fill the gaps between the Cu particles and at the processing temperature the IMCs formed and created a decent joint between a Cu die and substrate. The pores in the joint are mainly formed due to the burnt residues of the flux or trapped fumes in the joint.

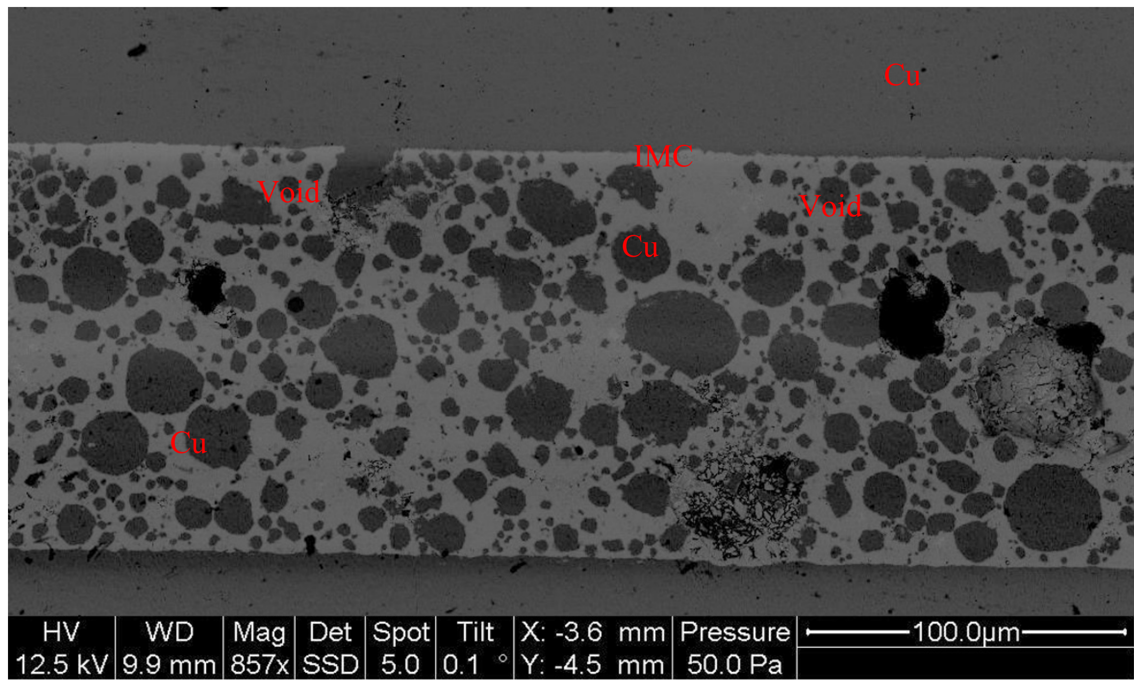


Figure 2-12: Cross section of a fully processed Cu-Sn TLPS joint

Two-step processing has considerable advantages, such as simplicity, low pressure during processing, and open-air environment. The main issue is lack of consistency due to significant dependence on operator skills. For example, for LMP paste injection, there are two considerations: first, it should be enough to diffuse all through the center of the joint; second, it should not be too much which results in extra LMP phase in or around the joint. Figure 2-13 shows an X-ray of a TLPS joint without enough LMP material from the top view. The lack of LMP material resulted in a huge un-wetted area and no attachment at the center. This results in oxidation of un-wetted HMP. Even with enough LMP material, there is always the risk that HMP particle arrangement prevents the molten material diffusion. Figure 2-14 shows having extra LMP material at the edges; obviously, a lot of unreacted material is left at the corners which results in continuous change in microstructure of the joint during operation. Also, having unreacted LMP, i.e. tin, limits the operation temperature to tin melting point and makes

the joint's behavior unpredicted at temperatures above that. Other issues with two-step processing is the limitation on placing components due to spreading of residues around the interconnection region, Figure 2-15, and increased possibility of shorting between the adjacent components and even top and bottom of the die as shown in Figure 2-16.

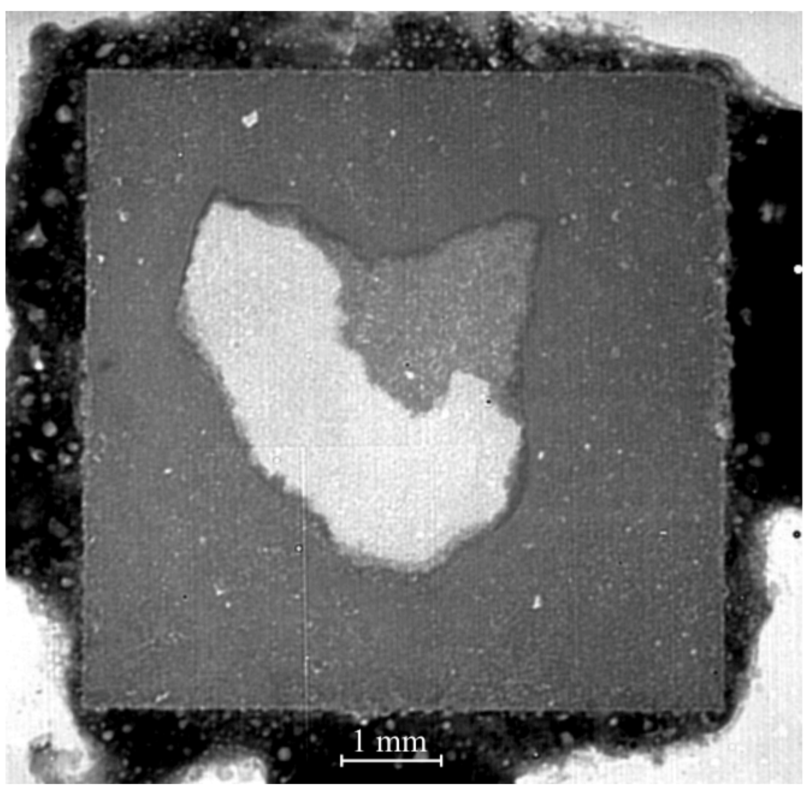


Figure 2-13: X-ray of a TLPS joint without enough LMP material from the top view; huge un-wetted area observed at the center of the joint

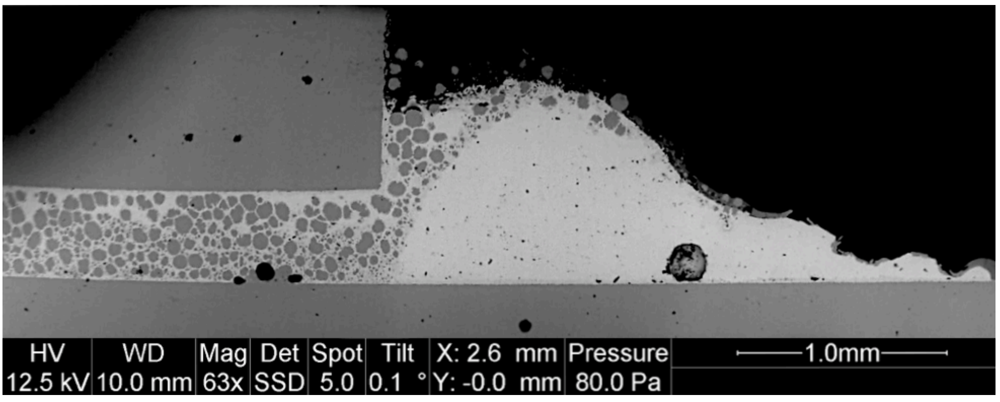


Figure 2-14: ESEM image of TLPS joint with too much LMP phase at the edges of assembly; unreacted LMP phase remained at the edge after processing

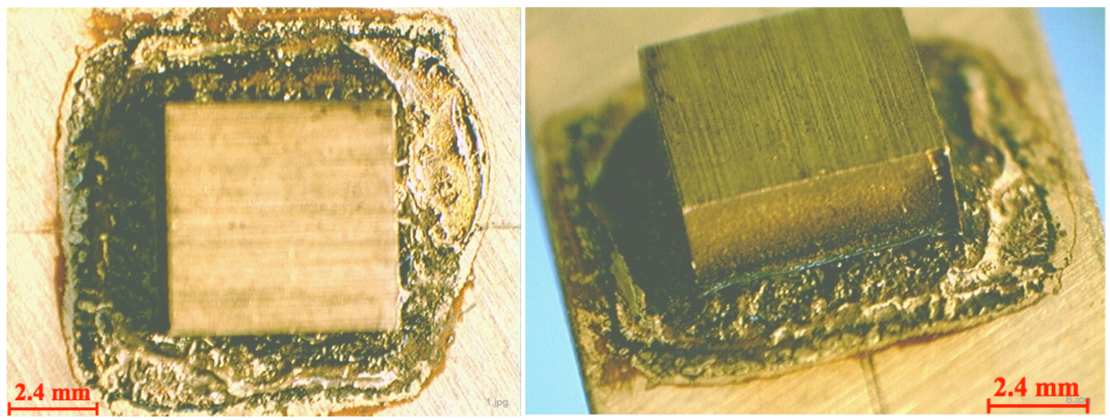


Figure 2-15: Extra LMP residues around the interconnection

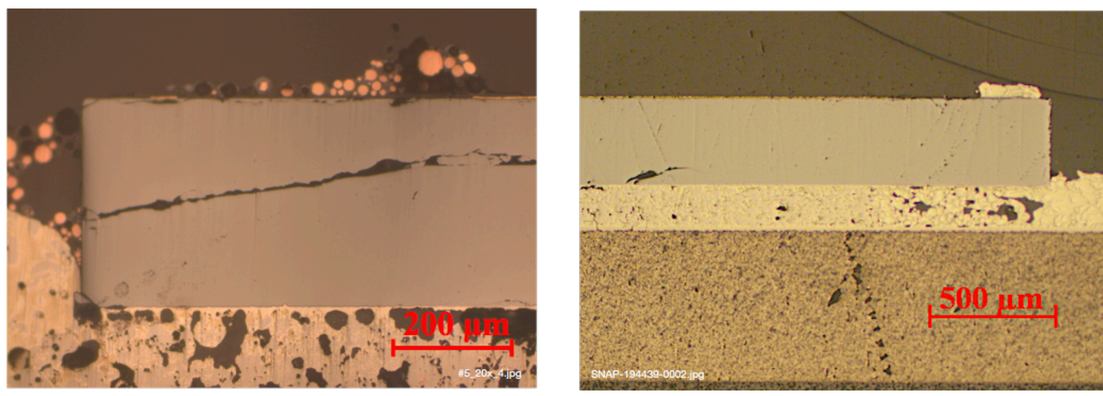


Figure 2-16: The LMP phase and migrated HMP phase moved to top of the die

<u>One-step processing</u>

The objective of one-step processing is to remove the inconsistencies in two-step processing and provide a simpler method that needs no specific training to process high quality joints. For this purpose, as the first step, the injection of LMP paste around the assembly as the source of most complications were removed and a combination of LMP and HMP phases paste was used. The proportion of copper to tin phase was considered lower than its weight percentage in Cu_6Sn_5 and slightly higher than its weight percentage in Cu_3Sn. This is due to the need for enough tin to facilitate the sintering process. Therefore, the final product is expected to have more Cu_3Sn than Cu_6Sn_5.

In one-step processing, the particles are mixed before ultrasonic cleaning step. 40wt.% copper and 48wt.% tin particles with less than 40 μm diameter were mixed, soaked in acetone, and cleaned with ultrasonic energy. This removes the oxides, breaks down the clusters, and rearranges the particles. Then, the TACFlux026 (12wt.%) was added and mixed manually for 3 minutes. Then, stencil-printed on a copper substrate, and a dummy copper die was mounted. The assembly was heated with a similar thermal profile use for two-step processing, except with one difference, lower maximum temperature (300℃), Figure 2-17. During the process, 3-5 MPa uniaxial pressure was applied on the die. This pressure induces the more solid-state sintering between the copper particles, and decreases the number of voids, and provides a decent quality joint.

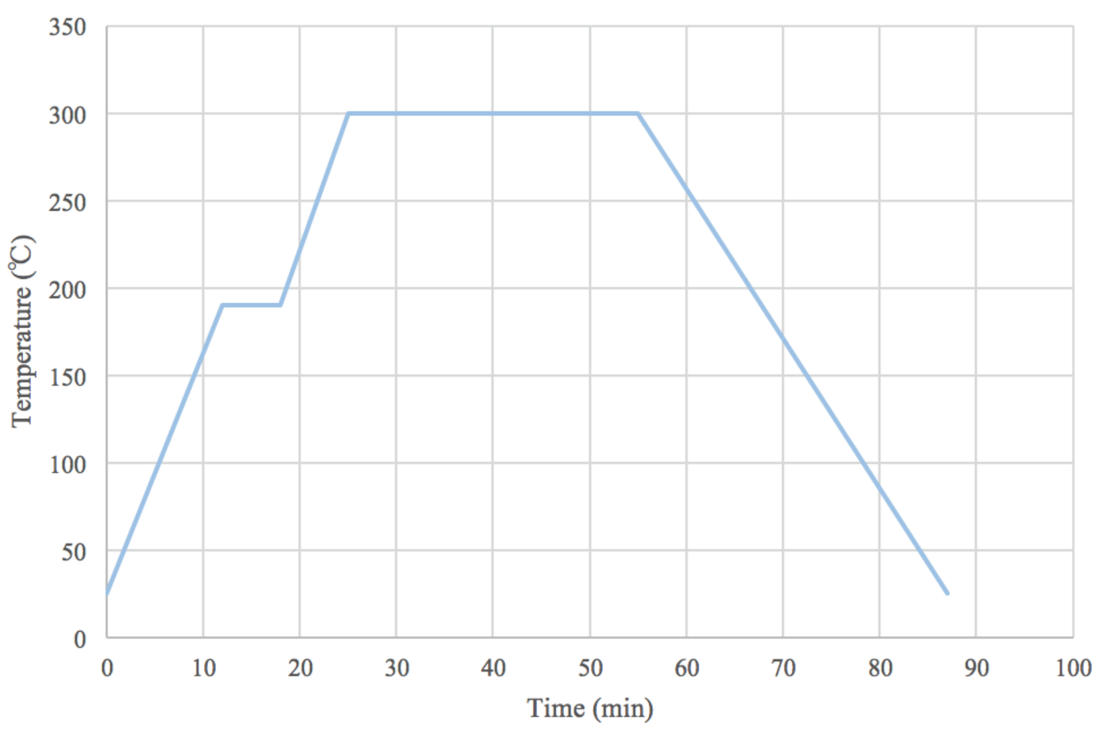


Figure 2-17: Cu-Sn one-step sintering thermal profile

Figure 2-18 shows the exterior view of a Cu-Sn joint made by one-step processing. The amount of residual material around the joint is insignificant compared to two-step processing. Obviously, the residual material is extra tin not used during processing. Unlike two-step processing residues, these tin residues can be removed by mechanical force without any damage to assembly and substrate. Figure 2-19 shows an ESEM image of the joint's cross-section. The joint has a very high copper content which improves its mechanical, electrical, and thermal properties. Also, the thickness is around 50 μm which is around one-third to one-fourth of common two-step TLPS joints. There are almost no voids and remaining tin in the joint. Higher magnification ESEM image, Figure 2-20, shows considerable formation of Cu_3Sn. Therefore, the Cu_6Sn_5 turns faster to Cu_3Sn and provides a more stable structure during operation.

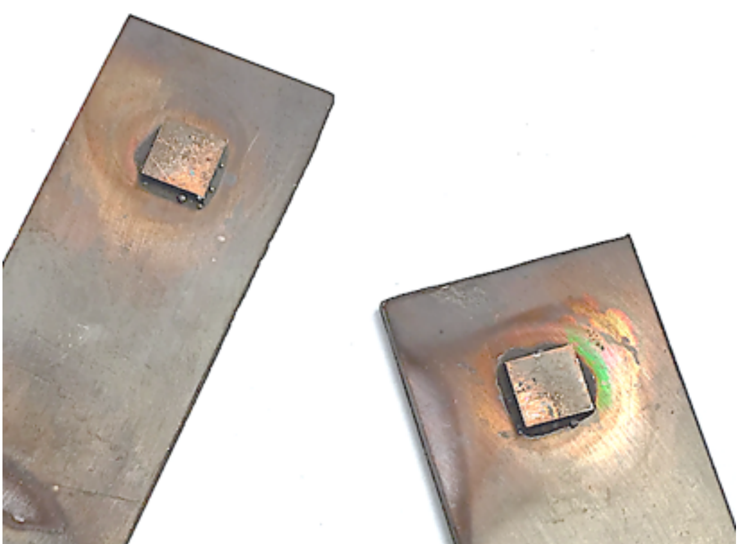


Figure 2-18: Cu-Sn interconnection exterior appearance using one-step sintering process

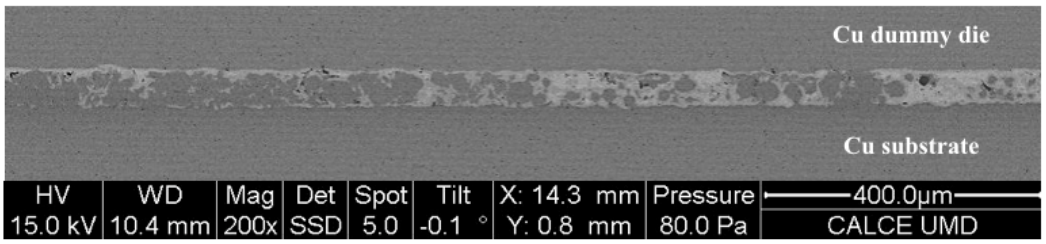


Figure 2-19: ESEM image of Cu-Sn TLPS joint (one-step processing)

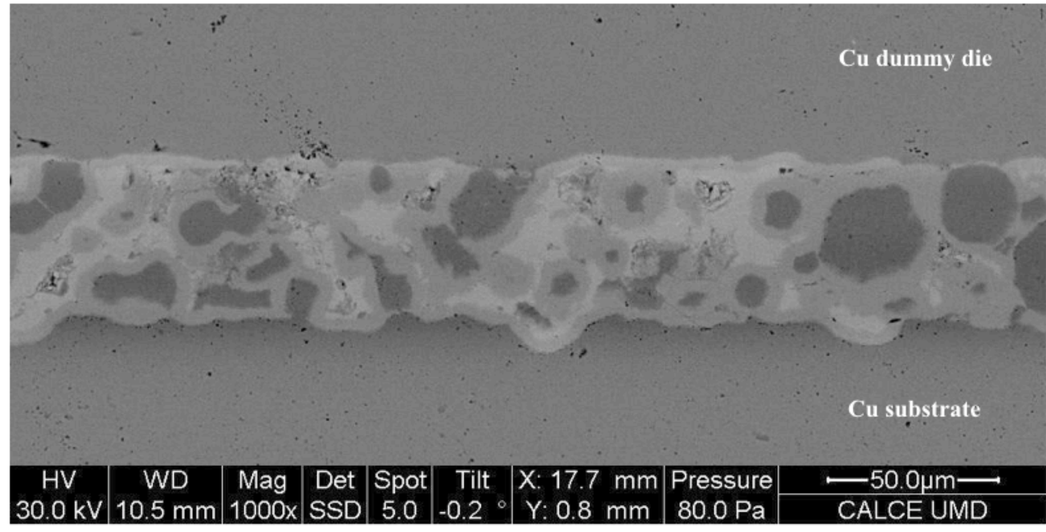


Figure 2-20: Higher magnification ESEM image of Cu-Sn TLPS joint (one-step processing)

<u>*Large-area interconnections*</u>

A significant advantage of one-step processing is its potential for processing large-area interconnections. The amount of LMP paste around the assembly in two-step processing depends heavily on interconnection area, in addition to LMP wetting and diffusivity ability. Most of the joints prepared with this method are limited to $6\times 6\ mm^2$ dimensions. An similar approach for joints with twice this size results in large un-wetted regions and low quality product, Figure 2-21. The maximum diffusion depth of the molten LMP is 5.7 mm which is close to the maximum capability of two-step TLPS processing. Thus, diffusion from the sides is not enough to create a high-quality joint.

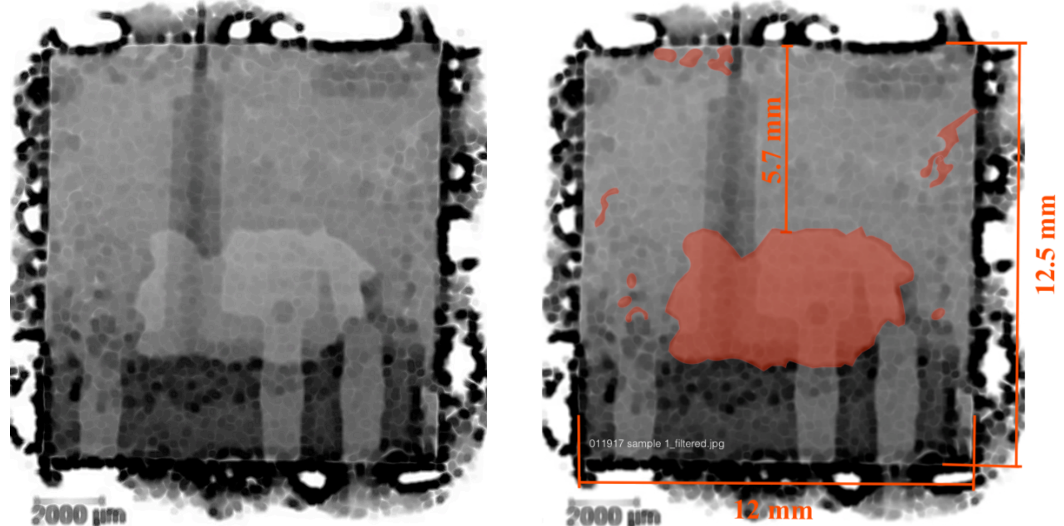


Figure 2-21: Top-view x-ray of a large-area interconnection processed by two-step Cu-Sn TLPS processing; the light-red regions define the un-wetted regions

Mixing the LMP and HMP phases with pressure assistance improves the diffusion and wetting properties of the paste. Figure 2-22 and Figure 2-23 show an interconnection with 3 times dimensions of the largest TLPS interconnection processed by two-step processing. This method decreases the fraction of un-wetted regions and pores, which improves mechanical, electrical, and thermal performance of the interconnection.

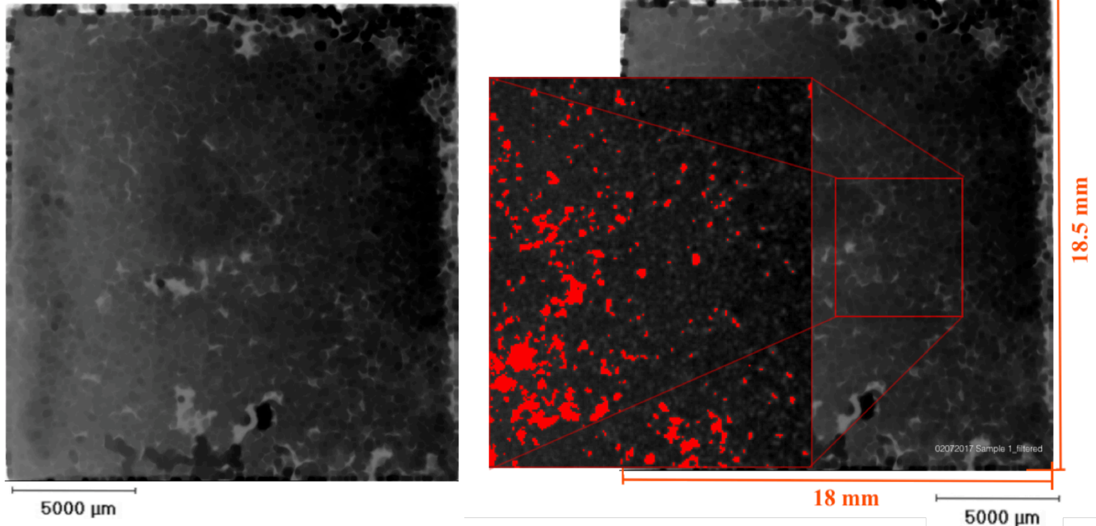


Figure 2-22: Top-view x-ray of a large-area interconnection processed by one-step Cu-Sn TLPS processing; the red regions define the pores regions

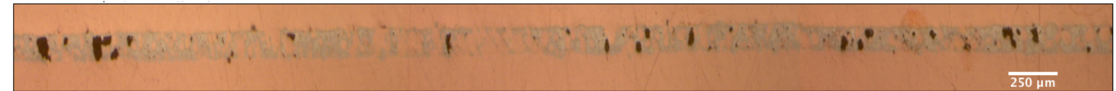


Figure 2-23: Cross-section image of a section of large-area interconnection processed by one-step Cu-Sn TLPS processing under optical microscope

Tertiary elements:

One-step processing provides an excellent approach to process TLPS joints with tertiary elements. In this section, the addition of carbon elements to Cu-Sn TLPS is demonstrated. Silver-plated graphite particles were added to copper and tin dry mixture with 25wt.% of dry mixture. Exact one-step TLPS processing method was used to create the interconnection.

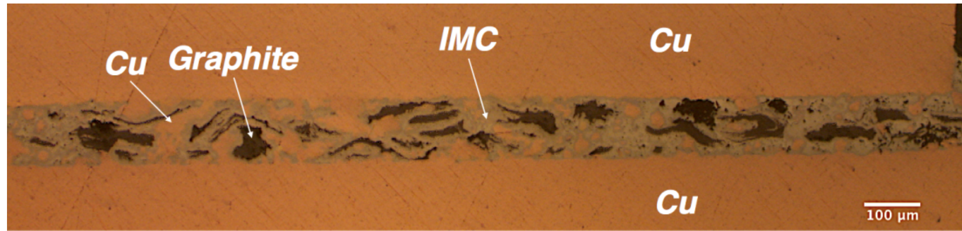


Figure 2-24: Cu-Sn TLPS with silver-plated graphite under optical microscopy

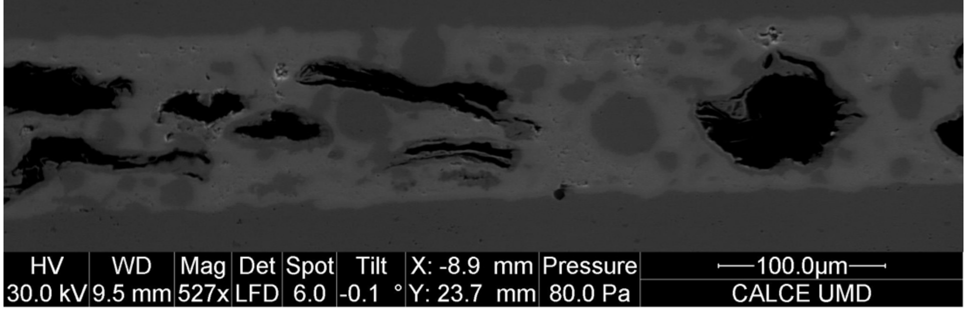
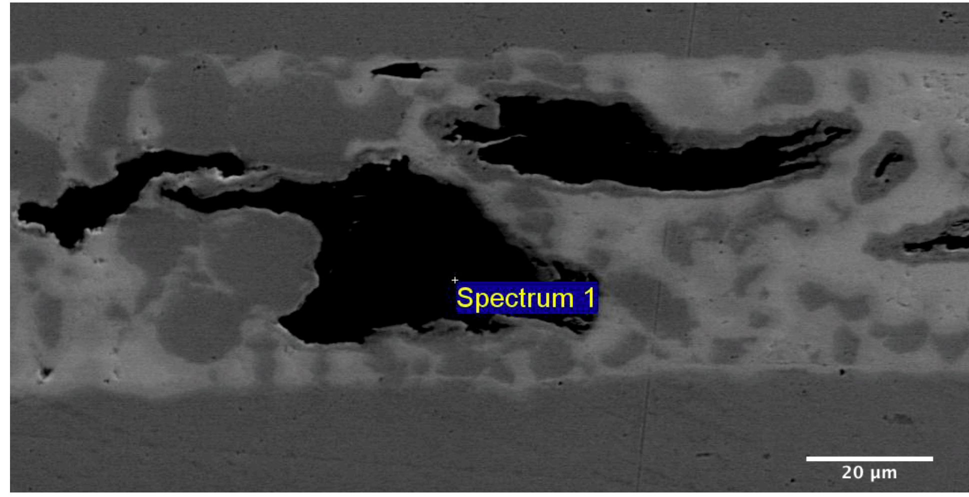
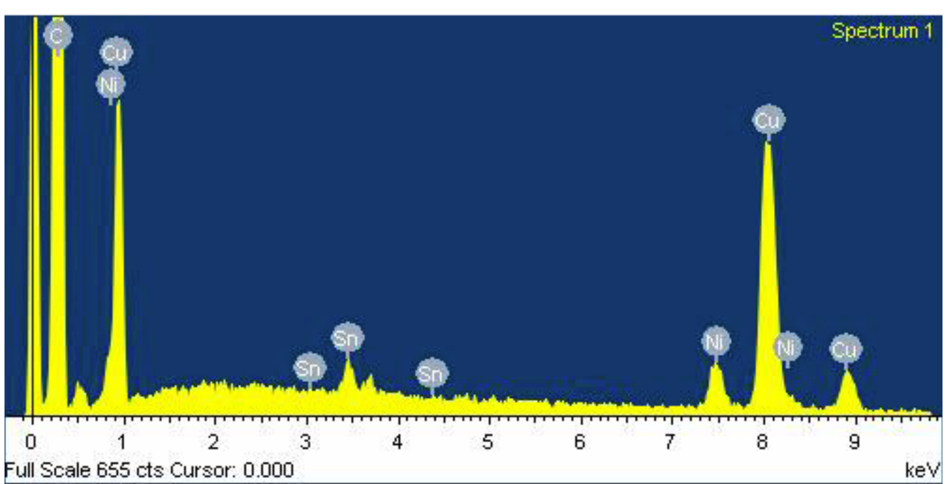


Figure 2-25: Cu-Sn TLPS with silver-plated graphite under ESEM

Figure 2-24 shows the cross-section graphite integrated Cu-Sn TLPS between a copper substrate and a dummy die. The joint has very low voiding and an excellent connection between graphite particles and IMC matrix. The magnified image of graphite particles in the joint is presented in Figure 2-25. The black regions were studied under energy-

dispersive X-ray spectroscopy (EDS) to verify the composition. The results in Figure 2-26 confirm that the black regions in ESEM are graphite.





Element	Weight%	Atomic%
C K	90.01	97.98
Ni K	1.08	0.24
Cu K	8.31	1.71
Sn L	0.60	0.07
Totals	100.00	

Figure 2-26:Cu-Sn TLPS with silver-plated graphite under optical microscopy

Conclusion

In this chapter, different categories of sintering method which are used in high temperature joint processing were introduced. The two main classes, solid-state and liquid sintering methods, were explained in detail and examples of materials used in each were presented. Then, the effective factors on quality of the joints and final product were discussed. These factors were selected with respect to different stages of interconnection, from paste preparation to sintering process. Factors such as paste constituents, placement, pre-drying, and shrinkage, sintering pressure, temperature, and ambient were considered. The second section of this chapter is dedicated to fabrication and development of high quality Cu-Sn TLPS.

Two methods were considered for fabrication of Cu-Sn TLPS interconnection. The first, was the two-step sintering process which is a common method used in research for preparing these joints. In this method, first, the high melting point (HMP) paste is printed on the substrate the die is mounted, and then, the low melting point (LMP) material is injected around the assembly. During the processing, the molten material diffuses through in interconnection region from the edges. Under controlled processing conditions, the LMP can reach all over the joint and creates a low porosity interconnection. The processing occurs under low pressure and open-air ambient. This method creates decent quality joints but depends a lot on the experience of the operator in controlling paste constituents, printing, low melting point material injection and other processing factors. Therefore, there is a need for a simpler approach which can

provide repeatable high quality products without sophisticated processing and operator training.

Second, the one-step processing method was introduced in this dissertation as a practical alternative for use in industrial applications. In this method, the TLPS paste is made of both LMP and HMP phases and does not need sophisticated procurement. The paste could be stencil printed and after mounting the die, the processing will be done under 3-5 MPa pressure. The pressure induces the sintering process and decrease the processing temperature. The results were interconnection with almost no voids or remaining LMP. The amount of LMP residues left around the interconnection region in one-step processing is negligible compared to two-step processing. It is worth mentioning that the amount of material used in this method is also less than the previous method. This could decrease material cost when working with more expensive systems, such as Ag-Sn, Au-Sn.

Chapter 3 : Microstructure evolution modeling during transient liquid phase sintering

Introduction

The complex microstructure of the sintered joints has considerable effects on their mechanical and physical properties that necessitate a detailed study of the microstructure evolution during the sintering process. Major microstructure transformations occur during the solidification step of liquid phase sintering. During the last two decades, the remarkable improvements of computational methods provided exciting opportunities to study the solidification process and created powerful methods to simulate and model microstructure evolution. The driving force behind the microstructure evolution during any thermodynamic process is reduction of the system's total (Gibbs) free energy. The formation and solidification of intermetallic compounds (IMCs) is a pivotal part of the sintering process which significantly affects the mesoscale morphology and microstructure of transient liquid phase sintering (TLPS) joints. During liquid sintering, solid-liquid interaction at the interface of high melting temperature particles and low melting temperature liquid is the most critical factor in IMC formation. Current numerical approaches consider two different models toward simulation of these interactions: classical "sharp interface" and phase-field-modeling.

In this chapter, first, an introduction to the conventional sharp interface model is presented, and then, the application of this method in derivation of the thermodynamics relations for solidification process is described. Next, the challenges in the way of

extending the sharp interface methods to more complicated phase transition cases[1] are mentioned. Then, the phase field model as an effective alternative for the sharp interface model is introduced. An overview of different phase field models and their fundamentals and assumptions are presented. Then, the requirements to employ each of these methods in TLPS processing are discussed. Then, a new multiphase PFM modeling method is introduced to improve the simulation of TLPS processes. Also, the simulation variables are evaluated based on experimental data. Finally, IMC formation during one and two-step TLPS processing are modeled and the shortcomings and advantages in the application of each method are discussed.

Classical Sharp-interface model

The sharp-interface model is also known as free boundary, moving boundary, and most famously the Stefan problem in the literature [80]. It is the conventional modeling method used in the study of microstructure evolution during solidification. In this approach, the solid-liquid interface, also known as phase change boundary, is a two-dimensional surface with zero thickness, mass, and structure. The kinetic and thermodynamic relations of each phase are developed separately based on physical relations and are related to the other phase as the boundary conditions at the sharp interface. This may result in some discontinuity in phase parameters, such as concentration, at the interface. The local interfacial velocity is either calculated from the driving forces for the interface motion or introduced as boundary conditions into the system and the interface position is tracked explicitly through the solidification

[1] Such as the process of phase transition in binary, eutectic, or multiphase alloys

evolution [81], [82]. The complexity of this process limited the application of the sharp-interface model to simple cases, such as modeling one-dimensional solidification of pure materials.

The three main governing equations in solidification of a sharp interface pure material liquid-solid system are: 1) Classic thermal diffusion equation that applies to each of the liquid and solid phases, 2) Discontinuity of the heat flux at the interface (also known as Stefan condition) that applies the energy conservation at the interface, and 3) The Gibbs-Thomson equation that applies the effects of capillary and kinetic effects on the melting temperature at the interface[1]. All these equations are represented as follows:

$$\rho C_P \frac{\partial T}{\partial t} + \nabla . q = 0 \tag{3-1}$$

$$K \frac{\partial T}{\partial n}\bigg|_s - K \frac{\partial T}{\partial n}\bigg|_l = \Delta H \rho V_n \tag{3-2}$$

$$T_i - T_m = d_0 \kappa T_m - \beta V_n T_m \tag{3-3}$$

where ΔH, T, t, ρ, C_p, q, V, V_n, and n respectively are latent heat of fusion the (absolute) local temperature, time, density, heat capacity, heat flux, volume, local growth velocity of the interface, and outer normal to the solid domain. Extension of the sharp-interface model to alloy systems requires the addition of concentration equations into the governing equations.

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[1] At the interface, the local interface temperature T is lower than the equilibrium melting temperature T_m due to the capillary and kinetic effects, which could be expressed by the Gibbs-Thomson relation [83]:
$T_i - T_m = mC_l - d_0 \kappa T_m - \beta V T_m$
First, correction term is based on local concentration. m is the liquidus slope and C_l is the solute concentration in liquid at the interface. The second term considers the effects of capillary forces and the curvature, d_0 is the capillary length, κ is the interface curvature and a positive curvature corresponds to a fingerlike solid projection growing into the liquid. Due to effects of this term the melting temperature is lower at curved interfaces compared to flat ones [82]. The last term $\beta V_n T_m$ applied the kinetic effects. β is the interface kinetics and V_n is the local growth velocity of the interface.

The implementation of the governing equations to the process of solidification of a pure material is presented briefly to further elaborate the mathematical procedure. A one-dimensional system composed of liquid and solid phases is considered. The interface of the two phases is considered to be flat. Therefore, the equilibrium temperature at the interface is equal to the melting temperature of the pure material (which is dependent on the pressure of the system). For a one-dimensional system with temperature gradient and heat flux, equation (3-1) transforms to [84]:

$$\frac{d}{dt}\int_V \rho C_P T\, dV = -\int_{\partial V} \nabla . q dV \tag{3-4}$$

where q is heat flux. Using the concept of material derivative (3-5), the equation (3-4) transforms to:

$$\frac{d}{\mathrm{dt}} = \frac{\partial}{\partial t} + v.\nabla. \tag{3-5}$$

$$\int_V [\frac{\partial}{\partial t}(\rho C_P T) + \nabla.(V_n \rho C_P)]\, dV = -\int_V \nabla . q \mathrm{dV} \tag{3-6}$$

Considering the differential form

$$\frac{\partial}{\partial t}(\rho C_P T) + \nabla.(V_n \rho C_P) = -\nabla . q \tag{3-7}$$

Developing the heat flux based on temperature gradient, transforms equation (3-7) to:

$$\frac{\partial}{\partial t}(\rho C_P T) + \rho C_P T \nabla . V_n = -\nabla.(K \nabla T) \tag{3-8}$$

where K is the heat conductivity of the material. Considering constant ρ, C_p, and K, the heat balance equation changes to standard heat conduction equation. As mentioned above the melting temperature in case of planar interfaces is the same at liquid and solid phases.

$$T_s = T_l = T_m \tag{3-9}$$

Considering the V_n as an input parameter, the system condition can be obtained from numerical solution of equations (3-8) and (3-2) at each time step. At the end of each time step, the shape of the interface should be analyzed to define the melting temperature at the interface based on Gibbs-Thomson equation.

The main challenge in the sharp-interface model is the continuous change in the shape of the interface and its effects on implementation of boundary conditions. The complicated interface shapes, such as cellular and dendritic patterns, require more grid points and finer mesh in numerical formulation to be able to locate the interface location. Also, this necessitates a higher processing power and increases the computational costs.

Phase field method

The phase field method was introduced to overcome the challenges in the application of sharp interface models. It enables modeling microstructure evolution through numerical calculations. In this section, the fundamentals and applications of this method in different phase transition cases are explained.

Material microstructure has significant effects on its physical and mechanical properties. During a process, such as solidification or phase transformation, the microstructure of materials evolves to reduce the total free energy of the system. The study of microstructure and its evolution provides the knowledge to understand and predict material behavior under different loading conditions. Additionally, it reveals the effects of different process parameters on the final microstructure. The need for this study is more serious for materials with complicated microstructures, such as TLPS

joints[1]. During the last two decades, the phase-field method has shown a great potential in the modeling of various types of microstructure evolution. The main advantage of the phase field method over the conventional sharp interface method is its independence from explicit tracking of the moving interface.

In the phase field method, a phase field variable (also, known as order parameter) ϕ, is introduced to continuously represent the state of the entire microstructure. The phase field variable is a function of time and position. Thus, it can identify the material phase in each location and time during a microstructure evolution process. For example, in a pure material solidification process, $\phi = 0$, $\phi = 1$, and $0 < \phi < 1$ represent the solid, liquid, and interface, respectively. In contrast to the conventional sharp interface method, the phase field method considers the interface based on a diffuse-interface description, shown in Figure 3-1[86]. Therefore, the heat and solute transport behavior of this variable is governed by the diffuse–interface description developed by Cahn and Hilliard [87]. The temporal microstructure evolution is a nonlinear phenomenon, and it is described by a pair of continuum equations Cahn-Hilliard nonlinear diffusion equation and the Allen-Cahn (time-dependent Ginzburg-Landau) equation [81].

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[1] It also includes spatially distributed phases of different compositions and/or crystal structures, grains of different orientations, domains of different structural variants, domains of different electrical or magnetic polarizations, and structural defects [85]

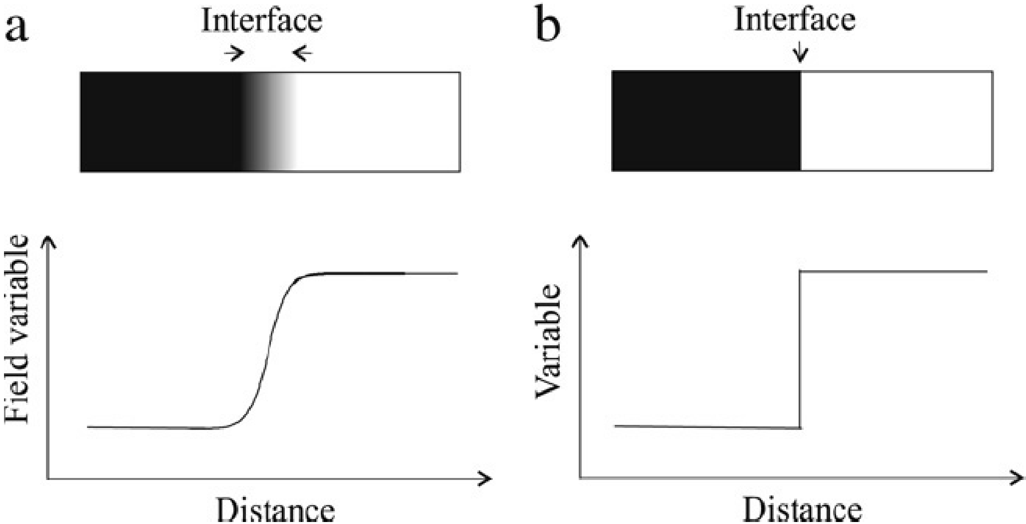


Figure 3-1: (a) Diffuse interface: properties evolve continuously between their equilibrium values in the neighboring phases. (b) Sharp interface: properties are discontinuous at the interface.[86]

Different categories can be classified for phase field models. One method divides the models based on their phase field variable: single scalar and multiple order parameters are two categories of this division. Another method considers the formulation implemented in the modeling, whether it is based on thermodynamic relations or geometrical arguments. In some cases, the methods are divided based on whether they represent a real physical phenomenon or only serve as a computational technique [88]. A simpler method of classification categorizes the phase field models based on the purpose that their phase field variables serve in computation. There are two categories considered in this method of classification. In the first, the phase field variable is only used to avoid tracking of the interface. All the phase field models developed for solidification of a pure material belong to this category. In the second type, the phase field variables are based on well-defined physical order parameters, such as long-range order parameters for order-disorder transformations and the composition fields for

phase separation. These types of models are extensively applied to modeling of solid-state phase transformations [81]. In the next section, the thermodynamic relations considered in derivation of phase field relations are described.

Thermodynamics treatment

The phase field method can be developed based on a few basic concepts of irreversible thermodynamics. The first concept is that the entropy of a conserved system during an irreversible process increases. Now, let's consider a system with conserved internal energy and concentration. It is possible to obtain the fluxes of internal energy and concentration based on thermodynamics relations. The contributing terms in the generalized entropy function are: gradients of energy density, composition, and phase field variable at the interface in addition to terms that relate thermal and compositional driving forces to energy and solute fluxes [89]. The broad form of entropy functional can be considered as follows [89]:

$$S = \int \left[s(e, X, \phi) - \frac{\epsilon_e^2}{2} |\nabla e|^2 - \frac{\epsilon_c^2}{2} |\nabla c|^2 - \frac{\epsilon_\phi^2}{2} |\nabla \phi|^2 \right] dV \tag{3-10}$$

where *s, e, c,* and ϕ, are the entropy density, internal energy density, concentration, and phase field variable, respectively. ϵ_e, ϵ_c, and ϵ_ϕ are the gradient entropy coefficients associated to the internal energy, composition, and phase field. During the solidification process of a pure material, the phase field variable ϕ identifies the liquid and solid phases. In an isothermal case, the enthalpy density can be expressed from the entropy formulation with $\epsilon_e = 0$ as $h = h_0 + C_p T + L\phi$. A formulation for thermal diffusion with a source term from the enthalpy equation as [84]:

$$C_p \frac{\partial T}{\partial t} + L \frac{\partial \phi}{\partial t} = \nabla . (k \nabla T) \tag{3-11}$$

where T, k, C_p and L are temperature, thermal conductivity, heat capacity and latent heat per unit volume, respectively. The relation of latent heat and phase field variable is considered in this equation. Therefore, the changes of the phase field with time near the moving interface are considered in latent heat evolution.

Another approach to phase field modeling is through the total free energy functional of the system. The total free energy of a system with isothermal condition can be represented as follows:

$$F = \int_V [f(\phi, c, T) + \frac{\epsilon_c^2}{2} \mid \nabla c \mid ^2 + \frac{\epsilon_\phi^2}{2} \mid \nabla \phi \mid ^2] \, dV \tag{3-12}$$

where $f(\phi, c, T)$ is the free energy density.

When the system is in equilibrium state, the free energy functional is located at its local minimum. Therefore, the derivative of the free energy functional with respect to phase field variable is equal to zero. On the other hand, the derivative of the free energy functional with respect to concentration should be constant due to conservation of mass through the whole system (concentration is a conserved quantity).

$$\frac{\delta F}{\delta \phi} = \frac{\partial f}{\partial \phi} - \epsilon_\phi^2 \nabla^2 \phi = 0 \tag{3-13}$$

$$\frac{\delta F}{\delta c} = \frac{\partial f}{\partial c} - \epsilon_c^2 \nabla^2 c = cte. \tag{3-14}$$

Now consider an isothermal system which is not in equilibrium state. Based on the principal of minimum energy, it is expected that the system transforms towards the global (or local) minimum free energy states. For conserved variables, such as concentration and chemical potential, the changes occur through fluxes (i.e. diffusive

fluxes driven by conserved parameters gradients). In contrast, the non-conserved field parameters, such as phase field variable, do not require physical fluxes to change the local free energy. The following Allen-Cahn and Cahn-Hilliard equations are simple equations to follow the non-conserved phase field variable and conserved concentration, respectively, in an isothermal system with respect to time [90]:

$$\frac{\partial \phi}{\partial t} = -M_{\phi}[\frac{\partial f}{\partial \phi} - \epsilon_{\phi}^{2}\nabla^{2}\phi] \quad (3\text{-}15)$$

$$\frac{\partial c}{\partial t} = [M_{c}c(c-1)\nabla(\frac{\partial f}{\partial c} - \epsilon_{c}^{2}\nabla^{2}c) \quad (3\text{-}16)$$

The parameters M_{ϕ}, and M_{c} are the interface kinetic, and solute diffusion coefficients, respectively.

Isothermal phase transitions in binary alloys

The two most famous phase field models applied to isothermal phase transition in binary alloys are: WBM model, which is named after Wheeler, Boettinger and McFadden [90]; and KKS model, named after Kim, Kim, and Suzuki [91]. The difference between the two models is in their definition of the free energy density for the interfacial region at equilibrium state [91].

The fundamental assumption in both models is that a system, which is not in equilibrium, relaxes along the fastest path to minimize its free energy. A free energy functional should be considered to define the situation of different phases during the phase transition process. The two models consider different types of functional relationships. This difference is based on the associated cost that is considered in each model to the process of phase transition. The general method in defining the free energy

functional is considering the existence of a double-well potential contributing function, such as:

$$g(\phi) = \phi^2(1-\phi)^2 \tag{3-17}$$

$$f(\phi, T) = W\int_0^{\phi} p(p-1)\left[p - \frac{1}{2} - \beta(T)\right]dp\,; \qquad p(\phi) = \phi^3(10 - 15\phi + 6\phi^2) \tag{3-18}$$

The double-well potential function presents the energy barrier between the two neighboring metastable energy states in a free energy functional. In the case of phase transition or solidification, we can consider $\phi = 0$ and $\phi = 1$ as solid and liquid phases, respectively, and at the interface region phase field variable is $0 < \phi < 1$. The example double-well functions presented above ensure that the derivative of the free energy density is equal to zero when $\phi = 0$ and $\phi = 1$ at all temperatures. Figure 3-2 shows the double-well function employed in the WBM model presented in equation (3-18) with respect to temperature. In all three cases presented in this figure, transformation from one metastable phase (ϕ=*0*) to the other (ϕ=*1*) requires the system to overcome an energy barrier ~ϕ=0.5.

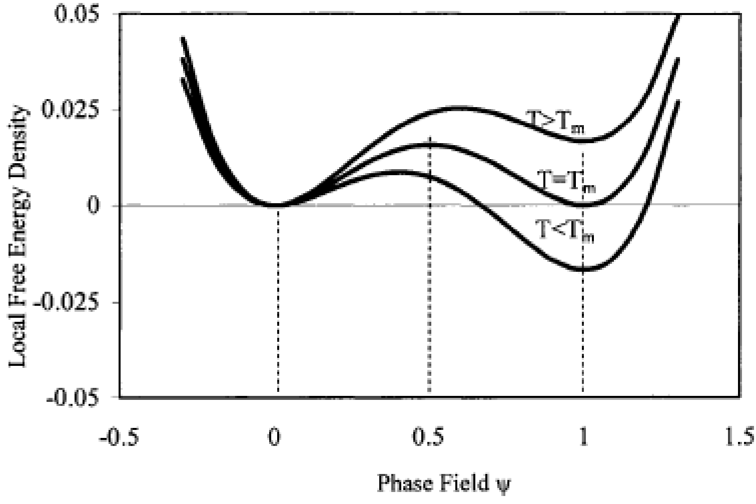


Figure 3-2: The free-energy density f(ϕ,T), employed in WBM model, displayed as a function of ϕ for three values of the temperature near the melting temperature T_M: for $T<T_M$ (β= -0.2), $T=T_M$ (β=0), and $T> T_M$ (β=0.2) [90].

For a binary system consisting of A and B components, the WBM model defines the free energy density for each component as follows [90]:

$$f_A(\phi, T) = W_A \int p(p-1)[p - \frac{1}{2} - \beta_A(T)]\mathrm{dp} \quad (3\text{-}19)$$

$$f_B(\phi, T) = W_B \int p(p-1)[p - \frac{1}{2} - \beta_B(T)]\mathrm{dp} \quad (3\text{-}20)$$

The WBM model selected these types of double-well potential functions developed by Kobayashi (private communications). Additionally, the formulation for evaluating the free energy density of a mixture is employed to apply the effect of concentration and mixing the two components at the interface [90]:

$$f(\phi, c, T) = (1-c)f_A(\phi, T) + cf_B(\phi, T) + \frac{RT}{v_m}[(1-c)ln(1-c) + clnc] \quad (3\text{-}21)$$

where v_m, and W are the molar volume, and the height of energy barrier between two metastable energy states, respectively. β is a shape factor which defines the shape of free energy function with respect to the components' melting temperature $(-0.5 < \beta_A(T) < 0 < \beta_B < 0.5)$. The first two terms correspond to the contribution of molar Helmholtz free energy densities of each component to the energy density. The last term considers the decrease in the free energy of the system to the mixing based on the assumption of ideal solution mixing in all phases.

The governing equations for evolving phase field and concentration stated in the WBM model are:

$$\frac{\partial \phi}{\partial t} = -M_{\phi}\left[\frac{\delta F}{\delta \phi}\right] \quad (3\text{-}22)$$

$$\frac{\partial c}{\partial t} = M_c \nabla \left[c(c-1)\nabla \frac{\delta F}{\delta c}\right] = M_c \nabla . (c(1-c)\frac{\nabla \partial f}{\partial c}) \quad (3\text{-}23)$$

M_{ϕ} and M_c are positive constants. Inserting the equation (3-21) into the defined free energy functional

$$F(\phi, c, T) = \int^{V} [f(\phi, c, T) + \frac{\epsilon^2}{2} \mid \nabla\phi \mid {}^2]\mathrm{dV} \quad (3\text{-}24)$$

equations (3-22) and (3-23) transform to:

$$\frac{\partial \phi}{\partial t} = M_{\phi}\left(\epsilon^2 \nabla^2 \phi - \frac{\partial f}{\partial \phi}\right) = M_{\phi}[\epsilon^2 \nabla^2 \phi - (c\frac{\partial f_B}{\partial \phi} + (1-c)\frac{\partial f_A}{\partial \phi})] \quad (3\text{-}25)$$

$$\frac{\partial c}{\partial t} = M_c \nabla . (c(1-c)\frac{\nabla \partial f}{\partial c}) = M_c \nabla . [c(1-c)\nabla(f_B - f_A)] + D\nabla^2 c \quad (3\text{-}26)$$

It is critical to identify the relationship of the WBM parameters to the materials' physical properties to obtain the ability to model and predict microstructure evolution. The following relations are considered to determine these parameters for the solidification of a pure material (A) by relating them to common sharp-interface parameters.

First, the difference in free energy of solid and liquid phases of component A at temperature T near its melting temperature can be defined based on the latent heat of fusion L_A as follows:

$$f_A(1, T) - f_A(0, T) = \frac{L_A(T - T_M^A)}{T_M^A} \quad (3\text{-}27)$$

$f_A(1, T)$: free energy of component A in liquid phase ($\phi = 1$)

$f_A(0, T)$: free energy of component A in solid phase ($\phi = 0$)

Evaluating the free energy of component A in liquid and solid phases from WBM equation (3-19) results in:

$$f_A(1,T) - f_A(0,T) = \frac{W_A \beta_A(T)}{6} \tag{3-28}$$

Hence,

$$\frac{W_A \beta_A(T)}{6} = \frac{L_A(T - T_M^A)}{T_M^A} \tag{3-29}$$

Next, the interfacial energy of the system (in the WBM model) at the interfacial region is obtained from the definition of the interfacial energy as:

$$\sigma_A = \epsilon\sqrt{2}\int_0^1 \sqrt{f_A(\phi,T)}\,d\phi \tag{3-30}$$

Evaluation of this integral at the melting temperature of material A using equation (3-19) yields:

$$\sigma_A = \epsilon \frac{\sqrt{W_A}}{6\sqrt{2}} \tag{3-31}$$

Another relation that is considered in the WBM model is the interface velocity. This parameter can be identified from common relations used in sharp-interface theories as

$$V_n = \mu_A(T_M^A - A) \tag{3-32}$$

μ_A is the linear kinetic coefficient of material A at the interface. This equation will be used in future to define M_ϕ.

In equilibrium, the one-dimensional solution for the uniform motion of a planar diffuse interface (with velocity V_n) of a pure material exists at the melting point of component A in a transition zone between liquid and solid can be obtained as [90]:

$$\phi(x) = \left[1 + \exp(x\sqrt{\frac{W_A}{2\epsilon^2}})\right]^{-1} \tag{3-33}$$

This solution exists when

$$V_n = -M_\phi \epsilon \beta_A(T)\sqrt{2W_A} \tag{3-34}$$

Relating equations (3-22) and (3-34):

$$M_1 = \frac{\mu_A T_M^A}{6L_A\delta_A} \tag{3-35}$$

The thickness of the interface region is extracted from the form of solution (3-33), from the Allen and Cahn [92] as

$$\delta_A = \epsilon\sqrt{\frac{2}{W_A}} \tag{3-36}$$

The WBM model needs either the height of the energy barrier in the double-well potential function (W_A) at the melting point of material A or the interface thickness (δ_A) to calculate the values for all parameters. Here, all the WBM parameters are presented as a function of interface thickness [90]:

$$\epsilon^2 = 6\sigma_A\delta_A \tag{3-37}$$

$$W_A = 12\frac{\sigma_A}{\delta_A} \tag{3-38}$$

$$M_1 = \frac{\mu_A T_M^A}{6L_A\delta_A} \tag{3-39}$$

$$\beta_A(T) = (\frac{L_A\delta_A}{2\sigma_A})(\frac{T - T_M^A}{T_M^A}) \tag{3-40}$$

Wheeler $et\ al.$ [90] claimed that whatever choice is considered for the interface thickness, the resulting values for ϵ, W_A, M_1, and $\beta_A(T)$ will provide a model that has

the required parameters to match the results from the classical theory [90]. Additionally, two restrictions were considered to extend the case from a pure material to a binary-alloy material. These restrictions were applied to extract single values of ϵ and M_ϕ from equations developed based on each of the components A and B. Another approach is to consider ϵ and M_ϕ functions of the composition and relate the system of equations based on that.

$$\frac{\delta_A}{\delta_B} = \frac{\sigma_B}{\sigma_A} \tag{3-41}$$

$$\frac{\mu_A}{\mu_B} = \frac{\delta_A}{\delta_B}\frac{L_A}{L_B}\frac{L_A}{L_B}\frac{T_M^B}{T_M^A} \tag{3-42}$$

Kim $et\ al.$ [91] introduced another approach to model binary alloys. In their model, the free density function of each component in the alloy is defined as follows [91]:

$$\begin{gathered} f[H(T),\phi] = h(\phi)f^s[H_s(T_s)] + [1-h(\phi)]f^L[H_L(T_L)] + Wg(\phi) \\ \phi = 1 \rightarrow Solid\ phase \\ \phi = 0 \rightarrow Liquid\ phase \end{gathered} \tag{3-43}$$

T_s and $T_L$are temperatures, and $H_s(T_s)$ and $H_L(T_L)$ are enthalpies of solid and liquid, respectively. $g(\phi)$ is the double-well potential function defined in equation (3-17), and $h(\phi)$ is a monotonously changing function from $h(0)$ to $h(1)$. Also, it is assumed that solid and liquid phases have the same temperature at the interfacial region.

$$h(\phi) = \phi^3(6\phi^2 - 15\phi + 10) \tag{3-44}$$

$$T_s(x,t) = T_L(x,t) \equiv T(x,t) \tag{3-45}$$

Relating temperature and enthalpy and matching sharp interface models to the current relations, the composition and phase field evolution developed in the KKS model with respect to time as

$$c_t = \nabla . \frac{D(\phi)}{f_{cc}} \nabla f_c \tag{3-46}$$

$$\phi_t = M(\epsilon^2 \nabla^2 \phi - f_\phi) \tag{3-47}$$

where $D(\phi)$ is the diffusivity dependent of the phase field and composition c is defined in (3-48). The f_{cc} is added to guarantee constant diffusivities in both the bulk solid and liquid.

$$c = h(\phi)c_s + [1 - h(\phi)]c_L \tag{3-48}$$

where c_s and c_L are the composions of the solid and liquid, respectively, at a certain infinitesimal point which is assumed to be a mixture of solid and liquid phases (in the interfacial region).

The free energy density function (3-43) should be revised in terms of phased field variable and composition.

$$f[c,\phi] = h(\phi)f^s[c_s] + [1 - h(\phi)]f^L[c_L] + Wg(\phi) \tag{3-49}$$

The diffusion (3-48) and phased field equations (3-49) are similar to the WBM defining equations. The difference between the two models is that the WBM assumes same composition (3-50) and different chemical potential for the liquid and solid components in the interfacial region while the KKS model considers different composition and same chemical potential for the phases (3-51). This difference in interfacial region conditions is justified based on the definition of interfacial region in the phase field model. The KKS technically considers the interfacial region as a mathematical concept and does not regard it as a real physical entity. Thus, it does not matter that the assumptions are physically reasonable as long as they are mathematically correct and powerful in the interpretation of the system. Also, considering the definition of c_s and c_L in equation

(3-48), the condition of equal chemical potential does not imply constant chemical potential in across the interfacial region except at the thermodynamic equilibrium state.

$$c_S = c_L = c \tag{3-50}$$

$$f_{c_s}[c_s(x,t)] = f_{c_L}[c_L(x,t)] = f_c \tag{3-51}$$

Considering the above relations and conditions, the explicit forms of diffusion and phase field models can be expressed as

$$\frac{\partial \phi}{\partial t} = M\nabla.\epsilon^2\nabla\phi + h'(\phi)[f^L(c_L) - f^s(c_s)] - (c_L - c_s)f^L_{c_L}(c_L)] - \mathrm{Wg}'(\phi) \tag{3-52}$$

$$\frac{\partial c}{\partial t} = \nabla[\frac{D(\phi)}{f_{\mathrm{cc}}}\nabla f^L_{c_L}(c_L)] \tag{3-53}$$

The solution of above equations in equilibrium condition for a one dimensional stationary system is presented as follows

$$\phi_0(x) = \frac{1}{2}[1 - \tanh(\frac{\sqrt{W}}{\sqrt{2\epsilon}}x)] \tag{3-54}$$

Using a similar procedure as the WBM model, the phase field parameters can be obtained as

$$\sigma = \frac{\epsilon\sqrt{W}}{3\sqrt{2}} \tag{3-55}$$

$$2\lambda = \alpha\sqrt{2}\frac{\epsilon}{\sqrt{W}} \tag{3-56}$$

where λ is half of the interface thickness and α is a constant dependent on the definition of the interface thickness, e.g. $\alpha \simeq 2.2$ when ϕ_0 changes from 01. to 0.9 at $-\lambda < x < \lambda$. The parameter relationships (3-55) and (3-56) are the same as those in the phase field model for a pure material.

The main difference between the KKS and WBM models is in the definition of the free energy density for the interfacial region. The WBM model, an extra double-well potential, is considered in addition to the main double-well potential function, *i.e.*$Wg(\phi)$. This extra potential is hidden in the definition of the free energy density function. In the WBM model, any point within the interfacial region is considered as a mixture of solid and liquid in equilibrium with the same composition, $c_0^*(x)$. Therefore, this composition locates between equilibrium composition of liquid (c_L^e) and solid $c_S^e(x)$ phases across the interface, Figure 3-3. The WBM free energy density, e.g. $h(\phi)f^S(c_0^*) + [1 - h(\phi)]f^L(c_0^*)$, lies on the dotted line curve in Figure 3-3 and the extra potential is shown as $\overline{PQ}$. This extra potential is negligible either at the sharp interface limit where $W \rightarrow \infty$ or in alloy with a very small difference between c_S^e and c_L^e where $\overline{PQ}$ is very small. In contrast, the extra potential will be a significant factor with increasing the interface thickness or increasing the difference between c_S^e and c_L^e and cannot be neglected [91].

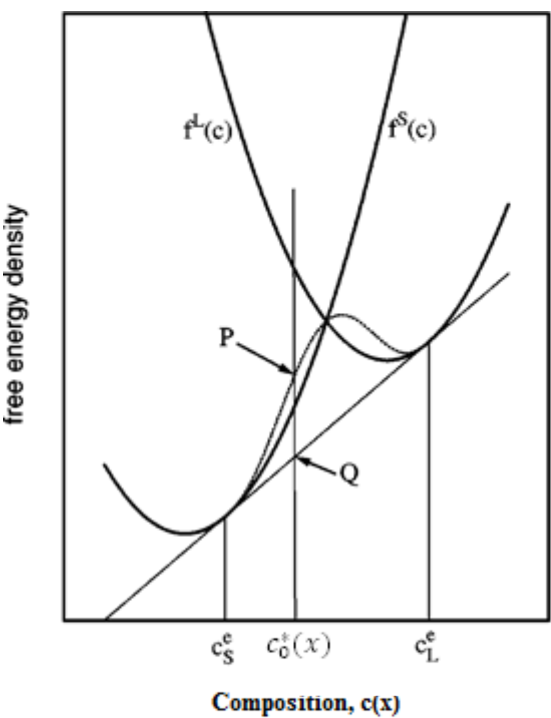


Figure 3-3: Free energy density curves of solid and liquid phases with respect to composition [91]

The rest of this chapter is dedicated to expanding the KKS method to multiphase filed problems such as eutectic solidification. In the last chapter, a modification to KKS method will be proposed to increase its accuracy and facilitate its application in multiphase solidification problems.

Multiphase field models

The WBM and KKS were developed to study phase transition in binary alloys, e.g. systems involving only two distinct phases. A multiphase field approach is required to consider more generalized systems involving more than two phases. Steinbach *et al.* [93] derived a multiphase field method based on interface fields concept. This method can analyze systems involving several phases in global non-equilibrium condition. This

method is based on the assumption that local scale pairwise interactions between two phases are near thermodynamic equilibrium [94].

In two-phase models, only one phase field variable ϕ was enough to identify the existence of each phase at different locations and times in the system. For example, in the KKS model, ϕ is considered to be equal to 0 and 1 at liquid and solid phases, respectively. A value between 0 and 1 indicates the mixture of these two phases. The closer this value to 0 or 1 shows the larger concentration of liquid or solid phases, respectively. Steinbach method uses similar definition of phase field variable in its model. Here, the standard definition of phase field variable in Steinbach method is presented to clarify how it evolves in a multiphase system: a phase field parameter (or order parameter) ϕ represents a property of the system that is non-zero in a distinct region of the phase space and zero otherwise [94]. Based on this definition, the phase field variable can be obtained as the distinction between two phases instead of only relating to one single phase. Considering a system involving three phases (e.g. $\alpha, \beta, and\ L$), phase α may transform into phase L, or phase L may transform into phase β. Therefore, a region (or position) consisting of two or three coexisting phases can be considered in the system. Steinbach method defines a set of phase field variables ($\phi_i: i = 1, \dots, N;\ N = Number\ of\ phases$) with property $0 \leq \phi_i \leq 1$. Also, it considers constraint (3-57) to relate all these phase field variables at a point at which different phases coexist.

$$\sum_{i=1}^{n} \phi_i = 1 \tag{3-57}$$

The free energy functional F of the system is defined as [94]

$$F[\phi_1, \phi_2, \phi_3, .., \nabla\phi_1, \nabla\phi_2, \nabla\phi_3, ..] = \int_V f[\phi_1, \phi_2, \phi_3, .., \nabla\phi_1, \nabla\phi_2, \nabla\phi_3, ..] \quad (3\text{-}58)$$

where f is the local free energy density function. The free energy density function for a multiphase system defined as [94]

$$f = f^0 + \sum_i f_i^1 + \sum_{i,j(i\neq j)} f_{\text{ij}}^2 + \sum_{i,j,k(i\neq j\neq k)} f_{\text{ijk}}^3 + \ldots \quad (3\text{-}59)$$

f^0 is the part of the free energy that is independent of the phase state; f_i^1 contains the energy difference of the bulk phases; f_{ij}^2 is the energy part that is sensitive on the boundary between phases i, j; similarly f_{ijk}^3 considers the contributions of triple point energies. Thus, this definition considers the free energy of each single phase, regions including two and three phases and so on.

The transition of ϕ_i with time toward the minimum of the free energy function can be obtained using relaxation ansatz [93]

$$\frac{\partial\phi_i}{\partial t} = (\nabla \frac{\nabla\partial}{\partial\nabla\phi_i} - \frac{\partial}{\partial\phi_i}) f(\phi_i) \quad (3\text{-}60)$$

$$\frac{\partial\phi_i}{\partial t} = -M_{\text{ij}} \frac{1}{N_p} \sum_{i\neq j} (\frac{\partial}{\partial\phi_i} - \frac{\partial}{\partial\phi_j}) F \quad (3\text{-}61)$$

where M_{ij} is the mobility. N_p is the number of coexisting phases.

Multiphase field modeling method provides the capability to consider systems involving one liquid and one or more solid phases, cases such as eutectic or peritectic solidification. For this purpose one phase field parameter will be considered for each phase. This variable is non zero when its related phase exists at a considered position.

Up to this point, phase field modeling defined a new description for the interface region and also, introduced phase field parameters to follow phase transitions at various locations with respect to time. Furthermore, Steinbach approach facilitates phase field modeling of multiphase systems and solves more sophisticated physics and thermodynamics problems. Yet, the phase field approaches alone cannot describe complicated situations such as eutectic solidification without considering the other fundamental existing relations, such as diffusion equation.

In binary and eutectic alloy solidification, the composition of each phase at different times and locations is monitored and related to the phase field variables. At interfaces the average composition of the mixture with respect to the fraction of constituent phases (mixture rule):

$$c(x,t) = \sum_{i} \phi_i c_i \tag{3-62}$$

Consider the mixture rule and WBM (3-50) or KKS (3-51) composition assumption at the interface along with Steinbach pairwise equilibrium relations; the composition c_i $(i = 1,2,3,..)$ of each phase can be defined as a function of c and ϕ_i.

Now, considering the Steinbach method for a generalized multiphase field model, Kim *et al.* [95] derived the conventional multiphase model for solidification of a eutectic system as:

$$\frac{\partial \phi_i}{\partial t} = \frac{-2}{N_p} \sum_{i \neq j} M_{\mathrm{ij}} \chi_i \chi_j \left(\frac{\partial F}{\partial \phi_i} - \frac{\partial F}{\partial \phi_j}\right) \tag{3-63}$$

where

$$\frac{\partial F}{\partial \phi_i} = \sum_{i \neq j} [\frac{\epsilon_{\text{ij}}^2}{2} \nabla^2 \phi_j + \omega_{\text{ij}} \phi_j] + f^i(c_i) - f_c c_i \tag{3-64}$$

ϵ and ω are the gradient energy coefficient and the height of double-well potential.

Inserting (3-64) into (3-63) results in [84]:

$$\frac{\partial \phi_i}{\partial t} = \frac{-2}{N_p} \sum_{j \neq i}^{N} \chi_i \chi_j M_{\text{ij}} \left\{ \frac{\epsilon_{ij}^2}{2} \left(\nabla^2 \phi_j - \nabla^2 \phi_i \right) + \omega_{\text{ij}} \left(\phi_j - \phi_i \right) \right.$$
$$+ \sum_{k \neq i,j}^{N} \left[\left(\frac{\epsilon_{ik}^2}{2} - \frac{\epsilon_{jk}^2}{2} \right) \nabla^2 \phi_k + \left(\omega_{\text{ik}} - \omega_{\text{jk}} \right) \phi_k \right] \tag{3-65}$$
$$\left. + \left[(f_i - c_i f') - \left(f_j - c_j f' \right) \right] \right\}$$

Similar to binary alloys, the conditions of equal chemical potential (the KKS model) or equal composition (the WBM model) can be applied to multiphase systems in the interfacial regions.

Applying the composition relation (3-62) to Cahn-Hilliard equation while considering the KKS assumption, the diffusion equation will be defined as:

$$\frac{\partial c}{\partial t} = \nabla . D \sum_{i} \phi_i \nabla c_i \tag{3-66}$$

Multiphase field modeling of Cu-Sn transient liquid phase sintering

Multiphase field model (PFM) is a very powerful method capable of modeling the microstructure evolution during eutectic solidification. This characteristic facilitates design and modeling of TLPS joints. Park and Arroyave simulated eutectic soldering of lead-free (Cu-Sn solders) and layer-wise transient liquid phase diffusion bonding of Cu/Sn/Cu layers [96], [97]. They used CALPHAD method to define the free energy

density function for Cu, Sn, and Cu-Sn IMCs (Cu_6Sn_5 and Cu_3Sn) at T=324°C. More generally, the free energy density functions of the α-phase solid, liquid tin, and Cu_6Sn_5 can be calculated from thermodynamic assessment of Cu-Sn with respect to composition and temperature (CALPHAD) [98]:

$$\mathrm{G}\alpha = (1 - c_{Sn})G_{\mathrm{Cusern}} + c_{Sn}G_{\mathrm{Snfcc}} + RT((1 - c_{Sn})\mathrm{Log}[1 - c_{Sn}] + c_{Sn}\mathrm{Log}[c_{Sn}]) + \overset{\alpha\mathrm{pex}}{G}[c_{Sn}]; \tag{3-67}$$

$$\mathrm{G}_{liq}[c_{Sn}] = (1 - c_{Sn})\, G_{\mathrm{Culiq}} + c_{Sn}G_{\mathrm{Snliq}} + RT((1 - c_{Sn})\mathrm{Log}[c_{Sn}] + c_{Sn}\mathrm{Log}[c_{Sn}]) + \mathrm{G}_{liqPEX}[c_{Sn}]; \tag{3-68}$$

$$\mathrm{G}\eta[c_{Sn}] = 2 * 10^5 * (c_{Sn} - 0.435)^2 + .545G_{\mathrm{Cusern}} + 0.455G_{\mathrm{Snsern}} - 6869.5 - 0.1589T; \tag{3-69}$$

where

$$\overset{\alpha\mathrm{pex}}{G}[c_{Sn}] = (1 - c_{Sn})c_{Sn}\left[\overset{0}{\mathrm{L}}\alpha_{\mathrm{CuSn}} + \overset{1}{\mathrm{L}}\alpha_{\mathrm{CuSn}}(1 - 2c_{Sn}) + \overset{2}{\mathrm{L}}\alpha_{\mathrm{CuSn}}(1 - 2c_{Sn})^2\right] \tag{3-70}$$

$$G_{\mathrm{Culiq}} = 5194.277 + 120.973331T - 24.112392T\mathrm{Log}[T] - 2.65684\times10^{-3}T^2 + 0.129223\times10^{-6}T^3 + 52478T^{-1} + 5.849\times10^{-21}T^7; \tag{3-71}$$

$$G_{\mathrm{Snliq}} = 9496.31 - 9.809114T - 8.2590486T\mathrm{Log}[T] - 16.814429\times10^{-3}T^2 + 2.623131\times10^{-6}T^3 - 1081244T^{-1}; \tag{3-72}$$

$$\overset{0}{\mathrm{L}}_{l_{\mathrm{CuSn}}} = -9002.8 - 5.8381T; \tag{3-73}$$

$$\overset{1}{\mathrm{L}}_{l_{\mathrm{CuSn}}} = -20100.4 + 3.6366T;$$

$$\overset{2}{L}_{l_{\mathrm{CuSn}}} = -10528.4;$$

$$\mathrm{G}_{liqPEX}[c_{Sn}] = (1 - c_{Sn})c_{Sn}\{\overset{0}{\mathrm{L}}_{l_{\mathrm{CuSn}}} + \overset{1}{\mathrm{L}}_{l_{\mathrm{CuSn}}}(1 - 2c_{Sn}) + \overset{2}{\mathrm{L}}_{l_{\mathrm{CuSn}}}(1 - 2\,c_{Sn})^2\}; \tag{3-74}$$

Considering the above equations, the free energy density function of the solid, liquid and Cu_6Sn_5 IMC per unit molar volume can be plotted with respect to c_{Sn}concentration, Figure 3-4. Uniform molar volume of 16.20 (cm^3/mole) is considered for all phases. The equilibrium phase compositions of IMC and each of solid and liquid phases can be defined as: $c_\eta^{\alpha\eta} = 0.380$, $c_\alpha^{\alpha\eta} = 0.1954$, , $c_\eta^{\eta L} = 0.441$, $c_L^{\eta L} = 0.9768$; where : c_a^{ab} is the composition of a phase at $a - b$ interface.

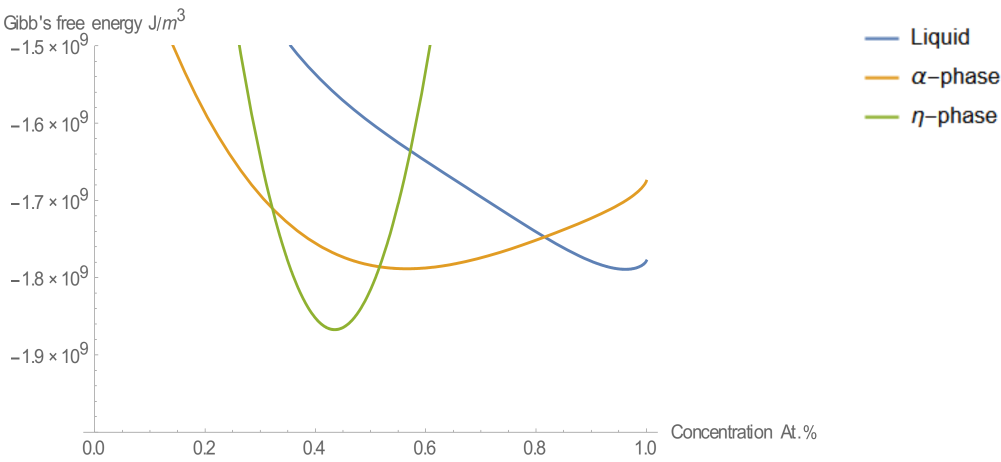


Figure 3-4: Gibb's free energy of Cu-Sn interface at 324°C consists of: 1. Sn (liquid phase) 2. α-phase (Solid) 3. η-phase (Cu_6Sn_5 IMC)

Modified phase-field model

In eutectic solidification, the KKS method is a very powerful approach to determine the interface condition and evaluate the composition of each constituent based equal

chemical potential condition. This solves the inherent extra potential issue of the WBM method. The KKS method solves the Cahn-Hilliard (3-13) equation at each pairwise interface and finds the phase parameters of the constituents. These values will then be used in coupled chemical potential condition (3-51) and Allen-Cahn (3-14) equation to find each constituent's composition. This clearly defines the situation of each material at the interface. However, the equal chemical potential condition is not an easy condition to satisfy at all times. Furthermore, in a time-dependent numerical solution, detailed analysis of KKS results is required at each time-step to assure its compliance with the physics of the problem. In eutectic solidification of Cu-Sn, sometimes this condition results in compositions outside the region between the equal points of pure materials.

A new assumption was made to overcome this issue with a more compliant method with physics of the interface region. This method provides acceptable values for constituents' compositions, while considering double-well potential behavior of the interface ingredients. The main assumption in this method is that the constituents' composition at non-equilibrium stay at close vicinity of equilibrium points in free energy density curves. This prevents sudden jumps in compositions of interface materials from one time-step to the other problems with a material which has a narrow free energy density function. In most cases, this assumption acts very similarly to considering similar chemical potential for the constituents during the non-equilibrium state (KKS method), while covering the limitations of KKS method.

In this modified version of PFM, the non-equilibrium composition of each material at the interface region is considered as follows:

$$c_i = c_i^{eq} + \beta_i \textit{where i=1,2,3,..,n (n: number of phases at the interface)} \quad (3\text{-}75)$$

Therefore, equation (3-62) transforms to:

$$c(x,t) = \sum_i \phi_i c_i + \sum_i \phi_i \left(c_i^{eq} + \beta_i\right) \quad (3\text{-}76)$$

The non-equilibrium compositions are selected in close neighborhood of the equilibrium points. Thus, the following condition is applied to minimize the summation of β_i for different constituents:

$$min\,\{g(\beta_1, \beta_2, \dots)\} = \beta_1^2 + \beta_2^2 + \cdots \quad (3\text{-}77)$$

The above assumption changes the fundamental KKS equations (3-64) and (3-65) defined to determine the non-conserved variable (phase parameter) with respect to time based on Allen-Cahn equation. Therefore, it is necessary to establish the Allen-Cahn equation based on the new composition condition at the interface.

Let's start with the conditional Steinbach free energy functional (3-78) [93] and consider the relaxation ansatz (3-61) and composition condition (3-79):

$$F = \int_V [f^P + f^T + \lambda_L(\Sigma\phi_i - 1)]\mathrm{dV} \quad (3\text{-}80)$$

$$\frac{\delta F^P}{\delta \phi_i} = \sum_{i \neq j} [\frac{\epsilon_{\mathrm{ij}}^2}{2} \nabla^2 \phi_j + \omega_{\mathrm{ij}} \phi_j] \quad (3\text{-}81)$$

$$\frac{\delta F^T}{\delta \phi_i} = f^i(c_i) + \Sigma_j \phi_j f_{c_j}^j(c_j) \frac{\partial c_j}{\partial \phi_i} = f^i(c_i) + \Sigma_j \phi_j f_{c_j}^j(c_j) \frac{\partial c_j}{\partial \beta_i} \frac{\partial \beta_i}{\partial \phi_i}$$
$$= f^i(c_i) + \Sigma_j \phi_j f_{c_j}^j(c_j) \frac{\partial \beta_i}{\partial \phi_i} \quad (3\text{-}82)$$

The only unknown in the above equation is $\frac{\partial \beta_i}{\partial \phi_i}$ which can easily be defined based on the pairwise interaction of the interface constituent, minimization objective function,

and composition boundary conditions. Following is the pairwise interaction of the interface constituents explained with a binary solidification example.

In a binary solidification problem, at each time step, the phase parameters ϕ_1 and ϕ_2 will be defined based on equation (3-65) and interface mixture c composition from equation (3-83). Now, by considering any of the WBM, KKS, and modified PFM assumptions, it is possible to define each phase's compositions. According to equation (3-62), the composition of interface material consisting of phase 1 and 2 can be defined as:

$$\phi_1 c_1 + \phi_2 c_2 = c \tag{3-84}$$

Where c_1 and c_2 were defined based on equation (3-85). The composition should be a number in range of 0 and 1. This applies an inherent constraint on β_i values:

$$-c_i^{eq} < \beta_i < 1 - c_i^{eq}; i = 1,2 \tag{3-86}$$

β_i values can be defined based on minimization of the following function:

$$min\ g(\beta_1, \beta_2) = \beta_1^2 + \beta_2^2 \tag{3-87}$$

subject to

$$\begin{gathered} 0 < c_1^{eq} + \beta_1 < 1 \\ 0 < c_2^{eq} + \beta_2 < 1 \end{gathered} \tag{3-88}$$

using Lagrange multiplier with constraints optimization methods, the above conditions will be considered as following functions:

$$\begin{gathered} g_1(\beta_1) = 1 - c_{\mathrm{eq}_1} - \beta_1 \\ g_2(\beta_1) = c_{\mathrm{eq}_1} + \beta_1 \\ g_3(\beta_2) = 1 - c_{\mathrm{eq}_2} - \beta_2 \end{gathered} \tag{3-89}$$

$$g_4(\beta_2) = c_{\mathrm{eq}_2} + \beta_2$$

$$g_5(\beta_1, \beta_2) = c - (c_{\mathrm{eq}_1} + \beta_1)\phi_1 - (c_{\mathrm{eq}_2} + \beta_2)\phi_2$$

all of which will be considered in the solution of the following function:

$$g_0 = \beta_1^2 + \beta_2^2 - \lambda_1 g_1(\beta_1) - \lambda_2 g_2(\beta_1) - \lambda_3 g_3(\beta_2) - \lambda_4 g_4(\beta_2) - \lambda_5 g_5(\beta_1, \beta_2) \quad (3\text{-}90)$$

Solving the above equation defines the (β_1, β_2), and moves the solution to the next time step. This method can easily be expanded to multiphase interface interactions.

Experiment procedure

Microevolution of Cu-Sn intermetallic compounds around high-melting points was monitored with respect to sintering duration in a particle-based TLPS process. The samples were prepared by two-step processing. The low pressure during two-step processing (0.3 MPa) decreases the possibility of solid-state sintering and the IMC formation is completely related to liquid-state sintering. The Cu-Sn HMP and LMP pastes were prepared based on the description in the previous chapter. Copper samples with $12\times12\times4\ \mathrm{mm}^3$ and $6.35\times6.35\times4\ \mathrm{mm}^3$ were used as substrate and die. Samples were prepared on an open-air hot plate with 30s, 2, 4, and 30 minutes.

Two-step processing was chosen for this process due to its limited solid-state sintering and extensive liquid-state sintering. Each sample was cross-sectioned and studied under environmental scanning electron microscope (ESEM). Figure 3-5 shows the IMCs formed during two-step TLPS processing after 30s. Most of the joint is large copper particles and considerable unreacted tin. The average copper particle size and thickness of IMC formed during this process is measured by ImageJ, Figure 3-7 and Figure 3-8. At this stage, the IMCs have a uniform smooth fillet shape.

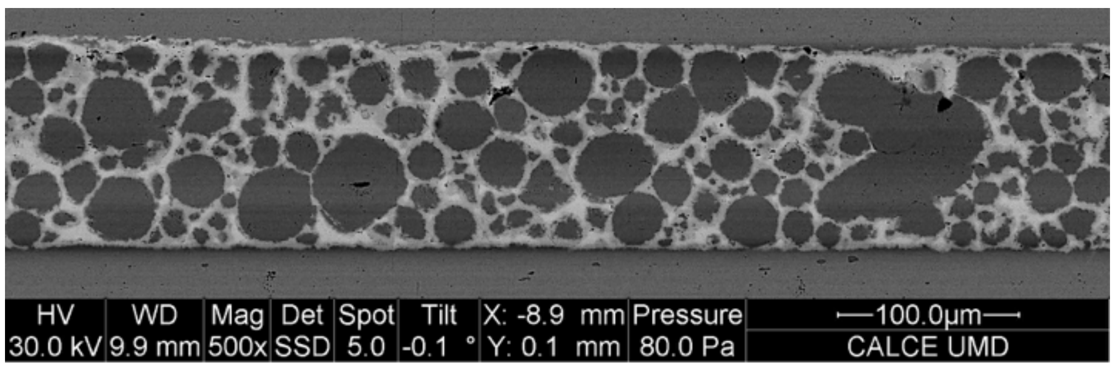


Figure 3-5: ESEM image of Cu-Sn TLPS sintered for 30s

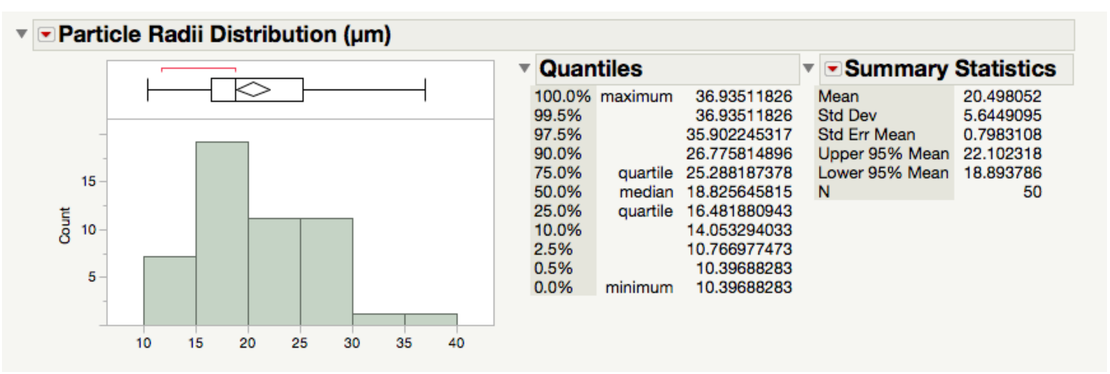


Figure 3-6: Particle radii distribution for particles with radius>10µm shown in Figure 3-5 (sample size: 50 particles)

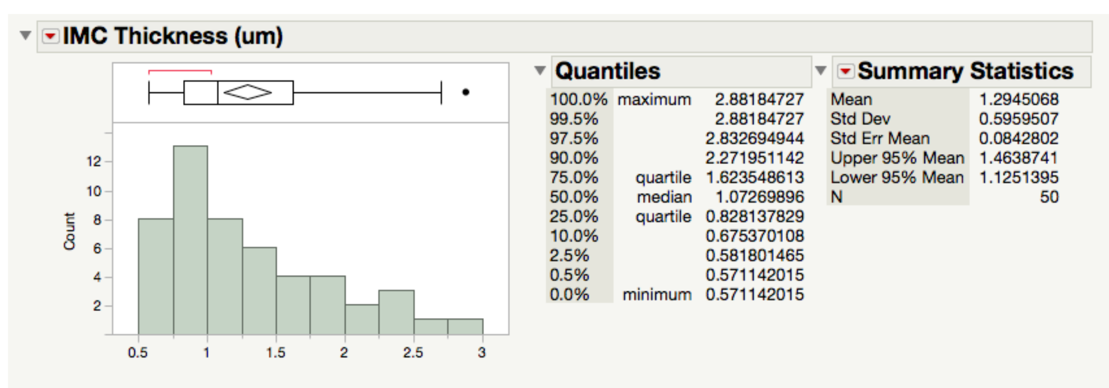


Figure 3-7: Average IMC thickness around the particles shown in Figure 3-5 (sample size: 50 particles)

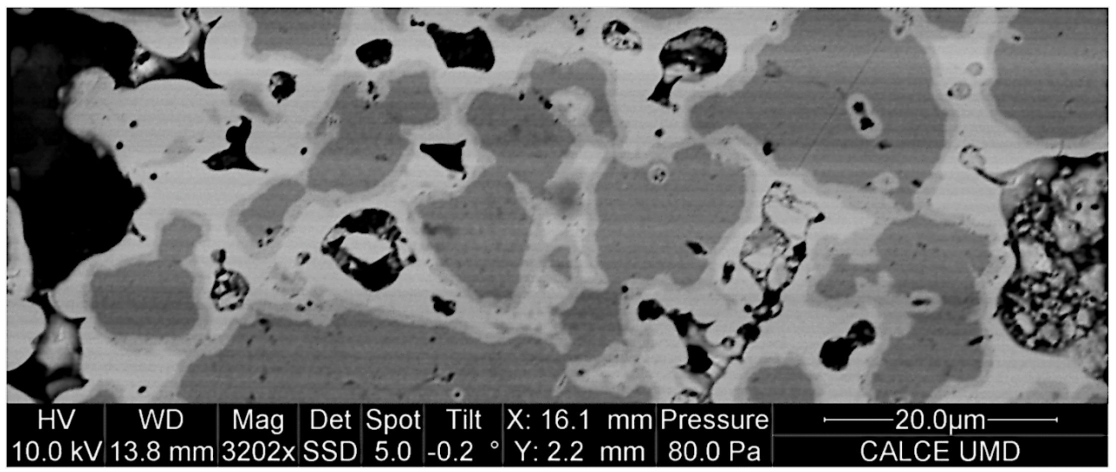


Figure 3-8: Higher magnification image of a copper particle in Cu-Sn TLPS interconnection processed for 30s at the high temperature (300°C)

As time passes the IMCs grow and take scallop-shape after sintering for 2 minutes, Figure 3-9. The IMCs formed around the particles grew faster compared to the ones on the surface of flat copper plates (die and substrates). The average height for IMC scallops is 6.1 µm on copper particles compared to 4 µm on flat surfaces, Figure 3-10. The spherical surface provides more space for IMCs to grow. Therefore, liquid tin could diffuse between them easier and interact with solid copper.

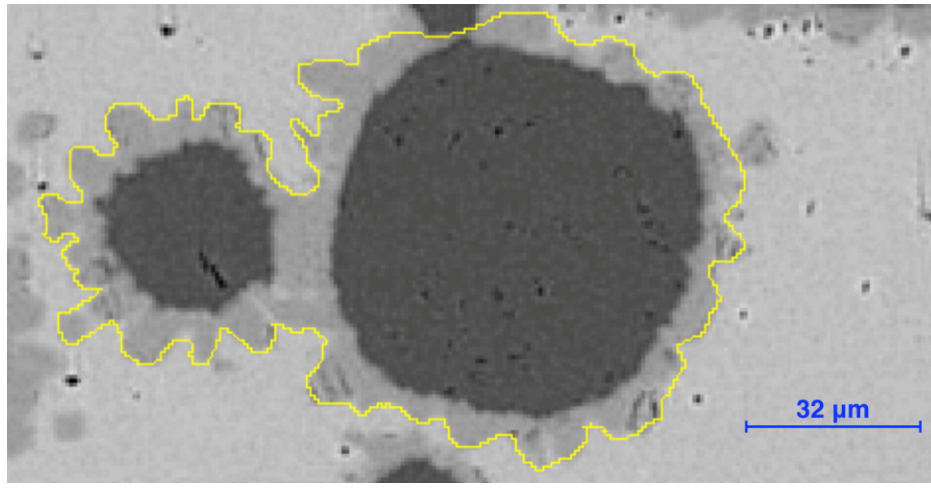


Figure 3-9: IMC growth around copper particles after 2 minutes sintering at 300°C[99]

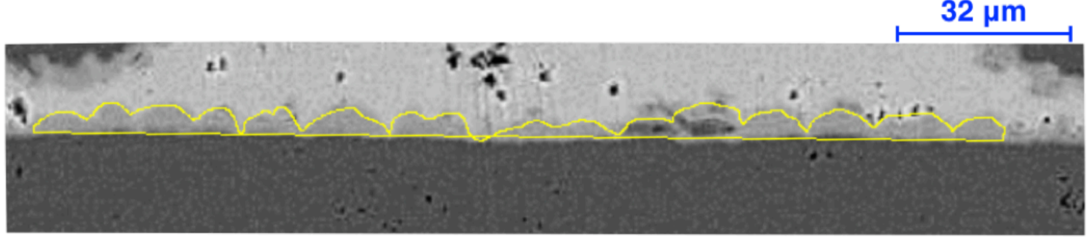
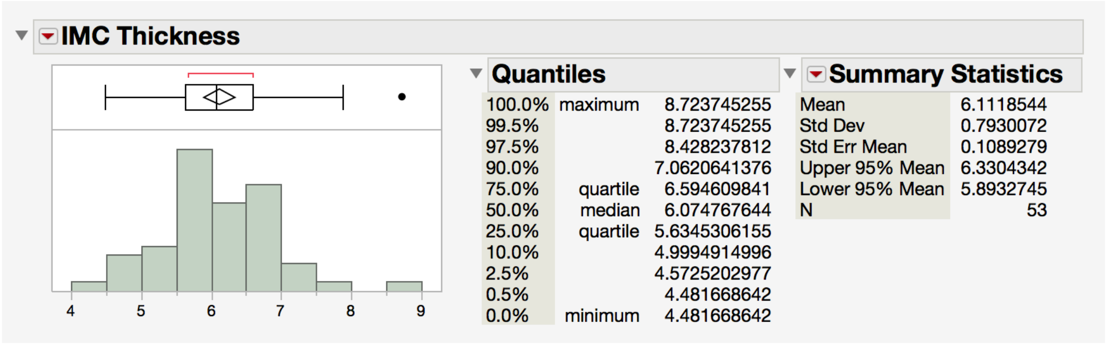


Figure 3-10: IMC growth on copper flat surface after 2 minutes sintering at 300°C



Quantiles

100.0%	maximum	8.723745255
99.5%		8.723745255
97.5%		8.428237812
90.0%		7.0620641376
75.0%	quartile	6.594609841
50.0%	median	6.074767644
25.0%	quartile	5.6345306155
10.0%		4.9994914996
2.5%		4.5725202977
0.5%		4.481668642
0.0%	minimum	4.481668642

Summary Statistics

Mean	6.1118544
Std Dev	0.7930072
Std Err Mean	0.1089279
Upper 95% Mean	6.3304342
Lower 95% Mean	5.8932745
N	53

Figure 3-11: Average IMC thickness around the particles after 2 minutes of sintering at 300°C (sample size: 53 particles)

Increasing the sintering duration to 4 minutes almost covers all the interconnection regions with IMCs, Figure 3-12. Voids and unreacted tin were observed where there were no copper particles. On the right side of the image, the combination of particles with different sizes created a perfect TLPS joint. The copper particles form vertical paths from the top interface to bottom. Since copper particles have better thermal and electrical conductivities, this improves thermal and electrical properties of the joint. However, the left side of the joints lost their functionality due to a redundant number of large particles and lack of small particles to complete the matrix.

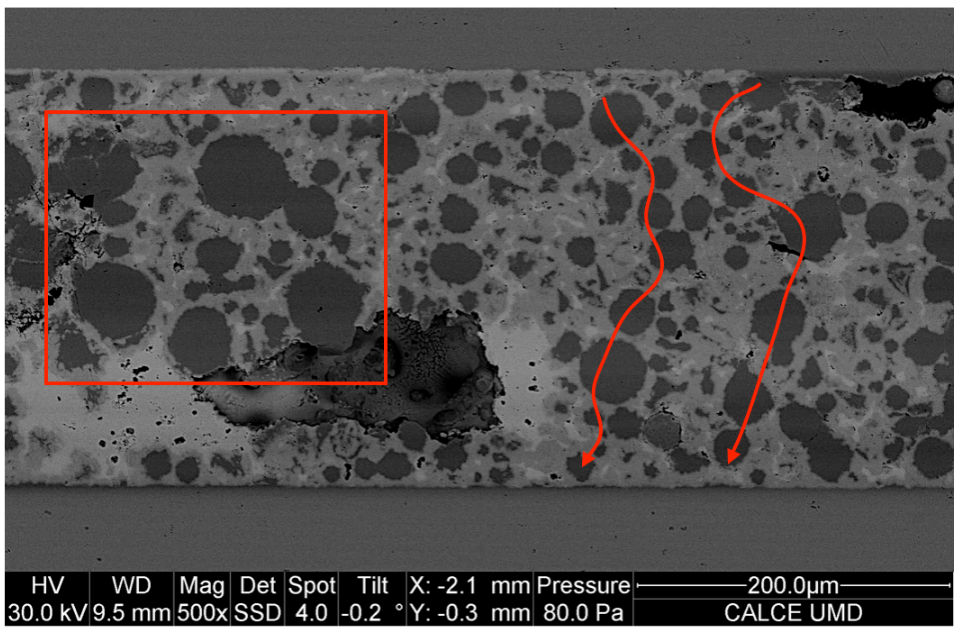


Figure 3-12: ESEM image of Cu-Sn TLPS sintered for 4 minutes at 300°C

After 30 minutes of sintering at 300°C, the joints are almost fully IMC with some copper particles, Figure 3-13. Cu_3Sn starts growing on copper particles at the interface of copper and Cu_6Sn_5. It has a uniform smooth shape and an average thickness of 3.5 μm. Like sintered joints for 2 minutes, the IMC thickness at the particles is larger compared to the ones on the copper die and substrate surfaces; however, the difference is not that considerable, i.e. <1.5 μm.

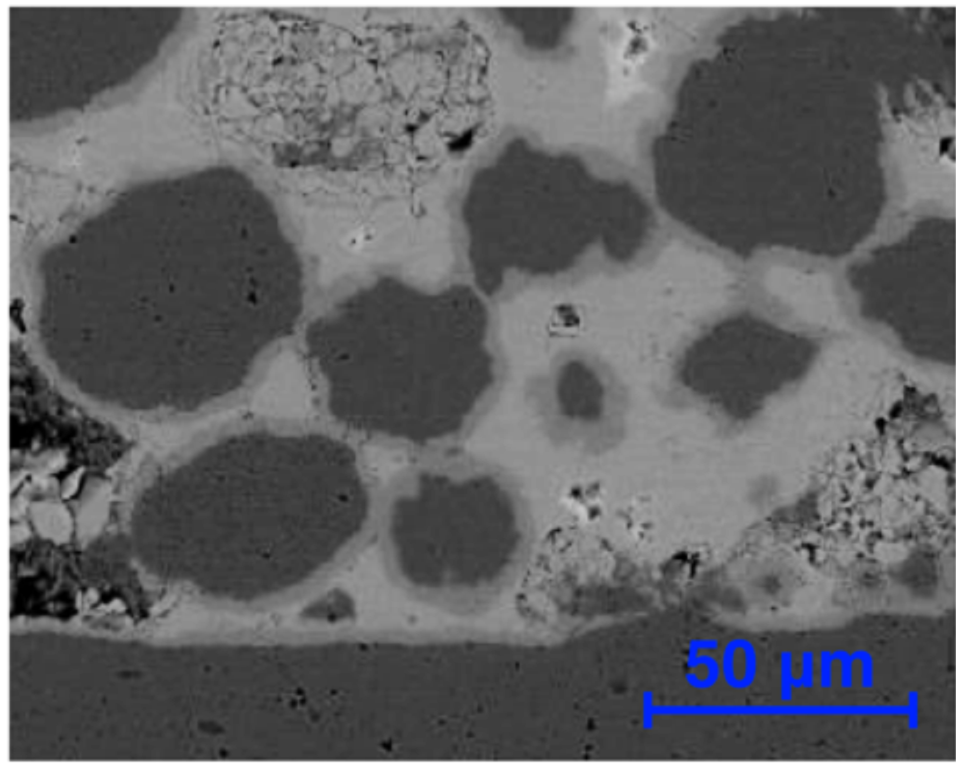


Figure 3-13: ESEM image of Cu-Sn TLPS sintered for 30 minutes at 300°C

Cu-Sn Microstructure evolution modeling:

Cu_6Sn_5 IMC growth during TLPS processing at 300°C was simulated at three different scenarios[1]:

1. IMC growth around a single particle surrounded by liquid tin
2. Two-step processing joint formation
3. One-step processing joint formation

Finite difference was used to solve the PFM equations. Same meshing size in x, y direction was considered to discretize the local equations, 0.25 μm. Time step equal to 0.1 ms was considered to solve the temporal part. The diffusion and phase field evolutions equations will be discretized as follows:

---

[1] information on simulation of PFMs could be found in [100]

$$\frac{c_{ij}^{n+1} - c_{ij}^{n}}{\Delta t} = \nabla^2 M \left(\frac{\delta F_{ij}}{\delta c}\right)^n \tag{3-91}$$

$$\frac{\phi_{ij}^{n+1} - \phi_{ij}^{n}}{\Delta t} = -M_{\phi} \left(\frac{\delta F}{\delta \phi}\right)^n \tag{3-92}$$

The constraint equations (phase composition and minimization of square summation of $\boldsymbol{\beta}$ values) will be used at each time step to find the phase parameters and concentration of each phase in the interface.

IMC growth around a single particle:

The main purpose of this simulation is to find the correct parameters to match the experimental data presented in the previous section. A copper particle surrounded by liquid tin at 300°C was considered. Cu_6Sn_5 grains were considered at the interface of solid-liquid. Cu_3Sn does not start forming in the early stages of sintering, and its main microstructure evolutions occur during solid-state sintering. Thus, it is not considered in the scope of this simulation. The particle size was selected based on the data, Figure 3-6. Number of grains was estimated based on the shape of grown IMC on the particle as shown in Figure 3-14. The distribution of grain numbers around copper particles during a TLPS process is shown in Figure 3-15.

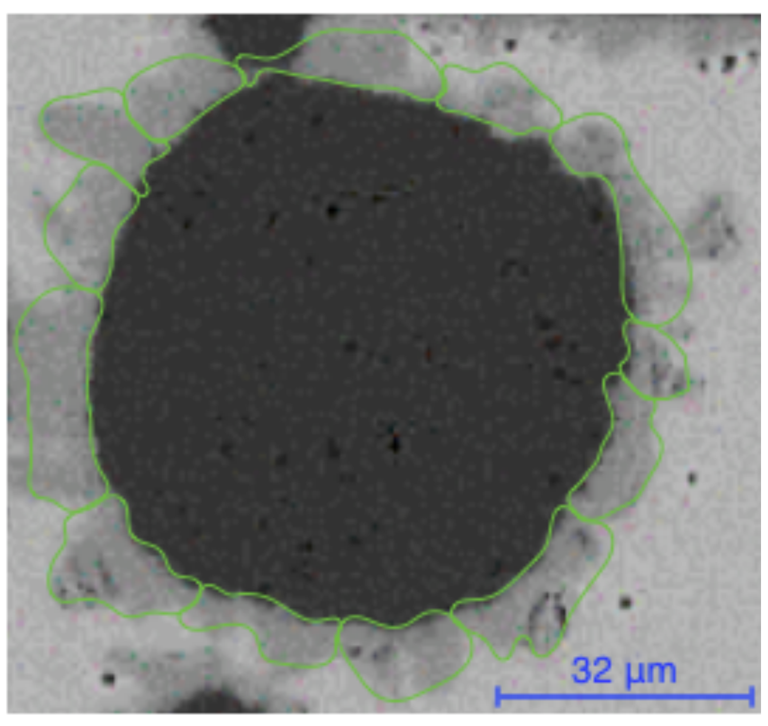


Figure 3-14: Grains formed around a copper particle after 2 minutes of sintering at 300°C

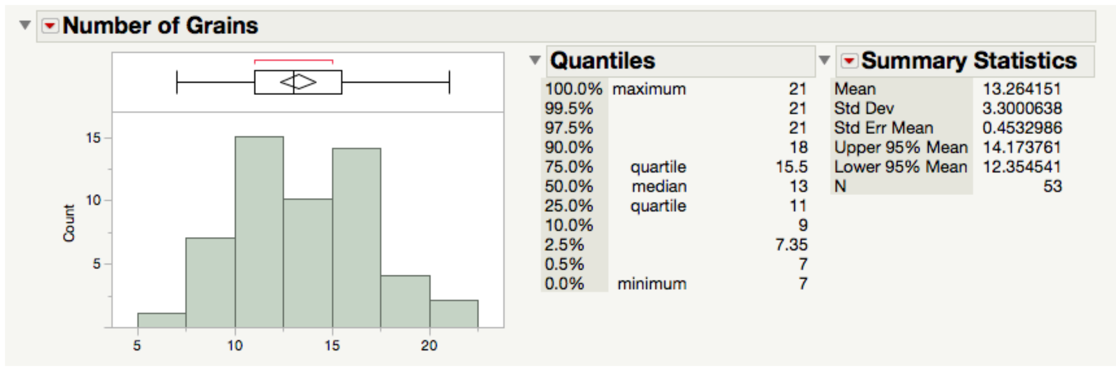


Figure 3-15: Average number of IMC grains around the particles after 2 minutes of sintering at 300°C (sample size: 53 particles)

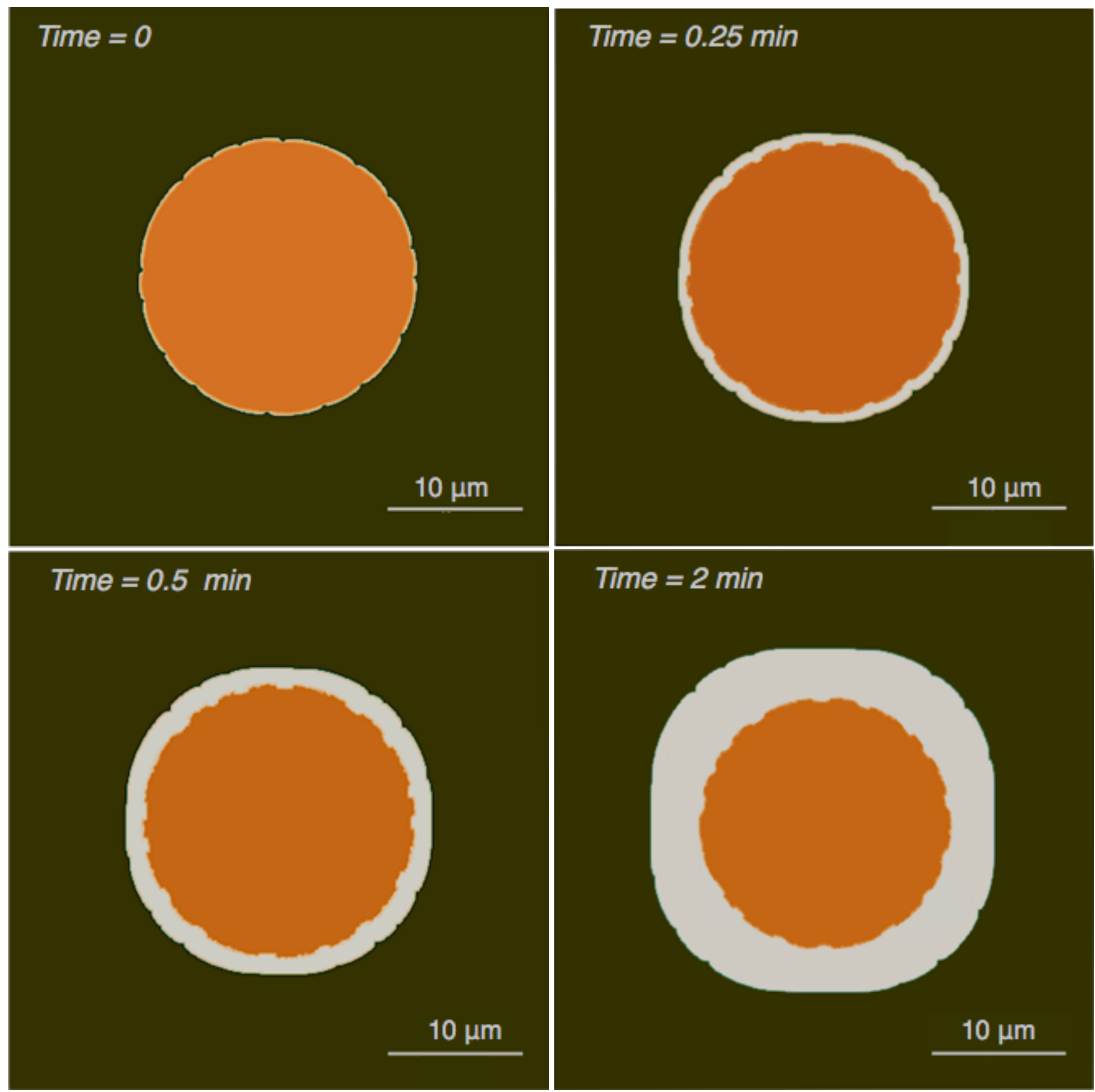


Figure 3-16: Cu_6Sn_5 growth during TLPS after a) 0, b) 0.25, c) 0.5, d) and 2 minutes processing at 300°C

Figure 3-16 shows the gradual IMC microstructure evolution at 0, 0.25, 0.5, 2 minutes processing at 300°C. At time zero, 16 grains emerge at the edge of the particle and slowly, start to use the liquid tin and solid copper. The average IMC thickness at 0.5 and 2 minutes match the experiment data, perfectly. Therefore, the simulation parameters are selected as follows:

$$D_{Sn} = 2\times 10^{-11} m^2/s$$

$$D_\eta = 2\times 10^{-12}\frac{m^2}{s}; \text{Diffusion coeffients} \quad (3\text{-}93)$$

$$D_{Cu} = 2\times 10^{-14} m^2/s$$

$$\sigma_{Sn-\eta} = 0.1\, J/m^2 \sigma_{Cu-\eta} = 0.3\, J/m^2; Interfacial\ energy \quad (3\text{-}94)$$

$$M_{Cu-\eta} = 5\times 10^{-12}, M_{Sn-\eta} = 5\times 10^{-11};\ Mobility \quad (3\text{-}95)$$

Two-step processing joint formation

In this section, IMC growth around copper particles in a two-step TLPS processing is simulated. Due to the lack of pressure during this process, there isn't considerable solid-state sintering between copper particles and they stay in farther distance from each other, compared to one-step processing. Therefore, the copper particles are placed completely disconnected from each other, as seen in Figure 3-17.

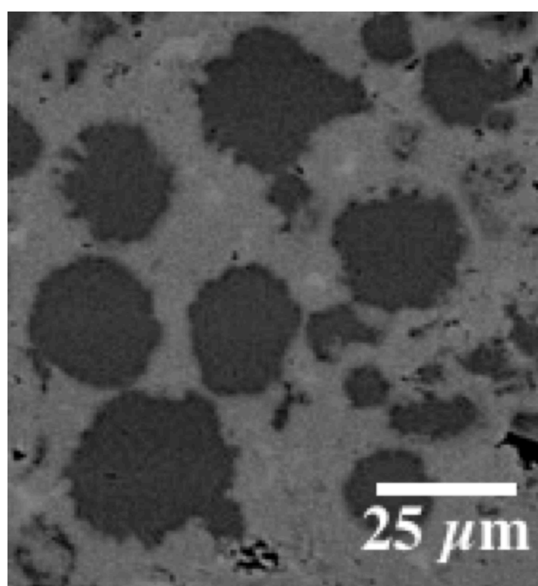


Figure 3-17: Copper particles in a two-step TLPS joint

An algorithm was developed in MATLAB to process cross-section images and detect copper particles, and their interfaces with IMCs or unreacted tin. These data were used to develop the shape parameter matrices in PFM method.

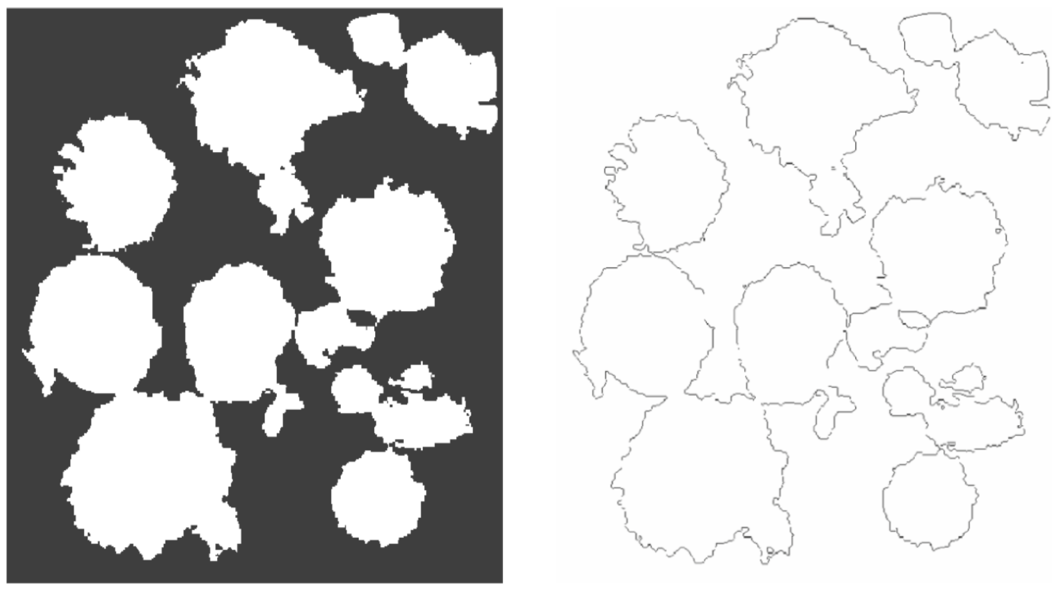


Figure 3-18: Image processing of Figure 3-17: left image shows copper phase, and right image shows the interface of copper and tin

Copper, tin, and Cu_6Sn_5 shape parameter matrices were developed based on the image processing results. Then, the simulation parameters defined in the previous section were used to monitor IMC growth around copper particles and into liquid tin. The whole process was assumed to occur at 300°C. Figure 3-19 shows the simulation results at 0, 30, 60, and 120 seconds. The process takes considerable time to fully cover the large distances between the copper particles. Additionally, it results in large IMC regions between the particles or even unreacted tin. Having unreacted copper in the joint improves electrical and thermal properties of the interconnection; however, unreacted tin and large IMC supplies provide enough reactants to consume copper particles and turn them to Cu_6Sn_5 and consequently, transform Cu_6Sn_5 to Cu_3Sn.

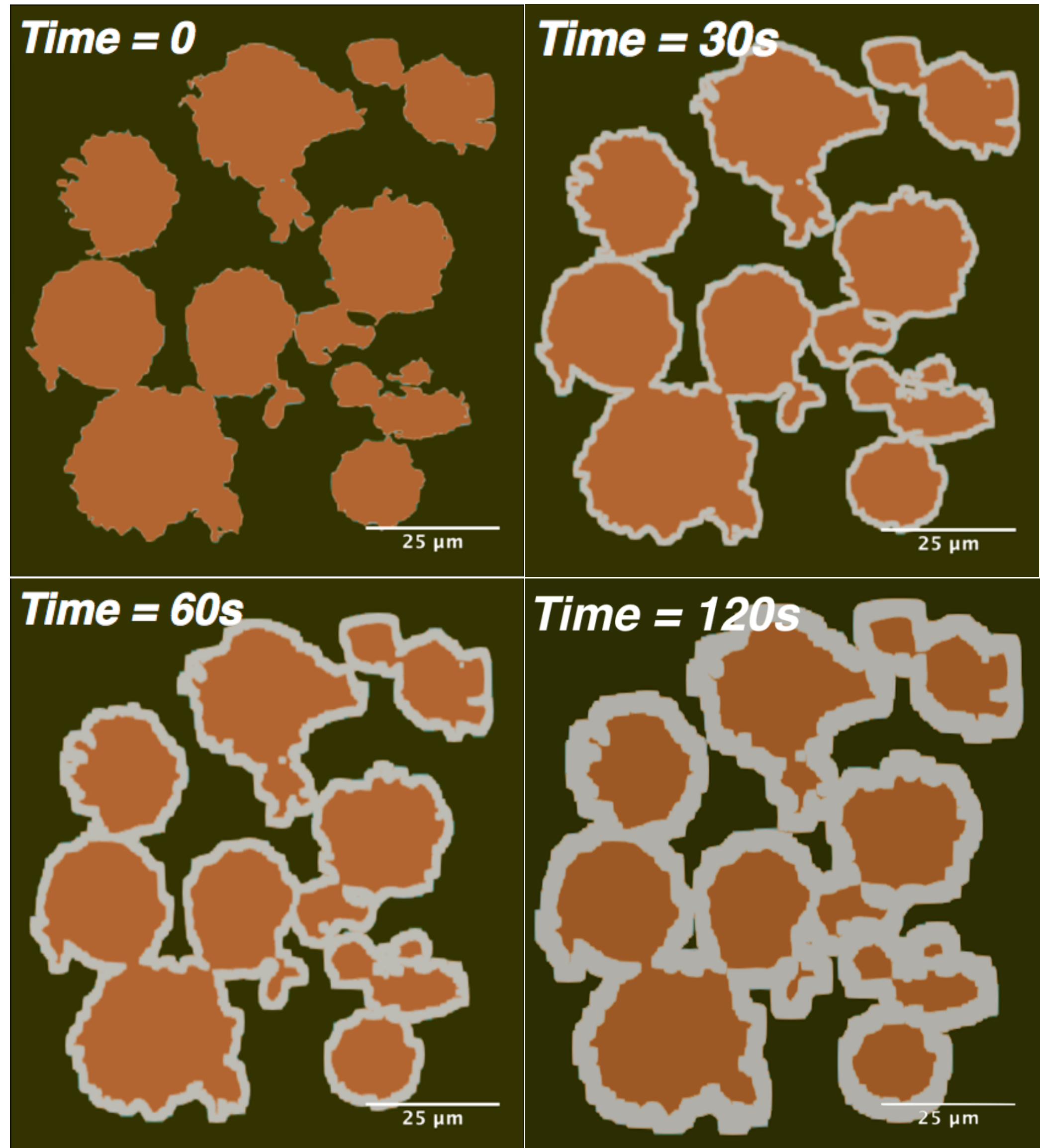


Figure 3-19: IMC growth around copper particles in one-step TLPS processing at 300°C

One-step processing joint formation

Due to considerable solid-state sintering in one-step processing, the HMP particles connected and formed a metal matrix. The gaps between the particles filled with LMP phase, and at processing temperature it would be filled with IMCs. In this section, a cross-section of one-step TLPS processed Cu-Sn interconnection is considered. Like

the previous section, the image was processed to develop HMP and interface parameters. Then, the rest of the area was filled with liquid tin.

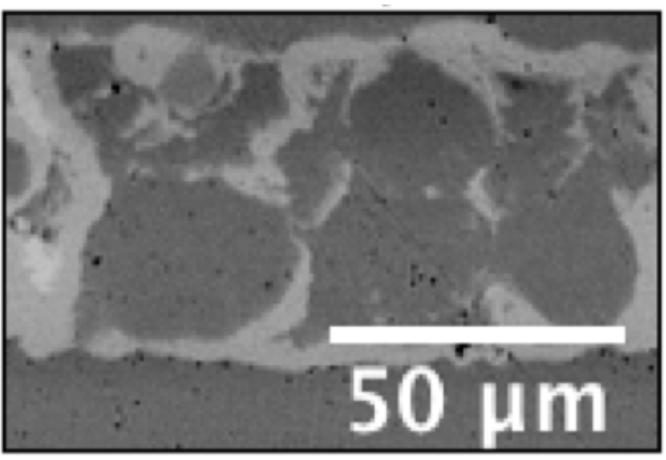


Figure 3-20: Solid-state sintered copper particles in a one-step TLPS joint

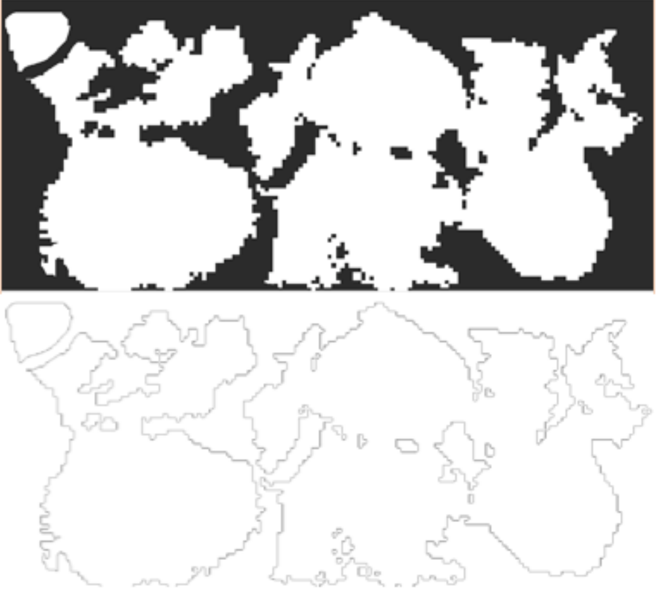


Figure 3-21: Image processing of Figure 3-20: top image shows copper phase, and bottom image shows the interface of copper and tin

Figure 3-22 shows Cu_6Sn_5 around copper matrix in one-step TLPS processing at 300°C. The processing time required to fill the empty areas between the particles is significantly shorter than two-step processing. After only 120 seconds, the joint is almost fully IMC and copper. Also, it will have improved mechanical, electrical, and

thermal properties due to the high amount of unreacted copper. The insignificant amount of unreacted tin stops the formation of Cu_6Sn_5 and furthermore, the low amount of Cu_6Sn_5 compared to unreacted copper limits the formation of Cu_3Sn. Therefore, the final product is a porous matrix of copper particles filled with IMCs with high operation temperature, and decent properties.

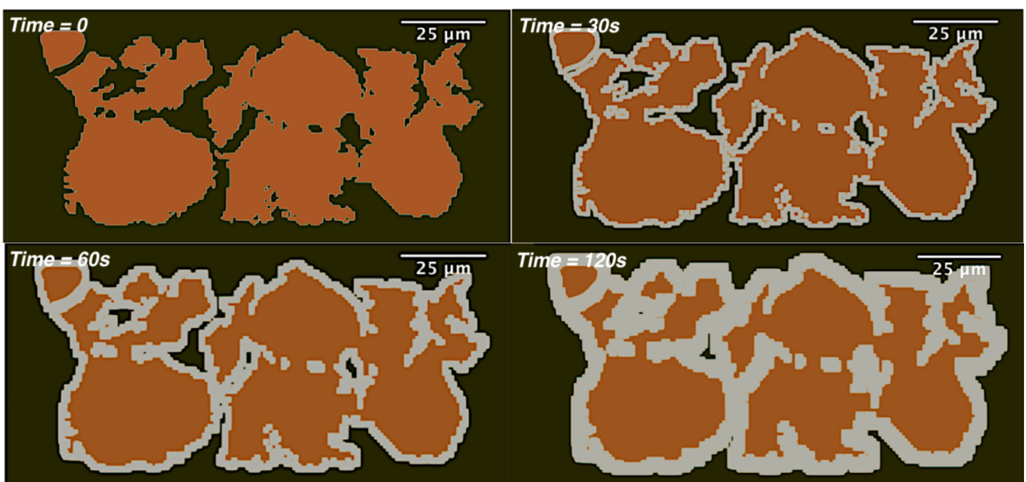


Figure 3-22: IMC growth around copper matrix in one-step TLPS processing at 300°C

Conclusions

Common physics solution to solid and liquid interface interactions were presented as sharp-interface and Phase field modeling (PFM). PFM as a powerful microevolution simulation method showed significant potential for modeling eutectic solidification and TLPS processes. The driving force behind PFM is minimizing the free energy of the system and following phase changes through shape (order) parameters. The common PFM models and their assumptions were introduced and their advantages discussed in detail in this chapter. Furthermore, a new assumption was considered in PFM solution to improve its performance for TLPS applications.

This method was used to model a single spherical copper particle in liquid tin in a TLPS process at 300°C. Copper, tin, and IMC free energies were developed based on

CALPHAD method. The simulation parameters were calibrated by my experiment results. Later, these parameters were used to model IMC growth in two and one-step processing copper-tin TLPS processing at 300°C. The copper and tin mapping in these processes was developed by using an image processing method developed in MATLAB. The shape parameter matrices were created based on the results from these mappings. The simulation showed faster completion of process in one-step processing method and how IMCs cover all the gaps between the particles, without any unreacted tin remaining. This leaves extra unreacted copper particles in the joint which improves mechanical, electrical, and thermal properties of the joints.

Chapter 4 : Experimental process

Introduction

Die-attach materials provide mechanical stability, thermal and electrical paths to the semiconductor dies. They are the first packaging component in contact with semiconductors and their performance critically affects the reliability and performance of the package and device. There are a number of requirements to consider a die attach material as a potential candidate for electronic applications: high electric and thermal conductivity, ability to manage the thermal expansion stresses, and low cost [101]. For high temperature power electronic applications, high-temperature threshold and reliable performance at temperature limits are other significant requirements. There is no specific framework for testing and comparing die-attach materials, and generally, similar approaches to solder bump qualification methods are considered. Common test procedure for these materials targets repeatable performance of die-attaches under cyclic loads, such as thermal and power loads in package levels. These loads create thermomechanical stresses in packages under test and consider mechanical performance and thermal/electrical properties as the reliability indicators. A comprehensive list of reliability tests used to evaluate reliability and quality of sintered die-attaches is presented in the literature review chapter.

This chapter is dedicated to experimental approaches used to test TLPS joints under different loading conditions. The first part explains the screening methods to qualify the joints for reliability tests. The second part mainly concentrates on reliability tests, power cycling, drop-shock, thermal cycling, their requirement, test setup, and procedure. Finally, the results from these experiments are presented and investigated

to identify the failure modes and mechanisms of interconnections to reveal potential ways to improve the reliability and our understanding of the TLPS interconnections.

Quality metric

Figure 4-1 shows the cross-section of a fully processed Cu-Sn two-step processed TLPS joint with decent quality under ESEM. The liquid tin filled the gaps between the Cu particles and at the processing temperature, formed IMCs with high melting point to connect a copper die and substrate. The pores in the joint are mainly formed due to the burnt residues of the flux or trapped fumes in the joint. Due to manual processing and different processing factors (defined in previous chapters), the quality of final interconnection can vary from one sample to the other. One method to evaluate the quality of TLPS joints is considering the fraction of un-wetted or voided regions to the whole joint area or cross-section, respectively. Lower void content and un-wetted regions provide better mechanical stability, and electrical and thermal paths to the semiconductor device. In the subsequent sections, image-processing and machine-learning approaches are introduced to measure the constituents' fraction and void content of TLPS interconnections.

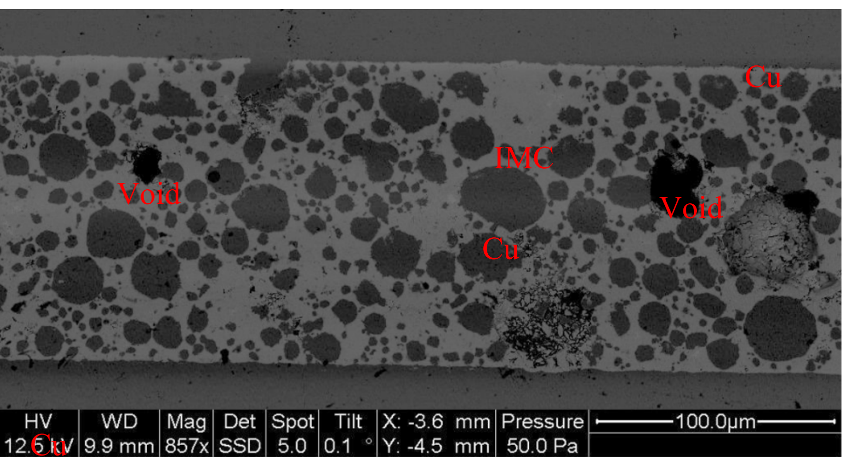


Figure 4-1: Cross section of a fully processed Cu-Sn TLPS joint

Screening

The non-destructive screening methods are more popular in industrial applications; however, in many cases, they are not enough to have a comprehensive quality evaluation. In this dissertation, a hybrid approach, including destructive and non-destructive methods, was considered to assure the quality of TLPS joints.

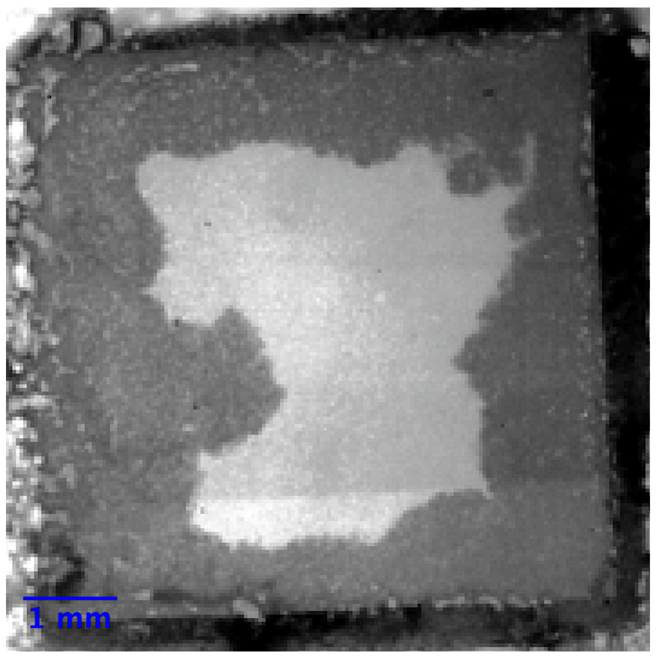


Figure 4-2: A low quality joint rejected in X-ray screening

In each TLPS processing, three samples were made under similar conditions. All the samples were X-rayed to analyze liquid tin wetting and diffusion. Figure 4-2 shows a two-step TLPS processed sample under X-ray. The sample is a silver-plated silicon diode mounted by Cu-Sn TLPS joint on a copper substrate. The diode and substrate dimensions are 6.5×6.5 and 10×10 mm^2, respectively. The bright region (~32.4% of the joints area) at the center of the diode is the un-wetted area. The liquid tin either was not enough to reach that region or could not penetrate through the copper particles. This

joint obviously does not have the standards for power electronic applications. Figure shows a joint with acceptable quality. Liquid tin completely wetted the whole surface of the joint and then, formed IMCs and solidified. The cutoff line of minimum 95% wetted area was considered in this work to pass the X-ray screening. The un-wetted region either concentrated in one region or spread through the joint should in exceed more than 5% joint area, as seen Figure 4-4.

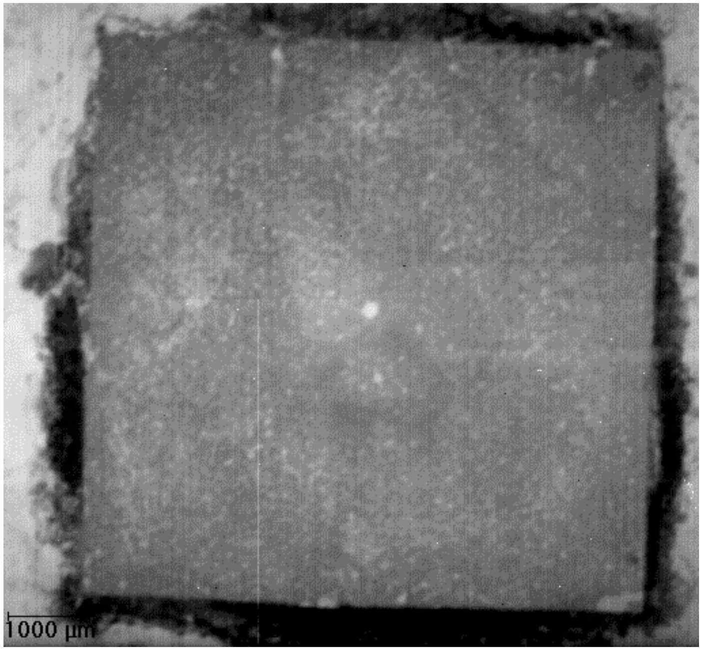


Figure 4-3: A high quality joint; passed the X-ray screening

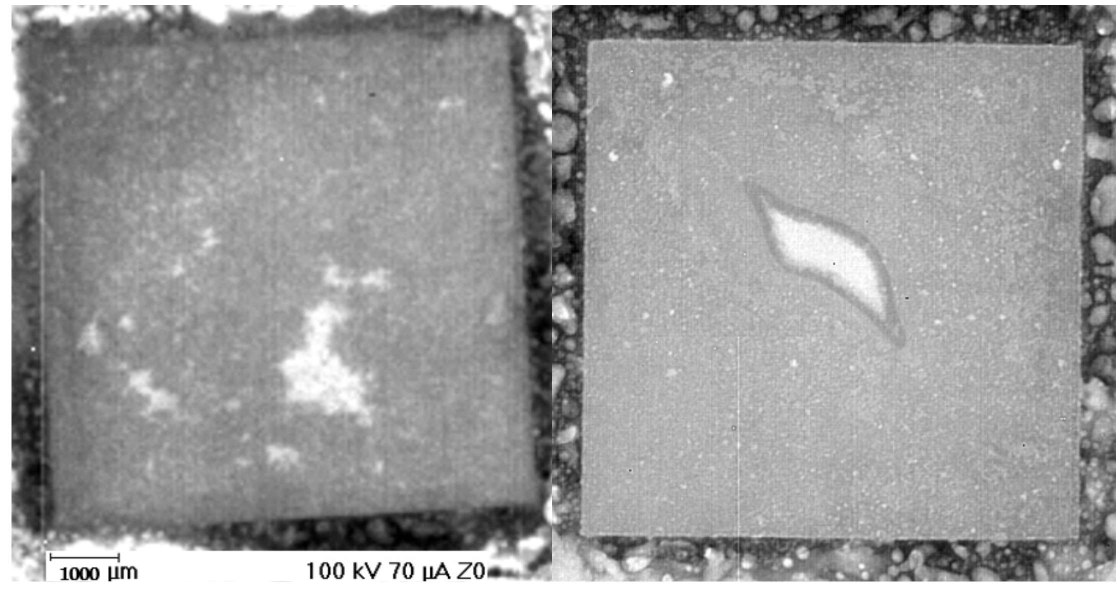


Figure 4-4: Joints passed the X-ray screening with wetting (~96%)

After X-ray, one sample was selected for the destructive analysis. The diode was removed by shear force and the surface of the TLPS joint analyzed under optical microscope to validate that the dark area, observed under X-ray, is joint matrix. This step is essential since particle oxides in a poorly processed TLPS joint create very similar X-ray pattern to dark regions.

It is worth mentioning that the hybrid screening only considers the wetting ability of the TLPS paste and not the small voids inside the joint. Since the voids are mixed with HMP metal and IMCs, while sandwiched between power substrate and metal layered component/dummy die, it is not possible to detect them effectively without destructive methods. Figure 4-5 and Figure 4-6 show two Cu-Sn joints that passed the X-ray screening. The first joint is almost void-free; however, the second one has lots of small and large voids. It is important to measure the extent of these voids. First, ImageJ software was used to measure 2D volumetric percentage the voids in the joint area. But

this method was very time-consuming. A MATLAB algorithm was developed to measure the fraction of void with respect to the joint area, Figure 4-7.

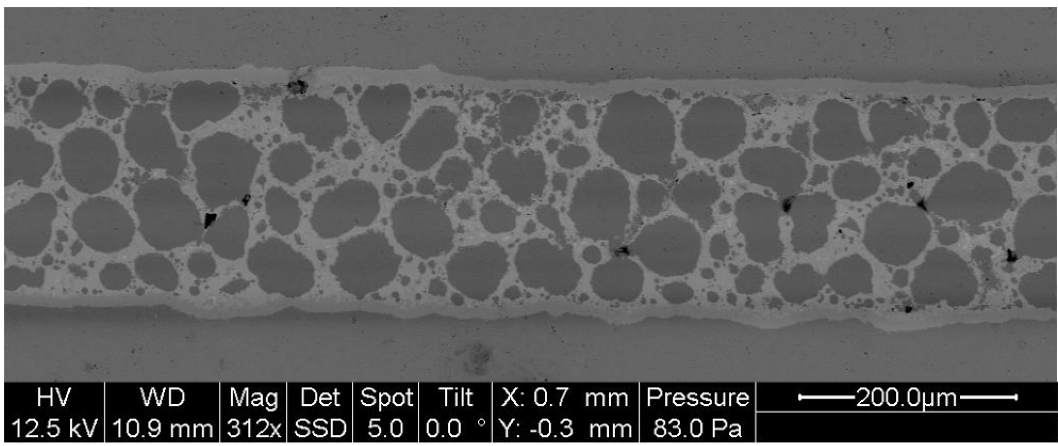


Figure 4-5: Almost void-free TLPS joint

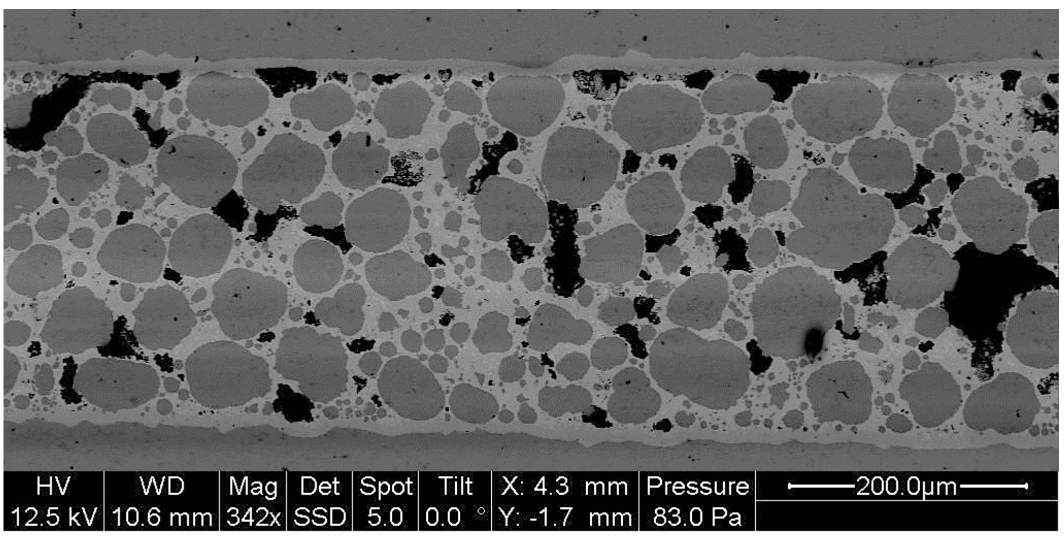


Figure 4-6: Voided TLPS joint that passed X-ray screening

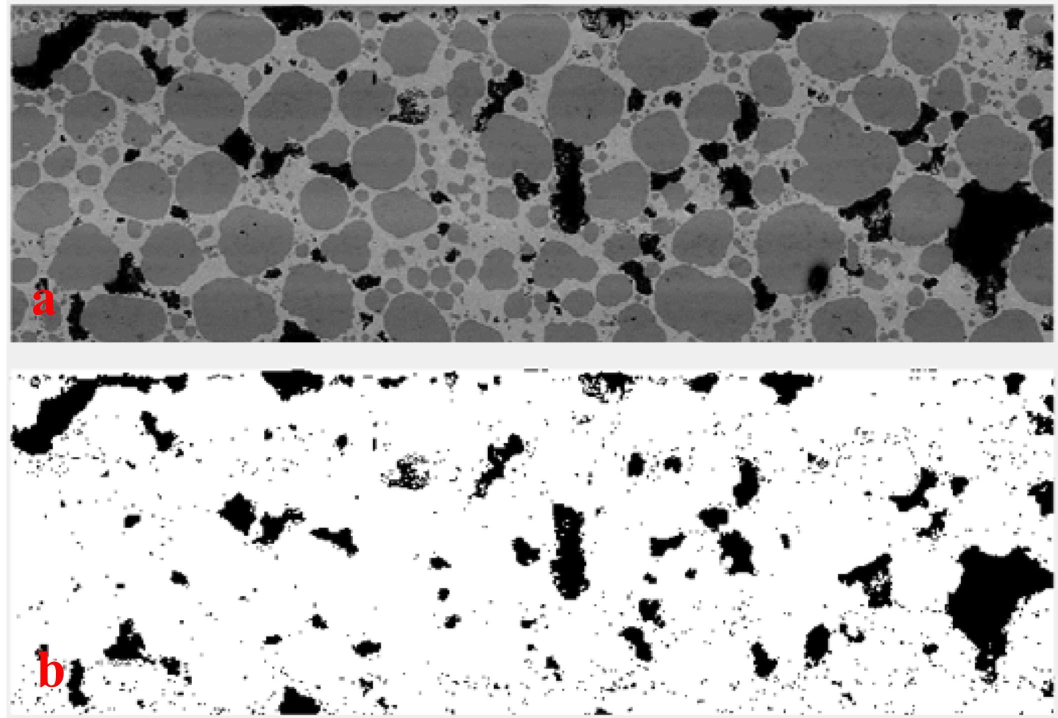


Figure 4-7: a) Joint image (MATLAB code input), b) Processed image with threshold=80, 87.7% joint density

The algorithm works as follows: first, an image is imported to MATLAB and a threshold value anywhere from 0 to 100 is selected. This value is used to differentiate the dark and bright regions. Then, the region of interest (ROI) is defined by selecting four corner points of the joint using the cursor, Figure 4-7 (a). The ROI is processed and a black and white image is produced. The black and white regions represent the voided and healthy regions, respectively, Figure 4-7 (b). Finally, the algorithm calculates the area of black region and white region with respect to the whole joint area. The selection of threshold value is based on the comparison of the main and the processed images. Very large threshold values increase the estimated more an unrealistic void content and creates a noisy reconstruction. For example, the threshold for Figure 4-7 is 80, and the voided and healthy regions are 12.3% and 87.7%, respectively. Increasing the threshold value to 90 results in estimating 20.5% voids in

the cross section, as seen in Figure 4-8. A comparison of the results shows that the processed image with threshold value 80 is matching better with joint's cross-section. Therefore, the correct value for the joint density is 87.7%, which is an acceptable joint density based on the previous discussions in chapter 3.

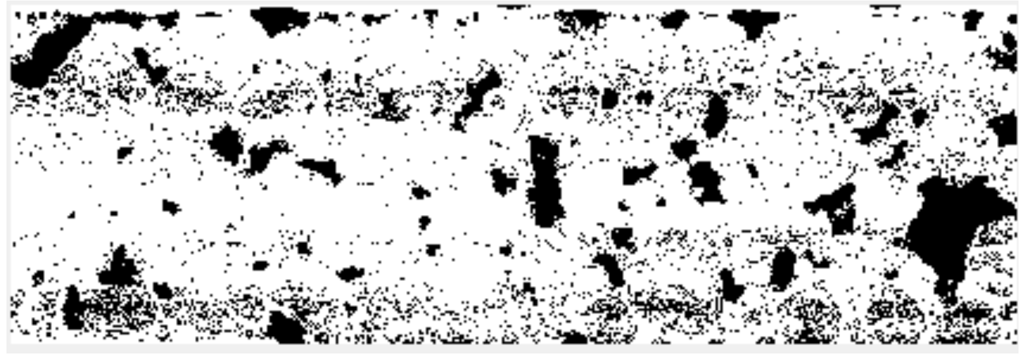


Figure 4-8: Processed image with threshold=90, 79.5% joint density

Composition classification

Machine learning approaches could extend the void content evaluation algorithm to automatically define each material and its fraction in the ROI. For this purpose, Fiji software was used. It provides a powerful library of different machine learning algorithms. Figure 4-9 shows the overview of training steps used in composition classification approach. Figure 4-10 shows the input image used for the training purpose. Five classes of materials were defined in this image: copper particles (red), unreacted tin (cyan), Cu_6Sn_5 (yellow), Cu_3Sn (green), and voids (purple). After several training steps, the software defines different materials with high accuracy, as shown in Figure 4-11. The fraction of each material in the ROI is presented in Table 5.

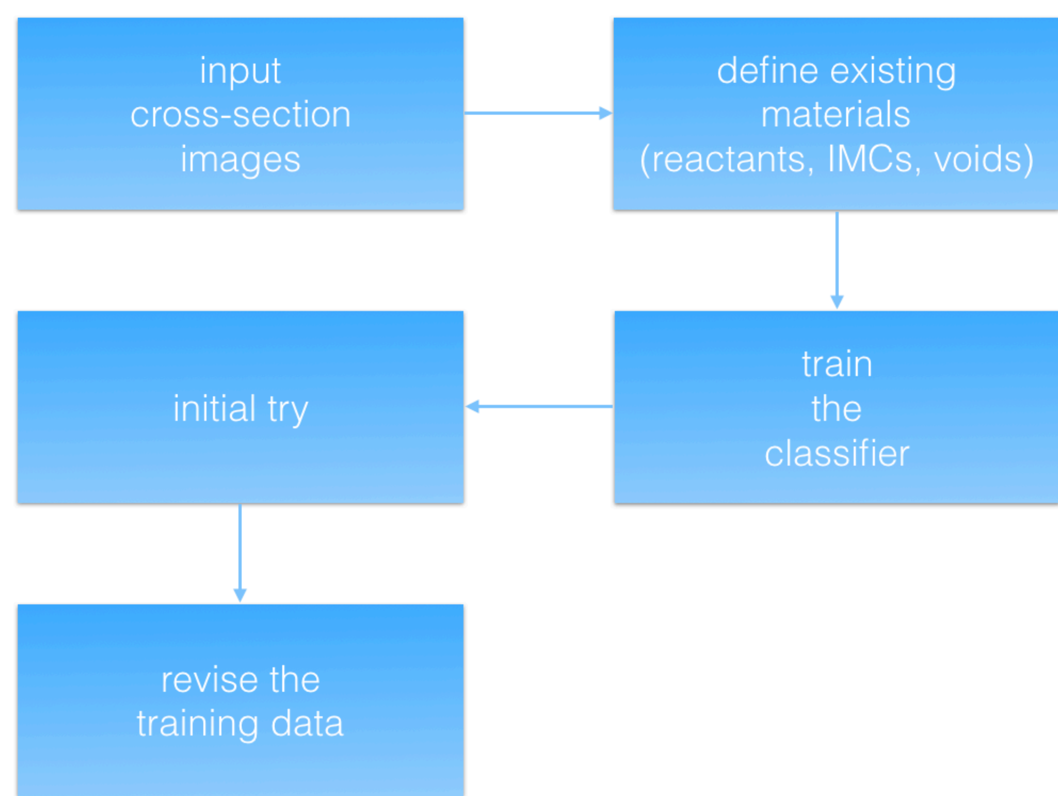


Figure 4-9: Machin-*learning composition classification approach*

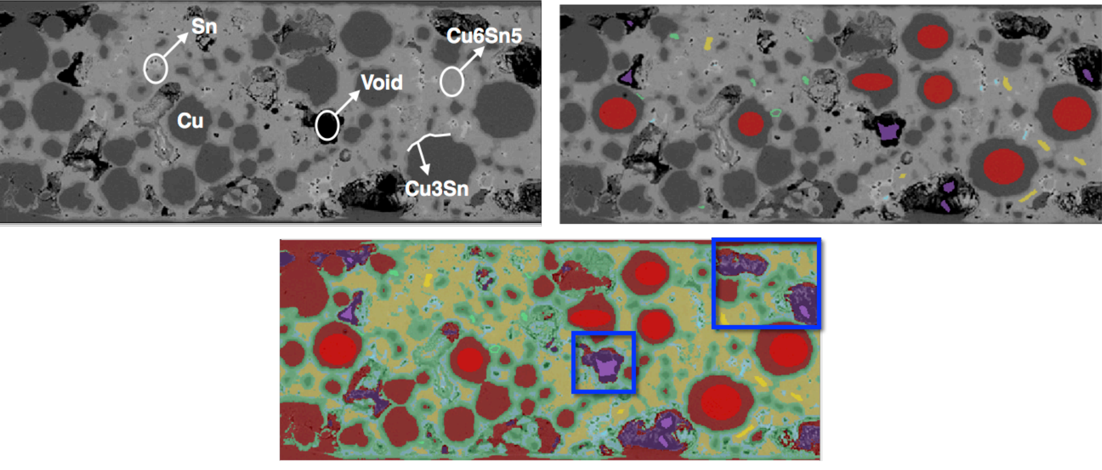


Figure 4-10: a) Input ESEM image, b) Defined material classes: copper particles (red), unreacted tin (cyan), Cu_6Sn_5 *(yellow),* Cu_3Sn *(green), and voids (purple), and c) First try results with low accuracy*

Table 5: Joint composition classification results

Material	*Cu*	*Sn*	*Cu_3Sn*	*Cu_6Sn_5*	*Voids*
Area (%)	34.6	2.4	23.1	31.4	8.5

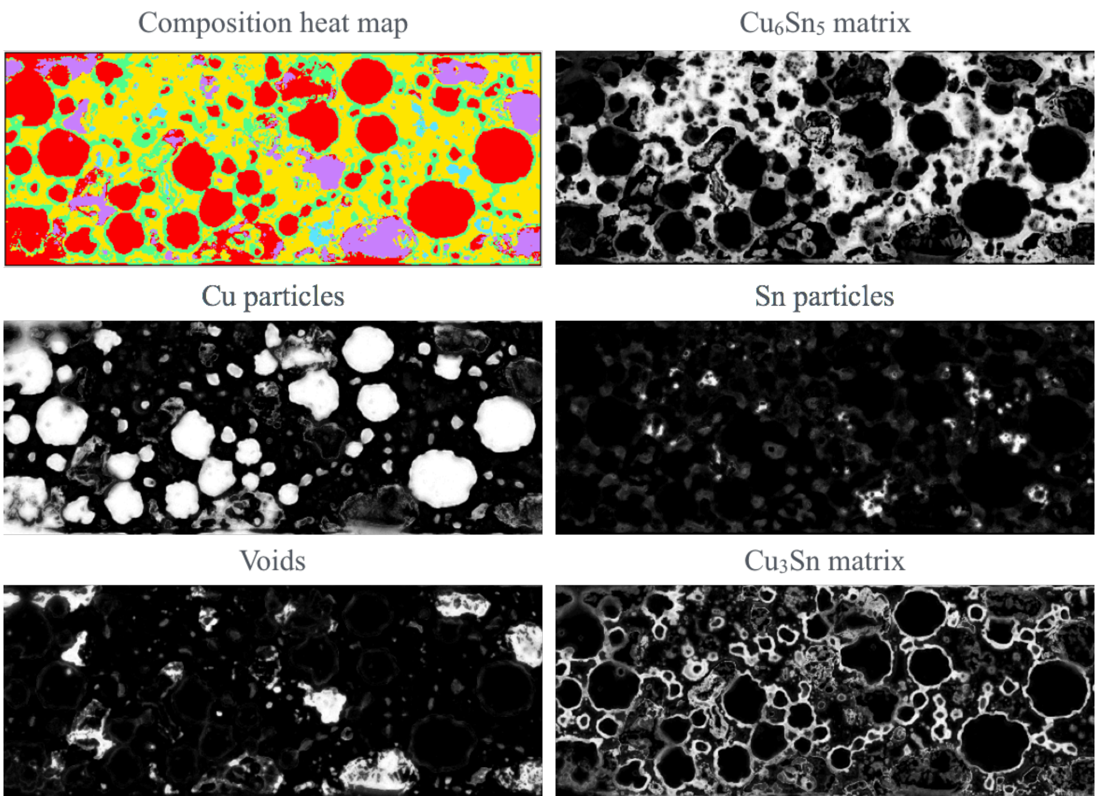


Figure 4-11: Composition classification results after finalizing training step

<u>*Composition evolution*</u>

Composition classification provides a perfect approach to measure IMC evolution during a TLPS process. For this purpose, TLPS joints with different processing times (i.e. 30s, 60s, 120s, and 240s) at 300°C were prepared. Joints were mounted in epoxy, cross-sectioned, and analyzed under ESEM. The ESEM cross-section images were imported to composition classification algorithm and each component's fraction was evaluated. Figure 4-12 shows the variation of each component's fraction in the joint with respect to processing time. The fraction of Cu_3Sn is not considered in this experiment because it is mainly formed during solid-state sintering and takes more than

240s to appear in interconnection region. The processing time is enough to decrease the void and unreacted tin level to less than 10% and create a high quality joint.

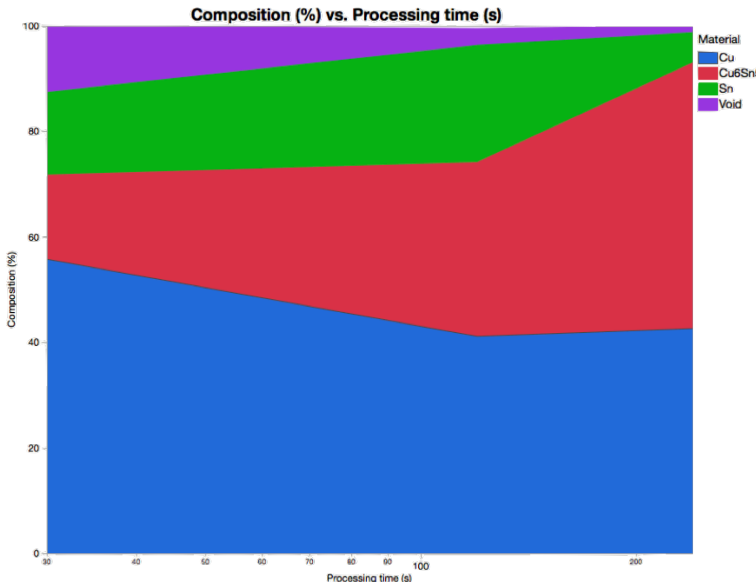


Figure 4-12: Composition evolution with respect to processing time for TLPS at 300C

In the following sections reliability and performance of Cu-Sn and Ni-Sn TLPS joints are evaluated under different loading conditions, such as drop-shock, power cycling, and thermal cycling.

Reliability and failure analysis

Increasingly harsh environments and loading conditions for electronic systems render a time-to-failure assessment of interconnect materials under dynamic loads—a crucial factor in their reliability assessment. Fracture and crack propagation at the interface of the IMC and the substrate metallization is the most common failure mode for solder interconnects under high strain rate vibration and drop/shock load conditions. Therefore, it has generally been presumed that the IMCs are the limiting factors in joint reliability under dynamic loads. In TLPS systems, the joint bulk material either consists of IMCs only for layer-based systems, or of metal particles connected by a matrix of

IMCs for the paste-based approaches. This requires more reliability investigations to qualify their performance under dynamic loading conditions [102]. In this section, three common reliability tests, thermal cycling, power cycling, and drop-shock, were considered to investigate the performance of TLPS joints made of Cu-Sn and Ni-Sn.

Dynamic loading (drop-shock test)

The ability of an interconnect material to survive dynamic loads is a crucial factor for the life cycle analysis of electronic packages. From solder interconnects vibration and shock tests, it is generally known that joint failure occurs at or within the IMCs that form between the solder and the substrate during processing or operation. It has therefore been hypothesized that the IMC layer is the limiting factor for the reliability of interconnects under dynamic loads. IMCs are the main constituents of TLPS joints. If the reliability of interconnects is limited by the IMCs, they should be suspect to limited life time under dynamic drop loads.

Most of the consumer electronic manufacturers focus on the mechanical reliability of the component to board connections (solder joints). However, there is no specific standard method which includes the mechanical reliability evaluation of die attach materials. In most cases, it is expected that the component to board connections fails faster than the die attach material because of the smaller contact area. Increasing the intermetallic content of the die attach materials in transient liquid phase sintering joints requires more investigation in the behavior of these joints under mechanical loads. In this study, drop shock test is considered as a qualification method to simulate highly accelerated mechanical loads on TLPS joints.

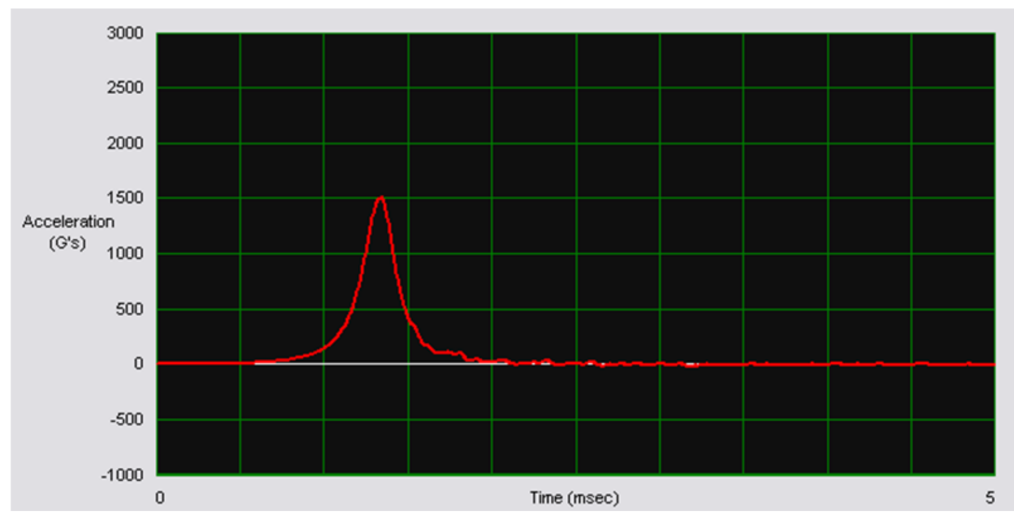


Figure 4-13: Drop shock test acceleration over time

Sample preparation and test procedure

Due to the lack of a standard method to assess mechanical reliability of die attach materials under drop shock loading, a method similar to Board Level Drop Test Method of Components for Handheld Electronic Products (JEDEC Standard: JESD22-B111) and the qualification method for TLPS adhesive composites is used [5]. For this purpose, a drop tower capable of providing 1,500 G was used. The acceleration pulse duration of 0.5 milliseconds which follows a half sine curve (similar to JESD22-B111 requirements) was considered, as shown in Figure 4-13. An aluminum fixture was designed to mount the samples on the drop tower. Figure 4-14 shows the fixture and how it is mounted on the drop tower. Samples are prepared by attaching a metal die on metal strips with Ni-Sn TLPS pastes and Sn3.5Ag solder, as shown in Figure 4-15. To define the reliability of the samples some exploratory tests were designed.

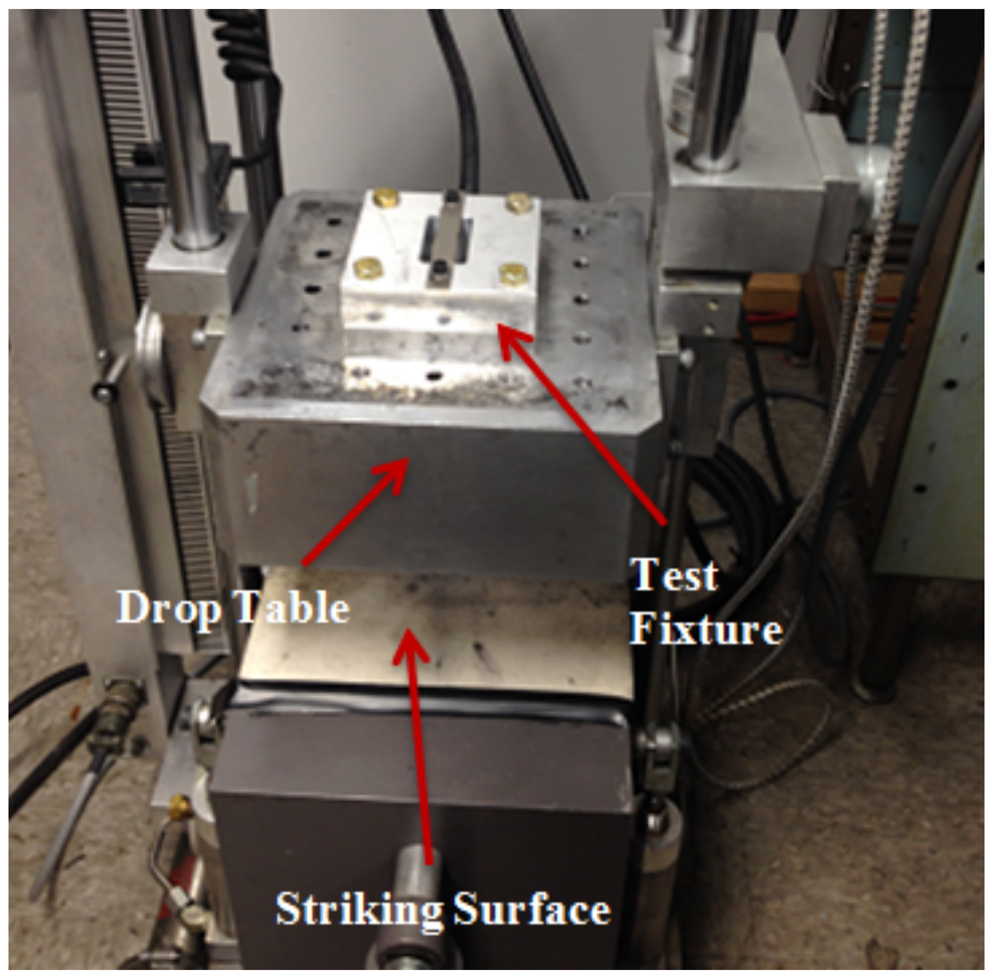


Figure 4-14: Sample fixture mounted on drop tower

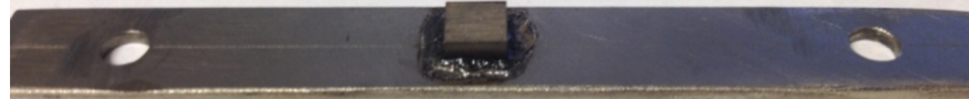


Figure 4-15: Ni-Sn TLPS drop test sample

Ni-Sn sinter specimen was tested for a combination of 500 drops under 1,500 G and 10 drops under 7,500 G. The samples were cross-sectioned after the shock cycles and investigated for initiated cracks. Environmental Scanning Electron Microscope (ESEM) was used to identify and capture the cracks.

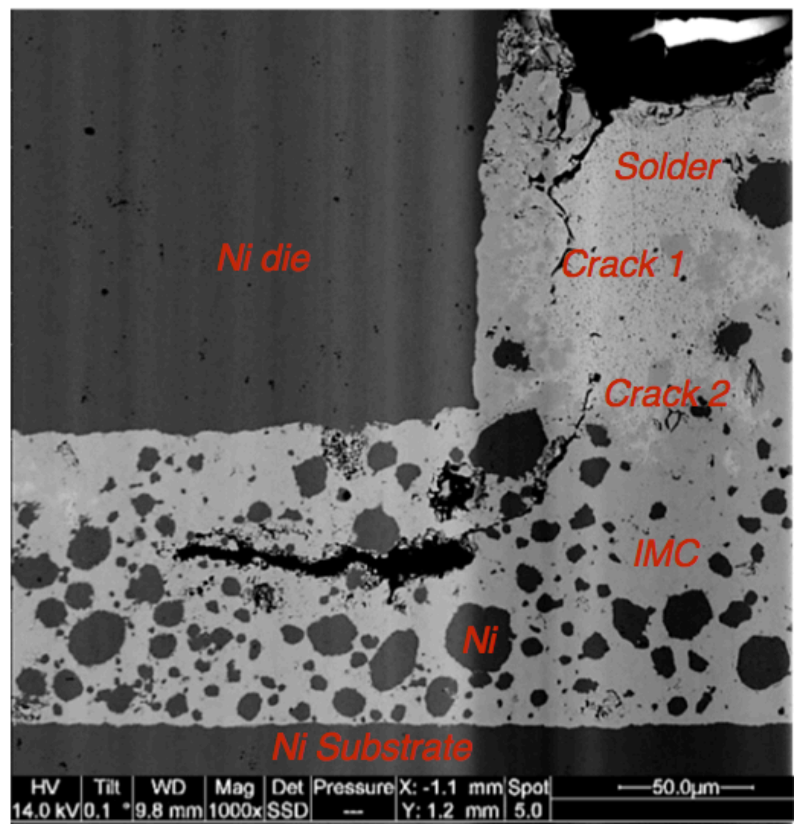


Figure 4-16: ESEM image of Ni-Sn sinter joint between Ni-die and Ni-stripe) after drop tests; magnification x1000

Results and discussion

Figure 4-16 shows the ESEM image of Ni-Sn TLPS sinter after drop cycles. The image shows two cracks initiated at the right corner of the joint; they were observed at the corner of the die. Both cracks started in solder material region. Crack 1 propagated on the edges of intermetallic; however, the second one went through the intermetallic and stopped at a void. Figure 4-17 shows small cracks formed near a nickel particle at die corner. No other cracks were observed in the studied cross section.

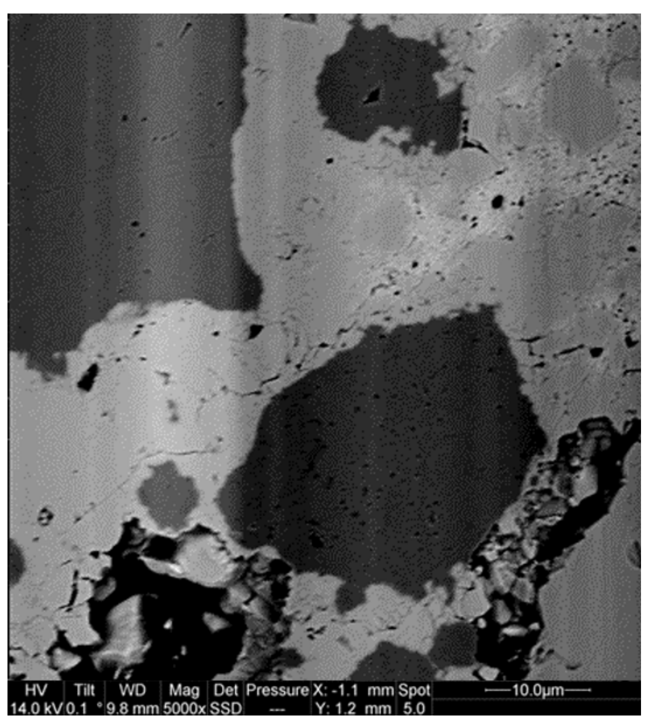


Figure 4-17: ESEM image of Ni-Sn sinter joint between Ni-die and Ni-stripe) after drop tests; magnification x5000

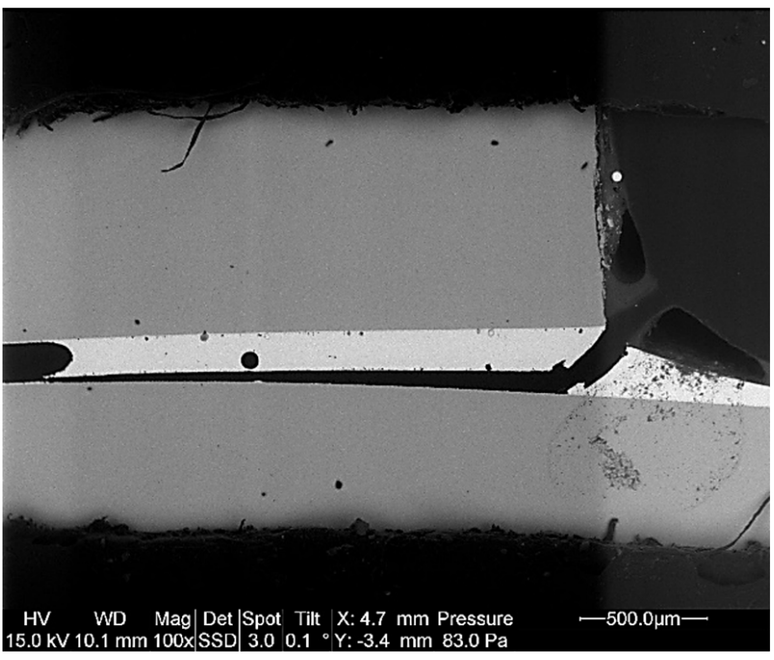


Figure 4-18: ESEM image of Sn3.5Ag solder joint between Ni-die and Ni-stripe) after drop tests; magnification x1000

Sn3.5Ag solder samples were cross-sectioned and analyzed under ESEM. The joint cross-section is presented in Figure 4-18. A crack started at the edge of the die and propagated though the interface of solder material and Ni substrate. In this figure, it is obvious that the solder material crack growth under mechanical drop shock loading is faster compared to that of Ni-Sn sinter pastes; the joint was close to complete detachment. In both solder and TLPS samples, crack initiation location was not the IMC layer. The cracks started and propagated in solder regions. In TLPS, the inhomogeneous microstructure creates more barriers for propagation. Therefore, the crack was directed to lower resistance and energy regions, i.e. voids. Depending on crack propagation energy the void could trap their growth and stop complete destruction of the interconnection. In solder, more uniform microstructure provides an easier path for propagation until crack reaches solder-IMC interface. Crack could propagate in either solder-IMC interface or IMC layer. Due to the thickness and void content, the IMC layer is a convenient path for propagation, Figure 4-19.

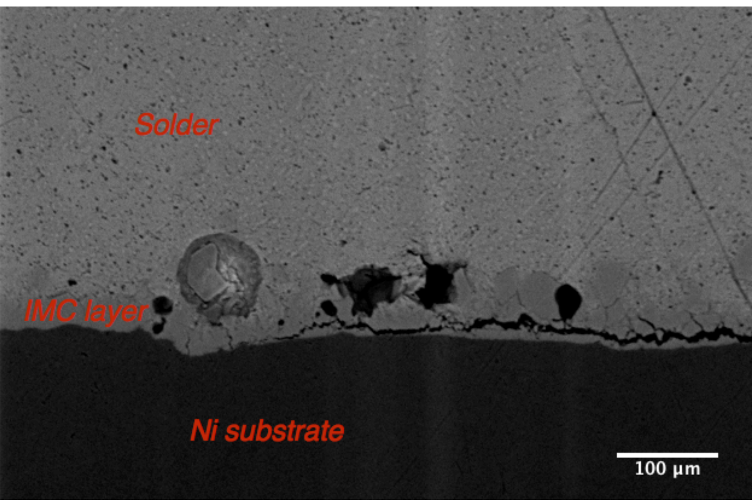


Figure 4-19: Magnified ESEM image of crack propagation in IMC layer between Sn3.5Ag solder Ni-stripe) after drop tests; magnification x3500

TLPS attachments showed superior performance under drop-shock loading compared to solders. This shows great potential for harsh environment and condition applications, such as well-drilling, space exploration.

Dynamic loading (drop-shock test) after aging

Sample preparation and test procedure

Two sets of test samples (six samples in each set) were prepared by attaching copper dies (with $1/4 \times 1/4 \times 1/8$ inch^3 dimensions) to copper stripes (with $4 \times 1/2 \times 1/40$ inch^3 stripes), Figure 4-15. First set used Ni-Sn3.5Ag TLPS paste, and the other Sn3.5Ag solder as the interconnection. Samples were isothermally aged for 0, 100, and 500 hours at 185˚C, and then, drop-shocked for 1,000 cycles.

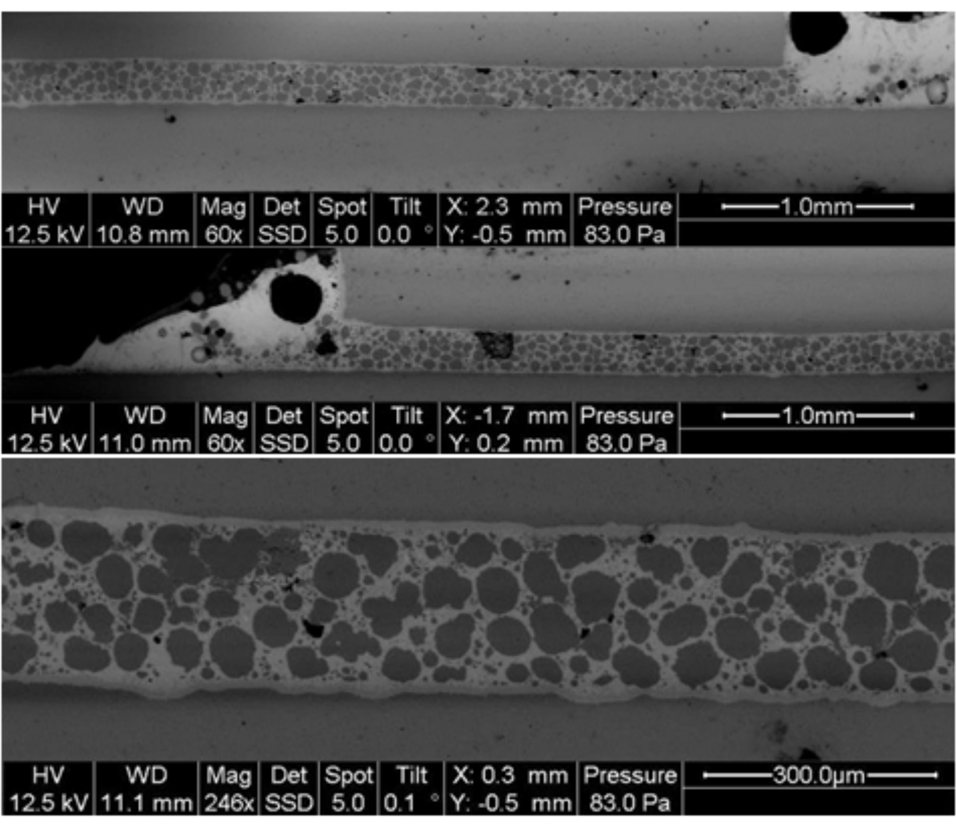


Figure 4-20: ESEM image of TLPS joint (no isothermal aging)

Figure 4-20 shows the condition of a TLPS joint before aging. This sample shows less voids compared to the aged samples (Figure 4-21and Figure 4-22). The IMCs in the middle of the joint are mainly Ni-Sn IMCs, but at the top and bottom interfaces Ni-Sn-Cu IMCs form due to the existence of copper. Aged specimens show more and larger voids, mostly concentrated below the IMC layer between TLPS material and the die. These voids form and grow during aging by consumption of Sn because of growth of Cu-Sn IMCs within the Cu substrate and die.

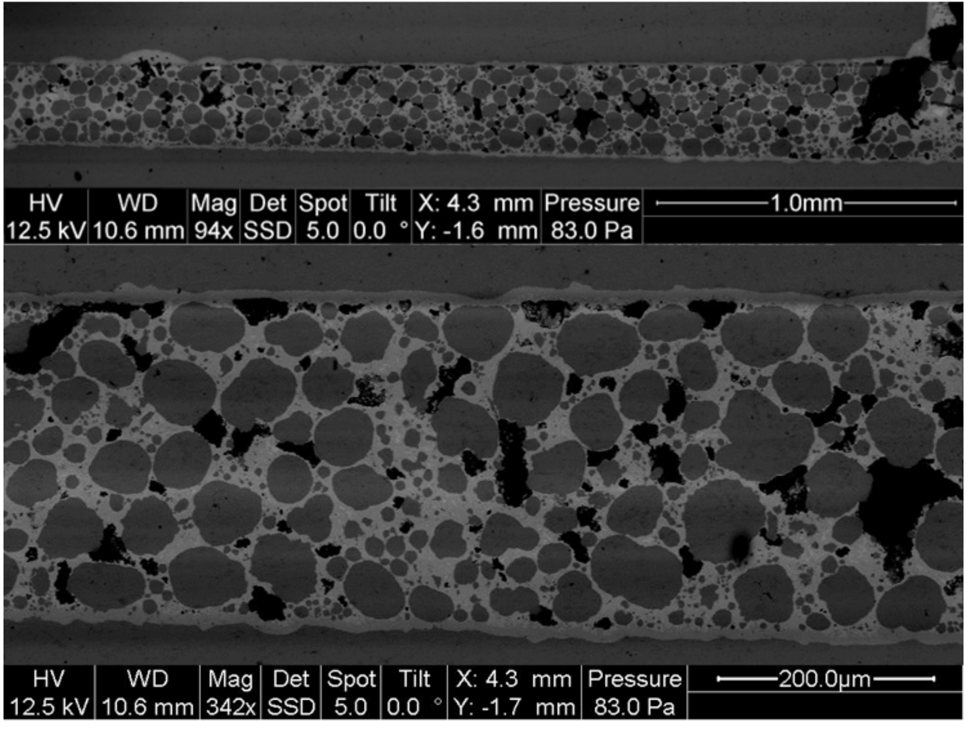


Figure 4-21: ESEM image of TLPS joint after 100 hours isothermal aging at 185˚C

<u>*Results and discussion*</u>

Figure 4-23 shows the solder joint formed between copper die and substrate before the aging process. Formation of small IMCs at the interfaces of the solder material and the copper die and substrate can be observed. Figure 4-24 and Figure 4-25 show the joints after 100, and 500 hours isothermal aging at 185˚C, respectively. Here, two distinct

layers of Cu-Sn IMCs of significant thickness are present: Cu_6Sn_5 which is formed during processing and grows during aging, and Cu_3Sn, which forms between the Cu_6Sn_5 IMC and the Cu metallization. The diffusion of Sn into the copper parts resulted in more voids at the interfaces. This increases the probability of failure under dynamic loads, such as drop.

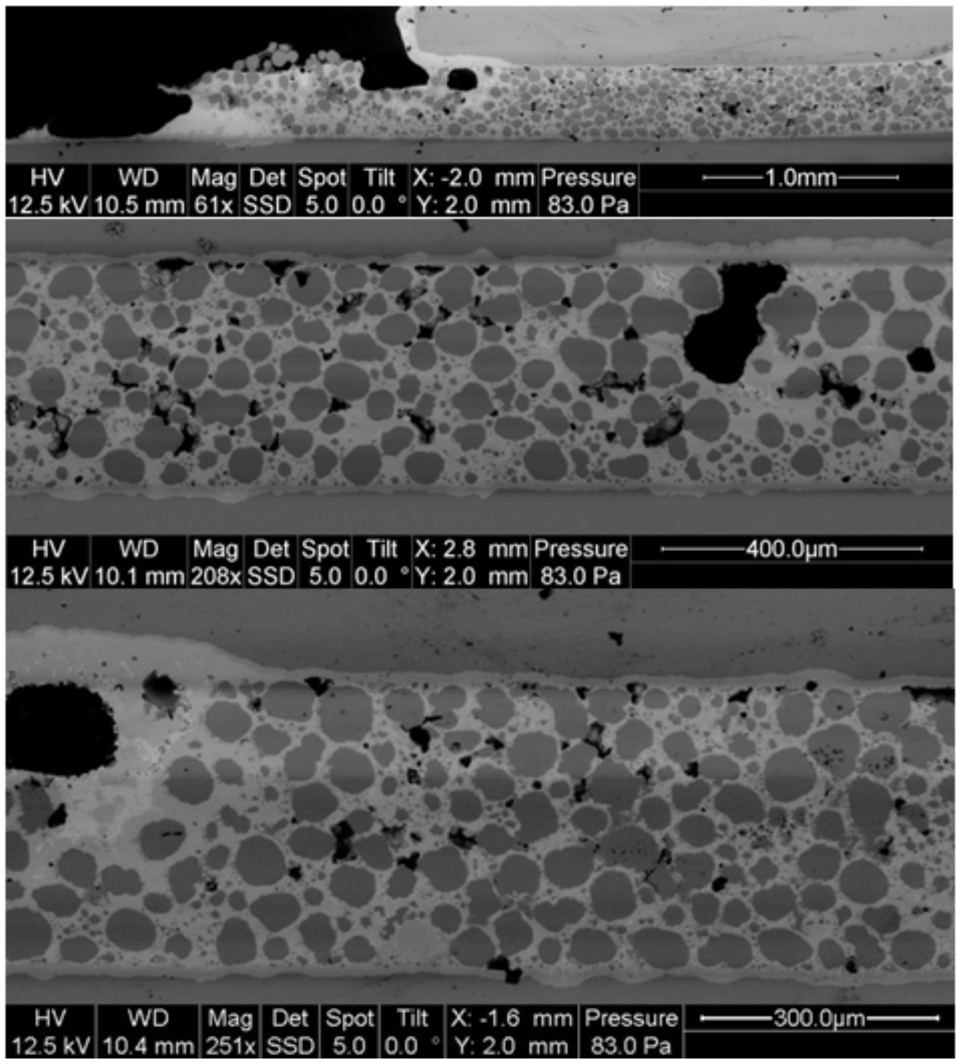


Figure 4-22: ESEM image of TLPS joint after 500 hours isothermal aging at 185˚C

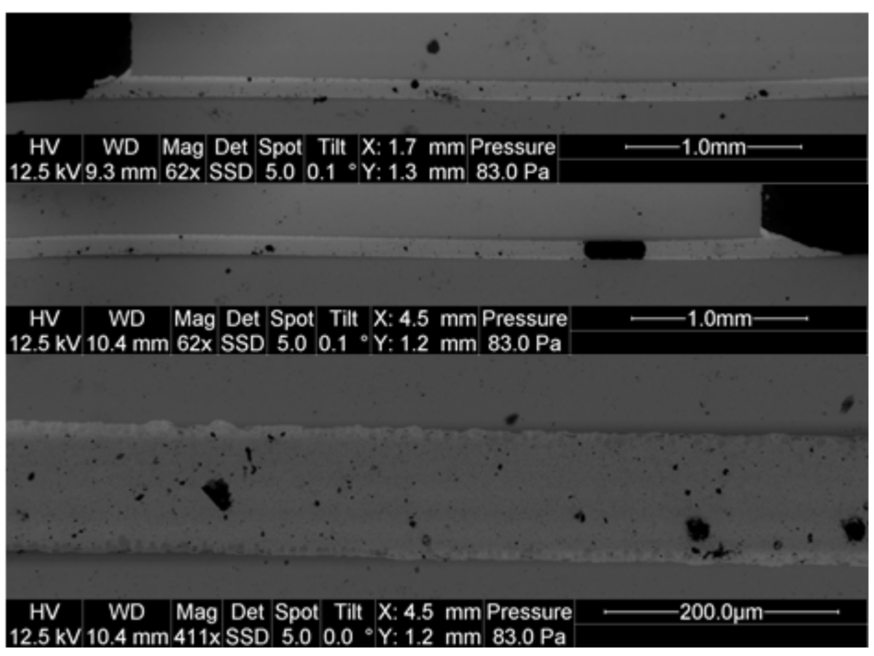


Figure 4-23: ESEM image of Sn3.5Ag solder joint (no isothermal aging)

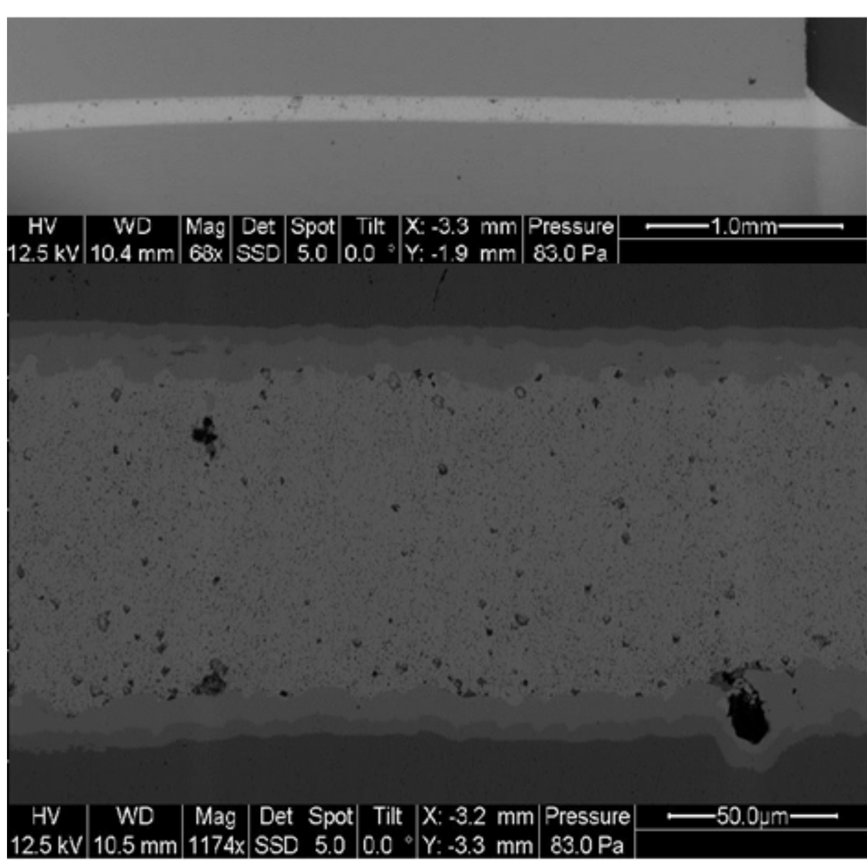


Figure 4-24: ESEM image of Sn3.5Ag solder joint after 100 hours isothermal aging at 185˚C

Here, ESEM analysis of samples isothermally aged at 185˚C and dropped with 1,500G acceleration is presented. Six joints between copper die and substrate (three TLPS (Ni-Sn3.5Ag) and three Sn3.5Ag samples) were isothermally aged for 0, 100, and 500 hours at 185˚C and dropped for 1,000 times from 19.3 inches (i.e. 1,500G). All specimens were cross-sectioned and analyzed by ESEM to detect possible cracks.

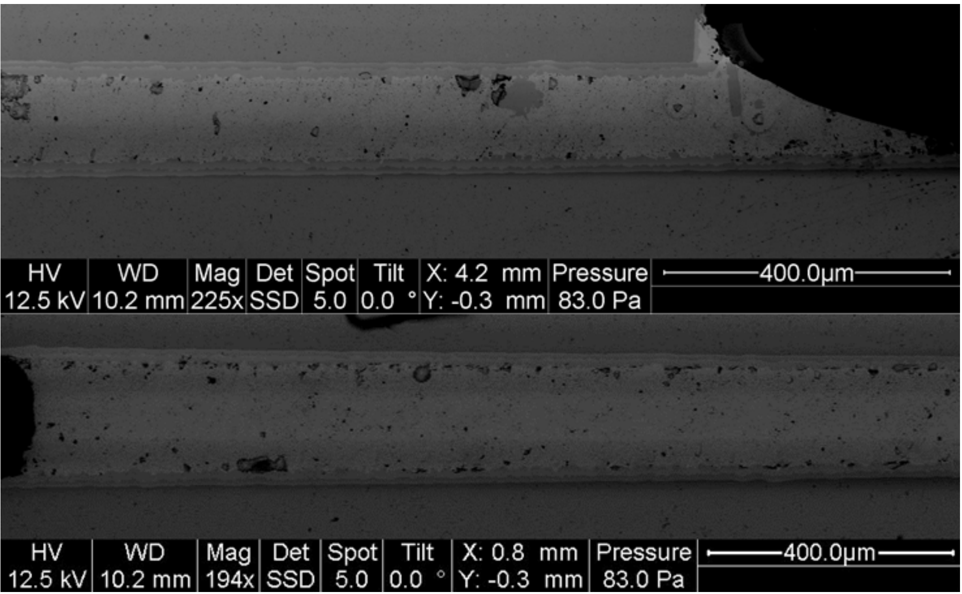


Figure 4-25: ESEM image of Sn3.5Ag solder joint after 500 hours isothermal aging at 185˚C

ESEM images of TLPS joint after 1,000 drops with 1,500G accelerations are presented in Figure 4-26 and Figure 4-27. This specimen was not exposed to aging and tested under mechanical shock right after the manufacturing process was completed. The joint kept its integrity and did now show any signs of detachment. The voids shown in Figure 4-26 are initiated during the manufacturing process; due to formation of IMCs on interface regions. A few small cracks were observed at the corner of the joint, which endures the most stress during dropping. Most of the cracks were initiated at the solder material and propagated along the edges of IMCs, shown in Figure 4-27.

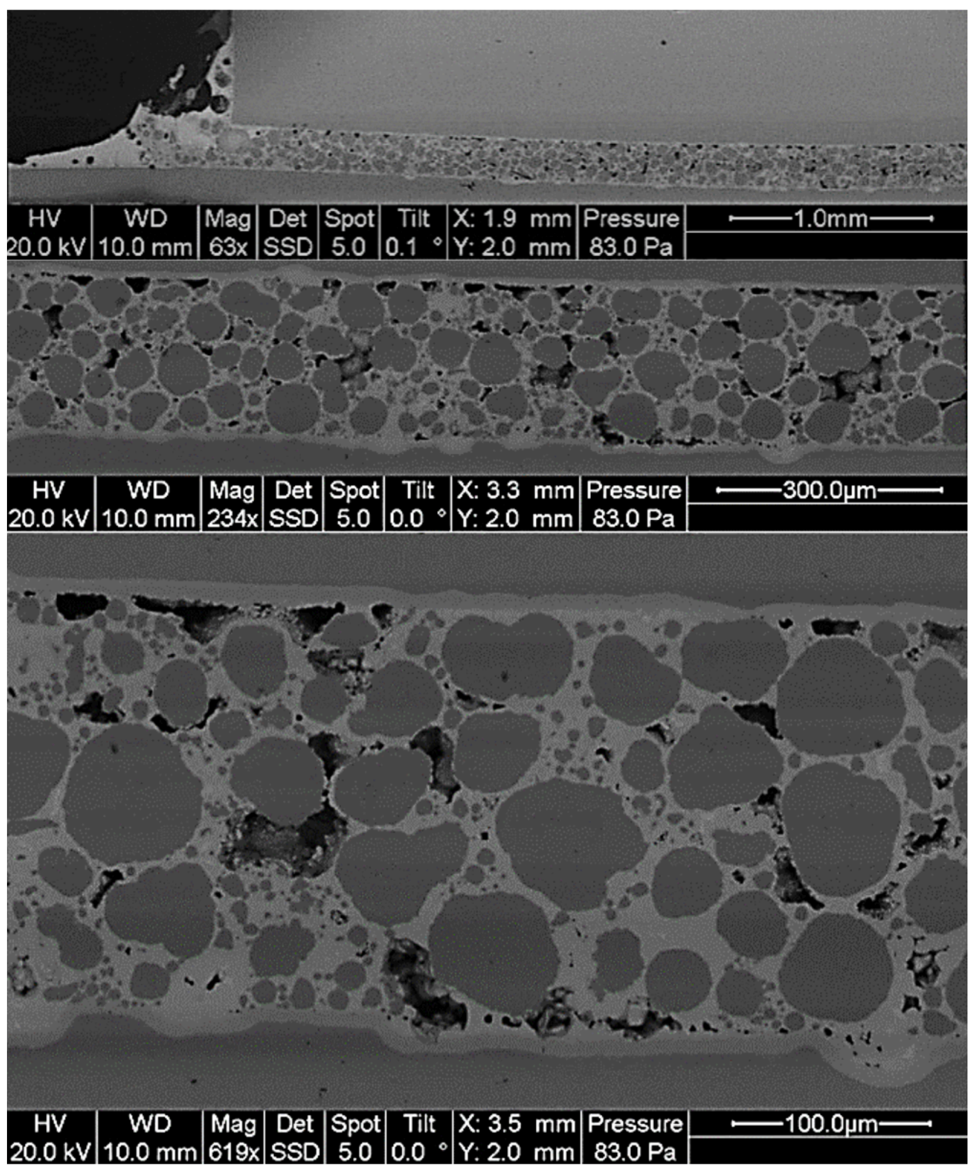


Figure 4-26: ESEM image of TLPS joint; after 1000 drops, no isothermal aging

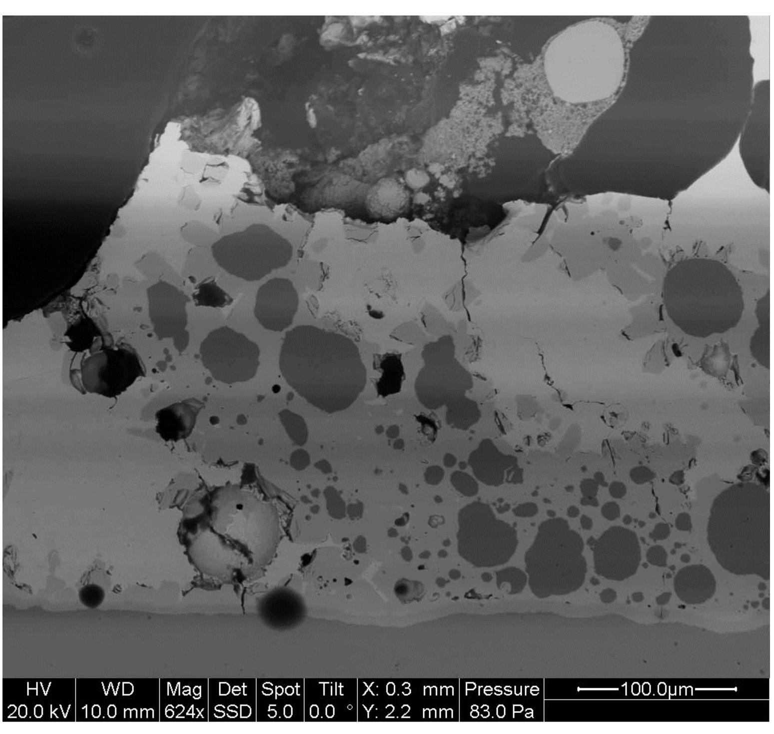


Figure 4-27: Cracks observed at the corner of TLPS joint; after 1000 drops (no isothermal aging)

Figure 4-28 shows the cross section of Sn3.5Ag sample after 1,000 drops (with 1,500G) without isothermal aging. The joint did not deteriorate under drop shocks. During ESEM analysis, no cracks were detected in the joint. At the left corner of the die, an accumulation of voids was observed. A small crack connected some of these voids, see Figure 4-29. There seems to be high potential for crack propagation at the interface of the die and solder material.

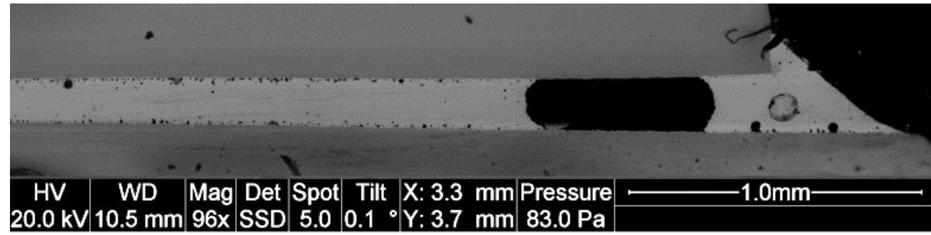


Figure 4-28: ESEM image of Sn3.5Ag solder joint; after 1000 drops, no isothermal aging

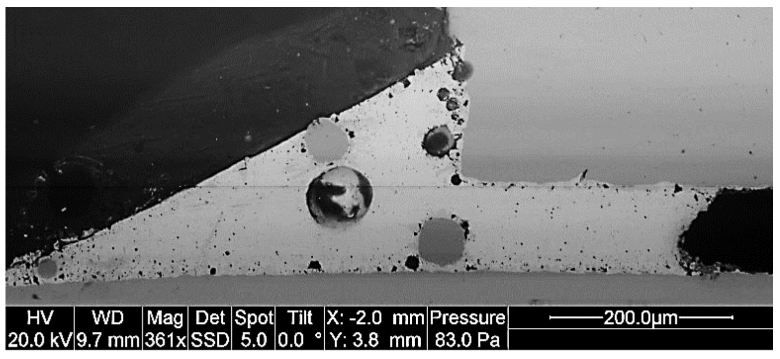


Figure 4-29: ESEM image of crack in Sn3.5Ag solder joint; after 1000 drops, no isothermal aging

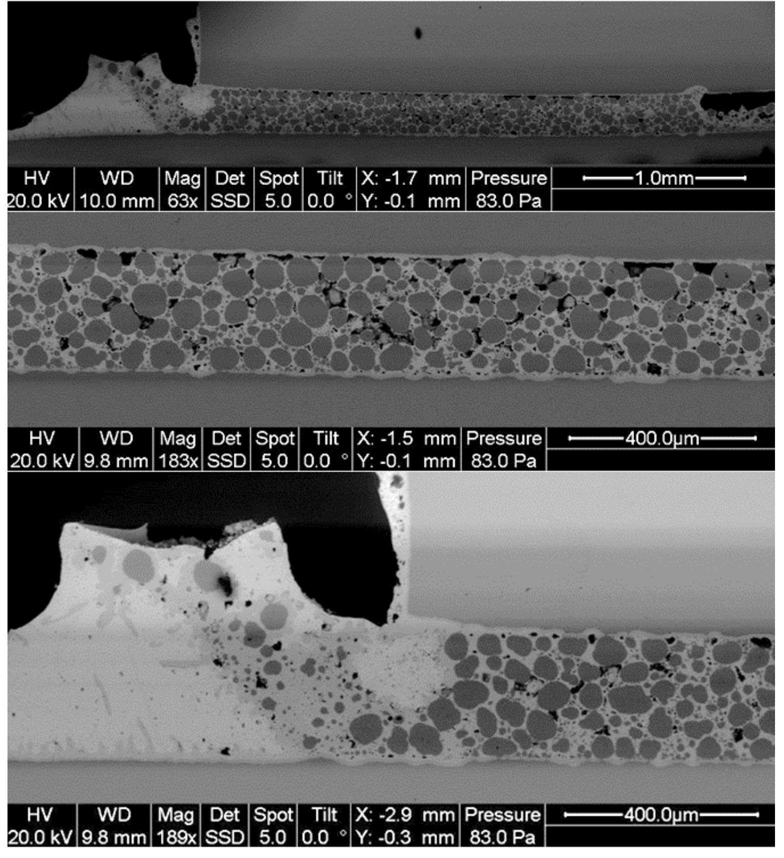


Figure 4-30: ESEM image of 100 hours isothermally aged TLPS joint; after 1000 drops

Figure 4-31 shows a solder joint cross-section after 100 hours aging at 185˚C and 1000 drops at 1500G. A big crack was observed at the right corner of the joint. This crack initiated from the side of the die and propagated towards the solder joint center. It continued along the interface of the joint and Cu substrate. A magnified image of this

crack is presented in Figure 4-32. Furthermore, another crack was detected on the left side of the joint (see Figure 4-33). The crack initiation is similar to that found for the crack on the right side of the solder joint. However, this crack did not propagate towards the Cu substrate, but rather into a void located below the Cu die. Multiple small cracks were observed at the lower interface. These are vertical cracks mainly propagated across the two Cu-Sn IMC layers. The magnified ESEM images of these cracks are presented in Figure 4-34 and Figure 4-35.

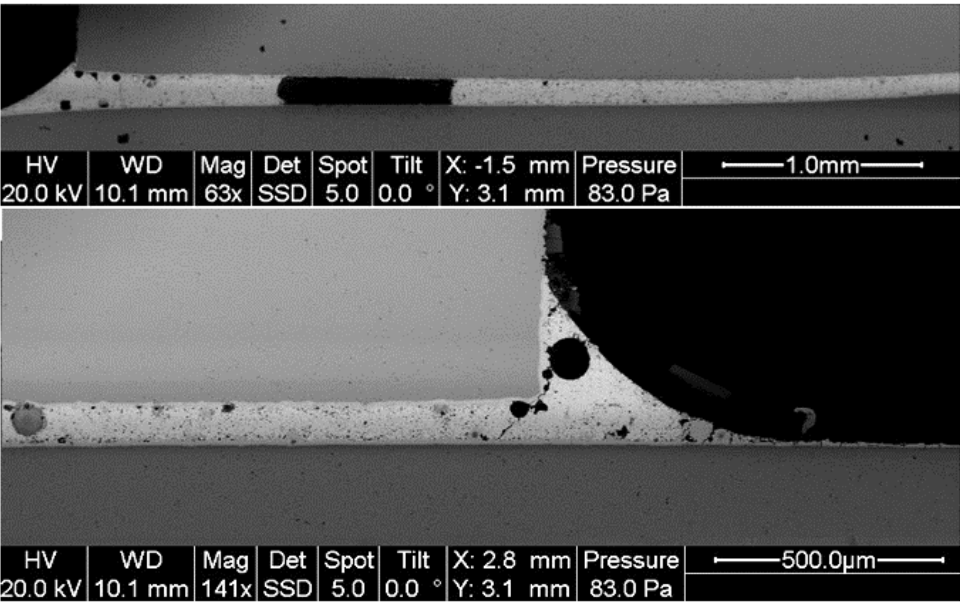


Figure 4-31: ESEM image of 100 hours isothermally aged Sn3.5Ag solder joint; after 1000 drops

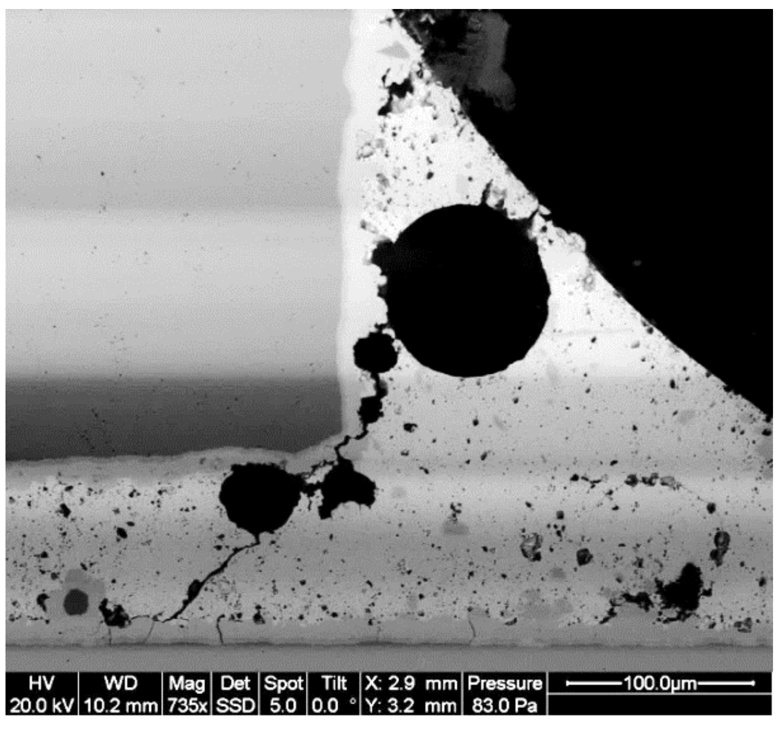


Figure 4-32: Magnified ESEM image of crack in 100 hours isothermally aged Sn3.5Ag solder joint; after 1000 drops (right corner)

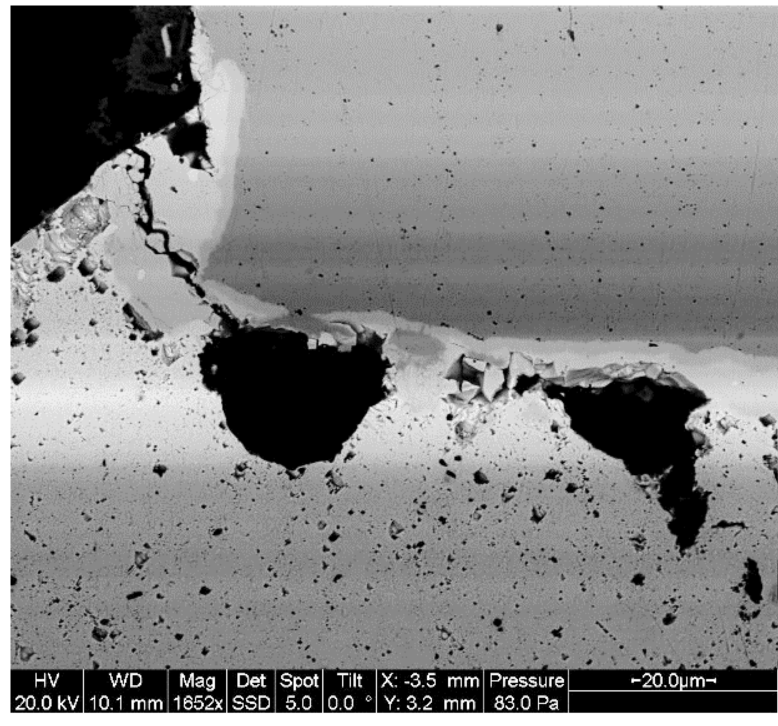


Figure 4-33: Magnified ESEM image of crack in 100 hours isothermally aged Sn3.5Ag solder joint; after 1000 drops (left corner)

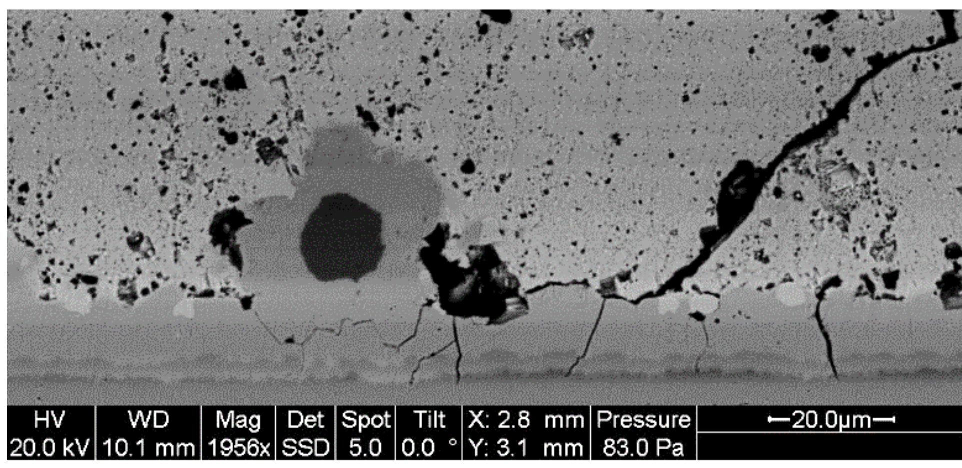


Figure 4-34: Magnified ESEM image of vertical cracks in 100 hours isothermally aged Sn3.5Ag solder joint; after 1000 drops (right corner)

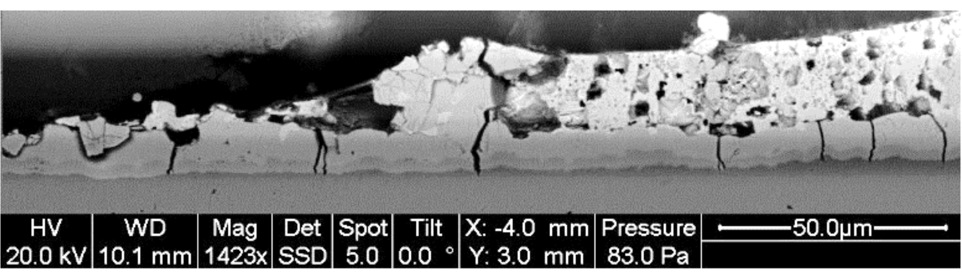


Figure 4-35: Magnified ESEM image of vertical cracks in 100 hours isothermally aged Sn3.5Ag solder joint; after 1000 drops (left corner)

ESEM image of cross section view of 500 hours aged (at 185˚C) TLPS joint after 1000 drops (with 1,500G) is presented in Figure 4-36. The specimen did not show any signs of deterioration. A few small vertical cracks were observed on the left side of the joint. The location of these cracks is shown in Figure 4-36 with a red circle. The magnified ESEM image of these cracks is presented in Figure 4-37. These cracks were found in areas outside the joint with localized starvation. These are not deemed critical for the integrity and reliability of the die-to-substrate interconnect. Some voids were detected on the upper interface of the joint.

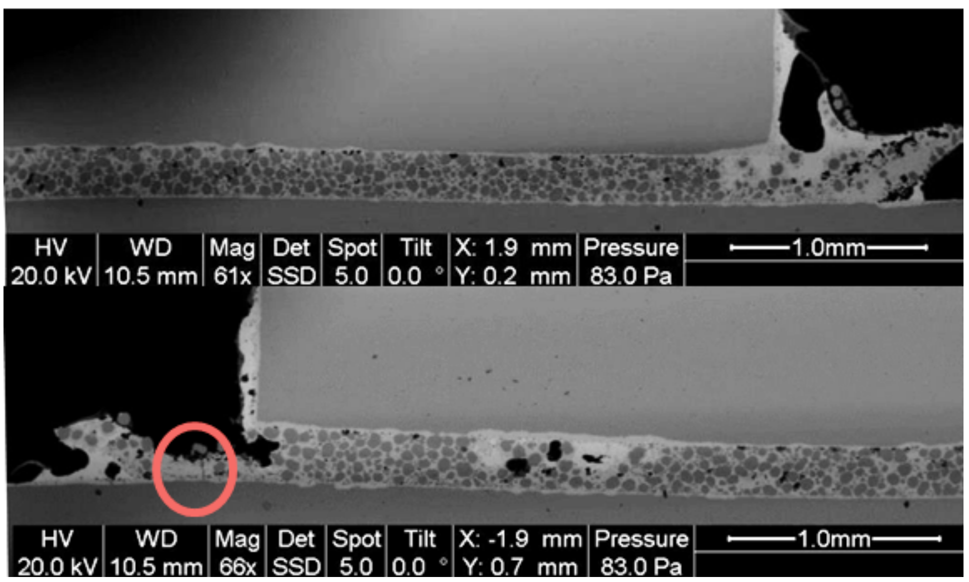


Figure 4-36: ESEM image of 500 hours isothermally aged TLPS joint; after 1000 drops

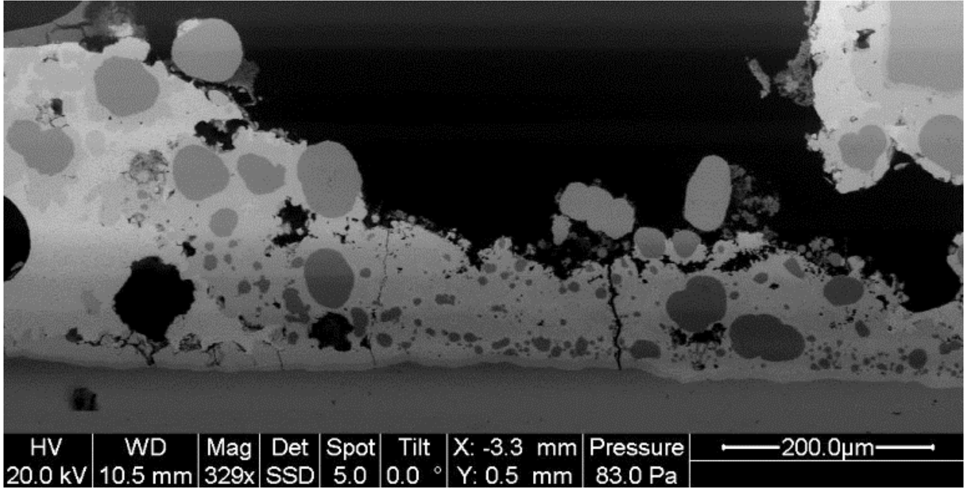


Figure 4-37: Magnified ESEM image of vertical crack in 500 hours isothermally aged TLPS joint; after 1000 drops (left corner)

Figure 4-38 shows the ESEM image of cross sectioned solder joint aged for 500 hours and dropped for 1000 times. A big crack was observed at the left corner of the joint. The crack was initiated at the side of the die and propagated at the solder to substrate interface of the joint. Figure 4-39 and Figure 4-40 show the crack propagation path and a detailed view of the fracture behavior. Two different failure modes are present: The vertical cracking through both IMC layers (Cu_6Sn_5 and Cu_3Sn) that has been described

above, as well as horizontal cracking along the solder-to-IMC interface. No horizontal cracking between Cu6Sn5 and Cu3Sn occurred. This indicates that the IMCs themselves are not the weakest element for drop shock reliability, but rather the interaction of the ductile solder and the brittle IMCs. Another crack was observed on the left side of the joint, see Figure 4-41. The crack initiation location is very similar to the right corner crack.

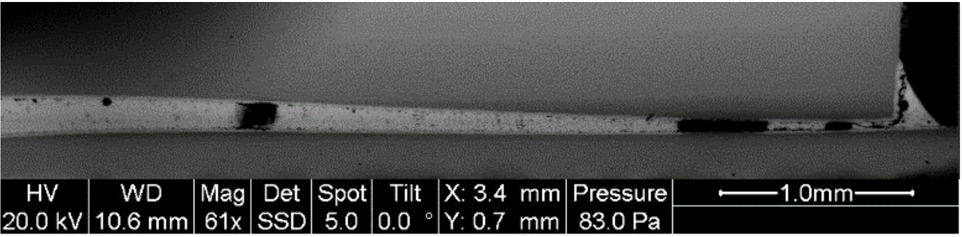


Figure 4-38: ESEM image of 500 hours isothermally aged Sn3.5Ag solder joint; after 1000 drops

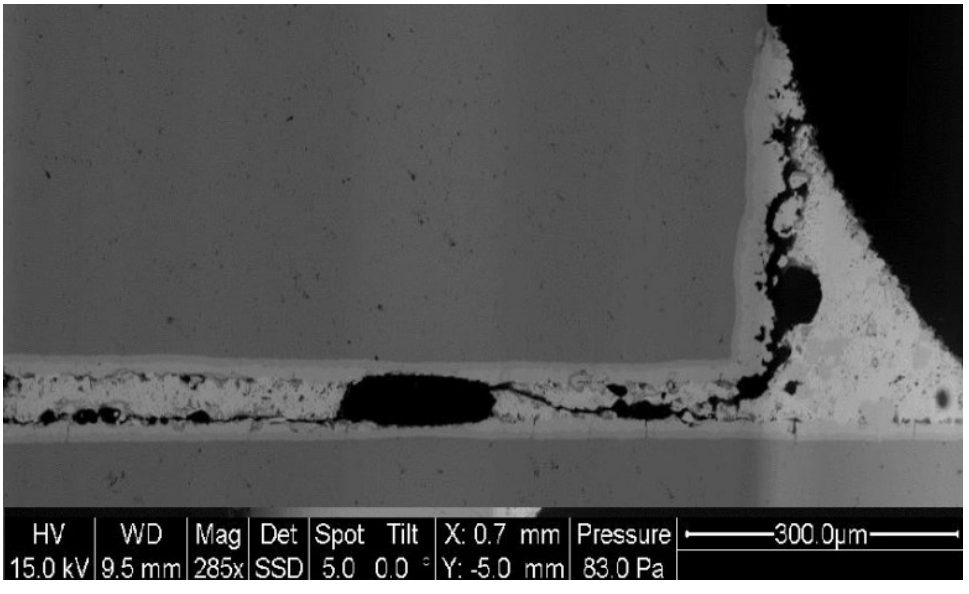


Figure 4-39: Magnified image of right corner crack presented in Figure 4-38

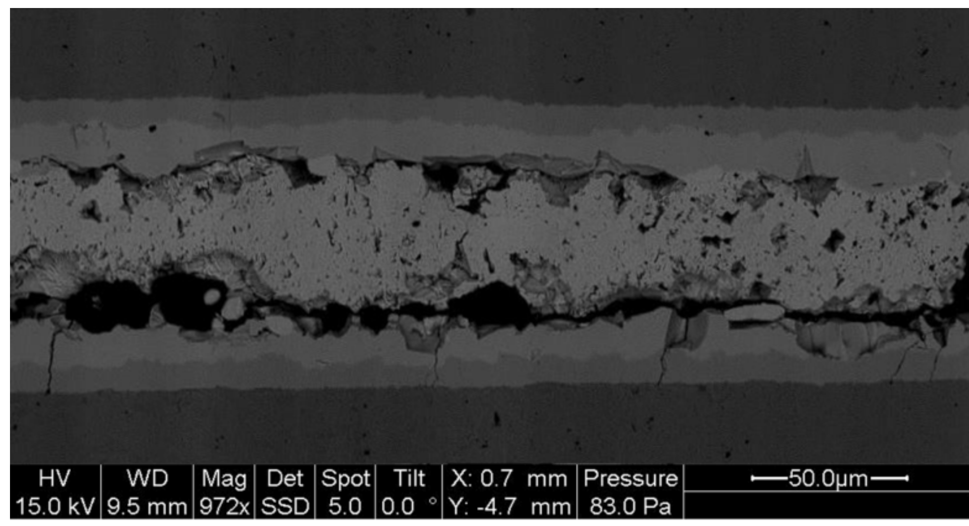


Figure 4-40:Fracture behavior of the Sn3.5Ag solder joint aged for 500 hours after 1000 drops of 1500G acceleration

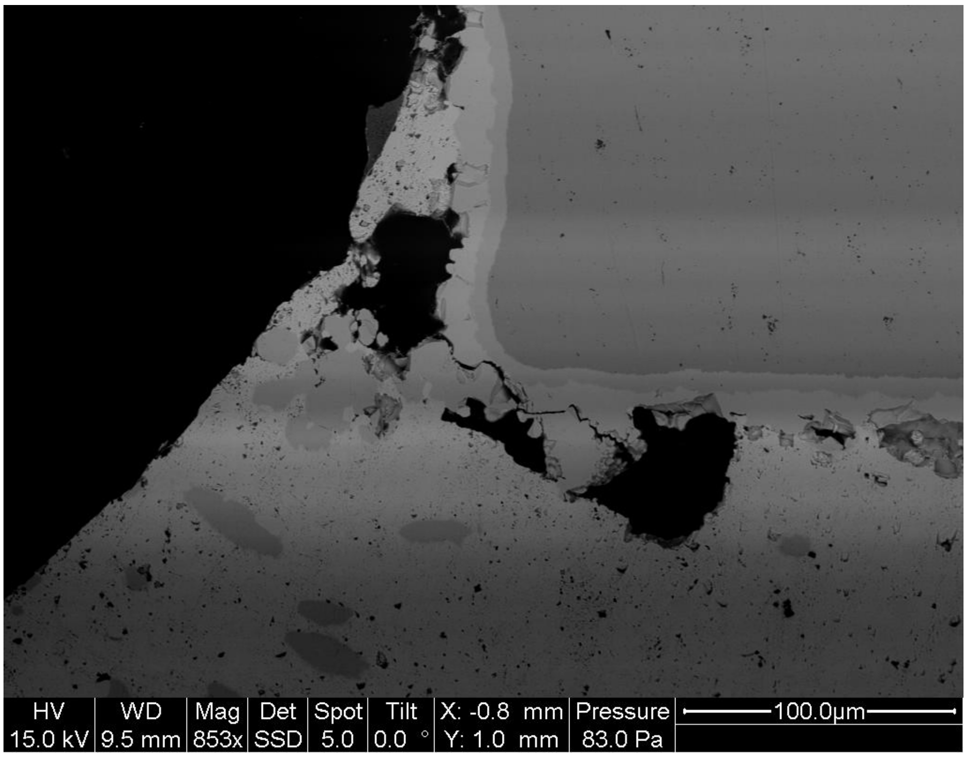


Figure 4-41: Smaller crack propagating from the left side of the Sn3.5Ag specimen after ageing for 500 hours and 1000 drops

In conclusion, the TLPS joint material showed better performance after aging under mechanical drop shock loading compared to Sn3.5Ag solder. Isothermal aging did not

influence the TLPS joint strength, even though it slightly increased the voiding level. In contrast, solder joints showed a significantly increased potential for crack initiation and propagation after isothermal aging. Two types of cracks were detected: Vertical cracks through the IMCs at multiple locations along the interfaces, and horizontal cracks through the solder joints. The horizontal cracks were initiated at the joint edge and propagated primarily towards the solder-to-substrate interface, between the solder and the IMCs. Increased aging time increased the crack propagation distance. It is hypothesized that the interaction of ductile solder and brittle IMCs are the most susceptible elements for accelerated failure under drop shock conditions. TLPS joints do not contain significant residual quantities of solder, and therefore show improved drop shock reliability.

<u>Power cycling</u>

The application of TLPS joints made of Cu-Sn on three types of power substrates (under power cycling loads) is investigated in this section. A commercially available silicon power diode was mounted on all three substrates and power packages were tested under power cycling loads. A test set-up was designed and assembled to perform power cycling and monitor the temperature of packages during cycling. Failed components were mounted in epoxy and cross-sectioned to prepare for optical and environmental scanning electron microscopies (ESEM). The failure modes and mechanisms were identified and future approaches were suggested.

Sample preparation

The main objective of this study is identifying failure mechanisms of TLPS interconnections under power cycling loads. For this purpose, three types of samples were prepared and a specific power cycling test setup was designed and assembled to identify the failure modes and mechanisms related to the application of TLPS interconnections. The three types of samples have the same TLPS joints made of Cu-Sn and power device (diode) while the substrates are different. The performance of the TLPS joints on different types of substrates provides the insight to clarify if the failure cause is related to the joint material or the substrate. Also, since different substrates are made of different materials, it is possible to compare the IMC interface layers on different surfaces. Figure 4-42 shows the cross section of the three types of substrates used in this study. The first substrate (DBA) is made of Al (~625 μm) on both sides of an AlN (~600 μm) layer. The second (Ni plated-DBC) and third (DBC) substrates are made of Cu (~290μm) layers on an AlN (300 μm) layer. The first two substrates (DBA and Ni plated+DBC) have 5 μm Ni plating on top and bottom sides of the substrate. These substrates are of high reliability and high temperature power electronic products manufactured and provided to us by Mitsubishi Material Corporation (MMC). A commercially available power diode was mounted on all power substrates, the schematics of package design are presented in Figure 4-43.

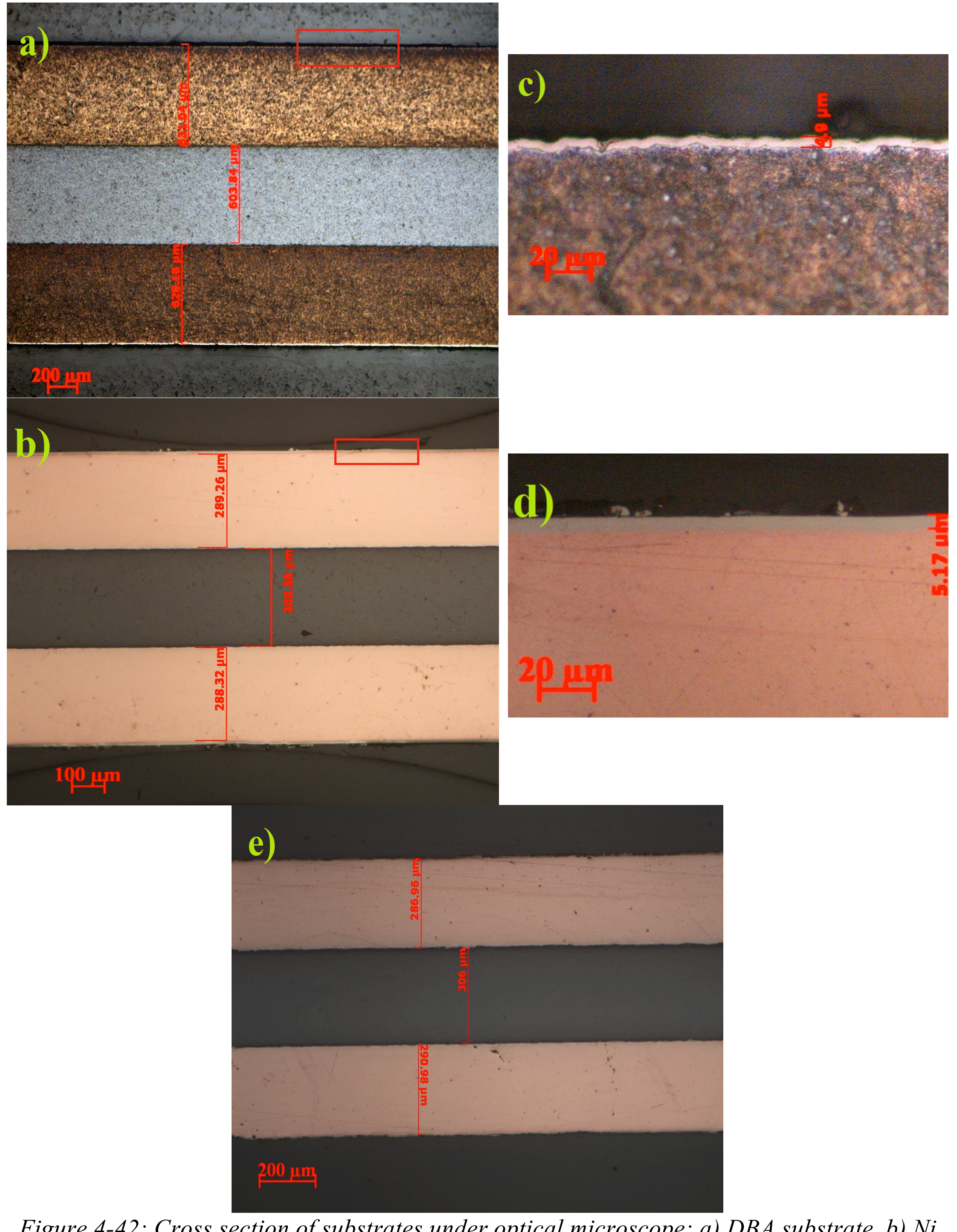


Figure 4-42: Cross section of substrates under optical microscope: a) DBA substrate, b) Ni plate DBC substrate, c) Nickel plating on the surface of DBA substrate; magnified image of the red-square area shown in image a, d) Nickel plating on the surface of DBC+Ni plated substrate; magnified image of the red-square area shown in image b, e) DBC substrate (without any plating)

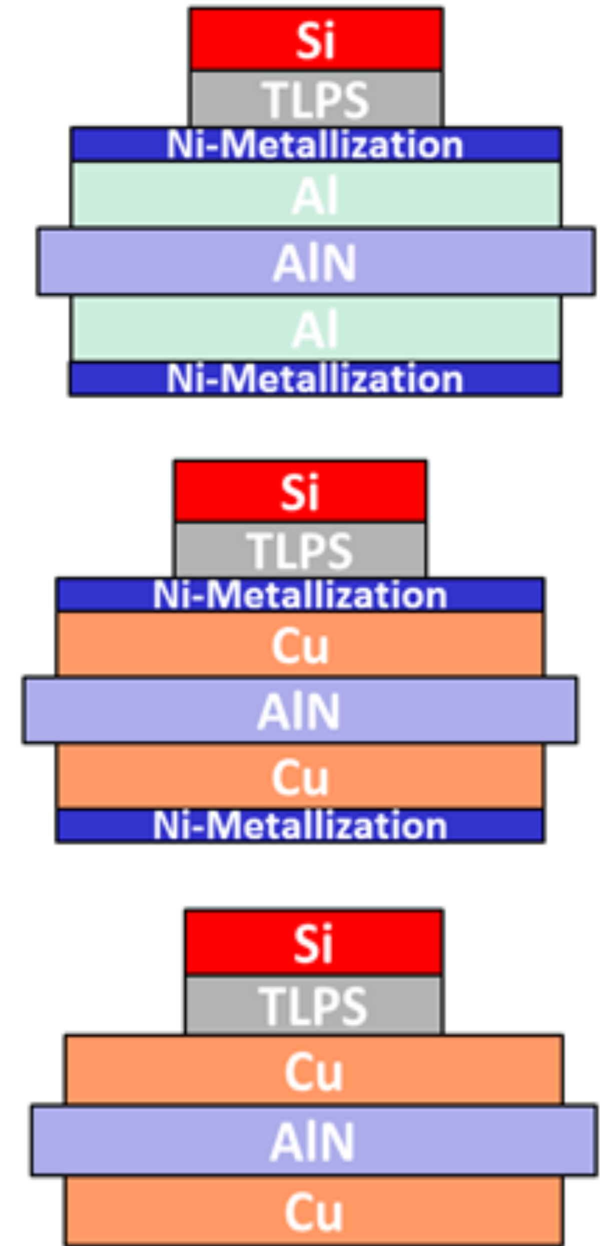
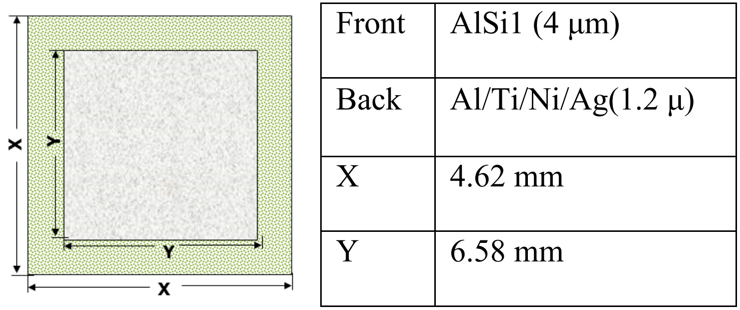


Figure 4-43: Schematic view of packages designed for the power cycling test

Commercially available silicon power diodes (dies) with 6.58×6.58×0.39 mm^3 dimensions and up to 50 amps current and 175˚C temperature ratings were used in the experiments. The assumed electrical failure modes for the diodes during power cycling are open circuit and shorting of the device. Therefore, the electrical performances of the devices were tested before mounting on substrates to filter the defective devices.

The metallization type and dimension of diodes on top and bottom surfaces are shown in Figure 4-44. Also, the forward voltage of the diodes based on the manufacturer's datasheet is 1.9 V at IF=50 amps and T=150˚C.



Front	AlSi1 (4 µm)
Back	Al/Ti/Ni/Ag(1.2 µ)
X	4.62 mm
Y	6.58 mm

Figure 4-44: Diodes' dimensions and metallization

The TLPS joint used in this section is made of Cu-Sn and prepared by the sintering method explained in previous sections. Figure 4-45 shows the cross section of one of the joints prepared on DBA substrate under environmental scanning electron microscope (ESEM). A porous matrix of IMCs containing copper micro-particles was formed between the power device and substrate surfaces. An EDS analysis was performed to identify different constituents at different locations of the IMC matrix. Figure 4-46 and Table 6 show the location of each spectrum and quantified results of the EDS analysis in the ESEM image, shown in Figure 4-45: ESEM image of TLPS joint prepared between a DBA substrate and power diode. Different IMCs can be identified from their slightly different shading/color in the ESEM images. Thus, the spectrums' locations were selected at regions with different colors/shading to present a comprehensive understanding of the IMC matrix. Three samples were made for each type of substrate (total number of 9 samples) and were tested under power cycling condition. An important point about the packages prepared and described in this section is that they only consisted of power device, TLPS joint, and power substrate; wire-

bonds were not used on the top surface of the diodes. Wire-bond connections were eliminated in our design to concentrate on the failure mechanisms related to die-attach issues. For this purpose, a specific power cycling test setup was designed and assembled which does not rely on wire-bond connections for electrical connection on the top surface of diodes.

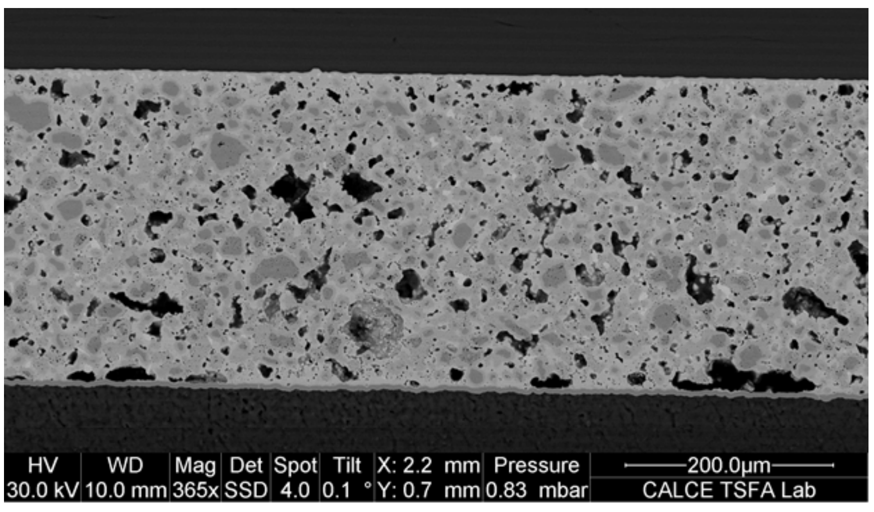


Figure 4-45: ESEM image of TLPS joint prepared between a DBA substrate and power diode

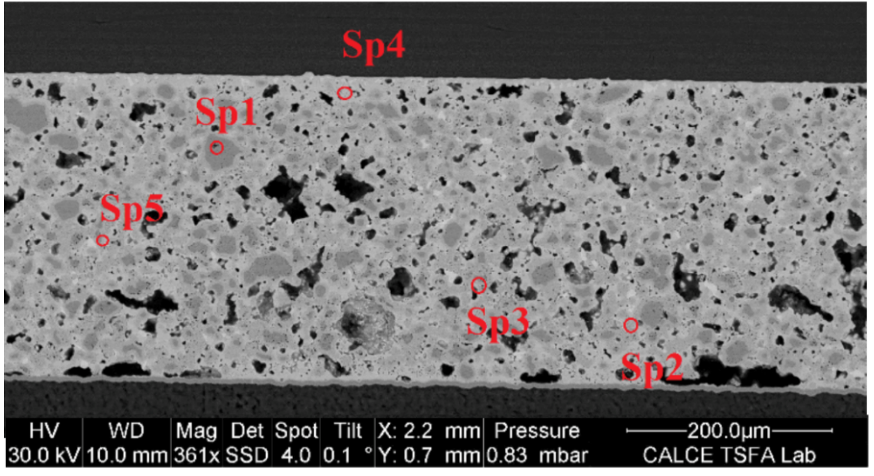


Figure 4-46: Location of five spectrums analyzed under EDS

Table 6: EDS analysis, constituents and their weight percentages at each spectrum (wt.%)

	Cu	Sn	Ag	Ni
Spectrum 1	93.70	6.30		
Spectrum 2	55.71	42.61	1.68	
Spectrum 3	54.12	45.88		
Spectrum 4	33.45	58.18	7.24	1.13
Spectrum 5	33.70	34.65	31.64	

Experimental setup

The assembled test setup was designed to power cycle power packages under repetitive electric loading while thermal condition is being monitored and recorded to a computer Figure 4-47. Main features of this setup are:

- Working at high current condition (limited by power supply capacity, i.e. 300 amps in our study)
- Working at high temperatures (up to limits of commercially available power devices: i.e. 175˚C)
- Rapid cooling
- Temperature monitoring (up to 105Hz sampling rate)
- Automatic heating and cooling processes
- Catastrophic failure prevention control

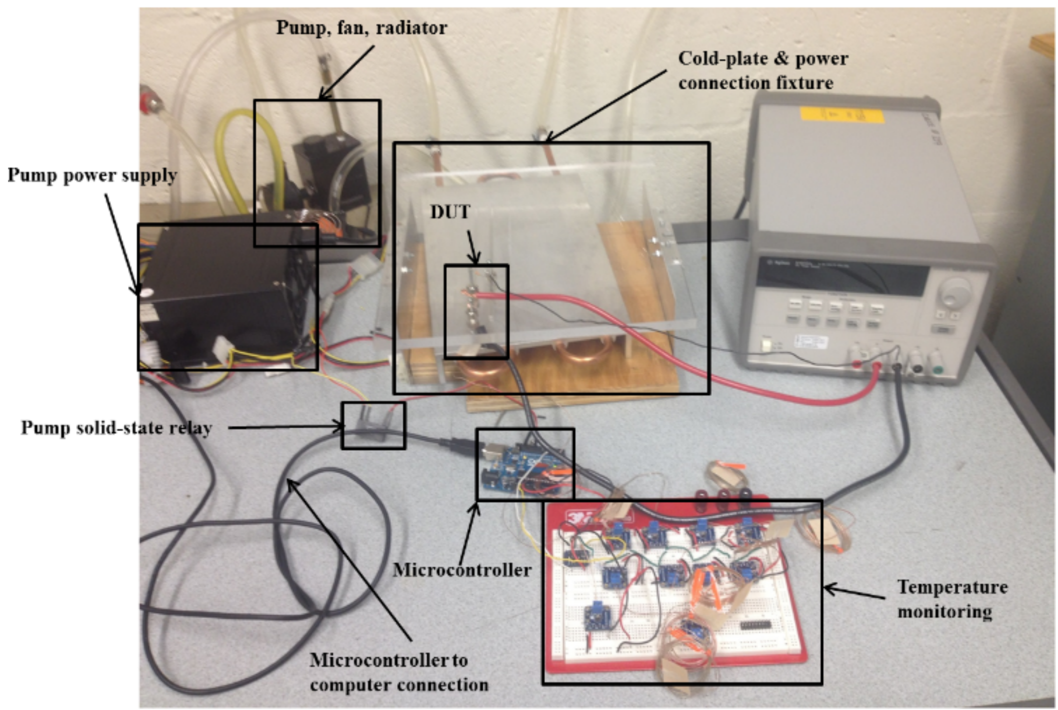


Figure 4-47: Overall view of the power cycling test setup prepared for testing UUT without wire-bonds

Three major modules considered in the design of power cycling setup (PCS) are electric, thermal and control modules. Electric module, which provides the current to the unit under test (UUT), is an electric circuit consisting of a power supply, high current wires, and switches. The main feature of this module is its independence from wire bonds by using flexible copper springs for top side connection of the diodes, Figure 4-48. Two switches are considered for controlling the electric loads; one, for normal duty cycle control and the other one for stopping the current in case of emergency and overheating. The electric module works with opposite duty cycles to thermal module.

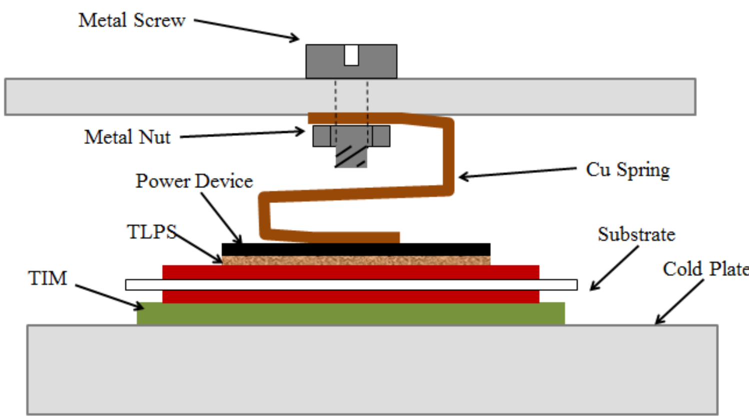


Figure 4-48: Schematic of Cu spring connection used instead of wire-bonding

The thermal module, which cools down the device temperature during OFF duty step and prevents it from overheating, consists of a cold-plate, pump, radiator-fan, switch, and a power supply. During OFF duty step when the electric loop is off, it is preferred to cool down the device to room temperature with a fast cooling rate to increase the number of cycles in per time. A cold-plate using water as cooling fluid was used to increase the cooling rate of thermal module. Power devices were placed on top of the cold-plate with a thermal interface material (electrically insulating). The water flows through the cold-plate pipes with a small pump. During ON duty step, the pump stops and the water will stay stationary in the cold-plate. The thermal module performance is controlled by a switch which turns on/off by control module's commands.

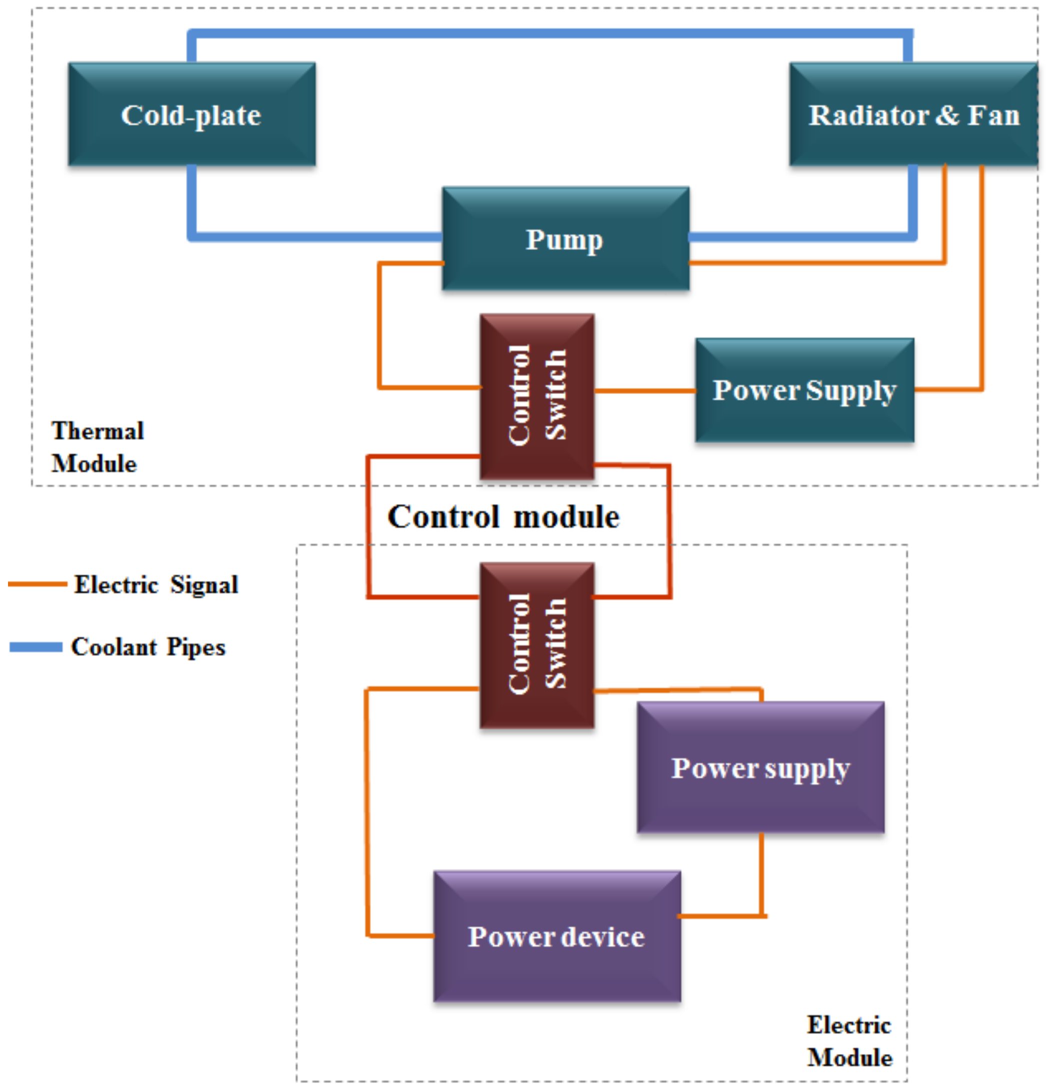


Figure 4-49: Schematic diagram of three modules considered in power cycling setup

The most important part of power setup is the control module. It delivers tasks such as measuring and recording UUT temperature, defining duty cycle periods, switching thermal and electric modules, and catastrophic failure check and prevention. This module includes two submodules: 1. Monitoring submodule which consists of thermocouples to measure power device temperature, a data-logger to cyclically read the thermocouples and record the values to a computer. The thermocouples used in this setup are connected to the top surface of diodes through a non-conductive adhesive

layer with up to 175˚C temperature limit. 2. Control/decision submodule which commands the switches in electric and thermal modules, continuously checks the recorded temperatures by the data-logger with pre-defined limits of the setup, and shuts down the system in case of emergency. All these functions are programmed in an Arduino UNO microcontroller which works in connection with a computer. Schematic diagram, presented in Figure 4-49, shows three modules of PCS and how they connected to each other. Figure 4-50 shows the detailed logic of control module and how it controls electric and thermal modules are connected.

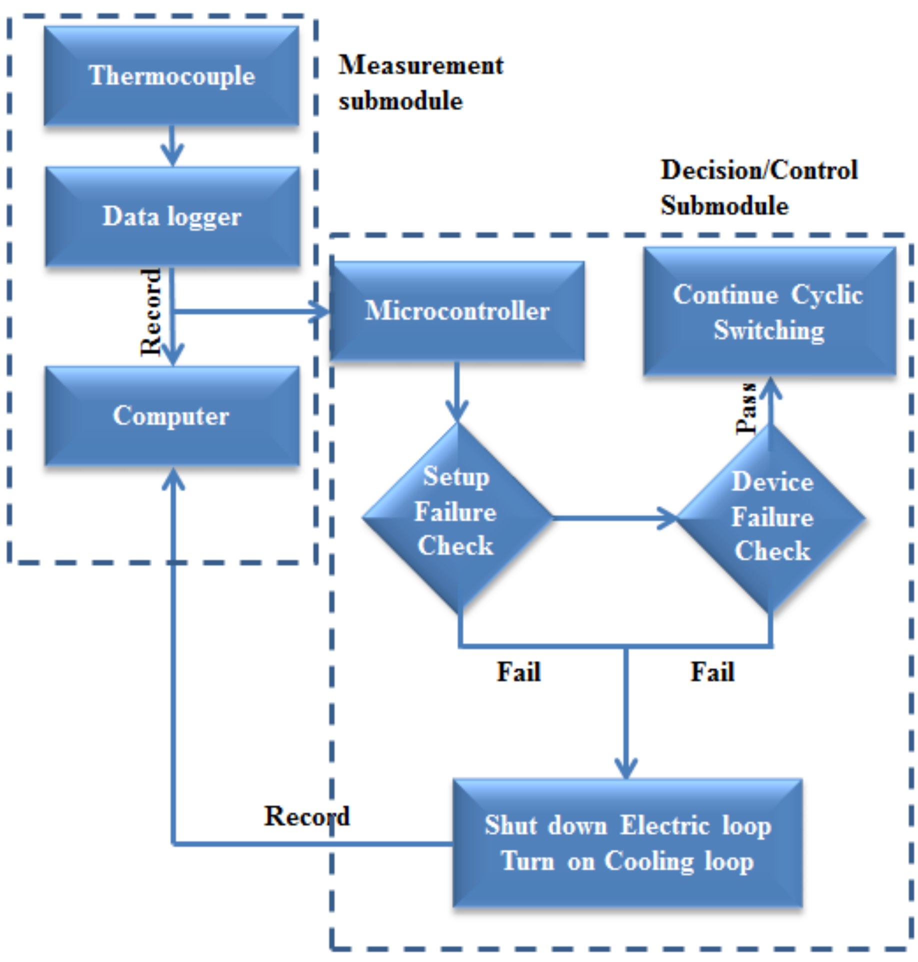


Figure 4-50: Schematic diagram of logic used in the submodules of the control module and their connection

Test procedure

The prepared samples were placed on an electrically insulating thermal interface material on the cold-plate and copper spring ribbons were placed on the top surface of diodes and substrates. The diodes were connected in series pattern by connecting metal screws attached to the copper springs Figure 4-48 with high current rating copper wires. The samples were tested under fixed electric loading conditions (i.e. 35-50 amps) with 15s ON/20s OFF duty cycles. This resulted in different temperature swings at different samples due to joint quality and substrate differences. Each diode's temperature was measured by a thermocouple attached to its surface every second. The microcontroller decides when to stop the test based on two criteria: first, 30% overheat in device temperature, and second, continuous decrease in temperature swings which demonstrates that diode shorted. The failed devices were removed from the set-up and the test continued until all samples failed. The failed devices were investigated electrically to identify the failure mode, such as short-circuit in diode. Then the samples were mounted in epoxy and cross-sectioned to identify failure mechanism under optical and electron microscopy.

Results and discussion

Power packages prepared in previous sections were tested under power cycling condition until failure. The main objective of this study was to define the end of life failure mechanism of these packages to identify the limitations of TLPS interconnections and find approaches to improve the reliability. It was expected of power packages to work under power cycling loads for hundreds of thousand cycles (or even millions) [103] but this objective was not fulfilled in this experiment. Samples

prepared on DBA substrates survived up to one thousand cycles; however, most of the samples prepared on the other substrates failed during the first tens of cycles. Figure 4-51 shows the number of cycles to failure for different packages (substrates) with respect to the temperature swing during power cycling. In addition to previous samples, sintered silver and tin solder were used on DBA to compare the results with TLPS interconnections.

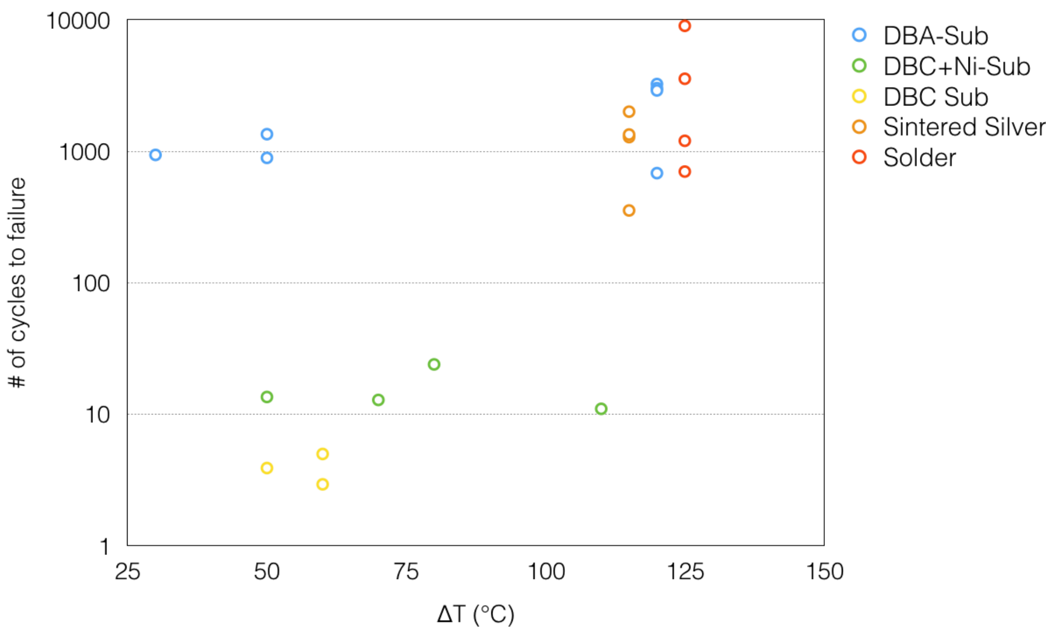


Figure 4-51: Number of cycles to failure with respect to temperature swing

Figure 4-51 shows that packages fabricated on DBC substrates fail faster than the other types of packages. DBA substrates showed the best performance compared to the other packages; however, the maximum number of cycles obtained by this type of substrate is ~1300 cycles. The failure was detected observing a drop in the maximum temperature during power cycling due to shorting of the diodes. Short-circuit was the main failure mode observed in all the samples. In some samples this failure mode occurred after several cycles of over-limit temperature increase in the diodes. Failure in TLPS joints

or substrate or even small cracks in the diode can cause such temperature increase. To further investigate the failure mechanism and cause, different types of packages were mounted in epoxy and cross-sectioned. The cross-sectioning process was done until observing a crack in one component of the packages.

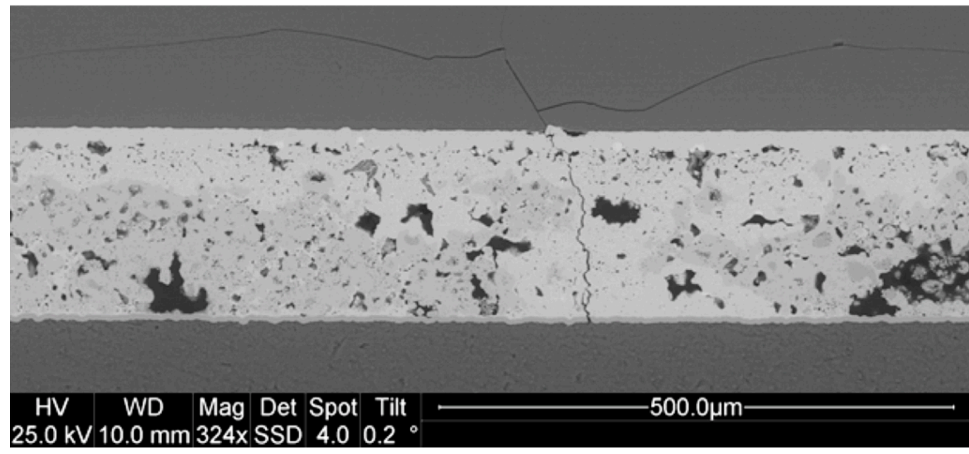


Figure 4-52: Vertical crack in TLPS joint that induced diode fracture (DBA)

Figure 4-52 shows cross section of cracks observed in DBA power cycling sample. Similar behavior was observed in other specimens as well. The samples had similar temperature swing (50˚C) during power cycling and failure mode (diode electrical breakage). The cross-section view of the samples shows that vertical crack through the TLPS joints propagated and reached the attached surfaces on both sides of the joints. Furthermore, the cracks initiated horizontal or vertical cracks in diodes' chip.

Further investigations showed that though these cracks damaged the package integrity, they are not the main cause of diodes' failure. Monitoring the temperature swings over periods of one hundred cycles shows that the temperature swing does not increase considerably. Therefore, it can be concluded that vertical cracks do not affect thermal and electrical performance of the package, considerably. The common failure mode in all diodes was shorting. Visual investigation of diodes shows arc roots on the surface.

Monitoring the sample during power cycling showed that imperfect connection of top surface to the copper band creates a small gap to form high current arcs. The arc's high temperature and current result in the failure of diodes.

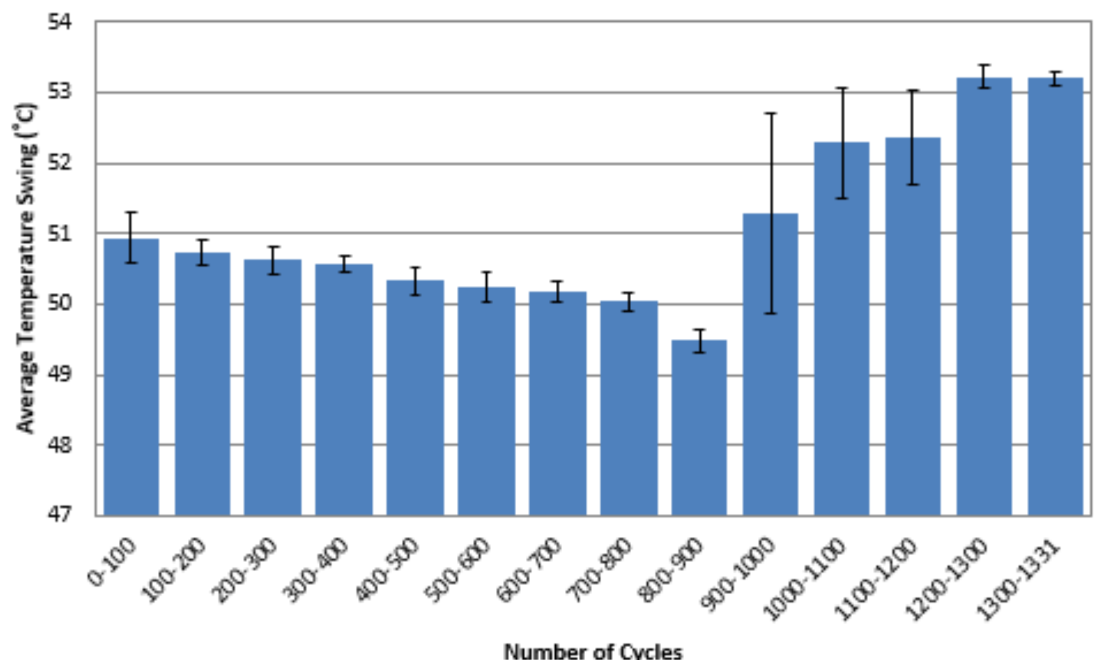


Figure 4-53: Mean and standard deviation of temperatures measured over 100 cycles period until failure for a DBA package

An interesting observation in this experiment was the interaction of cracks and power substrates. The cracks did not propagate through the copper part of the DBC and DBC+Ni substrates. But it moved into the aluminum part of DBA substrate. The lower elastic modulus of aluminum compared to copper helps to dissipate some strain energy. DBC substrates do not allow the fracture to penetrate the substrate beyond the intermetallic layers. Figure 4-54 shows the crack route of three types of packages at interface of TLPS joints and substrates. This could affect the performance of these packages under thermal loadings.

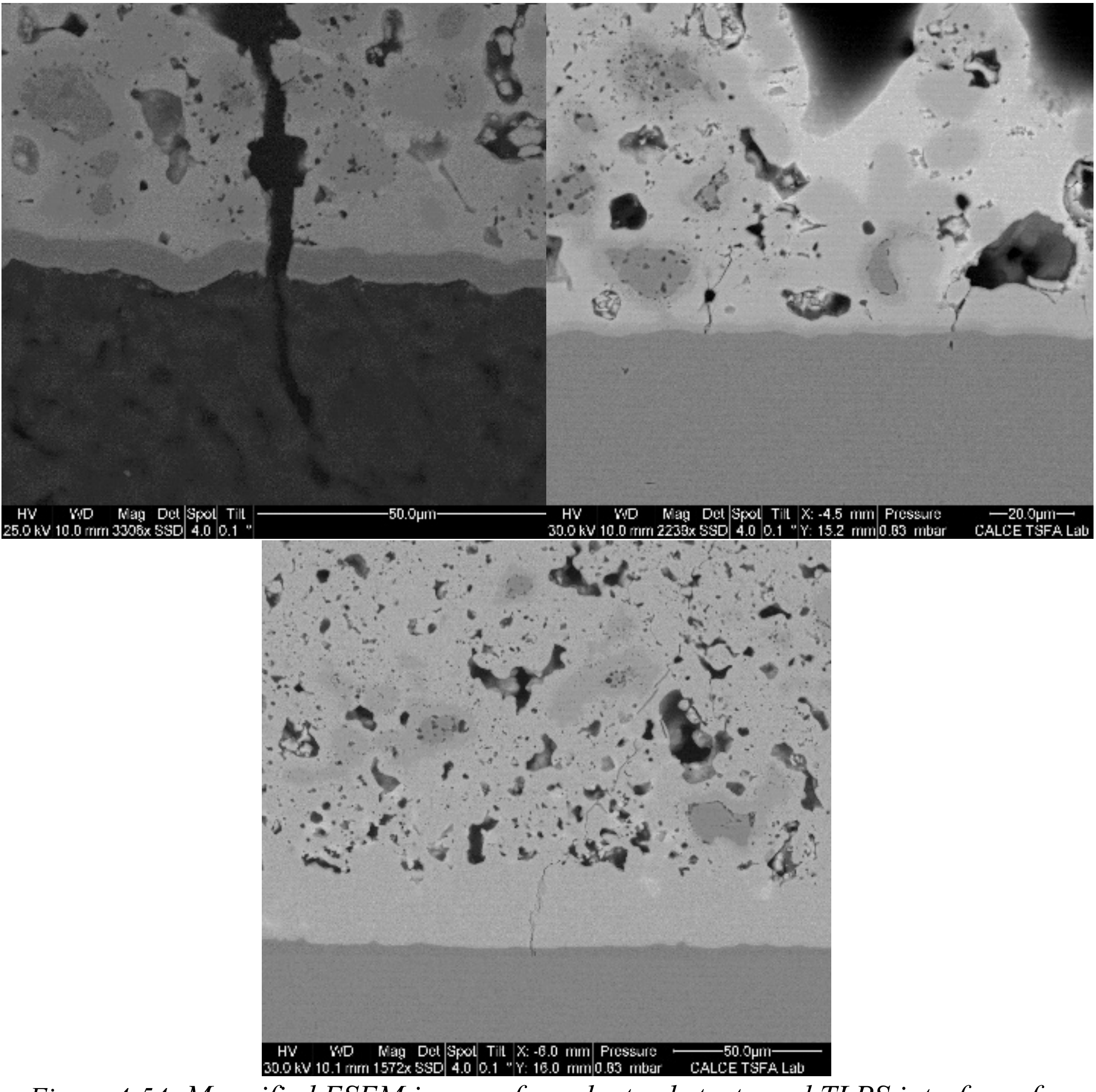


Figure 4-54: Magnified ESEM image of crack at substrate and TLPS interfaces for three types of substrates (DBA: top left, Ni plated DBC: top right, DBC: bottom)

Thermal cycling

Power electronic packages experience cycling thermal loading during their life. In this section, the performance of different types of die-attach materials under thermal cycling load between is investigated.

Sample preparation and test procedure

Three types of die-attach (Sn-Cu solder, sintered silver, and Cu-Sn TLPS) were used to mount a commercial silicon diode (5LSY 86E1200, ABB) on two types of substrates

(DBA and AMB substrates). The substrate properties and features are defined in the power cycling section of this chapter. The substrates were plated by a thin layer of silver and nickel layer for silver sintering, and solder/TLPS processing, respectively. Commercial Sn-Cu solder sheets (thickness = 150µm) were heated to 300°C in vacuum and reduction furnace to bond die and substrates. For sintered silver, Nano Tach-X, NBE tech LLC paste were stencil printed on each substrate with 50 µm and processed at 250ºC for 30 minutes. The TLPS samples in this section were prepared with two-step processing introduced in previous chapters.

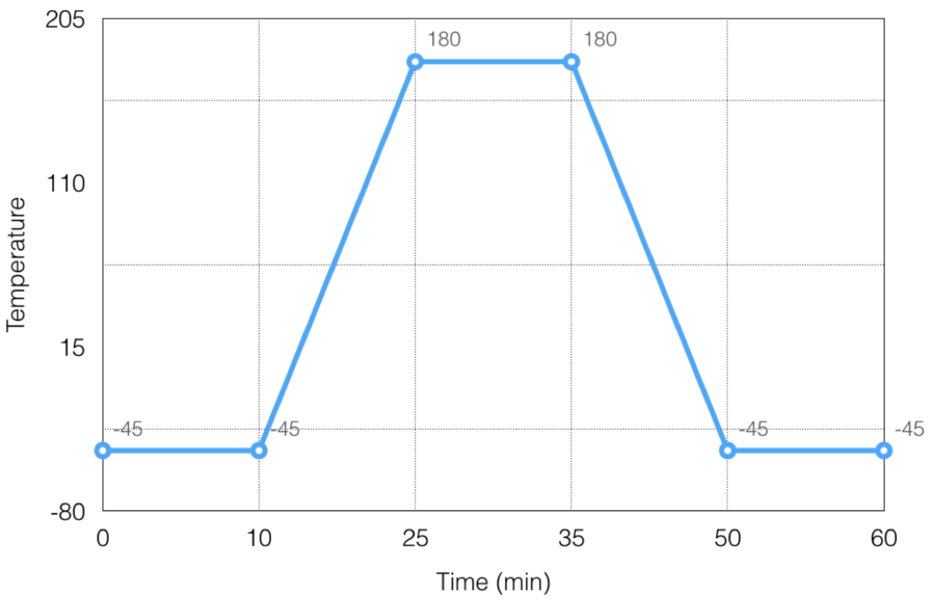


Figure 4-55: Thermal cycling profile

Thermal cycling was performed in Sun electronic furnace. Figure 4-55 shows the thermal profile used in this experiment. The profile consists of four steps: 1) Dwell time at low extreme temperature (-45°C) for 10 min, 2) Heating ramp to extreme high temperature (200°C) with 15°C/min rate, 3) Dwell time at high extreme temperature (200°C) for 10 min, and 4) Cooling ramp to extreme low temperature (-45°C) with

15°C/min rate. Die-attach were examined every 100 cycles for fracture propagation with Scanning Acoustic Microscope (CSAM). Substrates were mounted and cross-sectional observation of microstructure was demonstrated.

Results and discussion

Figure 4-56 and Figure 4-57 show different interconnection technologies status under CSAM at the start of the test, 300, and 900 cycles on DBA and DBC, respectively. The bright spots show defects (voids or fractures) in the attachment. In both scenarios, the defects increase with respect to the number of cycles; however, it is more sever for attachments on DBC substrates. Since aluminum has a lower yielding strength and elastic modulus compared to copper, its plastic deformation absorbs some of the CTE mismatch deformation energy and decreases attach degradation.

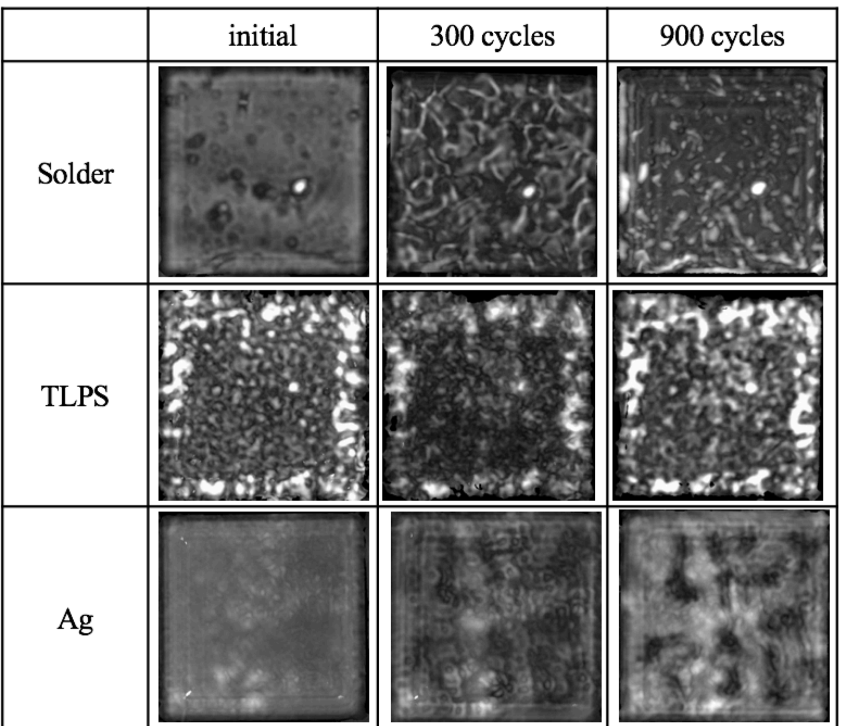


Figure 4-56: CSAM inspection of under each die-attach technology on DBA substrates

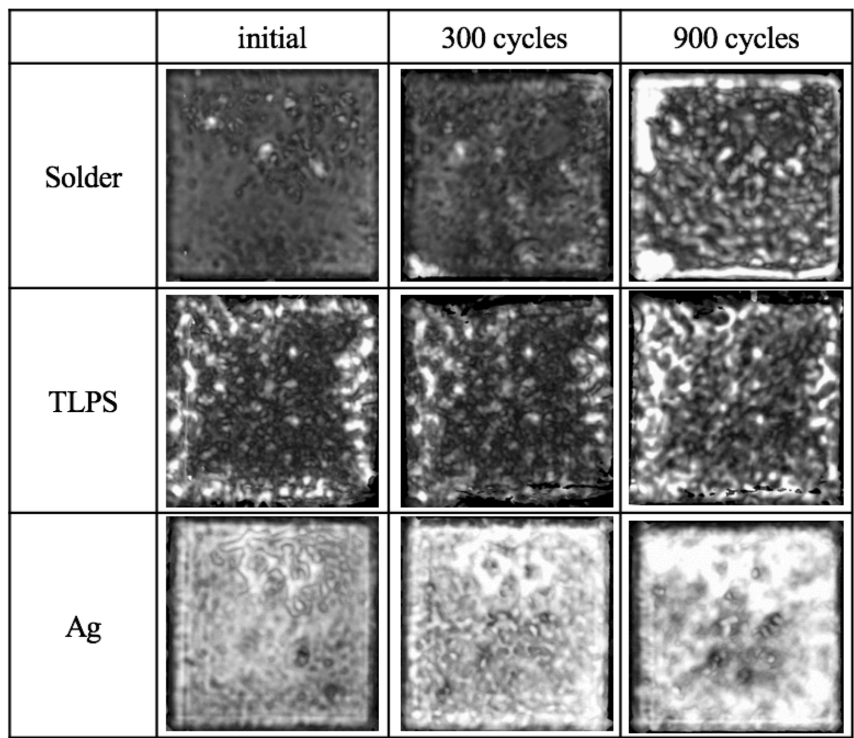


Figure 4-57: CSAM inspection of under each die-attach technology on DBC substrates

Figure 4-58 - Figure 4-61 show the ESEM cross-section of solder die-attach on DBC and DBA after 300 and 900 cycles. For DBC, the solder cracked at the edge and started detaching from the silicon diode. The detachment occurs at the IMCs formed at the top interface. For DBA, since both aluminum and solder have low yielding strength deform during thermal cycling. This prevents severe detachments like what solder attaches experience on DBC substrates; however, vertical cracks still occur at the bottom interface and accumulation of these cracks results in joint degradation and complete destruction.

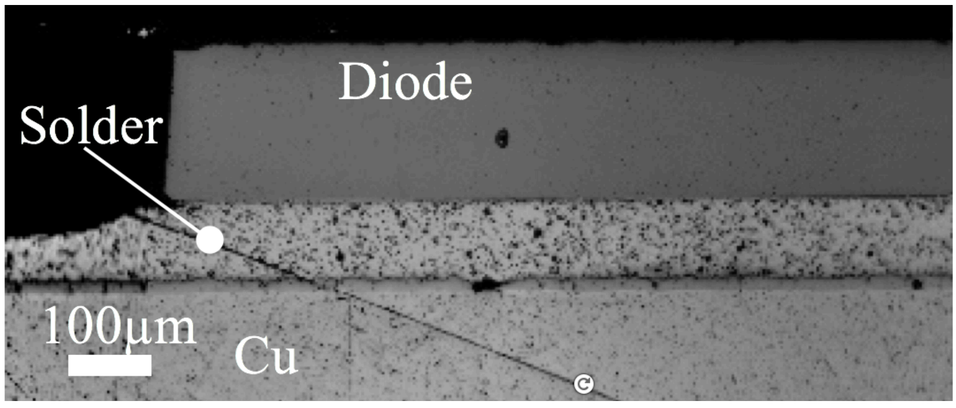


Figure 4-58: Cross-section image of the solder die-attach on DBC substrates after 300 cycles

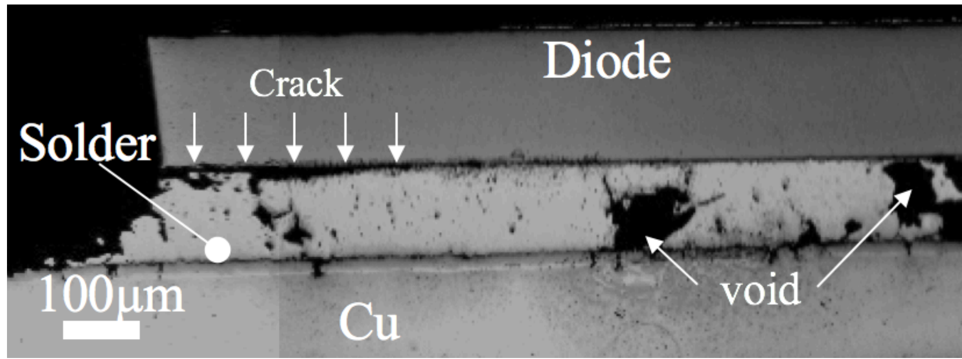


Figure 4-59: Cross-section image of the solder die-attach on DBC substrates after 900 cycles

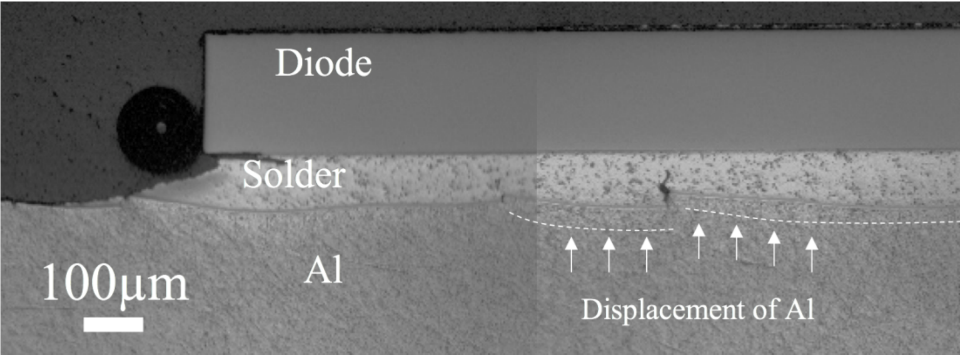


Figure 4-60: Cross-section image of the solder die-attach on DBA substrates after 300 cycles

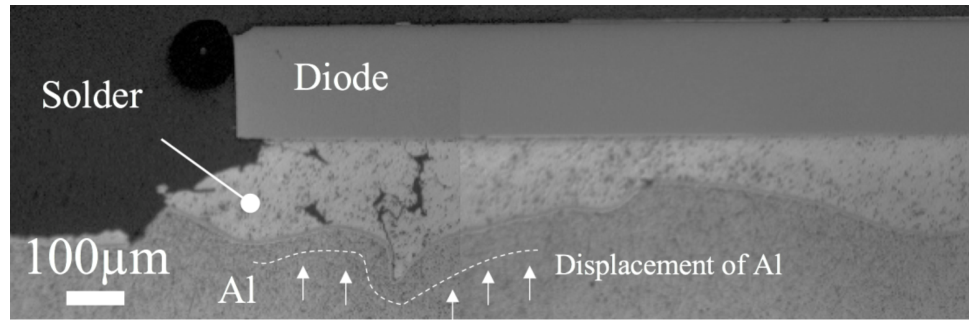


Figure 4-61: Cross-section image of the solder die-attach on DBA substrates after 900 cycles

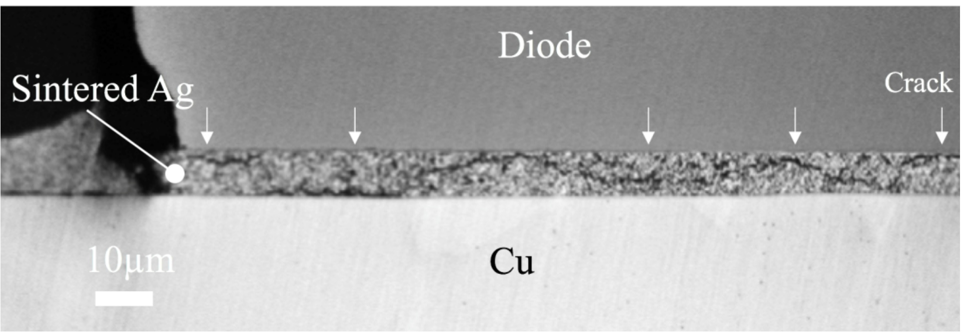


Figure 4-62: Cross-section image of the sintered-Ag on DBC substrates after 900 cycles

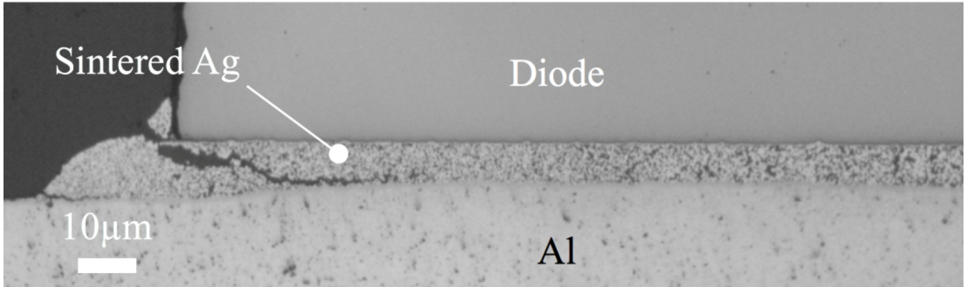


Figure 4-63: Cross-section image of the sintered-Ag on DBA substrates after 900 cycles

After 900 cycles, the sintered silver shows considerable degradation under thermal cyclic loads. Same as the solder, the degradation is more severe on DBC substrates. Figure 4-63 and Figure 4-62 show silver sintered attachments cross-section on DBA and DBC substrates after 900 cycles under ESEM. It is obvious that sintered silver on DBC is significantly damaged and is close to complete disconnection. The higher yield strength and elastic modulus of silver compared to solder prevents major deformation in the DBA surface (aluminum); however, its homogenous porous structure, shown in

Figure 4-64, creates an easy path for the cracks to propagate and damage the interconnection.

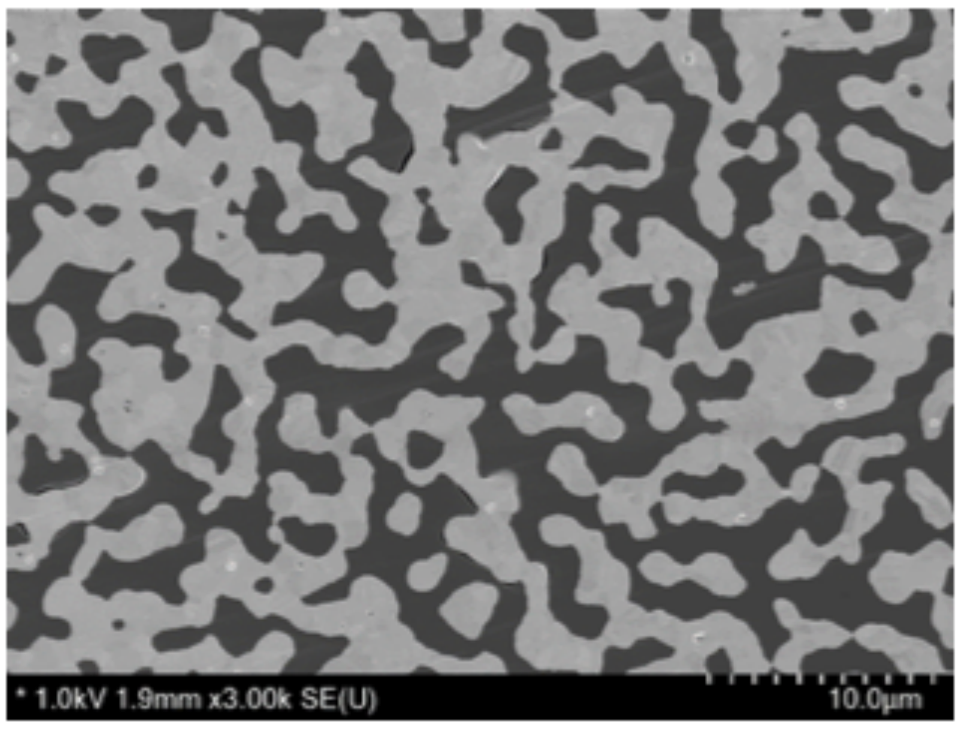


Figure 4-64: Sintered silver high magnification structure

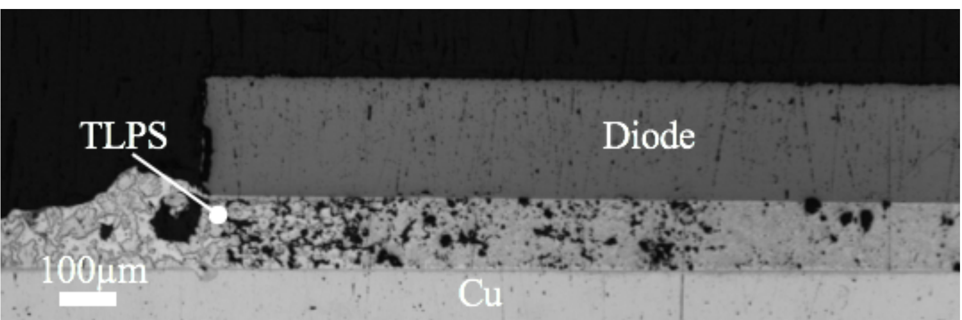


Figure 4-65: Cross-section image of the sintered-Ag on DBC substrates after 900 cycles

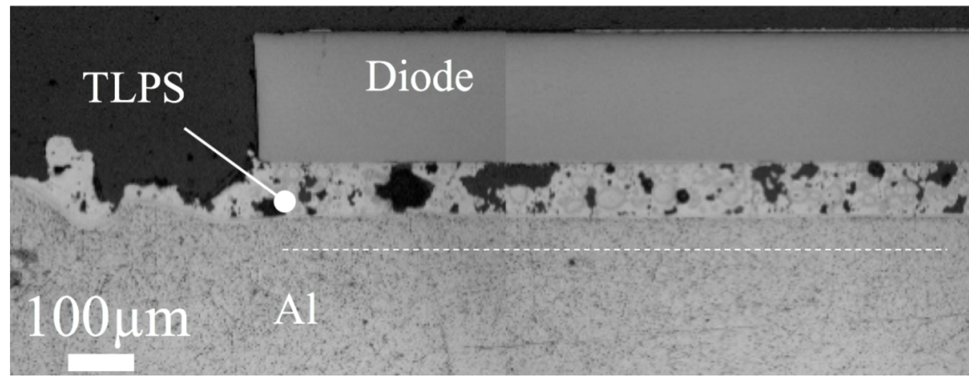


Figure 4-66: Cross-section image of the Cu-Sn TLP on DBC substrates after 900 cycles

For TLPS, the joints start with a porous structure due to common issues with two-step TLPS processing but the amount of defects (bright spots) in the CSAM does not increase with the steep rate as solder and sintered silver. The increase is mainly due to consumption of unreacted tin and solid-state phase transformation between IMCs. This, in general, creates a weaker joint compared to time zero but in overall no major crack or detachment was observed after 900 cycles.

Conclusion

In this chapter, the reliability and performance of TLPS interconnections under different types of loads, such as drop-shock, power and thermal cycling, were tested and evaluated. For this purpose, four sections were considered:

First, an approach to screen the quality of joints was tested. A hybrid of destructive and non-destructive methods, employing X-ray images, cross-section, and ESEM analysis, were used to monitor joint area and cross-section. This creates a reliable approach to measure void fraction and un-wetted regions. Additionally, machine-learning approach was used to measure joint constituents in the final product. The process includes training and verification steps and later, accurately defines the material types from

ESEM images. This provides a reliable method to measure microstructure evolution during TLPS processing.

Second, the performance of Ni-Sn and Cu-Sn TLPS under dynamic loading, i.e. drop-shock, was evaluated. Fresh and aged die-attach samples, made of TLPS and solder, were prepared and tested under 1,500G drop load. Then, the samples were cross-sectioned to monitor joint condition. In all cases, the TLPS samples showed superior performance compared to solder samples. While the die-attach was close to detachment, only minor cracks were observed in TLPS samples.

Third, performance of three types of power packages made of a commercially available power diode, TLPS joint, and power substrates were investigated under power cycling loading condition. A specific power cycling test setup capable of cycling and monitoring power packages without wire-bonds was designed and assembled. Prepared samples were tested under constant current condition (35-50 amps) until failure. Then, they were mounted in epoxy and prepared (cross-sectioned) for optical and scanning electron microscopy. Failure modes and mechanisms were identified.

The results showed that TLPS stiff mechanical properties result in transferring thermos-mechanical stresses to the semiconductor device. Vertical cracks induced in the TLPS under these loads further propagate through the semiconductor device. This is a degrading factor and decreases the reliability of packages, but the main cause of failure is defined to be imperfect connection on the top side of the diode. This created a very small gap between the two conductive surfaces. High temperature and current arc occurred at the gap and resulted in the diode's failure.

Fourth, since all these power components and packages are designed for cyclic thermal loading condition, their performance under thermal cycling. Six types of samples were prepared (three interconnection materials on two types of substrates, DBA and DBC, and tested for 900 cycles between -40°C and 180°C. The samples were analyzed under CSAM each 100 cycles and finally, cross-sectioned to evaluate joint condition and monitor crack propagation. In general, the die-attaches showed inferior performance on DBC substrates compared to DBA. All along, TLPS showed better performance compared to other technologies in both DBA and DBA samples. Crack initiated and propagated considerably in solder and sintered silver joints after 900 cycles while TLPS did not show considerable degradation.

The results from this chapter confirm the superior quality of TLPS joints for power electronic applications. The TLPS joints performed greatly under dynamic loads while the general presumption is that the brittle nature of IMCs makes them prone to easy failure under dynamic loads. Also, under thermal and power cycling loads, TLPS showed similar or better performance compared to the competition.

Chapter 5 Wood carbon Cu-Sn high temperature die-attach technology

Introduction

The ever-increasing demand for higher power density and functionality in power electronic packages increases the operation temperature beyond the limitations of the traditional packaging technologies. This demands innovative and practical methods to overcome the current limitations on packaging properties, such as operation temperature. The efforts are directed in finding novel improvements and replacement for main packaging components, i.e. semiconductor device, die-attach technology, wire-bonds, and substrates. The successful substitution of traditional silicon semiconductor devices with wide-band-gap (WBG) semiconductors increased the threshold operation temperature (175°C) of power electronics to above 500°C [1]. While the reliability research is ongoing on the WBG devices to qualify them for high-end applications, i.e. aerospace, well drilling, space and earth exploration applications, the other packaging technologies are still lagging to satisfy similar temperature limits. The expanding ban on the application of high lead solders in electronic applications emphasized the need for new attachment technologies [6], [39]. The power electronics are temporarily exempted from this ban until a reliable and non-hazardous solution is found. A cutting-edge solution in die-attach materials and technologies enables the application of WBG devices creating powerful high functionality packages.

The search for high temperature die-attach solutions is in progress in the following directions: lead-free solders, and sintering technologies. During the last two decades,

numerous studies were conducted on the application of lead-free solders in electronics [5], [8], [104], [105]. Most of the research is dedicated to Sn-based solders, such SAC solders. The issue with these materials is their low melting temperature compared to WBG threshold limits. Sn melting temperature is 232°C which does not satisfy harsh and high temperature requirements of power electronics. The other soldering options also have their own limitations, i.e. high price of raw material in Au-based [17], [18], weak thermal and electrical properties in Bi-based solders [23]–[25], and corrosive behavior in Zn-based alloys [5]. The need for higher processing temperature than melting temperature (~50°C) to achieve decent wetting behavior is another common issue in soldering technologies [106]. Thus, more advanced and practical technologies are required to improve the current state of the art die-attach solutions.

Sintering technologies have desirable characteristics required for high temperature applications. They provide low processing temperature with high operation limits. Also, there is a vast combination of materials that could be used as sintered joints. Generally, the sintering technologies are divided in two categories: solid and liquid state sintering [40]. The driving force behind both processes is decrease in interfacial energies of the reactants [28]. Nano-silver sintering is the most widespread type of application of solid state sintering in high temperature die-attach fabrication. Since the 2000s, numerous articles have investigated influential factors in fabrication and qualification of silver sintered joints [39], [107]. Effective factors in fabrication are: raw material (particle or flake) size and shape, sintering pressure, processing temperature, sintering duration, sintering environment, paste shrinkage, and surface metallization [38]. Achieving a high-quality joint requires meticulous control over the

abovementioned factors. High thermal and electrical properties are expected due to the application of pure silver. However, quality and reliability depend on porosity [54], high cost of raw material, complicated processing, and steady state creep at elevated temperatures [108].

Transient liquid phase sintered (TLPS) die-attach is the main liquid state sintering technology used in fabrication of high temperature applications. The joints are formed from reaction of at least two phases: one high melting point phase (HMP) and one low melting point (LMP). The processing temperature should be above the melting point of the LMP phase. During the processing, the LMP phase will melt down and form IMCs with HMP phases. The processing temperature and IMCs are dependent on the combination of reactant materials. Common candidates are Cu-Sn, Ni-Sn. Cu-Ni-Sn, Au-In, Ag-In, Au-Sn, Ag-Sn [79], [109]–[112]. Layer-wise and particle based sintering are the two main processing methods of TLPS joints. In layer-wise, an LMP layer will be sandwiched between two HMP layers. During processing, this layer will melt and form an IMC layer, Figure 5-1. The shortcomings of this method are its long processing time and imperfect contact (voids) at interfaces due to mismatched surface roughness of the layers. In particle based processing, a paste made of HMP and LMP particles with specific ratios is prepared. Similar to layer-wise TLPS technology, the processing is done at temperatures higher than the melting point of LMP phase. The melted particles form a liquid medium which surrounds the HMP particles and form IMCs, Figure 5-2. The pastes provide the flexibility to fill the gaps due to mismatched surface roughness at the interfaces and decreases the processing time.

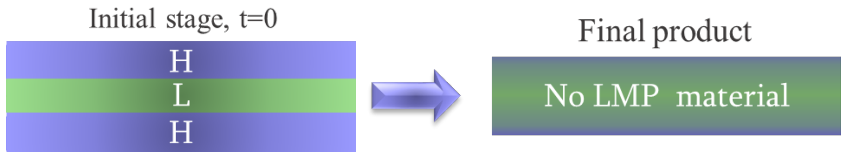


Figure 5-1: Layer-wise TLPS processing

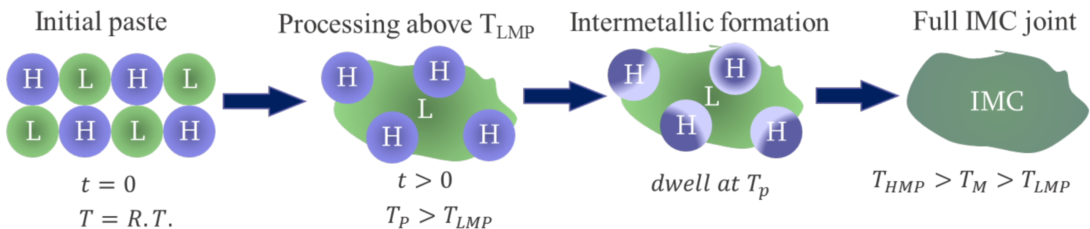


Figure 5-2: Particle based TLPS processing

An essential factor in successful sintering in this method is proper ratios of raw materials in the paste. Having extra LMP particles in the green paste results in unreacted LMP phase in the final joint. This decreases the stability of joints at temperatures above melting points of LMP phase. Increasing the HMP particles, results in unreacted HMP particles in the final product. This can be used to control some joint properties, such as mechanical elasticity, electrical and thermal conductivity. This could optimize the joint performance in cases, such as Cu-Sn system, in which the IMCs have higher elastic modulus, lower electrical and thermal conductivity compared to the HMP material. Another effective factor is joint porosity. Higher porosity joints tend to have better mechanical compliance while having lower thermal and electrical performance. Adding unreactive tertiary elements with desirable mechanical, thermal, and electrical properties to binary TLPS systems is an efficient method to improve the joint quality [113].

In this article, a novel high temperature joining technology based on transient liquid sintering method is introduced. The joining technology is a combination of using TLPS

technology in a high thermal and electrical conductive scaffold of wood carbon. Application of wood carbon provides higher compliance joints which improve mechanical stability of the joints similar to porosity effect. On the other hand, while voids decrease thermal and electrical properties of the joint, superior properties of carbon improve joints' thermal and electrical performance. The rest of this article is divided into the following sections: First, the method used in preparation of the joints has been explained. Second, the prepared joints were cross-sectioned and their quality inspected under scanning electron microscope. Then, a specific test setup was designed and used to test the joints under room temperature and high temperature (200°C) with common TLPS joints. Finally, thermal conductivity of an empty wood carbon scaffold, filled with green paste, and processed was measured and compared to the literature.

Methods:

Wood carbon with initial thickness of 300-500 μm was prepared. The samples went through a step by step grinding process starting with 240 grit SiC paper to 1200 grit to reach 100-200 μm thickness. The samples were immersed in acetone and ultrasonic cleaned for 10 minutes. Then, the samples were immersed in fresh acetone and ultrasonic cleaning was performed for 30 minutes. This process was repeated three more times, with 1, 3, and 6 hours. After cleaning, the samples were kept in acetone until injection of TLPS paste. Figure 5-3 shows environmental scanning electron microscopy (ESEM) of ground wood carbon after cleaning. The magnified images show a wide channel with 40-50 μm diameter. The smaller channels have diameters ranging from 5 to 20 μm. Figure 5-4 shows the cross-section of wood carbon channels.

The channels go through the thickness of the sample and connect the top and bottom surfaces.

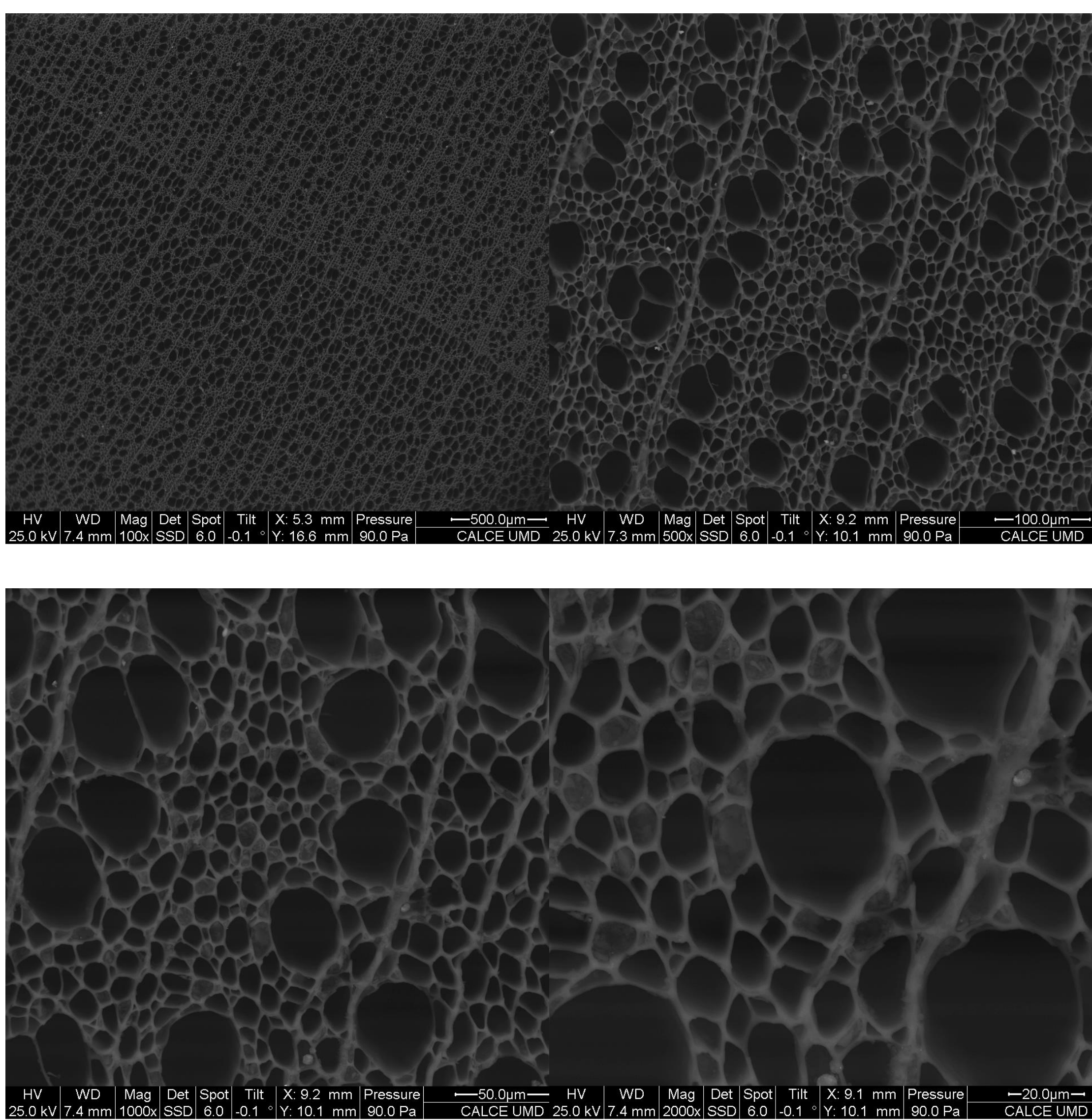
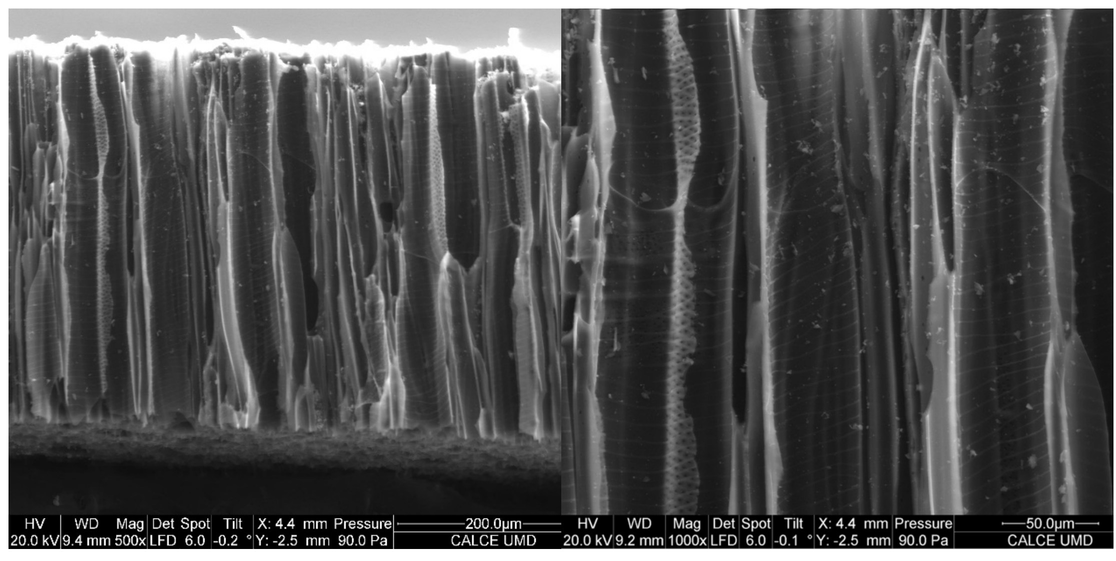


Figure 5-3: Environmental scanning electron microscopy of wood carbon after grinding



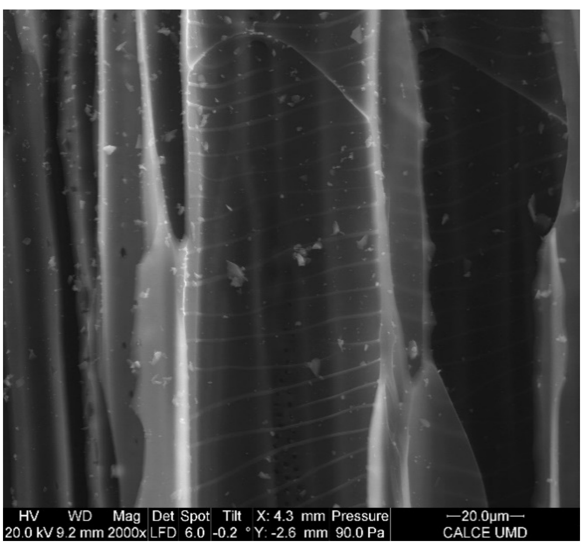
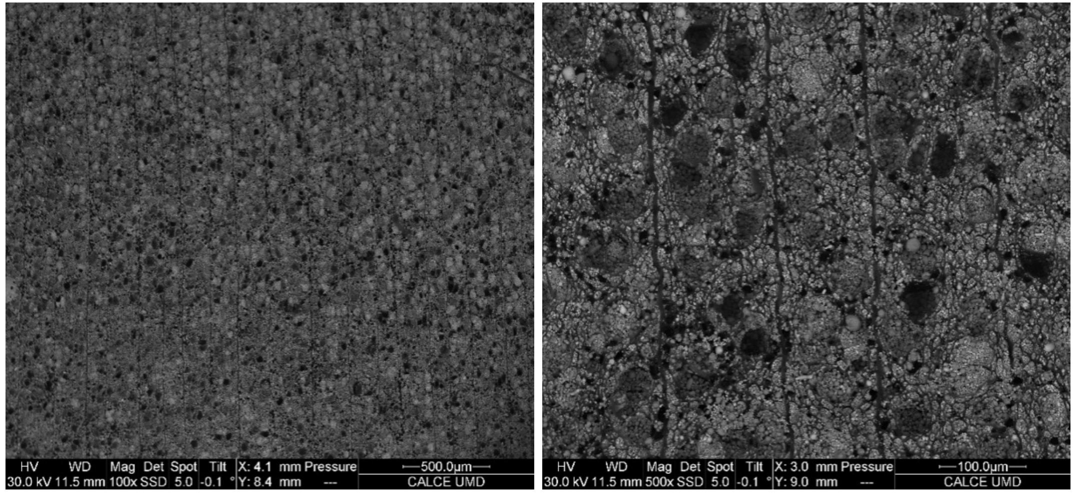


Figure 5-4: Cross-section of wood carbon channels

The TLPS system considered in this study to fill the channel was Cu-Sn. Cu particles with diameters <4 μm (Alfa Aesar copper powder -625 mesh) were immersed in acetone and ultrasonic cleaned for 15 minutes. Similar cleaning process was done on Sn particles with diameters between 3 and 9 μm (ACuPowder Sn115). The particles were mixed manually in TACFlux026 (INDIUM CORPORATION) for 10 minutes with 35wt% Cu, 35wt% Sn, and 30wt% flux. The paste was stencil printed on a microscope slide. The stencil thickness was 150 μm. Then, the wood carbon sample

was removed from acetone and left in the open air for 10-15s. While some of the acetone evaporates during this period, there is still some left to facilitate the penetration process. The wood carbon was placed on the surface of the printed paste. Another microscope slide was placed on top of the sample and pushed slowly with homogeneous pressure through the paste. The paste penetrated through and filled the channels. This process was repeated on the other side of the wood carbon sample to fill the channels all the way from top to bottom surfaces. Figure 5-5 shows the top view of wood carbon sample filled with Cu-Sn sintering paste. The particles perfectly filled the wide channel while the empty spaces in small channels provided the escape path for the flux to evaporate during processing. Figure 5-6 shows the cross-section of the filled sample with 400 μm thickness (for demonstration purposes). As shown in the image, the paste successfully filled the channels and there is a decent connection between the top and bottom of the sample.



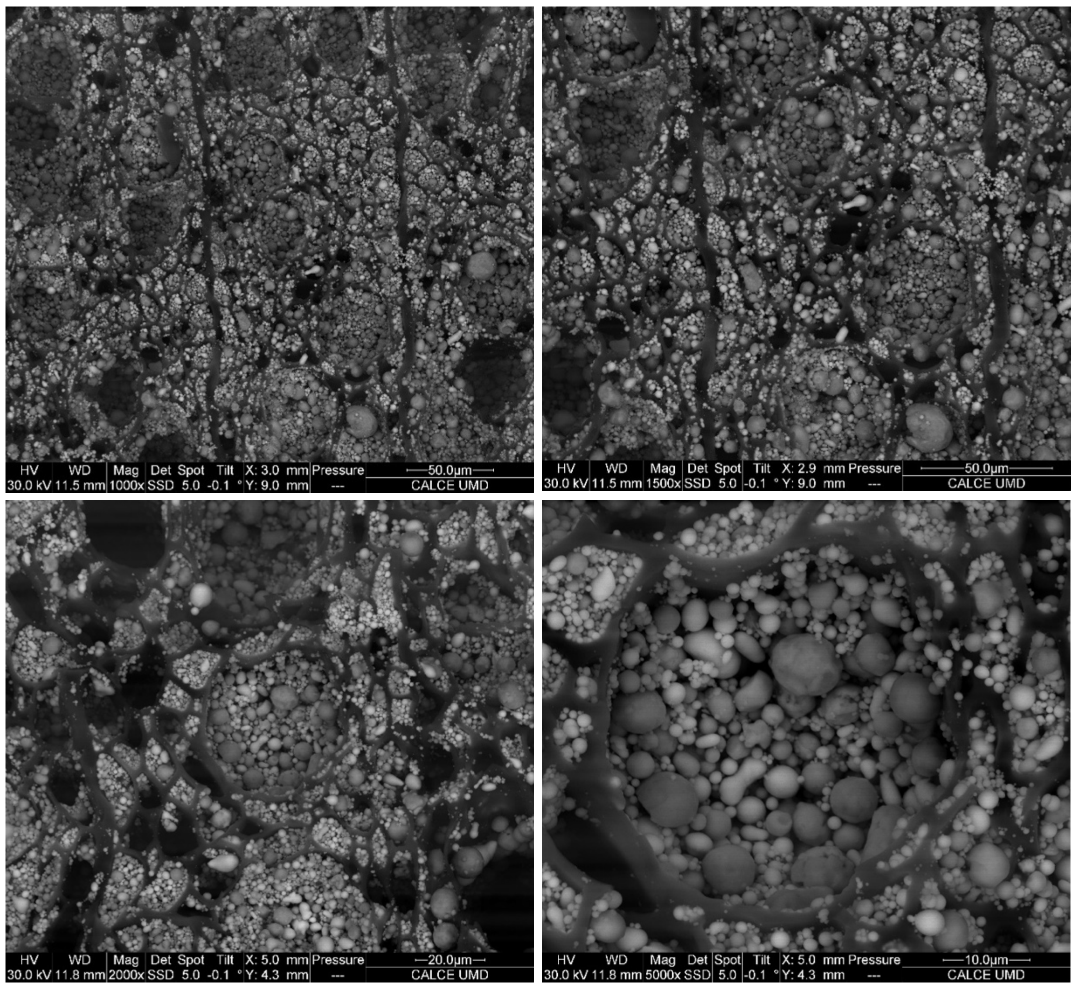


Figure 5-5: Top view of filled wood carbon with Cu-Sn paste

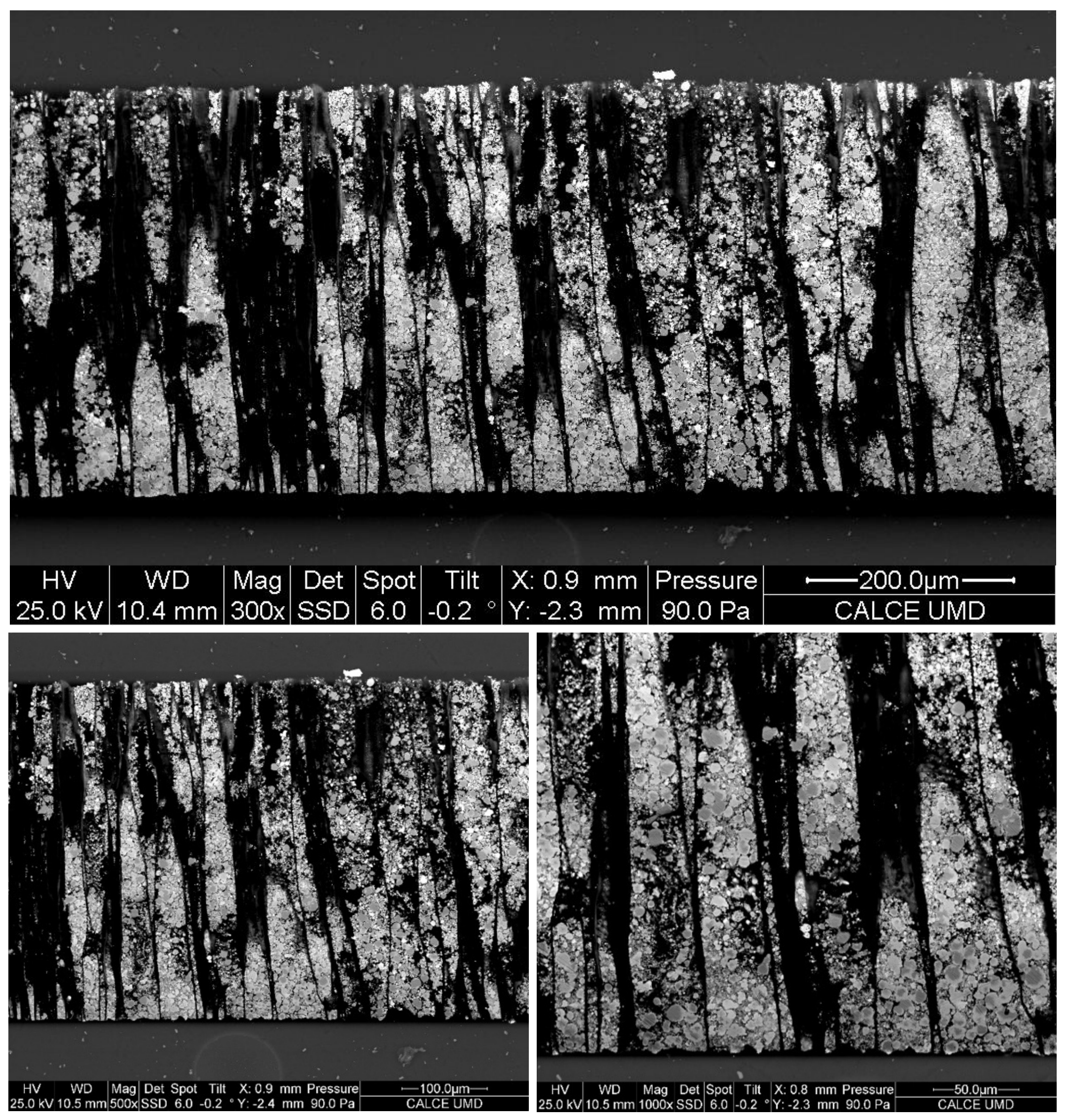


Figure 5-6: Cross-section view of filled wood carbon with 400 µm thickness

An EDS analysis of the filled wood with TLPS paste shows the distribution of Cu and Sn particles inside the carbon channels. The cross-sectional view of the channel under ESEM is presented in Figure 5-7 (a). Figure 5-7 (b-d) shows the material mapping for carbon, Cu, and Sn. The EDS images show how Cu particles are located between the Sn particles and filled the gaps in carbon channels.

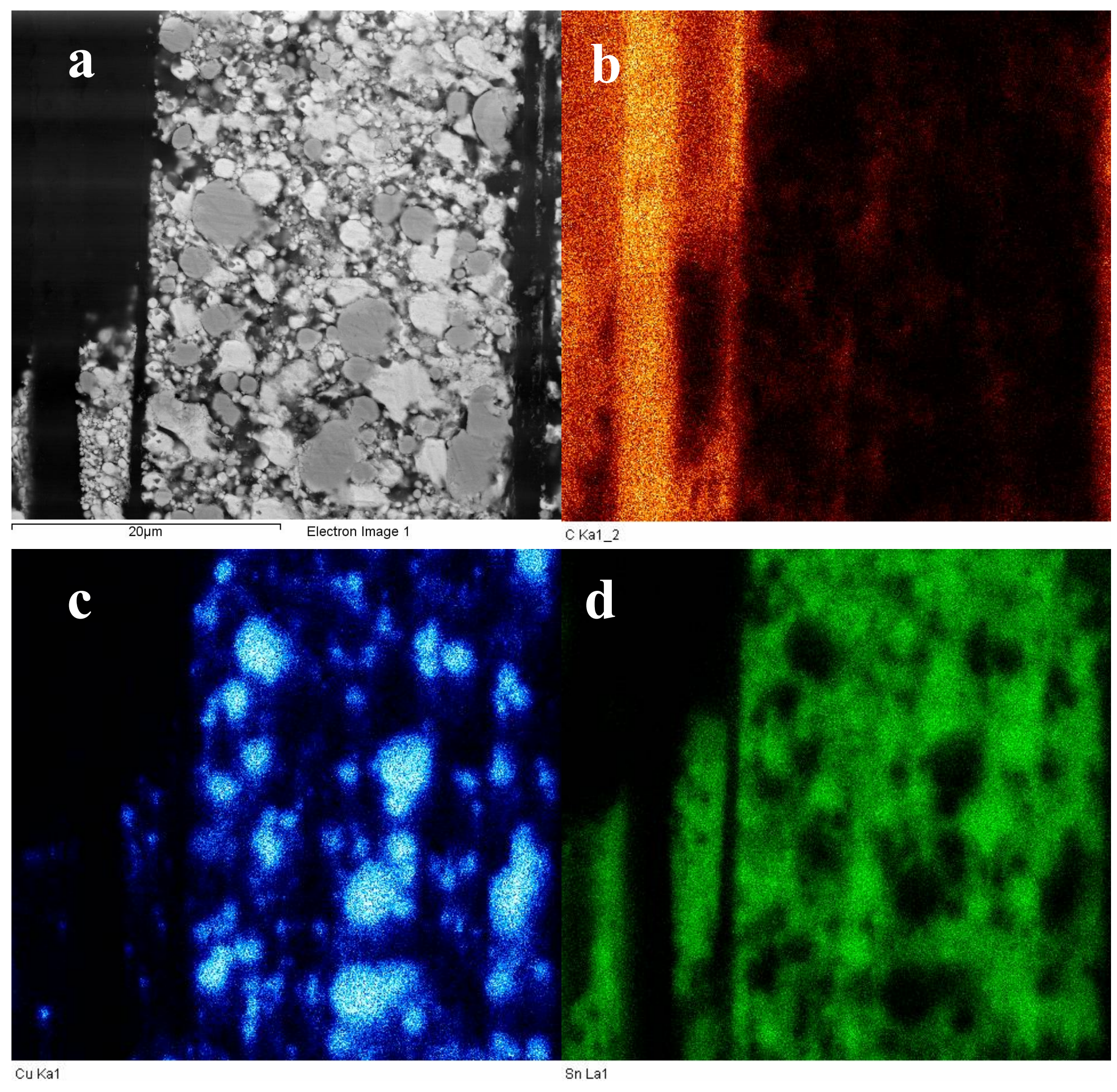


Figure 5-7: EDS analysis of filled carbon-wood channel with TLPS paste

A sample wood carbon Cu-Sn TLPS was prepared between a dummy Cu die with 6.35×6.35×3 mm^3 dimensions on a Cu substrate. Both Cu components were ground by 240 grit SiC paper. A TLPS paste, 90wt% Cu -325 and 10wt% TACFlux 026 (INDIUM Corporation), was stencil printed on both the substrate and die. The thickness of printed pastes was 75 µm. The wood carbon (with 4×4 mm^2) was placed at the center of substrate paste, Figure 5-8 (a). The die was placed on top of the wood carbon. Slight pressure was applied on the die to help the TLPS infiltrate the channels, Figure 5-8 (b). A ring of Sn100 solder (check the manufacturer) was printed around the sample and die, Figure 5-8 (c). During processing, when the temperature increases the TACFlux evaporates and burns just before the solder and Sn particles melt. The molten Sn diffuses between the Cu particles and forms IMCs. This creates a solid bonding between the two Cu components. The sample was processed on a heat plate under normal atmosphere (no reducing or inert agent). The heating ramp rate was 50°C/min. The maximum temperature used during the process was 300°C with 30min dwell time.

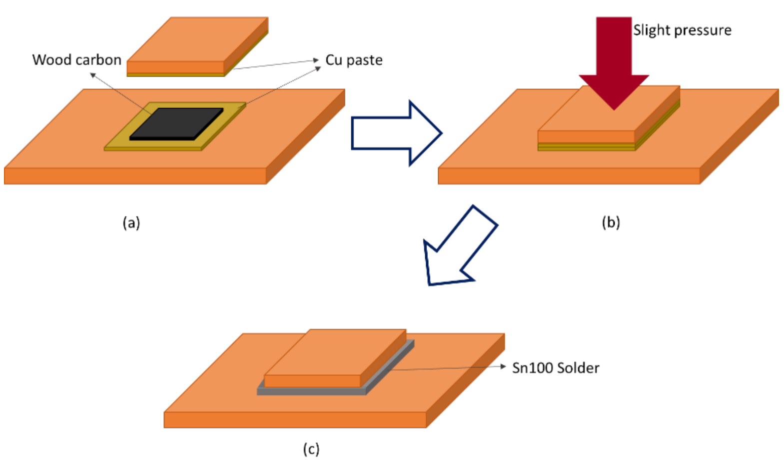


Figure 5-8: Wood carbon Cu-Sn TLPS sample preparation

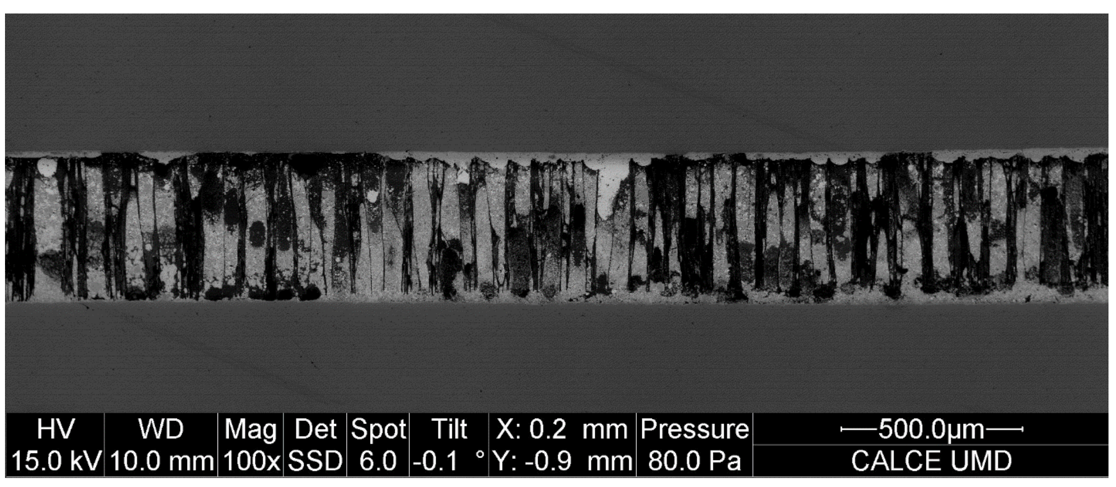


Figure 5-9: Cross-section of wood carbon Cu-Sn TLPS joint

The samples were potted in epoxy and later, cross-sectioned and polished. Figure 5-10 shows the cross-section of the joint under ESEM.

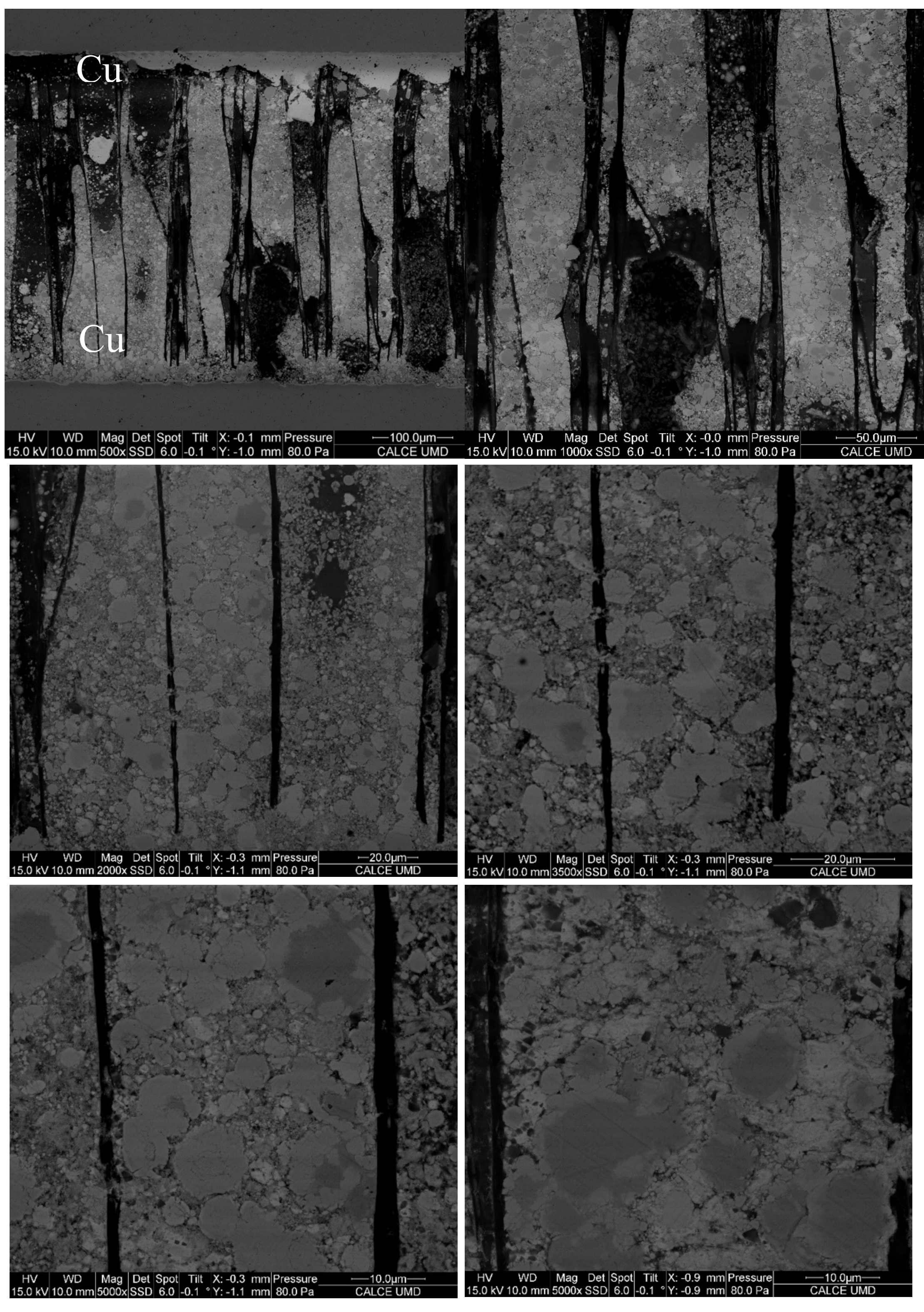


Figure 5-10: Cross-section of wood carbon channels filled with Cu-Sn TLPS joint

Shear test results:

The prepared samples were tested under shear stress condition. A specific shear sample specimen and setup similar to [114] was used. Two samples from Cu-Sn TLPS and wood-carbon Cu-Sn TLPS were tested at room temperature under 0.4 mm/s strain rate. Figure 5-13 shows maximum shear strength of Cu-Sn and wood carbon Cu-Sn TLPS. In both cases, room temperature and high temperature, wood carbon joint showed comparable results to TLPS joints.

Figure 5-11: Shear test specimen

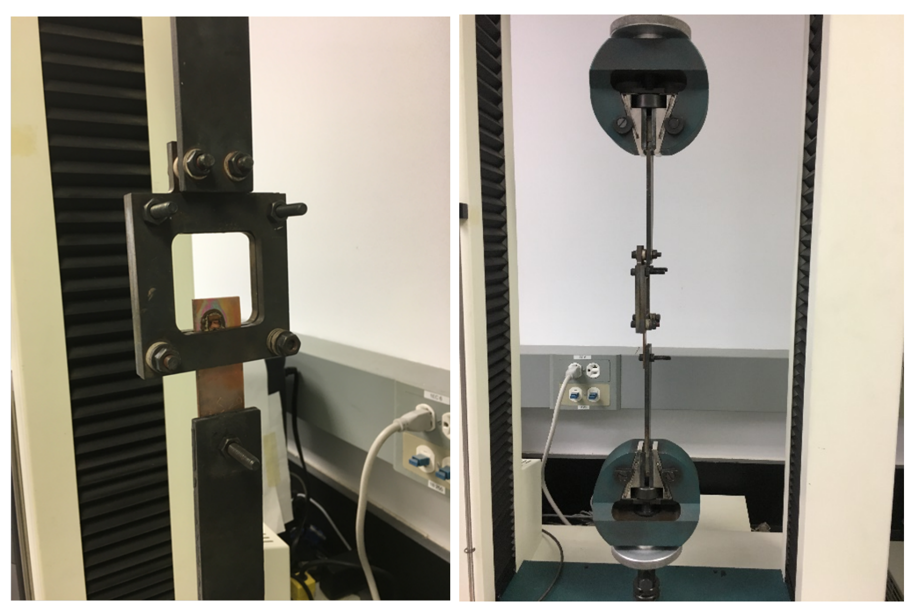


Figure 5-12: Test setup

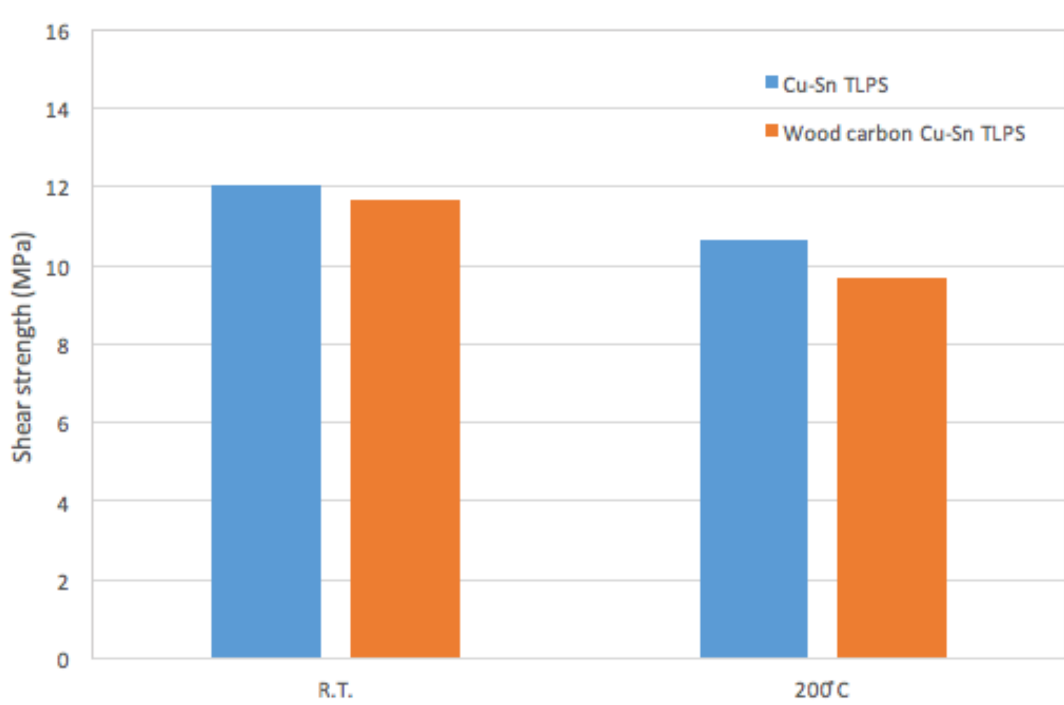


Figure 5-13: Shear test at room temperature and at 200°C

Conclusion:

In this chapter, an innovative approach to improve thermal properties of TLPS joints was introduced. Wood carbon was used as a medium to contain metallic particles during TLPS processing. Then, similar to normal TLPS processing the samples were processed and a high quality sintered joint was created. The mechanical strength of the joints was evaluated by room temperature and high temperature shear test. The results show comparable shear strength to normal TLPS joints.

Chapter 6 Contributions and future works

This chapter serves to list the academic and technical contributions of this dissertation and suggests a possible future direction to further improve the current state of the art in processing, modeling, and application of TLPS joints.

The main contribution of this dissertation is providing a simple, reliable approach to process TLPS interconnections without the need for complex preparation or specific environment. This facilitates the application of TLPS materials in industrial applications and provides consistency in the results. This technology can be used for large area die-attachment purposes. Additionally, it makes it possible for the integration of tertiary elements in the joint structure without any change in the processing. The paste application and processing, proposed by this dissertation, could be performed by current solder processing equipment or simple electrical furnaces. This makes the transfer from high-lead solder to TLPS more convenient for industries.

Solid-liquid interactions are sophisticated phenomena for modeling and simulation. This dissertation introduced a modified PFM method for modeling and simulation of TLPS processes. The experimental results were used to estimate PFM simulation parameters. Then, IMC microstructure evolution during two-step and one-step Cu-Sn TLPS processing were modeled to confirm the capability of one-step processing to improve the current state of the art in interconnection processing. To the best of the author's knowledge, this is the first time that the application of PFM simulation and experimental results were combined for TLPS processing. Also, this is the first time PFM method has been used in particle-based TLPS processing and furthermore, no

other work has used PFM to compare different TLPS processing methods to select the most appropriate approach to obtain the desirable product.

Reliability and performance of TLPS interconnections under different loading conditions are an important factor for their commercialization and industrial applications. In this dissertation, TLPS joints were studied under dynamic and thermal loads. The general presumption in the literature is that TLPS interconnection will fail easily under dynamic loads due to the brittleness of the IMCs; however, the results from this work showed great performance under drop-shock loads in TLPS joints after processing and even aging. The results were significantly better than solder die-attach. Next, the performance of TLPS interconnection under power and thermal cycling loads were evaluated. In both cases, the TLPS joints showed similar or better performance to their competition. To the best of the author's knowledge, this is the only study that has comprehensively considered drop-shock, power and thermal cycling effects on TLPS interconnections.

Finally, a novel and innovative method to impregnate wood carbon with TLPS paste was introduced. This is the first study that introduces the impregnation of wood carbon and its application in TLPS processing.

Future works

TLPS joints have great potential for integration of other elements to improve interconnection properties. One major improvement could be addition of different tertiary elements based on thermomechanical properties of joining surfaces to make the interconnection more compatible. One candidate for this purpose is aluminum which with its low elastic modulus and yield strength could mitigate the mechanical stresses

by plastic deformation. A novel approach to use this feature is functionally graded TLPS interconnections with mechanical properties changing gradually from one surface to the other. The functionally graded TLPS interconnections are more suitable to be processed as preforms to decrease the processing steps and remove the unnecessary ones.

Appendix I

Au-In SLID Joints

Optoelectronics devices require a bonding material with high thermal conductivity and stress relief properties to prevent reliability challenges such as high temperature sensitivity and stress-induced degradation [115]. The existence of flux in the joint may contaminate the optically active surface by organic residue leftover, and a conventional cleaning method may not be effective for these devices [109]. Previously, low temperature bonding polymers have been used for attaching optoelectronics devices but due to outgassing and misalignment during the curing process and degradation during service life, the search for a better die-bonding process is ongoing [116]. Au-In SLID joints are of interest to researchers because of their potential to provide high reliability and performance joints in optoelectronic fields [109], [115], [116].

Au and In are an acceptable materials combination for solid liquid interdiffusion. In has a low melting point of 157˚C; Au has a high melting temperature of 1064˚C [117]. The rate of interdiffusion between In and Au is the fastest among metals and can occur at temperatures as low as 50˚C [118], [119]. In diffuses into gold through grain boundaries and its diffusion coefficient is evaluated to be 6.05×10^{-4} m^2/s with activation energy of 0.97 eV [120]. Due to this high interdiffusion coefficient, Au and In layers interact upon contact, resulting in the formation of $AuIn_2$ intermetallics. $AuIn_2$ is a stable compound with a melting point of 495˚C [117] that remains unaltered even after nine months at room temperature [118], [121]. Formation of this stable IMC layer on the surface of In prevents oxidation during processing, while $AuIn_2$ breaks and dissolves into the liquid In that was melted during joining [115].

The tendency of In to oxide under open air atmosphere requires special provisions to be made during fabrication to prevent defective bonds. Deposition of sintering layers in vacuum chambers is the most common SLID fabrication technique. In this method, a layer of chromium is deposited on the substrate and chip to improve the adhesion [122]. Other layers such as diffusion barrier (Ni/Pt), adhesion (Ti), and Ohmic contact (W), may be used depending on fabrication conditions. Then, the joining layers are deposited directly on the chromium layer. The deposition should process such that the In layer is sandwiched between two Au layers. In flip chip manufacturing processes which pick and place the chip on the substrate metallization, the Au and In layers may touch each other. In these cases, a very thin layer of gold or silver is deposited on the In to prevent oxidation of the surface prior to flip-chip processing. As mentioned above, interaction between these two layers results in the formation of $AuIn_2$/$AgIn_2$[115], [122]–[125]. Another method prevents the formation of $AuIn_2$ by the desposition of a thin Ti layer (10nm), which prevents low temperature diffusion between Au and In layers while keeping the high temperature diffusion intact [126]. Table 7 shows some of the multilayer Au-In depositions in the literature. The thickness of Au and In layers should be selected based on the desired intermetallic composition. For example, the large ratio of In to Au in the joint processed in [122] resulted in a high amount of pure In left in the joint and a low melting point ~157˚C, close to the melting point of In.

Table 7: Example of multilayer build-up on the substrate and chip

Chip Material	Chip layers	Thickness (μm)	Substrate Material	Substrate Layers	Thickness (μm)	Ref.
Si	Cr	0.03		Cr	0.1	[122]

	In Au	5 0.1	Copper	Au	0.1	
Si	Ti Au In	0.1 0.1 3-5	Si	Ti Au Au	0.1 0.1 2	[123]
Si	Ti Au In	0.1 0.1 3-5	alloy42	Ni Au Au	0.1 0.1 2	[123]
Si	Ti Pt Au In Au	0.05 0.1 0.2 6 0.1	GaInP/ AlGaInP			[115]
Glass	Ti Ni Au In Au	0.05 0.2 0.05 2.5 0.05	Glass	Ti Ni Au	0.05 0.1 2	[116]
Glass	Ti Ni Au In Au	0.05 0.2 0.05 2.5 0.05	Glass	Cr Au	0.04 2	[116]
Si_3N_4 DBC 12mils Cu	W Ti Pt Ti Au Au	0.3 0.3 0.1 0.1 0.5 4	SiC	W Pt Ti Au In Au	0.2 0.1 0.1 0.05 3.3 0.05	[125]

Other important factors during processing of Au-In joints are sintering atmosphere, temperature, pressure, and time. Sintering atmosphere will impact the resulting joint quality. The sintering process is usually conducted under N_2/H_2 ambient or flow to prevent oxidation [122]. Obviously, temperatures above the melting point of In are required to start the liquid phase sintering process. The combination of temperature, pressure and sintering time can affect the mechanical properties of the joints significantly. It is reported that increasing the sintering temperature, pressure, and sintering duration increases the shear strength of Au-In joints [109], [115]. Shear strength of the Au-In joints will also increase when annealing at high temperatures.

Joints annealed at 400˚C showed better resistance under shear stress compared to normal sintered joints [115], [125]. The main reason for this increase in joint shear strength is the formation of more IMCs during annealing. The produced IMCs have better shear strength than that of raw materials, in addition to acceptable melting temperatures. Increase in the intermetallic content of the joint improves mechanical properties while simultaneously increasing electrical resistance [115].

Reliability data is not readily available on Au-In sintered joints. Thermal cycling is the most common method used for life analysis of the joints. Wang et al. [123] reported survival of Au-In joints between silicon wafers after 1,503 cycles of thermal cycling between -65 ˚C and 150˚C. Liu et al. [115] measured sintered joint shear strength of thermal shock samples cycled between -196˚C and 80˚C after 500 cycles. Only ~0.5 MPa shear strength decrease is evaluated for the joints. The maximum shear strength reported for Au-In joints is ~42.5 MPa for a joint with 470˚C melting point , the melting temperature of Au_7In_3 [116]. Grummel et al. [124] reported ~78% and 83.23% increases in the resistivity of joints after 200 and 800 thermal cycles, respectively, between 25 ˚C and 200˚C.

Ag-In SLID Joints

The SLID process for Ag-In is comparable to that of Au-In. Silver diffuses into In via rapid interstitial mechanisms while In diffuses into silver through grain boundaries, with a diffusion coefficient of 2.4×10^{-12} m^2/s and activation energy of 0.43 eV [127], [128]. Due to these diffusion properties, silver and In interact with each other to form $AgIn_2$ intermetallics. These intermetallics are extremely stable and remain unaltered even after fifteen years at room temperature [119]. The existence of stable $AgIn_2$ IMCs

protects the underlying In layer from oxidation. Similar to Au-In, all deposition processes occur in a vacuum; sintering processes occur in N_2/H_2 chambers. Temperatures above 156˚C are required to activate sintering. Generally, temperatures near 210˚C are used, while the produced joints can have melting points exceeding 700˚C [129].

Homogenization and annealing after processing of Ag-In provides stronger joints. This process can increase Ag-rich alloy content of the joint and therefore, improves mechanical properties [125], [129]. Because silver and Ag-rich alloys have lower Young's modules than the copper plating on power electronic devices, stress relief through plastic deformation is more prevalent in silver joints [42]. Mustain et al. [125] investigated Ag-In and Au-In TLPS die attaches for SiC devices. The authors tested the tensile strength of sintered and annealed joints at 400˚C for 100 hours according to MIL-STD-883G Method 2027.2 and showed annealed samples had higher tensile strength under pull-in tests. Similar results are reported for shear strength measurement of samples thermal cycled from -55˚C to 400˚C for 10 cycles. In another study, Wu and Lee showed that decreasing silver and In thicknesses while keeping their proportion constant can result in higher shear strength joints. They identified three phases in their joints: pure Ag, Ag-rich alloy, and Ag_2In. Samples broke through the Ag2In layers and showed a wide distribution in shear strength from 6.6 to 36.8MPa [130].

An interesting study of Ag-In joints was conducted by Kim et al. [131]. Four types of Ag-In bonds were processed with two different preparation methods and under bump metallization (UBM). The first method was electroplating a 60 μm silver layer on a copper substrate; second method, a silver foil with 280 μm thickness was bonded

directly on the copper substrate. They indicated that electroplated silver layers more than 60 μm tend to detach from the substrate. On the chip side two types of UBM were utilized: 1) Cr 0.03μm/Au 0.1μm; and 2) Cr (0.03μm)/ Ni (0.5μm)/ Au (0.1μm). They tried to detach the chip from the substrate with a hand tool. For the first type of metallization, the fracture occurred in the Ag_2In IMC layer and no pure In was found. Ag_2In was formed due to an abundance of silver atoms during bonding. It appears that Ag_2In molecules are not inclined to share electrons with Cr; hence, the reason for lack of strength at the interface. The second type of UBM design produced very strong joints consisting of In_7Ni_3 IMCs. It is reported that in all attempts to detach the chip from the substrate the chip fractured first.

<u>Au-Sn and Ag-Sn SLID Joints</u>

Sn is another low temperature material that can be used with silver and Au in SLID joining technology. Temperatures higher than the melting point of Sn (232˚C) are required to activate the liquid phase diffusion process. During deposition of Sn layers, it is necessary to prevent oxidation. The sintering process can be completed under air atmosphere at temperatures around 280˚C or higher. Joints produced under these conditions have shear strengths up to 11 MPa [110]. It is known that Sn-based alloys show lower fatigue resistance compared to In-based alloys [132]. However, the reliability experiments of Quintero and McCluskey on Au-Sn SLID joints under two thermal conditions (-55˚C to 150˚C and -55˚C to 180˚C) with two die sizes ($25mm^2$ and $100\ mm^2$) shows superior and comparable performance to nano-silver sintered and high lead joints, respectively [29].

Ag-Sn joints are similar to Au-Sn. A layer of noble metal material should be used to protect the uncovered Sn layer before the sintering process. Kim et al. [42] processed Ag-Sn SLID joint on a Cr (0.03μm)/ Ni (0.5μm)/ Au (0.1μm) substrate and obtained strong joints with melting temperatures beyond 700˚C. The joints were processed at 245˚C for 8 min under 0.29 MPa pressure. Existence of four phases of Ag3Sn, Ni3Sn4, Ag-rich alloy, and very little amount of pure Sn was reported. The authors aged the samples at 430˚C for 30 hours to dissolve the remaining pure Sn. Nobeen et al. [111] investigated the effects of temperature, pressure and raw material fractions on shear strength of Ag-Sn SLID joints. They reported that increase in the processing pressure from 0.2 MPa to 0.3 MPa and eventually to 0.4 MPa at 280˚C for 30 min resulted in shear strength increase from 3MPa to 9±1.2 MPa and finally to 10.6±5.7MPa, respectively. Also, shear strength from 7.5MPa to 14MPa was reported when processing temperatures were changed from 250 to 290˚C. Then, they processed three types of joints: 1) fully Ag3Sn IMCs 2) Ag-rich and 3) Sn-rich. The First type was processed under 30 MPa pressure and obtained average shear strength of 13MPa. The second and third types were prepared by changing the thicknesses of Sn and Ag layers and achieved average 22MPa and 17.5 MPa shear strength, respectively.

Cu-Sn SLID Joints

Cu-Sn can be used in a solid liquid IMC combination. Above the melting temperature of Sn, solid Cu diffuses into liquid Sn via grain boundaries and forms Cu6Sn5; in the second step of diffusion, solid-state diffusion occurs and thick Cu_6Sn_5 IMCs convert to Cu_3Sn. The solid-state diffusion process is than the solid-liquid inter-diffusion process. Cu-Sn has similar reaction rates to Au-Sn: slower than Ni-Sn and faster than Ag-Sn

[133]. The desirable properties of Cu-Sn SLID joints make them a candidate for flip chip micro-bump BGA manufacturing. It is possible to fabricate joints with 7.5 µm diameter and 15 µm pitch [133]. These joints were tested under thermal cycling, high temperature aging, and humidity conditions. Resistance measurement was used to evaluate the performance of a series of joints. After 1,000 hours of storage at 175˚C and 200˚C no change in resistance was reported. Microstructure analysis of the joints after 1,000 cycles of temperature swing from -65˚C to 150˚C with 10 min dwell time at the extreme temperatures (1hr/cycle) did not show any change in the morphology of the contacts; however, the resistance increased. The humidity tests revealed an interesting property of Cu-Sn IMCs. Similar corrosion resistance to Cu was reported for Cu_6Sn_5, but Cu_3Sn is inert and can be used as a corrosion barrier under humidity condition.

The effects on the joints of bonding pressure, temperature, and duration have been investigated. It is reported that an increase in pressure and temperature improves the bonding and 30 min is acceptable time to process a decent join. Under 20 MPa pressure at 260˚C for 30 min, joints with 39.8 MPa shear strength were produced. Thermal cycling from -40˚C to 150˚C for 1000 cycles decreased the joints' shear strength to 33.3 MPa. Also, the authors indicated that more pressure during sintering results in less paste squeeze-out during bonding. The reason for this phenomenon is further reaction of Cu and Sn under pressure and less amount of liquid Sn is able to squeeze out of the bonding area [112].

Table 8. Different SLID joints properties [41]

Joint	Bonding Temp(˚C)	Remelt Temp	CTE/Si	CTE/SiC	Thermal cond.*	Electrical cond.*
Ni-Sn	300	400	4.4	4.8	1	1

Ag-Sn	250	600	6.3	6.8	4.7	4.4
Au-SN	450	900	4.7	5.1	3.5	3.1
Cu-Sn	280	415	5.5	6	4.4	4.1
Au-In	200	495	4.7	5.1	3.5	3.1
Ag-In	175	880	6.3	6.8	4.7	4.4

**Relative to Ni*

Ni-Sn SLID Joints

The properties of Ni and Sn promise strong and reliable joints. Due to the low price of the raw materials, Ni-Sn can be considered as one the most economical solutions to the high temperature interconnect problem in power electronic devices, Table 8. Ni_3Sn_4 is the expected IMC product in Ni-Sn sintering and has a melting temperature around 798˚C [79]. Yoon et al. [41] investigated SLID bonding of Sn foils between pre-existing Ni plating on Si substrates. Homogeneous Ni_3Sn_4 layer formed at the bond-line. The joints did not show any sign of degradation under SAM analysis after 1000 thermal cycles from -40˚C to 200˚C.

Other Materials

Cu-In is another combination of materials that can be used for SLID bonding. Joints produced using Cu-In at different temperatures and soaking time were lap-shear tested to evaluate their strength. Brittle fracture was observed in all broken samples. Shear strengths 5.08, 5.44, and 9.07 MPa were recorded for samples processed at 260˚C for 40, 160, and 360 min, respectively. It is reported that increase in processing duration provides enough time to convert $Cu_{11}In_9$ into Cu_2In; this proves that Cu_2In phase has better properties than $Cu_{11}In_9$. Samples processed at 360˚C showed higher average shear strength, 13.65, 12.44, and 12.31 MPa for 40, 160, and 360 min, respectively [134].

Ni-Sn-Zn can also be used for partial SLID bonding. In one process, a layer of Zn 100 μm thick was sandwiched between Sn layers 10 μm thick and the whole assembly placed between two Ni substrates. The sintering process was tested under 12 kPa pressure in N_2 atmosphere at 250˚C, 300˚C, and 350˚C. During processing, Zn diffuses into the Ni and forms Ni-Zn IMCs while a Sn-rich layer forms. Samples processed at 250˚C did not show acceptable shear strength. Samples processed at 300˚C and 350˚C for 30 min showed average shear strengths of 10 MPa and 27.4 MPa, respectively. Fracture and microstructure analyses of the joints showed that Sn-rich and pure Zn phases existed in the joint. Zn can keep the stability of joints at high temperatures while the Sn-rich layer is a stress-relaxing layer expected to compensate for the brittleness of Zn [97].

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