ABSTRACT

Title of Dissertation:	HIGH-FREQUENCY BIDIRECTIONAL DC-DC CONVERTERS FOR ELECTRIC VEHICLE APPLICATIONS
	Peiwen He, Doctor of Philosophy, 2018
Dissertation directed by:	Professor Alireza Khaligh Department of Electrical and Computer Engineering

As a part of an electric vehicle (EV) onboard charger, a highly efficient, highly compact, lightweight and isolated DC-DC converter is required to enable battery charging through voltage/current regulation. In addition, a bidirectional on-board charger requires the DC-DC converter to achieve bidirectional power flow: grid-to-vehicle (G2V) and vehicle-to-grid (V2G). In this work, performance characteristics of two popular DC-DC topologies, CLLC and dual active bridge (DAB), are analyzed and compared for EV charging applications. The CLLC topology is selected due to its wide gain range, soft-switching capability over the full load range, and potential for a smaller and more compact size. This dissertation outlines the feasibility, analyses, and performance of a CLLC converter investigated and designed to operate at 1 MHz and 3.3 kW for EV onboard chargers. The proposed design utilizes the emerging wide

bandgap (WBG) gallium nitride (GaN) based MOSFETs to enable high-frequency switching without sacrificing the conversion efficiency. One of the major challenges in MHz-level power converter design is to reduce the parasitic components of printed circuit boards (PCBs), which can cause faulty triggering of switches leading to circuit failure. An innovative gate driver is designed and optimized to minimize the effect of parasitic components, which includes a +6/-3 V driving logic enhancing the noise immunity of the system. Another challenge is the efficient design of magnetic components, which requires minimizing the impacts of skin and proximity effects on the transformer winding to reduce the conduction loss at high frequencies. A novel MHz-level planar transformer with adjustable leakage inductance is modeled, designed, and developed for the proposed converter. A comprehensive system level power loss analysis is completed and confirmed with the help of experimental results. This is the first prototype of a 3.3 kW power bidirectional CLLC converter operating at 1 MHz operating frequency with 400-450 V input voltage range, 250-420 V output voltage range. The experiment results have successfully validated the feasibility of the proposed converter conforming to the analysis carried out during the design phase. With an appropriate design of driving circuit and control signal, the prototype achieves a peak efficiency of 97.2% with 9.22 W/cm^3 (151.1 W/in^3) power density which is twice more power dense than other state-of-the-art isolated DC-DC converters.

HIGH-FREQUENCY BIDIRECTIONAL DC-DC CONVERTERS FOR ELECTRIC VEHICLE APPLICATIONS

by

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List of Abbreviations

CC-CV	constant current-constant voltage
DAB	dual active bridge
DPS	dual phase shift
EMI	electromagnetic interference
EPS	extended phase shift
EV	electric vehicle
EVSE	electric vehicle supply equipment
FBCLLC	full-bridge CLLC
FBDAB	full-bridge dual active bridge
FEA	finite element analysis
FHA	first harmonic approximation
G2V	grid-to-vehicle
GaN	gallium nitride
HBCLLC	half-bridge CLLC
HBDAB	half-bridge dual active bridge
HEV	hybrid electric vehicle
ICE	internal combustion engine
MMF	magneto-motive force
MPG	miles per gallon
MSCC	multistage current charging
NEDC	new European driving cycle
OBC	onboard charger

OEM	original equipment manufacturer
PCB	printed circuit board
PFC	power factor correction
PHEV	plug-in hybrid electric vehicle
PI	proportional-integrator
PWM	pulse-width modulation
SEPIC	single-ended primary-inductor converter
SMPS	switched-mode power supply
SNR	signal-to-noise ratio
SOC	state of charge
SOI	silicon-on-insulator
SPS	single phase shift
Si	silicon
SiC	silicon carbide
TPS	triple phase shift
V2G	vehicle-to-grid
WBG	wide bandgap
ZCS	zero-current switching
ZVS	zero-voltage switching

Chapter 1 : Introduction to Electric Vehicle Charging Systems

1.1 Background

In the last two decades, the concerns about fossil fuel depletion and global climate change [1], [2] are promoting the growth of electric vehicle market [3]. In 1997, the Toyota Prius was released in Japan and became the world's first mass-produced hybrid electric vehicle. In 2008, Tesla released its electric vehicle, Roadster, which was the first all-electric production car using Li-ion battery cell and with a range greater than 200 miles per charge. Nissan also released a Li-ion-battery-based affordable family car, the Nissan LEAF, in 2010, which became the world's all-time best selling highway-capable all-electric car [4].

As shown in Fig. 1-1, the global electric car stock has been growing fast since 2010. It surpassed 2 million vehicles in 2016 after crossing the 1-million threshold in 2015 [5]. Fig. 1-2 shows the global market share of the electric car. It can be inferred from the figure that there is an increasing trend in the purchase of electric cars. Furthermore, from the original equipment manufacturer (OEM) announcements and the EV development environment, there are predictions indicating that the electric car stock will range between 9 million and 20 million by 2020, with expectations of reaching between 40 million and 70 million by 2025[5].

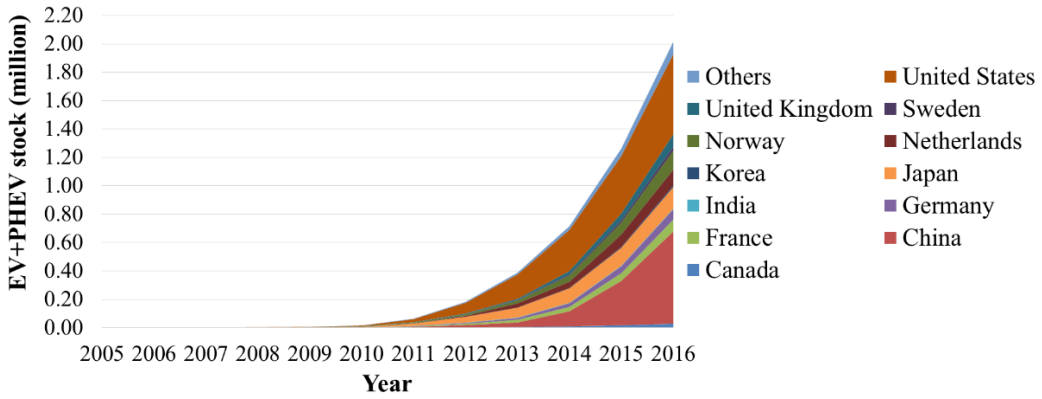


Fig. 1-1 EV+PHEV stock by country, 2005-2016.

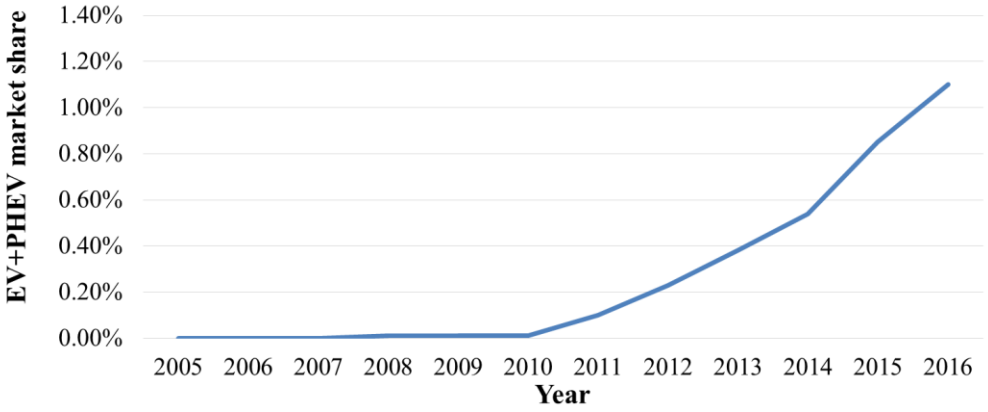


Fig. 1-2 Global EV+PHEV market share, 2005-2016.

In comparison to conventional fossil vehicles, EVs are typically propelled by one or more electric motors instead of an internal combustion engine (ICE). Large battery packs are used in EVs to store electric energy and charged by the grid through plug-in charging systems. Hybrid electric vehicles (HEVs) can be powered by both fossil and electric energies. Typically, an ICE and an electric motor with a battery pack are included in HEVs. The battery pack is charged through the ICE, not the grid, therefore, HEVs do not have plug-in charging systems [6]. Plug-in hybrid electric vehicles (PHEVs) also have both ICE and electric motors. However, in comparison to HEVs,

the battery pack of PHEVs can be charged through both the ICE and the grid. Therefore, plug-in charging systems are required in PHEVs [6].

EVs have several advantages over conventional ICE vehicles:

1) Energy efficient: EVs can convert about 59%-62% of the electrical energy from the grid to power at the wheels. However, conventional gasoline vehicles can only convert about 17%-21% of the energy stored in gasoline [7].

2) Environmentally friendly: Although the power plant producing electricity may emit pollutants, EVs are still more environmentally friendly than ICE vehicles. There is no tailpipe emission from EVs. Furthermore, the growing trend of including renewable energy for power generation by utilities helps in reducing overall carbon footprint by EVs [5].

3) Low charging cost: The fuel cost of driving an EV is dependent on the cost of electricity per kilowatt-hour (kWh) and the energy efficiency of the vehicle. Typically, with the higher energy efficiency and lower electricity cost, EVs have much lower energy cost per mile than that of ICE vehicles [8]. For HEVs and PHEVs, although they have ICEs, the miles per gallon (MPG) is always higher than that of conventional ICE vehicles, which means the total fuel cost of HEVs and PHEVs is still lower.

4) Maintenance benefits: EVs runs on electrically powered engines with less mechanical components and lubrication requirements. Therefore, EVs need less maintenance than normal gasoline powered cars [9].

5) Performance benefits: Comparing to ICEs, electric motors are very quiet and smooth. With accurate electric motor control, EVs are able to deliver a higher torque

during acceleration and achieve a better vehicle's stability. Therefore, EVs can provide an exhilarating driving experience.

1.2 EV Power System Configuration

Fig. 1-3 shows a typical EV power system configuration, which consists of an electric motor, an inverter, a high voltage battery pack, a 12 V low voltage auxiliary battery, and an onboard charger (OBC).

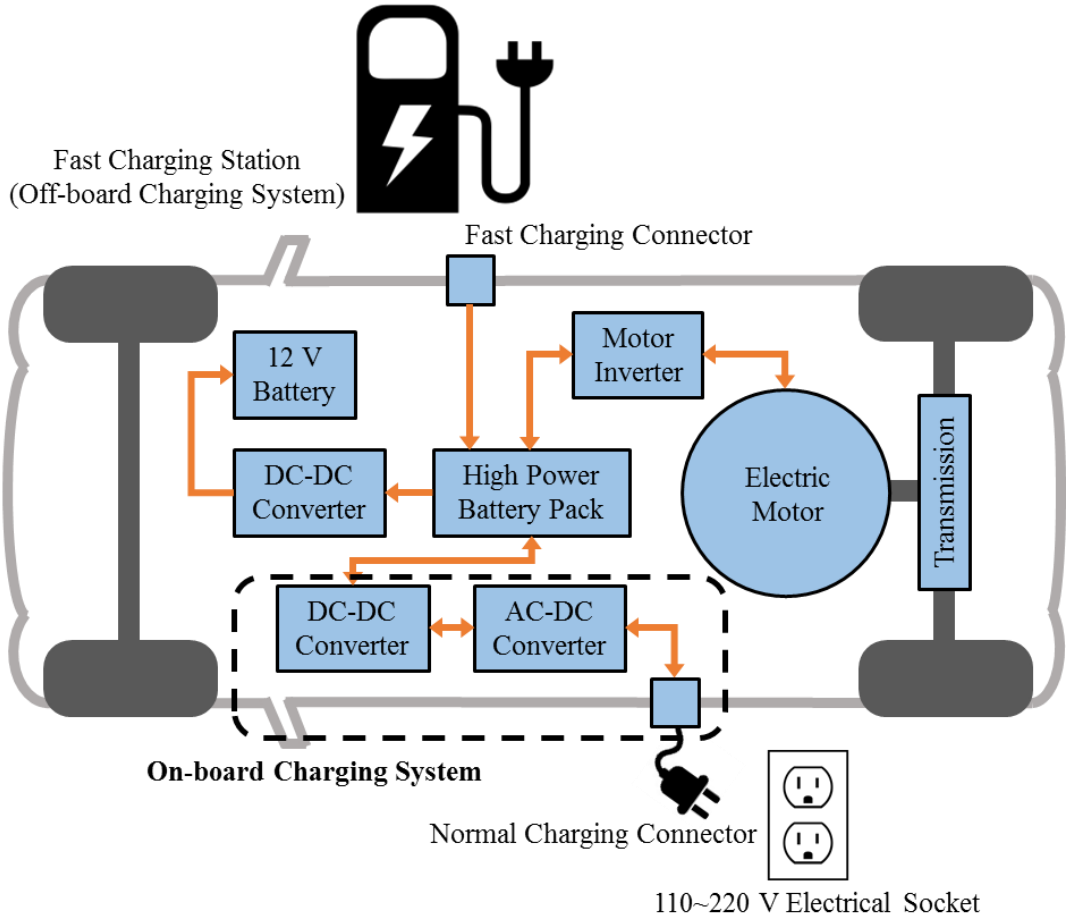


Fig. 1-3 Typical EV Power System Configuration.

There are two operation modes for the electric motor, propulsion and regenerative braking. In propulsion mode, the electric motor is propelled on the electric energy

stored in the high voltage battery. In regenerative braking mode, the electric motor works as a generator, which transfers the braking power to the high voltage battery. Therefore, the motor inverter should be able to operate in a bidirectional fashion.

The 12 V low voltage battery is charged by the high voltage battery through a DC-DC converter and provides power to the onboard auxiliary appliances, such as air conditioner, lights, stereo systems, and control systems. The power flow is unidirectional from high voltage battery to the low voltage battery.

The high voltage battery can be charged either by a slow or a fast charging system. A high power (up to 200 kW) off-board charging station is required for fast charging. The charging system has to be built off-board due to its large size and weight. The slow onboard charging system, which consists of a power factor correction (PFC) AC-DC converter and an isolated DC-DC converter, is designed for low to medium power rating (up to 17.2 kW) residential and/or office charging. The onboard charging system has low charging rate but allows EVs to charge everywhere through a wall socket. Since the slow chargers exist onboard of vehicles, weight and size play an important role in the design of OBCs.

1.3 EV Battery Charging Profile

For EV battery packs, energy density and weight are two critical parameters that determine the range of EVs. In comparison with different battery chemistries, such as lead-acid cell, nickel cadmium cell, and Ni-metal hydride cell, Li-ion cell has the highest energy density [10] with relatively light weight. Therefore, although Li-ion battery packs are more expensive than others, most of the EVs and PHEVs are still using them as their high voltage battery packs. Fortunately, as shown in Fig. 1-4, in

2016, the Li-ion battery price has dropped by 73% since 2010 [11]. The steep decrease in battery prices is in part due to improvements in technology and economies of scale. The fierce competition between major manufacturers also helps to bring down the prices [11]. The models in [11] also calculate that producing a battery in a Korean manufacturing plant in 2017 costs $162/kWh and dropping to $74/kWh in 2030. With falling prices and increasing energy density, it can be comprehended that the Li-ion battery technology will be a key enabler in EVs and PHEVs until a viable cost-effective substitute is developed.

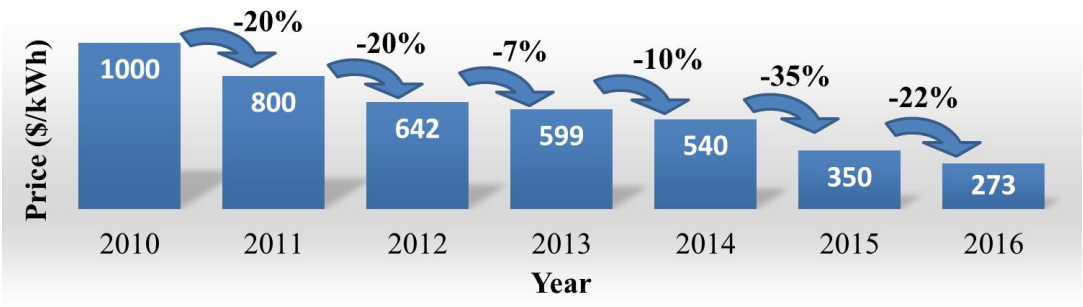


Fig. 1-4 Li-ion battery price survey, 2010-2016 [11].

Table 1-1 lists charging characteristics of some EVs and PHEVs available on the market including their New European Driving Cycle (NEDC) driving range. Most of these vehicles are equipped with Li-ion battery packs and level 1 or level 2 onboard charging systems.

Table 1-1 Charging characteristics of some manufactured EVs and PHEVs

Brand	Model	Model Year	Battery Energy Capacity (kWh)	Charge Power (kW)	Range NEDC (km)
Smart	fortwo El. Dr.	2015	17.6	3.3 (22)	145
Smart	fortwo BRABUS	2014	17.6	3.3 (22)	145
Toyta	iQ EV	2012	12	3	85
Fiat	500e	2015	24	6.6	-
Citroen	C-ZERO	2014	14.5	3.2	150
Peugeot	iOn	2014	14.5	3.2	150
Mitsubishi	i-MiEV	2014	16	3.7	160
Volkswagen	e-up!	2013	18.7	3.6	160
Chevrolet	Spark EV	2015	18.4	3.3	-
Bollore	Bluecar	2015	30	-	-
Mitsubishi	MiniCab MiEV	2014	16	3	-
BMW	i3	2014	22	7.4	190
Renault	Zoe	2015	22	43	240
Volvo	C30 Electric	2013	24	22	163
Volkswagen	e-Golf	2015	24.2	7.2	190
Nissan	Leaf (Visia)	2015	24	3.6 (6.6)	199
Nissan	Leaf (Acenta, SV)	2016	30	3.6 (6.6)	250
Honda	FIT EV	2014	20	6.6	-
Renault	Fluence Z.E.	2012	22	3.5	185
Ford	Focus EV	2015	23	6.6	162
Kia	Soul Electric	2015	27	6.6	212
Mercedes-Benz	B-Class El. Dr.	2015	36	10	200
BYD	e6	2015	61.4	40	-
Nissan	e-NV200 (Evalia)	2015	24	3.6 (6.6)	170

Toyota	RAV4 EV	2014	41.8	10	-
Tesla	Model S 60	2015	60	10(20)	390
Tesla	Model S 85	2016	85	10(20)	502
Tesla	Model X	2015	90	10(20)	-
Tesla	Roadster	2012	56	16.8	340
Rimac	Concept One	2015	82	22	600
Mercedes-Benz	SLS AMG El. Dr.	2015	60	22	250
Lightning	Lightning GT	2015	44	9	241
Detroit Electric	SP:01 Pure	2015	37	7.7	288
Venturi	Fetish	2015	54	-	-
Venturi	America	2014	53	22	-
Renovo	Coupe	2015	30	-	-
Audi	R8 e-tron	2015	90.3	7.2	450
Protoscar	LAMPO 3	2011	32	22	200

To safely charge Li-ion batteries, several charging methods are investigated to achieve a high charging acceptance rate [12]–[16]. Fig. 1-5 shows the constant current-constant voltage (CC-CV) charging profile, which is a well-established and widely used Li-ion battery charging method. A constant current is applied to charge batteries at the beginning of the charging cycle, while the charging voltage increases up to a preset maximum value (V_{max}), then the charging voltage is kept constant and correspondingly the charging current is reduced accordingly until the batteries are fully charged.

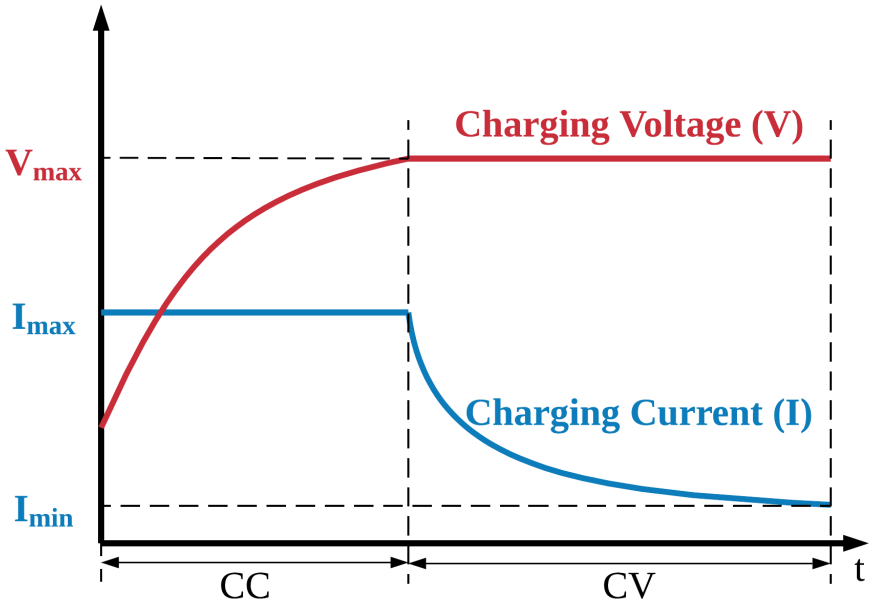


Fig. 1-5 CC-CV charging profile.

Another charging profile called multistage current charging (MSCC) algorithm is developed to optimize the battery charging process. Fig. 1-6 illustrates an example of an MSCC charging profile with 5 current stages. In this case, the charging current reduces to different levels but keeps constant in each level. In comparison with the CC-CV algorithm, the MSCC algorithm can achieve a faster charging speed and a higher charging efficiency. However, for the MSCC charging profile, the current values of different charging stages and at what time the charging process switches from one stage into another are the two issues that must be determined to avoid any damage to the batteries. Therefore, the control complexity of the MSCC is higher than that of the CC-CV.

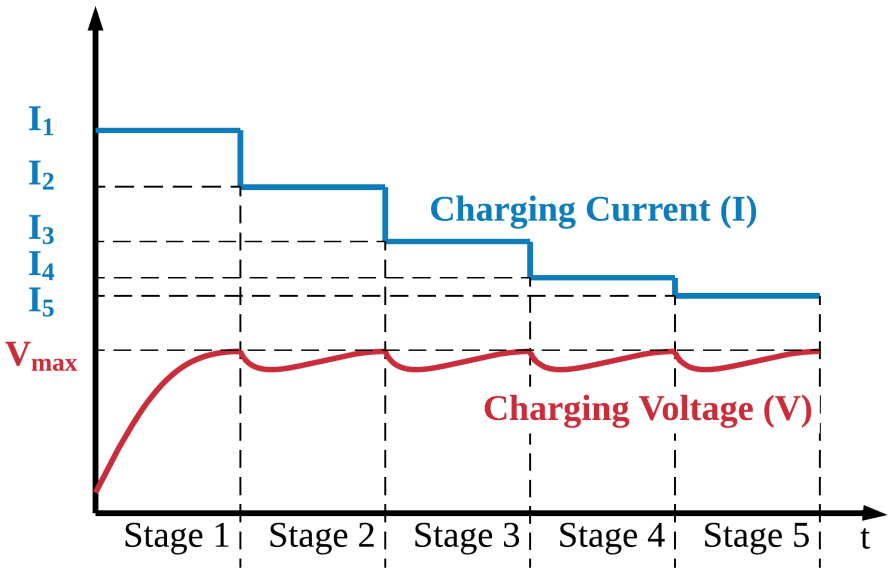


Fig. 1-6 MSCC charging profile.

Pulse charging method is another approach for fast and efficient charging [15], [16]. The pulse charging current can be modulated by either frequency (shown in Fig. 1-7(a)) or duty (illustrated in Fig. 1-7(b)). The main benefits of pulse charging are to reduce the accumulation of pressure inside the Li-ion batteries and be able to control the electrochemical reactions of the batteries. These benefits bring less heat producing and a higher charging efficiency as well as extend battery cycle life. Therefore, theoretically, the pulse charging method can achieve the best charging performance in comparison to others. However, this charging method requires highly complex control algorithm, which is difficult in implementation.

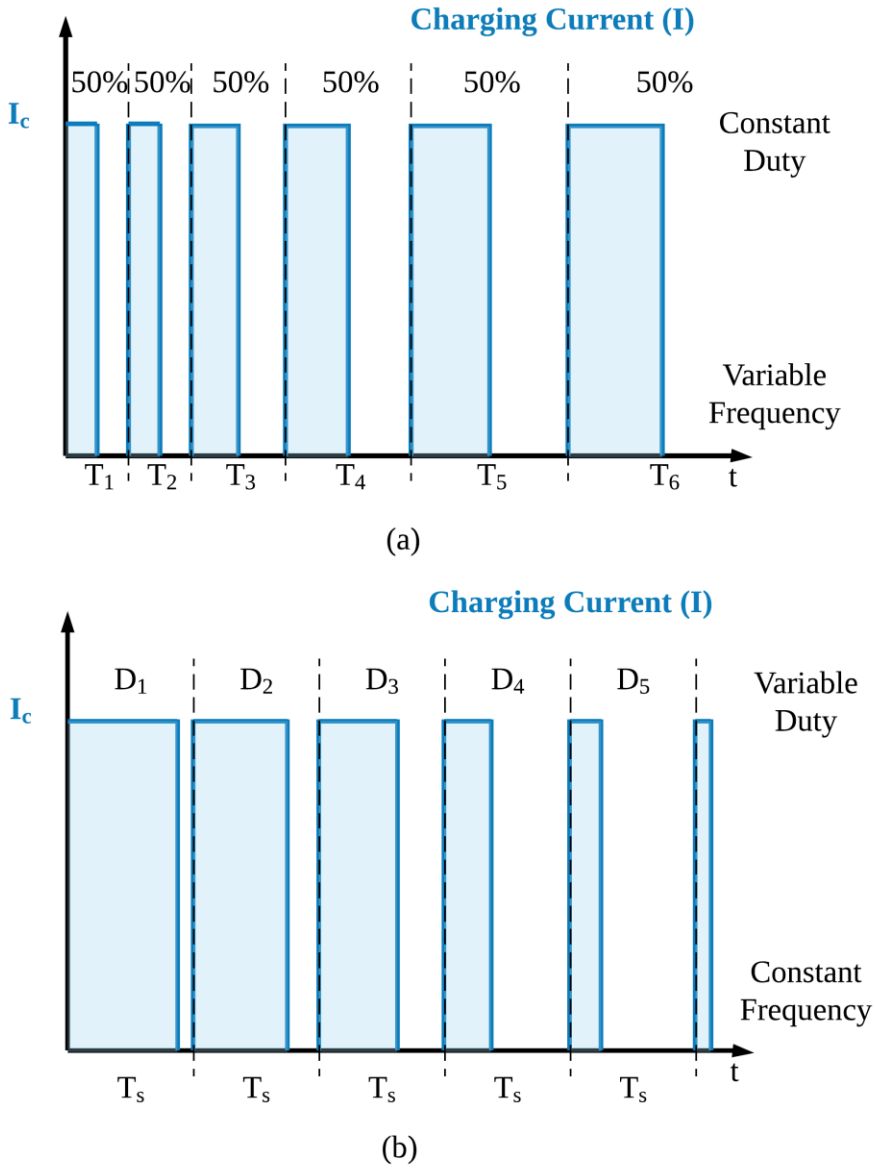


Fig. 1-7 Pulse charging profile with (a) variable frequency (b) variable duty.

Due to the reduced control complexity, the low-cost CC-CV charging technique is widely used in conventional onboard chargers available in the market. Hence, in this work, the CC-CV charging methodology is used to develop the design parameters of the converter.

1.4 EV Charging Techniques

1.4.1 Charging Power Levels

Table 1-2 summaries different charging power levels for EVs as proposed by SAE J1772 charging standard [5]. The charging level describes the maximum power output of an electric vehicle supply equipment (EVSE) outlet. The slow chargers typically use single-phase AC source as the input with relatively low power output levels. For the fast chargers, 3-phase AC sources are used to achieve high power levels. A new DC quick-charging standard is also established which enables fast charging up to 200 kW and developments are now targeting 350 kW [5].

Table 1-2 Charging power levels

Classification	Level	Current	Power
Slow chargers	Level 1	AC	$\leq$ 1.92 kW
	Level 2	AC	> 1.92 kW and $\leq$ 19.2 kW
Fast chargers	Level 3	AC, 3-phase	> 20 kW
	Level 3	DC	Currently, < 200 kW

Level 1 charger is designed for 120 V/12 A, 60 Hz, single phase grid outlet. It is easy to be built on-board with approximate $500 to $800 installation cost [17] which is applicable for home charging. However, the charging time of battery pack is slow at this charging power and it typically takes up to 17 hours to charge a 20-kWh battery pack from 20% state of charge (SOC) to full SOC.

A Level 2 charger requires 240 V single phase power outlet, which is available at public facilities and some house garages. With higher charging power, the level 2

charger needs much less charging time in comparison to a level 1 charger. The installation cost of a level 2 EVSE is expected to be $3,150 to $5,000 [18]. The level 2 charging is expected to be the main charging method available in the majority of public and private facilities [19].

Level 3 chargers utilize 3-phase AC sources or high-power DC sources to achieve ultra-fast charging. It is expected to charge the EV battery pack from 0 to 50% SOC in 20 minutes. Tesla has targeted a 5 minutes fully charging time for its EVs through its supercharging stations in the foreseeable future [20]. However, the extremely high costs including infrastructure, installation, and maintenance limit the large-scale deployment of the fast charging systems [21]. Furthermore, overheating and potential damage to the battery cells due to the rapid power delivery are other main issues that are under research. Moreover, local grid distribution facilities need to be upgraded to handle the intermittent ultra-high power demand from the grid caused by the fast charging [22], [23]. Consequently, the level 3 charging requires large off-board charging stations and is mainly designed for commercial and public charging applications [24], [25].

1.4.2 Alternative Charging Technique

Although the fast charging technique can significantly reduce the EV charging time, it is still much slower than filling up a traditional ICE car at a gas station. Instead of charging the EV battery pack overnight at home or waiting 30 minutes to 1 hour at charging stations, Tesla reported a battery swapping technique in 2013 [26]. The battery swapping technique takes only 90 seconds to swap an empty battery with a fully charged battery, which is even faster than filling up a gasoline car [27]. However,

current battery swapping technique is too specific to be applied to different models of EVs. Therefore, universal industrial battery swapping standards and the cost per swapping must be determined before widespread deployment of this technology.

1.5 EV Onboard Chargers

1.5.1 Charger Configuration

Researchers have studied various techniques to improve efficiency and power density of EV chargers [28]–[31]. A typical EV charger configuration is shown in Fig. 1-8, which consists of an AC-DC PFC stage and a galvanically isolated DC-DC converter [32], [33]. The PFC stage interfaces between the AC grid and a DC voltage link to achieve unity power factor and rectification [34]–[36]. The DC-DC stage interfaces the DC voltage link and an energy storage system, such as a high voltage battery pack [37]. An EMI filter is required between the grid and the PFC stage to filter out high-frequency noises generated by the PFC stage.

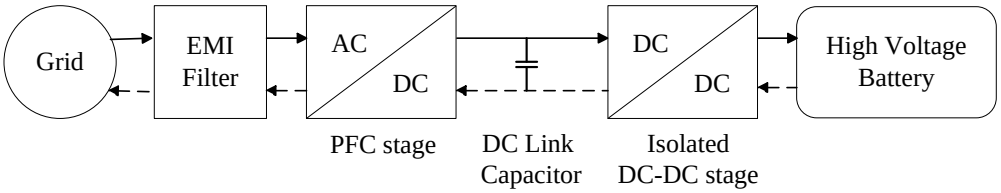


Fig. 1-8 Typical EV charger configuration.

1.5.2 Power Flow of Onboard Chargers

For unidirectional grid-to-vehicle (G2V) chargers, LLC converters are commonly selected as the DC-DC stage [38], [39]. Recent studies indicate that EVs can be considered as distributed power sources to store and send power back to the grid [40]–[42]. This vehicle-to-grid (V2G) concept allows EVs to provide voltage and frequency

regulation to the grid, absorb excess electricity and deliver it to the grid during periods of high demand. Additionally, V2G capability helps the users to supply power to household appliances in case of emergencies. The V2G capability requires EVs to have bidirectional charging systems which are able to operate in two power flow modes: charging mode (G2V) and discharging mode (V2G). Therefore, all the stages of the onboard charger (shown in Fig. 1-8) including the EMI, PFC, and DC-DC converter require bidirectional functionality [43]–[46].

1.5.3 MHz Onboard Chargers

Table 1-3 lists specifications of selected commercial onboard chargers for EVs. It can be seen that the onboard chargers can take up considerable vehicle space and weight. Inside the chargers, passive components, such as inductors, transformers, and capacitors, are the bulkiest and heaviest parts. Therefore, in order to reduce the size and weight of the onboard chargers, higher operating frequencies becomes a necessity.

Table 1-3 Specifications of selected commercial on-board chargers for EVs

Manufacture	Model Number	Input (V_{AC})	Output (V_{DC})	Power Rating (kW)	Efficiency	Cooling System	Size (L)	Weight (kg)
Delphi	N/A	85-265	170-440	3.3	94%	Liquid	5.6	5
Currentways	N/A	110-240	112-450	3	92%	Air	13.7	12
Currentways	N/A	110-240	112-450	3	92%	Liquid	7.5	N/A
Currentways	N/A	110-240	112-450	6.6	96%	Liquid	N/A	N/A
Delta	N/A	220	N/A	3.3	94%	N/A	5.5	N/A
Delta	N/A	240	N/A	6.6	94%	N/A	5.6	N/A
Lear	N/A	110-240	200-420	3.3	92%	Liquid	11.7	9.3
Signet	N/A	N/A	N/A	3.3	92%	Air	19.2	15

Global Power Eletronics	N/A	85-265	200-430	3.5	95%	N/A	3.2	3.7
Global Power Eletronics	N/A	85-265	200-430	6.6	95%	N/A	4.1	4
Brusa	NLG664	200-250	200-450	6.5	90%	Liquid	11	12
Brusa	NLG513	100-264	200-520	3.3	93%	Air	7.3	6.3
Brusa	NLG513	100-264	200-520	3.3	93%	Liquid	5.9	6.2
Brusa	NLG664	360-440	310-430	22	94%	Liquid	14.9	12.0
Brusa	NLG667	360-440	570-750	22	94%	Liquid	14.9	12.0
Tesla	N/A	85-300	50-430	19.8	N/A	Liquid	N/A	N/A

For a power MOSFET based onboard charger, the typical operating frequency is less than 100 kHz. For an IGBT based system, the operating frequency is in tens of kHz level. Theoretically, if the nominal operating frequency is increased from tens of kHz to 1 MHz, the size and weight of an onboard charger can be reduced by about 50% [47].

1.6 Power Device Selection for Onboard Chargers

MHz level operating frequency with multi-kW power rating is not achievable using conventional power devices. Traditional power switches, such as IGBTs, have very high voltage and current ratings (>1 kV, >500 A), therefore they are appropriate for applications with multi-kW power levels. However, IGBTs have a very low operating frequency (<20 kHz) [48], which results in bulky passive components in the converters. In comparison, silicon (Si) based power MOSFETs can achieve high frequency (>200 kHz) with multi-kW operation [49], but have a restricted operating temperature, which increases the cooling requirements for high power EV chargers leading to low power

density. Research on emerging wide bandgap (WBG) semiconductors, such as silicon carbide (SiC) and Gallium Nitride (GaN) based power devices, promote the development of high-power, high-switching-frequency MOSFETs with high operating temperatures. The properties of the WBG device make it a very good candidate for power dense applications in harsh environment. Hence, automotive manufacturers are considering SiC WBG devices for their future products [50], [51].

Table 1-4 lists some major electrical properties of different semiconductor materials [52], [53]. SiC and GaN have higher bandgaps in comparison with Si, which means more energy is needed for an electron moving from valence band to conduction band. This property brings the SiC and GaN higher temperature stability and makes them more suitable for the high-temperature environment such as the harsh operating conditions inside a vehicle. Furthermore, the WBG semiconductors have much higher electric breakdown fields than Si-based semiconductors, which leads to increased voltage blocking capabilities. Therefore, theoretically, with the same layer structure and dopant density, WBG materials can achieve higher drain-source voltages. In other words, with the same breakdown voltage, WBG semiconductors requires much lower blocking layer thickness.

Table 1-4 Electric properties of different semiconductors

Property	Si	GaAs	3C-SiC	6H-SiC	4H-SiC	GaN
Bandgap (eV)	1.12	1.43	2.4	3.0	3.2	3.4
Electric Breakdown Field (MV/cm)	0.25	0.3	2.0	2.5	2.2	3.0
Electron Mobility ($cm^2/V{\cdot}s$)	1350	8500	1000	500	950	800
Hole Mobility ($cm^2/V{\cdot}s$)	480	400	40	80	120	30

Thermal Conductivity (W/cm·K)	1.5	0.5	5.0	5.0	5.0	1.3
Direct/Indirect Bandgap	I	D	I	I	I	D

Due to these benefits, WBG semiconductor market is emerging rapidly in recent years [54]. Table 1-5 lists some major parameters of selected commercial MOSFETs [55]–[58]. It can be seen that, in comparison with Si-based devices, with the similar drain-source voltage and drain current, SiC and GaN devices have much less drain-source on resistances, which brings much lower conduction losses. Furthermore, reduced input and output capacitances make the WBG devices able to operate at high frequencies with lower gate driving and switching losses. Moreover, the body diode reverse recovery time and charge of the SiC device are much lower and less than those of the Si devices, which further lowers switching losses of the SiC device. For the GaN device, there is no intrinsic body diode, which means zero reverse recovery charge. This property allows GaN devices to be operated at multi-MHz levels with relatively low switching losses.

Table 1-5 Parameters of selected commercial MOSFETs

Part Number	IPB60R160C6	APT24M120L	C3M0075120K	GS66508T
Material	Si	Si	SiC	GaN
Technology	CoolMOS super junction	POWER MOS 8TM	C3M	Island Technology
Drain-source voltage (V)	650	1200	1200	650
Drain current at 25ºC (A)	24	24	30	30
Static drain-source on resistance (mΩ)	160	500	75	50

Input capacitance (pF)	1660	8370	1350	260
Output capacitance (pF)	314	615	58	65
Fall time (ns)	8	42	11	5.2
Rise time (ns)	13	27	11	3.7
Body diode forward voltage (V)	0.9@11.3A	1V@12A	4.5V@10A	-
Body diode reverse recovery time (ns)	460	1270	18	-
Body diode reverse recovery charge (nC)	8200	30000	220	-
Price (USD)	3.09	19.80	12.50	16.25

*Price data is based on Mouser as of March 2018 and is subject to change.

With all of these benefits, WBG devices have a promising future for high-frequency and high-power applications. Therefore, this work utilizes SiC and GaN devices for the converter designs.

1.7 Challenges in MHz-level DC-DC Converters

1.7.1 Parasitic Components

The major challenge in MHz level converter design is to minimize the impact of parasitic components of the PCBs since the ringing caused by the parasitic components will significantly affect the normal operation of the converter, and may even lead to system failure. Therefore, the PCB should be well designed with short routing paths

and as few through-hole vias as possible in the gate driving circuits to avoid unexpected parasitic components.

1.7.2 High-frequency Magnetic Components

At MHz-level frequencies, the skin effect will significantly reduce the effective cross-section area of the magnetic component windings, which results in high conduction loss. Moreover, the proximity effect plays another important role in planar transformer winding loss. A well-designed winding structure is a necessity to achieve a power dense design with low losses on the magnetic components.

1.7.3 Switching Loss

With the increasing of operating frequency, the switching losses of the MOSFETs will significantly rise, which results in considerable efficiency drop. Therefore, soft-switching techniques, such as zero-voltage switching (ZVS) and zero-current switching (ZCS) must be applied to reduce switching loss at MHz frequency level.

1.7.4 High-frequency Control Signals and Gate Drivers

The converter is controlled by a DSP-based platform, for which the control signals must be clean and robust at MHz frequencies. The control platform should be fast enough to respond based on the feedback from the sensors. In addition, gate drivers have to be properly designed to follow the control signals at high frequencies, have enough power to drive the gates, and have high noise immunity.

1.7.5 Integration between PFC and DC-DC Stages

Although the work in this dissertation mainly focuses on the DC-DC stage, a well design for a two-stage integration is crucial for future work, which will include integration of all stages of an onboard charger. Both PFC and DC-DC stages are switched-mode power supplies (SMPSs), which generate high-frequency electromagnetic interference (EMI). It is challenging to avoid the propagation of noise between the two stages when they are connected. Since the charger consists of two power converting stages, an appropriate control strategy for coordinating the two stages and maximizing the efficiency is another challenge in the MHz bidirectional onboard charger design.

1.8 Intellectual Merit and Contributions

This work mainly focuses on high-frequency high-power-density DC-DC converters for EV onboard chargers using emerging WBG devices. The proposed circuit design methodology, the detailed modeling and design of high-frequency and high-power magnetic components, the innovative planar transformer design, and the concept of the compact onboard charger will have a profound impact on the next generation EVs and PHEVs or any other applications required high-power-density converters.

The main contributions of this work are listed as below:

1) Detailed analysis and comparison of CLLC and dual active bridge converters for EV onboard chargers are presented.
2) An innovative planar transformer design with adjustable leakage inductance is proposed.

3) A comprehensive power loss model for MHz-level, high-power planar transformer is established.
4) A novel GaN-based MHz level 3.3 kW CLLC converter is designed and implemented that achieves a peak efficiency of 97.2%. Based on our best knowledge, this is the world's first bidirectional CLLC converter with such high operating frequency and power rating. The power density of the prototype reaches 9.22 W/cm^3 (151.1 W/in^3), which is twice higher than other state-of-the-art designs.
5) A generalized loss evaluation methodology is also proposed in this work to provide detailed power loss analysis of the entire system. The proposed methodology can be applied to future designs of converters with even higher frequency and power ratings.

1.9 Summary and Outline of Dissertation

This chapter introduces the charging systems for EV applications. The benefits of high frequency bidirectional onboard chargers are presented, and the challenges in the design are discussed. Different charging profiles for Li-ion batteries are also introduced and a brief comparison of different types of power semiconductors is provided. The rest of this dissertation is organized as follows.

Chapter 2 provides an overview of the state-of-the-art bidirectional DC-DC converters. Five different bidirectional DC-DC topologies (half-bridge, Ćuk, SEPIC, CLLC, and DAB) are discussed and compared for EV onboard charger applications. Several designs of MHz-level converters are also reviewed. The potential topologies for onboard charger applications are selected as well in this chapter.

In Chapter 3, a comprehensive comparison between the two potential topologies, CLLC and DAB, are provided. The operating principle, design methodology and appropriate application of the two topologies are analyzed. Furthermore, the performances of the CLLC and DAB converter prototypes are demonstrated and compared in this chapter, and finally, the CLLC topology is selected for the MHz-level, high-power converter design.

In Chapter 4, an innovative design methodology of a planar transformer with adjustable leakage inductance is developed. A comprehensive power loss model of the proposed high frequency integrated planar transformer is also presented.

In Chapter 5, the design of a bidirectional CLLC converter with 1 MHz operating frequency and 3.3 kW power rating is presented. The transformer designed in Chapter 4 is applied to the proposed converter. A detailed system level power loss analysis is provided. Furthermore, a control methodology of the proposed converter is investigated and introduce. Moreover, a prototype is designed to validate the proof of concept. Simulation and experimental results demonstrate that the proposed high-frequency compact bidirectional converter achieves high efficiency with wide output range.

Finally, a conclusion of this dissertation, the contributions of the research work, and the future work are presented in Chapter 6.

Chapter 2 : High-frequency Bidirectional DC-DC Converters - State-of-the-Art

2.1 Introduction

For a bidirectional onboard charger, an ultra-compact, highly efficient, and bidirectional DC-DC converter is desired. In order to achieve those objectives, the topology for the final converter design must be chosen and optimized from several different types of DC-DC topologies.

In this chapter, the state-of-the-art DC-DC converters are reviewed for EV onboard charger applications. Section 2.2 compares the performances of conventional half-bridge, Ćuk, SEPIC, CLLC, and DAB converters to select the best candidates for the onboard charger application. In Section 2.3, several high-frequency converter designs are studied to show the current status of the research on high-frequency and high-power DC-DC converters. Finally, a summary of the reviews is conducted in Section 2.4.

2.2 Review of Bidirectional DC-DC Converters

Many topologies have the potential to function as the bidirectional DC-DC converters for EV chargers [59]–[67]. Fig. 2-1(a) illustrates a conventional bidirectional half-bridge DC-DC converter topology. It can operate in either buck or boost mode to transfer power in both directions. During G2V mode, switch S_2 keeps off and the converter operates as a buck DC-DC converter as shown in Fig. 2-1(b). Similarly, during V2G mode, switch S_1 keeps off and the converter acts as a boost DC-DC converter as illustrated in Fig. 2-1(c). Therefore, with this bidirectional DC-DC converter, the DC link voltage should be higher than the battery voltage.

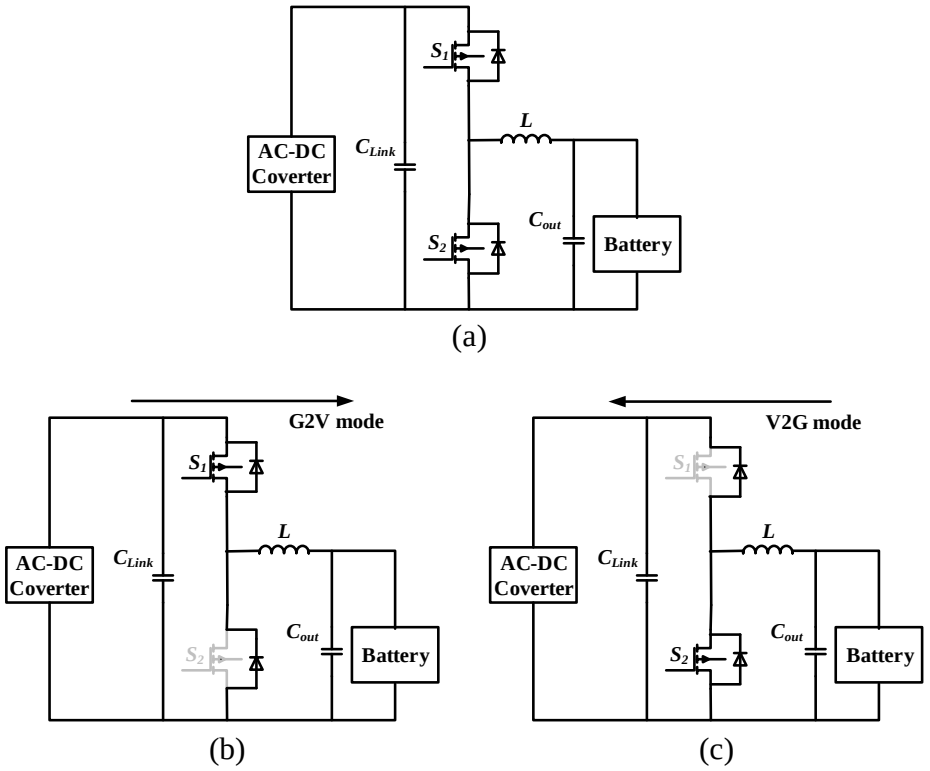


Fig. 2-1 Bidirectional half-bridge DC-DC converter (a) topology (b) G2V mode (c) V2G mode.

Ćuk converter as shown in Fig. 2-2(a) is another bidirectional DC-DC converter [68], [69]. It basically consists of a boost topology and a buck topology in series connected with an energy storage capacitor C_1. The inductors L_1 and L_2 can be coupled for reducing input and output current ripples. The output voltage of the Ćuk converter can be either higher or lower than the input voltage in both directions. In the G2V mode, S_2 is off and the body diode of S_2 operates as the main diode (shown in Fig. 2-2(b)). Similarly, in V2G mode, S_1 keeps off and the body diode of S_2 works as the main diode (illustrated in Fig. 2-2(c)). In comparison with conventional half-bridge converter, the Ćuk converter has benefits of continuous input and output current with lower current ripples, which are beneficial properties for the battery charging and discharging.

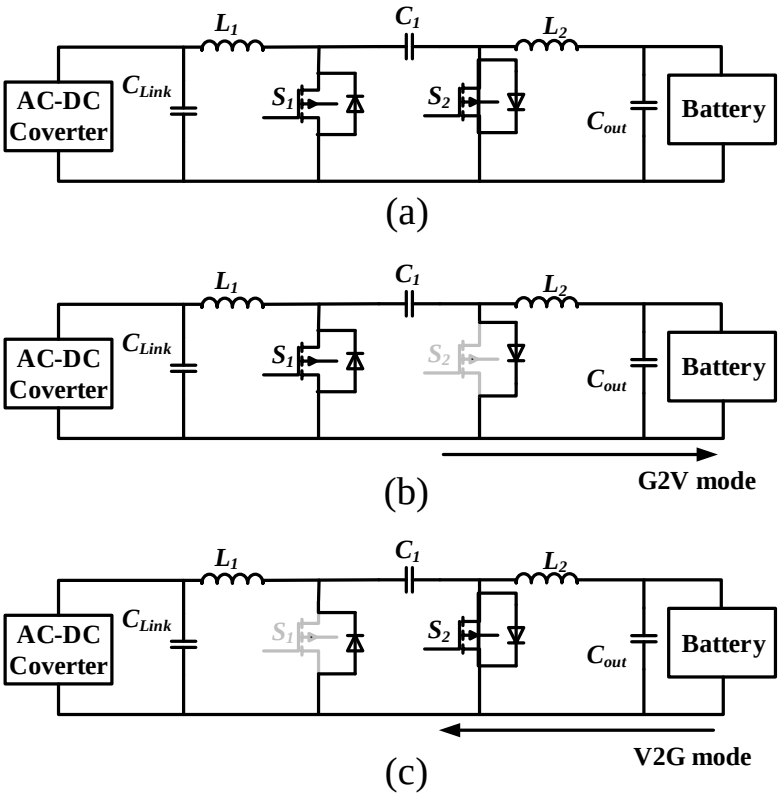


Fig. 2-2 Bidirectional Ćuk DC-DC converter (a) topology (b) G2V mode (c) V2G mode.

Fig. 2-3 shows a rearrangement of Ćuk converter called single-ended primary-inductor converter (SEPIC). It can also achieve either step-up or step-down gain with low current ripples and the operation modes are similar to those of the Ćuk converter. In addition, comparing to Ćuk converter, the output of SEPIC converter has the same polarity of the input.

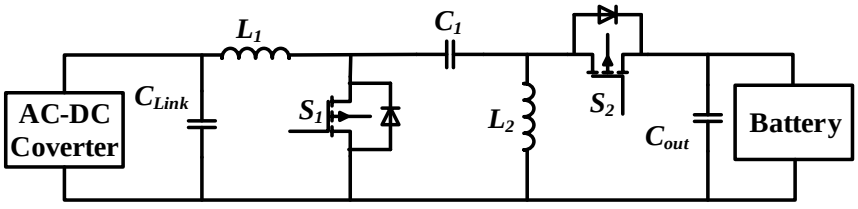


Fig. 2-3 Bidirectional SEPIC DC-DC converter.

One main issue of the DC-DC converters listed above is they operating under hard-switching conditions. The switching loss would be huge when the converters operate at MHz frequencies, which makes these converters not suitable for high-frequency designs. To achieve soft-switching operations, several variations of the conventional bidirectional DC-DC converters have been studied and developed [70]–[79]. However, those topology changes make the converters bulkier and heavier and the control strategies become more complex. Another issue of these converters is they are all non-isolated, Typically, a galvanic isolation is required for an EV onboard charger for safety consideration. Therefore, isolated bidirectional DC-DC converters are more popular for the EV charger designs. Moreover, with an isolated transformer in the DC-DC converter, a much wider gain range can be achieved and the control complexity becomes relatively lower.

CLLC and dual active bridge (DAB) converters are two typical galvanically isolated bidirectional isolated DC-DC converters, which are commonly used as the DC-DC stages for bidirectional EV chargers due to their advantages in terms of high power density, high efficiency, buck/boost capability, and controllable bidirectional power transfer [80]–[88]. Furthermore, both CLLC and DAB converters can achieve soft-switching operation naturally without adding any auxiliary circuits.

Both CLLC and DAB circuits can be designed with full-bridge and half-bridge structures. Different topologies require different design methods and are appropriate for different applications. A bidirectional full-bridge CLLC (FBCLLC) converter (illustrated in Fig. 2-4(a)) is introduced in [89]. The converter is proposed for a 500 W power rating, 400 V input, and 48 V output UPS system, and possesses ZVS and ZCS

features to minimize switching loss. The highest efficiency of the prototype exceeds 96%. In [90], a design methodology for a 5 kW FBCLLC converter with soft start control is presented. The prototype is proposed for a 380 V DC power distribution system and the highest efficiency is 97.8% at 4 kW. A CLLC-compensated capacitive power transfer system for electric vehicle charging applications is proposed in [91]. The power rating of the system is 2.9 kW and the efficiency is 89.3%. Basic operating principles and simulation results of a half-bridge CLLC (HBCLLC) converter (shown in Fig. 2-4(b)) are reported in [92] without providing detailed experimental verification.

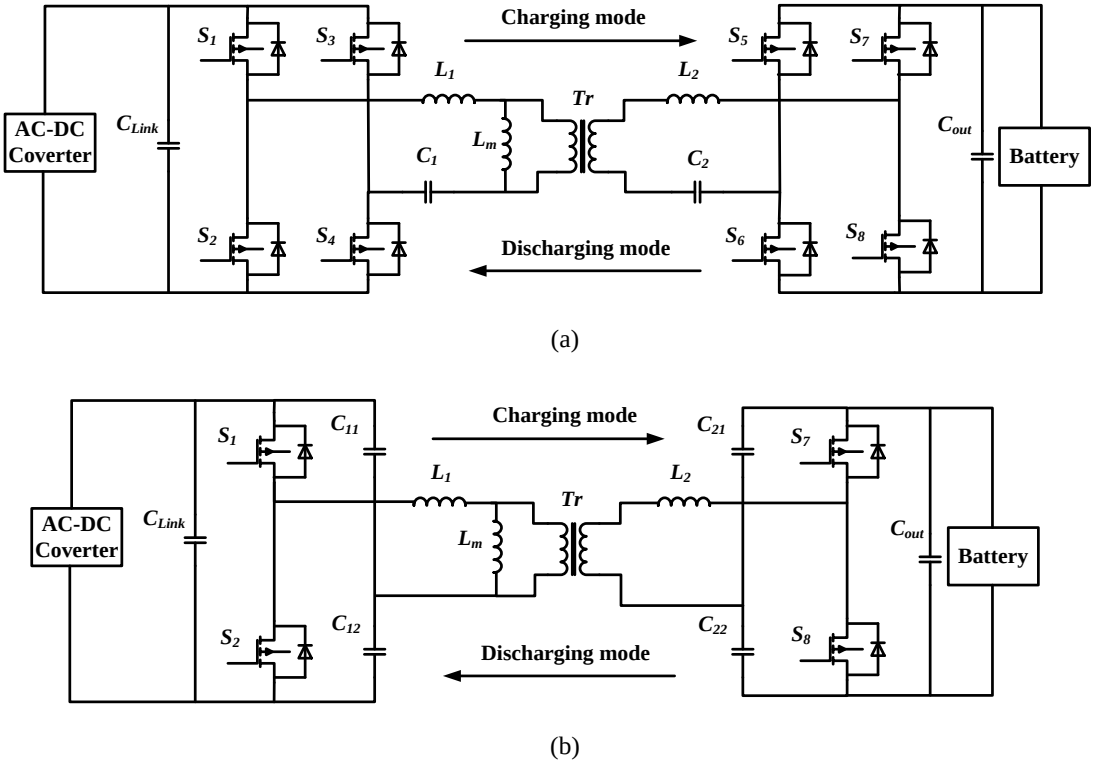
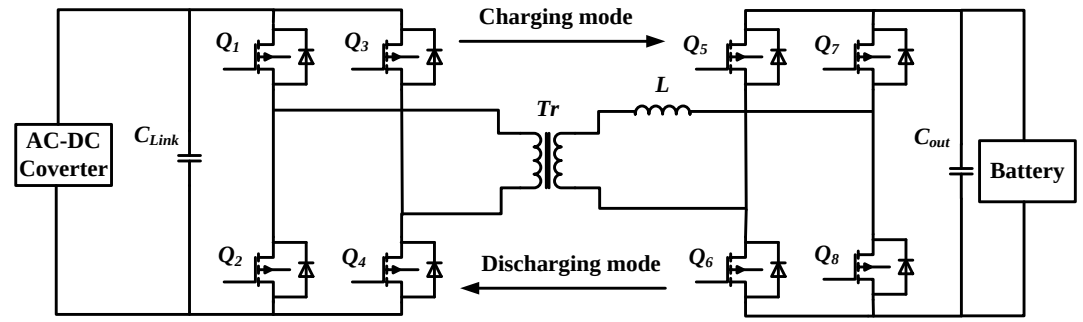


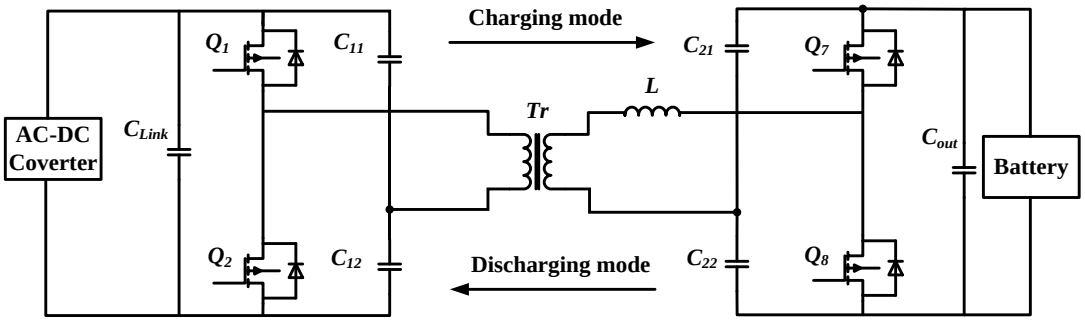
Fig. 2-4 Bidirectional (a) FBCLLC and (b) HBCLLC resonant converters.

Fig. 2-5(a) illustrates the topology of a full-bridge DAB (FBDAB) converter. An overall study of FBDAB converters, including steady state and small-signal analyses, is presented in [93]. Detailed operating principles, design considerations, and control

method for a 10 kW FBDAB converter are discussed in [94]. Furthermore, [95] presents a design of a 5 kW prototype FBDAB converter for a 380 V input and 20-28 V output charger for a UPS system. The highest efficiency of this converter exceeds 96%. In addition, [96] presents a 7 kW, 390 V input and 180 V output FBDAB converter for aircraft electric energy storage systems. The highest measured efficiency of this prototype is 90%. An analysis of switching condition and loss modeling of GaN-based DAB converter for EV charger is provided in [97], the modeling is verified by experimental measurement of a 500 kHz GaN DAB converter. A half-bridge DAB (HBDAB) converter (illustrated in Fig. 2-5(b)) for EV onboard charger is introduced in [98], and a 600 W prototype converter is built to verify the theoretical analysis and control method. An averaged-switch based small signal modeling of an HBDAB converter is proposed in [99], and a control method based on the small signal modeling is verified by a low power level prototype. By analyzing the optimal operation regions of both FBDAB and HBDAB converters, [100] proposes a combined circuit which is able to switch between FBDAB and HBDAB to achieve high efficiency for a wide load range. The validity of the circuit is verified by an 800 W prototype and the maximum efficiencies are 92.9% at light load and 93.4% at full load.



(a)



(b)

Fig. 2-5 Bidirectional (a) FBDAB and (b) HBDAB resonant converters.

Frequency modulation is the basic control method for both FBCLLC and HBCLLC circuits. For FBDAB circuits, various control strategies, such as single-phase-shift (SPS), extended-phase-shift (EPS), dual-phase-shift (DPS), and triple-phase-shift (TPS) controls, can be applied through manipulating the on/off status of the switches on both primary and secondary sides of the converters [101]–[103]. For an HBDAB circuit, which consists of four switches, only SPS control method can be applied. However, the half-bridge topology has benefits in terms of reduced size, weight and cost, due to the reduction of the switches, corresponding driving circuits, and cooling systems.

Therefore, both CLLC and DAB DC-DC converters can be the candidates for EV onboard chargers. A comprehensive analysis and comparison of these two bidirectional resonant DC-DC converters will be provided in next chapter.

2.3 Review of MHz-level DC-DC Converter Designs

As mentioned in Chapter 1, it is a challenge to design a DC-DC converter with MHz-level operating frequency and multi-kW power rating, simultaneously. Most of the available designes can achieve either high-power-low-frequency or high-frequency-low-power designs [104]–[109]. Most of the research on MHz range power converters still focuses on unidirectional converters, and the power levels are below 1 kW. A 1 MHz LLC resonant converter based on a DSP-driven Silicon-On-Insulator (SOI) power MOS Module has been designed in [105]. The maximum output power is 120 W and the highest efficiency is 94%. A GaN-based 25 V to 100 V Dickson switched-capacitor converter is designed in [106], and the converter achieves a switching frequency of 1.2 MHz and a peak efficiency of 92%. However, the maximum power output is only 263 W. In [107], a GaN-based 40 to 180 V input, 351 V output boost converter is proposed. The operating frequency reaches 1 MHZ, and the maximum power output is 425 W with 95% efficiency.

To achieve high-frequency and high-power operations, WBG devices are typically used in the designs. SiC devices, with over 1.2 kV voltage rating and over 48 A current rating, have operated successfully in a 1 MHz 1.2 kW converter [104]. The low on-resistance of the SiC MOSFETs brings low switch conduction loss in the design. As shown in the previous chapter, comparing to SiC MOSFETs, GaN MOSFETs have even lower on-resistance and shorter falling and rising times, which means the GaN

MOSFETs are able to operate at a higher frequency with lower conduction and switching losses. In [47], it is shown that increasing the switching frequency from 65 kHz to 1 MHz with GaN switches helps reduce the combined size of capacitors and inductors by about 50%. Two GaN-based 6.6 kW CLLC converters as a part of the onboard chargers are designed in [108], [109]. The converter operates at 500 kHz with the objective of making the magnetics flat-profile, which was facilitated by two interleaved planar transformers.

Based on the specifications, both SiC and GaN MOSFETs have the potential to be used as the switches in high-frequency on-board chargers of EVs.

2.4 Summary

In this chapter, different DC-DC converter topologies are discussed and compared. It is concluded that for high-frequency, high-power, bidirectional DC-DC converter designs, CLLC and DAB topologies are the best candidates due to their wide output range, high efficiency, galvanic isolation and capability of bidirectional power transfer. The detailed analysis and final topology selected for MHz-frequency design will be discussed in next chapter.

Chapter 3 : Comprehensive Analysis and Comparison of CLLC and DAB Converters for EV Onboard Charger Applications

3.1 Introduction

Among all the DC-DC topologies reviewed in Chapter 2, the CLLC and the DAB are the best two topologies for high frequency bidirectional onboard chargers for the following reasons:

1) Wide gain range: Both CLLC and the DAB converters have wide gain ranges. In addition, the transformer turns ratio can be adjusted to further extend the gain range.
2) Higher efficiency: Both CLLC and DAB are resonant converters. With careful design, the switches in these converters can operate with soft-switching, which would significantly reduce the switching loss, especially at MHz operating frequencies.
3) Galvanic isolation: Due to the existence of the transformer, the primary and secondary sides are galvanically isolated, which ensures the safety of the battery and the grid against electric failures.

CLLC and DAB converters have different structures and operating principles, and both of them have half-bridge variations. In order to determine which topology is the most appropriate for EV chargers, it is necessary to discuss the advantages and disadvantages of the different topologies. In this chapter, four DC-DC converter topologies, FBCLLC, HBCLLC, FBDAB, and HBDAB, are analyzed. The design

methods of the four topologies for EV charging systems are introduced, and 1 kW 200 kHz prototypes for each topology are built to validate the analysis and designs.

3.2 Theoretical Analysis

CLLC and DAB converters are resonant switching converters. In order to ensure higher efficiency, the circuits need to be designed to operate under soft-switching conditions. In the case of CLLC converters, ZVS operation can be achieved on primary side power MOSFETs, while ZVS and ZCS operations can be realized on secondary side rectifiers. In the case of DAB converters, both primary and secondary side power MOSFETs can operate under ZVS condition.

3.2.1 Bidirectional CLLC Converters

A) Operating Principles

The bidirectional CLLC converters have symmetrical structures consisting of primary inverting stages and secondary rectifying stages. For the FBCLLC circuit (shown in Fig. 3-1(a)), L_1 and L_2 are resonant inductors, C_1 and C_2 are resonant capacitors. In comparison, the HBCLLC circuit (shown in Fig. 3-1(b)) uses bridge capacitors (C_{11}, C_{12}, C_{21}, and C_{22}) as resonant capacitors. The turns ratio of the transformer T_r is $n:1$, and its magnetizing inductance is L_m.

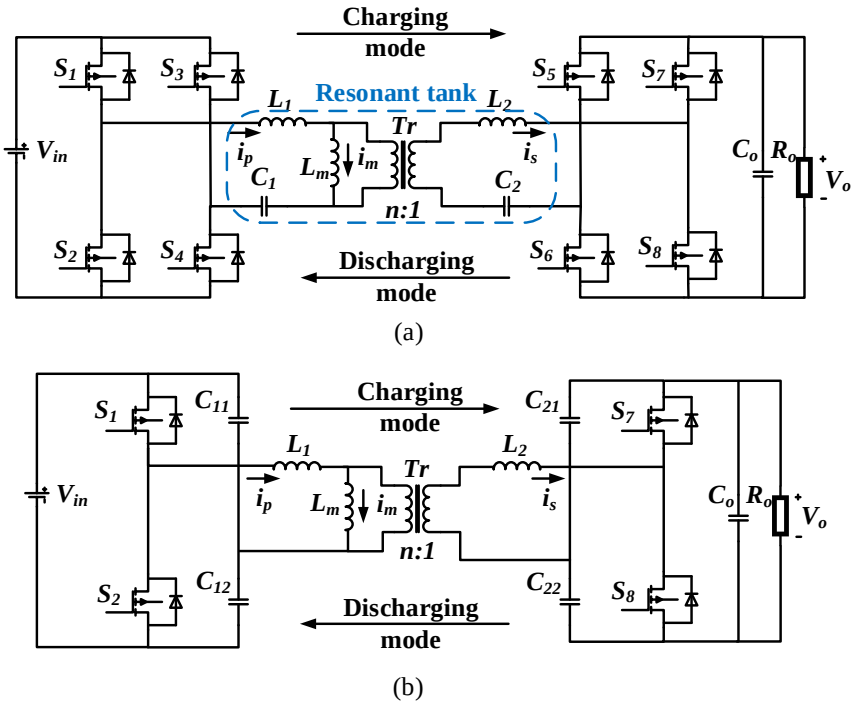


Fig. 3-1 Bidirectional (a) FBCLLC and (b) HBCLLC resonant converters.

The resonant components form a resonant tank in the converter which is shown in Fig. 3-1(a), and the resonant tank performs either capacitive or inductive with different operating frequencies. Fig. 3-2(a) shows the waveforms of the resonant tank voltage and current when the circuit operates in the capacitive region, which results in $i_{tank}(t)$ leading $v_{tank}(t)$ with a phase difference of $\varphi_{leading}$. It can be seen from the figure that the switches turn off with ZCS, however, when the switches turn on and freewheeling diodes turn off, hard switching occurs. The reverse recovery process of freewheeling results in significant switching losses and considerable electromagnetic interference (EMI) noises. Therefore, it is not recommended to apply this capacitive operation to high-frequency applications [110].

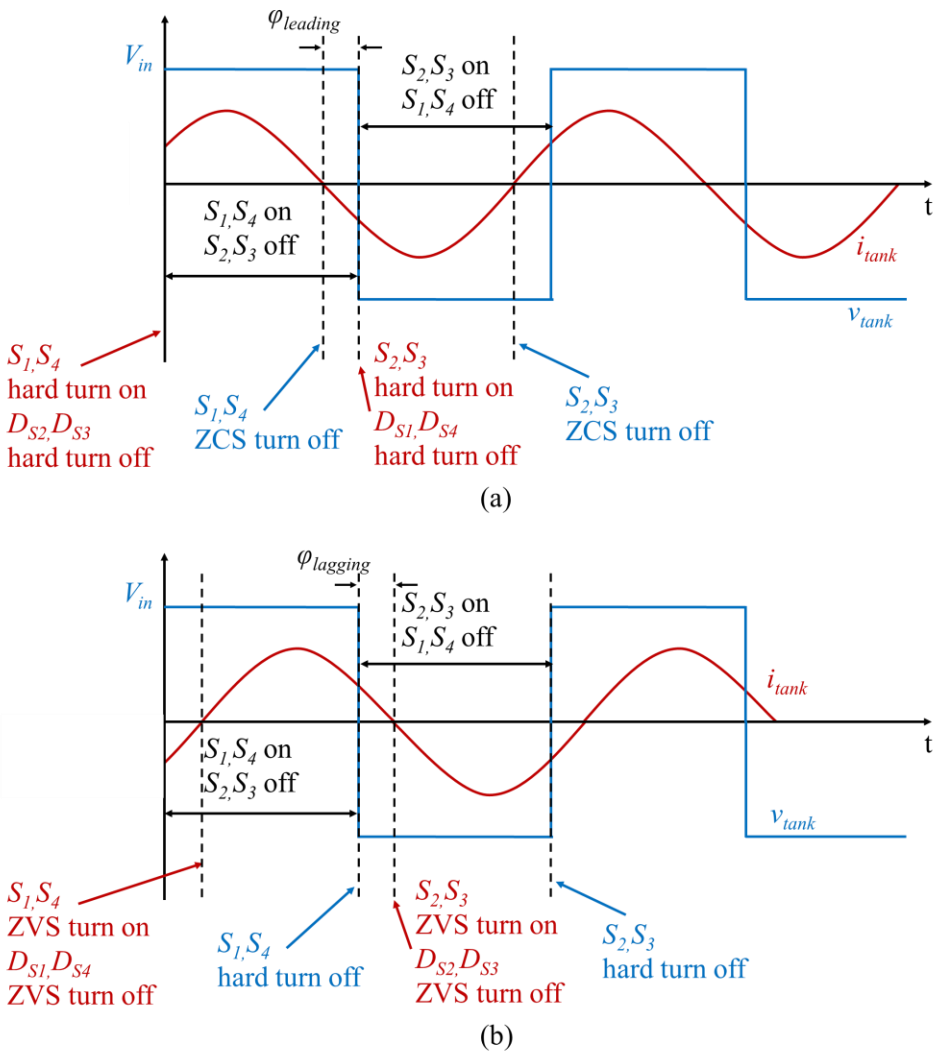


Fig. 3-2 Resonant tack voltage and current with (a) capacitive tank and (b) inductive tank

In comparison, Fig. 3-2(b) illustrates the waveforms of resonant tank voltage and current when the circuit operates in the inductive region. In this case, $i_{tank}(t)$ lags $v_{tank}(t)$ with a phase difference of $\varphi_{lagging}$. As seen in the figure, although the turn-off process of the switches is hard switching, the switches turn on with soft switching. Furthermore, the freewheeling diodes achieve soft switching during both turn-on and turn-off processes. Therefore, the reverse recovery losses from the diodes are eliminated, and

the EMI noises can be significantly reduced. Based on this analysis, in high-frequency and high-power applications, the CLLC converter is required to operate in the inductive region.

Fig. 3-3 illustrates detailed waveforms of a typical bidirectional FBCLLC or HBCLLC circuit operating at a switching frequency lower than its resonant frequency (f_s<f_r). The dead band duration is the time between t_a and t_b, where all the switches are off to prevent the bridge from shoot-through. In this interval, no power transfers to the secondary side, and the secondary side resonant inductor current, i_s, is zero. At time t_b, the gate voltages, v_{s1} and v_{s2} (only v_{s1} for the HBCLLC circuit) are applied. The primary side resonant inductor current, i_p, is negative, which means the current freewheels through the body diodes of S_1 and S_4 (only S_1 for the HBCLLC circuit), therefore S_1 and S_4 (only S_1 for the HBCLLC circuit) will turn on with ZVS at t_1. Beyond t_b, power transfers from the primary side to the secondary side through the transformer and i_s is positive. Between t_b and t_c, i_p resonates and the magnetizing inductance current, i_m, keeps increasing almost linearly, since L_m is much larger than L_1. When i_p meets i_m at t_c, previous resonance stops, and no power transfers to the secondary side, hence i_s becomes zero. The body diodes of S_6 and S_7 (only S_7 for the HBCLLC circuit) will turn off with ZCS naturally. The other half cycle has similar operating mode but with opposite current direction.

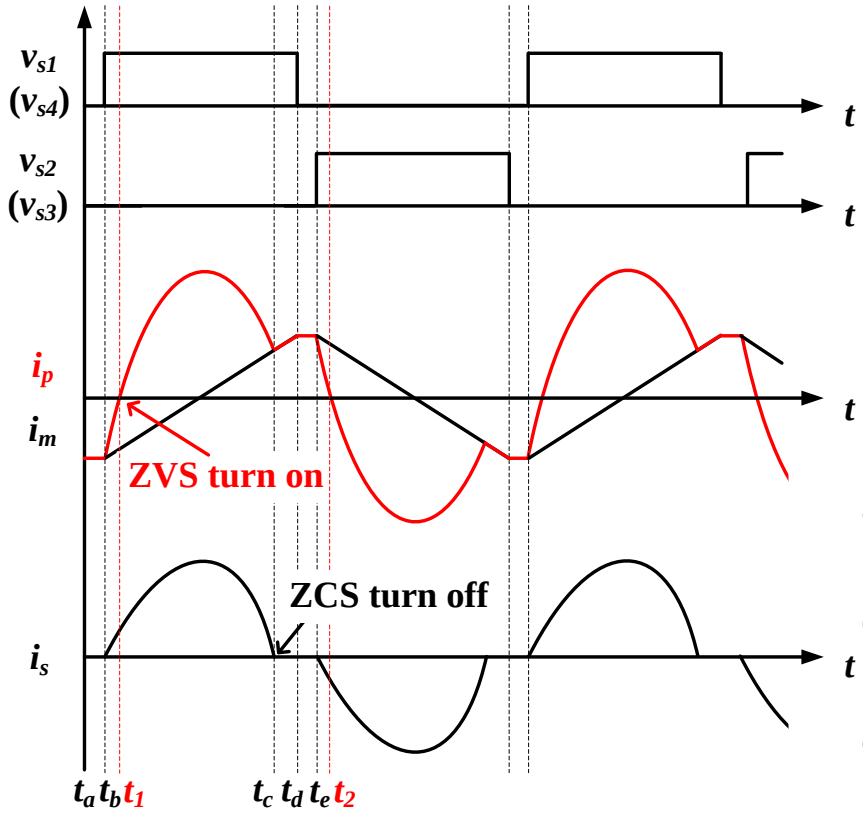


Fig. 3-3 Typical waveforms of a bidirectional FBCLLC or HBCLLC converter operating at a frequency lower than the resonant frequency ($fs < fr$).

The waveforms when the converters operate at the resonant frequency ($f_s = f_r$) and a frequency higher than the resonant frequency ($f_s > f_r$) are shown in Fig. 3-4(a) and (b), respectively. It can be seen from the figure that, the waveforms in these cases are similar to those in the case of $f_s < f_r$, however, there is no "cutoff" time (duration between t_c and t_d in Fig. 3-3) in the cases of $f_s = f_r$ and $f_s > f_r$. Therefore, the output currents in these cases are continuous (ignore the deadtime) and the efficiencies are higher.

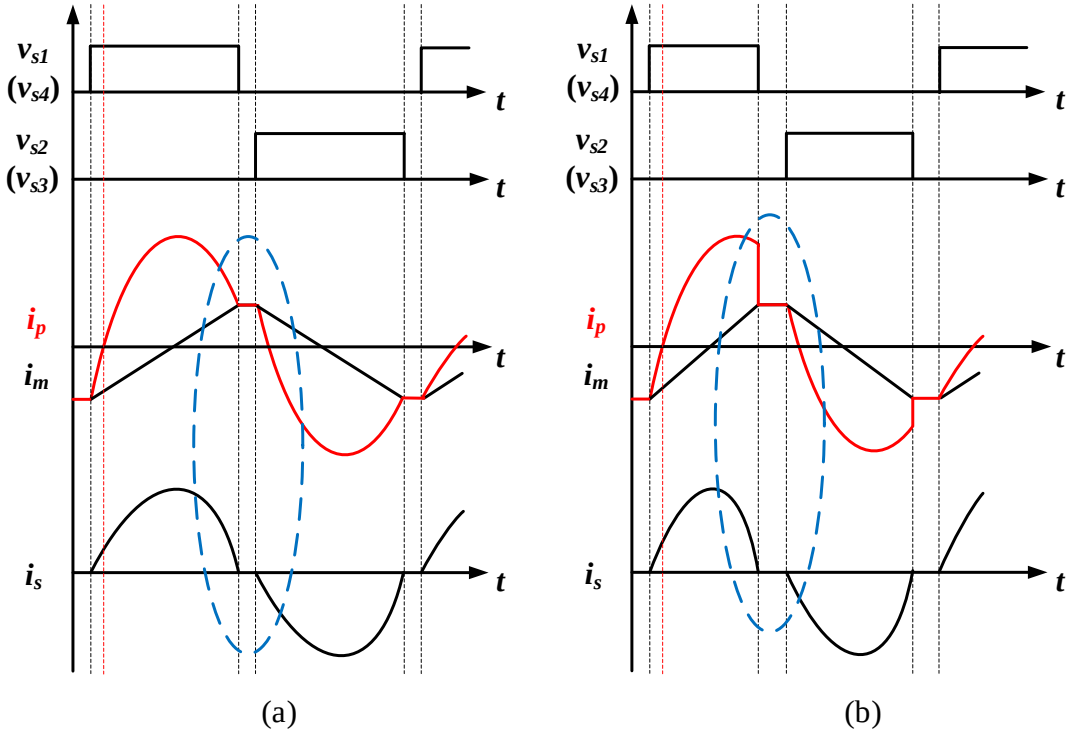


Fig. 3-4 Typical waveforms of a bidirectional FBCLLC or HBCLLC converter operating at (a) the resonant frequency ($f_s = f_r$) and (b) a frequency higher than the resonant frequency ($f_s > f_r$).

B) Gain Analysis

The equivalent circuits of the FBCLLC converter and HBCLLC converter for charging mode are shown in Fig. 3-5(a) and (b), respectively. R_e, L_2', and C_2' are the equivalent R_o, L_2, and C_2 of the converters, respectively.

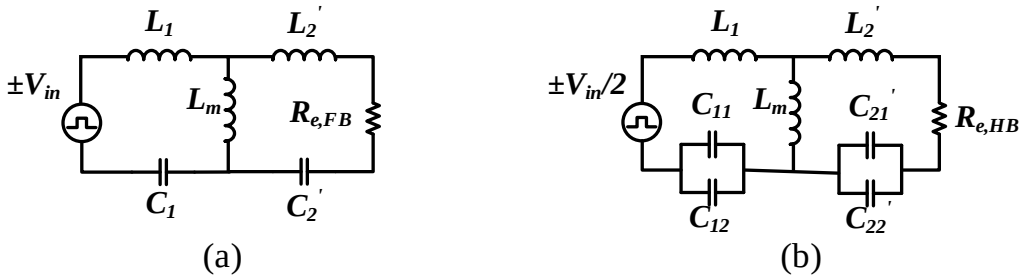


Fig. 3-5 Equivalent circuits of (a) the FBCLLC and (b) the HBCLLC converters in charging mode.

The general transfer function $H(s)$ of CLLC converters can be derived as follows:

$$H(s) = \frac{1}{n} \cdot \frac{R_{e,FB}}{R_{e,FB} + Z'_{L2} + Z'_{C2}} \cdot \frac{\left(R_{e,FB} + Z'_{L2} + Z'_{C2}\right) \parallel Z_{Lm}}{Z_{L1} + Z_{C1} + \left(R_{e,FB} + Z'_{L2} + Z'_{C2}\right) \parallel Z_{Lm}} \tag{3-1}$$

The gain of the FBCLLC converter can be calculated as

$$G_{CLLC,G2V} = |H(s)| = \left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{n} \cdot \frac{1}{\sqrt{a^2 + b^2}} \tag{3-2}$$

where,

$$a = \frac{1}{h} + 1 - \frac{1}{h \cdot \omega^2} \tag{3-3}$$

$$b = \left(\frac{k}{h} + 1 + \frac{1}{g \cdot h} + \frac{1}{g}\right)\frac{Q}{\omega} - \left(\frac{k}{h} + 1 + k\right)Q \cdot \omega - \frac{Q}{g \cdot h \cdot \omega^2} \tag{3-4}$$

$$\begin{cases} h = \dfrac{L_m}{L_1} \\ k = \dfrac{L'_2}{L_1} \\ g = \dfrac{C'_2}{C_1} \\ \omega = \dfrac{\omega_s}{\omega_r} \\ \omega_r = \dfrac{1}{\sqrt{L_1 C_1}} \\ Q = \dfrac{\sqrt{L_1/C_1}}{R_e} \end{cases} \tag{3-5}$$

ω_r and ω_s are the resonant frequency and operating frequency, respectively. ω is the normalized frequency, and Q is the quality factor. The First Harmonic Approximation (FHA) is applied to calculate the equivalent load. For FBCLLC circuit, the equivalent load, inductance, and capacitance can be calculated as:

$$\begin{cases} R_{e,FB} = \left(\dfrac{8n^2}{\pi^2}\right) R_o \\ L_2' = n^2 L_2 \\ C_2' = \dfrac{C_2}{n^2} \end{cases} \tag{3-6}$$

Similarly, for HBCLLC circuit, they are derived as follows:

$$\begin{cases} R_{e,HB} = \left(\dfrac{2n^2}{\pi^2}\right) R_o \\ L_2' = n^2 L_2 \\ C_1 = C_{11} + C_{12} \\ C_2' = C_{21}' + C_{22}' \\ C_{21}' = \dfrac{C_{21}}{n^2} \\ C_{22}' = \dfrac{C_{22}}{n^2} \end{cases} \tag{3-7}$$

Fig. 3-6 shows the gain curves versus normalized frequency at different loads (i.e. different Qs). The gain increases, but the slope of the curve decreases with a lower Q. To simplify the design, for both FBCLLC and HBCLLC converters, k and g are set to be 1, which means $L_1 = L_2'$ and $C_1 = C_2'$, and h is set to be 4. This brings the same resonant frequency in both G2V and V2G directions.

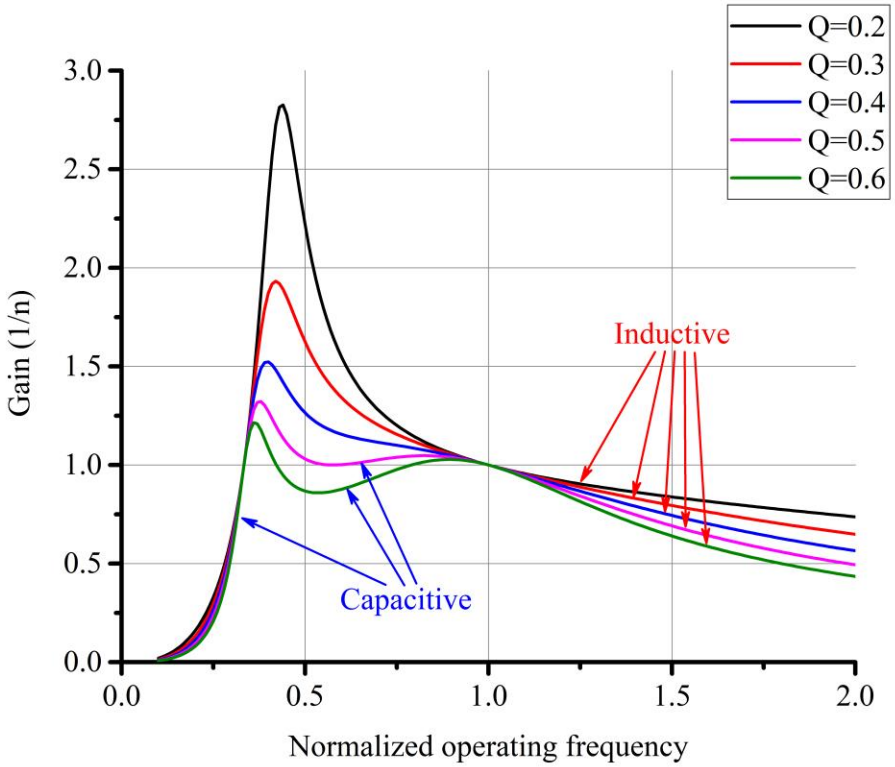


Fig. 3-6 Gain curves versus normalized frequency of CLLC converters at different loads.

In discharging mode, the equivalent circuits of the FBCLLC converter and the HBCLLC converter are shown in Fig. 3-7(a) and (b), respectively.

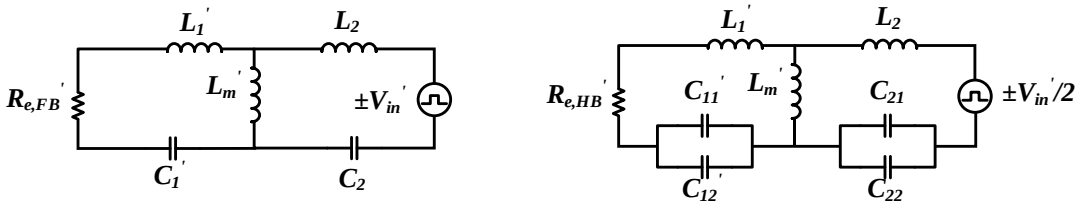


Fig. 3-7 Equivalent circuits of (a) the FBCLLC and (b) the HBCLLC converters in discharging mode.

For FBCLLC circuit, the parameters will be derived as:

$$\begin{cases} R'_{e,FB} = \left(\dfrac{8}{n^2\pi^2}\right) R'_o \\ L'_1 = \dfrac{L_1}{n^2} \\ C'_1 = n^2 C_1 \\ L'_m = \dfrac{L_m}{n^2} \end{cases} \tag{3-8}$$

Similarly, for HBCLLC circuit, they are derived as follows:

$$\begin{cases} R'_{e,HB} = \left(\dfrac{2}{n^2\pi^2}\right) R'_o \\ L'_1 = \dfrac{L_1}{n^2} \\ C'_1 = C'_{11} + C'_{12} \\ C_2 = C_{21} + C_{22} \\ C'_{11} = n^2 C_{21} \\ C'_{12} = n^2 C_{22} \\ L'_m = \dfrac{L_m}{n^2} \end{cases} \tag{3-9}$$

In discharging mode, the gain of the converter is derived as follows:

$$G_{CLLC,V2G} = n \cdot \frac{1}{\sqrt{c^2 + d^2}} \tag{3-10}$$

where,

$$c = \frac{1}{h'} + 1 - \frac{1}{h' \cdot \omega'^2} \tag{3-11}$$

$$d = \left(\frac{k'}{h'} + 1 + \frac{1}{g' \cdot h'} + \frac{1}{g'}\right)\frac{Q'}{\omega'} - \left(\frac{k'}{h'} + 1 + k'\right)Q' \cdot \omega' - \frac{Q'}{g' \cdot h' \cdot \omega'^3} \tag{3-12}$$

$$\begin{cases} h' = \dfrac{L'_m}{L_2} \\ k' = \dfrac{L'_1}{L_2} \\ g' = \dfrac{C'_1}{C_2} \\ \omega' = \dfrac{\omega_s}{\omega'_r} \\ \omega'_r = \dfrac{1}{\sqrt{L_2 C_2}} \\ Q' = \dfrac{\sqrt{L_2/C_2}}{R'_e} \end{cases} \tag{3-13}$$

With the same L and C values, the ω'_r, k', g', and h' of both FBCLLC and HBCLLC circuits will maintain the same values as the ω_r, k, g, and h in charging mode, respectively. However, Q' will change since the equivalent load changes. Q' can be calculated as:

$$Q' = \frac{n^2 R_o}{R'_o Q} \tag{3-14}$$

C) Soft-switching Region

Fig. 3-6 shows the inductive and capacitive resonate network regions of the CLLC circuit. The resonant network is inductive when the slope of the gain is negative. As previously discussed, soft switching can be realized in the inductive region. To ensure the primary switches turn on with ZVS, the magnetizing inductor current should be large enough to fully charge/discharge the output capacitors of the MOSFETs during the dead band time. The maximum value of L_m for a FBCLLC converter is derived in [90] as follows:

$$L_{m,FB} \leq \frac{t_{db}}{16 C_{oss} f_{s,max}} \tag{3-15}$$

Similarly, for an HBCLLC converter, the L_m can be calculated as:

$$L_{m,HB} \leq \frac{t_{db}}{8C_{oss}f_{s,max}} \tag{3-16}$$

where, t_{db} is the dead band time duration, C_{oss} is the output capacitance of the MOSFET, and $f_{s,max}$ is the maximum switching frequency.

3.2.2 Bidirectional DAB Converters

A) Operating Principles

Typical steady-state waveforms of an FBDAB converter (shown in Fig. 3-8(a)) with single-phase-shift control at heavy load conditions are shown in Fig. 3-9(a). It has been assumed that $V_{in}/n < V_o$ and $i_L(t_a) < 0$. T_s is the switching period, and $T_s = 1/f_s$, where f_s is the switching frequency. The phase-shift between the two bridges, t_{shift}, is $DT_s/2$, and D is from 0 to 0.5. v_1 is the voltage on the secondary side of the transformer, and v_2 is the input voltage of the rectifier. v_L is the voltage across the inductor, L, therefore, $v_L = v_1 - v_2$. i_L is the inductor current. Prior to t_a, Q_2, Q_3, Q_5 and Q_8 are on, and Q_1, Q_4, Q_6 and Q_7 are off. At t_a, Q_1 and Q_4 turn on, Q_2 and Q_3 turn off. t_{shift} later, Q_6 and Q_7 turn on, Q_5 and Q_8 turn off. i_L is negative at t_a and positive at t_b, which means Q_1, Q_4, Q_6 and Q_7 turn on with ZVS. However, in light load conditions, i_L may be positive at t_a and negative at t_b, as shown in Fig. 3-9(b), which means ZVS cannot be achieved. The other half cycle has similar operating modes but with opposite current direction. The HBDAB circuit (shown in Fig. 3-8(b)) has similar waveforms with half inductor voltage.

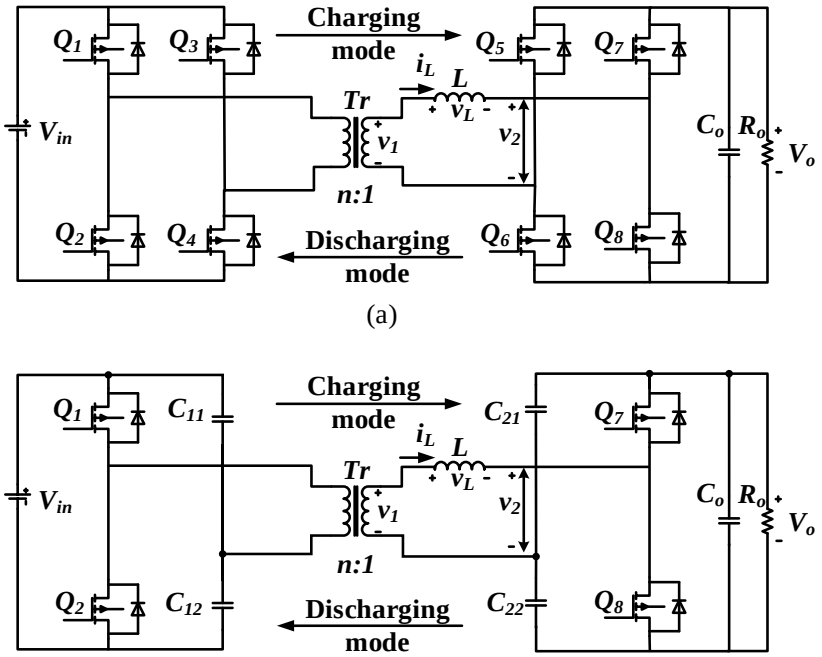


Fig. 3-8 Bidirectional (a) FBDAB and (b) HBDAB resonant converters.

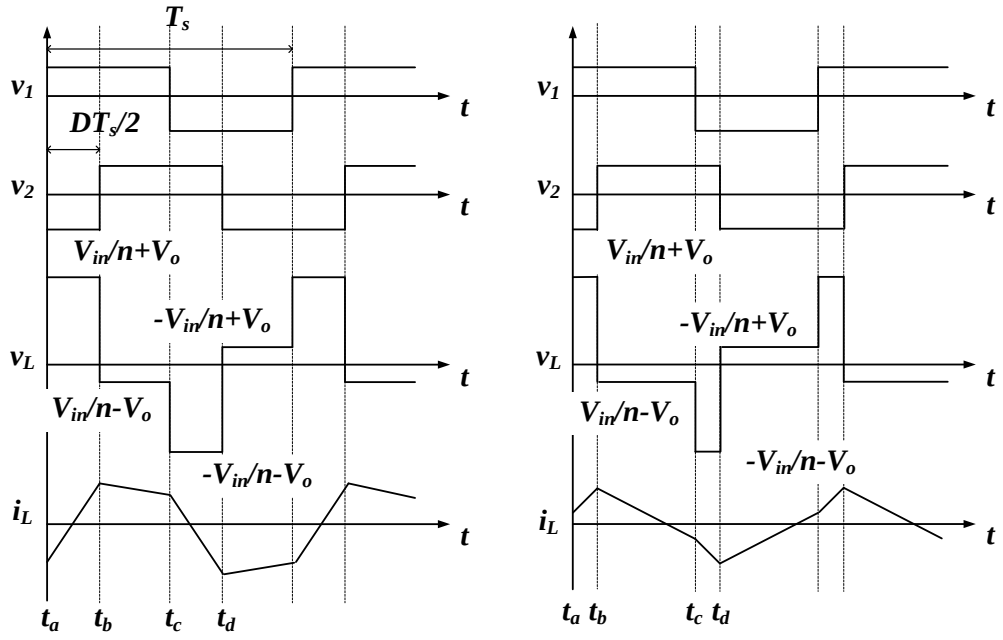


Fig. 3-9 Typical waveforms of an FBDAB converter for $V_{in}/n < V_o$ and $i_L(t_a) < 0$ in (a) heave load condition and (b) light load condition.

B) Gain Analysis

Fig. 3-9(a) shows the inductor voltage and current of the FBDAB circuit. Between t_a and t_b, v_L is $V_{in}/n + V_o$, and the inductor current at t_b is

$$i_L(t_b) = i_L(t_a) + \frac{DT_s}{2L}(V_{in}/n + V_o) \tag{3-17}$$

where, $i_L(t_a)$ is the initial inductor current. Similarly, at t_c, the current is

$$i_L(t_c) = i_L(t_b) + \frac{(1-D)T_s}{2L}(V_{in}/n - V_o) \tag{3-18}$$

At steady-state, the current waveform is symmetric, and $i_L(t_c)$ should be equal to $-i_L(t_a)$. Therefore, the initial current of the inductor can be calculated from (3-17) and (3-18) as

$$i_L(t_a) = \frac{T_s}{4L}[(1-2D)V_o - V_{in}/n] \tag{3-19}$$

The average inductor current in one-half cycle can be derived as

$$\begin{aligned} I_{avg} &= \frac{2}{T_s}\left[\frac{i_L(t_a)+i_L(t_b)}{2}D\frac{T_s}{2} + \frac{i_L(t_b)+i_L(t_c)}{2}(1-D)\frac{T_s}{2}\right] \\ &= \frac{1}{2f_sL}D(1-D)V_o \end{aligned} \tag{3-20}$$

Neglecting the power loss in the circuit, and assuming the load is resistive, the input power P_{in} should be equal to the output power P_{out}, therefore

$$P_{in} = \frac{V_{in}}{n}I_{avg} = \frac{V_o^2}{R_o} = P_{out} \tag{3-21}$$

From (3-20) and (3-21), the gain of the FBDAB converter can be calculated as:

$$G_{FBDAB,G2V} = \frac{V_{out}}{V_{in}} = \frac{1}{n}\cdot\frac{R_o}{2f_sL}D(1-D) \tag{3-22}$$

The output power is derived as

$$P_{FBDAB,G2V} = \frac{V_{in}V_{out}}{2nf_sL}D(1-D) \tag{3-23}$$

and the output current is

$$I_{FBDAB,G2V} = \frac{V_{in}}{2nf_sL}D(1-D) \tag{3-24}$$

Similarly, the gain, output power, and output current of the HBDAB can be derived respectively as follows:

$$G_{HBDAB,G2V} = \frac{1}{n}\cdot\frac{R_o}{8f_sL}D(1-D) \tag{3-25}$$

$$P_{HBDAB,G2V} = \frac{V_{in}V_{out}}{8nf_sL}D(1-D) \tag{3-26}$$

$$I_{HBDAB,G2V} = \frac{V_{in}}{8nf_sL}D(1-D) \tag{3-27}$$

In discharging mode, the gain, output power, and output current of the FBDAB can be derived respectively as follows:

$$G_{FBDAB,V2G} = \frac{1}{n}\cdot\frac{R'_o}{2f_sL}D(1-D) \tag{3-28}$$

$$P_{FBDAB,V2G} = \frac{V_{in}V_{out}}{2nf_sL}D(1-D) \tag{3-29}$$

$$I_{FBDAB,V2G} = \frac{V_{in}}{2nf_sL}D(1-D) \tag{3-30}$$

For the HBDAB circuit,

$$G_{HBDAB,V2G} = \frac{1}{n}\cdot\frac{R'_o}{8f_sL}D(1-D) \tag{3-31}$$

$$P_{HBDAB,V2G} = \frac{V_{in}V_{out}}{8nf_sL}D(1-D) \tag{3-32}$$

$$I_{HBDAB,V2G} = \frac{V_{in}}{8nf_sL} D(1-D) \tag{3-33}$$

C) Soft-switching Region

According to the analysis, to ensure fully ZVS operation, the inductor current is required to be negative at t_a (i.e. $i_L(t_a) \leq 0$), and positive at t_b (i.e. $i_L(t_b) \geq 0$). From (3-17), (3-19) and (3-22), the requirements of phase-shift D can be calculated as follows:

$$\begin{cases} D \geq \dfrac{G_{DAB}-1}{2G_{DAB}} & if\ G_{DAB} \geq 1 \\ D \geq \dfrac{1-G_{DAB}}{2} & if\ G_{DAB} \leq 1 \end{cases} \tag{3-34}$$

Equation (3-34) can be applied to the HBDAB circuit as well. Based on (3-34), the ZVS region of both FBDAB and HBDAB converters is shown in Fig. 3-10. The converters can always operate under ZVS condition when the gain is $1/n$. Otherwise, with lowering the phase-shift, the ZVS region of the converter decreases. Therefore, in light conditions, since the phase-shift must be smaller to maintain the gain, the converters may loss soft-switching, which will cause large switching losses.

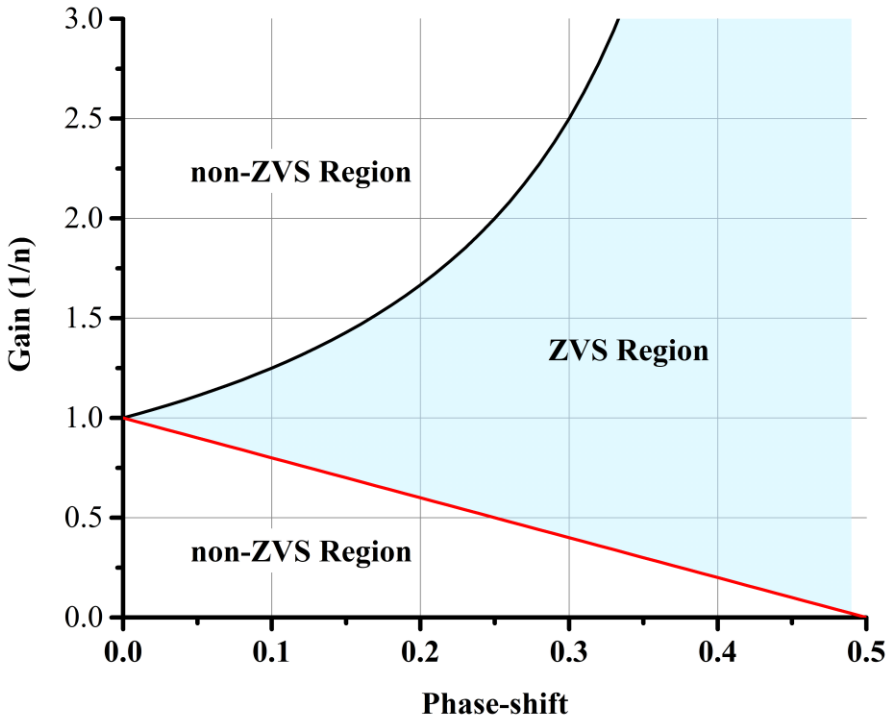


Fig. 3-10 ZVS region of DAB converters.

3.3 Design Methodology

To demonstrate the design methodologies of both CLLC and DAB converters, a design specification must be determined. In charging mode, the input voltages of all four topologies (FBCLLC, HBCLLC, FBDAB, and HBDAB) are 500 V, which is a typical DC-link voltage for an onboard charger. The output voltage range is 200 - 420 V for battery charging. For discharging mode, the input voltage (i.e. battery voltage) range is 350 - 420 V, in order to prevent the battery from deep discharge. The output voltage (i.e. DC-link voltage) is 500 V. In this chapter, the nominal operating frequency for both charging and discharging modes is 170 kHz and power rating for the converters is set to be 1 kW.

3.3.1 Bidirectional CLLC Converters

For the CLLC converters, the transformer turns ratio n is set to be 1.5 in order to step down the input voltage and simplify the control. The G2V gain, therefore, can be designed to be $0.6/n$ - $1.3/n$, and the V2G gain range should be wider than $0.79n$ - $0.96n$. Furthermore, the curve of the two gains should decrease monotonically in the designed zone for linear control. From Fig. 3-6, a larger Q can give a narrower operating frequency range, whereas a smaller Q can guarantee the gain and the monotony of the gain. In this design, $Q = 0.4$ is chosen for full load condition ($R_o = 176\ \Omega$) in charging mode and the resonant frequency f_r is designed to be 170 kHz. For a simplified design, C_1 is equal to C_2', and L_1 is equal to L_2'. The relation between Q and L_m is given in [111]. Large L_m reduces the peak current, which lowers conduction loss, but it will also reduce the gain of the circuit. Furthermore, from (3-15) and (3-16), larger L_m may cause hard switching of the power MOSFETs, due to an insufficient resonant tank current. Therefore, considering the trade-off between gain and conduction loss, L_m is chosen to be four times larger than L_1. Hence, L_1, L_2, L_m, C_1 and C_2, for the FBCLLC circuit can be calculated from (3-5) and (3-6), which will lead to,

$$\begin{cases} L_1 = 120.2\ \mu H \\ L_2 = 53.4\ \mu H \\ C_1 = 7.3\ nF \\ C_2 = 16.4\ nF \\ L_m = 480.8\ \mu H \end{cases} \tag{3-35}$$

Similarly, the parameters for the HBCLLC circuit can be calculated from (3-5) and (3-7) as follows:

$$\begin{cases} L_1 = 30.1\ \mu H \\ L_2 = 13.4\ \mu H \\ C_{11} = C_{12} = 14.6\ nF \\ C_{21} = C_{22} = 32.8\ nF \\ L_m = 120.4\ \mu H \end{cases} \tag{3-36}$$

Fig. 3-11 illustrates the gains of charging and discharging modes for both FBCLLC and HBCLLC circuits with the parameters calculated above, which satisfy the design requirements.

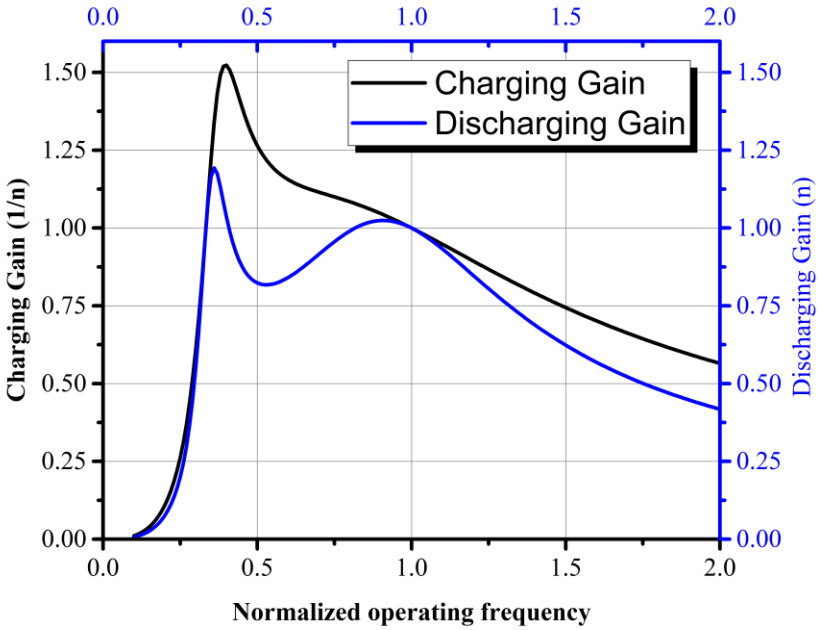


Fig. 3-11 The gains the CLLC circuits in charging and discharging modes.

3.3.2 Bidirectional DAB Converters

Equations (3-22) and (3-28) show that the transformer turns ratio n has the same effect on the gains of DAB circuit in both charging and discharging modes. For example, if $n > 1$, the transformer will help step down the voltage in charging mode, however, in discharging mode, the transformer will still step down the voltage. In this design, the transformer turns ratio n is set to be 1.5 to balance the control pressure in

both power flows and fully use the ZVS region shown in Fig. 3-10. The G2V gain, hence, can be designed to be $0.6/n$ - $1.3/n$, and the V2G gain range should be wider than $1.7/n$ - $2.2/n$. The operating frequency f_s of this circuit is 170 kHz. To reduce the reactive power and make the gain more linear, the maximum phase-shift D_{max} is set to be 0.45 for the worst case. Since the system cannot operate with full power when $V_o = 200$ V for battery charging, the worst case happens in discharging mode with $V_{in} = 350$ V, $V_o = 500$ V, and $P_o = 1$ kW.

For the FBDAB circuit, the inductance L, therefore, can be calculated from (3-29):

$$L_{FBDAB} = \frac{V_{in}V_{out}}{2nf_sP} D_{max}(1 - D_{max}) = 84.9\ \mu H \tag{3-37}$$

Similarly, for the HBDAB circuit, the inductance L can be calculated from (3-32):

$$L_{HBDAB} = \frac{V_{in}V_{out}}{8nf_sP} D_{max}(1 - D_{max}) = 21.2\ \mu H \tag{3-38}$$

From (3-34), the minimum phase-shift can be calculated for each gain. In this design, for both FBDAB and HBDAB converters, the full ZVS regions in both charging and discharging modes are shown in the shadow areas in Fig. 3-12. At light load, the phase-shift is reduced to maintain the gain; however, in this condition, the converters loss full ZVS and only partial ZVS can be achieved.

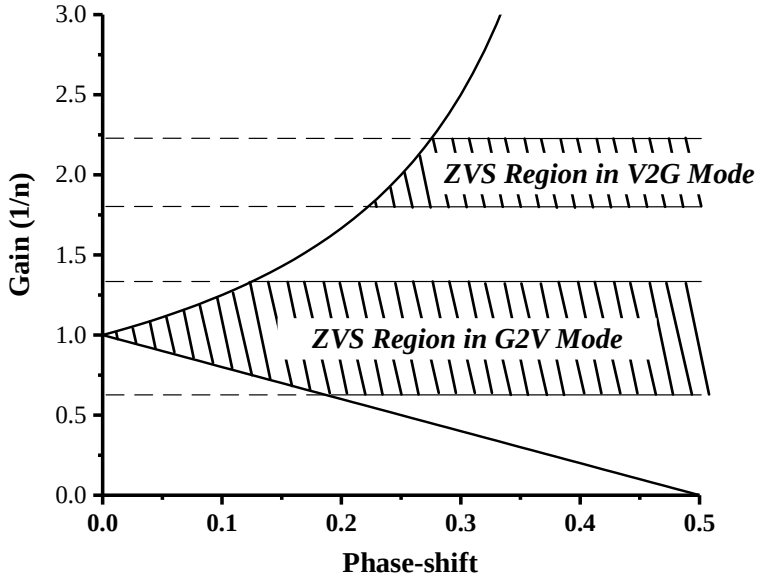


Fig. 3-12 Full ZVS regions in both charging and discharging modes.

3.4 Experimental Results

Fig. 3-13 illustrates the experimental setup for testing the prototypes. The components of the CLLC and DAB circuits are listed in Table 3-1 and Table 3-2, respectively. The switches are SiC power MOSFETs, which have high voltage and current ratings with low output capacitance. A TMS320F28335 DSP-based digital control platform is used to generate the control signal for the circuits. Since the required magnetizing inductance L_m of the transformer in the FBCLLC circuit is higher than that in the HBCLLC circuit, the transformer in the FBCLLC circuit requires more number of turns to ensure higher magnetizing inductance.

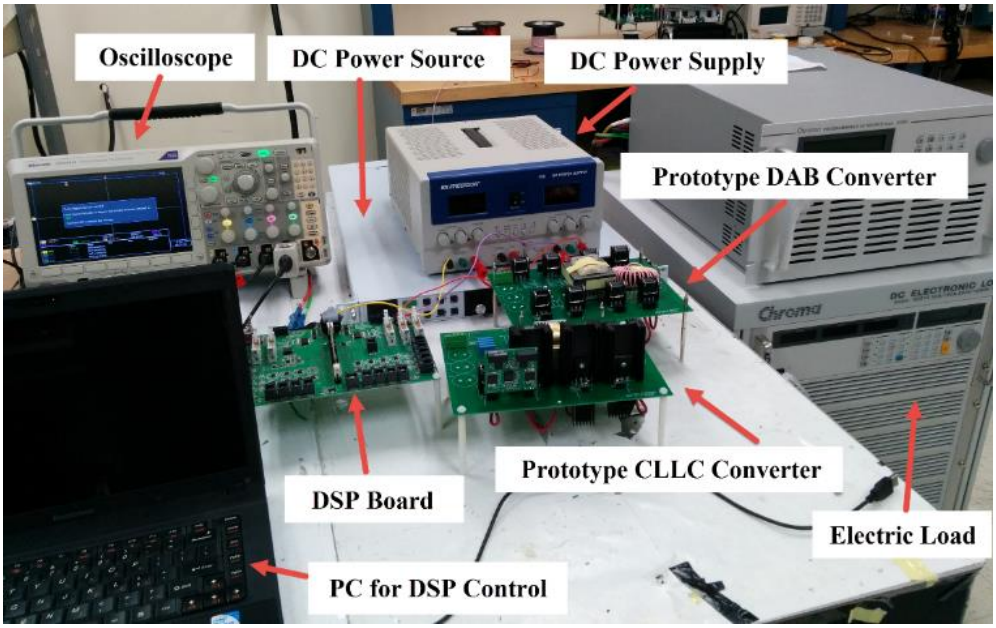


Fig. 3-13 Experimental setup to test the prototypes.

Table 3-1 The components of the CLLC converters

FBCLLC		HBCLLC	
Component	Product/Value	Component	Product/Value
S_1- S_8	C2M0080120D	S_1, S_2, S_7, S_8	C2M0080120D
n	18:12	n	12:8
L_m	522 μH	L_m	131 μH
L_1	131 μH	L_1	32 μH
L_2	60 μH	L_2	15 μH
C_1	7.8 nF	C_{11}, C_{12}	14.2 nF
C_2	17.0 nF	C_{21}, C_{22}	33.0 nF

Table 3-2 The components of the DAB converters

FBDAB		HBDAB	
Component	Product/Value	Component	Product/Value
S_1- S_8	C2M0080120D	S_1, S_2, S_7, S_8	C2M0080120D
n	12:8	n	12:8
L	90 μH	L	22 μH
		C_{11}, C_{12}, C_{21}, C_{22}	30 μF

Fig. 3-14 shows the four prototypes. Since the four converters have similar topologies and for simplicity as well as rapid prototyping, the converters are tested based on one general PCB platform. The film capacitors in CLLC converters are connected in parallel to reduce ESR. Other two bridge capacitors are connected on the bottom of the HBDAB board.

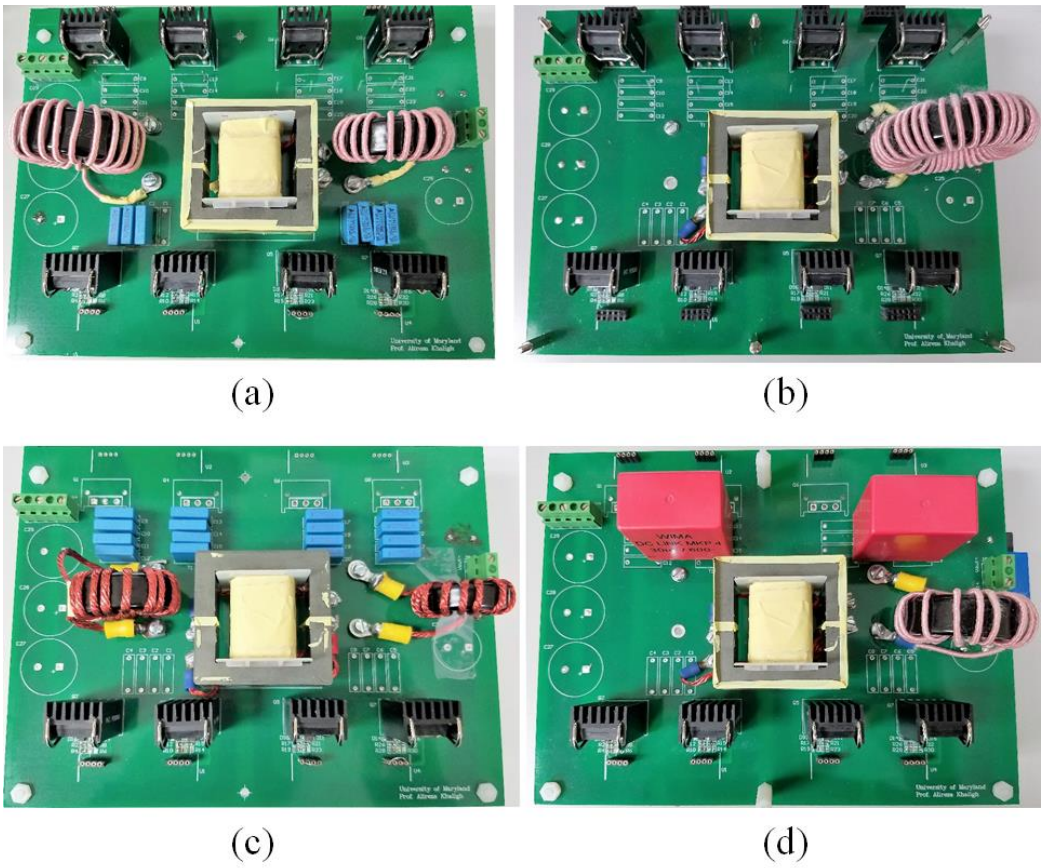
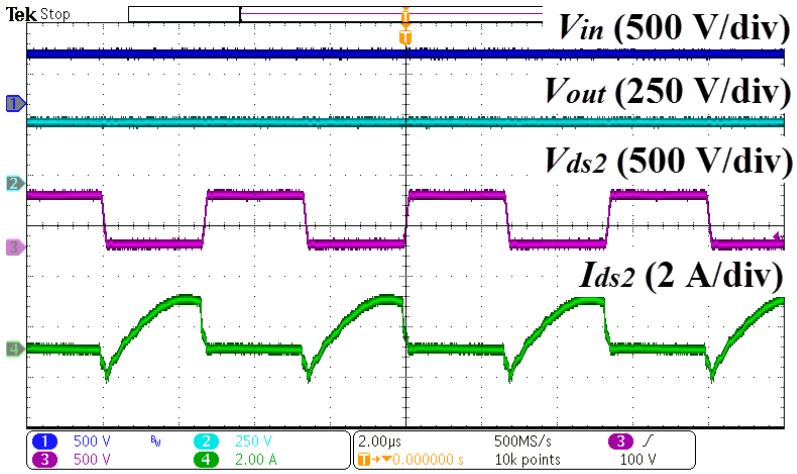


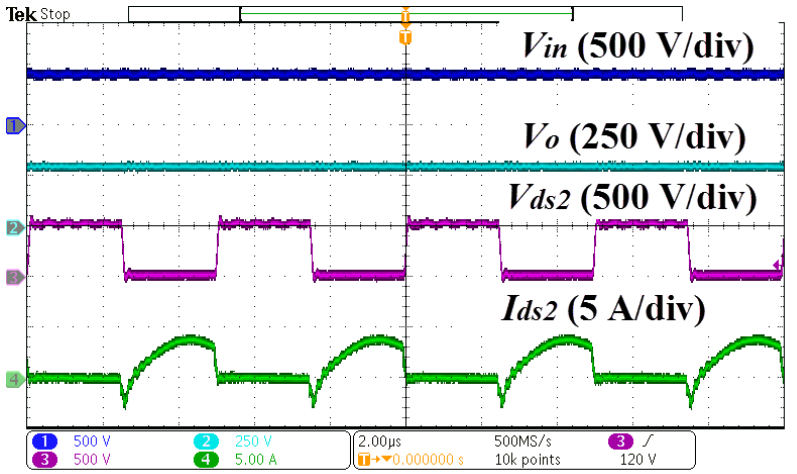
Fig. 3-14 Different DC-DC converter prototypes: (a) FBCLLC, (b) FBDAB, (c) HBCLLC, (d) HBDAB.

Fig. 3-15(a) and (b) illustrate the experimental waveforms of the FBCLLC and the HBCLLC circuits in charging mode. The load is 800 W, $V_o = 300$ V and $f_s = 200$ kHz. It is clear that, for each of the circuits, the switches turn on with ZVS. The circuits

have similar experimental results in discharging mode since the structures of the circuits are symmetrical.



(a)

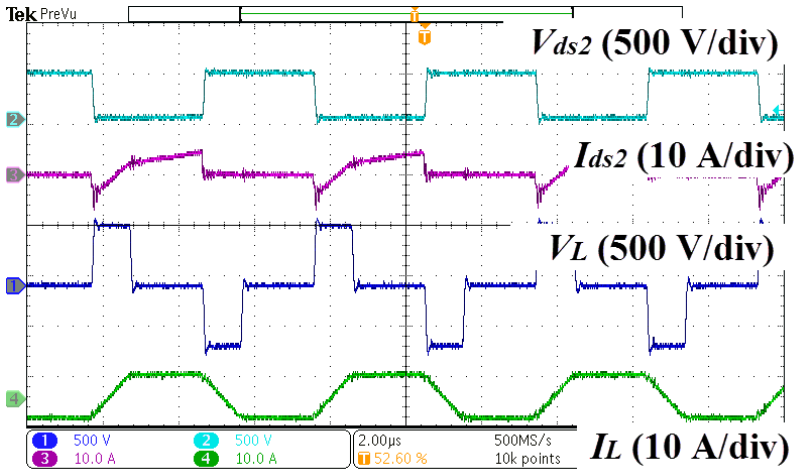


(b)

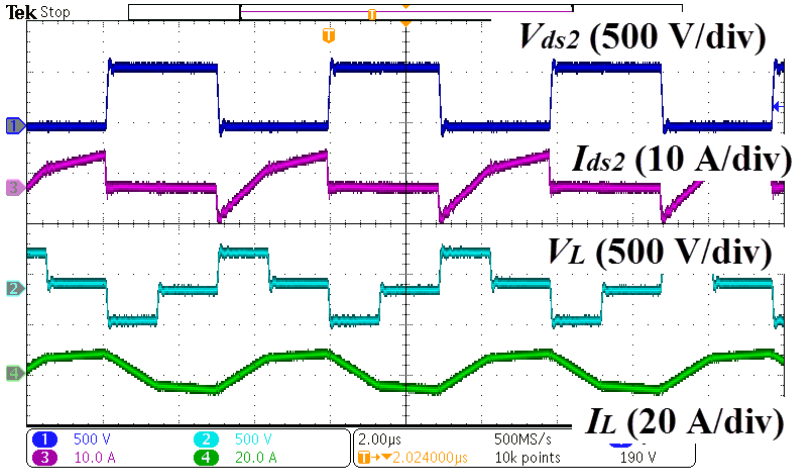
Fig. 3-15 Experimental waveforms of (a) the FBCLLC circuit and (b) the HBCLLC circuit at *load* = 800 W, V_o = 400 V, and f_s = 200 kHz.

Fig. 3-16(a) and (b) show the FBDAB and the HBDAB circuits experimental waveforms in charging mode at phase-shift $D = 0.4$, respectively. The load is 800 W, $V_o = 300$ V and $f_s = 170$ kHz. In this case, $V_o < V_{in}/n$. The waveforms show that the

switches turn on with ZVS. Similar experimental results are obtained in discharging mode.



(a)

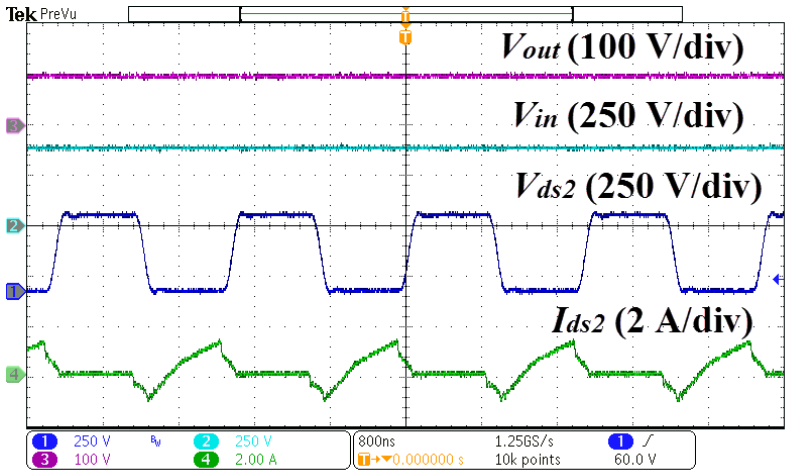


(b)

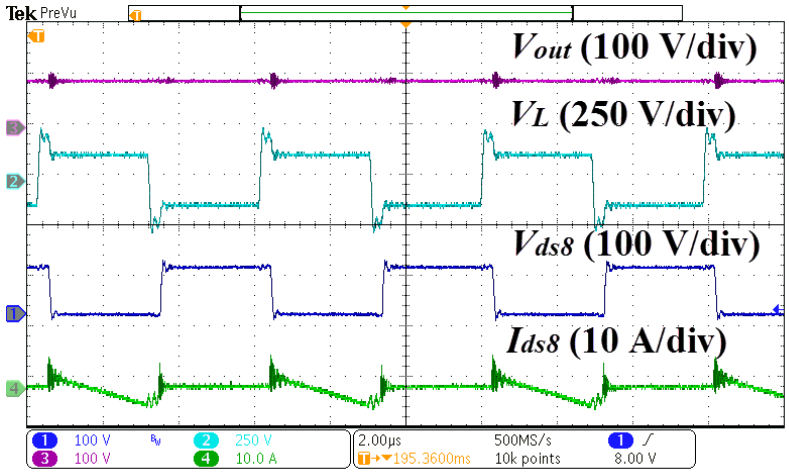
Fig. 3-16 Experimental waveforms of (a) the FBDAB circuit and (b) the HBDAB circuit at *load* = 800 W, V_o = 300 V, f_s = 170 kHz, and D = 0.4.

Fig. 3-17 shows an example of light load condition. The HBCLLC and HBDAB converters operate at 100 V output voltage and 50 W load condition. Since the CLLC converter is controlled through frequency modulation and the DAB converter is

controlled through phase-shift modulation, the operating frequency is 500 kHz for HBCLLC converter and remains 170 kHz for the HBDAB converter. The phase-shift *D* of the HBCLLC converter is set to be 0.1 for this light load condition. It is clear that the switch of the HBCLLC converter still operates with ZVS, whereas the secondary side switch of the HBDAB converter loses ZVS. The experimental results verify the previous analysis.



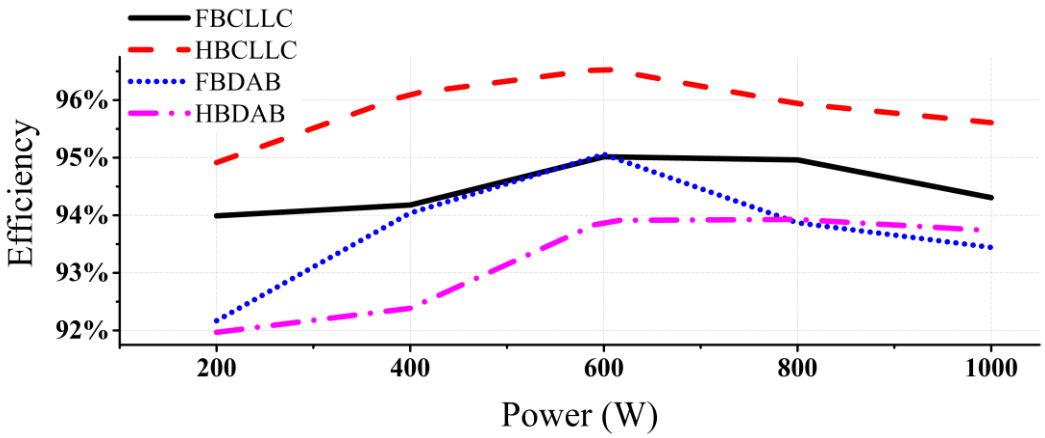
(a)



(b)

Fig. 3-17 Experimental waveforms of (a) the HBCLLC circuit and (b) the HBDAB circuit at *load* = 50 W, and V_o = 100 V.

Fig. 3-18(a) and (b) show the efficiencies of the four circuits in charging and discharging modes, respectively. The output voltage is 300 V for charging mode and 500 V for discharging mode.



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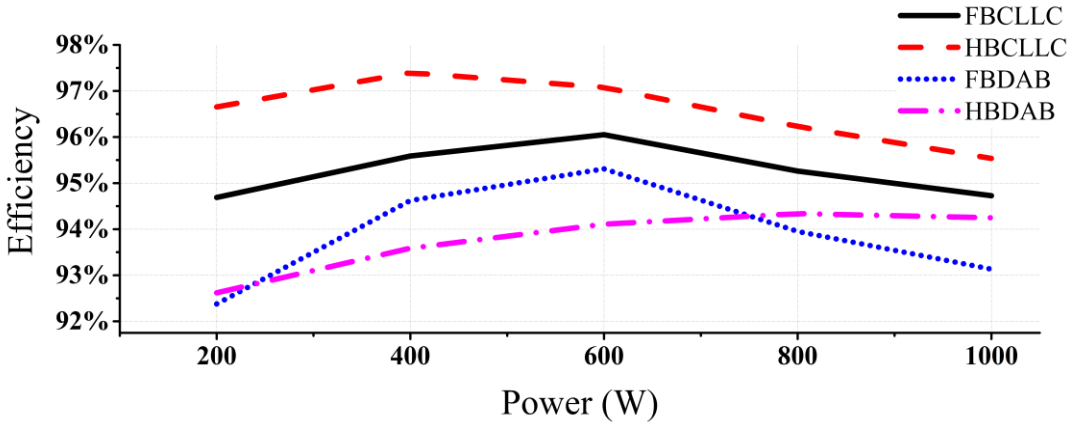
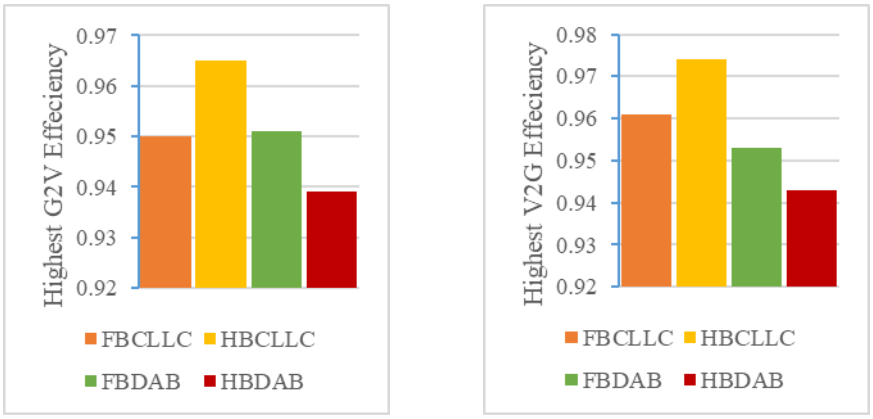


(b)

Fig. 3-18 Measured efficiencies of the four circuits in (a) charging and (b) discharging modes.

3.5 Experiment Results Analysis

Base on the analysis and experimental results, summaries of the comparisons are presented in Fig. 3-19 and Table 3-3.



(a)

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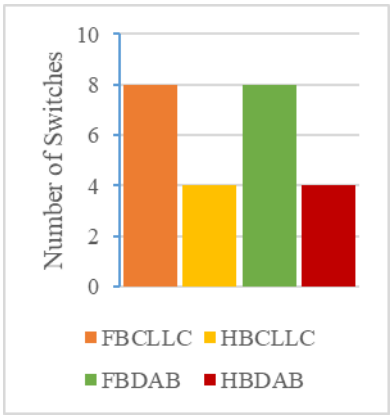

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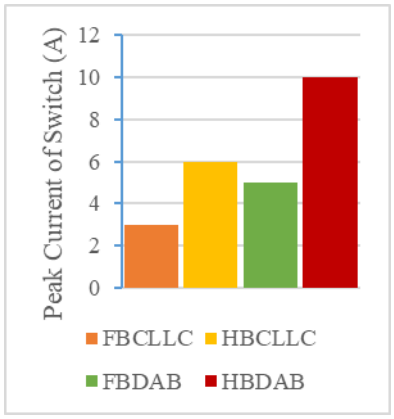

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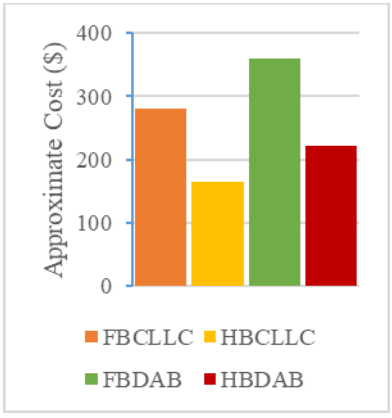

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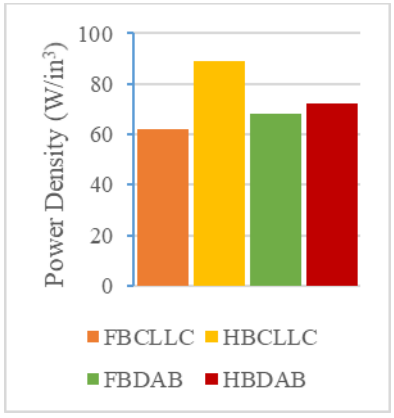


(f)

Fig. 3-19 Comparison for (a) Highest G2V efficiency, (b) Highest V2G efficiency, (c) Number of switches, (d) Peak current of the switch, (d) Approximate cost of each converter, and (f) Power density.

Table 3-3 The comparison of the converters

	FBCLLC	HBCLLC	FBDAB	HBDAB
Highest Efficiency	96.1%	97.4%	95.3%	94.3%
Soft-switching Region	Full load	Full load	Partial load	Partial load
Design Complexity	High	High	Low	Low
Output Filter Requirement	Low	Low	High	High
Component Stress	Low	High	Moderate	High
Power Density	Moderate	High	Moderate	Moderate
Cost	High	Low	High	Low

3.5.1 Efficiency

From the experimental results, all the circuits achieve high efficiency. The highest efficiencies in charging mode are 95.0% and 96.5% for the FBCLLC and the HBCLLC circuits respectively, and 96.1% and 97.4% in discharging mode. The highest efficiencies are achieved when the circuits operate close to the resonant frequency. When the operating frequency is much smaller or larger than the resonant frequency, the circulating loss will increase and reduce the efficiency. For the FBDAB and the HBDAB circuits, the highest efficiencies are 95.1% and 93.9% in charging mode, and 95.3% and 94.3% in discharging mode, respectively. The efficiencies of the CLLC circuits are higher than those of the DAB circuits, since the switches of the DAB circuits loss ZVS at light load conditions, and the SPS control strategy creates relatively large reactive power in the circuits which also reduces the efficiency.

In addition, comparing to the full-bridge structure, the half-bridge structure helps the circuits improves the overall efficiency, due to the reduction of the total number of switches and corresponding driving circuits. An extra benefit of the half-bridge

structure of the resonant converters is that the two capacitors in each leg can automatically reduce flux imbalance for the transformer.

3.5.2 Soft-switching Region

From the analysis in Section II, the soft-switching region of the CLLC circuits is much wider than that of the DAB circuits, especially at light load conditions. With an appropriate design, both FBCLLC and HBCLLC converters can achieve full soft-switching in the entire load range. However, for FBDAB and HBDAB circuits, Fig. 3.10 shows that the converters lose ZVS at light load conditions. Therefore, it is difficult to maintain soft-switching of all the switches for wide load range. Furthermore, for CLLC circuits, lighter loads provide wider soft-switching regions, whereas, for DAB circuits, it is opposite.

3.5.3 Design and Control Complexity

According to the analysis in Section 3.2, if the CLLC circuits operate closed to their resonant frequencies, the gains will be about $1/n$, independent of the loads. Therefore, if the operating frequency can be adjusted at the vicinity of the resonant frequency, both FBCLLC and HBCLLC circuits are perfect for constant output voltage, variable load conditions. However, the gains of the CLLC circuits are non-linear with the loads. Furthermore, depending on the value of Q and particularly at small Q values, the required operating frequency range will be very large. Hence, in the case of a wide output voltage range, the value of Q should be carefully chosen to limit the operating frequency range.

In the case of the DAB circuits, the gains are proportional to the loads, and almost linearly related to the phase-shift when $D \leq 0.45$. Therefore, comparing the DAB converters to the CLLC converters, the design and control complexity for the DAB converters is less.

3.5.4 Component Selection

For the CLLC converter, the output current is sinusoidal, whereas, for the DAB converter, the output current has more high-order-harmonic ripples than that of the CLLC converter. Therefore, an extra current filter may be needed for the DAB circuits.

Comparing the full-bridge and the half-bridge structures, under the same input and output conditions, in the half-bridge structure, both primary side and secondary side currents are twice larger than those in the full-bridge structure. Therefore, the switches, resonant components and transformer of the half-bridge converters are under about twice larger current stress than those of the full-bridge converters.

3.5.5 Power Density

It is clear that, with reducing the number of switches, the half-bridge structure has benefits in terms of size and weight, since the number of corresponding driving circuits and cooling systems can be reduced at the same time. Furthermore, with the same gain, the half-bridge structure requires less inductance than the full-bridge structure. Therefore, the size of the converters with half-bridge structure should be smaller than that with full-bridge structure. Comparing the two half-bridge converters, HBCLLC and HBDAB converters, although the HBCLLC converter requires one more inductor, the bridge capacitances of the HBCLLC converter are much smaller than those of the

HBDAB converter, since they are also used as resonant capacitors. Therefore, in this comparison, the size and weight of the HBCLLC circuit are much less than those of the other circuits, which means the power density of the HBCLLC circuit is the highest. Furthermore, the SiC MOSFETs and their gate drivers cost the most in the converters, thus, reducing the number of switches will reduce the cost of the converters. Therefore, the half-bridge converters cost less than the full-bridge converters.

3.6 Summary

In this chapter, a comprehensive analysis and comparison among the FBCLLC, HBCLLC, FBDAB, and HBDAB converters is conducted. The converters are designed and verified with about 170 kHz operating frequency and 1 kW power rating. All the converters can achieve high efficiency and bidirectional power flow. The topologies, operating principles and design methodologies of the converters are discussed, and the performances of the converters are compared.

Although the current stress on the HBCLLC converter is relatively high, the power density of the HBCLLC converter is the highest and the cost is low. Soft-switching can be achieved in full load range for HBCLLC converter, and in addition, if the input voltage could be adjustable, the HBCLLC converter can be operated at the resonant frequency which is with the highest efficiency. Therefore, for bidirectional, wide load EV charging systems, the CLLC converters are slightly better than DAB converters.

Therefore, the CLLC topology is selected for the 1 MHz and 3.3 kW compact design in the following chapters. Between FBCLLC and HBCLLC topologies, at 1 kW power level, the HBCLLC converter would be a better choice, considering the efficiency, size, and cost. However, at higher power levels such as 3.3 kW, the current

stress on the switches will be much higher for HBCLLC than FBCLLC and the higher resonant current will also result in a much higher switching conduction loss for HBCLLC. Therefore, the full-bridge structure is selected as the final 1-MHz, multi-kW, and bidirectional CLLC converter topology.

Chapter 4 : High-frequency High-power Planar Transformer with Adjustable Leakage Inductance

4.1 Introduction

In a typical switched-mode power supply, magnetic components, DC capacitors, and heatsinks are considered to take more than 80% of the total volume when compared to other components [112]. The trend towards a high-power-density and low-profile converters has been limited by the traditional wire wound magnetic components. In recent years, planar magnetics have gained more popularity due to their unique advantages, especially in high-frequency applications.

Fig. 4-1 illustrates a typical structure of a planar transformer. Generally, a planar transformer uses flat copper foils or PCB traces as its windings to reduce the height requirement of transformer cores. Moreover, with thinner windings, the planar transformers achieve low skin and proximity effects, which brings less AC current losses on the windings [113]. In comparison with a traditional transformer, a planar transformer has the following advantages:

1) Low-profile: The flat windings allow a shorter winding window, which brings a very low-profile transformer design. In other words, with the same core volume, the planar transformer core can have a larger cross-section area with a greater surface area, which brings a lower maximum flux density or a less winding turns number.

2) Light weight: Due to the smaller volume, the total weight of a planar transformer is typically lighter than that of a traditional transformer with the same performance.
3) Manufacturing simplicity: Since the planar transformer uses PCB traces which are repeatable, the performance and parasitic parameters of the planar transformer are more stable and predictable for mass production compared with a traditional wire-wound transformer.
4) Simple thermal management: With a larger surface area of cores and windings, the planar transformer has simpler heat dissipation capability, which results in an excellent thermal management and less heat sink requirements.
5) Reduced skin effect: With thin PCB windings, the skin effect can be minimized, which reduces the winding conduction loss at high frequencies.
6) High efficiency: A planar transformer can achieve over 99% efficiency [114], due to the low core loss and winding loss.

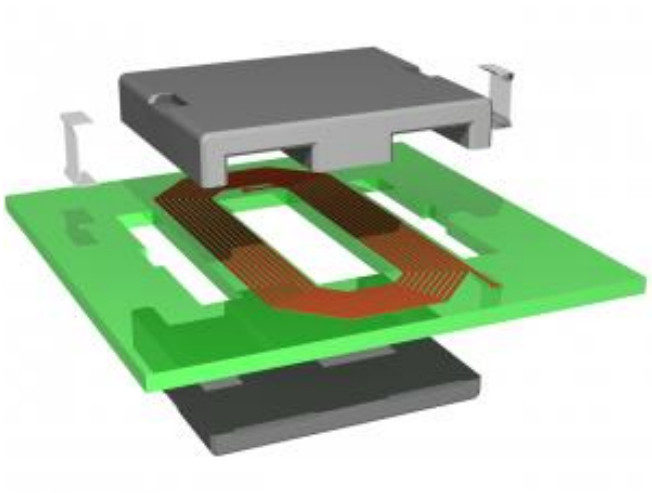


Fig. 4-1 Exploded view of a typical planar transformer [115].

With all of these benefits, the planar transformer is more suitable for a compact high-power converter design. Furthermore, as mentioned in Chapter 2, in order to reduce the size of magnetic components, higher switching frequency operation is the most straightforward approach. The values listed in Table 4-1 shows an example that if the operating frequency of the 1 kW FBCLLC converter (demonstrated in Chapter 3) is increased from 170 kHz to 1 MHz, the required resonant component values will significantly reduce, which results in about 60% resonant tank volume reduction.

Table 4-1 A comparison of passive resonant components in a 1 kW FBCLLC converter operating at 170 kHz and 1 MHz

FBCLLC	Value	
Component	170 kHz	1 MHz
L_m	522 µH	26 µH
L_1	131 µH	6.5 µH
L_1	60 µH	2.9 µH
C_1	7.8 nF	3.9 nF
C_2	17.0 nF	8.7 nF

Fig. 4-2 illustrates two transformer cores for a 3.3 kW converter. It can be seen that with a 1 MHz planar structure, the volume of the transformer can be reduced by at least 50%. Moreover, considering the bobbin size and wire winding of a 170 kHz transformer, the volume can be reduced by over 60%. Therefore, for the final 1 MHz, 3.3 kW FBCLLC converter design, a planar transformer is selected and designed optimally.

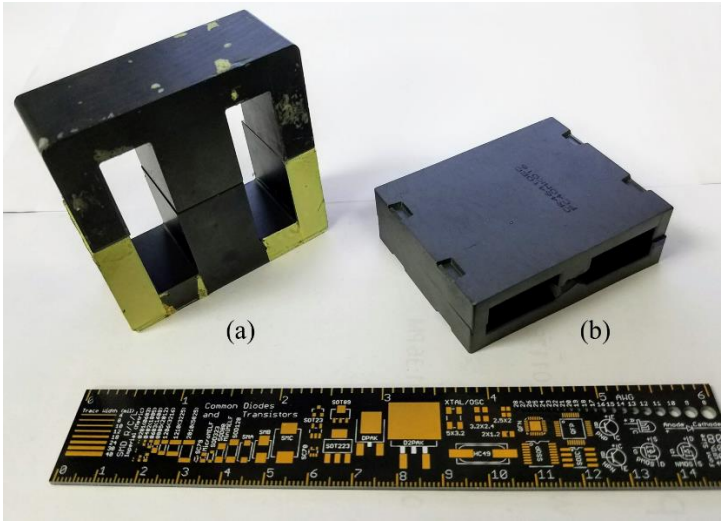


Fig. 4-2 Transformer cores for a 3.3kW DC-DC CLLC converter at (a) 170 kHz and (b) planar-1 MHz operating frequencies.

Considering the structure shown in Fig. 3-1(a), the resonant tank of the converter contains a transformer and two resonant inductors. Winding losses in transformers and inductors increase dramatically with the increase in frequency due to skin and proximity effect. For design and optimization of inductors and transformers, there is a need for an accurate prediction of the winding losses over a wide frequency range for a particular core geometry, which is discussed and analyzed in this work. At higher frequency operation, there is an upper bound for the thickness of the trace in order to avoid the skin effect. Moreover, in case of multilayer winding, the proximity losses strongly dominate over skin effect losses [116]. This is due to the fact that the current in the nearby conductor causes a time-varying field and induces a circulating current inside the conductor. For the MHz-level CLLC converter design in this work, all these effects are mathematically analyzed and validated through finite element-based simulation and experimental results. In this chapter, a detailed magnetic modeling analysis showing the magneto-motive force (MMF) distribution is performed for

optimal winding structure design. In order to further reduce the AC conduction loss and core loss, one objective is to reduce the total PCB trace length and minimize the net core volume. Therefore, the resonant inductor is integrated with the high-frequency planar transformer and is synthesized from the leakage inductance, which is adjustable by changing the air-gap between the windings and core halves. The intricate analyses of flux distribution, as well as fabrication strategy, are presented in this chapter.

4.2 Skin and Proximity Effects

Before designing the planar transformer, a brief introduction to skin and proximity effects is given in this section, since these two effects significantly affect the transformer efficiency at high frequencies.

4.2.1 Skin Effect

When a conductor carries an AC current, there is an alternating magnetic field produced by the AC current in and around the conductor. The magnetic field changes with the variation of the current. The change in the magnetic field creates an electric field which opposes the change in current intensity [117], [118]. This opposing electric field is strongest at the center of the conductor and forces the conducting electrons to the outside of the conductor as shown in Fig. 4-3. The AC current has a tendency to concentrate near the surface of the conductor. This phenomenon in AC current is called the skin effect. Due to this effect, the current is concentrated between the outer surface of the conductor and an inner level call skin depth, δ, as shown in Fig. 4-4.

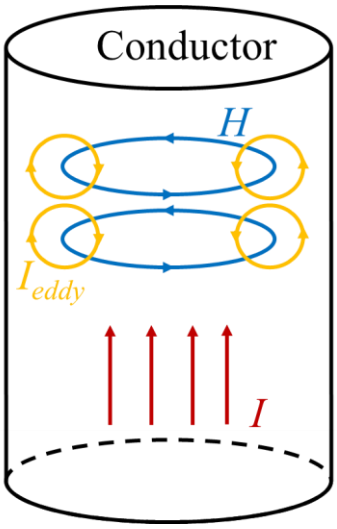


Fig. 4-3 A sketch demonstration of skin effect.

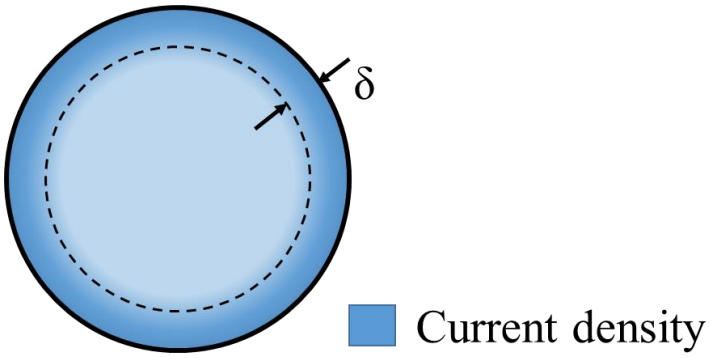


Fig. 4-4 Cross-section of a conductor with a skin depth of δ.

The general formula for calculating the skin depth is:

$$\delta = \sqrt{\frac{2\rho}{2\pi f \mu_0 \mu_r}} \sqrt{\sqrt{1 + (\rho 2\pi f \epsilon_0 \epsilon_r)^2} + \rho 2\pi f \epsilon_0 \epsilon_r} \qquad (4\text{-}1)$$

where,

ρ = resistivity of the conductor;

f = frequency;

μ_0 = permeability of the free space;

μ_r = relative magnetic permeability of the conductor;

ε_0 = permittivity of free space;

ε_r = relative permittivity of the material.

The skin effect depends upon the conductor material, cross-sectional area of the conductor, current frequency, and shape of the conductor. The higher the frequency, the smaller the skin depth becomes, which means the effective cross-section of the conductor reduces at higher frequencies. Consequently, the effective resistance of the conductor increases. For copper wires, the skin depth is only 65 μm at 1 MHz frequency.

4.2.2 Proximity Effect

When two or more conductors carrying AC current are close to each other, the alternating magnetic field, induces eddy currents in adjacent conductors (as shown in Fig. 4-5), affecting the overall distribution of the current flowing through the conductors. Therefore, when the nearby conductors carrying current in the same direction, the current is concentrated at the farthest parts of the conductors. Similarly, the current is distributed at the nearest sides of the conductors, when the conductors carrying current in opposite direction. This phenomenon (illustrated in Fig. 4-6) is call proximity effect.

Due to the proximity effect, the effective cross-section of the conductor is reduced, resulting in an increase in effective resistance. This is another reason that reduces the transformer efficiency at high frequencies. Furthermore, the proximity effect also rises with an increase in the frequency. Therefore, at MHz-level frequencies, the conduction loss caused by the proximity effect becomes considerable.

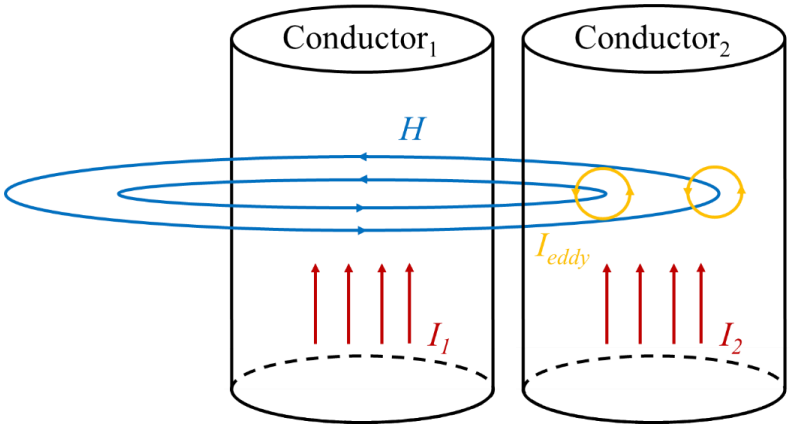


Fig. 4-5 A sketch demonstration of proximity effect.

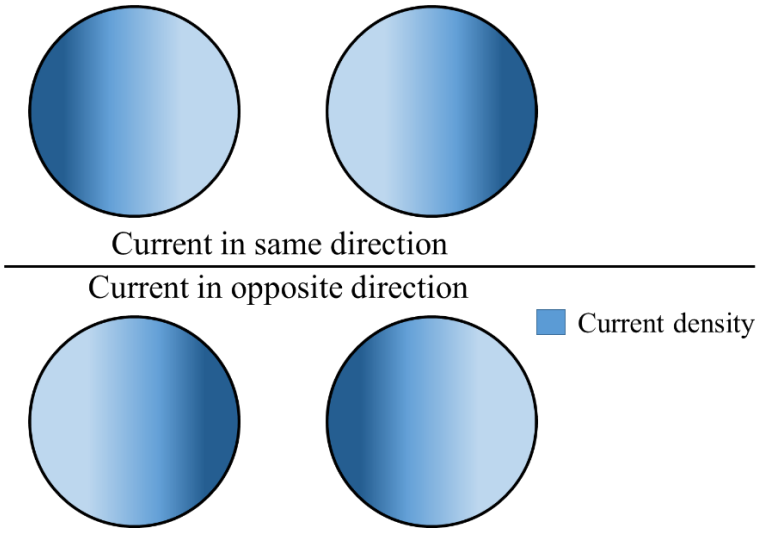


Fig. 4-6 Uneven distributions of current due to proximity effect

With all these considerations, an optimal design methodology of the planar transformer is proposed in this chapter to address the proximity and skin effects.

4.3 Planar Transformer Core Selection

The planar transformer is selected considering the tradeoff between the core size and core loss. To achieve a high-power-density design, the transformer core should be chosen as small as possible, however, small core results in a smaller effective cross-

section area, which increases the core loss. Moreover, a smaller effective cross-section area makes the transformer core easier to be saturated. Therefore, the planar transformer must be determined carefully.

For a MHz-level, 3.3 kW planar transformer, there are not many available cores on the market. CR46410EC planar EE-core from Magnetics with the R material and ER64/13/51 planar ER-core from Ferroxcube with the 3F4 material are two candidates for this design. Both cores can work at 1 MHz at this power rating. The parameters of two cores are listed in Table 4-2 [119], [120], where μ_0 is the permeability of air, μ_r is the relative permeability, A_e, l_e and v_e are the effective cross-section area, path length, and volume of the core, respectively.

Table 4-2 The parameters of the two transformer cores

	μ_0 (H/m)	μ_r	l_e (cm)	A_e (cm^2)	v_e (cm^3)
CR46410EC	$4\pi\times10^{-7}$	2300	8.02	5.16	41.4
ER64/13/51	$4\pi\times10^{-7}$	1760	9.3	5.66	52.6

The core loss of CR46410EC can be calculated through the curve fitting formula provided by Magnetics [121]:

$$P_{core,EE} = af^c B_{peak}^d \tag{4-2}$$

Similarly, the core loss curve fitting equation of ER64/13/51 provided by Ferroxcube [122] is shown as follows:

$$P_{core,ER} = C_m f^x B_{peak}^y \tag{4-3}$$

The values of the parameters in (4-2) and (4-3) for 100 ºC with over 500 kHz frequency conditions are listed in Table 4-3. f is the operating frequency and B_{peak} is the peak flux density with N winding turns of the transformer, which can be calculated using (4-4).

$$B_{peak} = \frac{V_{in}}{4NfA_e} \tag{4-4}$$

Table 4-3 Parameters for curve fitting formulas

CR46410EC					
a	c	d	f	B_{peak}	$P_{core,EE}$
0.014	1.84	2.2	in kHz	in kG	in mW/cm^3
ER64/13/51					
C_m	x	y	f	B_{peak}	$P_{core,ER}$
0.0012	1.75	2.9	in Hz	in T	in mW/cm^3

4.4 Adjustable Leakage Inductance

As one of the most important components in a CLLC converter, the resonant inductance must be well determined with a precise value. On the other hand, the inductor takes a considerable volume of the converter. Furthermore, AC winding loss caused by the skin and proximity effects become a dominating factor at high frequencies leading to significantly reduced system efficiency. In order to decrease the total winding losses from magnetic components and reduce the volume of the converter, it becomes a necessity to integrate the resonant inductors L_1 and L_2 (as shown in Fig. 3-1(a)) with the transformer leakage inductance. In other words, the leakage inductance is acting as the resonant inductor. Fig. 4-7 illustrates the structure of the proposed stacked planar transformer providing accurate control of leakage inductance.

The magnetizing inductance of the transformer can be adjusted by changing l_g, the air gap between two cores. The primary and secondary side windings are embedded separately on individual boards providing an extra degree of freedom l_b, the distance between the two windings. Hence, the proposed transformer can realize precise leakage inductance values by controlling l_b, which is an important design criterion for resonant converters.

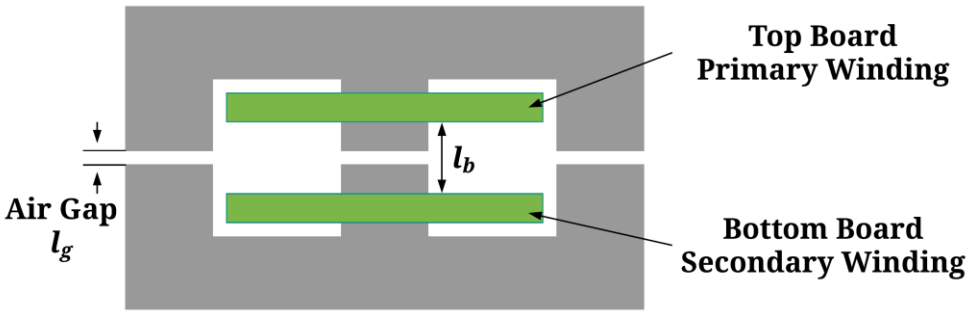


Fig. 4-7 Structure of the proposed planar transformer with adjustable leakage inductance.

4.5 Loss Modeling of Planar Transformer and Optimal Design

The PCB winding structure plays a vital role in reducing the AC losses. For high-frequency planar transformers, the skin and proximity effects are the key design constraints. The effective skin depth of copper at 1 MHz is only 65 µm, hence a 2-oz (69 µm) PCB trace thickness is selected for this design.

Fig. 4-8 shows the comparison between current distributions of a planar transformer with 2-oz PCB trace and operating at 65 kHz and 1 MHz, respectively. It can be clearly perceived that at 1 MHz frequency, the significant negative current induced by the proximity effect flows through the trace, leading to a substantial increase in the AC loss.

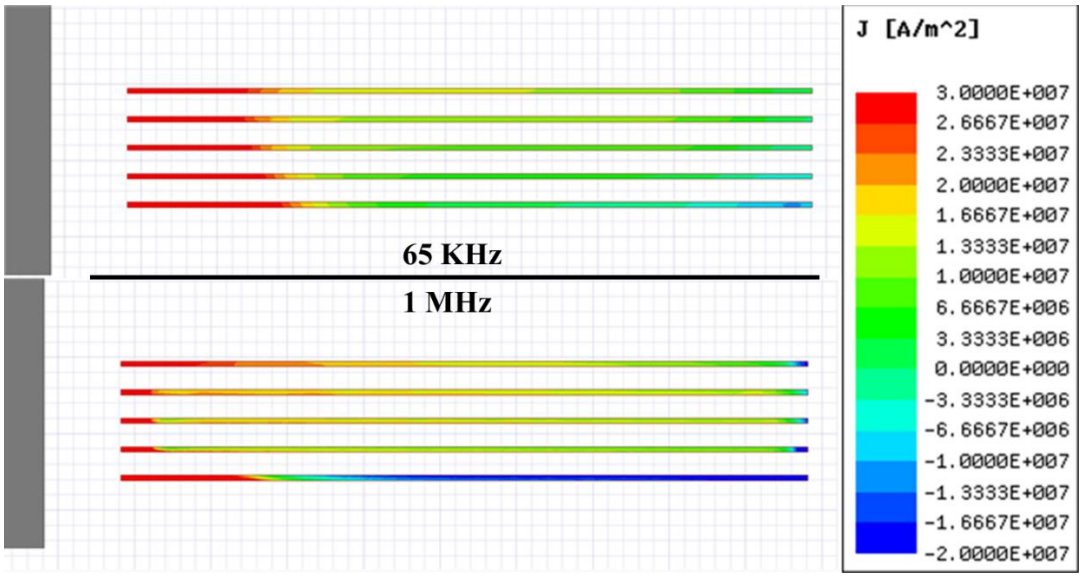


Fig. 4-8 Winding current distributions with 12 A_{rms} current flow, 2-oz trace operating at 65 kHz and 1 MHz frequencies, respectively.

To optimize the design of high-frequency transformer, an improved Dowell's equation [123] is used to calculate the effective winding resistance:

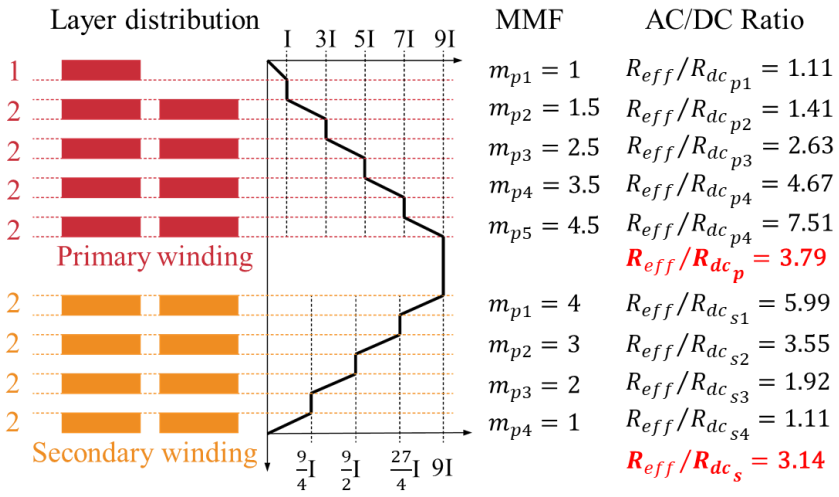
$$\left(\frac{R_{eff}}{R_{dc}}\right)_l = \frac{x}{2}\left[\frac{sinh(x)+sin(x)}{cosh(x)-cos(x)} + (2m_l-1)^2\frac{sinh(x)-sin(x)}{cosh(x)+cos(x)}\right] \tag{4-5}$$

$$\begin{cases} x = \dfrac{h}{\delta} \\ m_l = \left|\dfrac{MMF(l)}{MMF(l)-MMF(l-1)}\right| \end{cases} \tag{4-6}$$

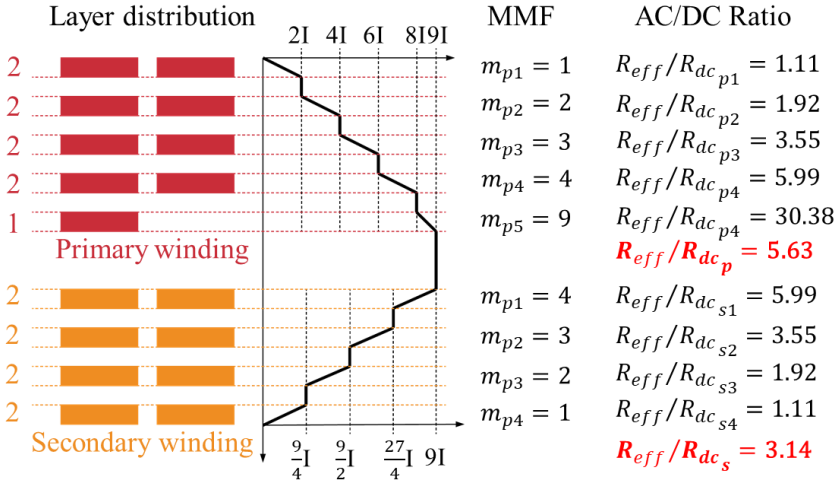
where $(R_{eff}/R_{dc})_l$ is the effective resistance to DC resistance ratio on the l^{th} layer, h is the PCB trace thickness, δ is the skin depth in the conductor, and $MMF(l)$ is the magnetomotive force of the windings on layer l. The first term in (4-5) characterizes the skin effect and the second term signifies the proximity effect.

Fig. 4-9 illustrates two examples of transformer winding structures, having 9 turns on primary-side and 8 turns on secondary-side. The value of m_l and resistance ratio $(R_{eff}/R_{dc})_l$ are calculated using (4-5) and shown in the figures. It can be clearly inferred

that the 1 2 2 2 2 winding structure on the primary side (Fig. 4(a)) has less resistance ratio of 3.79, leading to a lower AC loss at high power levels.



(a)



(b)

Fig. 4-9 Effective to DC resistance ratios for different 9:8 winding structures.

Another example of an 8:7 winding structure is shown in Fig. 4-10. Comparing to Fig. 4-9, less winding layers brings a lower effective to DC resistance ratio, resulting in a lower winding conduction loss as well.

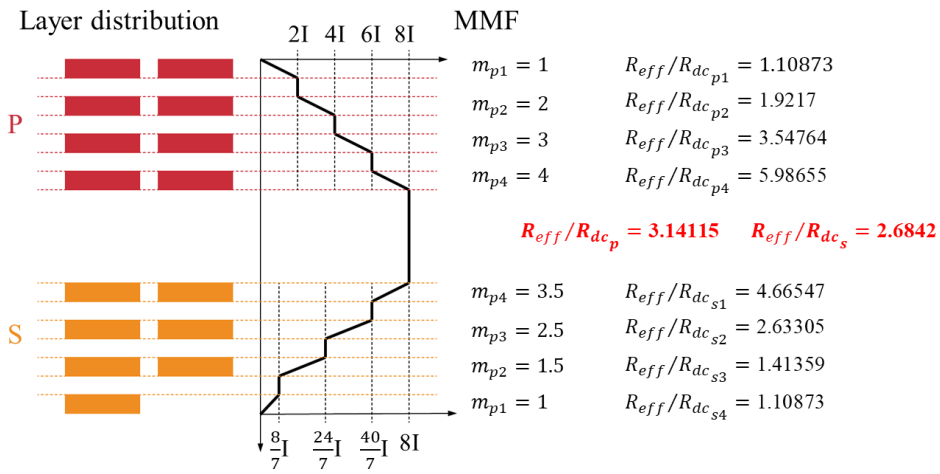


Fig. 4-10 Effective to DC resistance ratio for an 8:7 winding structure.

The DC resistance of the transformer can be calculated as follows:

$$R_{dc} = \frac{\rho_{cu} L}{wt} \tag{4-7}$$

where, ρ_{cu}=1.68×10^{-8} Ω·m is the resistivity of copper, and L is the winding length. From (4-5) and (4-7), the total winding loss can be computed as below:

$$P_{winding} = I_{rms}^2 R_{eff} \tag{4-8}$$

Thus, from (4-2), (4-3), and (4-8), the total loss of the transformer can be determined as follows:

$$P_{trans} = P_{core} + P_{winding} \tag{4-9}$$

Substituting parameters from Table 4-2, power losses for different winding structures and different cores are calculated. The operating conditions are 450 V input, 400 V output, 3.3 kW output power, and 1 MHz operating frequency for the calculations. These are the nominal working conditions of the proposed FBCLLC converter. The results are compiled in Table 4-4 and Table 4-5. Fig. 4-11 illustrates sketched winding areas of the ER and EE cores.

Table 4-4 Calculated power losses for different cores and winding structures (Part I).

Case	Core	*n*	Pri-winding	Sec-winding	Trace Thickness	R_{eff}/R_{DCp}	R_{eff}/R_{DCs}
1	CR46410EC	9:8	1 2 2 2 2	2 2 2 2	2 oz	3.79	3.14
2	CR46410EC	9:8	1 2 2 2 2	2 2 2 2	3 oz	12.77	10.04
3	CR46410EC	9:8	2 2 2 2 1	2 2 2 2	2 oz	5.63	3.14
4	CR46410EC	8:7	2 2 2 2	1 2 2 2	2 oz	3.14	7.08
5	CR46410EC	10:9	2 2 2 2 2	2 2 2 2 1	2 oz	4.36	3.79
6	ER64/13/51	8:7	2 2 2 2	2 2 2 1	3 oz	10.04	8.11
7	ER64/13/51	8:7	2 2 2 2	2 2 2 1	2 oz	3.14	2.68
8	ER64/13/51	8:7	2 2 2 2	1 2 2 2	2 oz	3.14	4.15
9	ER64/13/51	8:7	|2 2 2 2|	|2 2 2 1|	2 oz	9.35	7.52
10	ER64/13/51	10:9	2 2 2 2 2	2 2 1 2 2	2 oz	4.36	4.32
11	ER64/13/51	10:9	2 2 2 2 2	2 2 2 2 1	2 oz	4.36	3.78
12	ER64/13/51	9:8	1 2 2 2 2	2 2 2 2	2 oz	3.78	3.14
13	ER51/10/38	9:8	1 2 2 2 2	2 2 2 2	2 oz	3.78	3.14

Table 4-5 Calculated power losses for different cores and winding structures (Part II).

Case	L_p (cm)	L_s (cm)	$R_{eff,p}$ (Ω)	$R_{eff,s}$ (Ω)	$P_{winding}$ (W)	P_{core} (W)	P_{total} (W)
1	184.0	167.2	0.17	0.13	21.19	8.48	29.67
2	184.0	167.2	0.38	0.27	46.52	8.48	55.00
3	184.0	167.2	0.25	0.13	26.86	8.48	35.34
4	167.2	142.2	0.13	0.25	27.06	10.99	38.05
5	209.0	184.0	0.22	0.17	27.60	6.73	34.33
6	96.5	82.5	0.26	0.18	35.95	27.05	63.00
7	96.5	82.5	0.12	0.09	17.33	27.05	44.38
8	96.5	82.5	0.12	0.14	21.95	27.05	49.00
9	96.5	82.5	0.18	0.13	25.06	27.05	52.11

10	120.6	106.6	0.21	0.19	32.01	14.16	46.18
11	120.6	106.6	0.21	0.16	29.93	14.16	44.10
12	106.6	96.5	0.16	0.12	23.01	19.23	42.23
13	83.3	75.4	0.17	0.13	24.03	37.70	61.73

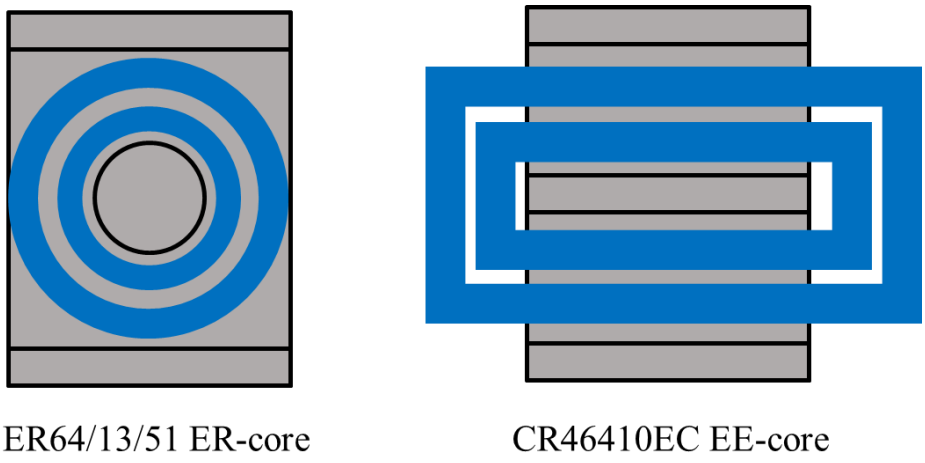


Fig. 4-11 Sketched winding areas of ER and EE cores

In the tables, Case 1 to Case 5 show the results of CR46410EC EE-core, while Case 6 to Case 13 show the results of ER64/13/51 ER-core. It can be seen from the figure that, with the same core dimensions, the ER core has higher winding area efficiency, which means the winding area of the ER core is smaller than that of the EE core. However, due to the relatively narrower trace width, the winding loss of the ER core is slightly higher than that of the EE core. More importantly, due to the different core materials, with same winding structure, the EE core from Magnetics has lower core loss than the ER core from Ferroxcube has.

In comparison with Case 1, Case 2 has 3-oz PCB trace thickness which brings a lower DC resistance, however, the thicker trace results in a much higher effective to DC resistance ratio due to the proximity effect, which leads to a higher winding loss.

With the same 2-oz thickness as Case 1, Case 3 has a different winding structure on the primary side, which also results in a higher winding loss due to the proximity effect (can be seen in Fig. 4-9 as well).

Similarly, for Case 6-8, different trace thicknesses or winding structures give different winding losses due to the proximity effect.

From Case 1, Case 4 and Case 5, it can be inferred that a larger number of turns brings a lower core loss, but a higher winding loss, vice versa. Therefore, the number of transformer turns must be determined with the tradeoff between the core and winding losses.

Comparing with Case 7, Case 9 has a paralleled winding structure, which means two 2-oz traces are connected in parallel to represent one trace. The benefit of this winding structure is increasing the effective cross-section area of the windings without increasing the skin effect. This results in a much lower DC resistance. However, with this winding structure, the proximity effect becomes much worse, leading to a higher effective to DC resistant ratio. Consequently, the total winding loss is still higher than that of Case 7.

In Case 10-12, power losses for different numbers of turns are calculated to find out the best value. Results for a smaller ER core is also calculated and provided in Case 13. With this core, neither the winding loss nor the core loss reduces, since the trace width is narrower and the effective cross-section area of the core is smaller compared with the core in Case 12.

With all of the calculated results, considering the balance between winding and core losses, the transformer design presented in Case 1 is the optimal design for the proposed system due to the lowest total power loss under the given condition.

The calculated results shown in Table 4-4 and Table 4-5 are based on a 2 or 3 oz trace thickness. Actually, a lower trance thickness can bring an even lower total transformer loss. Fig. 4-12 shows the calculated total transformer losses with different PCB trace thicknesses. The transformer core, number of turns, and winding structure are the same as those of Case 1. It can be seen that the minimum total transformer power loss is achieved with about 1 oz PCB trace thickness. However, considering the other parts of the PCB conducting DC current, a 2 oz trace thickness is necessary for a low DC conduction loss at high power levels.

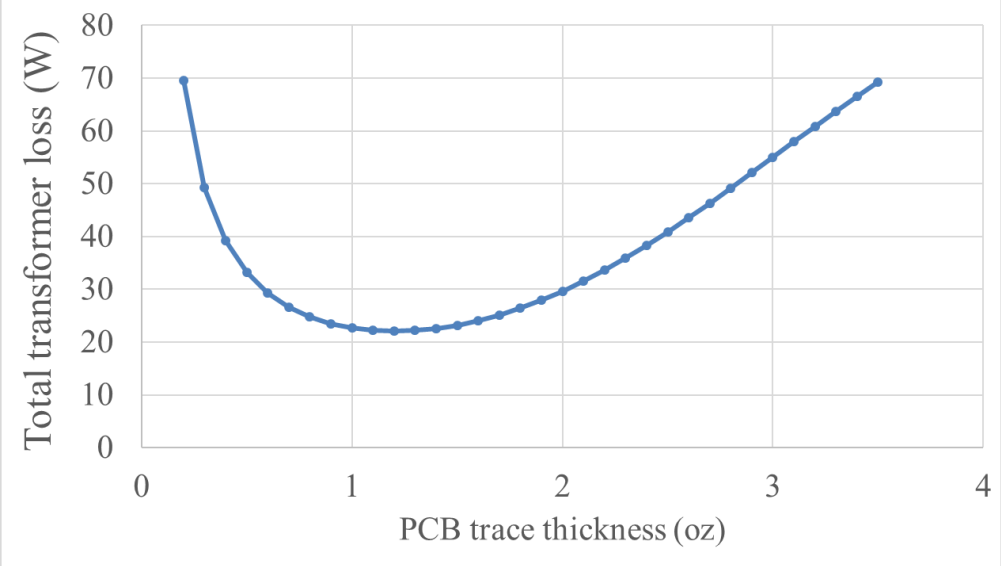


Fig. 4-12 Total transformer loss vs. different PCB trace thickness.

After a comprehensive comparison, the transformer design using CR46410EC EE-core with 1 2 2 2 2; 2 2 2 2 winding structure and 2 oz PCB trace thickness is selected as the optimal design for the proposed the CLLC converter.

The proposed CLLC converter is operating with a variable input DC link voltage of 400-450 V, generating 250-420 V (400 V nominal) output voltage with a power rating of 3.3 kW. The calculated parameters of the resonant tank are listed in Table 4-6, where n is the turns ratio, L_1 and L_2 are the leakage inductances, L_m is the magnetizing inductance and C_1 and C_2 are the resonant capacitances.

Table 4-6 Calculated parameters of the resonant tank

n	C_1 (nF)	C_2 (nF)	L_1 (μH)	L_2 (μH)	L_m (μH)
9:8	7.26	9.18	3.49	2.76	21

The structure of the proposed integrated planar transformer provides two degrees of freedom, l_g and l_b. The magnetizing inductance is very sensitive to the air gap l_g (shown in Fig. 4-7), but not to the board-to-board gap l_b. The leakage inductance, however, is sensitive to both l_g and l_b. In order to accurately design the transformer parameters, air gap has to be determined first. The required length of the air gap l_g is computed as below:

$$l_g = (\frac{N^2}{L_m} - \frac{l_e}{\mu_0 \mu_r A_e})\mu_0 A_e \tag{4-10}$$

where N is the primary side winding turns.

From Table 4-2, Table 4-6, and using (4-10), an air gap of 2.5 mm is calculated to generate an L_m of 21 μH. After designing the magnetizing inductance, the leakage inductance can be adjusted by tuning l_b. As shown in Fig. 4-7, l_b is limited by the core leg length, air gap l_g, and the board thickness. In this case, the l_b can be adjusted from 0 to 9.7 mm, which gives 0.4 to 12 μH leakage inductance. A 4 mm board to board gap

l_b is determined as the final value to generate the required leakage inductance. The final design of the planar transformer with adjustable leakage inductance is illustrated in Fig. 4-13.

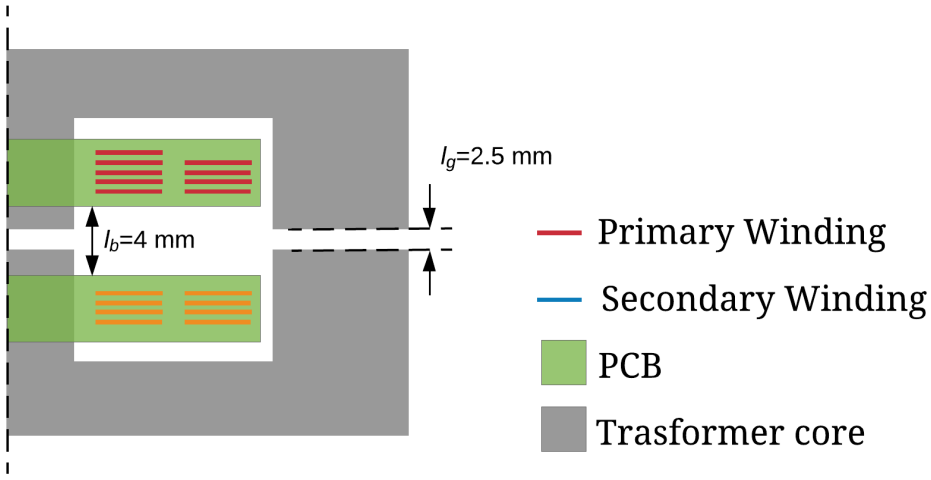


Fig. 4-13 Half-side view of the proposed planar transformer structure.

A finite element analysis (FEA) model is built using ANSYS Maxwell (shown in Fig. 4-14) to simulate the proposed planar transformer. The flux density in the cores is shown in Fig. 4-15. The flux density has a peak value of 55 mT, which is much lower than the saturation level (470 mT) of the selected core material. The magnetizing inductance obtained from the simulation is 20.47 μH, which is a close match to the analytical calculation. The current density distribution is illustrated in Fig. 4-16. It can be seen that the current is distributed unevenly, which is partially caused by the geometry of the winding and partially caused by the proximity effect. Fig. 4-17 displays the conduction loss of the windings. From the results shown in the figure and the values listed in Table 4-4 and Table 4-5, the winding loss is calculated as about 16 W, which matches the theoretical calculations.

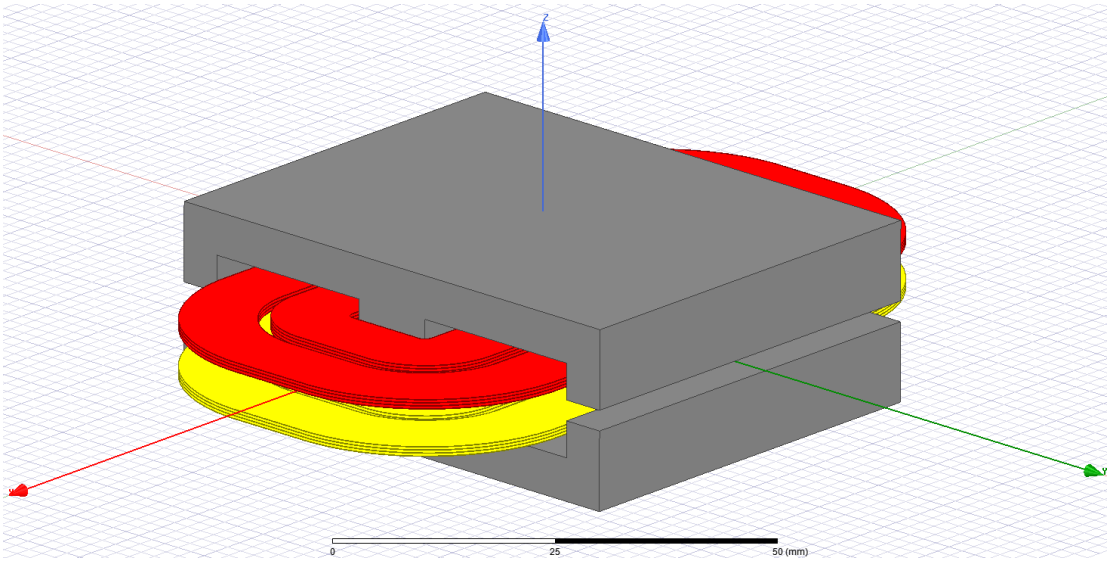


Fig. 4-14 FEA model of the proposed planar transformer.

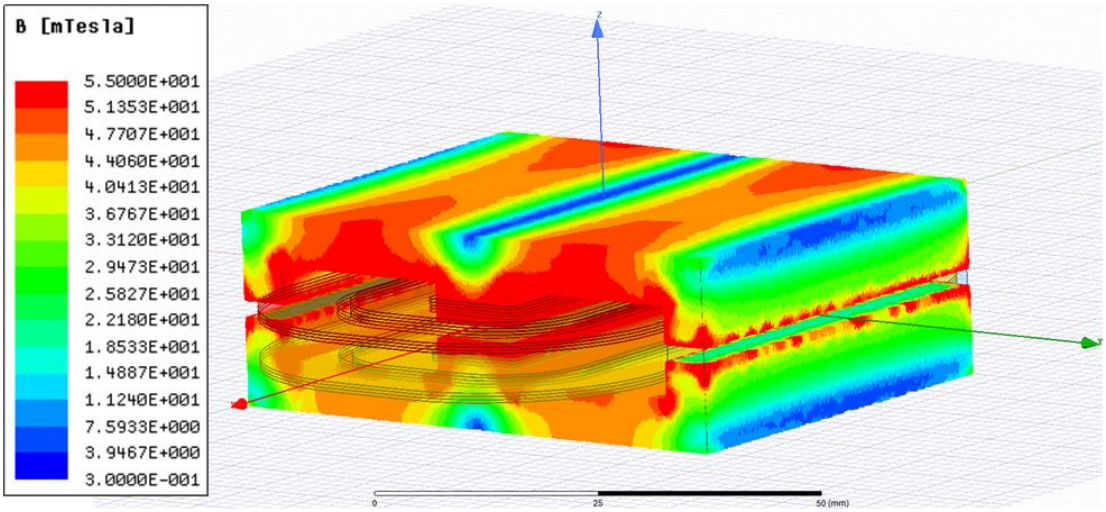


Fig. 4-15 Flux density distribution of the proposed planar transformer.

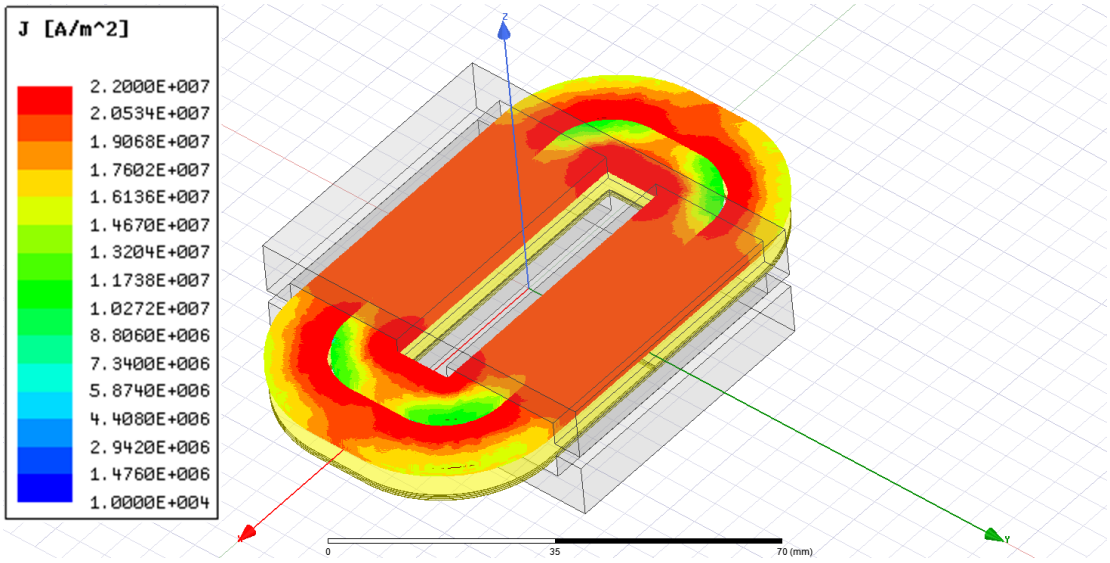


Fig. 4-16 Current density distribution of the proposed planar transformer.

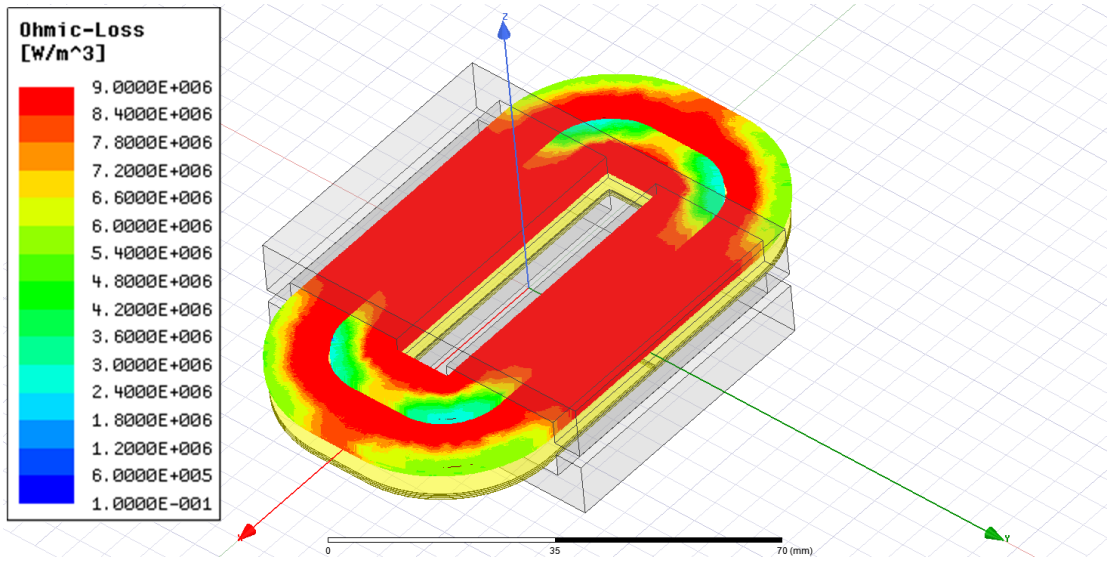


Fig. 4-17 Winding conduction loss of the proposed planar transformer.

4.6 Summary

In this chapter, the structure and advantages of a planar transformer are reviewed. The planar transformer utilizes PCB winding structure to achieve a low profile. With the PCB winding, the planar transformer achieves an excellent capability of

reproduction and stability. Moreover, the planar transformer can partially immune the skin effect at high frequencies, due to the thin PCB windings, which results in a higher efficiency comparing to a traditional wire-wound transformer. Furthermore, the large surface areas of planar cores and traces bring the planar transformer an outstanding capability of heat dissipation, which lowers the requirements of cooling systems.

Skin and proximity effects are the main factors causing large conduction losses at MHz-level frequencies. Skin effect can be reduced by using PCB trace with a thickness less than 2 oz. It is more complex to reduce proximity effect. Using less winding lays and optimizing the winding structure are the most efficient methods to reduce the conduction loss caused by the proximity effect. In this chapter, several transformer winding designs with different types of cores, different numbers of turns, variable winding structure, and different trace thickness are calculated and discussed. Considering the balance between the AC conduction loss on the winding and the DC conduction loss on the other parts of the PCB, the trace thickness of 2 oz is determined for the design. Considering the least total transformer loss, the CR46410EC EE-core from Magnetics with R material is chosen and the 9:8 turns ratio with 1 2 2 2 2; 2 2 2 2 winding structure is verified as the optimal design for the high-frequency, high-power CLLC converter design.

To integrate the resonant inductors with the transformer, the proposed planar transformer is designed with an adjustable leakage inductance. The magnetizing inductance is adjusted by tuning the gap between two halves of the transformer core. After the magnetizing inductance is determined, the leakage inductance can be tuned by adjusting the gap between the two boards. This innovative planar transformer design

achieves highly accurate leakage inductance control, which is important for a high-frequency resonant converter, such as a CLLC converter. Furthermore, an FEA model is built to validate the proposed planar transformer design. The simulation results match the calculated values closely.

Chapter 5 : 1 MHz 3.3 kW Bidirectional CLLC Converter for EV Chargers

5.1 Design Criteria

The schematic of a bidirectional CLLC converter is shown in Fig. 5-1. The optimized planar transformer with the required leakage inductance designed in Chapter 4 based on the desired nominal operating point is utilized in the proposed converter.

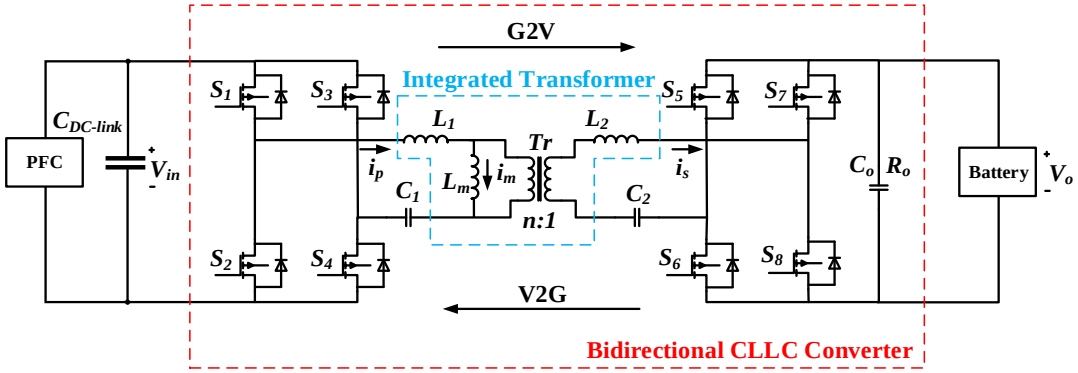


Fig. 5-1 Schematic of the proposed CLLC converter.

GaN switches from GaN systems with 650 V voltage rating and 30 A current rating are utilized in the design of converter to achieve MHz-level operations. The corresponding gate driver circuits must be well designed to drive the switches properly while making it immune to noises at high power levels.

The design specifications for the converter are carefully chosen based on the output of the PFC stage and the charging profile of a 420V battery pack. The minimum output voltage of a typical PFC stage is 380 V_{DC} working with a universal input range of 85-265 V_{rms} 50/60 Hz input voltage. For the GaN switches, the maximum drain-to-source voltage is 650 V. A factor of safety ranging from 1.2-2 is generally provided to

semiconductor devices to prevent overstressing. In this design, a factor of safety of 1.4 is chosen which restricts the maximum DC-link voltage to be 464V. For G2V mode, considering the voltage ripple on the DC-link and ringing on the switch drain-to-source voltage, a 400-450 V input voltage (i.e. DC-link voltage) of the CLLC converter is selected. For the battery side, a 250-420 V (400 V nominal value) output voltage range of the CLLC converter is sufficient to charge most of the commercially available EV battery packs. The charging profile with 3.3 kW power rating for the battery pack is presented in Fig. 5-2. The equivalent load corresponding to the charging profile is illustrated in this figure to assist the calculations of circuit parameters.

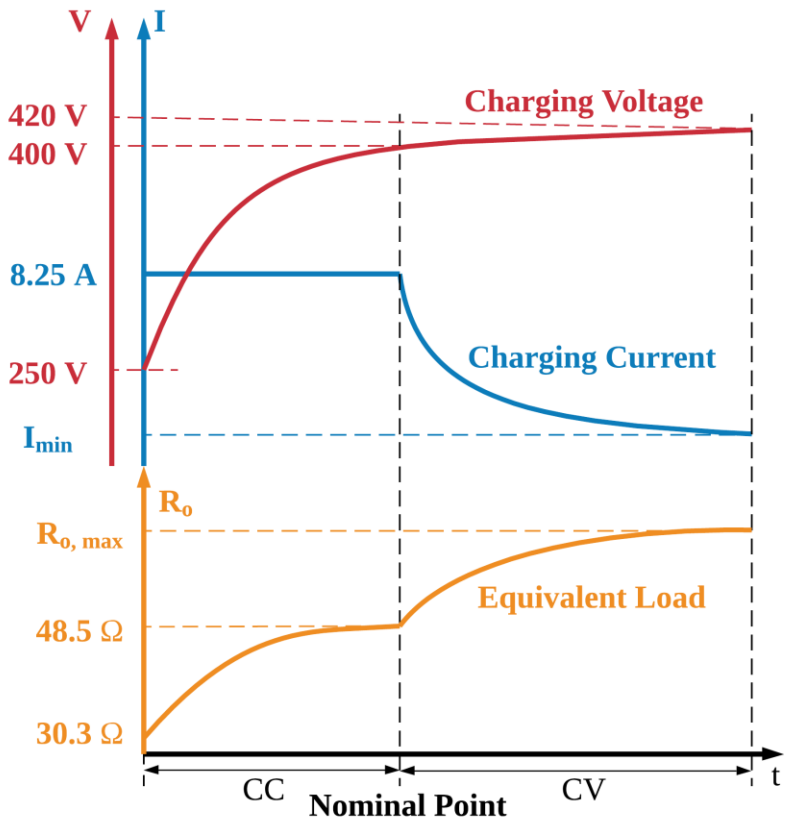


Fig. 5-2 3.3 kW charging profile with the equivalent load.

In the V2G mode, the power flows from the battery to the PFC side. The battery discharging voltage range is limited to 350-420 V in order to prevent the Li-ion battery pack from deep depletion, which results in shortening the battery life cycle. The DC-link voltage can be maintained in 400-450 V range in G2V mode. Finally, the design specifications of the proposed CLLC converter are listed in Table 5-1.

Table 5-1 Design specifications of the proposed CLLC converter

Specifications	Values
Power rating	3.3 kW
Resonant frequency	1 MHz
Topology	FBCLLC
Transformer turns ratio	9:8
G2V input voltage	400-450 V
G2V output voltage	250-420 V
V2G input voltage	350-420 V
V2G output voltage	400-450 V

5.2 Parameters of the Proposed CLLC Converter

Based on the design specifications listed in Table 5-1, with the 9:8 transformer turns ratio, the CLLC converter must have voltage gain ranging from 0.70-1.05 in G2V mode and 0.95-1.02 in V2G mode. The parameters of the resonant tank can be derived following the design methodology as presented in Section 3.2.1 and Section 3.3.1. To simplify the design, the design constraints $L_1 = n^2 L_2$ and $C_1 = C_2/n^2$ are maintained, which results in equalization of resonant frequencies for both G2V and V2G directions. Similarly, the design value of $L_m = 6L_1$ is selected as an optimized value considering the tradeoff in gain and conduction loss.

The selection of Q is critical in providing the desired operating gain under inductive region with a narrow frequency variation. If the frequency variation increases to achieve the required gain range, it may lead to higher switching losses. In this design, the worst-case scenario happens at the start of constant-current charging, where the output current is at its maximum value of 8.25 A, while operating with an output voltage of 250 V. At this condition, the converter gain reaches its lowest point of 0.7.

To meet the required gain range with narrow frequency variation, Q_{FL} at full load is chosen to be 0.45. The worst case Q_{WC} can be calculated as 0.72 from (3-5) and (3-6) using the value of Q_{FL}. Fig. 5-3 presents the gain curves of the converter operating at 400 V under full power and 250 V under the worst-case scenario, respectively. It can be seen from the curves that to achieve sufficient gains the operating frequency range is 0.87-1.34 MHz, which is a relatively-narrow range of operation for the CLLC converter. In the constant-voltage charging region, the load becomes lighter (i.e. load resistance becomes larger) as shown in Fig. 5-2, leading to a higher gain region. Hence, the operating frequencies for 420 V output are within the designed frequency range.

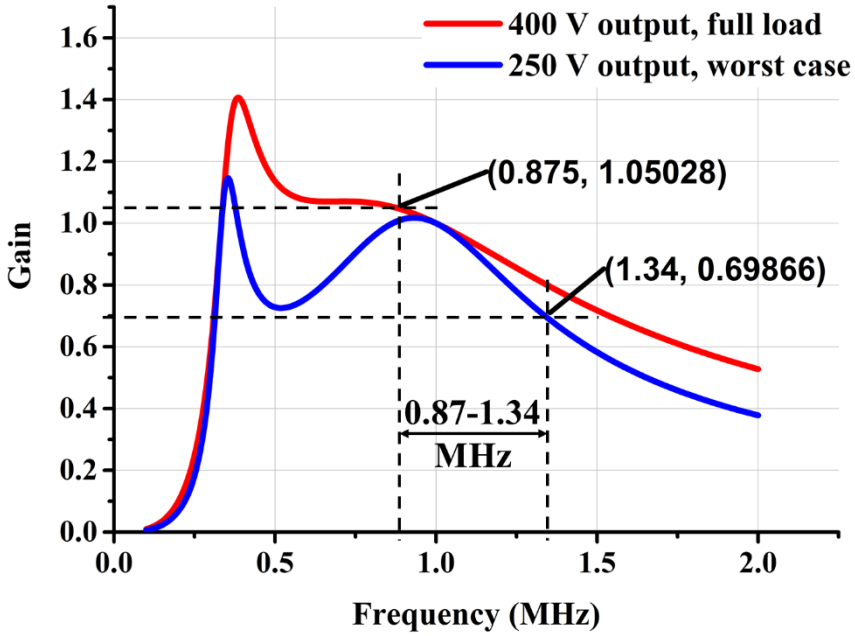


Fig. 5-3 Gain curves of 400 V output with full load condition and 250 V output in the worst case.

Similarly, for V2G mode, the gain is plotted in Fig. 5-4. Comparing to G2V mode, the variation of the load in V2G mode is less and the range of required gain is narrow due to restricted battery voltage. Hence, the operating frequency range in this mode lies between 0.95 MHz and 1.09 MHz.

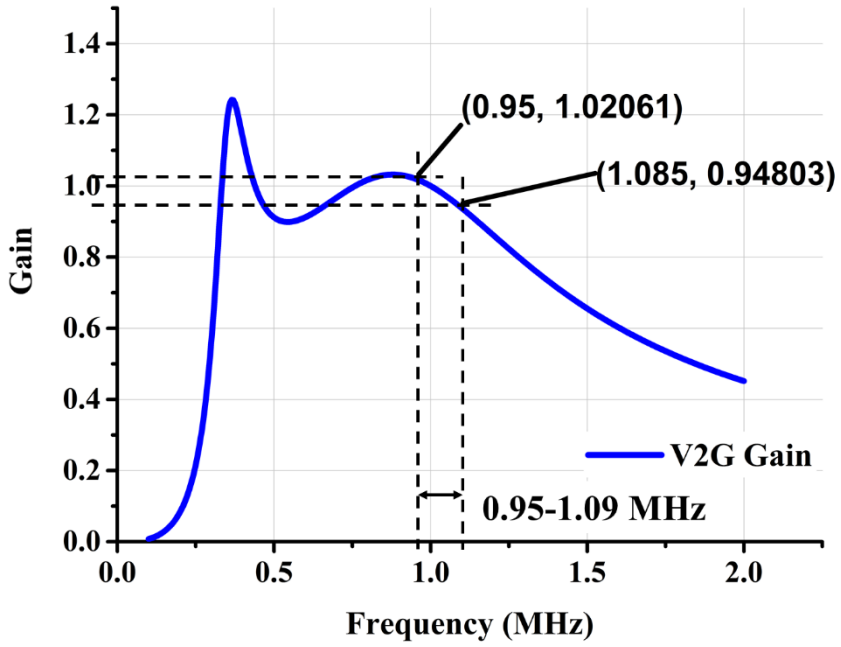


Fig. 5-4 Gain curve for the V2G mode.

Using the specifications selected based on requirements (shown in Table 5-1), the values of the resonant tank components, shown in Fig. 5-1, are computed and listed in Table 5-2. The relatively small parameter values of the resonant tank required for MHz operating frequency helps in designing a compact low volume transformer.

The output capacitance should be able to maintain the DC voltage with low ripple, which can be calculated as follows:

$$C_{out} = \frac{\Delta I}{8 f \Delta V} \tag{5-1}$$

where, ΔI is the maximum current ripple (15 A), f is the minimum output ripple frequency (2×0.875=1.75 MHz), and ΔV is the desired minimum output voltage ripple in the worst case, which is 0.4% of 250 V or 1 V. Using (5-1), the required capacitance

for a 0.4% voltage ripple is calculated as 1.07 µF, which helps in use of ceramic capacitors instead of bulky aluminum electrolytic capacitors for a compact design.

Table 5-2 Parameters of the resonant tank of the proposed CLLC converter

Parameters	Values
Transformer turns ratio, n	9:8
Primary-side resonant capacitor, C_1	7.11 nF
Secondary-side resonant capacitor, C_2	9.00 nF
Transformer leakage inductance on the primary side, L_1	3.56 µH
Transformer leakage inductance on the secondary side, L_2	2.81 µH
Transformer magnetizing inductance, L_m	21.36 µH
Output capacitance, C_o	1.07 µF
Frequency range in G2V mode	0.87-1.34 MHz
Frequency range in V2G mode	0.95-1.09 MHz

5.3 Power Loss Analysis

In order to achieve high efficiency as well as high power density, it is important to conduct a comprehensive analysis of the total power losses incurred in the converter, which will eventually assist in selecting components in an iterative manner. The losses in the converter under design can be categorized into the parts listed in Table 5-3, assuming soft-switching operation.

Table 5-3 Power losses in the proposed CLLC converter

Passive components	Active components
Resonant capacitor ESR loss	MOSFET conduction loss
Transformer core loss	MOSFET reverse conduction loss
Transformer winding loss	MOSFET turn-off loss

5.3.1 Power Losses in Passive Components

A) Resonant capacitor ESR loss

For calculating the ESR losses in the resonant capacitors, it is important to determine the corresponding RMS current. Assuming FHA equivalent circuit illustrated in Fig. 5-5, the current flowing through the resonant tank, i_p, can be determined by the ratio of the first harmonic amplitude of bridge voltage $<V_b>_1$, and equivalent tank impedance Z_{in}, seen from the primary side, where R_e is the equivalent load of the CLLC converter.

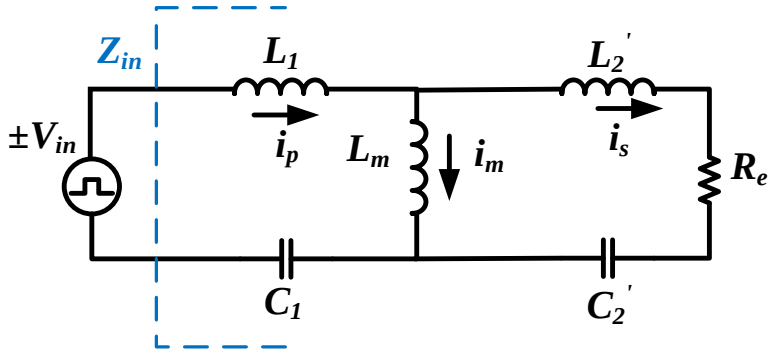


Fig. 5-5 FHA equivalent circuit of CLLC converter.

The resonant tank current, i_p, is calculated as follows:

$$i_p = \frac{< V_b >_1}{Z_{in}} = \frac{\frac{4}{\pi} V_{in}\, sin(\omega t)\, [R_e + j(\omega L_m + X_2)]}{-(\omega L_m X_1 + X_1 X_2 + X_2 \omega L_m) + j(R_e X_1 + R_e \omega L_m)} \tag{5-2}$$

where,

$$\begin{cases} X_1 = j(\omega L_1 - \dfrac{1}{\omega C_1}) \\ X_2 = j(\omega L_2' - \dfrac{1}{\omega C_2'}) \\ L_2' = n^2 L_2 \\ C_2' = \dfrac{C_2}{n^2} \end{cases} \tag{5-3}$$

Therefore, the RMS current through the primary-side resonant capacitor with a series resistance of $ESR_{p,cap}$ is the primary RMS current ($i_{p,rms}$), expressed as follows:

$$i_{p,rms} = \frac{2\sqrt{2}V_{in}\sqrt{[R_e^2 + (\omega L_m + X_2)^2]}}{\pi\sqrt{(R_e X_1 + R_e \omega L_m)^2 + (\omega L_m X_1 + X_1 X_2 + X_2 \omega L_m)^2}} \tag{5-4}$$

The primary side tank current is split between the magnetizing current and winding current, giving the following expression for the primary winding current ($i_{p,wind}$):

$$i_{p,wind} = i_{p,rms}\frac{\omega L_m}{\sqrt{R_e^2 + (\omega L_m + X_2)^2}} \tag{5-5}$$

Thus, the secondary side tank current can be calculated as:

$$i_s = n i_{p,wind} \tag{5-6}$$

and the total capacitor ESR loss can be formulated as:

$$P_{ESR} = i_{p,rms}^2 ESR_{p,cap} + n^2 i_{p,wind}^2 ESR_{s,cap} \tag{5-7}$$

where, $ESR_{s,cap}$ is the series resistance of the secondary-side resonant capacitor.

B) Transformer core and winding losses

The total transformer losses can be quantified as follows:

The core loss which depends on operating frequency and peak input voltage can be estimated using (5-8) and (5-9).

$$P_{core,EE} = a f^c B_{peak}^d \tag{5-8}$$

$$B_{peak} = \frac{V_{in}}{4NfA_e} \tag{5-9}$$

The winding loss ($P_{winding}$) depends on the effective resistance which is proportional to the frequency of operation due to skin and proximity effects is computed in (5-10).

$$P_{winding} = i_{p,rms}^2 R_{eff_p} + n^2 i_{p,wind}^2 R_{eff_s} \tag{5-10}$$

5.3.2 Power Losses in Active Components

A) MOSFET conduction loss

The switches turn on and off alternately with about 50% duty cycle, thus, each switch conducts within half of the operating period. There are four switches on each side, hence, the net conduction losses in the MOSFETs can be expressed as follows:

$$P_{MOSFET,cond} = 2(i_{p,rms}^2 R_{DS} + n^2 i_{p,wind}^2 R_{DS}) \quad (5\text{-}11)$$

where R_{DS} is the turn-on resistance of the MOSFET.

B) MOSFET reverse conduction loss

It is crucial to ensure soft switching at all the MOSFETs as the switching loss even at partial hard switching will dominate due to high switching frequency. To ensure ZVS in the primary side of the CLLC converter, there must be enough phase lag between the primary tank current and the drain-source voltage of the switch. While turning off any primary MOSFET, the stored inductive energy must be greater than the energy stored in the MOSFET body capacitor, C_B, expressed as follows [124]:

$$\frac{1}{2} L_1 I^2 > \frac{1}{2} C_B V_{in}^2 \quad (5\text{-}12)$$

$$I > V_{in} \sqrt{\frac{C_B}{L_1}} \quad (5\text{-}13)$$

From the FHA analysis of the CLLC circuit, the phase lag between the bridge voltage and resonant current can be calculated as the equivalent polar angle of input impedance phasor:

$$\varphi_{tank} = angle(Z_{in})$$

$$= arg\left(j\left(\omega L_r - \frac{1}{\omega C_r}\right) + \frac{j\left(R_{ac} + j\left(\omega L_2{}' - \frac{1}{\omega C_2{}'}\right)\right)\omega L_m}{R_{ac} + j\left(\omega L_2{}' - \frac{1}{\omega C_2{}'}\right) + j\omega L_m} \right) \quad (5\text{-}14)$$

Fig. 5-6 illustrates typical resonant tank voltage and current waveforms at the resonant frequency with a phase lag of φ_{tank}. The resonant current at the instant of turning-off a switch becomes:

$$I = \sqrt{2} i_{p,wind} sin(\varphi_{tank}) \quad (5\text{-}15)$$

Substituting (5-13) into (5-15), the lower bound of φ_{tank} can be calculated as shown below:

$$\varphi_{tank} > arcsin\left(\frac{V_{in}}{i_{p,wind}} \sqrt{\frac{C_B}{2L_1}} \right) \quad (5\text{-}16)$$

Equation (5-15) and (5-16) can be used to verify the calculated values in Table 5-2 to ensure the soft-switching conditions.

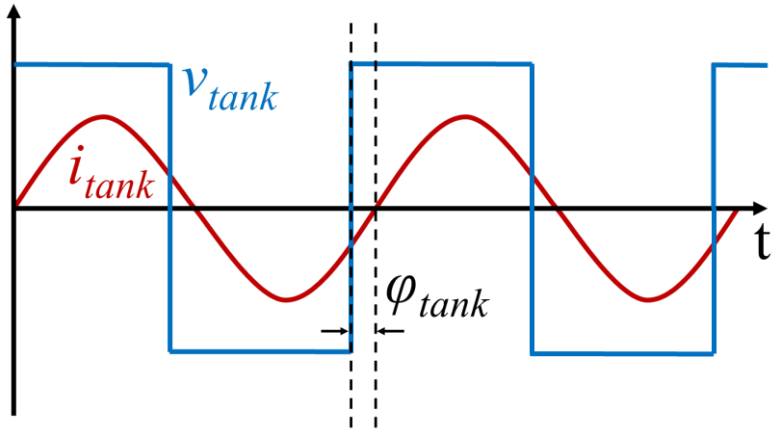


Fig. 5-6 Typical voltage and current waveforms in the resonant tank at the resonant frequency with a phase lag of φ_{tank}.

Another condition to ensure ZVS will be to set a minimum dead band interval, which would ensure the full discharge of body capacitor before the gate of MOSFET is triggered. Based on the equivalent circuit during the switching transition, shown in Fig. 5-7, the voltage across the body capacitor of MOSFET can be formulated as (5-17), which in turn sets a minimum requirement for the dead band time (t_{db}) to fully discharge the switch output capacitor (i.e. $V_{DS}(t) = 0$).

$$V_{DS}(t) = V_{in} - Z \cdot i(t) = V_{in} - Z \cdot A \cdot sin\left(\omega t_{db,min} + \varphi_{tank,min}\right) = 0 \qquad (5\text{-}17)$$

where,

$$\begin{cases} A = \sqrt{I^2 + \left(\dfrac{V_{in}}{L_m \omega}\right)^2} \\ Z = \sqrt{\dfrac{L_1}{2C_B}} \\ \varphi_{tank,min} = minimum\ tank\ phase \end{cases} \qquad (5\text{-}18)$$

Substituting (5-16) to (5-17), the ZVS condition can be fulfilled by maintaining the following requirement of the dead band time:

$$t_{db} > \frac{arcsin\left(\dfrac{V_{in}}{A \cdot Z}\right) - arcsi\,n\left(\dfrac{V_{in}}{i_{p,wind}}\sqrt{\dfrac{C_B}{2L_1}}\right)}{\omega} \qquad (5\text{-}19)$$

Thus, by satisfying the minimum dead band time and energy requirements, turn-on loss can be eliminated.

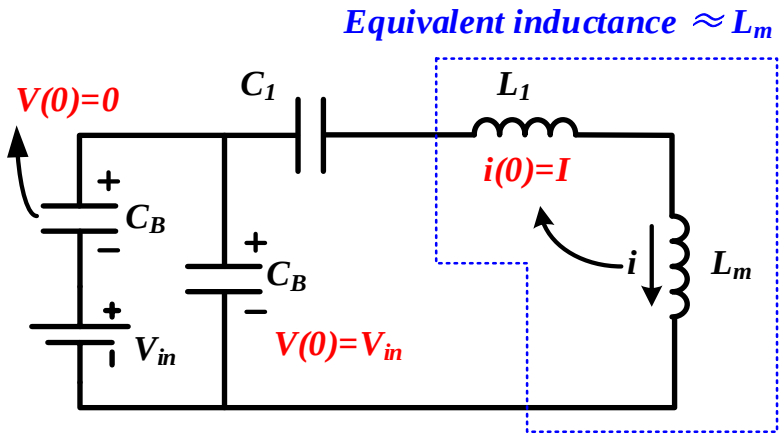


Fig. 5-7 Equivalent circuit during the switching transition.

After the voltage across the body capacitor becomes zero, the GaN MOSFET starts conducting in the reverse direction until the MOSFET gate is triggered. The reverse conduction loss ($P_{reverse}$) incurred in this interval is expressed as:

$$P_{reverse} = I(V_f + V_{GS,off})f_s \frac{\omega t_{dead} + arctan\left(\frac{I\omega L_m}{V_{in}}\right) - arcsin\left(\frac{V_{in}}{A \cdot Z}\right)}{\omega} \quad (5\text{-}20)$$

where, I and V_f represent instantaneous reverse current and voltage drop in the reverse conduction path, obtained from MOSFET datasheet; $V_{GS,off}$ represents the negative gate voltage amplitude during the turn-off period. Having a negative turn-off voltage (-3 V in this design) certainly increases the reverse conduction losses; however, it significantly enhances the noise immunity of the gate drive. The reverse conduction loss occurs for the eight switches on both the primary and secondary side GaN MOSFETs at the dead band intervals.

C) MOSFET turn-off loss

During the switching transition, on the secondary side, the MOSFETs are turned on based on the polarity of resonant current; therefore, the drain-to-source voltage and current of the device are in phase if zero-crossing of current is accurately detected, which ensures ZCS on the secondary MOSFETs. The additional turn-off loss may arise due to an inaccurate sampling of resonant current, resulting in a non-zero current during turn-off and causing losses according to

$$P_{off,sec} = \frac{V_o I t_{off} f_s}{2} \tag{5-21}$$

On the other hand, there prevail non-zero turn-off losses in case of primary MOSFETs since the current has to be non-zero for ensuring ZVS at turn-on and hence, results in hard turn-off in the rest of MOSFETs with loss $P_{off,pri}$ represented by (5-22).

$$P_{off,pri} = \frac{V_{in} I t_{off} f_s}{2} \tag{5-22}$$

5.3.3 Calculated Power Losses of the Converter

Based on the specifications of the selected components shown in Table 5-4 and using the aforementioned mathematical formulations, losses of individual components are calculated over the load range as illustrated in Fig. 5-8. Based on the analysis, the total converter loss is calculated as 98.93W for the G2V full load operation, implying approximate 97% full-load efficiency. The loss constituents are illustrated in Fig. 5-9 for better understanding.

Table 5-4 Main components of the converter

Components	Part number	QTY	Notes
Switches	GS66508T	8	R_{DS} = 55 mΩ; C_B = 67 pF
Cp	C0G 3.9 nF+1 nF	2+1	*ESR* = 10 mΩ each
Cs	C0G 3.9 nF	3	*ESR* = 10 mΩ each
Transformer core	CR46410EC	2	a = 0.014; c= 1.84; d = 2.2 $R_{eff,p}$ = 0.17; $R_{eff,s}$ = 0.13
Gate driver	Si8271AB	8	4 Amp ISOdriver; High Transient (*dV/dt*) Immunity
Voltage sensor	ACPL-C87A-500E	2	Optically Isolated
Current sensor	ACS723LLCTR	2	Galvanically Isolated

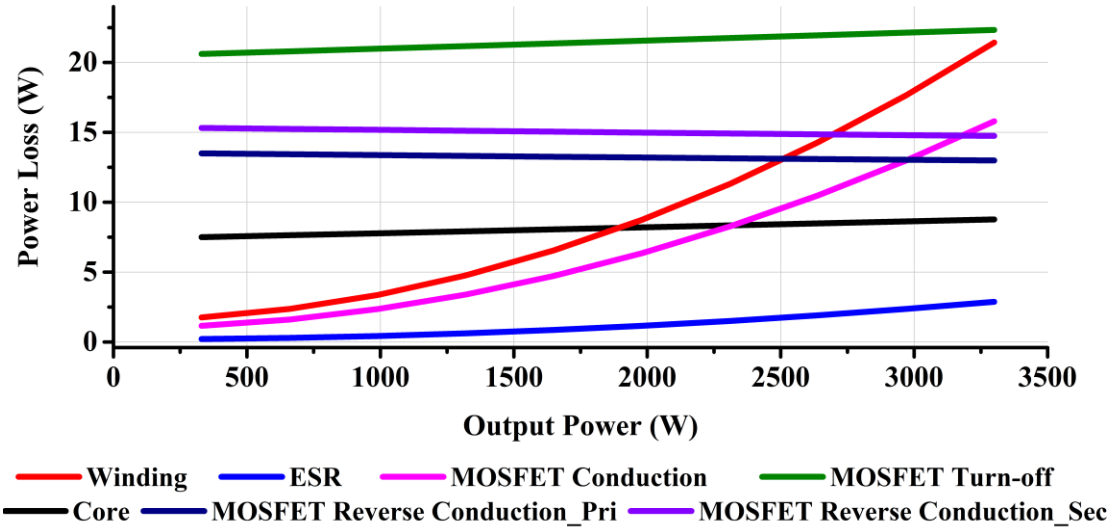


Fig. 5-8 Power loss breakdown of the converter in the entire output power range.

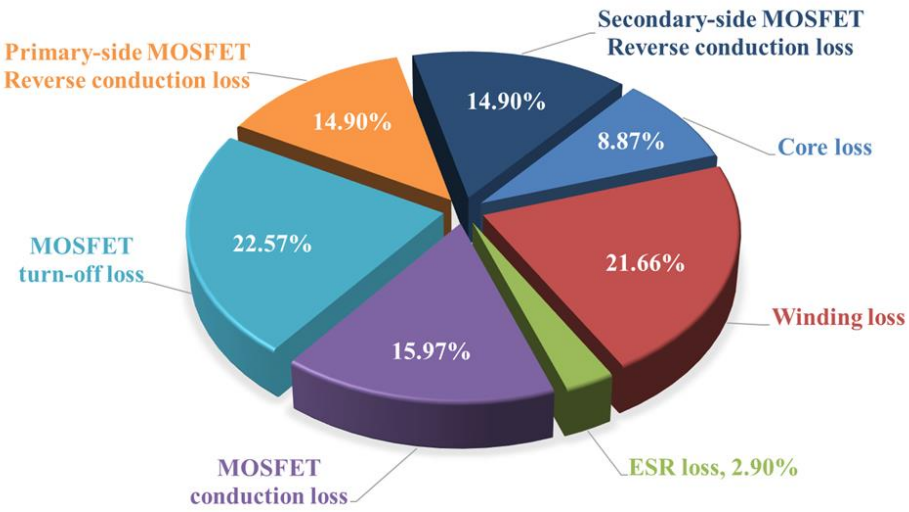


Fig. 5-9 Power loss breakdown of the converter at 3.3 kW.

Conduction losses in MOSFETs vary in a quadratic relationship with the load power, which results in a non-linear rise in junction temperatures of the power devices and hence, increases the on-state resistance of the switches. Therefore, experimentally obtained conduction losses would exceed their predicted values from a constant on-resistance based device model. On the other hand, core loss roughly remains constant due to a narrow variation range of input voltage and switching frequency subject to traversing the entire load range. The reverse conduction losses in both primary and secondary sides do not change much over the entire load range. These losses are linearly proportional to I as presented in (5-15), which remains roughly constant throughout the load power range (also illustrated in Fig. 5-8), since at heavier load (i.e. greater i_p or lower R_e), the phase angle of the input impedance (φ_{tank}) decreases and vice-versa. It is worth noting that occurrences of ZVS on both primary and secondary sides have been ensured during all the measurements. On the other hand, due to the non-zero current (i.e. enough inductive energy) to ensure ZVS on the primary side

MOSFETs, there is necessarily a certain turn-off loss in the complementary set of MOSFETs, which lowers the efficiency at lighter load operation.

5.4 Gate Driver

Since the GaN switches applied to the converter have a low threshold voltage of 1.6 V, they may be spuriously triggered in high noise conditions at high power levels. To improve noise immunity of the gate drivers, a +6/-3 V gate control voltage logic is selected. Fig. 5-10 illustrates the schematic of the gate driving system. The isolated 12 V to 9 V converter and gate driver ensure the galvanic isolation between the power and signal stages. The -3 V gate voltage reduces the probability of false triggering at the gate terminal by maintaining a larger clearance between off-state voltage and threshold voltage level. Proper layout of gate drive circuit plays an important role in the safe operation of high-frequency converters. Fig. 5-11 illustrates the PCB layout of the gate driver, where the gate paths are carefully designed with short traces to ensure reduced effective parasitic inductance.

A 10 Ω resistor is applied to the gate charging path considering the gate voltage rising time and the capability of damping the noises on the gate path. In comparison, the gate discharging path is required to release the charges accumulated on the gate-to-source and gate-to-drain capacitors in the switches as fast as possible and also be able to damp noises, thus, a 2 Ω resistor is used as the gate discharging path resistor. The ground of the driver connects to the power ground with a single point connection, which ensures low noise propagation from the power stage to the control loop.

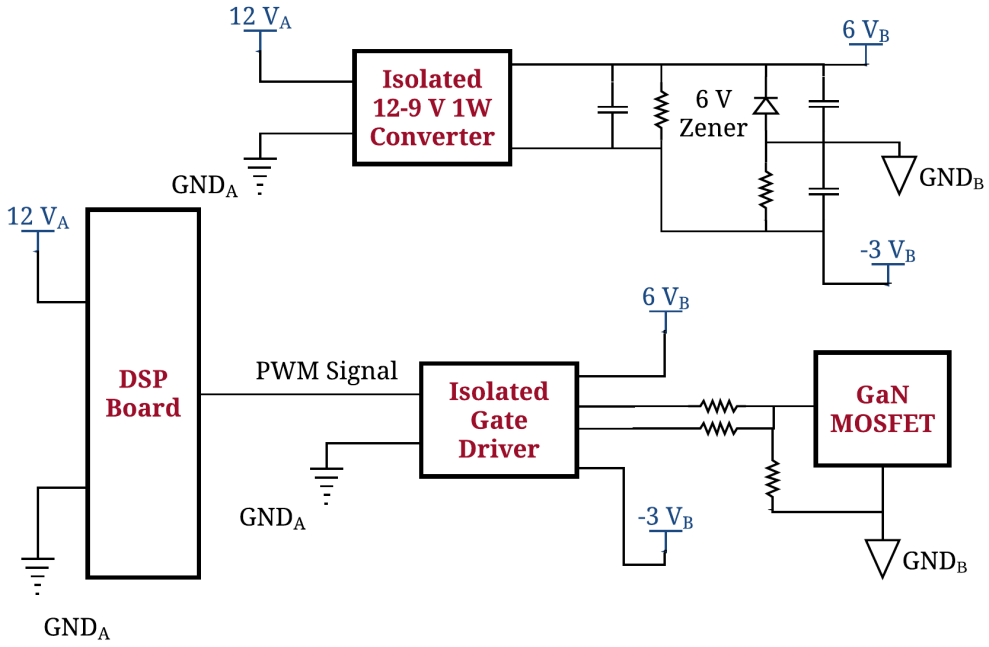


Fig. 5-10 Schematic of the +6/-3 V gate driving system.

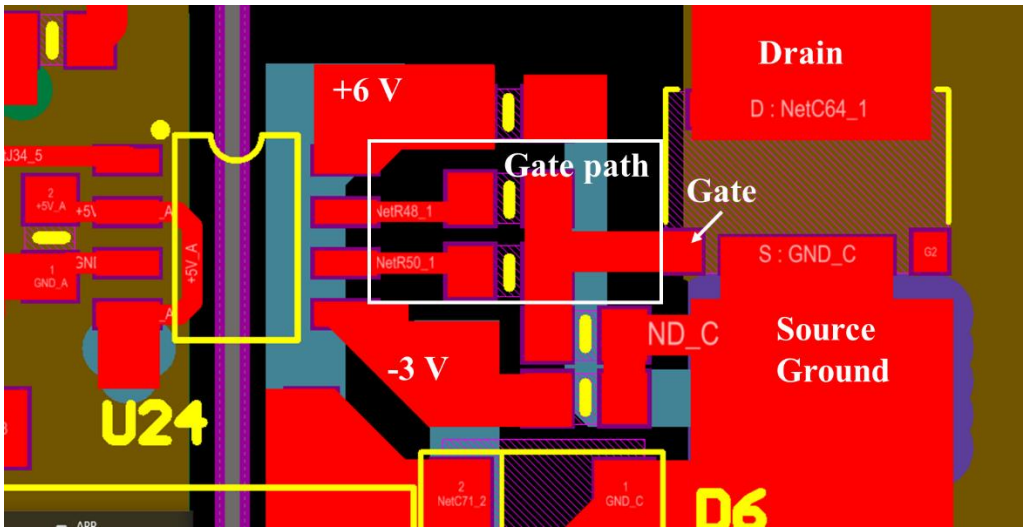


Fig. 5-11 PCB layout of the gate driver.

5.5 Control System

The converter is controlled using a TMS320F28377D-based DSP board as shown in Fig. 5-12. The pulse-width modulation (PWM) signals from the DSP card are buffered from 3.3 V to 5 V to improve the signal-to-noise ratio (SNR) and protect the DSP card against current surge or spikes on the power stage.

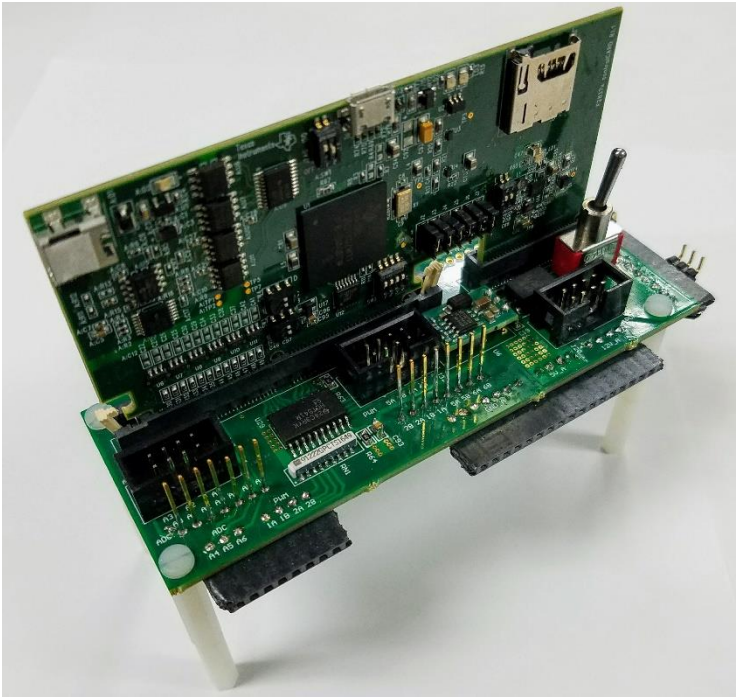


Fig. 5-12 TMS320F28377D-based DSP control board.

Fig. 5-13 shows the basic control logic for the converter. A proportional-integrator (PI) control is applied to achieve both constant-current and constant voltage control. A digital filter is implemented using DSP to filter out high-frequency noise in the feedback path. A 120 ns deadtime is set to achieve soft switching and avoid any potential shoot-through. The control algorithm is simple and computationally less intensive making it feasible for the proposed converter.

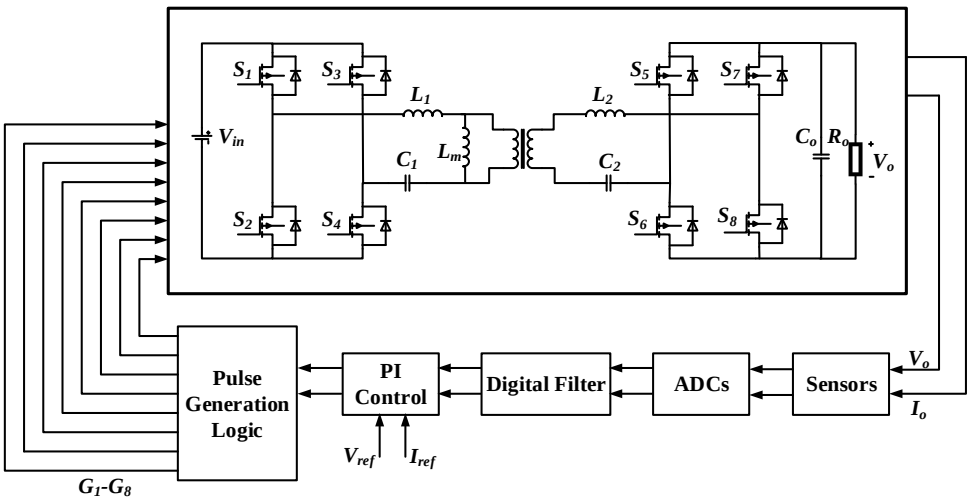


Fig. 5-13 Basic control logic of the converter.

5.6 Soft Start

To avoid surge current and protect the components during cold start, the power converter employs a soft-start operation. The output power is gradually increased during the system turn on restricting the current and voltages applied to the converter. For a CLLC converter, it is normally required to start at a switching frequency twice higher than its nominal operating frequency. In this design, it would be as high as 2 MHz operating frequency during the soft-start, however, the control platform may not be able to generate such high-frequency control signals. Therefore, the proposed soft-start strategy for the CLLC circuit combines a frequency modulation and a duty cycle modulation. With a lower duty cycle of the control signal, the switching frequency required during the soft-start operation is restricted well below twice the nominal operating frequency, which reduces the stress of the control system. The duty cycle will gradually increase up to 50% after the turn-on process is complete to ensure full power transfer.

5.7 Experimental Results

In order to verify the proposed concept, a prototype CLLC converter with 400-450 V_{DC} input, 250-420 V_{DC} (400 V_{DC} nominal) output, and 3.3 kW rated power is designed. The converter operates in a 900 kHz to 1.35 MHz frequency range with a designed resonant frequency of 1 MHz.

Fig. 5-14 shows the prototype of the proposed converter. The primary-side and secondary-side windings and components are embedded on different boards, respectively. The two boards are assembled in a stacked structure to create the transformer with appropriate leakage inductance and thorough galvanic isolation. This stacked structure can fully utilize the height of the transformer, and consequently achieve the highest power density. The converter is controlled by the DSP-based control board mentioned in the last section, which is interfaced using the connectors shown in Fig. 5-14.

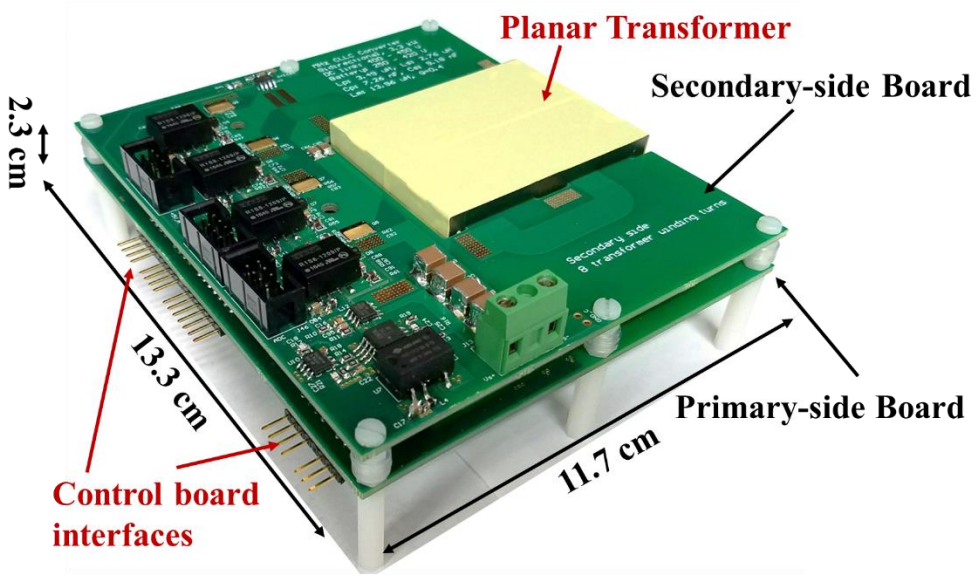
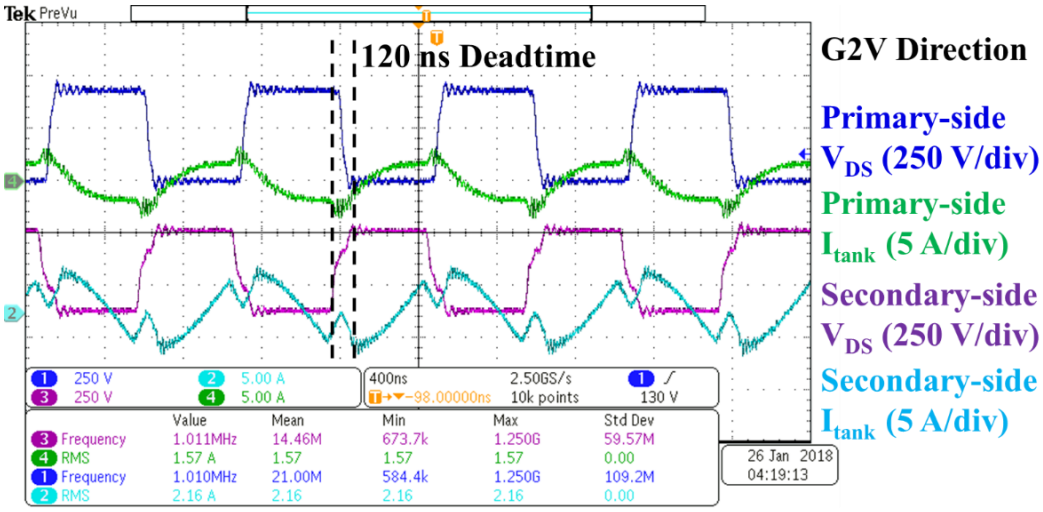


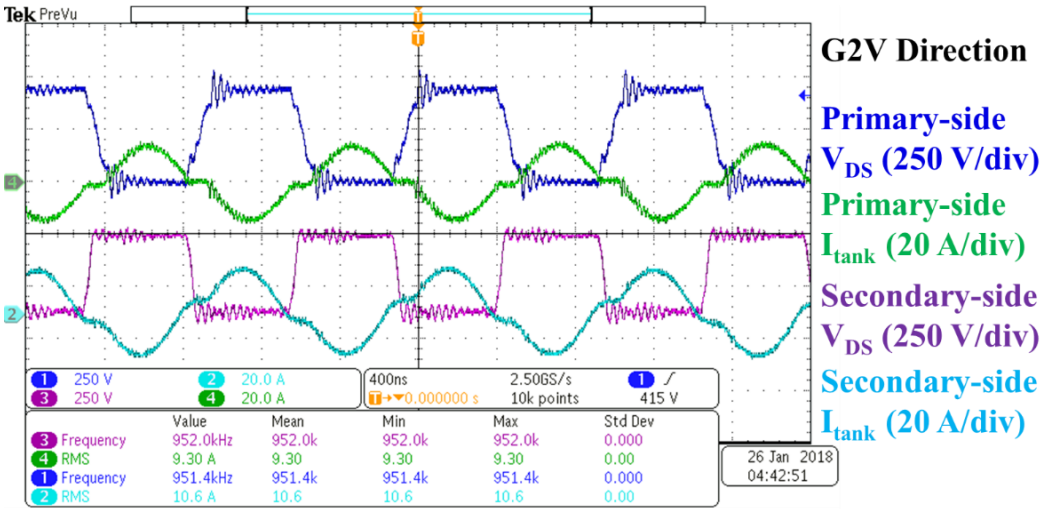
Fig. 5-14 Prototype of the proposed converter.

The volume of the prototype is 357.90 cm^3 with the dimensions (L × W × H) of 13.3 cm × 11.7 cm × 2.3 cm, achieving a power density of 9.22 W/cm^3 (151.1 W/in^3), which is about twice higher than other CLLC converters [86], [90].

Fig. 5-15 shows the experimental waveforms for G2V operation under 10% load and full-load conditions. The input voltage is 450 V and the output voltage is 400 V. The converter operates at 1.01 MHz under 10% load condition and 952 kHz under full load condition. At this timescale, it can be seen that there is a sudden drop in current during the dead time at light-load conditions (shown in Fig. 5-15(a)). The apparent discontinuity in the secondary current happens due to insufficient energy stored in the leakage inductance. The fall in current can be characterized by a piecewise sinusoidal segment with the resonant frequency generated by the MOSFET body capacitances and the series combination of leakage and magnetizing inductances. It can be inferred from the waveforms that under both light and heavy-load conditions, the primary-side switches operate with ZVS turn-on. For the secondary side switches, they operate under ZVS turn-on and ZCS turn-off at the heavy-load condition and partial ZVS turn-on with ZCS turn-off at the light-load condition.



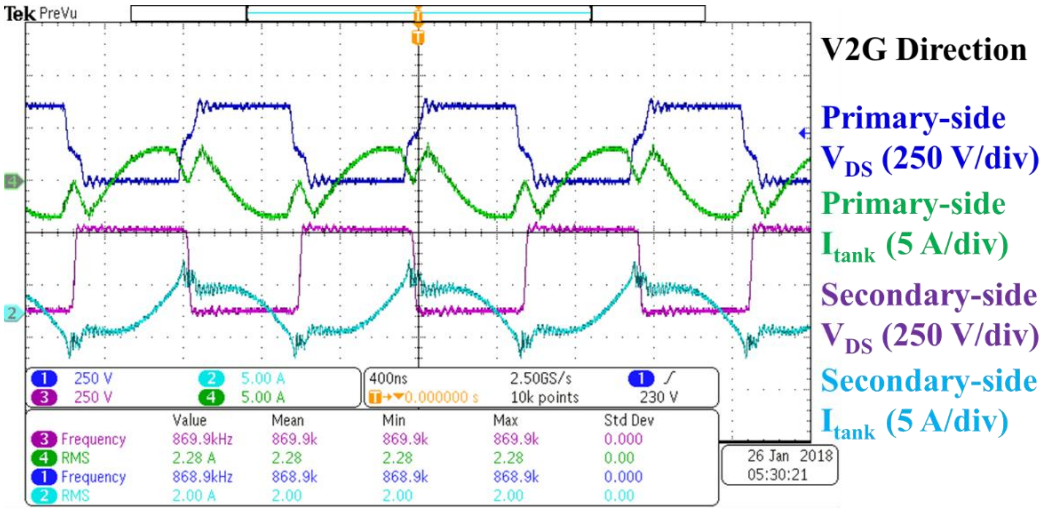
(a)



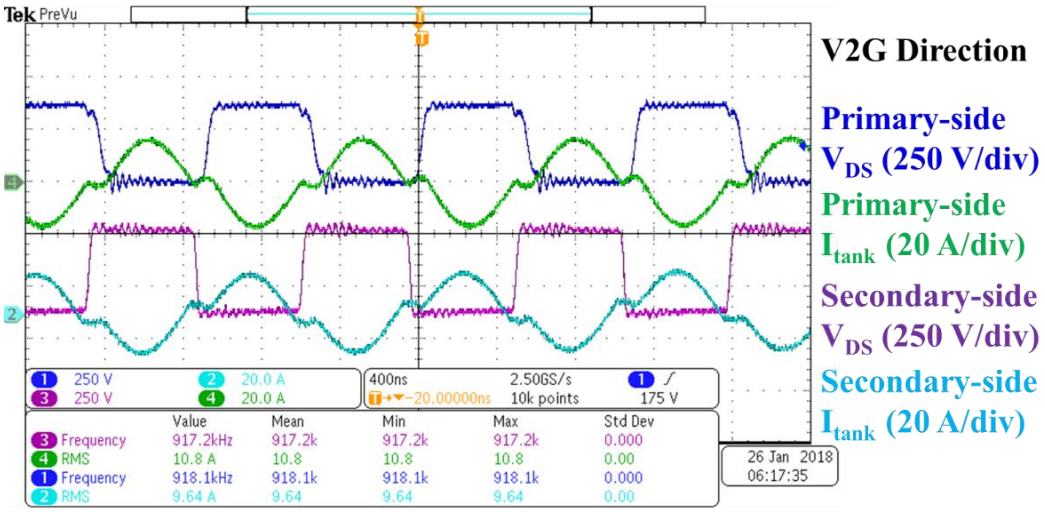
(b)

Fig. 5-15 Experimental waveforms under (a) 10% load and (b) full load in G2V direction.

In the V2G operation, the converter exhibits similar performances to those of the G2V operation. Fig. 5-16 shows the 10% and full load experimental waveforms in V2G direction. The output voltage is regulated at 400 V with a voltage ripple less than ±1% and ZVS is achieved on all the MOSFETs on primary and secondary sides at all power levels from 10% to the rated load.



(a)



(b)

Fig. 5-16 Experimental waveforms under (a) 10% load and (b) full load in V2G direction.

The conversion efficiency is measured using Tektronix PA 3000 power analyzer. The experimentally measured and theoretically calculated efficiency curves are shown in Fig. 5-17. The mismatch between experimental and theoretically predicted efficiencies at relatively lighter load can be explained by having a conservative estimate of turn-off loss assuming the device will block full DC link voltage during turn-off.

However, in practice, the blocking voltage during turn-off will be swinging down to a lower value than the DC link voltage due to resonant behavior of the tank formed during the switching transition interval.

The converter achieves a peak efficiency of 97.2% with 400 V output in G2V mode. It is also tested with 250 V output voltage and up to 2 kW power level in G2V mode, and the efficiency curve is shown in the figure as well. Due to the higher operation frequency (about 1.35 MHz), the efficiency of the 250 V output condition is slightly lower than that of the 400 V output one. For the V2G mode, a peak efficiency of 96.6% is achieved. The results show that the proposed MHz-level CLLC converter can achieve high efficiency as well as high power density.

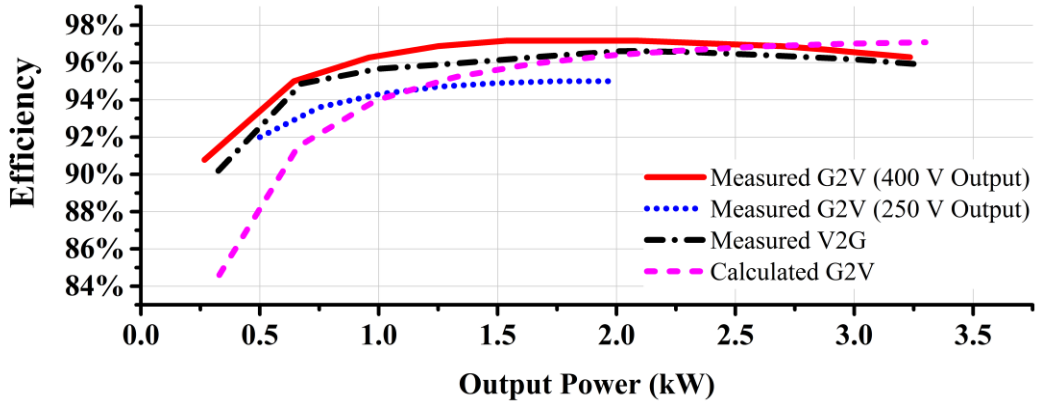


Fig. 5-17 Measured and calculated efficiency curves.

The entire converter including the DSP control board connected and attached heat sinks is presented in Fig. 5-18. Due to the high efficiency of the converter and sufficiently large surface area of the planar transformer windings, the thermal stress of the converter is controllable. Aluminum heatsinks (with a dimension of 2 cm × 2 cm × 1.7 cm) with fins are applied on each MOSFET. With 25˚C ambient temperature and

500 linear feet per minute (LFM) fan speed, the highest temperature of the converter is 40˚C at 2 kW and 70˚C at full load. The hotspot occurs on the transformer winding vias due to the heat transfer from the winding loss, as shown in Fig. 5-19.

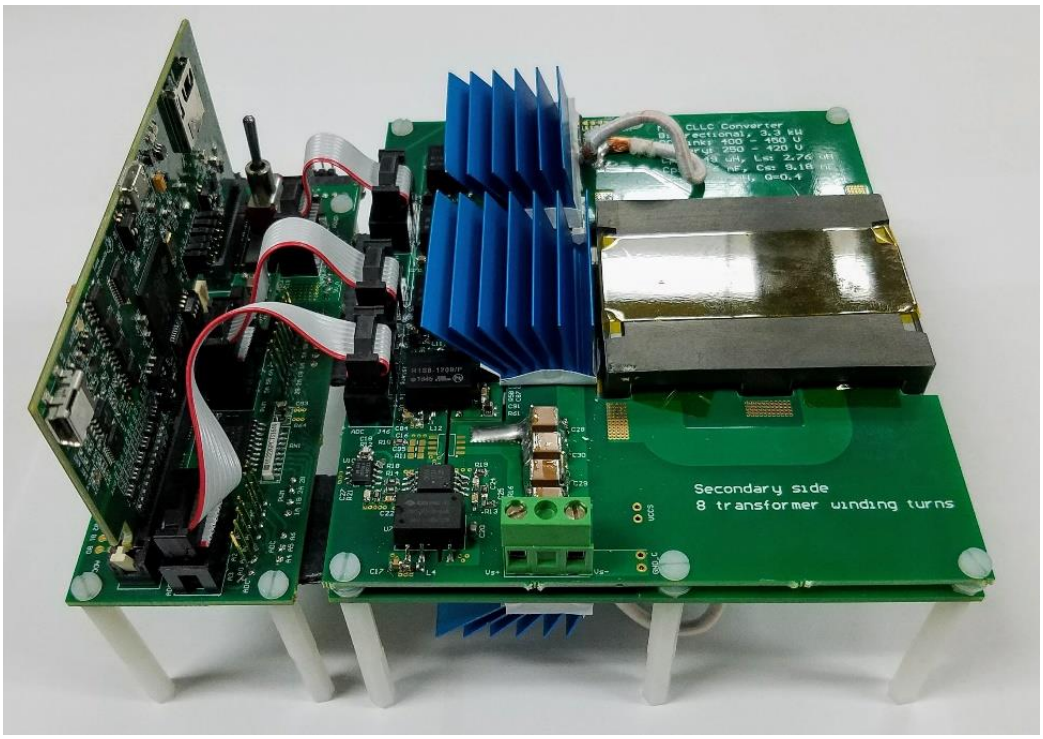


Fig. 5-18 Entire system with DSP board connected and heat sinks attached.

Fig. 5-19 Thermal test result of the converter prototype operating at 2 kW.

5.8 Summary

In this chapter, the design specifications for a 1 MHz 3.3 kW CLLC converter are determined based on the battery charging profile and electrical characteristics of the GaN switches. The required gain and frequency ranges of the converter are computed based on the specifications, and the values of the key components are calculated and verified. A detailed power loss model of the proposed CLLC converter is presented. The proposed CLLC topology ensures soft-switching of the switches on both primary and secondary sides, leading to a significantly reduced switching loss at MHz-level operating frequencies. The use of GaN switches allows the converter operating at high frequencies with high power levels, however, the GaN switches have a relatively low threshold voltage, resulting in a low noise immunity, thus a +6/-3 V gate driving system is designed to provide sufficient power to drive the switches with improved noise immunity. To control the proposed system precisely, a control platform based on

TMS320F28377D DSP card is designed and the control algorithm is presented in this chapter.

Finally, a proof-of-concept prototype of the proposed converter is designed, built and tested up to 3.3 kW with 400-450 V_{DC} input voltage and 250-420 V_{DC} (400 V_{DC} nominal) output voltage. The peak efficiencies reach 97.2% for G2V direction and 96.6% for V2G direction at around 50% rated load power. The high conversion efficiency leading to reduced cooling requirements, MHz passive components, and innovative stacked planar transformer structure play critical roles for the proposed converter in reaching a power density of 9.22 W/cm^3 (151.1 W/in^3), which is twice higher than other state-of-the-art designs.

Chapter 6 : Conclusion and Future Work

6.1 Conclusion

The fast growth of the EV market drives the development of high-performance and compact onboard chargers. As an essential part of a bidirectional EV onboard charger, an isolated DC-DC converter plays a critical role in achieving high power density, high efficiency, and bidirectional power flow.

In this work, to meet the challenges of power density and high efficiency, a bidirectional CLLC topology based DC-DC converter using a novel stacked planar magnetic structure is proposed with MHz level operating frequency. This research mainly focuses on providing innovative solutions for the design of MHz, power dense DC-DC converters.

This complex and multidisciplinary topic is decomposed into three stages. In the first stage, a comprehensive literature review on the state-of-the-art of high-frequency and bidirectional DC-DC topologies is completed. The advantages and disadvantages of two candidate topologies for EV onboard chargers, CLLC and DAB, are investigated, analyzed and discussed in details. A methodology to fully evaluate the performances and characteristics of the CLLC and DAB converters is proposed. Both CLLC and DAB converters can achieve high efficiency, galvanic isolation, and wide output range. Four prototypes (FBCLLC, HBCLLC, FBDAB, and HBDAB) are designed and developed with 1 kW power rating and 170 kHz operating frequency. The performances of the four converters are comprehensively analyzed and compared. The results show that at 1kW and 3.3kW power levels the CLLC converter is more suitable

for EV onboard charger applications due to the wider soft switching range and less output filter requirements, compared to the DAB converter.

Based on the conclusions of the first stage, the CLLC converter is selected for the compact, MHz-level, and multi-kW design. To achieve high power density, a planar transformer is a necessity to replace the bulky and heavy traditional wire-wound transformers. Therefore, in the second stage, an innovative stacked planar transformer structure with adjustable leakage inductance is proposed. In order to reduce the AC conduction loss of the magnetic components at high frequencies, resonant inductor integration with the planar transformer is a necessity. Hence, the leakage inductance of the transformer must be sufficient and precisely adjustable. The proposed stacked planar transformer structure can be used to achieve precise tuning on both magnetizing and leakage inductances. The impacts of skin and proximity effects on a planar transformer at MHz-level frequencies are mathematically modeled for accurate loss modeling. An optimal design methodology of the planar transformer is proposed to find the best winding turn number and winding structure to maximize efficiency. To validate the planar transformer design, an FEA model using ANSYS Maxwell is developed. It is shown that the simulation results favorably match the theoretical calculations.

Finally, in the last stage, a high-frequency, bidirectional, compact CLLC converter for EV applications is designed. A variable DC-link algorithm is used to reduce the gain range requirement of the CLLC converter, resulting in a relatively narrow operating frequency range, which is highly beneficial in MHz level design. Furthermore, CLLC converters typically have the highest efficiency at their resonant frequency; thus, a narrow operating frequency range makes the converter highly

efficient throughout the entire load range. Consequently, in this work, a 400-450 V input, 250-420 V output CLLC converter prototype is built and the prototype operates with 3.3 kW power rating and 1 MHz resonant frequency. With the help of the proposed optimal design methodology, the CLLC prototype achieves peak efficiencies of 97.2% in G2V mode and 96.6% in V2G mode, respectively.

The MHz-level operating frequency design leads to an ultra-compact design utilizing proposed innovative integrated planar transformer and low-profile ceramic resonant and output capacitors. Moreover, with the high-efficiency optimized design, the cooling requirement of the converter is relatively low, leading to a small heatsink volume. With the help of advanced design solution and optimization, the proposed converter achieves a power density of 9.22 W/cm^3 (151.1 W/in^3), which is twice power dense compared to other state-of-the-art solutions.

The major contributions of this dissertation are summarized as below:

First, we develop a comprehensive methodology to evaluate the performance of a DC-DC converter for EV onboard chargers. The evaluation is based on efficiency, soft-switching region, design and control complexity, component power stress, and power density. The evaluation methodology is simply applicable to different power and frequency levels.

Second, we propose an innovative stacked planar transformer structure which can be used to design a transformer with precise leakage and magnetizing inductances. This property can significantly help in resonant converter designs.

Third, we formulate a mathematical model of power losses in a planar transformer at MHz frequency. The model estimates the impact of skin and proximity effects on

the planar transformer windings and calculates the losses for different winding structures. Based on the proposed model, an optimal planar transformer design methodology is developed which helps to minimize the total power losses, leading to the highest transformer efficiency.

Fourth, we present a detailed system-level power loss model for MHz resonant converters. The loss model includes switch's conduction, reverse conduction, and partial hard switching losses, resonant capacitor ESR losses, and planar transformer losses, which helps in cooling system design.

Last, a prototype with the improved gate driving system is built, operating at 1 MHz and 3.3 kW. The measured results highly match the theoretical calculations. Based on our best knowledge, this is the *first* CLLC converter working at such high frequency and power levels. Moreover, using all the proposed design methodologies and optimizations, the prototype achieves 97.2% peak efficiency with the power density of 9.22 W/cm^3 (151.1 W/in^3).

6.2 Future Work

6.2.1 Development of a Maximum-efficiency Control Algorithm

A completed onboard charger can be built which requires the integration of a PFC stage and the proposed DC-DC converter as shown in Fig. 6-1. Since the charger operates with a variable DC-link voltage, developing an online, optimized, and real-time maximum-efficiency control algorithm for the charger becomes challenging. The control algorithm should be able to adjust the DC-link voltage considering load

conditions to achieve the maximum efficiency for the entire system. Several problems need to be addressed for its effectiveness and practicality.

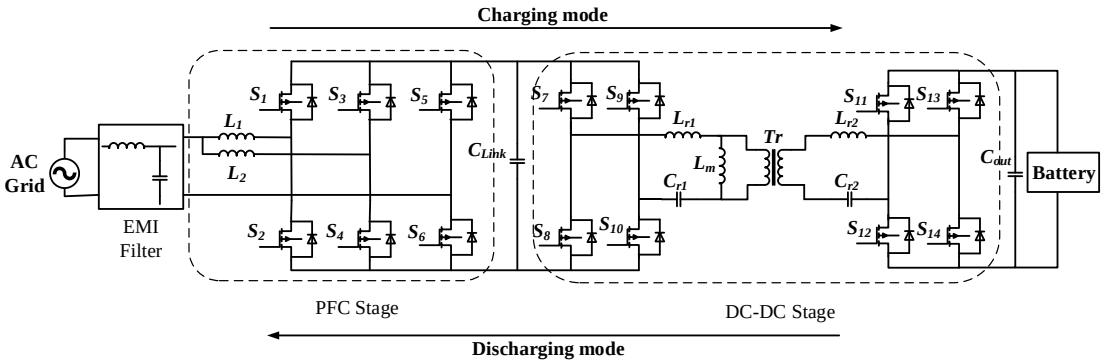


Fig. 6-1 Final topology of high frequency bidirectional onboard charger.

First, as shown in Fig. 6-1, an interleaved totem-pole bridgeless boost converter can be used as the PFC stage due to its small current ripple, low EMI and reduced inductor size [125]. The efficiency of this stage is related to the load and operating duty cycle (i.e. DC-link voltage), and the efficiency of the CLLC converter is dependent on the load and operating frequency (i.e. DC-link and output voltage). Based on these properties, two completed efficiency maps can be drawn for each stage within the entire load range and DC-link voltage range. Then, the optimal DC-link voltages with respect to the variable loads can be determined by finding the maximum efficient combination of two stages. Eventually, the maximum-efficiency control algorithm can be implemented by monitoring the real-time load condition and adjusting the DC-link voltage following the gathered data.

Second, a common problem in a system of cascaded switching power converters (AC-DC and DC-DC in this case) is the dominance of common-mode (CM) EMI noise, arising from the parasitic capacitances existing between DC link terminals and chassis

ground. Since the entire converter system can be considered as a single-phase PFC rectifier with a MHz switching DC-DC load, the high-frequency common-mode leakage current flows to the electrical ground and makes the CM EMI (between 10 MHz to 30 MHz) performance worse. In this aspect, an innovative approach of creating a noise circulation path inside the converter can be developed to prevent the noise from propagating to the grid. Also, the proposed solution should take care of minimizing the net volume and weight of the add-on filter components as a part of the EMI solution.

6.2.2 Optimal Designs for Higher Power Extensions

Currently the most common onboard charging power levels for PHEVs and EVs are respectively, 3.3kW and 6.6kW. However, the EV industry is looking for extending the onboard charging power levels to even higher power levels such as 11kW and 22kW. For higher power onboard charger designs, such as 6.6 kW, 11 kW, or even 22 kW, a multi-phase interleaved totem-pole topology can be implemented to extend the power rating of the PFC stage. However, limited by the size and magnetic core properties, the rated power of a single planar transformer is restricted. Higher power extension of the proposed 1 MHz converter is another challenge in the future work. Higher power results in a significant increase in winding loss and may lead to the saturation of the transformer.

Matrix transformer can be one solution as shown in Fig. 6-2 for higher power applications. Instead of using a single planar transformer, several (depends on the total power rating) planar transformers with relatively low power ratings are connected in parallel to form a matrix transformer. The current-split flows through all the transformers resulting in significantly reduced winding losses. The required power

rating of each transformer is also much lower than that of a single transformer. However, the matrix transformer requires all the individual transformers highly identical to avoid any unbalance conditions, which result in large circulating current and power loss. Fortunately, for planar transformers, with the PCB windings, it is not problematic to build all the individual transformers identically. For the other components, power rating should be sufficient to conduct higher current flow. Furthermore, due to the highly non-linear gain performance of CLLC converters as analyzed in Chapter 3, the design of a CLLC converter for 11 kW and 22 kW power levels can become exceedingly difficult. Moreover, the peak resonant current can be extremely large resulting in high component stress. Hence, at these power levels, a DAB topology with relatively low design and control complexity could be a more suitable solution.

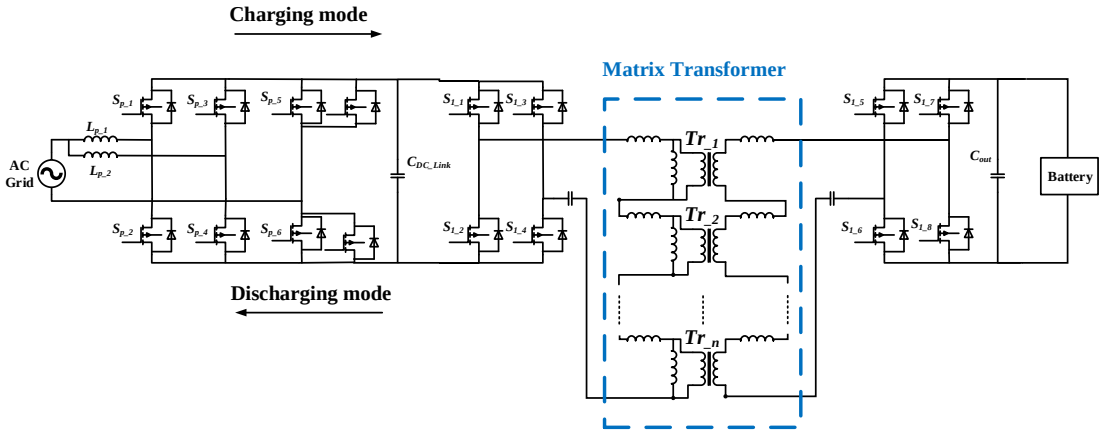


Fig. 6-2 Higher power extension with matrix transformer.

Another solution is to parallel connect multiple proposed 3.3 kW CLLC modules for higher power ratings as shown in Fig. 6-3. In comparison to the solution with a matrix transformer, this structure has a major advantage of a higher efficiency at light load conditions, since each CLLC module can be turned on and off independently. At

light load conditions, selected modules can be turned off to ensure the turn-on modules operating at their maximum efficiency conditions. More importantly, this structure does not increase the design complexity for high power levels. Furthermore, each module this structure can work individually which improves the robustness of the system. The main disadvantage of this solution is the relatively higher control complexity and higher cost of the gate driving system. Furthermore, this approach will lead to a larger and heavier system.

In the future work, the two potential solutions can be developed and compared for 6.6 kW, 11 kW, and 22 kW to find the optimal designs for the higher power extensions. A liquid cooling system is a necessity to maintain the operating temperature due to high loss density incurred from power dense design. With an optimal design, the power density could potentially be at least twice compared to other level 2 onboard chargers on the market.

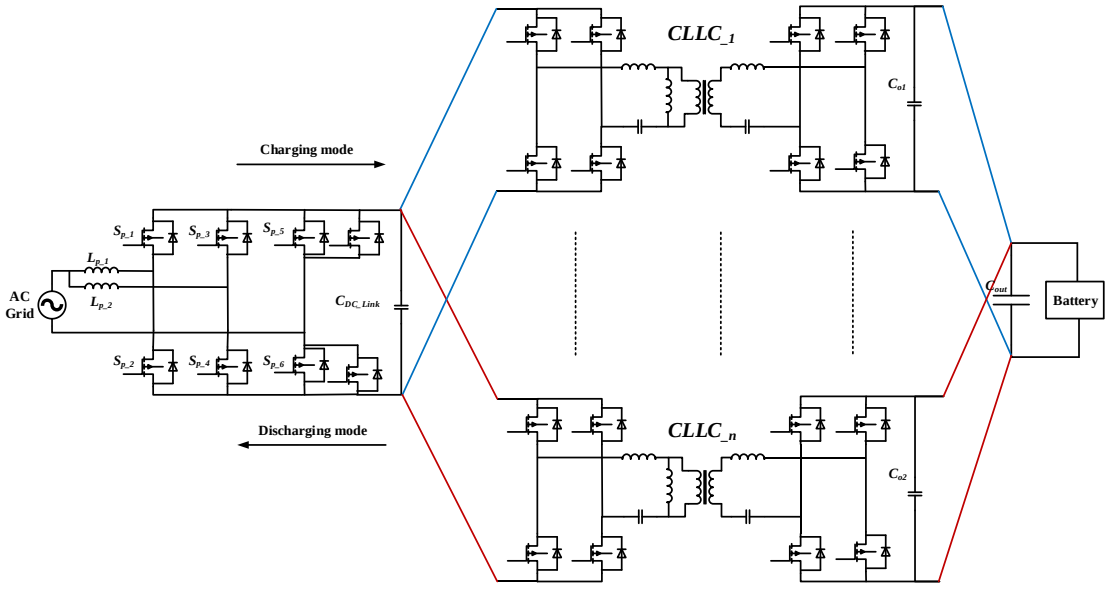


Fig. 6-3 Higher power extension with multiple proposed CLLC modules.

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