ABSTRACT

Title of Thesis: Design of a Quasi-Adiabatic Current-Mode Neurostimulator Integrated Circuit for Deep Brain Stimulation

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Electrical stimulation of neural tissues is a valuable tool in the retinal prosthesis, cardiac pacemakers, and Deep Brain Stimulation (DBS). DBS is being to treat a growing number of neurological disorders, such as movement disorder, epilepsy, and Parkinson's disease. The role of the electronic stimulator is paramount in such application, and significant design challenges are to be met to enhance safety and reliability. A current-source based stimulator can accurately deliver a charge-balanced stimulus maintaining patient safety.

In this thesis, a general-purpose current-mode neurostimulator (CMS) based upon a new quasi-adiabatic driving technique is proposed which can theoretically achieve more than 80% efficiency with the help of a dynamic high voltage supply (DHVS) as opposed to most conventional general-purpose CMS having less than 25% efficiency. The high-voltage supply is required to withstand the voltage seen across the electrodes (>10V) due to the time-varying impedance presented by the electrode-tissue

interface. The overall efficiency of the designed CMS is limited by the efficiency of the DHVS.

A HVDD of 15V is created by the DHVS from an input voltage (VDD) of 3V. The DHVS circuit is made by cascading five charge pump circuits using the AMI 0.5µm CMOS process. It can maintain more than 60% efficiency for a wide range of load current from 25µA to 1.4mA, with peak efficiency at 67% and this is comparable with existing specific-purpose state-of-the-art high-voltage supplies used in a current stimulator. The stimulator designed in this thesis employs a new efficient charge recycling mechanism to enhance the overall efficiency, compared to the existing state-of-the-art CMSs. Thus, the overall CMS efficiency is improved by 20% to 25%. A current source, programmable by 8-bit digital input, is also designed which has an output impedance greater than 2MΩ with a dropout voltage of only 120mV. Measurements show voltage compliance exceeding +/-15V when driving a biphasic current stimulus of 10µA to 2.5mA through a simplified R-C model of the electrode-tissue interface. The voltage compliance is defined as the maximum voltage a stimulator can apply across the electrodes to achieve neural stimulation.

Design of a Quasi-Adiabatic Current-Mode Neurostimulator Integrated Circuit for Deep Brain Stimulation

by

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Chapter 1: Introduction

Electrical stimulation of tissues is an increasingly valuable tool for the treatment of a variety of disorders. Stimulation of peripheral nerves [1], cochlea [2], retinal neurons [3], cardiac pacemakers, and deep brain stimulation (DBS) [4] are some common examples of neuromodulation applying an electrical stimulus. Deep brain stimulation is presently being used to treat a growing number of neurological disorders, such as movement disorders, epilepsy, and Parkinson's disease. It has also shown a potential benefit for a variety of other disorders such as Tourette syndrome, depression and obsessive-compulsive disorders [5, 6, 7, 8]. The role of electronic stimulators is paramount in such application. Significant design challenges need to be met in order to enhance safety and reliability.

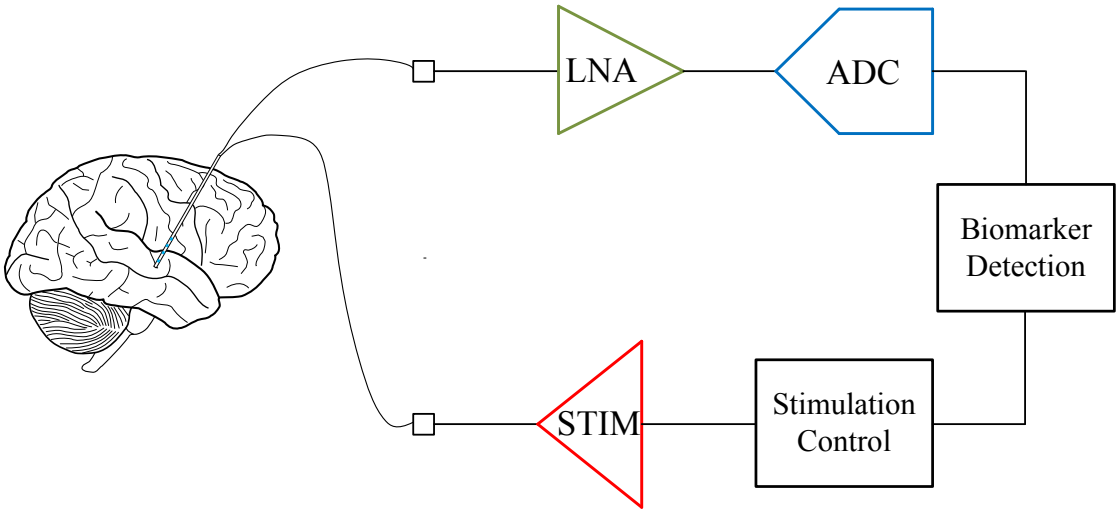

Fig. 1.1 Example of a bidirectional neuromodulation system used in DBS

Fig. 1.1 shows a closed-loop neuromodulation system used in DBS. Local field potential (LFP), ECoG or EEG signals are recorded from a relevant region of the brain

by a low-noise programmable-gain amplifier. Then the recorded signal is digitized for suitable biomarker detection by an on-chip digital signal processor. Upon detection of an anomaly, a stimulus is provided. Stimulus control determines the amount of charge to be delivered for the excitation of neurons. However, net charge injection must be zero for safety reasons. Non-zero charge injection generates DC offset voltages at the electrode-electrolyte interface within neural tissues [9]. The corresponding electric field strengths can rise beyond tolerable limits and cause tissue inflammation, and permanent damage [10]. Additionally, inadequate charge balancing induces a pH shift in biological electrolytes, which leads to the dissolution of electrode surface due to electrolysis and induces toxic substance into the biological environment. Finally, over time, charge accumulation can lead to increased electrode impedances, which adversely affect voltage compliance of the stimulator and induce noise in the neural recording. A strict requirement of the stimulus is, therefore, to be charge-balanced.

The charge-balanced stimulus may be either current regulated or voltage regulated. Current-source based stimulators can deliver accurate charge balanced-stimulus by controlling the stimulation duration from a constant current source [11]. However, they are generally inefficient, consuming as we show in Chapter 2, several times more energy necessary to achieve stimulation of the tissue.

In a voltage mode stimulator a constant voltage source is realized. They are sometimes used as an alternative to a current stimulator because of their inherently higher energy efficiency [12]. However, it cannot control the amount of charge delivered as in current mode stimulation due to varying electrode-tissue impedance

resulting in unknown amount of charge delivered. A new charge-metered and impedance invariant voltage stimulator is developed in [13, 14].

An energy-efficient charge-controlled stimulator was reported in [15]. Here the total number of injected charges are limited by discharging a series of capacitors, but the capacitors require a significant amount of area and the discharging time cannot be precisely controlled.

A conceptual diagram of how the neural stimulation is done in DBS is shown in Fig. 1.2. A Medtronic lead 3389 is illustrated here. There are four cylindrical shaped Pt-Ir electrodes present inside it [16]. Two of these electrodes are used for neural stimulation, and they are named "active" and "return" electrodes. The other two can be used for neural signal recording. Inside the stimulator there are a current source or a voltage source, either of which can be chosen to achieve current or voltage mode stimulation respectively.

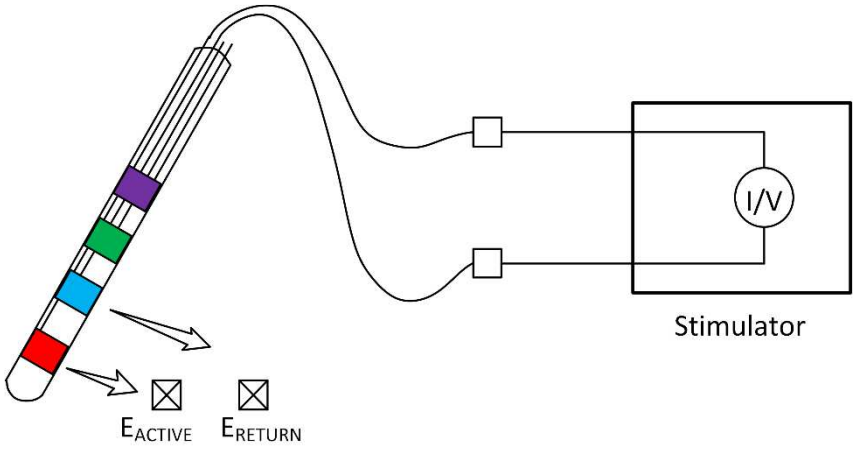

Fig. 1.2 Conceptual diagram of neural stimulation in DBS

Use of both current and voltage mode stimulation for DBS is reported in the clinical literature [8, 17, 18]. Commercial neurostimulators developed by Medtronic incorporate both modes [19, 20]. In this thesis, we will show the design of a current mode stimulator in the following chapters.

Neurostimulators are often powered by an implanted battery or by an implanted RF coil receiving energy wirelessly. Thus, the energy efficiency of the stimulator is critically important to determine the size of battery or coil, and improvement of energy efficiency of the stimulator leads directly to an increase in battery life and reductions in tissue heating. If the size of the implant can be reduced, patient safety and comfort are increased, and medical costs are reduced. Therefore, there is a strong motivation to improve the energy efficiency of the stimulator which often consumes the lion's share of power in a prosthesis or implant.

To improve the efficiency of a current mode stimulator, an adiabatic driving technique can be applied where the supply voltage is varied dynamically. Here "adiabatic" driving is defined as a process that has zero energy loss. Theoretically, in such process, all energy delivered is utilized in driving the impedance between the electrodes. This technique is implemented in [21] at the expense of large inductor and capacitors. Energy can also be delivered in a "quasi-adiabatic" way, which is defined as a process where the supply voltage changes in discrete steps and energy loss is permitted to a certain extent. Therefore, the quasi-adiabatic driving technique theoretically has non-zero losses. In both cases, the nomenclature is used to indicate that such driving techniques produce better efficiency figures than conventional driving at a fixed supply voltage. In this thesis, an energy-efficient current mode stimulator circuit is designed

which can drive a wide range of electrode-tissue interface impedance to achieve neural stimulation. The main contributions are listed below.

- A quasi-adiabatic driving technique is proposed to improve the overall efficiency of the current mode stimulator.
- A dynamic high voltage supply (DHVS) is designed to implement the proposed-quasi-adiabatic driving technique, using ON Semiconductor's 0.5μm CMOS technology. It can maintain efficiency over 60% for a wide range of load current from 25 μA to 1.4 mA, with a peak efficiency of 67%. It also dynamically changes the output voltage to keep the energy efficiency high.
- A constant current source which can provide a stimulus current from 10 μA to 2.55 mA, with output impedance greater than 2 MΩ is designed. The minimum voltage required across it, to keep the current constant, is only 120 mV.

Chapter 2 gives background on current mode stimulation and describes existing stimulator topologies. In Chapter 3 the overall architecture of the front-end is shown. The design and implementation of the energy-efficient DHVS and the low-voltage headroom current source are discussed in Chapter 4 and 5 respectively. Simulation results from Cadence Spectre are shown in Chapter 6. Chapter 6 concludes this thesis and suggests possible future works.

Chapter 2: Overview of Current Mode Stimulator

2.1. Background on Current Mode Stimulation

Many state-of-the-art stimulation systems today are designed to drive current-regulated biphasic stimulus with constant current amplitude. A conceptual current stimulator circuit and the applied current stimulus is shown in Fig. 2.1. Referring to Fig. 2.1(a) two electrodes are named as "active" (E_{ACTIVE}) and "return" (E_{RETURN}).

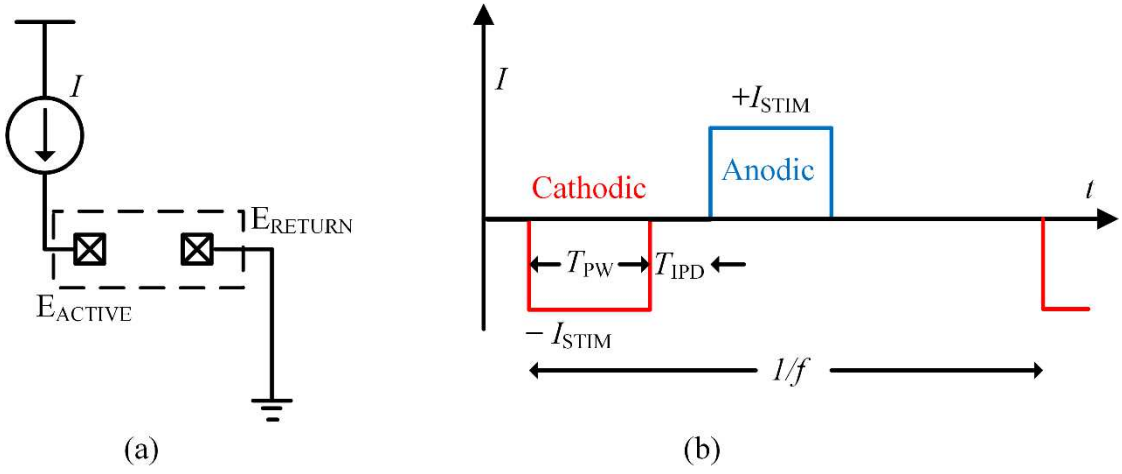

Fig. 2.1 (a) A conceptual current mode stimulator (b) Current stimulus waveform

A biphasic stimulus has two phases. Typically the current of the leading phase (or cathodic phase) is negative (sourced out of the "return" electrode), in order to depolarize the neurons near the active electrode [22], while the current of the balancing phase (or anodic phase) is positive (sourced out of the "active" electrode), and of equal amplitude and duration of the leading phase, as to make the stimulus charge-balanced. The current stimulus is shown Fig. 2.1. There is a delay between the two phases called the inter-phase delay (T_{IPD}). The key parameters of such stimulus are thus the pulse-

width (T_{PW}), pulse amplitude (I_{STIM}), and the pulse frequency (f). Depending on stimulation application and electrode, these stimulus parameters may vary significantly. However, generally, stimulus amplitude falls between 10 μA and 10 mA, pulse-width between 10 μs and 1 ms, and the pulse frequency below 130 Hz.

The voltage across the active and return electrode is dependent on the electrode-tissue interface impedance, and hence it is essential to know the model of the impedance. The equivalent circuit model of an electrode-electrolyte interface comprises an interface capacitance impedance C_D, shunted by a charge transfer resistance R_{CT}, together in series with the solution resistance R_S (resistance measured between "active" and "return" electrode) [23]. This model is shown in Fig. 2.2. Impedance between active and return eletrodes within the neural tissue can be modeled as Fig. 2.2(a).

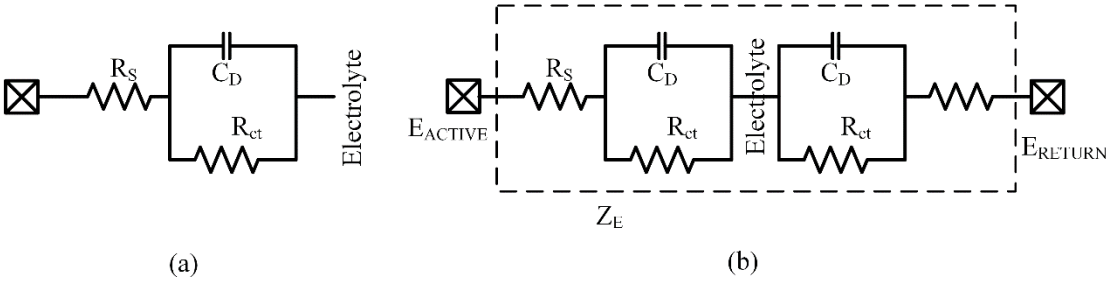

Fig. 2.2 (a) Equivalent circuit model of the electrode-electrolyte interface, (b) Equivalent impedance across active and return electrode

In the literature pertaining to the design of nerural interfacing electronics (e.g., neural recording and stimulation systems) [24], the electrode-electrode interface impedance, Z_E, is often modeled as a series R-C element as the value of R_{CT} is very high [23]. From Fig. 2.2(b), neglecting R_{ct} we get

$$Z_E \approx 2R_S + \frac{2}{sC_D}. \tag{2.1}$$

The voltage profile across the electrode-tissue interface and the applied biphasic current stimulus are shown Fig. 2.3.

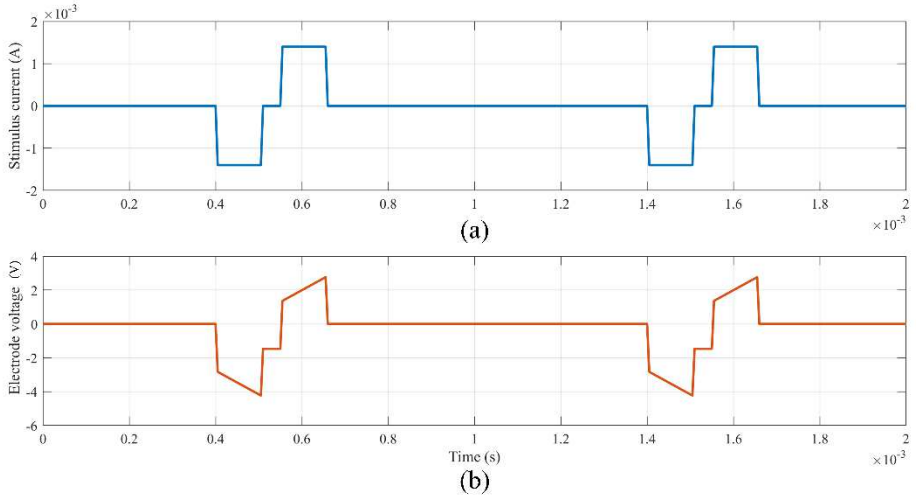

Fig. 2.3 (a) Applied biphasic current stimulus, (b) Voltage profile across the active and return electrode; $I_{STIM} = 1.4\ mA$, $R_S = 2\ k\Omega$, $C_D = 100\ nF$

Using the simplified linear R-C model, the maximum voltage observed across Z_E can be found as:

$$V_C = 2I_{STIM}R_S + 2\frac{I_{STIM}T_{PW}}{C_D}, \tag{2.2}$$

where T_{PW} is the width of each stimulus phase. V_C is defined as the voltage compliance required for the stimulator. The amount of chrage delivered at the end of the cathodic stimulus is $Q_{STIM} = I_{STIM} \cdot T_{PW}$. Although the parameters of the applied stimulus may vary widely across neural stimulation applications, when a bi-phasic stimulus with sufficuent amplitude and pulse-width is applled, high bipolar voltages (i.e., $> \pm 10\ V$)

may be observed across the active and return electrode due to the impedance presented by Z_E. Furthermore, Z_E has been observed to change significantly during in-vivo operation and after prolonged use [23, 22]. Accordingly, a robust and practical neural stimulation system not only requires high voltage compliance but also performance invariant to the frequency-dependent chracteristics of Z_E.

To achieve said performance electrical neural stimulation systems have been implemented across a wide range of technologies with varying levels of integration [25, 24]. Due to small form-factor and compatibility with low power design, single-chip CMOS solutions are advantageous to the development of neurostimulators, and the stimulator also can be integrated with the neural recording interface and biomarker detector processor. The aforementioned high-voltage compliance needed by practical neural stimulators presents significant barriers for implementation in a modern, low-voltage CMOS technology, since the terminal-to-terminal voltages of a transistor must be kept within a small window (e.g., $1\,V$, $2.5\,V$, $3.3\,V$); these limits are established by the foundary (TSMC, IBM, AMI etc.) to prevent device faliure and to ensure reliable operation over time. As a result, many neural stimulator integrated circuits published to date are constrainted in voltage compliance by these foundary ratings (e.g., A stimulator chip utilizing VDD-rated devices typically has a maximum voltage compliance of $\pm VDD/2$ [25, 21]).

Therefore, leveraging the form-factor and cost benefits afforded by the CMOS integration (which could enable the development of smaller and more sophisticated neural interfaces) lies in opposition to the implementation of practical neural stimulation systems. The front-end stimulator, designed in this thesis, can be used to drive a

constant-current biphasic stimulus, with voltage compliance decoupled from the VDD-rating of the transistors while maintaining high energy efficiency. The voltage compliance is restricted by the voltage limitations imposed by more voltage tolerant stuctures like metal-to-metal capacitors, the reverse breakdwon voltage of p-substrate-to-deep-n-well junction and the gate-oxide breakdown voltage.

2.2. State-of-the-art in High-voltage Compliant Stimulators

High-voltage compliant current mode stimulators implemented with low-voltage CMOS have been explored in [24, 26, 27, 28]. Said designs have two main components. First, the high voltage supply, HVDD, which supplies the stimulus current, is generated on-chip using a DC-DC converter. Second, a specialized stimulator front-end is used to interface HVDD with current sources and/or active and return electrodes, to drive a charge-balanced, current-regulated stimulus. Here we discuss current stimulators, explored in the literature until now; they can be divided into three categories, and they are described below.

2.2.1. Ground-return Front-end Topology

The most commonly used front-end topology for current-regulated neural stimulators is referred to as the "ground-return" topology. In this topology, current sources of both "source" and "sink" polarity can be connected to an active electrode via switches, and the return electrode is connected to a low-impedance node, which is typically at half of the supply potential. Fig. 2.4 illustrates the operation of the ground-

return front-end topology when delivering a biphasic, constant-current stimulus. During the cathodic phase, the active electrode sinks the I_{STIM} current and in the anodic phase the same amount of current is sourced out of the active electrode.

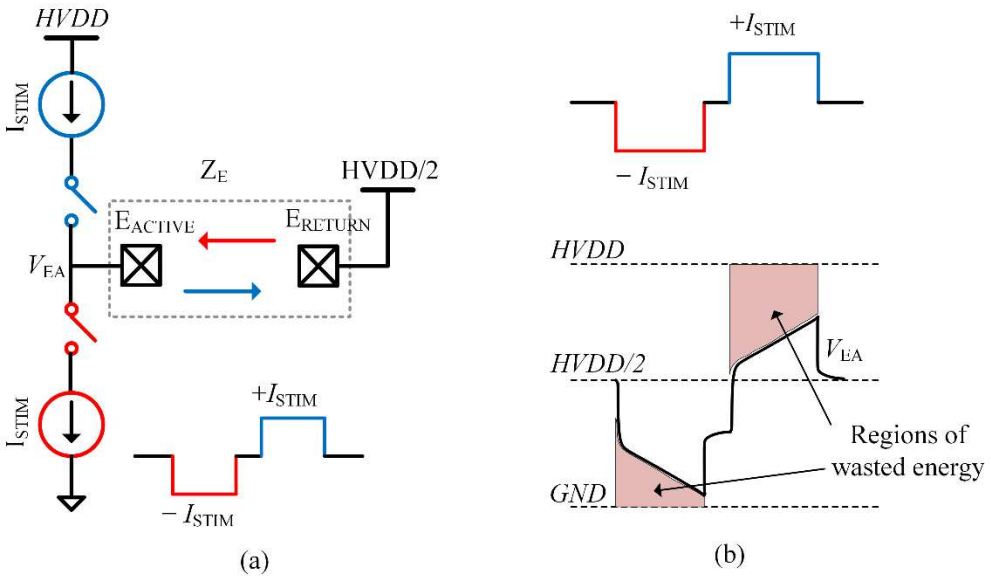

Fig. 2.4 (a) Operation of a ground-return front-end topology, (b) Potential at the active electrode terminal

As shown in Fig. 2.4(a) two voltage supplies, $HVDD$ and $HVDD/2$ are required for the ground-return stimulator front-end. If a dual-supply system with $+VDD$ and $-VDD$ is used, the return potential is held at ground. The ground-return front-end is often employed in neural stimulation systems featuring a high-channel count (such as retinal prosthesis), with each active electrode having dedicated source/sink regulation and a single common return electrode shared by all active/return electrode pairs [24, 29, 30, 31, 32].

As explained in Section 0 the impedance between the active and return electrodes can be simplified as a series R-C model. Under this approximation, the

waveform of the active electrode potential during stimulus delivery, V_{EA} is shown Fig. 2.4(b) and ithe voltage difference across active and return electrodes can vary between $\pm HVDD/2$. Accordingly, if the standard switch and current source designs were to be used in the front-end circuit, HVDD would be constrained to VDD and the resulting bipolar compliance would be slightly less than $\pm VDD/2$ since each current source will have non-zero saturation voltage.

However, by using stacking I/O transistors in implementing the switches, a ground-return front-end design featuring twice the typical compliance has been demonstrated in 65 nm bulk CMOS [24]. Further extending HVDD relative to VDD using the same technique that is in [24] will make the resulting circuit increasingly complex, if not impractical. Regarding high-voltage operation, another drawback of this topology is that it requires two power supplies that must be generated and regulated.

Fig. 2.4(b) also shows the energy wasted due to a fixed supply voltage. During the cathodic phase, the shaded region shows the voltage drop across the "sinking" current source and during the anodic phase the shaded region shows the voltage across the "sourcing" current source. It is evident a significant amount of energy is getting wasted across the current sources; this problem exacerbates if the electrode-electrode interface impedance is low and the stimulator circuit still operates at HVDD. This is an inherent drawback of a current-mode stimulator. If a current stimulus with $I_{STIM} = 0.7\,mA$, $T_{PW} = 100\,\mu S$, and $f = 1\,kHz$ is used in a ground return front-end with $HVDD = 10\,V$ and Z_E is approximated as a $2\,k\Omega$ resistor and a $50\,nF$ capacitor in series, then 504 µW power is wasted and efficiency of the stimulator is estimated to be only 28%.

2.2.2. *Differential Front-End Topology*

In a current-regulated stimulator employing a "differential" front-end topology, matched current sources of opposite source/sink polarity are simultaneously connected to the active/return electrode, via switches, to deliver a charge-balanced stimulus. Operation of the differential front-end topology when delivering biphasic, constant-current stimulus is illustrated in Fig. 2.5.

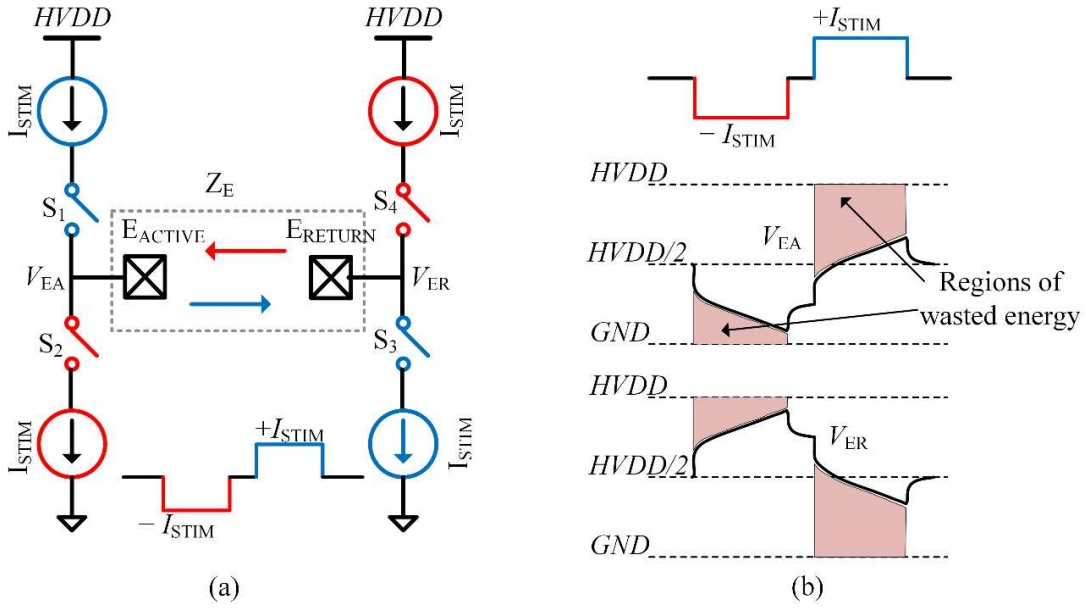

Fig. 2.5 (a) Operation of a differential stimulator circuit, (b) Potential of the active and return electrode terminals

Referring to Fig. 2.5(a), during the cathodic phase (marked by red color) S_1 and S_3 are ON. Thus the active electrode sinks a current with a magnitude of I_{STIM}. After a inter-phase delay period, S_2 and S_4 turn ON and the return electrode sinks the same amount of current for the same time period. In this way, a charge-balanced stimulus is delivered to the neural tissue between the electrodes.

If both current sources are well matched, and the electronics interfacing with each electrode have the same input impedance from their perspective, an equal and opposite (i.e., differential) voltage variation should be observed at the active and return electrode terminals during stimulus delivery. Accordingly, like other differential circuits, the common-mode of the front-end must be set; specifically, both electrodes need to be set to half of the supply voltage before stimulus delivery is commenced for the voltage compliance of the stimulator to be maximized. A distinct advantage provided by this topology is in stimulation systems employing multiple differential front-ends; a charge-balanced stimulus can be simultaneously delivered to multiple active and return electrode pairs as long as the total source and sink currents, at a given time, are well balanced.

As shown in Fig. 2.5(b), during stimulus delivery the voltages at both the active and return electrode terminals, denoted by V_{EA} and V_{ER}, can vary between HVDD and ground. If the standard switch and current source designs were to be used, HVDD would be constrained to VDD and the resulting bipolar voltage compliance would be slightly less than $\pm VDD$ (due to the non-zero saturation voltage of the current sources). Therefore, a standard differential front-end can achieve approximately twice the intrinsic voltage compliance of a ground-return stimulator topology. In Fig. 2.5(b) the energy wasted across the current sources is shown in the shaded region and energy efficiency for this topology is similar to the ground-return front end. If a current stimulus with $I_{STIM} = 1.4\ mA$, $T_{PW} = 100\ \mu S$, and $f = 1\ kHz$ is used in a diffential front-end with $HVDD = 10\ V$ and Z_E is approximated as a $2\ k\Omega$ resistor and a $50\ nF$ capacitor in

series, then 2016 μW power is wasted and efficiency of the stimulator is calculated to be 28%.

The stimulation system featured in [26] demonstrates approximately $\pm 6\,V$ compliance using $1\,V$ and $2.5\,V$ devices in 65nm CMOS technology. The stimulator is only demonstrated with a very capacitve looking Z_E, resulting in relaxed dV/dt at both electrodes during stimulation. The closed loop technique employed to quasi-adiabetically set the effective HVDD, may not be able to reliably operate with resistive Z_E.

With a differential front-end, a high degree of balance is required between the source and sink current sources as well as the impedance seen by each current source to ensure fully differential operation and prevent unpredictable common-mode variation at the electrodes.

2.2.3. H-Bridge Front-end Topology

In delivering a charge-balanced stimulus, an "H-bridge" front-end only employs current regulation of a single polarity (source or sink) and alternates the electrode (active or return) current source is interfacing while the other electrode is connected to a low-impedance node at an adequate voltage to keep the current regulation from dropping out. The operation of a sink-regulated H-bridge front-end topology is illustrated in Fig. 2.6(a).

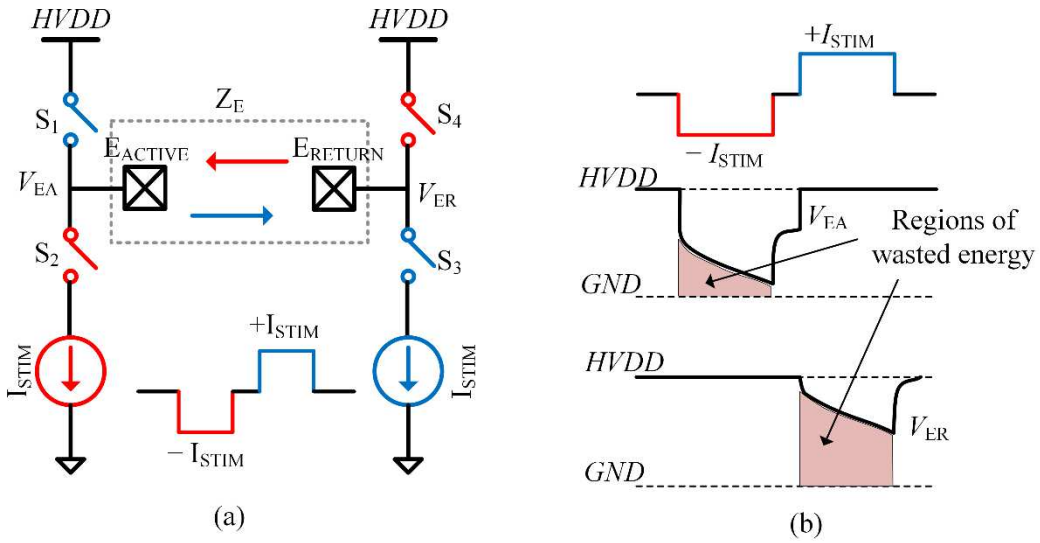

Fig. 2.6 (a) Operation of an H-bridge stimulator circuit, (b) Potential of the active and return electrode terminals

Referring to Fig. 2.6(a), in the cathodic phase S_1 and S_3 switches are ON, thus the return electrode is connected to HVDD and the active electrode sinks the stimulus current of magnitude I_{STIM}. During the anodic phase S_2 and S_4 are turned ON and the return electrode the same amount of current while the active electrode gets connected to HVDD. If the standard switch and current source designs were to be used in the illustrated front-end circuit, HVDD would be constrained to VDD and the resulting bipolar voltage compliance would be slightly less than $\pm VDD$.

Regarding the efficiency of the H-bridge topology, it is similar to the other current mode stimulators, since the area of the shaded region in Fig. 2.6(b) is almost the same as the ground-return and differential front-end structures. If a current stimulus with $I_{STIM} = 0.7\,mA$, $T_{PW} = 100\,\mu S$, and $f = 1\,kHz$ is used in a H-bridge front-end circuit with $HVDD = 10\,V$ and Z_E is approximated as a $2\,k\Omega$ resistor and a $50\,nF$

capacitor in series, then 2016 μW power is wasted across the current source and efficiency of the stimulator is estimated to be 28%.

A sink-regulated H-bridge front-end provides advantages in a high-voltage compliant stimulation system since only sink current regulation is required. Therefore, some of the most problematic high-voltage implementation challenges associated with other front-end topologies (i.e., designing source-regulating circuits that can float with HVDD, be controlled by VDD supply voltage) can be bypassed.

An H-bridge current stimulator was reported in [27, 28, 32, 33, 34]. The stimulator featured in [32] is approximately $\pm 11\,V$ compliant and implemented using 2.5 V 65nm CMOS process technology. An H-bridge front-end provides additional advantages with respect to stimulator performance and CMOS implementation. As shown in Fig. 2.6(a), only one sink-regulating current source is used at a time. Therefore, a single current source could be used to deliver an entire biphasic stimulus waveform; such a design could be potentially leveraged to provide improved charge-balance performance. Secondly, unlike a ground-return stimulator, the H-bridge front-end employs only one power supply (HVDD).

However, an H-bridge front-end also has its performance limitations. With regard to a sink-regulated H-bridge (Fig. 2.6), the active/return electrode is only directly connected to current regulated electronics during the cathodic/anodic phase of the stimulus. Accordingly, with a stimulation system employing multiple H-bridge front-end modules, each interfacing with an electrode (each module being a switch to sinking current source and switch to HVDD), a charge-balanced stimulus can only be reliably driven between a single active-return electrode pair at a time. Nevertheless, this

performance restriction does not prohibitively limit the potential uses of a stimulator employing H-bridge topology, since there are many neural stimulation applications that do not require simultaneous, multi-channel stimulus delivery (such as DBS). Furthermore, even some high channel-count stimulation systems employing ground-return front-ends (which could potentially stimulate multiple active electrodes simultaneously) are controlled in a manner that makes it only a single active electrode can be stimulated at a time [29].

Much more problematic than the inability to simultaneously stimulate through multiple channels is the performance of a bulk CMOS implemented, H-bridge front-end when Z_E looks capacitive, as illustrated in Fig. 2.7.

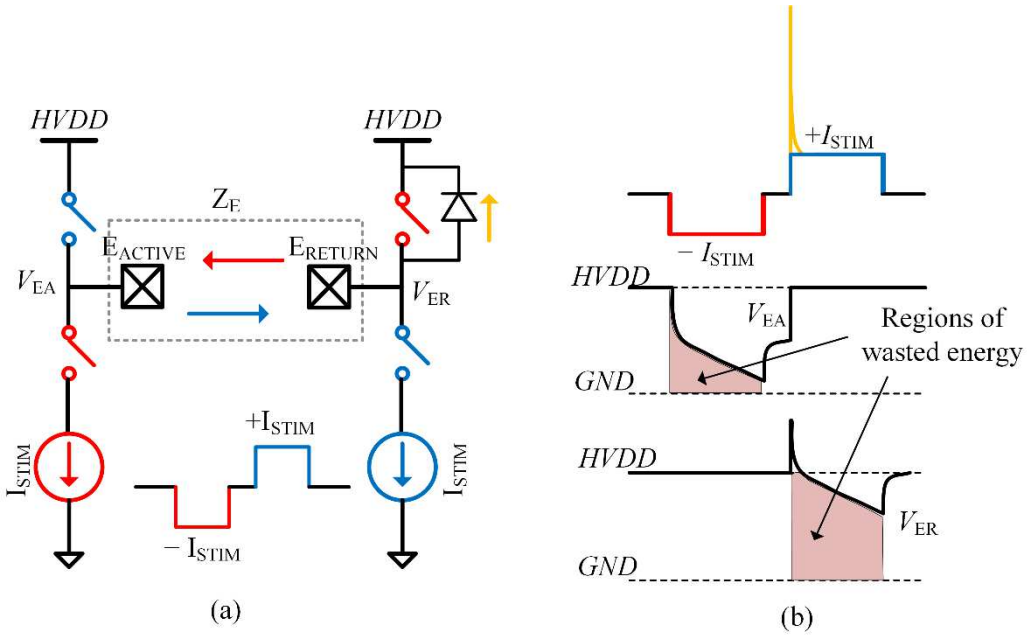

Fig. 2.7 Unpredictable and unreliable performance of H-bridge front-end stimulator for when Z_E stores charge

If Z_E holds a voltage through the interphase delay of stimulus delivery, the voltage exerted on the front-end electronics by an electrode will exceed HVDD. Considering the CMOS devices that would be used to implement the high-side switch, this supra-HVDD voltage, if large enough, would likely forward bias an internal p-n junction e.g., drain to body junction of a pMOS device. The other side of the forward biased junction would be at HVDD, and, therefore, active and return electrodes would be effectively shorted, resulting in high, unregulted current through the tissue. If HVDD is at its maximum possible voltage for a given process (as to maximize the voltage compliance of the stimulator), then a voltage exceeding HVDD could overstress the front-end electronics, or exceed the reverse breakdown voltage of a parasitic junction which would also result in unregulated current though the tissue. Accordingly, the H-bridge front-end shown in Fig. 2.6 can only be used to deliver a stimulus to a resistive electrode or to electrodes for which resistive impedance dominates.

To alleviate the problem discussed above an improved charge delivery method for the H-bridge front-end and its integrated circuit implementation will be discussed in the following chapters. A new high-voltage supply is proposed which helps to eliminate the inherent drawback of low power efficiency of a current stimulator.

Chapter 3: Architecture of the Front-end Stimulator

As discussed in the previous chapter, a stimulator employing an H-bridge front-end has demonstrated the ability to achieve high voltage compliance [27, 28, 32, 34] with less complex integrated circuit implementation. In this section an after review of existing energy-efficient H-bridge stimulators, a new H-bridge stimulator circuit is presented which i) is compatible with low-voltage CMOS integration and can achieve state-of-the-art voltage compliance, and ii) performs invariantly to the resistive/capacitive characteristics of the electrode-electrode interface impedance. The issue of inherent low energy efficiency of current mode stimulators is also addressed by i) using an adaptive driving voltage, which varies with the voltage profile of the electrode-electrode interface, and ii) recycling the charges accumulated from the stimulation phase for use in the balancing phase.

3.1. Topology Concepts

3.1.1. Overview of Existing Energy Efficient H-bridge Stimulators

The unaddressed problem with a standard H-bridge stimulator topology is its compatibility with a wide range of electrode-tissue interface impedances; specifically, capacitive looking impedances that may hold a significant voltage through the interphase delay of the biphasic stimulus. This compatibility issue stems from the fact that current delivery has two complementary phases, during which a single supply (HVDD) is used.

This issue could be potentially resolved if the electrode-tissue interface voltage could be assured close to $0\,V$ before an H-bridge driver uses HVDD to supply the balancing stimulus current. A passive way to achieve this functionality would be to extend the interphase delay as long as it needs to be, to allow Z_E to self-discharge. However, as many Z_E models referenced in the literature are a resistor and capacitor in series, it would be difficult to predict how long self-discharge may take. Futhermore, Z_E is, in reality, a non-linear impedance which can change over time [22, 23]. Considering that it is typically desired to keep the interphase delay as short as possible, having its duration dependent on a time-constant, which is electrode-dependent, time-varying, and only models the behavior of a non-linear impedance, is most likely not an acceptable solution.

Alternatively, the discharge of Z_E can be forced through active means; specifically by using the anodic stimulus, as shown in Fig. 3.1.

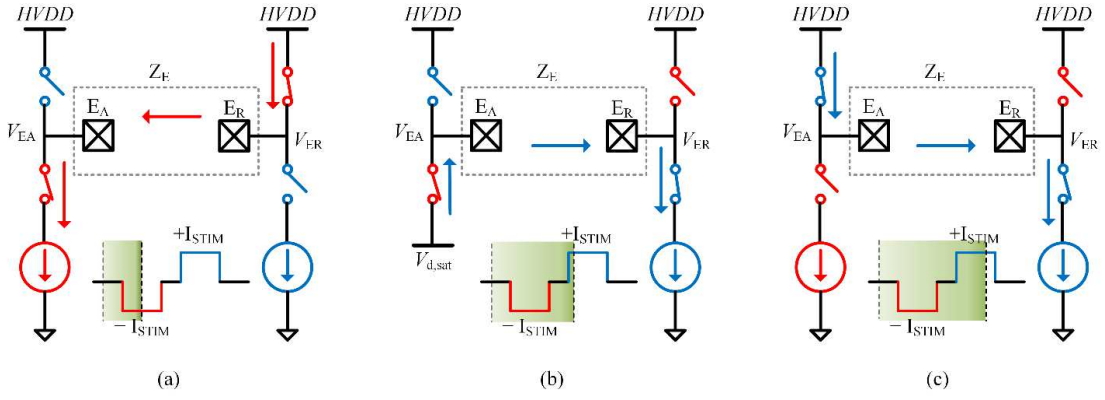

Fig. 3.1 Operation modes of the modified H-bridge stimulator circuit (a) cathodic phase, (b) first subphase of the anodic phase, (c) second subphase of the anodic phase

In Fig. 3.1(a) the cathodic pulse is driven through Z_E the same way as with a typical sink-regulated H-bridge. In this initial configuration, HVDD is connected to the return electrode, and a sinking current source, with a dropout voltage of $V_{d,sat}(< 250\ mV)$, regulates I_{STIM} though Z_E. Then after the interphase delay, anodic stimulus delivery is broken into two sub-phases. During the first sub-phase (Fig. 3.1(b)), a low-voltage power rail approximately equal to the current source drop out voltage $V_{d,sat}$, is connected to the active electrode and Z_E is discharged via I_{STIM}. As a result, voltage across Z_E is brought down to $0\ V$ while balancing stimulus is being delivered.

When the voltage across Z_E finally falls to $0\ V$, HVDD is connected to the active electrode, resulting in continued delivery of the anodic stimulus to the active electrode. This second sub-phase (Fig. 3.1(c)) configuration is maintained for the remainder of the balacing phase. For this way of stimulus delivery, the potential of each electrode (V_{EA}, V_{ER}) and voltage difference across them (indicated by V_{EAR}) is shown in Fig. 3.2. The shaded areas indicate the regions of wasted energy. Since, during the second sub-phase no voltage source is connected to the elctrodes, there is no power consumption, instead previously stored charge is recycled. This is another advantage of this technique. The H-bridge stimulator described in [32] employes this approach and thus has a similar type of energy loss.

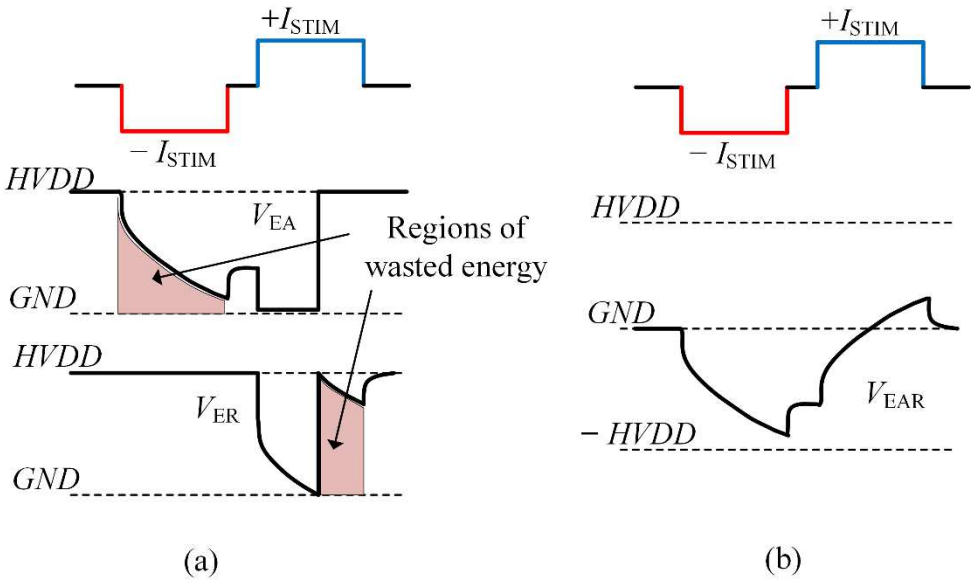

Fig. 3.2 (a) Active and return electrode potential, (b) Voltage difference between the electrodes

Energy consumption can be further reduced by applying an adaptive supply voltage. The idea is to provide just enough voltage to track the voltage across the electrodes and to keep the transistors inside the current source in saturation. Such a method is known as "adiabatic" driving of electrodes because most of the energy delivered is utilized to drive the electrode-tissue impedance and thus there is very little energy loss. This was first presented in [21]. However, its voltage compliance is only $3.3\,V$. The stimulator can be quasi-adiabatically driven by dividing the HVDD supply into several discrete levels, and such technique is presented in [28, 34]. Nevertheless, in the technique presented in [28, 34], during the first subphase of the anodic phase (charge-recycling period) the active electrode is connected to a DC voltage equivalent to VDD. Thus, a continuous current is being drawn from the power supply, and this will reduce the overall efficiency of the stimulator. Moreover, in [28] voltage compliance in

only $\pm 3.3\ V$ and the $HVDD = 3.3\ V$ is obtained from an off-chip power supply. In [34] the minimum voltage headroom required for the current source is not low, and thus the effective voltage compliance is reduced.

3.1.2. Proposed Stimulus Delivery Technique

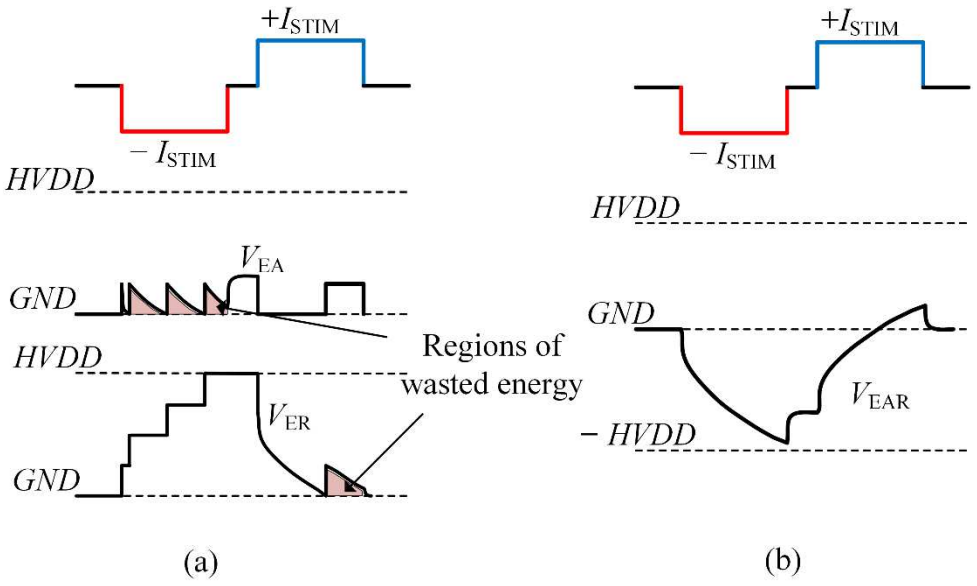

Fig. 3.3 A quasi-adiabatic neural stimulator (a) active and return electrode potential, (b) voltage difference across the electrode

Fig. 3.3 shows the waveforms of the electrode potential and the energy consumption for the proposed driving technique. Previously (Fig. 3.2), during the cathodic phase potential of the return electrode was fixed at HVDD. Now, a dynamic voltage supply is used to provide four discrete voltages, and the supply voltage is increased by a step when the current source goes to the edge of saturation. If the saturation voltage of the current source is denoted as $V_{d,sat}$, during the cathodic phase when V_{EA} is less than or equal to $V_{d,sat}$, V_{ER} is incremented to the next step. During the first-subphase of the anodic phase charge stored in the electrode capacitance is recycled

and when the return electrode potential reaches $V_{d,sat}$, V_{EA} is increased. One more advantage of this technique is that the voltage across the current source, when it is connected to the "active" electrode, never exceeds $HVDD/N$, where N is the number of discrete and equal levels in HVDD. Thus, the need for a high-voltage interfacing circuit for the current source, as decribed in [27, 32], no longer remains and design of the stimulator circuit is simplified.

To find out a quantitive measure of efficiency improvement let us consider such stimulator circuit where $HVDD = 10\ V$ is divided in five equal steps of $2\ V$. If a current stimulus with $I_{STIM} = 0.7\ mA$, $T_{PW} = 100\ \mu S$, and $f = 1\ kHz$ is used and Z_E is approximated as a $2\ k\Omega$ resistor and a $25\ nF$ capacitor in series, then only 218 µW power is wasted across the current source and efficiency of the stimulator is estimated to be 80%. Thus 50% improvement of the power efficiency can be achieved.

In this design, we propose an energy efficient neurostimulator circuit with on-chip dynamic high-voltage and a low voltage headroom (i.e., saturation voltage) current source.

3.2. Building Blocks of the Proposed Stimulator

A high-level architecture of the front-end current stimulator, to implement the technique described above, is shown in Fig. 3.4. Two most important building blocks for this design are a dynamic high voltage scaling (DHVS) block and a constant current source. The electrode-electrode impedance being driven is shown by the dotted box. We will consider a simplified series R-C model for this impedance.

A brief description of the building blocks is given next.

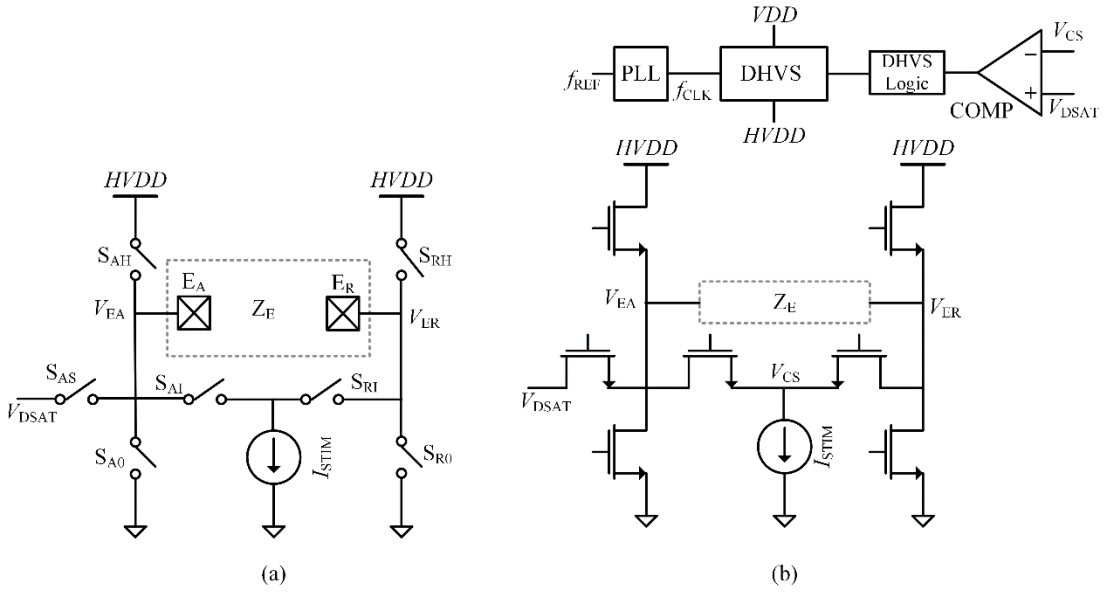

Fig. 3.4 High-level architecture of the designed H-bridge stimulator circuit (a) general implementation, (b) implementation with transistors

3.2.1. Dynamic High Voltage Scaling (DHVS)

The DHVS is the most critical block of the stimulator. A DHVS is used to supply stimulus current across a voltage range of 0 to HVDD. The DHVS can be designed to provide N discrete levels of voltages. A high frequency clock is required as an input to operate the DHVS circuit. A DHVS circuit is designed here to have a voltage compliance of 15 V while providing a stimulus current of 2.5 mA. The output voltage of the DHVS is denoted as HVDD.

3.2.2. Current Source

The current source provides a constant stimulus current through the neural tissue. As the voltage across the current source varies throughout the stimulation cycle, a minimum voltage headroom is required across it for providing a constant current.

Thus, the dropout voltage of the current source should be small, and the output impedance should be very high. This dropout voltage or minimum allowed output voltage is defined as V_{DSAT}.

A current source is designed here to provide stimulus current in the range of 10 µA to 2.55 mA. The output current is controlled by an 8-bit digital input. The design complexity of the current source is less as the maximum voltage across it, is VDD instead of HVDD. This is due to applying a quasi-adiabatic driving technique and can be observed in Fig. 3.3(a).

3.2.3. Frequency Synthesizer

To maintain high efficiency throughout a wide range of load current, the DHVS requires a variable frequency clock. A divide-by-N PLL can be used to synthesize several different clock frequencies from an input clock. There is an industrial, scientific and medical (ISM) radio band centered around 13.56 MHz, which will serve as the reference frequency signal.

3.2.4. Switches and Comparator

There are seven switches in the front-end circuit for delivering a charge-balanced stimulus. There are two high side switches: S_{AH}, S_{RH}, four low side switches S_{A0}, S_{R0}, S_{AI}, S_{RI} and another switch for charge recycling S_{AS}. A comparator is required to prevent the current source from going below its minimum allowed output voltage.

3.3. Stimulation State-Cycle

The configuration of the front-end stimulator circuit throughout delivering a biphasic current stimulus is shown in Fig. 3.5. Description of various states at different points within a stimulation period is given below.

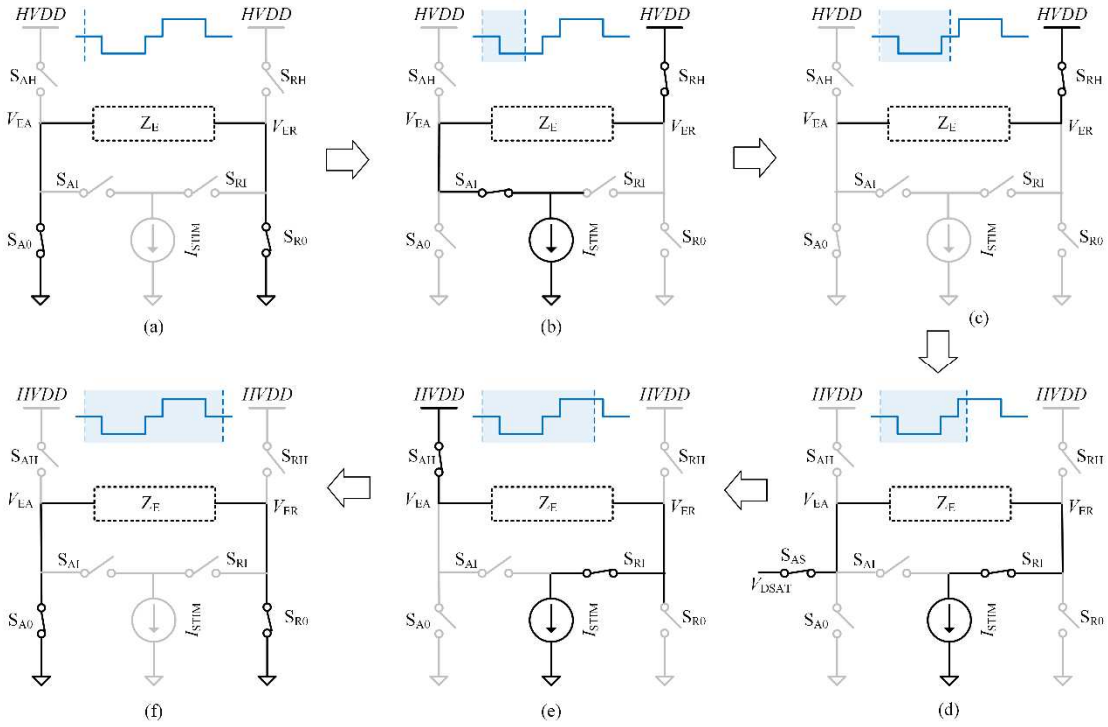

Fig. 3.5 State-cycle of the front-end stimulator circuit for implementing the quasi-adiabatic driving technique described in Section 0 (a) state 1: idle, (b) state 2: negative stimulus delivery, (c) state 3: interphase delay period, (d) state 4: positive stimulus delivery with charge recycling, (e) state 5: positive stimulus delivery using power supply, (f) state 6: residual charge discharge

3.3.1. State 1: Idle

Before the stimulus delivery is commenced, both electrodes are shorted to the chip ground by switch S_{A0} and S_{R0}. Both the DHVS and the current source are disabled. Hence the power consumption in this state is zero.

3.3.2. State 2: Negative stimulus delivery

In the cathodic phase, negative stimulus current is delivered to the neural tissue near the "active" electrode by closing the switch S_{RH} and S_{AI}. The voltage across the "active" and "return" electrode will continuously decrease as long as the negative current is delivered.

The output voltage of the current source is compared with a fixed low voltage V_{SET} to prevent it from failing to maintain a constant current delivery. When the voltage across the current source drops below V_{DSAT}, DHVS voltage is increased by one VDD step. If the "return" electrode voltage is observed, it will look like a staircase signal as shown in Fig. 3.3(a).

3.3.3. State 3: Interphase delay

After a negative stimulus delivered, there is a short interphase delay period. In the period the "return" electrode is still connected to DHVS through S_{RH}, and the "active" electrode is kept floating. If the electrode-electrode impedance, Z_E is capacitive, it will hold a charge through this period.

3.3.4. State 4: Positive stimulus via Z_E discharge

After an interphase delay period, positive stimulus current is delivered to the neurons near the "active" electrode to maintain the charge neutrality of the tissue. The anodic phase is divided into two subphases. The first subphase is denoted as State 4. In this state, any remaining charge in the electrode-tissue interface from the interphase delay period is discharged by closing the switches S_{AS} and S_{R1}. This state is continued until the voltage across "active" and "return" electrodes becomes zero. The DHVS is kept idle by disconnecting switch S_{AH} and S_{RH}. If Z_E is purely resistive, there is no voltage stored in the electrode-tisse interface and therefore this state will be omitted

3.3.5. State 5: Positive stimulus via current source

In this state, positive stimulus current delivery is continued by connecting the "active" electrode to HVDD through S_{AH}. The switch S_{AS} is disconnected. The stimulus delivery is continued until a charge balance is achieved. The DHVS output voltage will be increased by a step if the voltage across the current source drops below V_{DSAT}.

3.3.6. State 6: Z_E discharge

After a charge-balanced stimulus is delivered, both electrodes are shorted together by closing the switches S_{A0} and S_{R0}. In this way, if any voltage remaining due transistor mismatch or circuit nonlinearity will be forced to discharge through the internal charge transfer resistance R_{CT}.

The design of a power-efficient DHVS and a low-voltage headroom current source to implement the proposed stimulus delivery technique is shown in Chapter 4 and 5.

Chapter 4: Dynamic High-Voltage Scaling & Supply

For the CMOS stimulator front-end to have high-voltage compliance, the dynamic voltage supply of the system must be able to generate the high-voltage using the low-voltage CMOS device. Charge-pump and voltage-doubler circuits have been previously developed, in a variety of CMOS compatible topologies, to safely generate voltage, exceeding VDD (i.e., the terminal to terminal voltage rating of the implementing transistors) on-chip [35, 36, 37]. Such circuits rely on switched-capacitor operation and are based on a single-stage circuit, which can boost the output voltage with respect to the input by a voltage less than or equal to VDD. This single-stage circuit is then cascaded to generate a "high" output voltage. Accordingly, the magnitude of the terminal-to-terminal voltages in each stage is kept within foundry-defined device limit, while the voltage burden with respect to the chip ground, which increases with the number of cascade stages, is placed on the more voltage tolerant structures like metal-insulator-metal (MiM) and/or metal-oxide-metal (MoM) capacitors.

A dynamic high-voltage supply (DHVS) is required to provide a constant load current. Therefore, while generating a high voltage, such a circuit is also required to move significant charge across a potential gradient. One way to generate high-voltage and meet the requirement of providing a constant load current is to use charge pump circuits. CMOS charge pumps have been widely used in flash memories, EEPROMs, DRAMs, SRAMs to generate a voltage higher than the available supply voltage [37].

In this chapter analysis of a conventional charge pump is shown first. Then the design of a new charge pump circuit to be used in the front-end stimulator is shown, and

the designed circuit is compared with the conventional charge pump. Several such designed charge pump circuit is cascaded to build the dynamic high voltage scaling and supply block.

4.1. Overview of a Conventional Charge Pump Circuit

A power efficient charge pump with consideration of gate-oxide reliability was developed in [35, 36]. The schematic of the circuit is shown in Fig. 4.1.

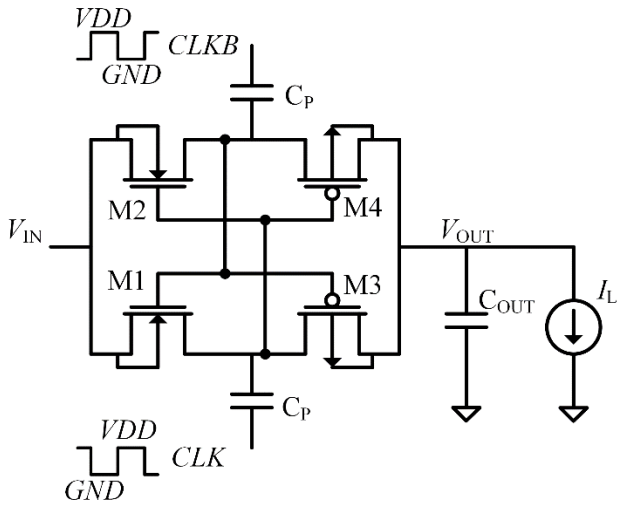

Fig. 4.1 Schematic of a conventional charge pump

This circuit can effectively double the input voltage, so it is also called a voltage doubler. The charge pump circuit uses triple-n-well nMOS transistors, and the body terminals of the MOSFETs are "locally" referenced to V_{IN} and V_{OUT}; thus the terminal-to-terminal voltage never exceeds VDD. Another advantage of this circuit is that multiple stages can be cascaded to generate a voltage equal to several multiples of VDD. The voltage burden is only placed on the pumping capacitors, C_P and the reverse biased p-substrate-to-deep-n-well junction.

The principles of operation and sources of power loss in the conventional charge pump circuit are described in the following sub-sections.

4.1.1. Principle of Operation

The charge pump circuit as shown in Fig. 4.1 is driven by two complementary pulses CLK and CLKB. Assuming the transistors, when these gate-driving signals are applied, function as ideal switches with negligible ON-resistance, the operation of the Fig. 4.1 circuit can be represented by Fig. 4.2. We will analyze the operation of the circuit when it reaches steady state. Steady state is defined when the average output voltage can be treated as a DC with a small ripple in it.

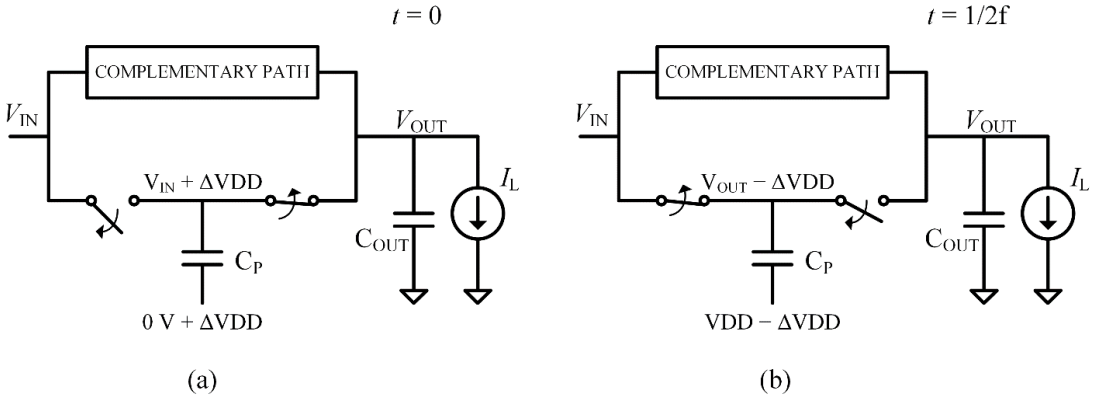

Fig. 4.2 Simplified operation model of a single-stage voltage-doubler circuit at (a) rising and (b) falling CLK pulse edge

In steady state, the gates of M1 and M3 (M2 and M4) are driven by a DC level shifted version of CLKB (CLK). Fig. 4.2(a) shows that the bottom plate of C_P is driven by the rising pulse edge at $t = 0$ and the same change appears at the top plate. At the same time the switches connecting the top plate of C_P to V_{IN} and V_{OUT} open and close respectively. After the C_P top plate voltage is driven upwards (to a voltage greater than

V_{OUT}) the charge sharing between C_P and C_{OUT} forces the C_P top plate voltage to equalize with V_{OUT} (if $C_{OUT} \gg C_P$). The source of this charge-sharing current is the voltage source providing the CLK signal. The voltage stored across C_P decreases during the charge sharing, and this lost charge is either stored in C_{OUT} (boosting the output voltage) or is used to offset the load current I_L. The amount of charge stored across C_P in this half-cycle is $Q_1 = C_P(V_{OUT} - V_{DD})$.

One half-clock cycle later the bottom plate of C_P is driven back down to $0\,V$, while at the same time switches connecting the C_P top plate to V_{IN} and V_{OUT} close and open respectively (as shown in Fig. 4.2(b)). If thme charge sharing during the previous half-cycle resulted in charge loss on C_P, V_{IN} will recharge C_P back to $Q_2 = C_P V_{IN}$.

The difference in the charge stored across C_P in these two half-cycles accounts for delivering the load current. Considering the charge delivered by C_P in the complementary path, I_L can be expressed as

$$I_L = 2C_P\left(V_{IN} - V_{OUT} + V_{DD}\right) f\,, \tag{4.1}$$

where f is the frequency of CLK. From this equation steady-state V_{OUT} can be derived as

$$V_{OUT} = V_{IN} + V_{DD} - \frac{I_L}{2fC_P}\,. \tag{4.2}$$

The open-circuit voltage of the single-stage circuit is $V_{IN} + V_{DD}$; accordingly if $V_{IN} = V_{DD}$, the circuit can double the input voltage under the absence of any load.

Now consider a circuit consisting of "N" voltage doubler circuits cascaded as shown in Fig. 4.3. Keeping the same assumption to describe the operation of the aforementioned circuit output voltage of this multi-stage charge pump can be derived as

$$V_{OUT} = V_{IN} + N \cdot V_{DD} - N \cdot \frac{I_L}{2fC_P}. \tag{4.3}$$

If the output is tapped from each stage, such a circuit will satisfy our requirement of a dynamic high-voltage supply.

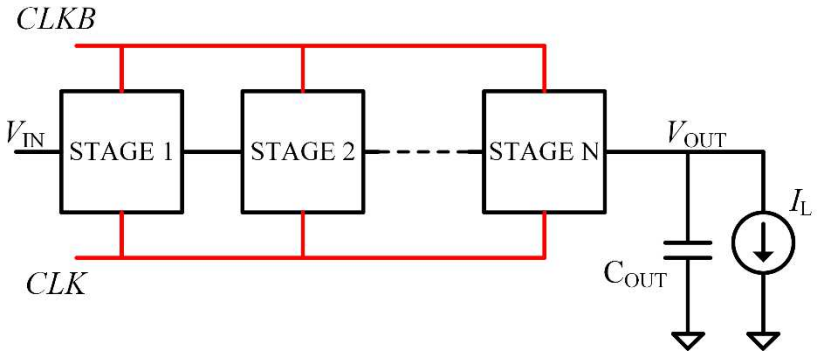

Fig. 4.3 Schematic of a multi-stage charge pump circuit

The output voltage ripple of the charge pump can be qualitatively expressed as

$$\Delta V_{OUT} = \frac{I_L}{2fC_{OUT}}. \tag{4.4}$$

If C_{OUT} is made larger, the output voltage can be treated as an average DC, which assumption is used while describing the operation of the circuit. The rise-time is another important performance metric. The charge-pump circuit in [35] demonstrates rise-time of approximately 1 μs when clocked at 100 MHz which is fast enough for the desired application. From a power supply perspective, a voltage doubler topology is capable of

providing the steady-state and transient performance required of a DHVS for the neural stimulator.

4.1.2. Power Loss in the Charge Pump Circuit

The power efficiency of the DHVS is critical for the design of an efficient current stimulator. We will discuss various sources of power loss in the charge pump circuit in this subsection.

Input power for the charge pump is comprised of the power drawn from the V_{IN} source and the power drawn from the VDD source in the CLK and CLKB driver. Hence ideally, input power is, $P_{IN} = V_{IN}I_L + NV_{DD}I_L$ and the efficiency can be express as,

$$\eta = \frac{V_{OUT}I_L}{P_{IN}} = \frac{V_{IN}I_L + N \cdot V_{DD}I_L - N \cdot \frac{I_L^2}{2fC_P}}{V_{IN}I_L + N \cdot V_{DD}I_L}. \tag{4.5}$$

If the parasitic capacitances at the top and bottom plate of the pumping capacitors are accounted for, a large discrepancy may be found in the value of V_{OUT} and efficiency obtained from the above expresssion. The origin of the top-plate parasitic capacitances is the MOSFET parasitics and the bottom-plate parasitic capacitance comprised of the intrinsic bottom-plate parasitic of the capacitor structure and the capacitance associated with the digital buffer driving the pumping capacitors. In an improved model for evaluating the output voltage and efficiency, the parasitic capacitances at the top and bottom plate can be lumped as C_{TP} and C_{BP} respectively. With these parasitics taken into account, the output voltage deviates from the ideal value and can be evaluated to be

$$V_{OUT} = V_{IN} + N\left(\frac{C_P}{C_P + C_{TP}}\right)V_{DD} - N \cdot \frac{I_L}{2f\left(C_P + C_{TP}\right)}. \tag{4.6}$$

There is also switching loss associated with the parasitic capacitances. The input power can be calculated as

$$P_{IN} = V_{IN}I_L + N\left(\frac{C_P}{C_P + C_{TP}}\right)V_{DD}I_L + 2N\left(C_{BP} + \frac{C_P C_{TP}}{C_P + C_{TP}}\right)V_{DD}^2 f\,. \tag{4.7}$$

Finally, the efficiency can be found to be

$$\eta = \frac{V_{IN}I_L + N\left(\frac{C_P}{C_P + C_{TP}}\right)V_{DD}I_L - N \cdot \frac{I_L^2}{2f\left(C_P + C_{TP}\right)}}{V_{IN}I_L + N\left(\frac{C_P}{C_P + C_{TP}}\right)V_{DD}I_L + 2N\left(C_{BP} + \frac{C_P C_{TP}}{C_P + C_{TP}}\right)V_{DD}^2 f}. \tag{4.8}$$

The output voltage and efficiency drops as the load current, I_L increases. At light load, switching losses becomes dominant and efficiency decreases. As the number of stages are increased, the peak efficiency of the charge pump drops.

In the Fig. 4.4. the variation of efficiency with load current is shown for a five-stage charge pump circuit. The parameters used to plot this curve are $V_{IN} = 2.5\,V$, $V_{DD} = 3\,V$, $f = 25\,MHz$, $C_P = 24\,pF$, $C_{TP} = 0.4\,pF$, and $C_{BP} = 0.8\,pF$. Maximum efficiency of 69% is observed at 0.7 mA of load current.

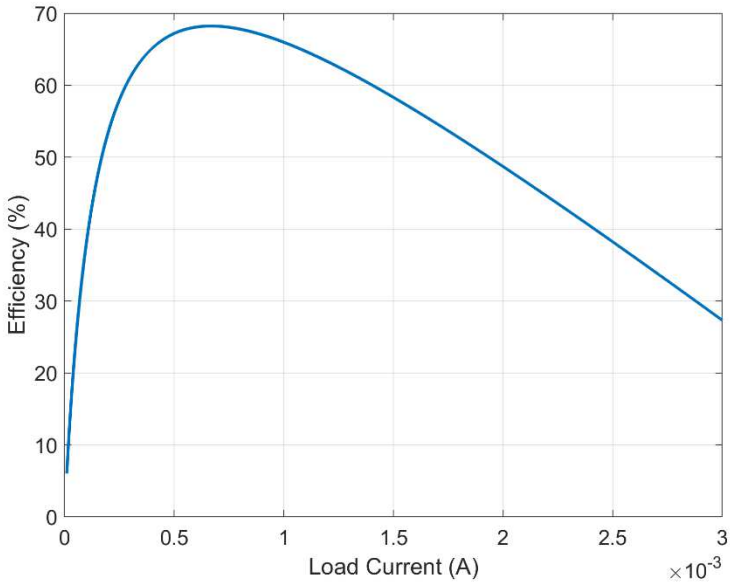

Fig. 4.4 Variation of efficiency with load current in a five-stage conventional charge pump circuit

Apart from the switching loss associated with the parasitic capacitances, various other type of losses are also present depending on the timing of the control CLK signal, and they are responsible for deviation of the output voltage from the calculated value. These sources of losses are described in [38] in detail. If CLK and CLKB are matched (i.e., their rising and falling edge appears at the same time instant and vice versa) three types of power losses are observed: i) pumping loss, ii) output loss, and iii) short-circuit loss. When the CLK signal goes high boosting cation at the top-plate of C_P starts before M1 becomes fully OFF; this is the reason of pumping loss. Similarly when the CLK becomes low charging of C_P begins before M3 turns off and this results in output loss. Short-circuit loss happens during the transition of the control clock when M1 and M3 turn on simultaneously. In the complementary path also these losses occur. The situation exacerbates when the timing of CLK and CLKB are not matched.

To eliminate these losses authors in [38] have used level shifted non-overlapping clocks as the gate signals for the transistors, whereas the pumping capacitors have the previous control clock. Two additional transistors are inserted two prevent the output loss. However, this control scheme requires additional circuitry which may result in additional power loss. We will discuss the design of an efficient charge pump, required in an integrated current neurostimulator, in this regard in the next subsection.

4.2. Design of an Efficient Charge Pump for DHVS

Efficiency is one of the most important aspects while designing a charge pump circuit. Maximum theoretical efficiency is dominated by the output voltage droop caused by the load current. Hence, the voltage droop at the rated load current should be minimized. This droop also depends on the clock frequency and the pumping capacitance. To keep the droop small, the frequency and pumping capacitance need to be large enough. But, high frequency will reduce the efficiency at light load. A pulse frequency modulation scheme might be applied to use a lower frequency under light load condition.

The expression of the output voltage and efficiency obtained in the previous subsection uses the assumption that the M1-4 transistors in Fig. 4.1 can be modeled as ideal switches. In reality, they have finite ON-resistance, and this will cause incomplete charge transfer which will, in turn, reduce the efficiency further. The time-constant in the charge transfer path can be approximated as the product of the MOSFET average ON-resistance and the pumping capacitance. To eliminate the effect of incomplete

charge transfer this time-constant needs to be small compared to half of the switching time period. The pumping capacitance cannot be decreased for keeping the output droop small. Another way to reduce the time-constant is to lower the ON-resistance, and that can be done by increasing the W/L ratio of the transistor. This also results in increased parasitic capacitance which will reduce the efficiency. Therefore, there is an upper limit to increasing the aspect ratio.

The desired charge-pump circuit will have a maximum output voltage of 12 V and can carry up to 3 mA load current. The circuits are implemented in AMI 0.5 µm CMOS technology. Following the optimization technique described above, pumping capacitance is chosen to be 30 pF. The maximum operating frequency of the charge pump is chosen to be 50 MHz to keep the switching loss small.

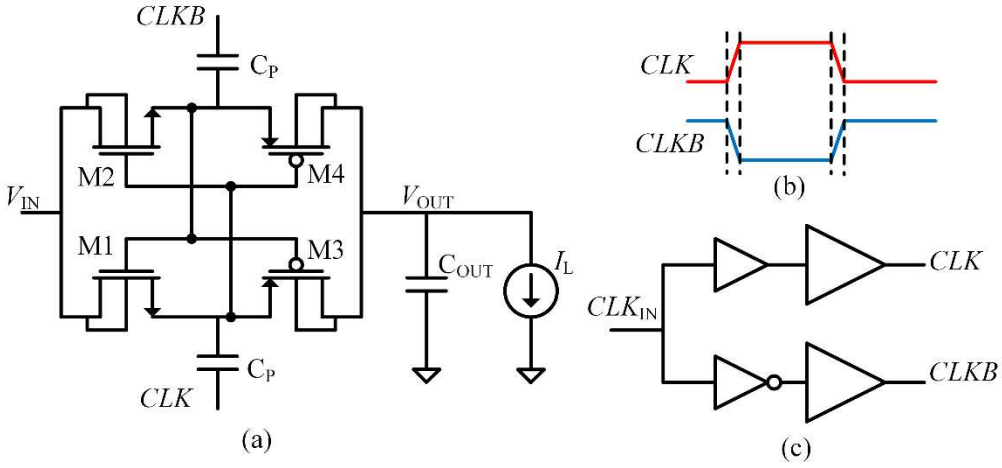

Fig. 4.5 (a) Schematic of the charge pump with overlapping clock, (b) timing diagram of the control signals in OVCP, (c) circuit diagram of the control signal generator

First, we shall show the optimized design of the charge pump circuit with/without non-overlapping gate signal and compare their efficiencies. Next, the design of DHVS circuit will be shown.

In Fig. 4.5 the schematic of a single stage of the charge pump with overlapping gate signals (OVCP) is shown. With $V_{IN} = V_{DD} = 5\ V$, two such stages can be cascaded in series to get an output voltage around 12 V. Mactched overlapping clock signals as shown in Fig. 4.5(b) can be generated from a single input clock, using the digital circuit shown in Fig. 4.5(c). For a single stage charge pump, the average charge delivered by the clock drivers is approximately equal to the load current. Since the rated load current of the charge pump is high, the aspect ratio of the output stage of the driver needs to be large and a therefore a tapered digital buffer structure is used. There is a significant amount of switching loss associated with the parasitic capacitance at the bottom-plate of the pumping capacitor and this is the primary source of efficiency degradation.

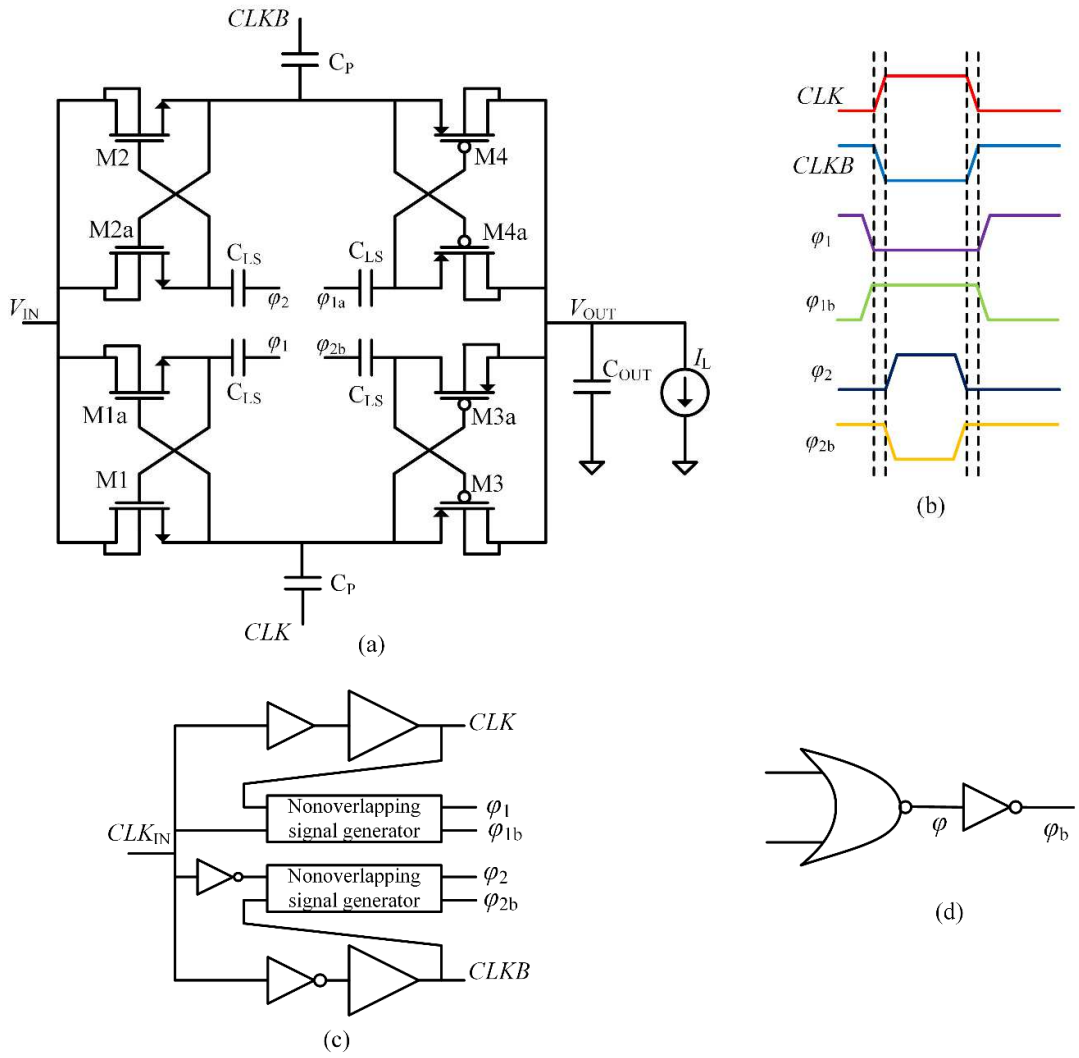

Fig. 4.6 (a) Schematic of the proposed charge pump with non-overlapping clock, (b) timing diagram of the control signals, (c) block diagram of the control signal generator, (d) circuit for generating the non-overlapping control signals

The schematic of the proposed charge pump with non-overlapping control signals (NOCP) is shown in Fig. 4.6(a). The circuit is modified from [38] to remove two additional pMOS transistors in the pumping path whose gate signal generation circuit adds extra switching loss. The auxiliary circuit for level shifting the control signals (φ_1, φ_{1b}, φ_2, φ_{2b}) requires 4 additional transistors and 4 capacitors. Timing diagrams for

these control signals are shown in Fig. 4.6(b) and the digital circuit required for generating them from a single input clock is depicted in Fig. 4.6(c) and Fig. 4.6(d).

Performance of these two charge pump circuits is shown in the next subsection.

4.3. Performance of the designed Charge Pump Circuits

Several charge pump stages can be cascaded to obtain output voltage around 11-12 V. The power loss and efficiency of OVCP and NOCP depend on the number of cascaded stages.

Table 4.1 Comparison of the Designed Charge Pump Circuits

	Stage	**V_{IN}, V_{DD} (V)**	**Load (mA)**	**Freq (MHz)**	**Output Voltage (V)**	**Switching Loss (mW)**	**Eff (%)**
OVCP	2	5	3	50	11.99	17.28	57.75
NOCP					12.12	18.52	57.25
Ideal CP					12.50	0	83.33
OVCP	2	5	2	25	11.55	8.52	59.97
NPCP					11.64	9.2	59.39
Ideal CP					11.67	0	77.78
OVCP	5	3.3	3	50	9.481	6.70	43.03
NOCP					10.67	7.98	47.50
Ideal CP					13.55	0	68.43
OVCP	5	3.3	2	25	9.865	3.33	45.95
NOCP					10.84	4.03	49.69
Ideal CP					11.47	0	59.88

Non-overlapping control signal generation circuitry has a non-negligible amount of switching loss, and thus this charge pump circuit with non-overlapping switching pulses (NOCP) has more power loss. For two cascaded stages, the charge pump circuit

without non-overlapping control signals (OVCP) has higher efficiency. As the number of stages increases the output voltage loss in this topology becomes dominant, and efficiency becomes less compared to NOCP. From Table 4.1, the efficiency of OVCP is 3 - 4% less than that of NOCP. For our current stimulator the DHVS needs to provide 4 to 6 discrete high-voltage levels, and thus an NOCP is a more suitable choice here.

4.4. Design and Performance of Dynamic High Voltage Supply Circuit

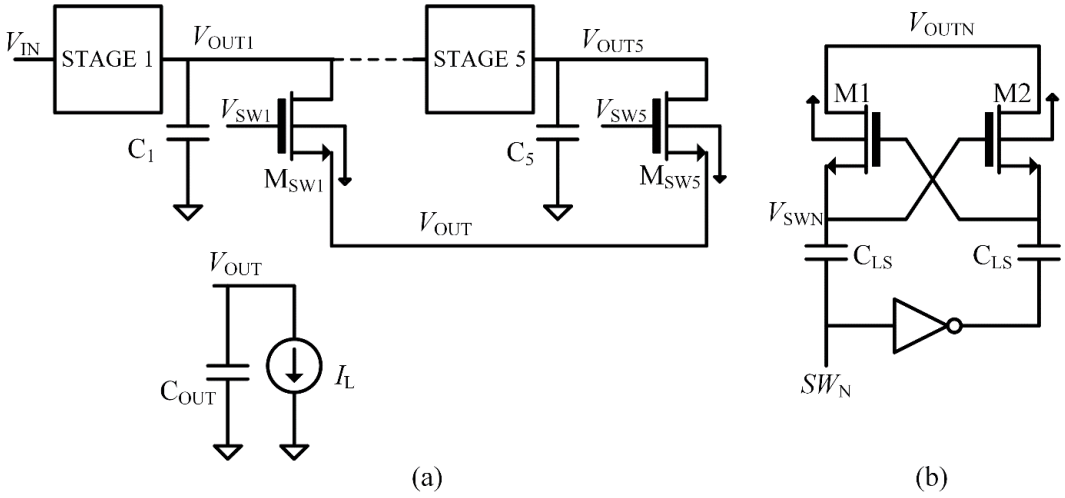

Fig. 4.7 (a) Schematic of the 5 stage dynamic high voltage generation circuit, (b) Schematic of the level shifter required to generate gate signal of the switches $M_{SW1\text{-}SW5}$(the transistor shown here are HV nMOS with thicker gate oxide)

To design the adaptive DHVS, five stages of NOCP are cascaded. A capacitance of 20 pF is connected at the output of each stage. Switches are placed between each stage output and the final output. If nMOS transistors are used as switches, its body terminal needs to be connected to the lowest potential in the circuit, i.e., GND. The

maximum drain-to-source voltage across the transistor switch is HVDD. Therefore HV nMOSs need to be used here.

Fig. 4.7 shows the schematic of the DHVS circuit. To improve the overall efficiency of the stimulator, the final output varies adaptively, as explained in Section 0. Therefore, the gate signals of the switches need to be level shifted accordingly. Fig. 4.7(b) illustrates the schematic of the level shifter required for this purpose. SW_n is the digital switch-control signal for the n-th stage and V_{SWn} is the level shifted version of this with respect to the output voltage of N-th stage. The SW control signal generation circuit is described in Appendix A.

$V_{IN} = 2.5\,V$, and $V_{DD} = 3\,V$ is chosen for the simulation of the DHVS circuit. A typical output voltage profile of the circuit at a load current of 1 mA and switching frequency of 25 MHz, is shown in Fig. 4.8.

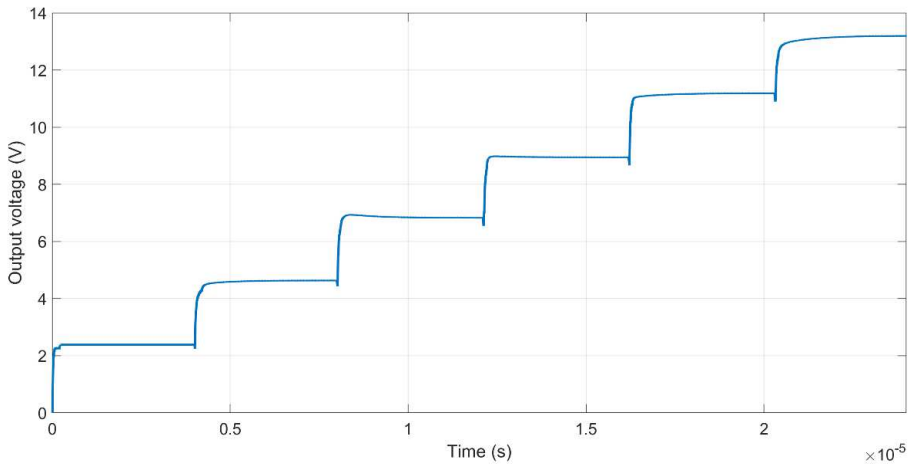

Fig. 4.8 Rise profile of the output voltage of the DHVS circuit

The efficiency of the circuit with the variation of load at six different switching frequencies is shown in Fig. 4.9. Peak efficiency is observed to be 67%. At higher load

current efficiency starts to decrease rapidly. At 3 mA load, current efficiency of the charge pump is 41.5%.

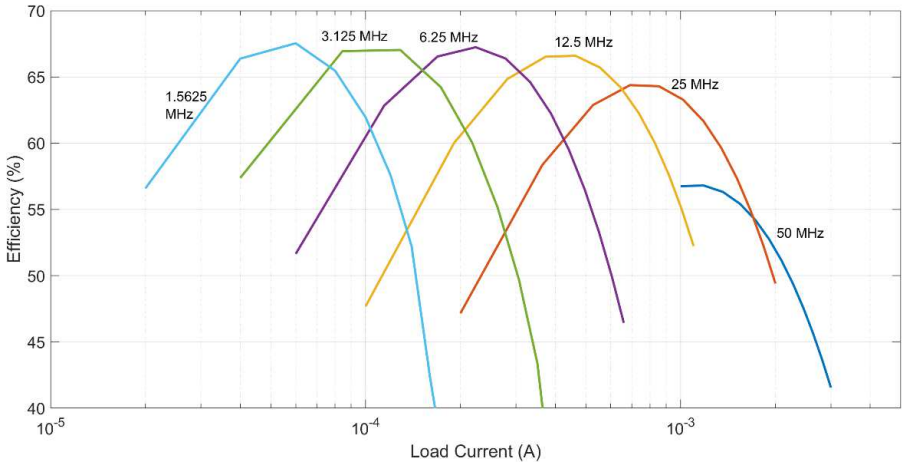

Fig. 4.9 Efficiency variation of the DHVS with load current and switching frequency

To keep the efficiency high for a wide range of load current (20 µA to 3 mA) a pulse frequency modulation (PFM) technique can be applied. Since the stimulator current is programmed digitally, its bits can be used to control the switching frequency. Table 4.2 describes the operating frequency of the charge pump for a particular load current range.

Table 4.2 PFM control strategy

Load Current	**Frequency**	**Determining Bit**
1.28 mA — 2.56 mA	50 MHz	B[7]
640 µA — 1.28 mA	25 MHz	B[6]
320 µA — 640 µA	12.5 MHz	B[5]
80 µA — 320 µA	6.25 MHz	B[4]
80 µA — 160 µA	3.125 MHz	B[3]
10 µA — 80 µA	1.5625 MHZ	

The digital circuit implementation for the PFM is shown in Fig. 4.10. The load current is represented by 8 bits, and the LSB is set to be 10 µA. Thus the maximum programmable load current is 2.55 mA. As shown in Fig. 4.10, the input clock is multiplexed from 6 different clocks. In this simulation, $f_{CLK} = 50\ MHz$ and in this way the power efficiency can be kept above 60% for load current from 25 µA to 1.4 mA.

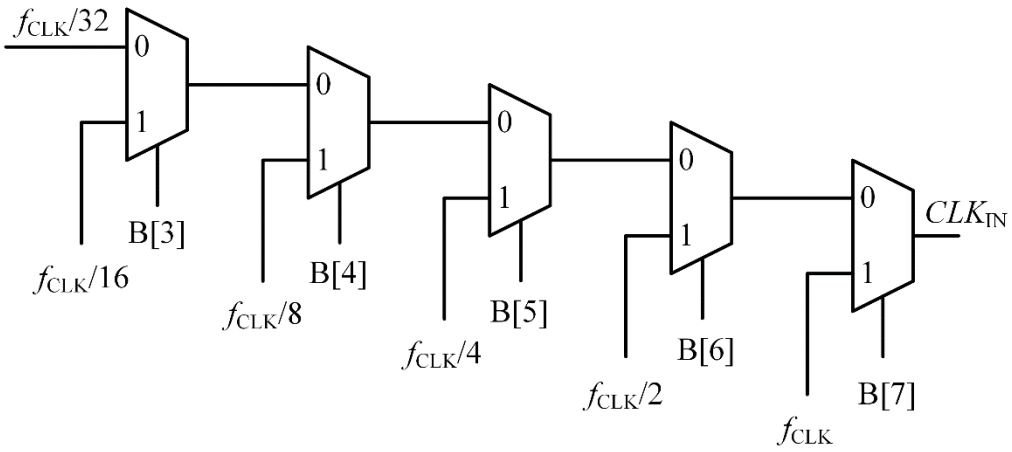

Fig. 4.10 Pulse frequency modulation (PFM) control circuit to enhance efficiency

Table 4.3 State-of-the-art High Voltage Supply Comparison

	[27] JSSC '14	**[26] JSSC '15**	**[32] ESSCIRC '16**	**[39] T. BioCAS '17**	**This Work**
Process	TSMC 0.18µm	TSMC 65nm	TSMC 65nm	0.18µm	AMI 0.5µM
Voltage Compliance	10 V	9 V	11 V	12 V	15 V
Load Current	30 µA	10 — 900 µA	20µA—2.5 mA	0.5 — 3.5 mA	20µA—3mA
# Stages	5	7	8	3	5
Adaptive Voltage	NO	YES	NO	YES	YES
Peak Efficiency	72%	68%	50%	69%	67%

A performance comparison of the designed high voltage supply with existing state-of-the-art current stimulator circuits is shown in Table 4.3. The peak efficiency of this work is comparable to the existing works, considering that this circuit is designed in 0.5μm CMOS technology which has higher parasitic capacitance. Although the peak efficiency in [27] is 72%, it is designed to deliver a load current of only 30 μA. Efficiency of this DHVS is less than the power supply featured in [39] because it has only three charge pump stages. The relatively higher efficiency the power supply reported in [26] can be explained by use of a switched capacitor DC-DC converter. In the future, the design of a switched-capacitor DC-DC converter can be explored to get better power efficiency.

Chapter 5: Design of the Constant Current Source

The desired specifications of the on-chip current source that is used to generate currents that activate neurons tissue present unique design challenges that must be addressed; namely the current range, output impedance and output voltage. The current stimulator integrated circuit is designed to function as a general purpose stimulator that is capable of being employed in one of the many medical applications that require an implantable stimulator, which may require widely varying levels of stimulator current. This is in contrast to other stimulator chips, which are often designed for a single application, such that they are only required to generate a small range of currents and can be optimized to do so [24, 27]. The output impedance of the current source must be large enough to accurately maintain a constant stimulation current as the stimulation cycle progresses and the voltage across the current source varies. When the electrode-tissue impedance is high, the voltage headroom required to keep a conventional current source in the saturation region increases. Thus, if a stimulator is designed to have voltage compliance of ± 2 to $\pm\ 3\ V$ where techniques described in the previous chapter are not necessary, its voltage compliance gets reduced further. In addition, despite the implementation of various techniques to shrink the circuit size, typical current sources need to be made very large to handle high stimulation currents with low dropout voltage [40].

In the current source designed here, the magnitude of the output current is controlled by eight digital bits B0 to B7, which provide access to 255 programmable levels of output current. The digital input, 1 for the current source is chosen to be the

equivalent of $10\ \mu A$, to deliver a reasonable amount of granularity for stimulation applications that require lower current magnitudes. The maximum deliverable stimulation current corresponding to the highest digital code, 255, is $2.55\ mA$, which is large enough to satisfy most stimulation applications that require high currents. The desired output resistance of the current source was chosen to be greater that $1\ M\Omega$ and the minimum output voltage is limited to approximately $160\ mV$.

5.1. Overview of the Existing Current Sources

A reference current scaled by a binary-weighted current mode digital-to-analog converters (IDAC) and replicated by a current mirror can be used as a current source. The schematic of such a circuit is shown in Fig. 5.1(a).

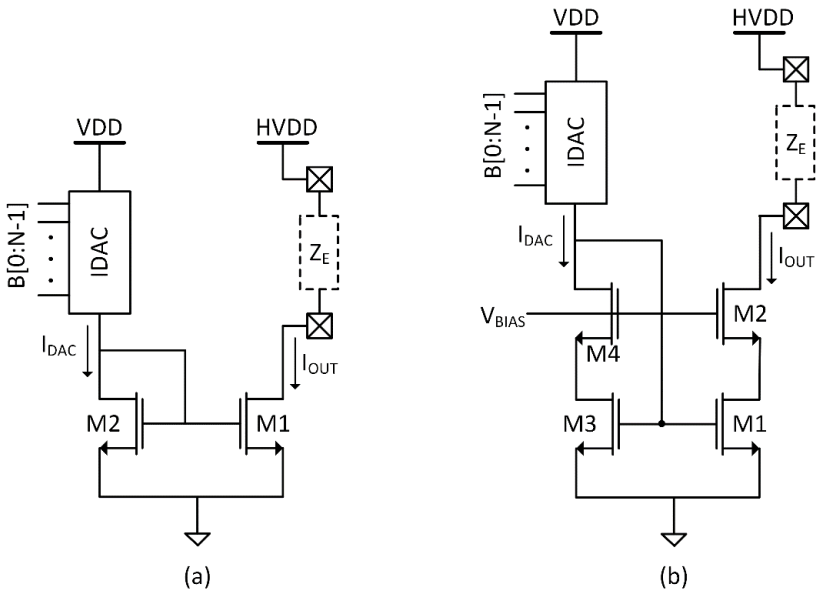

Fig. 5.1 (a) Simple current mirror, (b) Wide swing cascode current mirror; input current is controlled by an N bit current mode DAC

This circuit works properly as long as all transistors are kept in the saturation region, which means they need a minimum voltage of V_{Dsat} across their drain-source terminals. V_{Dsat} is equal to the overdrive voltage of the transistor and is given by,

$$V_{Dsat} = \sqrt{\frac{2I_D}{K_n^{'}(W/L)}} \tag{5.1}$$

where I_D is the drain current, K_n' is the process transconductance and W and L are the transistor width and length. For the stimulator to have high voltage compliance, V_{Dsat} needs to be low. If the stimulator is required to have high stimulus current, a low V_{Dsat} can be maintained by making the aspect ratio of the transistor very large. So this comes at the expense of a large area consumption. If a simple current mirror is used for stimulation, as shown in Fig. 5.1(a), a maximum voltage of $HVDD - V_{Dsat}$ could occur across the electrodes. The output resistance of a simple current mirror is $r_o = 1/\lambda I_D$, where λ is the channel length modulation factor. This resistance is not high enough for neural stimulation application, specially when it decreases at high currents, and causes the stimulus current to vary considerably with output voltage variation.

To improve the output impedance, a cascade configuration is used. A wide swing cascode current mirror is shown in Fig. 5.1(b). In this way, the output resistance can be increased by a factor of $g_{m2}r_{o2}$, where g_{m2} and r_{o2} are the small-signal transconductance and ouput resistance of the cascode transistor M2 respectively. However, the increased output resistance comes at the expense of reduced voltage compliance of $HVDD - 2V_{Dsat}$. Moreover, both M1 and M2 transistors need to have largeW/L ratio.

To solve these problems, a new current source was proposed in [40], and the circuit is shown in Fig. 5.2. In this circuit a voltage controlled resistor (VCR) is used to change the output stimulus current in accordance with the digital input. The voltage controlled resistor is implemented by forcing transistor M1 to operate in deep triode region by the negative feedback of an op-amp. In this way, the drain voltage of M1 is kept at a very low voltage (80 mV). However, cascode transistor M2 needs to be large to have a small overdrive voltage. Nevertheless, the minimum voltage headroom required for this circuit is still less than $2V_{Dsat}$ [40].

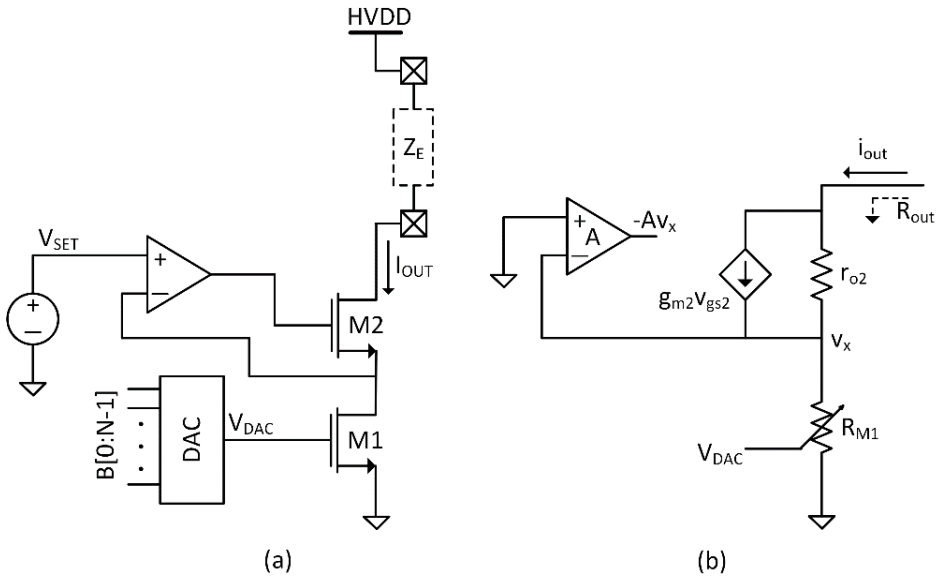

Fig. 5.2 (a) VCR current source proposed in [40], (b) small-signal equivalent circuit of the current source

The output current of this circuit is given by

$$I_{OUT} = K_n' \left(\frac{W}{L}\right)_1 \left(V_{DAC} - V_t - \frac{1}{2}V_{SET}\right) V_{SET} \tag{5.2}$$

M1 operates in the triode mode if $V_{DS1} = V_{SET} < (V_{DAC} - V_t)$. Therefore, smaller V_{SET}, provides a larger voltage compliance and a wider range of V_{DAC} voltages, where M1 stays in the triode region, both of which are desirable. It is also shown that to achieve the same stimulus current level, the aspect ratio of the M1 transistor is considerably smaller than that of the wide swing cascode current source.

The output resistance of the VCR current source can be derived from the small-signal equivalent circuit in Fig. 5.2(b).

$$R_{out} = A g_{m2} r_{o2} R_{M1} \tag{5.3}$$

where A is the open-loop gain of the operational amplifier, g_{m2} and r_{o2} is the small-signal transconductance and output resistance of M2. R_{M1} is the voltage controlled resistance of M1. Since V_{SET} is very small (80 mV), R_{M1} can be written as

$$R_{M1} = \frac{L_1}{K_n' W_1 (V_{DAC} - V_t)}. \tag{5.4}$$

The output resistance of a cascode current source is $g_{m2} r_{o2} r_{o1}$. Therefore if the VCR current source is designed such that $A R_{M1} = r_{o1}$, then its output resistance would be equivalent to that of the cascode current source. In our design R_{M1} has a minimum value of 31.25 Ω (80 mV/2.55 mA). To have a minimum of 1 MΩ output resistance, open-loop gain of the op-amp needs to be higher than 60 dB.

5.2. Implementation of Circuit Components in Current Source

5.2.1. Digital-to-analog Converter

5.2.1.1. Current DAC proposed by Ghovanloo [40]

Fig. 5.3 shows that N-bit current steering DAC, which provides digital control over V_{DAC} in 2^N steps. Thus each steps translates to $I_{REF}R_{DAC}$ V. The minimum step corresponding to the LSB should be greater than V_{SET} to keep the M1 transistor in Fig. 5.2(a) in triode mode. If V_{SET} is 80 mV, $I_{REF}R_{DAC}$ should be at least 120 mV to maintain the linearity in the triode region. For a N-bit digital input V_{DAC} can be express as

$$V_{DAC} = R_{DAC}\left(I_{DAC} + I_{offset}\right) \tag{5.5}$$

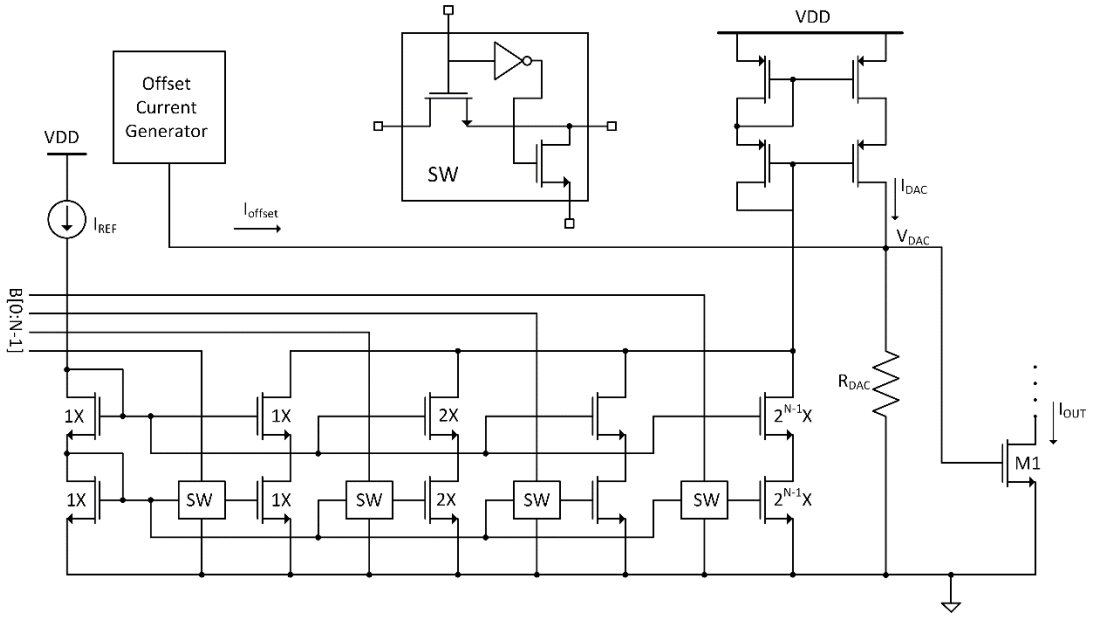

Fig. 5.3 Schematic of an N-bit current steering DAC [40]

An offset current is added to the circuit to cancel out the threshold voltage dependance of I_{OUT}. Ignoring this offset current V_{DAC} can be written as

$$V_{DAC} = R_{DAC} I_{DAC} = R_{DAC} I_{REF} \sum_{0}^{N-1} 2^n B_n \tag{5.6}$$

where, B_n is the n-th bit. Thus the output current can be expressed as,

$$I_{OUT} = g_{m1} R_{DAC} I_{REF} \sum_{0}^{N-1} 2^n B_n \tag{5.7}$$

where, g_{m1} is the transconductance of the M1 transistor.

5.2.1.2. Modified Current DAC

For our design $N = 8$. If the design [40] were to be adopted, the maximum value of V_{DAC} for our application would be $255 I_{REF} R_{DAC}$, which is greater than 30 V. Therefore, it is necessary to modify the design present in [40] to provide a wide range of stimulus current.

In our design the IDAC is divided into two subcircuits, the input of each subcircuit being 4 digital bits. Its schematic is shown in Fig. 5.4. Inputs to the subcircuit "L" (for LSB) are B[0:3], and inputs to the subcircuit "M" (for MSB) are B[4:7]. The final output current can be written as

$$I_{OUT} = g_{m1} R_{DAC} (V_{DAC\_L} + V_{DAC\_M}) = g_{m1} R_{DAC} I_{REF} \left(\sum_{0}^{3} 2^n B_n + \sum_{4}^{7} 2^n B_n \right) \tag{5.8}$$

It is evident from Fig. 5.4 that the DAC always conducts a DC current which will reduce the overall efficiency of the stimulator and this quiescent current depends on the digital input. In subcircuit "L" the maximum quiescent current is $2 \cdot 15 I_{REF} +$

I_{REF} and for subcircuit "M" the maximum quiscent current would be $2 \cdot 240 I_{REF} + I_{REF}$. To reduce this huge power loss in subcircuit "M", the DAC transistors are scaled in the same way as subcircuit "L" and instead M1_M is scaled by 16. Thus, the output current can be written as,

$$I_{OUT} = g_{m1}(V_{DAC\_L} + 16 \cdot V_{DAC\_M}) = g_{m1} R_{DAC} I_{REF} \left(\sum_0^3 2^n B_n + 16 \cdot \sum_4^7 2^{n-3} B_n \right) \quad (5.5)$$

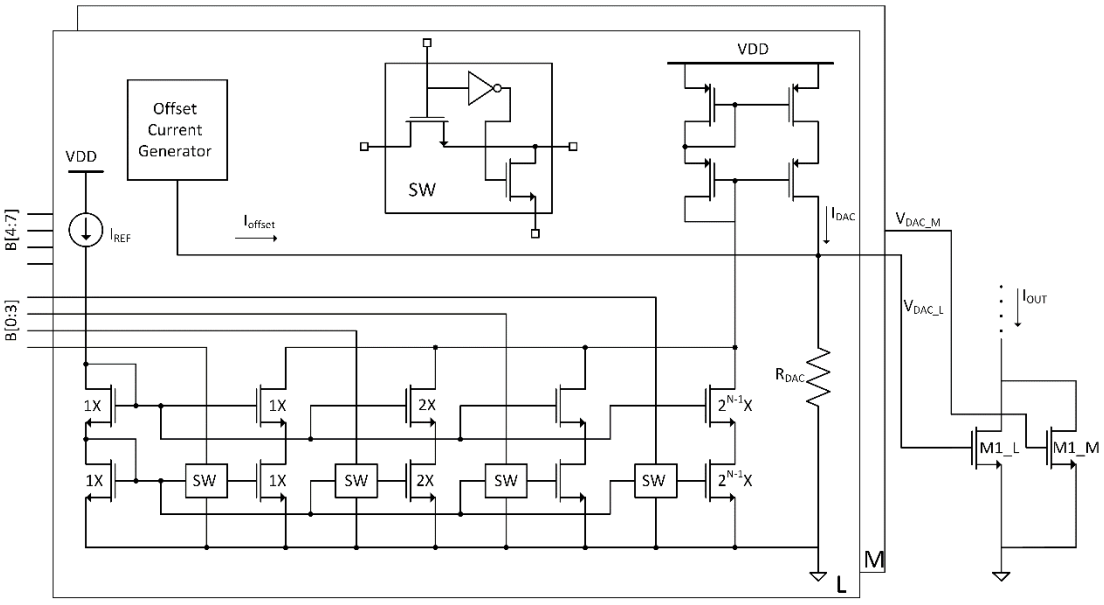

Fig. 5.4 Schematic of the 8-bit energy efficient current steering DAC

Thus schematics of the two subcircuits become the same. Maximum current drawn by the whole current DAC circuit will be $4 \cdot 15 I_{REF} + 2 \cdot I_{REF}$. To make this small, a low reference current needs to be chosen.

5.2.2. Operational Amplifier

The operational amplifier serves two purposes in this design. First, it keeps the M1 drain voltage at V_{SET} and second, it significantly increases the VCR current source

output resistance. The bandwidth of the op-amp is not a large concern, as inputs are not connected to any high frequency AC signals and the rise time of the output voltage of the current source is relatively slow due to the time it takes the DHVS to ramp up HVDD. The op-amp should also consume low current and area.

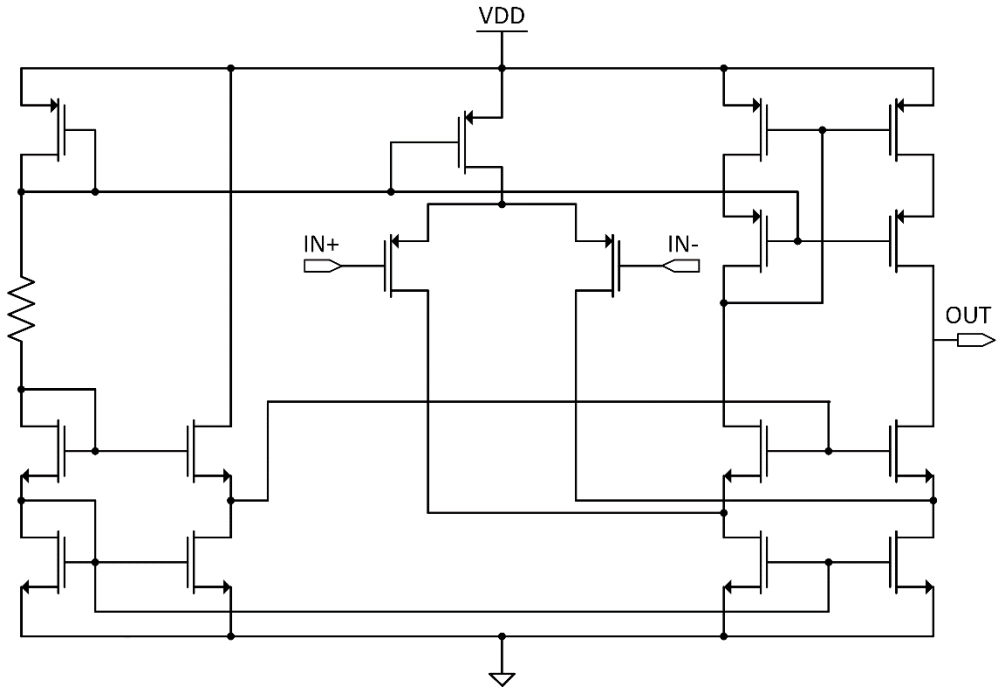

Fig. 5.5 Schematic of the operational amplifier with biasing circuit

A folded cascode op-amp is chosen as the topology for the feedback path amplifier. The output of the op-amp is connected to a large capacitive load due to the sizeable cascode transistor required to pass the high stimulus current, so a two-stage op-amp is not a good design choice. Stability concerns would arise due to the low-frequency pole created by the capacitive load. A folded cascode op-amp can achieve high gains in just a single stage and at small common mode input voltages while also maintaining a satisfactory phase margin [41]. Input transistors of the amplifier need to be pMOS as the input voltages are less than the threshold voltage of a transistor.

The schematic of the folded cascode op-amp is shown in Fig. 5.5. Simulation results show it can provide 68 dB open loop gain at $V_{SET} = 80\ mV$ common mode input, which is enough for our design. The designed amplifier draws only 4.3 μA DC current.

5.2.3. Current Source Linearity

It is important to have a linear voltage to current relationship in the VCR current source. For $0 < V_{DAC} < V_t$, M1 in Fig. 5.2(a) is off. If an offset current is added to I_{DAC} which produces a voltage equal to V_t across the resistor R_{DAC}, V_{DAC} corresponding to the zero digital input is set to $V_{DAC}(0) = V_t$. For $V_t < V_{DAC} < V_t + V_{SET}$, transistor M1 goes to saturation. If V_{SET} is made less than the single DAC voltage step, this region is avoided. For $V_{DAC} > V_t + V_{SET}$, M1 operates in triode region which is intended. The output current, I_{OUT} is given by (5.2). To cancel the non-linearity produced by the $0.5 \cdot V_{SET}$ term, it is better to make the single DAC step close to $2 \cdot V_{SET}$. For large V_{DAC} it is observed that the output current is less than the expected value. The main reason for this nonlineaity arises from carrier mobility degradation due to the high vertical electric field set by the large gate-body potential in M1 [40]. The effective carrier mobility is given by

$$\mu_{\text{eff}} = \frac{\mu_0}{1+\theta(V_{DAC}-V_t)} \approx \mu_0\left(1-\theta\cdot(V_{DAC}-V_t)\right) \tag{5.10}$$

where μ_0 is the low-field mobility and θ is the mobility degradation factor.

In our design the drain voltage of M1 is fixed to V_{SET} by the negative feedback of op-amp. So we need to linearize I_{OUT} with respect to V_{DAC}. Using the Taylor series appoximation in (5.10), the output current is written as

$$I_{OUT} = K_{no}^{'}\left(\frac{W}{L}\right)_1 (V_{DAC} - V_t) V_{SET} \times (1 - \theta(V_{DAC} - V_t)) \tag{5.11}$$

where $K_{n0}' = \mu_0 C_{ox}$. To cancel the second order term of V_{DAC} another transistor M1_1 is added in parallel to M1 and a gate voltage of $k_1 \cdot V_{DAC}$ is provided to it [40] such that M1_1 remains in saturation. Thus, the output current becomes

$$I_{OUT} = K_{no}^{'}\left(\frac{W}{L}\right)_1 (V_{DAC} - V_t) V_{SET} \times (1 - \theta(V_{DAC} - V_t)) + \frac{1}{2} K_{no}^{'}\left(\frac{W}{L}\right)_{1\_1} (k_1 V_{DAC} - V_t)^2 \tag{5.12}$$

To achieve a linear equation in terms of V_{DAC}, the coefficient of V_{DAC}^2 should be zero. Under this condition

$$k_1 = \sqrt{\frac{2(W/L)_1}{(W/L)_{1\_1}} \theta V_{SET}} \tag{5.13}$$

Although (5.13) provides an analytical guideline to estimate the size of M1_1, and the gate voltage ratio k_1, it has several limitations. First, the Taylor series approxmation is only valid when V_{DAC} stays close to V_t and second, the transistor M1_1 stays in saturation only in a certain segment of V_{DAC} as the drain voltage is very small (equal to V_{SET}).

A more practical approach to overcome these limitations is to use (5.13) to get an initial estimate of k_1 and aspect ratio of M1_1. Then simulation tool is used to fine-tune a linear relationship between I_{OUT} and V_{DAC}. When M1_1 goes out of saturation another transistor M1_2 with a gate-voltage of $k_2 \cdot V_{DAC}$ is added in parallel. Then the upper segment of I_{OUT}-V_{DAC} curve can be linearized. To linearize the output current for

the whole range of V_{DAC} three such transistors are added in parallel to M1. The schematic of the circuit is shown in Fig. 5.6.

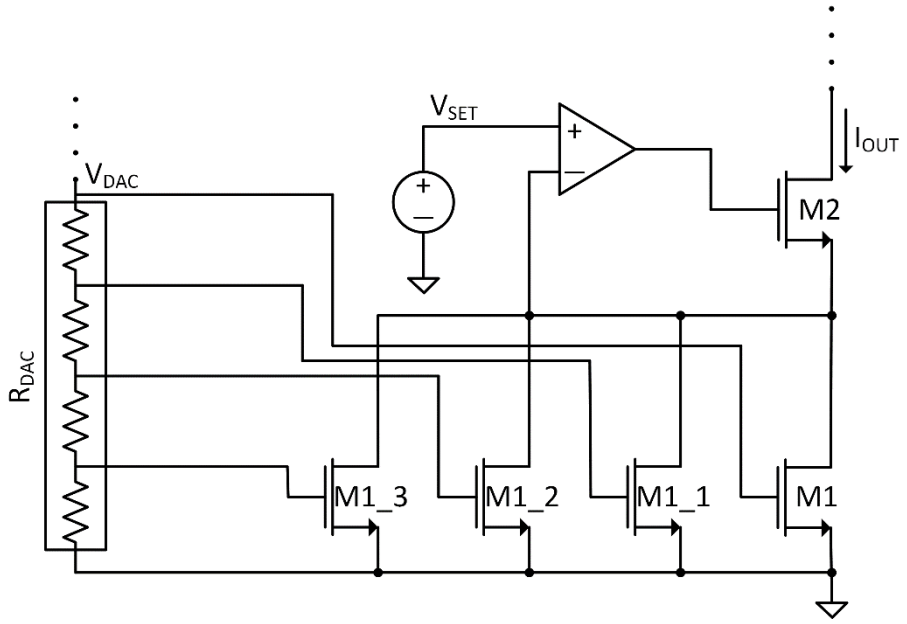

Fig. 5.6 Schematic of the circuit to linearize the output current

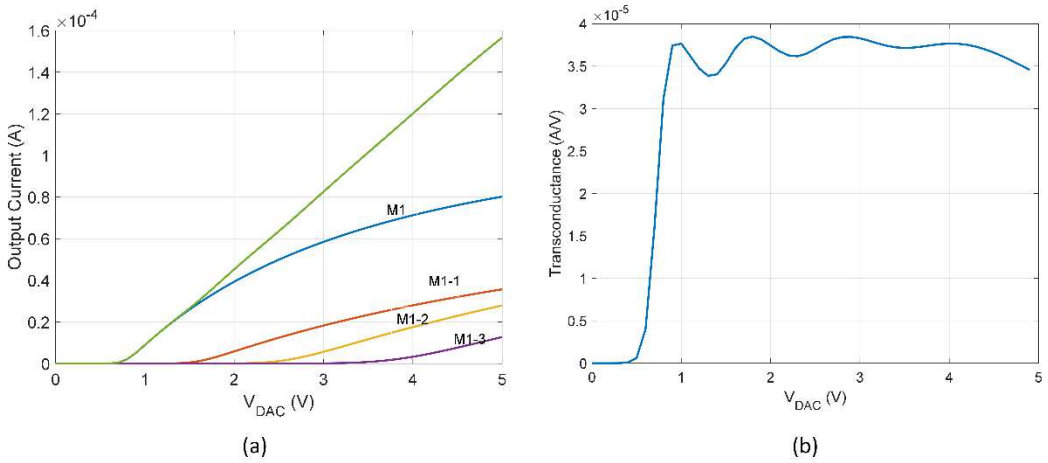

Fig. 5.7 (a) Output current (green color) variation with V_{DAC} in absence of the offset current, individual currents are also shown; (b) Slope of the I_{OUT}-V_{DAC} curve

The variation of the transisor drain currents as V_{DAC} is swept from 0 to 3 V, is shown in Fig. 5.7(a). The slope of the of I_{OUT}-V_{DAC} curve or the transcoductance is shown in Fig. 5.7(b). A small ripple is observed in the transconductance which can be further minimized by adding a few more transistor in parallel to M1. Still, if nonlinearity is present in the output current, a look-up table can be used to generate stimulus current at a desired level.

Since the input of the linearization circuit comes from the current DAC, two such linearization blocks are required for the two DAC subcircuits "L" and "M". First, the linearization is performed for the 4 LSB bits of the digital input (for DAC subcircuit "L"). Then another set of 4 transistors scaled by 16 (for DAC subcircuit "M"), are added in parallel.

5.2.4. Offset Current Generator

The offset generator circuit provides a current through R_{DAC} which creates a voltage equal to the threshold voltage of a MOSFET. For this purpose, a threshold referenced self-biased current source circuit is implemented, and its schematic is shown in Fig. 5.8. The current flowing in this circuit can be found solving the following equation.

$$I = \frac{V_t}{R_{os}} + \frac{1}{R_{os}}\sqrt{\frac{2I}{K_n^{'}\left(W/L\right)_1}} \tag{5.14}$$

If the R_{os} resistance and the M1 transistor in Fig. 5.8 are made large, then the second term in (5.14) becomes negligible. Now if $R_{os} = R_{DAC}$ this circuit will be able to cancel out the nonlinearity in the stimulus current due to the threshold voltage.

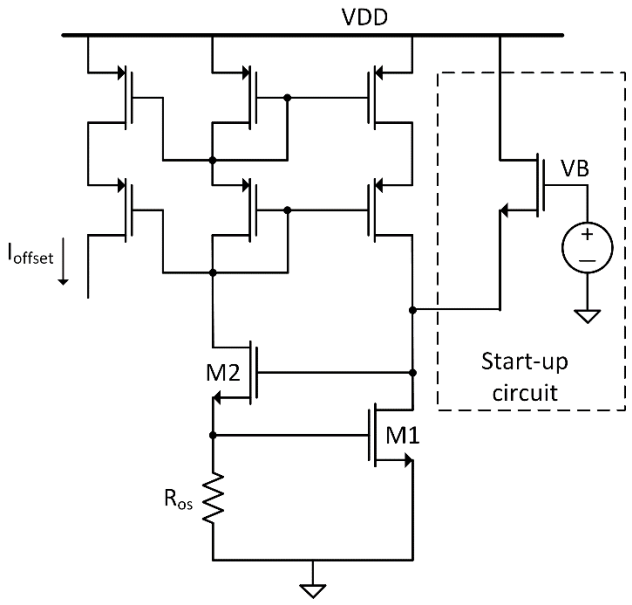

Fig. 5.8 Schematic of the offset generator circuit

As this is a self-biased circuit, a separate start-up circuit is required to produce the desired level of current. The offset current is tapped using a pMOS current mirror.

5.2.5. Design Procedure

Our designed current source should be able to provide an output current in the range of 10 μA to 2.55 mA, and this is controlled by 8 digital bits B[0:7]. The output current should be linear with the digital inputs, and the output impedance should be greater than 1 MΩ. Moreover, the current source should be able to operate with a very low output voltage. The parameters used for designing the current source are summarized in Table 5.1. To design the circuit components described above, these parameters need to be evaluated.

Table 5.1 Design parameters for the current source

Parameter	Description
I_{REF}	Reference current to the current source
$I_{OUT,min}$	10 µA, corresponding to the lowest digital input
$I_{OUT,max}$	2.55 mA, corresponding to the highest digital input
R_{DAC}	Resistance required for producing the gate-voltage in M1
$V_{DAC,min}, V_{DAC,max}$	Lowest and highest voltage observed across R_{DAC}
V_{SET}	Fixed drain voltage across M1, should not be too small to limit the area of the cascode transistor

To start the design, an initial reference current is selected based on the power consumption constraint. A small $V_{SET} < 100\,mV$ is chosen. The design procedure is shown in the flowchart in Fig. 5.9. The required gain of the current source is $K = I_{OUT,min}/I_{REF} = g_{m1}R_{DAC}$. Therefore, g_{m1} is needed to be kept constant throughout the range of operation. g_{m1} depends on the W/L ratio of the linearization transistors and V_{SET}. After following the linearization procedure described in section 5.2.3, if the current gain is not the same as the required gain, K, values of R_{DAC} and V_{SET} need to adjusted accordingly. However, the for new values of R_{DAC} and V_{SET}, I_{OUT} may no longer be linear with V_{DAC}. Then, the whole process is started over with a new initial value of I_{REF} and V_{SET}.

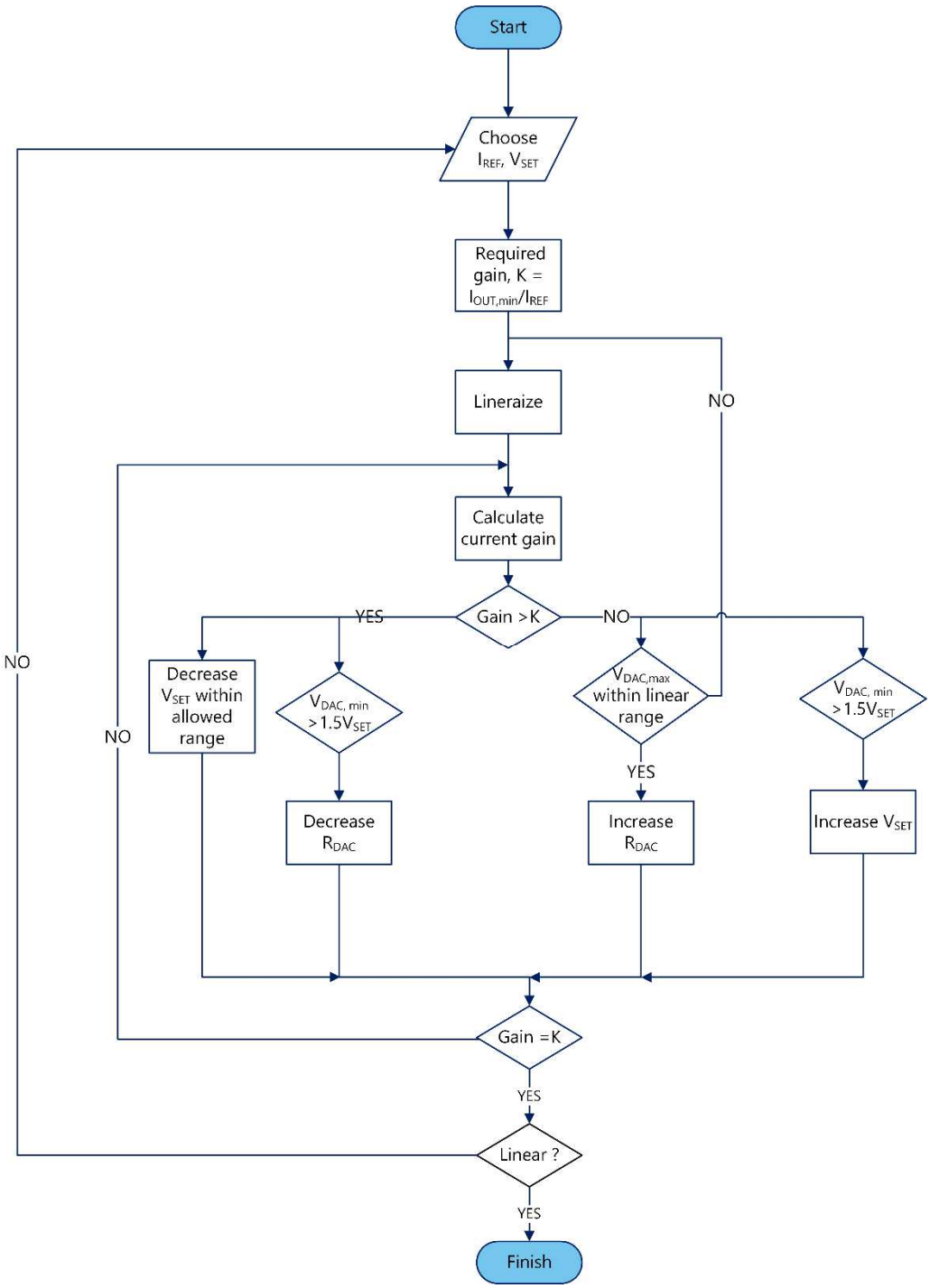

Fig. 5.9 Flowchart for determining the circuit component values

The final values of the design parameters are given in Table 5.2. A reference current 0.2 μA is used to minimize the power loss in the current source. The resistance required for R_{DAC} is 680 kΩ. Although two such high resistances are required, they can

be realized by the high-R poly layer (1000 Ω/square) in the AMI 0.5µm process, to reduce the area [42].

Table 5.2 Obtained values of the design parameters

Parmeter	Value
I_{REF}	0.2 µA
R_{DAC}	680 kΩ
$V_{DAC,min}, V_{DAC,max}$	136 mV + V_t, 2.04 V + V_t
V_{SET}	80 mV

5.3. Performance of the Designed Current Source

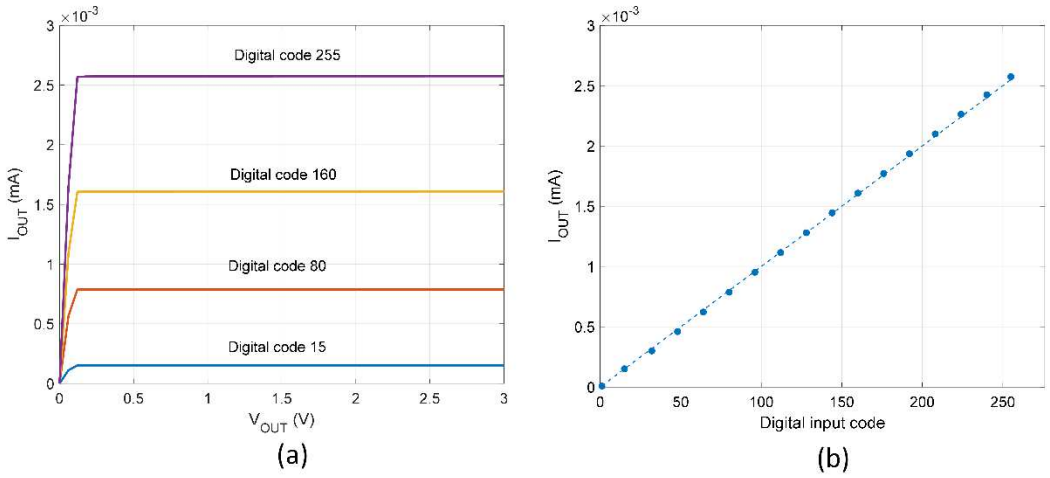

Fig. 5.10 Simulation results, (a) variation of I_{OUT} vs. V_{OUT}, (b) I_{OUT} vs. digital input code

Variation of the output current with output voltage is shown in Fig. 5.10(a). At the highest current the minimum voltage across the current source to maintain a constant current is measured to be only 120 mV. The designed current source delivers a stimulus current from 8.1 µA to 2.57 mA with good linearity. This is shown in Fig. 5.10(b).

The output impedance can be measured by calculating the slope of the $I_{OUT} - V_{OUT}$ curve. At the highest digital input, it is measured to be greater than 2 MΩ. The output impedance corresponding to the lowest digital input is in the range of GΩ. The current source draws 8.07 µA of current at the lowest digital input, 1. This is due to current consumed by the offset generator and the op-amp. So, the current source is inefficient for the digital inputs 1 to 5. Nevertheless, current consumed at the highest digital input is only 22.92 µA. These measured results are summarized in Table 5.3.

Table 5.3 Measured results from simulation

Parmeter	**Value**
$\boldsymbol{I_{OUT}}$	8.1 µA – 2.57 mA
$\boldsymbol{V_{OUT,min}}$	120 mV
$\boldsymbol{R_{OUT}}$	> 2 MΩ
Current Consumption	8 µA – 23 µA

Chapter 6: Simulation Results

The dynamic high-voltage supply, current source and the control logic for the DHVS are implemented using the AMI 0.5µm CMOS process, and the simulations are done using the Cadence Spectre tool. The BSIM3 SPICE model for the N8BN run is used for the simulation [43].

To test the stimulator, the impedance between the "active" and "return" electrode, Z_E is too be estimated. In the literature pertaining to current mode stimulator, often a simplified series R-C model is used for Z_E. The resistance is in the range of 1kΩ to 20kΩ, and the capacitance varies between 1nF to 100nF [25, 26, 28, 40]. The stimulator designed here is tested against a smaller capacitance since a long time is required to deliver the desired level of charge in a larger capacitance and its simulator takes a very long time.

The stimulator is tested for a biphasic stimulus current of 1mA, and the pulse-width and inter-phase delay are 40µS and 6µS respectively. The potential of the electrodes during the stimulus delivery for $Z_E = 12k\Omega$ is shown in Fig. 6.1(a). The DHVS provides the maximum output of 13.2 V for this case. Electrode potential for $Z_E = 12k\Omega$ is shown in Fig. 6.1(c). It is to be noted that during the cathodic phase due to the spike observed in the stimulus current (Fig. 6.1(d)), the DHVS skips to the next step and its output becomes 6.8 V. However, the magnitude of the spike in the anodic phase is less and DHVS operates at the desired level of 4.5 V. The origin of this spike is the high dV/dt at the beginning of the cathodic and anodic phase. The output voltage of the DHVS rises very fast to provide the required drop across resistive Z_E and this op-

amp inside the current source fails to respond within a short amount of time. Thus, the source voltage of the cascode transistor is no longer maintained at V_{SET} and since the output stimulus current depends on this source voltage, a spike in the source voltage also gets reflected in the output current. To reduce the magnitude of the spike the slew-rate of the DHVS output, i.e., its rise-time needs to be increased.

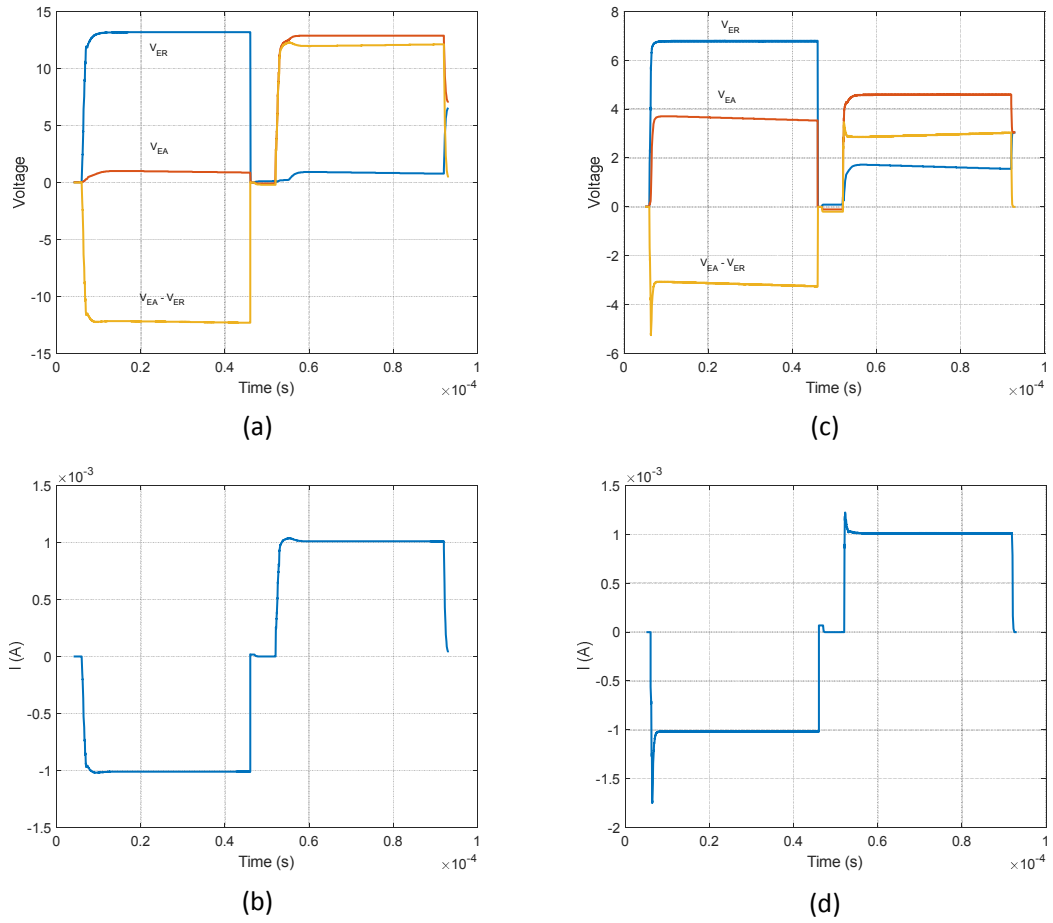

Fig. 6.1 (a) Potential of the electrodes for the stimulus shown in (b), $Z_E = 12k\Omega$, $T_{PW} = 40\mu S$, $T_{IPD} = 6\mu S$, $I_{STIM} = 1mA$; (c) Potential of the electrodes for the stimulus shown in (d), $Z_E = 3k\Omega$, $T_{PW} = 40\mu S$, $T_{IPD} = 6\mu S$, $I_{STIM} = 1mA$

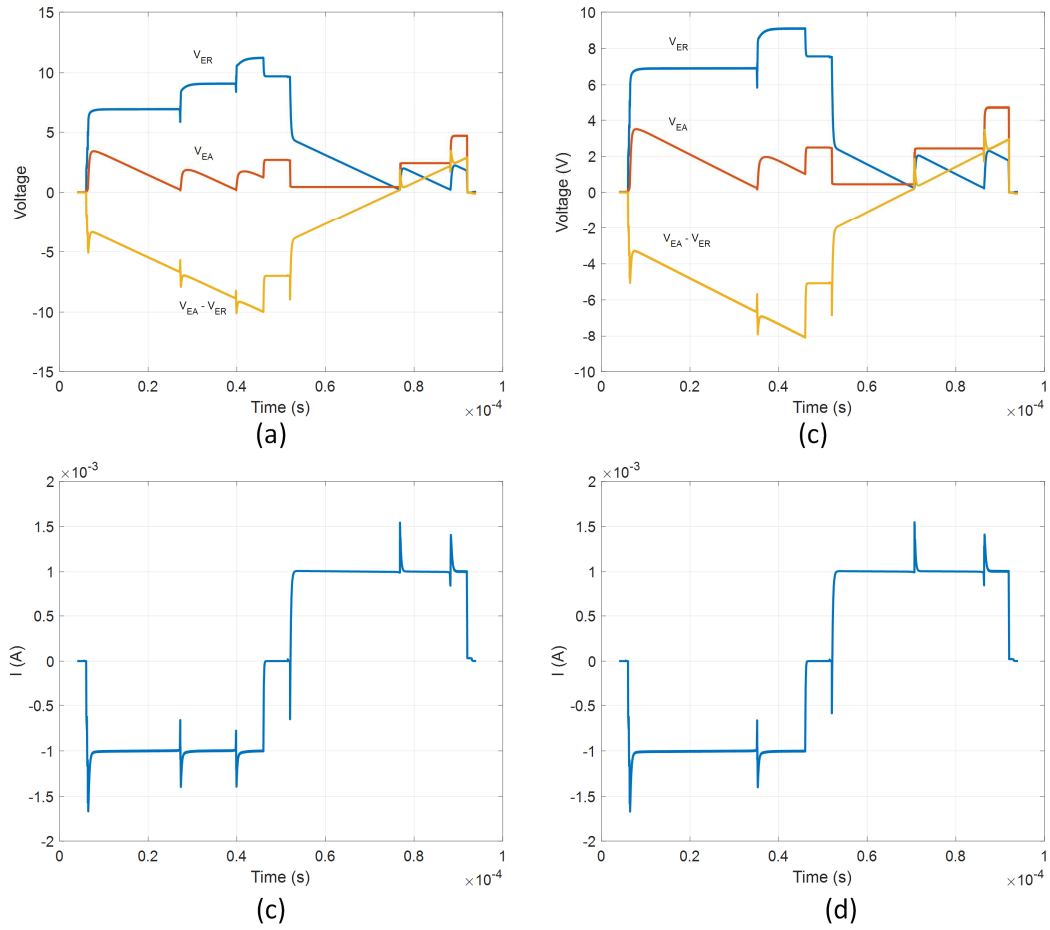

Fig. 6.2 (a) Potential of the electrodes for the stimulus shown in (b), $Z_E = 3k\Omega + 5.8nF$, $T_{PW} = 40\mu S$, $T_{IPD} = 6\mu S$, $I_{STIM} = 1mA$; (c) Potential of the electrodes for the stimulus shown in (d), $Z_E = 3k\Omega + 8nF$, $T_{PW} = 40\mu S$, $T_{IPD} = 6\mu S$, $I_{STIM} = 1mA$

Simulation results for $Z_E = 3k\Omega + 5.8nF$ and $Z_E = 3k\Omega + 8nF$ are shown in Fig. 6.2(a) and Fig. 6.2(c) respectively. Corresponding stimulus current is shown in Fig. 6.2(b) and Fig. 6.2(d). DHVS automaically goes to the next output stage to support the voltage across the capacitor. Voltage across the "active" and "return" electrode goes to zero after the stimulation period which means a charge-balanced stimulus has been delivered.

The overall efficiency of the stimulator with the proposed technique is compared with an ideal H-bridge stimulator with a fixed $HVDD = 13.2\,V$ and stimulus current of $1\,mA$. Here, $13.2\,V$ is the maximum output voltage of the design DHVS for $1\,mA$ stimulus current. For $Z_E = 3k\Omega + 5.8nF$, efficiency of the ideal H-bridge stimulator is 22%, whereas the efficency with the proposed technique is 42%. For $Z_E = 2k\Omega$, the efficiency of the stimulator is improved from 15% to 32%.

Table 6.1 State-of-the-art quasi-adiabatic CMS comparison

	[34] T. BioCAS '13	**[26] JSSC '15**	**[28] BioCAS '14**	**This Work**
Process	IBM 0.18µm	TSMC 65nm	IBM 0.18µm	AMI 0.5µM
DHVS Input/Compliance	3 V/11.5 V	1.3 V/9 V	3.3 V	3 V/15 V
Load Current	2 — 504 µA	10 — 900 µA	< 2 mA	10µA—2.55mA
N	4	7	4	6
Efficient charge-recycling	NO	NO	NO	YES
Peak Efficiency	82%	68%	NA	67%
CS drop-out	0.3 – 0.7 V	> 0.2 V	> 0.1 V	0.12 V
Supply Capacitance	900 pF	> 700 pF	-	540 pF
Z_E	R-Yes, C-Yes	R-?, C-Yes	R-Yes, C-Yes	R-Yes, C-Yes

Comparison of the design stimulator with existing state-of-the-art quasi-adiabatic current mode stimulators is shown in Table 6.1. The stimulator demonstrated in [28] uses an off-chip boosting converter. Although the peak efficiency of the

stimulator designed in [34] is 82%, the capacitance required to achieve that is high. Moreover, its maximum current range is only 504 µA. If a stimulator with maximum driving current less than 1 mA were to be designed in this thesis using the same DHVS structure described in Chapter 4, the efficiency could be improved by 10% to 15 %.

The drop-out voltage of the current source designed here is very low as compared to [26, 40, 28]. The drop-out voltage for the stimulator designed in [26, 28] is not reported, so they are estimated from the figures shown there. The designed stimulator can drive both capacitive and resistive Z_E as opposed to [26], where the stimulator is tested for purely capacitive Z_E.

Chapter 7: Conclusions & Future Work

7.1. Conclusions

The current mode stimulator designed in this thesis is able to perform as expected for both resistive and capacitive load with moderate efficiency. The stimulator can deliver current from 10μA to 2.55mA in steps of 10μA. The peak efficiency of the DHVS is 67%, and it can maintain the efficiency over 60% for load current in the range of 25μA to 1.4mA. To implement the proposed stimulus delivery technique, only 100pF additional capacitance is required in the high-voltage generation circuit. The ratio of maximum output current to total supply capacitance is better compared to the existing state-of-the-art quasi-adiabatic CMSs.

7.2. Future Work

- A layout of the whole stimulator circuit remains to be done using the AMI 0.5μm CMOS technology. After that, post-layout parameter extraction and simulation will be done to observe the effect of parasitics in the circuit.
- The devices inside the charge-pump circuit of the DHVS have VDD rating of 3 V. Therefore, they can be scaled to a lower technology node (e.g., 180nm, 65nm). However, the level shifters shown in Fig. 4.6 and the high-side switches use HV MOSFETs. An alternate level shifter circuit which maintains gate-oxide reliability needs to be used to design the circuit using only low-voltage devices. Such level shifter is used in [26], although the circuit is not shown there.

- To increase the efficiency a switched-capacitor based DC-DC can be used, but that will result in increased chip area.
- To reduce the magnitude of the spike in the stimulus current, the width of the cascode transistor can be reduced. Although that will increase the drop-out voltage of the current source, a trade-off can be achieved between the magnitude of the spike and the drop-out voltage. Another way to reduce the spike is to increase the rise-time of the DHVS output, and this can be done by increasing the output stage capacitance. The effect of this spike on the neural tissue is also needed to be considered.
- A limitation of the design CMS is its inability to drive small capacitances. During the interphase delay a capacitive Z_E holds its charge and this voltage appears across the current source at the beginning of the anodic phase. As the VDD rating of the AMI 0.5µm technology is 5 V, the following criteria must be satisfied.

$$2\frac{I_{STIM}T_{PW}}{C_D} - 2I_{STIM}R_S \leq 5V \tag{7.1}$$

Eq. (7.1) puts a lower bound to the capacitance for a given I_{STIM} and T_{PW}, the stimulator can drive. To remove this bound, a high voltage adapter circuit described in [27, 32] can be added to the "return" electrode side.

Appendix A: DHVS Logic Design

The output of the dynamic high voltage supply goes to the next step when the voltage across the current source becomes less than V_{DSAT}. Therefore, we need a comparator whose inputs are the voltage across the current source and the DC voltage V_{DSAT}. The comparator output becomes "high" when the current source voltage goes below V_{DSAT}, and that will tell the DHVS to increase the output voltage by one step. After the DHVS voltage goes up, the comparator output becomes "low". This comparator output is fed to a state-detector circuit which keeps track of the DHVS output at any instant. There is a 3-bit counter inside the state-detector for 6 discrete outputs of the DHVS. At the rising edge of the comparator output, the counter increases by one step and that signal is used to turn on the switches shown in Fig. 4.7. A block diagram of this logic is shown in Fig A.1. The logic circuit of the "State Detector" block is shown in Fig. A.2.

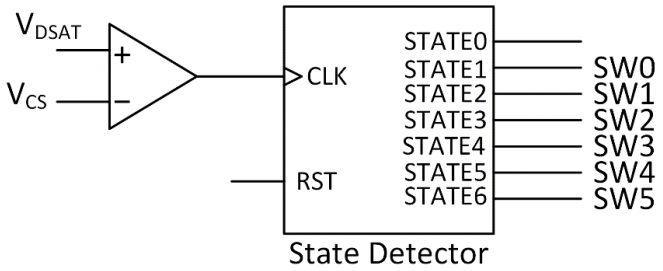

Fig. A.1 DHVS logic implementation

However, the level shifters shown in Fig. 4.7(b) are unable to respond immediately after the SW signal becomes high. The level shifter needs four to eight clock cycles to shift the digital logic by the output voltage of the corresponding stage.

Therefore, the logic shown in Fig. A.1 needs to be modified. The solution for this is given in the final DHVS logic circuit shown in Fig. A.3. The SW_DHVS signal is ANDed with the state-detector output to generate the corresponding SW signal.

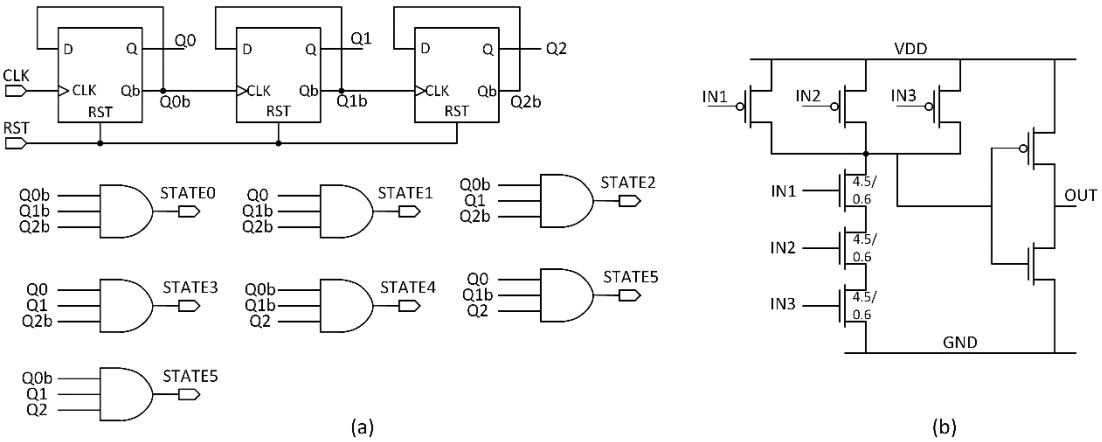

Fig. A.2 (a) State detector logic circuit, (b) Schematic of AND gate

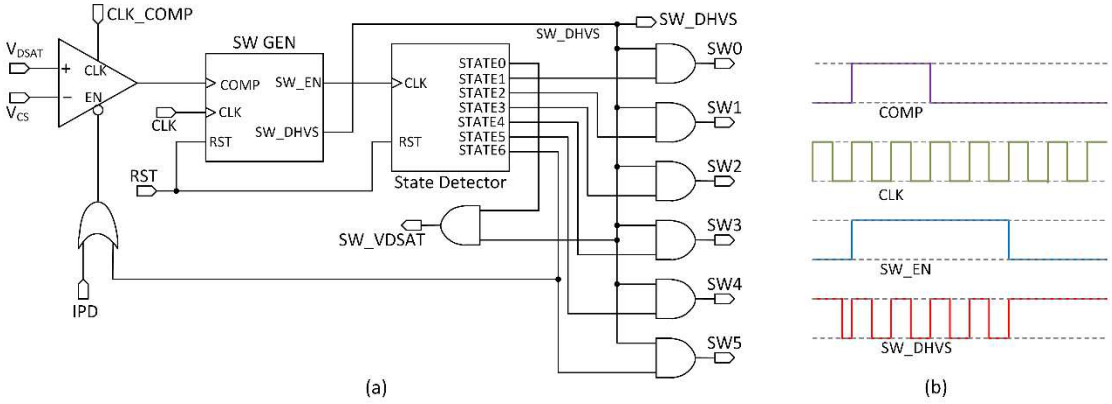

Fig. A.3. (a) Logic circuit to generate gate signals for the DHVS, (b) Waveforms of comparator output, clock input, SW_EN, and SW_DHVS signal of the SW GEN block (top to bottom)

The EN input of the comparator in Fig. A.3(a) is active low. After the STATE6 signal has become “high”, the comparator is disabled, so that the DHVS continue to operate at its hightest output. During the interphase delay period also the comparator is

disabled. The SW GEN block generates the bottom two waveforms in Fig. A.3(b). The width of the SW_EN signal varies between 4 to 8 clock cycles. Digital circuit for the SW GEN block is shown in Fig. A.4.

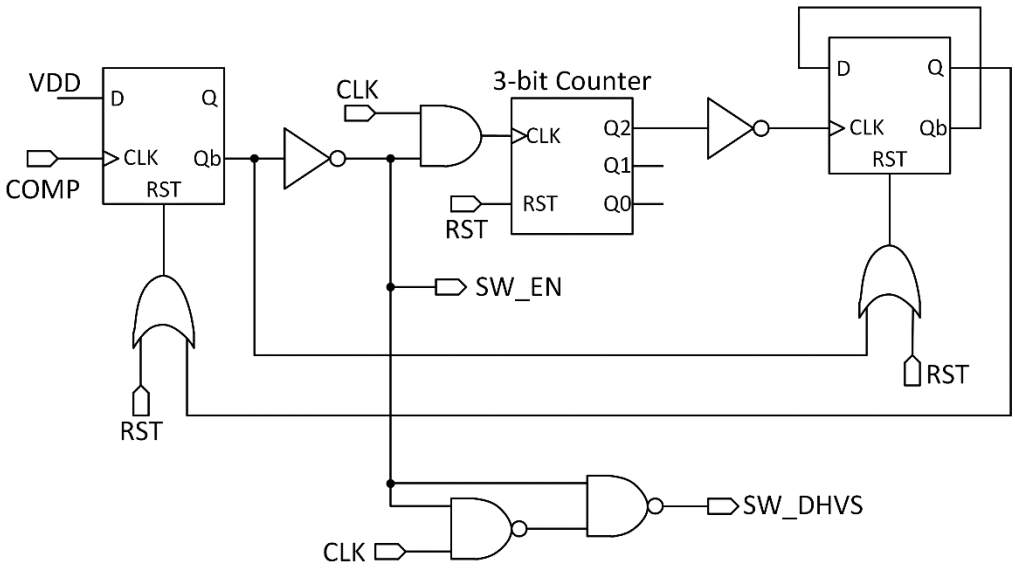

Fig. A.4 Logic circuit for SW GEN

Appendix B: Stimulator Circuit with Transistor Sizes

All dimensions are in µm. If dimensions are not mentioned nMOS width and length are 1.5µm and 0.6µm and for pMOS they are 4.5µm and 0.6µm respectively. In Fig. B.6, the "CA", "AN", and "IPD" signals represent the cathodic phase, anodic phase, and interphase delay period respectively. The "CS_EN" signal is high during cathodic and anodic phase only. The "RST" signal is high for a short period at the beginning and end of cathodic phase. These digital signals can be generated from a high frequency clock, using a counter.

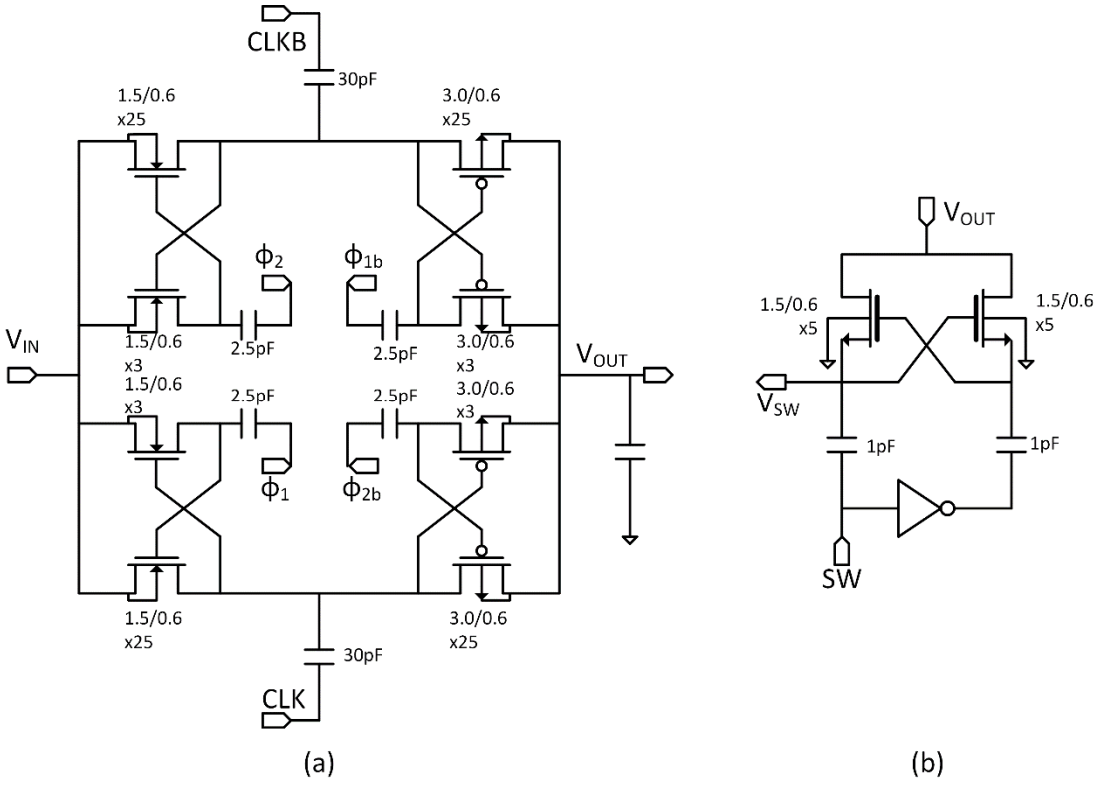

Fig. B.1 (a) Schematic of the charge pump to be used in the DHVS, (b) Schematic of the level shifter with HV nMOS transistors

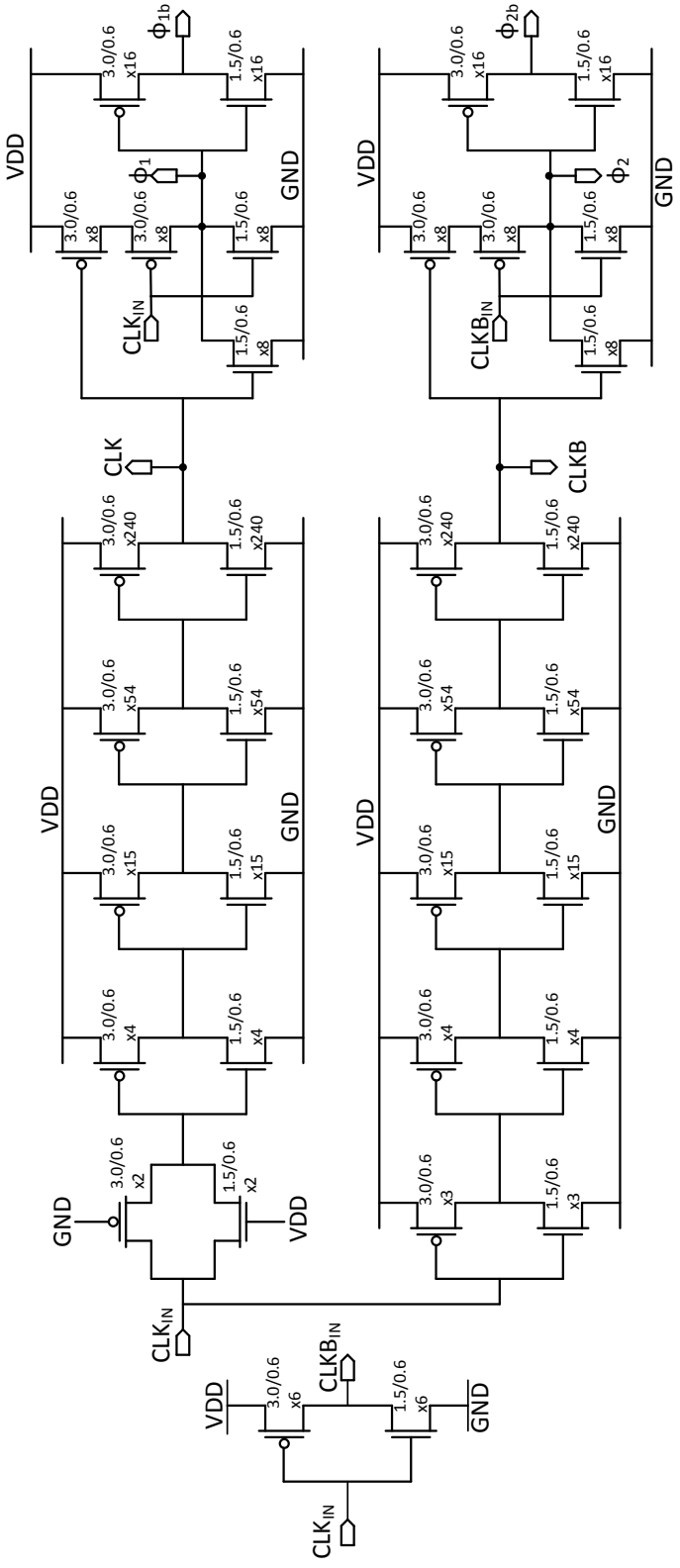

Fig. B.2 Schematic of the non-overlapping clock generator

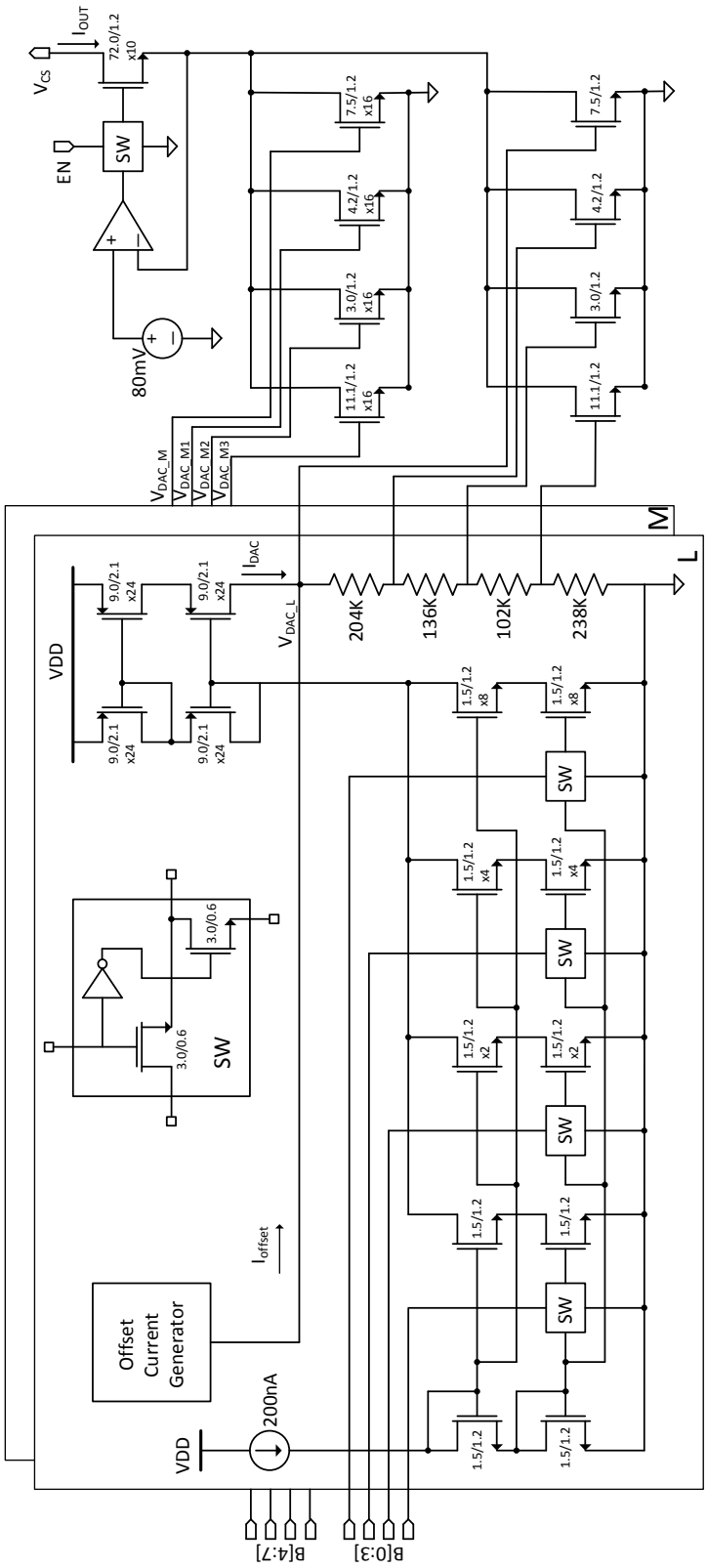

Fig. B.3. Schematic of the constant current source

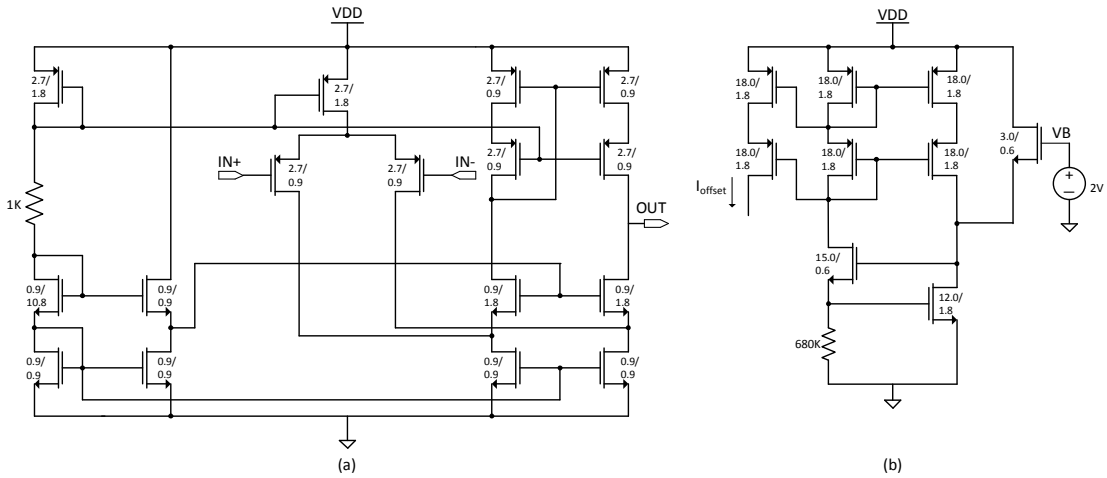

Fig. B.4 (a) Schematic of the operational amplifier, (b) Schematic of the offset current generator

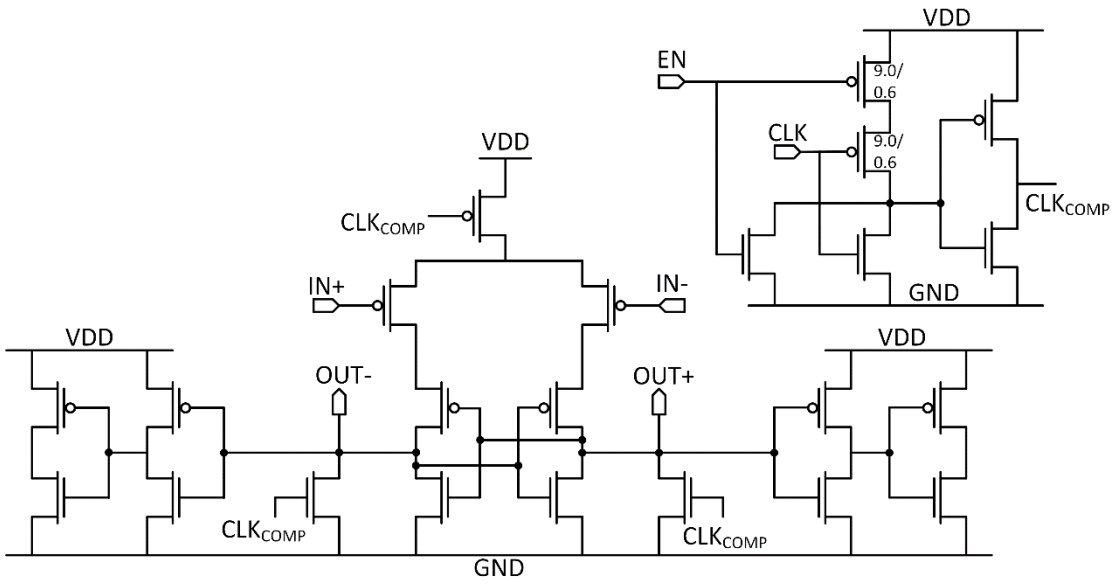

Fig. B.5 Schematic of the dynamic comparator

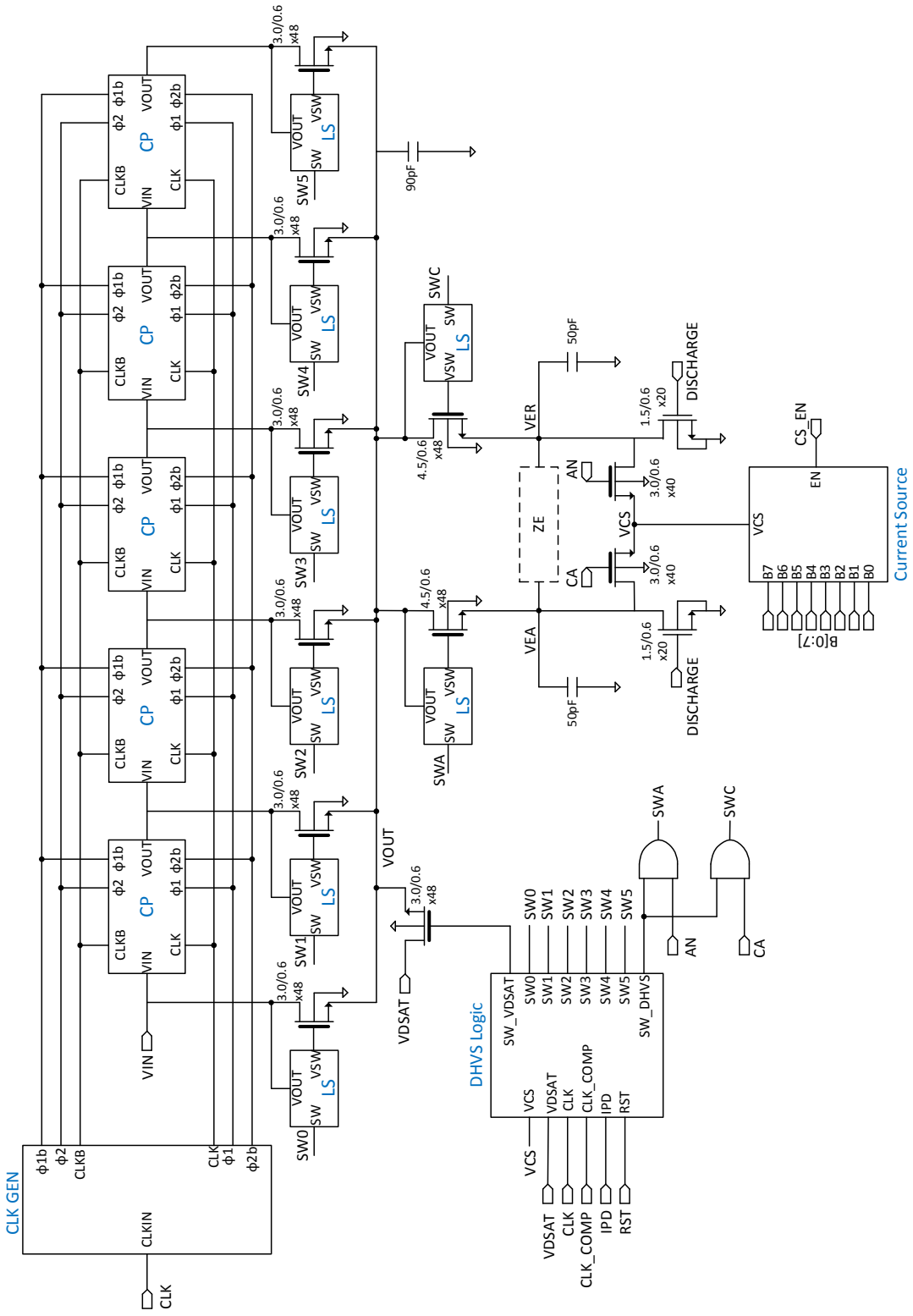

Fig. B.6. Complete schamtic of the designed current mode stimulator circuit

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