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Extending the power transfer capability of a three-port DC–DC converter for hybrid energy storage systems

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Abstract: Design considerations for a three-port bidirectional DC–DC converter to be used in hybrid energy storage systems (HESSs) with the aim to increase the power transfer capability are discussed in this study. For this, an analysis of the power flow that allows obtaining the current waveforms is presented. Then, a loss model, that includes losses in semiconductors and the magnetic core, is proposed based as a function of the voltage variations in the energy storage devices considering all possible cases of power transference. The analysis reveals that it is possible to size the converter auxiliary inductances to reduce the converter currents and losses and therefore increase the power transfer capability. The analysis and the proposal presented in this study are validated using a 5-kW experimental prototype. Results show that it is possible to increase the converter transfer capability up to 80%.

1 Introduction

The use of hybrid energy storage systems (HESSs) has significantly increased in recent years due to their potential applications in small generating renewable energy systems, able to operate either isolated or as part of micro-grids, among others [1]. HESS can use different kinds of energy storage devices, such as for instance batteries and supercapacitors, taking advantage of the high energy density of one, and the high power density of the other, respectively [2–4]. This requires the use of converters with suitable topologies, which allow connecting in parallel different energy storage devices with different characteristics. A possible solution is to use multiport converters to centralise the power flow control at only one unit in order to reduce size, cost and complexity [5–7].

There are different kinds of topologies for multiport converters that are characterised by their number of ports, ability to step-up and/or step-down voltage, ability to control energy flow bidirectionally and the inclusion of galvanic isolation [8]. The latter is a necessary feature in certain applications and it allows a better performance when the voltage between inputs and outputs is very different [9].

Different studies on isolated multiport converters for HESS have been reported recently [10–12]. In [10, 11], a bidirectional triple-active-bridge (TAB) converter is proposed as a solution for renewable energy system applications whose topology can be observed in Fig. 1*a*. It is isolated by means of a high-frequency transformer and able to step-up and step-down voltages.

In [13] it is proposed the use of a TAB converter in an on-board charger. In this proposal when one port is idling the overall efficiency decreases because the blocking action requires active switching in the three ports.

In order to improve the converter performance, in [10] it is proposed a new modulation strategy to control the duty cycle, besides of the conventional phase shift between the ac voltages at

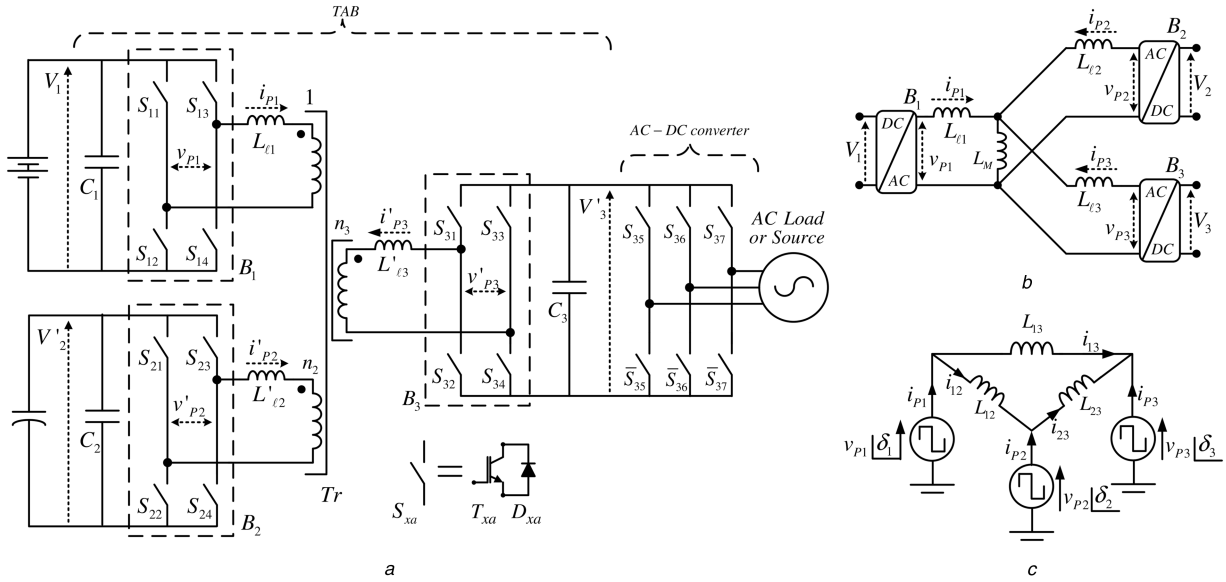

Fig. 1 *TAB converter and the equivalents circuits*
(a) Three-port bidirectional DC–DC converter topology, ***(b)*** *Y*-equivalent circuit of the transformer, ***(c)*** Δ-equivalent circuit of the transformer

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the terminals of the transformer, to minimise the reactive power, but with the drawback of reducing the operating range.

A similar strategy is proposed in [12] using an asymmetrical duty-cycle control method for a THB for HESS applications. This control strategy allows achieving a wide zero voltage switching (ZVS) operation range and also reduces the peak and rms current, reducing in consequence losses.

In [14] it is deduced that the power transfer is a function of the leakage inductances of the high-frequency transformer.

In [15, 16] it is concluded that leakage inductances have a significant influence in the converter losses, which requires to size them properly so as to reach a high efficiency.

In [10, 11, 13, 17], the leakage inductances of the transformer are dimensioned with the same value, which allows the transference of the same maximum power at each port. However, when different values of maximum power are required at each port, the total losses can be too high.

A proposal to size the converter auxiliary inductance to be used in HESS, to increase their power transfer capability is presented in this paper. This proposal is based on the analysis of the power flow, which allows obtaining the current waveforms. In addition, a loss model that includes losses in semiconductors and the magnetic core is proposed, as a function of the voltage variations in the energy storage devices, for all possible cases of power transference. Results show that the converter power transfer capability can be increased significantly, compared to those results obtained when the converter auxiliary inductances are sizing using the conventional methodology.

This work is organised as follows: Section 2 describes the TAB topology, its operation principle and an analysis of the current waveforms at each port. Section 3 presents the sizing of the converter auxiliary inductances. In Section 4, it is presented the model for losses and an evaluation of them. Section 5 determines de converter power flow maximum capability, considering the restrictions due to maximum semiconductor current capability and semiconductor losses. Then, Section 6 presents experimental results to validate the model of power losses. Finally, conclusions are drawn in Section 7.

2 Description and principle of operation of the converter

In the HESS application represented in Fig. 1*a*, V_1 is the voltage of a battery bank, V_2', is the voltage of a supercapacitor and V_3' is the DC voltage at the port where a bidirectional load can be connected. As an example, a regenerative AC drive was included in this figure. The objective of the TAB is to control the power and voltage required by the load, V_3'. This topology consists of three full active bridges, B_1, B_2, B_3 and a high-frequency transformer, *Tr*. $L_{\ell 1}, L_{\ell 2}'$ and $L_{\ell 3}'$ represent the auxiliary inductances, values that include the leakage inductances of each transformer winding. The switches S_{xa}, shown in Fig. 1*a*, can be implemented by a power transistor T_{xa} [e.g. insulated gate bipolar transistor (IGBT)] and an antiparallel diode, D_{xa}, where subscript x represents the number of ports and subscripts a denotes the number of switches. Each active bridge can operate either as a rectifier or as an inverter, depending on the direction of the power flow.

All variables and the parameters of ports 2 and 3 can be referred to port 1 considering a transformer Y-equivalent circuit, as shown in Fig. 1*b*, by using the following relations: $L_{\ell 2} = L_{\ell 2}'/n_2^2, V_{P2} = V_{P2}'/n_2, V_2 = V_2'/n_2$, and $i_{P2} = i_{P2}' n_2$ for port 2 and $L_{\ell 3} = L_{\ell 3}'/n_3^2, V_{P3} = V_{P3}'/n_3, V_3 = V_3'/n_3$ and $i_{P3} = i_{P3}' n_3$ for port 3, where n_2 and n_3 are the transformer turns ratios of ports 2 and 3, respectively.

The transformer's magnetising inductance is usually much larger than the leakage inductances, high enough as not to affect the converter operation, as it was demonstrated in [18]. Therefore, in this paper the transformer's magnetising inductance, L_M, is not included in the model.

In order to simplify the power flow analysis, the variables corresponding to the transformer *Y*-equivalent circuit are transformed into a Δ-equivalent circuit, as shown in Fig. 1*c*. In this figure, $V_{P1}\angle\delta_1, V_{P2}\angle\delta_2$ and $V_{P3}\angle\delta_3$, represent the AC voltages magnitude and phases of the bridges B_1, B_2 and B_3, respectively. The inductances L_{12}, L_{13} and L_{23} can be obtained from a *Y*–Δ transformation. In the following two subsections, the converter power flow and current waveforms are analysed.

2.1 Power flow analysis

According to the transformer Δ-equivalent circuit, current dynamics in each branch can be expressed as

$$\frac{\mathrm{d}i_{xy}(\theta)}{\mathrm{d}\theta} = \frac{V_{Px}(\theta) - V_{Py}(\theta)}{\omega L_{xy}}, \tag{1}$$

where x and y represent the ports involved in the equation, $\theta = \omega t, \omega = 2\pi f_s$ and f_s is the switching frequency.

Solving (1), for $i_{12}(\theta), i_{23}(\theta)$ and $i_{13}(\theta)$ the following expressions for currents at each port can be obtained:

$$i_{P1}(\theta) = i_{12}(\theta) + i_{13}(\theta), \tag{2}$$

$$i_{P2}(\theta) = i_{23}(\theta) - i_{12}(\theta), \tag{3}$$

$$i_{P3}(\theta) = -i_{13}(\theta) - i_{23}(\theta). \tag{4}$$

For this particular case of study, voltages V_1 and V_2' can change according to the state of charge at both storage units. It can be demonstrated that the TAB topology corresponds to a current source converter, in which the output current is a function of the phase shifts. Therefore, depending on the phase shifts and the converter parameters, this topology can operate in either step-down or step-up mode, regardless of the transformer's ratio.

Aiming to represent voltage variations V_1 and V_2' respect to V_3', in the converter mathematical expressions, the voltage conversion ratios are defined respect to the voltage of port 3 as

$$d_{23} = \frac{V'_2 n_3}{V'_3 n_2}, \tag{5}$$

and

$$d_{13} = \frac{V_1 n_3}{V'_3}, \tag{6}$$

then, the complete expressions to solve (2)–(4) are shown in Table 1.

The modulation strategy used in this paper consists in controlling the active bridges in order to generate a voltage square waveform with 50% of duty cycle. The power flow can be controlled by manipulating the phase shifts between the AC

Table 1 Current expressions of Δ-equivalent circuit for each interval

Current	Interval I ($0 < \theta < \delta_2$)	Interval II ($\delta_2 < \theta < \delta_3$)	Interval III ($\delta_3 < \theta < \pi$)
$i_{12}(\theta)$	$\frac{V_3(d_{13}+d_{23})}{\omega L_{12}}\theta + i_{12}(0)$	$\frac{V_3(d_{13}-d_{23})}{\omega L_{12}}(\theta-\delta_2) + i_{12}(\delta_2)$	
$i_{23}(\theta)$	$\frac{V_3(1-d_{23})}{\omega L_{23}}\theta + i_{23}(0)$	$\frac{V_3(1+d_{23})}{\omega L_{23}}(\theta-\delta_2) + i_{23}(\delta_2)$	$\frac{V_3(1-d_{23})}{\omega L_{23}}(\theta-\delta_3) + i_{23}(\delta_3)$
$i_{13}(\theta)$	$\frac{V_3(1+d_{13})}{\omega L_{13}}\theta + i_{13}(0)$		$\frac{V_3(1-d_{13})}{\omega L_{13}}(\theta-\delta_3) + i_{13}(\delta_3)$

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voltages at the transformer terminals. Thus, based on (1) and considering constant DC voltage in a half period, the power transferred from ports x to y can be expressed as [10]

$$P_{xy} = V_x \frac{1}{\pi} \int_0^{\pi} i_{xy}(\theta) \mathrm{d}\theta = \frac{V_x V_y \delta_{xy} (\pi - |\delta_{xy}|)}{\pi \omega L_{xy}}. \quad (7)$$

Considering the direction of the current flow adopted in (2)–(4), the expressions for the powers at each port, shown in Table 2, are obtained as a function of V_3 and the voltage conversion ratios, d_{23} and d_{13}, considering as the phase reference $\delta_1 = 0$◦.

2.2 Determination of the current waveforms at each port

The AC current waveforms at each port undergo variations according to the operating point of the converter, which can be represented for three intervals I, II and III, in a half period, defined as $\delta_1 < \theta \leq \delta_2, \delta_2 < \theta \leq \delta_3$ and $\delta_3 < \theta \leq \pi$ in Fig. 2, respectively.

In this paper, an algorithm to establish the waveforms of current i_{P1}, i_{P2} and i_{P3} for each converter operating point was developed, which uses the voltage conversion ratios and phase shifts as input variables. These variables and the converter parameters, are used to evaluate the currents expressions given in Table 1 at the beginning and at the end of each interval defined before. In this way, it is possible to establish the magnitude and slope of current at each interval. This algorithm also allows determining the zero-crossing angles used later to calculate the conduction losses. These angles can be obtained by equating to zero the current expressions of Table 1, and solving them for θ, for the corresponding current intervals.

Table 3 shows the expressions to evaluate the current zero crossing angles at each port. As a result, the AC current waveforms shown in Figs. 2*a*–*c* are obtained for ports 1, 3 and 2, respectively. These figures show all the possible cases for phase shifts are $\delta_1 < \delta_2 < \delta_3$. Subscripts a to g represent the different cases and the conduction intervals are represented by the segments 1–4, where 1 refers to the conduction interval of diodes D_{x1}, D_{x4}; 2 refers to the conduction interval of transistors T_{x1}, T_{x4}; 3 refers to the conduction interval of diodes D_{x2}, D_{x3} and 4 refers to the conduction interval of transistors T_{x2}, T_{x3}. In addition, the instants and magnitudes of currents when the semiconductors turn on and off with switching losses can also be observed in these figures. The other semiconductor switching occurs ideally without losses (soft switching). It can be shown that similar current waveforms can be obtained at each port for other phase shifts conditions.

3 Sizing of the converter auxiliary inductances

Usually, auxiliary inductances are dimensioned $L_{12} = L_{13} = L_{23}$ because the converter requires an equal power transfer capability between ports [10, 11, 17]. However, when a bidirectional power transference between ports is different, it can be demonstrated that the total converter losses increase when $L_{12} = L_{13} = L_{23}$, as it will be shown later in Section 4.3.

In this paper will be considered the following power transfer particular cases that correspond to the normal operation of a HESS application:

- Ports 1 and 2 transfer power to port 3.
- Port 3 transfers power to ports 1 and 2.
- Port 1 transfers power to ports 3 and 2 is in the idle mode.

Table 2 Expressions of power flow at each port

$P_1 = -\frac{V_3^2 d_{13} \delta_3 (\lvert\delta_3\rvert/\pi - 1)}{L_{13}\omega} - \frac{V_3^2 d_{13} d_{23} \delta_2 (\lvert\delta_2\rvert/\pi - 1)}{L_{12}\omega}$
$P_2 = \frac{V_3^2 d_{13} d_{23} \delta_2 (\lvert\delta_2\rvert/\pi - 1)}{L_{12}\omega} + \frac{V_3^2 d_{23} (\lvert\delta_{23}\rvert/\pi - 1)\delta_{23}}{L_{23}\omega}$
$P_3 = \frac{V_3^2 d_{13} \delta_3 (\lvert\delta_3\rvert/\pi - 1)}{L_{13}\omega} - \frac{V_3^2 d_{23} (\lvert\delta_{23}\rvert/\pi - 1)\delta_{23}}{L_{23}\omega}$

where $\delta_{23} = \delta_3 - \delta_2$.

The case corresponding to 'port 2 to port 3 and port 1 idle' is similar than the case 'port 1 to port 3 and port 2 idle', then will not be described.

3.1 Determination of L_{12}

For the case of study presented in Section 2, it will be considered that is not necessary to transfer power between the storage devices, connected in ports 1 and 2, that means $P_{12} = 0$.

The condition $P_{12} = 0$ suggests that it is possible to increase the inductance L_{12} in order to reduce the circulating current, consequently decreasing losses. Ideally, it could be an open circuit in the Δ-equivalent circuit shown in Fig. 1*c*.

3.2 Determination of L_{13} and L_{23}

Once defined the power requirements, P_{13} and P_{23}, it is possible to determine L_{13} and L_{23} from (7) as follows:

$$L_{13} = \frac{d_{13} V_3^2 \pi}{4\omega P_{13}}, \quad (8)$$

$$L_{23} = \frac{d_{23} V_3^2 \pi}{4\omega P_{23}}, \quad (9)$$

where phase shifts δ_3 and δ_{23} are evaluated for $\pi/2$ [rad] to achieve the maximum power transference. Conversion ratios, d_{23} and d_{13}, correspond to the minimum admissible voltage in the energy storage systems, which it is the worst case to be able to transfer the required power.

3.3 Determination of $L_{\ell 1}$, $L'_{\ell 2}$ and $L'_{\ell 3}$

In order to size the auxiliary inductances shown in the *Y*-equivalent circuit of Fig. 1*c*, a transformation Δ–*Y* can be used as follows:

$$L_{\ell 1} = \frac{L_{12} L_{13}}{L_{12} + L_{13} + L_{23}}, \quad (10)$$

$$L'_{\ell 2} = \frac{L_{12} L_{23} n_2^2}{L_{12} + L_{13} + L_{23}}, \quad (11)$$

$$L'_{\ell 3} = \frac{L_{13} L_{23} n_3^2}{L_{12} + L_{13} + L_{23}}, \quad (12)$$

It is possible to conclude from these expressions that when L_{12} tends to infinity, $L_{\ell 3}$ tends to zero. This indicates that it is possible to remove the auxiliary inductor $L'_{\ell 3}$ shown in Fig. 1.

By replacing (8) and (9) into (10) and (11), respectively, and considering that $L_{12} \to \infty$, it can be concluded that $L_{\ell 1} = L_{13}$ and $L'_{\ell 2} = L_{23} n_2^2$.

Transformation ratios n_2 and n_3 can be determined using (5) and (6) and the DC voltage energy storage units.

As it will be demonstrated in Sections 4.3 and 5, this proposed of method to size the auxiliary inductances can reduce the converter total losses, size, weight and consequently cost.

4 Power losses modelling

Semiconductor conduction and switching losses as well as transformer losses and those in the auxiliary inductor magnetic cores and windings [19], are considered in this paper and obtained as follows.

4.1 Losses in semiconductor switches

To calculate losses in semiconductor switches, data supplied by the manufacturer are used: voltage drop in conduction, energy dissipation during switching, both as functions of the current flowing through the switches.

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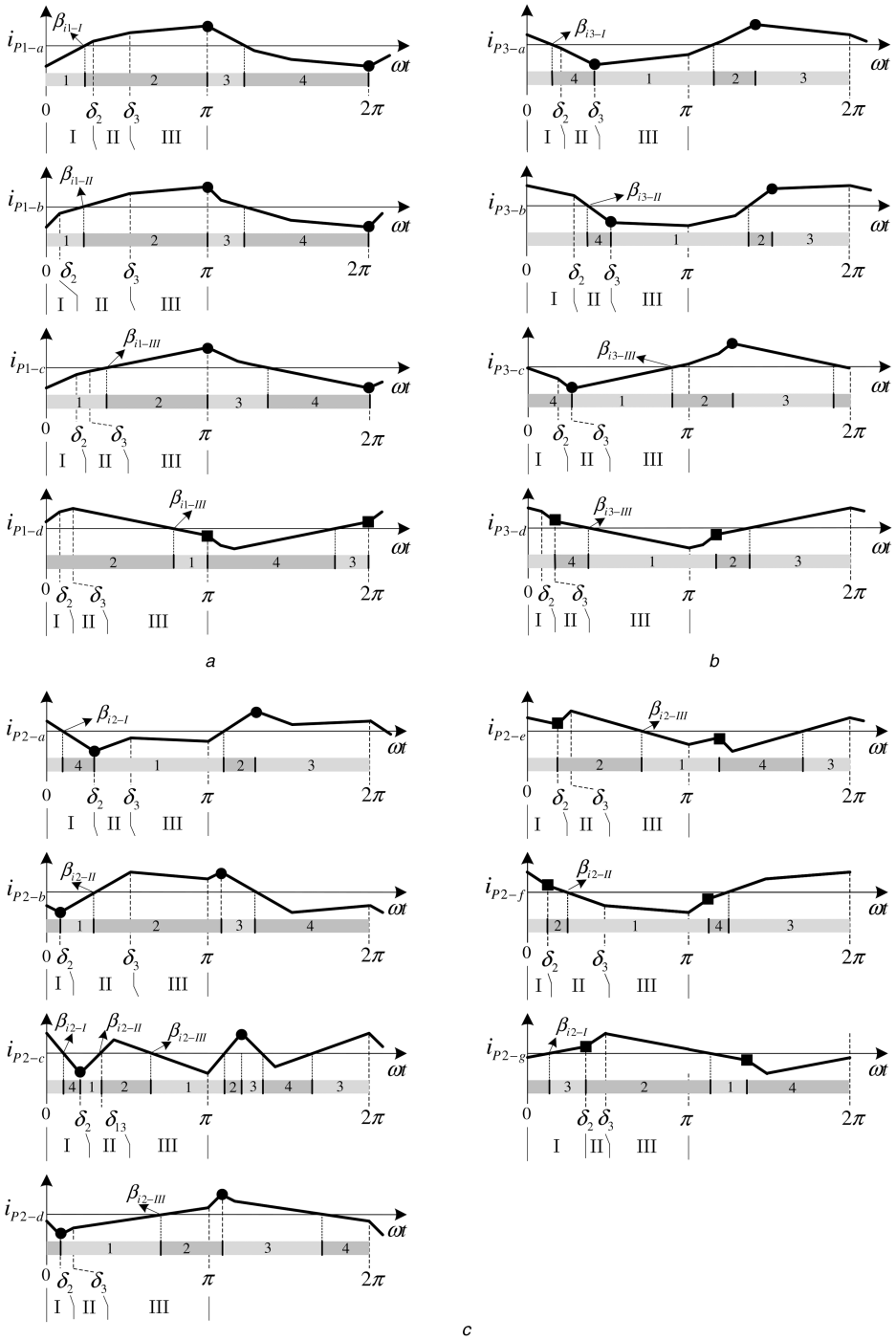

Fig. 2 *Converter AC current waveforms for each port, where 1, 2, 3 and 4 are the conduction intervals; (white square) corresponds to the instants and magnitudes of currents at which the transistors turn-on and diodes turn-off with switching losses; (open circle) corresponds to the instants and magnitudes of currents when the transistors turn-off with switching losses*

(a) Current waveforms at port 1, ***(b)*** Current waveforms at port 3, ***(c)*** Current waveforms at port 2

Conduction losses in IGBT transistors depend on collector–emitter voltage during the on-state and of the currents flowing through them [20], which can be expressed as

$$P_{cTx} = \frac{1}{2\pi}\int_{\gamma_1}^{\gamma_2} V_{CEsat(i_{Px})} i_{Px}\, \mathrm{d}\theta, \tag{13}$$

where $V_{CEsat(i_{Px})}$ represents voltage drop in the power transistor during the on-state as a function of the current flowing through port x.

Conduction losses in diodes can be determined as

$$P_{cDx} = \frac{1}{2\pi}\int_{\gamma_1}^{\gamma_2} \left(-V_{F(i_{Px})} i_{Px}\right)\mathrm{d}\theta, \tag{14}$$

where $V_{F(i_{Px})}$ is the diode forward voltage drop as a function of the current flowing through port x.

To evaluate (13) and (14), it is necessary to determine the angles γ_1 and γ_2, which determine the conduction interval for each device. These angles are obtained from the expressions β_{ix-z} shown in Table 3 and the phase shifts δ_1, δ_2 and δ_3 using the information in Figs. 2*a*–*c*. For instance, for the waveform of i_{P1-a} shown in Fig. 2*a*, $\gamma_1 = 0$ and $\gamma_2 = \beta_{i1-I}$ for D_{11} and D_{14}; whereas for $\gamma_1 = \beta_{i1-I}$ and $\gamma_2 = \pi$ for T_{11} and T_{14}.

Then, the total conduction losses at port x are

$$P_{cx} = P_{cTx} + P_{cDx}. \tag{15}$$

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Switching losses occur when any device is switched on/off under hard switching. On the contrary, when a device is switched on/off under soft switching, switching losses can be neglected. Then, power losses when the transistors are switched on/off can be determined as [20]

$$P_{swx} = E_{sw(i_{Px})} f_s k_{sw}, \tag{16}$$

whereas losses due to reverse recovery diodes can be determined as

$$P_{Dxoff} = E_{rr(i_{Px})} f_s k_{rr}, \tag{17}$$

where $E_{sw(i_{Px})}$ is the energy dissipated during switching on ($E_{on(i_{Px})}$) or off ($E_{off(i_{Px})}$) of the transistors, and $E_{rr(i_{Px})}$ is the energy due to reverse recovery diodes. The constants k_{sw} and k_{rr} are parameters which are functions of the resistance at the gate and voltage at the collector–emitter. These parameters allow adjusting the energy data supplied by the manufacturer, which were obtained with different parameters of the TAB converter implemented in this work [21].

Currents to calculate the previous stated losses and the instantaneous currents at the switching instants, shown in Table 4, can be obtained from expressions shown in Table 1.

Finally, total losses at the semiconductor switches of bridge B_x can be determined as

$$P_{tswx} = P_{cx} + \left(P_{swx} + P_{Dxoff}\right). \tag{18}$$

4.2 Losses in the transformer and auxiliary inductances

In this work, losses in the transformer and in the auxiliary inductances are determined as the sum of the resistive losses in each winding and the losses in the magnetic cores [22].

Resistive losses in each winding can be calculated as

Table 3 Expressions for the zero-crossing angle at each port

$$\beta_{i1-\mathrm{I}} = \frac{2L_{12}\delta_3 + 2L_{13}d_{23}\delta_2 + \alpha_1}{2(L_{12} + L_{12}d_{13} + L_{13}d_{13} + L_{13}d_{23})}$$

$$\beta_{i1-\mathrm{II}} = \frac{2L_{12}\delta_3 - 2L_{13}d_{23}\delta_2 + \alpha_1}{2(L_{12} + L_{12}d_{13} + L_{13}d_{13} - L_{13}d_{23})}$$

$$\beta_{i1-\mathrm{III}} = \frac{2L_{12}\delta_3 + 2L_{13}d_{23}\delta_2 - \alpha_1}{2(L_{12} - L_{12}d_{13} - L_{13}d_{13} + L_{13}d_{23})}$$

$$\beta_{i2-\mathrm{I}} = \frac{2d_{23}\delta_2(L_{12} + L_{23}) - 2L_{12}\delta_3 + \alpha_2}{2(L_{12}d_{23} - L_{12} + L_{23}d_{13} + L_{23}d_{23})}$$

$$\beta_{i2-\mathrm{II}} = \frac{2d_{23}\delta_2(L_{12} + L_{23}) + 2L_{12}\delta_3 - \alpha_2}{2(L_{12}d_{23} + L_{12} - L_{23}d_{13} + L_{23}d_{23})}$$

$$\beta_{i2-\mathrm{III}} = \frac{-2d_{23}\delta_2(L_{12} + L_{23}) - 2L_{12}\delta_3 + \alpha_2}{2(-L_{12}d_{23} + L_{12} + L_{23}d_{13} - L_{23}d_{23})}$$

$$\beta_{i3-\mathrm{I}} = \frac{2\delta_3(L_{13} + L_{23}) - 2L_{13}d_{23}\delta_2 + \alpha_3}{2(L_{13} + L_{23} - L_{13}d_{23} + L_{23}d_{13})}$$

$$\beta_{i3-\mathrm{II}} = \frac{2\delta_3(L_{13} + L_{23}) + 2L_{13}d_{23}\delta_2 + \alpha_3}{2(L_{13} + L_{23} + L_{13}d_{23} + L_{23}d_{13})}$$

$$\beta_{i3-\mathrm{III}} = \frac{2\delta_3(L_{13} + L_{23}) - 2L_{13}d_{23}\delta_2 - \alpha_3}{2(L_{13} + L_{23} - L_{13}d_{23} - L_{23}d_{13})}$$

where $\alpha_1 = -\pi L_{12} - \pi L_{12}d_{13} - \pi L_{13}d_{13} + \pi L_{13}d_{23}$, $\alpha_2 = \pi L_{12} - \pi L_{12}d_{23} + \pi L_{23}d_{13} - \pi L_{23}d_{23}$, $\alpha_3 = -\pi L_{13} - \pi L_{23} + \pi L_{13}d_{23} + \pi L_{23}d_{13}$

Table 4 Current expressions for each port, evaluated at the corresponding switching angles

$$i_{P1}(\delta_1) = -\frac{V_3(k_1 + \pi L_{12}(d_{13} - 1) + \pi L_{13}(d_{13} - d_{23}))}{2L_{13}L_{12}\omega}$$

$$i_{P2}(\delta_2) = -\frac{V_3(k_2 + \pi L_{12}(d_{23} - 1) + \pi L_{23}(d_{23} - d_{13})}{2L_{12}L_{23}n_2\omega}$$

$$i_{P3}(\delta_3) = -\frac{V_3(k_3 + \pi L_{23}(1 - d_{13}) + \pi L_{13}(1 - d_{23}))}{2L_{13}L_{23}n_3\omega}$$

where $k_1 = 2d_{23}\delta_2 L_{13} + 2\delta_3 L_{12}$, $k_2 = 2L_{23}d_{13}\delta_2 - 2L_{12}\delta_{23}$, $k_3 = 2L_{23}d_{13}\delta_3 - 2L_{13}d_{23}\delta_{23}$

$$P_{cux} = I^2_{rmsx}(R_{trx}), \tag{19}$$

where I_{rmsx} is the rms current, and R_{trx} is the effective resistance of the winding for port x.

Losses in the magnetic cores are proportional to the magnetic flux, the core volume and the voltage waveforms. To simplify the calculation of these losses, the transformer is assumed to be supplied with a sinusoidal voltage waveform, which allows using the following expression [23]:

$$P_{core\,x} = V_c K_c f_s^{\alpha_c} B^{\beta_c}, \tag{20}$$

where V_c is the volume of the core, f_s is the switching frequency, B is the flux density, K_c, α_c and β_c are the core parameters which can be determined from data provided by the manufacturer.

Then, the transformer total losses can be determined as

$$P_{tr} = \sum_{x=1}^{3} (P_{cux}) + P_{core}. \tag{21}$$

Finally, total losses can be obtained as

$$P_t = P_{tswx} + P_{tr} + P_{ai}\ . \tag{22}$$

The term P_{ai} corresponds to the losses produced in the auxiliary inductors. Such losses are determined using the expressions (19) and (20).

4.3 Evaluation of converter total losses

Fig. 3 shows a flowchart of the algorithm developed to evaluate the converter total losses, described as follows:

Step 1: The algorithm is initialised by assigning the converter parameter, the initial d_{23} and d_{13} as well as the requirements for the power transferred P_1, P_2 and P_3.

Step 2: The angles δ_1, δ_2 and δ_3 are determined from the expressions in Table 2 for each set of values d_{23} and d_{13}.

Step 3: The conduction intervals γ_1 and γ_2 are determined for each device using data from the current zero-crossings (Table 3) and the current waveforms shown in Figs. 2*a*–*c*.

Step 4: Conduction losses in the semiconductor switches, resistive losses in the transformer windings and the auxiliary inductors as well as losses in the magnetic cores are evaluated using (13)–(15) and (19)–(21), respectively.

Step 5: Switching mode of the switches is determined (transistors and diodes hard switching during turn-on and off) according (16), (17) and (22).

Step 6: Voltage conversion ratios are increased according to Δd_{23} and Δd_{13} which makes the process return to step 2.

This algorithm can be used for any TAB application. However, as a case of study, the characteristics are shown in Table 5.

Fig. 4 shows the total losses evaluation of the TAB converter expressed in pu respect to $P_b = 2$ kW, for different cases of power transference. The evaluations were carried out for two sets of auxiliary inductances, grey areas correspond to $L_{12} = L_{13} = L_{23}$ and the black to $L_{13} = L_{23}$ with $L_{12} \to \infty$. Transfer power positive values indicate that the port transfers power, whereas negative values indicate that the port receives power.

It can be concluded from Fig. 4 that the total losses in the converter are reduced considerably when the auxiliary inductances are dimensioned according to the criteria stated in Section 3. For example, when ports 1 and 2 transfer 1 pu to port 3, as it was shown in Fig. 4*a*, for a $d_{23} = 0.6$ and $d_{13} = 1.4$, the total losses are reduced in 0.13 pu. For the case when port 1 transfer 1 pu to port 3, with a $d_{23} = 1.5$ and $d_{13} = 0.8$, the total losses reduce 0.05 pu. For the case when port 3 transfer 0.5 pu to port 1 and 0.5 pu to port 2, with a $d_{23} = 1.5$ and $d_{13} = 0.8$, the total losses reduce 0.075 pu.

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5 Determination of the maximum converter power flow capability

The objective of this section is to determine the maximum power flow converter capability, considering the restrictions due to maximum semiconductors current capability and semiconductor losses.

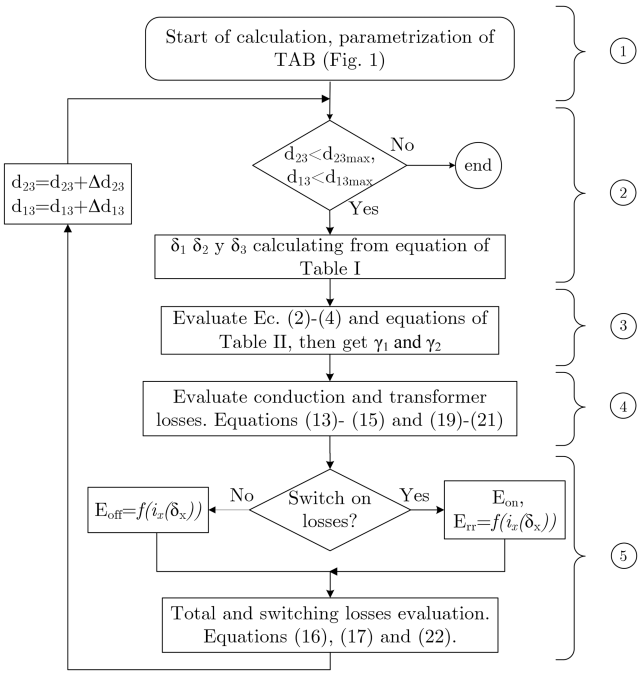

Fig. 3 *Flowchart of the implemented algorithm for calculation of losses*

5.1 Restrictions due to maximum currents

Using the current expressions shown in Table 1, allows to obtain the peak values of the currents for different power transfer cases as a function of the phase shifts, δ_2 and δ_3, and the voltage conversion ratios, d_{23} and d_{13}.

Figs. 5*a* and *b* show the peak values of the currents in ports 1 and 2, respectively, related to different voltage conversion ratios, normalised respect to $I_b = V_3/(\omega \,.\, L_b)$. The power transfer are $P_1 = 0.75$, $P_2 = 0.25$ and $P_3 = -1$ pu. The grey areas correspond to the case when the auxiliary inductances are $L_{12} = L_{13} = L_{23}$ and the black areas correspond to $L_{13} = L_{23}$ with $L_{12} \to \infty$. It can be deduced from these figures that a considerable increase in the currents peak values are produced when the auxiliary inductances take the same values and when the voltage conversion ratios are different than 1. Because current at port 3 is equal in both cases, it is not included in Fig. 5.

Based on the knowledge of the AC converter currents, is possible to calculate the transferred power flow as a function of the voltage conversion ratios considering a maximum admissible current supported by the converter (semiconductors and magnetic cores saturation).

Fig. 6 shows the maximum power that the converter is able to transfer, limited by the maximum currents, expressed in pu, as a function of d_{13} and with d_{23} as a parameter, and considering a constant voltage at port 3. These results correspond to ports 1 and 2 transferring power to port 3, and port 3 transferring power to ports 1 and 2. It can be demonstrated that similar results are obtained when port 1 transfers power to port 3. Figs. 6*a* and *b* show the maximum power able to be transferred for $L_{12} = L_{13} = L_{23}$, whereas Figs. 6*c* and *d* show the same case for $L_{13} = L_{23}$ with $L_{12} \to \infty$.

In Figs. 6*a* and *b*, when $L_{12} = L_{13} = L_{23}$, it can be concluded that a reduction in d_{23} or d_{13} produce a decrease in the maximum power transferred, almost to zero, due to the maximum current limitation. Compared Figs. 6*a* and *b* with Figs. 6*c* and *d*, it can be concluded

Table 5 Parameters of the experimental converter

power at nominal DC ports voltage[a]		4.8 kW	
power at minimal DC ports voltage[a,b]		3.3 kW	
DC nominal voltages	$V_1 = 340$ V	$V_2' = 150$ V	$V_3' = 150$ V
V_1 voltage range		Min. 204 V	Max. 544 V
V_2' voltage range		Min. 90 V	Max. 240 V
HF turns ratio		$n_2 = n_3 = 0.44$	
switching frequency f_s		20 kHz	
B_1 and B_2 IGBT/FWD		SKM150GB12T4G (Semikron)	
B_3 IGBT/FWD		BSM150GB60DLC (Infineon)	
μ controller		DSP T.I. TMS320F28335	
auxiliary inductors	$L_{\ell 1}$	$L_{\ell 2}'$	$L_{\ell 3}'$
$L_{12} = L_{13} = L_{23}$	100 μHy	19.36 μHy	19.36 μHy
$L_{13} = L_{23}, L_{12} \to \infty$	300 μHy	58.09 μHy	0 μHy

[a]Considering power transfer with the maximum phase-shift.

[b]Without consider maximum port current limitations.

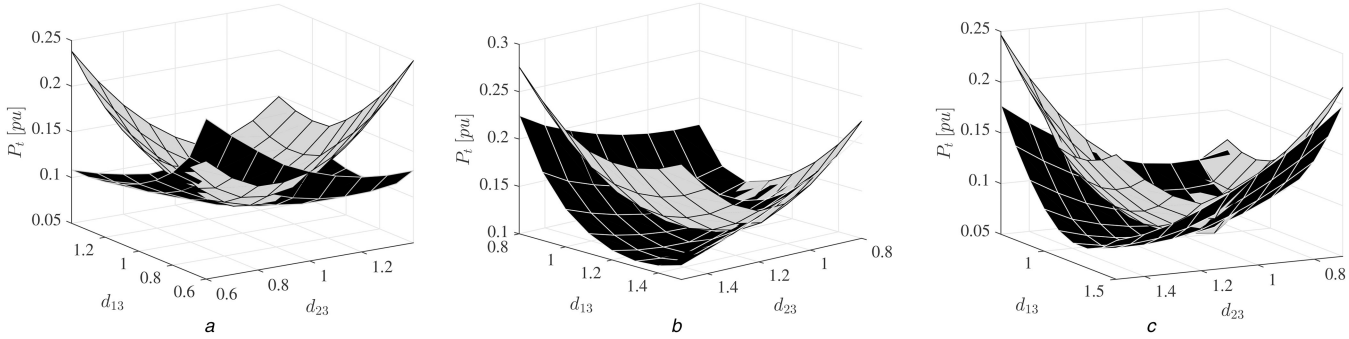

Fig. 4 *Converter total losses for different cases of power transference and different values of auxiliary inductances*
(a) Ports 1 and 2 transfer 1 pu to port 3, ***(b)*** Port 1 transfer 1 pu to port 3, ***(c)*** Port 3 transfer 0.5 pu to port 1 and 0.5 pu to port 2

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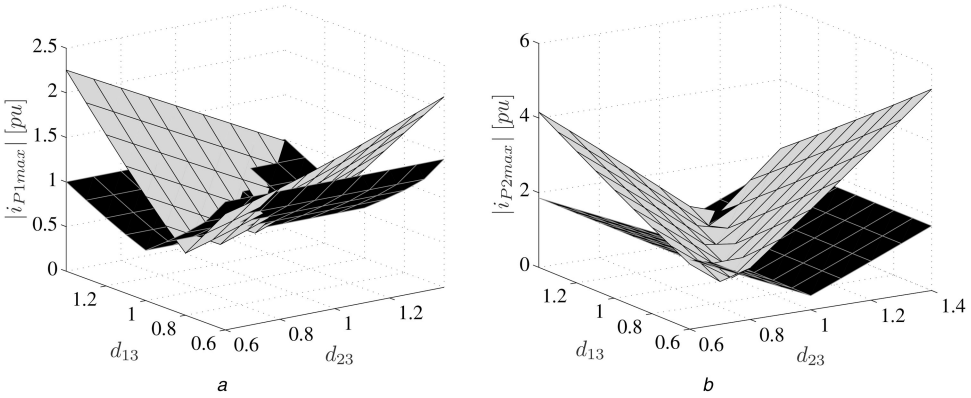

Fig. 5 *Peak currents as function of the voltage conversion ratios for $P_1 = 0.75$, $P_2 = 0.25$ and $P_3 = 1$ pu, where grey areas correspond to $L_{12} = L_{13} = L_{23}$ and black areas correspond to $L_{13} = L_{23}$ with $L_{12} \to \infty$*

(a) Port 1, ***(b)*** Port 1

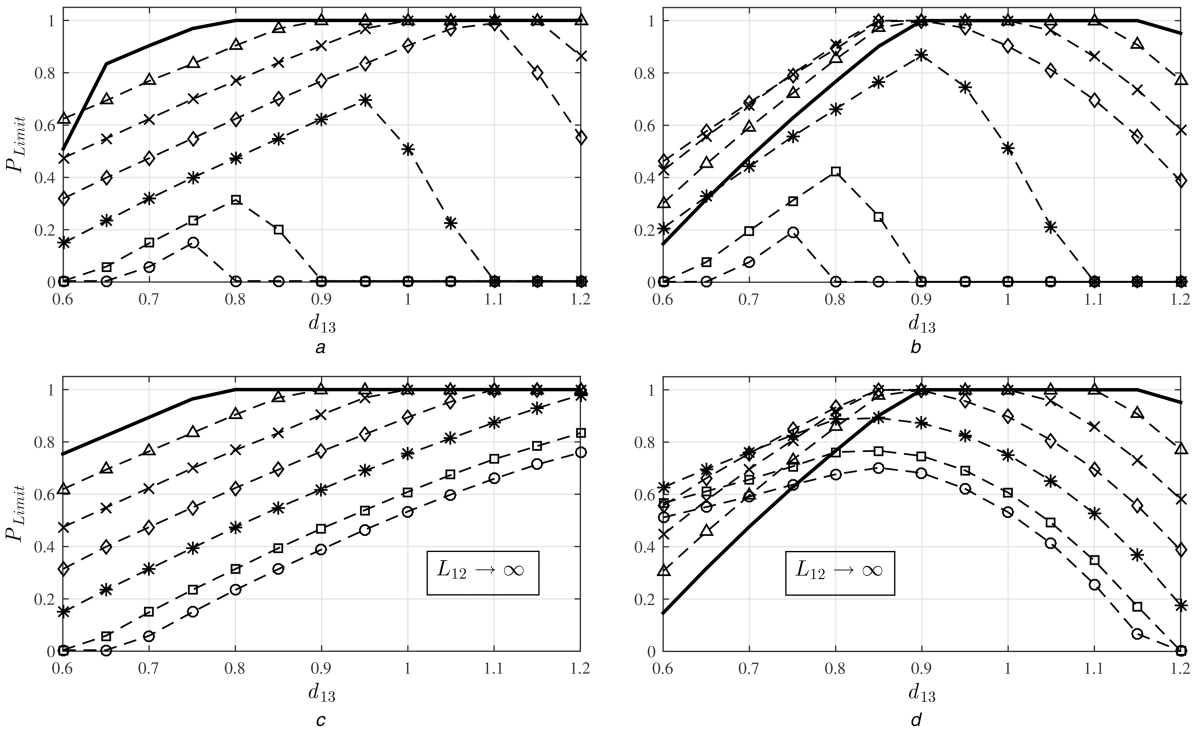

Fig. 6 *Maximum power able to be transferred, with current restrictions, as a function of d_{13} and with d_{23} as a parameter, where $d_{23} = 1$ corresponds to the solid line, $d_{23} = 0.9$* (open up − right triangle), *$d_{23} = 0.8$*(multiplication symbol), *$d_{23} = 0.7$* (diamond symbol), *$d_{23} = 0.6$*(asterisk), *$d_{23} = 0.5$* (open square), *$d_{23} = 0.45$* (open circle)

(a) Ports 1 and 2 transfer to port 3, ***(b)*** Port 3 transfers to ports 1 and 2, ***(c)*** Ports 1 and 2 transfer to port 3, ***(d)*** Port 3 transfers to ports 1 and 2

that when $L_{13} = L_{23}$ with $L_{12} \to \infty$ the maximum power transferred increases for all the voltage conversion ratios.

The previous analysis demonstrated that with a proper sizing of the auxiliary inductances is possible to increase the power transferred considerably. For example, when ports 1 and port 2 transferred 50% of the power each one to port 3, as it was shown in Fig. 6*c*, for a $d_{23} = 0.6$ and $d_{13} = 1.1$, the maximum power transferred can be increased in 0.87 pu. In the case when port 3 transferred to ports 1 and 2, 50% of power to each one, with a $d_{23} = 0.5$ and $d_{13} = 0.9$, the maximum power transferred can be increased in 0.75 pu.

Fig. 7 shows the effect of the uncertainty in the values of the auxiliary inductances on the maximum power transfer capability, when $d_{23} = 0.6$, using the same procedure as above. Different percentages of uncertainty were considered in the inductances L_{13} and L_{23}. The inductance L_{12} is kept constant for both cases: $L_{12} = L_{13} = L_{23}$ and $L_{13} = L_{23}$ with $L_{12} \to \infty$.

According to these results, it can be concluded that uncertainty in the values of the auxiliary inductances produce similar variation in the maximum power that can be transferred for both cases: $L_{12} = L_{13} = L_{23}$ and $L_{13} = L_{23}$ with $L_{12} \to \infty$.

In all the cases evaluated, the maximum variation of the maximum power that can be transferred is always close to the percentage of the uncertainty in the value of the auxiliary inductances, for the range of variation of d_{13} presented in Fig. 7.

Furthermore, it can be concluded that the improvement in the power transfer capability of the converter, considering both sets of auxiliary inductances, is maintained.

5.2 Restrictions due to semiconductor losses

Using the power losses modelling presented in Section 4, it will be determined and compare the converter thermal constraints due to the maximum semiconductors temperature [24] when $L_{12} = L_{13} = L_{23}$, and $L_{13} = L_{23}$ with $L_{12} \to \infty$.

Figs. 8*a* and *b* show the switches losses at bridges 1 and 2, respectively. Losses at bridge 3 are not represented in these figures as they have not difference between the two sets of inductances.

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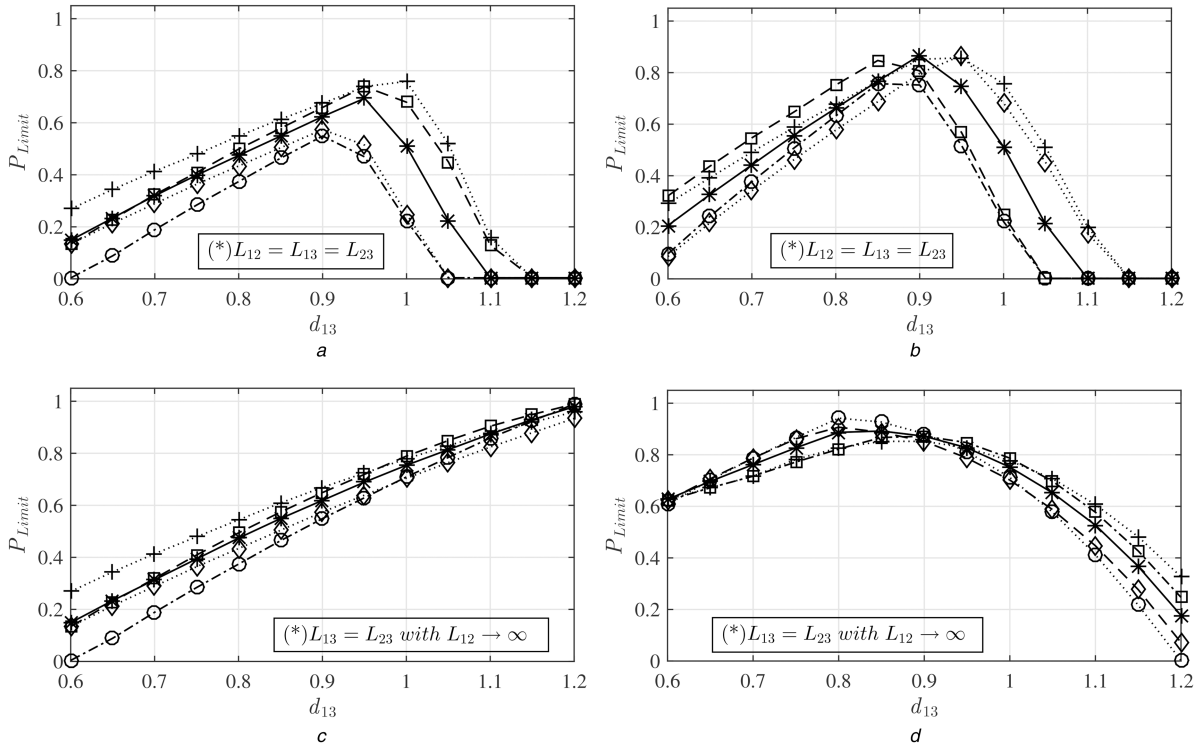

Fig. 7 *Maximum power able to be transferred, with current restrictions, as a function of d_{13} when $d_{23} = 0.6$, considering an uncertainty of ±10% in the values of the auxiliary inductances L_{13} and L_{23}, where (addition symbol) corresponds to + 10% in L_{13} and +10% in L_{23}, (open circle) to −10% in L_{13} and −10% in L_{23}, (*diamond symbol*) to +10% in L_{13} and −10% in L_{23} and (*open square*) to −10% in L_{13} and + 10% in L_{23}* ***(a)*** *Ports 1 and 2 transfer to port 3,* ***(b)*** *Port 3 transfers to ports 1 and 2,* ***(c)*** *Ports 1 and 2 transfer to port 3,* ***(d)*** *Port 3 transfers to ports 1 and 2*

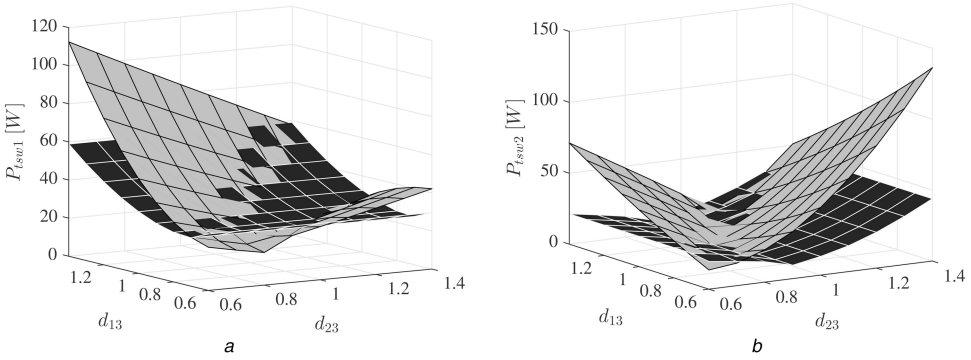

Fig. 8 *Total losses at the semiconductor switches where grey areas correspond to $L_{12} = L_{13} = L_{23}$ and black areas correspond to $L_{13} = L_{23}$, $L_{12} \to \infty$.*
(a) Bridge 1, ***(b)*** Bridge 2

Losses were calculated under the condition that port 1 transfers 1.5 kW and port 2 transfers 0.5 kW to the port 3. Similar results can be obtained for other power transference cases.

In Fig. 8, the grey areas represent losses for $L_{12} = L_{13} = L_{23}$, and black ones for $L_{13} = L_{23}$ with $L_{12} \to \infty$.

Fig. 8*a* shows that the maximum power dissipation in the switches of port 1 is $P_{tsw1} = 110$ W for the grey area, and $P_{tsw1} = 60$ W for the black area, for $d_{23} = 0.6$ and $d_{13} = 1.4$, that means a losses reduction of about 40%. Fig. 8*b* shows that the maximum power dissipation in the switches of port 2, for $d_{23} = 1.4$ and $d_{13} = 0.6$, is $P_{tsw2} = 135$ W for the grey area and $P_{tsw2} = 43$ W for the black area, that means a losses reduction of about 68.15%.

Comparing both areas in each figure, it can be concluded that by choosing a set of auxiliary inductances according to the criteria in Section 3, it is possible to reduce considerably the switches power losses. Consequently, it allows increasing the power flow capability or reducing the cooling system, reducing the converter size, weight and cost.

6 Experimental results

The analysis presented in the previous sections shows that the converter efficiency can be improved by using the auxiliary inductors designed according to Section 3. To validate this proposal and the power losses model, a laboratory prototype was implemented, and experimental results were obtained. The prototype specifications are given in Table 5. The high-frequency transformer was built using a ferrite core and a Litz wire to reduce skin effect. A digital controller to generate the phase-shift modulation was implemented using a DSP TMS320F28335 from Texas Instruments.

The evaluation and experimental measurement of losses were carried out for the three different cases of power transference presented in Section 4.3. Fig. 9 shows the calculation of losses (solid line) and experimental measurements (dotted lines) considering the sets of auxiliary inductances presented in the previous sections. All the curves are function of the voltage conversion ratio d_{13}, with d_{23} as a parameter. The square marks correspond to the case $L_{12} = L_{13} = L_{23}$, and circular marks to $L_{13} = L_{23}$ with $L_{12} \to \infty$.

Fig. 9*a* shows experimental measurements of total losses for power transference $P_1 \cong 1500$, $P_2 \cong 500$ and $P_3 \cong -2000$ W. As it can be observed, for $L_{12} \to \infty$, the total losses are reduced in 100

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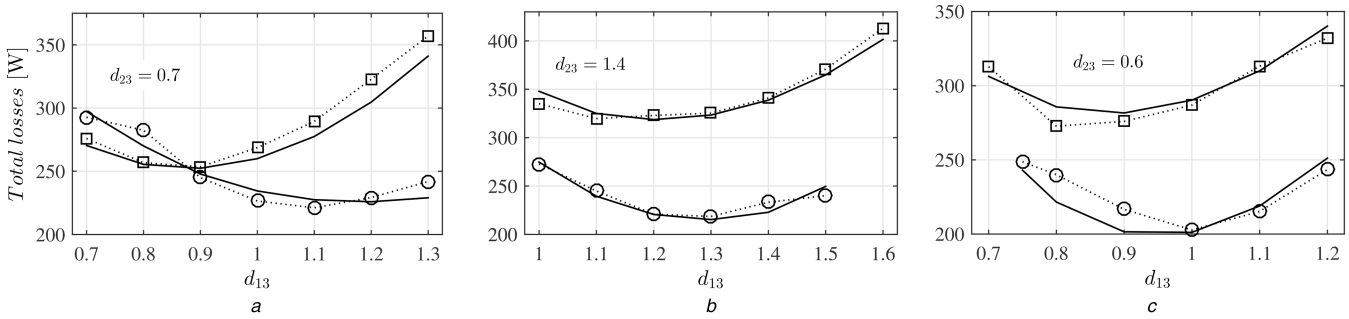

Fig. 9 *Total losses calculated (solid lines) and measured experimentally (dashed lines), where square marks correspond to $L_{12} = L_{13} = L_{23}$, and circular marks to $L_{13} = L_{23}$ with $L_{12} \to \infty$*

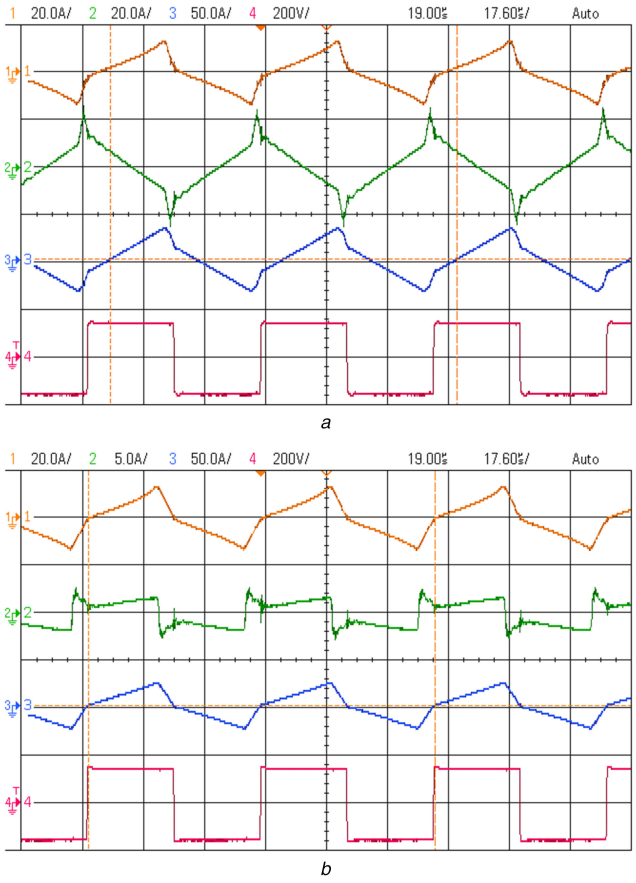

Fig. 10 *Waveforms when port 1 transfer to port 3, where i_{P1}, i_{P2} and i_{P3} correspond to channels 1, 2 and 3 of the oscilloscope, and v_{P3} corresponds to channel 4*

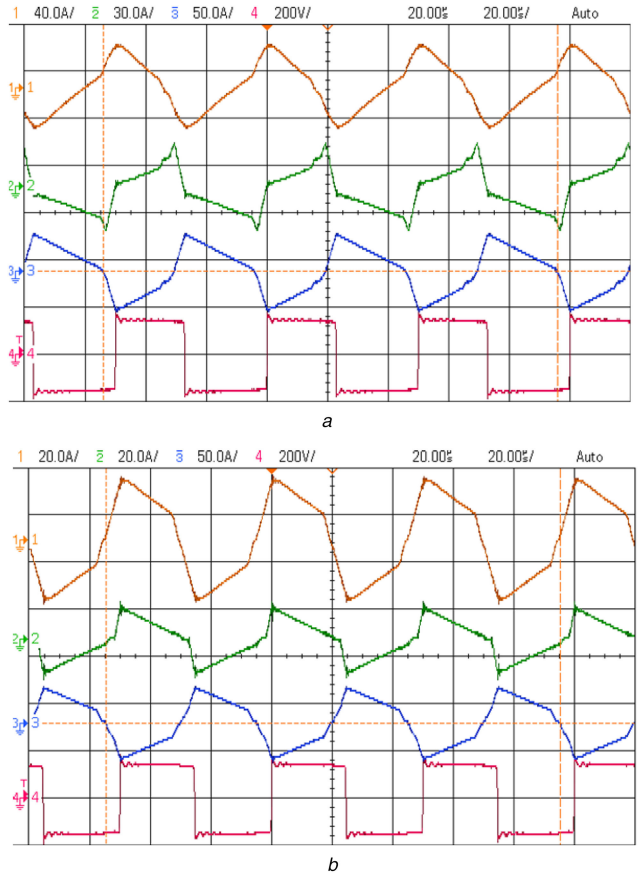

Fig. 11 *Waveforms when ports 1 and 2 transfer to port 3, where i_{P1}, i_{P2} and i_{P3} correspond to channels 1, 2 and 3 of the oscilloscope, and v_{P3} corresponds to channel 4*

W for $d_{13} = 1.3$ and $d_{23} = 0.7$, that means a reduction of about 28.5%.

From Fig. 9*b*, when power is transferred from ports 1 to 3, with $P_1 \cong 2000$, $P_2 \cong 0$ and $P_3 \cong -2000$ W, the converter total losses can be reduced up to 75 W for $d_{13} = 1$ and up to 125 W for $d_{13} = 1.5$, reducing losses about 33%.

Finally, Fig. 9*c* shows the evaluation and experimental measurements of losses for power transference $P_1 \cong -1000, P_2 \cong -1000$ and $P_3 \cong 2000$ W. It can be observed in this figure a decrease of total losses of about 80 W for $d_{13} = 1.2$ and $d_{23} = 0.6$, that means a reduction of about 32%.

Figs. 10–12 show the current waveforms for the test described before, carried out with two different sets of auxiliary inductances, defined in Table 5. Fig. 10 corresponds to port 1 transferring to port 3, with $d_{23} = 1.4$ and $d_{13} = 1.5$. Fig. 11 corresponds to ports 1 and 2 transferring to port 3, with $d_{23} = 0.9$ and $d_{13} = 0.7$. Finally, Fig. 12 corresponds to port 3 transferring to ports 1 and 2, and with $d_{23} = 0.6$ and $d_{13} = 0.9$.

Table 6 shows measured currents at switching instants and rms values. These measurements show a reduction in both variables when $L_{13} = L_{23}$ with $L_{12} \to \infty$ is used instead $L_{12} = L_{13} = L_{23}$.

Let us consider that $L_{12} = L_{13} = L_{23}$ and the semiconductor's maximum admissible currents are 22 A for ports 1 and 2, and 45 A for port 3. The experimental results presented in Fig. 10*a*, show that the peak current limitation is due to i_{P2}, because it achieves its maximum value when the power transferred at port 3 is 2 kW.

When $L_{13} = L_{23}$ with $L_{12} \to \infty$, for the same power transferred, the AC peak currents are kept below the peak current limitations indicated before, as shown in Fig. 10*b*, allowing to increase the power transfer capability.

Fig. 13 shows the experimental results when $L_{13} = L_{23}$ with $L_{12} \to \infty$ and the power transferred to port 3 is increased up to 3.6 kW. In this figure it is possible to observe that the peak value of i_{P1} reaches 22 A, which corresponds to the peak current limitation of port 1. The latter shows that it is possible to increase the power transfer capability up to 80%, if compared to the case presented in Fig. 10*a* when $L_{12} = L_{13} = L_{23}$.

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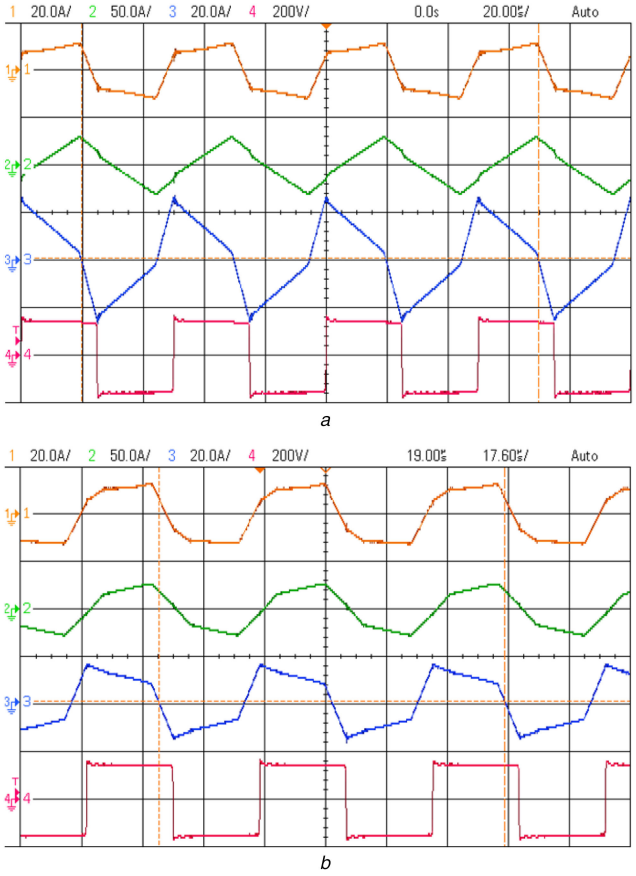

Fig. 12 *Waveforms when port 3 transfer to ports 1 and 2, where i_{P3}, i_{P2} and i_{P1} correspond to channels 1, 2 and 3 of the oscilloscope, and v_{P1} corresponds to channel 4*

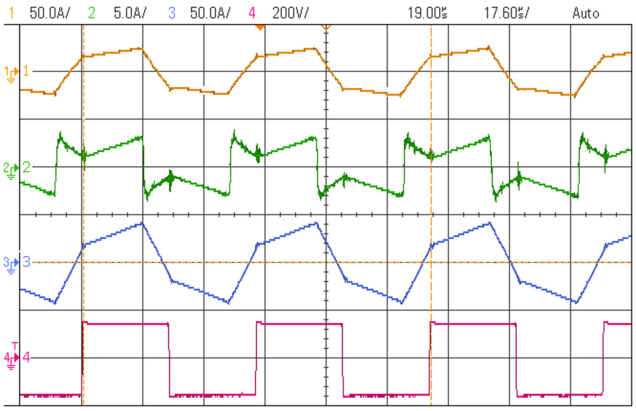

Fig. 13 *Experimental waveforms when port 1 transfers a magnitude of power equal to 3.6 kW to port 3, where i_{P1}, i_{P2} and i_{P3} correspond to channels 1, 2 and 3 of the oscilloscope, respectively; and v_{P3} corresponds to channel 4*

7 Conclusion

A three-port DC–DC converter to be used in hybrid energy storage systems was analysed in this paper. The principle of operation, including the power flow analysis and the determination of the current waveforms for different operating conditions was stated. The core of this paper is a proposal to size the converter auxiliary inductances so as to reduce de converter currents and losses. Different cases of power transference were analysed and as a result it was concluded that the inductance not involved with the ports exchanging energy can be removed, whereas the rest of the auxiliary inductances can be sized in order to allow transferring the maximum required power. Moreover, a model to evaluate the total converter losses, including semiconductors and magnetic core losses, was proposed. Based on the power flow and the current waveforms analysed before, it was deduced the maximum converter power flow capability as function of maximum currents and losses supported by the semiconductors. To validate the proposal and to demonstrate its practical feasibility, a laboratory prototype was implemented and experimental results were obtained. These results were in close agreement with the theoretical calculations. Based on the experimental results obtained using the proposed methodology, which consists of properly size the auxiliary inductances, the following improvements were obtained: total converter losses were reduced up to about 40%, and the power transfer capability was increased up to 80%.

Table 6 Experimental measurements of the currents at switching instants and its rms values

Variable	$L_{12} = L_{13} = L_{23}$	$L_{13} = L_{23}, L_{12} \to \infty$	Diff., %
	$P_1 \to P_3$		
$i_{P1}(0)$	−13.3 A	−13.17 A	−0.977
$i_{P2}(\delta_2)$	22.03 A	2.13 A	−90.33
$i_{P3}(\delta_3)$	−7.89 A	3.1 A	−60.71
I_{1rms}	10.88 A	10.32 A	−5.14
I_{2rms}	12.52 A	1.88 A	−84.98
I_{3rms}	14.71 A	13.67 A	−7.07
	$P_1\&P_2 \to P_3$		
$i_{P1}(0)$	12.8 A	0.85 A	−93.36
$i_{P2}(\delta_2)$	27.6 A	1.21 A	−95.61
$i_{P3}(\delta_3)$	42.5 A	38.75 A	−8.82
I_{1rms}	21.42 A	17.32 A	−19.14
I_{2rms}	6.72 A	6.46 A	−3.87
I_{3rms}	24.66 A	23.67 A	−4.01
	$P_3 \to P_1\&P_2$		
$i_{P1}(\delta_1)$	25.75 A	14.63 A	−43.18
$i_{P2}(\delta_2)$	7.51 A	15.83 A	110.78
$i_{P3}(0)$	7.11 A	12.57 A	76.79
I_{1rms}	14.51 A	8.23 A	−43.28
I_{2rms}	15.26 A	12.62 A	−17.3
I_{3rms}	8.7 A	8.3 A	−4.59

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