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A Robust Low Power Static Random Access Memory Cell Design

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A ROBUST LOW POWER STATIC RANDOM ACCESS MEMORY CELL DESIGN

A Thesis in partial fulfillment of the
requirements for the degree of
Master of Science in Electrical Engineering

by

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WRIGHT STATE UNIVERSITY

GRADUATE SCHOOL

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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY A.V. Rama Raju Pusapati ENTITLED A Robust Low Power Static Random Access Memory Cell Design BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Electrical Engineering.

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ABSTRACT

Pusapati, A.V. Rama Raju. M.S.E.E, Department of Electrical Engineering, Wright State University, 2018. A Robust Low Power Static Random Access Memory Cell Design

Stability of a Static Random Access Memory (SRAM) cell is an important factor when considering an SRAM cell for any application. The Static Noise Margin (SNM) of a cell, which determines the stability, varies under different operating conditions. Based on the performance of three existing SRAM cell designs, 6T, 8T and 10T, a 10 Transistor SRAM cell is proposed which has good stability and has the advantage of reduced read power when compared to 6T and 8T SRAM cells. The proposed 10T SRAM cell has a single-ended read circuit which improves SNM over the 6T cell. The proposed 10T cell doesn't require a pre-charge circuit and this in-turn improves read power and also reduces the read time since there is no need to pre-charge the bit-line before reading it. The Read SNM and Hold SNM of the proposed cell at a VDD of 1V and at 25˚C is 254mV. The measured RSNM, HSNM and Write SNM at temperatures 0˚C, 40˚C, 80˚C and 120˚C and also at supply voltages 1V, 0.8V and 0.6V show the design is robust. The Write SNM of the proposed cell at a VDD of 1V and Pull-up Ratio of 1 is 275mV. Finally, a 32-byte memory array is built using the proposed 10T SRAM cell and the read, write times are 149ps and 21.6ps, respectively. The average power consumed by the 32-byte array over a 12ns period is 13.8uW. All the designs are done in the 32nm FinFET technology.

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1. Introduction

As the feature size and voltage levels of chip design technologies decrease, high-performance power efficient circuits/components become greatly important. Static Random Access Memory (SRAM) is the fastest computer memory [1]. SRAM is embedded into the processor as Cache Memory at various levels. Levels L1 and L2 are confined to a particular processor core and L3 is shared by all the processor cores. Cache memory is the closest memory to the processor and occupies a large amount of portion on the chip. The amount of cache memory in modern day computers is increasing in order to make the systems faster. It is important that SRAM is power efficient and is robust to process voltage and temperature (PVT) changes. Reducing supply voltage reduces the overall power consumption, but will affect data stability. Three existing SRAM cell designs are considered in this thesis where their performance is tested. A novel 10T SRAM cell is proposed which addresses the stability and power issues. The proposed cell's stability is tested at various supply voltages and temperatures.

The thesis is organized as follows,

Chapter 1 discusses the basic computer memory classification. Chapter 2 talks about three existing SRAM cell designs including the conventional 6T cell and then describes the proposed cell design. The basic operations of an SRAM bit-cell are described and the concept of Static Noise Margin (SNM) is introduced. Chapter 3 discusses the simulation

results of the proposed SRAM cell and compares the results to the existing cell designs. The stability of the proposed cell is measured under different supply voltages and temperatures. Chapter 4 gives the conclusion of this work.

1.1 Memory Types

"Computer Memory" is defined as any physical device that can store information/data. The stored information could either be temporary or permanent. The following *Figure 1* shows the basic classification of computer memory.

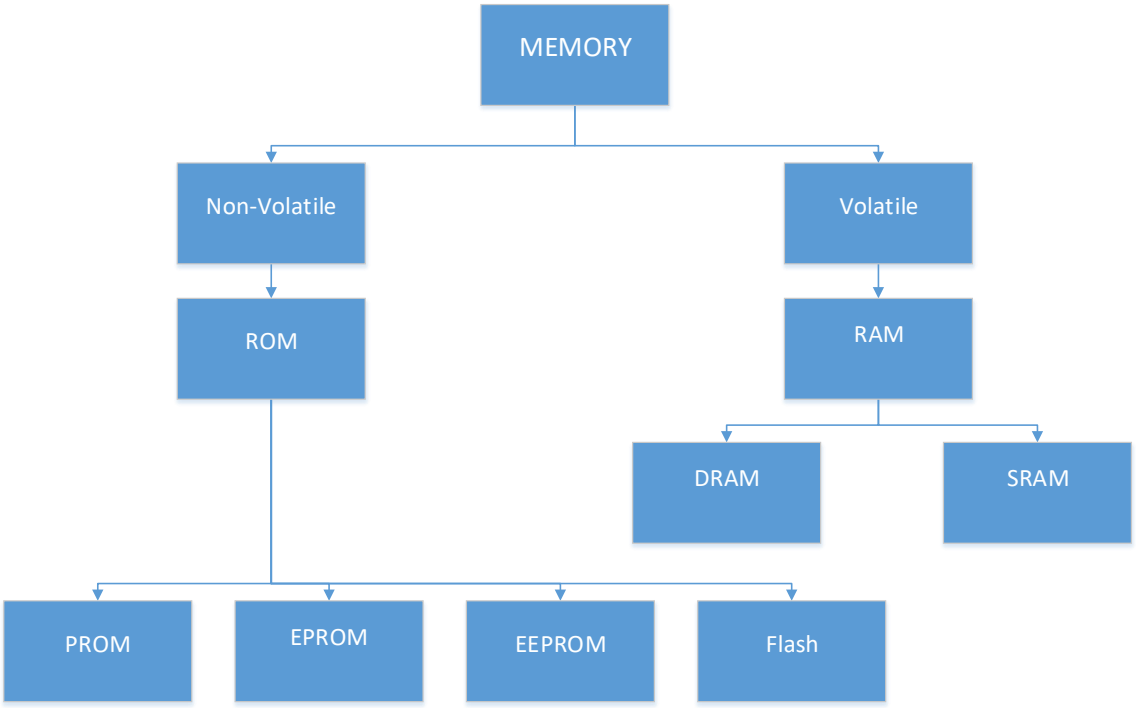

Figure 1 Memory Classification [2]

1.1.1 Non-Volatile Memory (NVM)

Non-volatile memory is the type of memory that can retain the data even in the absence of power. The computer storage devices like flash drives, Hard Disk Drives (HDD), Solid State Drives (SSD), optical discs etc., are some examples of Non-Volatile Memory.

1.1.2 Read Only Memory (ROM)

Read Only Memory refers to a type of memory that can only be read. The data written to it cannot be altered after the initial write operation i.e., the data written to a ROM is hard wired onto it during the manufacturing. However, certain types of ROM allow for the data to be re-written onto them, but, it is a rather difficult and slow process and requires special equipment. Because of the nature of ROM, it is used in applications where a piece of data is to be present permanently. For example, the Basic Input Output System (BIOS), which is the boot firmware that runs the computer until the operating system takes over, is programed onto a ROM. Some other applications like washing machines and television sets have their operating systems programed onto a ROM since they need not be updated.

The following *Figure 2* shows the schematic of a 4 word*4 bit Mask ROM in which the presence or absence of a transistor determines the data bit value [3]. As it can be seen from the figure, the data is written during fabrication and it is permanent.

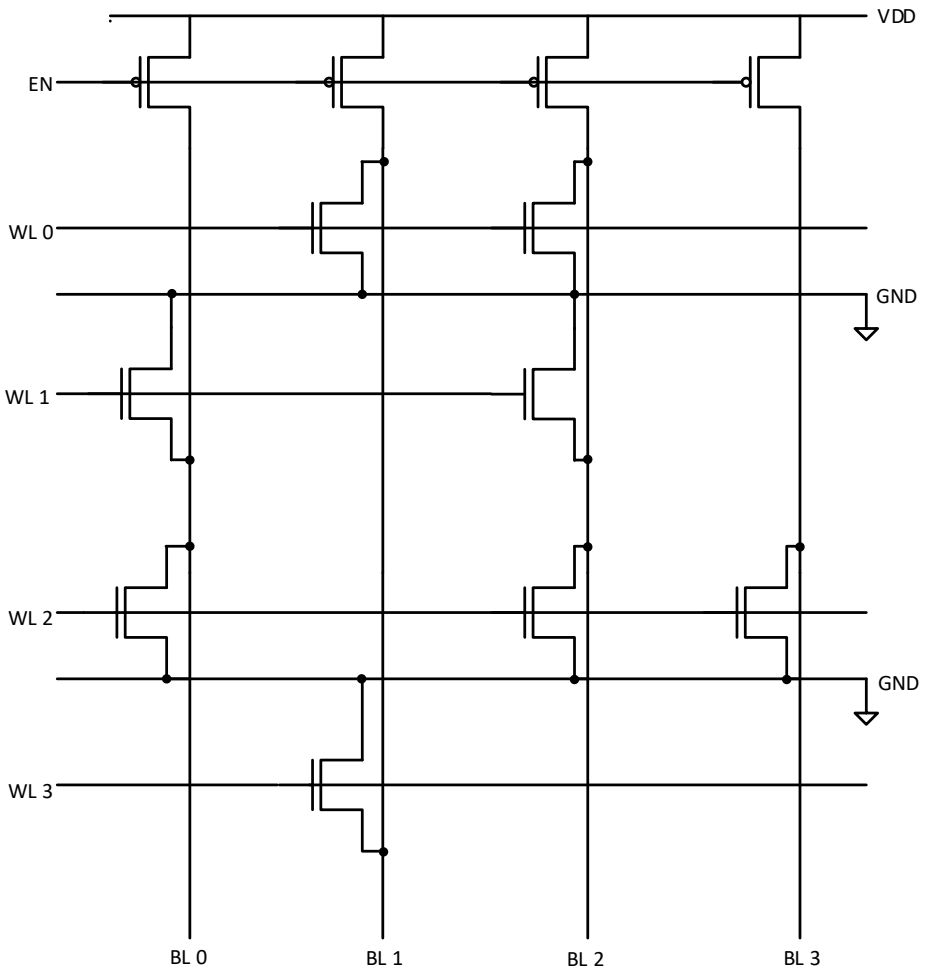

*Figure 2 Schematic of a 4*4 ROM [3]*

1.1.3 Programmable Read Only Memory (PROM)

Programable Read Only Memory is that type of ROM where the data is programed onto the device after manufacturing. During the manufacturing process, all the data bits are set to “1”. The user can later program his choice of data onto the device by burning the fuses. Burning a fuse will set that bit value to “0”.

When an abnormally high voltage is applied across the gate and substrate of a transistor, it causes the oxide between gate and substrate to breakdown. This results in high current in the oxide, which melts it and forms a conductive channel between gate and substrate. This process is called “burning of PROM” and the apparatus that does this is called a PROM Programmer.

As burning of fuses is an irreversible process, once the data is written, it cannot be altered which means that it’s a one-time permanent write. So, if the user programs incorrect data on to the PROM, it gets wasted. PROM is used for the same purposes as a regular ROM where the written piece of data is to be present permanently on the device. (e.g.: washing machines)

1.1.4 Erasable Programable Read Only Memory (EPROM)

Erasable Programable Read Only Memory is that type of ROM where the data written to it can be reprogrammed. The data written onto the ROM can be erased by exposing it to UV rays [4]. The exposure to UV radiation creates electron-hole pairs in the oxide region of the transistor thus enabling its normal operation. The EPROM devices are provided with a small window on them to facilitate the exposure and the device must be taken out of the system for erasing. This process of erasing by exposure to UV radiation is time consuming and can only be done a limited number of times.

1.1.5 Electrically Erasable Programable Read Only Memory (EEPROM)

Electrically Erasable Programable Read Only Memory enables erase operation by simply reversing the voltage. The memory array is made up of Floating gate Tunnel Oxide Transistors [5] (FLOTOX) which are similar to regular floating gate transistors but with thinner oxide layer between floating gate and drain. FLOTOX is based on Fowler-Nordheim tunneling hot carrier injection. A high voltage across the gate and substrate results in electrons gathering at floating gate which raises the threshold voltage. Reversing the voltage results in lowering the threshold voltage. EEPROMs have the advantage of more write-erase cycles and also longer data retention period when compared to EPROMs. EEPROMs perform erase operation either bit wise or multiple bits at a time.

1.1.6 Flash Memory

Flash memory is similar to EEPROM but the erase operation in flash memory is done in blocks instead of bytes as opposed to EEPROM. Since the erase operations in flash memory are done on a larger scale than EEPROMs, the flash memory has better speed. Flash memory uses arrays of floating gate transistors. There are two types of flash memory – NAND flash and NOR flash. The limitation to the flash memory is that it has a finite number of erase cycles. Flash memory is robust and can withstand high temperatures and pressures. Flash memory is used as ‘secondary memory’ in the form of memory cards, USB flash drives, solid-state drives (SSD), etc. *Figure 3* and *Figure 4* show the schematics of NAND flash and NOR flash [5].

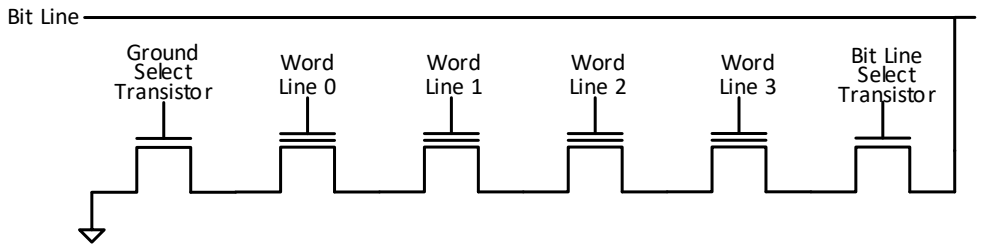

Figure 3 Schematic of NAND Flash [5]

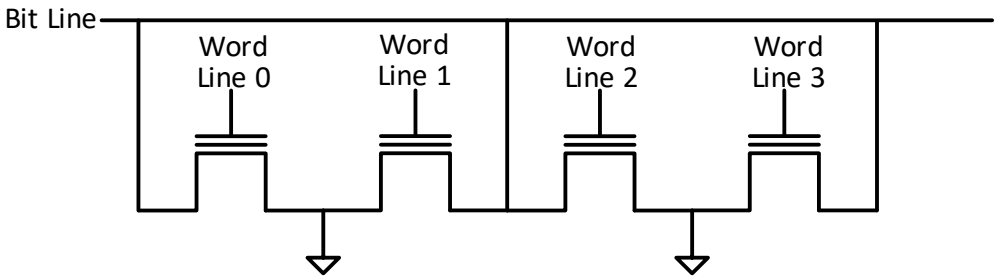

Figure 4 Schematic of NOR Flash [5]

1.1.7 Volatile Memory

Volatile memory is that type of memory which requires power to maintain its data i.e., volatile memory devices can retain their data as long as they are supplied with power. Volatile memories are much faster than non-volatile memories. Random Access Memory (RAM) is volatile memory. The word 'Random' in RAM refers to its ability to access any part of data on it regardless of its physical location (Tapes and magnetic discs are not 'random' access memories as the need to be moved over to a certain part of them to access the data). RAMs are fast but are more expensive than flash memories and draw more power to function. RAM is used as 'primary memory' in computers. There are two types of RAM [5] – Dynamic RAM (DRAM) and Static RAM (SRAM).

1.1.8 Dynamic Random Access Memory (DRAM)

Dynamic Random Access Memory stores its data in a capacitor [6]. The presence or absence of charge in the capacitor determines the data bit value. Since capacitors tend to leak their charge, the data bit value will be lost eventually. In order to prevent this from happening, DRAM cells are refreshed timely by the 'memory refresh' circuits. During the refresh cycle, the data in the bit is first read and then the same bit value is written onto it. A single cell of DRAM consists of one transistor and one capacitor. Since the cell is small, the DRAM can be made with high density. *Figure 5* shows the schematic of a 1-bit DRAM cell.

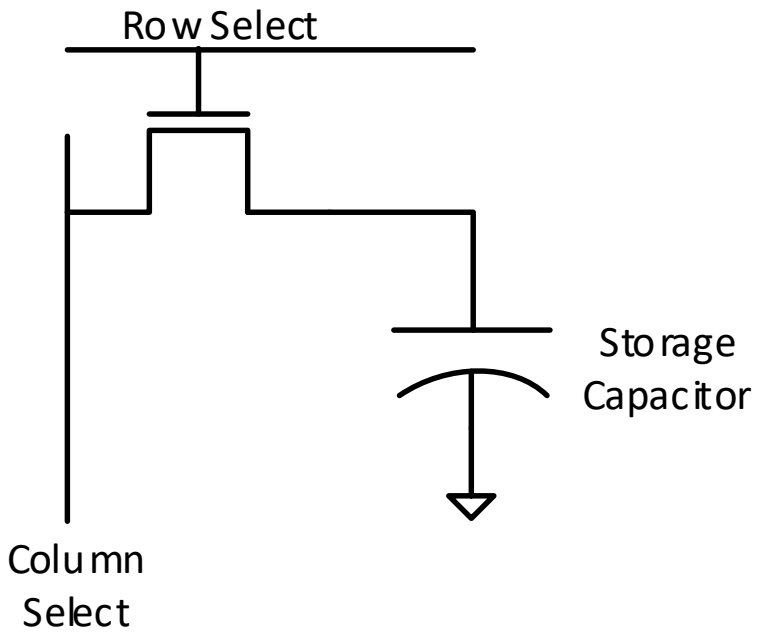

Figure 5 Schematic of a Dynamic RAM Cell [6]

1.1.9 Static Random Access Memory (SRAM)

Static Random Access Memory stores its data in a flip-flop. A traditional SRAM bit cell consists of six transistors [5] out of which two are access transistors and the remaining four transistors form two inverters which are cross-coupled. The cell has two stable states, '0' and '1'. Since the inverters function as long as power is supplied to them, SRAM keeps its value as long as there is power. The access transistors allow for writing and reading data to and from the bit cell. SRAM is faster than DRAM but takes up more space and so SRAM is more expensive than DRAM. SRAM cannot be made as dense as DRAM because of its size. SRAM is used as cache memory [1] in computers and is very low in memory when compared to DRAM. The following *Figure 6* shows a conventional 1-bit SRAM cell.

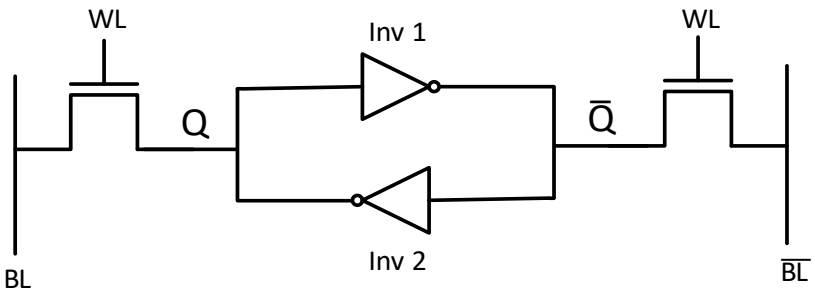

Figure 6 Conventional 1-bit SRAM Cell [5]

1.2 Why FinFET

The technology used in this thesis is 32nm FinFET. A FinFET (Fin Field Effect Transistor) is a type of FET where the channel is raised so that the gate surrounds the channel on three sides. This is also called 3D-FinFET because of its elevated channel. In case of MOSFETs, as the feature size decreases, the length between the source and drain terminals decreases and this in turn increases the leakage current through the channel i.e., I_{ON}/I_{OFF} reduces. The threshold voltage of the transistor reduces and makes it easier to turn ON the transistor which means that the control over the gate reduces. In simple terms, I_{out}/V_{in} increases. The contrast between ON state and OFF state reduces. The FinFET has a 3-D structure where the gate surrounds the channel. This has the advantage of better channel control over traditional MOSFET as the area of contact is more (in FinFET) [7]. The FinFET also has the advantage of reduced leakage and so this can be operated at lower supply voltages when compared to MOSFETs. FinFET is a great alternative to MOSFET to use in SRAM cells. FinFET based SRAM designs have been proposed [8] recently that are better at leakage power reduction when compared to the regular designs. The disadvantage FinFET has over MOSFET is the cost and complexity in manufacturing. Since SRAM is something that needs to function without errors, FinFET is a better option over MOSFET even at the expense of increased cost and complexity. *Figure 7* shows the structures of planar MOSFET, FinFET and multi-fin FinFET.

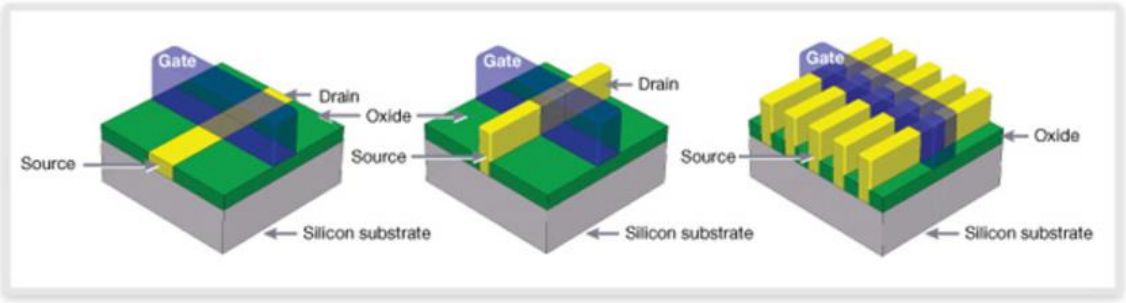

Figure 7 Planar MOSFET, FinFET and Multi-fin FinFET [7]

2. FinFET SRAM Cell Design

This chapter covers the basics of Static RAM which includes the architecture of SRAM array, the conventional 6T SRAM cell and its operation, design constraints Pull-up Ratio and Cell Ratio, stability aspects of an SRAM cell and Static Noise Margin. In addition to the 6T cell, it talks about two existing SRAM cell designs 8T and 10T.

2.1 SRAM Architecture

Figure 8 shows the basic SRAM architecture [9] [5]. The main blocks of SRAM architecture are, SRAM array, row decoder, column decoder, column multiplexer, sense amplifier circuitry and pre-charge circuitry. SRAM array consists of SRAM bit cells arranged in a matrix form of 2^P*(N2^Q). Here, 2^P is the number of rows in the array and 2^Q is the number of columns of words. Each word is of length "N" bits. This means that there are 2^P*2^Q words or 2^P*(N2^Q) bits in the entire array. When a row address of "P" is given to the row decoder, it activates one of the 2^P row lines of the memory array. When a column address of "Q" is given to the column decoder, it activates one of the 2^Q select lines of the column multiplexer (MUX). Depending on the select line inputs, the column MUX gives access to a particular word's N pairs of bit lines. These N pairs of bit lines are

given to N sense amplifiers which give out an N bit data. The data may then be sent through buffers before sending out as the final output. The pre-charge circuitry pre-charges the bit lines to facilitate read operation. In this way, different blocks function together to facilitate the read/write operations on a word of 'N' bits.

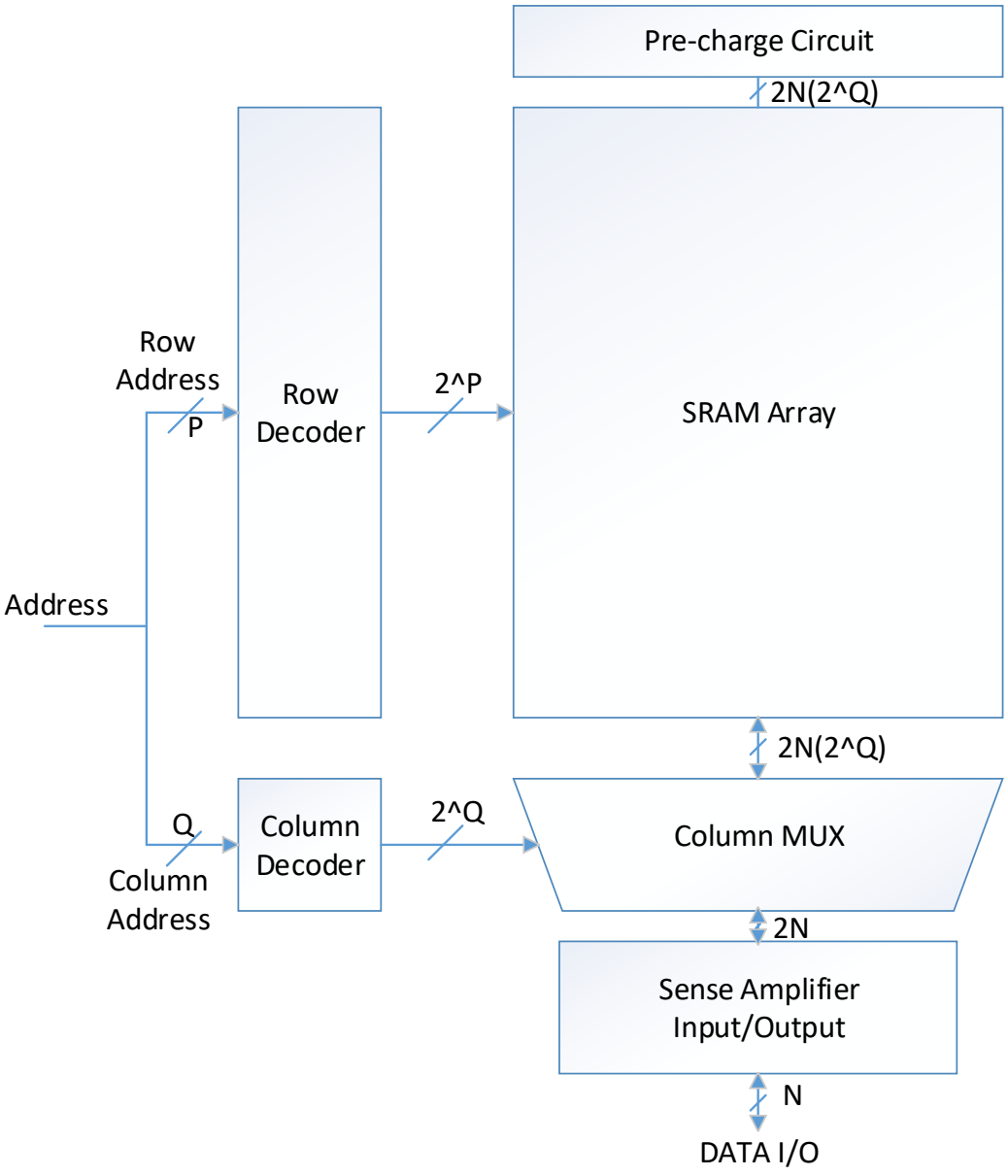

Figure 8 Architecture of SRAM [5]

2.2 6T SRAM Cell

The Six Transistor SRAM cell shown in *Figure 9* is the conventional SRAM bit cell. It consists of two cross-coupled inverters along with two access transistors [5]. As seen from *Figure 8*, transistors ‘M0’, ‘M2’, ‘M1’ and ‘M3’ form the two inverters and transistors ‘M4’, ‘M5’ are the access transistors. The cross-coupled inverters which form the latch are connected to the bit-lines BL and BLB through the access transistors. The word line ‘WL’ controls the access transistors. The latch has the stable states ‘0’ and ‘1’. The access transistors allow for writing and reading of data from the bit cell.

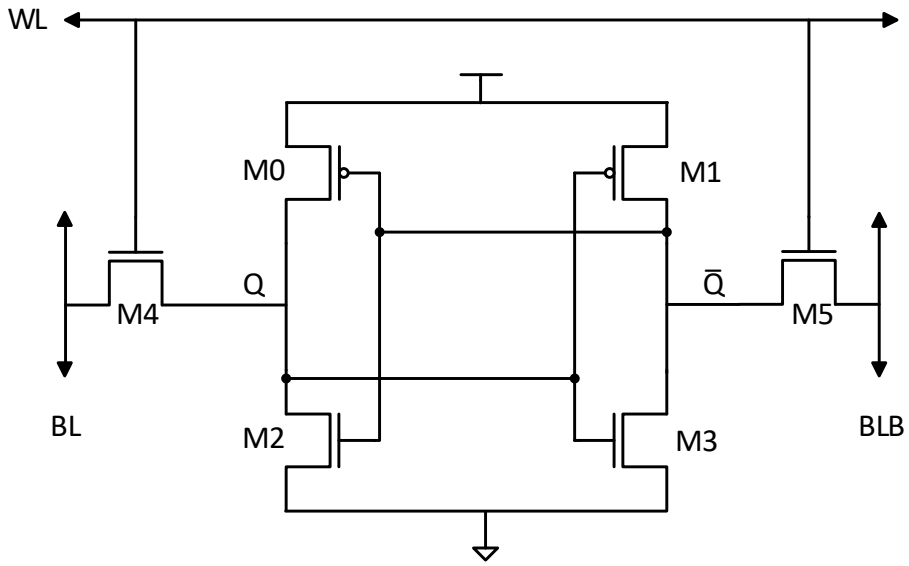

Figure 9 Schematic of a Conventional 6T SRAM Cell [5]

2.2.1 Write

To write a bit to the cell, the lines BL and BLB are set to opposite voltages and then the word line signal WL is enabled. Enabling the WL signal will give the bit-lines access to the inner bit cell. For example, if the bit to be written to Q is ‘0’, then BL is pulled down to ground and BLB is raised to VDD. After setting the bit-lines, the WL signal is enabled. Since BL is set to ‘0’ and is given as input to the inverter ‘M1-M3’, transistor M1 is turned ON and transistor M3 is turned OFF raising the node $\overline{Q}$ to VDD (logic ‘1’). Since BLB is set to ‘1’ and is given as input to inverter ‘M0-M2’, transistor M0 is turned OFF and transistor M2 is turned ON pulling the node Q to ground (logic ‘0’).

The *Figure 10* shows the cell during write ‘0’ operation and the *Figure 11* shows the cell during write ‘1’ operation.

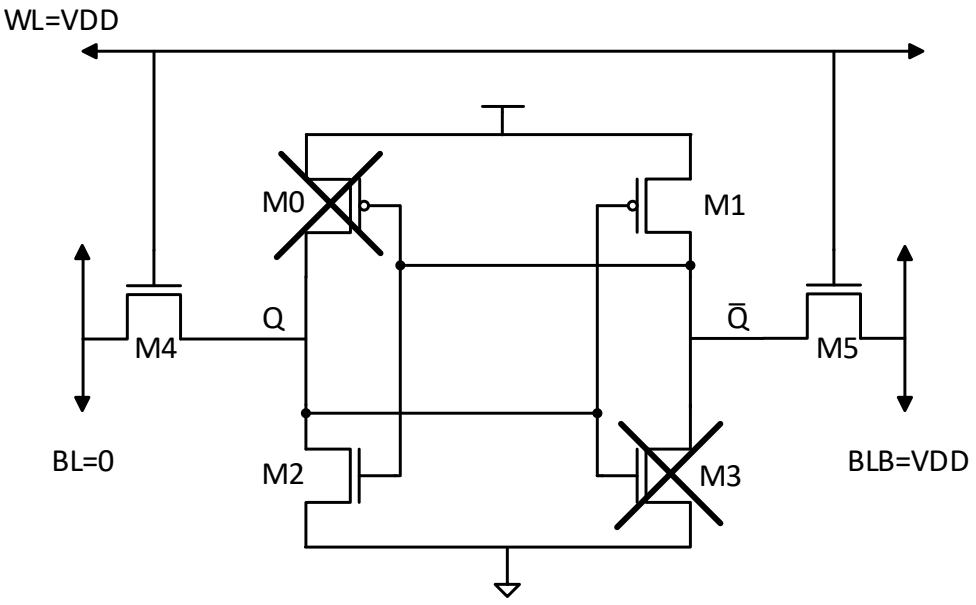

Figure 10 6T Cell during Write '0'

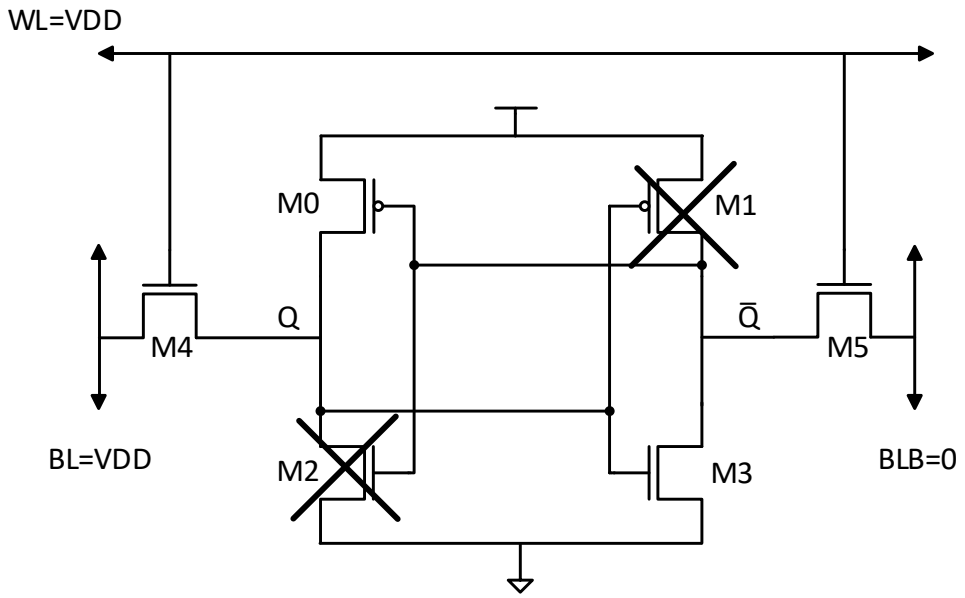

Figure 11 6T Cell during Write '1'

There is a design constraint called **Pull-up Ratio** (PR) that needs to be followed for a successful write operation. Consider the case where Q is at '0' and $\bar{Q}$ is at '1' and we need to write '1' to Q and '0' to $\bar{Q}$. According to the procedure, the BL is raised to VDD and BLB is pulled to ground and the WL signal is enabled. In this case, the PMOS transistor M1 and NMOS transistor M5 are in ON state. Since BLB is pulled to ground, node $\bar{Q}$ starts discharging through M5 and at the same time it is being charged through M1. Since both M1 and M5 are ON, they act as a potential divider. Now, if the potential at $\bar{Q}$ is not brought below the switching threshold voltage of the inverter 'M0-M2', the state of the bits doesn't change. In order to achieve a successful write operation, the potential at $\bar{Q}$ should be below the switching threshold of the inverter 'M0-M2' i.e., the resistance of transistor M5 should be less than that of M1 which in-turn means that the width of M5 should be greater than that of M1.

Pull-up Ratio [10] is defined as the ratio of (W/L) of PMOS pull-up transistor to the (W/L) of NMOS access transistor.

$$\text{Pull-up Ratio} = \left(\frac{W_0}{L_0}\right) \Big/ \left(\frac{W_4}{L_4}\right) \quad \text{and} \quad \left(\frac{W_1}{L_1}\right) \Big/ \left(\frac{W_5}{L_5}\right) \tag{1}$$

Lowering the Pull-up Ratio will make the cell more writable.

2.2.2 Read

To read a data bit from the cell, the bit-lines BL and BLB are initially pre-charged to VDD and then the WL signal is made high. Enabling WL will give the bit-lines access to the inner cell. For example, if the bit at Q is '0', then the bit-line BL which is pre-charged to VDD starts discharging through M4 and M2. This will gradually reduce the potential on the line BL. At the same time, since the bit at $\overline{Q}$ is '1' and the line BLB is high, the bit-line BLB continues to maintain its potential at VDD. The bit-lines BL and BLB are given to a sense amplifier which gives the appropriate output based on the difference between the two bit-lines.

The *Figure 12* shows the simulation setup of the cell during read operation.

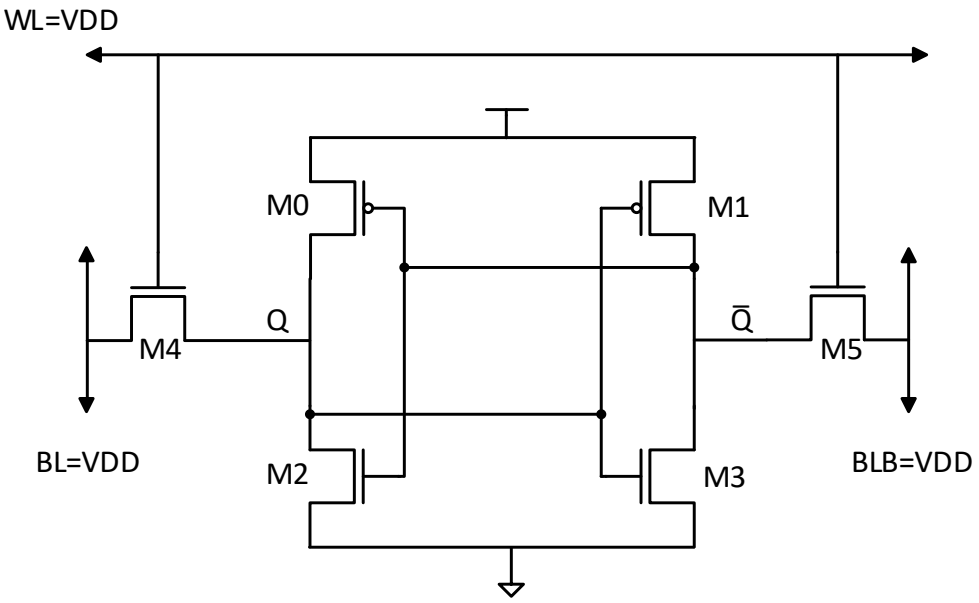

Figure 12 Setup of 6T Cell during Read operation

There is a design constraint called **Cell Ratio** [10] (CR) that needs to be followed for a successful read operation. Consider the case where node Q is at '0' and $\overline{Q}$ is at '1'. During the read operation, both bit-lines are set to VDD and signal WL is enabled. Transistors M4 and M5 turn ON to give bit-lines access to the inner cell. Since $\overline{Q}$ is at '1', the potential on BLB stays at VDD. Since Q is at '0', line BL starts discharging through M4 and M2. While discharging, transistors M4 and M2 which are currently ON form a potential divider. During the discharge, the potential at Q raises due to the fact that transistor M2 has an internal resistance that's causing the voltage drop. If this potential at Q raises above the switching threshold of inverter 'M1-M3', PMOS transistor M1 will be turned OFF and NMOS transistor M3 will be turned ON which results in the reversal of data bits and thereby corrupting the data. In order to avoid this situation, the internal resistance of M2 should be less than that of M4 i.e., the size of M2 should be made larger than that of M4.

Cell Ratio is defined as the ratio of (W/L) of NMOS pull-down transistor to the (W/L) of NMOS access transistor.

$$\text{Cell Ratio} = \left(\frac{W_2}{L_2}\right) \Big/ \left(\frac{W_4}{L_4}\right) \quad \text{and} \quad \left(\frac{W_3}{L_3}\right) \Big/ \left(\frac{W_5}{L_5}\right) \tag{2}$$

Increasing the Cell Ratio will make the cell more readable.

2.2.3 Hold

The state where the data is neither written to the cell nor read from the cell is called hold/standby state. During this state, signal WL is made low so that access transistors M4 and M5 are turned OFF which disables the bit-lines' access to the inner cell. During this stage, the cell is unaffected by the voltages on the bit-lines. *Figure 13* shows the setup of the bit cell during hold phase.

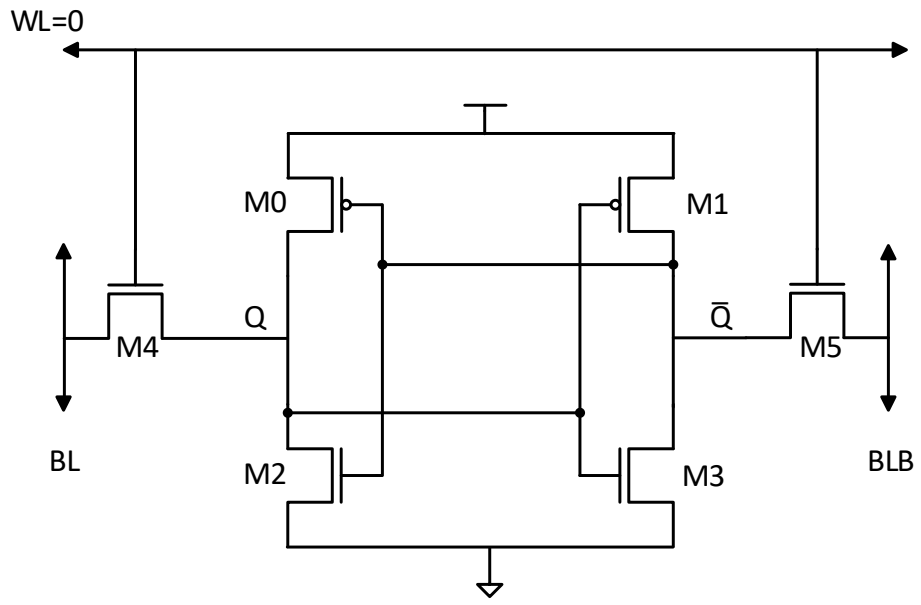

Figure 13 Setup of 6T Cell during Hold phase

Figure 14 displays the simulation result of a 6T cell. The order of phases is,

Write '0' – Hold '0' – Read '0' – Hold '0' – Write '1' – Hold '1' – Read '1' – Hold – '1'

'BL_ip' and 'BLB_ip' are the inputs given to the bit-lines whereas 'BL' and 'BLB' are the voltages on the bit-lines. The bit-lines are pre-charged to VDD during the hold phases before reading. The 'OUT' signal is the output of the sense amplifier connected across the bit-lines. The simulation is done at a VDD of 1V at 25˚C.

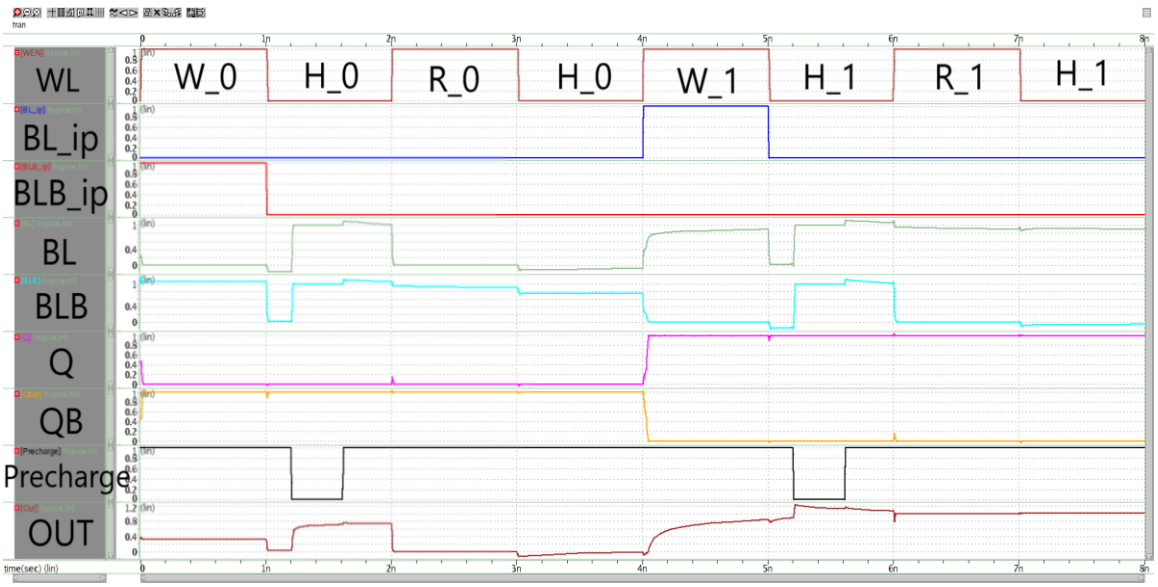

Figure 14 Simulation waveforms of 6T SRAM Cell

2.3 Static Noise Margin (SNM)

Stability is an important factor when choosing a cell design for any application. Stability of a cell can be assessed by its Static Noise Margin (SNM) [11]. Static Noise Margin is defined as the maximum noise that the cell can tolerate before its data is corrupted/altered. The SNM is measured during all the three phases of operation – read, hold and write. A noise source, 'Vn', is introduced at one of the bit nodes (Q or $\bar{Q}$) and is varied from '0' to VDD and the change in voltage at the other node is measured. The process is done at both the nodes and the curves thus obtained are combined to form a 'butterfly' diagram. The butterfly diagram has two 'eyes' when measured in read and hold phases. The SNM is the size of the biggest square that can be fit in these eyes. When measuring SNM in a particular phase of operation, the bit-lines, word-line, etc. are set to their appropriate values as done in regular working cases. For example, when measuring Read SNM, the bit-lines are set to VDD and the WL signal is enabled. The process of

measuring SNM will be explained in detail in the results section. The following figures show the simulation setup for SNM calculation of a 6T cell and also the graphs obtained during the simulations. It can be seen from Figure 16 that the RSNM is poor. The RSNM is the biggest disadvantage of the conventional 6T SRAM cell and number of designs [12], [13], [14], [15], [16] have been proposed to overcome this issue. One thing all those designs have in common is a separate read circuit that eliminates the disturbance during read operation.

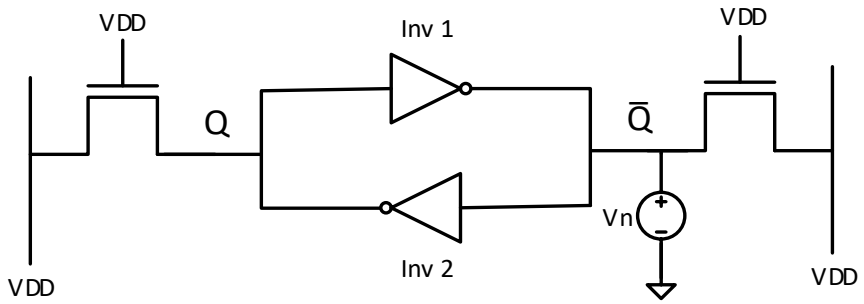

Figure 15 Simulation setup for RSNM

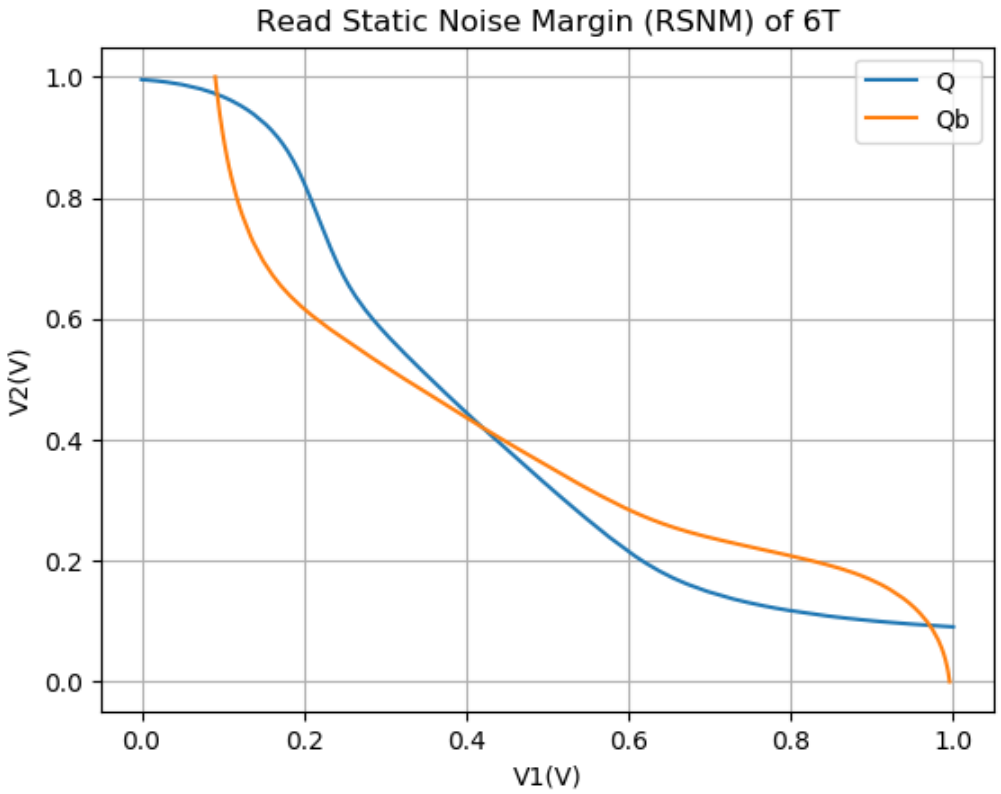

Figure 16 RSNM VTCs of 6T Cell

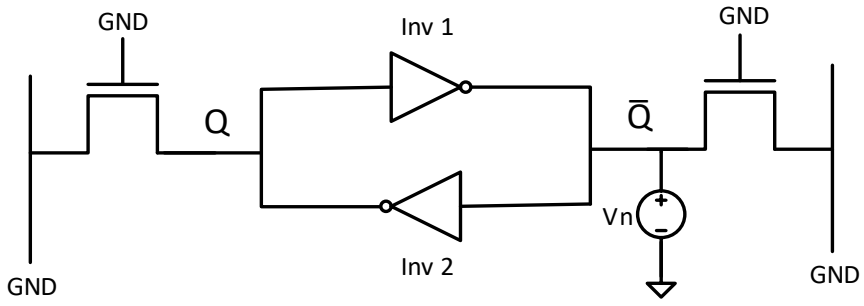

Figure 17 Simulation setup for HSNM

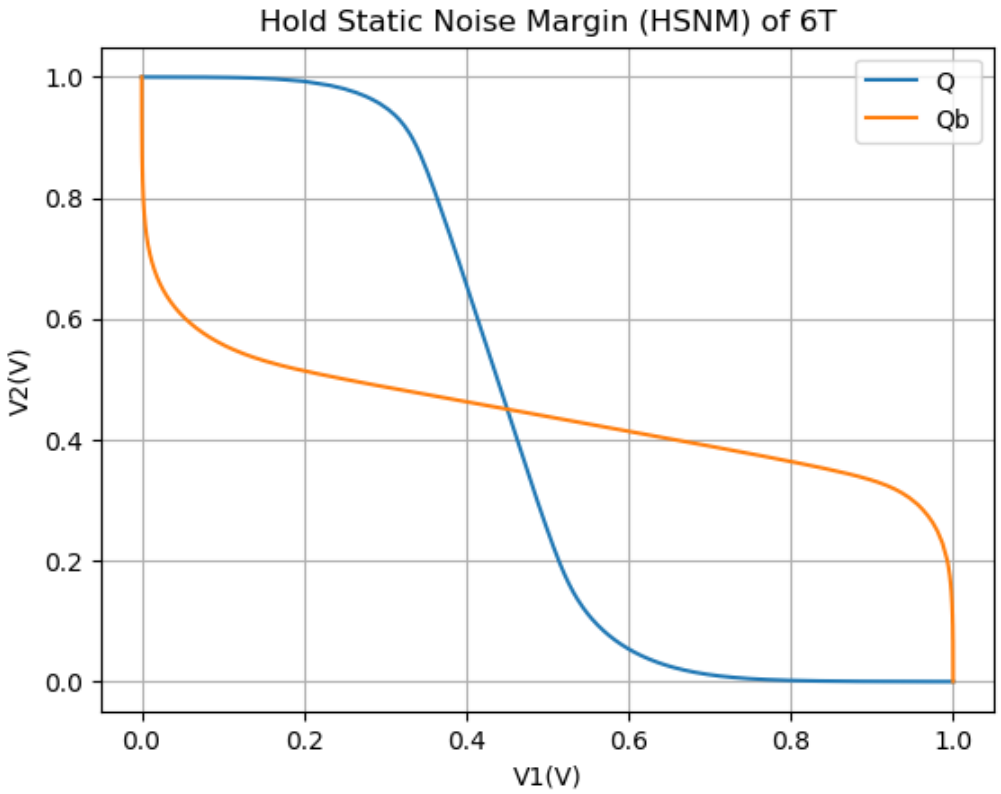

Figure 18 HSNM VTCs of 6T Cell

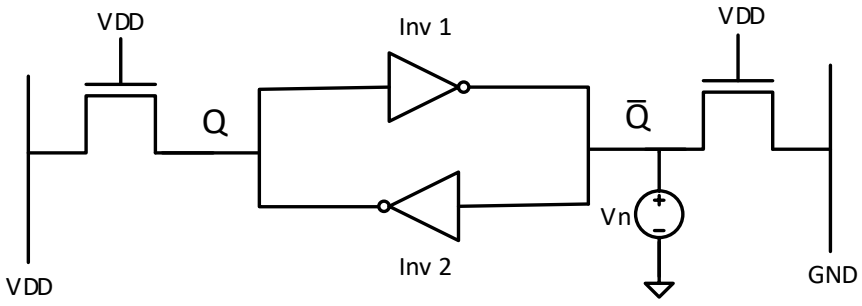

Figure 19 Simulation setup for WSNM

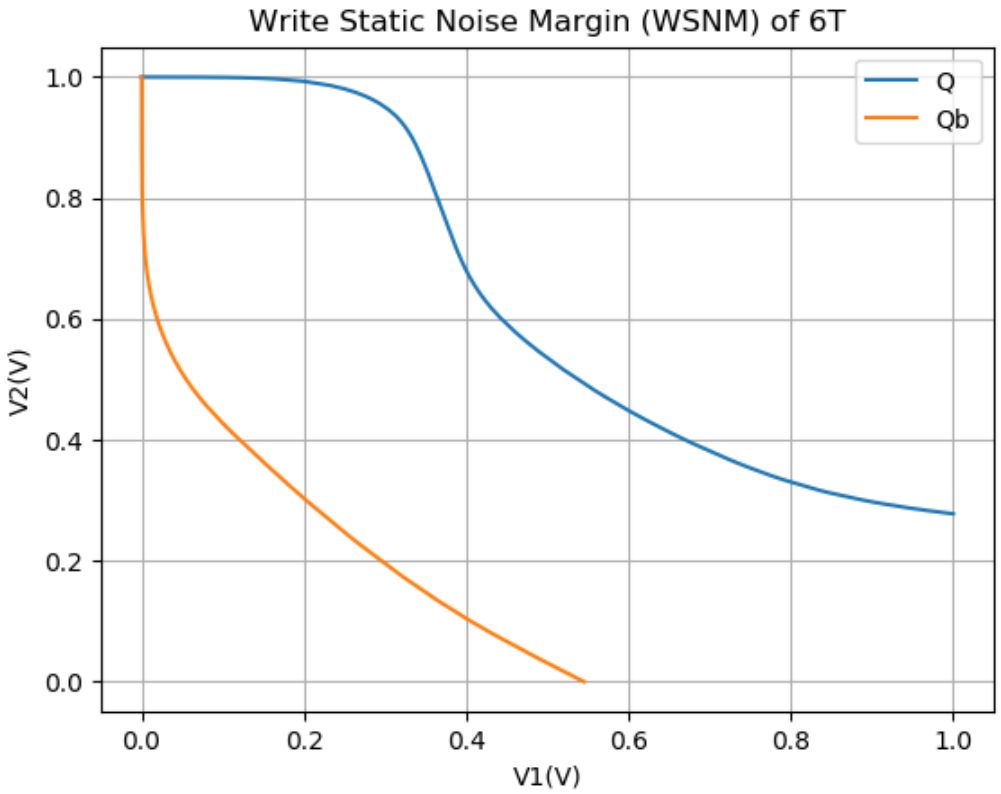

Figure 20 WSNM VTCs of 6T Cell

2.4 8T SRAM Cell

Various designs have been proposed to overcome the problem of poor Read SNM of the 6T SRAM cell. One of the cell designs is the 8T [17] SRAM cell which adds two transistors to the existing 6T SRAM cell to facilitate read disturb free operation. As shown in *Figure 21*, the 8T cell has two additional transistors M6 and M7 which form a single

ended read circuit. Bit $\overline{Q}$ is given to gate of M7 and since the data bit is driving a gate as opposed to a bit-line in 6T SRAM, the Read SNM is greatly improved.

During the write operation, bit-lines Write Bit Line (WBL) and Write Bit Line Bar (WBLB) are set to opposite voltages (VDD and GND) according to the bit value to be written to the cell. After bit-lines are set, the Write Word Line (WWL) is enabled which gives the bit-lines access to the inner cell to write data to it. During the write operation, the Read Word Line (RWL) signal is kept low.

To read the data from the cell, initially, the Read Bit Line (RBL) is pre-charged to VDD. After the pre-charge, the RWL signal is set high (M6 is ON) and depending on the bit value at $\overline{Q}$, transistor M7 is either ON or OFF. If bit value at $\overline{Q}$ is '1', then as both M6 and M7 are ON, RBL discharges through 'M6-M7' and voltage on the line RBL starts to drop. The RBL is given to a sense amplifier whose reference voltage is set at VDD/2. If the bit at $\overline{Q}$ is '0', transistor M7 is OFF and RBL maintains its voltage at VDD since there is no path for discharge. The sense amplifier senses the difference between the reference voltage and the bit-line voltage to give an appropriate output. During the read phase, the signal WWL is kept low.

During hold phase, both WWL and RWL are kept low isolating the latch from the bit-lines.

The read operation in 8T SRAM is single-ended. The power during read is only consumed when the bit being read is '0' (Q=0 and $\overline{Q}$=1), because that's when M7 is turned ON and RBL discharges through 'M6-M7'. In the case where bit being read is '1', the RBL remains at VDD. And every time after the reading of bit '0', the RBL needs to be pre-

charged to VDD. During the read phase, internal nodes are undisturbed, and this improves the Read SNM. Read SNM in an 8T cell is same as that of its Hold SNM.

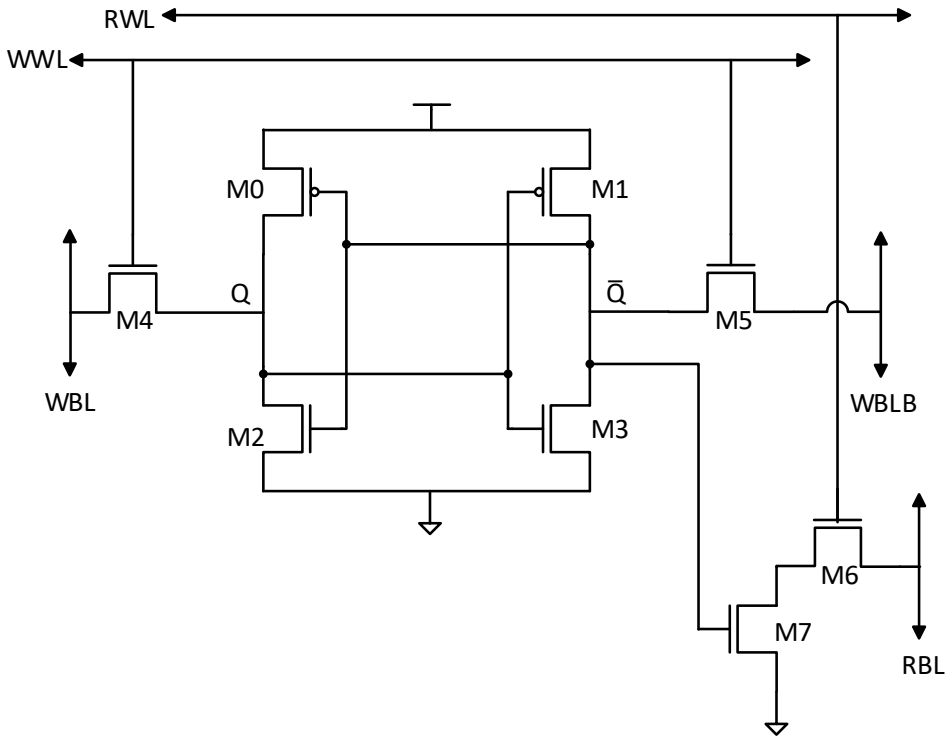

Figure 21 Schematic of 8T SRAM Cell

The *Figure 22* shows the simulation results of the 8T bit-cell. The order of phases is,

Write '0' – Hold '0' – Read '0' – Hold '0' – Write '1' – Hold '1' – Read '1' – Hold – '1'

The RBL is pre-charged to VDD during hold phases before reading. The reference voltage given to the sense amplifier is 0.5V. The 'OUT' signal is the output of the sense amplifier. The simulation is done at a VDD of 1V at 25˚C.

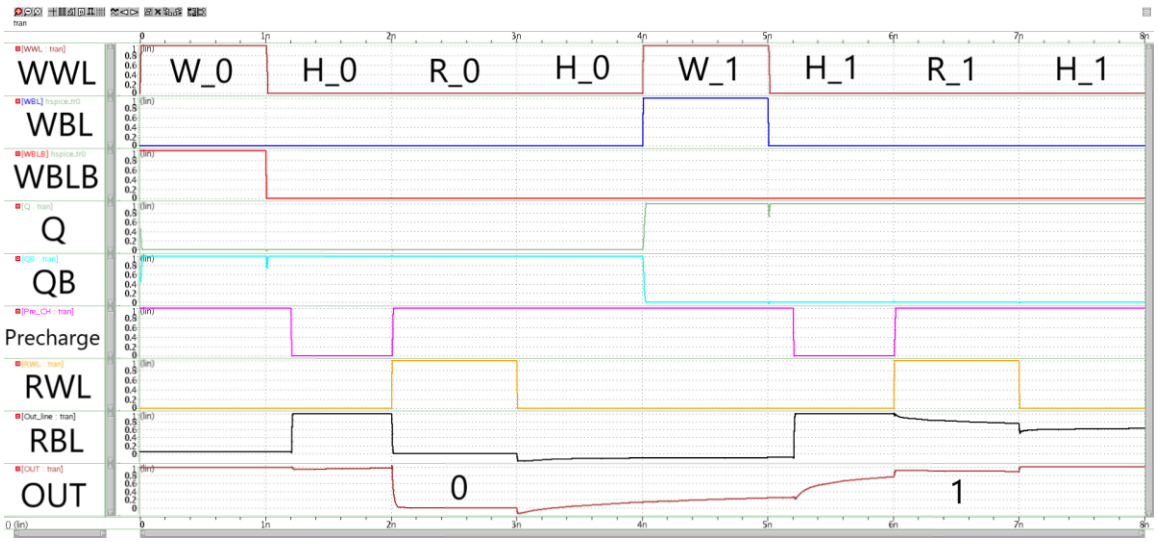

Figure 22 Simulation waveforms of 8T SRAM Cell

2.5 10T SRAM Cell

A 10 Transistor SRAM [18] cell is proposed to eliminate the need of a pre-charge circuit. An inverter and a transmission gate are added to the existing 6T SRAM cell as shown in *Figure 23*. Word Line (WL) is the control signal for write operation and the complementary signals Read Enable (RE) and Read Enable Bar (REB) are the control signals for read operation.

To write data to the 10T cell, the lines BL and BLB are set to opposite voltages (VDD and GND) according to the data to be written. Then, the WL signal is enabled to turn ON the access transistors and give the bit-lines access to the inner cell to perform write operation. During the write phase, RE signal is kept low and the REB signal is kept high.

To read data from the cell, RE signal is set high and the REB signal is set low in order to activate the transmission gate. The bit value that is present at $\overline{Q}$ is inverted by 'M6-M7' and sent through the transmission gate to the output line. Since the output is actually coming from an inverter, there is not a need to pre-charge the Rdout line in order to read the data. During the read operation, the WL signal is kept low.

During the hold phase, signals WL, RE are kept low and signal REB is kept high.

The read operation in the 10T cell is single-ended. The advantage of this design over the others is that when reading a bit that is the same value as the previously read bit, there is no dynamic power consumption. The power (read power) is consumed only when the two consecutive read bits are of different value. For example, when the previously read bit is '1', the Rdout line is pulled-up to VDD. If the current bit that is being read is '1', then since the Rdout line is already at VDD, there is no more pulling up of voltage. Since bit value at $\overline{Q}$ is driving a gate, it remains unaffected. This improves the Read SNM of the cell. Read SNM is the same as Hold SNM in the 10T SRAM cell. This design suffers from bit-line leakage through transistors M8 and M9. The design [5] solves this issue by pre-charging the Rdout line and introducing virtual power rails.

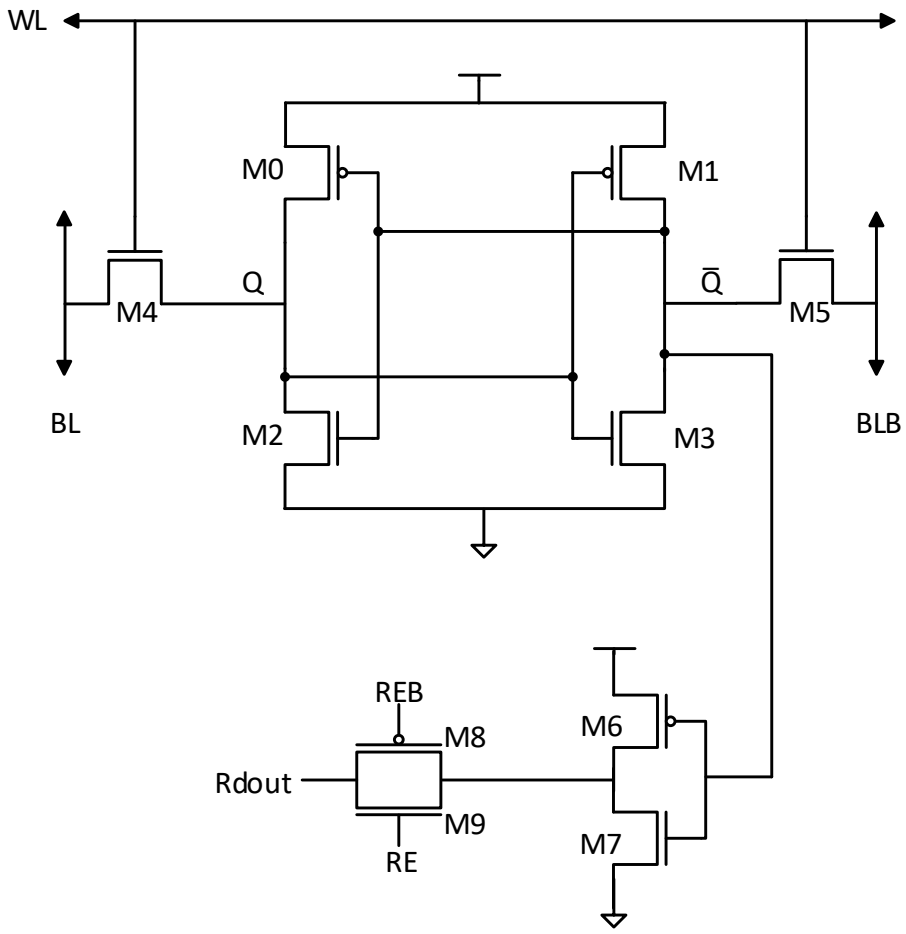

Figure 23 Schematic of 10T SRAM Cell

Figure 24 shows the simulation results of the 10T bit-cell. The order of phases is,

Write '0' – Hold '0' – Read '0' – Hold '0' – Write '1' – Hold '1' – Read '1' – Hold – '1'

As seen from the figure, the voltage on the 'Rdout' line changes only when the bit being read is of a different value from the previous one. A reference voltage of 0.5V is given to the sense amplifier. The 'OUT' signal is the output of sense amplifier. The simulation is done at a VDD of 1V at 25˚C.

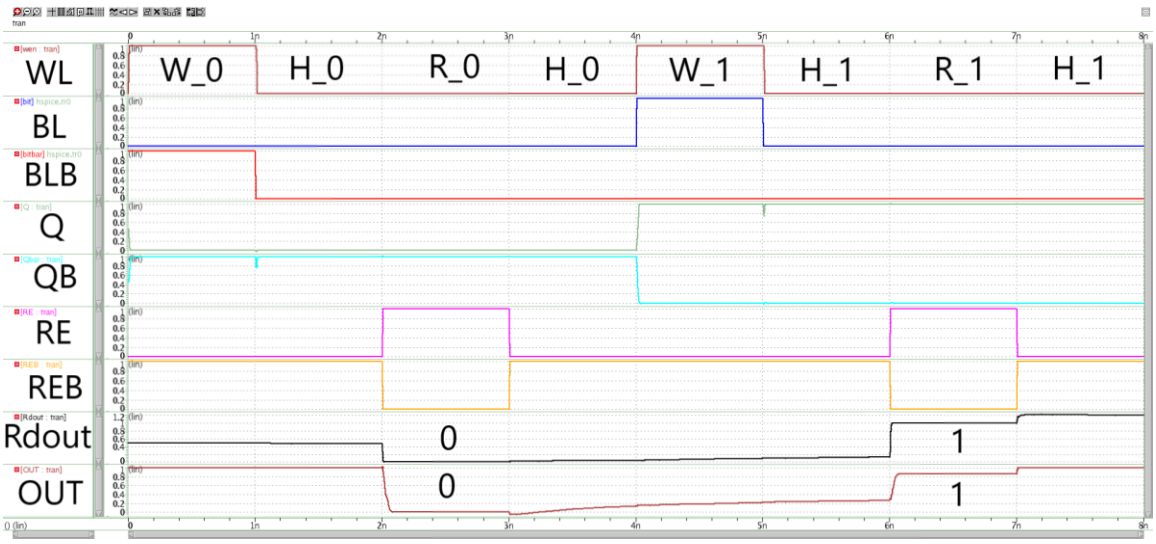

Figure 24 Simulation waveforms of 10T SRAM Cell

2.6 Proposed SRAM Cell

We propose a 10T SRAM cell with four transistors (M6-M9) to form a tri-state inverter to facilitate read operation in addition to the six transistors from the 6 SRAM cell. The goal is to improve the Read SNM from the 6T design by implementing a read disturb free circuit and have a low read time power consumption. The design is proposed in a way to minimize bit-line leakage by providing a more resistive leakage path when compared to existing 10T design. The noise that transmission gate allows in existing 10T design is eliminated in proposed design by introducing tri-state inverter. *Figure 25* gives the schematic of our proposed 10 Transistor SRAM cell. Transistors M6 and M7 form an inverter (inverting $\overline{Q}$ to Q at 'Rdout') and transistors M8 and M9 act as output paths to Rdout. The bit-lines, BL and BLB are used as data input lines during write operation. The Word Line (WL) signal controls bit-lines' access to the cell during write operation. Signals, Read Word Line (RWL) and Read Word Line Bar (RWLB) control read operation.

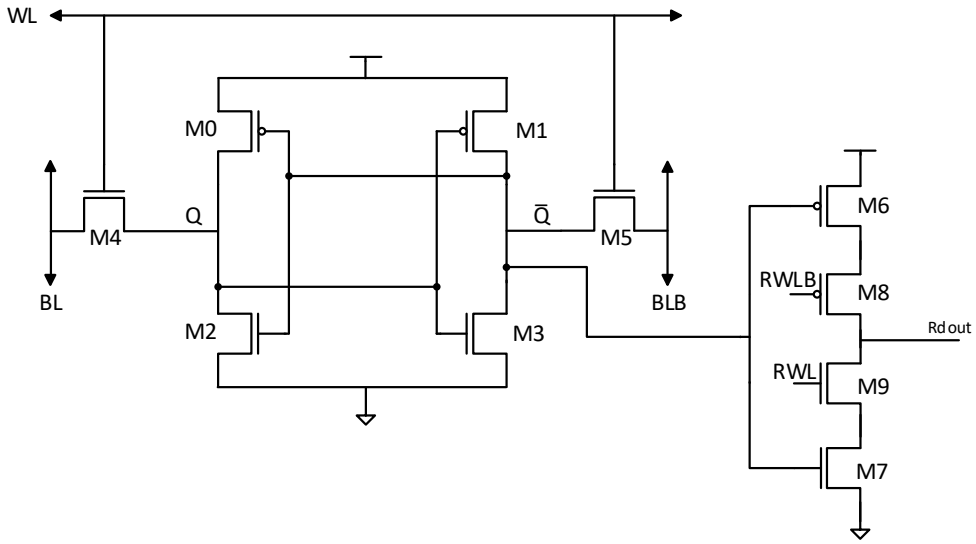

Figure 25 Schematic of Proposed 10T SRAM Cell

2.6.1 Write

To write a bit to the cell, the bit-lines BL and BLB are set to opposite voltages and then the Word Line (WL) signal is enabled. Enabling WL signal gives the bit-lines access to the inner cell. To write bit '0' to Q, the bit-line BL is pulled-down to GND and the bit-line BLB is pulled-up to VDD. After this, the WL signal is enabled which turns ON the access transistors M4 and M5. As BL is set to '0', which is also the input to the inverter 'M1-M3', transistor M1 turns ON (M3 is OFF) and pulls the potential at $\bar{Q}$ to VDD. As BLB is set to '1', which is also the input to the inverter 'M0-M2', the transistor M2 is turned ON (M0 is OFF) and the potential at Q is pulled-down to '0'. The signal RWLB is set to high and RWL is set to low during write operation.

Figure 26 shows the state of the cell during write '0' operation and *Figure 27* shows the state of the cell during write '1' operation.

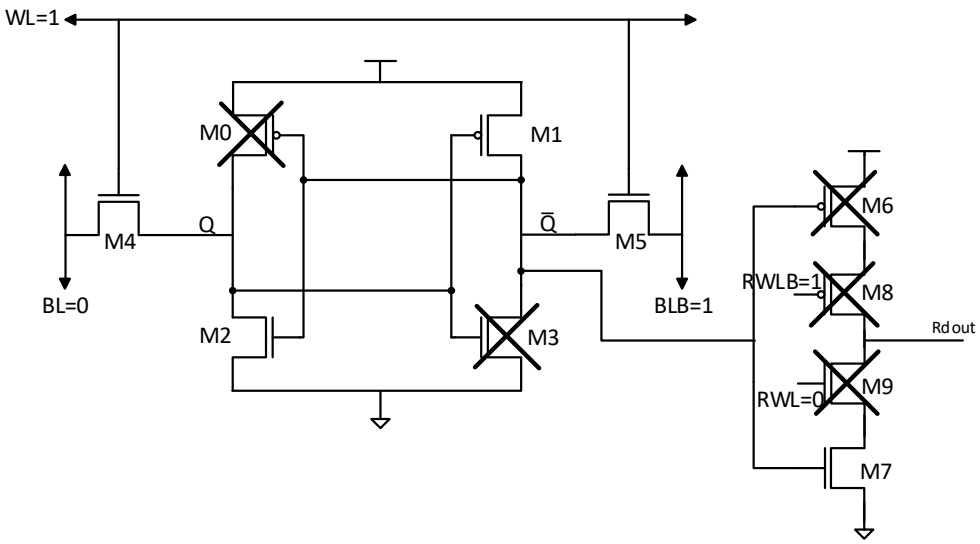

Figure 26 Proposed 10T SRAM Cell during Write '0'

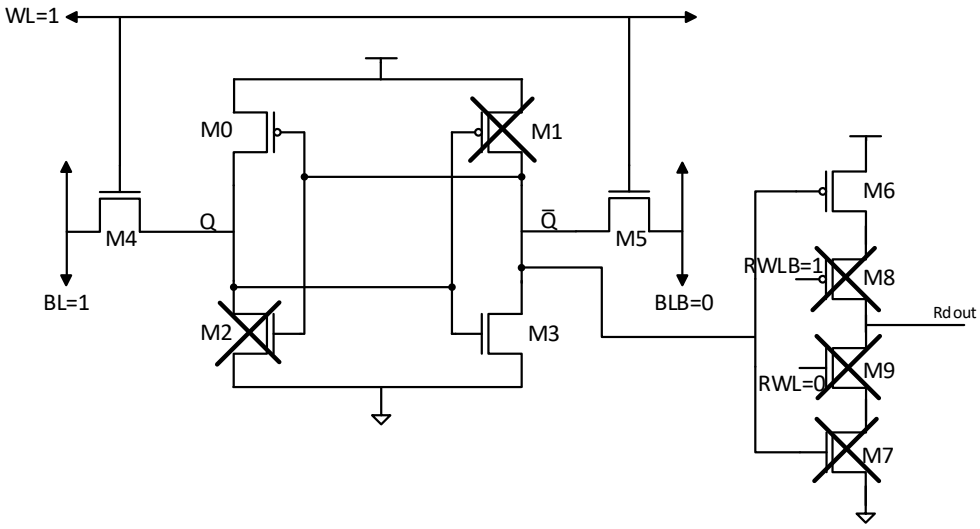

Figure 27 Proposed 10T SRAM Cell during Write '1'

2.6.2 Read

During read operation, signal RWLB is set to low and signal RWL is set to high. Setting the signals that way will turn ON transistors M8 and M9. Since M8 and M9 are turned ON, they are shorted and 'M6-M7' behaves as a regular CMOS inverter that inverts bit $\bar{Q}$ (which is the input to inverter) to Q at the output bit line 'Rdout'. For example, if the data bit $\bar{Q}$ is '1', transistor M7 is turned ON (M6 is OFF) and the potential at Rdout is pulled to '0' through the path M9-M7. And if the data bit $\bar{Q}$ is '0', transistor M6 is turned ON (M7 is OFF) and the output bit-line Rdout is pulled to VDD through path M6-M8. During read operation, the control signal WL is kept low. *Figure 28* shows the state of the cell during read '0' and *Figure 29* shows the state of the cell during read '1'.

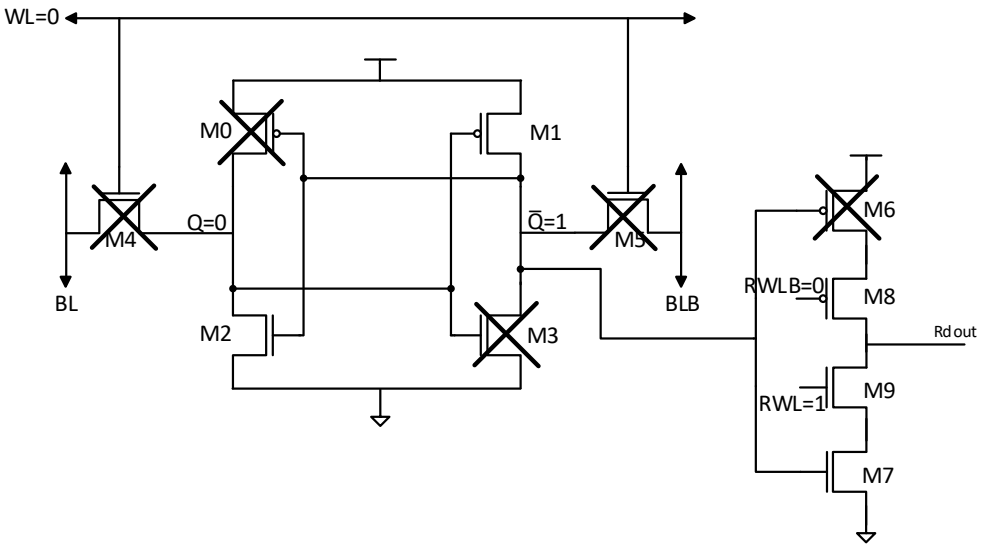

Figure 28 Proposed 10T SRAM Cell during Read '0'

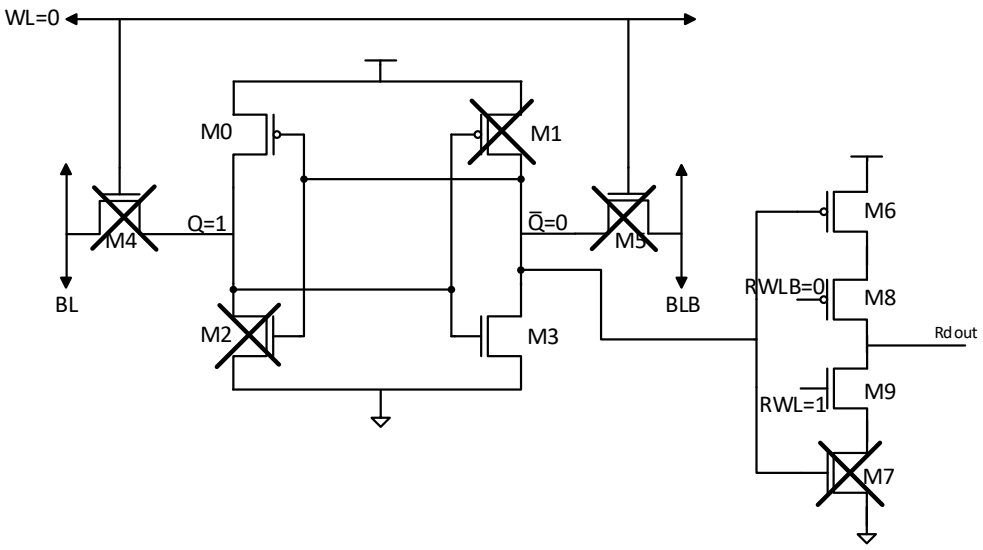

Figure 29 Proposed 10T SRAM Cell during Read '1'

The output bit-line Rdout is given as an input to a sense amplifier whose reference voltage is set at VDD/2. Depending on the difference between reference voltage and the voltage at the bit-line, the sense amplifier gives an appropriate output. If the bit that is currently read is the same (value) as that of the previously read data bit, then power is not consumed. For example, if the previous bit that was read is '1' (Q=1), it means that Rdout was raised to VDD. Now, if another bit along the same column whose value is '1' is being read, since Rdout is already at VDD, it is maintained at that potential. The power is consumed when a data bit of value '0' is read as it pulls-down Rdout to GND.

The read operation in this cell is single-ended. Since the output comes directly from an inverter, there is not a need to pre-charge the output bit-line. Since the bit $\bar{Q}$ is driving the gates of the inverter, the internal nodes of the cell are unaffected during read operation.

2.6.3 Hold

The state where data is neither written to nor being read from the cell is called hold/standby phase. During this phase, the signals WL, RWL are kept low and RWLB is kept high. During this phase, the bit-lines BL and BLB may carry data that is being written to a cell on a different row. Even when the access transistors, M4 and M5, are turned OFF, there will be leakages between the cell and the bit-lines which is discussed in Section 2.6.5. *Figure 30* shows the state of the cell during hold '0' phase and *Figure 31* shows the state of the cell during hold '1' phase.

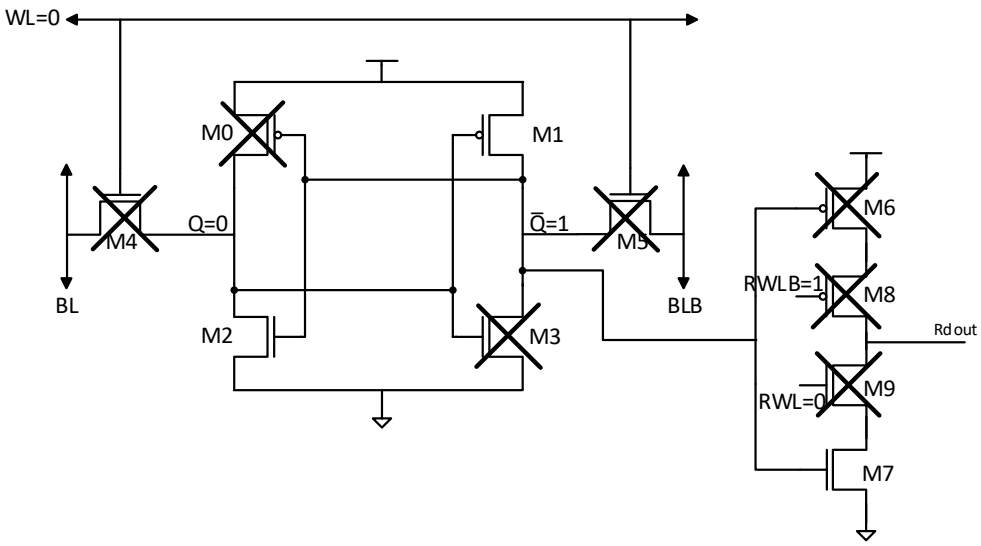

Figure 30 Proposed 10T SRAM Cell during Hold '0'

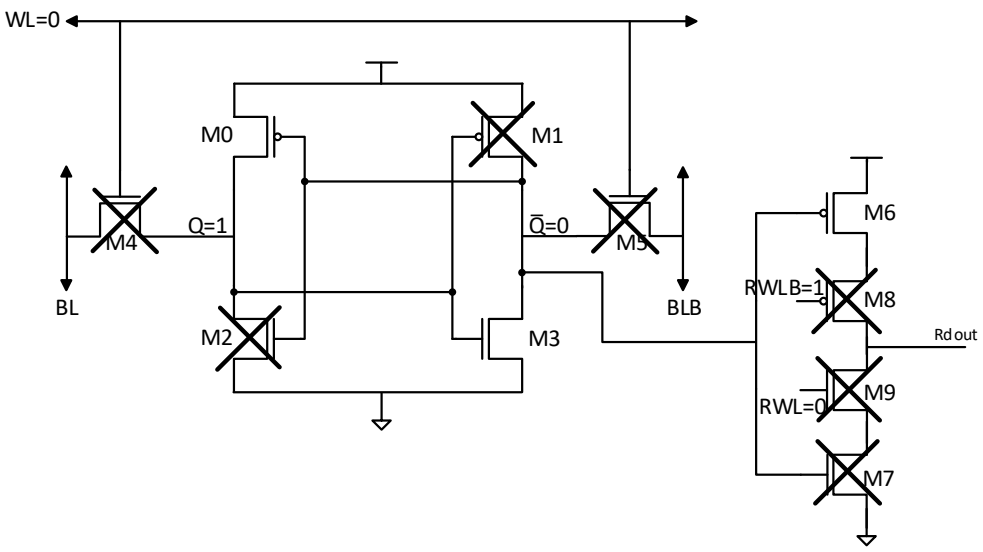

Figure 31 Proposed 10T SRAM Cell during Hold '1'

2.6.4 Static Noise Margin

The read operation in the proposed 10T SRAM cell is single-ended. The bit $\bar{Q}$ drives the gate of the inverter 'M6-M7' which means that the internal nodes of the cell are unaffected by the read operation which improves the Read SNM when compared to the 6T design. The Read SNM of the proposed 10T cell is same as that of the previously discussed 8T and 10T cells. The Read SNM in the proposed 10T is also its Hold SNM. Since the access transistors, M4 and M5, are not used for reading the bits, the design constraint 'cell-ratio' need not be considered. The design constraint 'pull-up ratio' is still in effect as the write conditions are same in the proposed cell as that of the 6T cell. Lowering the pull-up ratio improves the write ability or Write SNM. The simulation setup for calculating SNM for the proposed cell is discussed in detail in the results section. SNM varies with PVT variations [19]. The variation of SNM with VDD and temperature are also explained in results section.

2.6.5 Leakage

Transistors leak a small amount of current during the OFF state. The access transistors, M4 and M5, are turned OFF except during the writing phase. When the access transistors are OFF, they leak current through them (between the cell and the bit-lines). This may not be a big problem at a cell level, but on the array level when a lot of bit-cells are connected to the same bit-lines, the leakage current becomes an issue. The leakage happens during the case where Q and $\overline{Q}$ hold the bits '0' and '1' respectively and the bit-lines BL and BLB are at '1' and '0' respectively as shown in the *Figure 32*. This happens when data is written to another cell in the same column.

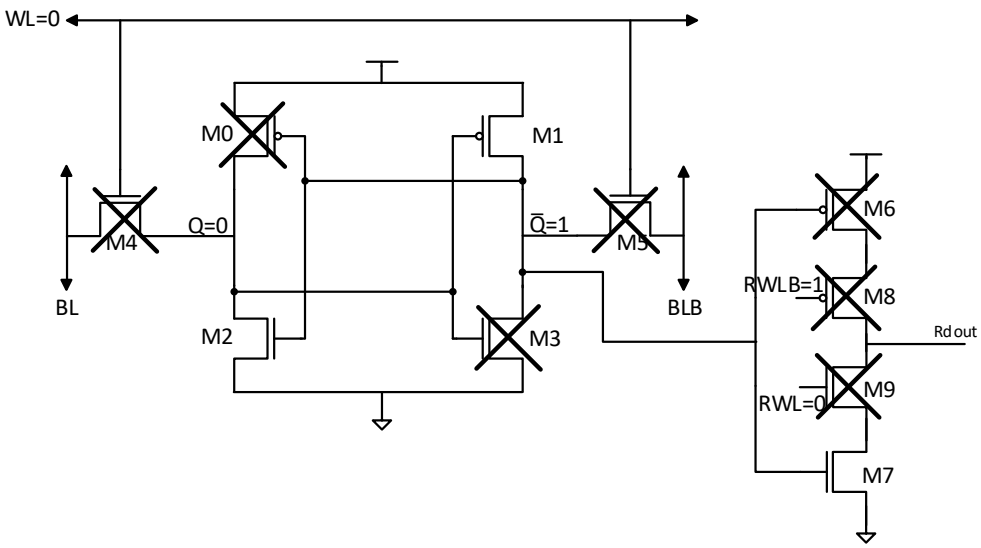

Figure 32 Proposed 10T SRAM Cell during Hold '0'

The leakage at read circuit happens during the write and hold phases. During write and hold phases, transistors M8 and M9 are OFF and the state of the transistors M6 and M7 depends on the value at $\overline{Q}$. Consider the case where $\overline{Q}$ is '0' as shown in *Figure 33*.

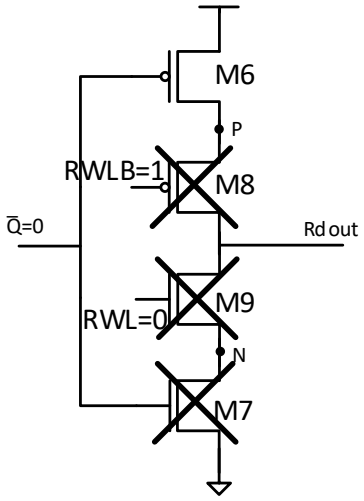

Figure 33 Proposed 10T Cell during QB=0

When $\overline{Q}$ is '0', the PMOS transistor M6 turns ON and the NMOS transistor M7 turns OFF. In this case, since M6 is ON, the potential at 'P' equals VDD. If Rdout is carrying '1', then the voltages at either side of M8 are same and so there is no leakage through M8. There will be leakage path through M9 and M7 but it is less because of the presence of two OFF transistors. If Rdout is carrying '0', there will be leakage through M8 and no leakage through M9, M7.

Now, consider the case where $\overline{Q}$ is '1' as shown in the *Figure 34*.

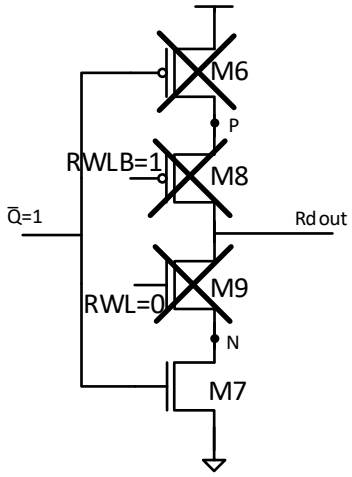

Figure 34 Proposed 10T Cell during QB=1

Since $\bar{Q}$ is '1', the NMOS transistor M7 is ON and the PMOS transistor M6 is OFF. In this case, since M7 is ON, potential at N is pulled down to GND. If the value at Rdout is '1', there will be leakage through M9 since potentials at either side of M9 are opposite and no leakage through M6, M8. If Rdout is carrying '0', then there will be leakage path through M8, M6 but it is less because of two series OFF transistors.

3. Simulation Results

3.1 Simulation setup for Proposed 10T SRAM Cell

Transient analysis is performed on the proposed 10T SRAM cell to find the cell parameters. The technology used for the simulation is 32nm FinFET. The supply voltage VDD is set to 1.0V. The simulation is run for a period of 8ns at a frequency of 1GHz. The order of phases of the simulation is,

Write ‘0’ – Hold ‘0’ – Read ‘0’ – Hold ‘0’ – Write ‘1’ – Hold ‘1’ – Read ‘1’ – Hold – ‘1’

Each of the above mentioned phases are of 1ns duration. *Figure 35* shows the schematic of the proposed 10T SRAM cell. *Figure 36* shows the schematic of the sense amplifier used for the simulation. *Figure 37* shows the block level simulation setup.

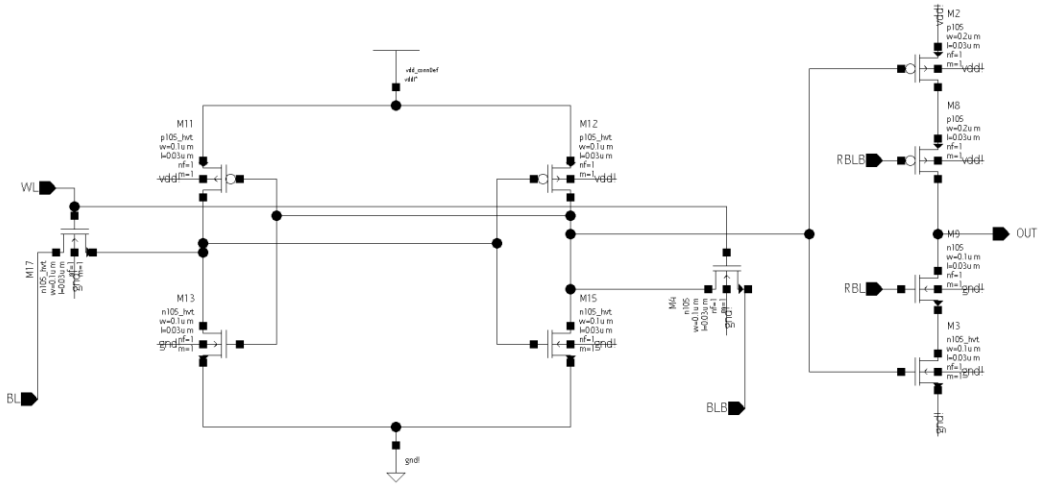

Figure 35 Schematic of Proposed 10T SRAM Cell

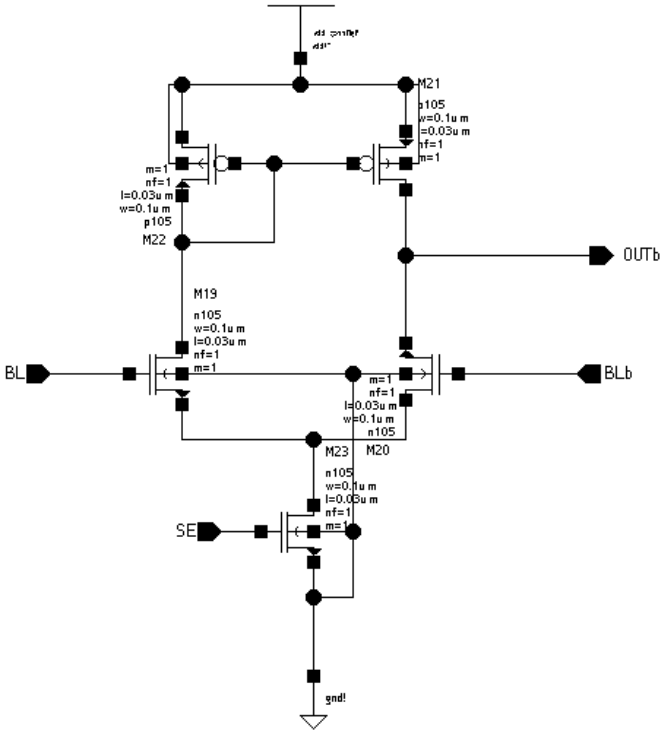

Figure 36 Schematic of Sense Amplifier

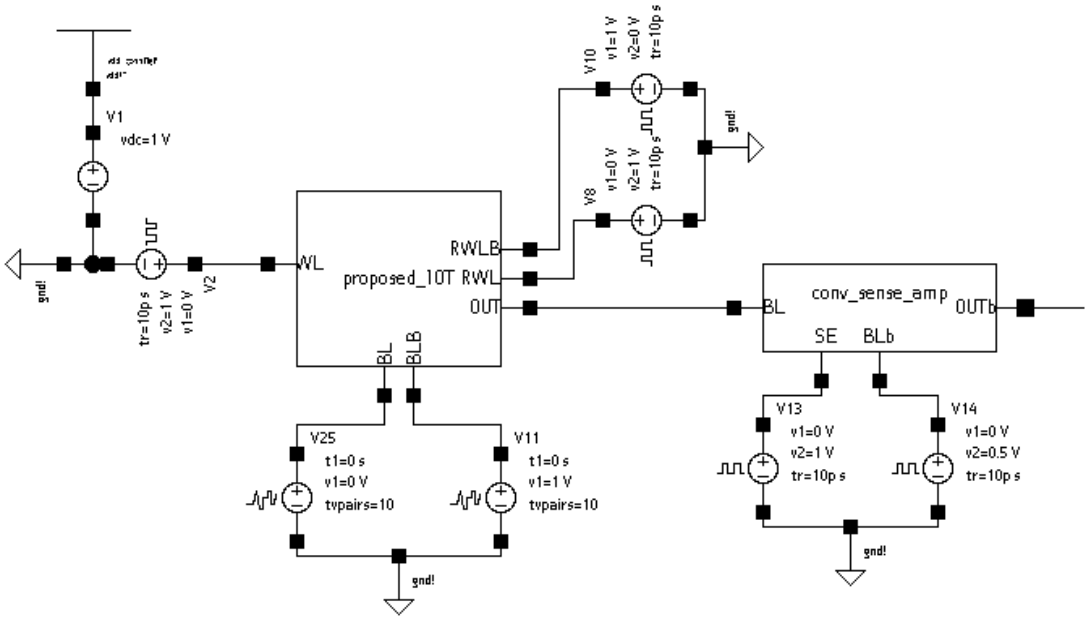

Figure 37 Simulation setup for proposed 10T SRAM Cell

Initially a write '0' operation is performed by setting the bit-lines BL and BLB to GND and VDD, respectively. The WL signal is activated which allows for the bits to be written onto the cell. After the initial write operation, the cell is brought to hold state by making the WL signal low. After holding the data for 1ns, the read operation is initiated where the RWL and RWLB signals are set to high and low respectively. At this instant, the bit $\overline{Q}$ gets inverted to Q at the output bit-line 'Rdout'. The sense amplifier, whose reference is set to VDD/2 (0.5V in this case), compares the value on Rdout to the reference voltage and gives the appropriate output as 'OUT'. After the read '0' operation, the cell goes to hold for 1ns and repeats the phases now with Q set to '1'.

. Signal ‘Rdout’ is the output bit-line of the SRAM cell and signal ‘OUT’ is the output of the sense amplifier. *Figure 38* demonstrates the SRAM operating correctly with the data nodes Q and QB being written with data correctly and the output bit-line Rdout being able to output the correct bit-value.

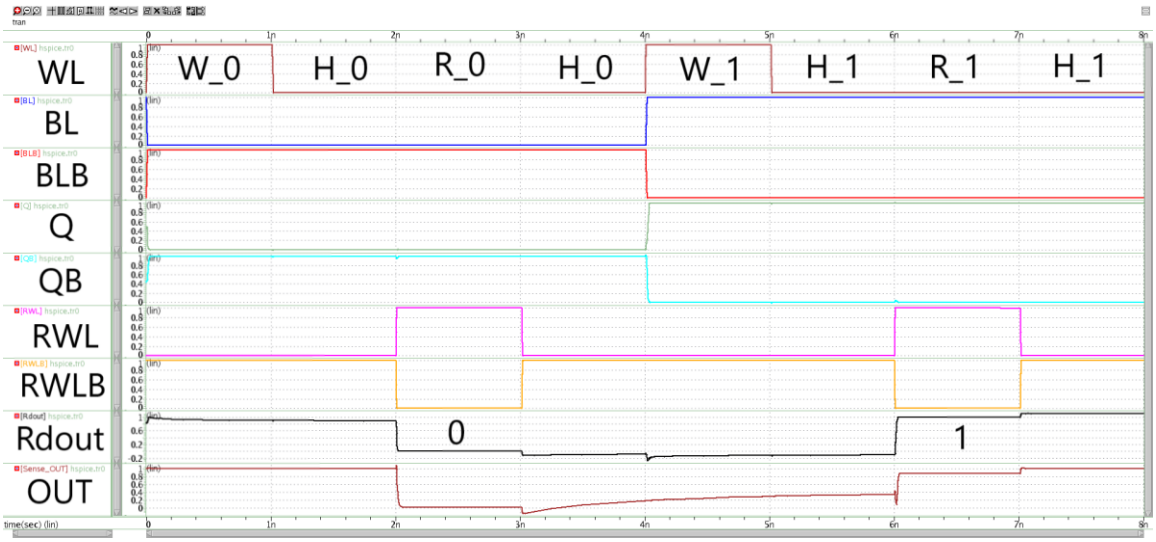

Figure 38 Simulation waveforms of proposed 10T SRAM Cell

Transient analysis is also done on the 6T, 8T and 10T bit cells and the read and write times are compared. These results are obtained from simulating a single bit cell and the conditions largely vary when the tests are performed on a whole memory stack/array. *Table 1* shows the write and read speeds of various SRAM cells where the proposed design has the fastest write speed and the conventional 6T design has the best read speed. t the cell level, the read and write times are close for different designs so it is hard to come to a conclusion yet. A 32-byte array is built for all the designs mentioned and the results are compared in section 3.5

Cell	Write (ps)	Read (ps)
6T	29.9	25.9
8T	36.4	26.8
10T	32.5	29.4
Proposed 10T	24.1	32.3

Table 1 Write and Read Speed comparison

3.2 Static Noise Margin (SNM) calculation of Proposed 10T SRAM

3.2.1 Read Static Noise Margin (RSNM)

Read Static Noise Margin is the maximum amount of noise that the cell can tolerate before its data is corrupted during read operation. To calculate RSNM, the bit cell is first set up according to the conditions of read operation i.e., the WL, RWLB signals are kept low and the RWL signal is kept high. A noise source 'Vn' is introduced at one of the bits (Q or $\overline{Q}$) and its value is varied from '0' to VDD. There are statistical methods [20], [11], [21] to measure SNM on which the current simulation procedure is based on. Consider the setup in *Figure 39*.

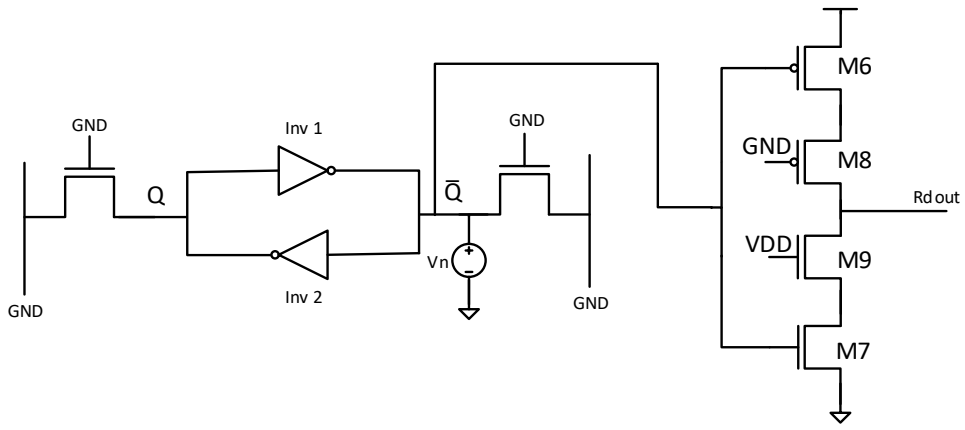

Figure 39 RSNM setup for Proposed 10T SRAM Cell

From *Figure 39*, a noise source 'Vn' is introduced at $\bar{Q}$. The noise source is varied from '0V' to '1V'(VDD) in this case. The voltage change at Q is recorded. The curve obtained this way is shown in *Figure 40*.

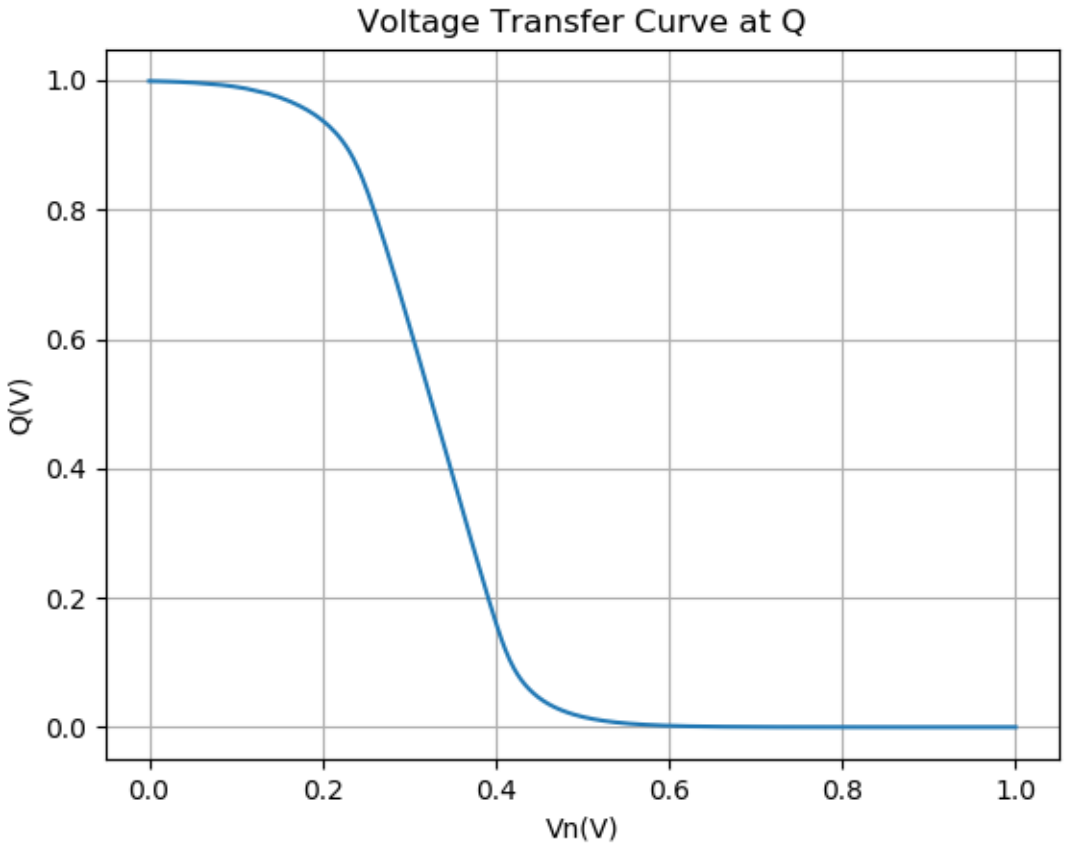

Figure 40 RSNM Voltage Transfer Curve at Q

The obtained curve (Q vs Vn) is called a Voltage Transfer Curve (VTC). Now, the noise source is moved to Q and the change in voltage at $\overline{Q}$ is recorded. This time when plotting the curve, the axis are inverted i.e., the curve to be plotted now is Vn vs $\overline{Q}$ as shown in *Figure 41*.

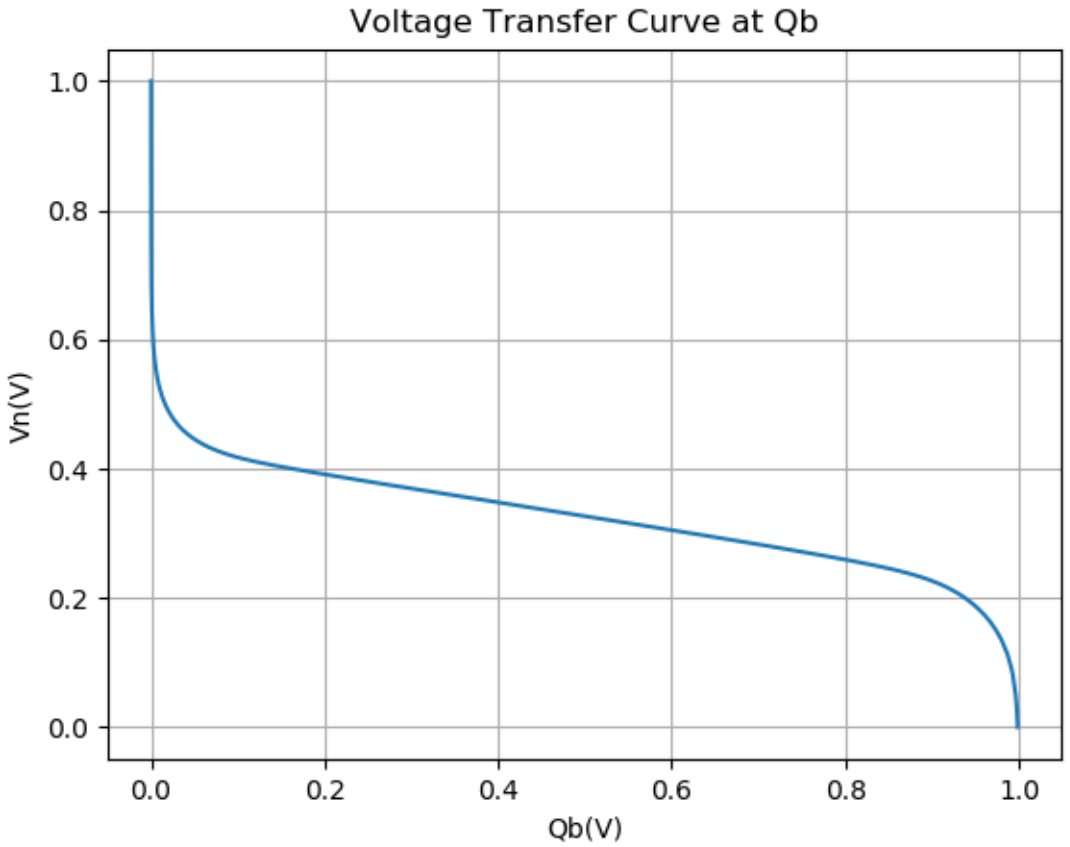

Figure 41 RSNM Voltage Transfer Curve at QB

Once both the VTCs are obtained, they are plotted on the same plane as shown in *Figure 42*.

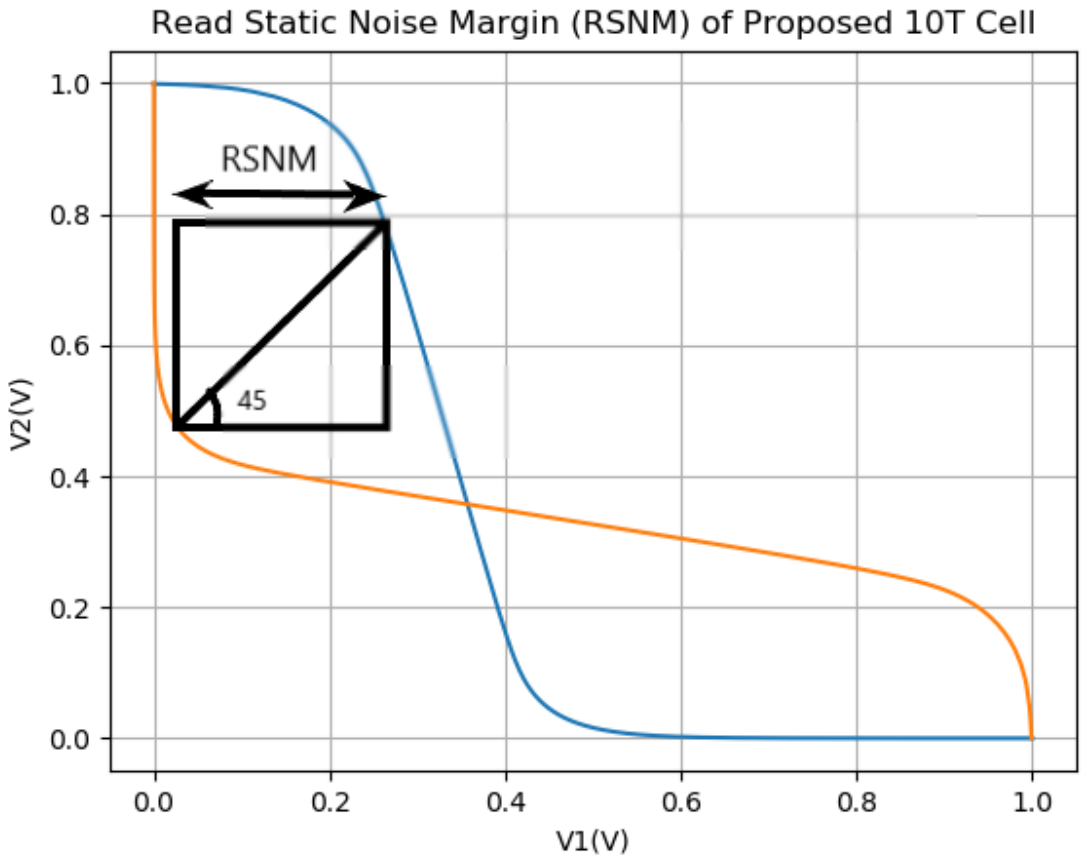

Figure 42 RSNM Voltage Transfer Curves of Proposed 10T

Now, as seen in *Figure 42*, two 'eyes' are formed by the VTCs. The RSNM is the size (side) of the largest square that can be fit in the eyes of the curves. If the sizes of the two largest squares (one square per eye) are different, then the smallest of them is chosen as RSNM.

Imagine a square in the eye as seen in *Figure 42*. If a diagonal, as shown in the figure, is drawn to that square, it will be 45˚ from both the axis and it will have its end points on the VTCs. Now, rotate the entire figure by 45˚ by the concept of rotation of axis. The end figure will look like the one in *Figure 43*.

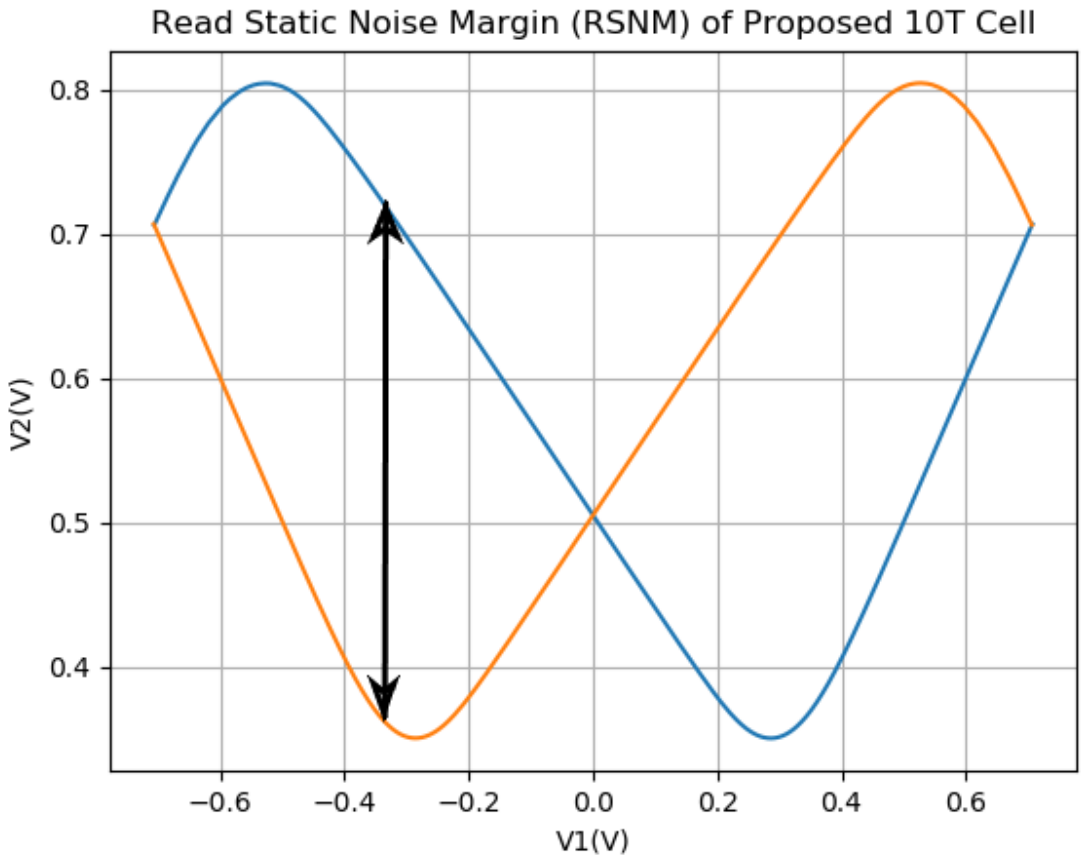

Figure 43 Rotated RSNM VTCs of Proposed 10T Cell

After the rotation of axis, the diagonal is now parallel to the y-axis. If the square we drew was the biggest possible square that can be fit in the eye, its diagonal is also the longest possible line that can be drawn between two points of the VTCs in an eye parallel to the y-axis. The length of the diagonal is the difference of y-coordinates at that particular x-coordinate. This means that, if we could plot a difference curve (VTC1-VTC2) along the x-axis, the peak of the difference curve is nothing but the longest diagonal (diagonal of the biggest square). Since we now know the length of the diagonal, the side (s) can be found

by considering a right-angled triangle within the square where the diagonal of the square becomes the hypotenuse (h) of the triangle. From Pythagorean theorem,

$$h^2 = s^2 + s^2 \quad (3)$$

$$s = {}^{h}/_{\sqrt{2}} = \text{RSNM} \quad (4)$$

The internal nodes of the proposed 10T cell are unaffected during the read operation unlike 6T. So, the RSNM in the proposed 10T cell is improved when compared to that of 6T. There is no design constraint like cell-ratio for the proposed 10T cell unlike 6T as the access transistors are in OFF state during read.

The Read Static Noise Margin of proposed 10T cell under the setup in *Table 2* is 254mV as shown in *Figure 44*.

VDD	1.0V
Pull-up Transistor (W/L)	100nm/30nm
Pull-down Transistor (W/L)	200nm/30nm
Access Transistor (W/L)	100nm/30nm
Cell-ratio	2
Pull-up ratio	1

Table 2 Simulation Conditions of SRAM Cell

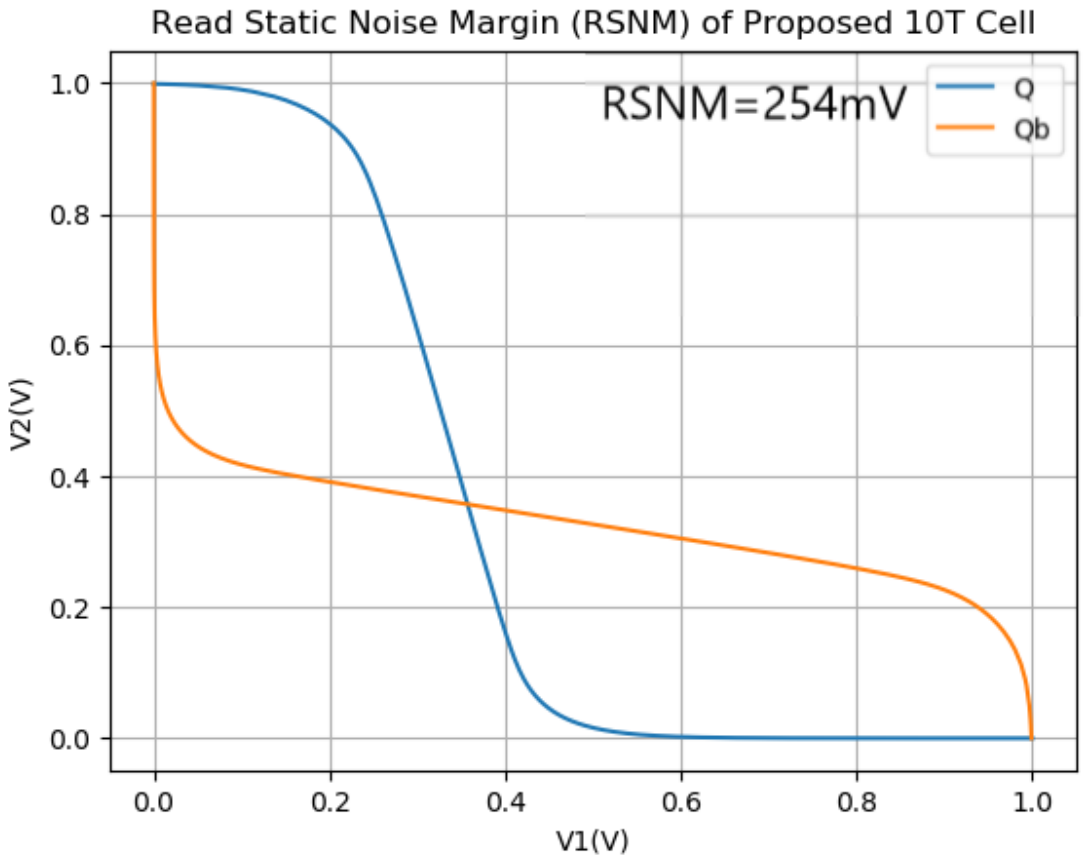

Figure 44 RSNM VTCs of Proposed 10T SRAM Cell

3.2.2 Variation of RSNM with VDD and Temperature

The SRAM cell could be operated in different working conditions and it is important to know the stability of the cell in these conditions. The variations in supply voltage (VDD) and temperature (T) are considered and stability is calculated to know the effects of these variations.

The variation of RSNM with supply voltage VDD is illustrated in *Figure 45*. The simulations are done under the setup in *Table 2* (except for VDD).

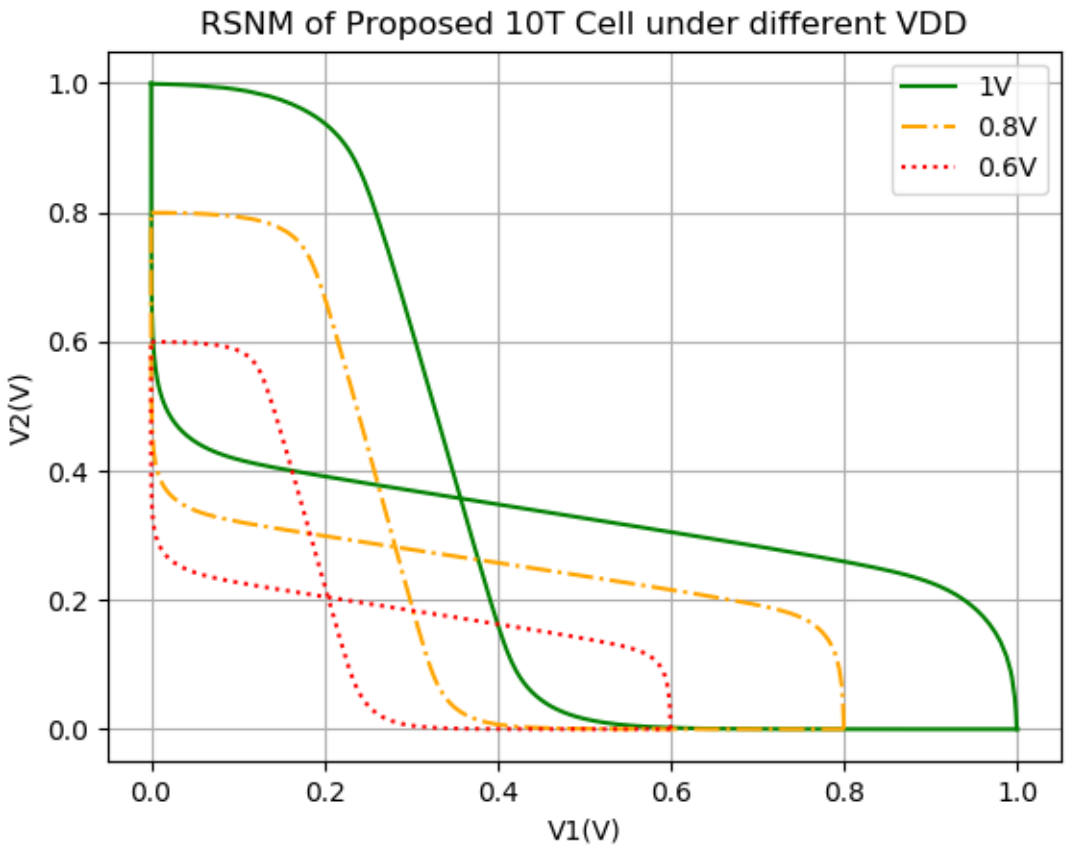

Figure 45 RSNM VTCs of Proposed 10T Cell under different VDD

As seen from *Figure 45***,** the butterfly curves shrink as VDD reduces. The 'eyes' shrink which indicates the decreasing of RSNM with decrease in supply voltage. Hence, reducing the supply voltage might save power but at the cost of stability as shown in *Figure 46*.

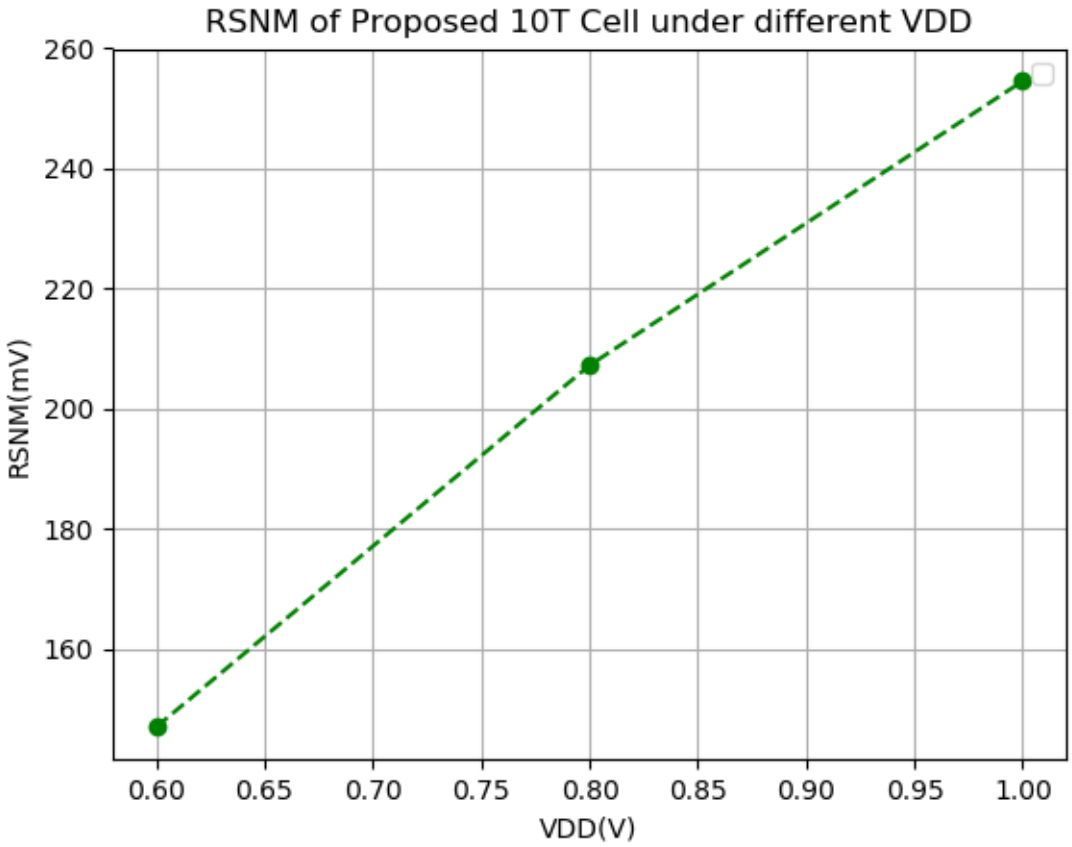

Figure 46 RSNM of Proposed 10T Cell under different VDD

The variation of RSNM with temperature is shown in *Figure 47*. The simulations are done under the setup in *Table 2*. As seen from the *Figures 47 and 48*, the RSNM of the cell decreases with increase in temperature, but not much. It varies from 259mV to 242mV as temperature changing from 0 to 120ºC. It is to be noted that the temperature of the cell is affected by both the environment conditions and the functions/processes done on the component.

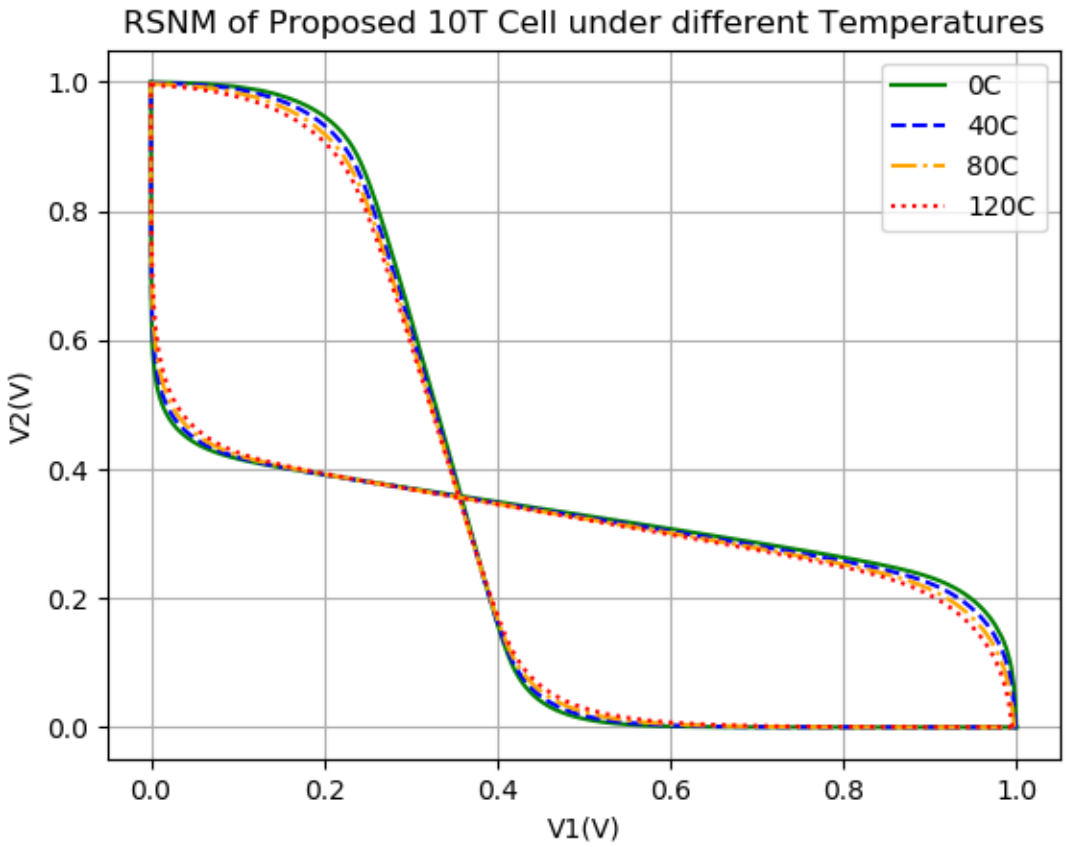

Figure 47 RSNM VTCs of Proposed 10T Cell under different Temperatures

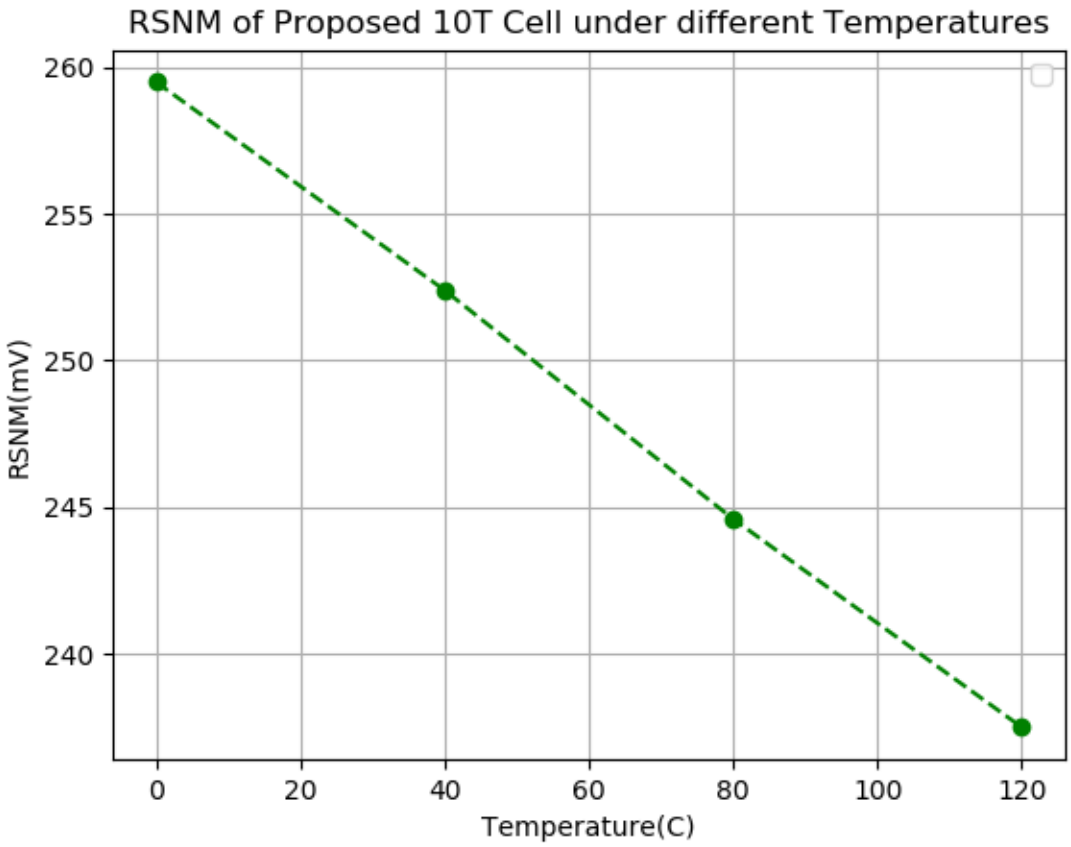

Figure 48 RSNM of Proposed 10T Cell under different Temperatures

3.2.3 Hold Static Noise Margin (HSNM)

Hold Static Noise Margin is the maximum amount of noise that the cell can tolerate before its data is corrupted during hold state. To calculate the HSNM, the bit cell is first set-up so as to maintain it in hold state i.e., the signals WL, RWL are set to low and RWLB is set to high. A noise source 'Vn' is introduced at one of the bits (Q or $\overline{Q}$) and it is varied from '0' to VDD. Consider *Figure 49.*

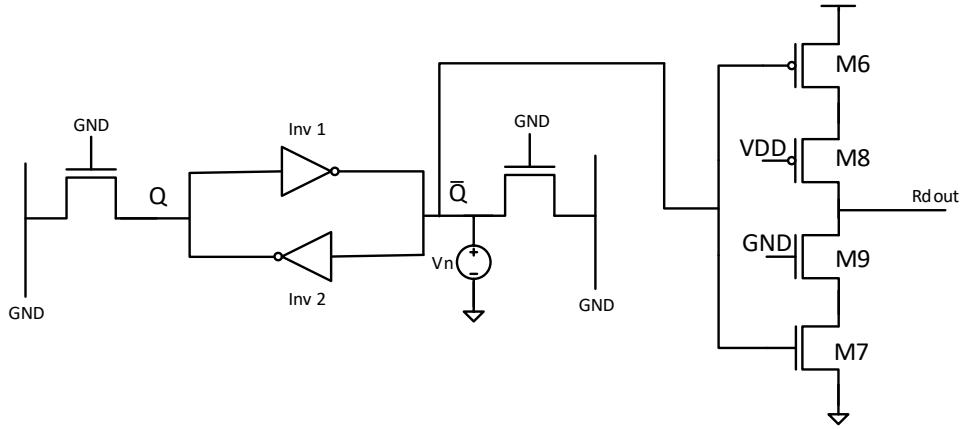

Figure 49 HSNM Simulation setup for Proposed 10T SRAM Cell

The process of finding HSNM is the same as that of finding RSNM. Two Voltage Transfer Curves (VTCs) are drawn to obtain a butterfly curve and the largest possible squares are fit in the eyes. The side of that square is the HSNM of the cell. The internal nodes are not affected during the hold state, same as in the case of read operation. For the proposed 10T SRAM cell, the value of HSNM is the same as that of RSNM. *Figure 50* shows the VTCs of the proposed 10T cell during hold state. The simulations are performed according to the setup in *Table 2*.

The effect of supply voltage and temperature on HSNM is the same as that of RSNM for the proposed 10T cell. Refer *Figures 45, 46, 47 and 48* for effect of supply voltage and temperature on HSNM.

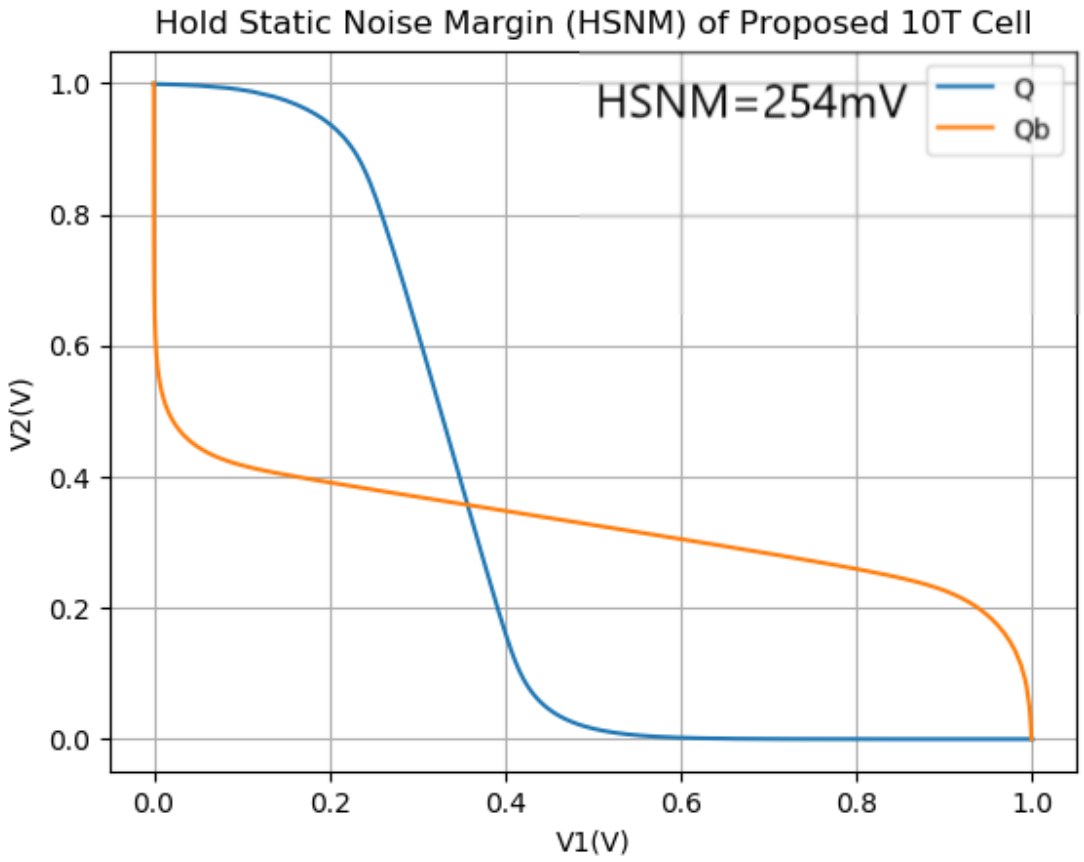

Figure 50 HSNM VTCs of Proposed 10T SRAM Cell

3.2.4 Write Static Noise Margin (WSNM)

Write Static Noise Margin of a cell is the maximum amount of noise that it can tolerate beyond which the data can't be written. WSNM is the minimum amount of noise which when acted moves the VTCs to a point where there exists a second stable operating point. To calculate the WSNM of the cell, the control signals are set-up for write operation as shown in *Figure 51*.

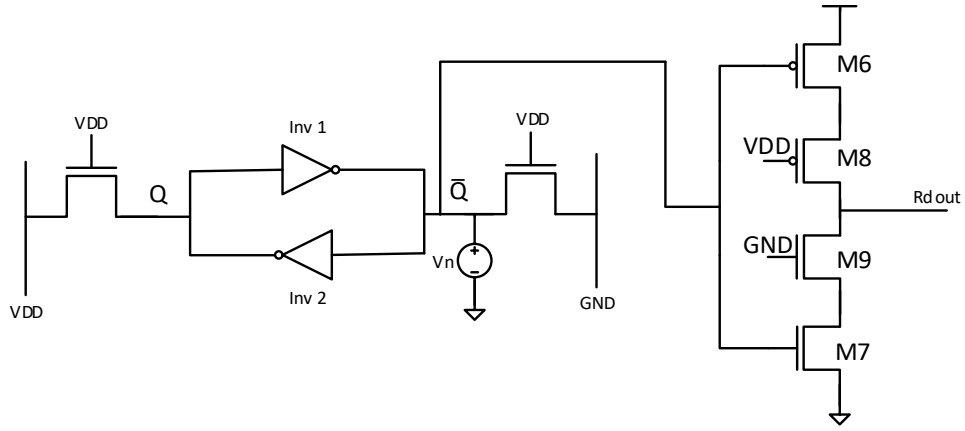

Figure 51 WSNM Simulation setup for Proposed 10T SRAM Cell

As seen from *Figure 51*, the signals WL, RWLB are set to high and RWL is set to low. The data being written to the cell is '1' (Q) and so the BL is set to VDD and BLB is set to GND. A noise source 'Vn' is introduced at $\overline{Q}$ and is varied from '0' to VDD. During this time, the voltage change at Q is plotted. Next, the noise source is moved to Q and the voltage change at $\overline{Q}$ is plotted. Upon plotting the two VTCs on the same plane ($\overline{Q}$'s VTC axis is inverted), the diagram is displayed in *Figure 52*.

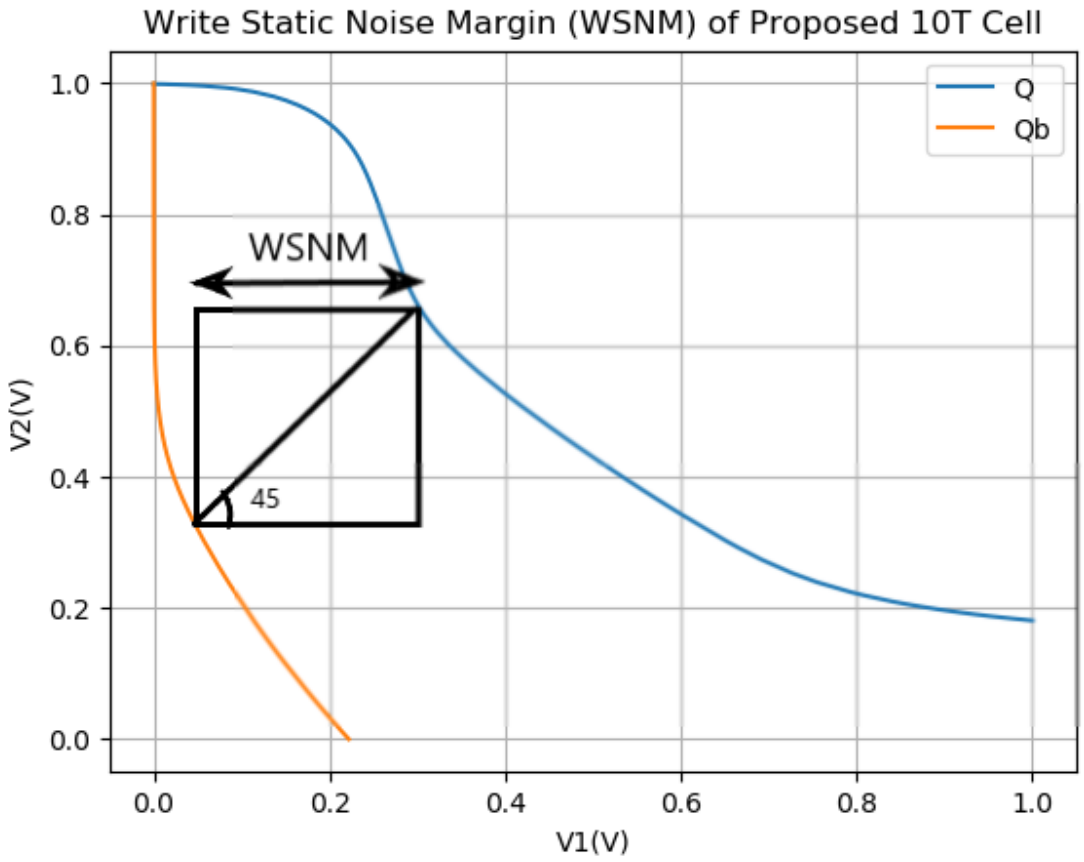

Figure 52 WSNM VTCs of Proposed 10T SRAM Cell

The graph has a single stable point which indicates a successful write operation. A second stable point means the write has failed [22]. If the two VTCs shown in *Figure 52* are brought close to each other, a second stable point would come up. The WSNM is the amount of noise that's separating the two curves to get to this second stable point. Consider *Figure 53* where the entire graph is rotated by 45˚.

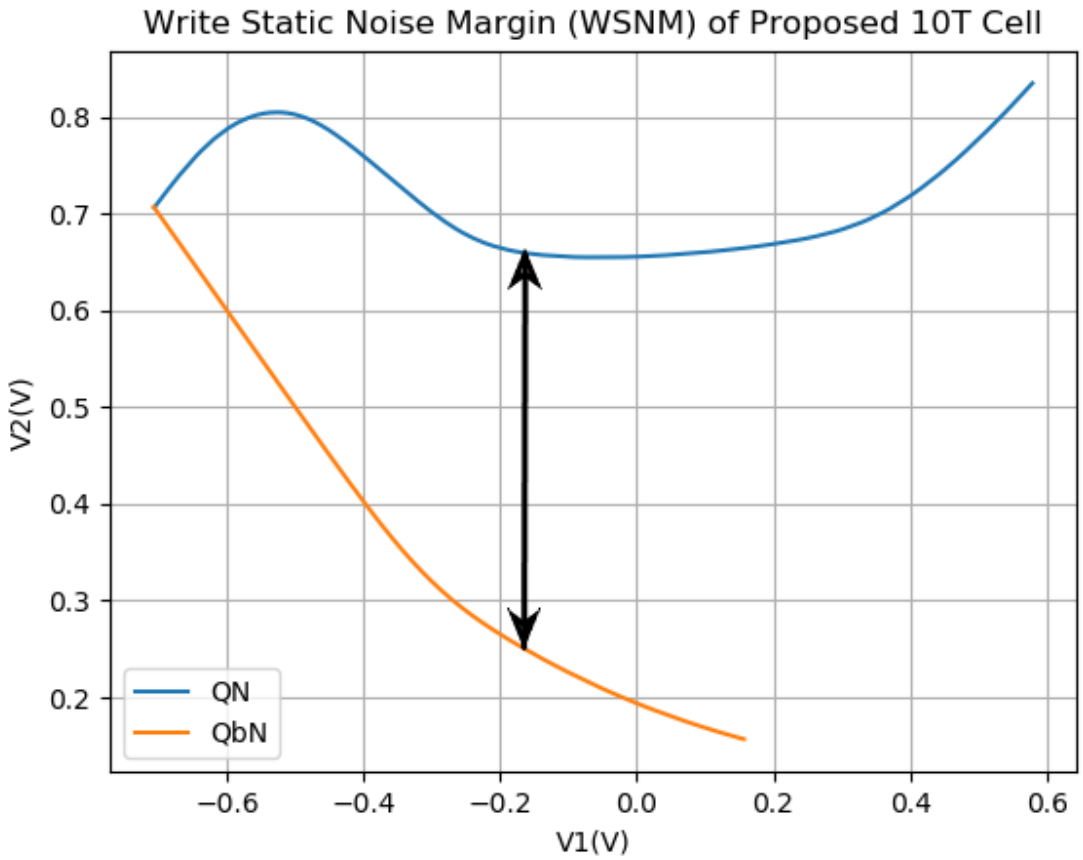

Figure 53 Rotated WSNM VTCs of Proposed 10T SRAM Cell

If we draw a difference curve between the two VTCs starting from the right hand side of the graph, we would reach a local minimum (in this case at x = -0.18V) after which the difference rises and then falls back to zero. The line drawn parallel to the y-axis, in this case, where we reach the first local minimum coming from the right hand side, is the diagonal of the required square. The side of this square is the WSNM of the cell.

The WSNM of the proposed 10T SRAM cell is 275mV as shown in *Figure 54*. The simulations are done under the same setup in *Table 2*.

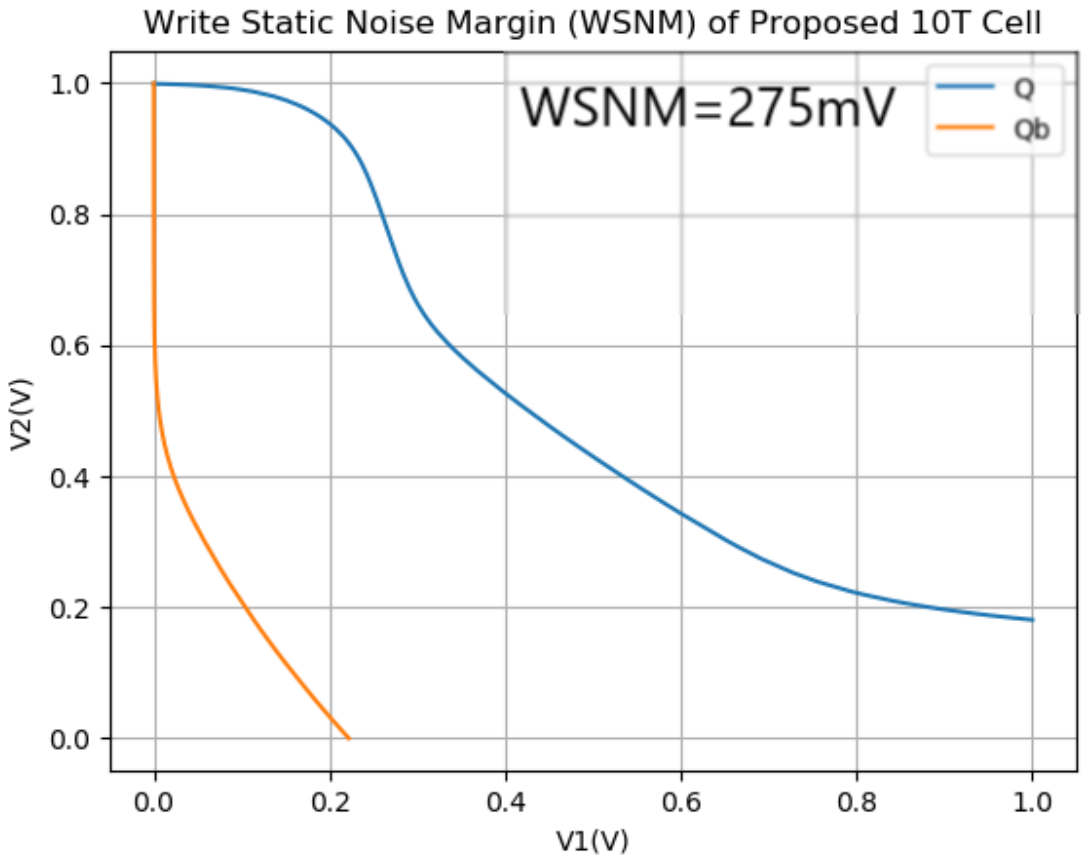

Figure 54 WSNM VTCs of Proposed 10T SRAM Cell

3.2.5 Variation of WSNM with Pull-up Ratio (PR)

Pull-up Ratio is the ratio of (W/L) of PMOS pull-up transistor to the ratio of (W/L) of NMOS access transistor. Considering three cases of PR as shown in *Table 3*, the variation of WSNM of the proposed 10T SRAM cell is plotted in *Figures 55 and 56*. As

discussed in *Section 2.2.1*, lowering the pull-up ratio improves the WSNM or writability of the SRAM cell.

W/L of Pull-up Transistor	W/L of Access Transistor	Pull-up Ratio (PR)
100nm/30nm	200nm/30nm	0.5
100nm/30nm	100nm/30nm	1
150nm/30nm	100nm/30nm	1.5

Table 3 Transistor sizes for different Pull-up Ratios

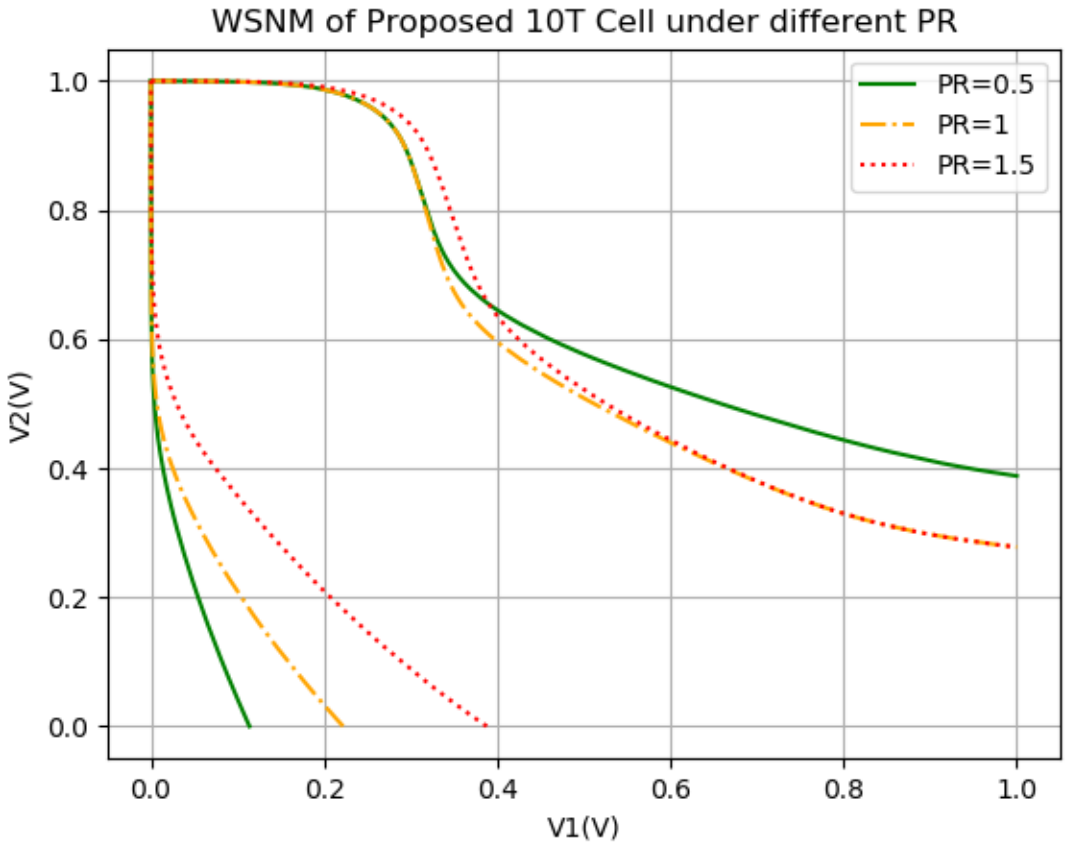

Figure 55 WSNM VTCs of Proposed 10T SRAM Cell under different Pull-up Ratios

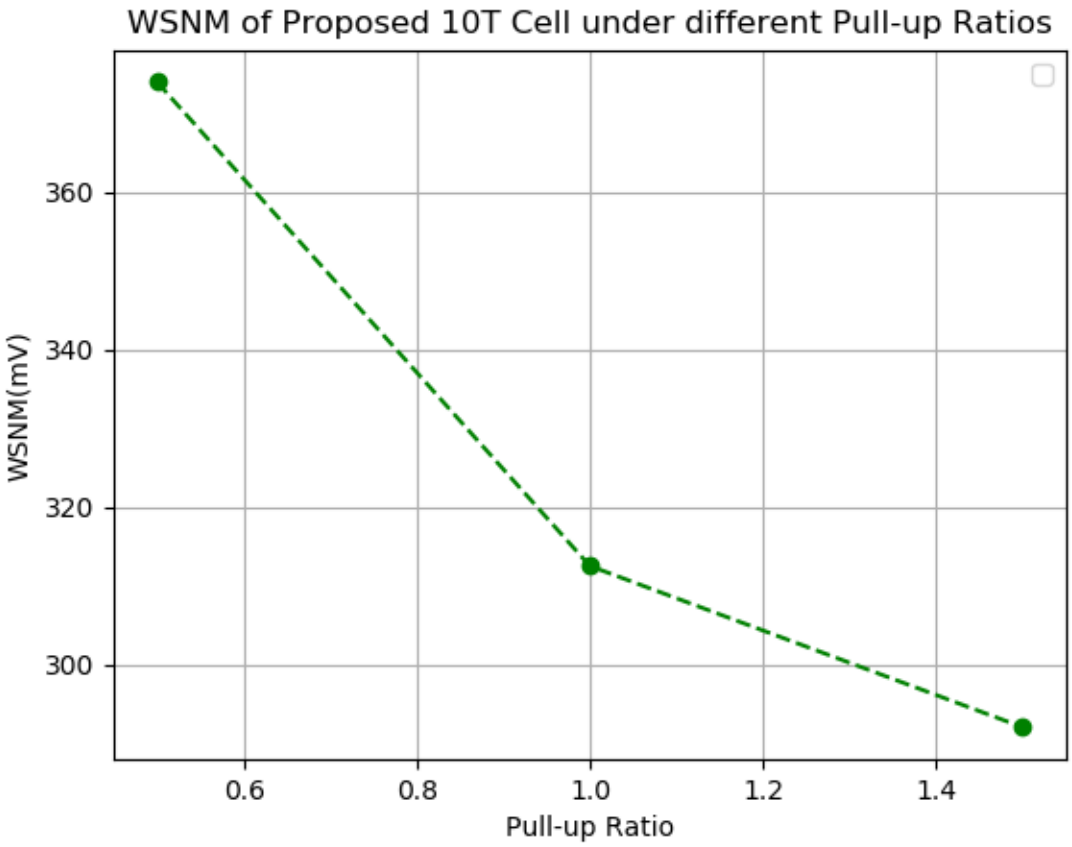

Figure 56 WSNM of Proposed 10T SRAM Cell under different Pull-up Ratios

3.2.6 Variation of WSNM with VDD and Temperature

The proposed 10T SRAM cell is tested for its writability under different supply voltages and temperatures. The cell's PR is kept at 1.5 (150nm/100nm). *Figure 57* shows the VTC plots under different supply voltages at a temperature of 25˚C.

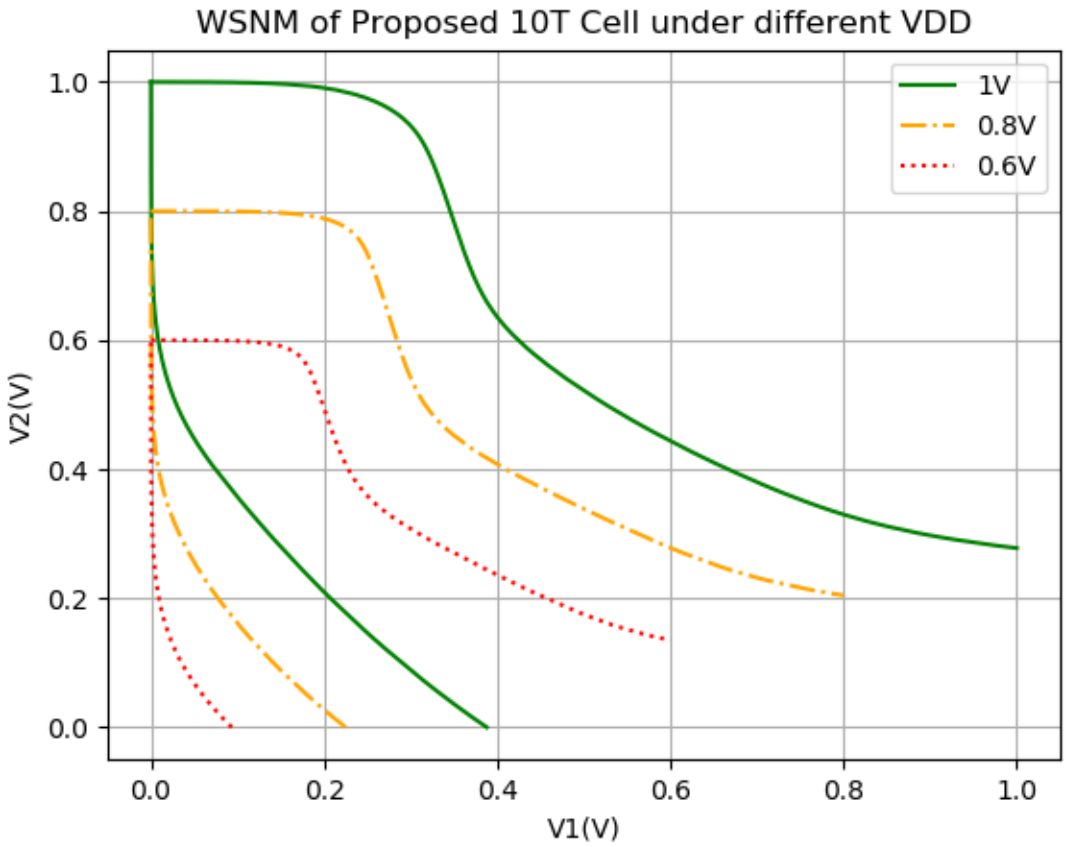

Figure 57 WSNM VTCs of Proposed 10T SRAM Cell under different VDD

Reducing the supply voltage would save power but at the cost of WSNM. The variation of WSNM with supply voltages is as plotted in *Figure 58*.

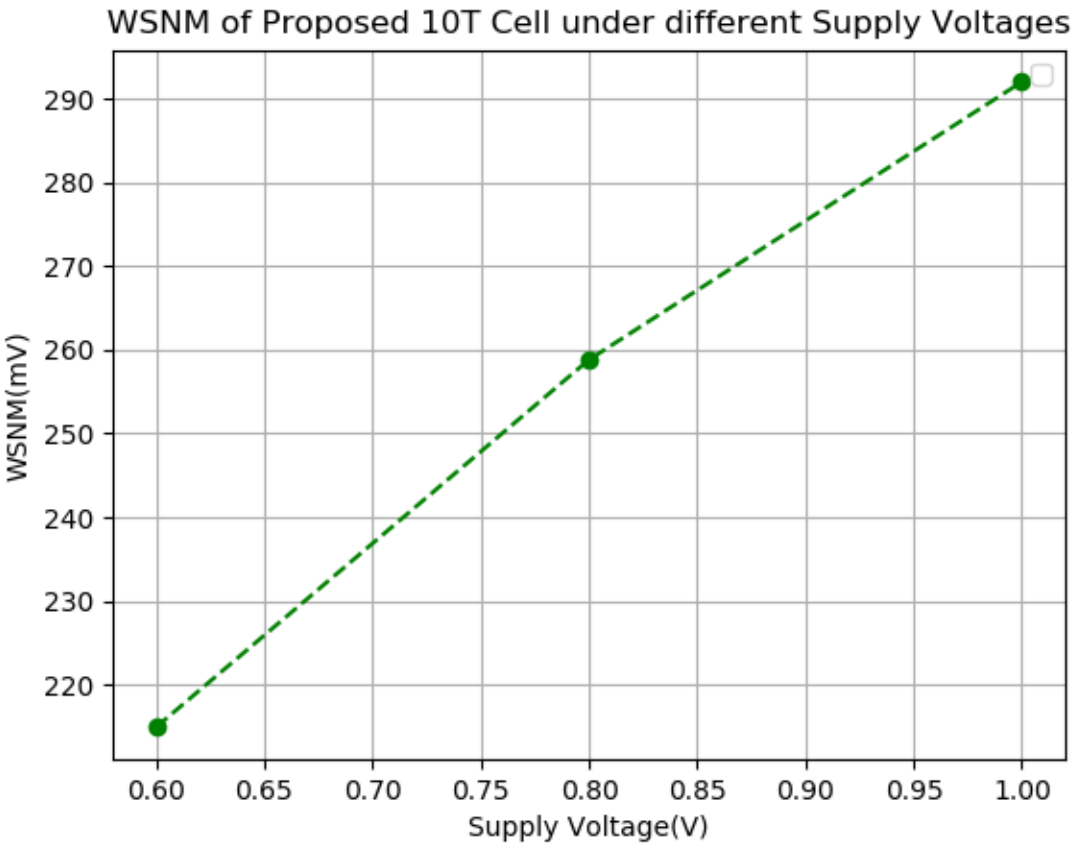

Figure 58 WSNM of Proposed 10T SRAM Cell under different VDD

Figure 59 shows the VTC plots under different temperatures at a supply voltage of 1.0V.

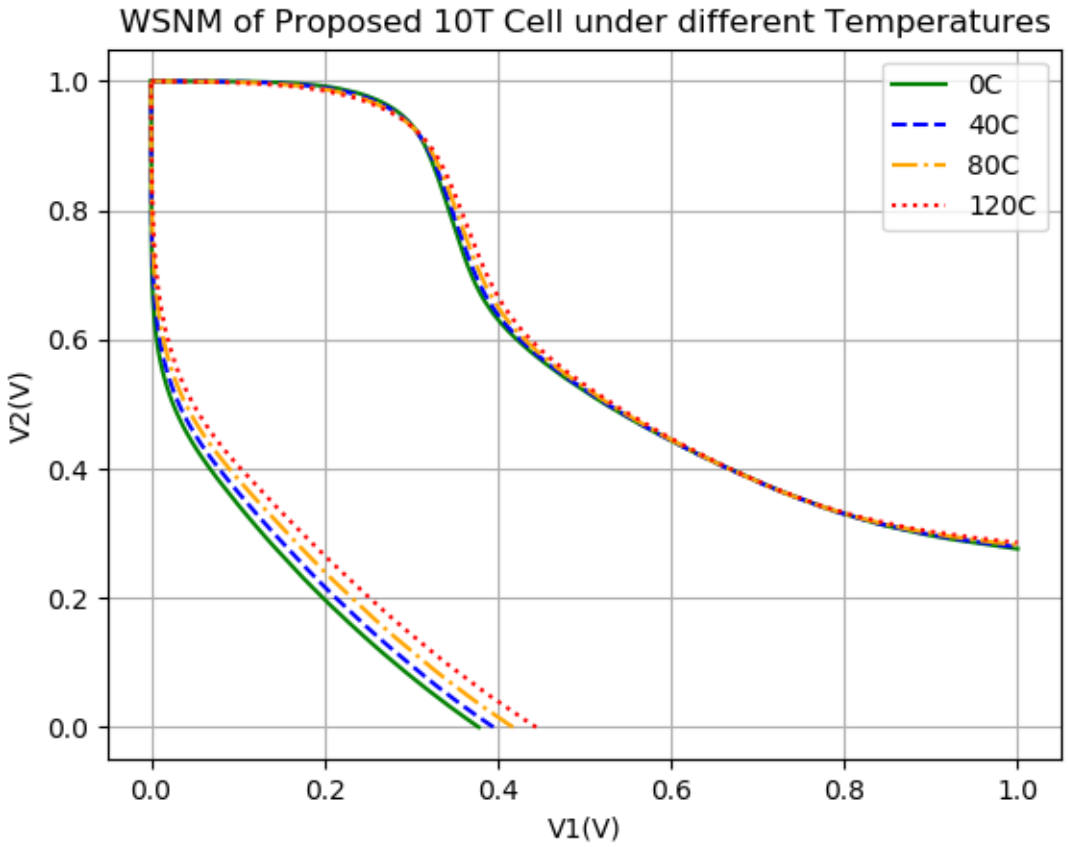

Figure 59 WSNM VTCs of Proposed 10T SRAM Cell under different Temperatures

From *Figure 60*, it can be observed that as the temperature increases, the WSNM decreases. The variations in operating temperature could be due to the environment conditions or the work load on the components.

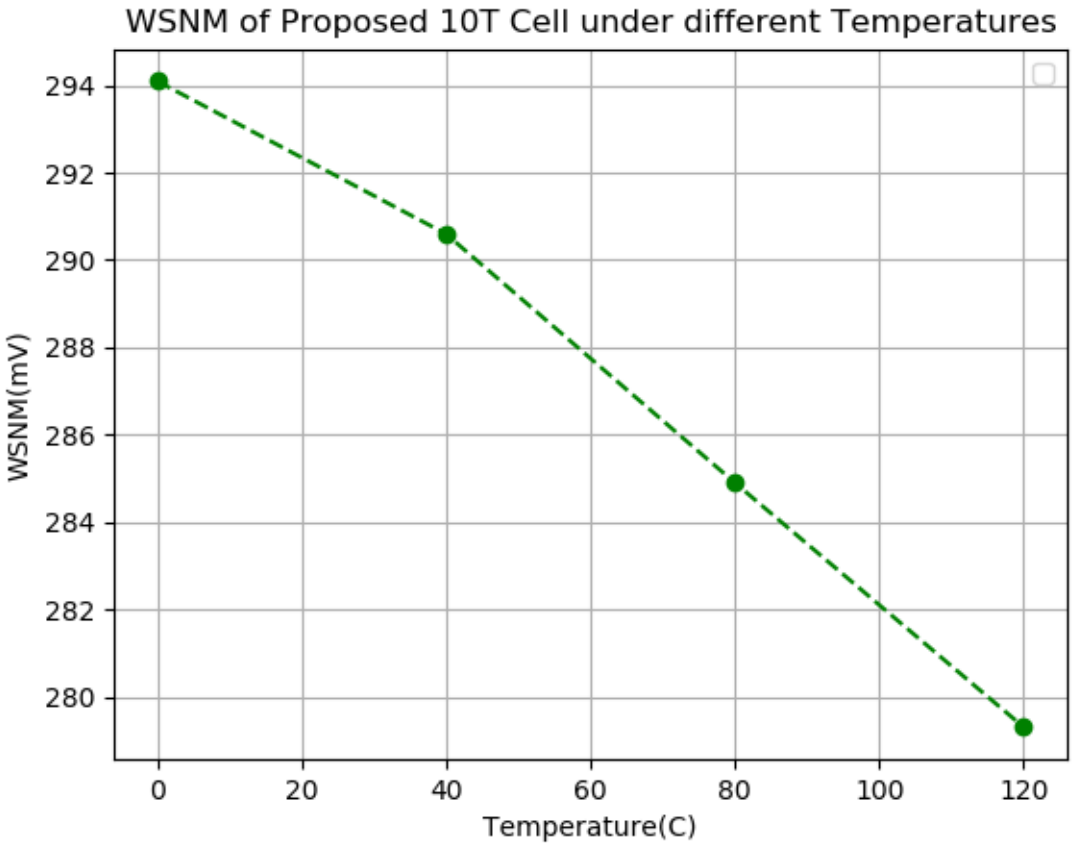

Figure 60 WSNM of Proposed 10T SRAM Cell under different Temperatures

3.3 Static Noise Margin Comparison

Static Noise Margins of different bit cells that are considered here are compared. The 6T, 8T, 10T and Proposed 10T cell designs all have the same write circuit but differ in their read circuits. The read operation in 6T cell is done along the same bit-lines that are used for writing whereas the remaining cells perform read operation through a single output bit-line. The bit-lines are pre-charged in 6T and 8T cells before the read operation whereas in 10T and Proposed 10T cells, there is no pre-charge of output bit-lines. The 6T has the

lowest RSNM and the rest of the designs have equal values of RSNM. This is because, unlike the 6T cell, the bit $\overline{Q}$ drives the gate(s) of transistors in 8T, 10T and Proposed 10T designs. The HSNM values are the same for all the designs as all their inner cells are isolated from the rest of the cell during hold phase.

And since they all have the same write circuit, the WSNM values are same for all at a particular pull-up ratio. *Figure 61* shows the comparison of RSNM, HSNM and WSNM of different cells. All the cells have same pull-up ratio of '1' and the 6T cell has a cell-ratio of '5'. Cell ratio is a design constraint only for the 6T cell. All the simulations are performed at a VDD of 1V at 25˚C temperature.

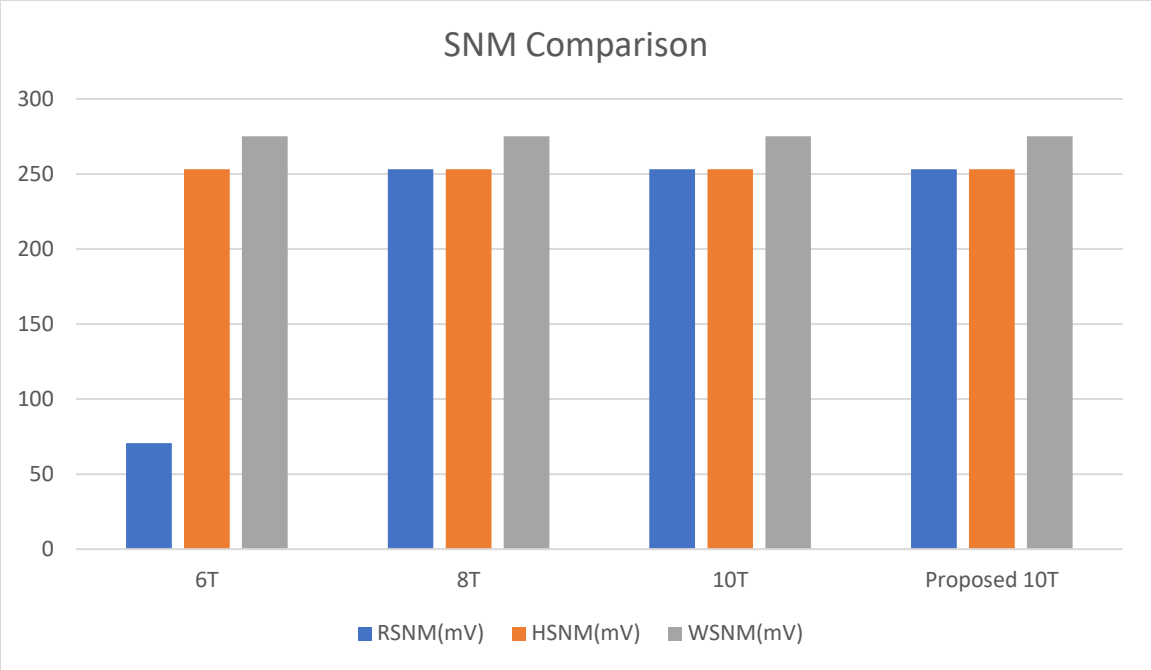

Figure 61 Static Noise Margin Comparison of different SRAM Cells

The proposed 10T cell has improved RSNM when compared to 6T cell but maintains the same WSNM and HSNM as the rest of the designs. Attempts have been made to improve the SNM of SRAM cells. One of them is to have a Schmitt-inverter instead of a regular inverter. Designs have been proposed [23], [24], [25], [26], [27], [28], [29] with success in improving SNM this way. The disadvantage it brings is increased area as it adds four transistors to the regular inverter.

3.4 32-bit*8-bit 10T Array

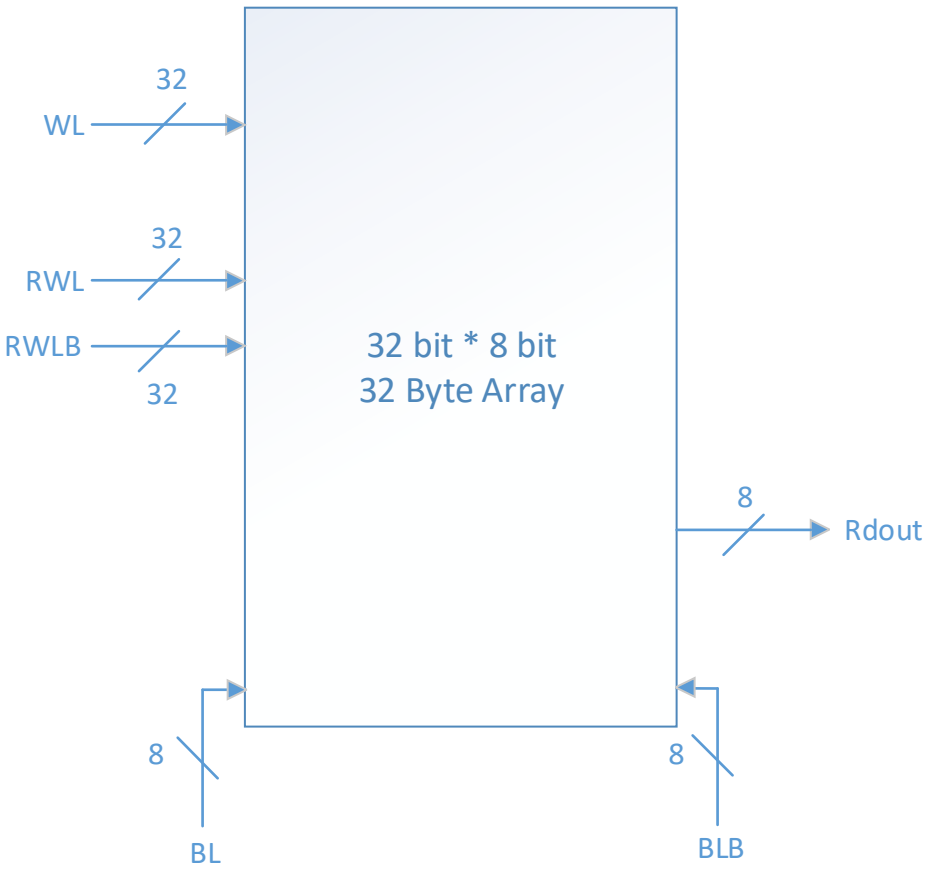

Figure 62 Block diagram of 32 Byte SRAM Array

A 32-byte memory array was built from the proposed 10T SRAM cells. The memory array has 32 word-lines each of 8-bits wide as shown in *Figure 63*. The simulation is carried in such a way that the 0^{th} word is written initially followed by the 17^{th} word and then the data is read from the 0^{th} word followed by the 17^{th} word. *Figure 64* shows the stimuli to the array. An 8-bit data '11010010' is written to the 0^{th} word. Then after leaving it in standby mode for a while, the 17^{th} word is written as '10011100'. *Figure 65* shows the input data for '0'th word and 17^{th} word.

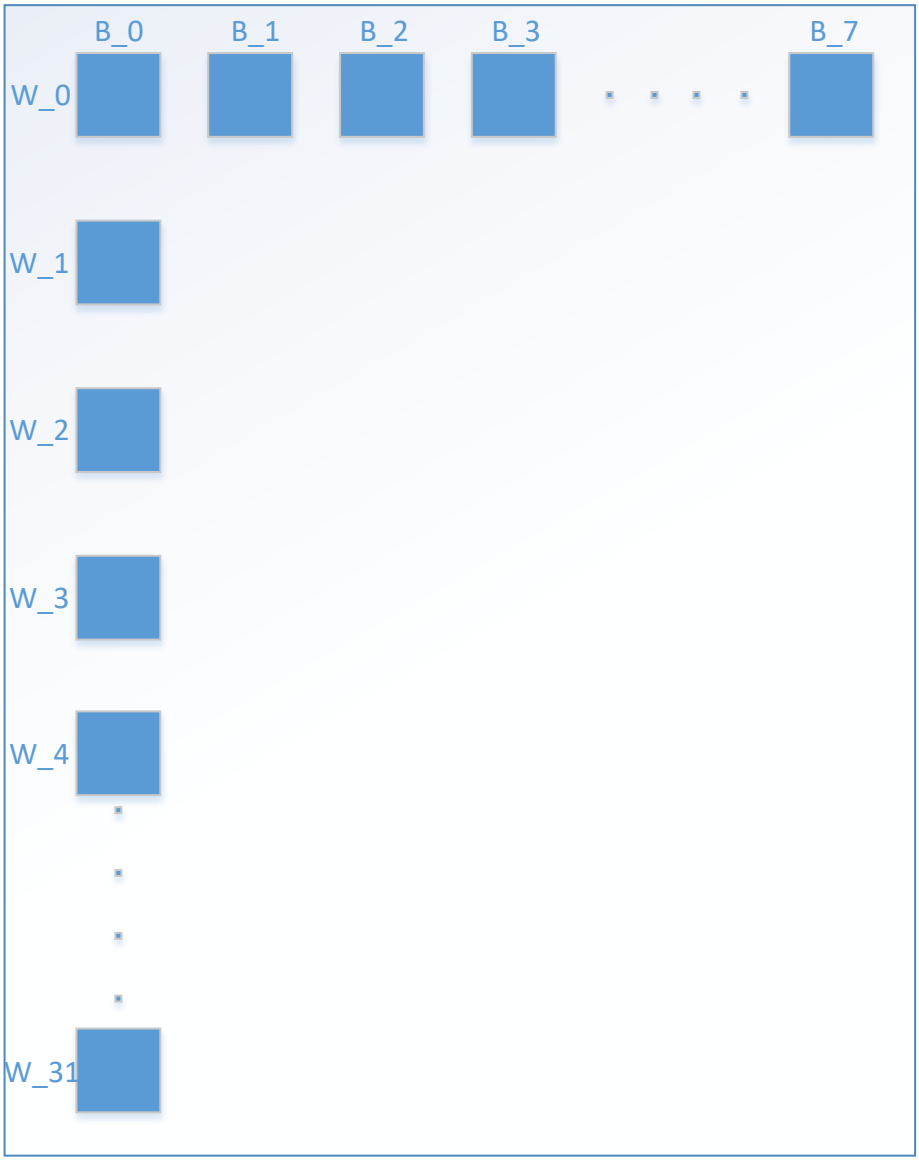

Figure 63 Matrix of 32 Byte SRAM Array

And then again leaving the array in standby mode for a while, data is read from the 0^{th} word followed by a short standby phase. Finally, the data from the 17^{th} word is read. *Figure 66* shows the output data at sense amplifiers during read operations. The data bits are chosen in such a way that all possible bit-value transitions occur between the 0^{th} and 17^{th} word i.e., '0' to '1', '1' to '0', '0' to '0' and '1' to '1'.

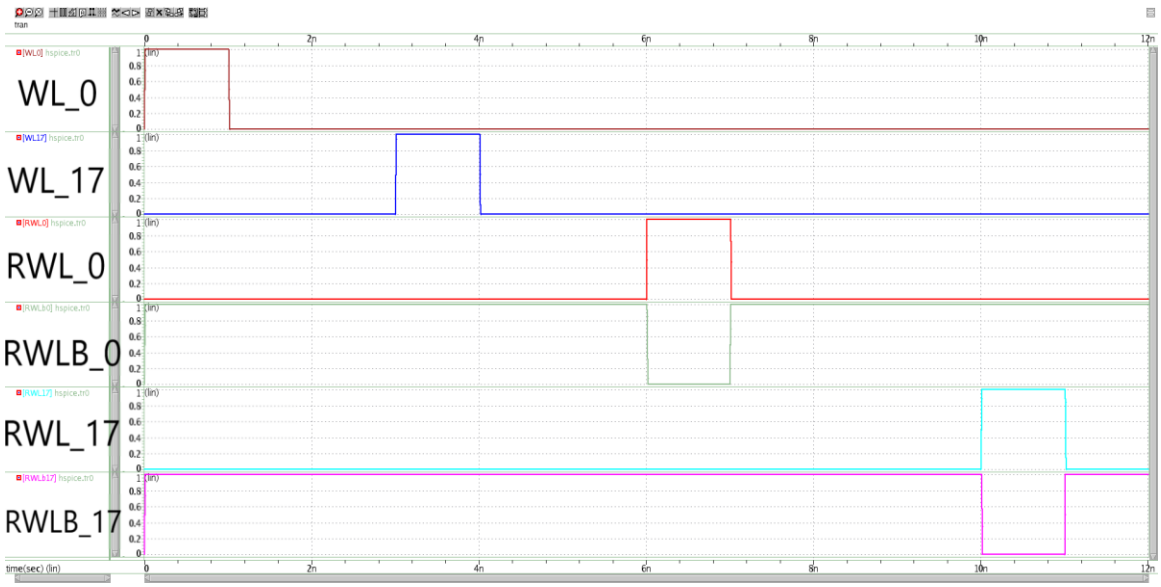

Figure 64 Stimuli for 32 Byte SRAM Array

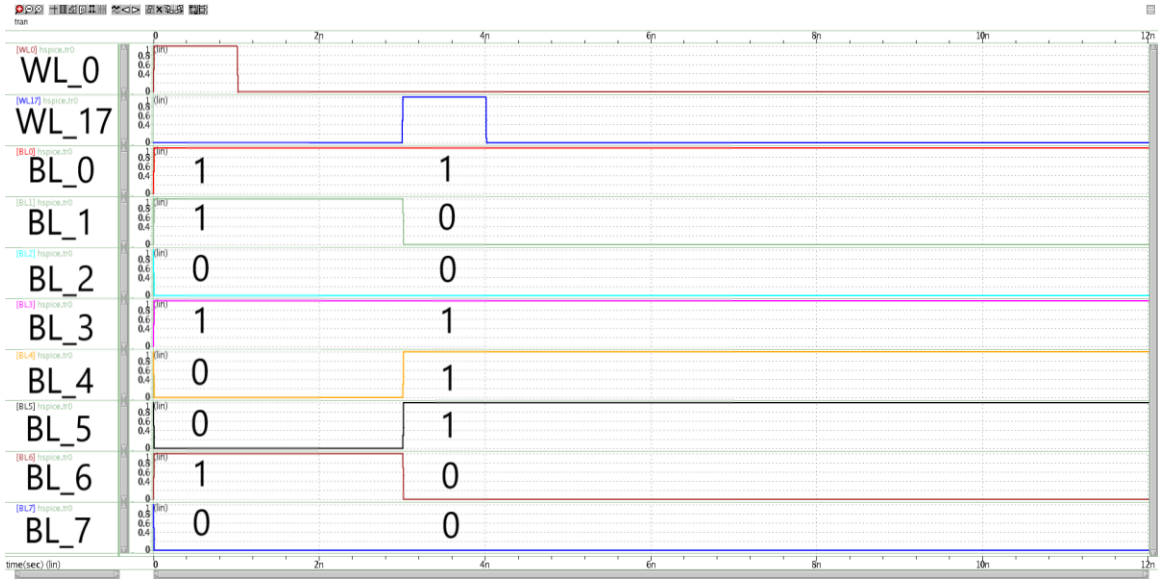

Figure 65 Input data words to 32 Byte SRAM Array

The transient analysis is run for a period of 12ns at a supply voltage of 1V and a temperature of 25˚C. Both the Cell-Ratio and Pull-up Ratio of the cells are set to '1'. *Table 4* shows the read and write times of the array.

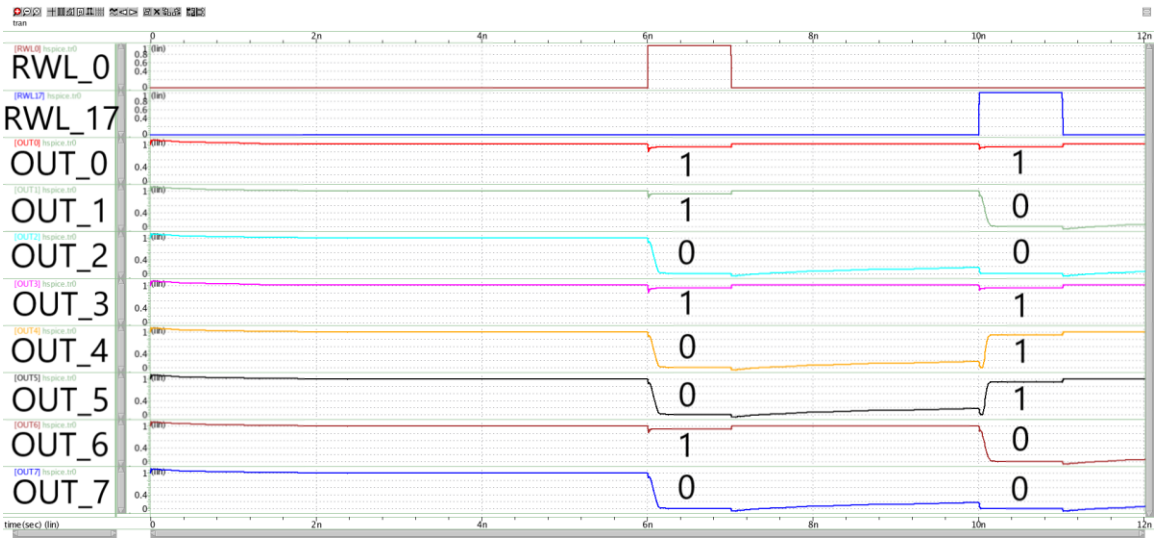

Figure 66 Output Data of 32 Byte SRAM Array

Operation	Time (ps)
Write '0'	15.4
Write '1'	21.6
Read '0'	149
Read '1'	106

Table 4 Write and Read speeds comparison of Proposed 10T 32 Byte Array

The write speeds are calculated at the internal node 'Q' of the cells with respect to the write signal WL. The read times are measured at the output of sense amplifier with respect to sense enable signal SE. The read speeds are measured during the data read of the 17^{th} word in order to see the effect of data transition on the output Rdout line from reading

the 0^{th} word to 17^{th} word. The average power is measured to be 13.8uW over the 12ns simulation period. The power consumption is at peak during the read phases at around 42uW. It is to be noted that sense amplifiers are part of the circuit and they have effect on the power consumed. During read operation, the power is consumed when there is a change in values read from the previous read operation. For example, if the previous bit value read is '1' and the current bit value read is also '1', the OUT line doesn't need to charge/discharge its value. *Figure 67* shows four cases where the out-line value is changed during two cases and does not change in the other two.

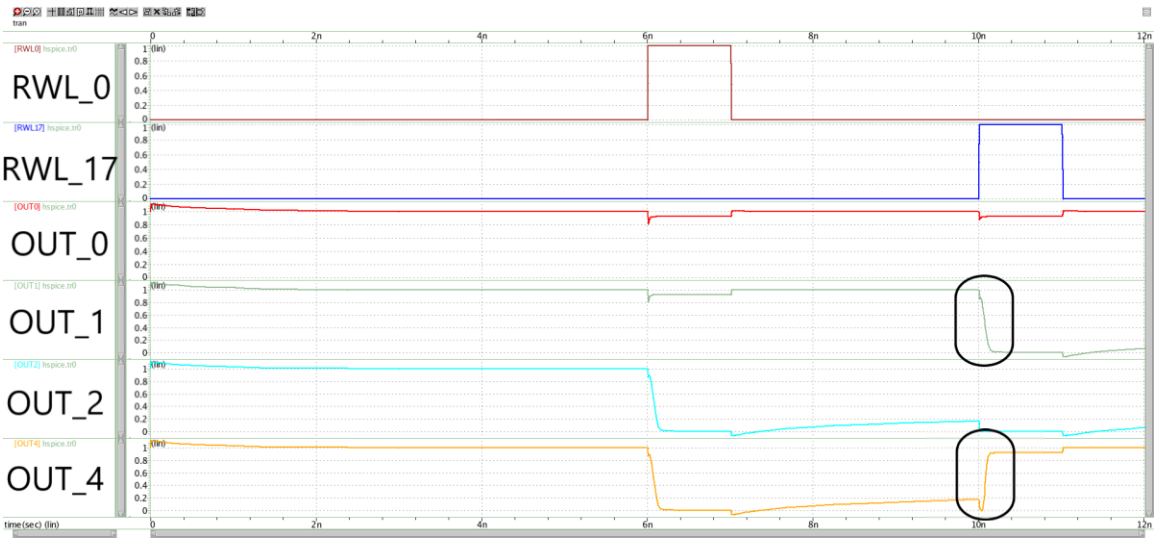

Figure 67 Variation of voltage on 'Rdout' lines of proposed 10T 32 Byte SRAM array

As seen from the *Figure 67*, the bit values 1 and 4 are different for 0^{th} word and 17^{th} word. When the 17^{th} word is read, the value on the 1^{st} and 4^{th} 'Rdout' bit-lines is changed from '1' to '0' and '0' to '1' respectively. The value remains pretty much the same for 0^{th} and 4^{th} bit-lines.

3.5 32 Byte Array Comparison

The comparisons of read speed, write speed and average power consumption of various 32-byte arrays are tabulated in Table 5. All four memory arrays are run according to the stimuli mentioned in *Figure 64*. The VDD is set at 1V and the simulations are run at 25˚C.

Cell	**Read(ps)**	**Write(ps)**	P_{avg}**(uW)**
6T	Precharge+78.7	38.3	13.0
8T	Precharge+84.4	19.6	17.2
10T	145.0	21.9	26.2
Proposed 10T	149.0	21.6	13.8

Table 5 Read speed, Write speed and Average Power consumption of different 32 Byte SRAM Arrays

As seen from *Table 5*, the conventional 6T has the best read speed (78.7ps) and best average power consumption (13.0uW) due to the absence of a separate read-out circuit. The proposed 10T design has the next best average power consumption at 13.8uW. The addition of inverter and transmission gate to existing 10T and tri-state inverter to proposed 10T affected the read speed when compared to 6T and 8T designs. The proposed 10T's read speed is comparable to existing 10T but the power consumed is a lot less because the inverter of existing 10T design keeps working all the time irrespective of the phase of

operation. Considering the poor noise margin of 6T and power consumptions of 8T and existing 10T designs, the proposed 10T design is a better design overall.

The results from the table may not mean the same in all cases. The pre-charge circuits have a couple of problems that associate with speed and power. For example, in case of the 6T cell, both bit-lines need to be pre-charged to VDD before the read operation. And during the read phase, one of those bit-lines will be discharged to GND. And for the next read operation, the bit-lines need to be charged to VDD again. This means that, there is a charge and discharge action for every read operation. This consumes a lot of power when compared to both the 10T cells where no pre-charge is required initially, and the output bit-line changes its value only when there is a change in the bit value read. In case of the 8T cell, the output bit-line is charged to VDD before the read operation and then during read, it either remains at VDD or discharges to GND based on the bit value. There is a 50% probability that the data bit is '0' in which case the output bit-line of 8T cell discharges. And after that, for the next read operation, it charges back to VDD. The power consumption even in this case is more than that of the 10T cells. The other problem with pre-charge is that it requires time to charge the bit-lines. Imagine a case where two words along the same column are to be read one after another. In case of 6T and 8T cells, after the first read operation, the output bit-lines need to be charged back to VDD before the next read operation. Whereas in case of the 10T cells, the second read operation can be initiated right after the first one without any delay. So, the 10T cells, or any cells in general that don't require pre-charge of output bit-lines, are power efficient and faster when compared to the cells that require the pre-charging of output bit-lines. This problem is explained in [30] where comparisons are done on cells requiring pre-charge and cells not

requiring a pre-charge for read operation. Some designs have been proposed [31], [32], [33], [8] with a goal to achieve low overall power by different methods but still having to pre-charge bit-lines for read operation. The designs [32] and [33] propose single-ended write which might reduce write speed but save power.

4. Conclusion and Future Work

4.1 Conclusion

Stability and power are considered the important specifications of an SRAM cell. The Static Noise Margins are measured from synthesis simulation for the conventional 6T, 8T, 10T cells. A 10T SRAM cell is proposed which has improved RSNM of 254mV at VDD of 1V when compared to that of 70.7mV for 6T cell. The SNM of proposed 10T cell is simulated under different supply voltages and temperatures. The RSNM of our proposed 10T cell under VDD of 0.6V, 0.8V and 1V is 147mV, 207.18mV and 254.5mV, respectively. And, RSNM at temperatures of 0˚C, 40˚C, 80˚C and 120˚C are 259.5mV, 252.4mV, 244.6mV and 237.5mV, respectively. The WSNM of the proposed cell is measured at pull-up ratios of 0.5, 1 and 1.5 to be 374mV, 312.5mV and 292mV, respectively. A 32-byte memory array is built for all the designs discussed including the proposed cell. The read and write times along with average power consumption are compared for all the designs. The read time, write time and average power of the 32-byte array of the proposed 10T array is 149ps, 21.6ps and 13.8uW, respectively. As discussed in the results *Section 3.5*, the proposed 10T design has the advantage of speed and power when compared to the 6T and 8T designs. Despite the advantages of a particular cell design, the ultimate choice of SRAM cell design is dependent on the type of application and its requirements.

4.2 Future Work

- Developing a layout of a large array of the proposed SRAM cell in the order of kB and MB
- Performing PVT variation and Monte Carlo Analysis on the layout of proposed SRAM cell
- Implementing an image processing application by using hybrid SRAM with the proposed SRAM cell on the MSB side

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