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A 13T Single-Ended Low Power SRAM Using Schmitt-Trigger and Write-Assist

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A 13T Single-Ended Low Power SRAM Using Schmitt-Trigger and Write-Assist

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By

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WRIGHT STATE UNIVERSITY

GRADUATE SCHOOL

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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Praneeth Namala ENTITLED "A 13T Single-Ended Low Power SRAM Using Schmitt-Trigger and Write-Assist" BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Electrical Engineering

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Abstract

Namala, Praneeth. M.S.E.E, Department of Electrical Engineering, Wright State University, 2017."A 13T Single-Ended Low Power SRAM Using Schmitt-Trigger and Write-Assist"

SRAMs are widely used in application based systems like medical instruments, portable electronic devices from caches to registers. Technology scaling of transistor into nanometer regime has substantially increased memory density that occupies large silicon area in today's IC's and consumes significant amount of active and leakage power. So, design requirements and challenges such as memory write and read speed, leakage power, noise margin and process-voltage-temperature (PVT) variations also significantly increase. In this thesis, a 13T single-ended low power SRAM using Schmitt-Trigger and write-assist technique is presented. It enhances read static noise margin, write-1 and read-0 access time, specifically at low supply voltages. Designed in 1.05V 32 nanometer CMOS process, employing a Schmitt-Trigger in SRAM design achieves a higher read static noise margin (RSNM) of 3.65x and 1.79x as that of the standard 6T and conventional 8T SRAM, respectively. The read port configuration used in this SRAM design reduces about 50% of the Read-Bit-Line (RBL) leakage from un-accessed memory cells as compared with conventional 8T SRAM. The SRAM functions successfully with a minimum V_{DD} of 340 mV, 100 mV lower than the threshold voltage so as to consume extremely low power.

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Acknowledgement

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Dedicated to

My Family

1. Introduction

1.1 Introduction to Memories:

Memories are an absolute necessity in modern digital systems and it occupies major area in System-on-Chip (SoC). Moreover, the density of memory rapidly increases as technology scaling continues advancing. It's leading to consume significant amount of leakage and dynamic power. The power necessity for battery operated devices, for instance, mobile phones and medical devices is more stringent. Therefore, leakage and dynamic power efficient designs need to be explored for longer operation of battery operated systems [1]. Lowering of the bit-lines switching (capacitance loading) and operating voltage reduces active and leakage power. Hence, the scaling of supply voltage has become primary concern to the low power application systems. However, circuit parameter sensitivity to the process, voltage, and temperature (PVT) variations increases with the V_{DD} scaling. The intra-die and inter-die process variations raises as technology scales down especially for SRAM bit cells. This additionally result in mismatch of threshold voltage between adjacent transistors. Moreover, the V_{DD} scaling and increased process variation potentially leads to memory failures such as read, write and hold failure [2]. Therefore, advanced design techniques to consume low power and improve the stability of memory are in critical stage.

1.2 Memory Arrays:

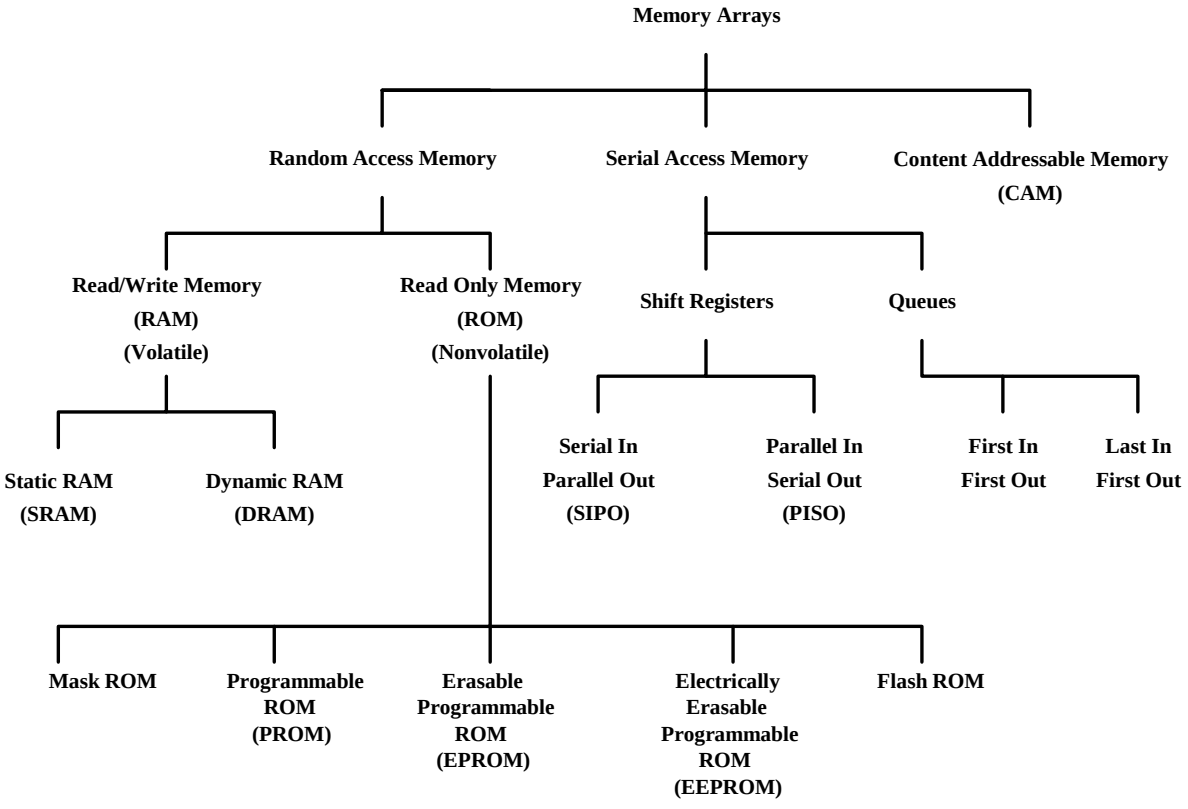

Fig. 1. Memory array design [3].

Memory arrays are divided into different categories as shown in Fig.1. On the basis of access patterns, the memory can be divided into random access memory and serial access memory. The random access memory is further classified as Read/Write memory and Read only Memory. It can access the data in random fashion. On the other hand, serial access memory gains access to the data in serial fashion and it's categorized as shift registers, queues. First-In-First-Out (FIFO) and Last-In-First-out (LIFO) are the examples for the Queues whereas Serial-In-Parallel-out (SIPO) and Parallel-In-Serial-Out (PISO) come under shift registers [4].
Read/Write memory perform both write and read operations which are divided into Static RAM (SRAM) and Dynamic RAM (DRAM). A Read-only memory can perform read operation and it cannot write the data as random access memories. ROM structures are nonvolatile memories whereas RAM structures are volatile. ROMs are further classified as Mask ROM, PROM, EPROM, EEPROM, and Flash ROM. The detail description of these memories is discussed in following sections.

1.2.1 Random Access Memory (RAM):

1.2.1.1 Static Random Access Memory (SRAM):

Static RAMs use a cross coupled pair of inverters store the data and it can retain the data as long as power is turned on. SRAM can perform both write and read operations by using access transistors. The standard 6T SRAM consists of six transistors, the data writing can be performed using the Word-Line (WL), Bit-line (BL) and Bit-line-bar (BLB). Row decoder and column decoder are used to control the word-lines and bit-lines in memory array. The operation of the standard 6T SRAM cell is discussed in chapter-2.SRAMs are mostly used in the application based systems like processors, electronic devices from caches to registers. It occupies large area over DRAM and offers high speed.

1.2.1.2 Dynamic Random Access Memory (DRAM):

DRAM cell utilizes capacitor to store one bit of data. Fig.1.1 depicts the schematic diagram of 3T DRAM.A noteworthy change in DRAM development has been the switch from three-transistor (3T) plans to one-transistor (IT) cell configuration, empowering generation of 4-to 16-Mb thickness DRAM that utilizations propelled 3-D trench capacitor and stacked capacitor cell structure [5]. The schematics of 1T and 2T DRAM is shown in Fig.1.2. DRAMs occupies less silicon area as compared with SRAMs. However, it offers less speed than the SRAM. The capacitor in DRAM cause leakage, so it should be refreshed periodically.

The bit-line (BL1) and WWL are used to perform write operation for the 3T DRAM. The capacitor stores the content based on the data at the BL1 after activating the WWL. As we know that NMOS passes degraded-1 so the capacitor can store the value as$V_{DD} - V_{thn}$. The information is held as charge on capacitance once WWL is activated low. The bit-line (BL2) need to be pre-charged before performing the read operation. When reading contents from the cell, the read-word-line (RWL) is activated high. Let us assume x=0, then it turns off the M2. Due to this, no discharging path exist from M3 to M2 so the bit-line (BL2) stays at high. The DRAMs read opposite value of the storage node, therefore it requires complementary sense amplifiers to validate the result.

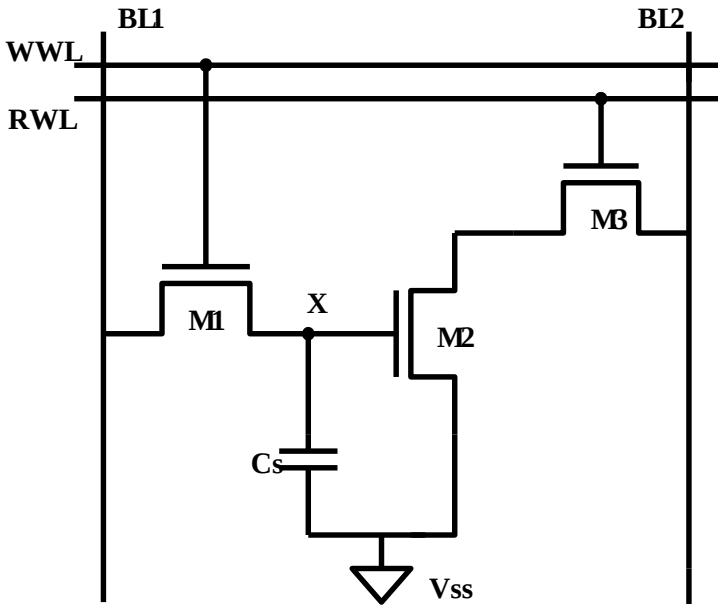

Fig. 1.1. Schematic of 3T DRAM [3].

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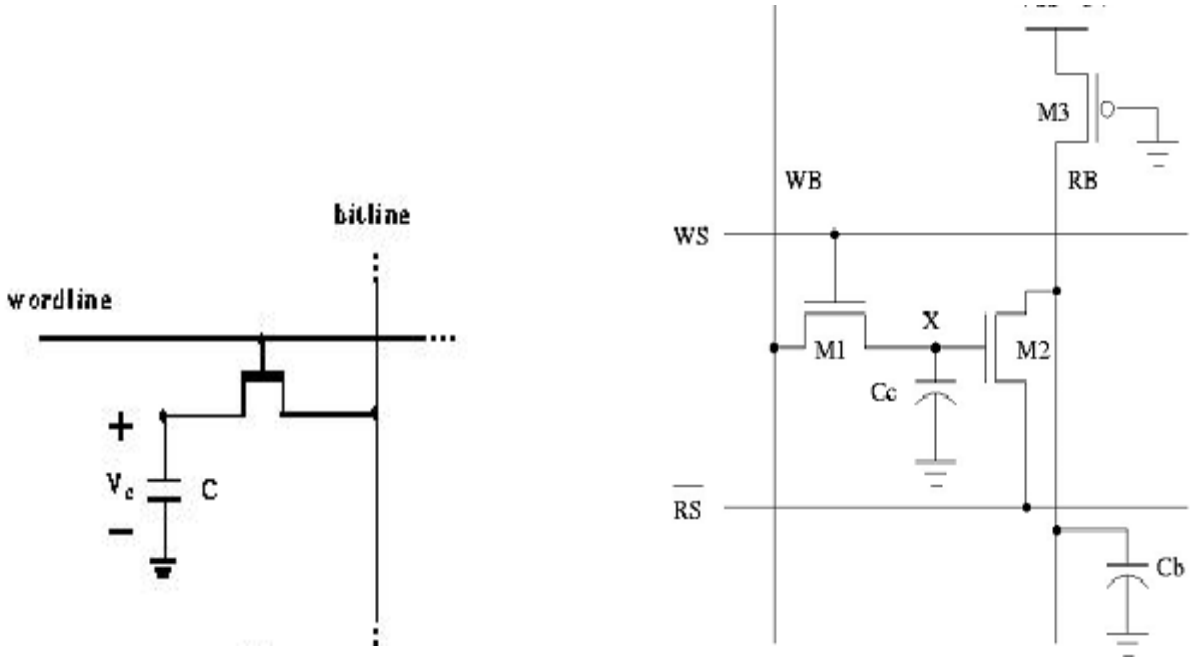


Fig. 1.2. Schematics of 1T and 2T DRAM.

1.2.2 Read-Only Memory:

ROMs are nonvolatile memory structure, it can retain the data without power. A ROM can uses single ended methodology and it can store the single data bit with one transistor. ROMs are used in many electronic devices such as computers and portable devices. There are different ways to implement ROMs, which are shown in below figure.

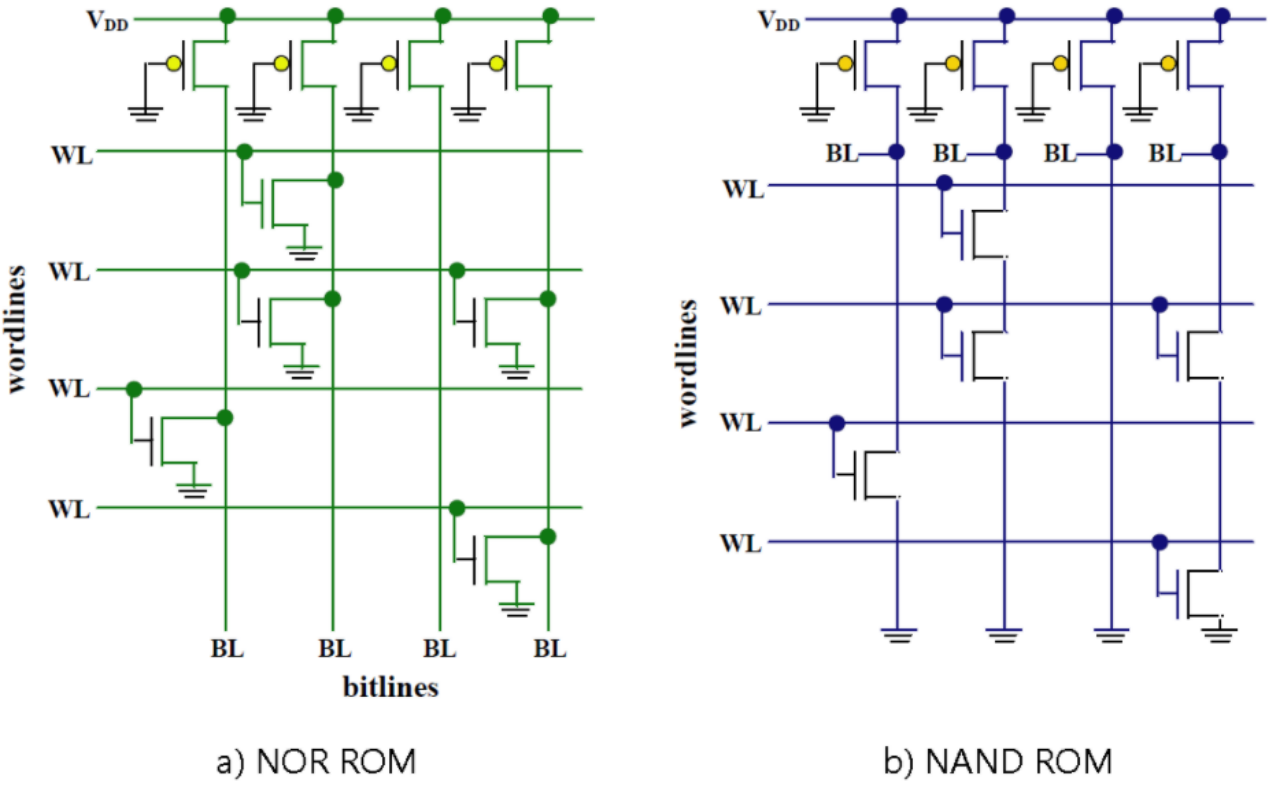


Fig. 1.3. NOR and NAND based ROM [6].

Fig. 1.3 (a) shows that the NOR based ROM design consists row based word-lines (WL), column based bit-lines (BL), and pre-charge transistors. Initially all the BLs are kept high using pre-charge transistor and the data is retrieved by managing the word-lines. To read the data, selected WL is activated high whereas remaining word-lines should be low. The transistor which is connected to the WL conducts and discharges the BL from high to low. So wherever there is a transistor a logic 0 is read; otherwise a logic 1 is read.

Fig. 1.3 (b) depicts that NAND based ROM structure. It looks like same as NOR ROM, the only difference is BL's are connected to pre-charged transistors to one end whereas the other end is connected to ground and in between transistors are placed. To read a word, all word-lines are pre-charged high except the selected word-line. In NOR ROM, selected word-line is activated high whereas in NAND ROM selected WL is activated low. The reading of the data in NAND ROM is opposite to the NOR ROM, if there is transistor it'll read 1 otherwise it'll read 0 [6].

1.2.2.1 Mask ROM:

Mask ROMs are a different type of ROMs it can provide high storage density. In Mask ROMs, the memory contents are determined by one of the mask technique. These ROMs are constructed with and without presence of transistor so as to reduce the amount capacitance on the word-lines and power consumption [7]. These read only memories are programmable according to the customer requirement.

1.2.2.2 Programmable ROM (PROM):

The main dissimilarity among Read only memory and Programmable ROM is programmed during manufacturing whereas PROM is produced as empty memory. The PROM programmer device is used to program the PROMs which are only one time programmable. This tool gives a high electrical current to particular cells in the ROM that viably blows a wire in them. This procedure of breaking the connection is called as burning the PROM [8].

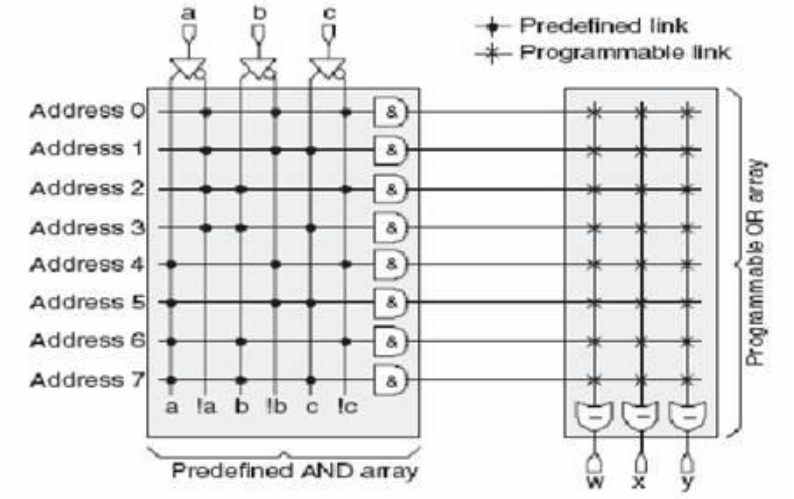


Fig. 1.4. PROM Design [6].

1.2.2.3 Erasable PROM (EPROM):

Erasable PROMs are a special type of memory it can erase the data by exposing to the strong ultraviolet light. It can reprogram the data but requires high voltage to write data into the memory. EPROMs are different from PROM. It can always erase data as well as reprogram data whereas PROMs are only one time programmable. EPROMs are mainly used in personal computers.

An EPROM utilizes a floating gate structure it stores data in each memory cell. This floating gate is inscribed in the dielectric layer which divides the external gate and silicon channel of the memory cell. Initially, all memory cells store the value 1 and due to the Erasable mechanism the data of the memory cell changes to 0. This happens by using memory cell censor, which decides the amount of charge stored in the floating gate and compares it with the threshold voltage. The higher charge changes the data to 0; otherwise, no change occurs[9].

1.2.2.4 Electrically Erasable PROM (EEPROM):

EEPROM is a user modifiable ROM. The contents of the memory can be erased as well as reprogrammed with the help of the electrical voltage. EEPROM is similar to EPROM; however, EEPROM does not require to take out the chip from the computer when it's reprogramming. The writing or reading of an EEPROM is much slower than the ROMs as well as RAMs. Usually, EEPROMs supports only for single byte operations. However, modern EEPROMs can support for the multi-byte operations. The main disadvantage of EEPROM is that data cannot be rewritten selectively. To make any changes in EEPROM, the entire chip must be erased and rewritten to update the contents. The life time to reprogram the EEPROM is limited to hundreds or thousand times[10].

1.2.2.5 Flash ROM:

Flash ROM is a modern type of EEPROM that can retain the data without requiring any power. It can be erased and reprogrammed same as EPROM but with higher speed. The flash memory replaces the data in block level whereas EEPROM replaces the data in byte level. Therefore, flash memories are extremely applicable to large amount of data updates. Flash ROMs utilizes floating gate structure to store data in memory cells, and changes gate voltage to erase the contents. Flash ROMs can be rewritten.

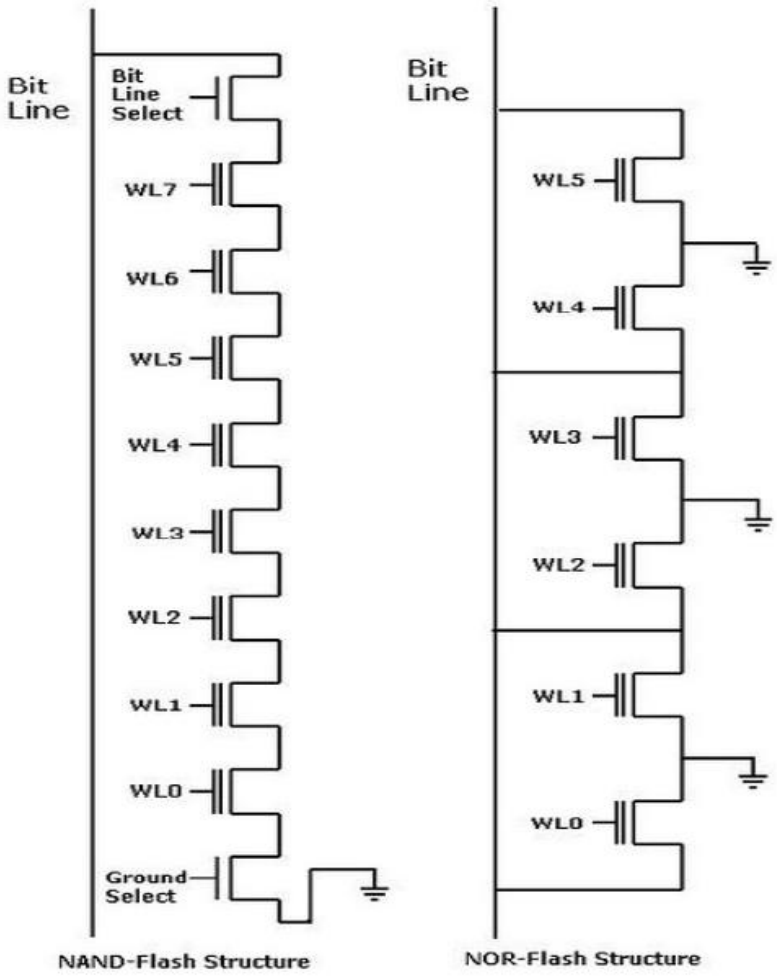


Fig. 1.5. NAND and NOR flash structures [6].

Flash ROMs are classified as NAND based flash memory and NOR based flash memory. NAND based flash structure minimizes the bit cell size and cost [6]. NAND flash memory performs both write and read operations at high rate. It can write one page data and erase the contents of one block at a time. NAND flash ROM is widely used in USB flash drives, cameras and audio players. NOR flash memory is slower than the NAND memories. It can write and erase the data in byte level. NOR based flash memory is often used in cell phones to store the operating system [11].

1.2.3 Serial Access Memory:

Serial access memory can access the data in serial fashion and it's categorized as Shift Registers, and Queues.

1.2.3.1 Shift Registers:

Shift registers are used to store the bits of data by connecting each flip-flop output to its next flip-flop input. In general, shift registers are exist in four types which are Serial-In-Parallel-Out (SIPO), Parallel-In-Serial-Out (PISO), Serial-In-Serial-Out (SISO), and Parallel-In-Parallel-Out (PIPO). SIPO and PISO are discussed.

Serial-In-Parallel-Out (SIPO):

A 4-bit shift register is shown in Fig.1.6. It consists of four flip-flops, which are connected in a chain controlled by a common clock. The data is entered in serially and it provides parallel outputs.

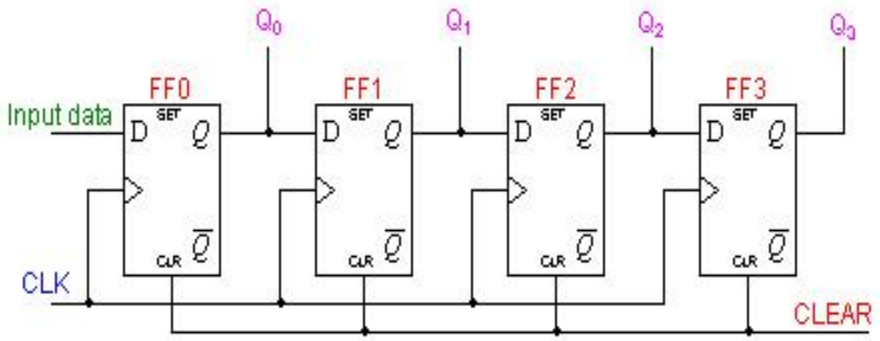


Fig. 1.6. Serial-In-Parallel-Out Shift Register.

Parallel-In-Serial-Out (PISO):

The below figure shows that the 4-bit parallel-in-serial-out shift register. It consists four flip-flops as well as mode control signal. Enabling of mode signal gives the successful shifting of the parallel data and produces the output in serial manner.

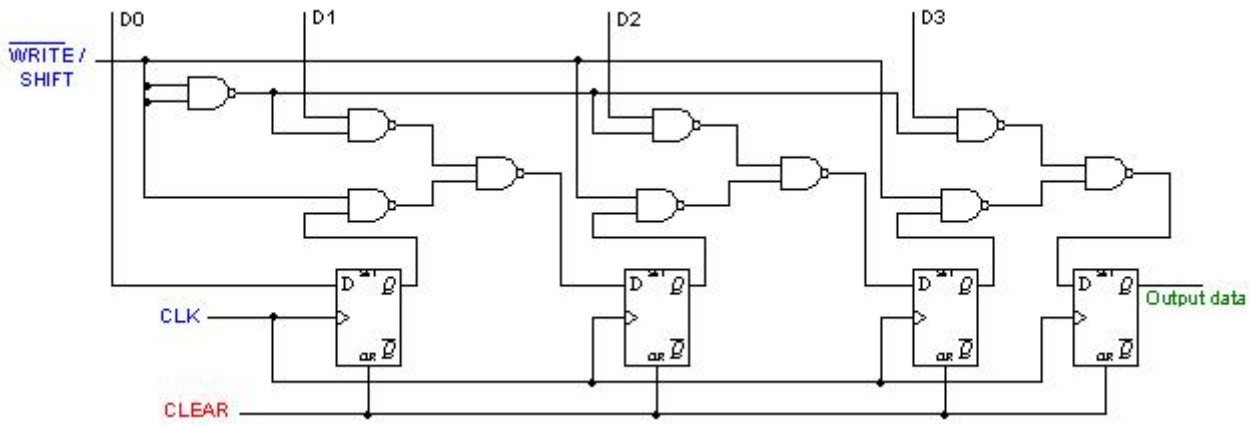


Fig. 1.7. Parallel-In-Serial-Out shift Register.

1.2.3.2 Queues:

Queues can perform both write and read operations. If there is no space to write the contents then the queue asserts a full flag as well as if there is no data to read empty flag asserted [7].

First-In-First-Out (FIFO):

In the beginning of operation, both read and write pointers are initialized to the first memory location. When write pointer increments then it's pointed to the next location in the queue. When the write pointer reaches the read pointer then the FIFO is full. The same concept is applied to read operation. In read mode, the read point is pointed to next location in the queue. When the read pointer reaches write pointer then the FIFO is empty [7].

Last-In-First-Out (LIFO):

While writing the pointer increments and when it achieves the last component the LIFO is full. While reading, the pointer decrements and when it gets to the first component the LIFO is empty[7].

1.2.4 Content Addressable Memory (CAM):

CAMs are a unique kind of memory it is composed of SRAM cells. The NOR based CAM architecture is shown in Fig.1.8. There are two kinds of CAM memories, which are binary and ternary CAM. Binary CAM can read, write and search the binary values 1 and 0 whereas Ternary CAMs perform the same function as the binary CAM, including supporting the don't care(X) value. In CAM designs, match signal is used to search the contents of the cells. The figure shown below consists of four horizontal word lines. The cells which are shown in the circuit consists both storage and comparison circuit. The horizontal word lines are connected to the match signal, initially all match signals are kept high. If there is any match occurs then the match signal activates otherwise it deactivates. The highlighted match signals are in figure indicating that the data is matched whereas other match signals are discharged to ground, indicating a mismatch. Finally, the encoder is used in this design to produce the address of the matched data [12].

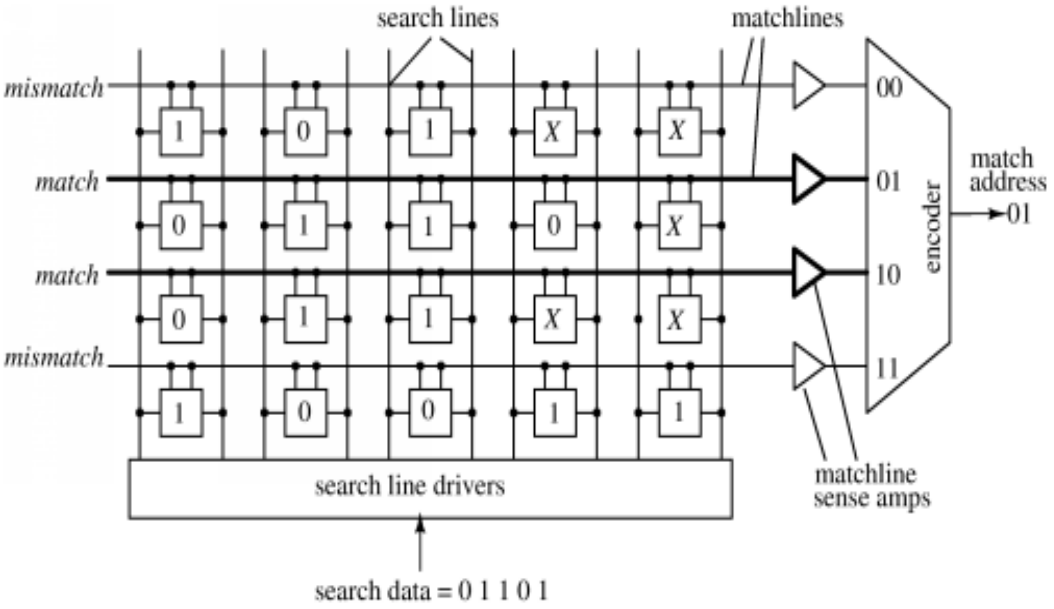


Fig. 1.8. NOR based CAM architecture.

1.3 SRAM Array Architecture:

Fig.1.9 shows SRAM array architecture. It mainly comprises of SRAM memory cells, row decoder, column decoder, input and output data control unit, and sense amplifier.

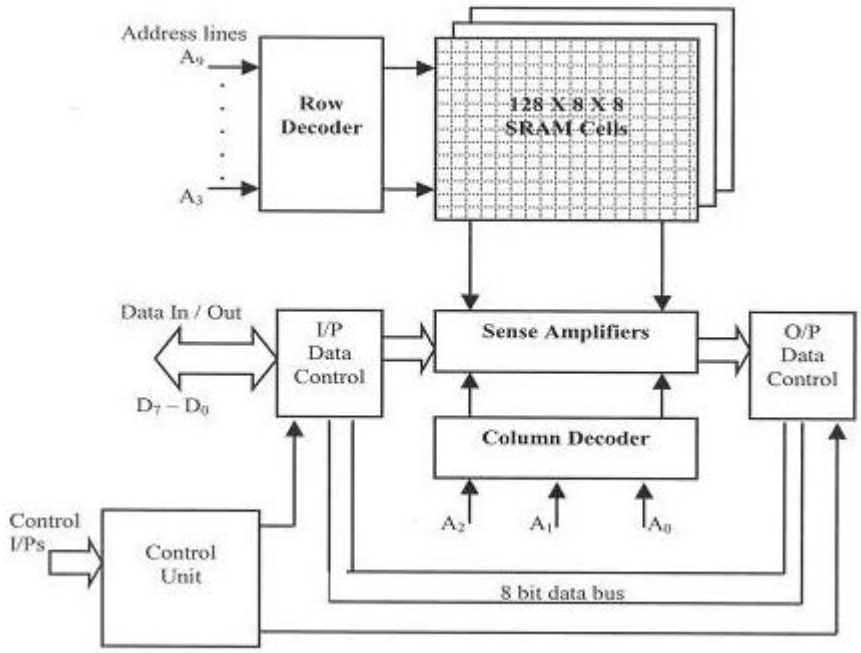


Fig. 1.9. SRAM Array Architecture.

As we discussed earlier, SRAM contains six transistors including word-line (WL),bit-lines (BL and BLB). The row decoder and column decoder are constructed using logic gates, which are employed in the

architecture to select particular WL and BL to perform the read/write operation. The WL is row based whereas bit-lines are column based. The row-decoder selects one word-line out of all and the column decoder selects one bit-line. The data is driven by controlling the input data control unit through data pin.

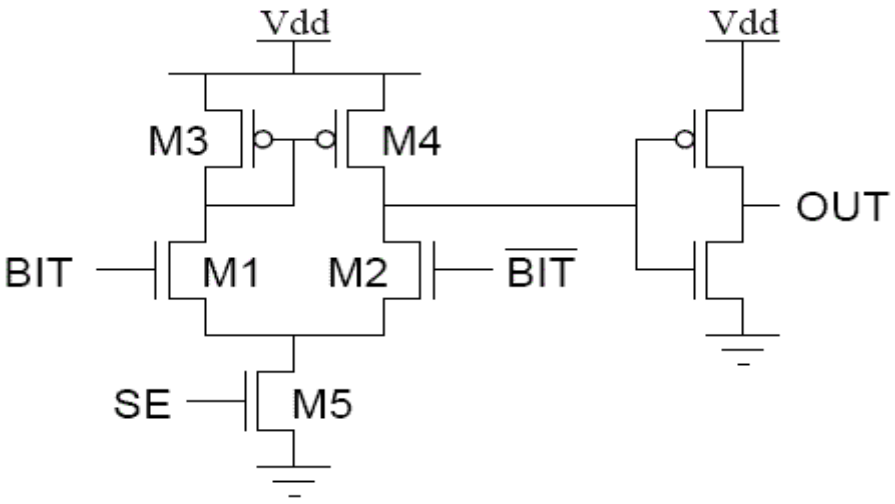


Fig. 1.10. Differential Sense Amplifier.

During read mode, the BLs are pre-charged to high, it can be done by the pre-charge circuit. When word-line (WL) turns on, the data at the output nodes determines the voltage level on bit-lines. The 0 storing node discharges the bit line through the pull-down transistor and access transistor. To read the data in memory array architecture, the sense amplifier which is shown in Fig.1.10 is used for differential topology SRAM cells. It can sense and amplify the BLs voltage level. The read access time is reduced by employing the sense amplifier.

2. Conventional 6T SRAM Cell

Fig.2 shows the schematic diagram of conventional 6T SRAM cell. It mainly comprises of a back-to-back connected pair of inverters and two access transistors (M1 and M2). It stores complementary values such as 0 and 1. Row-based word-line (WL) controls the access transistors whereas drains are attached to column based bit-line (BL) and bit-line-bar (BLB). The access transistors (M1 and M2), word and bit lines are used to perform write and read operations. By setting the data value on the bit-line decides whether output nodes to store 0 or 1, generally write driver circuit is used to set the bit–line voltages. The WL is set to low in data retention mode it can turn off the M1 and M2. In this condition the inverters are in complementary state. The write and read operations of the conventional 6T cell are illustrated in following sections.

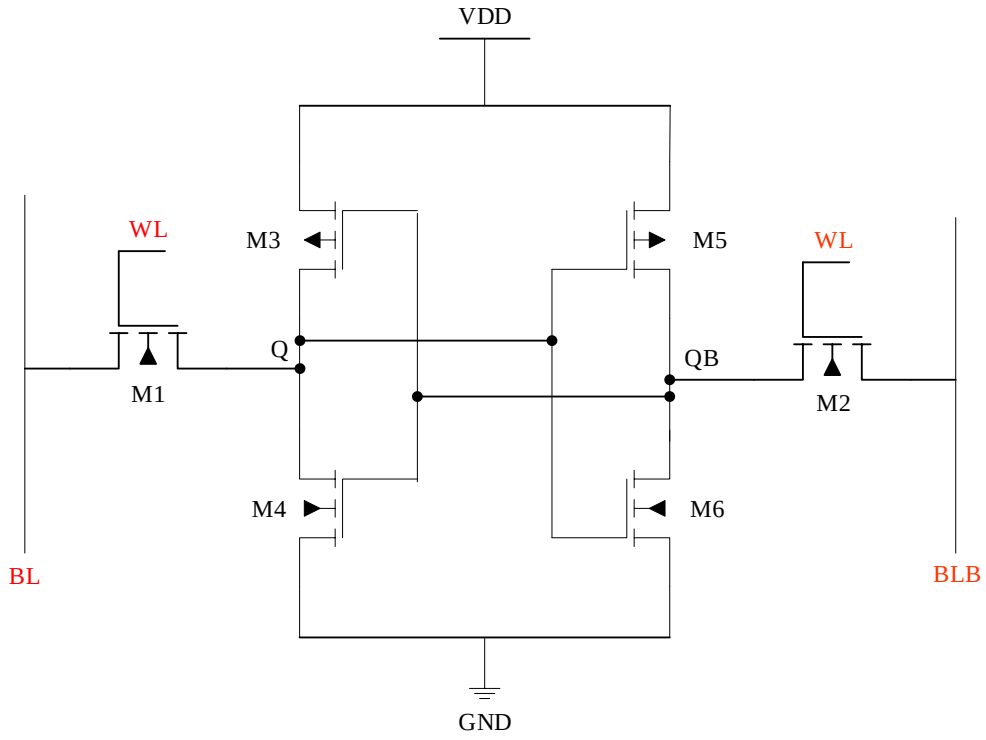


Fig. 2. Schematic of 6T SRAM cell.

2.1 Write-Operation:

The contents in the memory cell is written using write driver circuit as shown in Fig.2.1, which comprises of two stacked nMOS pair and inverter. Write enable signal is utilized to set the data on the bit-lines. Assume Q and QB initially store the values 0 and 1. If we wish to write 1 into the cell, bit-line (BL) should be pre-charged high and bit-line-bar (BLB) is kept low by controlling the write enable signal and data pin in write-driver circuit. In write mode word-line (WL) should be enabled and the data at the output node QB discharges through the access transistor (M2) and held at 0. The back-to-back connected inverter pair pull up transistor M3 is turned on so Q is pulled up to high. During write operation, data contention occurs among the access transistors (M1 and M2) and

pull up transistors (M3 and M5). To achieve successful write operation, pull up ratio(PR=W1/W3) is equal or greater than 1. Transient waveforms for successful operation is shown in Fig.2.2.

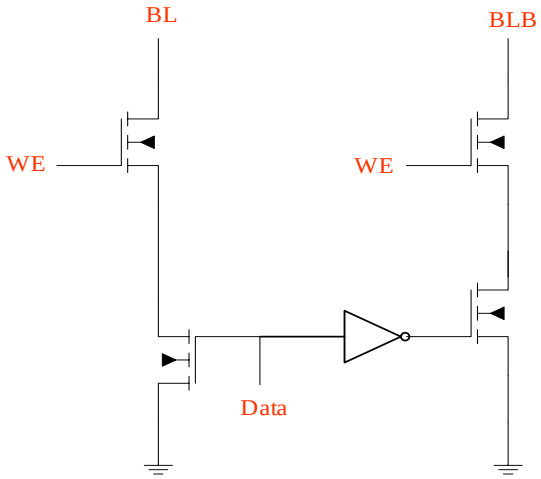


Fig. 2.1. Write-driver circuit.

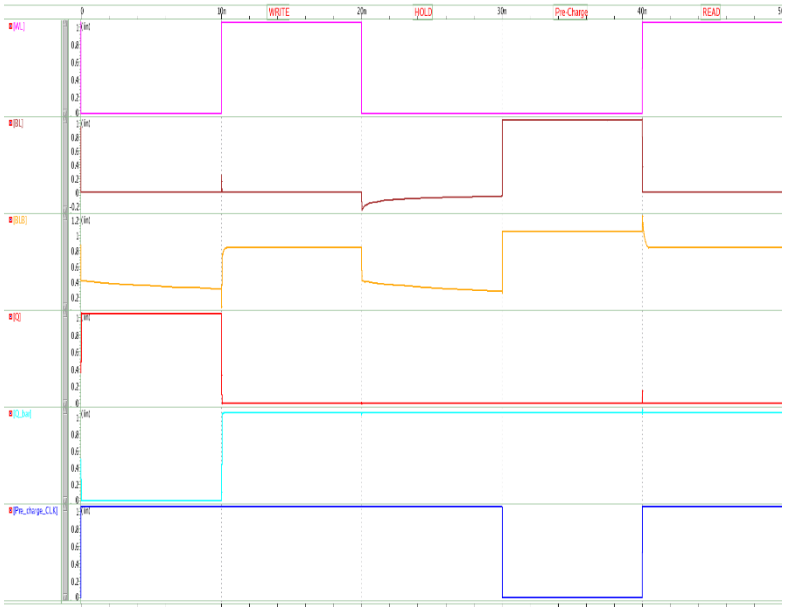


Fig. 2.2. Transient waveforms of 6T Cell.

2.2 Read-Operation:

Let us assume Q is initially set to 0 and QB is set to 1. The word-line disabled, bit-line (BL) and bit-line-bar (BLB)are pre-charged to high before performing read operation. A pre-charged circuit is shown in Fig.2.3. The bit-line (BL) voltage is discharged through the access transistor (M1) and pull down transistor (M4) after activating the word-line (WL) to high. At the same time, the output node Q is pulled up due to the current flowing through access transistor (M1), as shown in Fig.2.2. To make a successful read from the cell without flipping the contents of the cell, the pull down transistor must be strong enough than the access transistor.

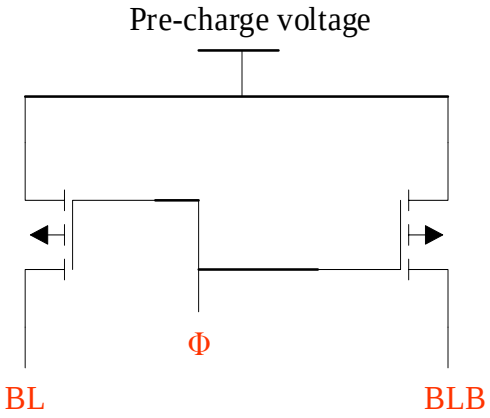


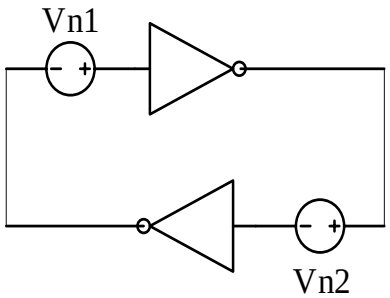
Fig. 2.3. Pre-charge Circuit.

2.3 Stability of 6T SRAM cell:

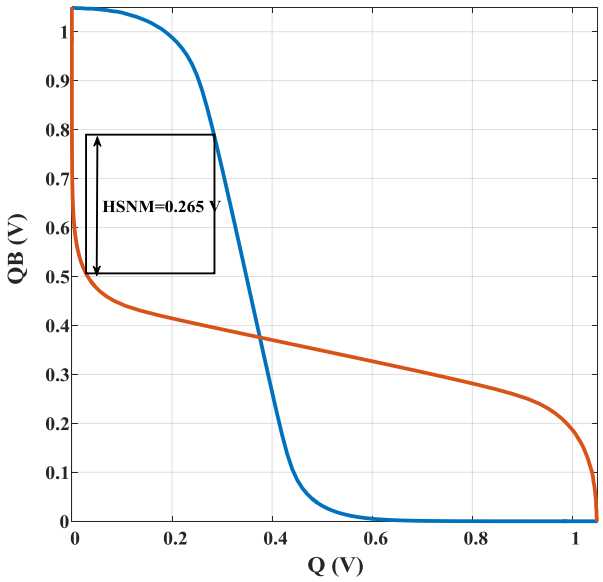
Cell stability is essential in memory cells. The transistor sizes play an important role in the stability of the conventional 6T SRAM cell. The nMOS pull down transistors (M4 and M6) must be strong enough whereas access transistors with intermediate size and pull up transistors must be weak [6]. Static Noise Margin (SNM) of the cell quantify the SRAM bit-cell stability during the write, read cycle and in standby mode. The SNM is described as the maximum amount of DC noise (V_n) that can be tolerated by the cross-coupled inverter pair such that the bit-cell holds its information (data) [13].

2.3.1 Hold Static Noise Margin (HSNM):

Hold static noise margin (HSNM) decides the SRAM cell stability in data retention mode. The method which is followed to find out HSNM is butterfly curve technique suggested in [13]. In this technique, a noise source V_n is applied to the output node voltages Q and QB. Fig.2.4. illustrates the test circuit and butterfly curves for 6T cell.



(a)



(b)

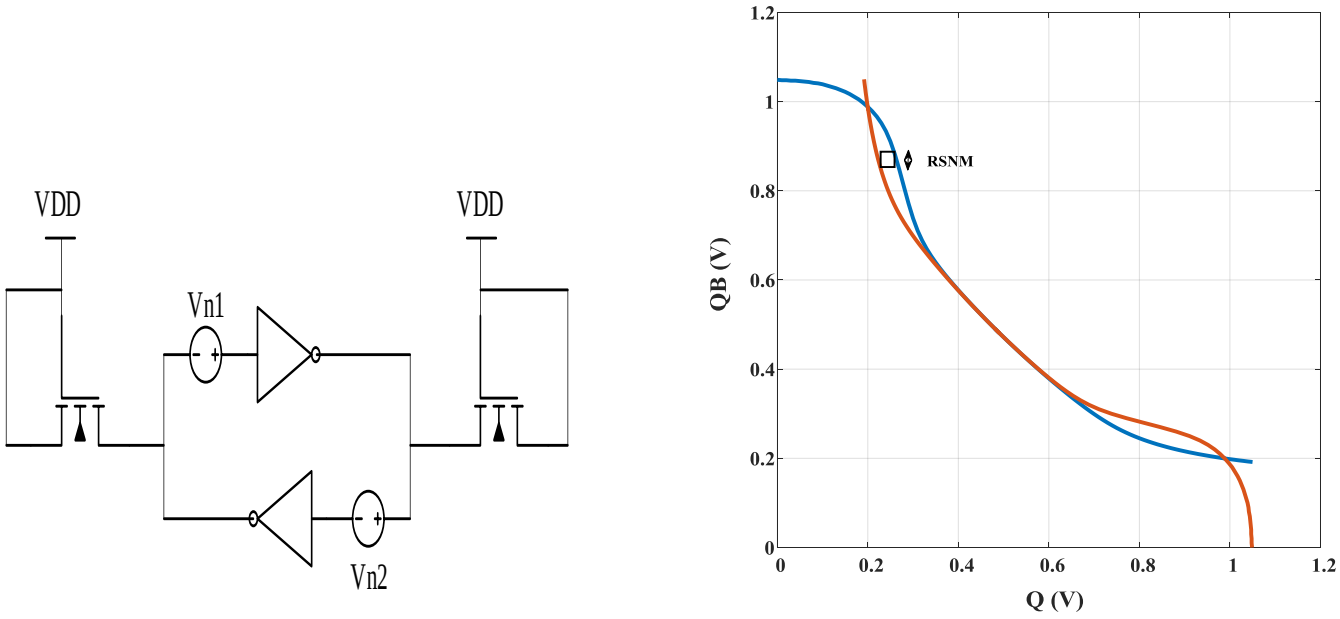
Fig. 2.4. (a) HSNM test circuit and (b) Butterfly curves for 6T SRAM Cell.

The access transistors are off to isolate the cell from BLs. The butterfly curves are plotted using 32nm CMOS technology. The 6T SRAM provides symmetrical butterfly curves in which the maximal square that can be implanted between the curves decides the HSNM of the SRAM bit cell. The conventional 6T SRAM cell achieves 0.265 V of HSNM at the supply voltage of 1.05V.

2.3.2 Read-Static Noise Margin (RSNM):

Read static noise margin (RSNM) for the 6T cell is measured using butterfly curves method as discussed earlier. Fig. 2.5 illustrates both circuit diagram and butterfly curves in read mode. To plot curves, bit-lines and word-line are tied to V_{DD} and swept the output nodes Q and QB to high. The read margin depends on the cell ratio and it's interpreted as the ratio of pull down transistor to the access transistor. The higher cell ratio of 6T cell gives higher read margin. However, it takes larger silicon area to build wider pull down transistors and reduces the number of bits per unit area.

$$Cell\ Ratio\ (CR) = \frac{W_4}{W_1} = \frac{W_6}{W_2}$$



(a) **(b)**

Fig. 2.5. (a) RSNM test circuit and (b) Butter fly curves in Read mode.

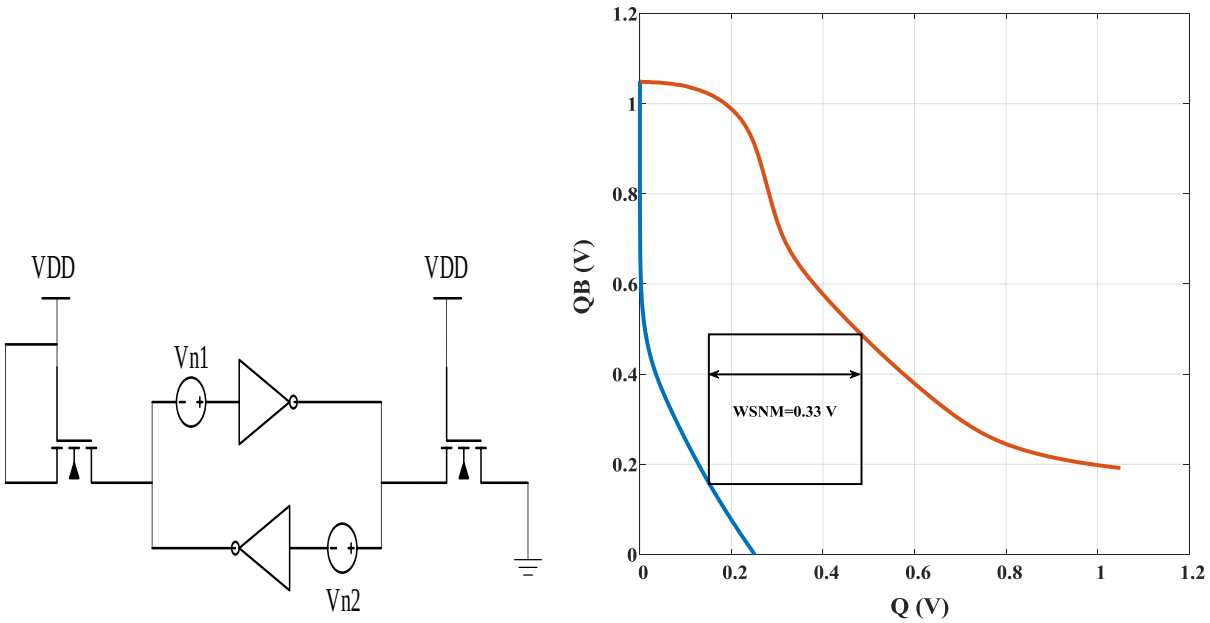
The conventional 6T SRAM cell provides extremely low read static noise margin (RSNM) as 0.07 V with CR=1 and 0.13V with CR=2 at the operating voltage of 1.05 V. Low read static noise margin leads to Q and QB flip at a lower supply voltages.

2.3.3 Write Static Noise Margin (WSNM):

The Write static noise margin (WSNM) determines the write ability of SRAM bit cell. Several methods have been presented to measure write static noise margin of the bit-cell such as butterfly curve method, Bit-line method, Word-line technique, and N-curve method [14] that are described in following sections.

2.3.3.1 Butterfly curve method:

In this technique, both bit-line (BL) and bit-line-bar (BLB) are tied to V_{DD} and 0. Word-line (WL) is set to high and butter fly curves are plotted by sweeping the node voltages Q and QB from low to high. Fig.2.6. depicts write static noise margin butter fly curves and the test circuit for 6T cell. The width of the square that can be implanted among the curves decides the write noise margin. The conventional 6T SRAM cell accomplishes 0.33 V of WSNM at the operating voltage of 1.05 V using the butterfly curve method.



(a) **(b)**

Fig. 2.6. (a) WSNM test circuit and (b) WSNM butter fly curves for 6T cell.

2.3.3.2 Bit-line method:

The bit line voltage can also be used to measure the write static noise margin [12]. In this method, bit-line (BL) and word-line (WL) are tied to V_{DD} and bit-line-bar (BLB) is swept from high to low. The bit-line-bar (BLB) voltage at which both output nodes Q and QB flips is defined as the write static noise margin of the cell. Fig.2.7 displays the test circuit for bit-line method.

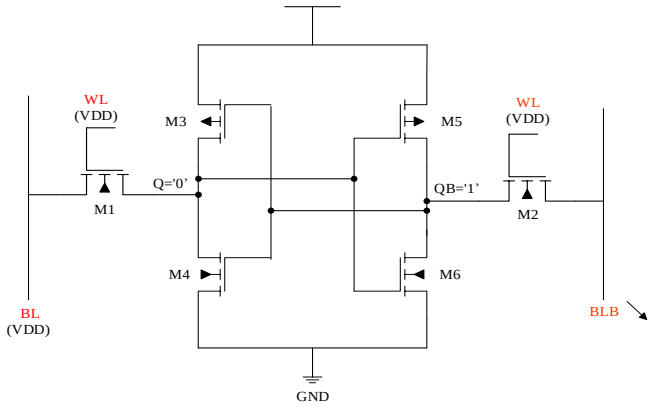


Fig. 2.7. Test circuit for bit-line method.

2.3.3.3 Word-line method:

In the word-line method, data is set on the BLs. The word-line is swept from 0to V_{DD}. The subtraction ofV_{DD} and word-line (WL) voltage at which the nodes Q and QB flips is called as write margin [14]. The test circuit and measurement are shown in Fig. 2.8.

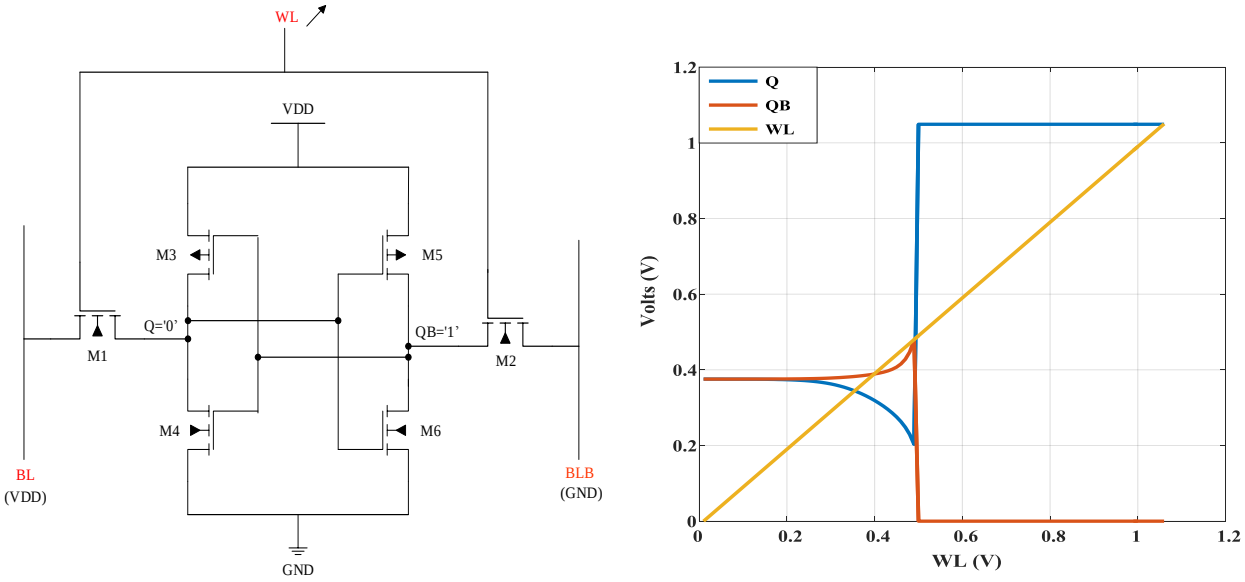


Fig. 2.8. Test circuit and write trip point for word-line method.

As discussed earlier, SRAM's occupies less area as compared with registers and gives better performance at higher technology nodes and threshold voltages. However, SRAM's functioning at lower technology nodes and threshold voltages have already faces challenges in present nanometer CMOS technologies. In the sub-threshold regime, the write and read stability of SRAM is degraded with increased global and local process variations at lower supply voltages. The storage node of conventional 6T SRAM cell raises while performing read operation, which may lead to read/write disturb problem. The major challenging in present nanometer technology is low power memory cell design. Scaling down supply voltages (V_{DD}) can minimize the amount of dynamic power. However, the threshold voltage variations increased to a large extent due to the scaled downV_{DD}. 6T SRAM cell still suffers from half select disturb, read disturb and read/write conflicting requirements at low supply voltages.

3. Past Work of SRAM Cell

Several SRAM bit cell configurations have been proposed herein, a few of them are discussed. A single ended6T SRAM cell was proposed in [15], which has a transmission gate at one side in place of single access transistor. Both write and read operations are conducted through the single transmission gate. This design reduces the bit-line switching. However, performing write and read operations through a single transmission gate increases the read disturb problem and also employing a transmission gate in read path reduce the stability of read operation.

A single ended 7T SRAM cell using a separate decoupled read port arrangement to avoid read disturb problem was proposed by Tawfik and Suzuki in [16-17]. However, the single ended designs suffers from write access time. It needs write assist circuits to minimize write-1 access time. Another single ended 7T SRAM cell was proposed by Takeda et al [18]. It comprises of an extra NMOS in pull down network of left inverter. This extra NMOS in pull down path helps to read disturb free operation. A 7T dual threshold voltage (Vth) SRAM bit cell was proposed in [19], which suffers from fabrication complexity.

Single ended 8T SRAM cell [20-24] utilizes a separate decoupled read buffer in read path similar to the single ended 7T SRAM. It performs differential mode write operation by using two write bit-lines as well as single ended mode read operation by using single RBL. In read mode, the storage nodes were decoupled from write bit-lines to eliminate read disturb as well as to improve the read static noise margin. However, read buffer used in this design still suffers leakage of read bit-line from un-accessed cells. Another single ended 8T SRAM using virtual ground technique is proposed in [25]. It utilizes separate read port configuration and reduces the read disturb problem.

Single ended 9T cell [26-27] separating read port configuration was used to decouple from write path like thye single ended 8T SRAM cell. It contains three stacked transistors in read path to decrease the amount of leakage power. However, this design takes more time to discharge the read bit-line but in turn increases the read access time. The single ended 8T and 9T cells are similar except read port circuit. A differential 9T SRAM cell was proposed by Liu and Kursun in [28] to remedy read disturb problem. This design performs both write and read operations comparable to the 6T SRAM cell. However, the two extra transistors attached to BLscause extra read access time. A different single ended 9T cell using FinFET technology was proposed in [29]. It employs regular back-to-back connected inverter pair to store data as that of traditional 6T cell and separate read port topology to minimize read disturb problem. Read port configuration used in this design reduces the read bit-line leakage from un-accessed memory cells.

Single ended and differential 10T SRAM cell were proposed in [30-33]. A single ended 10T cell utilizes decoupled read port design from write path. The separate read port design with four transistors used to manage the RBL leakage. A differential 10T bit-cell was proposed by Chang [33] with reduced read disturb difficulty. It employing two series adding of NMOS transistors in write path, which increases write access time and degrades the write ability of the cell. To improvewrite operation it needs write assist techniques like word line boosting. Another differential mode 10T cell was proposed with differential read buffer design to overcome read disturb problem [32].

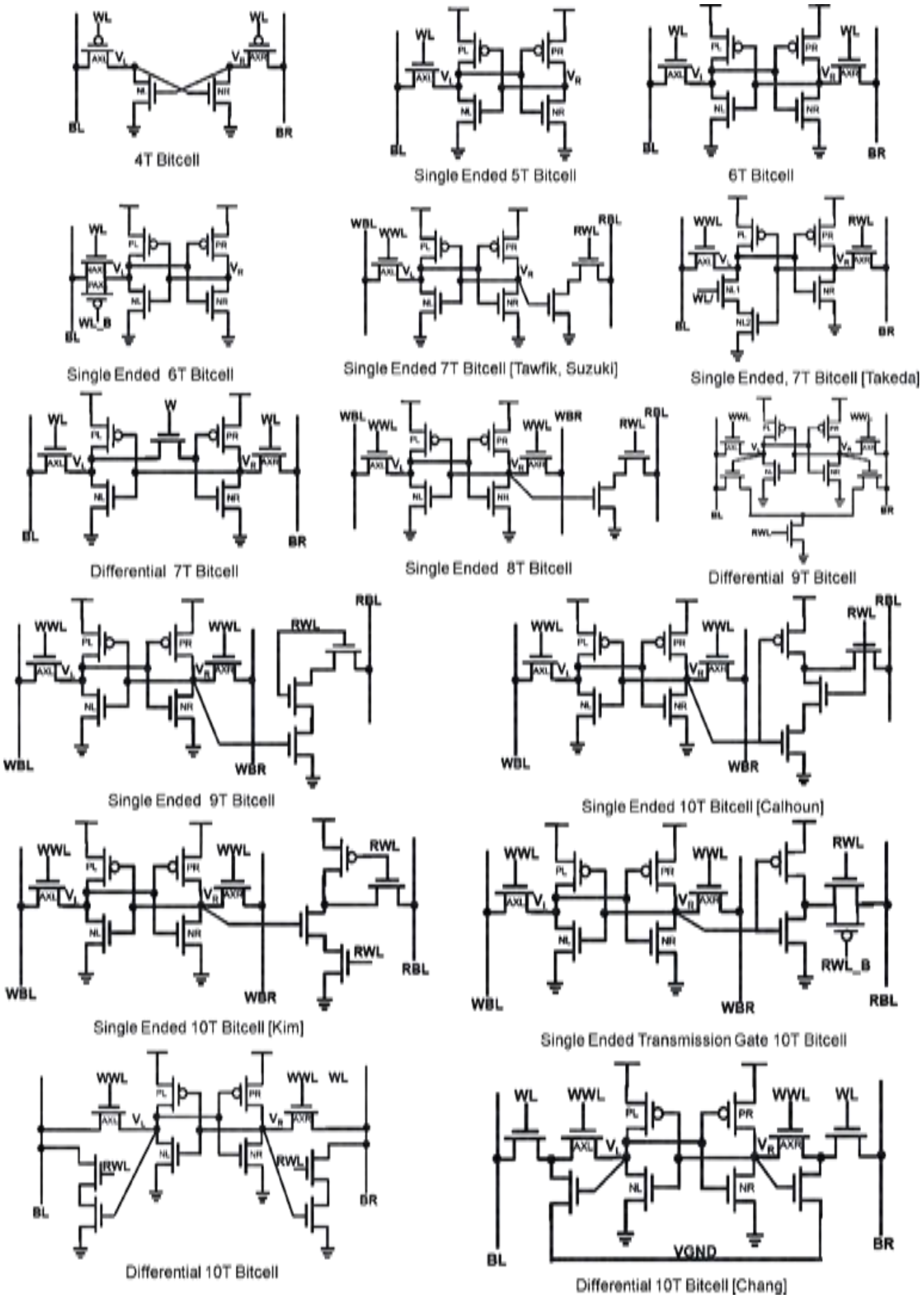


Fig. 3. Previous SRAM bit cells [15-33].

The above discussed SRAM cells utilizes cross coupled CMOS inverter pair for data storage. As we discussed earlier, the stability of inverter pair of SRAM cell is degraded with process, voltage and temperature (PVT) variations, specifically at low supply voltages. So, it requires a different approach to enhance the stability of SRAM cell at PVT variations [34]. Therefore, a Schmitt Trigger inverter was employed to improve the stability of inverter at lower technologies.

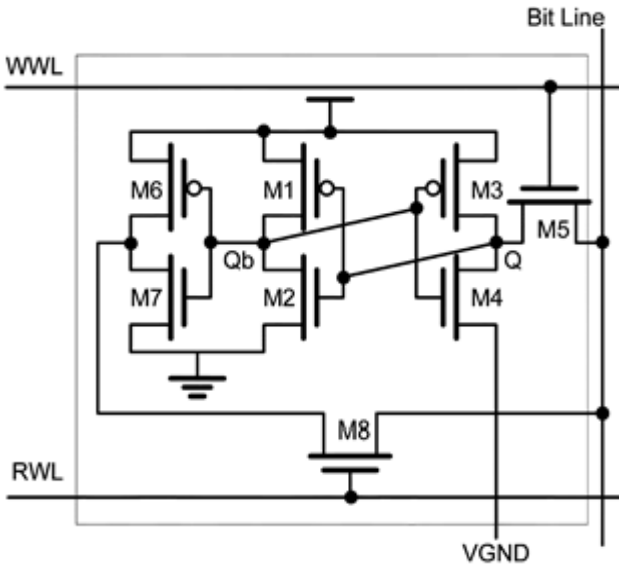
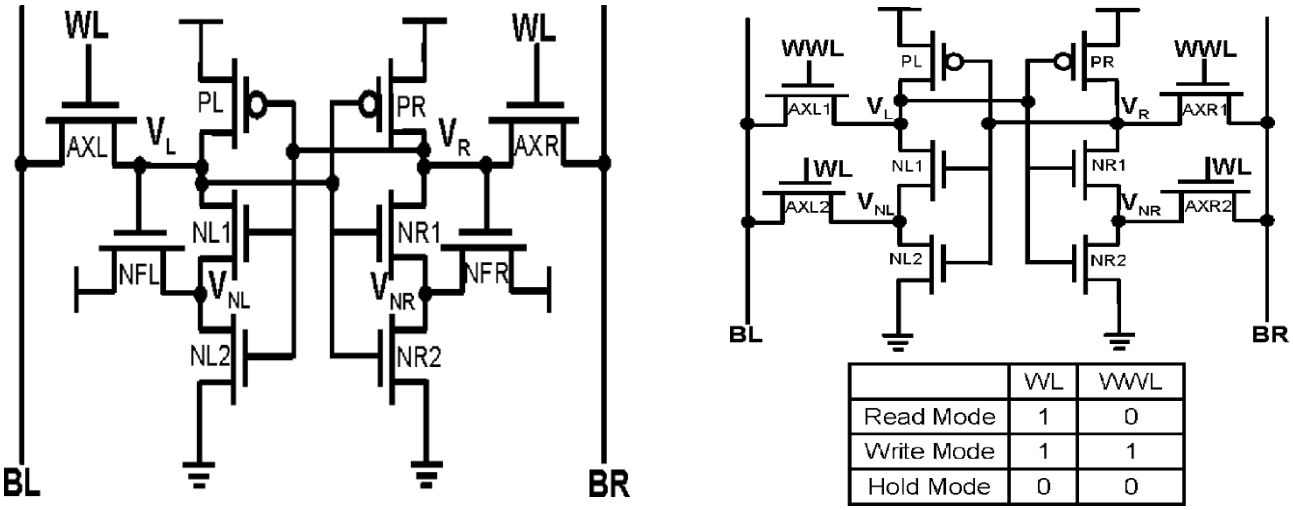


Fig. 3.1. Single Ended 8T SRAM using VGND write assist [25].



	WL	WWL
Read Mode	1	0
Write Mode	1	1
Hold Mode	0	0

Fig. 3.2. (a) ST-1 bit cell [2] and (b) St-2 bit cell [35].

Several Schmitt trigger based SRAM cells were proposed to increase the stability of SRAM at lower supply voltages with PVT variations. A differential 10T Schmitt trigger based SRAM bit cell (hereafter referred as ST-1) was proposed by Kulkarni [2] with improved read static noise margin (RSNM) over traditional 6T SRAM cell. However, this design still facing a problem of write read clash as that of 6T cell. As we know that 6T SRAM cell has a read destructive problem that 0 storing node rises above the ground voltage during read operation and the same problem also occurs in this 10T ST based SRAM cell. A 10T Schmitt trigger based

differential cell (hereafter referred as ST-2) [35] was proposed with a feedback mechanism. This design settles the read destructive problem of ST-1. However, this design includes two transistors connected to bit-lines, which increases the BL capacitance load and in turn reduces the speed of read operation.

Single ended Schmitt trigger based 11T SRAM (hereafter referred as ST11T) was proposed in [36]. The single ended designs points to consume low power due to lower bit line switching as discussed earlier. This design includes decoupled read port configuration, which reduces the read disturb problem and improves read static noise margin. Also, this design consumes less dynamic and leakage power compared to ST-1 and ST-2. However, this design still suffers from high write-1 access time at lower supply voltages. The read buffer same as that of conventional 8T cell is used in this design. It still suffers from higher read bit-line leakage, which may cause read-1 voltage sensing error at low supply voltages.

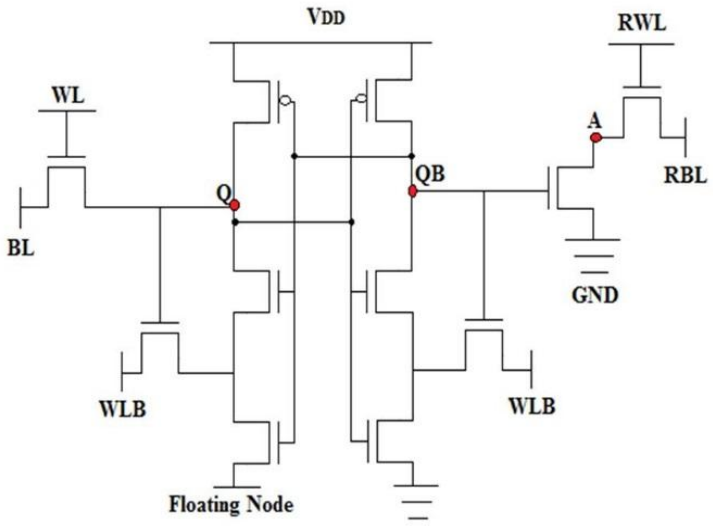


Fig. 3.3. Single Ended 11T Schmitt-trigger based SRAM [37].

4. Proposed 13T Schmitt-Trigger SRAM Cell

4.1 Single Ended SRAM Challenges:

Single ended SRAM topologies are key concept to improve the density of memory and to reduce the power consumption over differential SRAM topologies [1].Single ended SRAM cells minimizes the bit-line switching by half in comparison with the standard differential memory cell. The minimum bit-line switching reduces the capacitance load on the bit-line and in turn decreases dynamic power consumption. Also, single ended SRAM cell utilizes different path for both write and read and exhibits read decoupling. It also improves the read stability, mainly at lower supply voltages. In contrast to all these advantages, the major limitation of single ended SRAM cell is writing-1 into the cell through a single NMOS pass transistor. It increases write-1 access time and also degrades write-1 static noise margin at lower supply voltages. To overcome these there are several write assist techniques were employed. They are asymmetrical write/read assist [25], 7T dual threshold voltage (VTH) [19], boosted supply (access transistor gate voltage is greater thanV_{DD}), and gated feedback write assist [38].

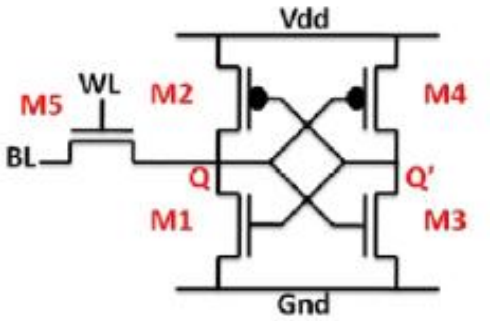
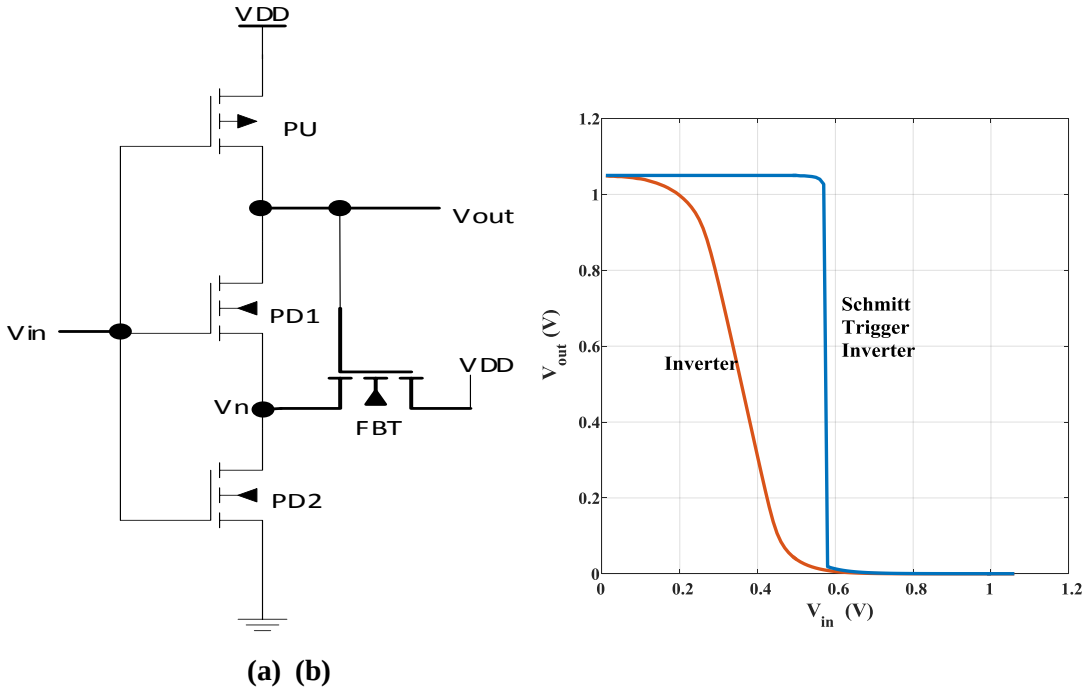


Fig.4. Single-Ended 5T SRAM cell

4.2 Schmitt-Trigger:

The standard 6T SRAM cell was developed using regular CMOS inverter pair. To maintain stability of SRAM, the back-to-back connected inverter pair stability is essential. The stability of CMOS inverter pair is a major concern at low supply voltages. Therefore, Schmitt trigger (ST) inverter pair is adopted to improve the stability as well as the voltage transfer characteristics. The Schmitt trigger inverter and VTC's are shown in Fig.4.1 (a) and (b). ST works on the principle of positive feedback.

The switching threshold of an inverter is controlled by ratio of NMOS and PMOS transistors. Increasing ratio leads to reduction of threshold and vice versa. So the increasing in the threshold voltage or decreasing the threshold voltage depending on the transition direction of the input. This can be accomplished by employing a positive feedback. Actually, Schmitt trigger consists of six transistors including feedback in pull up network as well as pull down network. The 6 transistors Schmitt trigger in SRAM design increase silicon area. So, in our design feedback path is used only for pull down network as that of ST-1 and ST-2.



(a) (b)

Fig. 4.1 (a) Schmitt Trigger (b) VTC's of Inverter and Schmitt trigger.

Considering input transition from 0 to 1, initially the output stays at high. The feedback transistor is controlled by output of the inverter, so the node (V_n)is $(V_{DD} - V_{th})$. In this case the switching threshold of inverter makes idealistic voltage transfer characteristics as shown in Fig.5 (b), which enhances the hold noise margin, read stability and write ability of the SRAM memory cell.

4.3 13T Schmitt-Trigger SRAM:

A new 13T Schmitt Trigger based SRAM cell (hereafter referred as ST13T) is proposed. It mainly comprises of a cross coupled Schmitt trigger Inverter pair, transmission gate (WAT) in write path, and a decoupled read port arrangement as displayed in Fig.4.2. The gate terminal of feedback transistors (FBL and FBR) are connected to output storage nodes Q and QB. Both drain terminals are connected to the WWLB (inversion of Write-Word-Line) to improve the feedback mechanism. N1 transistor in left ST is controlled by an input control signal (INC). The nodes VL and VR are formed by connecting source terminals of FBL and FBR to the series connected NMOS transistors of the Schmitt trigger Inverter.

In this design, we have used a transmission gate (WAT) in write path instead of single NMOS pass transistor to minimize the write access time of the cell. Transmission gate reduces the access time by producing both strong-0 and strong-1. An input terminal is connected to the Write-Bit-line (WBL) whereas output is connected to the storage node Q. The transmission gate is controlled by both Write-Word-line (WWL) and WWLB.

ST13T employs decoupled read port configuration to reduce read disturb problem and improve the read stability. In this design, read port arrangement was implemented by using regular CMOS inverter and read access transistor (RAT). An input of the inverter is connected to the output node QB and output is associated with one of the terminal of RAT. The source terminal of N5 is connected VVSS to reduce the read bit line leakage. As we discussed earlier, the proposed SRAM cell uses single ended methodology, so it has different Read-Bit-line (RBL) to execute read operation and it's connected to the drain terminal of RAT. Read access transistor (RAT) is controlled by Read-Word-line and enabling RWL gives a successful read operation. Transient analysis and operation of proposed SRAM cell in write, read and standby mode is described in following sub-sections.

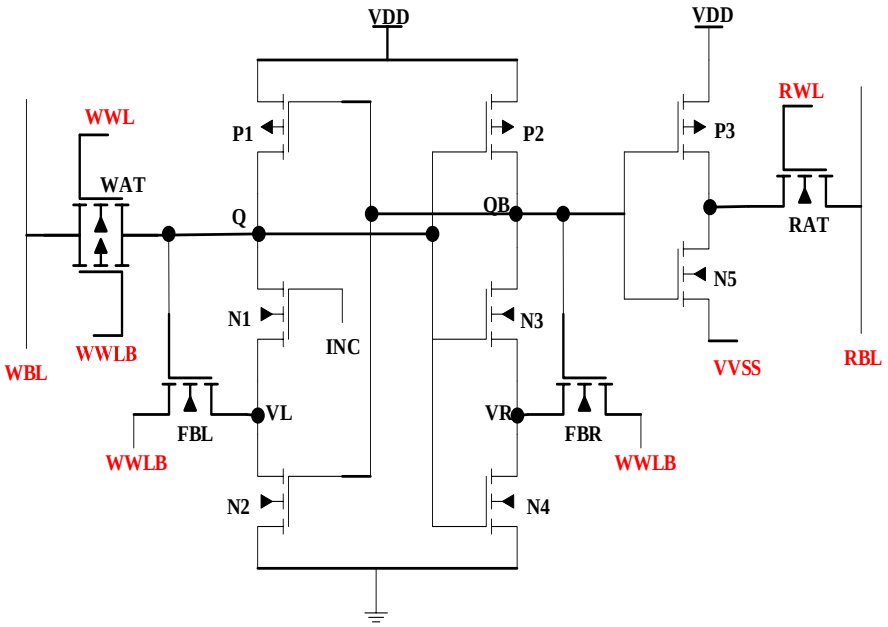


Fig. 4.2. Schematic diagram of proposed design (ST13T).

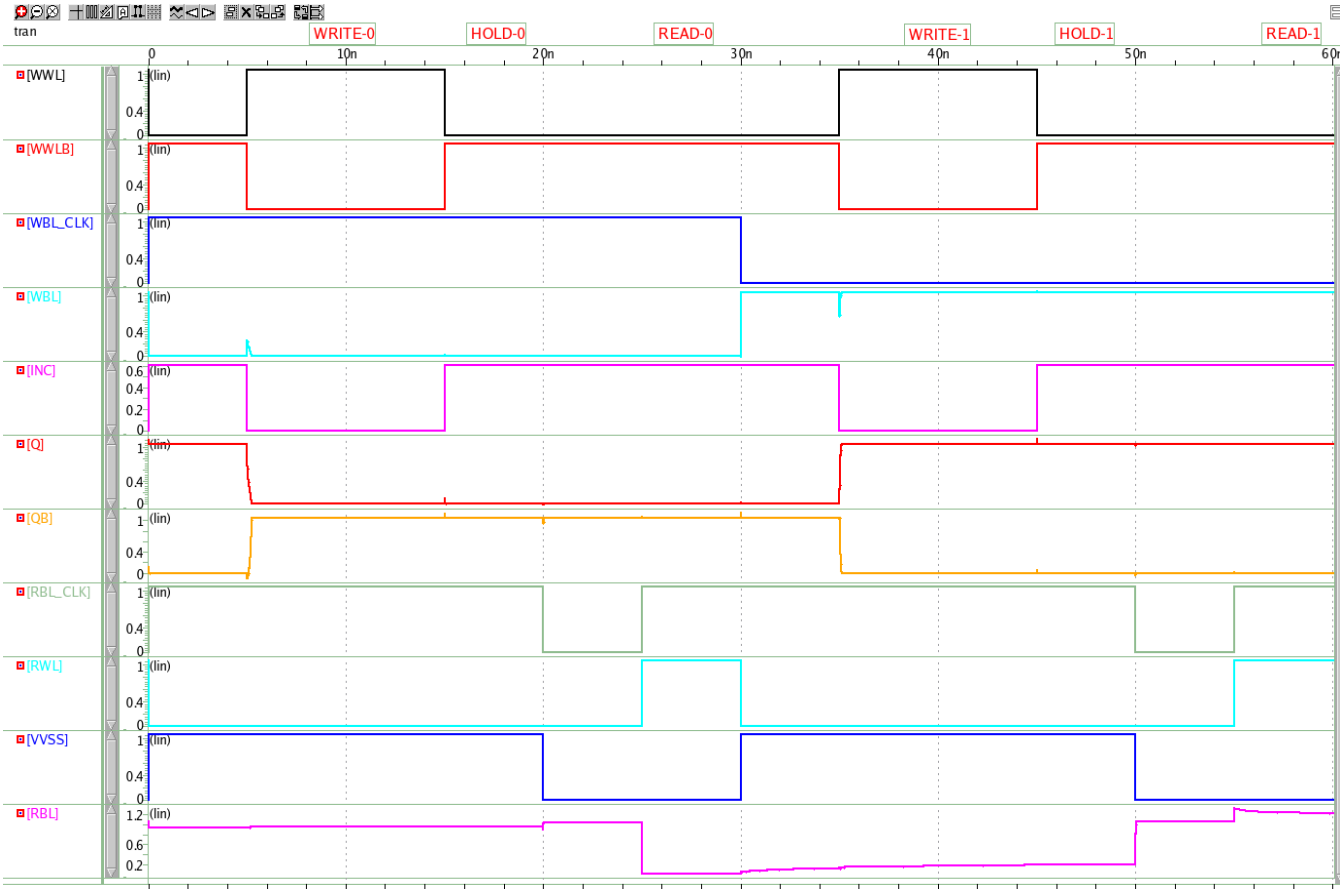


Fig. 4.3. Transient waveforms for the proposed design in write, hold, and read mode.

4.3.1 Write Operation:

To write data into the memory cell, initially we need to set/reset data on Write-Bit-line (WBL), then Write-Word-line (WWL) should be asserted as well as WWLB should be de-asserted. At the time of write operation Read-Word-line (RWL) should be kept low. In this design we have connected N1 transistor to input control signal (INC) to minimize the write-1 access time. In write-1 mode, the input control signal (INC) is set to low which turns off the N1 transistor and makes the storage node Q as float by restricting current through Q to ground. Once WWL and WWLB are activated, the data on the Write-Bit-line transferred to the storage node Q through transmission gate and the back-to-back connected inverter pair try to pulls up the Q to high. The amount of current passes through transmission gate decides write operation speed. The larger width of the transmission gate (WAT) reduces the time to write data to the cell. Similarly, write-0 operates by setting low voltage on WBL.

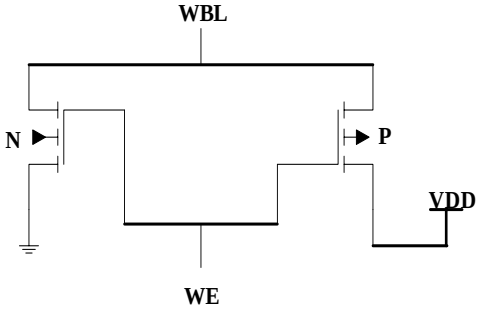


Fig. 4.4. Write-driver circuit.

To set/reset data on WBL, we have used write driver circuit as shown in Fig. 4.4. It comprises of NMOS (N) and PMOS (P) transistors. The source terminals of N and P are tied to ground and V_{DD}. Transistors N and P are controlled by write enable (WE) signal and drain terminals are connected to Write-Bit-line (WBL). Setting/Re-setting of the write-enable (WE) signal determine the data on the WBL.

4.3.2 Read Operation:

As discussed earlier, the proposed design has a separate read port configuration which increases the RSNM of the cell and solves the read disturb problem. To perform read operation, initially we keep both WWL and RWL at low and Read-Bit-line (RBL) is pre-charged at high then assert RWL to high. In addition to this, the virtual ground (VVSS) is low while reading the contents and changed to high in hold as well as write mode. The data on the output node QB determines whether RBL ought to be remain at logic-1 or discharge to logic-0. Feedback transistors (FBL and FBR) are tied to V_{DD} in read mode which enhances the characteristics of the Schmitt-trigger inverter. INC should be high in read mode.

4.3.3 Hold Operation:

In standby mode, the WWL and RWL are disabled whereas WWLB is enabled. Due to this, no connection exists between the cross coupled Schmitt trigger inverter pair and the access transistors. INC is set to high. An enabled WWLB makes drain terminals of the feedback transistors at V_{DD}. Let us assume Q=0 and QB=1, then VR becomes $V_{DD} - V_{thn}$.In this situation, the lowest voltage required at Q to flip the cell should be much greater than the threshold voltage of NMOS (V_{thn}). So, it enhances the hold static noise margin of the memory cell in standby mode.

4.4 13T SRAM Cell Performance Evaluation:

The proposed single-Ended Schmitt trigger based 13T SRAM memory cell was designed in Synopsys Galaxy Custom Designer Tool using Synopsys SAED FreePDK 32nm technology. The layout was designed and DRC,LVS checks were completed using Hercules and extracted view was generated by using StarRC. Post layout simulations were conducted by HSPICE and waveforms were analyzed by using Custom Wave-view. We have used minimum width of the transistors to validate the proposed SRAM cell at different supplies which is presented in Table-I. The following sub-sections illustrates performance metrics of the proposed design.

Table-I. Transistor length and widths of proposed design

TRANSISTOR	WIDTH/LENGTH
P1, P2, P3	100 nm/32 nm
N1, N2, N3, N4, N5	200 nm/32 nm
FBL, FBR	150 nm/32 nm
WAT	NMOS – 150nm/32 nm PMOS – 200 nm/32 nm
RAT	150 nm/32 nm
N	200 nm/32 nm
P	200 nm/32 nm

4.4.1 Write Access Time:

Single ended SRAM designs have higher write-1 access time than the write-0 at lower supply voltages due to single NMOS pass transistor in write-path. We have minimized this difference by implementing an input control signal(INC) and a transmission gate (WAT) in write path. Enabling of INC to low while writing 1 in the proposed bit cell minimizes the data contention between pull up and pull down path, this results to increased speed of write-1 operation. The write-1 access time is measured as the time gap between the 50% of write word-line (WWL) to the time when the storage node reaches 90% of V_{DD}. Similarly, the write-0 access time is measured as the time gap between the 50% ofWWL to the time when storage node discharges to 10% of V_{DD} [36]. Fig.4.5 and Fig.4.6 depicts both write-1 and write-0 access time with and without write driver circuit at different operating voltages.

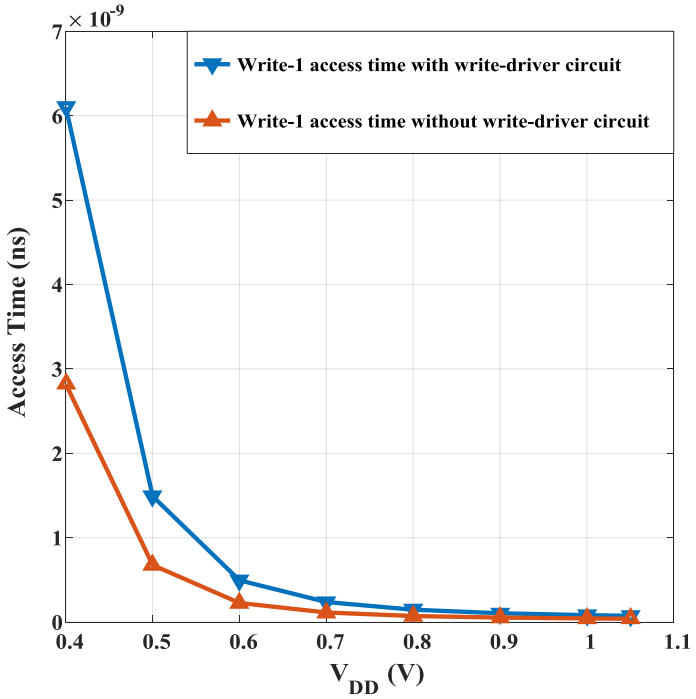


Fig. 4.5. Write-1 access time with and without write-driver circuit at different supply voltages.

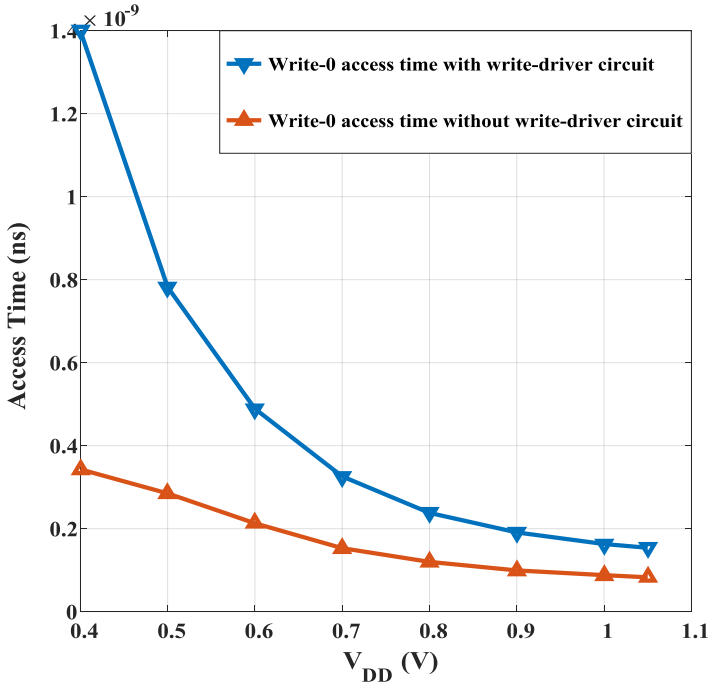


Fig. 4.6. Write-0 access time with and without write-driver circuit at different supply voltages.

The ST13T SRAM cell offers lower write-1 access time than write-0 at higher supply voltage nodes due to the input control signal (INC). At lower supply voltages, time takes to discharge Q below the threshold voltages of N3 and N4 decreases and this results in quick rise of QB. Furthermore, it takes less time to discharge Q to 10% of V_{DD} . Also, it shows that the write-1 and write-0 access times are decreases nearly 50% of that of ST13T SRAM cell without using write-driver circuit. The plots are in Fig. 4.7 and Fig. 4.8, displays both write-1

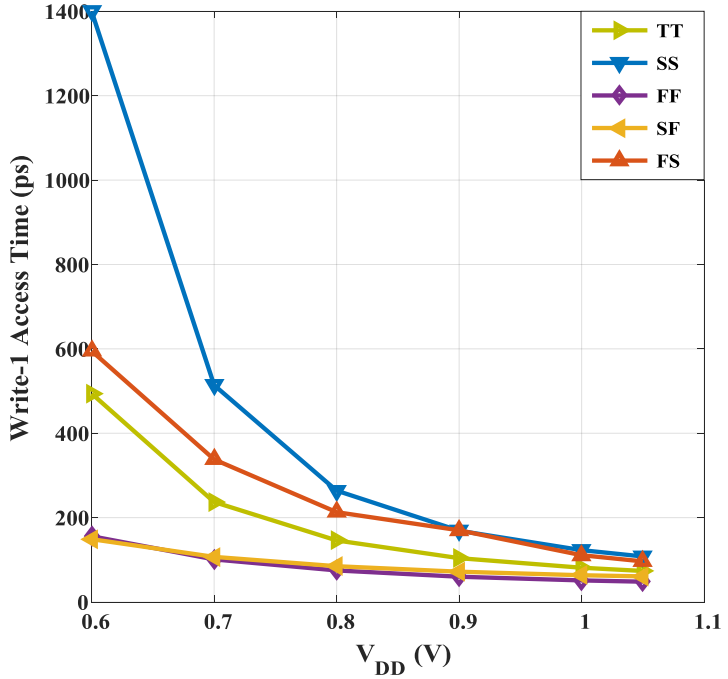


Fig. 4.7. Write-1 access time at different process corners with write-driver circuit.

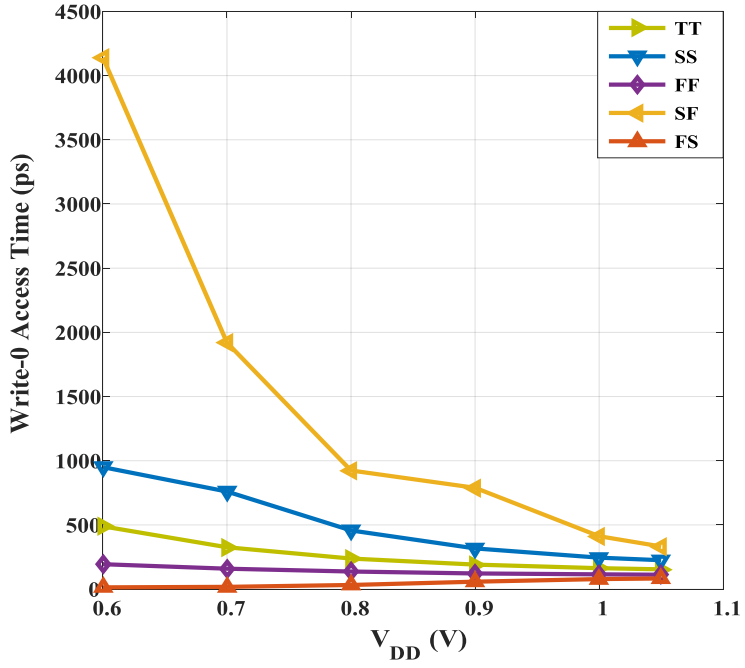


Fig. 4.8. Write-0 access time at different process corners with write-driver circuit.

and write-0 access times with write-driver circuit at different process corners SS, FF, TT, SF, and FS. Maximum write-1 access time for ST13T SRAM cell undergoes at SS corner whereas write-0 access time undergoes at SF corner. Sizes of N and P for write-driver circuit varied according to the process corners. Fig.4.9 and 4.10, shows both write-1 and write-0 access times at different process corners without write-driver circuit. The write-1 and write-0 access time reduces for without write-driver analysis.

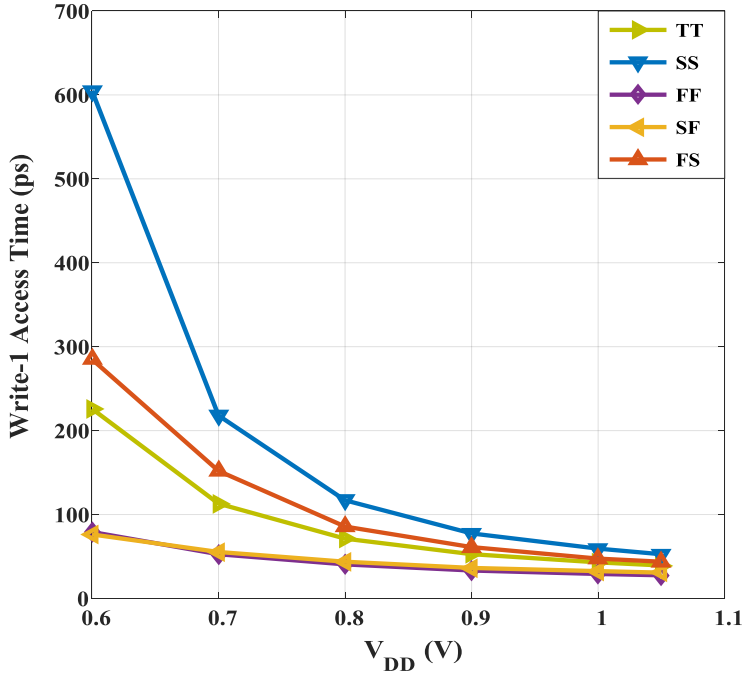


Fig. 4.9. Write-1 access time at different process corners without write-driver circuit.

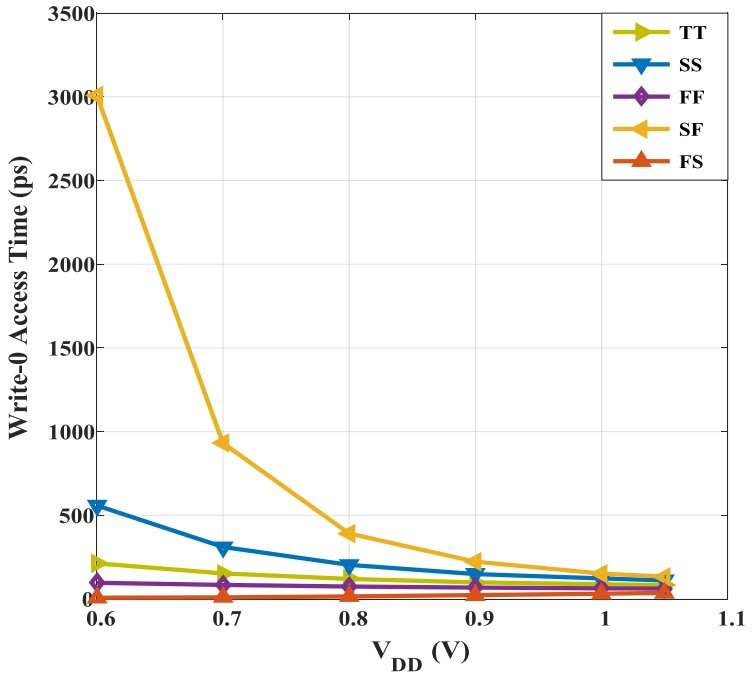


Fig. 4.10. Write-0 access time at different process corners without write-driver circuit

4.4.2 Read Access Time*:*

Read access time is estimated as the time duration between the 50% of Read-Word-line (RWL) to the time when Read-Bit-line (RBL) discharges to 10% of V_{DD}. The value stored at QB decides RBL voltage level whether it should be stay at logic-1 or discharges to logic-0. The proposed SRAM (ST13T) has inverter in read path, it makes the memory cell to achieve lower read-0 access time as well as an acceptable read-1 voltage level.

Pre-charged voltage is applied to RBL as equal to supply voltage before read operation. This reduces the RBL leakage from un-accessed memory cells while perform read-1 operation as compared with read buffer designs.

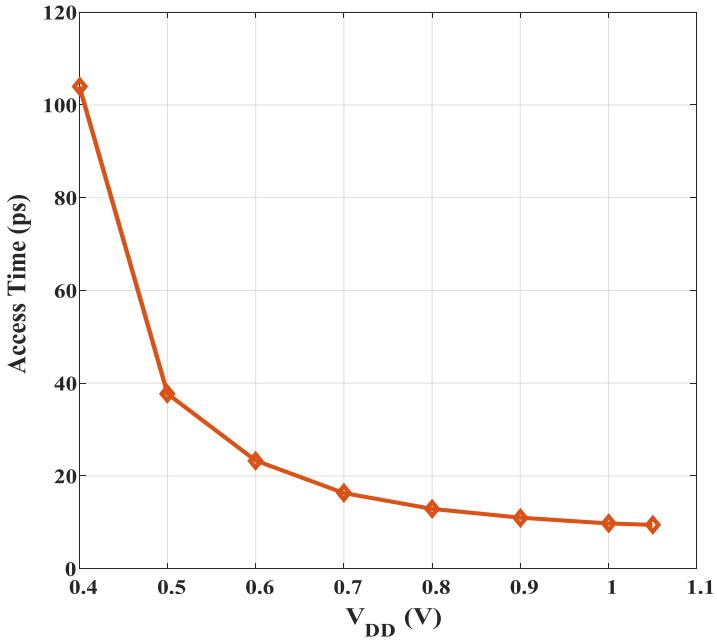


Fig. 4.11. Read-0 access time at different supply voltages.

Read-0 access time ST13T at different operating voltages is shown in Fig. 4.11. It displays that the proposed design achieves tremendously less read-0 access time at each supply voltage with 5ns pulse width of Read-Word-line (RWL). Fig. 4.12 shows that the read-0 access time at different process corners. It displays that the ST13T takes more time to discharge RBL to 10% of V_{DD} at SF corner due to slow NMOS in read path.

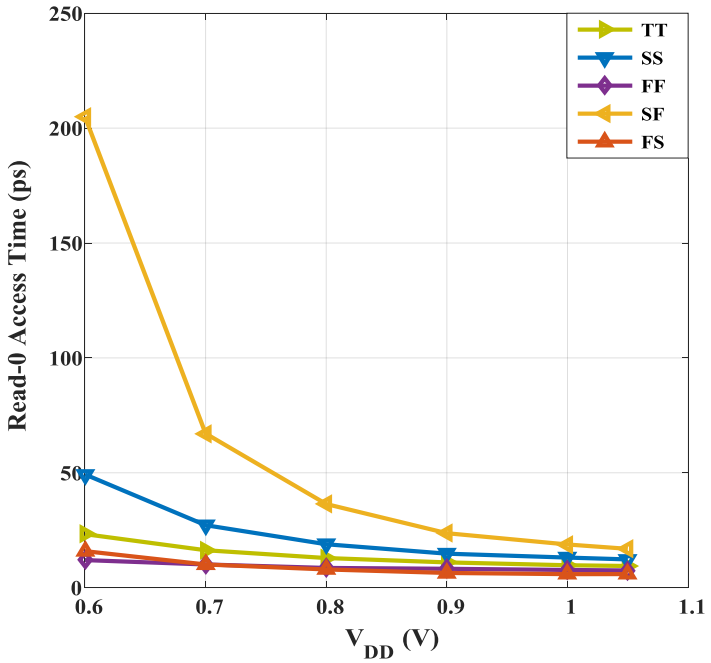


Fig. 4.12. Read-0 access time at different process corners.

4.4.3 Static Noise Margin:

The SNM is defined as the maximum amount of DC noise (V*N*) that can be tolerated by the cross-coupled inverter pair such that the bit-cell retains its data [13].

4.4.3.1 Hold Static Noise Margin (HSNM):

Hold static noise margin (HSNM) of the ST13T SRAM bit-cell is obtained using butterfly curves method, which is suggested in [13]. In this method, a noise source is applied to cross coupled ST based inverter pair by keeping the access transistors off. Usually, HSNM of the cell decides the stability of the memory cell in standby

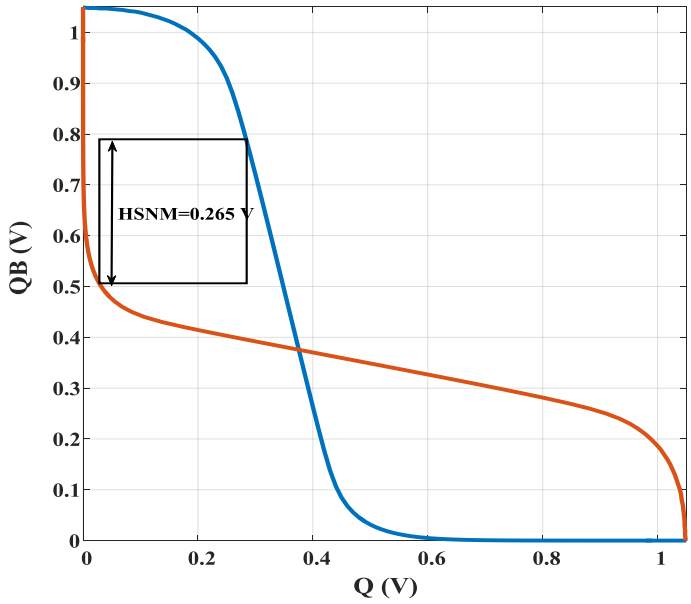


Fig. 4.13. HSNM of 6T SRAM at supply voltage of 1.05V.

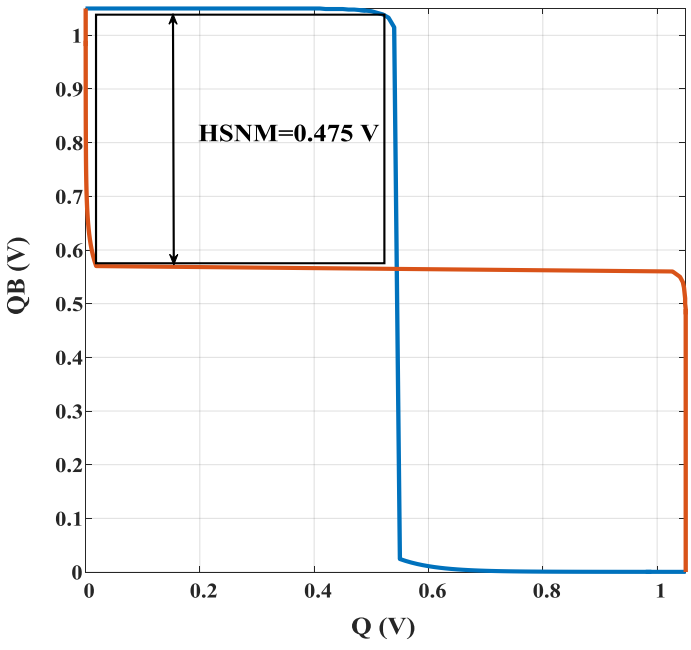


Fig. 4.14. HSNM of ST13T at supply voltage of 1.05V with INC=0.6V.

mode. Butterfly curves were plotted by sweeping the output node voltages Q and QB, calculated maximum length of the square is inscribed between curves. The maximum length of the square determines hold static noise margin of the SRAM memory cell. Fig.4.13 and Fig.4.14 shows butterfly curves for the 6T SRAM and ST13T SRAM. It exhibits the proposed design offers higher hold noise margin as compared with traditional 6T SRAM cell because of the feedback mechanism. To get higher HSNM for proposed design, input control signal (INC) should be connected to the 0.6V at the supply voltage of 1.05V. The HSNM for the proposed design is obtained as 0.475V whereas 6T cell achieves 0.265V at supply voltage of 1.05V.

Controlling of an input control signal (INC) is required to get higher HSNM as well as RSNM for the proposed design. The required minimum voltage for an INC should be slightly higher than 50% ofV_{DD} at the supply voltages changed from 1.05V to 0.6V and it should be same as the supply voltage below 0.6V. At these conditions, the output node does not float while reading as well as holding the data and it achieve high noise margins for the proposed design.

4.4.3.2 Write Static Noise Margin (WSNM):

The Write Static Noise Margin (WSNM) determines the write ability of SRAM cell. There are several techniques proposed to obtain write static noise margin of the bit-cell such as butterfly curve method, Bit-line method, Word-line technique, and N-curve method [14]. The Bit-line method was used in this design to compute write static noise margin of the cell. In this method, Write-Bit- line is swept from 0 to V_{DD}, both WWL and WWLB are tied to V_{DD} and GND. The input control signal (INC) is set to low. The voltage at which both output nodes Q and QB flips is called as write trip voltage or write trip point. The write trip point of the cell defines the write static noise margin.

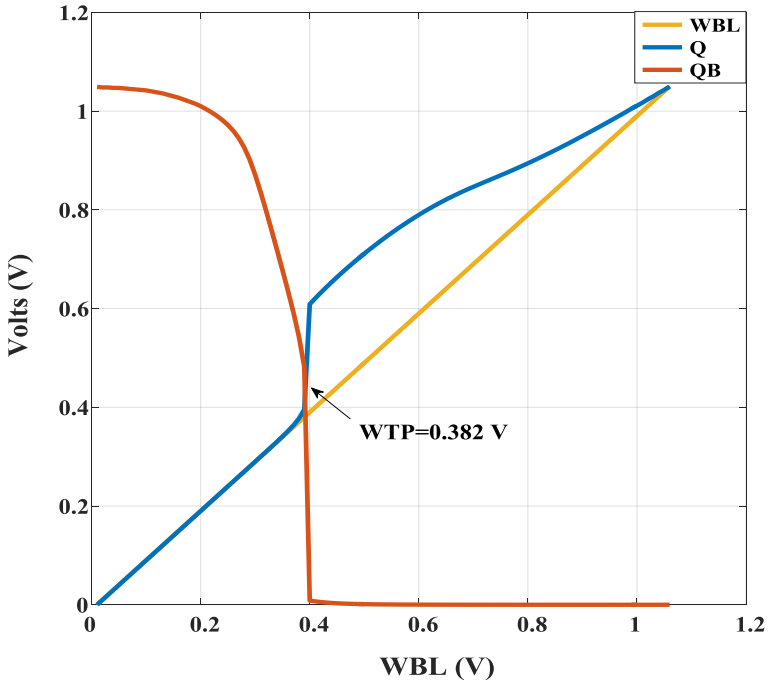


Fig. 4.15. Write-trip point of ST13T at V_{DD} =1.05V

As we know the single ended SRAM designs offers a high write-1 access time, so that write-1 static noise margin is less than the write-0 noise margin. For the proposed design, write-1 noise margin is 0.382V at supply voltage of 1.05V. We have measured write-1 noise margin at distinct operating voltages, which is shown in Fig.4.16.

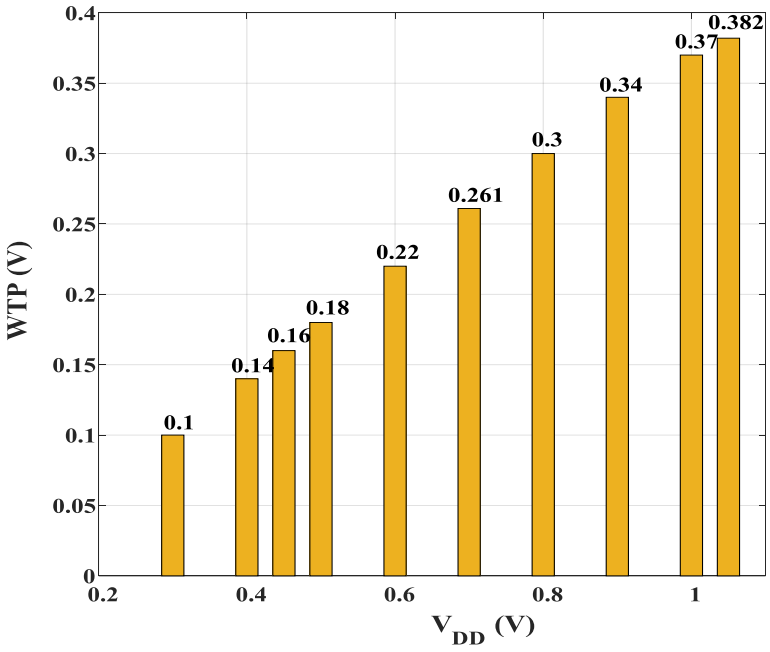


Fig. 4.16. WTP of ST13T at different supply voltages

4.4.3.3 Read Static Noise Margin (RSNM):

The Read Static Noise Margin (RSNM) or Read-stability of the proposed design is measured by butterfly curve method suggested in [13]. In this technique, RBL and RWL are tied to V_{DD}. Swept the output nodes Q and

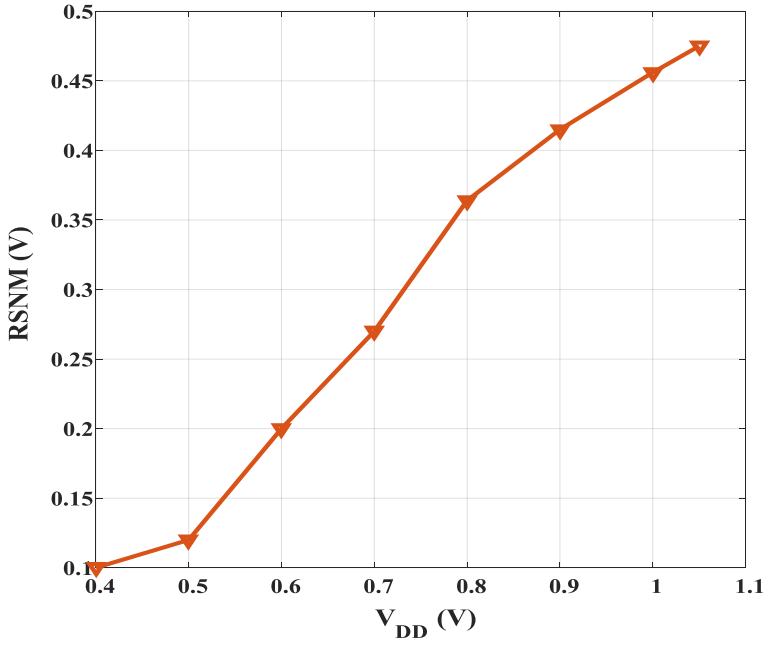


Fig. 4.17. RSNM of ST13T at different supply voltages.

QB by keeping the write-access transistor (WAT) off. RSNM is estimated as the length of the largest side square that can be embedded between the butterfly curves. Proposed design employs a decoupled read port configuration so it offers high RSNM as compared with differential topologies. Due to decoupled node, the RSNM of the cell is almost similar to HSNM of the cell. Since the HSNM is high for Schmitt trigger based SRAM, RSNMand read stability are improved to a large extent. Fig.4.17. shows that the RSNM of the proposed cell at different supply voltages. It is shown that ST13T offers very high RSNM as 0.47V at supply voltage of 1.05V. We noticed form Fig.4.18, the proposed ST13T SRAM cell produces significantly improvement in RSNM as compared with both 6T and conventional 8T SRAM cells.

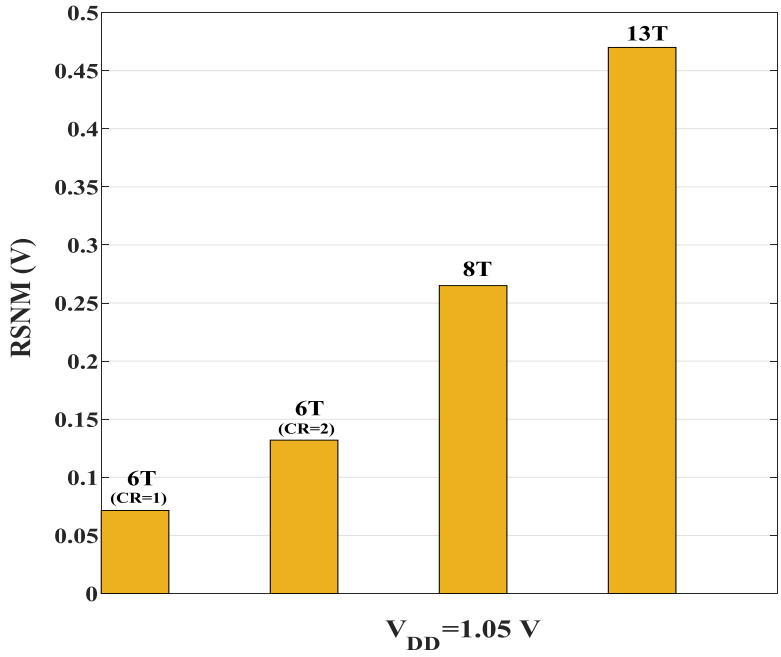


Fig. 4.18. Comparison of RSNM of 6T, 8T, and ST13T

4.4.4 Write and Read Power Consumption:

Power consumption for write-1, write-0 and read-0 at different supply voltages for the proposed cell (ST13T) is presented in Fig.4.19 and 4.20, which depict average power at different pulse widths of WWL and RWL. The average power consumption reduces with increasing of the pulse widths of WWL and RWL. First, we measured write-1 and write-0 power consumption at 10ns of WWL pulse width and minimum width of WWL to operate write-1 and write-0 correctly at different supply voltages. The required minimum pulse width of WWL increases as we reduce the supply voltage. It is evident from plot that the average power consumption of write-0 is more than the write-1 in both manner. As we discussed earlier, the capacitance load and bit-line switching are reduced in the single ended SRAM designs so it results in less power consumption for ST13T. To measure read-0 power, we have given Read-Word-line (RWL) pulse width of 5ns and required minimum pulse width to perform successful read operation. At these considerations, the proposed design consumes less power for read-0 over both write-1 and write-0. The ST13T achieves extremely low power at lower supply voltages. By making use of input control (INC) signal, write-1 power consumption is significantly reduced, specifically at higher voltages.

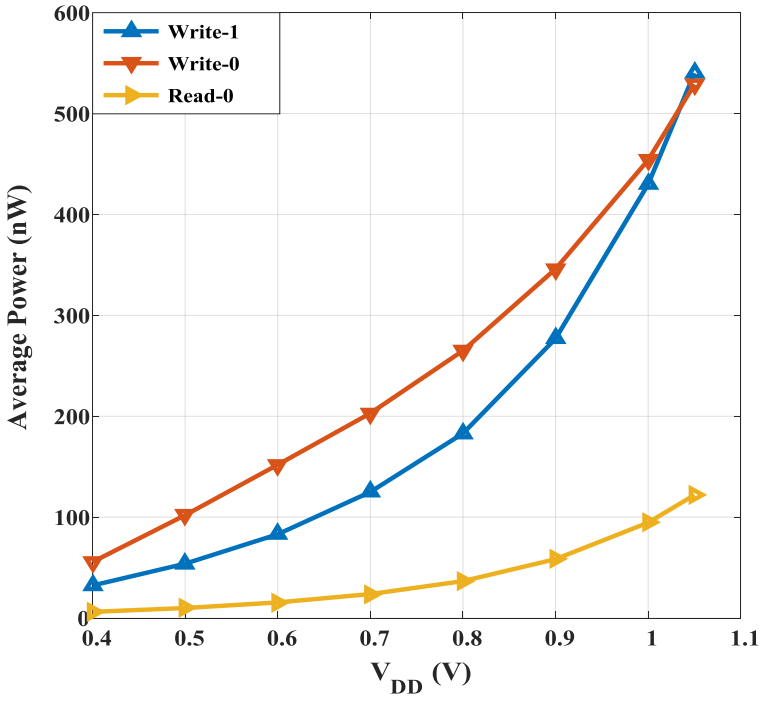


Fig. 4.19. Average power-consumption of Write-1, Write-0 and Read -0 with 10ns pulse width of WWL

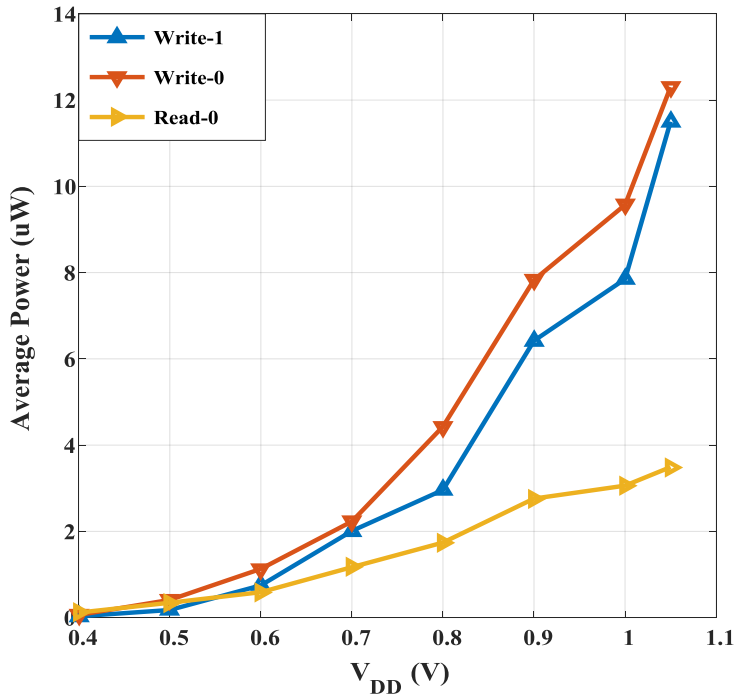


Fig. 4.20. Average power-consumption of Write-1, Write-0 and Read -0 with minimum WWL pulse width

4.5 4x4 memory array design:

Custom layout was developed for 4x4 memory array design of proposed (ST13T) SRAM bit-cell. Each Write-Bit-line (WBL) and Read-Bit-line (RBL) incorporates four bit cells in this array of design. WWL and WWLB of transmission gate are connected in row based fashion. INC is also row-based. To set/reset data on each Write-Bit-line (WBL), write-driver circuit was used as discussed earlier and minimum widths of transistors are

considered. RWL is connected in row based fashion whereas RBL is connected in column based. The schematic and layout views for 4x4 memory array design are shown in Fig.4.21 and 4.22. The applied pre-charged voltage is equal to the operating voltage so it gives less Read-Bit-line leakage from un-accessed cells. Due to inverter in read path, read-1 voltage is improved as compared with read buffer designs. To validate the design, we performed 4-bit operation at a time by setting INC of un-accessed cells as high and observed access times for each memory cell. The input control signal (INC) is set to low while performing write-1 and write-0 operation.

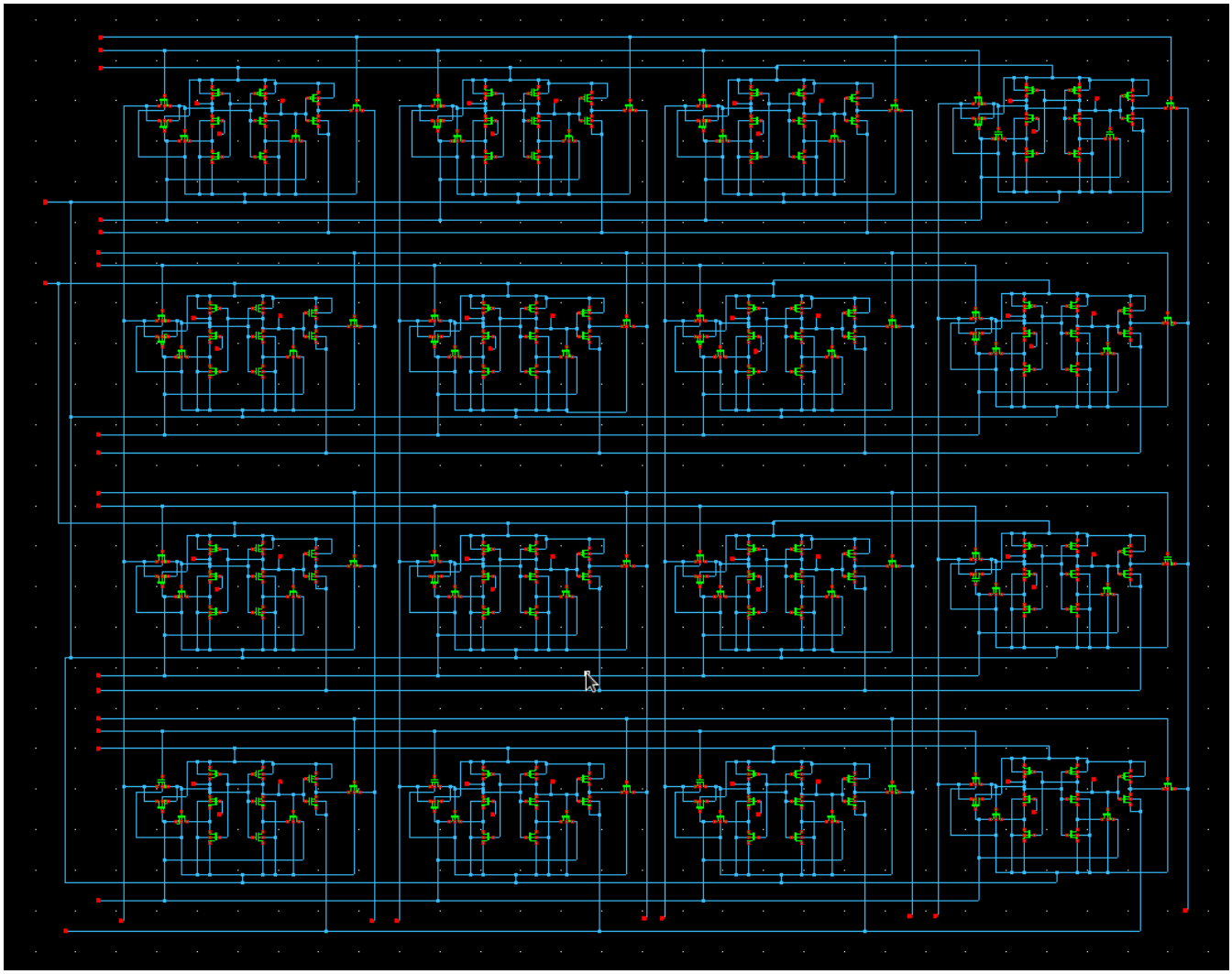


Fig. 4.21. Schematic of 4x4 memory array design

Table-II shows write-1, write-0 and read-0 access times for 4-bit operation whereas write-1 and write-0 performed through write-driver circuit. The Write-Bit-line capacitance load increases for 4x4 memory array as compared with single memory cell. So it affects both write access time and read access time. The worst case access time for write-1 and write-0 obtained as 75.9ps and 162ps at supply voltage of 1.05V. To make thorough comparison with single bit, Read-0 access time for 4x4 array is measured as time gap between activation of RWL to time when RBL discharges to 10% of V_{DD}. The worst case read-0 access time for 4x4 array obtained is 60.3ps at V_{DD} =1.05 V.

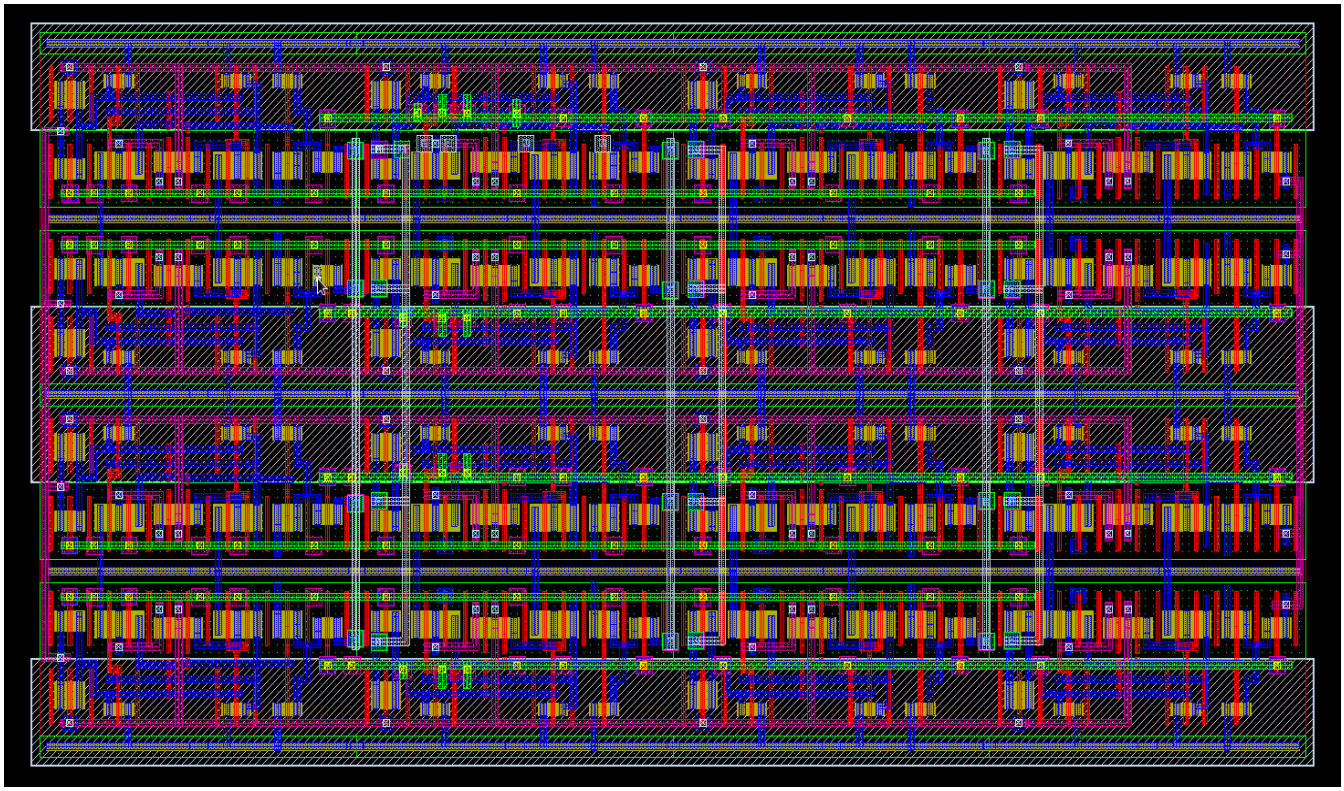


Fig.4.22. Layout view of 4x4 memory array design

Table – II. Write-1, Write-0, and Read-0 access times for 4x4 memory array

Operation	Write Access Time (ps)				Read-0 Access Time(ps)				Write Access Time (ps)				Read-0 Access Time (ps)			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q5	Q6	Q7	Q8
1111	75.6	75.5	75.7	75.7	-	-	-	-	76	75.5	75.6	75.7	-	-	-	-
0000	161	161	161	161	59	58.6	57.9	36.2	161	161	161	161	60.5	59.8	59.1	37
1010	75.6	160	75.7	160	-	58.4	-	36.1	76.1	160	75.7	160	-	59.6	-	37
0101	160	75.6	160	75.7	57.3	-	56.2	-	159	75.6	160	75.8	59	-	57.7	-
Operation	**Write Access Time (ps)**				**Read-0 Access Time(ps)**				**Write Access Time (ps)**				**Read-0 Access Time(ps)**			
	Q9	**Q10**	**Q11**	**Q12**	**Q9**	**Q10**	**Q11**	**Q12**	**Q13**	**Q14**	**Q15**	**Q16**	**Q13**	**Q14**	**Q15**	**Q16**
1111	75.9	75.5	75.6	75.8	-	-	-	-	75.5	75.8	75.6	76	-	-	-	-
0000	160	161	161	161	60.3	59.7	59.1	37	162	162	162	162	60.3	59.6	59.1	36.6
1010	75.6	160	75.3	160	-	59.3	-	37	75.6	160	75.6	160	-	59.5	-	36.5
0101	159	75.5	160	75.8	58.8	-	57.7	-	160	75.8	160	76	58.5	-	57.4	-

4.5.1 Read-Bit-line Leakage Analysis:

Read-bit-line leakage analysis were conducted for the 4x4 memory array design. Fig. 4.23 depicts the read port configuration of the accessed cells and un-accessed cells of the memory array. The source terminal of the nMOS is connected to the virtual supply (VVSS) to reduce the bit line leakage. It is set to low when reading the data from the cell otherwise it is set to high. The read-bit-line is pre-charged to high before performing the read operation. Read-Word-Line (RWL) and VVSS of the accessed cell is set to 1 and 0. The node QB=0 turns on P3 and pulls the output node to high, it successfully completesread-1 operation. To get accepted level of read-1 voltage, the RBL leakage must be low. There are two possible ways to verify leakage current from un-accessed cells. If QB stores 1 for the un-accessed cell, then it turns on the nMOS (N5) of inverter and the output node (Vx) becomes $V_{DD} - V_{thn}$ due to the high VVSS. So, the leakage from RAT and N5 is negligible. Similarly, if QB stores 0, then the output node (Vx) is pulled up to high due to the P3 transistor. The voltage level at the RBL, Vx, and VVSS is almost same, so it greatly reduces the RBL leakage.

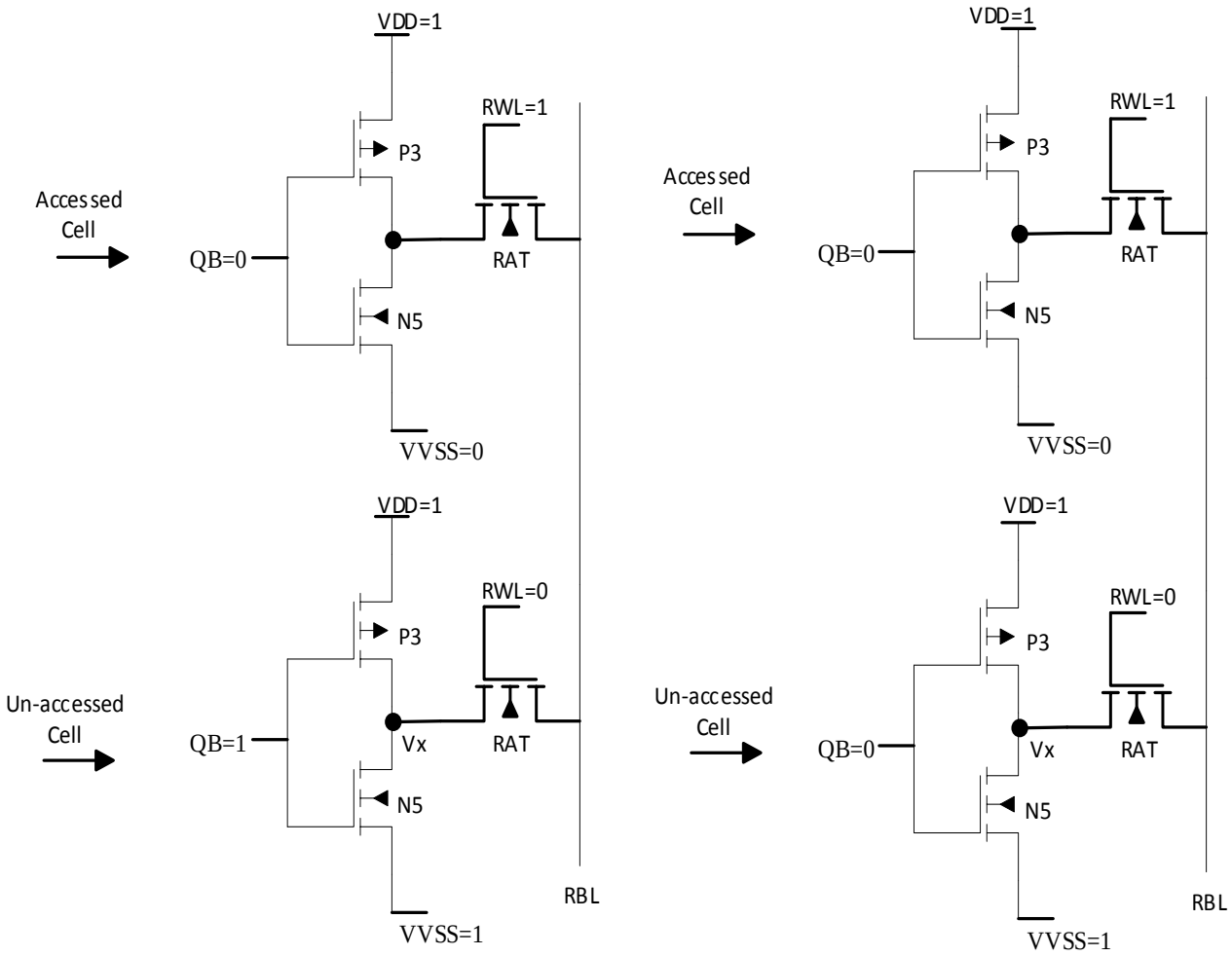


Fig. 4.23. Read port configuration of the accessed and un-accessed cells.

4.6 Comparison with Previous Work:

Performance comparison with previous memory cells in several aspects such as access time, static noise margin, and power consumption are presented. Table III summarizes all comparisons between 6T [36], 8T [25], ST-1 [2], ST-2 [35], ST11T [36] and proposed work (ST13T). The conventional 6T and 8T comprises of regular CMOS inverter pair to hold the data whereas ST-1, ST-2, ST11T and proposed design (ST13T) utilizes Schmitt-trigger inverter pair. As we know that differential bit cells accomplish very less access time over single ended designs, so that the conventional 6T cell takes less time as 0.5 ns and 0.1 ns to write 1 and 0 into the memory cell at the supply voltage of 0.4 V with 22nm technology. In contrast to this, ST11T bit cell utilizes the virtual ground technique to reduce the write-1 access time: however, due to the single ended methodology ST11T offers high write-1 access time than the 6T cell, 7.5ns at supply voltage of 0.4 V with 22nm technology. The proposed ST13T cell uses different write assist technique over ST11T to minimize the write-1 access time 6.1ns with 32nm technology. The wrie-1 access time for the ST13T without writ driver circuit also measured. It reduces the write-1 access time nearly 50%

Table-III. Comparison of various bit cells over different aspects

		6T [36]	**8T [25]**	**ST-1 [2]**	**ST-2 [35]**	**ST11T [36]**	**This Work**
Methodology		Differential	Single-Ended	Differential	Differential	Single-Ended	Single-Ended
Technology node		22 nm PTM	90 nm	130 nm	130 nm	22nm PTM	32 nm
Inverter pair		CMOS Inverter	CMOS Inverter	ST Inverter	ST Inverter	ST Inverter	ST Inverter
Write-1 access time	V_{DD} **=0.4 V**	0.5 ns	1 ns	-	-	7.5 ns	6.1 ns -with WD 2.8 ns -without WD
	V_{DD} **=0.5 V**	0.4 ns	-	-	-	2 ns	1.5 ns -with WD 0.7 ns -without WD
Write-0 access time At V_{DD}=0.4 V		0.1 ns	-	-	-	0.24 ns	1.4 ns – with WD 0.34 ns -without WD
Read-0 access time At V_{DD}=0.4 V		-	-	-	-	-	0.104 ns
WSNM	V_{DD} **=1 V**	-	0.4 V	0.49 V	0.53 V	-	0.37 V
RSNM	V_{DD} **=1 V**	-	0.42 V	0.18 V	0.2 V	-	0.45V
	V_{DD} **=0.9 V**	0.07 V	-	-	-	0.35 V	0.415 V
HSNM At V_{DD}= 1 V		-	-	0.4 V	0.38 V	-	0.45 V
Write-1 power At V_{DD}=0.9 V		13 uW	-	-	-	3 uW	6.42uW
Write-0 power At V_{DD}=0.9 V		18 uW	-	-	-	15 uW	7.83uW
Read-0 power At V_{DD}=0.9 V		-	-	-	-	-	2.76 uW

over write-driver circuit analysis. Differential topology cells offers very high write static noise margin over single ended designs and this is the reason the proposed design operates at a lower write ability than the 6T, ST-1, and ST-2. It is evident from the Table, 6T, ST-1 and ST-2 bit cells acquire very low read static noise margin at supply voltage of 1V and 0.9 V over 8T, ST11T, and ST13T. The proposed design uses decoupled read port configuration to minimize read disturb problem and Schmitt trigger to enhance read noise margin. So, it results in a higher read noise margin of 0.45 V at $V_{DD} = 1\,V$. As discussed earlier, single ended designs reduce the 50% of bit-line switching over differential SRAM. It is shown from the table ST11T and ST13T consume very less write-1 power than that of 6TSRAM cell. Moreover, ST11T consumes less power than the ST13T by using the virtual ground technique. The average write-0 power consumption for the proposed ST13T is 7.83uW at supply voltage of 0.9 V whereas the 6T and ST11T consumes 18 uW and 15 uW with 22nm technology, respectively.

5. Conclusion

This thesis presented a Schmitt trigger based low power single ended 13T SRAM cell. The proposed ST13T cell utilizes decoupled read port configuration and cross coupled Schmitt trigger pair, which significantly improved HSNM and RSNM. This design achieves higher RSNM, 3.65x and 1.79x as compared with 6T cell and 8T cell ($V_{DD} = 1.05\,V$), respectively. The inverter in read path enhances read performance as well as read-1 voltage level. In this design the source terminal of nMOS transistor of inverter in read path is activated low in read mode and activated high in write as well as in hold mode. It greatly reduces the read bit line leakage (RBL) from un-accessed memory cells as compared with the conventional 8T SRAM cell. Moreover, employing write assist technique improves write-1 access time, especially at lower supply voltages. Consequently, power consumption and read bit-line leakage are significantly reduced. The minimum voltage required to perform write-1 operation is obtained as 0.34 V (~ 100mV lower than the threshold voltage) in 32nm CMOS technology.

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