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Drafting in Self-Timed Circuits

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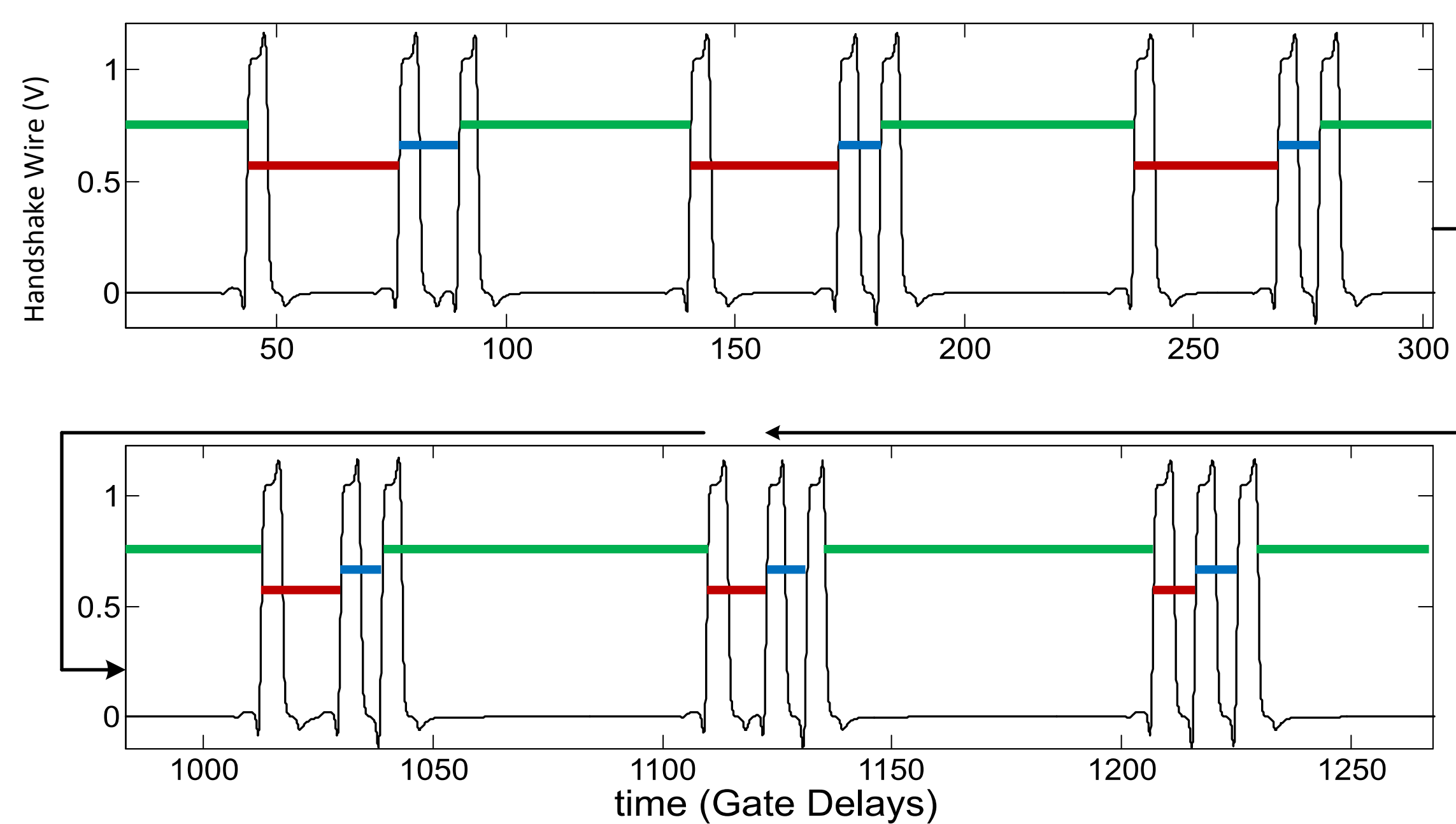
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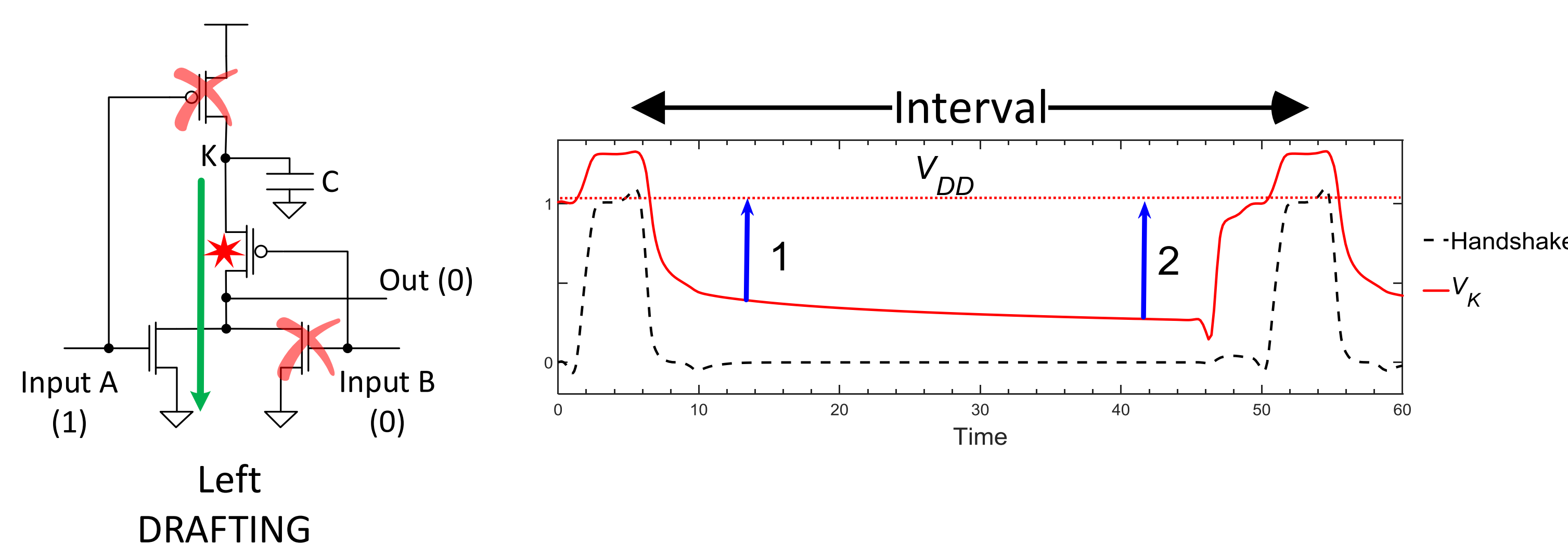
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What is Drafting?

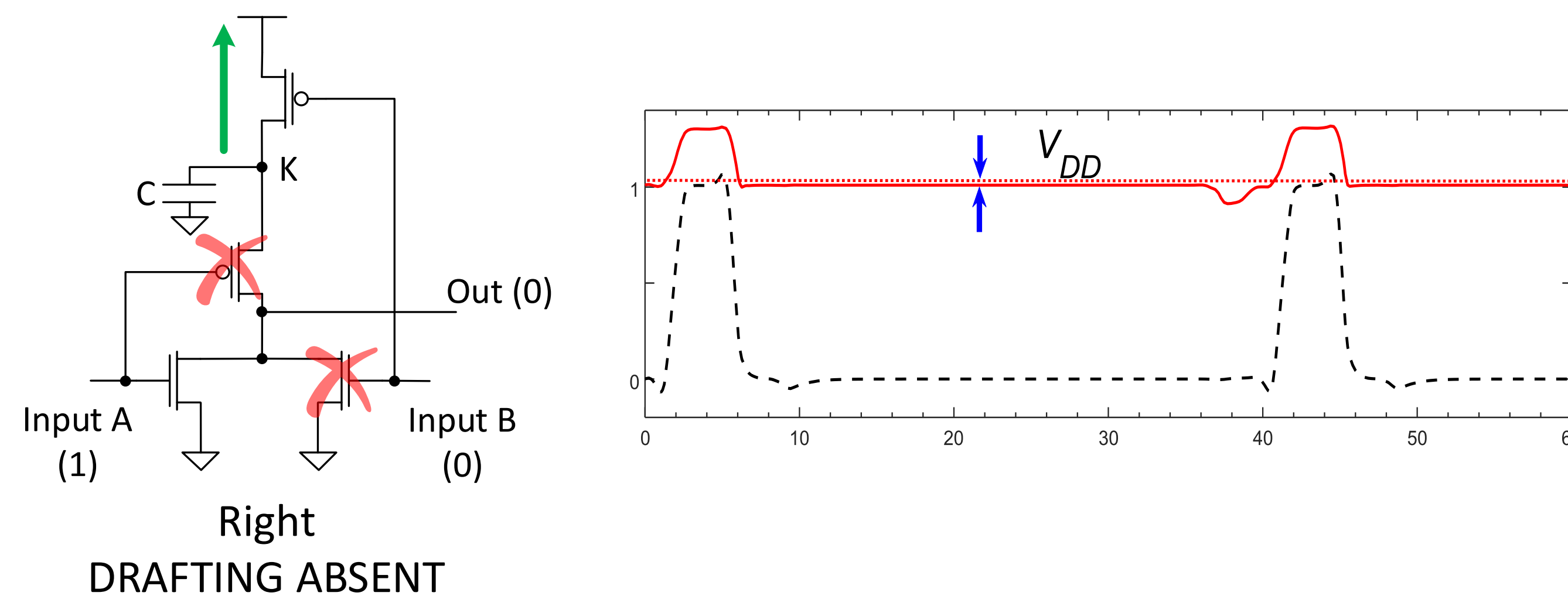
- Handshake pulses travel around a ring of stages.
- Intervals between the pulses change with time.
- The green interval lengthens, while the others shorten.
- This is called "drafting", like bicycle riders.
- If the interval is data, drafting corrupts the data.



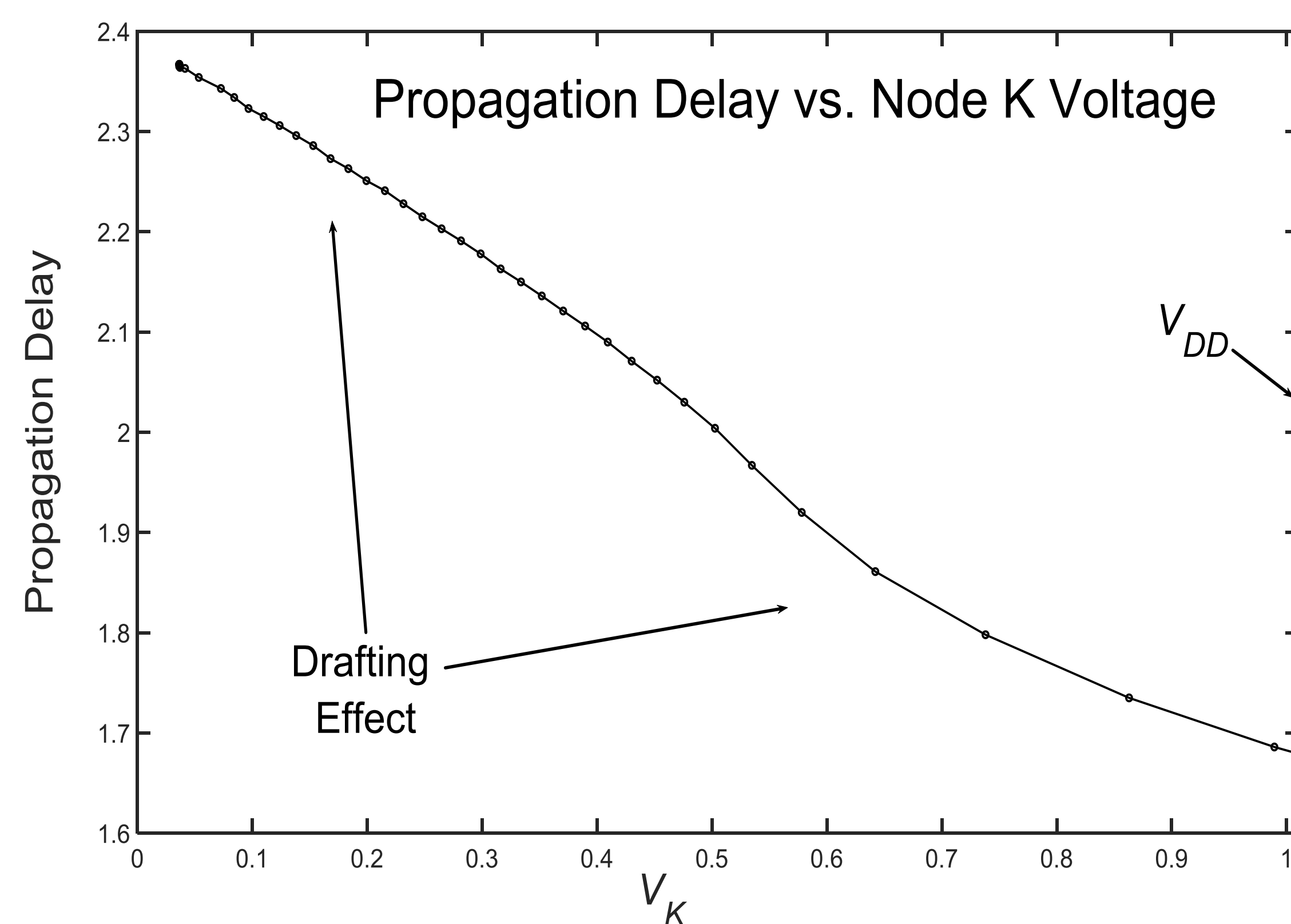
The Behavior of the Internal Node in the NOR Gate Causes Drafting



- Node K discharges during the interval via a diode connected PMOS. *
- As V_K decays it takes longer to charge it back to V_{DD} .
- Longer intervals (2) need longer charge time than shorter intervals (1).
- Longer charge = longer propagation delay through the NOR and drafting.

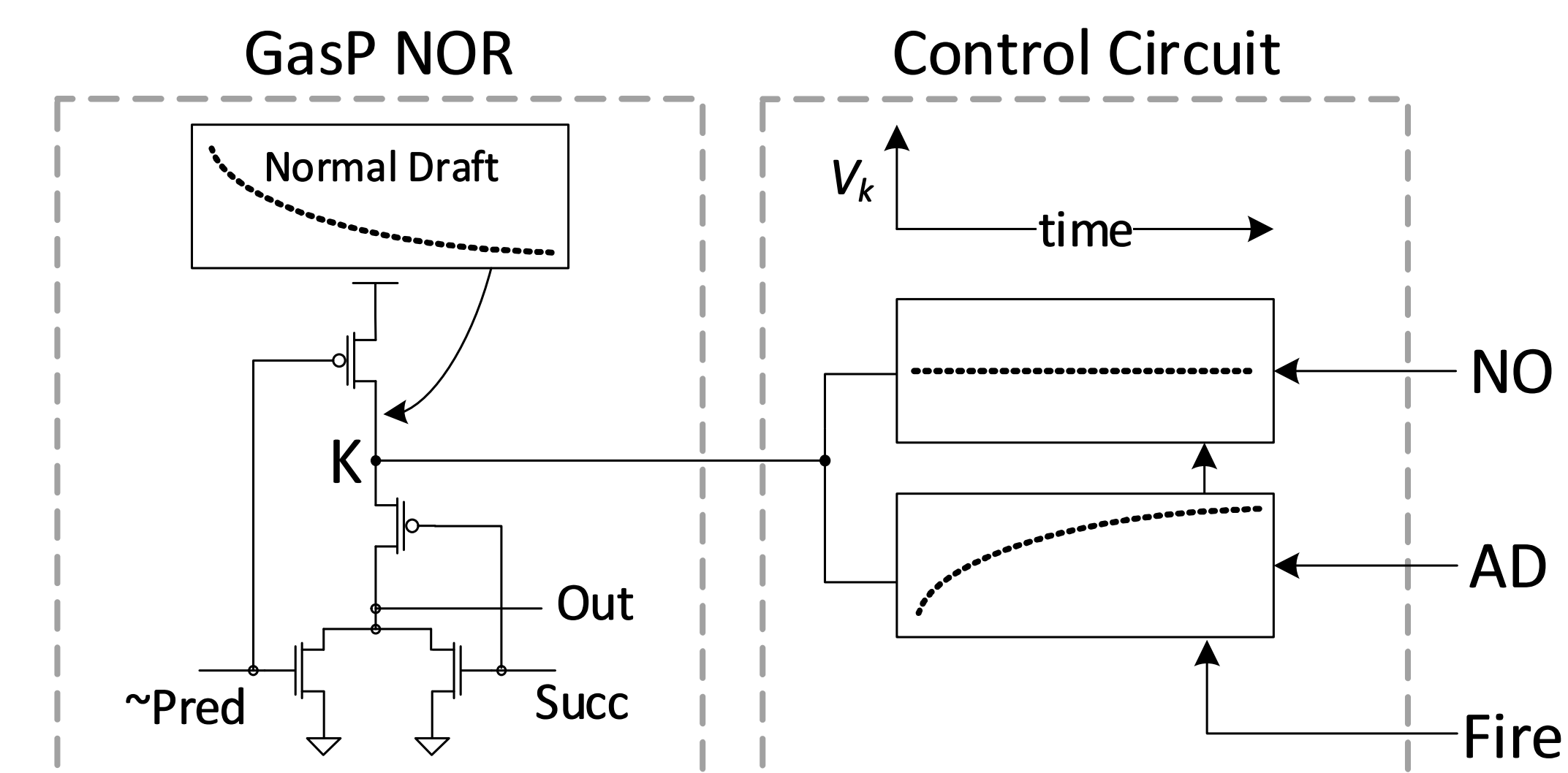


- In the NOR Right configuration V_K stays constant at V_{DD} .
- Propagation time through NOR is constant and drafting is absent.



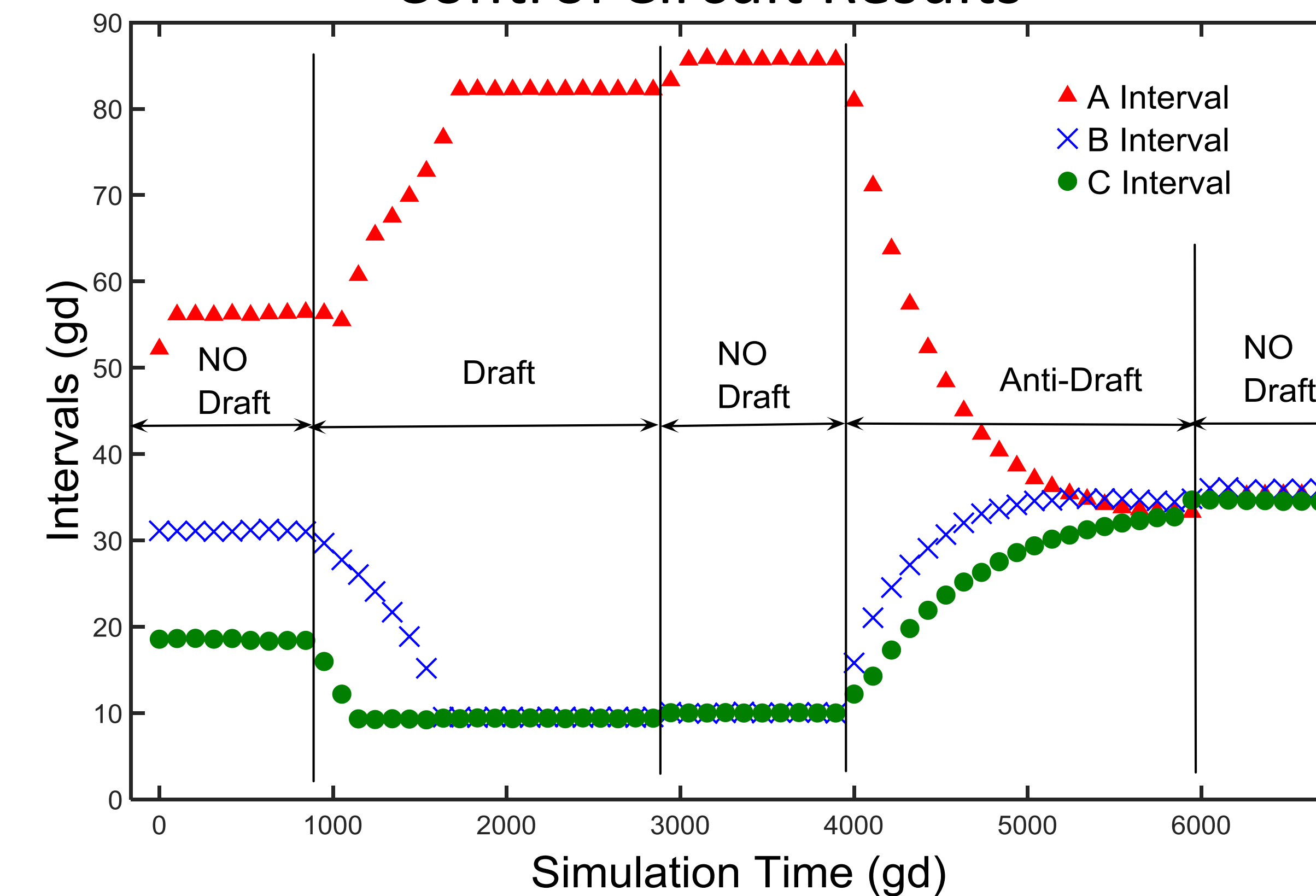
- Propagation delay changes with interval size by the decay of V_K .
- The varying propagation delay creates drafting.
- Short intervals shorten faster than longer intervals.
- In a ring FIFO this results in one long interval and the others short.

Circuit to Control Drafting



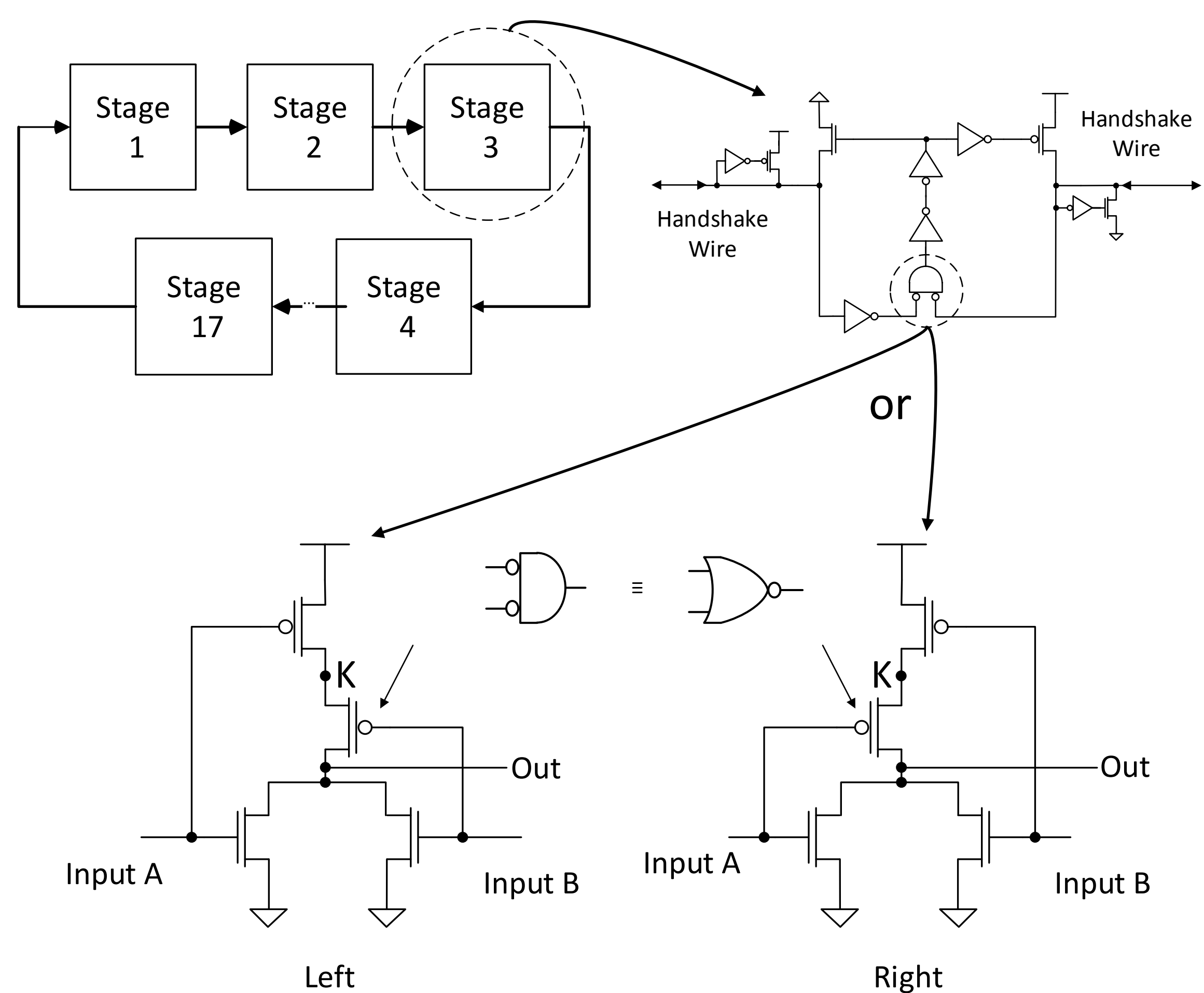
- For drafting, allow the K node to decay normally.
- For NO drafting, keep the K node constant.
- For anti-drafting (AD), force a rising profile at K.
- AD causes intervals to become equal rather than shrinking.

Control Circuit Results



- Three intervals are measured in nominal gate delays during simulation.
- During NO Draft control, the intervals do not change.
- During Draft control, two intervals become minimal and the third becomes maximum.
- During Anti-Drafting control, all intervals become equal.

Test FIFO for Drafting



- The test circuit is a 17 stage FIFO.
- Three circulating handshake pulses and three intervals.
- The handshake decision gate is a NOR.
- The NOR decision gate can be in a Left or a Right configuration with the same logical function.

References

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