Application of a Simplified PLL Algorithm for Unbalanced Three Phase Systems by Using Low Cost Microcontrollers

Mustafa Cem OZKILIC, Atiye Hulya OBDAN

Abstract: In literature, there are many Phased Locked Loop (PLL) methods achieving grid matching successfully under unbalanced grid conditions. However, these methods require high computational resources. In this article, a simplified PLL algorithm has been used with fixed point arithmetic for detecting phase and magnitude of an unbalanced three phase system. The simplification factor comes from the fact that an easy to implement low pass filtering algorithm has been implemented in a 16 bit microcontroller operating at 20 MHz clock speed. Sampling frequency has been selected as 20 kHz so that a low cost grid connected inverter operating up to 20 kHz switching frequency can be designed.

Keywords: Multiple Reference Frame Phased Locked Loop; Phase Locked Loop; Synchronous Reference Frame Phased Locked Loop; Unbalanced Three Phase Voltages

1 INTRODUCTION

One of the important aspects of designing grid connected power electronics systems such as active power filters, distributed power generation systems, flexible AC transmission systems, High Voltage DC transmission systems, distributed energy sources, is the synchronization of the inverter output with the grid itself. Synchronization with the grid means matching the phase and the magnitude of the inverter output voltage with those of the grid voltage. By having this phase information of the grid it would be possible to control the power factor, active and reactive power flow of the system as shown by the authors in [1-2].

Hardware and software adopted PLL methods for grid matching have already been implemented in many applications. Hardware adopted PLL, such as zero-crossing detection can be easy to apply; however at poor grid conditions it would be unreliable. Basic software PLL method, that can easily be implemented, is SRF-PLL (Synchronous Reference Frame PLL). However, just as zero-crossing detection hardware PLL, the quality of the results gathered with SRF-PLL as shown in Fig. 1 are not reliable in unbalanced grid conditions as stated by the author in [3].
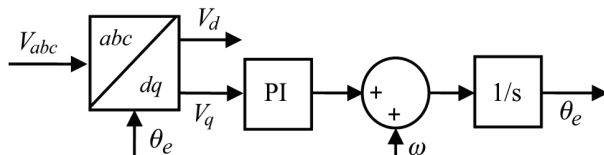

Figure 1 Block diagram illustrating SRF-PLL

In literature, solutions for synchronization with poor grid conditions have been vastly investigated and closed loop methods, such as double synchronous reference frame PLL, multiple reference frame PLL, synchronous reference frame PLL with positive sequence filter/detector, synchronous reference frame PLL with sinusoidal signal integrator etc. have been proposed by authors in [4-13]. In [14-16] authors have proposed open loop methods such as weighted least square estimation,

low pass filtering transformation angle detector, normalized positive sequence synchronous frame etc.

Even though the above mentioned methods have solved the poor grid synchronization problem effectively, the application of these methods in low cost systems becomes inefficient due to the fact that these systems require solutions with less complexity. In this paper, multiple reference frame PLL method utilizing easy to implement low pass filtering with a very low cost 16 bit microcontroller has been used. As a result, a low power low cost grid connected inverter even under unbalanced grid conditions could be designed without the need for high computational resource requirements provided by digital signal processors.

2 POSITIVE AND NEGATIVE SEQUENCE COMPONENTS OF GRID VOLTAGE

Three phase system voltages shown with Eq. (1) can be expressed as balanced positive sequence, negative sequence and zero sequence components according to Fortescue Theorem. Positive sequence components rotate in the positive direction of the reference frame. By locking to the phase and frequency of the positive sequence components, grid synchronization under unbalanced conditions could be achieved. Negative sequence components, on the other hand, which rotate in the reverse direction of positive sequence, are utilized for grid code compatibility in distributed power generation systems. In Eq. (2), positive and negative sequence components of each phase have been shown. The phase information of positive and negative sequence voltages are shown individually in Eq. (3) and Eq. (4). For the sake of simplicity θ_{1p_0} and θ_{1n_0} will be considered to be zero. The results after Clarke and dq transformations applied to $\vec{V}_{abc}$ are shown in Eq. (5). By considering $\theta_r \cong \theta_1$, and simplifying Eq. (5), Eq. (6) can be found.

As seen from Eq. (6), negative sequence components have twice the fundamental angular frequency rotating in the opposite direction to that of positive sequence components. Once these negative sequence components are eliminated, it would be possible to achieve effective PLL which is free of unbalanced grid conditions.

$$\vec{V}_{abc} = \vec{V}_p + \vec{V}_n + \vec{V}_h \tag{1}$$

$$\vec{V}_{abc} = \begin{bmatrix} |V_p|\cos(\theta_{1p}) \\ |V_p|\cos(\theta_{1p} - 2\pi/3) \\ |V_p|\cos(\theta_{1p} + 2\pi/3) \end{bmatrix} + \begin{bmatrix} |V_n|\cos(\theta_{1n}) \\ |V_n|\cos(\theta_{1n} + 2\pi/3) \\ |V_n|\cos(\theta_{1n} - 2\pi/3) \end{bmatrix} \tag{2}$$

$$\theta_{1p} = \int w_1 dt + \theta_{1p_0} = \theta_1 + \theta_{1p_0} \tag{3}$$

$$\theta_{1n} = \int w_1 dt + \theta_{1n_0} = \theta_1 + \theta_{1n_0} \tag{4}$$

$$\vec{V}_{dq}^+ = |Vp|\begin{bmatrix} \cos(\theta_1 - \theta_r) \\ \sin(\theta_1 - \theta_r) \end{bmatrix} + |V_n|\begin{bmatrix} \cos(-\theta_1 - \theta_r) \\ \sin(-\theta_1 - \theta_r) \end{bmatrix} \tag{5}$$

$$\vec{V}_{dq}^+ = |Vp|\begin{bmatrix} 1 \\ 0 \end{bmatrix} + |V_n|\begin{bmatrix} \cos(-2\theta_1) \\ \sin(-2\theta_1) \end{bmatrix} \tag{6}$$

3 APLICATION OF LOW PASS FILTERING WITH SIMPLE MICROCONTROLLERS

As shown in previous section, negative sequence components introduce sinusoidal values having twice the angular frequency of the fundamental angular frequency. PLL methods introduced in literature proposed for solving unbalanced grid condition problem utilize IIR or FIR type digital filters that are capable of either attenuating these sinusoidal values by low pass filtering or shifting the phase angle with all pass filters to utilize new sinusoidal values for their PLL algorithms. Though the filtering methods used are quite successful, due to the extensive resource requirements of mathematical calculation for these digital filter types, application of these filters with standard simple microcontrollers becomes the limiting factor for overall performance of a low cost grid connected inverter. Therefore in this paper, instead of using an IIR or an FIR type digital filter, a less complicated method for low pass filtering has been used.

The low pass filter used in this paper is actually based on the operating principle of an analog low pass RC filter as shown by author in [17]. Theoretically, a differential equation is required for solving an RC circuit. The voltage difference between output and input divided by the value of R will define the capacitor current. Considering that the current flowing on the capacitor is constant for a sampling period, Eq. (7) and Eq. (8) can be written. If the capacitor is selected such that the voltage change in consecutive sampling instants is low enough then Eq. (9) can be written. By using a single constant term k that covers all the constant terms Eq. (10), Eq. (9) turns into Eq. (11). Eq. (11) is the core formula for the low pass filter used. By changing the value of k it would be possible to change the corner frequency of the filter itself. The block diagram representation of Eq. (12) is shown in Fig. 2.
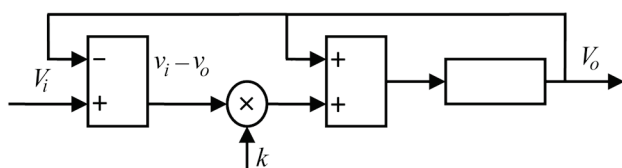

Figure 2 Block diagram representation of simplified RC filter algorithm

$$Q = C \times V = I \times T \tag{7}$$

$$V = \frac{I \times T}{C} \tag{8}$$

$$\Delta V_o = \frac{\Delta T}{R \times C} \times (v_i - v_o) \tag{9}$$

$$k = \frac{\Delta T}{R \times C} \tag{10}$$

$$\Delta V_o = k \times (v_i - v_o) \tag{11}$$

$$V_o' = V_o + k \times (v_i - v_o) \tag{12}$$

If constant k is selected as multiples of 2 then it would be possible to make the calculations much easier in a microcontroller used system. By taking $\Delta T = 50$ μsec, different corner frequency values have been calculated and shown in Tab. 1.

Table 1 RC time constant values and corresponding filter corner frequencies based on different values of k utilizing (10)

k	RC (msec)	*Filter Corner Frequency* (Hz)
1/16	0.8	5.62
1/256	12.8	1.64
1/4096	204.8	0.351

In Fig. 3, basic simulation results were shown by selecting RC values which are matching the corresponding RC time constant values in Tab. 1.
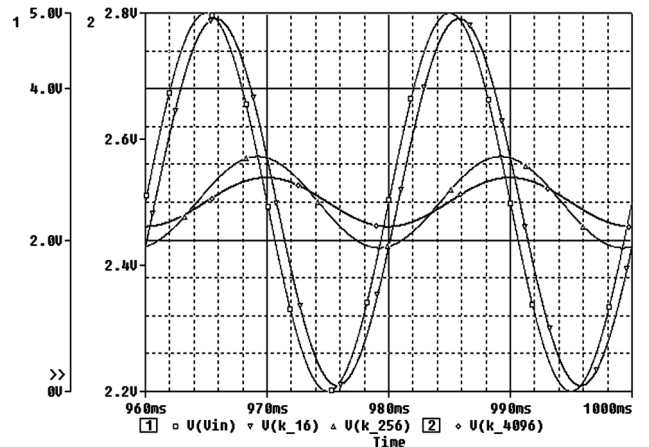

Figure 3 Simulation result of an RC filter for different RC time constants, V(k_16) represents k=1/16, V(k_256) represents k=1/256, V(k_4096) represents k=1/4096
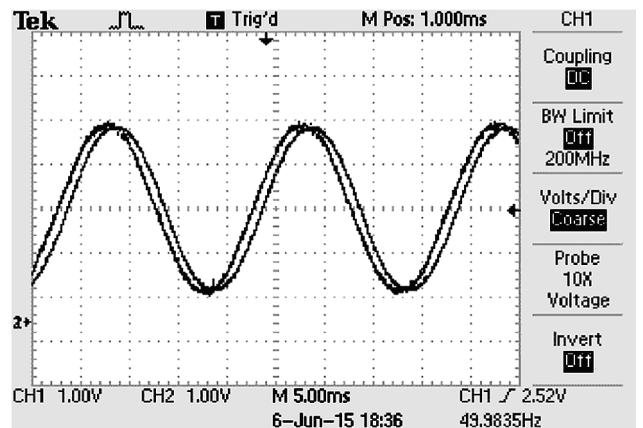

Figure 4 Experimental results of RC filter algorithm with microcontroller when k=1/16

In order to compare the simulation results with the results of the filter algorithm, a digital analog converter has been used to convert the digital filter output values into analog world signals. The actual application results which coincide with simulation results are shown in Fig. 4, Fig. 5 and Fig. 6.
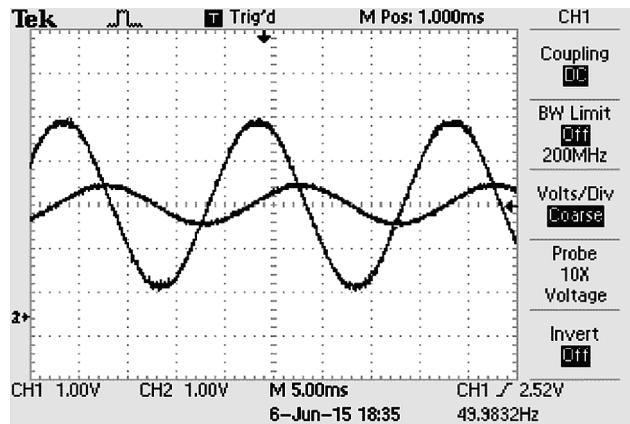

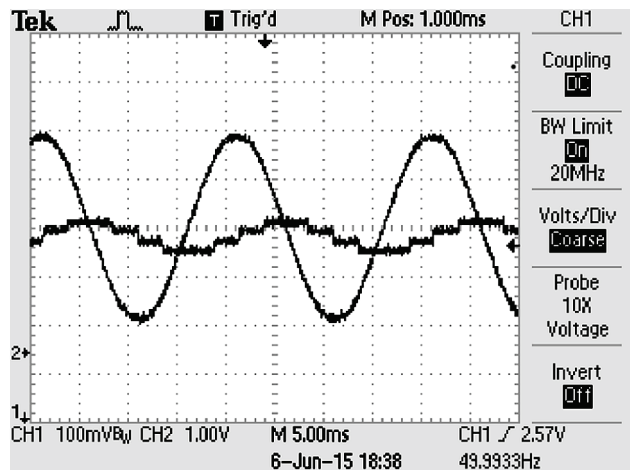**Figure 5** Experimental results of RC filter algorithm with microcontroller when k=1/256

Figure 6 Experimental results of RC filter algorithm with microcontroller when k=1/4096

4 EXPERIMENTAL RESULTS OF PLL ALGORITHM UNDER UNBALANCED GRID CONDITIONS BY USING A SIMPLE MICROCONTROLLER

Three phase input voltages have been applied to the measurement circuit which consist of isolation amplifiers and post amplifiers. Isolation amplifiers have differential outputs therefore post amplifiers have been implemented to have single-ended voltage level. In Fig. 7, unbalanced voltage levels at the analog digital converter of the microcontroller are shown. As seen in the figure, one of the sinusoidal input voltages has an amplitude value which is half of the amplitudes of the other sinusoidals so 50% of unbalance is present. The results gathered with SRF-PLL are not reliable under unbalanced grid conditions due to the presence of negative voltage sequence of the grid as explained in previous sections. Here, it can be seen that frequency locking could not be achieved with SRF-PLL.
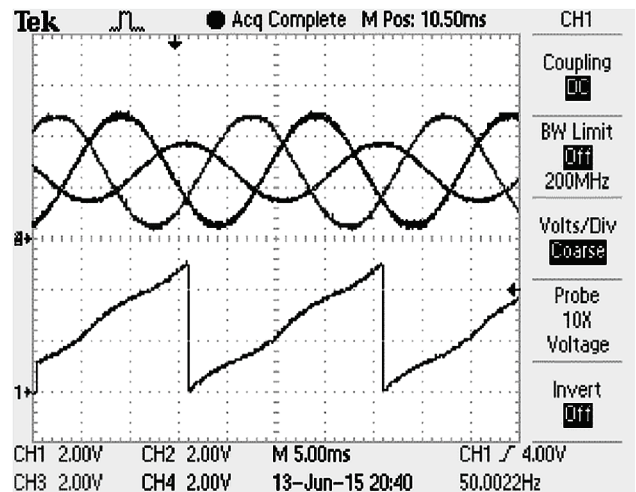

Figure 7 CH1: distorted locking of phase with SRF-PLL under unbalanced grid condition, CH2, CH3, CH4: input voltages
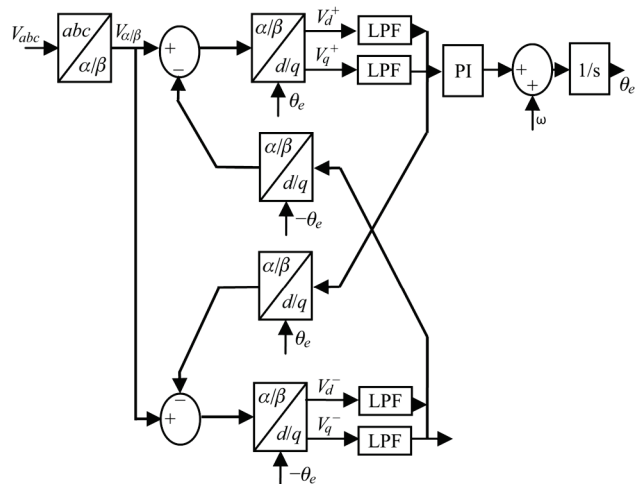

Figure 8 Block diagram representation of MRF-PLL

In order to gather the experimental results under unbalanced grid conditions, a PLL method which is attenuating the negative voltage sequence, such as MRF-PLL, has been used. Block diagram illustration of MRF-PLL is shown in Fig. 8.
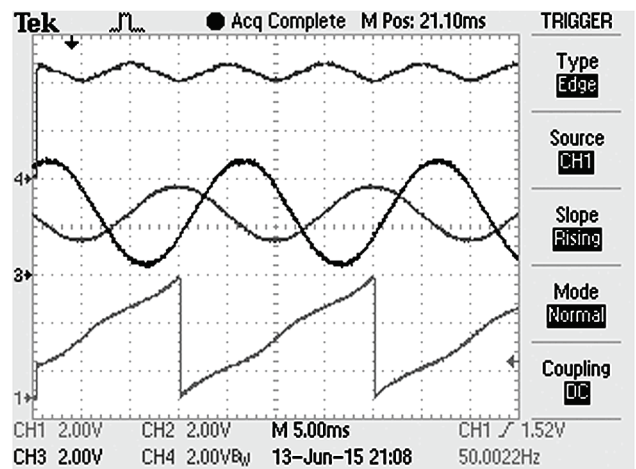

Figure 9 Before phase locked, CH1: detected phase information, CH2 and CH3: input phase voltages, CH4: positive sequence D component

Low pass filtering explained in previous section has been implemented into the algorithm used in the low cost microcontroller for MRF-PLL application under

unbalanced grid conditions. The microcontroller used is 78K0R/Ix3 Series 16 bit microcontroller having 50 ns of instruction execution time and hardware multiplier-divider. Any microcontroller having the same specifications could be used to get the same results.
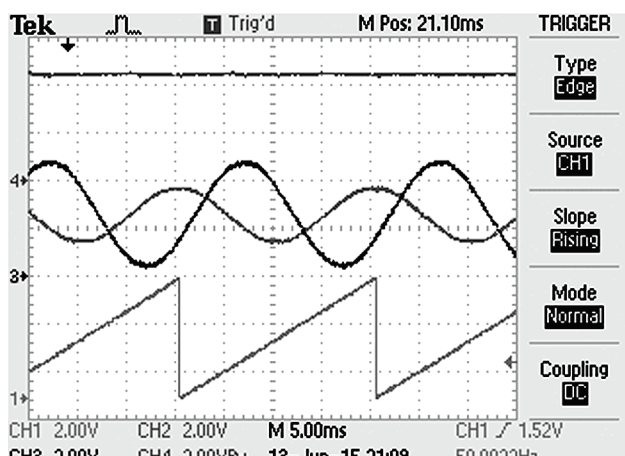

Figure 10 After phase locked, CH1: detected phase information, CH2 and CH3: input phase voltages, CH4: positive sequence D component
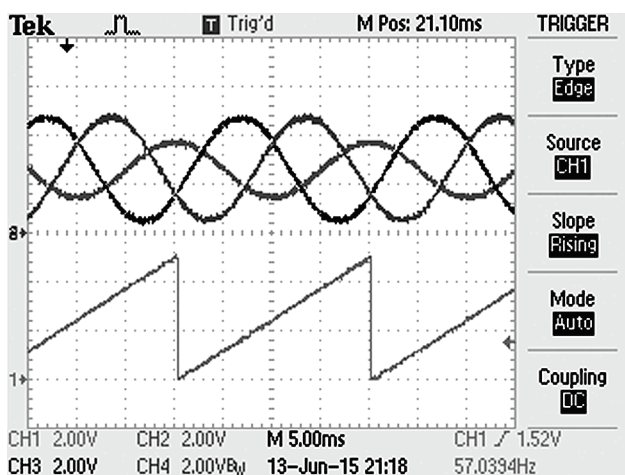

Figure 11 CH1: locked phase with MRF-PLL under unbalanced grid condition, CH2, CH3, CH4: input phase voltages

Fig. 9 illustrates positive sequence D component of input voltage along with the unbalanced two phases out of the three phases and the detected phase before the phase is locked. Before the detected phase settled to the final state, the effect of negative voltage sequence can be seen clearly. After phase is locked, phase information is free of the negative sequence components as shown in Fig. 10. Reliable grid matching under unbalanced grid conditions can be achieved with a low cost 16 bit microcontroller as shown in Fig. 11.

5 CONCLUSION

In order to solve the poor grid synchronization problem caused by the negative voltage sequence of unbalanced grid, effective PLL methods have been proposed and implemented in literature. The drawback of these methods is the complexity to apply with simple microcontrollers for low cost applications. In this paper, an easy to use low pass filter algorithm has been implemented in MRF-PLL method. The experimental

results have shown that at 20 kHz of sampling frequency, it is possible to detect the phase and frequency of the unbalanced grid by eliminating the negative sequence components. These results allow cost optimized grid connected inverter operating up to 20 kHz switching frequency to be designed using a simple 16 bit microcontroller without extensive resources.

6 REFERENCES

[1] Kim, Y., Kim, K., Kwon, B., & Choi, C. (2008). A Fast and Robust PLL of MCFC PCS under Unbalanced Grid Voltages. *2008 IEEE Power Electronics Specialists Conference,* 4712-4716. https://doi.org/10.1109/pesc.2008.4592713

[2] Lyons, J. & Vlatkovic, V. (2004). Power Electronics and Alternative Energy Generation. *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551),* 16-21. https://doi.org/10.1109/pesc.2004.13557052

[3] Kaura, V. & Blasko, V. (1997). Operation of a Phase Locked Loop System under Distorted Utility Conditions. *Proceedings of Applied Power Electronics Conference. APEC 96, 33*(1), 58-63. https://doi.org/10.1109/apec.1996.500517

[4] Golestan, S., Monfared, M., & Freijedo, F. D. (2013). Design-Oriented Study of Advanced Synchronous Reference Frame Phase-Locked Loops. *IEEE Transactions on Power Electronics, 28*(2), 765-778. https://doi.org/10.1109/tpel.2012.2204276

[5] Zhang, S., Chen, J., & Zhou, W. (2009). A Method for Electrical Network Voltage Compensation without PLL Based on Coordinate Transformation. In *International Conference on Electrical Machines and Systems* (pp. 2150-2153). IEEE. Retrieved February 2, 2009, from http://ieeexplore.ieee.org/document/4771101/3

[6] Hadjidemetriou, L., Kyriakides, E., & Blaabjerg, F. (2012). A New Hybrid PLL for Interconnecting Renewable Energy Systems to the Grid. *2012 IEEE Energy Conversion Congress and Exposition (ECCE), 49*(6), 2709-2719. https://doi.org/10.1109/ecce.2012.6342556

[7] Xiong, F., Yue, W., Ming, L., Ke, W., & Wanjun, L. (2010). A novel PLL for grid synchronization of power electronic converters in unbalanced and variable-frequency environment. *The 2nd International Symposium on Power Electronics for Distributed Generation Systems,* 466-471. https://doi.org/10.1109/pedg.2010.5545832

[8] Rodriguez, P., Pou, J., Bergas, J., Candela, J. I., Burgos, R. P., & Boroyevich, D. (2007). Decoupled Double Synchronous Reference Frame PLL for Power Converters Control. *IEEE Transactions on Power Electronics, 22*(2), 584-592. https://doi.org/10.1109/tpel.2006.890000

[9] Limongi, L. R., Bojoi, R., Pica, C., Profumo, F., & Tenconi, A. (2007). Analysis and Comparison of Phase Locked Loop Techniques for Grid Utility Applications. *2007 Power Conversion Conference - Nagoya,* 674-681. https://doi.org/10.1109/pccon.2007.373038

[10] Hoffmann, N., Lohde, R., Fischer, M., Fuchs, F. W., Asiminoaei, L., & Thogersen, P. (2011). A review on fundamental grid-voltage detection methods under highly distorted conditions in distributed power-generation

networks. *2011 IEEE Energy Conversion Congress and Exposition,* 3045-3052.
https://doi.org/10.1109/ecce.2011.6064179

[11] Sim, J., Kim, K., Son, R., & Oh, J. (2012). Ride-through of PMSG Wind Power System under the Distorted and Unbalanced Grid Voltage Dips. *Journal of Electrical Engineering and Technology, 7*(6), 898-904.
https://doi.org/10.5370/jeet.2012.7.6.898

[12] Jubayer, J., Mamun, R., Bin Ibne, M., Savisha, A., Syarizal Bin Zaina, C., & Tae Gyu, T. (2014). Evolution of Digitally Controlled Oscillators. *Technical Gazette, 21*(4), 897-902.

[13] Rodriguez, P., Teodorescu, R., Candela, I., Timbus, A., Liserre, M. & Blaabjerg, F. (2006). New Positive-sequence Voltage Detector for Grid Synchronization of Power Converters under Faulty Grid Conditions. *37th IEEE Power Electronics Specialists Conference,* 1-7.
https://doi.org/10.1109/pesc.2006.1712059

[14] Freijedo, F. D., Doval-Gandoy, J., López, Ó, &Acha, E. (2009). A Generic Open-Loop Algorithm for Three-Phase Grid Voltage/Current Synchronization with Particular Reference to Phase, Frequency, and Amplitude Estimation. *IEEE Transactions on Power Electronics, 24*(1), 94-107. https://doi.org/10.1109/tpel.2008.2005580

[15] Guo, X., Wu, W., & Chen, Z. (2011). Multiple-Complex Coefficient-Filter-Based Phase-Locked Loop and Synchronization Technique for Three-Phase Grid-Interfaced Converters in Distributed Utility Networks. *IEEE Transactions on Industrial Electronics, 58*(4), 1194-1204. https://doi.org/10.1109/tie.2010.2041738

[16] Gonzalez, O. L. & Buja, G. (2011). Novel PLL scheme for grid connection of three-phase power converters. *8th IEEE Symposium on Diagnostics for Electrical Machines, Power Electronics & Drives,* 372-377.
https://doi.org/10.1109/demped.2011.6063650

[17] Chapman, K. (2008). Digitally Removing a DC Offset: DSP without Mathematics. Retrieved October, 2008, from https://www.xilinx.com/support/documentation/white_papers/wp279.pdf

Contact information:

Mustafa Cem OZKILIC, PhD student
(Corresponding Author)
Yildiz Technical University,
Faculty of Electrical and Electronics,
Department of Electrical Engineering,
Davutpasa Campus, Esenler, İstanbul, Turkey
E- mail: mcozkilic@ohm.com.tr

Atiye Hulya OBDAN, Assistant Professor
Yildiz Technical University,
Faculty of Electrical and Electronics,
Department of Electrical Engineering,
Davutpasa Campus, Esenler, İstanbul, Turkey
E- mail: obdan@yildiz.edu.tr