Advanced Surface Texturing for Silicon Solar Cells

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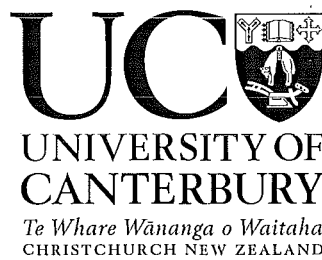
in

Electrical and Computer Engineering

at the

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UNIVERSITY OF
CANTERBURY
Te Whare Wānanga o Waitaha
CHRISTCHURCH NEW ZEALAND

University of Canterbury

6 April 2005

Dedicated
to
my parents,
Saravanamuthu Kumaravelu, Kamalavathi Kumaravelu
my wife,
Kamalini Kathir
and
my daughters
Shenpaha and Vishaka

iv

ABSTRACT

The multi-crystalline silicon (mc-Si) solar cell is considered to be one of the most promising cells capable of achieving high efficiency at low cost and high reliability. Improving solar cells efficiency using low cost materials requires careful design considerations aiming to minimise the optical and electrical losses. In this work plasma texturing was employed to reduce optical reflections from silicon surfaces well below 1%.

Plasma texturing is used to form light trapping structures suitable for silicon solar cells. Several plasma texturing methods are investigated and associated defects are analysed. Masked as well as mask-less texturing techniques are investigated. Conventional parallel plate Reactive Ion Etching (RIE), Inductively Coupled Plasma (ICP) and Electron Cyclotron Resonance (ECR) plasma system are used to compare the plasma induced defects in silicon. The influence of various plasma etch parameters on plasma induced defect is investigated. A correlation between the minority carriers lifetime and surface area increased by texturing is established.

Effective lifetime measurements using Quasi Steady State Photo Conductive (QSSPC) technique is mainly used to estimate the plasma induced defect in textured silicon substrates. Sinton lifetime tester is used to measure the effective lifetime of the substrates. The implied open circuit voltage is calculated from the lifetime data for textured substrates.

In this work low temperature photoluminescence spectroscopy is also used to analyse the defect caused by plasma on mc-Si substrates. Photoluminescence (PL) data is obtained using the 514.5 nm line of an Ar^+ laser as an excitation source. The luminescence is dispersed with SPEX 1700 spectrometer with a liquid nitrogen cooled Germanium detector.

Reflectance measurements are performed on textured surfaces using a purpose built integrating sphere attachment of a high accuracy spectrophotometer. Modelling is also performed using PV-optics software to compare the experimental and theoretical results.

Finally, silicon solar cells are fabricated with measured efficiency around 18% . The efficiency is estimated from the I-V characteristics data obtained using a calibrated halogen lamp and a HP semiconductor parameter analyser. Spin-on-dopant source as well as solid diffusion source is used to form the emitter junction of the solar cells fabricated on p-type silicon wafers. Multicrystalline silicon, CZ- silicon and FZ silicon wafers are used to fabricate solar cells in this thesis. The effect of single and double layer antireflection coatings on diffused reflections is also investigated.

PREFACE

This thesis describes research undertaken in the Department of Electrical and Computer Engineering at the University of Canterbury between March 2001 and November 2004. When I started this New Zealand's first silicon solar cell research from scratch, our laboratory was equipped with very limited facilities such as an old mask aligner, spinner, thermal evaporator and two new equipments, Reactive Ion Etcher and Atomic Force Microscope. Acquisition of tube furnace, Mask aligner, Sputterer with e-beam evaporator and a dicing saw helped improving the standard of this research. Thanks to the initiative of Mac Diarmid Institute for advanced materials and nanotechnology.

Being the first person to do solar cell research in the Micro electronic laboratory of our department, I gained useful experience in setting up fabrication processes and hopefully gained a good understanding of the tools. I'm grateful to my supervisor for giving me this great opportunity.

Aspects of the work described in this dissertation have been published as follows.

I) G.Kumaravelu, M.M.Alkaisi, D. Macdonald " The effect of surface area increase due to plasma texturing on the carrier lifetime of silicon solar cell substrates" , AMN2, Queenstown, New Zealand from 6-11 February 2005.

II) G.Kumaravelu, M.M.Alkaisi, D. Macdonald, J. Zhao, B.Rong, A. Bittar "Minority Carrier Lifetime In Plasma Textured Silicon Wafers For Solar Cells", *Solar Energy Materials and Solar Cells,* In Press, *Available online from 21 November 2004*

III) G.Kumaravelu, M.M.Alkaisi, D. Macdonald, J. Zhao, B.Rong, A. Bittar "Minority Carrier Lifetime In Plasma Textured Silicon Wafers For Solar Cells", Scell2004 conference proceedings, Badajoz, Spain, May13-15,2004.

IV) G. Kumaravelu, M. M. Alkaisi, A. Bittar, D. Macdonald, and J. Zhao, "Damage Studies In Dry Etched Textured Silicon Surfaces," Current applied Physics, vol. 4, pp. 108 -110, 2004.

V) G. Kumaravelu, M. M. Alkaisi, and A. Bittar, "Texturing for silicon solar cells using reactive ion etching technique," 29th IEEE Photovoltaic Specialists Conference, New Orleans, p. 258, 2002.

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Overview

Solar cells convert sunlight directly into electricity using the photovoltaic effect. They are a promising technology for satisfying current and future energy demands in a sustainable and environmentally-friendly way. The first commercial use of solar cells was in space applications for powering satellites in the late 1950s.
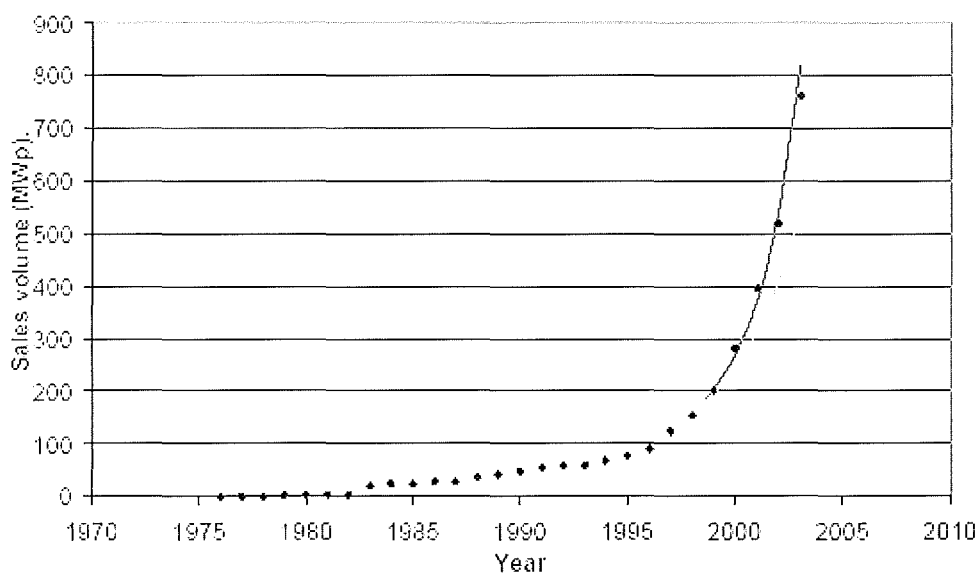
Figure 1-1: Sales volume of silicon solar cells till 2003 [1]

Today, the terrestrial market for solar cells greatly exceeds that for space applications, with a variety of end uses including grid connected systems, consumer products and for remote area power supply. This rapidly expanding market calls for

advanced technologies and devices capable of yielding a higher performance at lower cost.

To maximize the efficiency of solar cells, researchers have attempted various solar cell structures aiming to maximize the absorption of incident photons and collection of photogenerated carriers [2, 3]. Solar cell design involves the specification of the parameters of a solar cell structure in order to maximize efficiency (given a certain set of constraints). For example, in commercial solar cells, a constraint which must be considered is the cost of fabricating a particular solar cell structure. In contrast, for a high efficiency laboratory type solar cell, the objective is often to maximize efficiency without significant regard to cost. Cost of the solar cells could be reduced by choosing low priced substrates such as multicrystalline silicon. Multicrystalline silicon solar cells account for approximately 62% of the production volume for 2003, approximately 744MW [4] . Figure 1-1 shows the rapid increase in solar cell sales in the 3 years ending 2003. Multicrystalline silicon cell technology continued to take market share, now almost two-thirds of monocrystalline silicon market. Multicrystalline silicon (mc-Si) solar cell with efficiency 14.48% has already reached the market [5].

Historically, higher efficiencies have been achieved by minimization of optical and electrical losses of silicon solar cells. Combining low cost material with high light trapping features, the price of solar cells could be reduced.

One approach is through surface texturing of the silicon wafer to reduce reflections from front surfaces while maintaining high minority carrier lifetime by minimizing process induced defects [6]. Already laboratory mc-Si cells have reached 20.3 % efficiency with plasma texturing combined with wet chemical etching [7].

Texturing is very effective in reducing reflections and it is especially important for thin films, multicrystalline materials and for capturing long wavelength light. Surface texturing for enhanced absorption in Si has been obtained historically by creating randomly distributed pyramids [8] using anisotropic etchants, but this preferential wet etching works best on single crystalline silicon because of its crystallographic orientations. These wet etching techniques are not satisfactory for multicrystalline silicon (mc-Si) solar cells because of the random grain orientation. Also it places a limitation on the growth of solar production capacity due to the tremendous amount of material, water and chemicals

that need to be consumed. Mechanical texturing techniques require wafers with sufficiently thick material for mechanical stability. These methods are especially not applicable for thin, warped, and fragile materials. Plasma assisted processing has the potential to be an alternative method for industrial texturing of monocrystalline, multicrystalline and thin film based solar cells.

1.2 General features of solar cells

Some of the primary factors present in high efficiency designs are

1. Good light trapping to maximise photo capturing efficiency by minimising reflection.

2. Well passivated surfaces to minimise surface defects and recombination problems.

3. High minority carrier lifetime in the substrate material to enhance collection efficiency and reduce bulk recombination.

4. Thin substrates to get high open circuit voltage [9]. An optimum silicon solar cell with light trapping and very good surface passivation is about 100 μm thick. However, thickness between 200 and 500μm are typically used, partly for practical issues (such as in manufacturing and handling thin wafers) and partly for surface passivation reasons.

5. High quantum efficiency in the front doped region for blue and infrared resposnse.

6. Low series resistance for higher fill factor.

7. Low grid shadowing to minimise light losses.

8. High shunt resistance to increase open circuit voltage and fill factor.

This thesis concentrates mainly on improving .light trapping using plasma texturing while minimizing the plasma induced defects.

1.3 Solar cell efficiency

The power conversion efficiency of a solar cell is given by

$$\eta = \frac{FF \ J_{SC} V_{OC}}{P_{in}} \qquad \text{1-1}$$

where P_{in} is the incident power, FF is the fill factor, J_{sc} is the short-circuit current density and V_{oc} is the open circuit voltage. All of these three parameters (FF, J_{sc}, V_{oc}) should be maximised to improve the efficiency of a solar cell.

However, these three parameters are correlated to some degree as indicated by the following equation.

$$FF_o = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1} \qquad \qquad 1\text{-}2$$

where FF_o in Equation 1-2 is the ideal fill factor, v_{oc} is the normalised voltage,

$$v_{oc} = \frac{qV_{oc}}{nkT} \qquad \qquad 1\text{-}3$$

where n is the cell ideality factor. k is Boltzman's constant, V_{oc} is the open circuit voltage, T is the absolute temperature and q is the electronic charge.

The actual cell fill factor also depends on the cell's series resistance and shunt resistance. However, all well designed and processed high efficiency single crystalline silicon solar cells should have fill factors very close to FF_o obtained from Equations 1-2 and 1-3.

The open circuit voltage also depends on the short circuit current density J_{sc} as

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_{sc}}{J_o} + 1\right) \qquad \qquad 1\text{-}4$$

where J_o is the saturation current density.

The saturation current density J_o, is given by the following Equation [8]

$$J_0 = \left(\frac{qD_e n_i^2}{L_e N_A} F_P + \frac{qD_h n_i^2}{L_h N_D} F_N\right) \qquad \qquad 1\text{-}5$$

Where n_i is the intrinsic carrier concentration, N_A and N_D are the accepter and donor concentrations. F_P and F_N are coefficients which incorporate the effect of surface recombination[8].

$$F_N = \frac{S_p \cosh(W_N / L_P) + D_P / L_P \sinh(W_N / L_P)}{D_P / L_P \cosh(W_N / L_P) + S_p \sinh(W_N / L_P)}$$ 1-6

$$F_P = \frac{S_n \cosh(W_P / L_n) + D_n / L_n \sinh(W_P / L_n)}{D_n / L_n \cosh(W_P / L_n) + S_n \sinh(W_P / L_n)}$$ 1-7

where S_p and S_n are the surface recombination velocities at the respective surfaces. W_N and W_P are widths of the n-type and p-type regions and L_n and L_p are diffusion length of n and p type carriers.

Equation 1-4 shows that V_{oc} weakly depends on J_{sc}. Actually when J_o is low, J_{sc} will tend to be high due to lower recombination inside the cell. This will enhance V_{oc} as given by Equation 1-4.

Hence, V_{oc} is experimentally the most important parameter to be optimised first for a solar cell technology, because when optimising V_{oc}, the limiting fill factor FF_o is automatically optimised and it is likely that J_{sc} is also optimised. When the carrier recombination is high, J_o is high, and V_{oc} is low.
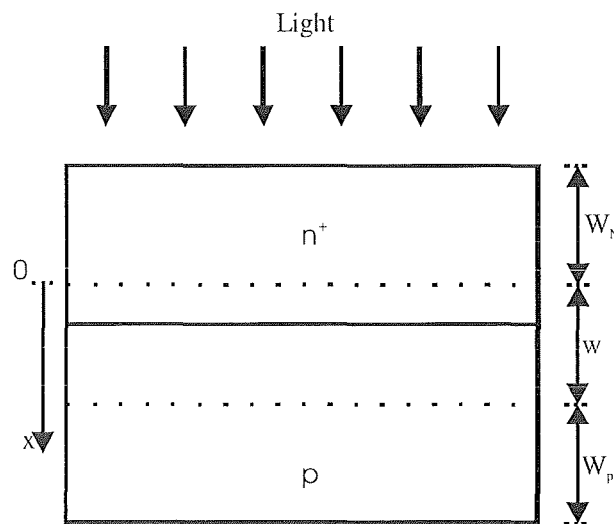
Figure 1-2: A typical n⁺ - p solar cell structure defining important dimensions.

The short circuit current density depends on the minority carrier diffusion lengths and will limit the cell efficiency when the cell dimensions are much larger than these diffusion

lengths. For an n$^+$- p type cell, as shown in Figure 1-2, it can be approximately expressed as

$$J_{sc} = q \int_{-Lp}^{w+L_n} G(x)dx \qquad\qquad 1\text{-}8$$

where $G(x)$ is the minority carrier generation rate, x is the position from the junction, w is the width of the junction depletion region, L_p and L_n are the minority carrier diffusion lengths in the emitter and the base regions, determined by recombination rates within the cell. The position $x=0$ is at the front edge of the depletion region. The active region of a cell is the junction depletion regions. J_{sc} depends on w, L_n, L_p and the location of the active region.

In order to collect all the light-generated carriers at the junction, surface and bulk recombination of light generated carriers must be minimized. For conditions commonly encountered in silicon solar cells, two approximations required for total current collection and they are:

- The carrier must be generated within a diffusion length of the junction.

- In the case of a high localized recombination site (such as surface recombination or a grain boundary) the carrier must be generated closer to the junction than to the recombination site. If the recombination is less severe, as is the case when the surface is passivated, carrier collection will extend closer to the surface,

1.4 The aim of this project

The aim of this project is to develop a plasma textured light trapping structure for silicon solar cells with minimum reflection and defect density. In this project various plasma texturing methods will be investigated and the associated defects will be studied so that they could be minimized in future. Even though the ultimate goal of this study is to apply the plasma texturing techniques to multicrystalline silicon substrates, high quality float zone silicon substrates will be used to study the plasma induced defects accurately. In particular this study will investigate:

1. The plasma induced damage caused by various gases.
2. The effect of various etching mechanism on plasma induced defects.

1.5 Thesis summary

- **Chapter 1: Introduction**

  This chapter briefly introduces the principles of silicon solar cell, main parameters that affect the cell performance and current trends in silicon solar cell market. Also it mentions the motives and aims of this project.

- **Chapter 2: Experimental techniques**

  Chapter 2 describes experimental techniques involved in the fabrication of solar cells and measurements performed on the silicon substrates. Fabrication techniques include optical lithography, plasma texturing (RIE, ICP and ECR), emitter junction formation by diffusion and material deposition techniques such as electron beam evaporation, thermal evaporation, sputtering and PECVD Si_xN_y. Measurement techniques include reflectance, minority carriers lifetime, photoluminescence, roughness analysis by atomic force microscopy and finally I-V characteristic of fabricated solar cells.

- **Chapter 3: Surface texturing**

  The plasma texturing methods including reactive ion etching using SF_6/O_2, various etch parameters and the scanning electron microscope (SEM) images of various textured structures are shown in Chapter 3.

- **Chapter 4: Minority Carriers Lifetime Measurements**

  Chapter 4 describes the theory associated with the carrier lifetime and the minority carrier lifetime measurements and their interpretations on various plasma textured silicon substrates.

- **Chapter 5: Photoluminescence (PL) Analysis**

  This chapter presents the photoluminescence measurement data mainly on plasma textured silicon substrates and discuss the possible cause of the PL peaks appearing in the plasma textured mc-Si substrates.

- **Chapter 6: Light Trapping and Reflection Control**

  Chapter 6 shows the reflectance measurements on various textured surfaces and antireflection coatings. Textured surfaces include maskless textured black silicon,

optically optimised honeycomb-like cone-type and hole-type plasma textured silicon substrates. It also shows the reflectance measurements of single and double layer antireflection coatings. Modelling using PV-OPTICS software has also been utilized to optimise the light trapping structures.

Chapter 7: Solar cell fabrication

The fabrication process and characterisation of various solar cells include spin on dopant and solid diffusion source solar cells for textured as well as untextured substrates are described in Chapter 7.

- **Chapter 8: Conclusions and Recommended future work**

Chapter 8 gives the conclusions and recommendations for future work.

CHAPTER 2

EXPERIMENTAL TECHNIQUES

2.1   Introduction

A number of experimental techniques were used in this work for surface texturing as well as cell fabrication and characterization. This chapter discusses some of the main techniques of relevant interest involved in fabrication as well as characterisations. Fabrication techniques such as optical lithography that was used to define the etch masks, reactive ion etching and other plasma etching techniques that were used for pattern transfer following the lithography steps, metal deposition techniques such as physical evaporation, sputtering, electron beam evaporation, diffusion of doping elements such as Phosphorous and Boron are described in this chapter. Characterisation techniques such as atomic force microscopy that is used to investigate submicron features, the carrier lifetime measurement techniques using Sinton's lifetime tester and finally the I-V characterisation technique for silicon solar cell are also given in this chapter.

2.2   Pattern Definition Techniques

2.2.1   Introduction

Optical lithography is the process of transferring patterns of geometric shapes on a mask to a thin layer of light-sensitive material called photoresist covering the surface of the substrate.   There are basically two optical exposure methods: shadow printing and projection printing [10, 11]. Shadow printing may have the mask and wafer in direct contact with one another as in *contact printing*, or in close proximity as in *proximity printing*. The shadow printing is faster and cheaper than projection printing. Projection is limited by the diffraction effect while contact printing is limited mainly by mask

contamination and mask wearing. To minimise the mask damage, the proximity contact is used in shadow printing.
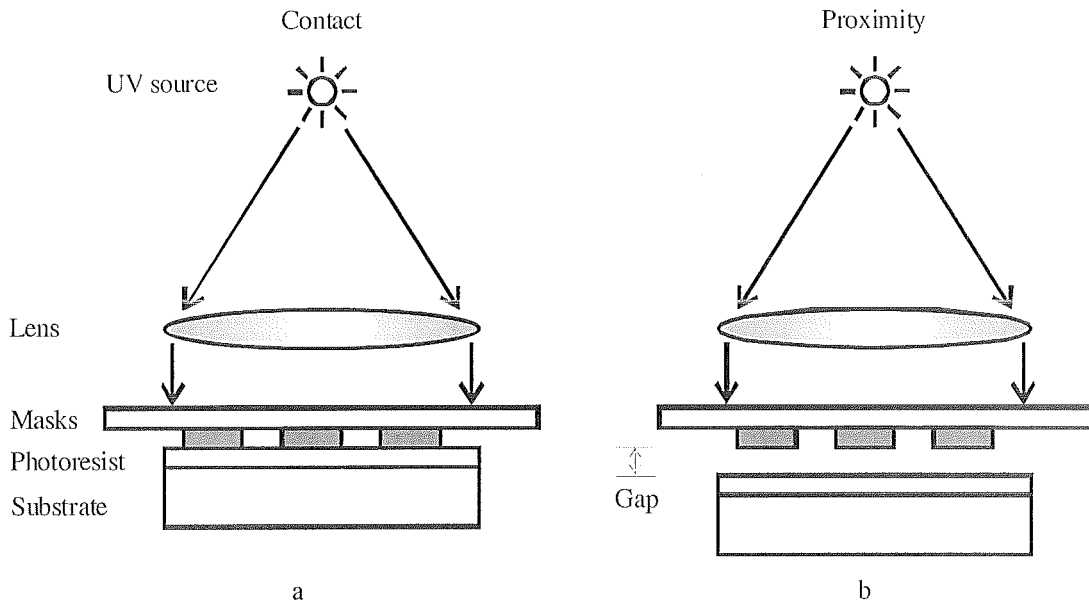
Figure 2-1: Schematic of optical printing modes. (a) Masks and wafers are in contact printing mode. (b) Masks and wafers are in proximity printing mode.

In shadow printing, the minimum linewidth that can be printed is roughly given by the following Equation 2-1.

$$l_m \cong \sqrt{\lambda g}$$

2-1

where λ is the wavelength of the exposure radiation and g is the gap between the mask and the wafer and includes the thickness of the resist.

A new Karl Suss MA6 mask aligner was used in most of my work. It is capable of performing several shadow printing modes such as Low vacuum, high vacuum, proximity, soft and hard contact with a resolution of as low a 0.6 μm. The Karl Suss MA6 contact aligner is equipped with a 350 W lamp house and Suss diffraction reducing optics which produces exposure wavelengths between 350 and 450 nm. With a deep UV source, it can produce an exposure wavelength of 248 nm.

2.2.2 Mask making

Chrome-on-quartz masks for optical lithography were designed using L-Edit computer program and were made using the facility at Industrial Research Limited, Wellington. Masks for larger features (20-100 µm) such as emitter contacts for solar cells were made transferring the patterns on a chrome plated quartz plate using contact printing method. But, masks for smaller features (2-10 µm) such as texturing patterns were made using step and repeat method.
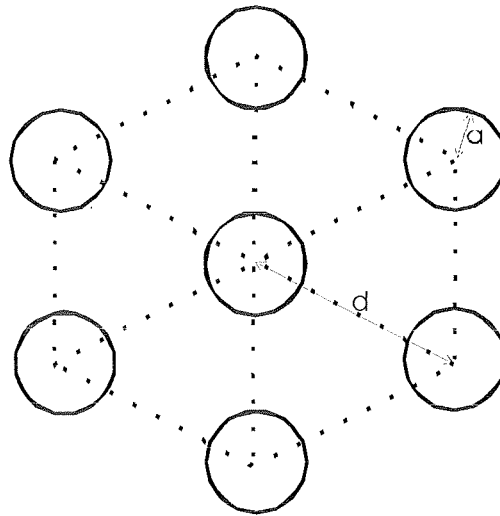
Figure 2-2: Honeycomb structure mask of circular holes or dots of radius a and pitch d.

Optimised surface texturing structures were achieved from hexagonally arranged circular holes or dots of radius a and pitch d as shown in the Figure 2-2. Typically a is in the range of 2-8 µm and d is in the range of 3-10 µm.

2.2.3 Pattern transfer techniques

In the initial part of this work, hole type texturing was done using subtractive pattern transfer scheme shown in Figure 2-3 (a). In this method we used Nichrome, Chrome or Aluminium as etch mask which was defined using wet etching method. Pillar type texturing was done using additive pattern transfer scheme shown in Figure 2-3 (b). Thick photoresist such as S4620 was used as etch mask for SF_6 plasma texturing in the latter

part of this work. The thickness of this resist is 6-10 μm depending on the spinning speed. Photoresist etch mask eliminates the metal evaporation, lift off / wet etch steps and save time and cost.

Silicon Wafer
Nichrome Layer(40nm)
Photo resist (500nm)
Broad band UV light
Mask
Exposed PR
Developed PR
Nichrome Layer
After Wet Etching
After Lift Off
After RIE

a   b
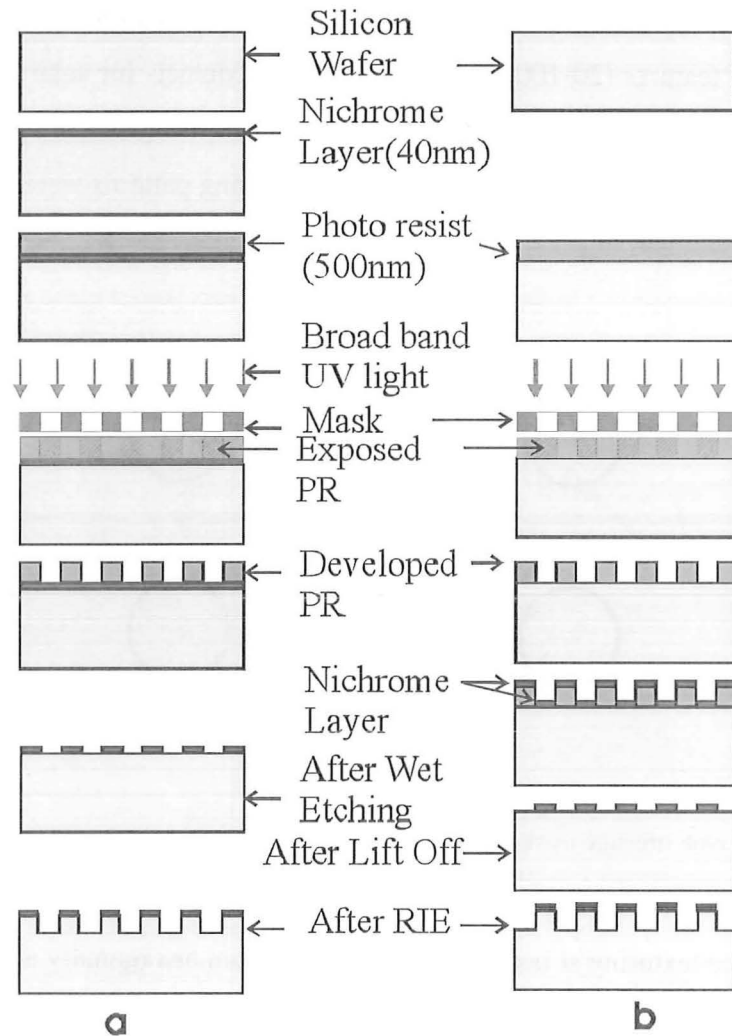
Figure 2-3: Schematic of the pattern definition and pattern transfer processes (a) Subtractive pattern transfer scheme used for the hole type structure.(b) Additive (lift-off) technique used for the column (or cone) type structure

2.3   Reactive Ion Etching (RIE)

Reactive ion etching was mainly used to form light trapping structures for silicon solar cells. Masked as well as mask-less methods were employed to texture the silicon surface. RIE demonstrate good control over etch profiles which is important in this application as anisotropic steep sidewall structures, which are slightly undercut, are required for successful light trapping surfaces. The principle of RIE, or dry etching as it is also known,

is the removal of material via a combination of physical bombardment and chemical reactions. The main advantage of RIE over the wet etching technique is the increased control over the etch profile. A number of parameters such as pressure, temperature and plasma power can be adjusted to control the anisotropy of an etch as well as various passivation mechanisms available through the choice of gas etchants. For a dry technique there are fewer waste products to dispose of and high throughput can be obtained in the case of the photovoltaic manufacturing industry.

2.3.1 Principle of Reactive Ion Etching

Reactive ion etching is a plasma etch process that combines controlled energetic ion bombardment with chemically reactive interactions to achieve high selectivity and a highly anisotropic etch. There are number of different etching configurations. The parallel plate electrode RIE is most common, and more recently high ion density reactors have become available such as electron cyclotron resonance (ECR) reactors and inductively coupled plasma (ICP) reactors. They are all based on the same basic principles, however, the high ion density reactors are configured to achieve higher ionisation densities compared to the parallel plate RIE. Higher densities of ion at lower pressures increases etch rates, while still maintaining a highly anisotropic etch.

Figure 2-4 shows a typical block diagram of the Oxford Plasmalab 80 Reactive Ion Etcher used for most of this work. In RIE a plasma is ignited by the application of radio frequency (RF) energy, typically at 13.56MHz. This promotes ionization of the constituent atoms and molecules in the process gases to create a plasma. This is essentially an electric discharge process. The plasma consists of reactive radicals, as well as a large proportion of neutral species. Of the reactive species, the majority of the positively charged species are singly ionised atoms or molecules, while the majority of the negatively charged species are electrons. The plasma appears to glow owing to photon emission during electron recombination process, with colours characteristic to the different gases. The higher mobility electrons are able to diffuse more through the plasma, recombining on the chamber walls. In the region immediately adjacent to the chamber surfaces, a sheath region forms. This is an area of low charge density created by the

recombination. As the electrons are able to diffuse more quickly in the plasma, a higher concentration of positive charge remains in the plasma.

The sheath plays a major role in etching. Because it has a low charge density, large fields can develop that accelerate positive ions across the sheath and onto the sample. Figure 2-5 shows how the electrical potential is distributed in the chamber for a simple parallel plate electrode system. The cathode becomes negatively biased during the etching process. This is a direct result of the higher mobility of the electrons over the positively charged ions. During the positive half of the RF cycle, negative ions are attracted to the cathode, while on the negative half of the RF cycle, positive ions are attracted. Initially, more electrons impinge on the cathode than positive ions, causing the cathode to take on the negative bias. This in turn means that there is a reduced percentage of the cycle when the cathode is more positive than the plasma potential.
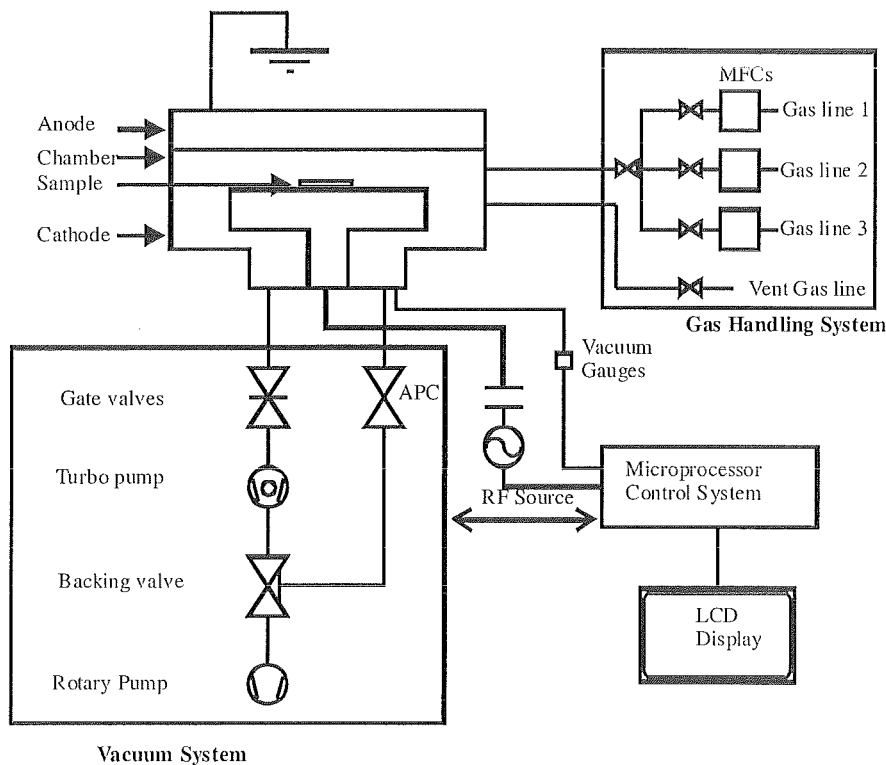
Figure 2-4: Block diagram of the Oxford Plasmalab 80 Reactive Ion Etching system

A steady-state is reached, when the number of electrons equals the number of ions hitting the cathode. The DC voltage of the cathode at the steady state conditions is called the

self–bias voltage, or bias voltage (V_b); it gives important information as to the energy of the impinging ions. A V_b large enough to obtain an anisotropic etch is generally desirable [12].
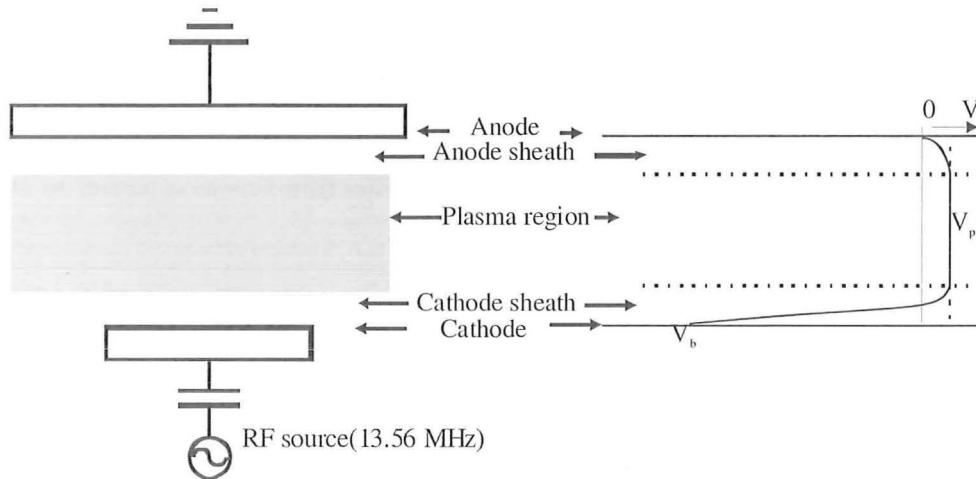
Figure 2-5: The electrical potential distribution across the discharge region of RIE

A much larger voltage is apparent over the cathode sheath, compared to the anode sheath as shown in Figure 2-5. This is a consequence of the anode area being much larger than the cathode, creating a larger capacitance and hence a lower voltage. This is desirable as larger fields, and therefore more energetic bombardment occurs on the samples placed on the cathode.

2.3.2   Reactive Ion Etching Mechanisms

Reactive Ion Etching can be divided into four basic etching mechanisms [13].

a. Sputtering: Sputtering is a low pressure process that creates a long mean free path for radicals. The radicals that cross the sheath are very energetic, and collide with the sample at predominately normal incidence due to the small number of collisions. The energetic nature of the collision causes surface material to be ejected. This is the least selective of the etching processes, as the etching is due to physical bombardment as opposed to a chemical process. Vertical etching can be achieved using this process.

b. Chemical gasification: Chemical gasification on the other hand is a chemical process. The plasma provides the reactive etchant species which chemically react with the

substrate to be etched. It is a very selective process, sensitive to differences in bonds and the chemical consistency of the material. It is similar to wet-etching in that it results in isotropic profiles

c. Energetic ion-enhanced chemistry: Energetic ion-enhanced chemistry works by having two species in the plasma, etchants and inhibitors. Normally the etchant and substrate would react and etch iostropically. However, the inhibitor forms a thin film in vertical surfaces that see little or no bombardment. This film acts as a barrier to etching, improving the anisotropy of the process, and

d. Inhibitor ion enhanced chemistry: This mechanism is mainly utilized for texturing highly anisotropic vertical structures for light trapping surfaces.

The dominance or otherwise of each of the different processes is dependent on a number of parameters, including the material to be etched, the process gases, pressure, RF power & frequency, temperature, and, etcher configuration.

2.3.3 Machine description

RIE was performed using and Oxford Plasmalab 80 system. It has a basic parallel plate electrode configuration with a cryogenic sample stage and a temperature range of -150° C to 200° C. A schematic of this system is shown in Figure 2-4. The RIE system can be divided into four subsystems: the chamber where the etching takes place with its RF electrode, the gas-handling system, the vacuum system, and the controller.

In the aluminium etching chamber there are two parallel plate electrodes; the upper electrode or anode that is grounded, and the lower electrode or cathode that is the drive electrode supplied with RF energy (at 13.56 MHz). The cathode is 200 mm in diameter, while the upper anode encompasses most of the chamber lid, approximately 280 mm in diameter. The lower electrode's temperature can be controlled with liquid N_2 to cool the electrode down to -150° C and has a heating element to heat the electrode to a maximum of 200° C (these are not indicated in Figure 2-4).

Process gases and a vent gas are supplied to the chamber. There are three process gas lines, allowing a maximum of three gases to be used simultaneously. In turn these three gas lines are connected in parallel to up to three gas cylinders. Available gases include SF_6, CHF_3, O_2, N_2 and Ar. Mass flow controllers (MFCs) control the flow-rate through each of the gas lines. The vent line vents the chamber with nitrogen has to bring the chamber back to atmospheric pressure to allow loading and unloading of samples.

The vacuum system consists of a two stage pumping system to evacuate the chamber as well as to control process pressures during etching. Prior to etching, the chamber pressure is lowered to a base pressure, typically lower than $7x10^{-5}$ Torr, to reduce contaminant species in the chamber. A rotary pump acts as the roughing pump to lower the pressure from atmospheric, providing the first stage of vacuum. A turbomolecular pump then lowers the chamber pressure further and can achieve pressure of around 10^{-8} Torr. The rotary pump backs the turbomolecular pump through backing line. During the etching process, the gate valve is shut and all process gases are removed via the rotary pump, with the automatic pressure controller (APC) valve maintaining the process pressure. The chamber pressure is monitored via two gauges, a capacitance manometer gauge for measuring relatively high pressure such as during etching, and a penning gauge for measuring low pressure such as the base pressure.

The control system is based on a microprocessor based control module. The user can specify pre-loaded recipes or set process parameters manually. The control module co-ordinates the operation of the vacuum system valves to control pumping and to set process pressures. It operates the gas valves and MFCs for controlling the gas inputs, as well as controlling the temperature of the cathode, and the application of RF power and etch time.

2.4 Inductively coupled plasma (ICP) etching.

Unlike the planer reactors, where the RF power is coupled capacitively, ICP reactors make use of an inductive coupling. In this case, the plasma is inductively heated by the electric fields generated by a coil wrapped around the discharge chamber. These systems typically operate at a frequency of 13.56 MHz.
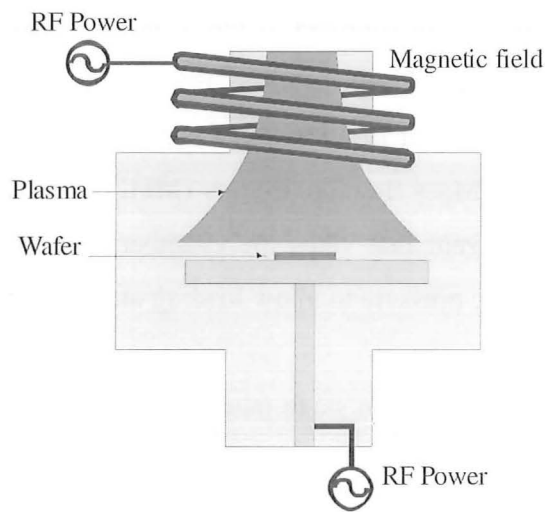
Figure 2-6: Schematic diagram of inductively coupled plasma reactor.

The drawback of the RIE system is that the energy of the bombarding ions is coupled to the dissipated power, which hampers control of ion bombardment. A way to overcome this is by changing the frequency of the source power [14]. At high frequencies, a low voltage is required for the same power. This results in independent of bias control. An important advantage of RF discharge over other discharges is that they are relatively easy to scale up to larger dimensions [14].

Another disadvantage of RIE is the relatively low plasma density. Source configuration like ECR and ICP shows high plasma densities. However, ECR source configuration is much more complex than that of ICP.

Figure 2-6 is the schematic drawing of an ICP reactor. The main difference between the two systems is that ICP has a source power separate from chuck power. The ICP plasma can create low energy ions, which is expected to cause less damage and at the same time has high ion current density. Secondly, the magnetic field of ICP reflects electrons to plasma, which collide with gas molecules to generate high density of charged radicals and high ion current density, and confines the plasma by keeping it away from the chamber wall. All these facts make sure that ICP has a high ion density and high reactive species content.

The main difference between ICP and RIE systems is, ICP uses Magnetic field but RIE does not use magnetic field.

2.4.1 Bosch process using ICP

A typical Bosch process mechanism is shown in Figure 2-7. Very high degree of anisotropic sidewall could be achieved through Bosch process. Sidewall passivation and etching are performed in alternative cycles.

Isotropic etching

Directional deposition

Isotropic etching

Directional deposition
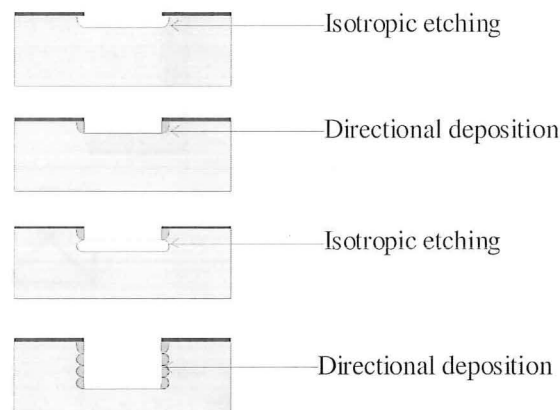
Figure 2-7: Very high degree of anisotropic etching of Bosch process. Sidewall passivation and etching are performed in alternative cycles.

To obtain anisotropic profiles, the process makes use of two alternating plasmas. The first plasma (SF_6, in this case) etches the silicon iostropically, the second plasma (C_4F_8, in this case) subsequently deposits a polymer layer to act as etch inhibition layer (in the next cycle) on the sidewalls of the etched structure. This cycle continues till the required depth is etched.

2.5 Electron Cyclotron Resonance (ECR) plasma etching
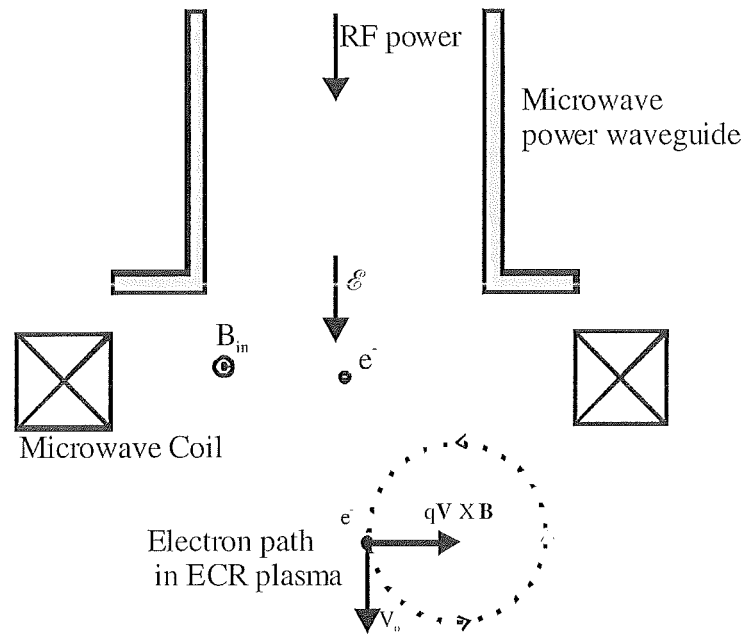
Figure 2-8: In ECR plasma, an alternating field causes the electrons to move in circular orbits, dramatically increasing the ion density.

In ECR, a discharge is produced by microwave excitation at 2.45 GHz. When a magnetic field of B = 875 Gauss is applied, resonance between the cyclotron motion of the electrons in the magnetic and microwave field occurs. Electrons at resonance efficiently convert microwave energy into dissociation of gas species. The wafer to be etched is placed inside the discharge chamber and can be rf or dc driven to control the etching process. This is not possible in conventional RIE process.

2.6 Material Deposition Techniques

The main deposition techniques are either Physical Vapour Deposition (PVD) or Chemical Vapour Deposition (CVD). PVD method can be divided into two sections known as thermal evaporation and sputtering. In our work, sputtering and thermal evaporation techniques using resistive heating source as well as an electron-beam evaporation system were used for depositing metals such as titanium, palladium, silver and aluminium. A newly acquired EDWARDS Auto 500 RF/DC sputtering system was

used for sputtering and e-beam evaporation. For depositing silicon Nitride, Plasma Enhanced Chemical Vapour Deposition (PECVD) was used.

2.6.1 Resistive heating method

Thermal evaporation represents one of the oldest thin film deposition techniques. Evaporation is based on the boiling off of a heated material and condensation onto a substrate in a vacuum. In our evaporator, metal is evaporated by passing a high current through a highly refractory metal containment structure. Tungsten was mainly used throughout this work. An alumina coated molybdenum boat was also used in few cases as it does not wet metals such as aluminium and hence prevents spilling. This is called resistive heating evaporation method. Bultzar evaporator, which is capable of achieving very low vacuum in the order of 1×10^{-7} bar, was used.

2.6.2 Electron beam evaporation method
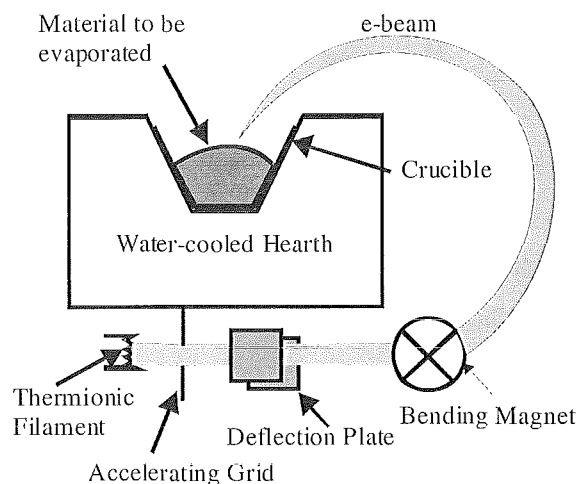
Figure 2-9 : Electron beam evaporation system. The electron beam evaporates the target material only.

In the e-beam mode of operation a high-intensity electron beam is focussed on the target material, that is, it is placed in a recess in a water cooled copper hearth. As shown in Figure 2-9, the electron beam is magnetically directed onto the evaporant which melts locally. In this manner, the metal forms its own crucible and the contact with the hearth is

too cool for chemical reactions, resulting in fewer source-contamination problems than in the case of resistive heating. One disadvantage of e-beam evaporation is that the process might induce X-ray radiation damage and possibly some ion damage on the substrate. Because this is at voltage > 10 kV, the incident electron beam will cause X-ray emission. This X-ray damage might induce some electronic defects and result in reduced silicon solar cell efficiency [15].

2.6.3 Sputtering

Sputtering is preferred over evaporation in many applications due to a wider choice of materials to work with, better step coverage, and better adhesion to the substrate.

During sputtering, the target, connected at a high negative potential, is bombarded with positive argon ions created in a plasma. A plasma is initiated by applying a large voltage across a gap containing a low pressure gas. The required breakdown voltage, V_{bd}, is given by Paschen's law:

$$V_{bd} \propto \frac{P \times L}{\log P \times L + b}$$
2-2

where P is the chamber pressure, L is the electrode spacing, and b is a constant. Once a plasma is formed, ions in the plasma are accelerated toward the negatively charged cathode. When they strike the surface, they release secondary electrons, which are accelerated away from the cathode. They may collide with neutral species while crossing from cathode to anode. If the energy transfer is less than the ionization potential of the gaseous species, the atom can be excited to an energetic state. The atom decays from this exited state through an optical transition, providing the characteristic glow. If the energy transfer is high enough, however, the atom will ionize and be accelerated toward the cathode. The bombardment of the cathode in this ion stream gives rise to the process of sputtering.

2.6.4 Plasma-Enhanced Chemical Vapour Deposition (PECVD)

In our work plasma-enhanced chemical vapour deposition was used for silicon nitride (SiN) passivation prior to measuring the minority carrier lifetime of textured silicon wafers.

Direct plasma method and Remote and plasma methods are the two major methods commonly used for PECVD SiN deposition. Remote plasma method was used in this work. This process was performed at Australian National University.

2.6.4.1 Direct plasma method

In this method the processing gases are excited by means of an electromagnetic field and where the wafers are located within the plasma. The electromagnetic field either has a frequency of 13.56 MHz or in the 10- 500 kHz range. Figure 2-10 shows a cross sectional view of such a direct –plasma reactor. As the wafers are directly exposed to the plasma, the ion bombardment of the sample surface during the film deposition cause a considerable surface damage[16].
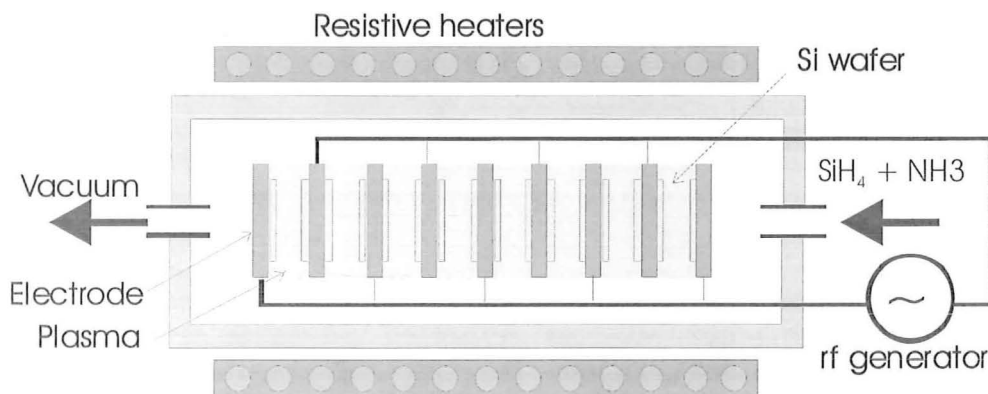
Figure 2-10: PECVD system employing direct plasma method

This problem can be largely eliminated as for plasma excitation frequencies above 4 MHz the acceleration periods are too short for the ions to absorb a significant amount of energy. In this case a direct surface bombardment by ions is only possible due to the acceleration of ions by the plasma sheath potential.

A promising alternative is the so called remoter PECVD method which is used to passivate our wafers before the minority carrier lifetime measurements.

2.6.4.2   Remote plasma method.

In this set up, an RF-induced plasma transfers energy into the reactant gases, allowing the substrate to remain at lower temperatures than in other CVD techniques.

With a simple parallel plate reactor, substrates can be placed horizontally or vertically when the pressure is low enough. Wafers are placed on the grounded electrode and are subjected to a less energetic bombardment than wafers placed on the powered electrode.

The PECVD films are not stoichiometric because the deposition reactions vary widely, and particle bombardment during growth of a multicomponent system changes the composition according to the ratios of sputtering yields of the component materials.

Good adhesion, low pinhole density, good step coverage, adequate electrical properties, and compatibility with fine line-width pattern transfer process are the main advantages of the PECVD films.

Figure 2-11 shows the schematic of the remote PECVD system used to passivate the FZ wafers prior to the minority carrier lifetime measurements. If the reactor is not optimised, the quality of the film is always non-stoichiomatric. It can be seen that in this PECVD approach, the Si wafer is located outside the plasma region, allowing the deposition of Si_3N_4 films with virtually no surface damage of the samples.
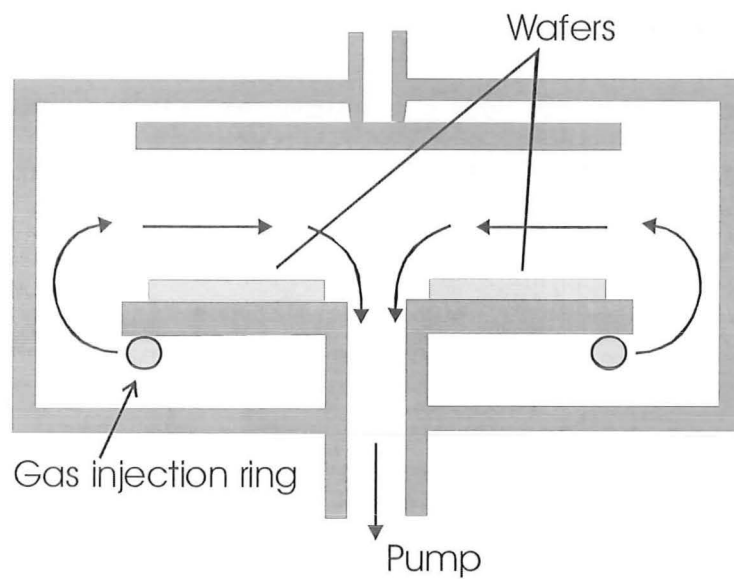
Figure 2-11: Schematic of the remote PECVD system

With regard to the surface passivation properties, remote-plasma and high-frequency direct-plasma Si_xN_y films produce about the same excellent surface passivation on phosphorous diffused as well as non–diffused Si surfaces. While Si_xN_y films generated by low frequency direct PECVD perform significantly poorly [17].

Some advantages of using remote-plasma method include [18]:

- Very high plasma densities and directional film deposition can be obtained.
- Wafer handling is easier.
- No electrical contact between the wafer and the wafer holder is required.
- An in-situ quality control is possible with automatic feedback to the deposition process.
- An upscaling to very large wafer can easily be realised.

2.7 Diffusion Techniques

Diffusion was performed in tube furnace in nitrogen environment. Phosphorous spin-on-dopant liquid source as well as phosphorous solid diffusion source was used to make the emitter of n^+ - p solar cells.
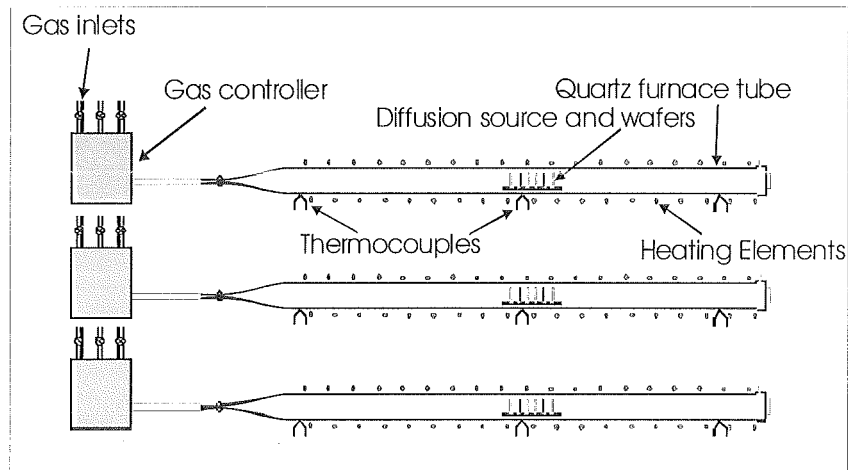
Figure 2-12: Schematic diagram of the tube furnace. Three Quarts tubes of 2 meter long and 150 cm diameter have separate gas controllers.

Diffusion, thermal oxide growth, annealing and sintering were performed in this quartz tube furnace shown in Figure 2-12. This furnace has 3 separate tubes and each tube has three power supplies separately for front section, middle section and the rear section. Temperatures are monitored at these 3 points using 3 thermocouple thermometers. For a uniform tube temperature, all three supplies were calibrated.
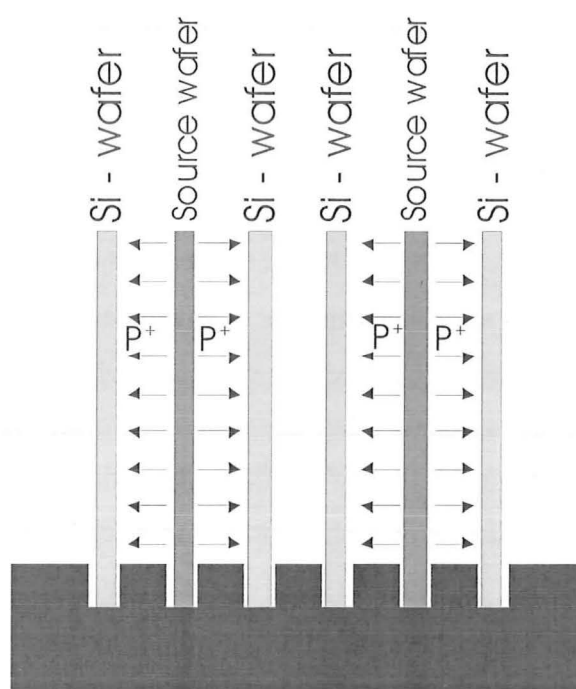
Figure 2-13: Arrangement of source wafer and silicon wafer for phosphorous diffusion.

Spin on dopant liquid source (Phosphorosilicafilm by Emulsitone Company) was spun on the destination silicon wafer and diffused in tube furnace in nitrogen environment. Solid diffusion source was arranged in a carriage as shown in Figure 2-13 and diffusion was done in a tube furnace in nitrogen environment. This first step of short time diffusion is called predeposition. After the predeposition, phosphorosilica glass was removed and drive in was performed. In this step emitter junction as well as SiO_2 passivation was done simultaneously. Nitrogen and oxygen gases were used and their flow rates depend on the junction depth and the thickness of the thermal oxide needed. For a high efficiency silicon solar cell, extremely high purity furnace tubes should be maintained. Particularly heavy metals reduce the minority carrier lifetime of silicon substrates and hence the cell efficiency.

2.8   Atomic force Microscopy (AFM)

Atomic force microscopy was used to investigate the topography of the submicron structures and the mask-less textured black silicon surfaces. The Digital Instruments Dimension 3100 (DI 3100) instrument was used in this work. It was very useful in

investigating insulating materials such as photoresist patterns while SEM can be used for conductive materials such as metals and silicon.

2.8.1 Principle of AFM

AFM belongs to the class of scanning probe microscopy techniques. An image is obtained by scanning the probe with a very sharp tip over a sample, with a tip to sample distance in the order of angstroms. The tip is attached to a cantilever which is deflected towards and away from the sample by separation-dependent atomic forces. In the common AFM configuration depicted in Figure 2-14 , the cantilever deflection is measured by a position-sensitive photodetector consisting of a photodiode and bi-cell split photodetector. From this deflection, an image topography can be obtained. There are many AFM configurations but for simplicity the configuration shown in Figure 2-14 will be discussed, as this resembles that of the DI 3100 instrument [19].
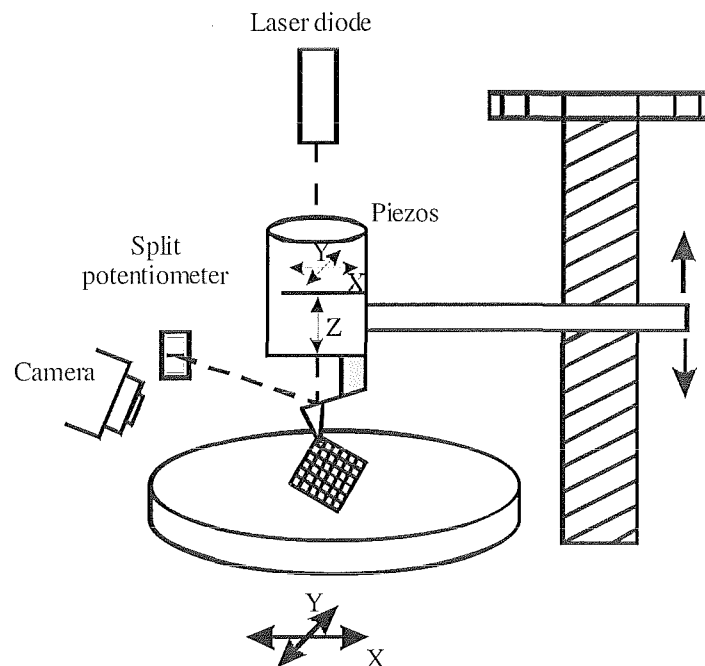
Figure 2-14: Schematic representation of a typical Atomic Force Microscope.

Coarse positioning of the sample in the x-y plane is provided by stepper motors, which shift the sample stage. An additional stepper motor controls the height of the probe, relative to the stage for coarse adjustments. A camera provides feedback to aid positioning of the sample and probe, so that specific regions of the sample can be located

and scanned. When an image is to be captured, the tip is lowered onto the sample (at a distance dependent on the AFM mode), and the z piezoelectric scanner brings the tip to the final scan position. The x-y piezoelectric scanners are approximately 100μm x 100μm for the DI 3100. The AFM instrument can be operated in a number of different modes: contact AFM, non-contact AFM, and tapping or intermittent-contact AFM. These modes correspond to the operation at different probe / sample separations. Figure 2-15 illustrates the relationship between the distance of operations, the relative strengths of these forces and their direction [19].
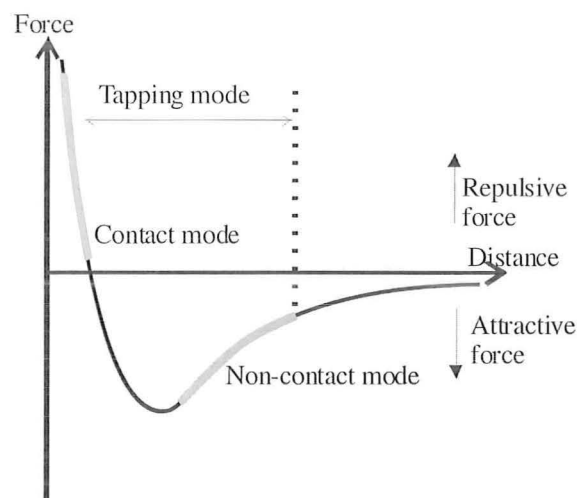
Figure 2-15: Three main modes of AFM operation, Tapping, Contact and Non-contact mode.

In contact mode (repulsive mode) the tip makes soft physical contact with the sample and a cantilever with a low spring constant is required. The advantage of operating in this mode is that the forces are large, and the distance-force curve quite steep so small deflections can be measured more easily. The spring constant of the cantilever should be lower than the effective spring constant of the surface to prevent surface deformation. During the scan the cantilever deflection is measured. The scan can proceed in either a constant- height or constant-force mode. In constant-height mode the deflection is translated directly into a surface topography. This is suitable for low relief surfaces. More common is the constant-force mode, which feeds back the deflection information to raise

or lower the cantilever to maintain a constant force. The cantilever motion then reflects the surface topography.

In non-contact mode, no physical contact is made with the sample. The cantilever is oscillated at a frequency which is slightly above the cantilever's resonant frequency, just above the sample surface (~10-100 Å). The resonance frequency or vibrational amplitude is monitored, and kept constant by a feedback mechanism that shifts the cantilever vertically. It operates with small forces that are suitable for studying soft or elastic samples. Because these forces are small, they are also more difficult to measure to the same accuracy. A stiff cantilever is used to prevent the cantilever being pulled into contact with the sample. Non-contact mode requires a slower scan mode than contact or tapping mode.

In tapping mode, an oscillating cantilever is brought close enough to the sample that it just taps the sample. It is less likely to damage soft samples compared to contact AFM as it eliminates friction and drag between the sample and tip. Again a constant oscillation amplitude is maintained and the cantilever motion is stored to obtain the topography. The majority of AFM imaging in this work was conducted in tapping mode.

2.9 Sinton Lifetime Tester

A schematic of the experimental apparatus used in this thesis for measuring the minority carriers lifetime of silicon wafers is given in Figure 2-16. The V_{oc} can be measured directly by the oscilloscope without the need for a coil or RF-bridge.
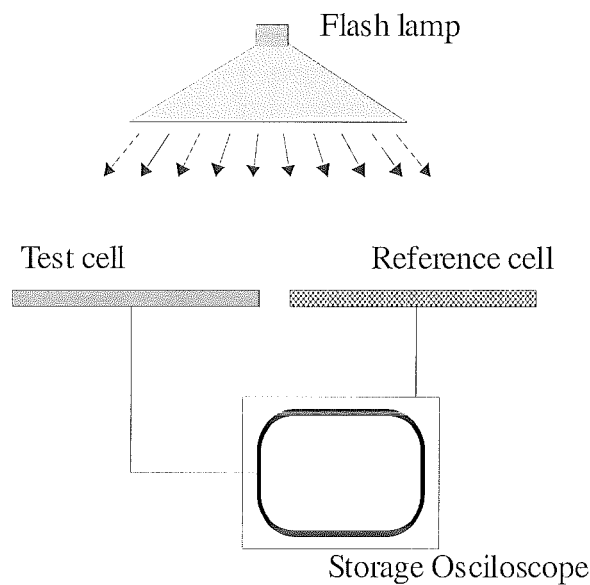
Figure 2-16: Schematic diagram of the apparatus used for measuring minority carrier lifetime of silicon solar wafers.

This technique is based on the simultaneous measurement of the excess conductance of the wafer, through an inductively-coupled coil, and the generation rate, via a calibrated solar cell. Under steady-state conditions, the generation and recombination rates are equal, and the lifetime is simply proportional to the ratio of the excess conductance and the generation rate. For a given irradiance, the total photogeneration within the sample J_{ph} can be easily and accurately estimated using available computer programs [20] or published tables and graphs [21] . The evaluation of J_{ph} requires that the absorption coefficient and the optical properties of the sample are known. All lifetime measurements were performed at the Department of Electrical Engineering, Australian National University.

2.10 Photoluminescence Measurement Technique

Photoluminescence measurement was performed at the department of physics, University of Canterbury, New Zealand. A newly acquired cryostat capable of reaching temperatures as low as 4K was used in this work. a close cycle liquid helium was used for low temperature measurements.
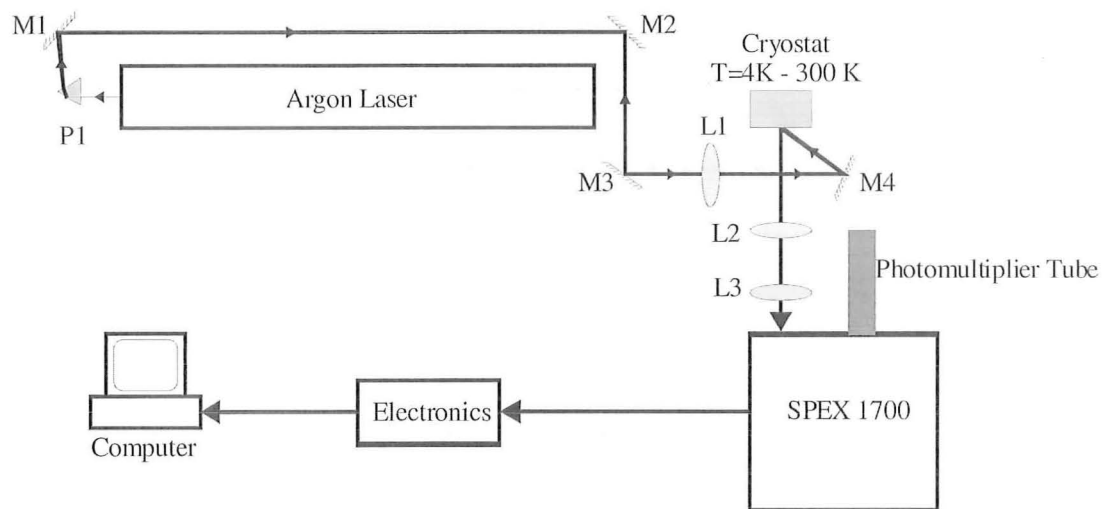
Figure 2-17: Photoluminescence experimental setup used to measure the photoluminescence of textured silicon substrates.

A schematic of photoluminescence experiment at the Department of Physics and Astronomy, University of Canterbury is shown in Figure 2-17. The detail of the experiment and the equipments is given below.

1. Argon Laser

A continuous wave (CW) Argon gas laser was used as the excitation source. The visible 514.5 nm laser wavelength was chosen as the excitation wavelength for these experiments, and 20 mW laser power was maintained by adjusting the laser current.

2. Optics

A prism (P1) was needed to disperse the laser beam and other unnecessary wavelengths were spatially filtered by an iris for these experiments. Four mirrors (M1, M2, M3, M4) are needed to guide and reflect the beam from the laser onto the samples. L1 is a focussing lens to adjust the laser spot size on the sample. L2 collects the scattered emission light from the sample, and L3 is a focussing lens with a focal length suitable for the SPEX 1700, to focus the collected light to the entrance slit of the spectrometer.

3. Cryostat

The Oxford Microstat close cycle cryostat is capable of maintaining temperatures from 4 K to 300 K with the help of liquid helium.

4. Spectrometer

The SPEX 1700 spectrometer is a double monochromator that selectively passes radiation on the basis of its frequency.

5. Photomultiplier Tube

A liquid Nitrogen cooled Germanium detector was used at 250 V.

6. Electronics

A PL signal was recorded with a conventional lock-in technique in phase with the frequency of a mechanical chopper. A custom written computer software called Lab Routine was used to store and analyse the PL data.

2.11 Reflectance Measurements

Reflectance was measured using a purpose built integrating sphere attachment of a high accuracy spectrophotometer. Besides the specularly reflected radiation, the diffuse radiation is also measured in this method. This will give us an idea of the absorbance of the textured surfaces. The hemispherical mirror collects the diffuse as well as the specular reflections and sends them to the detector. The schematic of the experimental set up used at Industrial Research Limited is shown in Figure 2-18. Although the reflectance was measured for spectral wavelength between 250 nm to 2500 nm, the wavelength beyond 1200 nm is too low energetic to be absorbed by silicon. Therefore the reflectance data for wavelengths lass than 1200 nm will not be included in any of the graphs in chapter 6.
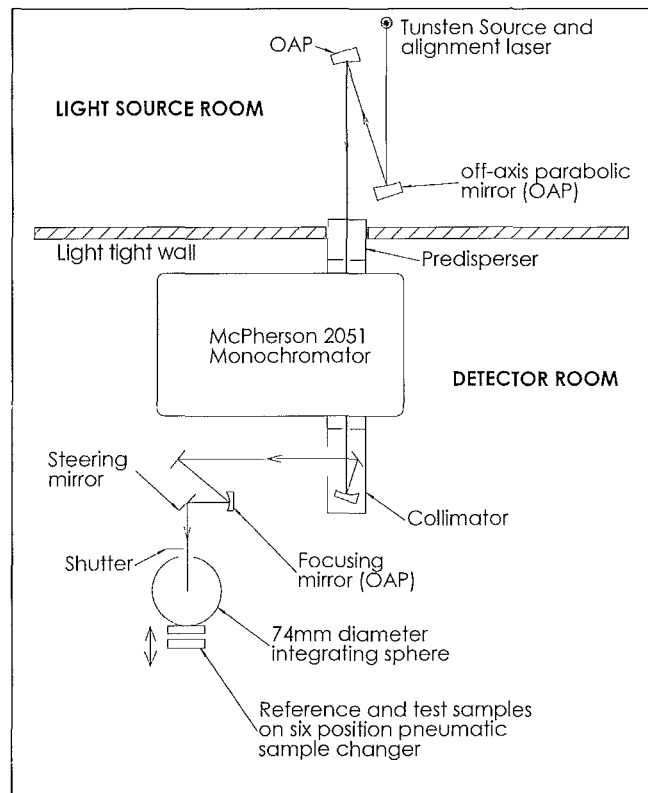
Figure 2-18 : Experimental set up of the reflectance measurements [22].

2.12 Characterisation of Solar cells
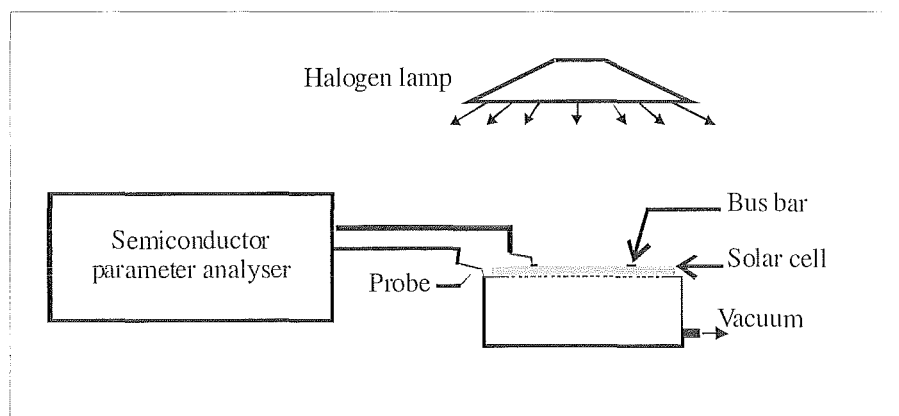
Figure 2-19: Experimental set up used for I-V characterisation of solar cells

Fabricated solar cells were tested using custom made apparatus shown in Figure 2-19. The halogen lamp was calibrated using a solar cell with known efficiency. The I-V data

were collected using a Hewlett Packard 4155A semiconductor parameter analyser and analysed using computer. This method is not accurate and has several errors such as series resistance added by probes.

Few cells were taken to UNSW for advanced characterisation and the measured efficiencies were compared with the efficiencies measured at ECE, University of Canterbury.

CHAPTER 3

SURFACE TEXTURING

3.1 Introduction

Surface texturing for enhanced absorption in Si has been historically obtained by creating randomly distributed pyramids using anisotropic etchants and this preferential etching works only on single crystalline silicon because of its crystallographic orientations. NaOH or KOH is used for wet chemical texturing of crystalline silicon. These techniques are not suitable for multicrystalline silicon (mc-Si) solar cells and thin film substrates because of the random grain orientation. Also this technique is not suitable for preparing substrates for thin film solar cells. Several attempts have been made to texture polycrystalline and multi crystalline silicon wafers, including laser-structuring [23], mechanical diamond saw cutting [24] porous-Si etching [25] and mask-less RIE etching which results in so-called "Black silicon" [26]. Also by applying an etch mask to the surface and using isotropic etching, structures can be etched in mc-Si for light confinement [3].

A number of texturing techniques that have been studied in this work will be presented in this chapter.

3.2 History And Principles of Light Trapping

Although the effect of surface texture on reflection is well known outside the solar cell area, there does not seem to have been much emphasis on surface texturing in cell literature prior to 1954. However, only months after the fabrication of the first efficient silicon cells at Bell laboratories in late 1953, one member of the group involved, Calvin Fuller, filed a patent application dealing primarily with boron diffusion but also describing cells with serrated top surfaces for reducing reflection [27]. However, Dale and Rudendberg [28] are usually credited with bringing the potential of surface structure for reflection control to the attention of the photovoltaic community in 1960. The structure in

which they were specifically interested was based on inverted tetrahedra, which would give excellent reflection properties as discussed in the following section. The main difficulty at the time was how to make this structure simple. The proponents explored ultrasonic machining, using a machine piece with projecting tetrahedra, but also foreshadowed the use of anisotropic chemical etches [28].

With the development of interest in anisotropic etching of silicon in the late 1960s for microelectronics, geometric texturing of the cell surface finally became practical. The first cell demonstrating major performance improvement using such texturing was the COMSAT non-reflecting cell reported in 1974 [29]. This structure of Figure 3-1 is formed by anisotropically etching a surface originally oriented parallel to the <100> crystallographic plane to expose equivalent planes which intersect to form the square-based pyramids shown.

a   b
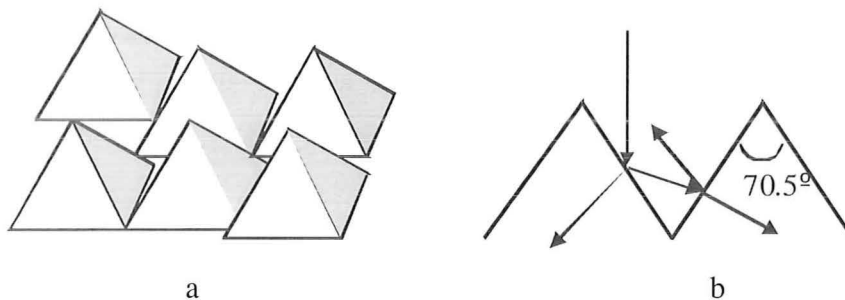
Figure 3-1: a. Wet textured pyramids formed by <111> crystallographic planes of c-Si and b. Ray tracing diagram for 2-D case.

Other roughly concurrent work used both KOH and hydrated hydrazine to form cells not only incorporating these pyramids, but also grooves [30]. Oxide strips were formed by photolithography to mask the etch and hence define groove location.

One feature of such surface texture as a means of reflection control is the wide bandwidth response. Not only did the textured surface couple useable light into the cell, it was also effective in coupling infrared wavelength which resulted in higher cell operating temperatures. Alternatives such as multilayer antireflection coatings developed at about the same time could be made more wavelength sensitive [31]. In the terrestrial environment, more mechanisms are available for getting rid of unwanted heat from the cell. Cells with texturing still operate a few degrees hotter than non-textured cells even in this case [32]. Texturing has become the norm for manufacturers of terrestrial crystalline

silicon cells. Several leading solar cell manufactures including BP solar and Sharp have already started to market surface textured solar cells.

Multicrystalline wafers are capturing an increasing share of the bulk silicon cell market because of their potential low cost. Although attempts have been made to control grain orientation [33], the grains in this material are generally randomly oriented. This means that only a fraction are suitable for crystallographic texturization. Processes based on photolithography combined with chemical or plasma etching, laser and mechanical texturing have been reported [23, 24].

3.3   SF$_6$/ O$_2$ Plasma Characterisation

Different structures from a few nanometres to tens of micrometers can be engineered on semiconductor surfaces by the dry etching process. A general requirement of silicon etching by plasma is that the plasma radicals react with the silicon surface, building gaseous and volatile reaction products. Some of the simplest reactions of fluoride plasma with silicon are:

$$Si + 4 \, F^* \rightarrow SiF_4 \qquad\qquad\qquad 3\text{-}1$$

$$Si + 2 \, O^* \rightarrow 2 \, SiO_2 \qquad\qquad\qquad 3\text{-}2$$

$$SiO_2 + 4 \, F^* \rightarrow SiF_4 + O_2 \qquad\qquad 3\text{-}3$$

$$SiF_4 + 2O_2 \rightarrow SiO_4F_4 \qquad\qquad\qquad 3\text{-}4$$

To enable these chemical processes, the wafer surface must have a certain purity. This is probably due to organic residuals from as-cut wafer cleaning, applied by the wafer producer after wire sawing. If silicon wafers are exposed to plasma, a surface damage could be generated. This RIE induced damage is discussed in Chapter 4 and Chapter 5. Additionally, residuals on the wafer surface from the applied etchants and impurities might penetrate into the crystal structure during the plasma etching. Even metallic contaminants of the plasma chamber walls were found inside the crystal and on the wafer surface [34].

3.3.1 Effect of oxygen flow rate

The principle of Si etching using SF_6/O_2 plasma is shown in Figure 3-2. In SF_6/O_2 plasma, SF_6 produces the F^* radicals for the chemical etching of Si by forming volatile SiF_4. Oxygen creates the O^* radicals to passivate the Si side wall surfaces with SiO_xF_y which helps to control etch profiles. SF_6 is the source of SF_x^+ ions, responsible for the removal of the SiO_xF_y layer at the bottom of the etching trenches forming the volatile SiO_xF_y.
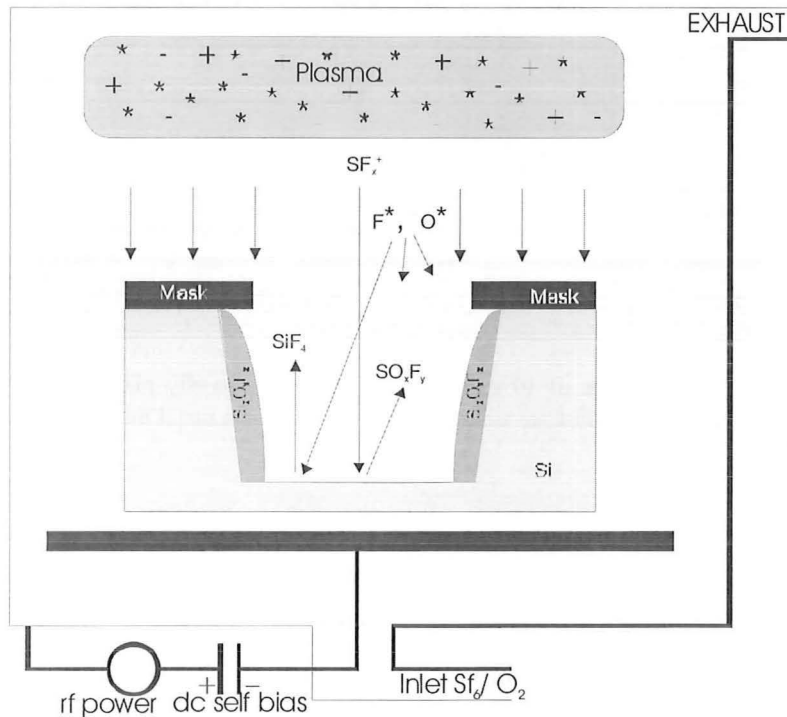
Figure 3-2: Schematic diagram of the etch mechanism of SF_6/O_2 plasma system.

Three p-type, CZ-silicon substrates with photolithographically defined NiCr mask of 40 nm thick were etched in the reactive ion etcher under the following etch conditions.

Table 3-1: RIE etch parameter O_2 flow rare experiment

SF_6 Flow rate	Temperature	RF power	Etch Time	Etch pressure	O_2 flow rate
40 sccm	173K	150W	30 min	70 mT	variable

When the O_2 flow rate is 10sccm, the etch profile is isotropic and the etch rate is calculated as 0.15 μm/min. As can be seen in Figure 3-3, the etched surface appeared

smooth. However, we could observe undercut due to the domination of chemical etching rather than physical etching during RIE.
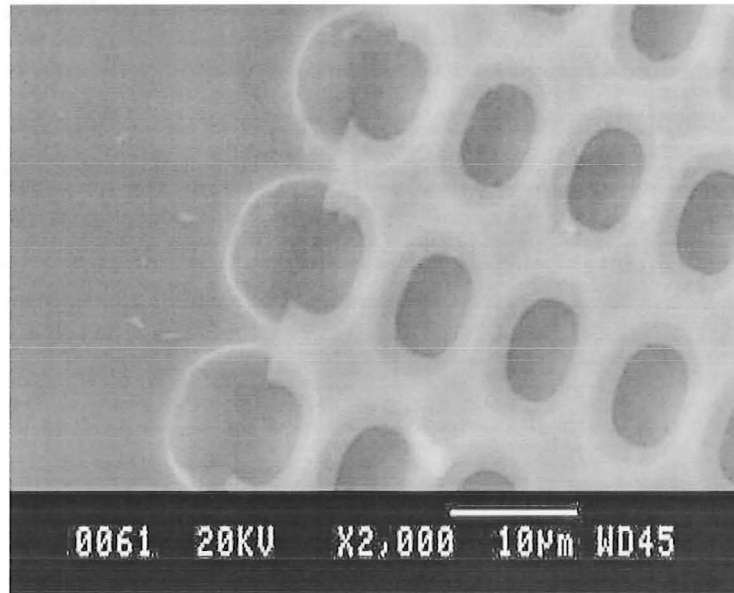
Figure 3-3: The effect of addition of 10 sccm of O_2 to the 40 sccm SF_6 plasma. 10μm diameter holes etched to a 4μm deep into silicon substrate isotropically. The Nichrome metal mask is not removed.
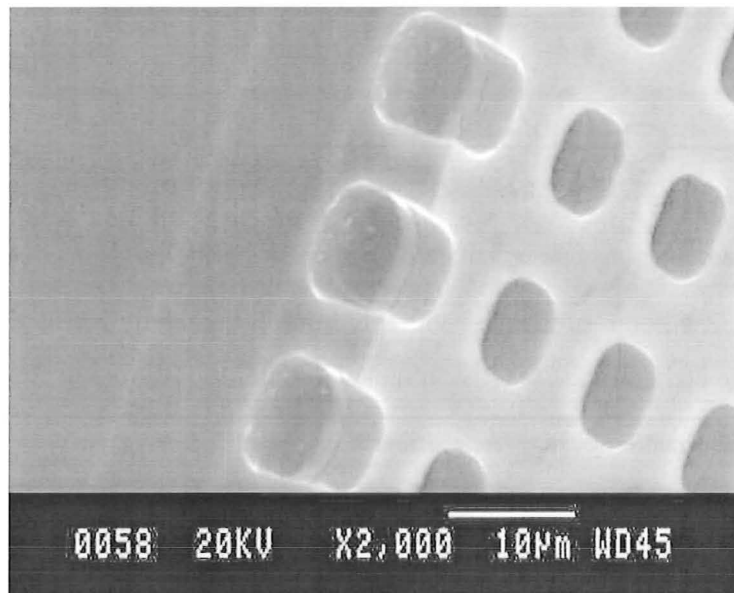
Figure 3-4: The effect of addition of 15 sccm of O_2 to the 40 sccm SF_6 plasma. 10μm diameter holes etched to a 7μm deep into silicon substrate anisotropically. The Nichrome mask is removed after etching.

When the O_2 flow rate is 15 sccm the etch profile is highly anisotropic. As can be seen in the Figure 3-4, the etched surface appears reasonably smooth. The etch rate is calculated as 0.25 μm/ min.
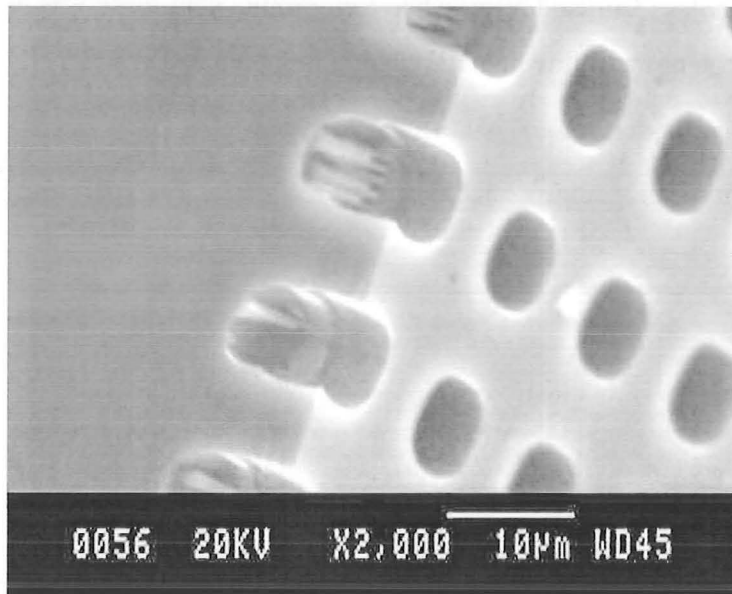
Figure 3-5: The effect of addition of 25 sccm of O_2 to the 40 sccm SF_6 plasma. The etch profile is highly anisotropic and micro grass formed inside the holes. The Nichrome mask is removed after etching.

Micrograss starts to appear at higher oxygen flow rates. This was observed for oxygen flow rate at 25 sccm and over. Figure 3-5 clearly shows the micrograss within the holes. Micromasking causes this type of needle like micrograss. The origin of micromasking is caused by native oxide, dust which are already on the wafer before etching [34]. But, it is also formed during the etching because silicon oxide particles coming from the plasma are adsorbed at the silicon surface or because of the oxidation of the silicon surface together with the angle-dependent ion etching of this oxide layer. Another source of particles during etching which will act as micromasking is the resputtering of mask materials due to imparting ions [34].

3.3.2 Effect of feature size on etch profile

Micrograss was highly likely to occur within the smaller holes (2μm) rather than relatively larger holes (3μm and 5μm) when a chromium etch-mask was used. The etch condition of the following RIE etching is shown in Table 3-2.

Table 3-2: RIE etch parameter to determine the effect of feature size

SF_6 / O_2 Flow rate	Temperature	RF power	Etch Time	Etch pressure
40 / 25 sccm	173K	150W	30 min	70 mT
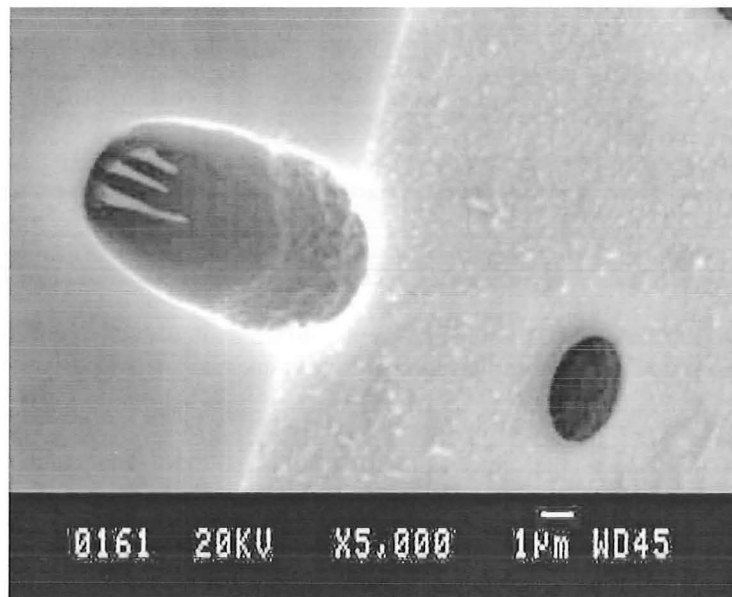
Figure 3-6: 2μ , holes Cr mask. High O_2 flow rate and small mask cause micrograss inside the cavity.

Figure 3-7 shows the magnified view of the micrograss formed inside the holes shown in Figure 3-6. They are as long as 3 μm and less than 200 nm in diameter. This feature demonstrates the very high degree of anisotropic etching of SF_6 / O_2 reactive ion etching.
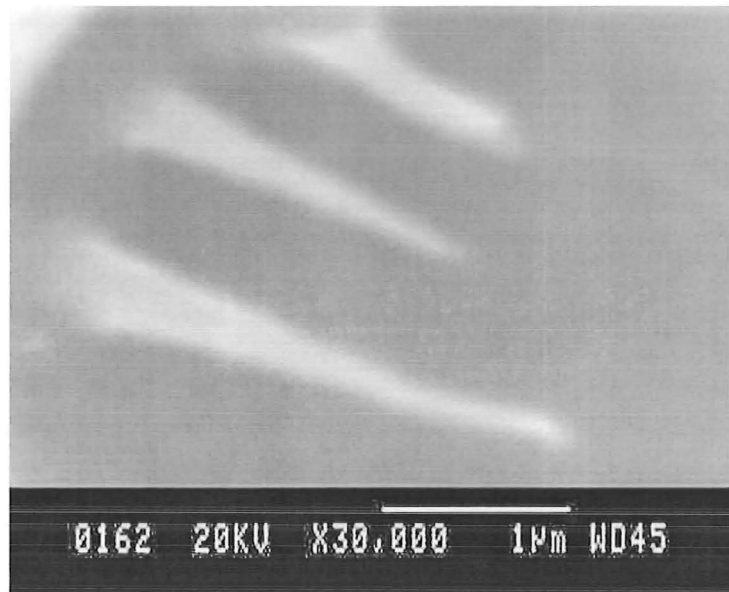
Figure 3-7: Magnified view of micrograss formed within the holes.
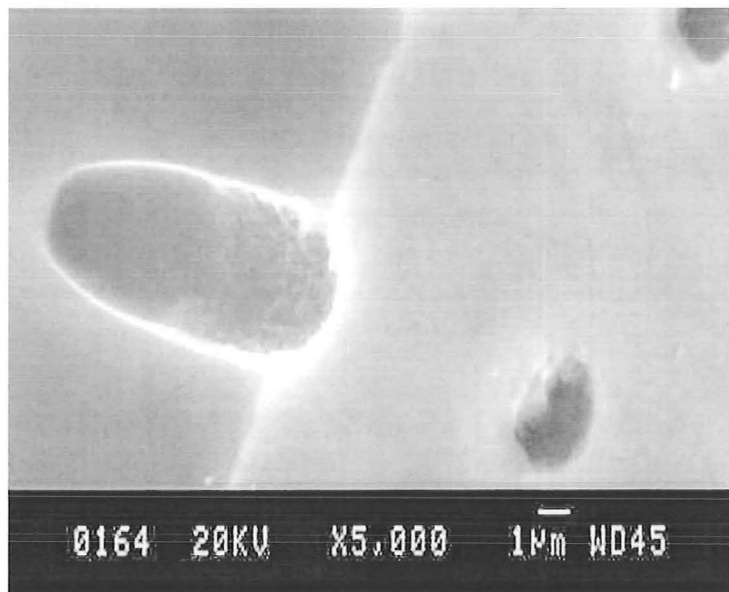
Figure 3-8: 3µ ,hole Cr mask. does not form micrograss during RIE when used in the same condition applied for the substrate shown in Figure 3-6.
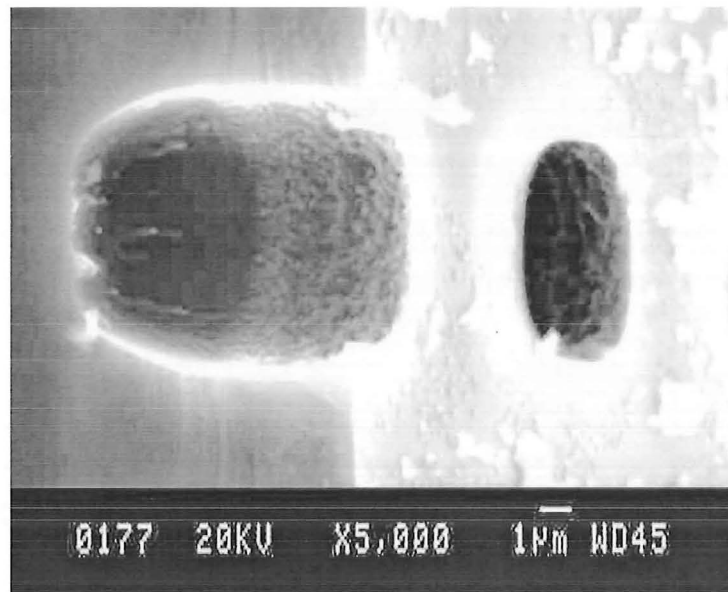
Figure 3-9:   5μ, hole Cr mask does not form micrograss during RIE when used in the same condition applied for the substrate shown in Figure 3-6.

Figure 3-8 and Figure 3-9 show the 3μm and 5 μm holes which did not form micrograss when etching.
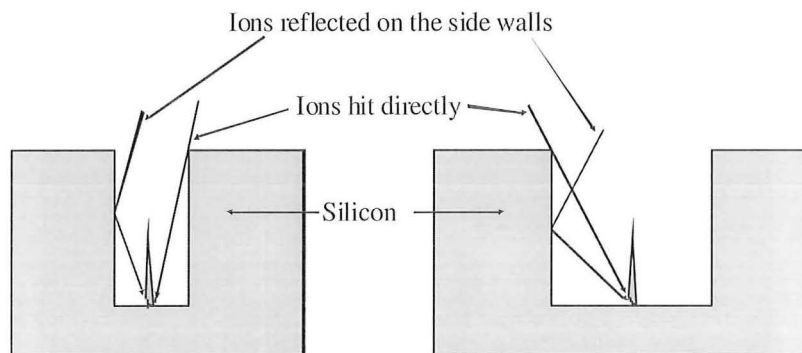
Figure 3-10: Schematic of the mechanism that removes micrograss faster in wider holes than in narrower holes. For wider holes, the direct as well as the reflected ions have a larger angle and hence can easily etch the bottom of micrograss.

Figure 3-10 shows schematically how the reflected as well as the direct ions in wider holes can easily reach the bottom of micrograss and eventually remove them.

3.3.3 Effect of mask material in High Density Plasma etching

This experiment was performed with the help of the Technical University of Delft, Netherlands. For this experiment, an ICP reactor was used. Aluminium, Nichrome, Chromium and Photoresist (S1813) were tested in the high density plasma. Square array of 3μm circular holes pattern was transferred using the wet etching technique. The etch condition is given below.

Table 3-3: RIE etch parameter for ICP etching

SF$_6$ / O$_2$Flow rate	Temperature	RF power	Etch Time	Etch pressure	Dc bias
20/2sccm	-90C	400W	25 min	0.19 Pa	20V

Aluminium mask:

Aluminium is a very suitable material for the solar cell industry and does not contaminate the wafer. In this experiment, pure Aluminium of 100 nm thickness was evaporated on a (100) oriented p-type cz-silicon wafer and a square array of 2μm holes pattern was transferred using wet etching technique.
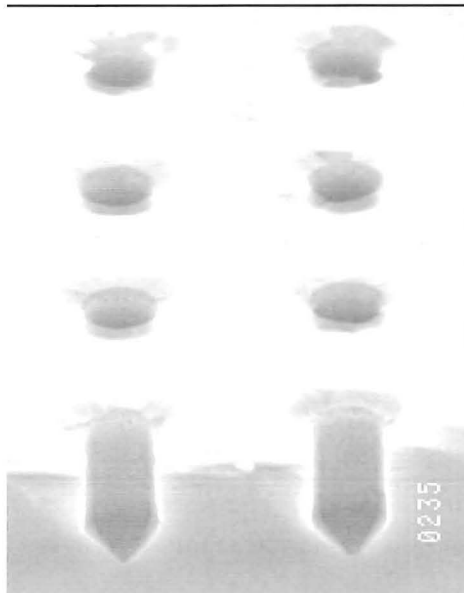
Figure 3-11: ICP etched silicon wafer with 100nm Aluminium mask. The holes are 2 μm diameter and 10 μm deep.

As you can see in Figure 3-11, the etching is highly anisotropic and the etch rate is higher for the <111> plane. This crystallographic preferential etching leads to inverted pyramid shape at the bottom of the hole.

Nichrome mask:
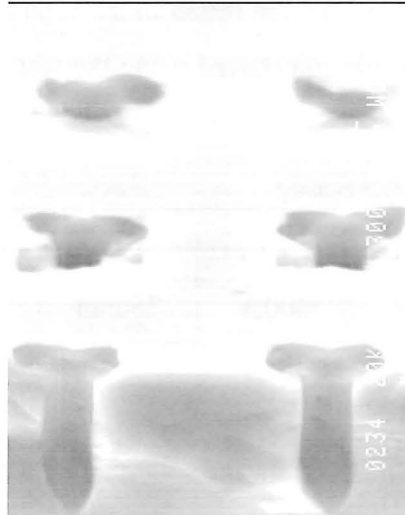
Figure 3-12: ICP etched silicon wafer with 100nm Nichrome mask. The holes are 2 µm diameter and 10 µm deep.

A 40 nm Nichrome layer was evaporated on a (100) oriented p-type cz-silicon wafer and a square array of 2µm holes pattern was transferred using the wet etching technique.

Figure 3-12 shows the ICP etched silicon wafer with NiCr mask. Despite the fact that the selectivity of NiCr/ Si is very high, this NiCr mask was heavily damaged closer to the holes by the ICP plasma and may be due to undercutting. In this case also we could see the inverted pyramid shape at the bottom of the hole.

Chrome mask:

A 40 nm chrome layer was evaporated on a (100) oriented p-type CZ-silicon wafer and a square array of 2µm circular holes pattern was transferred using the wet etching technique.
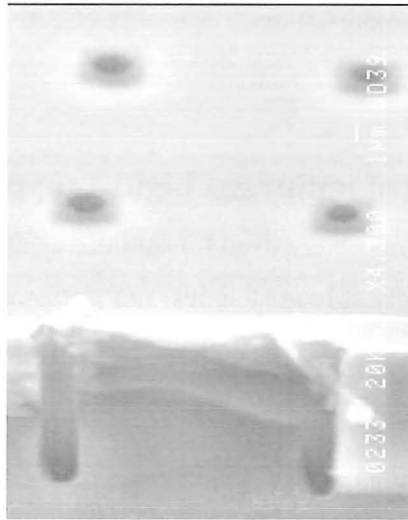
Figure 3-13: ICP etched silicon wafer with 100nm Chrome mask. The holes are 2 μm diameter and 10 μm deep.

Despite undercut the chrome mask is not damaged. Chrome seems to be stronger than the other masking metals we used.

Photoresist mask:

A square array of 5μm holes pattern was transferred on a silicon substrate using S1813 positive tone photoresist and postbaked at 130°C for 30 minutes in an oven.
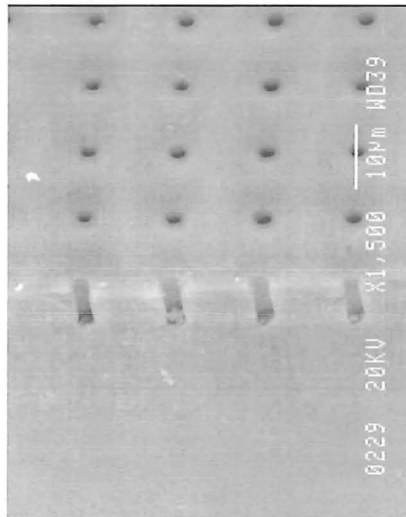
Figure 3-14: ICP etched silicon wafer with 100nm photoresist mask on Silicon. The holes are 2 μm diameter and 10 μm deep.

Figure 3-14 shows that the photoresist mask was very effective and the holes were highly anisotropic.

3.4   Surface Texturing of optimised Light Trapping Structures

So far masks of square dot arrays were used for optimizing etch condition. For better light trapping structure, hexagonally arranged holes and dots were prepared. Several masks were made with different feature sizes and pitches. Mask preparation procedures are discussed in Chapter 2.

3.4.1 Hole structures

A NiCr layer of 40 nm was evaporated on a p-type c-Si substrate and a honeycomb pattern of 3-4 µm holes in 5µm pitch was photolithographically defined on it. The wet etching technique was used to transfer the pattern to NiCr. The preparation procedure is shown in Figure 2-3. Three stages of the hole type texturing are shown in Figure 3-15, Figure 3-16 and Figure 3-17. The etch condition is given below:

Table 3-4: RIE etch parameter hole-type texturing

SF_6 / O_2 Flow rate	Temperature	RF power	Etch pressure
90 / 15 sccm	173K	150W	70 mT

After 20 minutes of RIE etching the holes are anisotropic cylindrical shape of 6-7 µm deep. Further 5 minutes of etching led to the widening of holes and when continuously etched for further 5 minutes those flat regions were eliminated because of over etching. These 30 minutes RIE etching yielded a good light trapping structure and is shown in Figure 3-17.
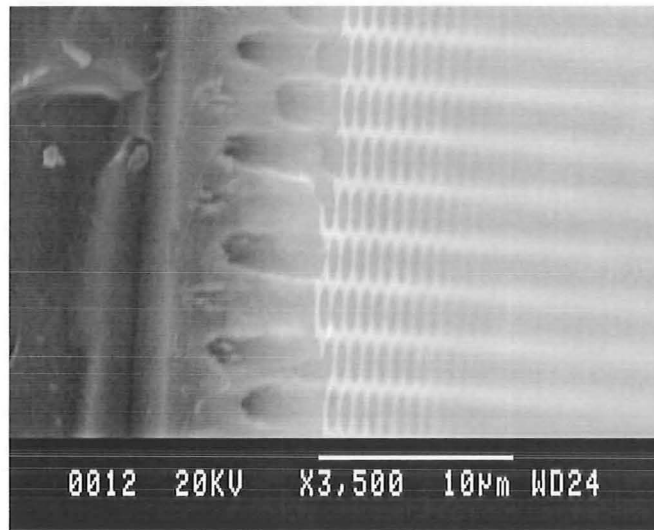
Figure 3-15: SEM photograph of anisotropically etched hole type structure. Holes are 6-7 μm deep and in 4 μm pitch. Etching time is 20 min.
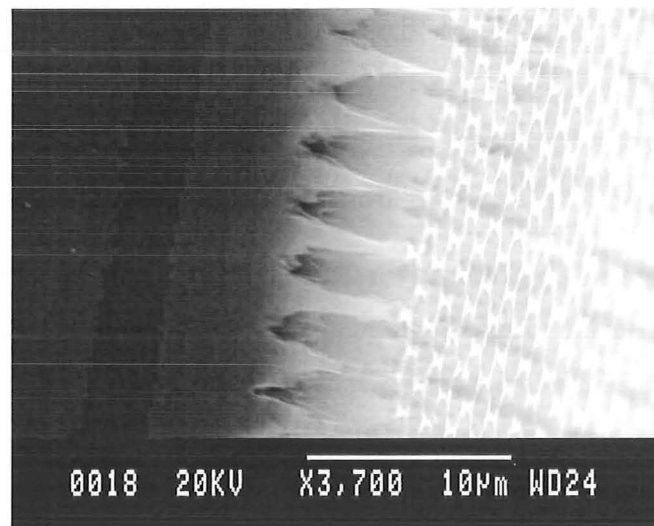
Figure 3-16: SEM photograph of slightly over-etched hole type structure. Holes are 7-8 μm depth and in 4 μm pitch. Etching time is 25 min.
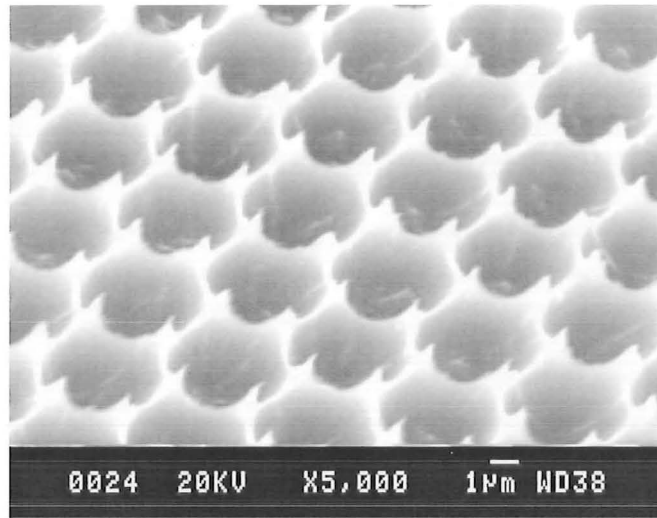
Figure 3-17: SEM photograph of hexagonally arranged hole type structure. Holes are 7-8 μm deep and in 4 μm pitch. The substrate was over-etched to eliminate the remaining flat surface to achieve better light trapping feature. Total etching time is 30 min.

The final textured surface of the hole-type structure is shown in Figure 3-17 after the dry etch processes. Its reflectance measurement is presented in chapter 6.

3.4.2 Column structures

Column structures are either cylindrical or tapered pillars. They can be formed using etch masks. SF_6/O_2 RIE etching forms very high aspect ratio structures. Wet chemical etching or over etching in RIE make them cone shaped or tapered cylinders.

High aspect ratio pillars:

Lift off technique was used to transfer the 2 μm dots in 4 μm pitch honeycomb patterns on a 2 inch, p-type, FZ-Si wafer. In this case solar cell friendly aluminium was used as the etch mask instead of NiCr. Unlike gold, copper and other heavy metal ions, Aluminium does not affect the silicon solar cell performance.   Honeycomb mask was used in this work.

Table 3-5: RIE etch condition for high aspect ratio pillars

SF_6 / O_2 Flow rate	Temperature	RF power	Etch Time	Etch pressure
90 / 25 sccm	173K	200W	30 min	100 mT
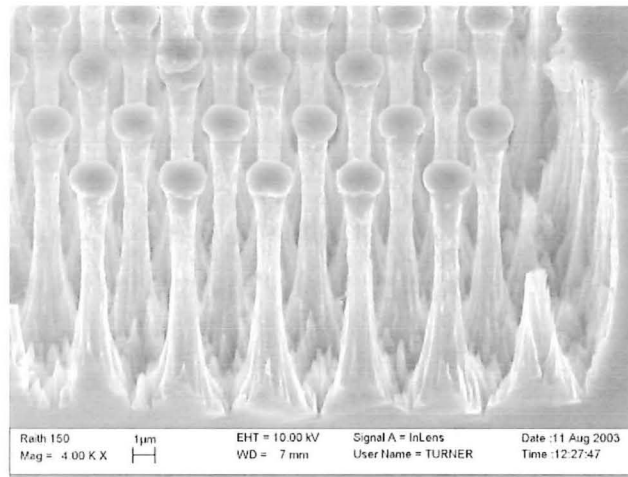
Figure 3-18: RIE textured column structures with a very high aspect ratio. The pillars are around 15 µm tall and the thickness is as small as 1µm at the middle.

Surface texturing has been achieved first using photolithography to define the textured patterns followed by a reactive ion etching pattern transfer process as illustrated in Chapter 2.

After 30 minutes of etching, the textured pillars looked like the ones in Figure 3-18. Further etching of another 10 minutes leads to the breaking of the pillars and hence a very good light trapping surface because of the absence of the flat top surface. The SEM image is shown in Figure 3-19. The surface looked very dark after the 40 minutes etching. Forming of high aspect ratio pillars is schematically explained in the Figure 3-20.
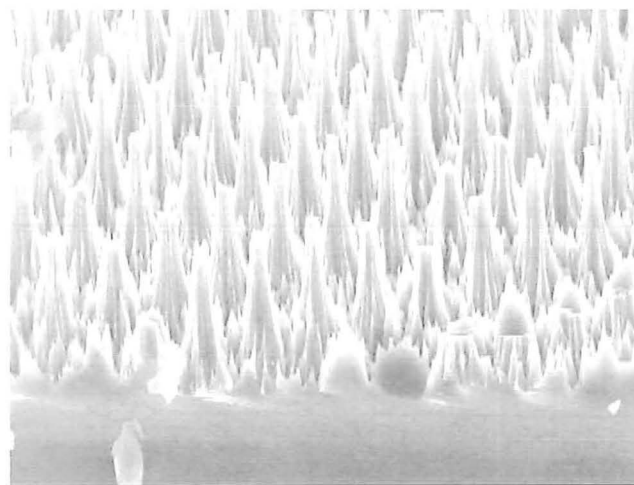
Figure 3-19: 40 minutes of etching leads breaking of the columns and hence a good light trapping surface.

Aluminum Mask

Silicon wafer

Silicon wafer

Silicon wafer

a   b   c
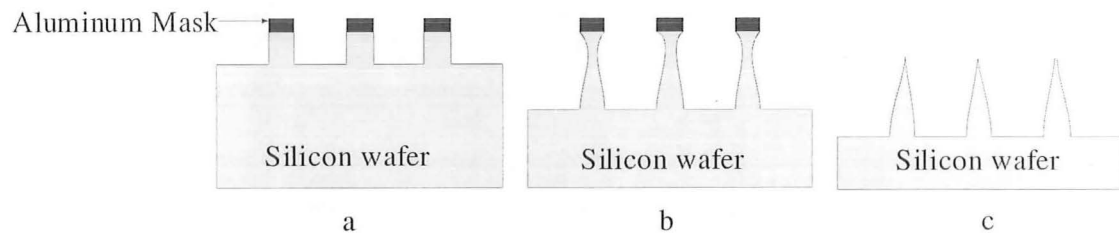
Figure 3-20: Schematic of the three stages of the RIE texturing. a: After 20 minutes of etching. b: After 30 minutes of etching, c:. After 40 minutes of etching.

Cone structure
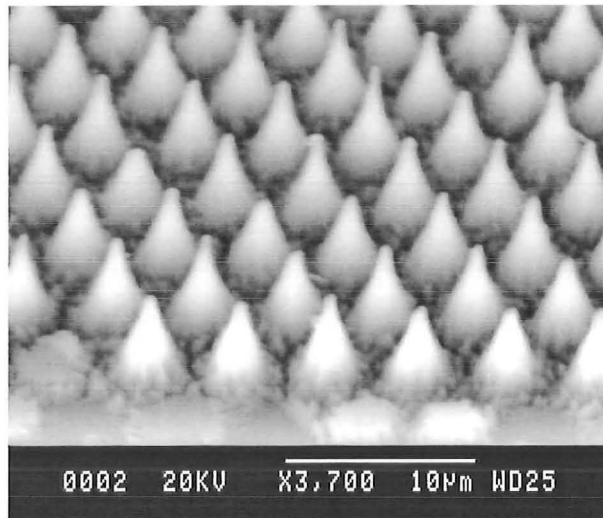
Figure 3-21: SEM photograph of cone type structure. Cones are 6-7 μm height and in 4 μm pitch.

The cone type textured surface shown in Figure 3-21 was etched using NiCr etch mask. The feature size is 3-4 μm diameter in 5μm pitch and the height is 6-7μm. The etch condition is as follows.

Table 3-6: RIE etch condition for cone-type texturing

SF_6 / O_2Flow rate	Temperature	RF power	Etch Time	Etch pressure
90 / 10 sccm	173K	150W	30 min	70 mT

The pillars ended up in cone structure due to our intentionally over etching. This cone type light trapping structures exhibited excellent result in the reflectance measurements performed. The reflectance is less than 0.5% for a wide range of solar spectrum regardless of wavelength. The detailed reflectance data is presented in chapter 6.

3.4.3 Maskless texturing

In this process no intentional mask is used. The black silicon texturing is based on local and regenerating oxide masking and therefore inhomogeneous etching. Initially the surface is covered with native oxide. This masking layer is not removed homogeneously, but perforated first. Unmasked spots are etched and pyramid to needle like structures are formed (depending on the degree of isotropy of the etch process) [35]. The walls of the structures are covered with adsorbed $Si_xO_yF_z$ and are therefore somewhat protected against etching as shown in Figure 3-22. The directed ion bombardment in RIE removes silicon as well as the adsorbed film. With the right choice of plasma parameters the regeneration of the adsorbed masking layer during the etch is just sufficient to maintain a kind of randomly perforated mask.
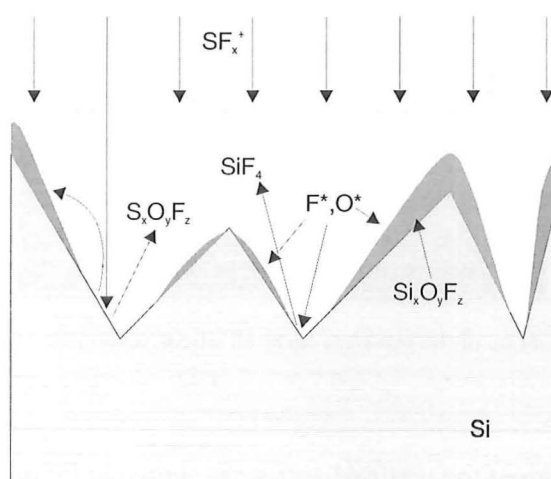
Figure 3-22: Schematic diagram of the formation of Black Silicon during maskless texturing.

An unmasked silicon wafer was dry etched for 10 minutes at a SF_6/O_2 flow rate of 90/25 sccm at RF power of 200W (0.45 W/cm^2) and temperature of 173K.
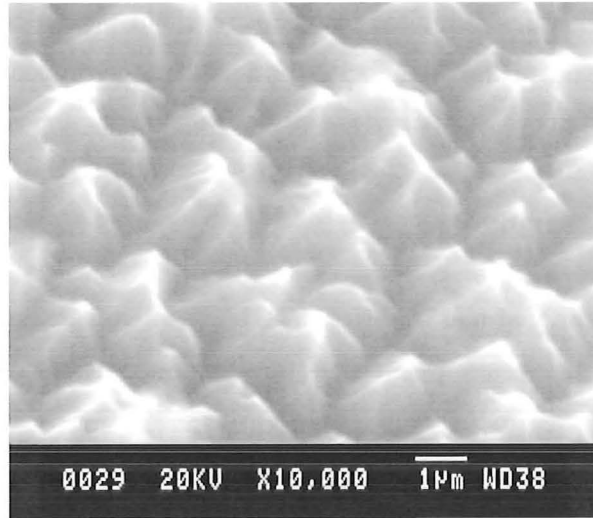
Figure 3-23: SEM photograph of black silicon. (No intentional mask is used). The bright areas represent highest points and dark areas represent lowest points.
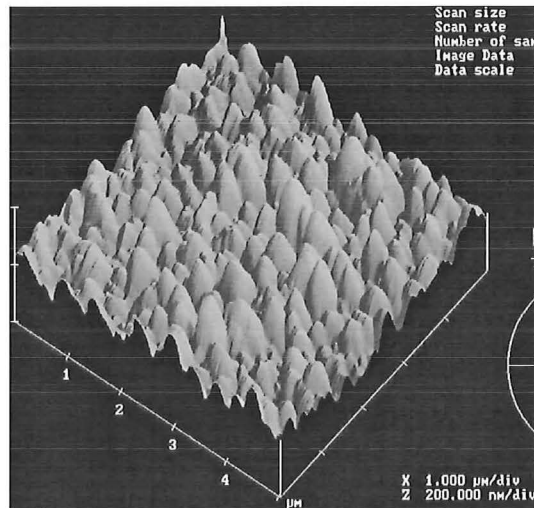
Figure 3-24: AFM picture of one of the maskless textured silicon substrates.

The resulting SEM image of the textured surface is shown in Figure 3-23 and Figure 3-24. High oxygen flow rate and high power were needed for the formation of black silicon. The surface was investigated using Atomic Forces Microscope and Surface Mean Roughness was calculated as 517 nm while the tallest structures were as high as 4 μm in size.

3.5   Inductively Coupled Plasma (ICP) texturing

Besides the RIE texturing, Inductively Coupled Plasma was also tried to texture the silicon substrates. The facility at the Technical University of Delft was employed to perform this experiment. One of the textured silicon substrates is shown in Figure 3-25. A technique called Bosch process was used in this texturing.

Bosch process:

To obtain anisotropic profiles, the process makes use of two alternating plasmas. The first plasma (SF_6) etches the silicon isotropically, the second plasma (C_4F_8) subsequently deposits a polymer layer to act as etch inhibition layer (in the next etch cycle) on the sidewall of the etched structure.

Table 3-7: Etch parameters for Bosch process

SF_6 / C_4F_8 Flow rate	Temperature	ICP power	Etch Time	dc bias
150 /150 sccm 6 Sec / 3 Sec cycle	25° C	2000W	25 min	90V
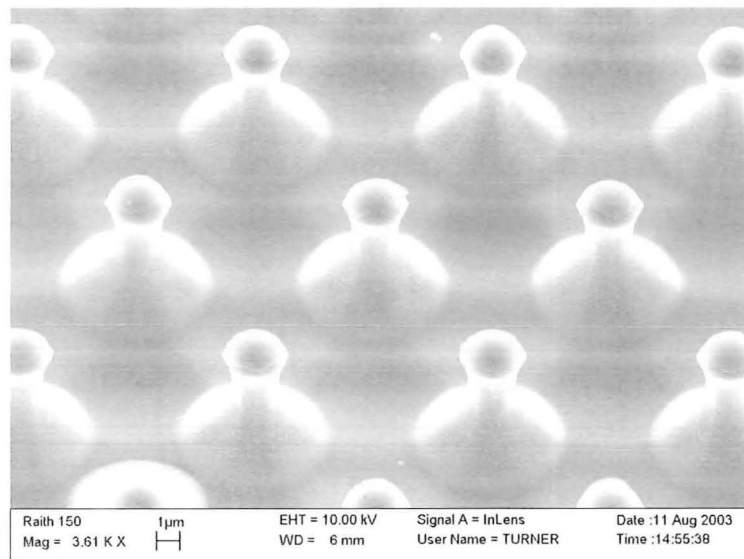
Figure 3-25: p-type FZ silicon wafer etched using a process called Bosch process.

Even though the Bosch process is meant for anisotropic etching, Figure 3-25 shows that the etching profile is highly isotropic. This is due to the intentional tuning of the reactor to achieve cone type structures.

3.6   Reactive Ion Etching Using SF$_6$ Plasma

Even though SF$_6$ plasma texturing creates fewer defects compared to SF$_6$/O$_2$ plasma, it is very difficult to control the shape of the textured structures. Undercut occurs due to the dominant chemical etching of Florien radicals.

The etch condition corresponding to the Figure 3-26 is given below

Table 3-8: RIE etch condition for SF$_6$ plasma etching

SF$_6$ / O$_2$ Flow rate	Temperature	RF power	Etch pressure
90 / 10 sccm	295K	200W	150 mT

Figure 3-26 shows the SF$_6$ plasma textured silicon substrate. Larger pitch was chosen because of high undercutting of SF$_6$ plasma etching. Also for minority carrier lifetime measurement, which is discussed in chapter 4, more room is needed for wet chemical etching.
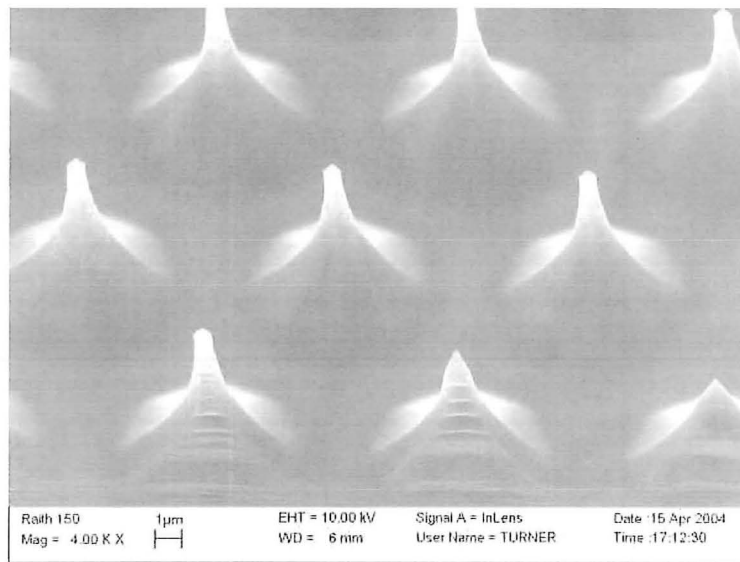
Figure 3-26: SF$_6$ plasma etched silicon substrate. The structures are hexagonally arranged and the pitch is 10 μm.
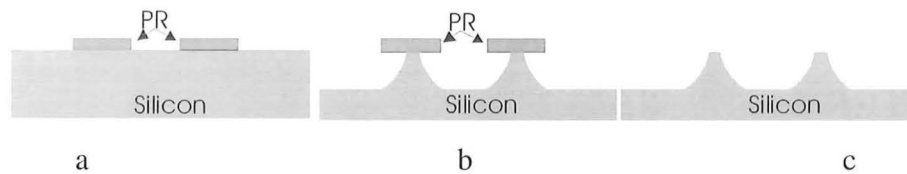
Figure 3-27: Schematic of the SF$_6$ plasma texturing. (a). Before texturing.(b) After texturing. (c) After removal of photoresist.

Since there is no sidewall passivation, SF$_6$ plasma cause severe undercut as shown schematically in Figure 3-27 .

3.7 Summary

The SF$_6$/ O$_2$ flow rates influence the formation of micrograss that helps in reducing the reflection. For SF$_6$/ O$_2$ flow rate of 40/25 sccm and higher micrograss was observed. Micrograss was more likely to occur in narrower holes than in wider holes. The ions can etch the narrow structures easily in wider holes as shown schematically in Figure 3-10. This was not consistence as other factors such as contamination of other gases and other etched residuals in the RIE chamber affect the reactive ion etching greatly.

Optimised light trapping structures were achieved by RIE texturing of hexagonally arranged holes and cone structures. Black silicon was achieved by maskless texturing. This was achieved by SF$_6$/O$_2$ RIE texturing.

The cone type structures exhibited excellent minimum reflectance less than 0.5 % for a wide range of solar spectrum regardless of wavelengths. The reflectance of black silicon was also less than 1% for over a wide range of solar spectrum regardless of wavelengths. The detailed reflectance results are presented in chapter 6.

The oxygen-less SF$_6$ plasma texturing leads to the formation of anisotropic structures. Maskless SF$_6$ plasma etching can also be used to etch away the saw damage in unpolished wafers. It will lead a relatively polished surface suitable for the solar cell fabrication. However maskless texturing using SF$_6$ plasma was not as successful as SF$_6$/O$_2$ plasma. However partial reduction in reflection is achieved and is discussed in the Chapter 4.

CHAPTER 4

MINORITY CARRIER LIFETIME MEASUREMENTS

4.1 Introduction

Minority carrier lifetime measurement is a very useful technique in monitoring the damage caused by the reactive ion etching. It is already reported that the surface recombination velocity is higher for the pyramid textured silicon substrates than the planar substrates [36] and is shown in Figure 4-1. Also the open circuit voltage of the solar cell could be predicted by measuring the minority carrier lifetime of the textured substrates. The theory, techniques and the results are presented in this chapter.
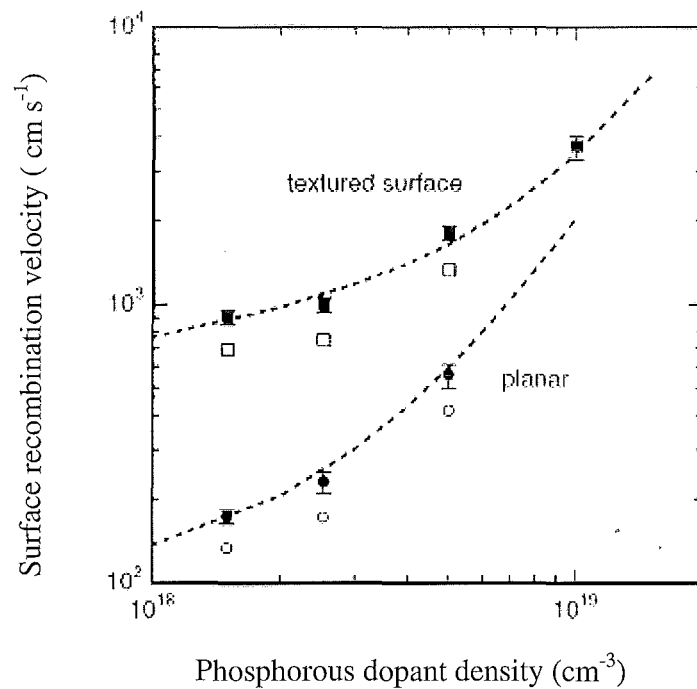
Figure 4-1: Surface recombination velocity of pyramid textured substrates and planer substrates [36].

4.2 Theory Behind The Carrier Lifetime Measurements

Surface recombination is a special case of Schokley-Read-Hall (SRH) recombination in which the localised states occur at the surface. Unlike bulk SRH centres however, these states do not usually occupy a single energy level, but rather form a set of states distributed across the band-gap. Surface recombination analysis is performed in terms of surface recombination velocities (SRV) instead of lifetimes. However, the principles are identical to bulk SRH recombination. A detailed description of the analysis of the general case in which the SRVs have arbitrary magnitude and may be injection-level dependent can be found elsewhere [17]. In the simpler case of a sample with a constant bulk lifetime τ_b , thickness W and a small constant SRV, S, that is the same on each surface, the effective lifetime is:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{2S}{W} \qquad\qquad 4\text{-}1$$

The requirement that S be small arises from the assumption that the surface recombination rate is not limited by the diffusion of carriers to the surfaces. The accuracy of this expression for various sample thicknesses and values of S has been discussed by Sproul for carrier decay mode [37]. In general in this thesis we are concerned with steady-state conditions, but in many cases the region of validity of Equation 4-1 will be similar for the two. In the extreme case of infinite surface recombination velocity, the effective lifetime will be dominated by the transit time of carriers to the surfaces, provided the bulk lifetime is not very small. Under steady-state conditions with a uniform generation profile, the effective lifetime in this case is given by[38].

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{12D}{W^2} \qquad\qquad 4\text{-}2$$

where D is the carrier diffusivity. In low-injection conditions, the value of D for the minority carriers should be used, while in high-injection an ambipolar diffusivity is appropriate. Note that this expression is slightly different to that corresponding to transient decay mode, for which the second term on the right is $\pi^2 D/W^2$ [17]. This amounts to a 22% higher effective lifetime measured in decay mode for a sample with a long bulk lifetime. For lower bulk lifetimes, the difference is reduced. The discrepancy arises because carriers near the surface recombine quickly in decay mode, leaving those further away to diffuse to the surfaces, whereas in steady-state

conditions carriers are constantly being generated near the surfaces, allowing their short lifetime to be incorporated throughout the entire measurement. It should be noted that neither lifetime is more 'correct' than the other from a fundamental viewpoint. However, it is definitely true that the steady-state result is more applicable to solar cells, which, of course, operate under steady-state illumination.

4.3   Types of Recombination

The energy lost by the electron in moving from the conduction band to the valance band can be given off either as heat or as a photon. Several types of recombination mechanisms exist, depending on how the electron releases its energy.

4.3.1   Radiative Recombination
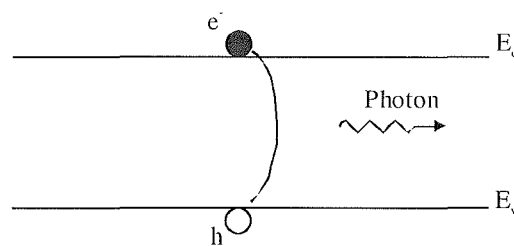
Figure 4-2: Energy band visualization of radiative recombination.

Radiative recombination is the recombination mechanism which dominates in devices such as LEDs and lasers made from direct band gap materials. However, for photovoltaic devices (which for most terrestrial applications are made out of silicon), radiative recombination is unimportant since silicon's band gap is an "indirect" band gap which does not allow a direct transition for an electron in the valence band to the conduction band. The key characteristics of radiative recombination are:

- In radiative recombination, an electron directly combines with a hole in the valance band and releases a photon.

- The emitted photon has energy similar to the band gap and is therefore only weakly absorbed - it can therefore exit the semiconductor.

4.3.2 Recombination through Defect Levels
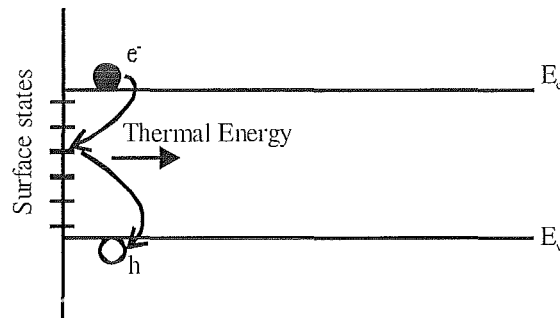
Figure 4-3: Energy band visualization of recombination at a semiconductor surface, where multiple defect states exist.

Recombination through defects, also called Schokley-Read-Hall recombination does not occur in perfectly pure, undefected material. SRH recombination is a two-step process. These are:

- An electron (or hole) is trapped by an energy state in the forbidden region which is introduced via defects in the crystal lattice. These defects can either be unintentionally introduced or can have been deliberately added to the material, for example by doping the material.

- If a hole (or an electron) moves up to the same energy state before the electron is thermally re-emitted into the conduction band, then it recombines.

The rate at which a carrier moves into the energy level in the forbidden gap depends on the distance of the introduced energy level from either of the band edges. Therefore, if an energy state is introduced close to either band edge, recombination is less likely to occur as the electron is likely to be re-emitted to the conduction band edge rather than recombine with a hole which moves into the same energy state from the valence band. For this reason, energy levels near mid-gap are very effective for recombination

4.3.3 Auger Recombination
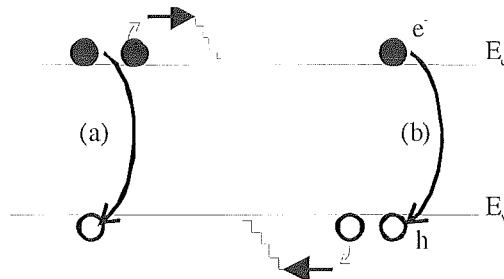
Figure 4-4: Energy band visualization of Auger recombination with the excess energy transferred to: (a) a conduction band electron; (b) a valence band hole.

In Auger recombination, a carrier recombines, but instead of emitting a photon it gives off its excess energy to another carrier in the same band. This then thermalises down to its respective band edge. Auger recombination is most important in heavily doped or heavily excited material.

4.4 Plasma Enhanced Chemical Vapour Deposited Silicon Nitride Passivation for lifetime measurements.

The thermally grown SiO_2 films provide very good passivation on silicon wafers. However they feature several severe drawbacks mainly due to high processing temperatures.

- In combination with contaminated furnace tubes, high temperatures can severely degrade the bulk carrier lifetime of silicon wafer, requiring expensive electronic grade processing gases and time and energy consuming furnace cleaning steps.

- The large oxygen content of CZ-silicon wafers is known to lead to oxygen precipitation during lengthy high-temperature (~1000° C) treatment, which may reduce the bulk carrier lifetime [39].

- Metal contacts cannot withstand the high oxidation temperatures, so that the oxide must be opened by means of photolithography and chemical etching or by means

of laser/mechanical scribing prior to the formation of the contacts, strongly affecting the cost of the finished cells.

Also SiO_2 does not provide efficient reduction of reflection losses because of their small refractive index of 1.46. This is explained in Chapter 6. However, stoichiometric silicon nitride was used for only passivating the silicon wafer prior to the minority carrier lifetime measurement.

4.5   Prediction of the Open-circuit Voltage of Solar Cells

The quality of a solar cell, given by its open-circuit voltage, short-circuit current and fill factor, cannot be fully assessed until the fabrication of the device has been completed. While of ultimate importance, these parameters do not provide information about the physical mechanisms that determine the performance of the solar cell.

The conductance (the inverse sheet resistance) of a semiconductor changes when exposed to light. The photoconductance is a particularly important parameter for solar cells and is directly related to the minority carrier lifetime and, on the other hand, it is also intimately related to the open-circuit voltage. It is, therefore, ideally suited to establish a close link between the final device performance and the optimization of the recombination parameters in the material. In addition, the photoconductance under steady or quasi-steady illumination can be measured in a convenient, contactless manner using very simple apparatus and procedures. The detail of the experimental technique is given in the chapter 2.

4.5.1   Relationship between Photoconductance, Effective Minority Carriers Lifetime and Open-Circuit Voltage

The minority carrier lifetime of a semiconductor material is directly related to its photoconductance. Under steady-state illumination, a balance exists between the generation and the recombination of electron-hole pairs, i.e. $J_{ph} = J_{rec}$, expressing them as current densities. As a consequence of this balance, an excess concentration of electrons and holes is established in the material. The total recombination in a sample of thickness W can be conveniently expressed in terms of an average excess minority carrier density, Δn_{av}, and an effective minority carrier lifetime, τ_{eff}

$$J_{ph} = \frac{q\int_0^w \Delta n dx}{\tau_{eff}} = \frac{q\Delta n_{av}W}{\tau_{eff}} \qquad\qquad 4\text{-}3$$

which essentially is a version of the classic relationship $\Delta n = G_L\tau_{eff}$. The photogenerated excess electron and hole densities, $\Delta n = \Delta p$, also result in an increase in the conductance of the sample. The excess photoconductance, i.e. the difference between the conductance measured under illumination and in the dark, is given by:

$$\sigma_L = q\int_0^W (\Delta n\mu_n + \Delta p\mu_p)dx \approx q\Delta n_{av}(\mu_n + \mu_p)W \qquad\qquad 4\text{-}4$$

For many semiconductors the electron and hole mobilities are well known and a measurement of the photoconductance is, therefore, a nearly direct way of probing for the excess carrier density. In general, the excess carrier density is position dependent; the total number of carriers divided by the wafer thickness gives the average carrier density, Δn_{av}, used in Equations 4-1 and 4-2 [40]. The approximation in Equation 4-4 assumes that the electron and hole mobilities are approximately constant across the sample and their possible carrier density dependence is accommodated for by evaluating them at the average carrier concentration. Equation 4-4 should be iterated to find a self-consistent set of values for both Δn_{av} and $\mu_n + \mu_p$, although this iteration is not necessary if the photogenerated excess carrier density is much smaller than the majority carrier density. For monocrystalline silicon, the dependence of electron and hole mobilities on both the dopant density and the injection level can be found in the literature [41, 42] . The application of Equation 4-4 to some materials might not be straightforward; for example, the mobility in some polycrystalline semiconductors might be orientation dependent. Combining Equations 4-3 and 4-4, the effective minority carrier lifetime can be determined as

$$\tau_{eff} = \frac{\sigma_L}{J_{ph}(\mu_n + \mu_p)} \qquad\qquad 4\text{-}5$$

The conductance and the incident light intensity can be measured using a calibrated instrument and a reference solar cell or photodetector, respectively. For a given irradiance, the total photogeneration within the sample J_{ph} can be easily and accurately estimated using available computer programs[20] or published tables and graphs[21]. The evaluation of J_{ph} requires that the absorption coefficient and the optical properties of the sample are known. The application of Equation 4-5 to materials that are not as comprehensively characterized as crystalline silicon might be problematic. This is illustrated by the case of amorphous silicon, for which photoconductance measurements have been used frequently to determine not the lifetime but just the mobility lifetime product. Photoconductance and open circuit voltage are measures of the excess minority carrier density. For a p-n junction solar cell made on a p-type wafer with dopant density N_A, the open-circuit voltage can be calculated from the electron and hole densities at the boundary of the space charge region.

$$V_{oc} = \frac{KT}{q} \ln\left(\frac{(\Delta n(0)[N_A + \Delta p(0)]}{n_i^2} \right)$$ 4-6

where the photogenerated electron density has been assumed to be much higher than the equilibrium electron concentration, $\Delta n(0) >> n_{eq}$; subject to this assumption, Equation 4-6 is valid for an arbitrary injection level. Note that the local excess minority carrier density, $\Delta n(0)$, is not, in general, identical to the average Δn_{av} that can be obtained from a measurement of the photoconductance using Equation 4-4.

4.6 Minority carrier lifetime measurements of plasma textured substrates

The Quasi-Steady-State Photo Conductance (QSSPC) technique [43] was used to measure the effective carrier lifetimes of the textured samples. This technique is based on the simultaneous measurement of the excess conductance of the wafer, through an inductively-coupled coil, and the generation rate, via a calibrated solar cell. The schematic of the experimental technique is given in Chapter 2. Under steady-state conditions, the generation and recombination rates are equal, and the lifetime is simply proportional to the ratio of the excess conductance and the generation rate. In this measurement, not only

the minority carriers lifetime can be deduced, but the implied open circuit voltage can be calculated.

Prior to lifetime measurement, it is essential to deposit a passivating film; in this case 80 nm stoichiometric Si_3N_4 was deposited on the wafer surfaces using PECVD method. Si_3N_4 passivation works by field-effect passivation, since the films contain relatively high densities of fixed positive charge. Silicon dioxide, on the other hand, passivates the surface chemically, by bonding with dangling bonds at the surface. In the absence of excessive surface damage, such films reduce surface recombination to the extent that the resulting effective lifetime is often dominated by the bulk lifetime of a sample. This is reflected by the lifetime measurements on the FZ control samples (see Figure 4-6), which have planar surfaces produced by chemical etching. Typical sample preparation for minority carriers lifetime measurement is illustrated.

Pattern transfer using photolithography

⇩

Plasma etching

⇩

Wet chemical DRE (except for reference)

⇩

RCA1 & RCA2 cleaning

⇩

PECVD Si_xN_y passivation

⇩

Lifetime measurement Using QSSPCD
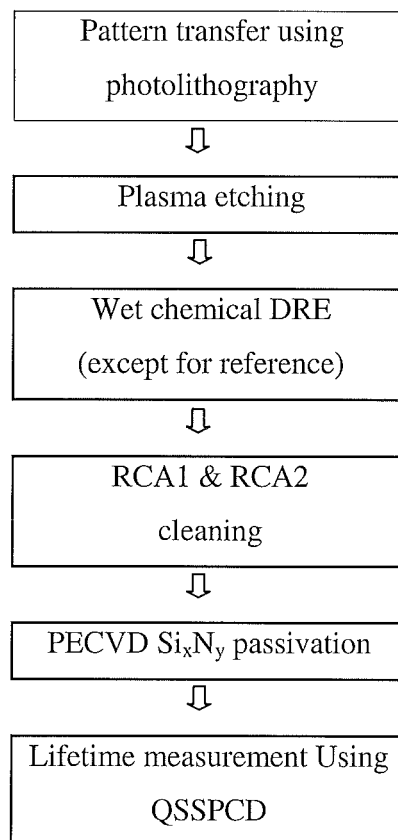
Figure 4-5: processing and characterisation steps involved in plasma textured silicon substrates.

Chemical Defect Removal Etching (DRE)

In most of the cases, plasma etching creates damage to the bulk near the surface and hence the minority carrier lifetime of the wafers. A thin layer of the textured surface was removed by wet chemical etching to reduce the defects caused by plasma. For this purpose, a mixture of HNO_3 (70%) and HF (40%) was used. HNO_3: HF (50:1) etches p-type silicon at around 0.5 μm / minute at room temperature. This process is called Defect Removal Etching (DRE).

Surface Passivation for lifetime measurement

PECVD silicon nitride was used to passivate the substrates prior to the minority carrier lifetime measurements. Remote plasma method was used to deposit about 80 nm of stoichiometric Si_3N_4 on textured substrates as well as reference substrates.

4.6.1 SF$_6$/O$_2$ plasma textured substrates

In this experiment, we measured the minority carrier lifetime of the Silicon substrate textured in the Oxford Plasmalab 80 reactive ion etcher using SF_6/O_2 plasma. The substrate description and the RIE etch parameters are given in Table 4-1.

Table 4-1 : Etch process and wafer specification for RIE etching

Substrate specification	Etch conditions
Growth = (100), FZ – silicon	SF_6 = 90 sccm,
Type = p-type ,	O_2 =10 sccm
Thickness = 0.5 μm	T = -100°C,
Resistivity = ~10 Ω cm,	RF power =150W,
Size = 3x3 cm,	Pressure= 70 mT
Polishing = Chemically polished (shiny etched).	dc bias = -103 V (self)

The minority carrier lifetime result is shown in the Figure 4-6. Minority carrier lifetime was measured for an un-textured substrate, a textured substrate without DRE and a textured substrate with DRE. After the texturing, the minority carrier lifetime is reduced and then recovered after a wet chemical DRE. For comparison, all effective lifetimes are given here at an excess carrier density of 1x 10^{15} cm^{-3}.
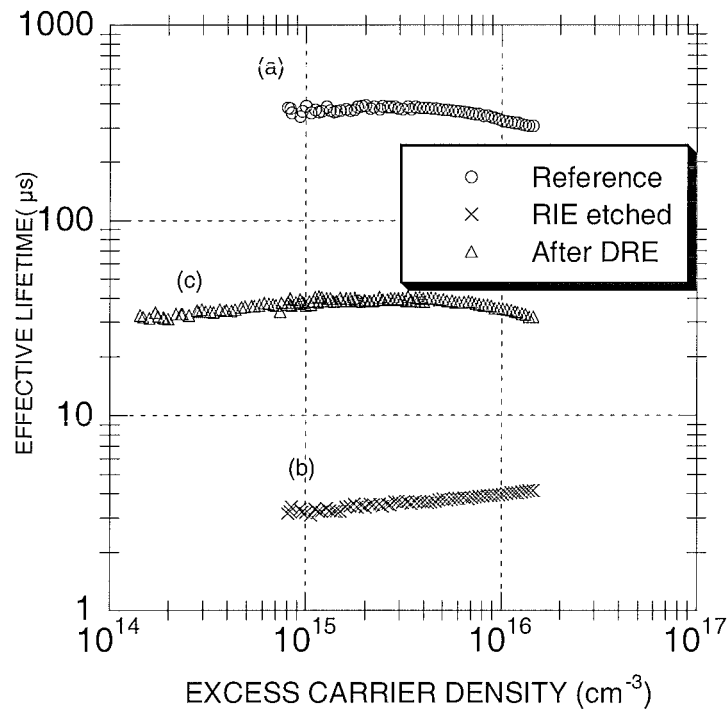
Figure 4-6: Minority carriers lifetime of (a) Reference wafer (b) RIE textured (hole-type) substrate without DRE (c) RIE textured (hole-type) substrate after DRE

The effective lifetime of the sample after DRE is 36µs, compared with 2 or 3µs for the RIE etched sample without DRE. This corresponds to an implied one-sun open-circuit voltage of around 605mV compared to about 550mV before DRE. Each order of magnitude increase in lifetime gives an extra 60mV, since the voltage is logarithmically dependent on the carrier density (and hence lifetime), assuming an ideality factor of 1. Thus the damage removal etch can be used to produce low defects surfaces and further reduction could be possible for deeper DRE.

4.6.2 ICP textured substrates

To investigate the influence of the plasma type on the plasma induced defects, a few ICP textured samples were studied by measuring their minority carriers lifetimes. The samples were prepared and sent to the Technical University of Delft, Netherlands, for the ICP etching. The so called Bosch process, described in the Chapter 2, was employed to texture theses substrates. The substrate description and the ICP etch parameters are given in Table 4-2.

Table 4-2: Substrate specification and etch parameters for ICP etching

Substrate specification	Etch conditions- Bosch process
Growth =(100), FZ – silicon	SF_6 = 150sccm-6 sec
Type = p-type ,	C_4F_8 = 150 sccm -3 sec
Thickness = 0.5 mm	T = 25°C,
Resistivity = ~10 Ω cm,	RF power = 2000w,
Size = 3x3 cm,	Pressure = 70 mT
Polishing = Chemically polished (shiny etched).	dc bias = -90 V
	Time = 100 sec

The minority carrier lifetime measurement is shown in Figure 4-7. The reference wafer (curve a) showed 350 μs at an excess carrier density of 1x 10^{15}/cm. But the ICP etched substrate (curve b) showed only about 18 μs. However, after 4 minutes of DRE to remove about 2 μm of damaged silicon layer, the lifetime (curve c) was recovered to 250μs..
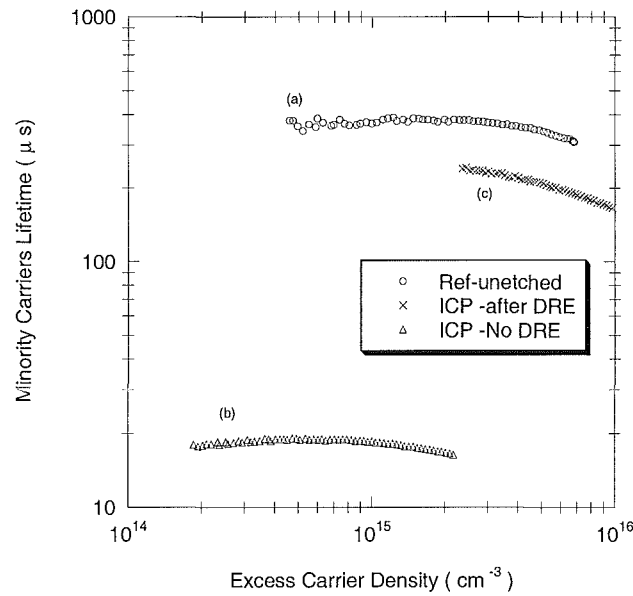
Figure 4-7: Minority carriers lifetime of (a) Reference wafer (b) ICP textured (hole-type) substrate without DRE (c) ICP textured (hole-type) substrate after DRE.

4.6.3 SF₆ plasma textured substrates

Oxygen added SF_6 plasma etches faster, but also causes more defects [44]. In this experiment we textured silicon substrates using SF_6 plasma without oxygen in the Reactive Ion Etcher to isolate the defects introduced by oxygen from the RIE process. Very high selectivity of silicon / photoresist etching is another advantage of using SF_6. A mask with hexagonally-arranged circular dots of 8 micron diameter on a 10 micron pitch was photolithographically transferred to the silicon substrates and was used as an etch mask for SF_6 texturing process.

Table 4-3: Etch process and wafer specification for SF_6 plasma etching

Substrate specification	Etch conditions
Growth =(100), FZ – silicon	SF_6 = 160 sccm,
Type = p-type ,	T =-100°C,
Thickness = 0.3 mm	RF =200w,
Resistivity = ~5 Ω cm,	P =150 mT
Size = 50mm (diameter	dc bias = -102 V (self)
Polishing = Double side polished	Time = 4 min

AZ 4620 positive photoresist was used as an etch mask. Previously, a metallic etch mask was needed for the SF_6/ O_2 base plasma texturing. HNO_3: HF (50:1) solution for a period of 5 min at room temperature was used to remove the damaged layer of thickness about 2-3 μm.
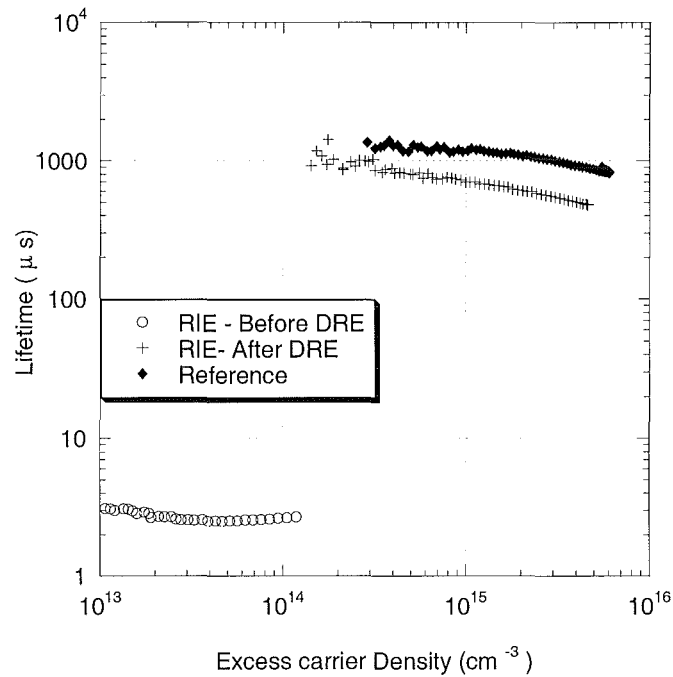
Figure 4-8: Minority Carriers Lifetimes of SF_6 plasma (RIE) textured (hole type) Silicon substrates before and after chemical defect removal etching is compared with an un-etched reference sample.

The minority carrier lifetime of the SF_6 plasma textured in the Oxford Plasmalab 80 etcher is shown in Figure 4-8. Even though oxygen was not used for this experiment, the lifetime result was not promising. However, the lifetime was improved dramatically after 5 min DRE, which removed about 2-3 μm of damaged layer.

4.6.4 ECR plasma textured substrates

A mask with hexagonally-arranged circular dots of 8 μm diameter on a 10 μm pitch was photolithographically transferred to the silicon substrates and was used as an etch mask for ECR plasma texturing process. AZ 4620 positive photoresist was used as an etch mask

in place of the metal etch masks which were used in our previous work. This is to eliminate any lift off processes and develop a method where only dry etching is employed.

Table 4-4 : The substrate specification and the etch conditions for the ECR etching

Substrate specification	Etch conditions
Growth =(100), FZ – silicon Type = p-type , Thickness = 0.3 μm Resistivity = ~5 Ω cm, Size = 50mm (diameter) Polishing = Double side polished	SF_6 = 22.5 sccm, T =250 K RF power=400W, P =1.5 mT dc bias = -18 V (self) Time = 8 min

The substrates were etched for 8 minutes in the High Density Plasma (HDP) with the Electron Cyclotron Resonance (ECR) source etcher to obtain a 7 μm deep structure. This ECR etching was done at Delft Institute of Microelectronics and Submicron Technology (DIMES), the Delft University of Technology, the Netherlands.
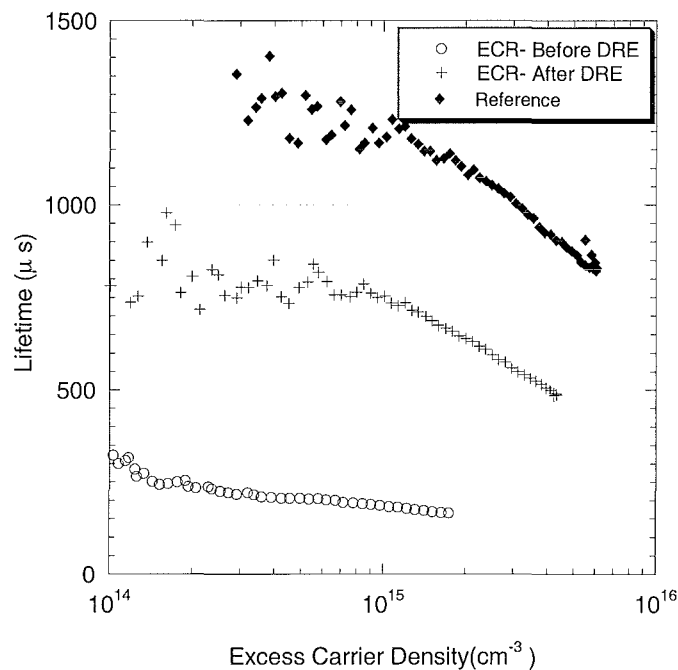
Figure 4-9: Minority Carriers Lifetimes of SF6 plasma (ECR) textured (hole type) silicon substrates before and after chemical defect removal etching is compared with an un-etched reference sample.

For comparison, one textured substrate was etched for 5 min in HNO_3/HF (50:1) solution to remove 2-3 μm of silicon layer. This ECR reactor was operated at 2.45 GHz. The etch condition and the substrate specification is shown in Table 4-4. The minority carrier lifetime of the ECR etched substrate is shown in Figure 4-9.

In the ECR textured substrates, the minority carrier lifetime obtained after the DRE corresponds to an implied one-sun open-circuit voltage of around 680mV compared to about 640mV before DRE. It is interesting to notice that for both ECR and RIE textured substrates the minority carrier lifetime can be recovered to such high level after the DRE step.

It is encouraging to note that for ECR textured wafer, the minority carriers lifetime is around 250 microseconds even before the DRE process. This indicates that high open circuit voltages can be obtained using these textured substrates even without DRE. This illustrates that with the proper choice of plasma conditions an effective plasma texturing process can be achieved.

4.6.5 Effect of etch temperature on minority carriers lifetime.

To study the effects of etching temperature on the RIE induced defects, the minority carrier lifetimes have been measured for substrates etched at 300K and at 173K in an SF_6 plasma. It is found that the minority carrier lifetime is significantly higher for substrates etched at 300K than those etched at 173K as shown in Figure 4-10. This result is obtained after a 1 minute DRE step and indicates that increasing the temperature during etching helps in annealing the structural damage as it forms.
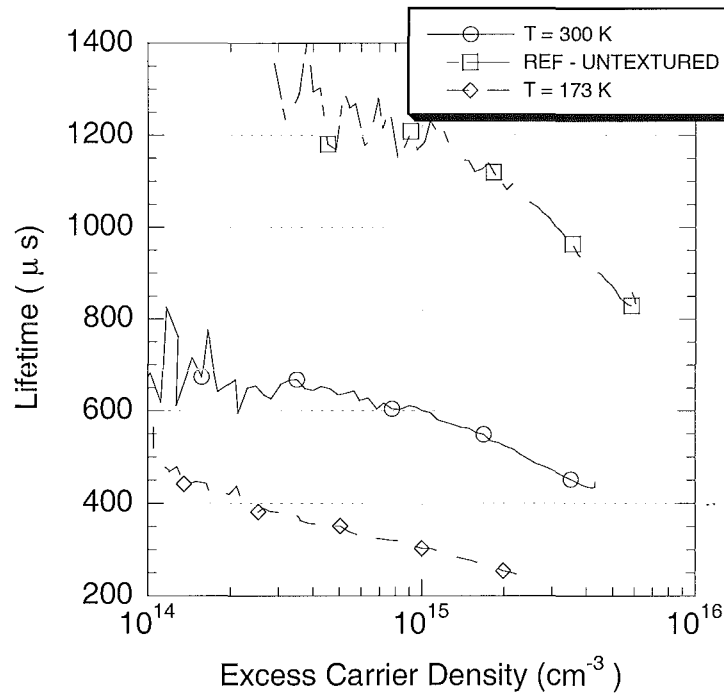
Figure 4-10: Minority carriers lifetime of substrates textured at 300 K and 173 K are compared with the reference substrate.

4.6.6 The effect of surface area increment due to plasma texturing

In our previous experiments, we assumed that the drop in minority carriers lifetime in plasma textured silicon substrates is entirely due to the plasma induced defects. In this experimental work we made an attempt to quantify the defects contributed by the increment of surface area due to the plasma texturing.

The origin and nature of defects induced in the bulk and at the surface due to texturing could be better understood by measuring the minority carrier lifetime and implied open circuit voltage for cells having different surface areas.

Minority carrier lifetimes of various silicon substrates were measured using the Quasi Steady State Photo Conductance technique and the corresponding implied V_{oc} were calculated. The starting silicon substrates were 50mm in diameter, double side polished, <100> oriented, p-type, FZ-Silicon of 5Ω cm resistivity. Three different patterns were photolithographically defined and the photoresist was used as an etch mask for reactive

ion etching (RIE). Atomic Force Microscopy (AFM) data and SURFER8 computer software were used to calculate the textured surface areas.
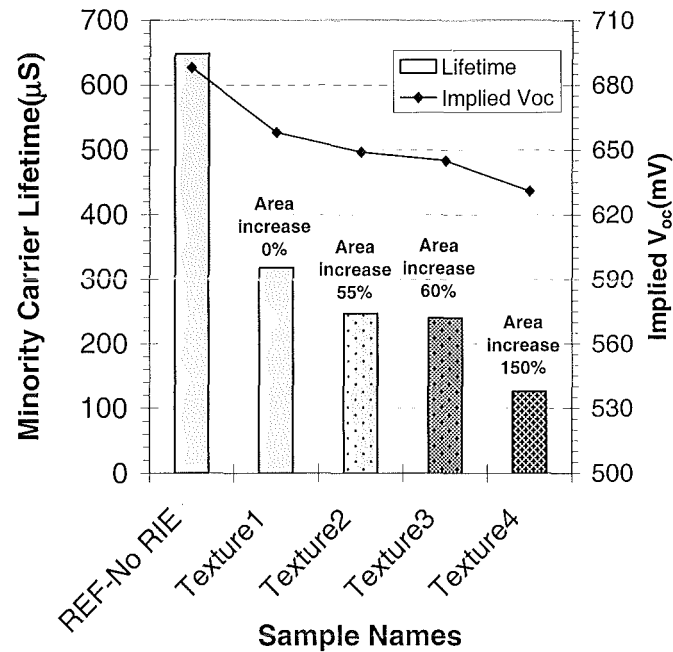
Figure 4-11: Minority carriers lifetime and implied V_{oc} of RIE textured FZ-Si for substrates with different surface areas.

Figure 4-11 shows a comparison of the effective minority carriers lifetime measured on a reference substrate and a SF_6 plasma textured substrate. Texture1 has a smooth polished surface after a maskless etch process while the other substrates have various textured structures. By using the same etching parameters for all substrates, but forming structures with different surface areas, it was possible to study the influence of surface area on minority carrier lifetimes and the implied open circuit voltage of the substrates.
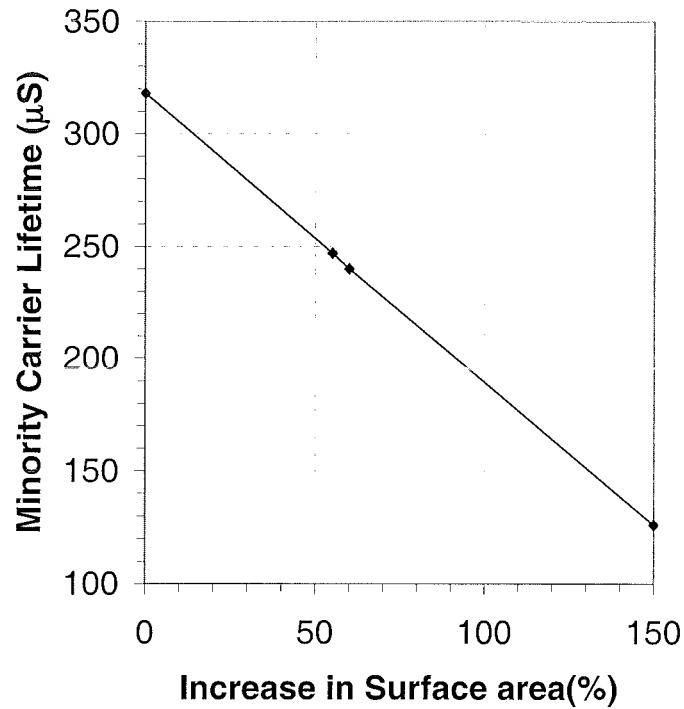
Figure 4-12: The minority carrier lifetime of RIE textured substrates as a function of increase in surface area.

The textured surface area increases up to 150% compared to untextured substrates. All substrates were subjected to a defect removal etching (DRE) in HF:HNO$_3$ (1:50) solution in order to remove a layer of about 250nm prior to Si$_3$N$_4$ passivation. Figure 4-12 shows a linear decrease in minority carrier lifetime as the textured area increases. Therefore, the drop in minority carrier lifetime is not only due to plasma induced damage, but partly due to an increase in surface recombination due to an increase in the surface area.

4.7   Surface Area Calculation

The surface area increment was calculated for a few geometrical structures using a mathematical software called MAPLE.

4.7.1 Hole-type structures

The 3-D algebraic equation 4-7 and 4-8 are used to generate the geometrical structures shown in Figure 4-13 and the surface area was calculated mathematically.

$$Z = \frac{3}{4}(x^2 + y^2)$$ 4-7

$$Z = \frac{1}{5}(x^4 + y^4)$$ 4-8

The increment of these structures over a planer surface is calculated as 154% for structure shown in Figure 4-13 and is 205% for the structure shown in Figure 4-14. These structure are similar to the RIE textured surface shown in Figure 3-17.

Figure 4-13: Over etched hexagonally arranged holes in 6 mm deep and in 4 mm pitch generated by the Equation 4-7.	**Figure 4-14:** Over etched hexagonally arranged holes in 6 mm deep and in 4 mm pitch generated by the Equation4-8.
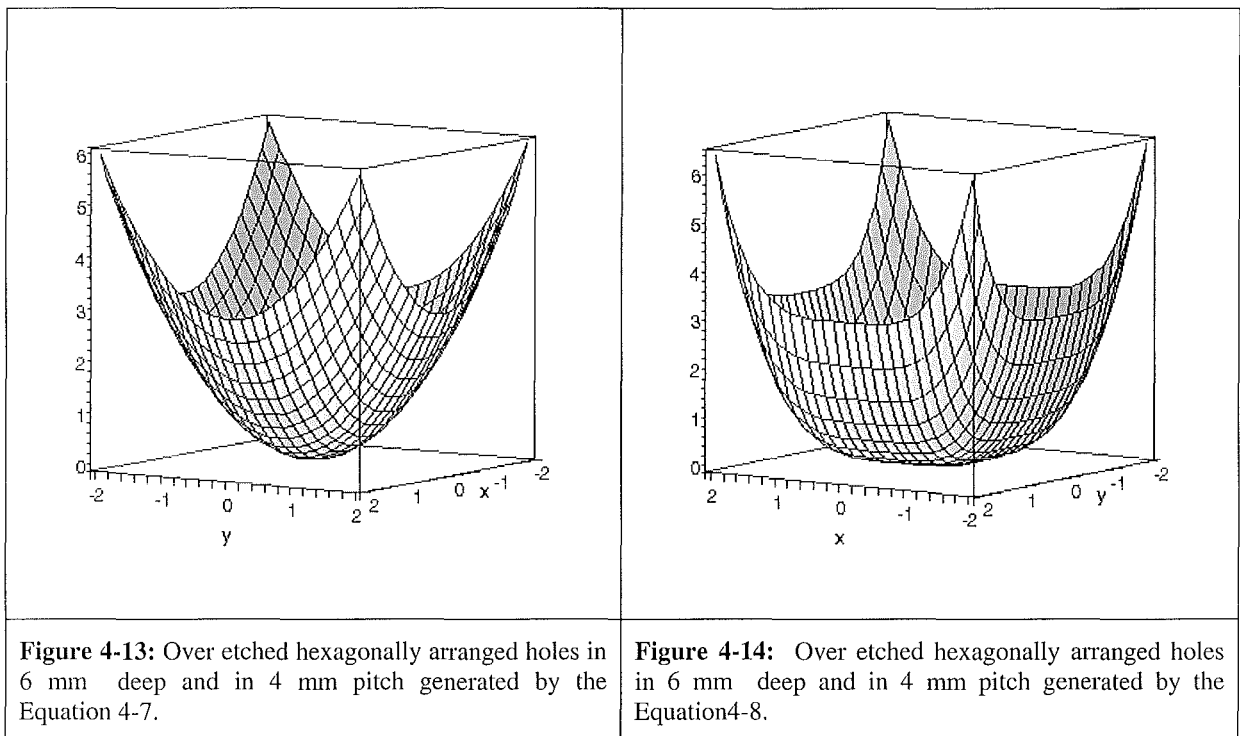
4.7.2 Column type structures

A number of column type structures are also generated using algebraic equations and their surface area increments were calculated
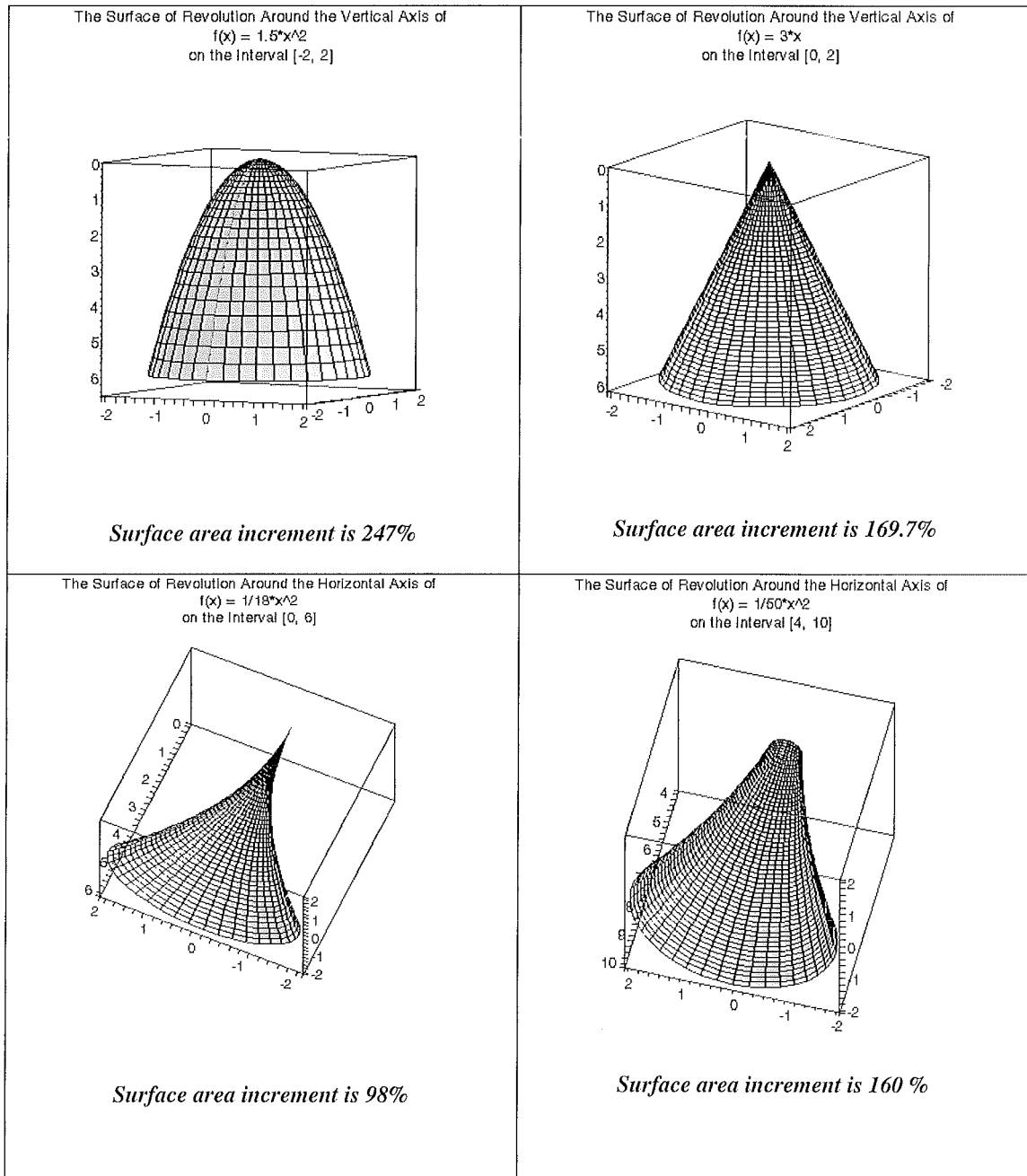
Figure 4-15: A number of column structures and their surface area increments over a planer surface are calculated using MAPLE software.

4.7.3 Pyramid Structures formed by (1,1,1) planes

The conventional alkaline etching forms square pyramids by exposing the <111> crystallographic planes in c-Si substrates. Figure 4-16 shows the <111> planes and the pyramid.

(a)   (b)
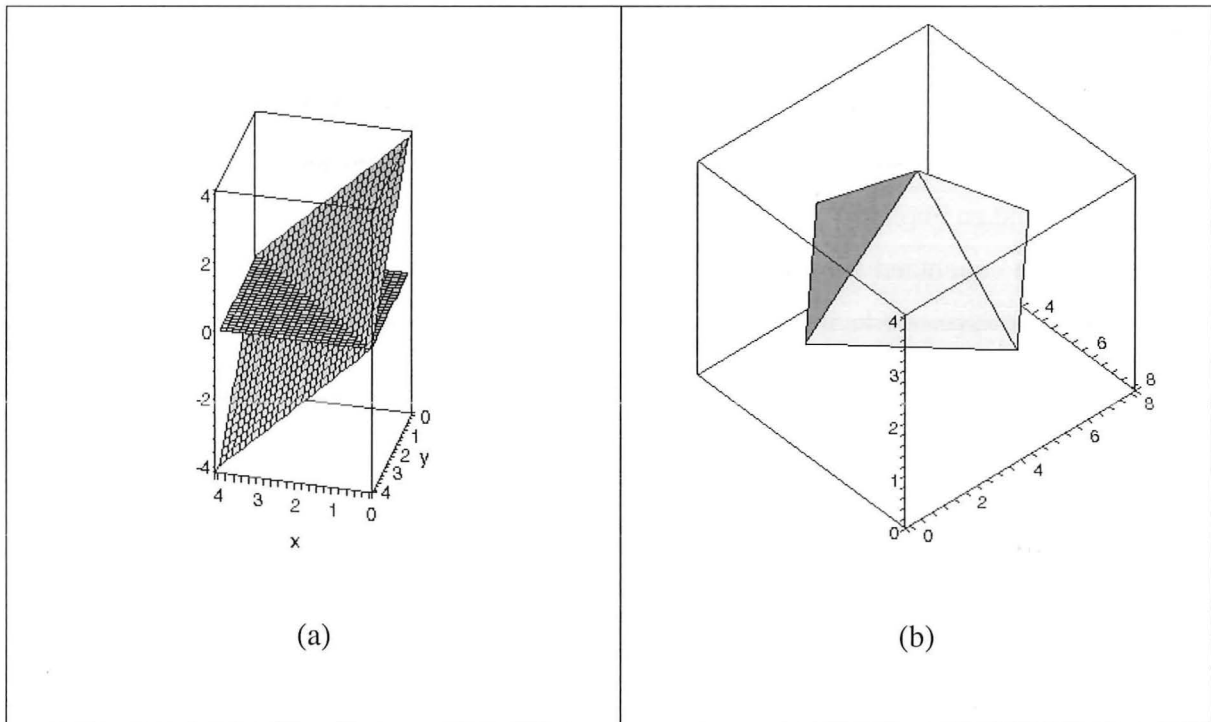
Figure 4-16: (a) <1,1,1> crystallographic planes **(b)** The pyramid structures formed by (1,1,1) crystallographic planes (c) cross section of a pyramid and apex angle.

The total pyramid area increment is calculated as 73%

4.8   Summary

A high minority carrier lifetime is an indication of low defect concentration and is essential for obtaining high collection efficiency in silicon solar cells.

It is demonstrated that the plasma induced damage is very high in the case of RIE textured substrates compared with the ICP textured substrates. This is illustrated by the extremely low minority carrier lifetime of less than 10 μS for RIE treated substrates. It is interesting

to notice that for both ICP and RIE textured substrates the minority carrier lifetime can be recovered to such high level after the chemical defect removal step.

The ECR created less damage compared to other plasma texturing methods. The minority carrier lifetime of the ECR textured substrate showed about 200 μs which is equivalent to 640 mV of implied open circuit voltage.

These results indicate that most of the plasma generated damage propagates into a shallow layer beneath the surface, as it only requires the removal of between 2-3 microns to notice a significant improvement in minority carrier lifetime.

However, one of our latest results showed that, 10 minutes of low power (17W) RIE texturing using 20sccm SF_6 on FZ-Si of similar specification gave as high as 400 μs lifetime and an implied V_{oc} of 660mV without any DRE.

It can be concluded from the surface area calculation that the minority carrier lifetime drop due to surface area increment is proportional to the area increase due to texturing.

Therefore, the drop in minority carrier lifetime is not only due to plasma induced damage, but partly due to an increase in surface recombination due to an increase in the surface area.

CHAPTER 5

PHOTOLUMINESCENCE ANALYSIS

5.1 Introduction

During RIE treatment the etching surface is exposed to bombardment by energetic ions, which greatly enhances the reaction rate of the reactive gas with the semiconductor surface; however, the bombardment also causes contamination to the surface and produces substantial damage in the near surface region, introducing various defects. Surface and near-surface modifications resulting from RIE can greatly affect the performance of electronic devices such as solar cells. The composition of the reaction layer formed at the Si surface after pure SF_6 RIE has been studied mainly by surface-characterization techniques including x-ray photoemission spectroscopy [45] atomic force spectroscopy [46] and in situ Raman scattering spectroscopy [47]. Less is known about defects that may be produced further away from the surface. The electrically active defects induced by SF_6 plasma have been studied by means of deep level transient spectroscopy (DLTS) and infrared absorption, where the formation of carbon interstitial-related defects and divacancies has been reported [48]. Important information about the RIE-induced defects can be obtained also by photoluminescence (PL) spectroscopy [49],[50]. The obvious advantages of this method are its high sensitivity and selectivity, as well as the possibility to study the defect structure in the below-surface region without any particular sample preparation, as needed, for instance, for DLTS characterization. The PL studies performed for silicon substrates etched with various plasmas, such as carbon-tetrafluoride (CF_4), argon (Ar), deuterium (D), hydrogen-bromide (HBr), as well mixtures of these gases, have shown that the creation of specific defects is mainly determined by ion bombardment, while surface contamination from the plasma is less important. The crucial role of ion bombardment in the creation of extended defects giving rise to broad PL bands has also been pointed out, whereas ion implantation of carbon from the CF_4 plasma has been suggested as a source for the formation of the carbon-related centres

responsible for C and G lines [51]. However, the creation of these specific centres as a result of bombardment-induced displacement of oxygen and/or carbon atoms during RIE treatment was also shown to occur [49],[50].

5.2   Photoluminescence spectrum of pure silicon

When excess carriers are created in silicon, a small fraction will recombine by emitting light, the reverse of the absorption process.   At low temperatures, carriers will have relaxed into the lowest possible energy states before recombining, i.e. they will recombine from excitation states. Figure 5-1 shows the luminescence spectrum from silicon at 26 K at increasing magnification (obtained by widening the monochromatic slit, sacrificing resolution).

The peak height indicates the strength of the coupling of the phonon to the optical transaction and, hence, the strength of the inverse absorption process. The strongest peak at 1.10 eV corresponds to recombination with TO (Transverse-Optical) phonon emission. When more than one phonon is involved, there is scope for an increasing number of combinations of phonons, which will conserve momentum during the multiphonon process.
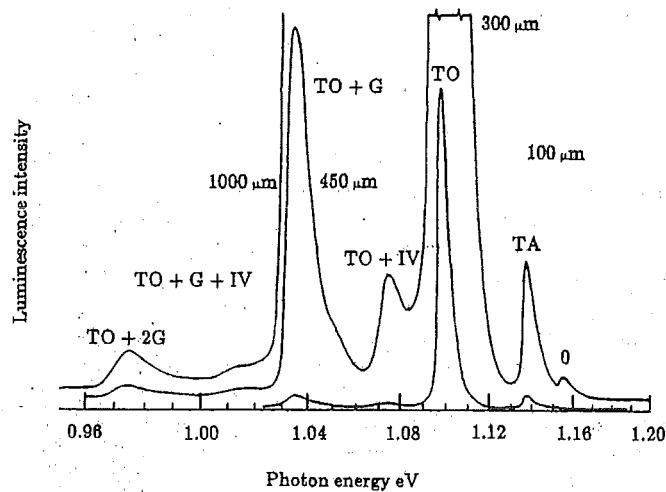
Figure 5-1:   Typical intrinsic photoluminescence of silicon at 26 K recorded with four different slit widths [52]
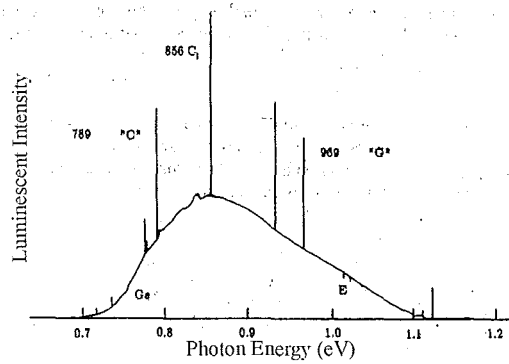
Figure 5-2: Photoluminescence spectrum of FZ- Silicon wafers.[53]

5.3 Photoluminescence Experimental Setup.

The aim of this experiment is to present the photoluminescence studies of defect formation in p-type silicon samples treated with SF_6 / O_2 plasma. The schematic of the experimental setup and equipment description are given in Chapter 2.

Photoluminescence (PL) was measured using the 514.5 nm line of an Ar^+ laser as an excitation source. The luminescence was dispersed with SPEX 1700 spectrometer with a liquid nitrogen cooled Germanium detector. The PL signal was recorded with a conventional lock-in technique in phase with the frequency of a mechanical chopper. PL measurement was done between 900meV to 1200 meV photon energy range because of the sensitivity of the Ge detector used.

The following measurements were done for mc-Si substrates. We identified few PL lines possibly due to the RIE induced defects in mc-Si substrates. SF_6 / O_2 plasma etched substrates were used in these experiments. These measurements were performed at room temperature as well as at 4.2K using liquid helium cooled probe.

5.4 Photoluminescence Measurement of Untextured Multicrystalline Silicon Substrates

In this experiment, all possible PL spectra were searched for the mc- Si wafer. The specification of the mc-Si wafer is as follows.

Table 5-1 : Specification of the mc-Si substrate

Doping	Resistivity	Thickness	Polishing
p-type (Boron)	10 Ω cm	200 μm.	Unpolished
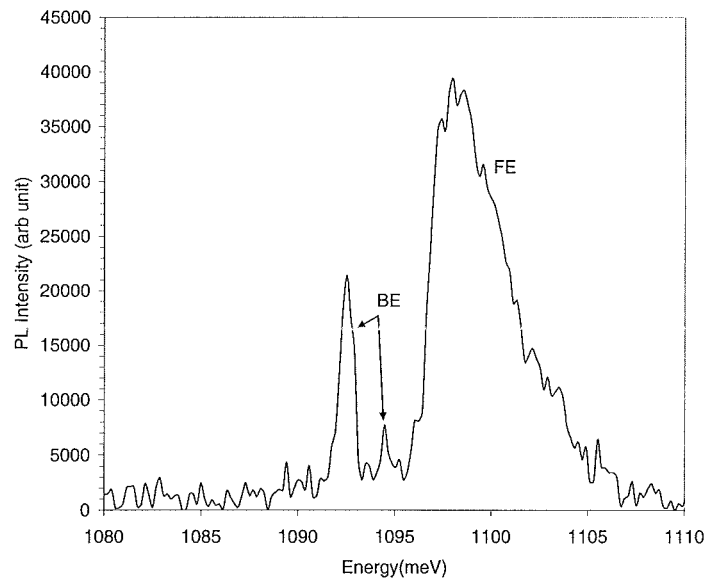
Figure 5-3: Photoluminescence spectrum measured at 4.3 K on the mc-Si reference wafer that was not exposed to plasma.

Only the TO line was able to be measured in the untextured mc-Si wafer. Figure 5-3 exhibits the well known features of the near band-gap PL in Si. The PL lines are due to bound exciton (BE) and free exciton (FE) in silicon [53]. The bound exciton and the free excitons in different phonon replicas are clearly resolved.

5.5 Photoluminescence Measurement of Untextured Cz-Silicon Substrates

In this experiment, all the possible PL spectra were searched for the Cz- Si wafer.
Table 5-2 shows the specification of the Cz-Si substrate.

Table 5-2: Specification of the Cz-Si substrate

Orientation	Doping	Resistivity	Thickness	Polishing
<100>	p-type (Boron)	10 Ω cm	450 μm.	Single side polished
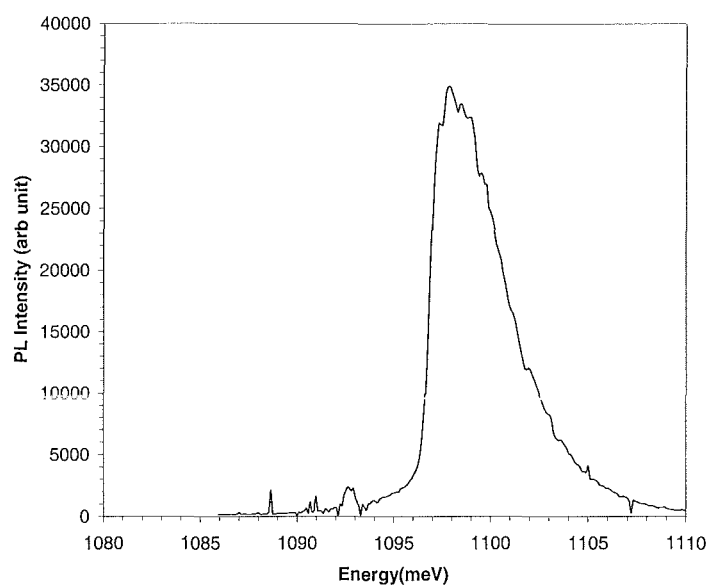
Figure 5-4: Photoluminescence spectrum measured at 4.3 K on the Cz-Si reference wafer that was not exposed to plasma. This is a merged figure and the relative intensity may not be in scale.

Only the PL lines at 1039 meV and 1100meV lines were able to be measured in the untextured Cz- Si wafer as shown in Figure 5-4.

5.6 Photoluminescence Measurement of RIE Textured mc-Si Wafers

The aim of this experiment is to present the photoluminescence studies of defect formation in p-type silicon samples treated with SF_6/O_2 plasma.

Boron doped mc-Si wafers of 10 Ω cm resistivity and 200 μm thickness were used for RIE texturing. A maskless etching technique was employed to texture the black silicon surface. The RIE etch condition is as follows.

Table 5-3:The RIE etch condition of the mc-Si wafer

SF_6 / O_2Flaw rate	Temperature	RF power	Etch Time	Etch pressure
90 / 25 sccm	173K	200W	30 min	80 mT

Liquid He was used to cool the samples for low temperature PL measurements. At low temperature, the PL spectrum lines were very sharp and free of noise.
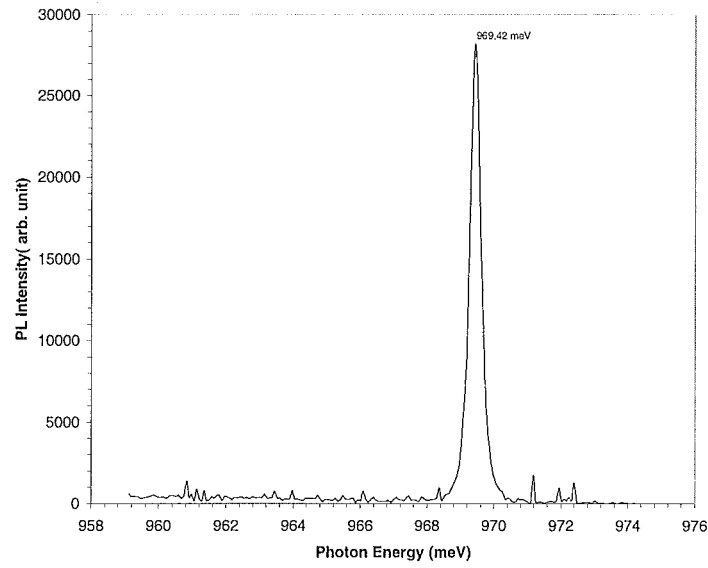
Figure 5-5: Reactive Ion Etched mc-Si substrate shows a sharp G line at 969.5 meV. PL measurement was performed at 4.3K.

The sharp G line at 969.5 could be associated with the plasma induced defects in this RIE textured mc-Si wafer.
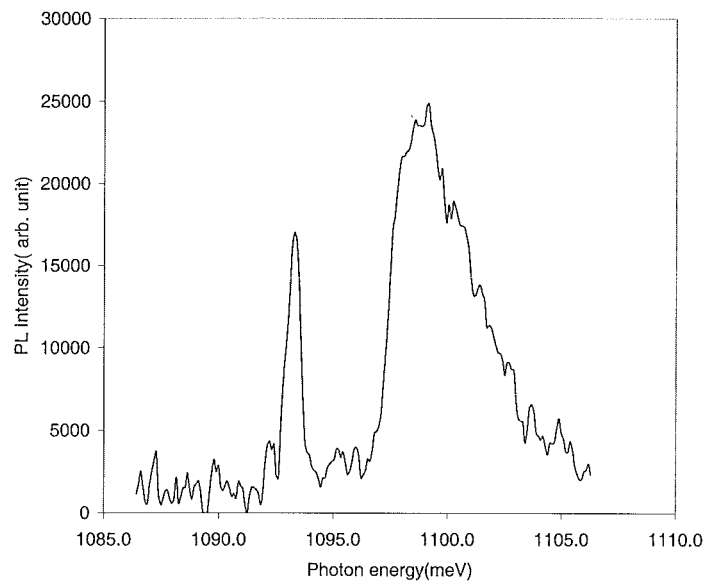
Figure 5-6: Photoluminescence of mc-Si etched with SF_6/O_2 measured at 4.2 K

5.6.1. Possible origin of 969.5 meV optical band

The 969 meV optical band shown in Figure 5-5 is one of the most intensively studied bands in silicon. In addition to this weak excitonic G line, another PL line associated with radiation defect is reported at the energy position at 789.3 meV, called C line [53]. Due to the wavelength limitation of the SPEX1700 used to measure the PL in this experiment, this particular C line could not be measured in this experiment.

Earlier studies [51] suggested that this defect centre consists of two carbon atoms and one unique silicon atom. The centre is produced by combining a mobile interstitial carbon atom C_i with a static substitution carbon atom C_s. The C_i may originate from radiation damage, when a silicon interstitial displaces a C_s atom or by injection of a C_i atom from outside the crystal, eg. from CF_4 plasma. However, the SF_6/O_2 plasma used in our experiment does not contain carbon atoms. Thus, the second mechanism of C-centre formation can be ruled out in our case

Normally, silicon wafers contain oxygen and carbon atoms in a small quantity. Also SF_6/O_2 plasma etching may inject O_2 related ions. A displacement of O and /or C atoms due to the ion bombardment may be a major mechanism for the formation of these defects [54].

Another study suggests that gamma–ray irradiation also produces this defect centre in silicon [55].

5.6.2. Depth of the defect centres associated with 969.5 meV optical band

It should be stressed that the depth of the near-surface layer probed in the PL experiment is determined by the depth of the photocreated carrier profile. The penetration depth of the 514.5 nm excitation light is about 1 μm at 2 K in silicon [54]. Taking into account the diffusion of photocreated carriers, the carrier profile should extend up to a few tens of microns, depending on the crystal quality. The intensity of a particular defect-related PL band depends crucially on the competition between various radiative and nonradiative channels. Thus, the PL spectroscopy permits only qualitative characterization of the surface condition after the plasma treatment.
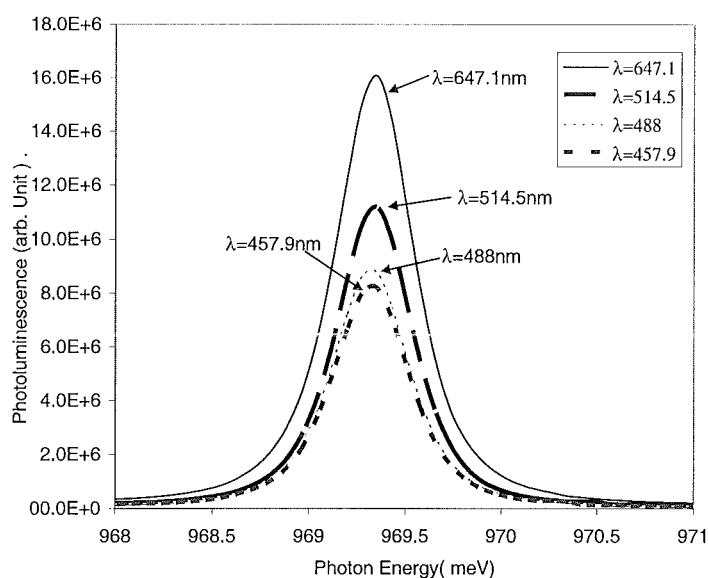
Figure 5-7: The relative PL intensities measured for the RIE etch mc- Silicon wafers when four different laser wavelengths were used. The power of the laser beam was kept constant at 100 mW.

When the wavelength of the laser was increased, the intensity of the PL spectrum was also increased, as shown in Figure 5-7. The penetration depth of this range of lasers is more than 1 μm in Si. This means, the particular luminescent centres are spread deeper. This is supported by our minority carrier lifetime measurements reported in Chapter 4.

5.7 Photoluminescence Measurement of RIE Textured Cz-Si Wafers

The 969.5 meV photoluminescence line was not seen in Cz-Si wafers. It is reported that the intensity of this particular line depends on the Carbon concentration in the wafer [53]. The C concentration may be too low to measure the PL in our Cz-Si wafer used in this experiment. However, the PL lines observed in the reference wafer were observed here as well and similar to Figure 5-4.

5.8 Effect of Annealing on RIE Textured mc-Si Wafers

RIE treatment in the SF_6/O_2 plasma leads to the appearance of the sharp excitonic G line with the energy position at 969.5 meV shown in Figure 5-5. They are absent in the un-

etched reference mc-Si wafers. When the etched wafer was annealed at 300° C, the *G* line at 969.5 meV was weakened and a new PL line at 950 meV appeared as shown in Figure 5-8.
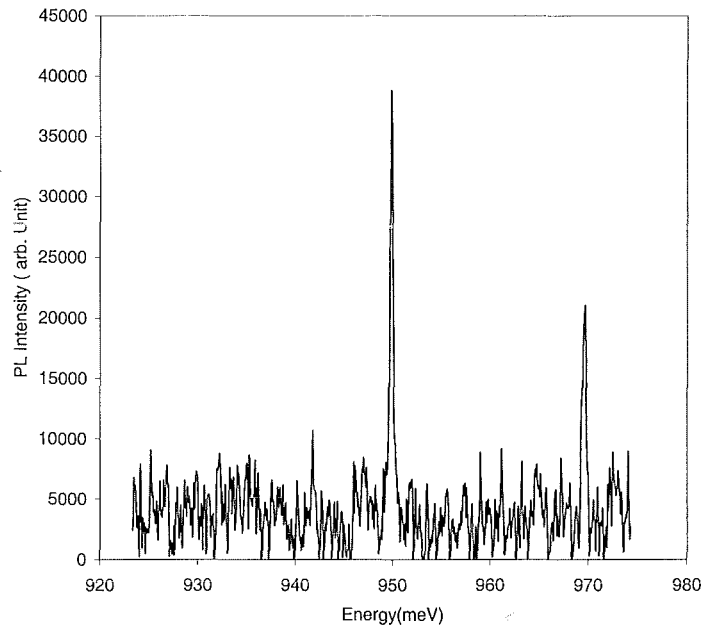
Figure 5-8: RIE etched mc-Si followed by annealing at 300°C for 30 min shows the weakening of G line at 969.5 meV and formation of a new line at 950meV. PL measurement was performed at room temperature.

When the SF_6/O_2 plasma etched mc-Si wafers were annealed at 400° C, those lines were further shifted towards the low energy end and splitting occurred. As can be seen in Figure 5-9, the intensity of the sharp *G* line at 969.5 meV gradually disappeared (or shifted) when annealed above 400° C. But another two PL lines started to appear when annealed above 300° C and they split and shifted towards the lower energy level when annealed above 400° C.
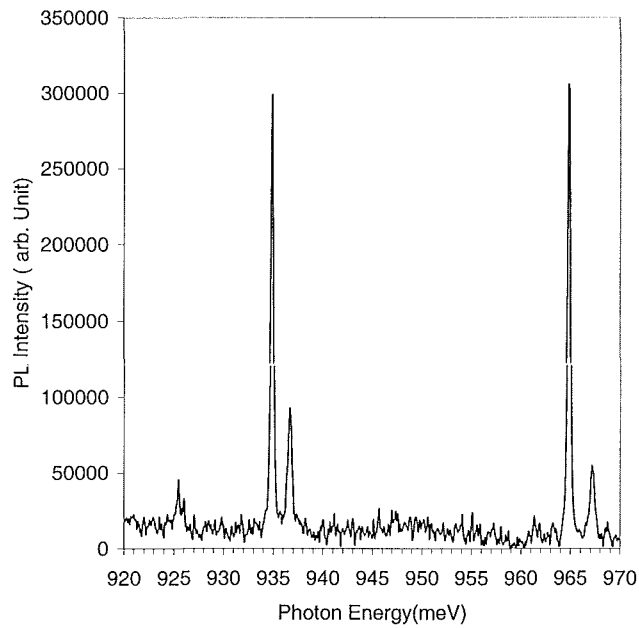
Figure 5-9: RIE etched mc-Si followed by annealing at 400° C for 30 min shows the disappearance of the G line at 969.5 meV and the two split lines at 935 meV and at 965meV and a weak line at 925.5 meV. PL measurement was performed at room temperature.
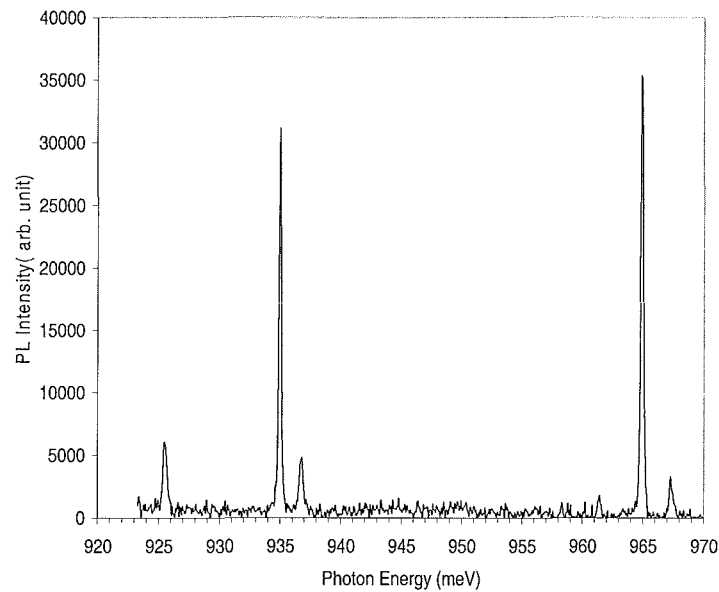
Figure 5-10: PL spectra of mc-Si etched with SF_6/O_2 and annealed at 425° C in N_2 for 30 min shows the disappearance of the G line at 969.5 meV and the two split lines at 935 meV and at 965meV and a weak line at 925.5 meV. PL measurement was performed at 4.3K.

The low temperature PL lines shown in Figure 5-10 are sharper and well resolved compared to that of room temperature PL lines shown in Figure 5-9.
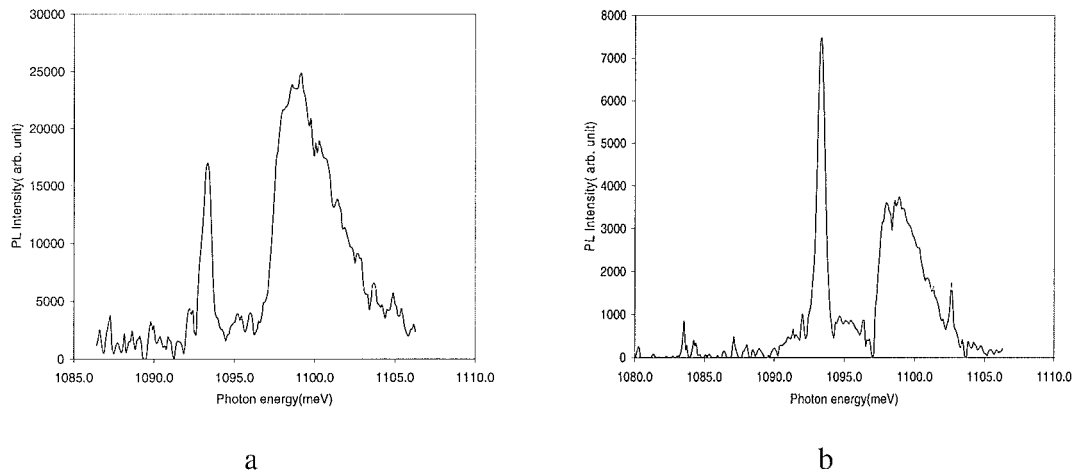
Figure 5-11 : Comparison of PL measured at 4.2K (a) mc-Si etched with SF_6/O_2 (b) mc-Si etched with SF_6/O_2 and annealed at 425° C in N_2 for 30 min. Measured at 4.2 K.

The intensity of the bound exciton PL line at 1093meV is weaker than the free exciton PL line at 1100 meV after the SF_6/O_2 etching as shown in Figure 5-11a. The intensity of the bound exciton PL line becomes stronger than the free exciton PL line after the N_2 annealing for 30 min as shown in Figure 5-11b.

5.8.1. Origin of 926 meV photoluminescence line

One of the e^- radiation damage centres in silicon is associated with very sharp and intense transitions at 926 meV (*H* line). A close correlation has been established between the intensity of these lines and the oxygen content of the sample [56]. The carbon content correlates also with the *H* line. It is shown that the formation of the *H* line is controlled by O_i (interstitial oxygen atom) migration, and that the centre leading to *H* must be similar to the *G* centre [56]. The origin should be the oxygen injected during SF_6 / O_2 RIE and the radiation during RIE. This defect must have been activated after annealing. Because O_i becomes mobile only after the temperature of 400° C [57].

5.8.2. Possible origin of the PL line at 935 meV

This 935 meV line was observed only after annealing above 400° C. This was also observed for the substrates irradiated by 1-2 MeV electrons [58]. The defect associated with this particular PL line at 935meV incorporates one carbon atom and oxygen is not involved [59]. There is a possibility of incorporation of boron as well [58]. Potential candidates for this defect centre are a vacancy, a silicon selfinterstitial and interstitial carbon. Boron in the defect is expected to occupy a substitutional lattice site.

5.8.3. Possible origin of the PL line at 965meV

By adding oxygen to the SF_6 plasma, the contamination of the Si surface by oxygen atoms is shown to considerably affect the PL spectra. It was argued that oxygen contamination enhances the formation of the all PL centres via the creation of extended defects, such as oxygen precipitates. The lattice stress near the oxygen-related extended defects is suggested to cause the splitting of the G line as well as the shift of the bound exciton lines observed after SF_6/O_2 RIE [54].

The defects corresponding to the G line are known to be formed by two nearest-neighbour substitutional carbon atoms and a Si interstitial and do not include the oxygen impurity. Thus, it is reasonable to assume that oxygen can form the precursor defects necessary to create G centres. The formation of radiation-induced defects is often considered using the "branching reactions" approach [60]. This model predicts an increase of the $[C_i]$ concentration by the production of selfinterstitials. The mobile C_i atoms are then trapped at another C_s to form G line centres. If the sample contamination by oxygen from the plasma is high enough, the formation of oxygen precipitates is likely to occur. Oxygen precipitation is known to be accompanied by the generation of Si interstitials, thus stimulating the formation of G defects.

5.8.4. Splitting of PL lines after annealing

The splitting of this line into two components indicates that the stress-induced defects cannot be destroyed at such annealing temperatures. High radiation damage of our

samples could be responsible for the low formation energy and, consequently, low formation temperature observed for these centres [54].

5.9 Behaviour of The 1.1 eV Free Exciton Line

Different laser powers were used to measure the intensity of the PL lines caused by the bound (BE) and free (FE) excitons at the near band-gap region around 1.1 eV. The PL line in the left is caused by BE and the right is caused by FE as shown in Figure 5-12.
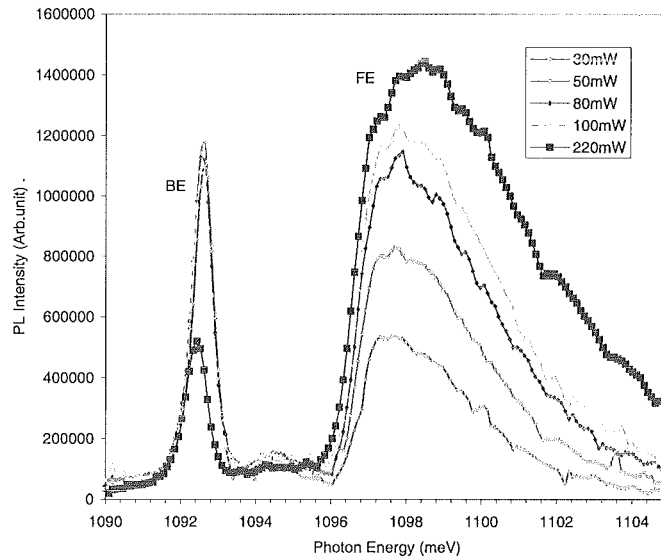
Figure 5-12: The relative PL intensities measured at 4.2 K for the RIE etch mc- Silicon wafers when five different laser power were used.
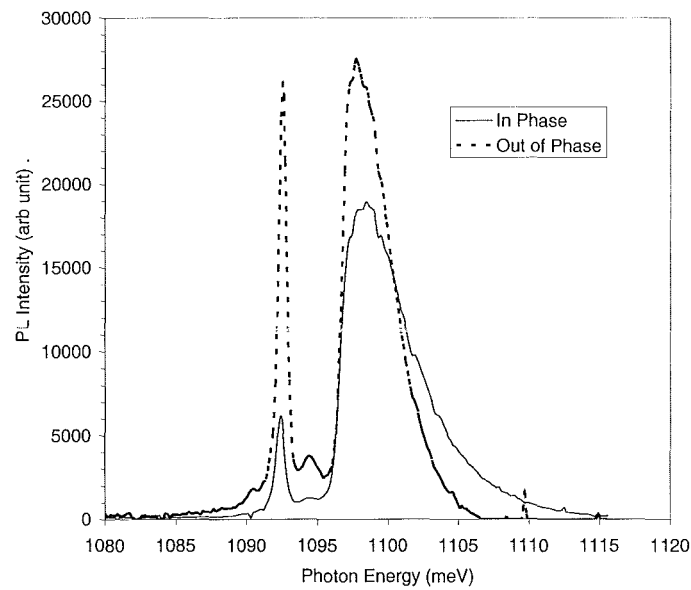
Figure 5-13: The BE and FE photoluminescence lines measured in phase and out of phase with the reference signal.

When the laser power is 30mW, the PL line of BE intensity is higher than that of FE. When the laser power is 220mW, the BE intensity is the lowest and the FE intensity is observed to be the highest.

The PL signal was much stronger when the phase difference of the reference beam and the beam from the sample was 90° as shown in Figure 5-13. This suggests that there could be a much longer time delay in the phonon assisted recombination process. A detailed study is needed to verify this claim.

5.10 Summary

Ion bombardment of the silicon surface during RIE produces defects, giving rise to the carbon related C and G lines. By adding oxygen to the SF_6 plasma the contamination of the silicon surface by oxygen atoms is shown to considerably affect the PL spectra. The oxygen contamination enhances the PL centres via the creation of extended defects, such as oxygen precipitates. A lattice contraction near these extended defects is suggested to cause the observed splitting of the C and G lines [54]. However, the minority carrier

lifetime results reported in Chapter 4 showed that SF_6 plasma alone causes significant defects in silicon wafers and result in a decrease in open circuit voltage of solar cells.

Radiation may play a considerable role in causing damage during RIE process. The C and G lines were observed by others for the substrates irradiated with e^- [60].

The splitting of PL lines after annealing suggests that those associated defects may not be annealed out further.

Long process times and high rf-power or self-induced dc bias were also suggested for resulting in a significant decrease in open circuit voltage in silicon solar cells [61]. These parameters influence in defect formation during plasma etching.

CHAPTER 6

LIGHT TRAPPING AND REFLECTION CONTROL

6.1 Introduction

Solar cells with high substrate lifetime and well passivated surfaces have collection efficiencies approaching 100 % of the photogenerated carriers, independent of where in the solar cell these carriers are generated. A significant number of photons in the solar spectrum have enough energy to create electron-hole pairs in the silicon, but are very weakly absorbed in the solar cell. Light trapping refers to schemes utilized to maximize the absorption of the weakly absorbed light by maximizing the path length traversed by the photon in the solar cell. One of the simplest implementations of this concept is to optimise the backside metallization for high reflectance, ensuring that the weakly absorbed photons will cross the cell twice. Another simple scheme is to structure the front cell surface to refract the photons into an angle with a larger path across the cell. More complex structures have been investigated that use structured front and back surfaces as well as mirrored surfaces to increase the effective path length of the photons by, in principle, up to 50 times the wafer thickness [9, 62, 63]. This can increase the current from the solar cell by up to 15 % for a 100 µm thick solar cell. Even higher degrees of light trapping are made possible by the use of a very high concentration of textured structures with a limited acceptance angle [9, 64].

These features of light trapping are important for any silicon solar cell, under one sun or concentrator conditions. They are especially critical for concentrator cells. Concentrator solar cells have very high current densities that cause transport losses due to bulk series resistance and carrier diffusion gradients. A minimization of these effects demands thin substrates. Light trapping is the means by which a very thin, optimised concentrator solar cell can be engineered to absorb most of the available light.

In this chapter, the background theory of antireflection, the reflectance measurements on various antireflection surfaces and theoretical modelling using PV-optics will be presented.

6.2   Optical Theory of Antireflection Coating
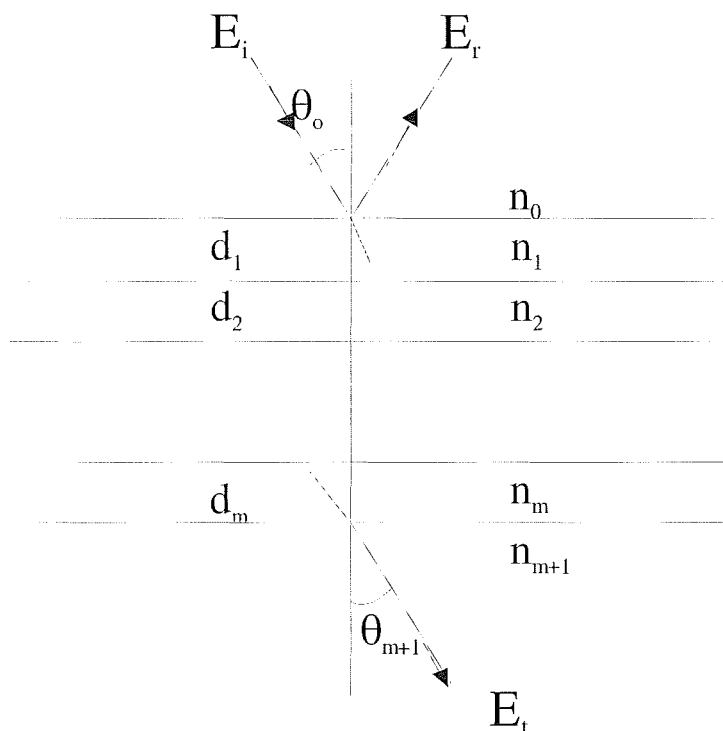
Figure 6-1: A multilayer nonabsorptive thin-film antireflection coating system.

A multilayer nonabsorptive thin-film AR coating system shown in Figure 6-1 can be solved by using a matrix method [65], [66]. Each layer j can be expressed by a matrix Mj

$$M_j = \begin{bmatrix} \cos\delta_j & -ip_j^{-1}\sin\delta_j \\ -ip_j\sin\delta_j & \cos\delta_j \end{bmatrix}$$ 6-1

$$\text{where } \delta_j = (2\pi/\lambda_o)n_j d_j \cos\theta_j$$ 6-2

where λ_o is the light wavelength in the air, n_j and d_j are the refractive index and the thickness of the coating material, θ_j is the incident angle in the layer which is determined by

$$n_j \sin \theta_j = n_o \sin \theta_o$$

6-3

For Transverse Electric (TE) waves $p_j = n_j \cos\theta_j$

6-4

and for Transverse Magnetic(TM) waves p_j changes to

$$p_j = (1/n_j)\cos\theta_j$$

6-5

The matrix

$$M = M_1.M_2.M_3...M_m$$

6-6

can be simply used to incorporate the optical property of all the layers of the film. There are three other matrices to be used to calculate the reflection. The detailed solution could be found elsewhere [65, 66]

$$\begin{bmatrix} a \\ b \end{bmatrix} = \begin{bmatrix} p_o & -1 \\ p_o & 1 \end{bmatrix} M \begin{bmatrix} 1 \\ p_{m+1} \end{bmatrix}$$

6-7

The polarized reflection

$$\Re = \left| \frac{a}{b} \right|^2$$

6-8

$\Re$ is different for TE and TM waves. If the incident angle is not zero, due to the sunlight being unpolarised, the total reflection R is half from TE waves and half from TM waves,

$$R = 0.5\Re_{TE} + 0.5\Re_{TM}$$

6-9

The solution for the expression for reflection R , which is derived from Equations 6-1 - 6-9, is published elsewhere [66].

$$R = \left(\frac{n_1 - n_o}{n_1 + n_0} \right)^2$$

6-10

At the interface from air, $n_o=1$, to silicon $n_j =3.85$, the reflection is calculated to be about 35%. Hence, AR coating is essential to reduce the reflection to be less than 5% for high efficiency solar cell.

For a single layer antireflection (SLAR) coating and normal incidence, a quarter wavelength thick film gives the minimum reflection, which has a thickness of d_j. The solution for d_j could be found elsewhere [66].

$$d_j = \lambda_o /(4n_j)$$ 6-11

where j is equal to 1, for SLAR coating.

Under this condition, the light reflected from the second interface will go back to the first interface with a phase change of $180°$. It will interfere with the reflected light from the first interface and weaken it due to their opposite phases. Applying Equation 6-11 to Equation 6-1 - 6-9 yields [66]

$$R = \left(\frac{n_1^2 - n_o n_2}{n_1^2 + n_o n_2} \right)^2$$ 6-12

Hence, at the condition

$$n_1 = \sqrt{n_o n_2}$$ 6-13

The reflection R becomes zero. Hence, Equations 6-11 and 6-13 are the conditions for the optimized SLAR coating.

For double layer antireflection (DLAR) coating at the normal incidence condition, also according to 6-1 - 6-9, when the same quarter wavelength is used for each film as from 6-10, the expression for R changes to [66]

$$R = \left| \frac{a}{b} \right|^2 = \left(\frac{n_1^2 n_3 - n_o n_2^2}{n_1^2 n_3 + n_o n_2^2} \right)$$ 6-14

When

$$n_1^2 n_3 = n_o n_2^2$$ 6-15

Then $R = 0$.

Hence Equations 6-11 and 6-15 are the conditions for optimized DLAR coatings. They give pairs of indices and thickness, but not a unique choice as for SLAR. Only Equations 6-1 - 6-9 can be used for solar cell calculations, because it is required to calculate the reflection over the very wide range of wavelength, and for some nonnormal incidence angle.

6.3   Theory of Reflection Control By Texturing

The effect of surface structure on reflection depends on the size of the structure relative to the wavelength of incident light. Following the discussion by Campbell [67], three different size ranges can be considered:

    (i)   macroscopic

    (ii)   microscopic and

    (iii)   intermediate.

In the macroscopic region, surface features are large compared to the wavelength of light. Optical interference effects can be neglected and ray tracing approaches used to describe the interaction between these features and light. The geometry of the features can be used to steer either reflected or refracted light in the desired direction.

In the microscopic region, feature size is much smaller than the wavelengths of light, say less than 0.1 μm. Such features may be treated by a "graded index" method where the true surface profile is approximated by a series of layers, each composed of different amounts of the two media involved [67]. Such feature sizes are not particularly effective in scattering the light [68] , acting much as if a graded index coating had actually been deposited on a flat surface.

For intermediate feature sizes (0.1 μm to a few microns), there can be strong interaction between the light and the features. Both reflected and refracted light can be strongly scattered. One simplification for strongly scattering cases is to treat the surface as "Lambertian" that is, as scattering light with uniform brightness in all directions. Another possibility is to regard any actual surface as a composite of Lambertian and non-scattering (specular) [68].

6.3.1. Two dimensional geometries
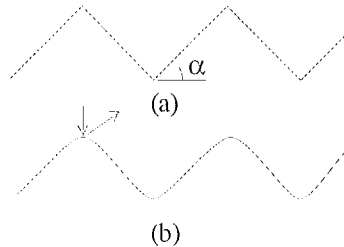
Figure 6-2:   2-D grooves . (a) ideal case shown groove angle, α; (b) rounded peaks and troughs.

Figure 6-2 (a) shows a simple two dimensional (2D) grooved surface structure. Groove size is assumed large compared to the wavelength of light so that ray tracing approaches can be used to describe the interaction between the groove and light. The groove angle is α, as shown. Such grooves reduce overall reflection by reflecting incident light downwards so it has a second chance of being coupled into the surface. For light incident perpendicular to the plane of the cell, there are several threshold values of a marking changes in reflection properties. Once α exceeds $30°$, some light incident near the base of the grooves, will benefit from this "double bounce" effect. Once α exceeds $45°$, all perpendicular incident light will benefit. As α increases beyond $54°$, triple bounces become possible for light incident near the base of the grooves. By $60°$, all such light experiences "triple bounces", and so on. These thresholds will become somewhat blurred if the light of interest has angles of incidence other than perpendicular.

If the angular dependence of reflection from a surface of reflectance R is neglected, reflectance after n bounces will be R^n. For the example of silicon embedded in an encapsulant of refractive index 1.5, surface reflectance is about 20% at free space wavelengths around 600nm, near the peak of the solar spectrum. Overall reflectance would reduce to 4% after a "double bounce" and less than 1% after a "triple bounce".

Mathematically, for $54°\leq \alpha \leq 60°$, the fraction of perpendicularly incident light experiencing triple bounces, f_3, can be shown to be :

$$f_3 = \frac{\sin(5\alpha - 270)}{\sin(90 - \alpha)} \qquad\qquad 6\text{-}16$$

For surface features formed by intersecting (111) crystallographic planes α is 54.7°. All perpendicularly incident light will get at least a double bounce, with 11.1% incident near the bottom of the groove experiencing triple bounces [21].

Although chemical texturing can produce very sharp edges between the differently oriented planes, edge rounding sometimes occurs as a result of subsequent processing or is deliberately used to reduce stress concentrations from overlaying layers such as mechanical abrasion, rounding is unavoidable. As shown in Figure 6-2 (b), rays incident on the flatter regions of the curves will experience only a single reflection for perpendicular light, once the angle of the tangent falls below 45° for the peaks and (45° - α/2) for the troughs.
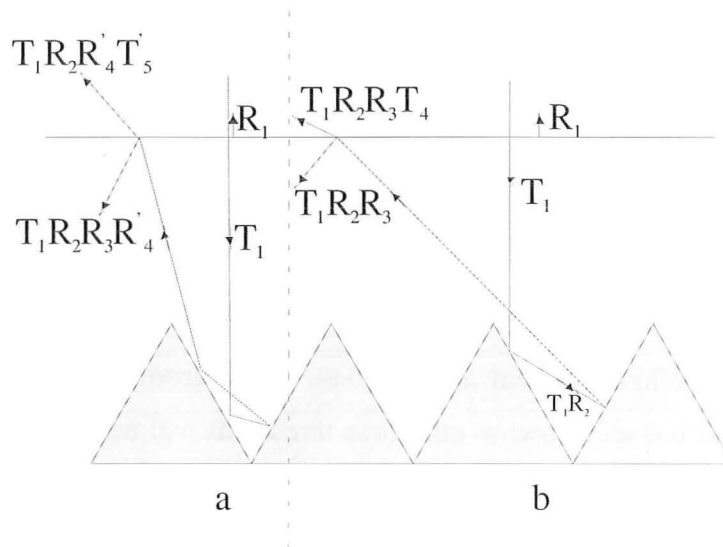
Figure 6-3: Ray paths for grooves formed for (111) equivalent planes (2D case). a. Ray striking closer to the bottom of the groove. b. Ray striking closer to the top of the groove.

Similar concentration will apply to other less regular shapes than the grooves of Figure 6-2. Generally, the design principle is "the steeper, the better" provided peak and trough reflection is also factored into the evaluation.

For precise calculation of reflection properties, the angular dependence of reflection has to be considered and polarization effects become important. Due to the higher reflectance

of light polarised perpendicularly to the place of incidence, reflected light has a progressively higher component of this polarization after each reflection.

Finally, most cells are not used directly exposed to air but are encapsulated, usually under glass. The important reflection properties are those of the combination of cell and encapsulant.

Figure 6-3 shows the ray path for light perpendicularly incident upon grooves formed by intersecting (111) planes encapsulated under glass or other material of refractive index equal to 1.5. For unpolarised light at 600 nm free space wavelength , 96.0% of the incident light energy will be coupled into the glass (T_1), 25.3% will be reflected after first striking the groove (T_1R_2), reducing to 5.1% strongly polarised after the second groove reflection ($T_1R_2R_3$) [67].

Most of this light then internally strikes the encapsulant / air interface at an angle close to 39° as shown. This is not sufficiently oblique for total internal reflection. However, light of this polarization is still quite strongly reflected at these wavelengths, giving only 3.6% of the originally incident light following this path coupled out here ($T_1R_2R_3T_4$). A fraction (11.1%) of incident light strikes the area near the base of the groove and has an additional reflection from the silicon surface. However, this third reflection is very oblique (86.3% from normal) giving high reflectance of light regardless of polarization. Moreover, this light strikes the glass less obliquely, giving lower reflection at the glass and higher transmission. The net result is that this "triple bounce" light fares slightly worse than the "double bounce" light with 4.0% coupled out. When combined with the 4.0% originally reflected (R_1) plus a strongly attenuated component of $T_1R_2R_3R_4$ (after further reflections) and $T_1R_2R'_3R'_4R'_5$, a total of 7.6% of the total incident energy is reflected.

This reflection loss can be reduced by applying antireflection coatings to the textured cell surface to reduce components R_2 and R_3 [69]. Additionally component R_1 can be reduced by applying an antireflection coating to glass, or by subjecting the glass to a chemical treatment. This gives the same effect by changing surface properties [70]or by texturing the glass [71], cleanability becomes an issue in the latter case.

Ray path visualisation for RIE textured 3D structures is not very easy. However high aspect ratio cones can be approximated to pyramids of small apex angle and high aspect

ratio holes can be approximated to inverted pyramids with smaller apex angle for theoretical modelling.

6.4   Reflectance Measurement of Textured Surfaces

Reflectance was measured using purpose built integrating sphere attachment of a high accuracy spectrophotometer. Besides the specularly reflected radiation, the diffuse radiation was also measured in this method. This will give us an idea of the absorbance of the textured surfaces. The experimental set up is given in Chapter 2.

6.4.1. Hole-type textured wafers

A p-type Cz-silicon wafer was textured using photolithographically defined NiCr mask. The SEM image of this sample is given in Figure 3-17. The reference wafer is a single side polished p-type Cz-Silicon wafer. The average thickness of the wafers is about 350 μm. The holes are about 7-8 μm deep and 4 μm in pitch. The detailed texturing procedure is given in Chapter 3.

As can be seen in Figure 6-4, at 400 nm wavelength the reflectance is reduced from 50% to 10 % and at 1000nm wavelength, it is reduced from 32% to 4.4 %. Beyond 1200nm wavelength, the incident light is almost fully transparent for silicon and the reflection is entirely from the backing material.

The reduction in reflectance in the ultraviolet region is very significant as it contributes a major part in boosting the solar cell efficiency. Approximately 80% reduction is observed in this region.
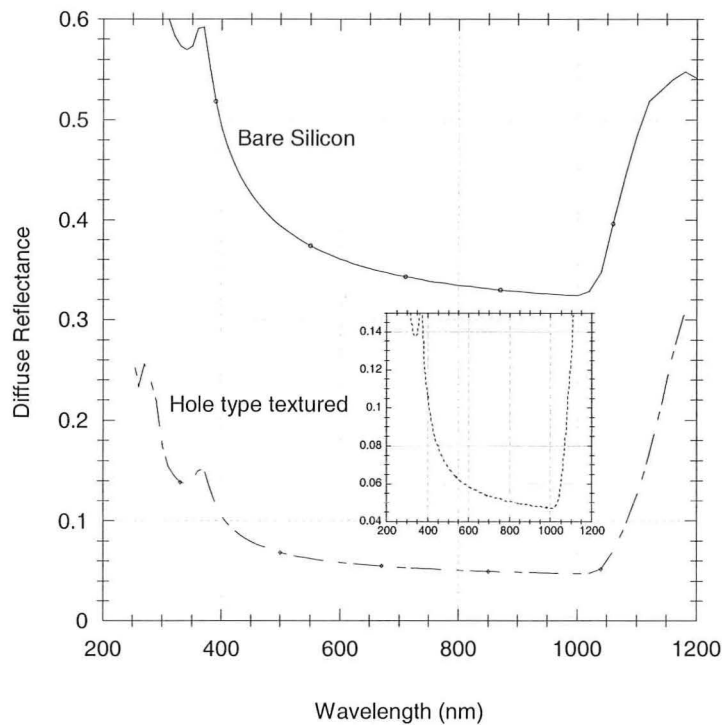
Figure 6-4: Diffuse reflectance of planar silicon and the hole - type textured silicon wafer. The magnified reflectance data for hole-type textured silicon wafer is also shown.

6.4.2. Cone-type textured wafers

A p-type Cz-silicon wafer of 350 μm thickness was textured using photolithographically defined NiCr mask. The SEM image of this sample is given in Figure 3-21. The reference wafer is a single side polished p-type Cz-Silicon wafer. The cones are about 6-7 μm high and 4 μm in pitch. The detailed texturing procedure is given in Section 3.3.2.

As can be seen in Figure 6-5, the reflectance is reduced from 50% to 1 % at 400 nm wavelength and, it is reduced from 32% to 0.3 % at 1000nm wavelength. Beyond 1200nm wavelength, the incident light is almost fully transparent and the reflection is entirely from the backing material.

Approximately 98% reduction in reflection is observed in the ultraviolet region.
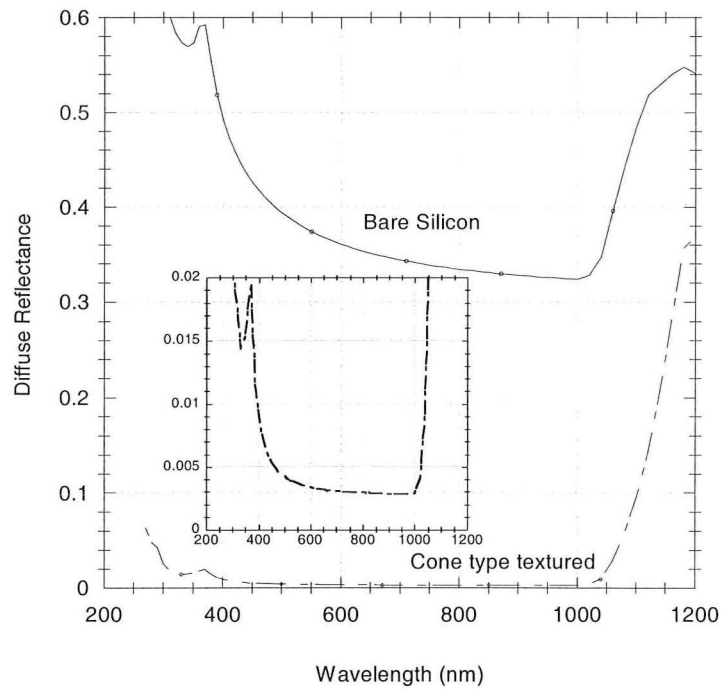
Figure 6-5: Diffuse reflectance of planer silicon and the textured surfaces of cone type structure. Insert is the magnified reflectance data for cone-type textured silicon wafer.

On average, the reflectance is less than 0.5 % in the effective wavelength region. This is a very significant achievement in controlling the reflection without any antireflection coatings.

6.4.3. Mask-less textured substrates

Unlike the previous texturing methods, a p-type Cz-silicon wafer of 350 µm thickness was textured without any photolithographically defined mask. This is called maskless texturing method. The texturing detail and the SEM image of the textured wafer are given in Section 3.3 and Figure 3-23 respectively. The reference wafer is a single side polished p-type Cz-Silicon wafer.

As can be seen in Figure 6-6, the reflectance is reduced from 50 % to 3 % at 400 nm wavelength and it is reduced from 32% to 0.9 % at 1000nm wavelength. Beyond 1200nm wavelength, the incident light is almost fully transparent and the reflection we get is entirely from the backing material.
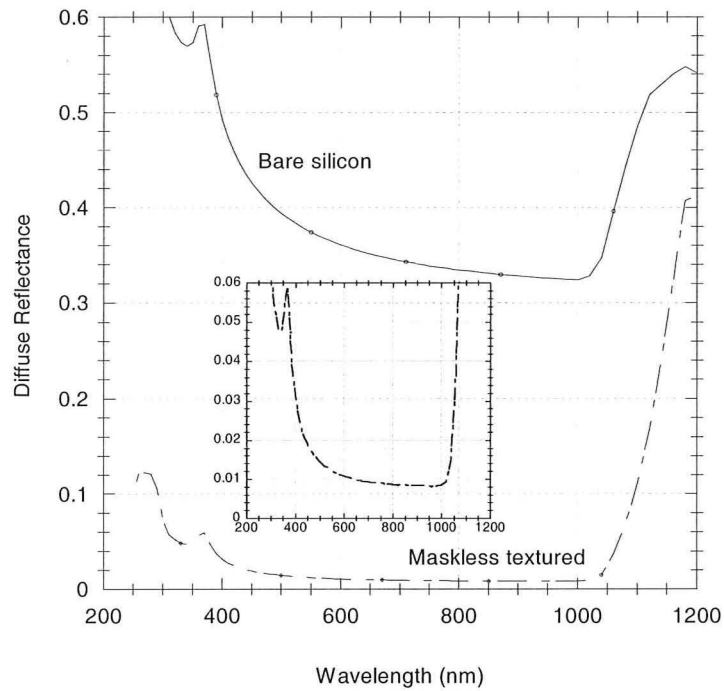
Figure 6-6: Diffuse reflectance of planer silicon and the maskless textured surfaces of silicon wafer. Insert is the magnified reflectance data of the maskless textured silicon wafer.

On average, the reflectance of the maskless textured silicon surface is around 1 % in the effective wavelength region. This is slightly higher than that of cone type texturing. However, the maskless method can save time, energy and cost as far as the photovoltaic industries are concerned.

For visual comparison, these three graphs are combined and given in the
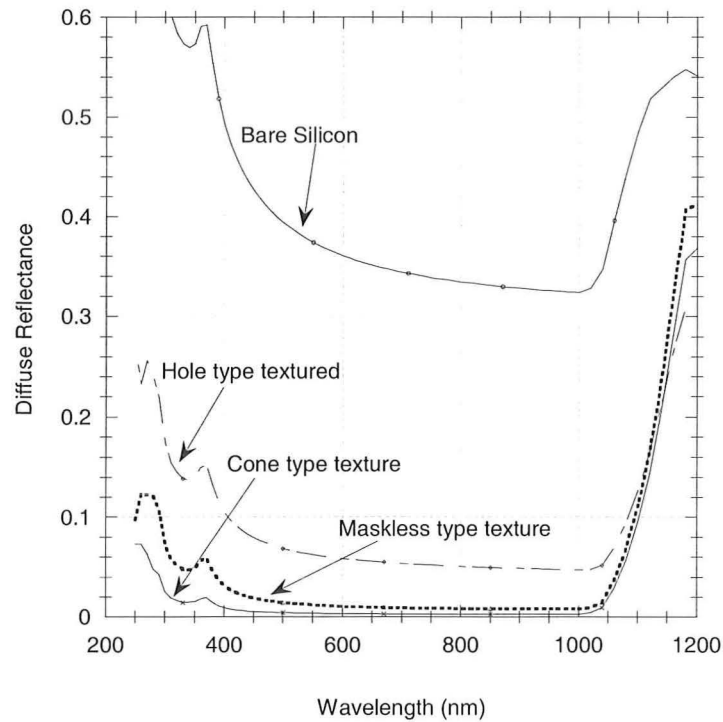
Figure 6-7: Diffuse reflectance of planer silicon, cone type textured surface, hole type textured surface and the maskless textured surfaces of silicon wafer are given in a single graph for visual comparison.

6.5   Reflection measurement on antireflection coatings.

Several antireflection coatings (ARC) including Si_3N_4, SiO_2 TiO_2, ZnS,MgF_2, and Titanium silica film are used in silicon solar cells. The reflectance is measured for SiO_2 ARC and ZnS / MgF_2 double layer anti reflection coatings (DLARC). The wafer used in this experiment is 300 μm, p-type, double side polished, FZ–silicon of 5Ωcm resistivity. For RIE texturing, SF_6 gas was used and the SEM image of cone type texture is similar to that of Figure 3-26 and the hole type texture is similar to the one in Figure 3-17. The purpose of this ARC experiment is to compare the reflectance measured on textured wafers.

6.5.1. Thermal silicon dioxide

Generally, SiO_2 absorbs wavelength less than 500 nm and hence reduces the efficiency of solar cells. However, SiO_2 is generally used as ARC in commercial solar cells because of

its ability to passivate the silicon solar cells. A 110 nm of SiO_2 can be used as an ARC as well as a passivation layer for silicon solar cells.

In this experiment, dry thermal SiO_2 was grown in an O_2 environment at 1000° C. in a tube furnace as described in Chapter 2.
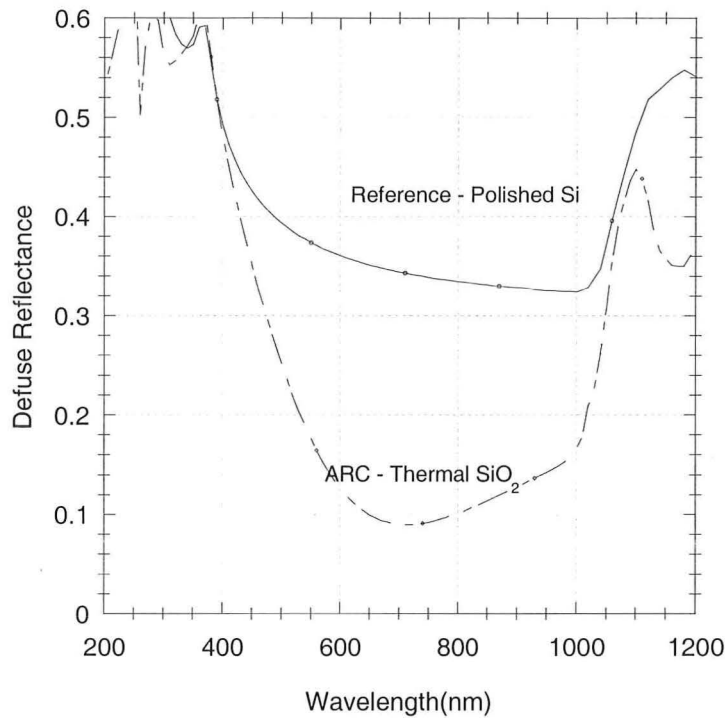
Figure 6-8: The reflectance of FZ- silicon wafer with 130nm of thermal oxide is shown with the reflectance of polished silicon wafer. The minimum reflectance is 9% at 700nm.

The thickness of the thermal oxide was calculated as 130 nm which is 20nm higher than the ideal value of 110 nm. The trough of the reflectance is at 700 nm instead of the ideal 600nm as shown in Figure 6-8.
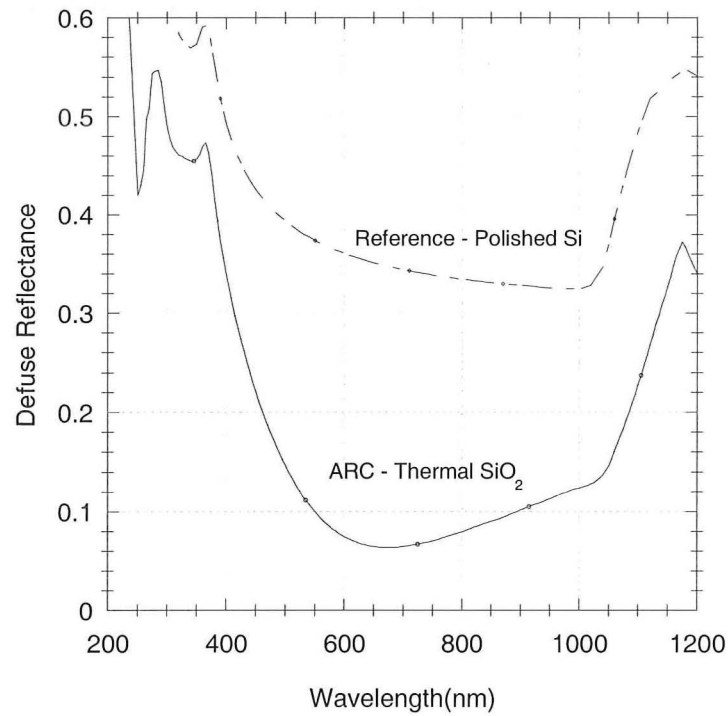
Figure 6-9:– The reflectance of the hole-type textured FZ- silicon wafer with 130nm of thermal oxide. The textured wafer was wet etched in diluted HF: HNO₃ (50:1) solution for 8 min to remove about 5 μm of silicon before growing thermal oxide.

The reflectance of the textured silicon wafer with 130nm of SiO_2 as ARC is shown in Figure 6-9. The textured surface consists of hexagonally arranged   hole-type structures in 10μm pitch. The surface is similar to the one shown in Figure 3.17. The reflection measured in Figure 6-9 is much higher than that measured in Figure 6-5.

This less effective surface texturing may be due to the following reasons.

a. The 10μm pitch holes in Figure 6-9 is much larger compared to the 4μm pitch holes in Figure 6-5.

b.   The 8 min defect removal etching removed about 5μm silicon and hence made the textured surface very smooth.

c. Larger pitch and DRE end up with more flat surfaces in the bottom of the holes.
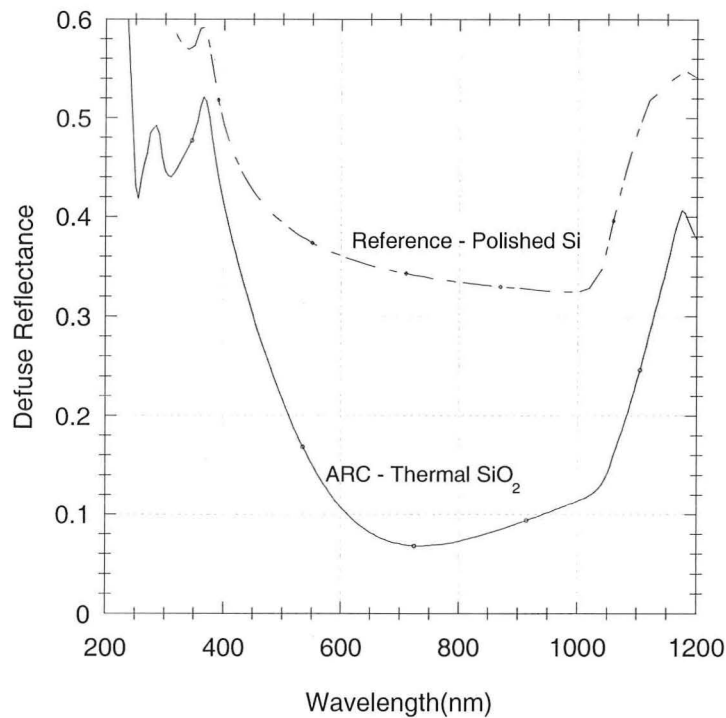
Figure 6-10:. The reflectance of the cone-type textured FZ- silicon wafer with 130nm of thermal oxide. The textured wafers were wet etched in HF: HNO_3 (50:1) solution for 8 min to remove about 5 μm of silicon before growing thermal oxide.

The reflectance of a cone-type textured silicon surface with 130 nm of thermal SiO_2 is shown in Figure 6-10. In this case the reflection is much higher than expected. The above mentioned three reasons could be applicable to this case as well. For short wavelength region, the cone-type textured wafer give lower reflectance than cone-type textured wafer.

6.5.2. MgF₂ antireflection coating

An MgF_2 layer can reduce reflection from silicon surfaces. The reflective index of MgF_2 is 1.3-1.4. A good single layer ARC should satisfy Equations 6-11 and 6-13. Therefore the best ARC material should have a reflective index of 1.96. That is why very low reflection could not be obtained at any wavelength as shown in Figure 6-11. However MgF_2 is better than SiO_2 as it is evaporated at very low temperature and it does not absorb UV very much. Thermal SiO_2 is grown at temperature around 1000° C and cause diffusion of impurities easily.
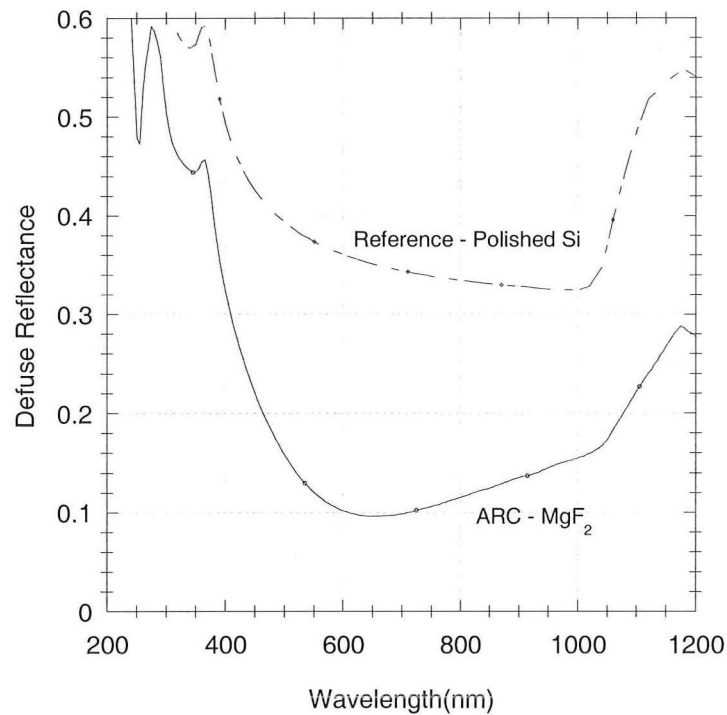
Figure 6-11: The reflectance of the cone-type textured FZ- silicon wafer with thermally evaporated 110nm of MgF$_2$. The textured wafers were wet etched in HF: HNO$_3$ (50:1) solution before evaporating MgF$_2$.

6.5.3. Double layer anti reflection (DLAR) coating (ZnS and Mg F$_2$)

Multilayer antireflection coatings reduce reflection in broader band [72].

In this work, MgF$_2$ of refractive index 1.38 and ZnS of refractive index 2.3 are coated using thermal evaporation technique. The thickness of MgF$_2$/ZnS layers has been theoretically optimised to be 110 nm and 35 nm respectively and it was experimentally verified [69]. Such DLAR coatings give very low surface reflectance over the entire absorbable solar spectrum.
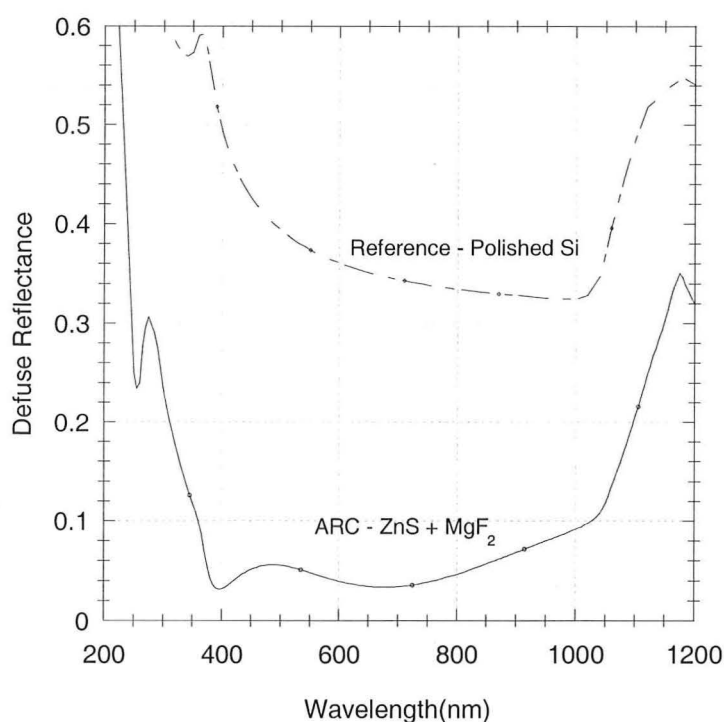
Figure 6-12: The reflectance of the cone-type textured FZ- silicon wafer with thermally evaporated 35nm of ZnS and   110 nm MgF_2. The textured wafers were wet etched in HF: HNO_3 (50:1) solution before growing thermal oxide.

A Fz- silicon substrate was textured using an etch mask of hexagonally arranged   6μm dots in 10 μm pitch. The textured wafers were coated with a double layer antireflection (DLAR) coating of ZnS (35 nm) and MgF_2(110 nm). Thermal evaporator was used for this purpose. Thermally evaporated ZnS/MgF_2 exhibits a very broad band antireflection as shown in Figure 6-12. Unlike SiO_2, it reduces reflection in the UV region as well.

6.6   Modelling using PV- Optics software

PV-Optics is a software package for the design and analysis of solar cells and modules [73]. PV Optics is easy-to-use software that accurately models the optics of most solar cells or modules, and provides information needed to design a device with maximum-effective light-trapping and optimum photocurrent. PV Optics can handle multilayer structures consisting of a combination of dielectrics, absorbing semiconductors, and highly absorbing metallic layers with planar and non planar interfaces. Each of the layers

may be thin or thick as compared to the coherence length of light in that layer. It uses this criterion to select the application of the ray or wave optics to analyze the layer or the structure. This package outputs a variety of data including plots of the net reflectance, transmittance, and absorbance, the AM1.5 weighted absorbed photon flux and its distribution within each layer, and the Maximum Achievable Current Density (MACD) from each active layer. MACD is the value of the photocurrent produced within an active layer corresponding to the generation of one electron-hole pair for each absorbed photon, and subsequent collection of all of the generated carriers.
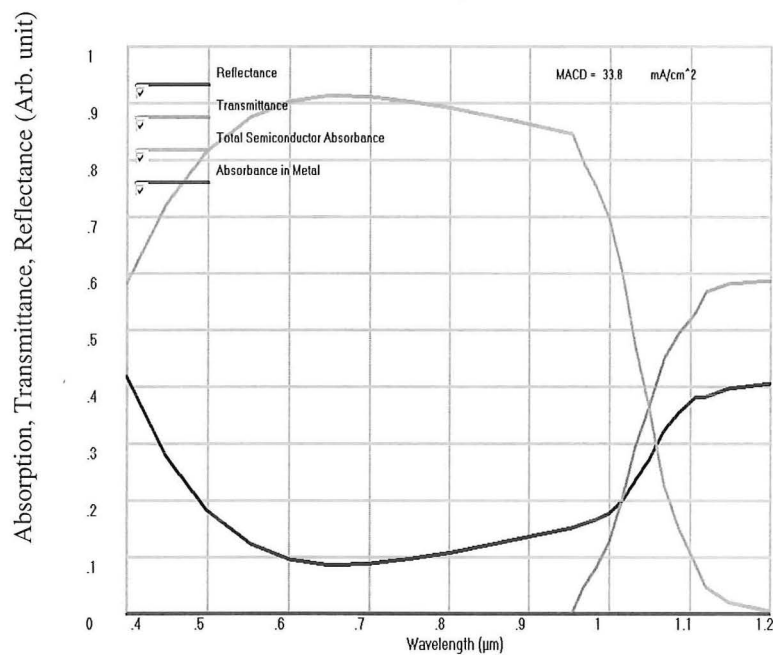
Figure 6-13: The PV-Optics data of reflectance, transmittance and the total absorption of a plane silicon with 110 nm of SiO_2 as anti reflection coating (ARC).

Thermally grown SiO_2 could act as an ARC as well as a good surface passivation agent. The PV optics modelling shown in Figure 6-13 reveals that the Maximum Achievable Current Density (MACD) of an untextured silicon wafer with 110 nm of SiO_2 as ARC is 33.8 mA/cm^2. The reflectance calculated using PV-Optics agrees with the measured reflectance.
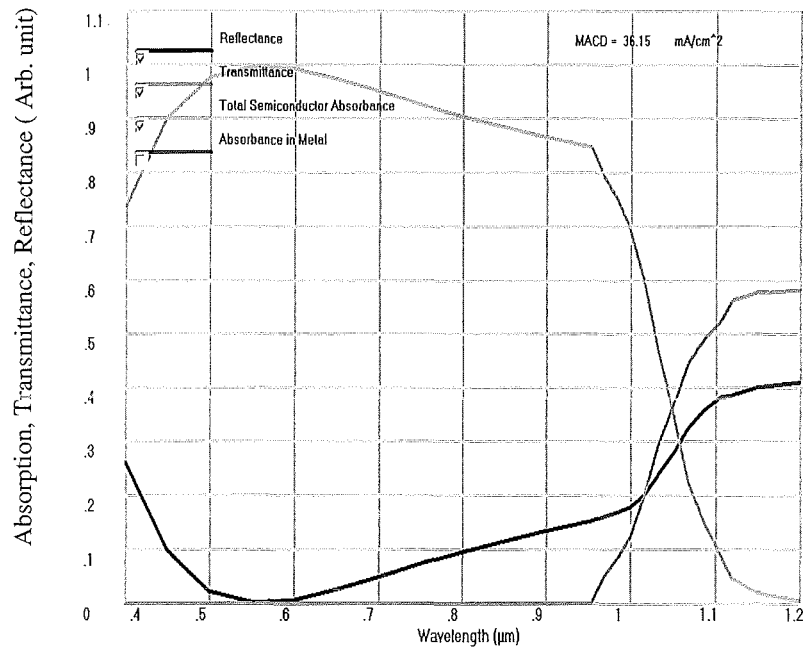
Figure 6-14: PV-optics data of 70 nm of Si_3N_4 antireflection coating on plane silicon wafer.

The refractive index of Si_3N_4 is 1.9 and satisfies the 6-13. A 70nm Si_3N_4 ARC gives very low reflection in the blue response region as shown in Figure 6-14. The MACD is calculated as 36.15 mA/cm^2. However, the optimum antireflection could be obtained by a DLARC of 71 nm of Si_3N_4 and 10 nm of SiO_2 as passivation layer. PV- optics calculation shows a MACD of 36.38 mA/cm^2 for this DLARC as shown in Figure 6-15.
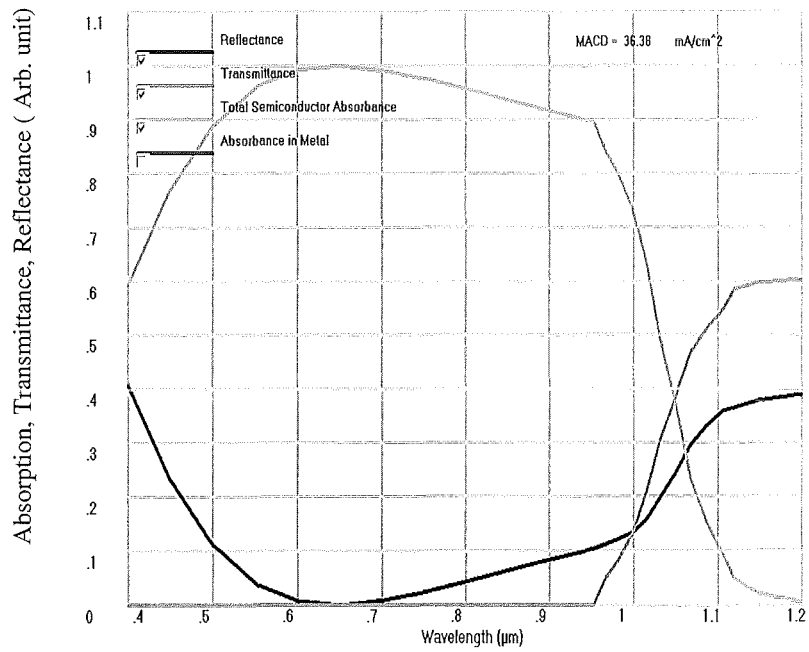
Figure 6-15: PV-optics data of 71 nm of Si$_3$N$_4$ and 10 nm of SiO$_2$ as double layer antireflection coating(DLARC) on a planer silicon wafer.
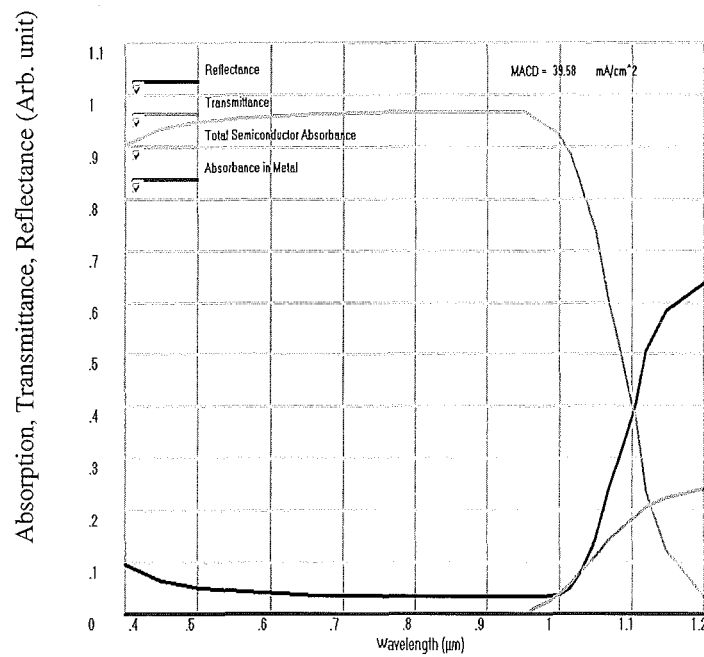
Figure 6-16 The PV-Optics data of reflectance, transmittance and the total absorption of a textured silicon without any anti reflection coating (ARC). The texturing structure is 6 μ m high square pyramids with 50 ° apex angle.

The PV-optics modelling for a silicon wafer textured with pyramids of 6 μm high and 50° apex angle exhibits a tremendous boost in MACD and is 39.58 mA / cm^2 without any antireflection coatings as shown in Figure 6-16.
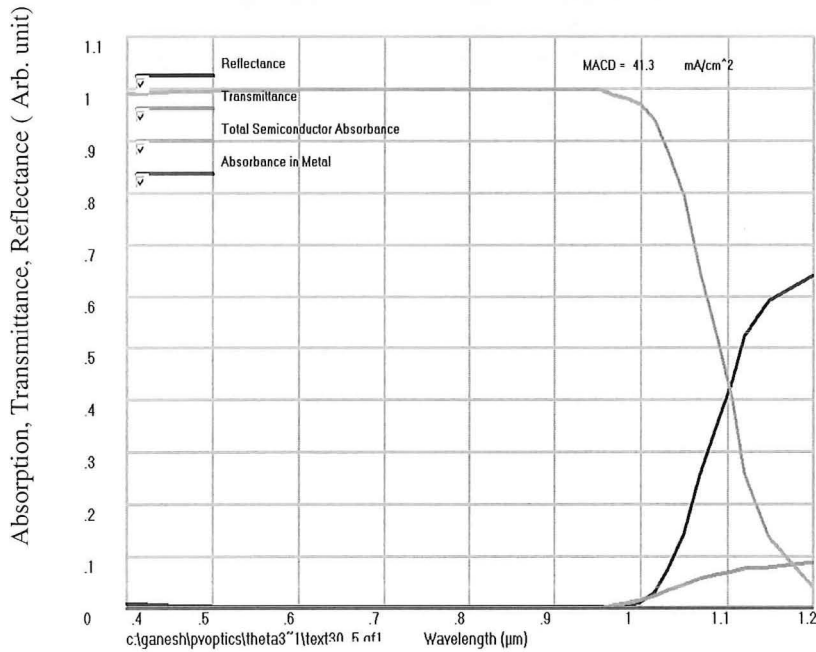
Figure 6-17: The PV-Optics data of reflectance, a textured silicon without any anti reflection coating (ARC). The assumed structure is 6 μ m high square pyramids with 35° apex angle.

The PV optics calculation for square pyramids of 6 μm high and 35° apex angle is shown in Figure 6-17. Pyramids of smaller apex angle will give better antireflection features and hence the MACD. These square pyramids can be assumed to be similar to the cone type texturing shown in Figure 3-21. This assumption agrees with the experimental data shown in Figure 6-1 for the cone type texturing.
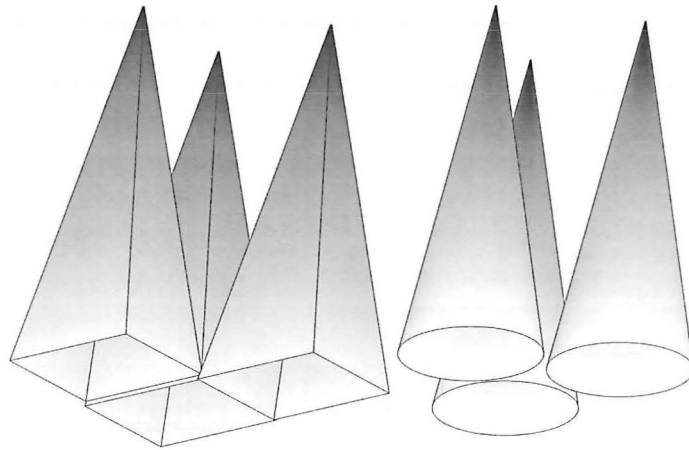
Figure 6-18: The square pyramids of small apex angle (left) and high aspect ratio cone-type structures (right) are shown in this illustration.

The Figure 6-18 shows how the hexagonally arranged cone-type texturing of high aspect ratio can be approximated to pyramids of smaller apex angle for theoretical PV-Optics calculations.
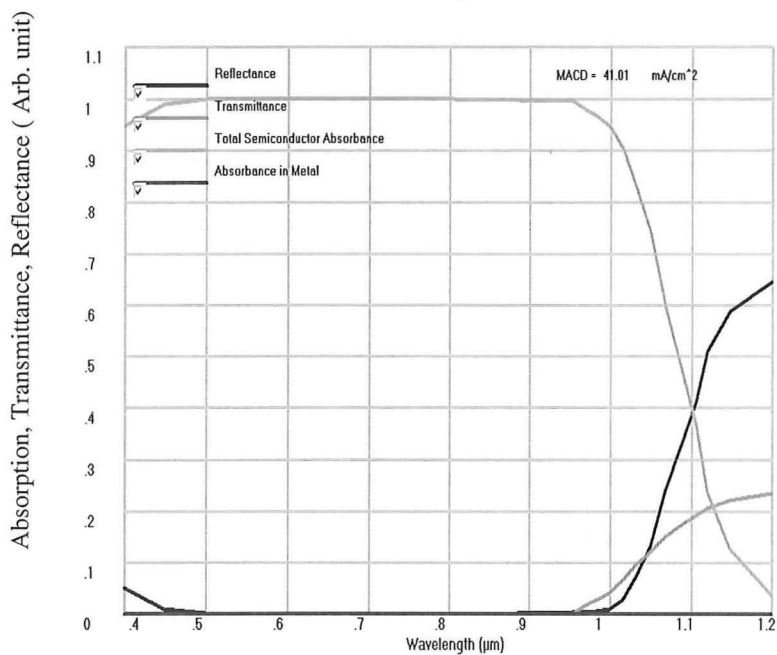
Figure 6-19: The PV-Optics data of a textured silicon wafer with 70nm of Si_3N_4 and 10 nm of SiO_2 as double layer anti reflection coating (DLARC). The texturing structure is 5 μm high square pyramids with 50 ° apex angle.

A DLARC of 70nm of Si_3N_4 and 10 nm of SiO_2 on texturing structures of 50° apex angle boosts the MACD from 39.58 mA/cm^2 to 41.01 mA/cm^2 as shown in Figure 6-19.

6.7   Effect of rear texturing
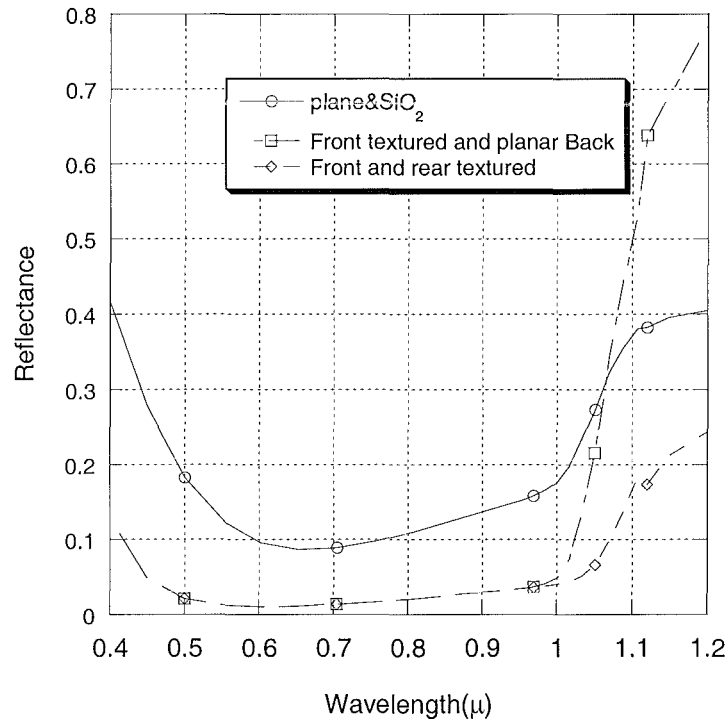
Figure 6-20: Reflectance calculated for textured silicon wafer with SiO_2 antireflection using PV-Optics software. The thickness of SiO_2 is 110 nm and the texturing structure is 5μm tall square pyramids of apex angle 70.5°.

Rear texturing for a front textured silicon wafer becomes effective only in the long wavelength range, particularly after 975nm, as shown in Figure 6-20. The energy of the photons beyond 975 nm is too small to be absorbed in silicon. Therefore, rear texturing may bring adverse effects to the silicon solar cells by absorbing the unwanted infrared wavelengths which will raise the cell temperature. Cell temperature is an efficiency limiting factor in silicon solar cells. . The approximately linear relationship of temperature and the open circuit voltage is shown in Equation 6-18 which is derived from the basic Equation 6-17 for the short circuit current of silicon solar cell [8].

$$I_{sc} = I_o(e^{qV_{oc}/kT} - 1)$$ 6-17

where , I_{sc} is the short circuit current of solar cell

I_o is the saturation current

V_{oc} is the open circuit voltage.

$$\frac{dV_{oc}}{dT} = -\frac{V_{go} - V_{oc} + \gamma(kT/q)}{T}$$ 6-18

where, $V_{go} = E_{go}/q$, E_{go} is the band gap of Si.

γ includes the temperature dependencies of parameters determining the saturation current I_o.

This equation predicts that, Voc decreases by about 0.4 % per °C. Power output also will decreases by 0.4 to 0.5 % per °C [8].

6.8 Summary

Different types of texturing structures and antireflection coatings have been examined for their reflectance. Very low reflectance was achieved for the SF_6/O_2 etched cone-type texturing. The reflectance is less than 0.5% in the majority of the absorptive region of the solar spectrum. However, the reflectance of the maskless etched wafer is very impressive as it is very cost effective compared to the masked process. Less than 1% reflectance was observed in the most of the effective region of the spectrum for these maskless textured silicon substrates. However, the reflectance increased above 3% for the wavelength less than 400nm. This is expected as the absorption coefficient is 100 times higher at the wavelength of 350 nm than at 500 nm.

Our results show that a good texturing does not need any antireflection coating except a thin SiO_2 or Si_3N_4 needed for surface passivation.

The SF_6 textured 10μm pitch structures did not exhibit low reflectance as these structures were not optimized. Larger pitch of the structures and much longer defect removal etching caused high reflectance. But the minority carrier lifetime analysis and the photoluminescence analysis shows that longer DRE is inevitable to achieve a high open circuit voltage.

The PV-Optics modeling shows that the maximum achievable current density could be increased from 33.8 mA/cm^2 for planar silicon to 41.3 mA/cm^2 for textured silicon. As shown in Figure 6-16, for a textured silicon with reflectance as high as 4% could exhibit MACD of above 39.5 mA/cm^2.

Our experimental and modelling results clearly show the advantage of using texturing over antireflection coatings. Textured surfaces give very low reflectance over a wide range of solar spectrum while the ARC give minimum over a selective wavelength range.

However there are disadvantages of texturing as well.

- More care is required in handling the textured wafers as textured wafers break easily.

- Textured surfaces are much more effective in coupling light of all wavelengths into the cells, including unwanted infrared radiation of insufficient photon energy to create electron-hole pairs. This tends to make the cell run hotter. Additional precautions are needed to reduce the cell temperature.

CHAPTER 7

SOLAR CELL FABRICATION

7.1 Introduction

A simple silicon solar cell fabrication involves three major processes.

1. Cleaning of silicon wafers.

2. Junction diffusion

3. Metallisation

However, more complicated steps such as texturing, surface passivation, antireflection coating and back surface field are necessary for a high efficiency silicon solar cell. In this chapter the wafer cleaning procedures, junction diffusion procedures, front and back metallisation and the cell characterization techniques and their results are presented.

7.2 Cleaning process of Silicon wafers

Transition metals in silicon are highly recombination active and affect silicon solar cells efficiency very much [74]. The purity of a Si wafer is a key prerequisite for a high efficiency silicon solar cell. However, only the contamination on the surface of Si wafers could be cleaned by chemical means. Wafer cleaning chemistry has remained unchanged during the last 30 years and is based on hot alkaline and acidic hydrogen peroxide solutions, a process known as RCA standard clean [75]. These cleaning steps remove inorganic and organic contaminations on the surface of wafers. All samples investigated in this work received this type of cleaning sequence prior to any thermal processes such as diffusion, oxide passivation and Si_3N_4 passivation. The following Table 7-1 summarises the details of the cleaning sequence used for the samples processed.

Table 7-1: Silicon wafer cleaning procedure called RCA cleaning.

Step	Process	Chemicals	Details
1	RCA1	$H_2O:H_2O_2:NH_4OH$ (5:1:1)	12 min at 80° C
2	DIW Rinse	Deionized Water (18MΩ cm)	1min at 18° C
3	HF	HF: H_2O (1:10)	15 Sec at 18° C
4	RCA2	$H_2O:H_2O_2:HCl$ (6:1:1)	12 min at 80° C
5	DIW Rinse	Deionized Water (18MΩ cm)	1min at 18° C
6	Dry	Dry N_2	1min

7.3   Emitter Diffusion

7.3.1. Theory of diffusion

According to the First Law of Diffusion, the transfer of solute atoms per unit area in a 1-dimensional flow can be described by the following equation:

$$J = -D \frac{\partial C(x,t)}{\partial x}$$ 7-1

where J is the particle flux, C is the concentration of the solute, D is the diffusion coefficient, x is the distance into the substrate, and t is the diffusion time. The negative sign indicates that the diffusing mass flows in the direction of decreasing concentration.

From the Conservation of Mass, we also know that:

$$\frac{\partial C}{\partial t} = -\frac{\partial J}{\partial x}$$ 7-2

If this relationship is combined with the 1st Law of Diffusion, then the 2nd Law of Diffusion (otherwise known as Fick's Law) is derived, which states:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2}$$ 7-3

In order to solve Fick's Law, one initial condition and two boundary conditions are required. Two solutions to Fick's Law are generally encountered in IC fabrication: infinite-source and limited-source diffusion. These are each described below.

7.3.2. Infinite-source diffusion (pre-deposition)

Infinite-source diffusion requires a constant surface concentration of diffusing atoms. This generally corresponds to the process step known as "pre-deposition." In this case, the initial condition and boundary conditions are:

$$C(x,0) = 0 , C(0,t) = Cs, C(\infty,t)=0 \qquad \text{7-4}$$

where Cs is the surface concentration. The solution to Fick's Law under these conditions is:

$$C(x,t) = Cs \ erfc\left[\frac{x}{2\sqrt{Dt}}\right] \qquad \text{7-5}$$

where "*erfc*" is the complementary error function.

7.3.3. Limited-source diffusion (drive-in)

Limited-source diffusion requires a constant amount of total dopant per unit area of the diffusing surface. This corresponds to the process step known as "drive-in" or any subsequent heat cycles. In this case, the initial condition and boundary conditions are:

$$C(x,0) = 0, \quad \int C(x,t) = S , C(\infty,t)=0 \qquad \text{7-6}$$

where S is called the "dose." The solution to Fick's Law under these conditions is:

$$C(x,t) = \frac{S}{\sqrt{\pi Dt}} \ exp\left[\frac{-x^2}{4Dt}\right] \qquad \text{7-7}$$

7.4 Spin On Dopant Solar Cells

Phosphorosilicafilm (Emulsitone Company) was used as the phosphorous diffusion source. Phosphorosilicafilm-3 x 10^{20} is a dopant formulation designed to produce phosphorous diffused layers in silicon for solar cells. When applied by spinning or spraying, a film is generated that consists of silica with phosphorous dissolved in it. This phosphorous doped silica layer provides an *erfc* source, and the sheet resistance decreases linearly with the square root of the diffusion time.

7.4.1. Local selective emitter solar cell with aluminum emitter contact

A mc-silicon wafer and a CZ-silicon wafer were used to fabricate the 1st spin on dopant solar cell in this project. The specification of the wafers is as follows.

Table 7-2: Substrate specification of spin on dopant solar cells

	Doping	Surface	Thickness (μm)	Resistivity (Ω cm)
mc-Si	p-type (Boron)	unpolished	250	~10
CZ-Si	p-type (Boron)	Single side polished	350	~10

This multicrystalline silicon is a commercial photovoltaic grade wafer donated by BP solar, Australia. The wafer was chemically polished by a method called "shiny etch". In this method a mixture of HNO_3 (70%) and HF(40%) at the ratio of 9:1 v/v was used at room temperature for 2 minutes with slight agitation. This not only removes about 10 μm of silicon layer from both sides of the unpolished wafer, but also reduces the roughness of the wafer from 1μm to less than 100 nm.. This process will get rid of the saw damage as well as the metallic contamination on the surfaces.

The CZ- silicon used in this process is laboratory grade and also shiny etched to remove the saw damage.

Other procedures are the same for both cells and are described here.

1. RCA 1 and RCA 2 clean

2. SOG (Phosphorosilicafilm-3 x 10^{20}) was spun at 4000 rpm.

3. Dried on hotplate at 100 °C for 1 min.

4. Diffusion in N_2 environment at 1100 °C for 15 min. (sheet resistance=10 Ω/square)

5. Phosphorosilica glass was removed using buffered oxide etch (BOE).

6. Aluminium (1.8μm) was sputtered to front and rear.

7. Emitter contacts were photolithographically defined and unwanted aluminium was etched away using wet Al-etch

8. Heavily diffused emitter (except the finger region) was etched for 30 sec using HNO_3:HF (100:1) – Resultant sheet resistance is around 50 Ω/□.

9. Titaniumsilica film was spun to the front as antireflection coating.

10. Annealed at 475° C for 30 min on hotplate.

11. Cells were isolated to remove the edge shunting.

12. I-V characteristic was performed using HP-semiconductor parameter analyser using the 2 probe technique.

The effective overall cell size is 2 x 2cm. As the Hewlett Packard 4155A parameter analyser can handle a maximum current of 100 mA, it was not possible to test this 2 x 2 cm cell in AM1.5 light condition. Our light source was a halogen lamp calibrated using a solar cell of known efficiency. For more accurate characterisation, few cells were sent to UNSW for efficiency varificartion.

The first mc-Si substrate solar cell and the CZ-Si solar cell fabricated in this works showed an encouraging result. I-V characterisation of the mc-Si substrate solar cell is shown in Figure 7-2. The open circuit voltage was around 530 mV. The I-V data clearly shows a leakage current which is indicated by a low shunt resistance which affect the fill factor extensively and hence the solar cell efficiency.

Si-wafer

SOG predeposition

Diffusion at 1100 C followed by phosphoroglass removel

Aluminium sputtering

Photoresist defined by photolithography

Al Emitter contact is defined by wet chemical etching

15 sec HNO$_3$:HF (100:1v/v) etching

N^{++} selective emitter contact region

Aluminium rear contact evaporation

Titaniumsilicafilm Antireflection coating

N^+
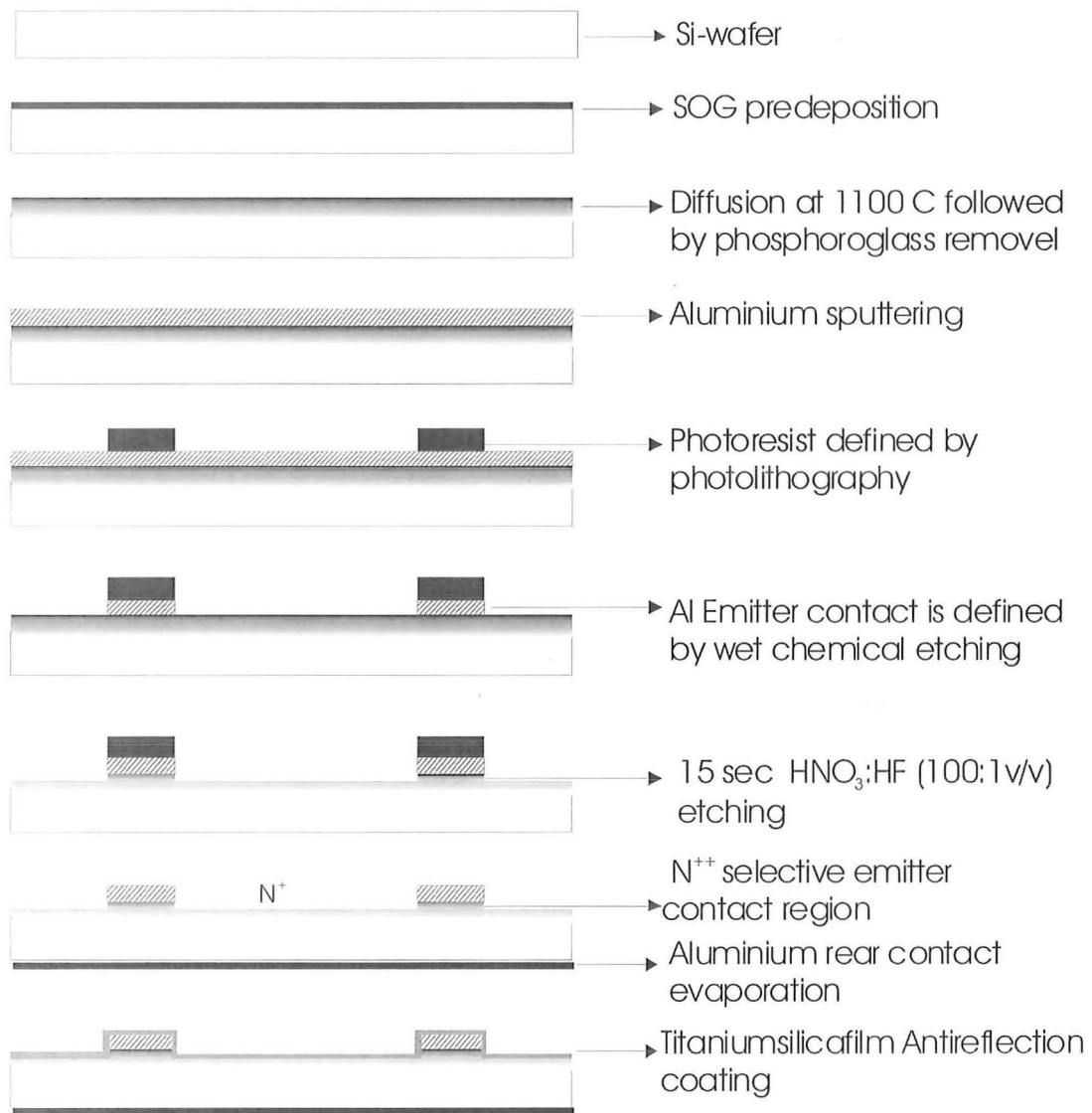
Figure 7-1: Schematic representation of spin on dopant silicon solar cell fabrication.

A fast data acquisition mode led to the picking up of the main frequency of the power supply and is clearly seen by the ripples in Figure 7-2 and Figure 7-3. This problem was solved by choosing a rather slow data acquisition mode in characterising the other sets of cells. This is a demonstration for the ability to make working solar cells.

I-V characterisation of the CZ-Si substrate solar cell is shown in Figure 7-3. The open circuit voltage was around 520 mV.
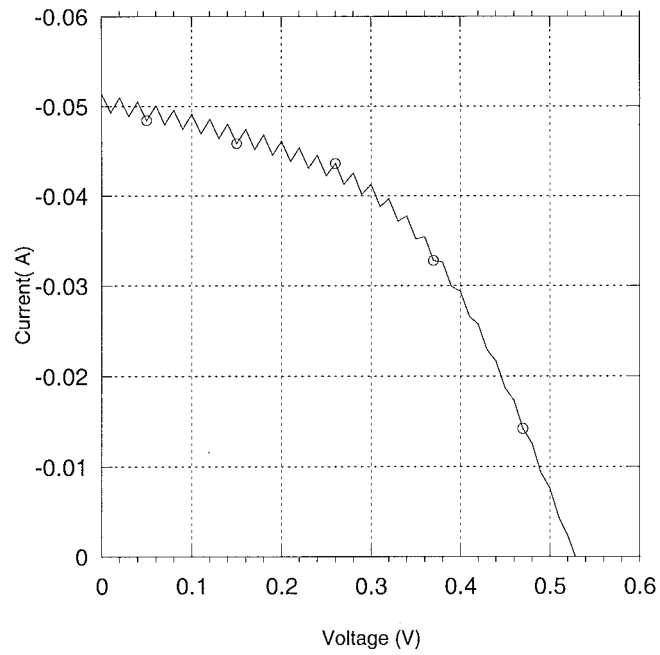
Figure 7-2: The I-V characteristic of a 2 x 2 cm, multicrystalline-silicon substrate solar cell fabricated using spin on dopant diffusion source and Titaniumsilicafilm ARC. An uncallibrated light source was used for this measurement.
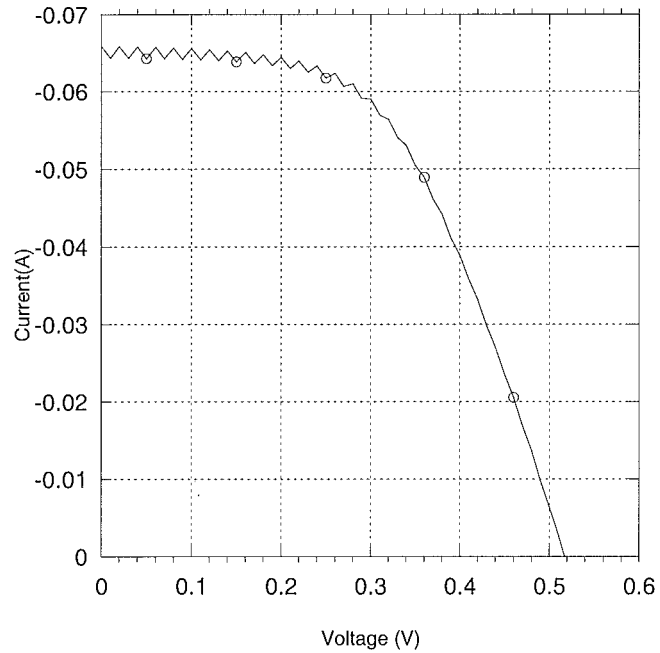
Figure 7-3: The IV characteristic of a CZ- Si substrate solar cell made using spin on dopant diffusion source. An uncallibrated light source was used for this measurement. Titaniumsilicafilm was used as ARC. The cell size is 2 x 2 cm.

7.4.2. Role of aluminium emitter contact.

Aluminium is a cheap metal compared to other possible emitter contacts metals such as silver. Solar cell friendliness(does not create considerable defect) and high adhesion to silicon are the other main advantages of aluminium. However, it was noted that vacuum evaporated aluminium emitter contacts tend to shunt through the shallow emitter easily at temperatures above 400 C while sputtered aluminium withstand at temperatures as high as $500°$ C. An Al / Si (98 / 2 %) alloy was found better than pure aluminium for emitter contacts. Al / Si alloy can stand temperatures as high as $550°$ C without shunting.

7.4.3. Double layer photolithography for thick metal lift off.

To reduce series resistance and improve current density, thicker metal contact is necessary. A special double layer photoresist system was used to lift off 1μm silver. In this technique,

1. AZ 4620 photoresist was spun at 5000 rpm

2. Soft baked for 2 min at $100°$ C on a hotplate

3. Flood exposed for 1 min

4. AZ 1500(20 cp) photoresist was spun at 4000 rpm for 1 min and softbaked for 1 min.

5. Exposed for 12 sec under emitter contact mask

6. Developed for 45 sec in AZ 300 MIF developer.
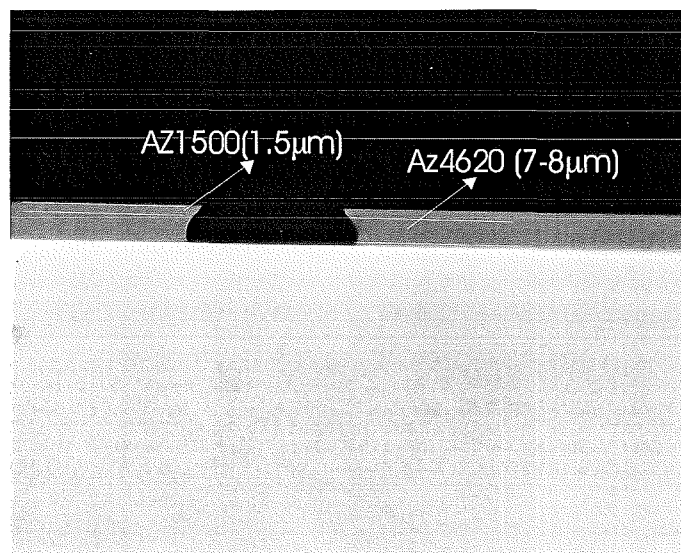
Figure 7-4: Optical microscope photograph of the double layer photoresist system for thick metal lift off.

The optical microscope image of the double layer photoresist system and its resultant developed pattern is shown in Figure 7-4. This technique is capable to lift off even 2μm metals.

7.4.4. Back surface field (BSF) solar cell with Ti/Pd/Ag emitter contact

Back surface field improve cell efficiency by improving open circuit voltage and short circuit current density [76].

High quality FZ-silicon wafer was used in this work. The specification of the wafer is as follows.

Table 7-3: Specification of the FZ silicon wafer

Growth	Doping	Surface	Thickness (μm)	Resistivity (Ω cm)
FZ, (50mm), <100>	p-type (Boron)	Double side polished	300	~5

Approximately 10μm silicon layer was removed by wet etching technique from the wafer to remove saw damage. Usual RCA cleaning was performed before starting the fabrication process. The fabrication process of Boron BSF solar cell with Ti/Pd/Ag emitter contact is shown schematically in Figure 7-5.

Si-wafer(FZ)

Thermal Oxidation(100nm)

Cell window opening

Phosphorosilicafilm predeposition

Borosilicafilm predeposition

Simultaneous diffusion of phosphorous and Boron

Phosphorosilica glass and Borosilica glass are removed

Thermal Oxidation for passivation and mask for local emitter diffusion

Local emitter diffusion by SOG 5×10^{20} followed by drive in

(Ti/Pd/Ag) emitter metalisation by lift off technique

Al (99.999%) evaporation

Figure 7-5: Schematic representation of BSF and local emitter silicon solar cell fabrication.

The important fabrication steps of the BSF and local selective emitter solar cell are shown in Figure 7-5. Phosphorosilicafilm-3×10^{20} was used to diffuse the emitter area at 950C for 15 min and Phosphorosilicafilm-5×10^{20} was used to diffuse the local selective emitter at 1000° C for 30 min. These diffusion steps would result in 50Ω /□ emitter sheet resistance and $10\ \Omega$ /□ local emitter contact sheet resistance. Borosilicafilm100 was used to diffuse the back surface field. Four 10 x 10mm cells were fabricated in a 50mm wafer and isolated finally by cleaving.

7.4.1.1   Ti / Pd / Ag emitter contact

Al shunts through the emitter when annealed above 400 C. Ag is the best metal for emitter contact as it has very high conductivity. However the adhesion of Ag with silicon is very poor. Therefore Ti and Pd have to be used for adhesion improvement. A 20 nm of Ti, 20 nm of Pd and 1 μm Ag were evaporated using e-beam evaporation technique and a double layer PR system was used to lift off. The cells were annealed at 400° C for 30 min in nitrogen environment in the tube furnace shown in Chapter 2.

7.4.1.2   I-V characterisation

The I-V characteristic was performed using the HP- parameter analyser using the two point probe technique. A calibrated halogen lamp was used to illuminate the cell. After this measurement, another 1 μm of Ag was added on top of the Ti /Pd /Ag using double layer photoresist and lift off.
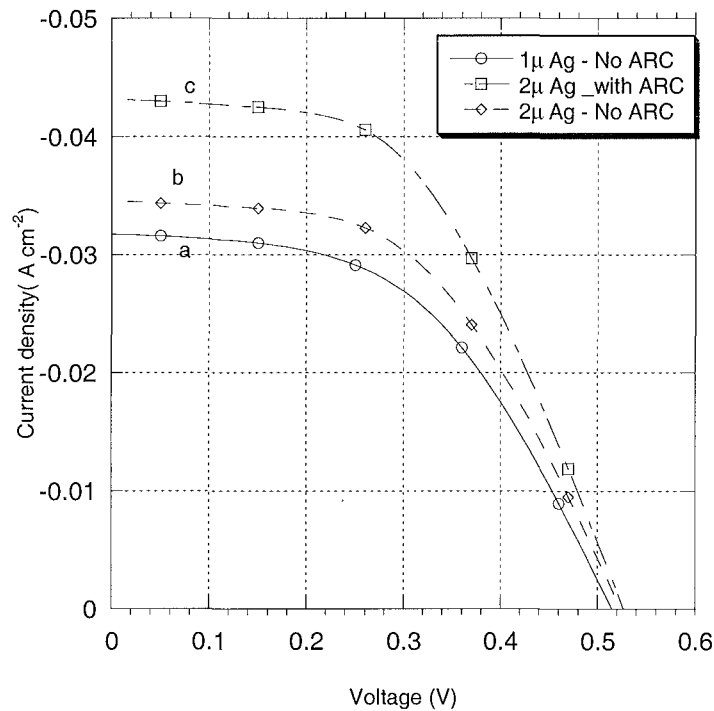
Figure 7-6: SOG solar cell with Boron back surface field. (a) 1μm of Ag without ARC. (b) 2μm of Ag without ARC. (c) 2μm of Ag with Titaniumsilicafilm ARC.

As can be seen in Figure 7-6, 2μm Ag emitter contact gives about 8% more current density and adding an antireflection coating boosts the current density by 35%. However, the open circuit voltage is around 520 mV despite the high quality FZ-Si substrate.

7.4.1.3   Effect of Boron back surface field

Borosilicafilm (Emulsitone company) spin-on dopant source was used for back surface field. However, it is reported that boron diffusion causes high surface damage and low carrier lifetime in silicon solar cells [15]. However it is solved by selective BSF diffusion.

7.5   Solid Diffusion Source Doping Solar Cells

Spin on dopant source solar cells were not successful as far as the V_{oc} and efficiency are concerned. We suspected the quality of the source and moved to solid diffusion source. Hereafter a PH950 solid diffusion source will be used for making n-type junction for solar cells. PH950 solid diffusion source consists of an active component Silicon Pyrophosphate (SiP_2O_7) carried on and in an inert porous Silicon Carbide (SiC) substrate. Prior to actual silicon diffusion take place, new phosphorus source wafers were annealed at 950° C in an ambient of 100% N_2 for 8 hours to activate the P source. Several textured as well as untextured solar cells were made using the solid diffusion source and the best results are presented in this chapter.

7.5.1. RIE textured silicon solar cells

One 50mm FZ-silicon substrate and other CZ-silicon substrate were used in this batch to fabricate the textured solar cell. Four 10x10mm cells were fabricated on every wafer.

Table 7-4 : Substrate specification for textured silicon solar cells

Substrate	Doping	Surface	Thickness (μm)	Resistivity (Ω cm)
CZ-Si	p-type (Boron)	Single side polished	350	~10
FZ-Si	p-type (Boron)	Double side polished	300	~5

The substrate specification for the RIE textured solar cells are shown in Table 7-4. A mask of hexagonally arranged 8μm dots in 10 μm pitch was used to transfer the pattern

photolithographically on AZ4620 thick resist, which was used as etch mask for RIE

texturing. RIE etch condition is shown in Table 7-5.

Table 7-5: RIE etch condition for SF6 plasma etching

SF$_6$ Flow rate	Temperature	RF power	Etch pressure	Time
160 sccm	173K	200W	150 mT	7 min

The textured pillars were about 7-8 μm high and are similar to the surface shown in

Figure 3-27. A 5 min defect removal etching was performed in HNO$_3$: HF (50:1) solution.

This step removed about 3 μm of silicon at a rate of 0.6μm/min. The cell fabrication steps

are given in Table 7-6 and schematically shown in Figure 7-7.

Table 7-6: Process sequence of the CZ-Si and FZ –Si textured solar cells

Steps	Details
1. Cleaning	RCA 1 and RCA 2
2. RIE texturing	SF$_6$, 160sccm, 200 W, 150 mT, 7 min
3. Oxide growth	950°C for 2 hours in O$_2$
4. Cell size	10 X10mm
5. Finger opening	optical lithography followed by BOE
6. Finger selective (N^{++}) predeposition	950°C for 30 min.
7. Emitter window opening	Optical lithography followed by Buffered Oxide Etch (BOE). (HF:H$_4$NF=1:7)
8. Emitter N$^+$ predeposition	Phosphorous predeposition at 875° C for 30min
9. Deglaze	BOE
10. Back surface field (BSF)	2 μm of 99.999 % Al was evaporated using Balzers thermal evaporator.
11. Simultaneous drive in of Phosphorous and Al and oxide passivation	5% O$_2$ and N$_2$ at 1050°C for 3 hours.
12. Oxide patterning	For Front metallisation
13. Optical lithography for top contact	Lift off.
14. Emitter contact	Tl/Pd/Ag (30nm/30nm/100nm) were evaporated.
15. Thickening the fingers	Ag metal lift off (1μm Ag)
16. Back metal contact	2 μm Al evaporated using Balzers physical evaporator.
17. Sintering	450°C, 30 min in Forming gas.
18. Cell isolation	Diced using diamond saw

A double layer thick photoresist was used to add further 1μm Ag on top of the Ti/Pd/Ag (30nm/30nm/100nm) emitter contact.

→ Si-wafer

→ Texturing

→ Thermal Oxidation(100nm) for local emitter diffusion

→ local emitter diffusion (Phosphorous predeposition)

→ emitter diffusion (Phosphorous predeposition)

→ Al predeposition

→ Simultaneous diffusion(drive in) of phosphorus and Al. and Oxide passivation

→ emitter metalisation(Ti/Pd/Ag)

→ Back metalisation(Al) followed by Forming gas annealing
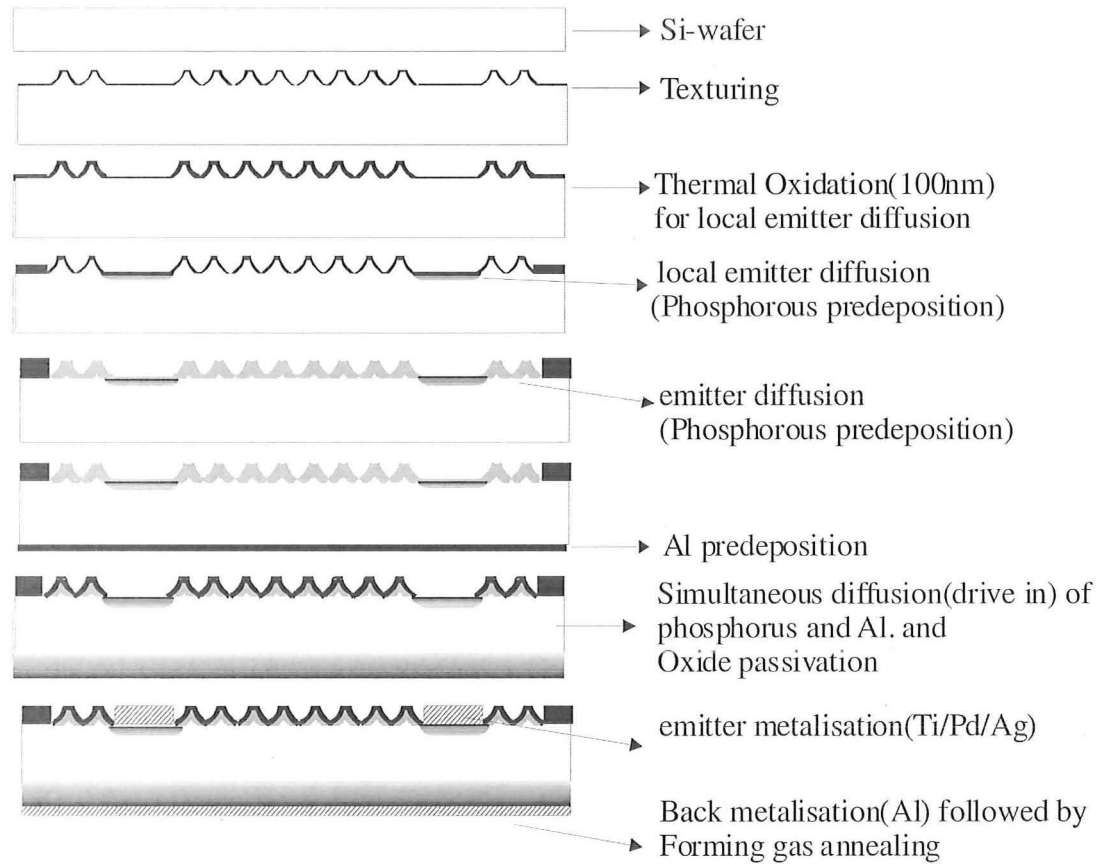
Figure 7-7: Schematic diagram of the process sequence of textured silicon solar cell

emitter metalisation(Ti/Pd/Ag)
Thermal Oxide passivation and ARC
→ Thermal Oxide
N⁺ Phosphorous diffusion
N⁺⁺ Phosphorous diffusion
Alloyed Al
▲ Back metalisation(Al)
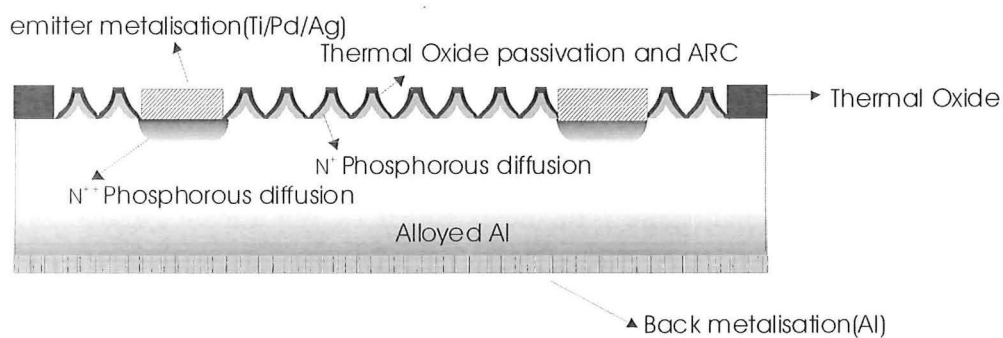
Figure 7-8: Schematic diagram of the textured silicon solar cell

Alloyed aluminium was used as back surface field and 110 nm of thermal oxide was grown for surface passivation and ARC. Figure 7-8 shows details of the structure of the

finished cell. The sheet resistance of the emitter and local emitter was measured using four point probe technique and was found as around 150 $\Omega/\square$ and 20 $\Omega/\square$ respectively.

7.5.1.1   I-V characteristics of RIE textured Si solar cells

The I-V characteristics of the textured cells were measured using a calibrated halogen lamp under AM 1.5 condition at room temperature. The lamp intensity was calibrated using a solar cell of know efficiency.
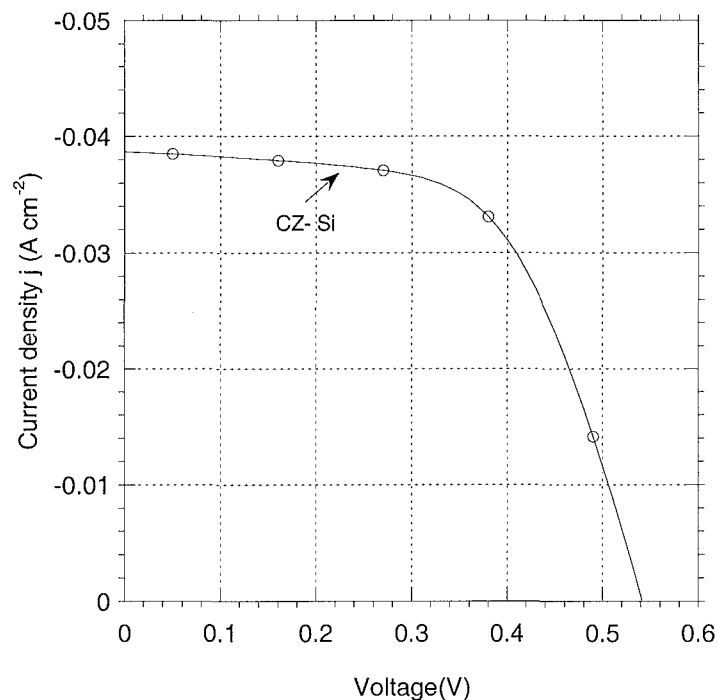
Figure 7-9: I-V characteristics of a textured CZ- Si solar cell with selective emitter. The estimated efficiency of this cell is 13.5%.

As shown in Figure 7-9 and Figure 7-10, the measured V_{oc} was around 540 mV for CZ-Si wafer and 560 for FZ-Si substrate. There was a marked difference in j_{sc} as well and was 38.6 mA cm^{-2} for CZ-Si solar cell and 40.5 mA cm^{-2} for FZ-Si cell. The efficiency was calculated by comparing their performance with a 20% efficient pyramid textured FZ-Si solar cell fabricated by Photovoltaic Specialists Centre (PVSC), University of New South Wales (UNSW), Australia. The efficiency of the CZ-Si solar cell was around 13.5% and the FZ-Si solar cell was around 14% with fill factor of about 58%.
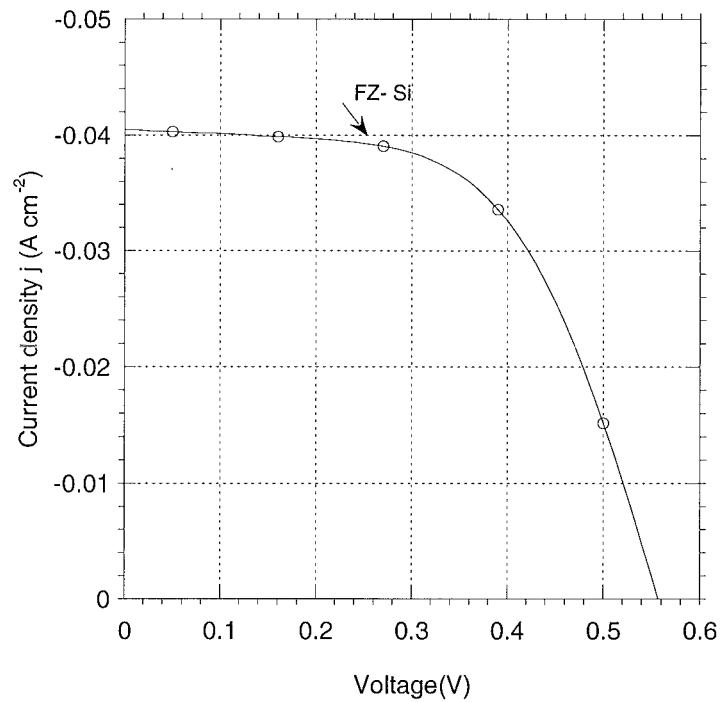
Figure 7-10: I-V characteristics of a textured FZ- Si solar cell with selective emitter. The estimated efficiency of this cell is 14%.

7.5.2. Untextured low resistivity FZ-Si solar cells

In this batch, an extremely high quality float-zone wafer (manufactured by Wacker) donated by PVSC, UNSW, was used to fabricate the cell. Four 1x1 cm cells were fabricated on one quarter of a 100mm diameter wafer.

Table 7-7: Substrate specification of Wacker wafer.

Substrate	Doping	Surface	Thickness (μm)	Resistivity (Ω cm)
FZ-Si ,<100>	p-type (Boron)	Double side semi polished	350	0.8-1.2

The wafer specification is given in Table 7-7. The fabrication step is illustrated in Table 7-8. The solid diffusion source was used for a sheet resistance of 150 Ω/□ for the emitter

area and 20 $\Omega/\square$ for the local emitter. Sputtering was used for all metallisation to avoid contamination of other metals such as gold from the physical evaporator. Figure 7-11 shows the main fabrication steps and Figure 7-12 shows the finished cell schematically.

Table 7-8: The steps involved in the fabrication of selective emitter solar cell

Steps	Details
1. Cleaning	RCA1 and RCA2
2. Oxide growth	950°C for 2 hours in O_2
3. Cell size	10 x10mm
4. Finger opening	optical lithography followed by BOE
5. Finger selective (N^{++}) predeposition	950°C for 30 min (Ph950 solid diffusion source)
6. Emitter window opening	Optical lithography followed by Buffered Oxide Etch(BOE). (HF:H_4NF=1:7)
7. Emitter N^+ predeposition	Phosphorous predeposition at 875° C for 30min (Ph950 solid diffusion source)
8. Deglaze	BOE
9. Back surface field (BSF)	99.999 % Al was sputtered to the back.
10. Simultaneous drive in of Phosphorous and Al and oxide passivation	5% O_2 and N_2 at 1050°C for 3 hours.
11. Oxide patterning	Front metallisation
12. Optical lithography for top contact	Lift off.
13. Emitter contact	Ti/Pd/Ag (30nm/30nm/100nm) were Sputtered
14. Thickening the fingers	Ag metal lift off (1μm Ag)- sputtered
15. Back metal contact	2 μm Al sputtering for back contact
16. Sintering	500°C, 30 min in Forming gas.
17. Cell isolation	Diced using diamond saw

► Si-wafer

► Thermal Oxidation(100nm)

► Finger window opening

► N⁺⁺ predeposition

► Emitter window opening

► N⁺ predeposition

► Al predeposition

► Simultaneous diffusion(drive in) of phosphorous and Al and thermal oxide passivation

► window for emitter metalisation

► emitter metalisation (Ti/Pd/Ag)

► Back metalisation (Al) followed by Forming gas annealing
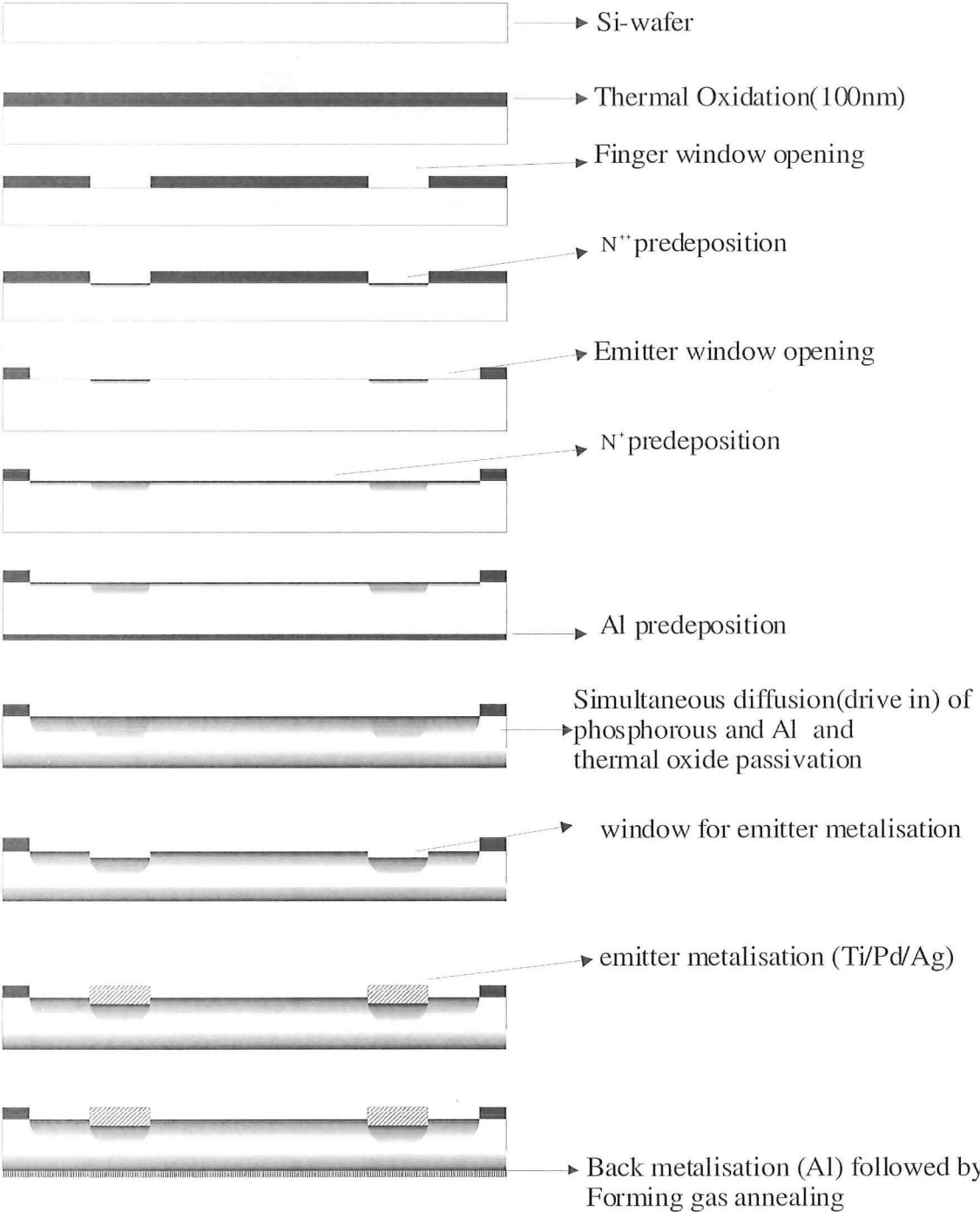
Figure 7-11: Schematic of the selective local emitter silicon solar cell preparation.
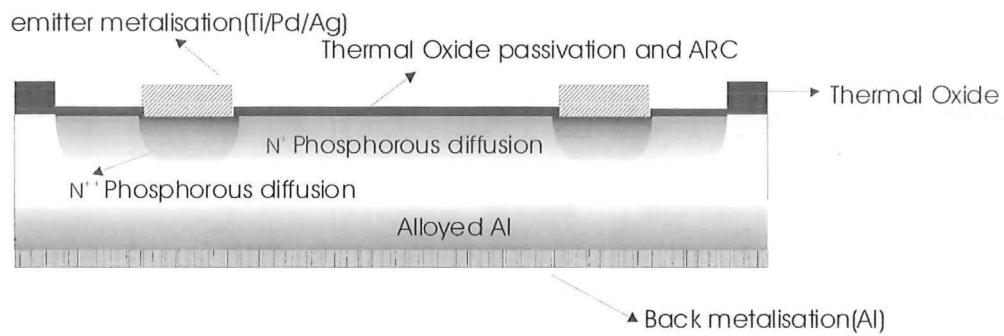
Figure 7-12: Schematic description of selective local emitter solar cell.

7.5.1.2 I-V characteristics of untextured low resistivity FZ-Si solar cells

The I-V characteristic of a local selective emitter solar cell is shown in Figure 7-13. The light used was a halogen lamp with an approximate power of 100 mW cm^{-2}.
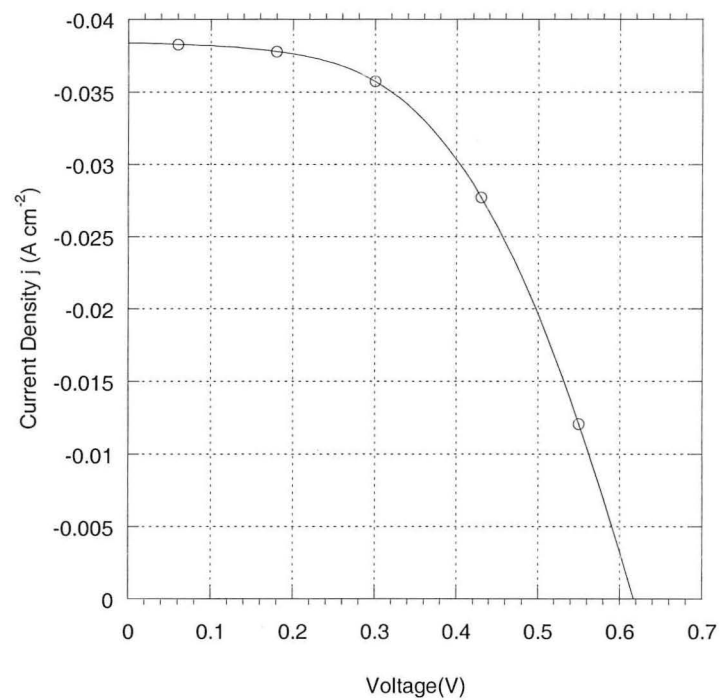
Figure 7-13: I-V characteristics of 18.7 % efficient local selective emitter solar cell (η=18.7%)

The main reason for this high open circuit voltage and efficiency may be due to the low resistivity, the high quality of the Wacker's FZ- silicon wafer and use of sputtering instead of thermal evaporation.

The measured V_{oc} was around 620 mV for this FZ-Si substrate. The j_{sc} was measured as 38.4 mA cm^{-2} .The efficiency was calculated as 18.7 %by comparing its performance with a 20% efficient pyramid textured FZ-Si solar cell fabricated by Photovoltaic Specialists Centre (PVSC), University of New South Wales (UNSW), Australia. The fill factor was calculated as 51%. The low fill factor may be due to the series resistance added by the testing probes. This could be avoided by using four point probe I-V characterisation technique.

7.6 Furnace Contamination Test
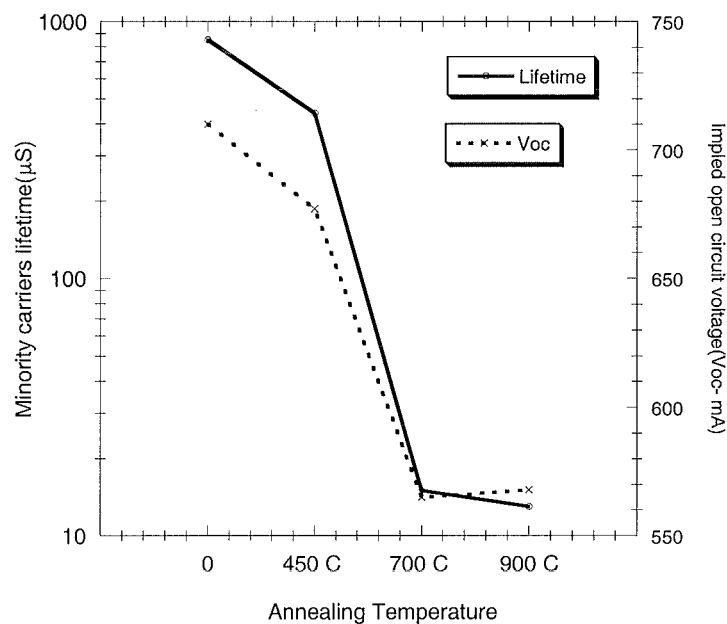
Figure 7-14: Minority carrier lifetime and the implied V_{oc} of FZ-Si wafers annealed at different temperature in forming gas is compared with a reference wafer.

Contaminated diffusion furnace is suspected to be the main reason for low V_{oc} measured for most of the cells. The following experiment supports this argument. Figure 7-14 shows the minority carrier lifetime and the corresponding implied V_{oc} of four FZ-Si substrates of 5 Ω cm resistivity placed in the diffusion furnace tube at different

temperatures for 1 hour in forming gas environment. Data show that when a silicon substrate is placed in this furnace at temperature above 700° C, the minority carrier lifetime reduces sharply below 20 μS and the implied V_{oc} reduces below 570 mV.

7.7 Summary

Spin on dopant source and solid diffusion source were successfully used to fabricate Si solar cells. mc-Si, CZ-Si and FZ-Si wafers were used to make solar cells. Textured as well as untextured substrates were used to fabricate different types of cells. The maximum V_{oc} of 620 mV was obtained for the Wacker's FZ wafer of approximately 1 Ω cm resistivity while V_{oc} of 560 mV was obtained for the textured FZ wafer of approximately 5 Ω cm resistivity. RIE textured FZ silicon wafer with thermal oxide ARC showed a short circuit current density of 40.5 mA cm^{-2} which is in agreement with the PV-optics modelling in Chapter 6. Minority carrier lifetime results in Chapter 4 predicted a V_{oc} of more than 700 mV for untextured FZ-Si substrates of 5 Ω cm resistivity and even more for 1 Ω cm resistivity. The furnace contamination test results clearly show that solar cells fabricated at temperatures above 700° C in this diffusion furnace from substrate resistivity of 5 Ω cm will not exhibit V_{oc} of more than 570mV. A lower resistivity substrate can exhibit relatively higher V_{oc} [77]. This result reflected in most of the solar cells fabricated in this tube furnace. Heavy metal or gold contamination in the tube furnace is suspected for this low V_{oc} and efficiency.

CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

8.1.   Conclusions

Optimised light trapping structures were achieved by plasma texturing of hexagonally arranged holes and column structures. Maskless texturing was also highly successful. This was achieved by RIE texturing using SF_6/O_2 (90/20 sccm) plasma at 173 K for 10 minutes at an RF power of 0.45 W/cm^2.

For cone-type texturing, the reflectance was less than 0.5% in the majority of the absorptive region of the solar spectrum. However, the reflectance of the maskless etched wafer is very impressive as it is very cost effective compared to the masked process. Less than 1% reflectance was observed in most of the effective region of the spectrum for this maskless textured silicon substrate. These reflectance measurements were performed without any anti reflection coatings. Our results show that a good texturing does not need any antireflection coating except a thin SiO_2 or Si_xN_y needed for surface passivation.

However the effective lifetime measurements on SF_6/O_2 plasma textured silicon substrates revealed a very high level of plasma induced damage. A wet chemical defect removal etching helped considerably recover the lifetime. The damaged layer appeared to be very deep and spread beyond 4μm for the most of the textured substrates etched with full power. A deep chemical etching tends to remove the textured structures. Alternatively, a less reactive SF_6 plasma was used to texture silicon substrates. In this case also the plasma damaged layer appeared to be deeper than 5 microns. Therefore, relatively larger structures were textured and deeper defect removal etching was performed. Typically, 8μm dots in 10 μm pitch were textured and deeper DRE was performed. For SF_6-RIE textured silicon substrates, the effective lifetime was reduced from 1.2 ms to few μs and then recovered to around 800 μs after a defect removal etching of around 2-3 μm of silicon.

However one of our latest results showed that, 10 minutes of low power (17W) reactive ion etching using 20sccm SF_6 on FZ-Si of similar specification gave as high as 400 µs lifetime and an implied V_{oc} of 660mV without any DRE. In this case no mask is used and the etched depth is around 400 nm and the surface profile is planar.

However, a high density plasma etcher using electron cyclotron resonance (ECR) source exhibited relatively lower damage than that of conventional parallel plate RIE. This ECR etching was done at Delft Institute of Microelectronics and Submicron Technology (DIMES), Delft University of Technology, Netherlands. It is encouraging to notice that for ECR textured wafer, the minority carriers lifetime is around 250 microseconds even before the DRE process which indicates that high open circuit voltages can be obtained using these textured substrates even without DRE. The calculated open circuit voltage (implied Voc) for this ECR textured FZ- Si substrate was 640 mV. A defect removal etching of 2-3 µm of silicon recovered the effective lifetime to around 750 µm which is equivalent to an implied V_{oc} of 680 mV. Since the high density plasma etched substrate has less defects, we can conclude that the defect is process dependent and can be minimized by choosing appropriate plasma conditions.

A correlation between the surface area increment due to texturing and the drop in minority carrier lifetime was established. It was found that the minority carrier lifetime drop due to surface area increment is proportional to the area increase due to texturing.

Therefore, the drop in minority carrier lifetime is not only due to plasma induced damage, but partially due to an increase in surface recombination due to an increase in the surface area.

Photoluminescence studies of plasma textured multicrystalline silicon substrates suggested that ion bombardment of the silicon surface during RIE produces defects giving rise to the carbon related defect centres. By adding oxygen to the SF_6 plasma, the contamination of the silicon surface by oxygen atoms is shown to considerably affect the PL spectra. The oxygen contamination enhances the PL centres via the creation of extended defects, such as oxygen precipitates. A lattice contraction near these extended defects is suggested to be the observed splitting of the C and G lines. However, the minority carrier lifetime results reported in Chapter 4 showed that oxygen less SF_6 plasma texturing also causes significant defects in silicon substrates and results in a decrease in open circuit voltage of solar cells.

Radiation may play a considerable role in causing damage during RIE process because the C and G lines were observed by others for the substrates irradiated with e⁻.

The splitting of PL lines after annealing suggests that those associated defects may not be annealed out further.

The SF$_6$ textured 10μm pitch structures did not exhibit low reflectance as these structures were not optimized for minimum reflection. Larger pitch of the structures and much longer defect removal etching caused high reflectance. But the minority carriers lifetime analysis and the photoluminescence analysis shows that longer DRE is inevitable to achieve a high open circuit voltage.

The PV-Optics modeling shows that the maximum achievable current density (MACD) could be increased from 33.8 mA/cm^2 for a planer silicon to 41.3 mA/cm^2 for textured silicon. It also shows that for a textured silicon with reflectance as high as 4% could exhibit MACD of above 39.5 mA/cm^2.

Therefore, there is a tradeoff between the open circuit voltage and short circuit current for a high efficiency silicon solar cell. For a high minority carriers lifetime and hence for a high V_{oc}, a deep defect removal etching is needed. However, a deep defect removal etching would increase the reflectance and, hence, would reduce the I_{sc}. For a high efficiency solar cell a balanced must be maintained in optimizing V_{oc} and I_{sc}.

There are a few disadvantages of texturing as well. More care is required in handling the textured wafers as they tend to break easily. Textured surfaces are much more effective in coupling light of all wavelengths into the cells, including unwanted infrared radiation of insufficient photon energy to create electron-hole pairs. This tends to make the cell run hotter.

Finally, several solar cells were fabricated and tested. Spin on dopant source and solid diffusion source were successfully used to fabricate Si solar cells. mc-Si, CZ-Si and FZ-Si were used to make cells. Textured as well as untextured substrates were used to fabricate different types of cells.

A two layer photolithography system using a thin and a thick photoresist system was developed to lift off thick metal emitter contact.

The maximum V_{oc} of 620 mV was obtained for the Wacker's FZ wafer of approximately 1 Ω cm resistivity while V_{oc} of 560 mV was obtained for the textured FZ wafer of approximately 5 Ω cm resistivity. RIE textured FZ silicon wafer with thermal oxide ARC exhibited a short circuit current density of 40.5 mA cm^{-2}, which is in agreement with the PV-optics modelling in Chapter 6. Minority carriers lifetime results in Chapter 4 predicted the V_{oc} of more than 700 mV for untextured FZ-Si substrates of 5 Ω cm resistivity and even more for 1 Ω cm resistivity. Contaminated diffusion furnace tube is suspected to be the main cause for the low V_{oc} obtained in our work. An experiment on a few FZ-Si wafers treated in this particular furnace tube confirmed this suspicion. The lifetime measurements on these substrates suggested that solar cells fabricated from substrate resistivity of 5 Ω cm at temperatures above 700° C in this diffusion furnace would not exhibit V_{oc} of more than 570mV.

8.2.   Recommendations For Future Work

In the absence of a lifetime tester, photoluminescence analysis on plasma textured FZ–Si could be used for investigating the plasma induced defects in the bulk near the surface. This is possible if a more sensitive detector of wide range is acquired. Currently, the lower limit of the detector used in this work is 800meV. The sample dos not need surface passivation for PL analysis. This is one of the advantages of minimising the plasma induced defect by observing the defects level by PL measurement.

A better solar cell could be fabricated from ECR textured substrates in a TCA cleaned furnace tube.

Conventional silicon solar cell processes involve large amount of chemical waste. Also the amount of deionised water required for traditional processing is a very significant cost factor in solar cell production. In future, the following recommendation should be considered when fabricating a silicon solar cell with minimum use of wet chemicals and deionised water. This is driven partly by environmental concern but also by economic considerations.

Less reactive SF_6 plasma with very low dc-bias and power could be used to remove the plasma induced defect instead of chemical defect removal etching.   An optimised maskless texturing method could be used to eliminate unnecessary photolithography steps. Nano and micro imprint technology and interferometric lithography also could be used to texture the solar cell surface.

At least 10 nm of SiO_2 is needed for surface passivation. Nowadays photolithography is used to etch away the SiO_2 layer for defining the front metal contacts. Instead of photolithography, a reusable PDMS shadow mask could be used to remove this thin layer of SiO_2 in the contact region. Screen printing of front metal contacts will further reduce the waste of chemicals and deionised water.

REFERENCES

[1]   A. Luque, "Novel high efficiency concepts in photovoltaics to change the energy
       system," International Conference for Renewable Energies, Bonn,
       http://europa.eu.int/comm/energy/res/events/doc/2004_06_02_bonn_antonio_luque.
       pdf, 2004.

[2]   D. S. Ruby, S. H. Zaidi, and S. Narayanan, "Plasma-texturization for
       multicrystalline silicon solar cells," 28th IEEE Photovoltaic Specialists Conference,
       p. 75 -78, 2000.

[3]   J. Zhao, A. Wang, and M. A. Green, "19.8% efficient "honeycomb" textured
       multicrystalline and 24.4% monocrystalline silicon solar cells," *Applied Physics
       Letters*, vol. 73, p. 1991-1998, 1998.

[4]   "Statistics of the world's solar cell production," in *PV News 2004*:
       http://www.pvenergy.com/news.html, 2004.

[5]   "Efficiencies of solar cells," in *http://www.pvresources.com/*, 2004.

[6]   D. H. Macdonald, A. Cuevas, M. J. Kerr, C. Samundsett, D. Ruby, S. Winderbaum,
       and A. Leo, "Texturing industrial multicrystalline silicon solar cells," *Solar Energy*,
       vol. 76, p. 277-283, 2004.

[7]   O. Schultz, S. W. Glunz, J. C. Goldschmidt, H. Lautenschlager, A. Leimenstoll, E.
       Schneiderlöchner, and G. P. Willeke, "Thermal Oxidation Processes For High-
       Efficiency Multicrystalline Silicon Solar Cells," 19th European Photovoltaic Solar
       Energy Conference, Paris, p. 604 - 607, 2004.

[8]   M. A. Green, *Solar cells - Operating Principles, Technology and System Applications*. N.J: Prentice Hall, 1982.

[9]   M. A. Green, "High Efficiency Silicon Solar Cells," *Trans tech Publications*, p. 69–82, 1987.

[10] M. C. King, "Principle of optical lithography," in *VLSI Electronics*, vol. 1, N. G. Einspruch, Ed. New York: Academic, 1981.

[11] J. H. Bruning, "A Tutorial on Optical Lithography," *Journal of the Electrochemical Society*, vol. 129, p. C102-C102, 1982.

[12] D. Bollinger, S. Lida, and O. Masumoto, "Reactive ion etching: Its Basics and Future, Part I," *Solid State Technology*, p. 111-117, 1984.

[13] D. M. Anos and D. L. Flamm, "Plasma Etching an Introduction," in *Plasma-Materials Interactions*: Academic Press Inc, 1989.

[14] W. J. Goedheer, *Plasma Source Sci. Technol*, vol. 9, p. 507-516, 2000.

[15] J. Zhao, "High Efficiency Silicon Concentrator Solar Cells," Ph.D thesis, *School of Electrical Engineering*. Sydney: University of New South Wales, 1989

[16] M. Schiller and W. Kulisch, "Plasma properties at the transition from remote to direct plasma," *Surface and Coatings Technology*, vol. 98, p. 1590-1599, 1998.

[17] A. G. Aberle, *Crystalline silicon solar cells: advanced surface passivation and analysis*. Sydney: Centre for Photovoltaic Engineering, University of New South Wales, 1999.

[18] H. Nagel, A. G. Aberle, and R. Hezel, "Optimised antireflection coatings for planar silicon solar cells using remote PECVD silicon nitride and porous silicon dioxide," *Progress in Photovoltaics*, vol. 7, p. 245-260, 1999.

[19] R. Howland and L. Benatar, *A practical guide to scanning probe microscopy*: Park Scientific Instruments, 2000.

[20] P. A. Basore and D. A. Clugston, "PC1D version 4 for Windows: from analysis to design," 25th IEEE Photovoltaic Specialists Conference, p. 377-381, 1996.

[21] M. A. Green, *Silicon Solar Cells*: Centre for Photovoltaic Devices and Systems, UNSW, Australia, 1995.

[22] A. Bittar,"Diffuse reflectance schematic at Industrial Research Limited, Wellington," Private Comunication, 2004

[23] S. Narayanan, "High efficiency polycrystalline silicon solar cells," Ph.D thesis, *Department of Engineering*: University of New South Wales, Australia, 1989

[24] P. Path, G. Wileke, E. Bucher, J. Szlufcic, R. M. Murti, K. De Clercq, J. Nijs, and R. Mertens, "Mechanical wafer engineering for high efficiency solar cells: An investigation of the induced surface damage," 24th IEEE Photovoltaic Specialists Conference, p. 1347-1350., 1994.

[25] R. R. Bilyalov, L. Stalmans, and L. Schirone, "Use of porus silicon antireflection coating in multicrystalline silicon solar cell processing," *IEEE Trans. Electron Devices*, vol. 46, p. 2035-2040, 1999.

[26] H. Jansen, M. D. Boer, and R. Legtenberg, "The black silicon method: a universal method for determining parameter settings of a fluorine-based reactive ion etcher in deep silicon trench etching with profile control," *Journal of Micromechanics and Microengineering*, vol. 5, p. 115-120, 1995.

[27] C. S. Fuller, "Fabrication of Semiconductor Devices," in *US patent 2,794,846*, 1954.

[28] H. G. Rudenberg and B. Dale, "Radiant Energy Transducer," in *US patent 3,150,999*, 1961.

[29] J. Haynos, J. Allison, R. Arndt, and A. Meulenberg, "The Comsat non Reflective Silicon Solar cell: A Second Generation Improved Cell," International Conference on Photovoltaic Power Generation, Hamburg, p. 487-490, 1974.

[30] C. R. Baraona and H. W. Brandhorst, "V-groove silicon solar cells," 11th IEEE Photovoltaic Specialists Conference, p. 44, 1975.

[31] M. A. Green, A. W. Blakers, J. Shi, E. M. Keller, and S. R. Wenham, "19.1% efficient silicon solar cell," *Applied Physics Letters*, vol. 44, p. 1163-1164, 1984.

[32] S. R. Wenham, M.A.Green, and M.Watt, *Applied Photovoltaics*. Sydney: Bridge Printry, 1993.

[33] H. Fischer and W. Pschunder, "Low cost solar cells based on large area unconventional silicon," 12th IEEE Photovoltaic Secialists Conference, p. 86-92, 1976.

[34] M. Elwenspoek and V. H. Jansen, *Silicon Micromachining*: Cambridge University Press, 1998.

[35] M. Schnell, R. Ludemann, and S. Schaefer, "Plasma surface texturization for multicrystalline silicon solar cells," 28th IEEE Photovoltaic Specialists Conference, p. 367-370, 2000.

[36] P. P. Altermatt, J. O. Schumacher, A. Cuevas, M. J. Kerr, S. W. Glunz, R. R. King, G. Heiser, and A. Schenk, "Numerical modeling of highly doped Si : P emitters

based on Fermi-Dirac statistics and self-consistent material parameters," *Journal of Applied Physics*, vol. 92, p. 3187-3197, 2002.

[37] A. B. Sproul, "Dimensionless Solution of the Equation Describing the Effect of Surface Recombination on Carrier Decay in Semiconductors," *Journal of Applied Physics*, vol. 76, p. 2851-2854, 1994.

[38] A. Cuevas and R. A. Sinton, "Prediction of the open-circuit voltage of solar cells from the steady-state photoconductance," *Prog. in Photovoltaics*, vol. 5, p. 79-90, 1997.

[39] A. Borghesi, B. Pivac, A. Sassella, and A. Stella, "Oxygen precipitation in silicon," *Journal of Applied Physics*, vol. 77, p. 4169-4244, 1995.

[40] R. A. Sinton and A. Cuevas, "Contactless determination of current-voltage characteristics and minority carrier lifetimes in semiconductors from quasi-steady-state photoconductance data," *Appl. Phys Lett.*, vol. 69, p. 2510-2512, 1996.

[41] G. Massetti, M. Severi, and S. Solmi, "Modeling of carrier mobility against carrier concentration in arsenic, phosphorus, and boron-doped silicon," *IEEE Trans. Electron Dev.*, vol. 30, p. 764 -769, 1983.

[42] F. Dannhauser, *Solid State Electron*, vol. 15, p. 1371-1376, 1972.

[43] R. A. Sinton, A. Cuevas, and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization," 25th IEEE Photovoltaics Specialist Conference, Washington, p. 457- 460, 1996.

[44] P. Manshanden, A. R. Burgers, W. A. Nositschka, O. Voige, and A. W. Weeber, "Silicon solar cells textured by low damage RIE with natural lithography," 29th IEEE Photovoltaic Specialists Conference, p. 324-327, 2002.

[45] G. S. Oehrlein, "Effects of ion bombardment in plasma etching on the fluorinated silicon surface layer: Real-time and postplasma surface studies," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 11, p. 34-46, 1993.

[46] R. Petri, P. Brault, O. Vatel, D. Henry, E. Andre, P. Dumas, and F. Salvan, "Silicon roughness induced by plasma etching," *Journal of Applied Physics*, vol. 75, p. 7498-7506, 1994.

[47] P. Brault, J. Mathias, C. Laure, P. Ranson, and O. Texier, "In-Situ Raman-Spectroscopy of Silicon Surfaces During Sf_6 Plasma-Etching," *Journal of Physics-Condensed Matter*, vol. 6, p. L1-L6, 1994.

[48] A. Belkacem, Y. Arnal, A. Chantre, and C. Pomot, "Electronic defects induced in p- and n-type silicon by SF_6 plasma etching," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 11, p. 709-716, 1993.

[49] H. Weman, J. L. Lindstrom, G. S. Oehrlein, and B. G. Svensson, "Reactive-ion- and plasma-etching-induced extended defects in silicon studied with photoluminescence," *Journal of Applied Physics*, vol. 67, p. 1013-1021, 1990.

[50] A. Henry, B. Monemar, J. L. Lindstrom, T. D. Bestwick, and G. S. Oehrlein, "Photoluminescence characterization of plasma exposed silicon surfaces," *Journal of Applied Physics*, vol. 70, p. 5597-5603, 1991.

[51] J. Weber, R. J. Davis, H. U. Habermeier, W. D. Sawyer, and M. Singh, "Photoluminescence Detection of Impurities Introduced in Silicon by Dry Etching Processes," *Applied Physics a-Materials Science & Processing*, vol. 41, p. 175-178, 1986.

[52] P. J. Dean, J. R. Haynes, and W. F. Flood, "New Radiative Recombination Processes Involving Neutral Donors and accepters in Silicon Germanium," *Physical Review*, vol. 161, p. 711, 1967.

[53] G. Davies, "The optical properties of luminescence centres in silicon," *Physics Reports*, vol. 176, p. 83-188, 1989.

[54] I. A. Buyanova, A. Henry, B. Monemar, J. L. Lindstrom, and G. S. Oehrlein, "Photoluminescence of defects induced in silicon by SF_6/O_2 reactive-ion etching," *Journal of Applied Physics*, vol. 78, p. 3348-3352, 1995.

[55] A. V. Mudryi, A. I. Patuk, I. A. Shakin, A. G. Ulyashin, R. Job, W. R. Fahrner, A. Fedotov, A. Mazanik, and N. Drozdov, "Impurities and defects in multicrystalline silicon for solar cells: low-temperature photoluminescence investigations," *Solar Energy Materials and Solar Cells*, vol. 72, p. 503-508, 2002.

[56] N. Magnea, A. Lazrak, and J. L. Pautrat, "Luminescence of carbon and oxygen related complexes in annealed silicon," *Applied Physics Letters*, vol. 45, p. 60-62, 1984.

[57] J. W. Corbett, R. S. McDonald, and G. D. Watkins, "Luminescent centres and anneling in silicon," *J. Phys. Chem. Solids*, vol. 25, p. 873, 1964.

[58] E. Irion, N. Burger, K. Thonke, and R. Sauer, "The defect luminescence spectrum at 0.9351 eV in carbon-doped heat-treated or irradiated silicon," *Journal of Physics C: Solid State Physics*, vol. 26, p. 5069-5082, 1985.

[59] N. S. Minaev and A. V. Mudryi, *Phys. Status Solidi a*, vol. 68, p. 561, 1981.

[60] G. Davies, E. C. Lightowlers, R. C. Newman, and A. S. Oates, "A model for radiation damage effects in carbon-doped crystalline silicon," *Semiconductor Science and Technology*, vol. 8, p. 524-532, 1987.

[61] S. Schaefer and R. Ludemann, "Low damage reactive ion etching for photovoltaic applications," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 17, p. 749-754, 1999.

[62] E. Yablonovitch and G. D. Cody, *IEEE Transactions on Electron Devices*, vol. 29, p. 300-305, 1982.

[63] S. R. Wenham, P. Campbell, S. Bowden, and M. A. Green, "Improved optical design for photovoltaic cells and modules," 22nd IEEE Photovoltaic Specialists Conference, p. 105-110, 1991.

[64] R. A. Sinton and R. M. Swanson, *IEEE Electronic Device Lett.*, p. 547-549, 1987.

[65] L. A. Brickman, "A unified thick / thin-film optical model for silicon solar cells and model for silicon solar cells and modules," 7th European Photovoltaic Solar Energy Conference, p. 1050-1054, 1988.

[66] M. Born and E. Wolf, *Principles of Optics*, 7th ed. New York: Cambridge University Press, 1999.

[67] P. R. Campbell, "Light Trapping and Reflection Control in Silicon Solar Cells," PhD thesis: University of NSW, 1989

[68] H. W. Deckman, C. R. Wronski, H. Witzke, and E. Yablonovitch, "Optically Enhanced Amophous Silicon Solar Cells," *Applied Physics Letters*, vol. 42, p. 968-970, 1983.

[69] J. Zhao and M. A. Green, "Optimized Antireflection Coatings for High Efficiency Silicon Solar Cells," *IEEE Transactions on Electron Devices*, vol. 38, p. 1925-1934, 1991.

[70] H. A. Miska, "The use of Leached Gradient Index Antireflection Surfaces on
      Borosilicate Glass Solar Collector Cover Tubes," *Solar Energy Materials*, vol. 11, p.
      231-238, 1984.

[71] A. Scheydecker, A. Goetzberger, and V. Wittwer, "Reduction of Reflection Losses
      by Structured Surfaces," 10th European Communities Photovoltaic Solar Energy
      Conference, Lisban, Portugal, p. 39-42, 1991.

[72] E. Y. Wang, "Optimum design of antireflection Coatings for Siliocon Solar Cells,"
      12th IEEE photovoltaic Specialists Conference., Palo Alto, p. 168, 1973.

[73] B. Sopori, J. Madjdpour, Y. Zhang, and W. Chen, "PV Optics: An Optical Modeling
      Tool for Solar Cell and Module Design," Electrochemical Society, International
      Symposium, Seattle, Washington, p. 138-144, 1999.

[74] A. A. Istratov, H. Hieslmair, and E. R. Weber, "Iron contamination in silicon
      technology," *Applied Physics a-Materials Science & Processing*, vol. 70, p. 489-
      534, 2000.

[75] W. Kern, "The evalution of silicon wafer cleaning technology," *J.Electrochem. Soc*,
      vol. 137, p. 1887, 1990.

[76] R. Gereth, H. Fischer, E. Link, S. Matters, and W. Pschunder, "Contribution to the
      solar cell technology," *Energy Conversion*, vol. 12, p. 103-107, 1972.

[77] M. Y. Ghannam, S. Sivoththaman, H. E. Elgamel, J. Nijs, M. Rodot, and D. Sarti,
      "636 mV open circuit voltage multicrystalline silicon solar cells on Polix material:
      trade-off between short circuit current and open circuit voltage," 25rd IEEE
      Photovoltaic Specialists Conference, p. 106-110, 1993.