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***Abstract*—DC shipboard power systems have been considered as a promising solution for stricter environmental regulations on ships due to their main benefits in fuel savings with variable speed engines and easy integration of energy storage systems. In order to employ the DC solution in the shipboard power systems, the DC power systems have to be protected from a system fault with protection selectivity to minimise impacts of the fault or to avoid other undesirable situations in the system. For low-voltage DC shipboard power systems, a three-level protection has been proposed: fast action (1st) - bus separation by solid-state DC bus-tie switch, medium action (2nd) - feeder protection by high-speed fuse and slow action (3rd) - generator-rectifier fault controls. This paper proposes a new method by means of additional bus capacitance added in main DC buses to help the reliable operation of the three-level protection. The principle of the proposed method is introduced and the sizing of the additional bus capacitance is addressed in this paper. With the modelling of the DC shipboard power systems, the analyses of voltage drops for the bus separation failure and fault clearing time for the feeder protection are carried out to verify the proposed method. The results show that the proposed method not only mitigates the voltage drop for the bus separation failure, but also achieves the selectivity and the sensitivity for the feeder protection.**

***Index Terms*—Additional Bus Capacitance, DC Micro Grid, Protection Coordination, Selectivity, Sensitivity, Shipboard Power System, Three-level Protection.**

I. Introduction

SINCE 2013, greenhouse gas emissions from the maritime transport and shipping sector have been controlled by mandatory energy efficiency regulations, e.g., energy efficiency design index (EEDI) and/or ship energy efficiency management plan (SEEMP) [2], [3]. According to [2], [3], by 2025, all new ships have to be designed to have $30\,\%$ less carbon dioxide emissions than those built in 2004. One of the most promising solutions to comply with these regulations is the DC shipboard power system (SPS) with its advantages in the marine domain [3]–[6]:

- fuel savings with variable-speed engines
- easy integration of energy storage systems
- weight reduction in electrical installation
- optimisation of running engines by closed-bus operation

With these benefits, various DC solutions have been introduced for low- and medium-voltage DC SPSs [4], [6]–[9]. Moreover, low-voltage DC solutions with power levels up to $20\,\mathrm{MW}$ and DC voltage levels of around $1\,\mathrm{kV}$ have been employed for dynamic positioning vessels, e.g., shuttle tankers and platform supply vessels, and their schematic diagrams are shown in Fig. 1 [10]. For high-power navy ships, medium-voltage DC SPSs have been investigated in [9], [11]–[15] and their power systems are based on the ring bus configuration which provides better reconfigurability and greater survivability compared to the radial configuration mainly used for commercial ships.

These new power systems come with technical challenges in protection coordination. The main bottleneck of the protection coordination in the DC SPS is originated from the low thermal capability of power converters based on semiconductors, e.g., diodes, thyristors and IGBTs [16]. While conventional AC equipment like generators, transformers, switchgears and cables can sustain the maximum fault current for several seconds (e.g., transformer: $2\,\mathrm{s}$ [17]), faults in the DC networks have to be cleared within several milliseconds or a few tens of milliseconds to avoid converter failures [18]–[20]. This implies that the DC protection process, consisting of fault detection, fault localisation, fault isolation and backup protection, has to be completed within such a short period of time.

There are several protection methods for the SPSs, already presented in the literature. Firstly, the unit-based protection for the ring-configured DC SPS is based on power converters interfaced with electric sources [21]–[26]. The port and the starboard in the ring configuration are separated during normal operation. When a fault occurs in one bus, the fault current is controlled by the converters and the DC ship network is reconfigured by disconnectors to isolate the fault and re-energise the healthy part of the system. In this approach, complex communication is required [14] and the system restoration is relatively slow due to the use of the mechanical disconnector. On the other hand, the breaker-based protection for the ring-configured DC SPS enables the closed-bus operation and the fault isolation with the minimum power outage because the solid-state breaker in the DC SPS can disconnect the fault with ultra-fast speed [11], [13], [27]. In the breaker-based protection the costly DC circuit breaker and the communication are necessary.

For radial-configured medium-voltage DC SPSs, differential and directional protections combined with an intelligent elec-

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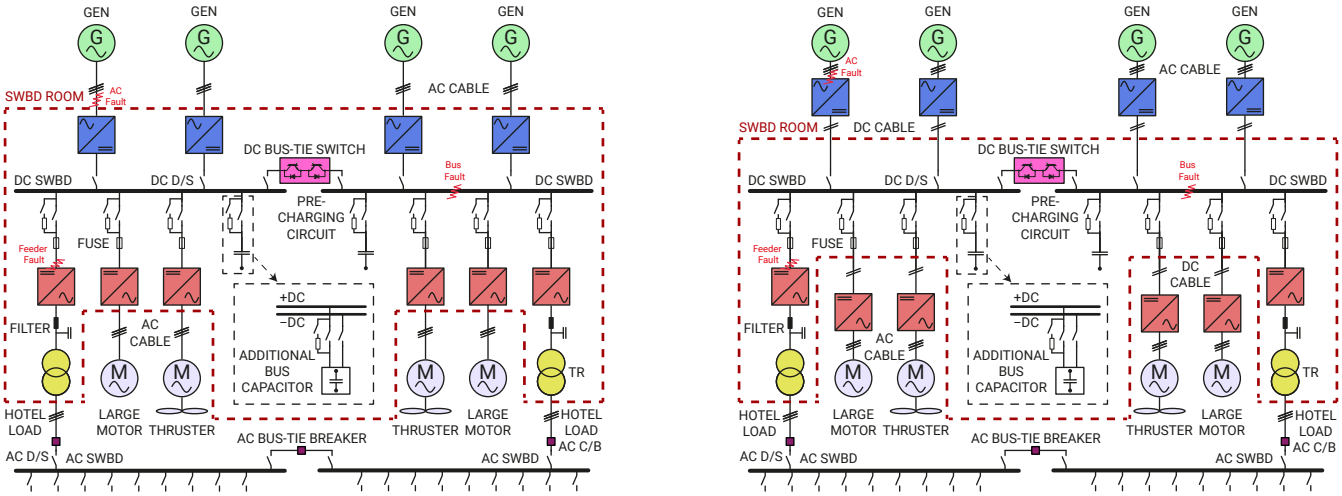


(a) (b)

Fig. 1: Schematic diagrams of low-voltage DC SPS: (a) centralised architecture and (b) distributed architecture. The proposed additional bus capacitor (ABC) is installed between the positive and negative poles of the DC buses.

tronic device (IED) and a solid-state DC circuit breaker have been investigated in [28]–[30]. In these protections, the IED plays an important role to detect the fault current and find the fault location by analysing the difference in current and/or the direction of current with the communication between adjacent IEDs. After the fault localisation, the solid-state DC circuit breaker disconnects the fault with the minimum system disconnection. For the implementation of these protections a combination of the solid-state DC circuit breaker and the IED is necessary in every feeder.

A three-level protection has been proposed in [4], [6], [7] as an economic solution for the low-voltage DC SPSs. The three-level protection consists of three different fault controls (Fig. 2): fast action (the 1st level) - bus separation with DC bus-tie switch based on solid-state technology ($10-40\,\mu$s), medium action (the 2nd level) - feeder protection with high-speed fuse ($0.2-1$ ms) and slow action (the 3rd level) - generator-rectifier fault control ($0.003-10$ s). For the generator-rectifier fault control, several methods have been proposed depending on rectifier type, e.g., an excitation removal for a diode rectifier [7], a fold-back fault control for a thyristor rectifier [31] and an artificial short-circuit method for an active rectifier [19]. When the feeder fault shown in Fig. 1 occurs, the DC bus-tie switch rapidly disconnects the DC buses. Then the high-speed

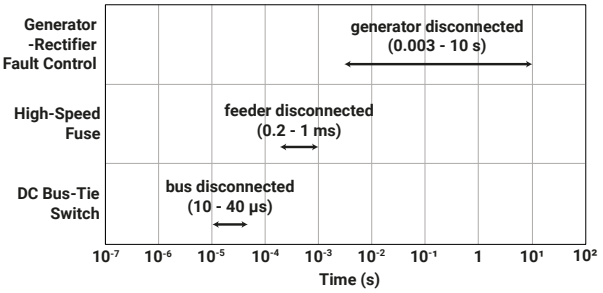


Fig. 2: Operating time frames of three-level protection for low-voltage DC SPS. Time discrimination in the three-level protection is coordinated with their different operating times and the time margins between the level protections.

fuse on the faulty feeder isolates the fault from the system. As the last level, the generator-rectifier fault control eliminates the fault contribution of the generator for the feeder protection failure or the DC bus fault (Fig. 1). For the AC fault shown in Fig. 1 the conventional generator protection is operated.

The three-level protection does not utilize communication and uses the economic fuse solution for the feeder protection instead of the solid-sate DC circuit breaker. Therefore, it can be stated that the three-level protection is simple and cost effective. Such benefits motivate to employ the DC solution in SPSs in commercial vessels [10]. However, apart from the notable disadvantages of the fuse (manual replacement and less reliable operation), the fuse-based feeder protection presents the following main drawbacks: 1) difficulty in management of the bus separation failure (the 1st level protection failure) and 2) difficulty in selectivity and sensitivity of the feeder protection. Firstly, when the DC bus-tie switch fails to disconnect the healthy bus from the feeder fault at other bus (the bus separation failure), the fuse on the faulty feeder has to clear the fault before the undervoltage trip of the loads at the healthy bus, to avoid undesired healthy-side load disconnection. Moreover, the fuse on the faulty feeder has to clear the fault not only without the operation of the fuses on other healthy feeders, but also under the maximum and minimum loading conditions [6].

While in [6], [7] converters having high value of the DC link capacitor are proposed to achieve the selectivity and the sensitivity for the feeder protection, due to different ship operation modes and fault locations, there are configurations that do not have sufficient amount of energy to blow the fuse. Hence, this paper proposes a new method employing additional bus capacitor (ABC) in Fig. 1 as a solution for the issues on the feeder protection. Moreover, the proposed method can support the management of the bus separation failure by mitigating the voltage drop at the healthy side.

This paper is divided in five sections. In section II, the modelling of the two architectural DC SPSs with system parameters and ship operation modes used in this study are

described. The principle of the ABC method is addressed and the ABC sizing is introduced in section III. Section IV deals with the performance of the ABC method with the comprehensive analyses: the voltage drops at the healthy bus for the bus separation failure and the selectivity/sensitivity for the feeder protection. The last section (section V) summaries the findings and the main results.

II. DC SPS Modelling

As shown in Fig. 1, two system architectures are considered for the low-voltage DC SPS: centralised architecture (or a multidrive approach in [4], [32]) and distributed architectures (or a fully distributed system in [4], [32]). The main difference comes from ways to connect different equipment, e.g., generator-rectifier, rectifier-DC bus, DC bus-inverter and inverter-load. The centralised architecture uses AC cables to connect generator-rectifier and inverter-load. All DC parts, e.g., rectifiers, inverters, isolators and bus-tie switches, are connected to the DC bus through metallic busbars in the cabinet, as illustrated in Fig. 1a. On the other hand, the DC cables are mainly used to integrate the converters in the DC bus in the distributed architecture. The distributed architecture allows for installing power converters next to machines and can achieve high energy efficiency by using the DC cables which have lower power losses than AC cables (Fig. 1b).

If a high-impedance DC short-circuit fault occurs, it may draw low current and develop low voltage drop, as shown in Fig. 3b. Such a fault gives insignificant system impact and can be removed by the fuse with delayed operation or managed by ship monitoring and supervision systems. On the other hand, a low-impedance DC short-circuit fault causes high voltage drop and huge fault currents (significant system impact), as shown in Fig. 3c. Therefore, the low-impedance fault has to be cleared as quickly as possible and its management is a challenging issue. For this reason, the low-impedance DC fault (e.g., $R_F = 1\,\mathrm{m}\Omega$ in Table I) is considered in this study.

Due to fast discharging characteristics of capacitors, an initial transient current during a DC fault (DC pole-to-pole fault) is mainly contributed by DC link capacitors which are applied to the power converters [33]–[36]. In particular, in the $1\,\mathrm{ms}$ time range of the 1^{st} and 2^{nd} level protections (the bus separation and feeder protections), the fault current contribution of the AC generator is much lower than that of the DC capacitors (shown in Fig. 3c) and can be neglected for such a time range. By neglecting the fault current contribution of the AC generator, the centralised architecture DC SPS without the ABC (T1) for the DC short-circuit fault can be modelled as R-L-C circuits connected via busbar inductance, as depicted in Fig. 4a [7]. In case of the distributed architecture DC SPS without the ABC (T3), the series resistance and inductance of the DC cable play an important role in initial fault current amplitude and its rate of change. Therefore, an equivalent circuit in Fig. 4c including the parameters of the DC cable is used. The capacitance of the DC cable is neglected because its capacitance value is much smaller than that of the DC link capacitor.

The equivalent circuits for both the architectural DC SPSs with the ABC are shown in Fig. 4b (T2) and 4d (T4),

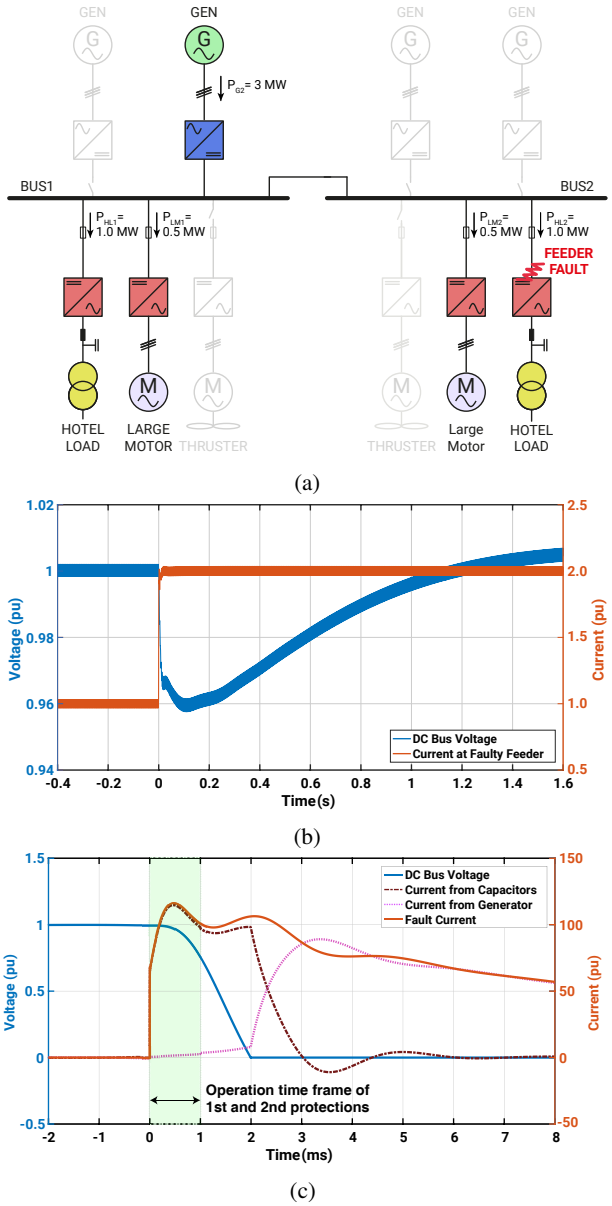


Fig. 3: DC short-circuit faults: (a) ship configuration and power flow before the fault under operation mode 3 (OM3) in Table II, (b) high-impedance fault ($R_F = 1\,\Omega$) and (c) low-impedance fault ($R_F = 1\,\mathrm{m}\Omega$). $1\,\mathrm{kV} = 1.0\,\mathrm{pu}$ and $1\,\mathrm{kA} = 1.0\,\mathrm{pu}$ are used.

respectively (Note that T2 and T4 are the main elements of the study.). ESR and ESL in Fig. 4 are the equivalent series resistance and inductance of the capacitor, respectively. The four equivalent circuits in Fig. 4 are implemented by use of EMTP-RV. Note that the DC SPSs considered are classified in the four categories: T1, T2, T3 and T4.

The system parameters used in the study are provided in Table I, where I^2t_{pf1} and I^2t_{tf1} are the pre-arcing and total clearing I^2t ratings of fuse 1 selected for the protection of the LM and TM feeders in the distributed architecture DC SPSs (T3 and T4). I^2t_{pf2} and I^2t_{tf2} are those of fuse 2 selected for the protection of the LM and TM feeders in the centralised architecture DC SPSs (T1 and T2). The fault resistance R_F

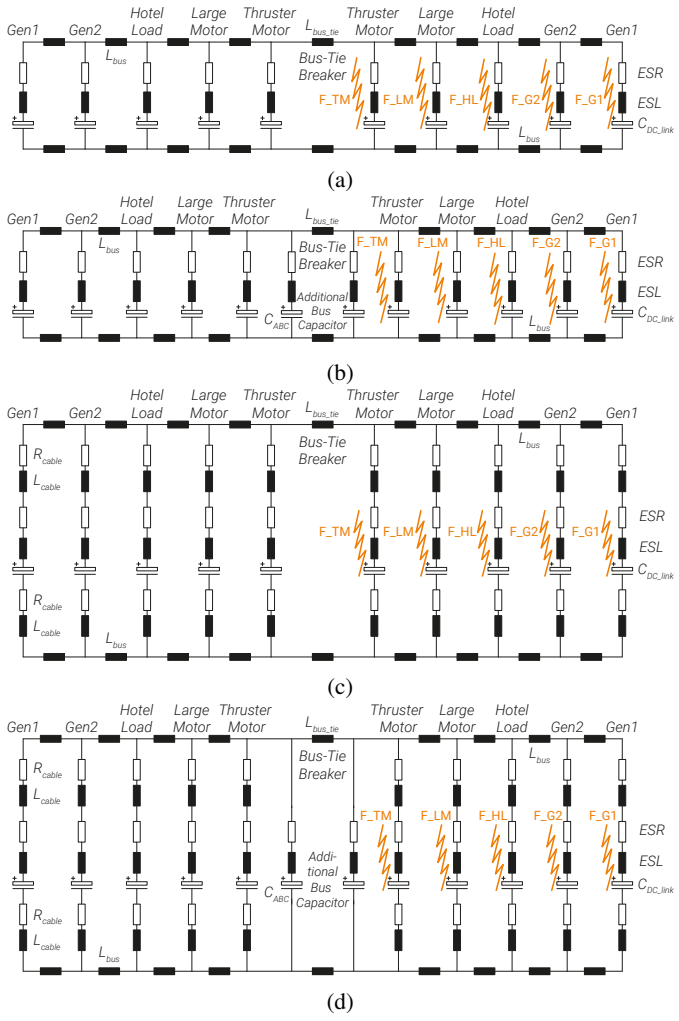


Fig. 4: Equivalent circuits for DC SPSs: (a) centralised architecture without ABC (T1), (b) centralised architecture with ABC (T2), (c) distributed architecture without ABC (T3) and (d) distributed architecture with ABC (T4).

and the DC cable length l_{cable} are assumed to be $1\,\mathrm{m}\Omega$ and $25\,\mathrm{m}$, respectively. The ABC value (C_{ABC}) is discussed and determined in section III.

A shuttle tanker, which is designed for oil transport from an off-shore oil field and is one of the representative dynamic positioning vessels, is considered for the study. Three considered operation modes of the shuttle tanker are presented in Table II with electric load matrix. A dynamic positioning mode (OM1, the maximum loading condition) is turned on when the shuttle tanker should be manoeuvred accurately. In OM1, the maximum number of generators and several high power motors with hotel loads have to be operated, e.g., thruster motors for the dynamic positioning, cargo pumps for the crude oil transfer, ballast pumps for the ship balance and volatile organic compound (VOC) compressors for the return of VOC emission gases. During a port in/out mode (OM2, the medium loading condition), thruster motors with hotel loads are in service to improve the manoeuvrability when the shuttle tanker approaches and leaves a port. For a sailing mode (OM3, the minimum loading condition), the mechanical power from main

TABLE I
SYSTEM PARAMETERS USED FOR THE STUDY

V_{DC}	$1kV$	C_{G1}, C_{G2}	$80mF$
L_{bus} [a]	$1\mu H$	C_{HL}	$20mF$
L_{bus_tie}	$1\mu H$	C_{LM}, C_{TM}	$60mF$
R_{cable} [b]	$60.7m\Omega/km$	R_F	$1m\Omega$
L_{cable} [b]	$0.284mH/km$	ESR [c]	$58m\Omega$
l_{cable}	$25m$	ESL [c]	$20nH$
I^2t_{pf1} [d]	$1.1 \cdot 10^6 A^2s$	I^2t_{tf1} [d]	$5.4 \cdot 10^6 A^2s$
I^2t_{pf2} [e]	$1.7 \cdot 10^6 A^2s$	I^2t_{tf2} [e]	$8.5 \cdot 10^6 A^2s$

[a] Data for a metallic busbar with $1\,\mu\mathrm{H/m}$ [37] and $1\,\mathrm{m}$ length
[b] Data for a single core cable with $1\,\mathrm{kV}$ and $631\,\mathrm{A}$ [38]. Several cables in parallel are used depending on current rating.
[c] Data for two capacitors with $0.5\,\mathrm{kV}$ and $10\,\mathrm{mF}$ [39] in series (capacitance with $1\,\mathrm{kV}$ and $5\,\mathrm{mF}$). Several capacitors in parallel are used depending on capacitor rating.
[d] Data for four fuses (170M1833 in [40]) in parallel
[e] Data for five fuses (170M1833 in [40]) in parallel

TABLE II
ELECTRIC LOAD MATRIX OF SHIP OPERATING MODE

Electric Load		Operation Mode		
		OM1	*OM2*	*OM3*
Bus1	Gen1 (G1)	✓ [a]		
	Gen2 (G2)	✓	✓	✓
	Hotel Load (HL)	✓	✓	✓
	Large Motor (LM) [b]	✓		✓
	Thruster Motor (TM)	✓	✓	
Bus2	Thruster Motor (TM)	✓	✓	
	Large Motor (LM) [b]	✓		✓
	Hotel Load (HL)	✓	✓	✓
	Gen2 (G2)	✓	✓	
	Gen1 (G1)	✓		

[a] In service.
[b] Carge pumps, ballast pumps and VOC compressors are grouped in a large motor.

engines is used for the propulsion and small number of large motors (like ballast pumps) with hotel loads are in service.

III. PROPOSED ABC METHOD

This section discusses technical issues in the bus separation failure and the feeder protection. As a solution for the issues, the ABC method is introduced and its operational principles are presented. In addition, the sizing of the ABC method is carried out for the centralised and distributed architectures considering iterative process addressed in this paper.

A. Voltage Drops for Bus Separation Failure

When the feeder fault occurs, the fault current reaches the threshold value of the DC bus-tie switch operation, which is based on solid-state technology to achieve ultra-fast disconnection. The switch rapidly interrupts the fault current within several tens of microseconds [6], [7]. But, if the switch fails to interrupt, all loads in the healthy bus suffer a huge voltage drop and may be disconnected due to their own undervoltage protection. Thus, the minimum remaining voltage at the healthy

bus has to be higher than any undervoltage trip conditions of the converters during the fault clearing time of the feeder protection (1 ms) in the three-level protection. With a simple equivalent circuit depicted in Fig. 5, a sensitivity analysis on the voltage drop is carried out not only to investigate the role of the system inductance and capacitance, but also to understand a benefit of the ABC method.

As aforementioned, an initial current of the DC fault is mainly contributed by the capacitors which have much faster response than the AC generators. Therefore, an equivalent circuit of the DC fault in the initial phase of the fault can be simplified as a series R-L-C circuit, as illustrated in Fig. 5. The analytical expression for the DC fault circuit (Fig. 5) with the underdamped condition is [41]:

$$i_f(t) = \underbrace{Ae^{-\alpha t}\sin\omega_d t}_{1^{\text{st}}\text{ term}} + \underbrace{Be^{-\alpha t}\sin(\omega_d t+\beta)}_{2^{\text{nd}}\text{ term}} \quad (1)$$

where $\alpha = R_{eq}/L_{eq}$, $\omega_0 = 1/\sqrt{L_{eq}C_{eq}}$, $\omega_d = \sqrt{\omega_0^2-\alpha^2}$, $\beta = \arctan(\omega_d/\alpha)$, $A = \omega_d V_{DC0}/L_{eq}$ and $B = \omega_0 i_{DC0}/\omega_d$.

With the assumption of $i_{DC0} = 0$ (the 1st term is strongly dominant in current amplitude.) and $V_{DC0} = 1kV$ (the rated DC voltage) in (1), the remaining voltage of the capacitor can be calculated by (2) in pu.

$$\frac{\Delta V}{V_{DC0}} = e^{-\alpha t}\cos\omega_d t \quad (2)$$

Fig. 6 shows the sensitivity analysis in the remaining voltage of the DC capacitor depending on the values of the capacitor and the inductor by using (2). Note that $R_{eq} = 1m\Omega$ (the equivalent resistance, e.g., line resistance, fault resistance and parasitic resistance) and $t = 1ms$ (the fault clearing time of the feeder protection) are used for the voltage drop analysis.

It is seen that the voltage drop can be mitigated with several tens of microhenries of inductance. In addition, capacitance with several tens of millifarads can also reduce the voltage drop. Therefore, there are two ways to control the voltage drop level: 1) installing additional inductance between the healthy bus and the faulty bus and 2) installing the additional capacitance between the healthy bus and the faulty bus (the proposed ABC method).

From the point of view of the system stability, while high system inductance might cause instability issue depending on the system condition and the converter type, high system capacitance supports the system stability [42]. Therefore, for the bus separation failure, the ABC method is a suitable

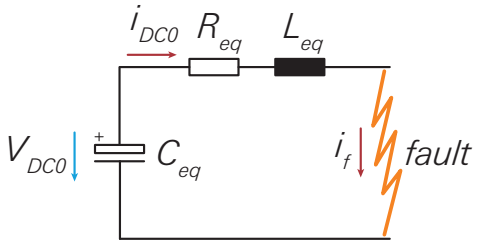


Fig. 5: Equivalent circuit for initial DC fault. The voltage of the DC capacitor V_{DC0} and the current i_{DC0} are the initial conditions for the DC fault current i_f.

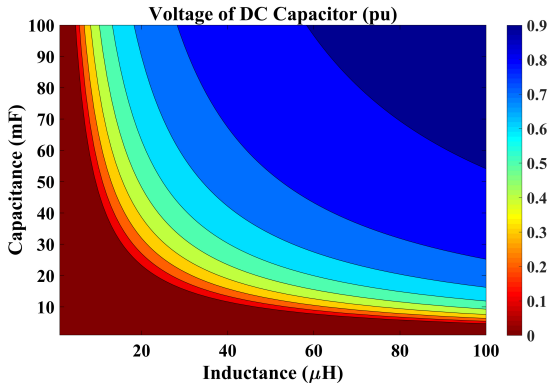


Fig. 6: Sensitivity analysis in remaining voltage of DC capacitor. High remaining voltage of the DC capacitor implies its low voltage drop.

solution to mitigate the impact on the voltage drop at the healthy bus and to make the system more stable, compared to adding more inductance.

B. Selectivity and Sensitivity for Feeder Protection

Unlike the AC-based SPSs, in the DC SPSs, each feeder has a DC link capacitor and it rapidly provides fault energy to other feeder faults passing through its own fuse and the fuse on the faulty feeder. Thus, the operation time between the fuse on the faulty feeder and the fuse on the healthy feeder has to be coordinated to achieve the maximum continuity of service with the minimum system disconnection. The term 'selectivity' is used to describe this fuse coordination between adjacent feeders in this paper. Note that the selectivity concept in this paper is different with that of the AC power system, where it is widely intended as "the process to select the protective relays to operate the relays as fast as possible within their primary zone, but to have delayed operation in their backup zone" [43].

As aforementioned, in the DC SPS, the system capacitance installed in every converter is the main energy source to blow the fuse for the feeder protection and its value is related to the fault clearing time. Usually, higher capacitance allows for faster fault clearing. The fuse on the faulty feeder is melted by the energy provided by the external capacitance installed at other feeders. In order to achieve the selectivity, the fuse on the faulted feeder has to clear the fault without the pre-arcing

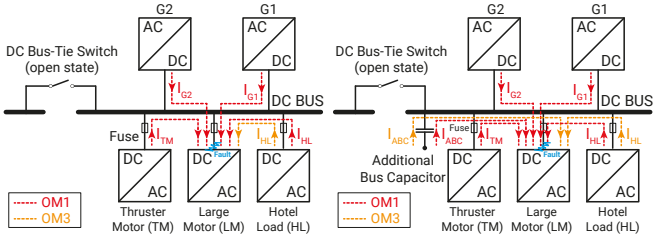


Fig. 7: Fault current flows depending on ship operation mode: (a) without the ABC and (b) with the ABC. The two ship operation modes described in Table II are represented: OM1 (red-dotted line) and OM3 (orange-dotted line).

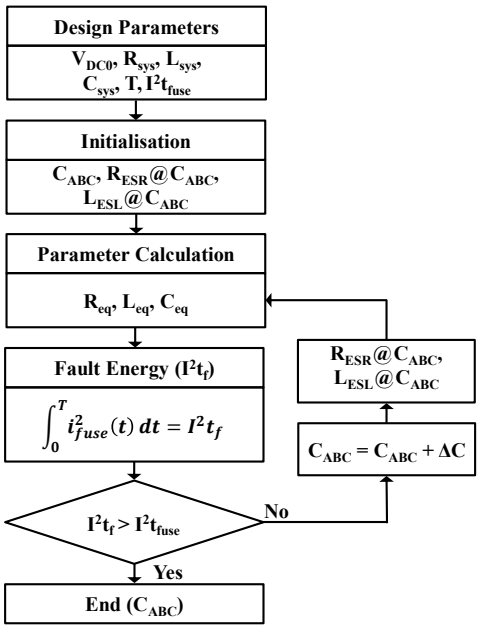


Fig. 8: Flowchart representing iterative process for sizing of ABC value.

of the fuses on other feeders. For example, the fuse on the LM feeder in Fig. 7a (the faulty feeder) has to totally clear the fault without the pre-arcing of other fuses (the fuses on the thruster motor and the hotel load) [44].

On the other hand, the fuse on the faulty feeder has to clear the faults under the maximum fault condition as well as the minimum fault condition, something termed 'sensitivity' in this paper. For example, the fuse on the LM feeder in Fig. 7a (the faulty feeder) has to be blown by the fault currents ($I_{G1} + I_{G2} + I_{TM} + I_{HL}$) under OM1 (the maximum loading condition) and by the fault current (I_{HL}) under OM3 (the minimum loading condition).

The feeder protection with the high-speed fuse has to comply with these technical aspects, the selectivity and the sensitivity. For the DC SPSs and the system conditions considered in this study, the selectivity between the fuse on the LM feeder (faulty feeder) and the fuse on the TM feeder (healthy feeder and having the same fuse and current ratings with the LM feeder as given in Table I) in Fig. 7a cannot be guaranteed without the selectivity analysis. Furthermore, the sensitivity under OM1 and OM3 may not be achieved for the LM feeder fault since the fault energy from the capacitor at the HL may be insufficient to blow the fuse on the LM feeder.

In order to achieve the selectivity and the sensitivity for the feeder protection, the ABC method is proposed as illustrated in Fig. 7b. The ABC method directly contributes the additional fault current (I_{ABC}) to the fuse on the faulty feeder under OM1 and OM3. This additional fault energy can significantly assist in melting the fuse with shorter time than the case without the ABC. With this principle, the proposed method ensures both the selectivity and the sensitivity, if the DC SPSs have the ABC with high enough energy to blow the fuse.

C. Sizing of ABC

As mentioned above, the voltage drop of the DC bus, which is related to the bus separation failure, is the function of the system capacitance and inductance values. In detail, the system inductance has more impacts than the system capacitance in this matter. The system capacitance, by contrast, is the dominant factor to determine the fault clearing time for the feeder protection. Hence, the sizing of the ABC is based on the consideration of the feeder protection and the selection process addressed is shown in Fig. 8.

In order to control the fault clearing time with the ABC method, the fault energy to the faulty feeder is calculated with:

$$\int_0^T i_{fuse}^2(t)dt = I^2t_f > \text{Total clearing } I^2t \text{ of fuse} \qquad (3)$$

where i_{fuse} is the fault current passing through the fuse.

Using (1), (3) can be expressed in:

$$I^2t_f = \left[e^{-2\alpha t}\left(\frac{A}{2}\right)^2\left(\frac{\alpha\cos 2\omega_d t - \omega_d \sin 2\omega_d t}{\alpha^2+\omega_d^2} - \frac{1}{\alpha}\right)\right]_0^T \qquad (4)$$

In (4), the expansion of the equation in a variable C_{eq} is impossible since (4) is an implicit equation. Therefore, an iterative method is used to find the value for the ABC which can clear the fault within the desired time according to the process in Fig. 8. Firstly, the design parameters are needed to start the calculation like initial DC voltage V_{DC0}, system resistance R_{sys}, system inductance L_{sys}, system capacitance C_{sys}, target fault clearing time T and total clearing I^2t rating of fuse I^2t_{fuse}. In the initialisation step, equivalent series resistance (R_{ESR}) and inductance (L_{ESL}) are calculated at the base of an initial capacitor value for the ABC method. Higher values of the ABC make lower values of R_{ESR} and L_{ESL} due to the capacitor connection in parallel. With these parameters, the equivalent values (R_{eq}, L_{eq} and C_{eq}) are calculated to determine the integrated fault energy I^2t_f during T by (4). If the fault energy is less than I^2t_{fuse}, the higher ABC value should be considered than that of the previous iteration step

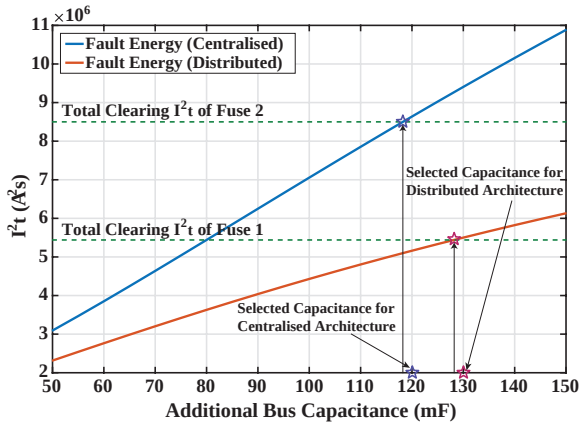


Fig. 9: Result of ABC sizing for centralised and distributed architectures.

and the parameters for the capacitor should be calculated at the base of the updated ABC value. When I^2t_f is greater than I^2t_{fuse}, the process for the ABC sizing is completed with the result of the minimum required ABC value.

With $T = 1ms$ (the operation time of the feeder protection) and the system parameters in Table I and under OM3 in Table II (the worst case, considered to ensure the sensitivity), the required ABC values are determined by the process and the results are shown in Fig. 9. The ABC values with $120\,\mathrm{mF}$ and $130\,\mathrm{mF}$, which are slightly higher than the minimum required values, are finally selected to enable the capacitor combination for centralized and distributed architectures, respectively. Note that due to the presence of the DC cables in the distributed architecture the different fuses are used. Fuse 2 for the centralised architecture and fuse 1 for the centralised architecture are used, as shown in Table I.

IV. Verification

With the system modelling of the DC SPSs in Fig. 4 by EMTP-RV, the voltage drops are calculated under all the fault conditions in Table I and all the ship operation modes in Table II for the bus separation failure. Furthermore, the fault clearing times are analysed under the maximum and minimum loading conditions for the feeder protection. From these analyses, the effectiveness of the proposed method is investigated.

A. Bus Separation Failure

The voltage drop analyses under the operation modes in Table II and the fault locations in Fig. 4 are carried out for the four DC SPSs in Fig. 4 and the results are shown in Fig. 10. It is observed that, due to absence of the DC cable, the centralised architectures (T1 and T2) have higher voltage drops than the distributed architectures (T3 and T3) for all the operation modes and the fault locations. When the ABC method is employed with $120\,\mathrm{mF}$ for T2 and $130\,\mathrm{mF}$ for T4, the voltage drops for T2 and T4 are clearly reduced, compared to those of T1 and T3.

While high amount of the system capacitance is presented in the system, certain value of the system inductance is also necessary to control the voltage drop level at the healthy side, as shown in Fig. 6. Among the various study cases in Fig. 10a, the fault at the thruster motor feeder (F_TM) under OM2 is chosen to conduct the worst case study in terms of the voltage drop. The result shows that in order to keep the voltage of $0.8\,\mathrm{pu}$ at $1\,\mathrm{ms}$ after the fault, the system inductance values of $30\,\mu\mathrm{H}$ and $20\,\mu\mathrm{H}$ are needed for T1 and T3, respectively. By installing the ABC, the required inductance values can be minimised as $20\,\mu\mathrm{H}$ for T2 and $3\,\mu\mathrm{H}$ for T4 as shown in Fig. 10b. Note that the voltage level of $0.8\,\mathrm{pu}$ is chosen for the undervoltage trip condition of converters and the time of $1\,\mathrm{ms}$ is chosen with the consideration of the feeder protection time.

The results under the studied condition are summarised:

- The distributed architecture has an advantage considering lower voltage drops.
- The ABC method helps to mitigate the voltage drop for both the architectures (benefit for the bus separation failure).

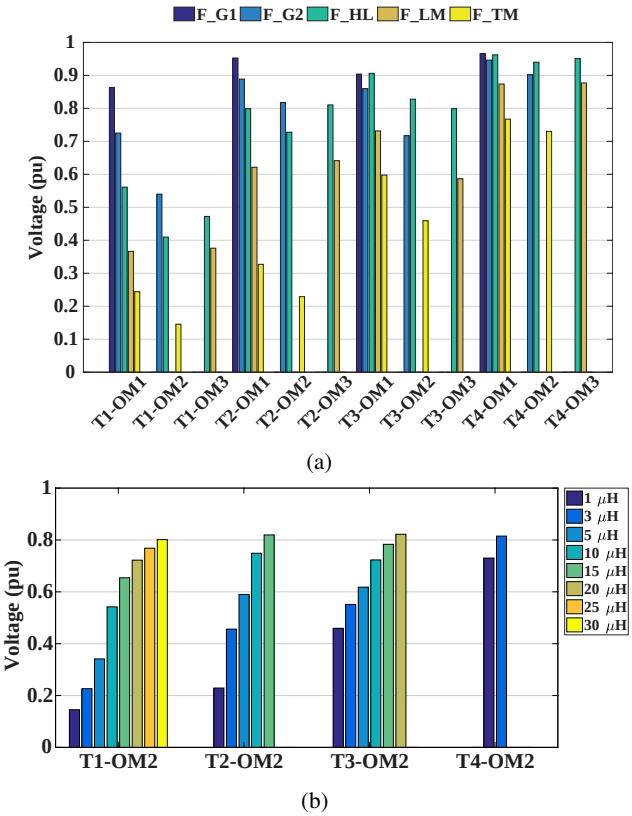


Fig. 10: Analysis of voltage drop for bus separation failure: (a) remaining voltage of healthy bus at $1\,\mathrm{ms}$ after fault depending on ship architecture, ship operation mode and fault location and (b) required inductance value to keep remaining healthy bus voltage with $0.8\,\mathrm{pu}$.

- The ABC method can reduce the required system inductance value for both the architectures (benefit for the system stability [42]).

B. Feeder Protection

After the bus separation (the operation of the 1st level protection), the capacitors connected to the bus, which includes the faulty feeder, have to provide enough fault energy to blow the fuse corresponding to the faulty feeder, as shown in Fig. 7. As aforementioned, with this capacitor discharging energy, the fuse on the faulty feeder has to clear the fault not only without the operation of the fuses on other healthy feeders (the selectivity), but also under the maximum and minimum loading conditions (the sensitivity). Therefore, the selectivity and sensitivity analyses are conducted under OM1 and OM3 for T1, T2, T3 and T4. The transient voltage and current waveforms are shown in Fig. 11g, 11h, 11i and 11j and the time-current curves in Fig. 11a and 11b are their RMS currents. Note that the characteristics of the pre-arcing and total clearing I^2t ratings of fuse 1 and 2 (black dotted-lines) in Fig. 11a and 11b are drawn by the values given in Table I.

For T1 in Fig. 11a, it is observed that the current ($I_{TM} - T1 - OM1$) passing through the fuse on the TM feeder starts to melt the fuse (pre-arcing) at $448\,\mu\mathrm{s}$ before the total clearing of the fuse on the LM feeder (the total clearing time: $554\,\mu\mathrm{s}$).

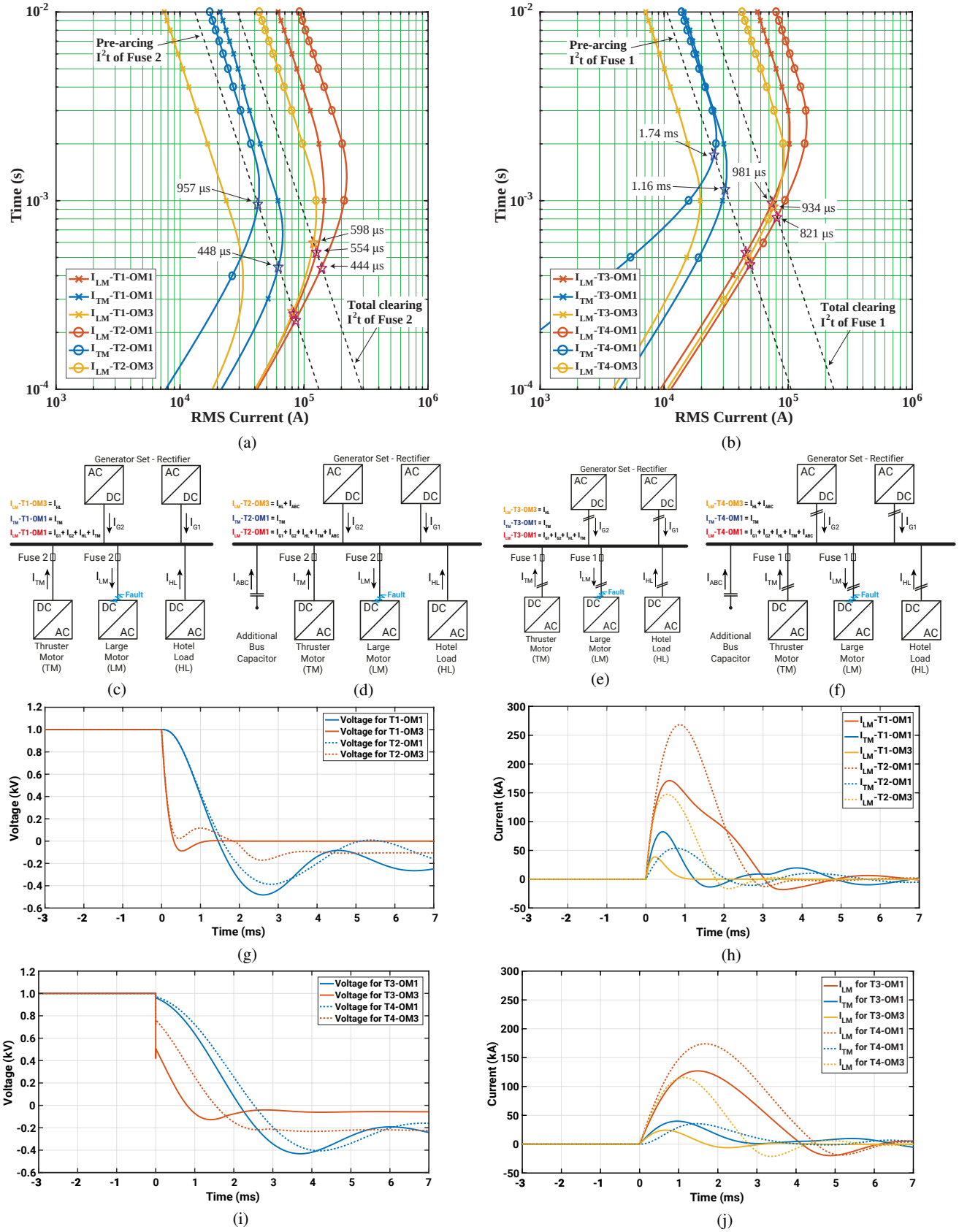


Fig. 11: Selectivity and sensitivity analyses for DC SPSs: (a) time-current curve for T1 and T2 , (b) time-current curve for T3 and T4, (c) fault current flow for T1, (d) fault current flow for T2, (e) fault current flow for T3, (f) fault current flow for T4, (g) voltage waveform for T1 and T2, (h) current waveform for T1 and T2, (i) voltage waveform for T3 and T4 and (j) current waveform for T3 and T4.

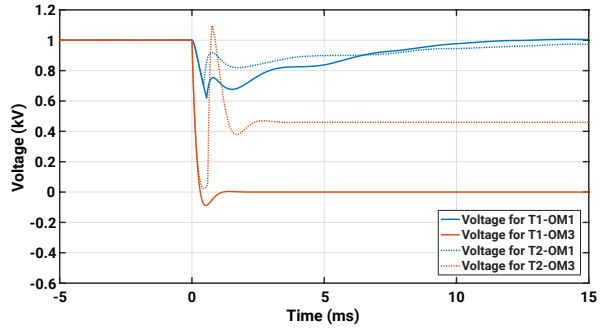
It means that the selectivity between the LM and TM feeders is not achieved for the fault at the LM feeder under OM1. Moreover, the sensitivity under OM1 and OM3 is not available for the fault at the LM feeder since the current ($I_{LM}-T1-OM3$) is not enough to blow the fuse 2.

When the ABC method is employed in the centralised architecture as the configuration of T2 in Fig. 11a, the fault at the LM feeder can be cleared at $444\,\mu$s under OM1 by the current ($I_{LM}-T2-OM1$) and at $598\,\mu$s under OM3 by the current ($I_{LM}-T2-OM3$). This implies that the sensitivity is available with the ABC method. Otherwise, the pre-arcing of the fuse on the TM feeder is delayed about $500\,\mu$s (from $448\,\mu$s to $957\,\mu$s). This delayed pre-arcing time provides an enough margin to implement the selectivity between the LM and TM feeders.

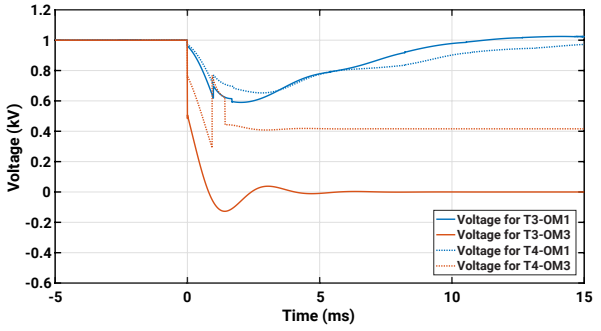
In Fig. 11b, the total clearing time by the current ($I_{LM}-T3-OM1$) and the pre-arcing time by the current ($I_{TM}-T3-OM1$) are $981\,\mu$s and $1.16\,$ms, respectively. Therefore, the selectivity issue is not observed in T3. However, there are still the sensitivity issue under OM1 and OM3 because the fault energy provided by the capacitor at the HL feeder is not enough to blow the fuse 1 under the study condition.

For T4 in Fig. 11b, the total clearing time of the fuse 1 on the LM feeder can be reduced from $981\,\mu$s to $821\,\mu$s. Otherwise, the ABC method can delay the pre-arcing time of the fuse 1 on the TM feeder from $1.16\,$ms to $1.74\,$ms. This increased time margin helps to provide the reliable selectivity. In T4, the fault clearing is available at $934\,\mu$s under OM3. Thus, the sensitivity is enabled with the ABC method.

Transient waveforms considering fault clearing by the fuses are shown in Fig. 12 and the results under the studied condition are summarised:



(a)



(b)

Fig. 12: Transient voltage waveforms considering fault clearing by fuse: (a) T1 and T2 and (b) T3 and T4.

- Depending on the ship operation modes and the fault locations, there are configurations for both the architectures that may have issues on the selectivity and/or the sensitivity.
- The ABC method reduces the fault clearing time for the fuse on the faulty feeder and delays the pre-arcing time for the fuse on the healthy feeder for both the architectures (achieving or helping the selectivity).
- The ABC method ensures the clearing of the fault under the maximum and minimum loading conditions for both the architectures (enabling the sensitivity).

V. Conclusion

This paper has proposed the ABC method, which is based on the additional bus capacitor installed at the DC bus, to achieve the selectivity for the bus separation failure and the feeder protection. The modelling of the low-voltage DC SPSs has been conducted, and the principle and the selection of the ABC method have been addressed. The analyses on the voltage drop and the fault clearing time have been carried out and the study results have been discussed.

For the bus separation failure, the ABC method can mitigate the voltage drop for both the centralised and distributed architectures. This improves the selectivity for the bus separation failure by reducing the possibility of the undesired converter trip in the healthy bus.

It has been shown that the ABC method can not only reduce the fault clearing time under high loading condition, but also allow for the fault clearing under low loading condition. In other words, the method helps to achieve the selectivity and the sensitivity by directly providing the additional energy to the fuse on the faulty feeder under any system conditions.

With the above results, it has been concluded that the proposed ABC method, which can be employed with relatively low cost, offers superior features in terms of the selectivity as well as the sensitivity for the bus separation failure and the feeder protection in low-voltage DC SPSs.

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