Nanotechnology

PAPER

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To cite this article: C Jürgensen *et al* 2019 *Nanotechnology* **30** 285302

IOP Publishing Nanotechnology
Nanotechnology 30 (2019) 285302 (7pp) https://doi.org/10.1088/1361-6528/ab1699

Growth of nanowire arrays from micron-feature templates

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Received 6 February 2019, revised 3 April 2019
Accepted for publication 5 April 2019
Published 24 April 2019

Abstract

Here, we present a two-step annealing procedure to imprint nanofeatures on SiO_2 starting from metallic microfeatures. The first annealing transforms the microfeatures into gold nanoparticles and the second imprints these nanoparticles into the SiO_2 layer with nanometric control. The resulting nanohole arrays show a high ensemble uniformity. As a potential application, the nanohole mask is used as a selective mask for the Ga self-assisted growth of GaAs nanowires (NWs). Thus, for the first time, a successful implementation of nano-self-imprinting that links high-throughput microlithography with bottom-up NW growth is shown. The beneficial hole morphology of the SiO_2 mask promotes high Ga droplet contact angles with the silicon substrate and the formation of single droplets in the mask holes. This droplet predeposition configuration enables a high vertical yield of NWs. Thus, this article describes a new protocol to grow NW devices that combines simultaneously nanosized holes and parallel processing.

Keywords: parallel lithography, semiconductor nanowires, nanoholes, templated dewetting, self-assembly

(Some figures may appear in colour only in the online journal)

1. Introduction

Semiconductor nanowires (NWs) are promising future building blocks in many fields such as electronic, electrochemical and photonic devices [1, 2]. With their sub-wavelength size and high aspect-ratio geometries the NWs exhibit intriguing physical phenomena that can be exploited for several applications: enhanced surface sensitivity to its surroundings for biochemical sensors, or strong light confinement for lasers and solar cells [3–8]. Besides, the NW geometries also promise additional benefit in comparison with devices based on thin films, e.g. substantial amount of material can be saved since NW devices work at relative large pitch distance [9–11]. Such material savings through the use of NWs can be best achieved with growth techniques based on the bottom-up approach instead of top-down nanosculpting of NWs from a bulk material.

Among the most common bottom-up fabrication methods are selective-area epitaxy, self-assisted or vapor–liquid–solid (VLS) growth [12–14]. For all of them, obtaining a deterministic localization of NWs on a substrate in form of arrays requires substrate patterning prior to the NW growth [15]. In the case of VLS, the pattern will consist of an array of metal (usually gold) nanoparticles. In the case of self-assisted growth, the substrate is covered with a mask (e.g. SiO_2) which is then patterned with nanoscale holes. Well-controlled self-assisted NW growth can only be obtained from small-sized holes in the diameter regime below 100 nm [16]. In addition, the NW growth by the self-assisted method requires a prior droplet deposition with high contact angles between the droplet and the surface substrate [17].

Out of a wide range of lithographic techniques, the most common approaches to achieve nanometer features have been scanning beam techniques, and in particular electron beam

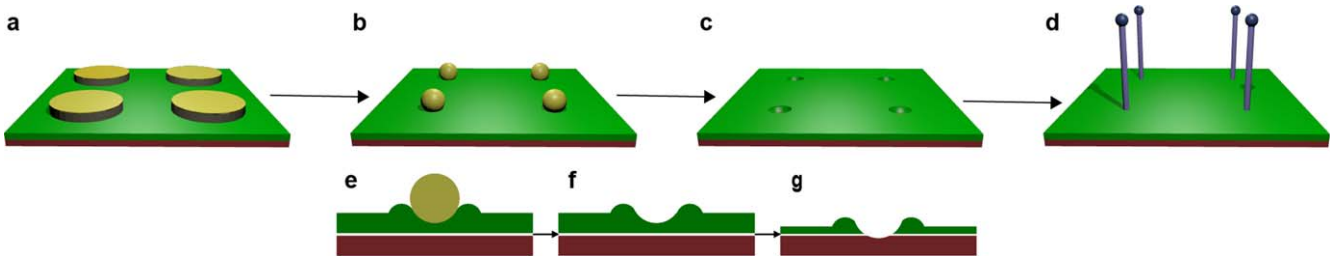

Figure 1. Schematic view of the downscaling feature fabrication process of nanohole arrays for bottom-up NW growth. Materials and colors (in brackets) used in the subfigures (a)–(g) are: silicon (red), silica (green), antimony (gray), gold (yellow), GaAs NWs (blue). (a) Micrometer-features of thin-film bilayers of antimony and gold created by deposition through a shadow mask. (b) Gold nanoparticle array after the templated dewetting by annealing step. (c) Final nanohole array in SiO_2 mask. (d) GaAs on silicon NW array using Ga self-assisted VLS growth by MBE. (e)–(g): Etching protocol for the final hole mask. Cross-section scheme of (e) the self-imprinted gold inside the SiO_2 mask after the annealing process, (f) SiO_2 hole mask deformation after removing the gold by solvent etching, and (g) hole morphology transferred by dry etching to expose the underlying silicon.

lithography, due to its accuracy and pattern flexibility [16, 18–20]. This step represents a major obstacle for future NW device commercialization since high-throughput applications require parallel processing instead of linear techniques [21].

Today, laser interference lithography and nanoimprint lithography seem to be two of the most promising parallel lithographies [22–27]. In particular, nanoimprint lithography patterns the substrate by mechanical deformation of a resist with the help of a nanoscale stamp. These stamps with features in the nanoscale range are fabricated using e-beam lithography. The main advantage of nanoimprint lithography is the direct contact, that theoretically allows single-digit nanometer resolution. This is simultaneously its most sensitive point: continuous degradation of the working nanoscale master, by resist diffusion (in soft-masters) or mechanical abrasion (in hard stamps) has limited the repeatability for holes in the nanoscale range to below one thousand consecutive imprints [28–31]. Still, notable results have been obtained for hole arrays with diameter smaller than 100 nm for NW growth [32, 33]. In general, the requirement of a hole size with a diameter smaller than 100 nm is the reason why only e-beam lithography and nanoimprint lithography have been successfully applied for self-assisted NW growth so far [16, 32, 33].

As an alternative to techniques that use top-down fabricated stamps with features in the nanoscale range, emerging high-throughput techniques such as nanosphere and block copolymer lithography decrease the feature size up to the nanoscale range using self-assembly processes [34–37]. These alternatives avoid the use of expensive masters generated by e-beam lithography. These fabrication methods are also not free of shortcomings: the pattern flexibility is relatively limited. Thus, the pitch and diameter remain closely coupled.

Here, we present a novel two-step methodology to generate a SiO_2 mask on a Si substrate to produce NW arrays by self-assisted growth starting with features in the scale of microns that can be generated by high-throughput lithography such as photolithography or stencil lithography [38]. The protocol is based on the following steps. During the first annealing, the microstructures dewet individually. The whole process is also called templated dewetting [39]. The initial volume of the microdisks defines the eventual size of the dewetted particles as it is conserved during the reshaping process. Secondly, the final morphology of the mask needs to promote self-assisted NW growth, i.e. ideally as an edge-free and smooth hole array. This might be achieved by imprinting the metal nanoparticles in the SiO_2 using a high-temperature metal-substrate interaction. This alternative has so far shown to be of limited success, with initial crater-like structures or enhanced etching rates [40–43]. Here, we consider the application of this protocol at slightly lower temperatures.

Thus, we make use of the two above-mentioned processes (volume-conserving dewetting, and metal-substrate interaction/nano-self-imprinting). This combination turns a microscale-pattern into an array of nanoholes with feature sizes lower than 100 nm allowing the use of high-throughput lithography with microscale resolution such as photolithography to grow well-controlled NWs. In our case, we demonstrate the potential of this protocol growing GaAs NWs on a silicon substrate using the Ga-assisted VLS method.

2. Experimental

Figure 1 depicts the main steps of the NW growth process. First, we generate microscale-sized features (figure 1(a)). In our case, the microstructures consist of disk-shaped metallic thin films on an oxidized silicon substrate. The dewetting process of extremely thin films (e.g. few nanometers) is improved by depositing an additional thin film with lower melting point at the interface with the substrate. In our case we have used antimony [44]. During the annealing, antimony sublimates through the sidewalls of the microdisk and thus promotes the dewetting of the metallic top layer. Ultimately, this approach results in single nanoscale particles starting from micrometer-scale features (figure 1(b)). Thus, the nanoparticles will be located close to the center of the previous microdisks and the average pitch distance between the nanoparticles will be the predefined distance between two adjacent microdisks' centers.

The following step consists in the imprinting of the nanoparticle shape into the oxide of the substrate using a second high-temperature annealing (figure 1(e)) [40–43]. The

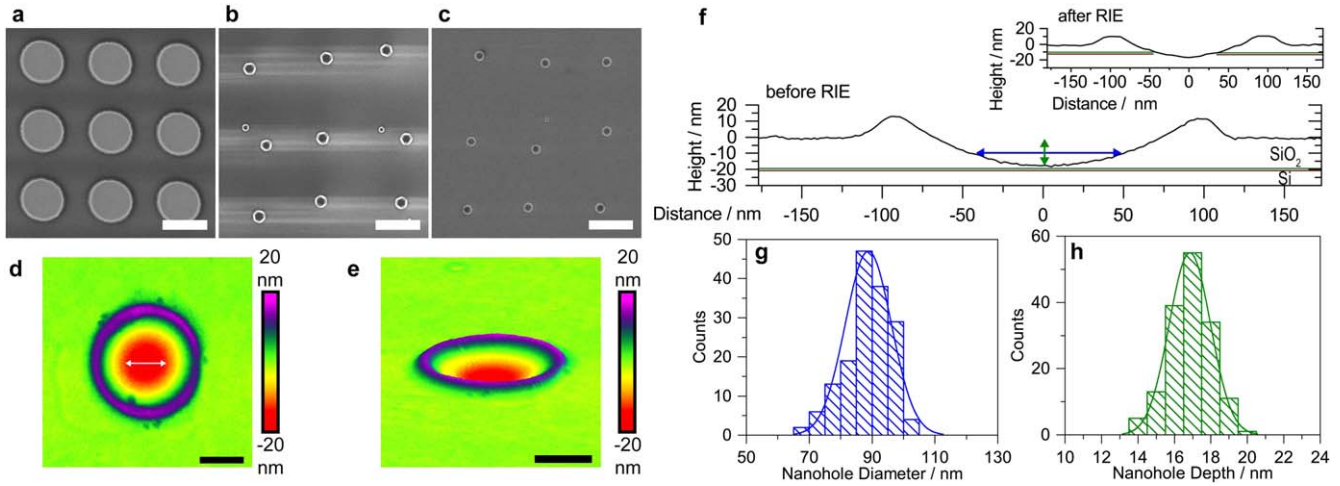

Figure 2. Characterization of the SiO_2 mask. Top-view SEM images of (a) micrometer-scale structures of a thin bilayer of antimony and gold on a SiO_2-silicon substrate, (b) slightly randomized gold nanoparticle array after the annealing, and (c) self-imprinted nanoholes generated on the substrate after the solvent etch. Scale bars are 1 μm. (d) Top-view color-coded AFM image of a single nanohole. The main characteristics that can be seen from the color contrast are its lateral roundness and the ring formation around the nanoparticles. The arrow indicates the Si open area diameter. Depicted scale bar: 100 nm. (e) 70°-tilted view of the hole. Depicted scale bar: 100 nm. (f) AFM profile of a representative hole in the mask, with diameter and height of the Si open area shown by lateral blue and vertical green arrows. Inset: AFM profile after RIE step. - The silica–silicon interfaces are depicted with a green-and-red horizontal line. The material transition in the border of the open holes is smooth after the RIE step. (g) Histogram of diameter of the Si open areas and (h) histogram of the Si open area depth based on AFM measurements of 158 holes.

gold nanoparticles, and therefore the self-imprinted nanoholes, do not reach the Si substrate, avoiding the metal contamination of the silicon substrate. Figures 1(e)–(g) depict the process of creating the final hole mask. The cross-sectional sketch on the left shows a gold nanoparticle that has self-imprinted into the oxide layer and leaves behind a footprint on the SiO_2 mask. To create a two-material oxide-patterned hole mask, the hole morphologies need to be shifted into the underlying silicon substrate (figures 1(f)–(g)). This etching process of the SiO_2 layer and the underlying silicon substrate can be done homogeneously using standard etching protocols such as dry etching. The step described in figures 1(e)–(g) combines the advantages of parallel processing with the production of small-scale features and control over the three spatial dimensions. Thus, the substrate can now be used as a growth mask (figure 1(c)), since the NW growth will only occur inside the nanoscale holes. In this article, we describe the gallium-assisted method to grow arrays of GaAs NW (figure 1(d)).

3. Results and discussion

Figures 2(a)–(c) present a top view of the mask formation using scanning electron microscopy (SEM). We started with Sb/Au microdisks (thickness of 100 nm and 8 nm, respectively) on a silicon substrate with 15 nm of thermal oxide. The disks are 1 μm in diameter (figure 2(a)). The antimony layer has been depleted by an annealing process using a similar protocol to as is described in [44] (two consecutive temperature steps at 615 °C during 10 min and 1030 °C during 30 min, with heating rates of 60 °C min^{-1}). The microdisks have shrunk into a slightly randomized array of gold nanoparticles (figure 2(b)). We observed deviations of up to hundreds of nanometers, which are similar to results presented by Farzinpour *et al* [44].

An additional temperature step (at 950 °C, 8 h) results into the partial removal of the oxide below the gold nanoparticles. We then remove the gold particles by wet etching (potassium iodide and iodine, concentration of 25 g l^{-1} and 12 g l^{-1}, respectively), showing the nanoscale marks imprinted on the substrate (figure 2(c)). We observe ring-like structures that appear brighter in the top-view SEM compared to both the unaltered substrate around them and the areas they are enclosing. We turn now to the three-dimensional characterization of the nanoscale holes by atomic force microscopy (AFM). Figure 2(d) shows a typical AFM measurement of a nanoscale hole created by the nano-self-imprinting process. The figure shows the round shape of the nanohole. Figure 2(e) shows the same hole but with a 70° perspective, highlighting the low aspect ratio and the internal shape of the hole.

The AFM-cross-section hole profile is shown in figure 2(f). The parabolic shape of the imprinted hole allows to control the diameter of the substrate open area by controlling the reactive ion etching (RIE) parameters (figures 1(f)–(g)). We targeted a substrate open area of 90 nm in diameter and thus its deepest point is almost 20 nm below the surface of the surrounding substrate as we show with the arrows in figure 2(f). It is surrounded by a ring of about 15 nm in height above the substrate surface. In addition, AFM measurements after the dry etch confirm that the hole morphology has been conserved and the holes expose the silicon substrate (see inset in figure 2(f)). With this step, we transferred the morphology into the underlying silicon. Figures 2(g)–(h) provide statistical data, i.e. mean diameter

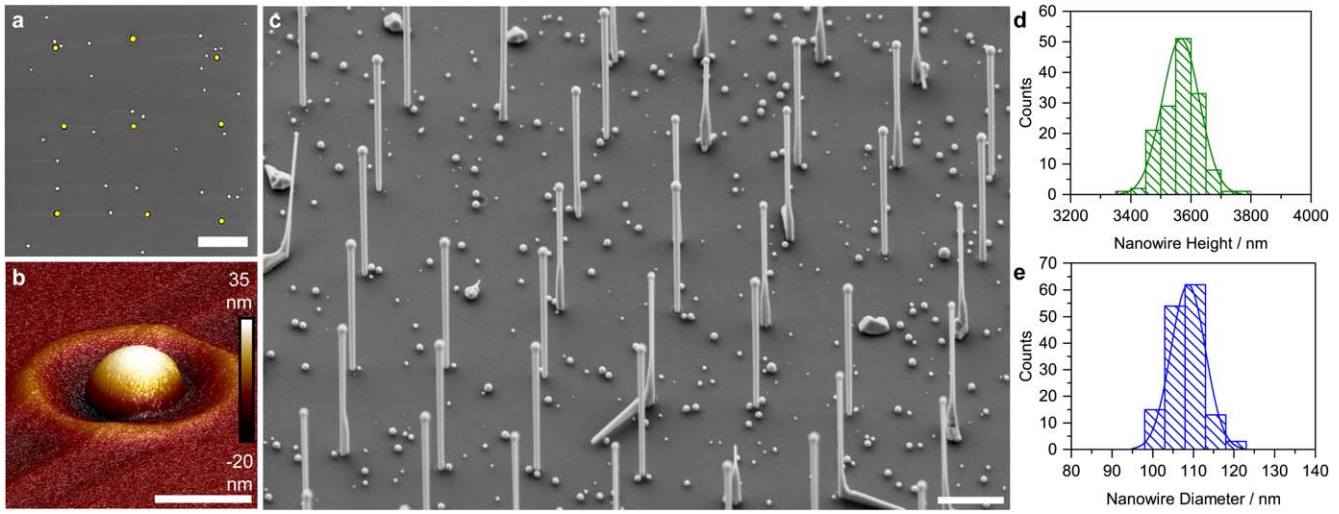

Figure 3. Characterization of the Ga predeposition and NW growth by MBE. (a) Top-view SEM image of the mask filled with single Ga droplets (droplets within holes are color-coded in yellow). Scale bar: 1 μm. (b) Magnified 60°-tilted AFM image of an individual hole filled with a Ga droplet. Depicted scale bar: 100 nm. (c) 35°-tilted SEM view of the NW array. Scale bar: 1 μm. (d)–(e) Histogram of the NW diameter and height. Only uniformly grown vertical NWs (applies to 50% to 60% of vertical NWs) were analyzed (147 wires).

and standard deviation (SD) of the diameter and hole depth of the open silicon area, taken from 158 holes. We confirm a similarly narrow distribution of open-area diameter (89 nm, SD: 8.2%) and of the depths of the holes (17 nm, SD: 6.7%) - a signature of the high reproducibility of the process. A comparison with the microdisks (mean diameter of 933 nm, SD: 1.3%) and the nanoparticles (mean diameter: 275 nm, SD: 2.3%) shows that the SD slightly increases.

Prior publications on gold nanoparticles digging into SiO_2 substrates have shown that nanoholes or pores can be fabricated by high temperature heating. Vreede and co-workers achieved narrowing nanopores with high aspect ratio by homogeneous furnace-heating of gold particles close to their melting point (1050 °C) [40]. Local plasmonic heating or joint photothermal and magnetic heating of single nanoparticles have likewise shown that one can produce small and smooth holes [41, 42].

The lateral hole dimension is governed by the gold volume before the initial dewetting step. Vreede describes the underlying mechanism of the process as a continuous transport of SiO_2 along the gold–silica interface to optimize the gold–silica–air triple line. This explains the build-up of a ring [45]. The key parameter for the final three-dimensional achieved morphology is the temperature. The intrinsic limits are the onset of viscous flow of silica observed at temperatures above 925 °C in silica films, and the gold melting point at 1064 °C [46]. Being close to the lower value of this temperature range has enabled us to control the imprinting velocity rate of the SiO_2 and achieve morphologies that are smooth as shown in figure 2(f). In addition, the roundness of the holes can be explained by the fact that the solid gold nanoparticles at high temperatures are approximately spherical, i.e. truncated spheres on a substrate, without elongated facets [47, 48]. During the cooldown the nanoparticles undergo facet formation, whilst the amorphous silica substrate remains with the same morphology and the holes maintain their round shape [46–48].

In summary, the here proposed approach combines the parallel processing with the nanometric control over the depth. Thus, we have been able to transfer a pattern with a micron-feature size down to 90 nm, more than one order of magnitude. In general, the final feature diameter can be further downscaled by reducing the dimensions of the initial microdisks or modifying the nano-self-imprinting step according to the application requirements.

As a proof of concept, we demonstrate the robustness of the nanoscale holes using the developed SiO_2 mask to grow semiconductor NWs by molecular beam epitaxy (MBE). We use the Ga-assisted VLS growth of GaAs NWs. In this method, Ga droplets are used to gather $As_{2/4}$ to create GaAs NWs [13, 16, 49]. In organized growth, the Ga droplets are pre-deposited before the introduction of As_4 so that the growth can be deterministically localized. Theoretically, Ga is collected mainly inside the open silicon areas, as its sticking coefficient on SiO_x is mostly null. In practice, the formation of Ga pre-deposited droplets on top of the mask has been reported. Many reasons can explain this effect e.g. different substrate preparation. It was confirmed though that the Ga droplets on the mask do not affect the NW growth [50–52].

Figure 3(a) displays a representative top-view SEM image of the substrate after a 10 min exposure of a Ga flux at the NW growth temperature (Ga rate 1.1 Å s^{-1}). The majority of Ga atoms are collected within the holes. The Ga droplets inside the silicon open areas are highlighted in yellow and show that almost all of the self-imprinted nanoscale holes are occupied. In total, close to 99% of the holes are occupied by a single droplet. These results prove that almost all the holes are open, emphasizing the quality of the developed mask.

A magnified tilted AFM image of a single nanohole shows that the Ga droplets are centered inside their holes (figure 3(b)) and exhibit a high contact angle (higher than

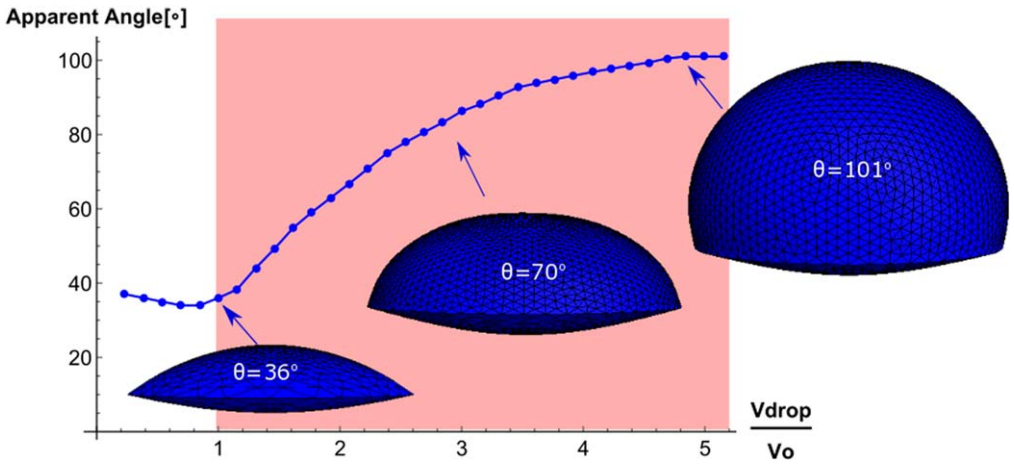

Figure 4. Theoretical study of the Ga droplet contact angle change in a Gaussian-shape two-material hole morphology. Apparent angle means the Ga droplet contact angle with respect to the horizontal plane. The regime of droplet-pinning at the material interface is highlighted in red. Three respective droplets during the volume increase are shown as insets with their respective apparent contact angles.

85°). This high contact angle is a key requirement for NW growth [53]. Contact angles of this value have previously been achieved in successful NW growth by tailoring the native oxide thickness, or by filling a nanohole completely [17, 53]. In our case, the droplet size matches closely with the silicon open area size and simultaneously exhibits a high contact angle (figure 3(b)). The implications of the hole morphology in the Ga droplet growth can be modeled using the Surface Evolver program [54]. Thus, we studied the change of the Ga contact angle with the increment of the Ga droplet volume (V_{drop}).

The results of our simulations are shown in figure 4, where the apparent angle is plotted as a function of the droplet volume. The apparent contact angle is defined as the angle between the Ga droplet tangent at the triple-phase line with respect to the horizontal plane. Two regimes can be identified. In the first regime, the droplet size increases whilst the apparent angle slightly reduces until the value of 34°. At $V_{drop}/V_o = 1$, the Ga droplet reaches the sharp two-material separation interface. This decrease is connected to the variation of the inclination of the sidewalls, particularly relevant close to the center; the angle corresponds to the difference between the value of the Ga wetting contact angle on silicon (51°) and the inclination of the sidewalls of the hole. In the first case, the increase of volume corresponds to the spread of the droplet perimeter. In the second regime, the increment of the droplet volume promotes the increment of the droplet's wetting apparent angle. The apparent angle is saturated at the apparent value of 101°, in agreement with the expected contact angle for a Ga droplet on a SiO_2 substrate (real wetting angle of 116°). The availability of a wide range of possible apparent angles for sessile droplets at the interface between different materials is known as 'pinning effect' [55, 56]. Thus, we argue that our observed high contact angles are indeed the result of the pinning at the material interface line and we can postulate that this phenomenon is associated with the smooth geometrical transition (figure 2(f)) between the two materials produced by the nano-self-imprinting step [56].

After the predeposition of Ga droplets, we continued with the standard growth procedure by providing As_4 and Ga (the growth conditions are explained in methods section). A tilted-view SEM image of the NW array is shown in figure 3(c). The NWs grow vertically on the Si substrate in a well-organized manner at their predefined positions defined by the self-imprinted nanoscale holes. The growth of the GaAs NWs is highly uniform, and each NW ends with the Ga droplet on top. Note that the spatial arrangement of the NWs is slightly shifted from a perfectly regular array. This low degree of non-periodicity could be used to optimize light absorption in applications such as NW-based solar cell devices [11].

Vertical NWs (55%) and nanocrystalline growth (41%) are the two dominant NW growth phenomena. Tilted wires are rare (3%) and less than 1 of 1000 holes are empty. Thus, the ratio of vertical to tilted wires is extremely high (19:1). For the vertical NWs without a broadened base or appending crystalline growth (50%–60% of vertical wires, 147 wires measured), both height (mean value: 3.57 μm, SD: 1.7%, figure 3(d)) and diameter (mean value: 109 nm, SD 3.9%, figure 3(e)) show a narrow distribution.

This proves that NWs can be grown selectively in the nano-self-imprinted holes with high vertical yield and there is a prospect for uniform growth with perfect yield. The special shape of the holes also inhibits the undesired tilted growths. These results place nano-self-imprinted holes as a real alternative parallel technique that is able to produce a mask for high-yield self-assisted VLS NW growth. Suitable applications of this technology should combine the need for small features at relatively large pitch and high-throughput fabrication, e.g. NW solar cells, LEDs and biochemical sensors.

4. Method section

111 silicon wafers with 15 nm thermal oxide (Centrotherm furnace, 950 °C) were diced into equilateral triangles with a side length of 12 mm. A carbon TEM-grid (Quantifoil, nominal hole diameter: 600 nm, nominal pitch: 1600 nm) was

coated from both sides with 40 nm titanium by magnetron sputtering (Alliance-Concept DP 650, Sputter single chamber multi-target) and used as a shadow mask for metal deposition. Conformal contact was achieved by capillary forces of a droplet of acetone added from the top. Thin films of antimony (100 nm) and gold (8 nm) were deposited by magnetron sputtering.

After mechanical removal of the mask, the samples were placed into an alumina crucible (Coorstek AD-998, 100 ml) and annealed in a programmable furnace (Neytech Centurion Qex) with the following temperature profile: heated to 615 °C, kept for 10 min, heated to 1030 °C, kept for 30 min, passive cooldown to 950 °C, kept for 8 h, passive cooldown to room temperature (atmospheric pressure with nitrogen inflow of 300 l h^{-1}, heating rates: 60 °C min^{-1}).

Afterwards, the gold was removed by a potassium iodide and iodine etching solution (concentration of 25 g l^{-1} and 12 g l^{-1}, respectively) and the samples were cleaned with acetone, isopropyl alcohol and oxygen plasma. The oxide thickness of the mask was reduced with RIE (CHF_3, Ar) to a nominal thickness of around 12 nm.

The chips were shortly dipped in buffered hydrofluoric acid (BHF1:7) prior to the introduction into the ultra-high-vacuum (UHV) chamber of the MBE The substrates were annealed at 500 °C for 2 h in UHV condition in order to ensure a pristine surface. The substrates were then transferred to the growth chamber. There, the chips were degassed at 770 °C for 30 min to further remove surface contaminants. In the first step, Ga was predeposited for 10 min at a beam equivalent pressure (BEP) of Ga of 1.4×10^{-7} Torr (corresponding to a nominal Ga growth rate of 1.1 Å s^{-1}) by keeping the shutter opened. For the NW growth recipe, once the growth temperature had been reached, the As_4 source was opened for 30 min at BEP of As_4 of 2×10^{-6} Torr, at a substrate temperature of 634 °C, as measured by pyrometer, and with 7 rpm rotation.

Oxide thicknesses were characterized by ellipsometry (Sopra GES 5E). All SEM images shown in the figures and those used for analysis were taken with a Zeiss Merlin and Zeiss Leo Microscope. AFM images were taken in the ScanAsyst mode with a silica tip and silicon nitride cantilever (AFM Bruker, ScanAsyst-Fluid+). Diameter calculations were based on areas from AFM isoheight lines using the NanoScope Analysis software. Hole depth and ring height were analyzed with the Gwyddion software. In all statistics, multiple-hole features and growth therein were excluded. The simulations regarding the apparent angle were performed with the Surface Evolver software package [54]. We approximate the system with a droplet sitting at the center of an inverted Gaussian-shaped hole due to its computational advantage and close fit with the observed inner holes morphology of the mask (figure 2(f)). The interface between different materials is implemented by a sharp modification of the interfacial energies as a function of the vertical dimension. The stability of the droplet configuration is ensured by the radial symmetry of the hole geometry.

5. Conclusion

We have shown a novel process to produce nanoscale silicon open areas on a silicon wafer covered with a SiO_2 mask by a novel self-assembly two-step method. We show the potentiality of the SiO_2 mask by growing self-assisted NWs on a silicon substrate. The two steps - templated dewetting and nano-self-imprinting - give nanometric control of all three spatial dimensions and enhance the single feature resolution of the lithographic technique by more than one order of magnitude, from 1 μm to 90 nm. The formed holes were filled with a single Ga droplet (99%), showing the quality of the nano-self-imprinting process. The hole morphology is advantageous for high droplet contact angles and suppresses tilted growth and leads to a promising vertical yield of 55%, which is predicted to improve. Thus, these results put this post-lithographic approach as another method - next to e-beam and nanoimprint lithography - to produce nanohole arrays for successful self-assisted VLS NW growth. A large variety of future applications of NWs seem destined to become realizable at high throughput using the nano-self-imprinting procedure.

Acknowledgments

The funding for this research was provided by Swiss National Science Foundation (SNSF, projects nr 200021_172547, 200021_169908 and IZLRZ2_163861) and Horizon 2020 European Union Funding for Research and Innovation through projects ITN INDEED and Marie Curie (3G-R2R).

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