# Nanocrystalline Silicon Oxide Stacks for Silicon Heterojunction Solar Cells for Hot Climates

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**Abstract.** Today, solar cells are generally optimized for 25 °C, whereas in most climates, especially hot and sunny ones, the operating device temperature is usually much higher, e.g. in the range of 60 °C. We investigate the use of n-doped nanocrystalline silicon oxide layers (nc-$SiO_x$:H(n)) as front contact stacks in silicon heterojunction solar cells and compare them with oxide-free front contacts. Whereas a short-circuit current density of 41 $mAcm^{-2}$ could be obtained due to the increased transparency of the nc-$SiO_x$:H(n) layers, the fill-factor is drastically reduced and leads to a reduced efficiency at 25 °C. Albeit the FF can be partly recovered at 60 °C, the highest efficiencies at 60 °C were so far obtained for the solar cells with oxide-free front contact stacks.

## INTRODUCTION

Usually, solar cell devices are optimized to give the highest performance at standard test conditions (STC), which is at 25 °C. In operation conditions, usually the temperature of the device is much higher, especially in hot and sunny climates [1], [2]. In silicon heterojunction (SHJ) solar cells, charge carrier transport is partly thermally activated due to the existence of transport barriers, which are more easily overcome with increasing temperature. Thus, the optimization for silicon heterojunction solar cells for operation at e.g. 60 °C might be different from the one at 25 °C. Possibly, more transparent layers could be used at the front side as e.g. oxygen-doped layers. While the addition of oxygen might hinder charge carrier transport at 25 °C, transport might be impacted only marginally at 60 °C. In previous experiments [3] it has been shown that with the addition of $CO_2$ during PECVD the transparency of a-Si:H can be increased for wavelengths below 500 nm. However, charger carrier transport is strongly limited, also at 60 °C, for a-$SiO_x$:H(n) versus an a-Si:H(n) front contact, when $CO_2/SiH_4$ ratios are chosen such that a significant increase in transparency is obtained (conclusion drawn from previous experiments, data not shown).

It is possible to grow nanocrystalline silicon oxide (nc-$SiO_x$:H) films with a filament-like structure that consists of a nanocrystalline silicon (nc-Si:H) phase within an amorphous oxide matrix [4]–[6]. Two strategies have been pursued to increase the crystallinity of the n-contact layer stack: a lower deposition temperature (175°C) and an $SiO_x$-plasma pre-treatment as it was reported that both increase the crystallinity of nanocrystalline silicon [7], [8]. With increased crystallinity, we expect an increased transparency as well as increased conductivity.

# EXPERIMENTAL

## Methods: Solar Cell Preparation & Analysis

Silicon heterojunction solar cells have been prepared on 240 µm 1-5 Ωcm n-type silicon Fz wafers. As front contact layers, we chose different n-doped stacks as depicted at the bottom of **FIGURE 1**. The wafers have been wet-chemically cleaned and dipped in hydrofluoric solution prior to the deposition of the silicon-based contact layers by plasma enhanced chemical vapor deposition (PECVD). The minority charge carrier collecting contact consists of a stack of intrinsic and p-doped amorphous silicon at the rear side of the wafers (rear junction configuration). The amorphous layers have been deposited at 200 °C. All front-contact nanocrystalline silicon stacks are approximately 16 nm thick. For (v) and (vi), the subjacent a-Si:H(n) layer is approximately 15 nm thick. The nc-$SiO_x$(n) layers of (iii) and (iv) account for approximately two thirds of the stack (~11 nm), while nc-Si(n) accounts for one third (~5 nm). All layer thickness values correspond to depositon on a planar glass sample, we assume the actual layer thicknesses on the textured wafer to be lower by a factor of 1.7. The temperature during the deposition of the nanocrystalline layers was set to either 200°C or 175°C (indicated with red and blue color respectively in **FIGURE 1**). The $SiO_x$-plasma pre-treatment (samples ii, iv, and vi) was carried out by PECVD in the same chamber and at the same temperature as the nanocrystalline layers with a gas mix of $SiH_4$, $H_2$, and $CO_2$. During a five-second plasma-treatment, no layer is deposited (thickness change not detectable with ellipsometry), but the surface of the subjacent layer is modified to promote crystalline growth [7], [9], [10]. Directly after the plasma-treatment, the nanocrystalline layer is deposited, without vacuum break.

A sputtered indium tin oxide (ITO) and a screen-printed Ag grid finalize the front contact. At the rear side, sputtered ITO/Ag forms the rear electrode.

The solar cells have been measured on a temperature-controlled chuck, under one-sun AM1.5g irradiation of a AAA solar simulator. The temperatures of the chuck were 25°C and 60°C. SunsVoc and lifetime characteristics have been obtained using a Sinton Instruments lifetime tester. Raman spectroscopy has been carried out with a UV (325 nm) laser.

## Solar Cell JV Parameter & Raman Crystallinity

**FIGURE 1** shows the illuminated JV parameters open-circuit voltage ($V_{OC}$), short-circuit current density ($J_{SC}$), fill-factor (FF), and efficiency (Eff) of the solar cells as well as implied $V_{OC}$ ($iV_{OC}$) and fill-factor (iFF) obtained from lifetime measurements after PECVD. The passivation for injection conditions corresponding to $V_{OC}$ and maximum power point (MPP) are on a high level which is reflected by $iV_{OC}$ values above 725 mV and iFF values generally above 85% for the samples. For the devices (iii)-(vi) the $V_{OC}$ is around 715 mV. The lower $V_{OC}$ compared with the $iV_{OC}$ is partly due to the application of a shadow mask during JV measurement and partly due to other damage caused by the TCO deposition, screen-printing and curing. For the devices with a nc-Si:H(n) front contact (i), (ii) deposited at 175 °C the $V_{OC}$ is significantly lower compared with devices with a nc-Si:H(n) front contact deposited at 200 °C, which suggests that the selectivity provided by the layers deposited at 175 °C is insufficient to transmit the $iV_{OC}$ to the external contact. This is most significant when an additional $SiO_x$-plasma is used (ii). Raman measurements suggest a higher crystallinity with the plasma treatment. However, in the experiments shown here, this does not result in increased selectivity as can be seen from the lower FF. Implementing nc-SiOx(n) (iii and iv) in the front contact stack yields a $J_{SC}$ of 41 $mAcm^{-2}$ which is a gain of 1 $mAcm^{-2}$ over the oxide-free front contacts (i and ii). This $J_{SC}$ gain is, however, counterbalanced by a reduction in FF and leads thus to a lower efficiency at 25 °C.

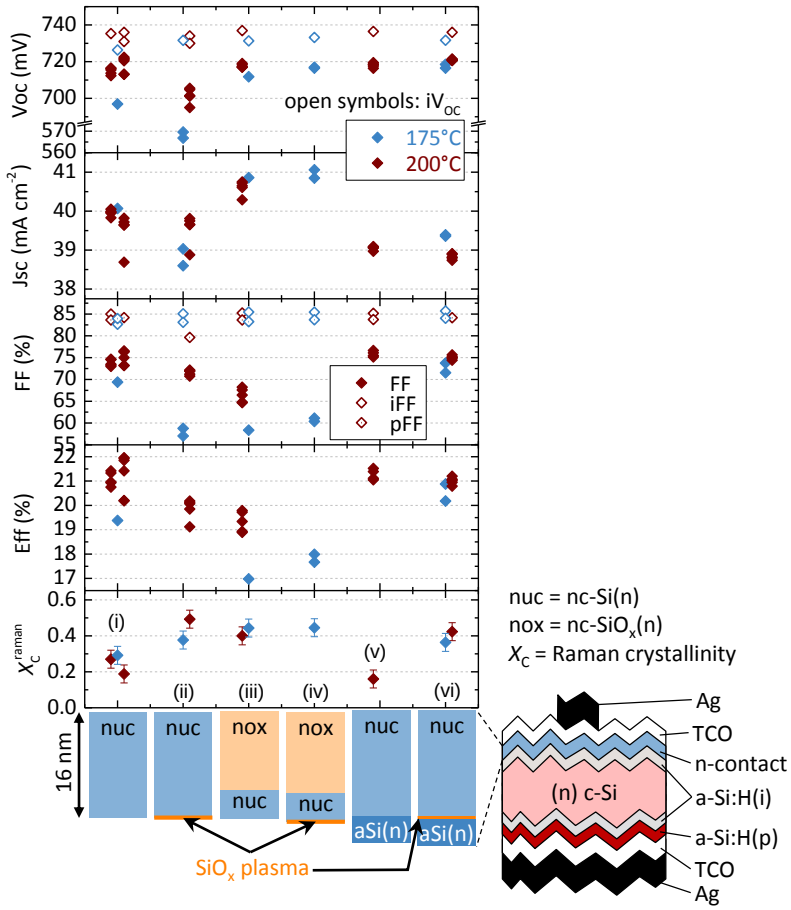


**FIGURE 1.** Illuminated JV parameters at standard test conditions of silicon heterojunction solar cells with the minority charge carrier collecting contact at the rear side and a variation of n-contact stacks at the front. The implied $V_{OC}$ and implied FF (open symbols) were obtained from Sinton lifetime tester measurements. The Raman crystallinity of the front contact stack is included as well.

## External Quantum Efficiency

**FIGURE 2** shows the external quantum efficiency (EQE) for the wavelength range between 320 nm and 700 nm. Solar cells with an oxide-containing front-contact stack feature a lower parasitic absorption in this wavelength range. Albeit the $SiO_x$-plasma increases Raman crystallinity, the decrease in parasitic absorption is negligible.

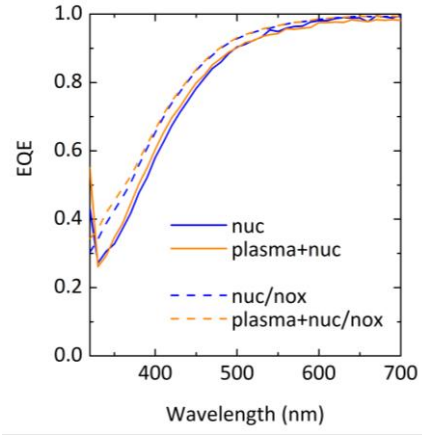


**FIGURE 2.** External quantum efficiency (EQE) for the solar cells (i)-(iv) from FIGURE 1.

## Performance at Higher Temperature

**FIGURE 3** shows the JV parameters of two selected solar cells (iii and v from FIGURE 1) under 1-sun-illumination at 25 °C and 60 °C, and calculated trends for temperature dependency from literature [11], [12]. With the use of an nc-$SiO_x$:H(n)/nc-Si(n) stack a $J_{SC}$ gain of 5% is obtained over an a-Si:H(n)/nc-Si(n) front contact stack. However, at 25 °C, the FF suffers a reduction of 20% for the stack containing nc-$SiO_x$:H(n). This reduction is

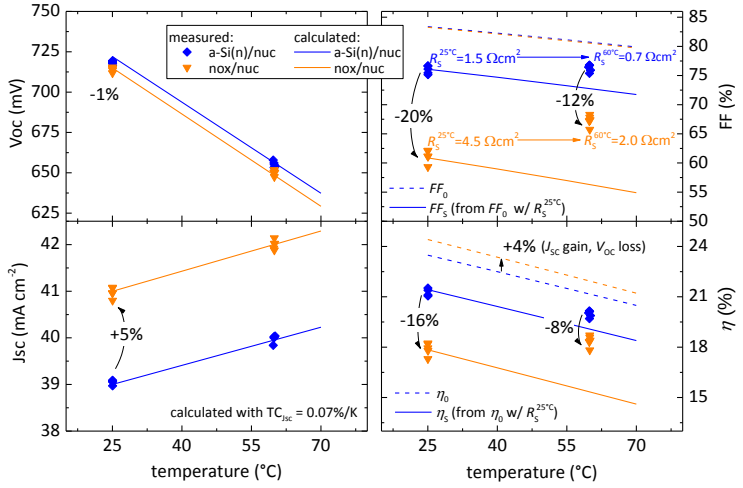


**FIGURE 3.** JV parameters of two selected solar cells (iii and v from FIGURE 1) under one-sun illumination for 25°C and 60°C. The measured data are compared with models from literature. For the calculated trends (solid lines), the series resistance is considered to be independent from temperature.

decreased to 12% at 60 °C which corresponds to a reduction of the series resistance from 4.5 $\Omega cm^2$ at 25 °C to 2.0 $\Omega cm^2$ at 60 °C. This effect is not aligned with the literature models, and can be explained by a thermionic barrier present in our devices. It also leads to a slightly positive temperature coefficient for the cell containing oxide in the front contact. However, we would like to underline that the important figure of merit is the performance at higher temperature and not the temperature coefficient, as despite the decrease of transport hindrance and the $J_{SC}$ gain, the efficiency at 60 °C is higher for the oxide-free front contact stack. It is important to note that also charge carrier transport in the oxide-free solar cell is thermally activated as its $R_S$ is decreased from 1.5 $\Omega cm^2$ at 25 °C to 0.7 $\Omega cm^2$ at 60 °C. Thus, it appears as if first, our SHJ solar cell process should be optimized to be able to deliver SHJ solar cells with very high FF (well above 80%). Then, in a second step, FF at 25°C could possibly be sacrificed to increase current by using a more transparent but less conductive contact layer. Finally, if the FF can be sufficiently recovered at 60°C, this would result in an efficiency gain at 60°C.

## SUMMARY

We have shown results of silicon heterojunction solar cells featuring n-type crystalline silicon-based front contact stacks. With an nc-$SiO_x$:H(n)/nc-Si:H(n) stack, a short-circuit current density of 41 $mAcm^{-2}$ has been achieved for a screen printed cell with external busbars and standard ITO (ITO/Ag) as front (and rear) electrodes. However, a temperature-dependent transport hindrance leads to a strong fill-factor (FF) decrease at 25 °C when nc-$SiO_x$:H is used. The FF is partly recovered at 60 °C, however, the highest performance at 60 °C is obtained for the oxide-free front-contact stacks so far.

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## REFERENCES

[1] J. Haschke, J. P. Seif, Y. Riesen, A. Tomasi, J. Cattin, L. Tous, P. Choulat, M. Aleman, E. Cornagliotti, A. Uruena, R. Russell, F. Duerinckx, J. Champliaud, J. Levrat, A. A. Abdallah, B. Aïssa, N. Tabet, N. Wyrsch, M. Despeisse, J. Szlufcik, S. De Wolf, and C. Ballif, “The impact of silicon solar cell architecture and cell interconnection on energy yield in hot & sunny climates,” *Energy Environ. Sci.*, vol. 10, no. 5, pp. 1196–1206, 2017.

[2] A. Abdallah, D. Martinez, B. Figgis, and O. El Daif, “Performance of Silicon Heterojunction Photovoltaic modules in Qatar climatic conditions,” *Renew. Energy*, vol. 97, pp. 860–865, 2016.

[3] J. P. Seif, A. Descoeudres, M. Filipič, F. Smole, M. Topič, Z. C. Holman, S. De Wolf, and C. Ballif, “Amorphous silicon oxide window layers for high-efficiency silicon heterojunction solar cells,” *J. Appl. Phys.*, vol. 115, no. 2, p. 024502, Jan. 2014.

[4] P. Cuony, D. T. L. Alexander, I. Perez-Wurfl, M. Despeisse, G. Bugnon, M. Boccard, T. Söderström, A. Hessler-Wyser, C. Hébert, and C. Ballif, “Silicon Filaments in Silicon Oxide for Next-Generation Photovoltaics,” *Adv. Mater.*, vol. 24, no. 9, pp. 1182–1186, Mar. 2012.

[5] A. Richter, V. Smirnov, A. Lambertz, K. Nomoto, K. Welter, and K. Ding, “Versatility of doped nanocrystalline silicon oxide for applications in silicon thin-film and heterojunction solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 174, no. July 2017, pp. 196–201, 2018.

[6] L. Mazzarella, A. B. Morales-Vilches, M. Hendrichs, S. Kirner, L. Korte, R. Schlatmann, and B. Stannowski, “Nanocrystalline n-Type Silicon Oxide Front Contacts for Silicon Heterojunction Solar Cells: Photocurrent Enhancement on Planar and Textured Substrates,” *IEEE J. Photovoltaics*, vol. 8, no. 1, pp. 70–78, 2017.

[7] J. P. Seif, A. Descoeudres, G. Nogay, S. Hanni, S. M. de Nicolas, N. Holm, J. Geissbuhler, A. Hessler-

Wyser, M. Duchamp, R. E. Dunin-Borkowski, M. Ledinsky, S. De Wolf, and C. Ballif, “Strategies for Doped Nanocrystalline Silicon Integration in Silicon Heterojunction Solar Cells,” *IEEE J. Photovoltaics*, vol. 6, no. 5, pp. 1132–1140, Sep. 2016.

[8] M. Boccard, R. Monnard, A. N. Fioretti, L. Antognini, and C. Ballif, “Silicon Oxide Treatment to Promote Crystallinity of p-type Microcrystalline Layers for Silicon Heterojunction Solar Cells,” in *Proceedings of SiliconPV2018, AIP*, 2018.

[9] L. Mazzarella, S. Kirner, O. Gabriel, S. S. Schmidt, L. Korte, B. Stannowski, B. Rech, and R. Schlatmann, “Nanocrystalline silicon emitter optimization for Si-HJ solar cells: Substrate selectivity and CO2 plasma treatment effect,” *Phys. Status Solidi Appl. Mater. Sci.*, vol. 214, no. 2, 2017.

[10] M. Boccard, R. Monnard, A. N. Fioretti, L. Antognini, and C. Ballif, “Silicon oxide treatment to promote crystallinity of p-type microcrystalline layers for silicon heterojunction solar cells,” in *SiliconPV 2018*, 2018.

[11] M. Green, K. Emery, and A. Blakers, “Silicon solar cells with reduced temperature sensitivity,” *Electron. Lett.*, vol. 18, no. 2, pp. 97–98, 1981.

[12] M. A. Green, “Accuracy of analytical expressions for solar cell fill factors,” *Sol. Cells*, vol. 7, no. 3, pp. 337–340, Dec. 1982.