Doping-free complementary inverter enabled by 2D WSe_2 electrostatically-doped reconfigurable transistors

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Introduction

Amongst 2-dimensional (2D) semiconductors of the transition-metal di-chalcogenide (TMDC) family [1], tungsten diselenide (WSe_2) has shown ambipolar behavior [2,3] coupled with high carrier mobility [4] and CMOS-like devices have been experimentally demonstrated using chemical doping of the material [5,6]. However, since chemical doping is often non-compatible with conventional CMOS processes and is limited by the desorption of the chemical species used [5-7], we explore the possibilities offered by electrostatic doping. Here, we exploit the presence of Schottky barrier contacts in WSe_2, and using electrostatic doping we achieve dynamic control of the polarity of the transistors. We fabricate, for the first time on a 2D material, a doping-free complementary inverter, providing a path for the realization of CMOS logic with a single ambipolar, undoped 2D semiconducting material.

Device concept and fabrication

The key to unlock the possibility of controlling the polarity of the transistor is the separate gating of different channel regions, thanks to a double-independent-gate (DIG) structure [3]. By adding a second gate, named polarity gate (PG), we are able to electrostatically dope the contact interfaces and select the injection of either electrons or holes. A conventional gate, i.e. control gate (CG), separated by the PG, acts in the central region of the channel, controlling the ON/OFF state of the device. For the fabrication of the devices, WSe_2 flakes are exfoliated and then transferred on a target substrate with pre-patterned back-gates (2nm Ti/10nm Pt) isolated with ALD-deposited ZrO_2. Metal contacts (2nm Ti/50nm Pd) are then evaporated (see Fig. 1(a-b)). The channel length is around 1μm.

Results and Discussion

Fig. 2(a) shows the measured transfer characteristics of the single device where ambipolar conduction and reconfigurable behavior can be observed. When the PG is biased at 0 V or below, electron conduction is suppressed and holes are favorably injected in the channel, with the device behaving as a *p*-type transistor. Conversely the transistor is programmed to function as a *n*-type device when the PG is biased at 3V and above. In both cases, the CG is able to turn ON and OFF the transistor when swept between 0 and 2V. High ON/OFF ratios of respectively 10^5 and 10^6 for *n*- and *p*-type conduction are achieved on the same device, with low leakage floor of around 1pA. Thanks to the use of Pt gates, *p*-type operation is achieved for V_{PG} = 0V, which is an essential step to ensure cascadability of the logic gates (i.e. no negative voltages need to be supplied). Subthreshold-slopes (SS) below 100 mV/dec are measured over 2 and 4 decades of current for *n*- and *p*-type conduction respectively, as shown in Fig. 2(b-c). Notice how the different biases of the PG only affect the maximum ON current (different barrier modulation at the contacts) without impacting the SS, as the switching of the device is controlled independently by the CG. Fig. 3(a) shows an optical micrograph of the fabricated inverter with the bias and name of all the terminals reported also in the cartoon cross-section view (see Fig. 3(b)). The proper operation of the logic gate is achieved biasing the PG respectively at 0 V and 4 V for the *p*- and *n*-type transistor, while having V_{DD} = 1 and 2 V. The inverter behavior is verified, see Fig. 3(c), for both supply voltages, achieving high inverter gains ($d(V_{OUT})/d(V_{IN})$ > 10 and 50) for V_{DD} = 1 and 2 V respectively.

Conclusions

We study electrostatic doping as an effective alternative to physical and chemical doping. We used ambipolar, un-doped 2D-WSe_2 and thanks to the electrostatic doping of the contacts regions, we fabricate reconfigurable, polarity-controllable devices. We demonstrate high ON/OFF ratios of respectively 10^5 and 10^6 for *n*- and *p*-type operation mode on the same device. For the first time, we show a doping-free complementary inverter, with high-gain realized with a simple fabrication process and a single 2D semiconducting material.

References

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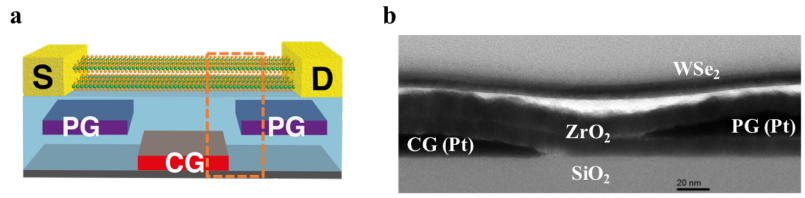

Fig. 1. (a) Cartoon schematic of the fabricated polarity-controllable device showing the position of the overlap between PD and S/D contacts and the underlap between PG and CG. **(b)** Cross-sectional TEM image of the region highlighted in (a), showing the Pt gates, the ZrO_2 dielectric and the WSe_2 channel.

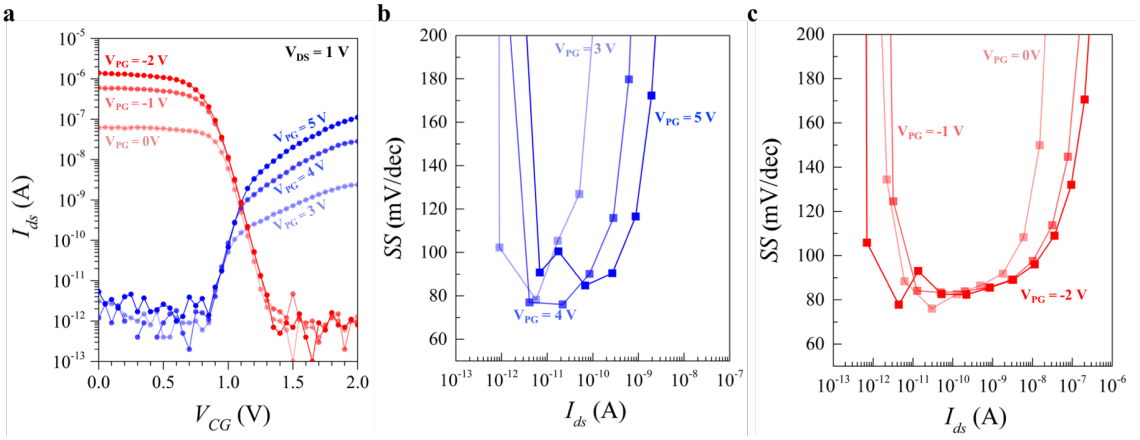

Fig. 2. (a) Transfer characteristics demonstrating polarity controllable behavior. *p*-type (*n*-type) operation is achieved for V_{PG} < 0 V (> 3 V). **(b-c)** Sub-threshold slopes extracted from (a) for *n*- and *p*-type behavior respectively. For both polarities a minimum SS of 80 mV/dec is achieved.

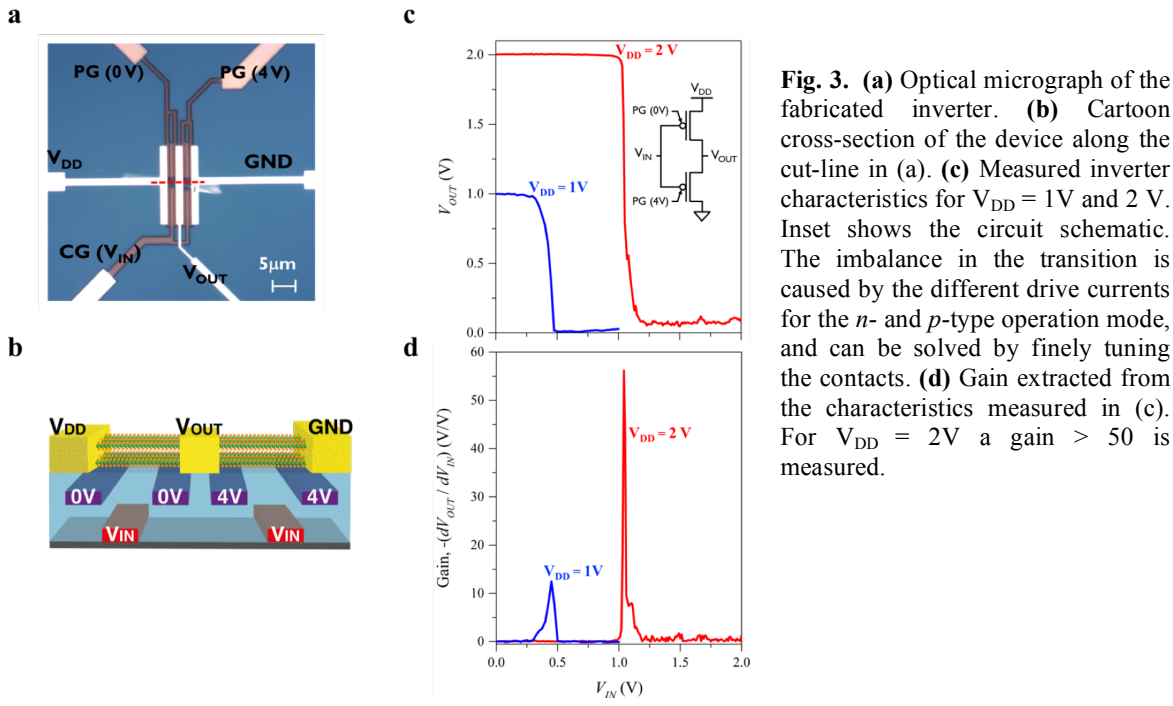

Fig. 3. (a) Optical micrograph of the fabricated inverter. **(b)** Cartoon cross-section of the device along the cut-line in (a). **(c)** Measured inverter characteristics for V_{DD} = 1V and 2 V. Inset shows the circuit schematic. The imbalance in the transition is caused by the different drive currents for the *n*- and *p*-type operation mode, and can be solved by finely tuning the contacts. **(d)** Gain extracted from the characteristics measured in (c). For V_{DD} = 2V a gain > 50 is measured.