645 V Quasi-Vertical GaN Power Transistors on silicon substrates

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***Abstract*—In this paper, we present GaN-on-Si vertical transistors consisting of a 6.7 µm thick n-p-n heterostructure grown on 6-inch silicon substrates by MOCVD. The fabricated vertical trench gate MOSFETs exhibited E-mode operation with a threshold voltage of 3.3 V and an on/off ratio of over 10^8. A specific on-resistance of 6.8 mΩ·cm^2 and a high off-state breakdown voltage of 645 V were achieved. These results show the great potential of the GaN-on-Si platform for the next generation of cost-effective power electronics.**

Keywords—GaN; vertical transistors; GaN-on-Si; power; semiconductor; devices; MOSFETs

I. INTRODUCTION

GaN-based semiconductors and devices have progressed rapidly in the past decades. The dominant III-nitride power devices with a high breakdown voltage are lateral AlGaN/GaN high electron mobility transistors (HEMTs), which have the distinct advantages of polarization charges at the heterointerface to produce a high-density and high-mobility two-dimensional electron gas (2DEG) that effectively reduces the on-resistance and increases the switching speeds of high-voltage devices. However, lateral GaN HEMTs have some limitations for power applications. For example, the threshold voltage (V_{TH}) of most GaN HEMTs is not high enough for fail-safe operation in power systems. In addition, the lateral topology is not suitable for high-voltage and high-current applications. Substantial gate-to-drain spacing is required to achieve high breakdown voltages, which increases the chip size and reduces the effective device current density.

Vertical topology, on the other hand, provides a feasible solution for high-power-density devices. By increasing the thickness of the drift layer, the breakdown voltage can be increased without sacrificing the device size. There have been several reports of high performance GaN-based vertical transistors on freestanding GaN substrates [1-13]. However, the high cost and small available size of bulk GaN substrates limit the wide-spread commercial adoption of vertical power devices on bulk GaN. The GaN-on-Si platform offers a cost-effective alternative for vertical GaN power devices, due to its large-scale availability, low cost, and a mature fabrication technology [14-20].

In this work, we demonstrate quasi-vertical GaN-on-Si vertical transistors based on a 6.7 µm-thick n-p-n heterostructure grown on 6-inch silicon substrates. The fabricated vertical trench gate MOSFETs exhibited E-mode operation with a V_{TH} of 3.3 V and an on/off ratio of over 10^8. A specific on-resistance ($R_{ON,SP}$) of 6.8 mΩ·cm^2 and a high off-state breakdown voltage of 645 V were achieved. The excellent performance can be attributed to the optimized 4 µm drift layer. This excellent performance reveals the great potential of GaN-on-Si to serve as a platform for future power electronic applications.

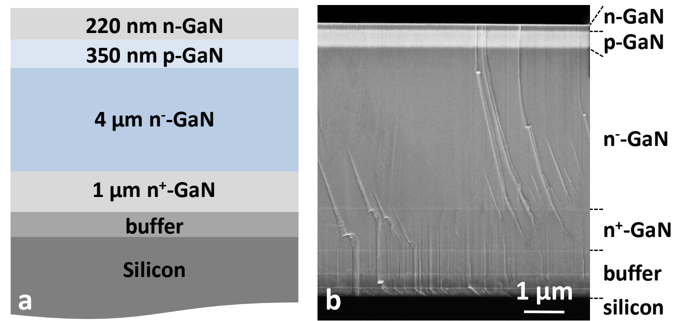

Fig. 1. Cross-sectional (a) schematic, and (b) SEM image of the as-grown n-p-n heterostructure on 6-inch silicon substrates.

II. DEVICE STRUCTURE AND FABRICATION

The n-p-n heterostructure used in this work was grown on 6-inch Si (111) substrates by metal organic chemical vapor deposition system. Fig. 1 (a) presents the schematic structure of the n-p-n structure on silicon substrates. From bottom to top, the n-p-n structure consisted of a 1.1 µm-thick buffer layer, a 1 µm-thick n-type GaN layer (Si dopant concentration ~ 1 × 10^{19} cm^{-3}), a 4 µm-thick n-type GaN layer (Si dopant concentration ~ 2 × 10^{16} cm^{-3}), a 350 nm-thick p-type GaN layer (Mg dopant concentration ~ 4 × 10^{19} cm^{-3}), a 200 nm-thick n-type GaN layer (Si dopant concentration ~ 5 × 10^{18} cm^{-3}), and a 20 nm-thick n-type GaN layer (Si dopant concentration ~ 1 × 10^{19} cm^{-3}). Cross-sectional SEM image in Fig. 1 (b) shows a total epitaxial thickness of 6.7 µm, with an abrupt junction interface. A thick GaN drift layer with high crystalline quality is required to achieve high breakdown characteristics for GaN vertical devices. A 4 µm-thick continuously grown GaN drift layer on silicon was achieved with a low dislocation density of 3×10^8 cm^{-2}, without the use of any interlayer which would significantly degrade the $R_{ON,SP}$. After growth, the wafer bowing was X ~ -57 µm, Y~ -45 µm, indicating excellent strain management of the thick GaN growth.

A schematic process flow is depicted in Fig. 2. The device fabrication started with a plasma-based dry etching process of

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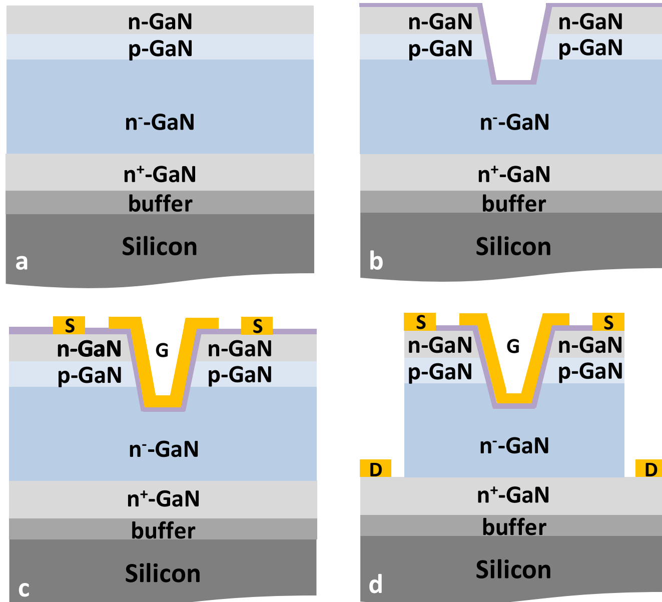

Fig. 2. Schematic process flow for GaN-on-Si vertical MOSFETs, (a) as-grown n-p-n structure on silicon, (b) trench etching and ALD SiO_2 deposition, (c) source contact opening, and gate/source metal deposition, (d) deep etching and drain metal deposition.

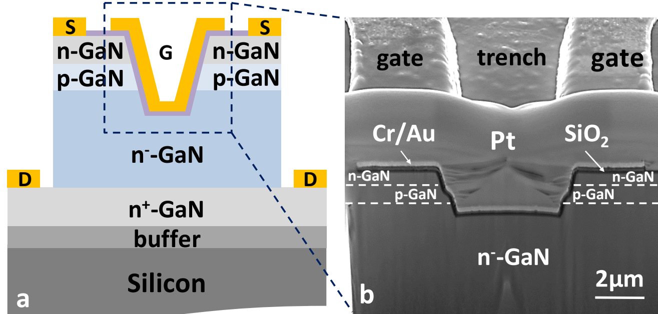

Fig. 3. Cross-sectional (a) schematic, and (b) SEM image of the fabricated quasi-vertical trench gate MOSFETs on Si substrate.

GaN to form the trench structures for the vertical gate. The sample was then treated with a Tetra Methyl Ammonium Hydroxide (TMAH) solution. A rapid thermal annealing was performed at 850°C for 20 min in a N_2 ambient to activate the p-type GaN. Subsequently, a SiO_2 gate dielectric for the vertical MOSFETs was deposited on the top surface and trenches by atomic layer deposition. After opening contact holes, a double-layer metal stack of Cr/Au was evaporated to form both the source and gate electrodes for the vertical MOSFETs. Finally, a 5 µm-deep etching was performed using a ICP etch, followed by the evaporation of drain electrodes. More Details of fabrication can be found in [21].

III. Results and Discussion

Fig. 3 (a) and (b) presents the cross-sectional schematic and SEM image of the GaN-based vertical trench gate MOSFET on silicon substrates. A 1.6 µm deep gate trench can be observed by FIB-SEM. The trench sidewalls were inclined by 13.2° from the c-axis, resulting in a trench width of 4.0 µm and 5.5 µm at the bottom and the top, respectively. Due to the erosion of the edge of the SiO_2 hard mask during dry etching, a small kink

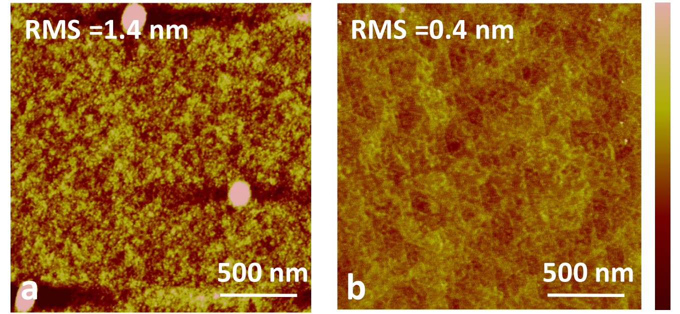

Fig. 4. AFM images of the ICP etched surface (a) without TMAH treatment, and (b) with TMAH treatment.

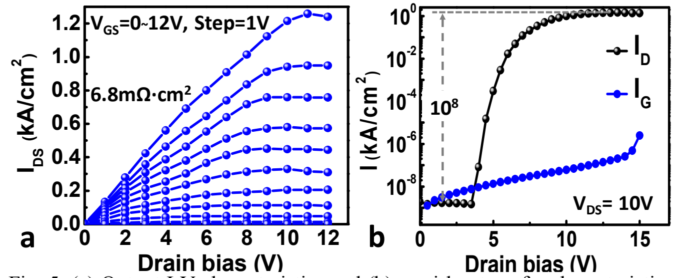

Fig. 5. (a) Output I-V characteristics and (b) semi-log transfer characteristics of the vertical trench gate MOSFETs on silicon substrate.

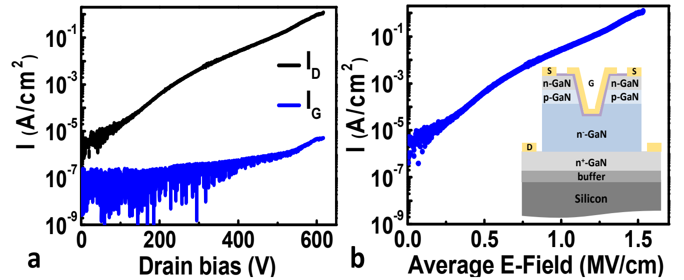

Fig. 6. (a) Off-state I-V characteristics and (b) semi-log plots of I versus E at V_{GS} = 0 V of the vertical trench gate MOSFETs on silicon substrate.

was formed at the middle position of the sidewall. The sidewall and bottom of the gate trench were well covered by SiO_2 gate dielectric and Cr/Au gate metal, which is crucial to obtain a low leakage and low on-resistance vertical trench gate MOSFET.

It has been reported that TMAH wet etch is effective in removing damage from the sidewall and bottom of the dry-etched gate trench, which can improve the conductivity of the inversion channel and eliminate the high electric field peaks at the bottom of the gate region [22]. To investigate the effect of TMAH treatment on the dry etched GaN surface, ICP etching was carried out to remove the top 1 µm layer from the as-grown n-p-n structure, followed by TMAH treatment at 85°C for 60 minutes. Fig. 4 compares the AFM images of the dry etched sample (a) before and (b) after TMAH treatment in an area of 2 × 2 µm². Large dots can be observed on the ICP exposed n⁻-GaN surface, which might be caused by the un-optimized ICP etching conditions. The surface morphology of the TMAH treated sample is dramatically improved with a root mean squire (RMS) roughness of 0.4 nm from 1.4 nm before treatment, indicating that TMAH is effective in removing the dry etching damages and smoothing the etched surface.

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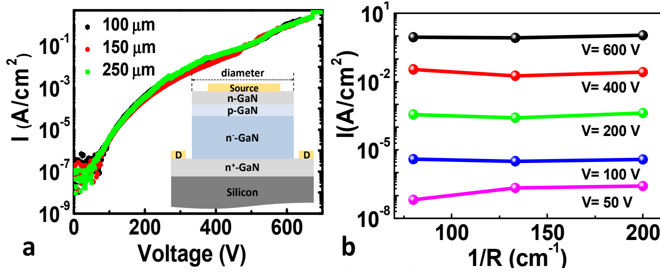

Fig. 7. (a) Two-terminal I-V characteristics of the as-grown n-p-n structure and (b) leakage current density of the two-terminal circular n-p-n test structure with different mesa radius R.

Fig. 5 (a) shows the output I-V characteristics (I_D-V_{DS}) of the fabricated vertical MOSFETs. The $R_{ON,SP}$ calculated from the linear region using the trench area was 6.8 mΩ·cm^2, which could be further reduced by post-trench-etching treatment using a higher concentration of TMAH. At V_{GS} = 12 V and V_{DS} = 11 V, the drain current density of 1.3 kA/cm^2 was obtained, with good saturation behavior. Fig. 5 (b) shows the transfer I-V characteristics (I_D-V_{GS}) of the vertical MOSFETs at a drain-source voltage of 10 V. The fabricated vertical MOSFETs showed a current on/off ratio of over 10^8 and a sub-threshold swing (SS) of 250 mV/dec. A slight increase in gate leakage at V_{GS} = 15 V can be observed, which indicates that the trench etching and gate dielectric deposition can be further improved. A V_{TH} of 3.3 V can be extracted from semi-log scale plots. The high V_{TH} is highly desirable to guarantee a fail-safe operation in high power applications. The off-state leakage current level was below 10^{-8} kA/cm^2, indicating effective current blocking by the n-p-n heterostructure.

Fig. 6 (a) shows the off-state I-V characteristics measured at V_{GS} = 0 V for the fabricated trench gate MOSFETs. A large hard breakdown voltage (V_{Boff}) of 645 V was observed at 2.8 A/cm^2 for the vertical MOSFETs. The breakdown was destructive and mainly observed at the mesa edge regions, which could be improved with edge termination technologies. However, the performance observed even without edge termination is remarkable, which shows the huge potential for GaN on Si vertical transistors. The gate current below 10^{-5} A/cm^2, implying that the drain leakage current originates from a leakage current between the source and the drain contacts. The off-state leakage mechanism was further identified by studying the correlation between leakage current density I and E field. A nearly linear relationship of ln (I) ∝ E was found for the fabricated vertical MOSFETs, as plotted in Fig. 6 (b). Referring to [23], the ln (I) ∝ E linearity indicates that the leakage mechanism is dominated by variable-range hopping for the vertical MOSFETs in this work.

A two terminal breakdown test for the as-grown n-p-n structure was also performed. As shown in Fig. 7 (a), the breakdown voltage of the n-p-n structure (V_{BR}) is ~ 679 V, which is consistent with the MOSFET breakdown voltage. The measured leakage current mainly flows through the n-p-n heterostructures, instead of the etched surfaces. To test this, we have measured the leakage current from two-terminal circular n-p-n test structures with different mesa radius (R = 50 µm, 75 µm, and 125 µm), and found the exact same leakage current density with different radius (no dependence of leakage current density on the mesa periphery in Fig. 7 (b)). This indicates that the device leakage current is mainly through the heterostructure instead of the etched sidewall.

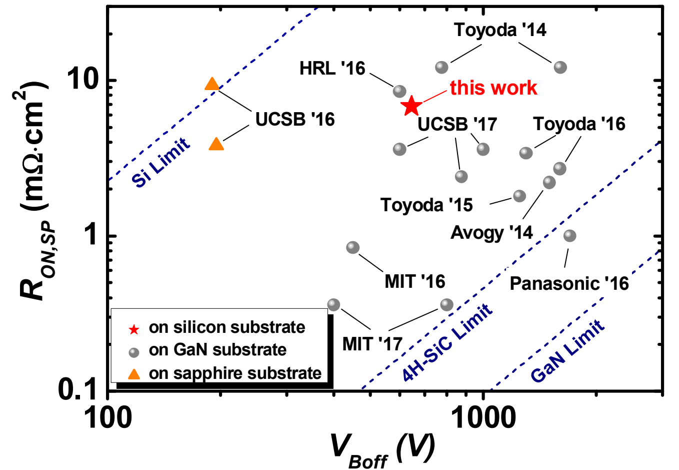

Fig. 8. $R_{ON,SP}$ versus V_{Boff} benchmarks of the vertical trench gate MOSFETs on silicon substrates with state-of-the-art E-mode vertical transistors on sapphire and GaN substrates.

Our GaN-on-Si vertical transistors were benchmarked in Fig. 8 against state-of-the-art E-mode vertical GaN transistors on GaN, and sapphire substrates as a function of V_{Boff}. With a V_{Boff} of 645 V and $R_{ON,SP}$ of 6.8 mΩ·cm^2 , our GaN-on-Si vertical transistors showed a very good Baliga figure-of-merit (FOM) of 61 MW/cm^2. The FOM can be significantly improved by designing field plate and edge termination technologies as well as optimizing the growth and device fabrication.

CONCLUSION

In summary, GaN-on-Si vertical MOSFETs are demonstrated on 6-inch silicon substrates. The fabricated vertical MOSFETs exhibited a threshold voltage of 3.3 V and a specific on-resistance of 6.8 mΩ·cm^2. An off-state breakdown voltage of 645 V was achieved, thanks to the high-quality 4-µm-thick GaN drift layer. These results make this GaN-on-Si vertical MOSFETs very promising for cost-effective and high-performance power electronics applications.

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