Vertical GaN-on-Si MOSFETs with Monolithically Integrated Freewheeling Schottky Barrier Diodes

Chao Liu, Riyaz Abdul Khadar, and Elison Matioli, *Member, IEEE*

Abstract—We demonstrate for the first time the monolithic integration of vertical GaN MOSFETs with freewheeling Schottky barrier diodes (SBD), based on a 6.7-µm-thick n-p-n heterostructure grown on 6-inch silicon substrates by metal organic chemical vapor deposition. The anode of the SBD is integrated in the source pad of the MOSFET and the cathode is directly connected to the MOSFET drain through the bottom n^+-GaN layer, eliminating the need of any metal wire interconnection. This monolithic integration scheme offers reduced footprint, minimized parasitic components and simplified packaging. The integrated MOSFET-SBD showed enhancement-mode operation with a threshold voltage of 3.9 V, an on/off ratio of over 10^8 and a dramatic improvement in reverse conduction, without degradation in on-state performance from the integration of the SBD. The integrated GaN-on-Si vertical SBD exhibited excellent performance, with a specific on-resistance of 1.6 mΩ·cm^2, a turn-on voltage of 0.76 V, an ideality factor of 1.5, along with a breakdown voltage of 254 V. These results reveal the promising potential of emerging GaN vertical devices for future power converters.

***Index Terms* – Gallium nitride, vertical, quasi-vertical transistors, GaN-on-Si, power, semiconductor, MOSFETs, freewheeling, SBDs, diodes.**

I. Introduction

GaN-BASED lateral and vertical devices have emerged as excellent candidates for high-efficiency power converters. While the lateral AlGaN/GaN high electron mobility transistors (HEMTs) continue to penetrate the 600 V -class medium-power electronics market, vertical GaN devices are developed for high-voltage high-current applications. In the past few years, numerous GaN vertical power transistors have been reported on freestanding GaN substrates [1-9]. However, the high cost and small available size of bulk GaN substrates could limit the widespread commercial adoption of vertical power devices on bulk GaN.

GaN-on-Si offers a cost-effective alternative for vertical GaN power devices, due to its large-scale availability, low cost, and a mature fabrication technology. Vertical GaN-on-Si P-i-N and Schottky diodes [10-18], and more recently, the first vertical transistor have been demonstrated on 6-inch Si substrates [19]. For practical use of the emerging vertical transistors in several topologies of power converters, such as buck/boost converters, voltage-source inverters, and resonant converters, an extra freewheeling diode is required to allow a reverse flow of current during off-state [20-22]. The intrinsic body P-i-N diode embedded in GaN vertical MOSFETs could work as a freewheeling diode. However, its large turn-on voltage would increase the losses during switching events. One solution lies on the integration of a Schottky barrier diode (SBD) with the MOSFET, which would be preferable for efficient converter topologies due to its much smaller turn-on voltage, lower resistance, and faster switching properties [23]. Nevertheless, the large parasitic inductance of an externally connected SBD would result in circuit ringing and system instability due to the external wiring. A monolithic integration of these devices would be very desirable for a reduced footprint, smaller parasitic components, and simplified packaging [24]. But so far there have been no reports on GaN vertical transistors with monolithically integrated SBDs.

In this work, we demonstrate the first vertical GaN MOSFET with monolithically-integrated freewheeling SBD on 6-inch silicon substrates. The integrated MOSFET-SBD exhibited enhancement-mode (E-mode) operation with a threshold voltage (V_{TH}) of 3.9 V, an on/off ratio of over 10^8, and a drastic improvement in reverse conduction, without degradation in on-state performance of the MOSFET. The integrated SBD

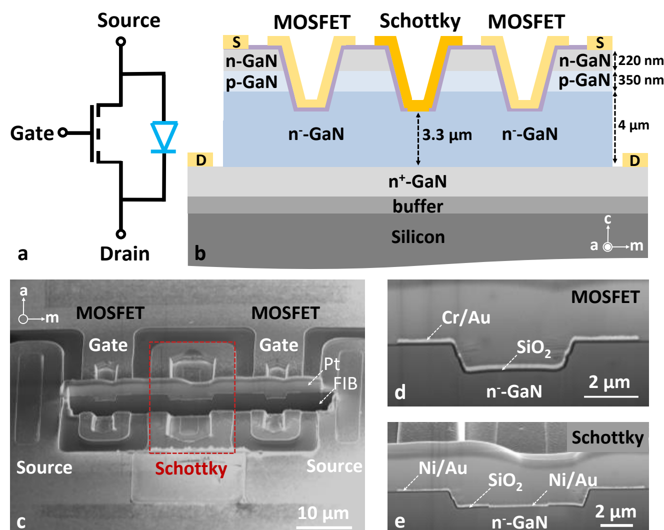

Fig. 1. (a) Equivalent circuit, (b) Schematic of integrated vertical MOSFET-Schottky barrier diode (SBD). (c) SEM image of integrated vertical MOSFET-SBD, (d) Cross-sectional SEM image of the integrated vertical MOSFET, and (e) of the integrated vertical SBD.

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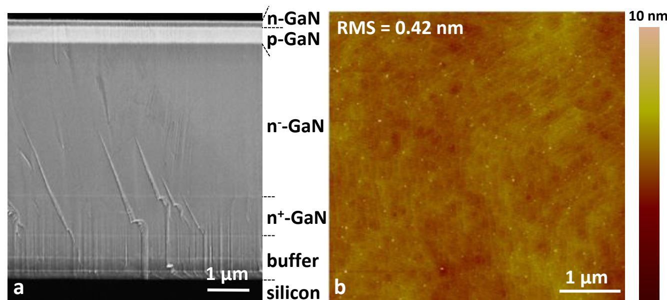

Fig. 2. (a) Cross-sectional SEM image of the as-grown n-p-n GaN structure on 6-inch silicon, (b) AFM image of the Schottky region after dry-etching to reach the n-GaN layer, followed by 25% TMAH treatment at 85 °C for 90 min.

exhibited excellent performance, with a specific on-resistance ($R_{ON,SP}$) of 1.6 mΩ·cm^2, a turn-on voltage of 0.76 V, an ideality factor of 1.5, along with a state-of-the-art breakdown voltage of 254 V compared to vertical GaN-on-Si SBDs. These results reveal the great potential of GaN-on-Si vertical MOSFETs with integrated freewheeling SBD for power converters.

II. Device Structure and Fabrication

Fig. 1 (a) depicts an equivalent circuit of the monolithically integrated vertical MOSFET-SBD, along with a cross-sectional schematic presented in Fig. 1 (b). Both the integrated vertical MOSFET and SBD feature a trench structure along the a-axis of GaN. A tilted-view scanning electron microscope (SEM) image of the integrated vertical MOSFET-SBD is shown in Fig. 1 (c). The etched middle region corresponds to a cross-sectional cut by focused ion beam (FIB). It shows the anode of the SBD integrated in the source pad of the MOSFET, while the cathode is directly connected to the MOSFET drain through the bottom n^+-GaN layer. As a result, the interconnection metal wires between the MOSFET and SBD could be eliminated, leading to a minimized footprint, reduced parasitic components, and enhanced switching speed. Fig. 1 (d) and (e) show the cross-sectional SEM images of the integrated MOSFET and SBD, respectively. The depth of the etched trench was 1.3 µm for both devices, which was sufficient to reach the n^--GaN drift layer. A direct contact of the Schottky metal (Ni/Au) to the n^--GaN drift layer can be observed in Fig. 1 (e), which forms the integrated vertical SBD.

The cross-sectional SEM image of the n-p-n epitaxial structure grown on 6 inch Si (111) in Fig. 2 (a) shows a total thickness of 6.7 µm, with abrupt junction interfaces and a drift layer thickness of 4 µm. The device fabrication started with a plasma-based dry etching process to form the trench structures for the vertical MOSFET and SBD. The samples were then treated with a 25% Tetra Methyl Ammonium Hydroxide (TMAH) solution at 85 ℃ for 90 minutes to smooth the sidewall and bottom of the etched trenches [25]. Fig. 2 (b) reveals the very smooth surface morphology of the trench bottom after TMAH treatment, with a root-mean-square (RMS) roughness of 0.42 nm, which is crucial to achieve good Schottky contacts. More details of the epitaxial structure and fabrication process used in this work can be found in Ref. [19].

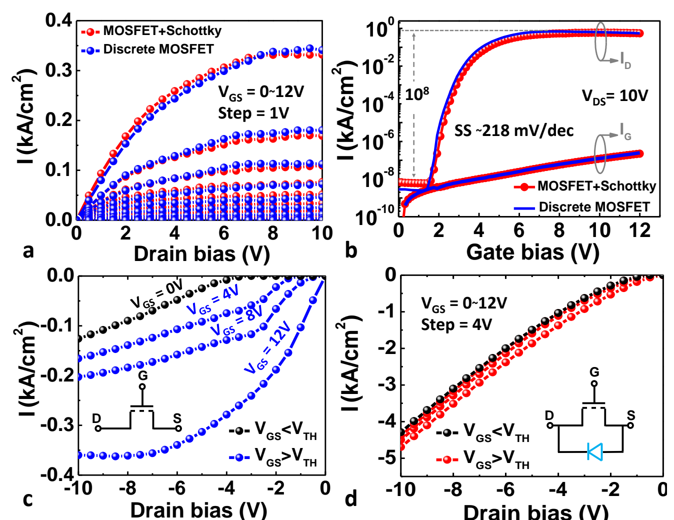

Fig. 3. (a) Output and (b) Transfer characteristics of the vertical MOSFET with/without integrated freewheeling SBD. Reverse-bias characteristics of (c) the discrete vertical MOSFET and (d) integrated vertical MOSFET-SBD.

III. Results and Discussion

The output characteristics (I_D-V_{DS}) of the integrated MOSFET-SBD and discrete reference MOSFET are shown in Fig. 3 (a). Both devices presented good saturation behavior, an on-state current density of ~ 0.35 kA/cm^2, and a similar $R_{ON,SP}$ (10.1 mΩ·cm^2 and 12.6 mΩ·cm^2, normalized by the trench area [26]). The difference in $R_{ON,SP}$ is within the variation observed for devices of the same kind in this wafer. Fig. 3 (b) plots the transfer characteristics (I_D-V_{GS}) of the integrated MOSFET-SBD and discrete MOSFET at V_{DS} = 10 V. Both devices exhibited E-mode operation with a V_{TH} (obtained by linear extrapolation) of ~ 3.9 V, a current on/off ratio of over 10^8, and a sub-threshold swing (SS) of ~ 218 mV/dec. The off-state leakage current level of the integrated MOSFET-SBD is slightly higher as compared to the discrete MOSFET. This can be attributed to the integrated SBD, which is under reverse bias during forward operation of the integrated MOSFET. Despite this, the overall leakage current level value for the integrated MOSFET-SBD was below 10^{-8} kA/cm^2, revealing a very effective current blocking from the integrated MOSFET-SBD in off state. The minor gate leakage increase, from 6 ×10^{-10} kA/cm^2 at V_{GS} = 0 V to 2 ×10^{-7} kA/cm^2 at V_{GS} = 12 V, can be eliminated by improving the quality and conformity of gate dielectric.

Fig. 3 (c) illustrates the reverse characteristics of the discrete vertical MOSFETs. In the on-state ($V_{GS} > V_{TH}$), the current flows through the MOSFET channel from source to the drain with an $R_{ON,SP}$ of 9.5 mΩ·cm^2, comparable to that in the forward conduction. In the off-state ($V_{GS} < V_{TH}$), the current in the MOSFET channel is blocked, resulting in a large V_{ON} of -3.7 V, corresponding to the built-in P-i-N diode, as well as a high resistance in the reverse current path. In this case, a voltage spike could occur during switching, causing arcing on contacts or possibly destroying transistors. The reverse characteristics of the integrated MOSFET-SBD are depicted in Fig. 3 (d). A drastically improved reverse conduction is observed in off-state ($V_{GS} < V_{TH}$), thanks to the integrated anti-parallel SBD. In the reverse condition, the electrons can flow through the drift

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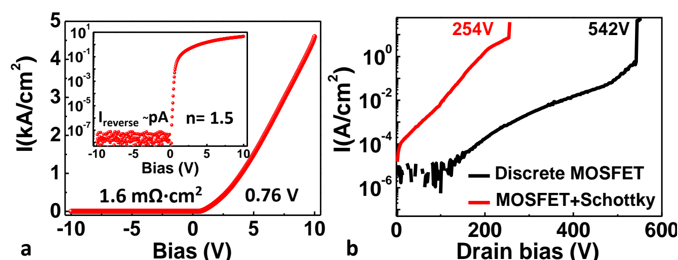

Fig. 4. (a) I-V characteristics of the integrated SBD. The inset shows semi-log scale of the I-V curves, and (b) Off-state breakdown characteristics of the integrated vertical MOSFET-SBD and of discrete MOSFET.

region via the Schottky contacts to the source, even if the channel under the MOSFET gate is pinched-off. In on-state ($V_{GS} > V_{TH}$) of the integrated MOSFET, an additional current can flow through the MOSFET channels from drain to source, which explain the minor gate modulation observed and adds to the forward current of the integrated SBD.

Fig. 4 (a) shows the forward current density (normalized by the anode area) versus voltage (J-V) characteristics of the SBD. The V_{ON}, extracted at a current density of 20 A/cm^2 was 0.76 V, which is among the lowest values reported in vertical GaN diodes so far [27]. The $R_{ON,SP}$ extracted from the forward J-V plot at 8.7 V was 1.6 mΩ·cm^2. The inset plots the forward current density J in logarithmic scale as a function of bias. A small ideality factor of 1.5 was extracted at a forward voltage of 0.4 V, together with an extremely low reverse current, in the range of pA. A combination of such low $R_{ON,SP}$ and good ideality factor is a result of the excellent drift-layer quality with low defect density, high electron mobility [10], as well as excellent Schottky contact formed on the smooth n$^-$-GaN surface subject to TMAH treatment.

Fig. 4 (b) plots the off-state I-V characteristics measured at V_{GS} = 0 V for the discrete vertical MOSFET and integrated vertical MOSFET-SBD. The discrete vertical MOSFETs exhibited a large breakdown voltage (V_{BR}) of 542 V, while the integrated vertical MOSFET-SBD presented a V_{BR} of 254 V, which was limited by the V_{BR} of the integrated SBD. The integrated SBD in this work was benchmarked against state-of-the-art vertical SBDs on silicon, sapphire and GaN substrates in Fig. 5, revealing state-of-the-art performance compared to vertical GaN-on-Si SBDs [17], [18], [27-38]. The V_{BR} of the integrated MOSFET-SBD can be significantly improved: 1. By using low-defect-density GaN substrates [27], [29], [30]; 2. By increasing the drift layer thickness and further reducing the background carrier concentration from 2×10^{16} cm^{-3} in this work to ~10^{15} cm^{-3} [30], [31]; 3. By employing field plate, edge termination, and guard ring technologies [32-34]; 4. By utilizing trench or junction SBD architecture [35-39]. This excellent performance shows the great potential of GaN vertical devices for future power converters.

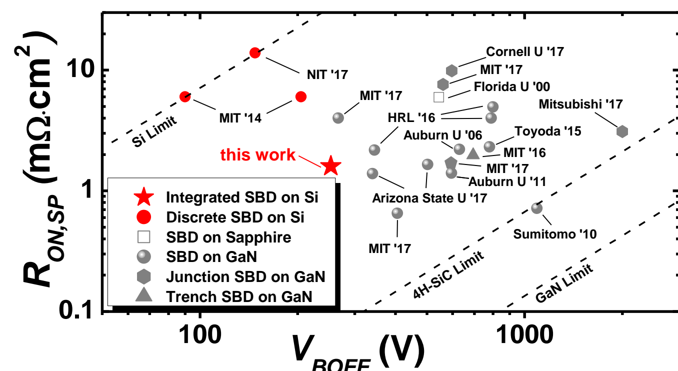

Fig. 5. $R_{ON,SP}$ versus V_{Boff} benchmark of the vertical SBD against state-of-the-art vertical SBDs on Si, sapphire and GaN substrates.

IV. Conclusion

In summary, we have demonstrated the first GaN vertical MOSFETs with monolithically integrated freewheeling SBDs. The integrated GaN-on-Si MOSFET-SBD exhibited E-mode operation with a threshold voltage of 3.9 V, an on/off ratio of over 10^8 and a drastic improvement in reverse conduction, without degradation in on-state performance from the integration of the SBD. These results mark a major step forward for GaN-on-Si vertical transistors for cost-effective high-voltage and high-power electronic applications.

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