High voltage metal oxide thin film transistors to drive arrays of dielectric elastomer actuators

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PAR

Alexis Pierre Henri MARETTE

acceptée sur proposition du jury:

Prof. L. G. Villanueva Torrijo, président du jury
Prof. H. Shea, Dr D. Briand, directeurs de thèse
Prof. S. Seelecke, rapporteur
Dr F. Zanella, rapporteur
Prof. E. Charbon, rapporteur

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Chacun ramasse à terre un caillou, et le jette dans le feu.
Ce caillou s'appelle dès lors : Anaon.
— *Anatole Le Braz*

A la mémoire de mon grand-père, André Marette.

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Neuchâtel, June 21, 2018 Alexis

Abstract

This thesis advances the field of high-voltage thin film transistors (HVTFTs) and dielectric elastomer actuators (DEAs) by demonstrating a strategy for low-voltage addressing of an array of high voltage soft actuators suspended on a flexible substrate.

First, I present the first HVTFTs operating at 1 kV drain-source voltage, switching with an on-off ratio of 20 at 80 V gate-source voltage. The HVTFTs can operate at high voltage thanks to geometrical features increasing the breakdown voltage: a thick gate dielectric composed of a bilayer of alumina (100 nm) and Parylene-C (1 µm), a long semiconducting channel (500 µm), and a 150 µm long non-gated region between the drain and the gate electrode called the offset gate. The use of an amorphous oxide semiconductor (AOS), zinc tin oxide (ZTO), enables a high on-currents of 0.1 mA. The ZTO was synthesized by a sol-gel process after spin-coating on a flexible polyimide substrate, previously passivated with alumina. I optimized the HVTFT switching properties by doping the ZTO layer with yttrium (5%). It improved the on-off ratio up to 1000 at 500 V operation voltage by decreasing the leakage current down to 100 nA.

Then, I show the first integration of HVTFTs with DEAs. My ZTO HVTFTs switch DEAs on and off with only 30 V gate voltage under a bias voltage of 1.4 kV. The system time response in 50 ms. The demonstrator is a 4x4 array of diaphragm DEAs. A layer of 4x4 DEAs is suspended over a layer of 4x4 HVTFTs built on flexible polyimide. The DEAs and the HVTFTs were interconnected thanks to a flexible PCB in a resistive load inverter circuit architecture. A flexible 3D printed chamber was constantly biasing the DEA diaphragms with a back-pressure. The DEAs were made of PDMS and the active region is defined by overlapping carbon-PDMS electrodes. The device operates down to a 5 mm radius of curvature.

Finally, I demonstrate latching of the HVTFT and the DEA by using triboelectric sensors. Under a constant 500 V circuit bias, the control of the HVTFT gate with triboelectric generators enabled 4s latching of the inverter output voltage at 470 V for the off-state and at 120 V for the on-state. The latching of the DEAs with the HVTFT circuit finally proves that this approach can lead to a bistable control of DEAs.

This PhD thesis results show that my HVTFTs are versatile components usable not only to

address DEAs but also to interface low voltage sensors with high voltage actuators.

Keywords: thin film transistors, high voltage, amorphous oxide semiconductor, zinc tin oxide, dielectric elastomer actuators, haptic display, triboelectric generator, electromechanical latching.

Résumé

Les travaux défendus dans cette thèse impactent deux thématiques de recherche : Celles des transistors à films fins de haute tension (HVTFTs) et des actionneurs à élastomère diélectrique (DEAs). J'y présente une stratégie pour contrôler des matrices d'actionneurs souples à haute-tension sur substrat flexible.

Dans un premier temps, je démontre les premiers HVTFTs opérationnels à une tension drain-source de 1 kV. Le rapport de courant on-off est de 20 et la commutation s'effectue sur un intervalle de 80 V à la grille. Quelques optimisations géométriques ont été effectuées, lesdites optimisations entrainant une augmentation de la tension de claquage du HVTFT : J'ai utilisé un diélectrique de grille épais, composé d'une double-couche d'alumine (100 nm) et de Parylène-C (1 µm). Le canal semiconducteur est long, sa taille est de 500 µm et l'électrode de grille a été décalée de 150 µm par rapport au drain. Cette modification est appelée grille en décalage ou offset gate selon la terminologie anglaise. L'utilisation d'un semiconducteur en oxyde amorphe (AOS), l'oxyde de zinc étain (ZTO) comme canal de transistor procure un courant de canal de 0.1 mA à l'état on. Le ZTO a été synthétisé par un procédé sol-gel sur un substrat en polyimide préalablement passivé à l'alumine. J'ai optimisé ce semiconducteur en le dopant avec de l'yttrium (5%). Le rapport on-off s'est amélioré et est monté à 1000 pour une tension d'opération de 500 V et ce, grâce à une diminution des courants de fuite du transistor à 100 nA.

Dans un deuxième temps, je présente la première intégration de HVTFTs avec des DEAs. Mes transistors en ZTO parviennent à commuter les DEAs sur un intervalle de 30 V de tension de grille, sous une alimentation générale de 1.4 kV. Le temps de réponse du système est de 50 ms. Mon démonstrateur est une matrice 4x4 membranes DEAs suspendue au-dessus d'un substrat de 4x4 HVTFTs sur polyimide. Un PCB flexible connecte HVTFTs et DEAs dans une configuration électronique d'inverseur résistif. Une chambre flexible imprimée 3D, permet la mise sous pression constante des membranes actives. Celles-ci sont faites en PDMS et leur région active est définie par deux électrodes étirables en silicone carboné. Le dispositif fonctionne jusque un rayon de courbure minimal de 5 mm.

Dans un dernier temps, je démontre le verrouillage de l'état du HVTFT et du DEA en utilisant

des capteurs triboélectriques. Sous une alimentation constante de 500 V, on peut contrôler la tension de grille des HVTFTs via les dispositifs triboélectriques et verrouiller pendant quatre secondes la tension de sortie de l'inverseur à 470 V lorsque le transistor est bloquant, et à 120 V quand ce dernier est passant. Leur verrouillage par l'intermédiaire du HVTFT et des capteurs triboélectriques démontre que cette approche mène à un contrôle bistable des DEAs.

Les résultats de ma thèse de doctorat montrent que ces HVTFTs sont des composants polyvalents utilisables non seulement pour contrôler des matrices d'actionneurs, mais aussi pour permettre d'interfacer ces derniers avec des capteurs basse tension.

Mots clefs : Transistors film fin, haute tension, semiconducteur en oxyde amorphe, oxyde de zinc étain, actionneur à élastomère diélectrique, écran haptique, générateur triboélectrique, verrouillage électromécanique.

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1 Introduction

1.1 Background and motivation

An actuator is a device generating a mechanical response to an electrical stimulus. To operate systems made of large arrays of actuators such as haptic displays or projectors, integrated drive electronics such as transistors are required to independently control each actuator. This thesis focuses on the development and integration of transistors to address high-voltage soft actuators: dielectric elastomer actuators (DEAs).

DEAs are soft actuators [6] with a unique combination of properties [7, 8]: They actuate fast (< 1 ms time response [9]), are compliant, can achieve high actuation strain (> 100 % [10]) and consume almost no power compared e.g. to electromagnetic actuators. These appealing properties have recently made DEAs an active field of research [6, 11]. DEAs have been applied to several fields including optics, cell biology, energy harvesting and grippers [7, 8, 12, 13]. Several of these applications such as active microfluidic valves [14] or haptics displays [15] require the independent actuation of 10s to 100s DEAs. As an example, a Braille display requires the independent out-of-plane actuation of 6 dots or taxels (tactile pixels) to be able to form every letter of the Braille alphabet. A refreshable Braille text on an A4 page requires the independent actuation of > 1000 DEAs [16].

DEAs typically reach their maximum actuation strain at a drive voltage of several kVs. As a consequence, the circuit required to address a matrix of DEAs has to include power transistors or optocouplers, bulky components preventing any possible integration. Figure 1.1a shows the picture of a high-voltage power supply used to drive and switch on and off a single DEA. We would need 16 similar boxes to switch a matrix of 16 independent DEAs as represented in Figure 1.1c. This solution is unacceptable if we aim at achieving a compact or a wearable device made of DEAs.

The thin-film transistor (TFT) is an interesting compact candidate for addressing actuators. TFTs belong to the family of field effect transistors and were invented by Paul K. Weimer in

1962 [17]. TFTs differ from metal oxide semiconductor field effect transistors (MOSFETs) because their semiconductor is independent from the substrate. The conduction in a TFT occurs indeed in a thin-film semiconductor deposited on an insulator. Originally processed on glass, TFTs are processed today on flexible polymers to address flexible and stretchable sensors [18–20]. Despite being less performant than the standard MOSFET, the TFT was successfully used as a switching elements to address organic light emitting diodes (OLEDs) or liquid crystal display (LCD) matrices [1, 21, 22]. In term of size, a TFT enables a more compact integration of switches than bulky optocouplers and power MOSFETs. However, prior to this thesis, no TFT was reported operating at 1 kV or more.

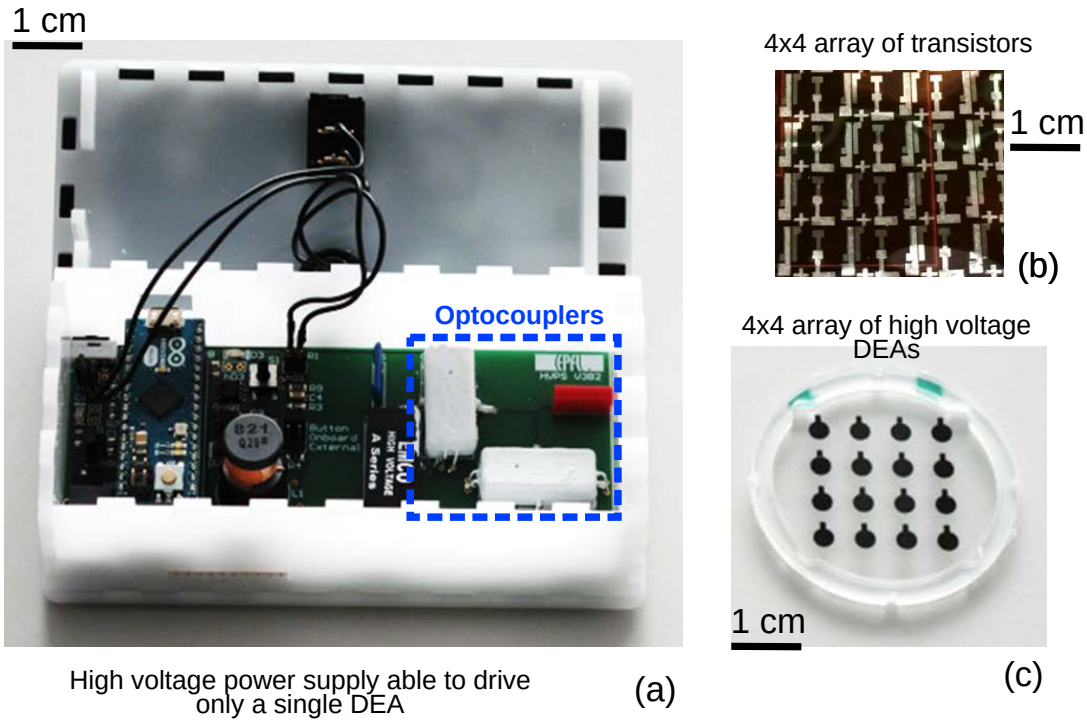


Figure 1.1 – Picture showing (a) a high voltage control box enabling the addressing of 1 single DEA [23].(b) A matrix of 16 compact high voltage thin film transistors used to drive DEAs. Each transistor replaces an optocoupler circuit (taken from the experimental batch that will be presented in the next chapters). (c) An array of 16 DEAs towards a haptic display.

In this thesis, we designed a high voltage thin-film transistors (HVTFTs) matching the high voltage required to drive DEAs. We integrated and demonstrated these HVTFTs with a matrix of DEAs. We also demonstrated that our HVTFTs were able to amplify and treat a sensor signal to drive a DEA. Figure 1.1b shows HVTFTs on foil that we fabricated in the frame of this thesis. Every transistor is more compact than the optocouplers shown in Figure 1.1a and can be integrated and control one DEA such as the ones shown in Figure 1.1c.

1.2 Thesis objectives

This PhD project has been funded by Fond National Suisse de la Recherche Scientifique (FNSNF) grants (Nos. 200020-153122 and 200020-165993). The HVTFTs developed in this thesis respect the following basic requirements:

- The HVTFTs should be able to drive DEAs.
- The HVTFT should be designed, fabricated and demonstrated at a voltage higher than 500 V with a control voltage lower than 100 V, while having a time response enabling operation of DEAs at a frequency higher than 10 Hz.
- A HVTFT matrix should be integrated with an array of 4x4 DEAs.
- The HVTFT should operate under flexure.

1.3 Thesis outline and contribution

In the PhD framework, we designed a HVTFT suitable for DEA addressing and sensor interfacing. This work shows the feasibility of low-voltage addressing of DEAs by removing the need for bulky, rigid and unpractical switches. First, we demonstrated and characterized a 1 kV HVTFT made of amorphous oxide semiconductor (AOS) materials. Then, we showed that DEAs operating at 1 kV can be switched by these integrated HVTFT with a control voltage of 30 V. We built a haptic display demonstrator as a proof of concept (Figure 1.2).

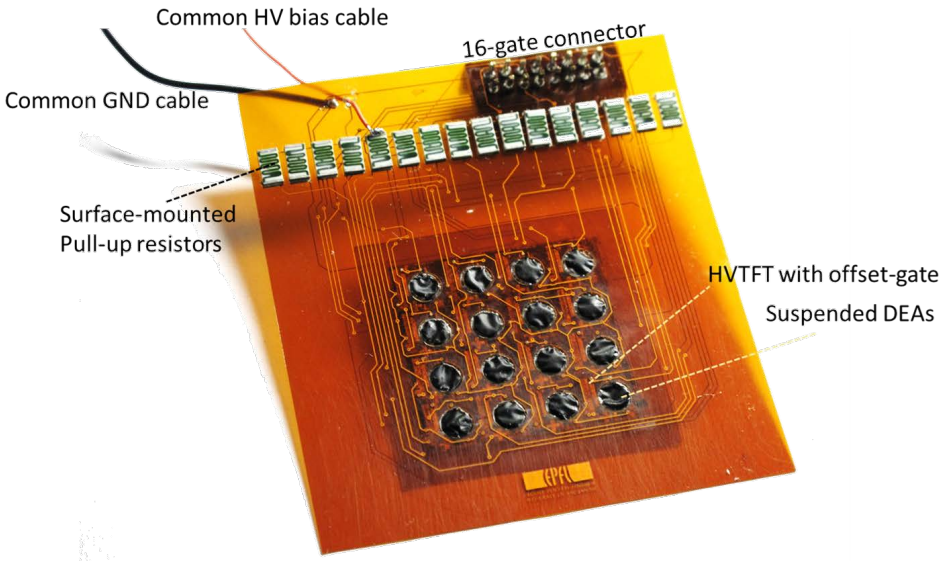


Figure 1.2 – The first DEA-HVTFT machine: a haptic display demonstrator. The 4x4 DEA matrix is addressed by a 4x4 HVTFTs matrix a single high voltage power supply and 16 low-voltage command lines [24].

Finally, we demonstrated a high-voltage flip-flop made of a HVTFT and triboelectric generators to drive a DEA. By demonstrating a novel high-voltage, flexible and compact transistor to address high voltage actuators, this work opens up additional perspectives of research projects (DEAs self-switching and automation, understanding the physics behind HVTFT and printing HVTFTs...), and a path towards novel practical applications for DEAs (Compact Braille displays, articulated soft locomotion robots...).

State of the Art

The first two chapters of this thesis cover the fundamentals of HVTFTs and provide an introduction to DEAs and their applications.

Chapter 2 introduces the field of DEAs, summarizes the underlying actuation principles and presents several applications of DEAs where HVTFTs addressing is a critical addition.

Chapter 3 summarizes the working principle of TFTs. It presents the typical semiconductor channel technologies available for TFTs. We report state-of-the-art HVTFTs technologies and we show that metal oxide HVTFT technology is the most promising to achieve high performance HVTFTs.

High-voltage thin film transistors design and characterization

Chapter 4 presents the design requirements and defines a concept for our HVTFT. The HVTFT constraints are defined relatively to its integration with the DEA in a resistive load inverter configuration. We select an AOS semiconductor, zinc tin oxide as the channel semiconductor to achieve high performance, tunable devices. To operate at high voltage, a gate dielectric composed of a bilayer of alumina and Parylene-C and an offset gate geometry are chosen. We conclude this chapter by describing the entire HVTFT architecture.

Chapter 5 presents the fabrication and demonstration of zinc tin oxide (ZTO) HVTFTs. The process developed to design HVTFTs is described. Then, the semiconductor synthesis, has been extensively studied with various material characterization methods including thermogravimetric analysis (TGA) coupled with differencial scanning calorimetry (DSC), X-ray photoelectron spectroscopy (XPS) and X-ray diffraction (XRD). Then, we discuss the HVTFTs electrical characteristics. The fabricated HVTFTs can operate up to 1 kV, have an on-off ratio of 20, high 100 µA on-current and no charge hysteresis. We present and discuss a LT-Spice circuit model for the HVTFT. Afterwards, we show an optimization for the HVTFTs by yttrium doping. The drain-source leakage current drop from an order of magnitude to 100 nA. We conclude this chapter by presenting a route for optimization of the zinc tin oxide (ZTO) semiconducting properties by yttrium doping.

Integration of HVTFTs to address dielectric elastomer actuator arrays

Chapter 6 describes the integration of HVTFTs with a matrix of out-of-plane DEAs similar to a haptic display. First we show the design and the fabrication of DEA diaphragms for out-of-plane actuation. The DEAs operate at a maximum voltage of 1 kV. Afterwards, we demonstrate and characterize the first integration of an array of DEAs with HVTFTs. The DEA actuate under a circuit bias of 1.4 kV and a gate voltage swing of 30 V. We conclude this chapter by demonstrating the device operation under static bending down to 5 mm radius of curvature.

Sensors and flip-flop made of HVTFTs and triboelectric sensors to drive DEAs

Chapter 7 presents how the HVTFTs can be used as intermediate components to amplify and treat a low-voltage sensing signal to a DEA. We present how the use of triboelectric generators (TrEGs) can bias the HVTFT gate, and thus generate the 30 V gate voltage signal required to switch a 1 kV DEA on and off. We show the control of HVTFT drain-source current with a bending TrEG and we demonstrate actuation of DEA with this methodology. Then we demonstrate a high-voltage flip-flop made of two triboelectric sensors and one HVTFT: We demonstrate the bistable latching of the HVTFT and of the DEA by triggering the two parallel triboelectric sensors. This last chapter opens a path towards fully automated and integrated DEAs.

1.4 Impact of this thesis

This thesis advances the field of HVTFTs by introducing the first zinc tin oxide HVTFT operating at 1 kV. It also shows the first practical application of HVTFTs at a bias voltage > 500 V.

This thesis also advances the field of DEAs by showing the first compact addressing of a 4x4 DEA matrix with an active array of 4x4 HVTFT. The low voltage required to switch the DEAs, 30 V, is more than 30 times lower than the driving voltage of the DEAs (1 kV).

Finally this thesis advances the field of DEA systems and automation by demonstrating that triboelectric sensors be used to modulate the HVTFT gate voltage to control the DEA actuation. The HVTFT makes possible the transfer of the triboelectric signal to the DEA actuation signal. Also, the combination between triboelectric sensors and HVTFTs can lead to logic gates able to drive DEAs.

2 Dielectric elastomer actuators

Summary

In this chapter, we describe the dielectric elastomer actuator (DEA), an electrostatic actuator converting an applied electric field into a mechanical strain.

We start by defining the DEA and its properties. We illustrate the DEA appealing properties, compliance, high strain and high speed with practical examples. Then, we describe the DEA operation modes, in-plane expansion and out-of-plane compression.

Afterwards, we present the working principle of the DEA actuation. We discuss how the DEA actuation stress and strain relate to the applied voltage. Then, we briefly discuss typical failure mechanisms of DEAs.

After that, we describe typical elastomer membrane materials. We compare the specific advantages of polydimethylsiloxane (PDMS) membranes and VHB acrylic membrane. Then we discuss the different conductors usable to fabricate the stretchable electrodes of DEAs.

Finally, we discuss two examples of applications exploiting DEAs devices, which require addressing: haptic displays and soft robots. Haptic displays require the individual addressing of 100s of DEAs and more than 1000 in the particular case of Braille displays [16]. In the case of soft robots, individual controls of multiple actuators would enable soft locomotion with articulated arms and soft grippers with multiple degrees of freedom. These two examples show how the implementation of integrated high-voltage transistors is necessary to achieve compact complex DEA machines.

2.1 Definition and properties of the DEA

In this section, we present the concept of DEAs. The DEA is first defined. Then, its qualities (compliance, speed, high strain and low power consumption) are described with concrete examples.

2.1.1 Basic structure and definition

A DEA is a soft actuator composed of a dielectric elastomer straining under the application of a high voltage, typically several kVs [6, 11]. A DEA includes three main structural elements, one dielectric elastomer membrane with a thickness typically in the order of tens of µm and two stretchable electrodes. Each electrode is respectively patterned on the top and the bottom surface of the membrane. The active area is the region were both electrodes overlap. The application of a voltage leads to charge accumulation in the active region, which creates an electric field leading to an electrostatic pressure exerted by the electrodes. The membrane responds by compressing out-of-plane inducing in-plane expansion because of elastomer incompressibility (see Figure 2.1).

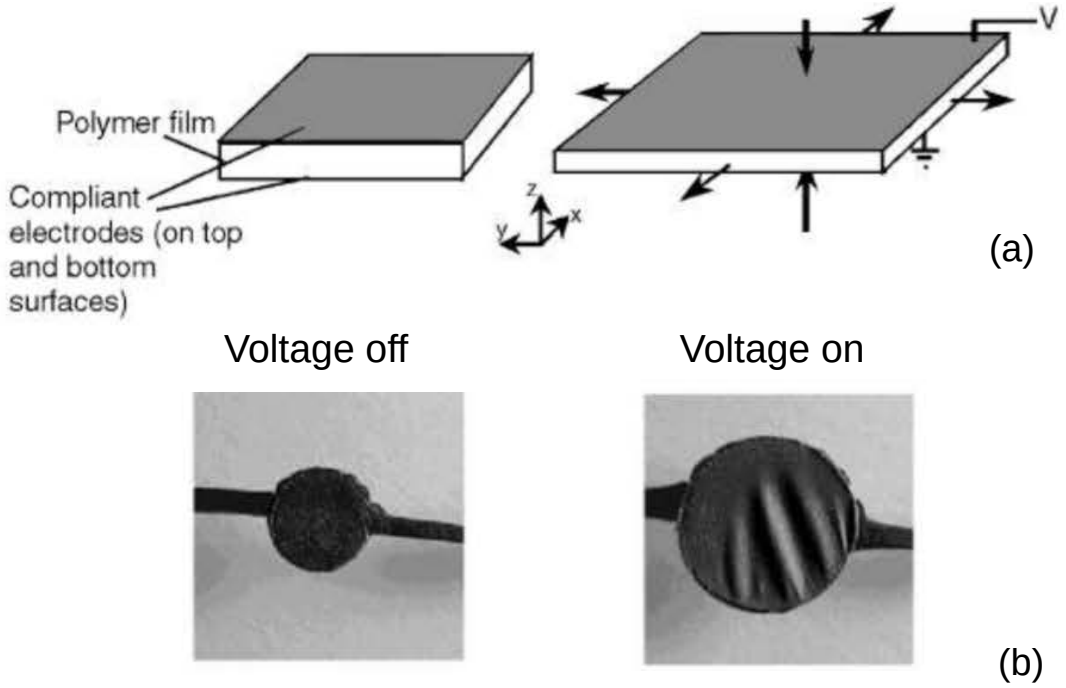


Figure 2.1 – (a) Description of a DEA structure and of its actuation principle. (b) Top view picture of the in-plane expansion of a DEA under a voltage bias. When a voltage is applied across a dielectric elastomer, the charges accumulating in the active region induce a compressive stress leading to in-plane expansion of the actuator (Adapted from [25]).

2.1.2 DEAs, high strain, compliance and high speed actuators

DEAs have a lot of interesting properties, among which the ability to actuate at high strain and high speed with compliant structures.

DEAs are able of very high strain. Figure 2.2a and b show the example of a DEA straining in-plane by 488 % [26] under the application of 3.9 kV. In order to achieve a very high deformation, the DEA had to be prestretched with a dead load of 25.5 g to avoid electromechanical instability (see section 2.2 for the detailed mechanism and the working principle of DEAs actuation). The highest strain achieved by DEAs with an acrylic elastomer membrane has been reported to be 1692 % area strain [27]. It consisted in a bubble DEA that was prestretched with a backpressure of 18 mbar. The highest strain reported for silicone based DEA in the order of 80% linear strain [28].

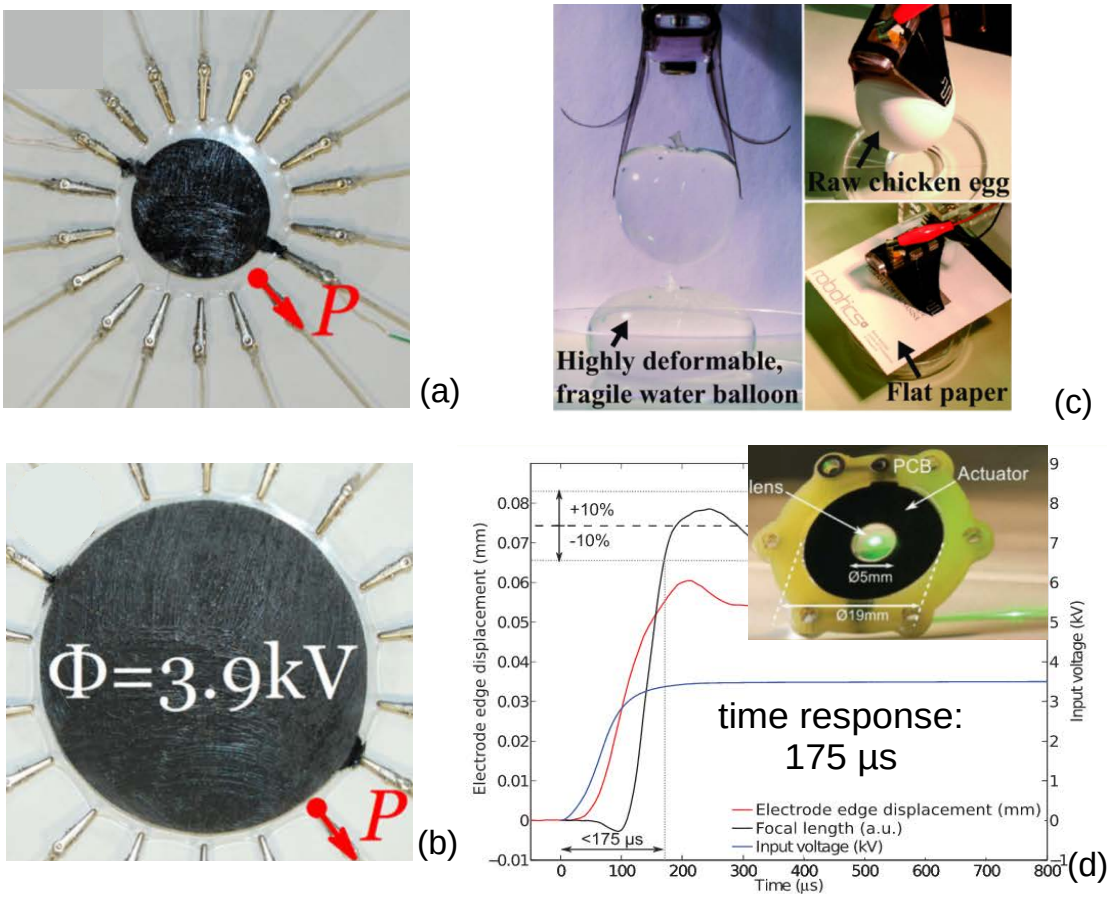


Figure 2.2 – Picture of a DEA (a) idle and (b) actuated with an in-plane actuation area strain of 488 % under the application of 3.9 kV (adapted from [26]). (c) DEA based gripper. The compliance of the DEA enables it to adapt and grab a wide variety of surfaces(adapted from [29]). (d) A DEA tubable lense and its transient characteristics showing an actuation response time of 175 µs (adapted from [9])

A key quality of DEAs is also their speed. It is highly dependent on the dielectric elastomer membrane material. Silicone membrane DEAs are the fastest polymer-based actuators. The time response for such devices has been reported to be less than 200 µs. Figure 2.3d presents the transient characteristics of an active lens made of DEAs [9]. The actuator time response has been reported to be 175 µs and to be able to operate at 4.7 kHz. A similar device made with acrylic DEAs can operate only up to a few Hz. The higher time response are due to the losses induced by the viscoelasticity of the acrylic elastomer.

DEAs are also compliant structures because they are made of stretchable polymers of low Young's moduli, typically in the order of 1 MPa. They can be suspended on both rigid or flexible frames depending on the application. The DEA compliance makes the actuator practical for applications related to flexible grippers [29–31], as the actuator can cover and adapt to a variety of shapes of an object more efficiently than rigid grippers. In the case of the DEA gripper, presented in Figure 2.2d, the actuation was combined with electro-adhesion to generate sufficient force to grip objects.

2.1.3 Operation modes

DEAs can operate either in surface expansion or in thickness compression mode. Actuators used in surface expansion mode can generate large actuation strain and actuators in thickness compression mode can generate high forces.

Figure 2.3 describes different applications achievable with surface expansion actuation of the DEA. Different motions can be achieved with the constraints applied on the DEA active region. When the active region can move freely without constraints (see Figure 2.3a), we are in planar expansion mode. Prestretching the membrane along a single axis leads to uniaxial strain deformation when the DEA actuates. This operation mode has been used e.g. for biological cell-stretcher [12, 28]. Figure 2.3a shows a cell-stretcher made of two parallel in-plane DEAs actuating simultaneously and the strain-voltage characteristics of the device [12]. They have been prestretched mostly along the x-direction to lead to an uniaxial actuation along the y-direction. When the actuators actuate, they strain the gap in-between e.g. in order to strain cells on top of it.

Constraining the active region of the DEA in a rigid frame prevents the DEA of moving in plane, which leads to vertical deflection of the actuator. The actuators are then operating in buckling or vertical deflection mode. Bubble DEAs were demonstrated using this principle [15, 16, 24, 27, 32, 33]. Figure 2.3b) shows a DEA deflecting more than 500 µm out-of plane with a bias voltage of 2500 V [32].

Constraining a uniaxially prestretched DEA on a flexible frame leads to the bending of the entire structure. The actuators are then operating mode and are called dielectric elastomer minimal energy structures (DEMES). This structure is used in soft robotics for grippers [29–31] and walking robots [34]. A variety of other operation modes such as zipping [35] and springroll

DEAs [36] are also achievable.

The compression mode of DEAs is used in structures requiring a high-force DEAs. The problem of operation mode is the small out-of-plane displacement it generates. To increase the vertical displacement, DEAs can be stacked as shown Figure 2.4 [36–38].

Figure 2.4a and b shows the picture of DEA with stacked architectures used to lift weights when contracting [37]. These DEA are made of 400 layers of 1.6 cm diameter acrylic circular DEAs stacked together. The DEA could lift a 2 kg weight and block a 20 N force while weighing only 4 g and contracted 10 %. Stacked structures were used eg for microfludic valves [39] and haptic display [38] applications.

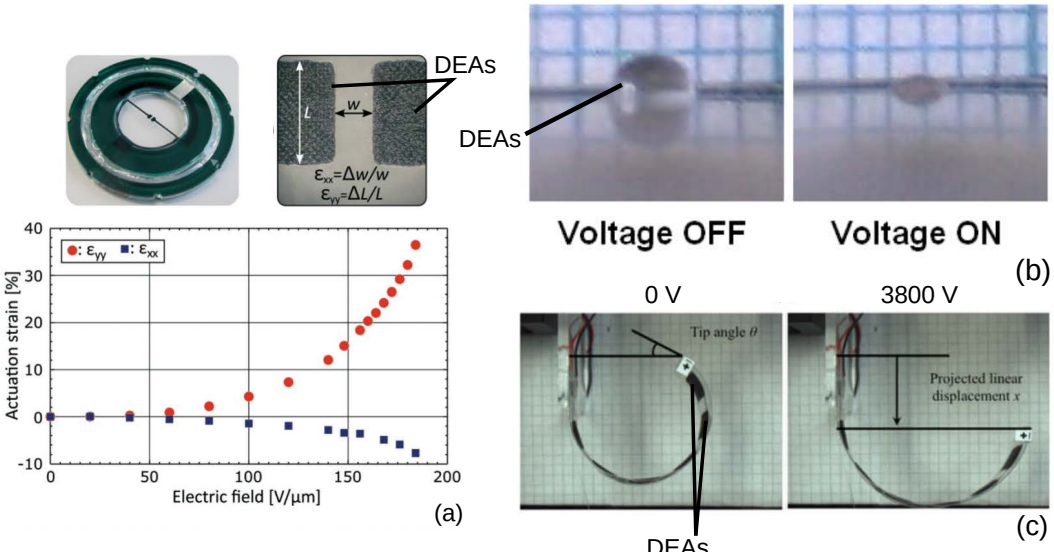


Figure 2.3 – Picture and actuation characteristics of DEAs operating in surface expansion mode. (a) Actuator operating in planar expansion used for cell-stretching. The uniaxial prestretch orientates the strain direction as shown in the strain electric field characteristics. (adapted from [12]) (b) Out-of plane actuator operating like a taxel with transparent electrodes (adapted from [32]). (c) Bending actuator operating for gripping. (adapted from [30])

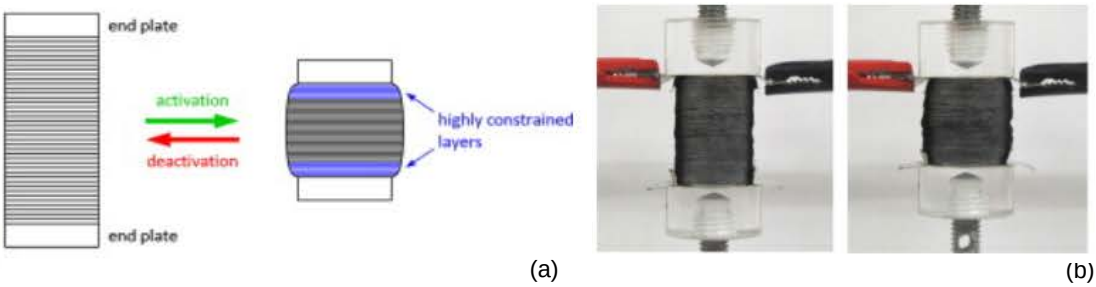


Figure 2.4 – Picture and actuation of DEA devices operating in compression mode. Stacked DEA (a) working principle and (b) pictures of actuation. (adapted from [37]).

2.2 Working principle

2.2.1 Dielectric elastomer actuation

As we already mentioned, the DEA membrane is typically made of acrylic or silicone elastomers. These materials are hyper-elastic polymers. We call λ_{DEA}, the in-plane stretch of the DEA membrane. The stress-strain relationship of the membrane is increasing non linearly until saturation when approaching a stretch value $\lambda_{DEA} = \lambda_{lim}$, where the polymer stiffens and no further extension is possible [10, 40]. The stress-strain relationship of hyperelastic materials can be approximated such as the Neo-hookean model, good for small deformation (stretch < 1.2) of hyperelastic materials, or the Gent model [41], which additionally takes into consideration the limit stretch of the hyperelastic membrane.

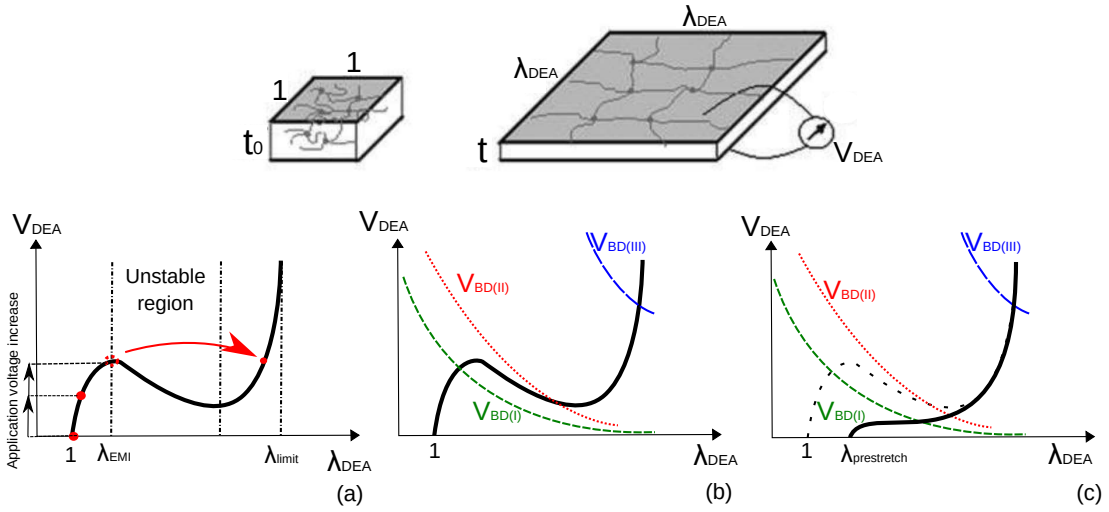


Figure 2.5 – (a) Voltage-stretch characteristics of a DEA without initial prestretch. Three regions in the curves can be identified: First, the monotonous increase of the stretch with applied voltage until a critical stretch λ_{EMI}. Then the DEA "snaps-through" and the stretch increases until a new stable value, where the increase of voltage leads again to a monotonous increase of the stretch until the limit stretch defined by the elastomer material λ_{limit} or the DEA breakdown field. (b) Dielectric breakdown curves of three different types of elastomer materials are superimposed with previous plot. Type I elastomers, break down after low electromechanical stretch (typically less than 1.1). Type II elastomers break down, when the DEA snap through and the type III survives the snap through and break down at very high stretch values. (c) Plot showing the effect of prestretch of the elastomer membrane on the stretch voltage characteristics of a DEA. The electromechanical instability region disappears and the stretch increases monotonously with the actuation voltage, enabling actuation at very high stretch values for type II and type III materials (adapted from [40])

.

As the compressive electrostatic stress σ_z can be connected to the stretch of the dielectric elastomer [6, 40], it is possible to plot the relationship between the stretch of the DEA and the

voltage applied across the DEA. σ_z can be expressed as a function of the applied electric field E or voltage V by Maxwell's equation [11]:

$$\sigma_z(\lambda) = \varepsilon_m \varepsilon_0 \cdot E^2 = \frac{\varepsilon_m \varepsilon_0}{t_m^2} \cdot V_{DEA}^2 \tag{2.1}$$

Where ε_m is the relative permittivity of dielectric elastomer, t_m is the membrane thickness and ϵ_0 is the vacuum permittivity constant.

Figure 2.5b adds up to the stretch voltage relationship of the previous graph the breakdown curves for three different types of elastomers. To calculate the strain-breakdown voltage relation, we have to first consider that an elastomer is incompressible, which means that the product of the stretch along every direction of space is equal to 1:

$$\lambda_x \lambda_y \lambda_z = 1 \tag{2.2}$$

In case of equibiaxial actuation strain:

$$\lambda_z = \frac{1}{\lambda_x \lambda_y} = \frac{1}{\lambda^2} \tag{2.3}$$

where λ is the lateral stretch. The breakdown voltage can be expressed as a function of the compressive stretch λ_z and the initial thickness of the DEA membrane:

$$V_{bd} = E_{bd}\, t = E_{bd}\, t_0 \lambda_z = \frac{E_{bd}\, t_0}{\lambda^2} \tag{2.4}$$

For the type I the DEA breaks down at $\lambda < \lambda_{EMI}$. The type II breaks down as soon as the stretch becomes equal to λEMI. The type III breaks down in the region beyond the second stable point $\lambda_{DEA} > \lambda_{giant}$. This last type leads to the highest stretches and is responsible for the giant actuation reported [10, 27].

The key to very high and continuous actuation of DEAs is the removal of the electromechanical instability phenomenon. The solution is either to prestretch it [40] or to densify the polymer with interpenetrated polymer networks [42]. As shown in Figure 2.5c, the bump in the stretch-voltage characteristics disappear and the voltage stretch function increases monotonously, meaning that continuous actuation until dielectric breakdown is possible.

2.2.2 Actuation of DEAs under a low strain

In this PhD thesis, the DEAs are all operating at low strain (< 20 %). In this strain range, the stress-strain relationship of the DEA can be considered as linear [6] if we neglect the stiffening impact of the DEA electrodes [43]. For a Young's modulus Y_m the compressive strain s_z can

therefore be expressed as, based on Equation 2.1 [6]:

$$s_z = -\frac{\varepsilon_m \varepsilon_0}{Y_m t_m^2} \cdot V_{DEA}^2 \tag{2.5}$$

2.2.3 Failure mechanisms

DEAs have three major failure mechanisms, the dielectric breakdown, the material rupture and the loss of mechanical tension [44]. Dielectric breakdown occurs when the electric field across the dielectric membrane reaches the dielectric strength or breakdown field of the membrane (see before and Figure 2.5b). Electronic charges bypass the membrane and a current is created through the membrane, irreversibly destroying it. The loss of mechanical tension occurs when the reaction force from the passive area of the membrane cannot accommodate for the in-plane expansion of the active area. The membrane relaxes and locally buckles, and no in-plane expansion happens anymore.

2.3 Materials for DEAs

In this section, common materials used to fabricate DEAs are presented. First, we describe typical materials for the elastomer membrane and then, we discuss conductive stretchable electrodes for the DEA active area.

2.3.1 Elastomer membrane

For maximizing in-plane strain, dielectric elastomer membranes need ideally to have a high breakdown field and a low Young's modulus in the order of 1 MPa or lower according to Equation 2.5. Beyond some marginal cases [15, 45], most DEAs are made in acrylic and in silicone elastomers.

Acrylic elastomers are usually made in Very High Bond (VHB), a commercial adhesive from $3M^{TM}$. VHB is a very interesting material as its combination of low Young's modulus and high breakdown strength makes it capable of the highest strain reported for DEAs up to date (up to 1690% area strain [27]). However, VHB has several drawbacks. VHB being a commercial product only available in pre-fabricated thin films, the thickness of one VHB membrane cannot be directly tuned. In addition, VHB is very viscoelastic leading to higher actuation time-constant [9]. The creep of a VHB membrane induces progressive relaxation of the pre-stretch preventing any long-term usage of acrylic DEA [46, 47].

These main limitation are the causes of the increase of popularity of silicone elastomers as membranes for DEAs. Silicone membranes lead to actuators with less actuation strain (up to 80% [28]) than VHB, but are excellent at solving the limitations of VHB DEAs. PDMS can be fabricated from commercial solutions and membranes thickness can be accurately tuned, while processing it, thus enabling calibration of the maximum DEA operation voltage [48]. PDMS has a very low viscoelasticiy and the absence of creep removes tension loss under prestretch and after actuation, enabling long-term usage for millions of cycles [49]at a very high frequency > 1kHz [9], making silicone DEAs applicable for vibrational applications. PDMS can either be selected from commercial pre-fabricated membrane (eg [50]) or in solution form, combining two elements, the silicone solution and its cross-linker (eg [51]). From a solution-form PDMS, membranes can be fabricated by blade-casting [48, 52], spray-coating [53], spin-coating [54], stamping [43] to achieve thicknesses varying from 100s of nm to 100s of µm.

2.3.2 Stretchable electrodes

In order to actuate, DEAs require stretchable (at least 10 %) electrodes able to adhere well on the elastomer membrane with limited stiffening impact. Also, to avoid the DEA response time to be limited by its charging time constant, the RC time constant combining the resistance of the DEA stretchable electrode and the capacitance of the actuator has to be low. Typically, the values of the capacitance of DEAs is between 10 pA and 1 nA, which means that the electrodes

should induce a resistance lower than 1 MΩ to enable at worst a RC time constant of 1 ms. Most conductive stretchable electrodes available for DEAs have been reviewed in [55, 56]. Several works report electrode materials such as hydrogels [57], ionogels [58] but most of the actuators are either metal based or carbon based. Metal based electrodes have very low sheet resistance but highly impact DEA actuation by stiffening [55] and, as thin film of continuous material, crack at very low strain [56]. To avoid this, metallic stretchable electrodes can be obtained from thin film pattering on corrugated membranes [55], nanolayer ion implantation [33], and nanowires [59]. As an example, 10 nm implanted gold electrodes in 30 µm PDMS membranes have been demonstrated [33] for a sheet resistance between 100 Ω and 1 kΩ per square. The implantation of gold electrodes multiplies the Young's modulus of the membrane from 1.5 to 5, decreasing thus the actuation performance [33]. Silver nanowire electrodes can achieve 16 Ω per square [60].

Carbon based material are the most used to fabricate dielectric elastomer actuators electrodes. Various forms of carbon electrode DEAs have been reported such as carbon powder [49, 55], carbon grease [49, 55], carbon loaded PDMS [52, 55], graphene [61] and carbon nanotubes [62]. Carbon nanotube electrodes can lead to very conductive thin films and very thin membranes can be achieved without a negative impact on the DEA speed. Carbon nanotube in polymer nanolayers enabled a resistance of 0.1 kΩ per square [55]. The main advantage of carbon grease and powders DEAs is the minimal stiffening impact on the elastomeric membrane. Carbon powder is difficult to handle as it is very sensitive to static electric fields, and is challenging to manipulate except if encapsulated in an additional silicone film [55]. However, as they are in powder and grease form the electrodes are subject to abrasion after several cycles, making these materials unpractical to design long-term devices. Carbon loaded PDMS solves the problem of abrasion, as the carbon black particles are encapsulated in a crosslinked PDMS matrix. The dispersion, in solution form can be deposited on the membrane by various means such as pad-printing [52], blade-casting [63], screen-printing [64], spray-coating [65] and the thickness obtained by these methods is often in the order of 1 or 2 µm. Carbon grease, powder and elastomer have sheet resistances in the order of 10s kΩ per square.

2.4 Example of DEA applications requiring integrated addressing

Among the DEA applications, several require more the control of 10s to 1000s actuators to operate. Up to now these applications have required bulky external circuits to operate. To achieve compact devices an integrated high voltage switch driving the DEA is a critical building block that has been missing up to now.

In this section, we present two examples of such applications, haptic displays and soft robots, that would take advantage of integrated high-voltage control addressing.

2.4.1 Haptic displays

A haptic display is a display composed of 10s to 1000s of tactile pixels, often refered as taxels. Each taxel is an actuator providing a tactile information to a user. It can be a dynamic information such as a vibration (e.g. provided by a piezoelectric actuator) or a a static bump such as a Braille dot (e.g. provided by an out-of-plane actuator at mechanical equilibrium).

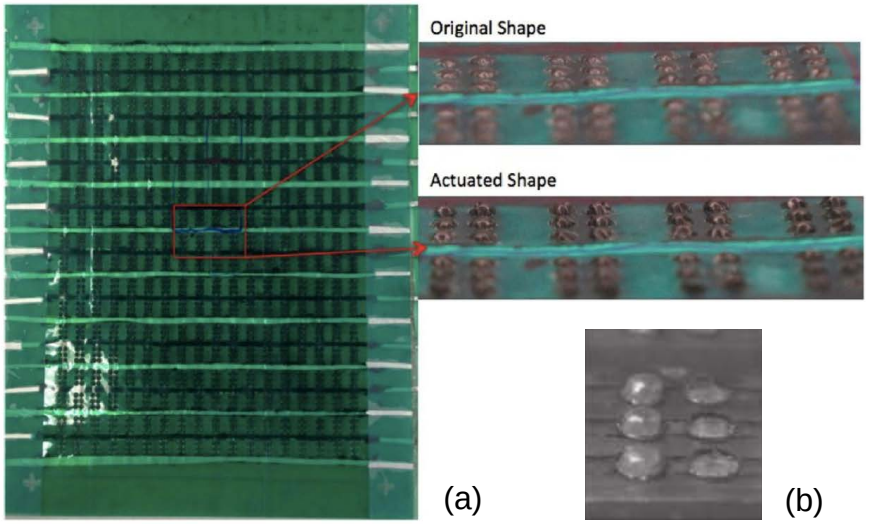


Figure 2.6 – (a)Haptic display made of more than 1000 DEAs. (b)Picture of an "l" in the Braille alphabet a DEA based haptic display. Each dot requires independent addressing so that every group of 6 dot can form every letter of the Braille alphabet.(Adapted from [15, 16])

Active braille sheets, in particular, can be an interesting application of out-of-plane DEA. A Braille display requires a refreshing rate < 100 ms, a force > 150 mN at a vertical displacement > 250 µm and its taxels have to operate after 10^7 cycles [66]. A DEA-based braille display can take advantage of the actuator's high refreshing rate, the flexibility, the high cycle lifetime and vertical displacement > 100 µm.

Figure 2.6 reports a braille display based on DEA and bistable electroactive polymer technology [15] reported in 2014. The actuation of one dot generates a displacement > 500 µm. It includes

324 Braille cells, i.e. 1944 actuators requiring individual driving, motivating thus the need of integrated high voltage switches instead of bulky external addressing.

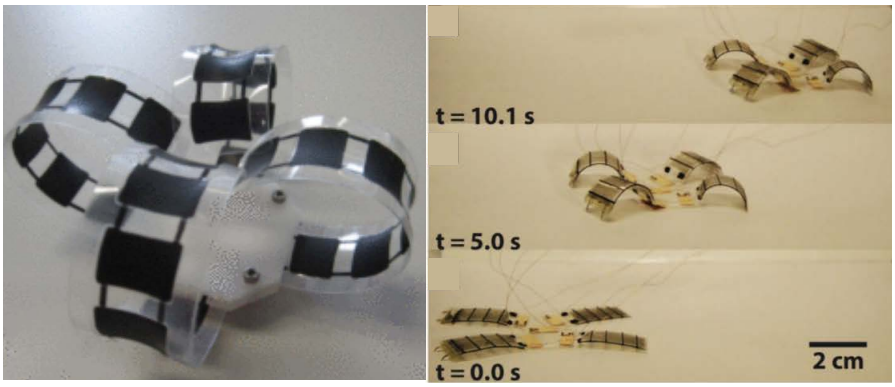
The low-force generated by in-plane expansion of such devices (< 1 mN) has classically been a problem for DEA base haptic displays. In this case, the problem is overcome by using thermally bistable electroactive polymers as the dielectric elastomer material [15, 16]. Other work report the use of liquid [32, 67] or rigid coupling [68, 69]. Alternatively, stacked DEAs can be used [37] or DEAs with bias mechanisms consisting in springs to amplify the force [70].

Up to date, one of the biggest challenge that has not been addressed is the requirement of "a high-voltage active matrix control circuitry which is currently unavailable"(sic [15]). Prior to this thesis, no work had been published demonstrating successful addressing of dielectric elastomer actuators haptic displays with active integrated controls.

2.4.2 Soft robots

A soft robot is made of soft structural or functional elements [71]. Figure 2.7 shows different soft robots applications made of DEA that could take advantages of the implementation of high voltage thin-film transistors (HVTFTs).

Figure 2.7a shows four soft grippers made of four DEA segments [30]. When a high voltage is applied to this gripper every segment opens simultaneously. By controlling independently each segment, we would be able fabricate flexible, lightweight, compact articulated grippers with multiple degrees of freedom. For this, the integration compact flexible high voltage switches is required at every independent segment.



(a) (b)

Figure 2.7 – (a)Multisegment rollable gripper [30]. (b)Fiber-based DEA tethered soft robot able of soft locomotion able of [34].

Another advantage of DEAs in soft robotics compared to other soft actuators comes from their very high speed, enabling very fast displacement. As an example, an inchworm robot made of DEAs has recently been demonstrated to be able to move at a speed of 1 body-length per

second [34]. Figure 2.7b shows a four legged robots [34] fabricated using the same principle as the grippers described by [31]. The robot has 5 layer stacked structure to amplify the force 1 DEA can generate. Compared to an inchworm robot actuator, composed of a single arm crawling, multi-legged robots have higher directional control and could combine several modes of displacement (walking, crawling, etc...). Integrating HVTFTs with this technology would enable to make all actuators independent from one another and integrate directly the power supply on the body of the robot with compact microcontrollers, moving forward towards untethered soft robots. Also adding thin film transistors on the leg of the soft robot could enable articulated motion by separating the DEAs in several segments, similarly to [30]. Adding HVTFTs could also enable the integration of smart sensors able to detect collision or self-switching the walking motion in a closed-loop, towards autonomous robots.

These two examples motivate the need for integrated HVTFTs. Compact addressing of several actuators in a soft robots with integrated flexible switches has not been demonstrated yet and would be a breakthrough for soft robotics.

2.5 Reducing the operation voltage of DEAs vs addressing high voltage DEAs with low-voltage switches

Up to this point, we have seen the qualities, the working principle, the materials of DEAs and applications requiring addressing. From Equation 2.1, we have seen that the reduction of the membrane thickness reduces the voltage required to actuate a DEA. Intuitively, it would therefore be practical to reduce the voltage of DEAs down to several volts and address them with performant flexible low-voltage thin-film transistor (TFT) or with miniaturized silicon-chips integrated on flexible substrates as shown in [72] rather than designing HVTFTs. However, shrinking down DEAs comes at the cost of the DEA force and displacement [73]. In particular, shrinking down the membrane of the DEA means increasing the stiffening impact of the electrodes on the DEA, limiting thus the actuation strain [43, 52]. Figure 2.8 shows the effect of shrinking down of DEA with 2 µm electrodes on the actuation strain, highlighting how the stiffening impact limits the actuation stretch. When the DEA has a membrane above 50 µm the drop in actuation stretch is negligible. For 5 µm thick membranes, the actuation strain drops by 50 %. Shrinking down the electrodes have recently been demonstrated to avoid stiffening impact [74], with a DEA having a maximum actuation strain of 7% at 150 V but at the cost of an electrode resistance higher than 20 MΩ per square.

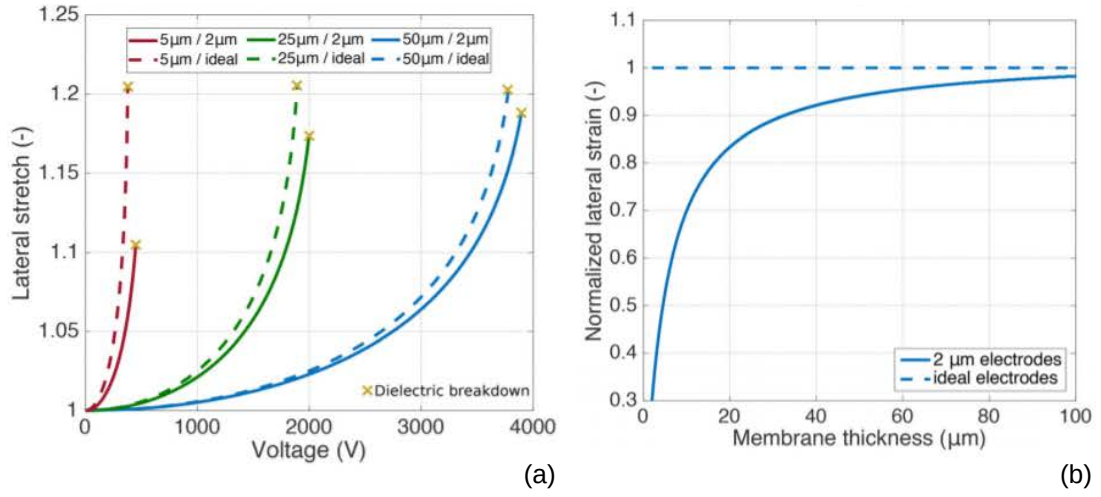


Figure 2.8 – (a) Lateral stretch vs voltage for different membrane thickness under constant thickness 2 µm electrodes. (b)Normalized lateral strain evolution vs the membrane thickness with 2 µm electrodes. The dashed curves represent devices for which we would neglect the stiffening impact (Adapted from [73]).

By designing a high-voltage TFT, we can keep processing DEAs operating higher than 500 V, while switching them with a voltage lower than 100 V, a voltage that can be controlled with compact commercial components that can be integrated on foil.

3 High voltage thin film transistors: fundamentals and technologies

Summary

This chapter covers fundamentals of thin-film transistors (TFTs) and high voltage thin-film transistors (HVTFTs) for operation above 100 V.

First, we introduce the TFT technology as an alternative technology to crystalline silicon (c-Si) metal oxide semiconductor field effect transistor (MOSFET) to be processed on insulated flexible substrate. We compare the four main semiconducting channel technologies that can be used for TFTs, amorphous silicon (a-Si), polycristalline silicon (poly-Si), organic polymers and metal oxides (MOxs). The latter, MOxs is the only one having demonstrated at the same time TFTs with high mobility (up to 100 $cm^2 V^{-1} s^{-1}$ [75]), good uniformity over a large area and stability under mechanical stress.

Afterwards, we present the working principle of TFTs and figures of merit to determine if a TFT behaves as a good switch: the threshold voltage, the gate voltage swing, the on-off current ratio and the on-current.

Then, based on these figures of merit, we classify and compare the HVTFTs reported up to date. From this classification, we identify a trade-off between performance and high voltage operation. The highest on-off ratio and on-current are achieved for the TFTs with the lowest operation voltage typically below 400 V. Only a-Si HVTFTs were reported operating above 500 V, specifically at 800 V [76].

Finally we report the failure mechanisms in HVTFTs and identify the ones that are specific to a channel technology. Kink effect makes poly-Si HVTFTs complicated to use for applications above 400 V. Channel length modulation and space charge limited current (SCLC) in organic HVTFTs lead to transistor failure above 500 V. Only a-Si and MOx technologies appear to be viable for applications > 500 V. However the limitation in on-current, typically in the μA range, for a-Si make us select MOx as the channel semiconductor for the HVTFTs of this thesis.

3.1 Introduction to TFT technology

A field effect transistor (FET) is a component with three terminals, a source, a drain and a gate. When a potential is applied at the drain or the source and at the gate, the current flow between the source and the drain is modulated. Therefore, a FET can act as a switch. A FET can operate as a p-type device or an n-type device, depending on the channel's majority carriers. The respective charge transport carriers of n-type and p-type devices are electrons and holes.

In this section, we first describe the TFT technology, a particular case of FET. Then, we describe the different TFTs channel technologies and compare them.

3.1.1 MOSFETs and TFTs

Today, the most widely used FET is the MOSFET. Table 3.1 and Figure 3.1 show the main differences between MOSFET and TFTs.

Table 3.1 – Comparison between the c-Si MOSFET and the TFT

	MOSFET	TFT
Channel technologies	c-Si	Mainly poly-Si, a-Si, organic, MOx
Conduction mode	Inversion	Accumulation
Mobility	$> 1000\ cm^2 V^{-1} s^{-1}$	$< 100\ cm^2 V^{-1} s^{-1}$
Substrate	Semiconductive, rigid	Insulating, bendable, stretchable

On the channel technology aspect, MOSFETs are made of crystalline semiconductors, mainly silicon. This channel is part of the crystalline wafer used as a substrate. A TFT is a FET device, in which the channel is made of with a thin film semiconductor acting as the conductive channel between the source and the drain. A gate dielectric separates the channel from the gate electrode. The channel of TFTs is made of various thin film technologies, including a-Si, poly-Si, organic, polycristalline and amorphous MOxs [1]. As a consequence the TFT channel conduction is substrate independent.

The channel of a MOSFET is created by the inversion of the majority carriers at the interface between the substrate and the gate dielectric, when applying a potential at the gate electrode. As an example, for a p-doped substrate, when applying a positive voltage the gate dielectric, the holes deplete and n-type conduction occurs between the n-type source and the drain. The channel of a TFT is created by the accumulation of the majority carriers at the interface between the gate dielectric and the semiconductor. As an example, for a n-type semiconductor, if a positive voltage is applied across the gate of the TFT, the electrons accumulate in the channel, and n-type conduction occurs between the metallic source and drain.

A figure of merit for field effect transistors is the channel mobility. It describes the scattering events of the charge carriers in the semiconductor. The higher the mobility, the less scattering

events occur, the more performing the transistor is. For silicon MOSFET, the electron mobility is in the order of 1500 $cm^2 V^{-1} s^{-1}$ [77], whereas the highest mobilities reported for TFTs is in the order of 100 $cm^2 V^{-1} s^{-1}$ [1].

Despite the better performance of c-Si MOSFETs, a key advantage of TFTs is the fact they can be processed on flexible [78] and stretchable [18] substrates over a large area since they rely on thin film deposition. As the TFT channel conduction is substrate independent, they can be processed on insulating substrates from glass to polymers, with, as main application, backplane addressing of matrix for transparent displays like liquid crystal displays (LCDs) [79].

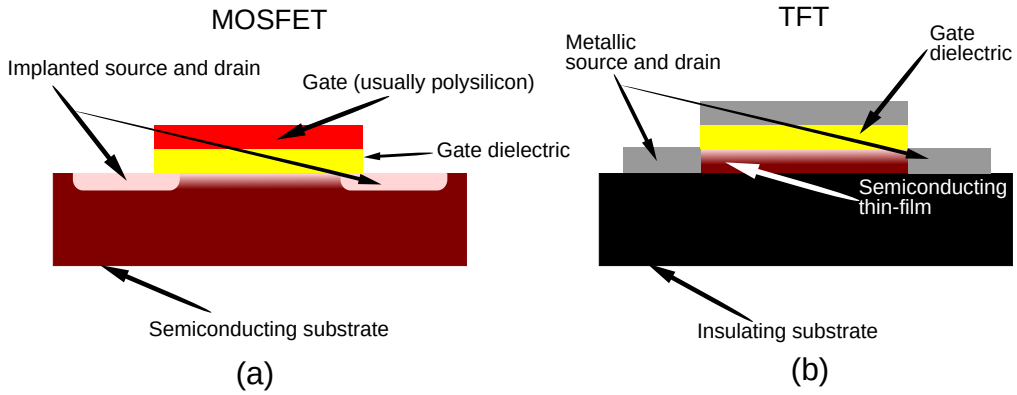


Figure 3.1 – Comparison between (a) the MOSFET and (b) the TFT architecture.

3.1.2 TFT channel technologies

TFTs can be made of polycristalline silicon, amorphous silicon, organic and metal oxide. Other technologies such as cadmium based [17], carbon nanotube (CNT) [80] or 2D-materials (MoS_2 [81], graphene [82]) based TFTs exist but are less frequently used due to fabrication process, stability, toxicity issues. Table 3.2 reports a comparison between TFTs made of a-Si, poly-Si, organic and MOx.

Table 3.2 – Comparison between amorphous silicon poly-silicon, organic and metal oxide TFT technologies(adapted from [1,2])

	a-Si	poly-Si	Organic	MOx
Mobility ($cm^2 V^{-1} s^{-1}$)	< 1	50-100	10^{-4}-40	0.01-100
Preferred conduction type	n-type	both	p-type	n-type
TFT to TFT uniformity	good	poor	poor	good
Stability under mech. stress	poor	poor	good	good
Printable?	No	No	Yes	Yes

In silicon systems, the high mobility higher than 1000 $cm^2 V^{-1} s^{-1}$ is obtained from the crystalline orders of sp3 orbitals. The mobility of a silicon transistor strongly depends on

its crystalline morphology and structural disorders creates scattering events. As a consequence, polycrystalline silicon TFTs and amorphous silicon TFTs have respectively a mobility < 100 $cm^2 V^{-1} s^{-1}$ and < 1 $cm^2 V^{-1} s^{-1}$ [1,78].

The mobility of organic TFTs (OTFTs) strongly depends on the chemistry of the organic materials used. The highest mobility reported for OTFTs is 40 $cm^2 V^{-1} s^{-1}$ [83] for a channel made of a C8-BTBT layer, which process has been optimized to obtain a highly crystalline and continuous semiconducting thin film with densely packed organic networks.

Finally, the metal oxides semiconductors exhibit the highest mobilities with poly-Si TFTs. One of the key advantages of metal oxide semiconductors is that their mobility is obtained from overlapping circular s-orbitals [78], making the crystallography dependence of the mobility negligible, compared to silicon or organic technologies. As a consequence, amorphous MOx thin film can lead to TFTs as performant as crystalline MOx. Another advantage of MOxs semiconductor is their tunability. By combining metallic cations together, the performance of the TFTs can be optimized and its mobility maximized. As an example, in 2014, Avis et al. reported an amorphous indium zinc tin oxide (IZTO) TFT with a very high mobility of 114 $cm^2 V^{-1} s^{-1}$ [75].

Most TFTs have one prefered conduction type. a-Si and MOx TFTs are preferentially n-type transistors and organic TFTs are mostly p-type [2]. Exceptions exist but p-type MOx such as tin oxide or copper oxide TFTs (< 10 $cm^2 V^{-1} s^{-1}$ [84]) and n-type organic TFTs (< 5 $cm^2 V^{-1} s^{-1}$ [85]) require high optimization to reach mobility values > 1 $cm^2 V^{-1} s^{-1}$. Therefore, complementary architectures are very challenging. poly-Sis TFTs can be doped and therefore can be used in complementary architecture like c-Si MOSFETs.

a-Si and MOx technologies enable TFTs over a large scale with uniform properties. However, it is not the case for organic technologies, which depends of organic molecule densities and poly-Si technology, which depends on the crystal size and channel length.

Under flexure, both organic and metal oxide technologies have good stability, especially amorphous oxide semiconductor (AOS) [78], whereas a-Si and poly-Si lack of stability under bending [2].

Finally, organic technologies and metal oxide technologies have been more widely studied as printable materials [1]. Organic technologies can be synthesized by dispersing the semiconductive organic compound in an organic solvent, eg TIPS-pentacene [86,87]. Metal oxide semiconductors can be synthesized by sol-gel process [1,75,88] or by nanoparticles deposition [1,89].

3.2 TFTs working principle

In this section the working principle of TFTs is described along with the key figures of merit to characterize TFTs performance. We start by presenting the output and transfer characteristics and the current voltage relation of a TFT. We then present different figures of merit, the mobility, the threshold voltage, the on current, the on-off current ratio and the voltage swing.

3.2.1 TFT characteristics

The TFT behavior is now described by the FET equations from Sze [90]. We only consider the case of a n-type TFTs. Let V_{ds} and I_d be the voltage and current between the drain and the source. Let V_{gs} be the voltage applied between the gate and the source. When the TFT source and drain are biased, the channel forms and starts to conduct carriers when the gate voltage exceeds a threshold value, called threshold voltage, V_t. When $V_{ds} < V_{gs}$-V_t, the current depends on V_{ds} and V_{gs} and can be expressed as :

$$\left(I_{ds}\right)_{V_{ds}<V_{gs}-V_t} = \frac{W}{L} K_n \left(V_{gs} - V_t\right) V_{ds} \tag{3.1}$$

Where W is the channel width of the TFT, L is the channel length of the TFT and K_n is the transconductance constant of the TFT defined as follow:

$$K_n = \mu C_{ox} \tag{3.2}$$

Where C_{ox} is the dielectric capacitance per unit of area of the TFT gate and μ is the field effect mobility. C_{ox} is expressed as:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_\delta}{t_{ox}} \tag{3.3}$$

Where ϵ_0 is the vacuum permittivity constant ($\varepsilon_0 = 8.854 \cdot 10^{-12}\ \mathrm{F\,m^{-1}}$)

When $V_{ds} > V_{gs}$-V_t, the current saturates and does not depend on V_{ds} anymore. V_{ds} follows then a quadratic law with the applied gate voltage:

$$\left(I_{ds}\right)_{V_{ds}>V_{gs}-V_t} = \frac{W}{2L} K_n \left(V_{gs} - V_t\right)^2 \tag{3.4}$$

Figure 3.2a shows the example of an I_d-V_{ds} characteristics, called the output characteristics, with a clear separation between the ohmic and the saturation regime.

Figure 3.2b and c show respectively the transfer characteristics, I_d-V_{gs} and the $\sqrt{I_d}$-V_{gs} charac-

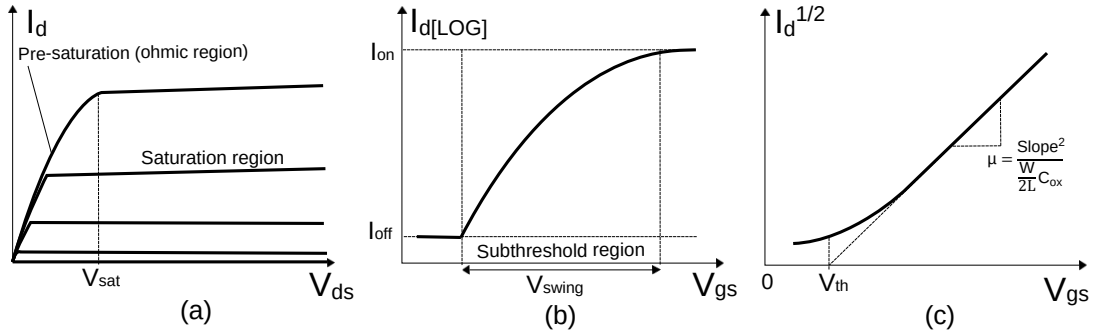


Figure 3.2 – (a) TFT output and (b) transfer characteristics example. In the output characteristics, the drain voltage is swept for stepped values of gate voltage. In the transfer characteristics, the gate voltage is swept at a constant value of the drain voltage in linear or saturation regime. The mobility and the threshold voltage of the TFT can be extracted from (c) the square-root transfer characteristics.

teristics used to extract the key parameters of the HVTFT: the on-current I_{on}, the off-current I_{off}, the voltage swing V_{swing} required to switch the TFT on and off, the threshold voltage V_{th} and the TFT saturation mobility μ.

3.2.2 Quantifying TFT performance

A high mobility semiconductor is a necessary condition to achieve a performant TFT because, as seen in Equation 3.1 and in Equation 3.4, it is a key parameter to have a high current across the TFT channel in on-state ($V_g > V_{th}$), ie I_{on}. However, a good TFT exhibits a high on-current, it also needs to block current in off-state ($V_g < V_{th}$), ie its off-current, I_{off}, needs to be small. We quantify this characteristics with the on-off ratio, $\frac{I_{on}}{I_{off}}$. The TFT should be off for a gate voltage of 0 V, which means the threshold voltage should be > 0 V. Finally, the subthreshold swing, S, expresses the gate voltage required to increase the drain current by one decade in the subthreshold region of the transfer characteristics. Typically, the subthreshold swing is aimed to be in the order of 0.1 V/dec [1].

For HVTFTs it is more practical to speak about voltage swing rather than subthreshold swing, because the latter is rarely reported in the HVTFT literature. In this PhD thesis, we used V_{swing} to replace the subthreshold swing S. In the subthreshold regime, V_{swing} relates to S with the following formula:

$$V_{swing} = \frac{S}{\log I_{on} - \log I_{off}} \tag{3.5}$$

As a switch, the TFT requires a low-gate voltage swing to switch between I_{on} and I_{off}, ideally, < 1 V.

3.3 High voltage thin film transistors

The goal of this section is to provide a literature review on HVTFTs. The HVTFT is first introduced and a state-of-the-art for every channel technology HVTFTs is provided. HVTFTs have not been widely explored and the conclusions that have been drawn from these works also relate to phenomena that have been observed at low-voltage, especially in short channel devices, which are also exposed to high electric fields.

3.3.1 Introduction to the HVTFTs

Table 3.3 and Figure 3.3 show a comparison between HVTFTs and low voltage TFTs cross-sections. HVTFTs are TFTs able to switch at a voltage above 100 V [87, 91]. Low-voltage TFTs have to achieve high current at low operation voltage, below 10 V, which means having a high transconductance as said in Equation 3.2, ie a high mobility semiconductor and a high dielectric capacitance. The mobility depends on the semiconductor material. The high dielectric capacitance means a low dielectric thickness and a high dielectric constant.

Table 3.3 – Differences between TFTs and HVTFTs

	Low voltage TFT	High voltage TFT
Target	High speed, low power	High operation voltage
Operation voltage	< 10 V	> 100 V
Typical V_{swing}	< 1 V	> 10 V
Typical I_{on}/I_{off}	$> 10^8$	$< 10^4$
Typical I_{on}	> 100 µA	< 10 µA
Typical V_t	var.	var.
Semiconductor	High mobility	High mobility
Dielectric	High K, thin	High E_{bd}, thick
Gate electrode	Fully overlapping	Offset from high potential electrode
Source and drain contact	Minimal contact resistance	-

HVTFTs have to operate at very high voltage, which means that the dielectric should not break down due to excessive electric field. As a consequence, HVTFTs are implemented with thick gate dielectrics with high breakdown field E_{bd}. As an example, a lot of HVTFT technologies use 300 nm SiN [76, 91–93], which has a breakdown strength of 10 $MV cm^{-1}$ and a dielectric constant of 5.5 [94]. As a comparison low-voltage TFTs are usually made of high-K dielectrics such as hafnium oxide (dielectric constant of 25, breakdown field of 2 $MV cm^{-1}$) or yttrium oxide (dielectric constant of 25, breakdown field of 4 $MV cm^{-1}$) with a thickness from 10 to 100 nm [95, 96]. To also decrease the electric field between the gate and the high voltage electrode (the drain in n-HVTFTs and the source in p-HVTFTs), the gate is offset by several µms [91]. As a consequence, the problem of minimizing the contact resistance between the electrodes and the channel in low-voltage TFTs is less important for HVTFTs. Indeed, the

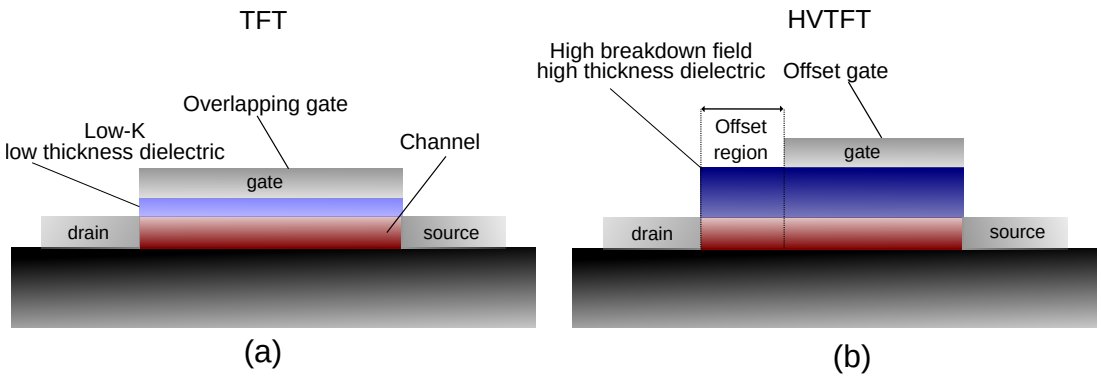


Figure 3.3 – Cross-sections of a (a) Low voltage TFT and the (b) HVTFT.

intrinsic offset region dominates the contact resistance.

3.3.2 HVTFTs state-of-the-art

We now describe the different HVTFTs reported up to date by semiconductor channel technology. Table 3.4 shows a review of the different HVTFT technologies reported up to date. We added to the figures of merit of TFT the breakdown voltage and the maximum operation voltage of the HVTFT. The breakdown voltage of a HVTFT is the voltage at which the HVTFT fails electrically by its channel or by its dielectric. The maximum operation voltage is the highest voltage demonstrated in the article through a transfer or an output characteristics. The field plate input is used in devices stabilizing the transition between the offset region and the gated region, to suppress high electric field effects. We will discuss these aspects in the next section.

Cadmium Selenium HVTFTs

We describe the polycristalline cadmium selenium (CdSe) HVTFT published in 1979 by Luo [97], as it has the highest operation voltage (400 V) reported for CdSe HVTFT reported up to date. The CdSe HVTFT is described in Figure 3.4.

Figure 3.4 shows a cross-section and the output characteristics of the CdSe dual-gate HVTFT operating at 400 V [97]. No transfer characteristics was provided. As shown in Figure 3.4a, the transistor had been processed on glass. The HVTFT had a dual-gate architecture for increased transconductance. No offset gate was applied. The CdSe layer had a mobility of $200\,cm^2\,V^{-1}\,s^{-1}$. An interesting fact is the use of a nanometric layer of indium, deposited between the semiconducting layer and the dielectric, inducing an additional increase of the transconductance of the HVTFT. The dielectric layer was a 550 nm layer of Al_2O_3.

Figure 3.4b shows the output characteristics of the HVTFT. The maximum operation voltage was 400 V. The off-current was 10 nA. The on-current was 200 µA. The on-off ratio was

Table 3.4 – Review of HVTFTs, classified by channel materials.

Semiconductor	Year	Dielectric	Offset gate	Field plate	V_d(max)	I_{on}	I_{on}/I_{off}	V_{swing}	Flexible	Breakdown voltage
CdSe	1979 [97]	550 nm Al2O3	No	Dual gate	400 V	200 µA	20000	20 V	No	> 400 V
CdSe	1990 [98]	400 nm Al2O3	No	No	200 V	500 µA	10000	8 V	No	> 200 V
CdSe	1998 [99]	400 nm SiO2	No	Dual gate	100 V	10 µA	*ND*	20 V	No	*ND*
Poly-Si	1988 [100]	150 nm SiO2	40 µm	No	400 V	50 µA	10000 (at 20V)	15 V	No	400 V
Poly-Si	1988 [101]	300 nm SiO2	15 µm	No	100 V	50 µA	1,00E+07	5 V	No	130V
A-Si	1987 [92]	SiN	16 µm	No	200 V	5 µA	ND	6 V	No	*ND*
A-Si	1991 [102]	300 nm SiN	20 µm	Yes	400 V	4 µA	ND	*ND*	No	*ND*
A-Si	1993 [91]	300 nm SiN	16 µm	Yes	400 V	5 µA	10000	6 V	No	> 400V
A-Si	2004 [93]	250 nm SiN	*ND*	No	110 V	2 µA	*ND*	20 V	No	> 110 V
A-Si	2006 [76]	300 nm SiN	100 µm	No	800 V	1 µA	10000	10 V	No	> 800 V
Organic	2012 [103]	200 nm parylene-C/200 nm BZN	20 µm	Yes	400 V	6,5 nA	ND	20 V	No	700 V
Organic	2015 [104]	200 nm parylene-C/200 nm BZN	20 µm	Yes	400 V	6,5 µA	ND	20 V	radius: 37.5 mm	700 V
Organic	2017 [87]	2 nm Parylene-C/400 nm BZN	20 µm	Yes	100 V	250 nA	20	40 V	radius: 50 mm	150 V
Metal oxide	2016 [105]	200 nm SiO2	20 µm	No	200 V	5 µA	1,00E+08 (V_{ds} = 200V)	50V	No	610 V

ND = Not defined

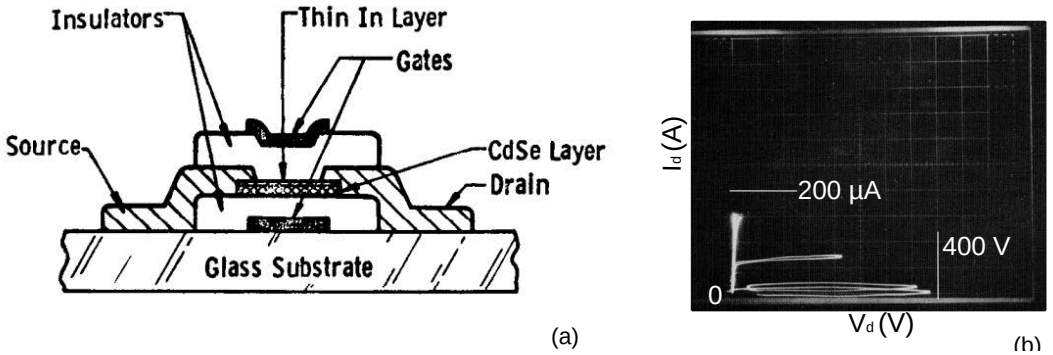


Figure 3.4 – CdSe HVTFT. (a) Cross-section and (b) output characteristics (adapted from [97]).

consequently 20,000.

Other works mention the use of CdSe as the channel for a HVTFT but none of them demonstrates it above 200 V [106–108]. If CdSe HVTFTs present excellent transconductance properties, the lack of stability, the toxicity and the carcinogenicity of the material, make CdSe not ideal as a channel semiconductor for HVTFTs.

Polycrystalline Silicon HVTFTs

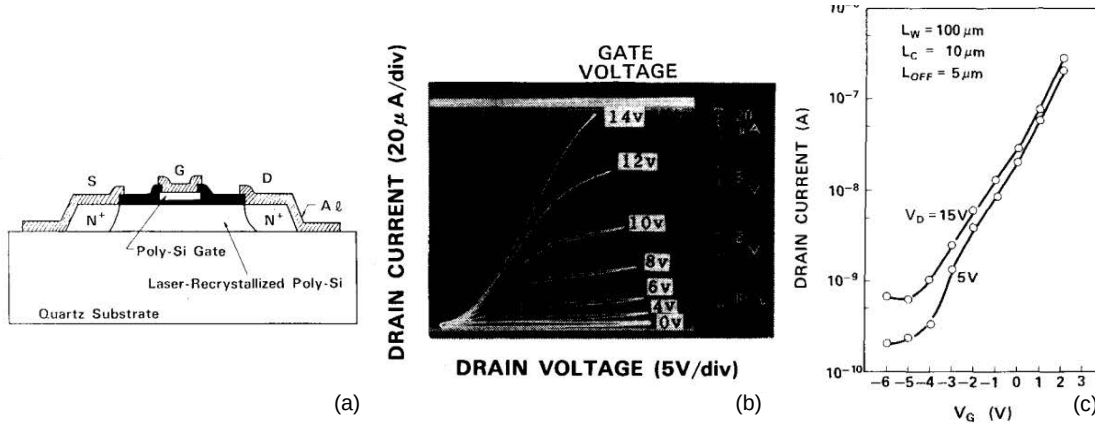


Figure 3.5 – Polycristalline HVTFT. (a) Cross-section, (b) Output characteristics at 50 V, (c) Transfer characteristics. (adapted from [100])

Poly-Si channels present the advantage of being composed of crystalline silicon domains, leading to high mobility materials (in the order of 100 $cm^2 V^{-1} s^{-1}$ [1,2]). Several works demonstrated poly-Si HVTFTs [100, 101].

Figure 3.5 shows the cross-section of the HVTFT, the output and transfer characteristics of the HVTFT reported by Unagami in 1988 [100]. The device was built on a quartz wafer. The n-doped poly-Si has been deposited by CVD at 625°C and large crystalline grains have been obtained by laser annealing. The gate electrode was made-of p-doped poly-Si. The source and

drain were made in n-doped poly-Si. The gate dielectric was a 300 nm thick silica. The HVTFT had an offset gate geometry to operate under a high drain voltage. The offset gate is 10 µm for a channel length of 100 µm and a width of 10 µm.

The on-off current ratio was 10^5 at 20 V drain-source voltage but dropped at 10^3 was at 400 V drain-source voltage. The on current was 50 µA and the gate voltage swing was 15 V.

Poly-Si HVTFTs present some critical problems to be used as a technology for flexible thin film transistors. The processes used to deposit and the silicon layer requires very high temperature. Also, due to the heterogeneity of polycrystalline domains, reproducible characteristics are difficult to obtain over a large area. In addition to those problems, the grain boundaries due to polycrystalline domains lead to kink regime preventing operation higher than 400 V (see section 3.4) .

Amorphous Silicon HVTFTs

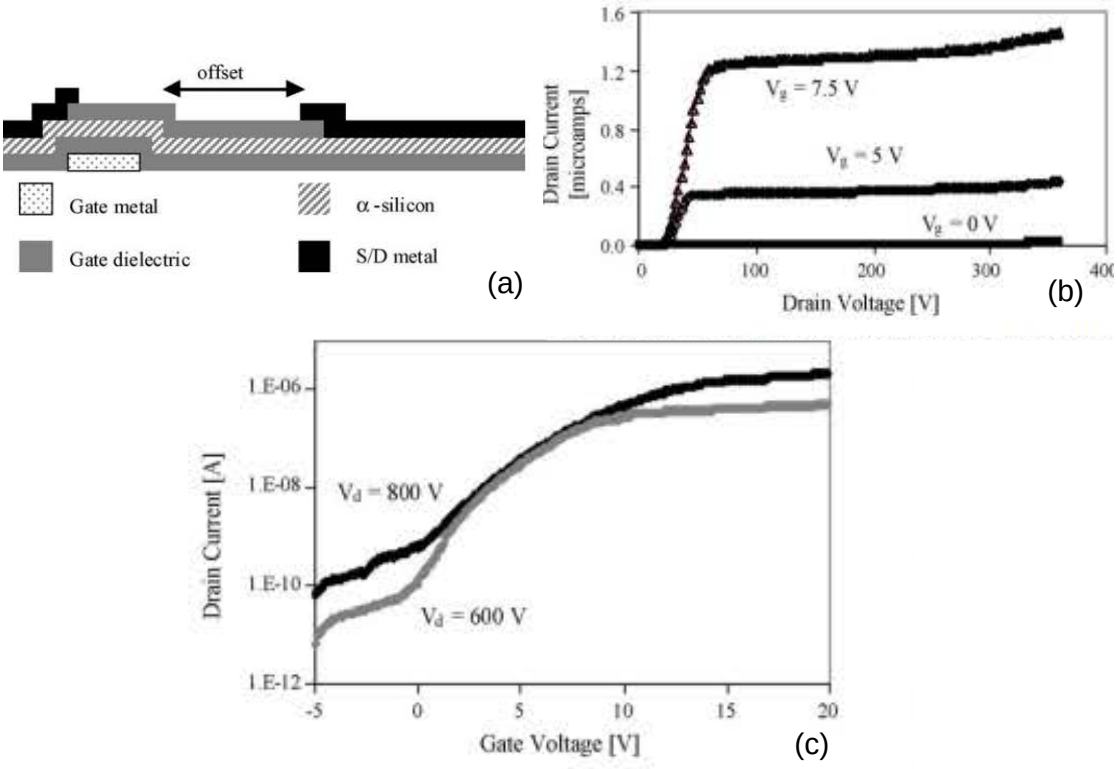


Figure 3.6 – a-Si HVTFT. (a) Cross-section, (b) Output characteristics, (c) Transfer characteristics (adapted from [76])

The a-Si technology originally aimed at providing an alternative to poly-Si. HVTFTs can be synthesized uniformly on a wider area than poly-Si at room temperature.

Figure 3.6 shows the cross-section, the output and the transfer characteristics of the HVTFT

reported by Chow et al. in 2006. The device was processed on glass. The gate dielectric was made of a 300 nm thick silicon nitride. It had an offset gate geometry with an offset of 100 µm for a channel length of 110 µm.

The HVTFT showed stable operation at 800 V [76]. It was the highest operation voltage reported for HVTFTs prior to this thesis work. The on-off ratio is 10^4 and the maximum blocking voltage is higher than 800 V. The on-current is around 1 µA.

As the a-Si do not have grain boundaries, the kink effects are less problematic in HVTFTs. As a consequence the maximum operation voltage has been limited by the gate dielectric breakdown and self-heating of the semiconductor [91] (see section 3.4). The low mobility of a-Si leads however to low on-current HVTFTs in the µA range [76, 91].

Organic HVTFTs

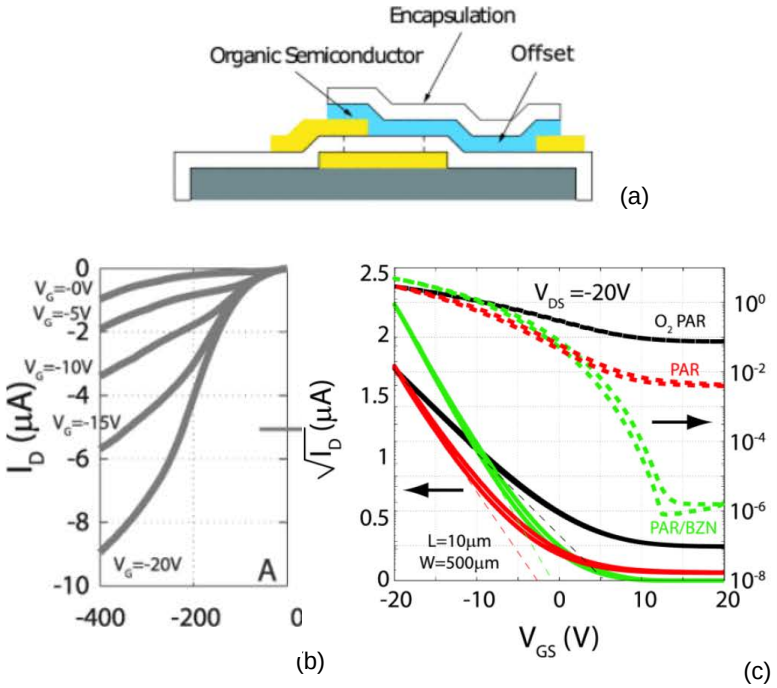


Figure 3.7 – Organic pentacene HVTFTs. (a) Cross-section. In yellow, the metal electrodes are in gold, in white, the dielectric layer is based on Parylene-C and the semiconductor is pentacene. (b) Output characteristics for the HVTFT with a Parylene-C BZN dielectric bilayer, (c) Transfer characteristics (right scale in µA) and square-root transfer characteristics (left scale) of organics HVTFTs at 20 V with 3 different dielectric layers: Parylene-C, oxygen plasma treated Parylene-C and a bilayer of BZN and Parylene-C. (adapted from [104])

The main advantage of organic semiconductors are their compatibility with flexible substrates and their low processing temperature. A wide range of range of organic semiconductors can also be solution processed. They can achieve extremely low off-currents and therefore very

high on-off ratios. It is very challenging to design high mobility materials and most reports use semiconductors with a mobility less than 1 $cm^2 V^{-1} s^{-1}$, leading to very low on-current, and the need to use geometrical modifications to increase the channel current like interdigitated source-drain electrodes [86].

Figure 3.7 shows the cross-section, output and transfer characteristics of Pentacene HVTFTs [104]. The device was processed on flexible Cirlex. The material of the channel was pentacene and the dielectric was a stack of 200 nm high-K BZN (bismuth zinc niobate oxide) and 200 nm of flexible Parylene-C. It had an offset gate geometry with a channel length of 30 µm and an offset gate length of 20 µm .

The high-voltage organic thin film transistor (HVOTFT) exhibited a breakdown voltage of 600 V and the maximum operation voltage reported was 400 V. At 400 V, the on-off current ratio was 20 for a gate swing of 20 V and the on-current was 6 µA. No mobility value was reported. Operation under static bending was demonstrated down to a radius of curvature of 37.5 mm.

Additionally Shih et al. reported a comparison between pentacene (thermally evaporated) and TIPS-pentacene (printed) as a semiconductor materials [87]. The dielectric was composed of bilayer of 2 nm parylene-C and 400 nm of BZN. The offset gate was varied from 5 to 30 µm.

The pentacene and TIPS-pentacene broke down respectively at 550 V and at 150 V drain-source voltage. The on-off ratio at 500 V were respectively 3000 and 20. The on-currents were respectively 30 nA and 100 nA and the gate swing 50 V and 30 V. The reported mobility 0.00025 and 0.00079 $cm^2 V^{-1} s^{-1}$, respectively.

HVOTFTs present several challenges at high voltage. Space charge limited current (SCLC) and channel length modulation led to the divergence of the saturation region of the semiconductors and very high off-current at high voltage, which caused failure at 600 V [103, 104] (More details are provided section 3.4). Like a-Si, organic HVTFTs require optimization to achieve high on-current.

Metal Oxide HVTFTs

Very few MOx HVTFTs - none before the start of this project - have been demonstrated up to date despite the excellent properties of MOx TFT [78]. Figure 3.8 shows the cross-section of a MgZnO HVTFTs and its output and transfer characteristics [105]. In order to avoid channel breakdown and electric field unbalance due to the edges of the source and the drain the HVTFT had a ring-shape. The semiconducting thin film was sputtered magnesium zinc oxide thin film (Mg:Zn = 3:97). The gate was offset from the drain (5, 10, 20 µm) and the source (3 µm) for a channel length of respectively 10, 15 and 25 µm. The dielectric was a 200 nm thick silica layer.

The HVTFT breakdown voltage was 600 V with an on-current of 4 µA. Information about the on-off ratio and the voltage swing at 600 V were not provided. The HVTFTs had only been fully

characterized up to 200 V as shown in Figure 3.8c. Despite this, the transfer characteristics remained remarkably stable up to the application of a 200 V drain-source voltage as shown in Figure 3.8c.

Compared to other technologies, MOx HVTFTs have a great potential in achieving higher performance at high voltage because of their high mobility in amorphous phase. The latter protects the HVTFTs from high-voltage effects related to grain boundaries appearing in poly-Si technologies.

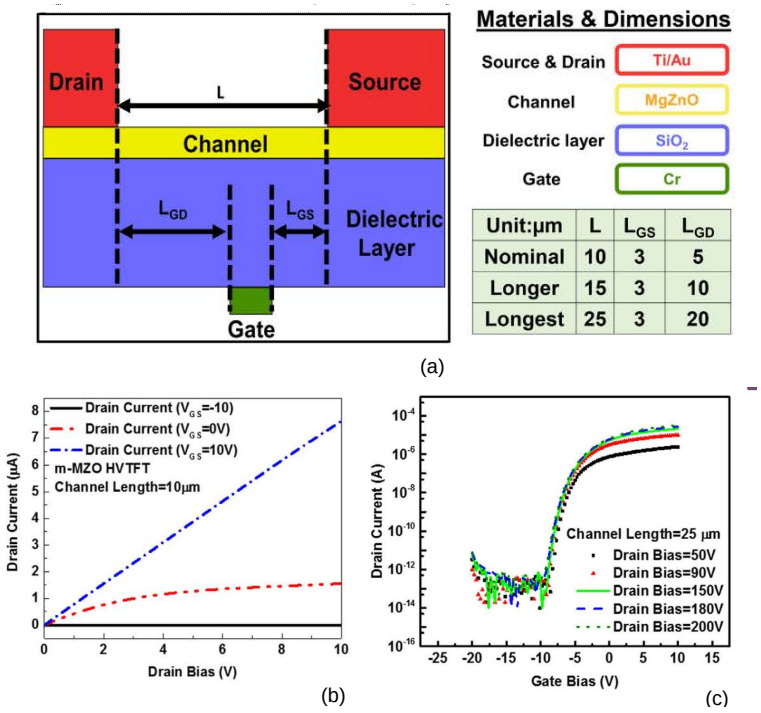


Figure 3.8 – Amorphous oxide semiconductor HVTFT made of MgZnO as the semiconductor channel. (a) Cross-section, (b) Output characteristics, (c) Transfer characteristics. (adapted from [105])

3.4 High electric field effects and failure modes for HVTFTs

The operation voltage limit is defined by the failure mechanisms in HVTFTs. To select a reliable technology at high voltage it is crucial to identify these phenomena. The goal of this section is to analyze the different failure mechanisms of HVTFTs. Those can either be caused by dielectric or channel breakdown. Some of these high voltage effects are also present in short channel field effect transistors such as channel length modulation (CLM). Some others are caused by the offset gate geometry (space charge limited current, potential barrier at offset edge), or the material used (space charge limited current in organic semiconductors, kink effects in poly-Si semiconductors). We present these failure modes and the most relevant effects in the section below. Other effects such as carrier velocity saturation or threshold voltage roll-off [104] can also occur, but are less relevant as they do not irreversibly damage the HVTFTs.

3.4.1 Dielectric breakdown

Dielectric breakdown [109] occurs between the semiconductor channel and the gate electrode. When the potential difference between the channel at the gate edge and the gate electrode is higher than the breakdown voltage of the gate dielectric of the HVTFT, then the electrons bypass the gate dielectric. The gate and the channel being thus short-circuited, the device cannot operate anymore. The quality of the dielectric layer is essential for a high breakdown voltage device. A high pinhole concentration in the dielectric leads to lower breakdown voltage. The HVTFT offset gate is of primary importance to increase the breakdown voltage as the channel potential drops in the non-gated region to reach values below the dielectric breakdown voltage in the gated region of the HVTFT.

3.4.2 Channel failure and high electric field effects

Channel length modulation and punch-through effect

Figure 3.9 shows an output characteristics subjected to channel length modulation. Channel length modulation occurs in HVTFTs under high electric fields [93, 103, 104]. When a high drain-voltage is applied, the effective distance between the drain and the source decreases. As a consequence, an increase in the drain voltage leads to a linear increase of the channel current in the saturation region of the thin film transistor. Equation 3.4 is then modified as follows:

$$\left(I_{ds}\right)_{V_{ds}>V_{gs}-V_t} = \frac{W}{2L} K_n \left(V_{gs}-V_t\right)^2 \cdot (1+\lambda V_{ds}) \tag{3.6}$$

Where $\lambda = \frac{1}{V_a}$. V_a is the voltage at the cross-point between $I_d = 0A$ and the the saturation curve (often called Early Potential).

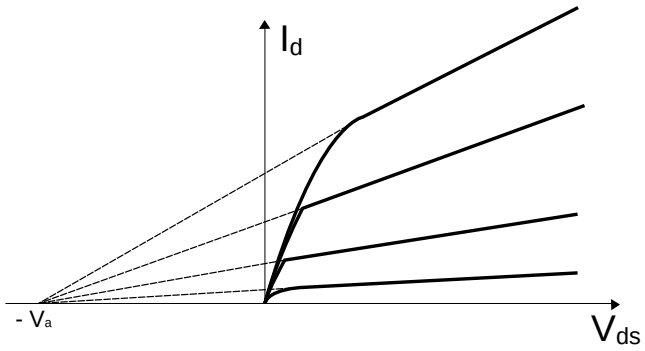


Figure 3.9 – Output characteristics of HVTFTs affected by channel length modulation.

The problem associated with channel length modulation is the high current values reached for lower gate voltage, leading to increased off-current, therefore, lower on-off current ratio and higher power consumption. Under excessive bias, the accumulation regions created by the source and the drain electrodes merge and the channel length modulation results in a punch-through effect, i.e. the formation of a continuous electron path between the drain and the source, leading to drain-source breakdown. The current diverges, the damage in the channel are irreversible and the HVTFT fails. Alternatively, channel length modulation and punch through effect can also lead to the reduction of the potential drop in the offset region of the HVTFT triggering thus dielectric breakdown [104].

Kink regime

The a-Si and poly-Si short-channel semiconductor technologies face a type of instability suppressing the field effect in the TFT under high drain-source electric field [110–112]. Figure 3.10 shows an output characteristics where this effect appears.

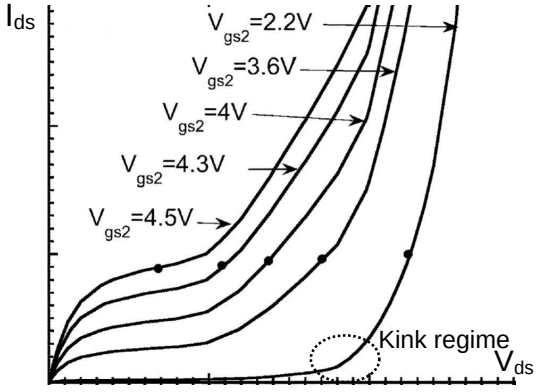


Figure 3.10 – Example of output characteristics showing kink effect(adapted from [113])

This is the kink effect. When $V_{ds} > V_k$, where V_k is the kink regime voltage, the drain-current increases abruptly and becomes independent from the gate voltage. The kink effect is sus-

pected to be due to charge carriers impact ionization at grain boundaries and self-heating near the drain electrode under the application of a high electric field [111, 112].

Space-charge limited current

A polycrystalline or an amorphous thin film semiconductor usually has a high concentration of traps and the high electrical potential applied leads to even more trap generation due to high energy electron scattering. As the offset region is not gated, the electrical conduction happens in the thin-film bulk, where are located a high density of trapped carriers. The offset region is therefore a space-charge medium and the electrons conduction is controlled by the trapped and free charges in the bulk. Space charge limited current is the current flowing through an electrically non-neutral medium [114]. In general, the semiconductor channel is assumed to be charged-neutral (ie the bulk of the semiconductor is assumed to have a zero charge). As shown in the output characteristics of Figure 3.11, a consequence of SCLC is the saturation voltage shift, which can cause problems for circuit integration.

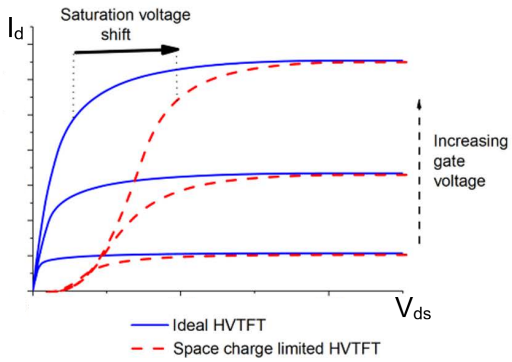


Figure 3.11 – Example of output characteristics showing space-charge limited current and its effect on saturation voltage shift(adapted from [91]).

In an ohmic region, the current depends linearly from the voltage. In a space-charge region, the output current is a power law of the input voltage. The relationship is quadratic in a trap free medium, where only the free charges contribute to space-charge limited current. However in a medium with a high concentration of traps, such as in amorphous silicon, the I-V curve is modulated by the space-charge limited current [91, 115]. Martin et al. reported a model to predict the SCLC behavior of a-Si HVTFTs [91], in which trapped charges dominate free charges. It consists in solving the Poisson's equation, Equation 3.7 in the offset region.

$$\frac{dE}{dx} = q\frac{n_t}{\varepsilon_0 \varepsilon_{SC}} \tag{3.7}$$

Where n_t is the density of trapped charges, E is the electric field across the space-charge region and ε_{SC} is the semiconductor permittivity.

Potential barrier induced by gate offset edge

Figure 3.12 shows the comparison between the output characteristics of a HVTFT subjected to a potential barrier and one that is not.

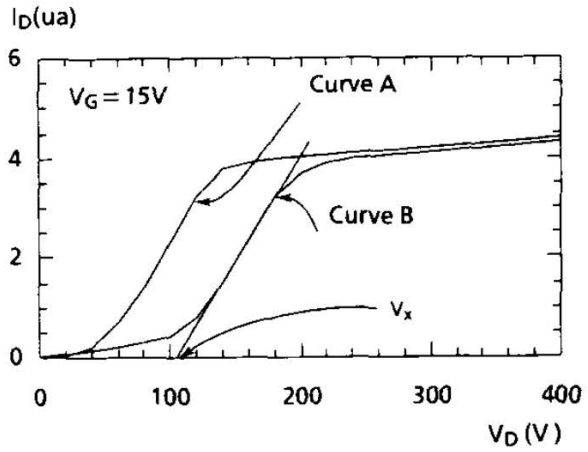


Figure 3.12 – Output characteristics of two HVTFTs. The HVTFT A is only affected by space charge limited current (quadratic shape of the linear region) and the HVTFT B is affected by space charge limited current and the potential barrier induced by the gate offset edge. The curve is offset in the x-axis by V_x. (adapted from [91])

Applying a very high positive voltage to the drain, when the offset-gate voltage is under the threshold value leads to the depletion of the charge carriers in the offset region. As a consequence, the Fermi level of the semiconductor decreases below its intrinsic value. In order to recover the Fermi level, the material fills the zone with charges, leading thus to the apparition of traps behaving as acceptors. This increase behaves like a potential barrier that needs to be overcome for the charges to be injected in the offset region. This barrier is effective only in the vicinity of the gate edge [102, 116]. Conjugated to SCLC, this effect is dramatic as it shifts the onset drain voltage value to the right (see Figure 3.12). Equation 3.1, Equation 3.4 and Equation 3.6 become :

If $V_x < V_{ds}$, the charges are blocked at the offset edge and:

$$\left(I_{ds}\right)_{V_{ds}<V_x} \approx 0 \tag{3.8}$$

If $V_x < V_{ds} < V_{gs} + V_x - V_t$, we are in the linear/space-charge limited current regime.

$$\left(I_{ds}\right)_{V_{ds}<V_{gs}+V_x-V_t} = \frac{W}{L} K_n \left(V_{gs} - V_t\right) \cdot \left(V_{ds} - V_x\right) \tag{3.9}$$

If $V_{ds} > V_{gs} + V_x - V_t$, we are in the saturation/channel length modulated regime.

$$\left(I_{ds}\right)_{V_{ds}>V_{gs}+V_x-V_t} = \frac{W}{2L} K_n \left(V_{gs} - V_t\right)^2 \cdot \left(1 + \frac{V_{ds}}{V_a + V_x}\right) \tag{3.10}$$

This effect has been proven to be reversible for a-Si techonology if the devices were annealed [102]. Every technology with an offset gate that has reported an output characteristics at V > 100 V is affected by the potential barrier at the offset position [87, 92, 100, 104]. The potential barrier can reduce or disappear by adding a field plate at the offset [87, 91, 104] but at the cost of a lower dielectric breakdown voltage [87].

3.4.3 Failure mechanisms of the different HVTFT technologies

Table 3.5 – Failure mechanisms per HVTFT channel technology

Technology	Failure localization	Failure mechanism
Poly-Si [100, 112]	Channel	Kink effects
a-Si [76, 91]	Dielectric or channel	Dielectric breakdown or self-heating
Organic [103, 104]	Channel	SCLC and CLM
AOS [105, 117]	Dielectric	Dielectric breakdown

The four semiconductor technologies poly-Si, a-Si, organic and AOS have different sensitivity to high electric field effects. Table 3.5 summarizes the failure mechanisms for each channel technology, leading to HVTFT failure.

Organic technologies are particularly sensitive to SCLC and channel length modulation (CLM). In organic technologies, SCLC also occurs in the gated channel and contributes to the non-saturation of the HVTFTs [103, 104, 118]. Ultimately, channel length modulation appear to be causing the breakdown of the HVTFTs described. Even if those effects could be decreased by decreasing the electric field across the channel by increasing the channel length, it is difficult to envision high voltage organic technologies operating for a drain voltage higher than 500 V.

Poly-Si technologies are affected by kink effects [110, 112]. The latter appears to be the cause of the divergence of the drain-source current in poly-Si HVTFTs [100]. Kink effects are essentially due to an avalanche effect at the grain boundaries of poly-Si and to the floating body effect in TFTs [119]. In order to reduce the kink effect in high-voltage poly-Si HVTFT, similar strategies could be used, e.g. splitting the channel with highly doped floating electrodes [113]. Such modification could however affect the potential distribution in the channel leading thus to premature breakdown. As long as the kink effect remains unsolved for poly-Si technology, it will be very complicated to fabricate poly-SiHVTFTs operating above 400 V.

The a-Si technologies can fail due to self-heating of the channel or dielectric breakdown [76,91]. They are affected by kink effects [111], however less than poly-Si as a-Si HVTFTs have been

proven to operate up to 800 V [76]. Self-heating is due to the very poor thermal conductivity of a-Si (1.1 W/mK [111]) and the fact that the film usually deposited on glass [111]. In the report demonstrating 800 V [76] operation of a-Si, it is possible that the heat generated by the high potential gets dissipated in the silicon nitride encapsulation(thermal conductivity up to 25 W/mK). The a-Si HVTFTs are also affected by SCLC but only in their linear region leading to saturation voltage shifts [91].

For MOx technologies, it is complicated to estimate how high electric fields affect the devices as those effects can essentially be read on the output characteristics. As the only output characteristics of the HVTFT presented in Figure 3.8b goes only up to 10 V, we cannot draw any conclusion [105]. From the transfer characteristics in Figure 3.8c, we can however see that the off-current does not increase with increasing drain-source voltage, indicating thus insensitivity to channel length modulation and kink effect up to 200 V. It has been reported that AOS are by far less sensitive to kink and short channel effects than the other semiconductor technologies [117, 120], which is extremely promising, considering most high voltage effects replicate short channel effects [104].

Conclusion

In this chapter, fundamentals on HVTFTs were presented. An introduction was made on TFTs and their different channel technologies. Then, the working principle of TFTs was described along with the TFT key parameters to evaluate performance. Afterwards, the HVTFT was introduced and the state of the art was summarized. Finally the HVTFTs failure mechanisms were described and correlated to the type of channel technology used.

Table 3.6 shows a comparison between the different HVTFT technologies synthesizing according to two technical parameters what we have seen in this chapter, the limit in operation voltage and the performance as a TFT. Poly-Si and organic HVTFTs require very complex and challenging improvements to be operating at > 400 V. Poly-Si and organic HVTFT are respectively limited by kink effects and by the combination of CLM and SCLC. The a-Si HVTFTs were demonstrated up to 800 V, but the low mobility of this semiconductor technology does not enable high on-current. Metal oxide are able of very high performance. The only drawback of MOx HVTFTs compared to the three other technologies is the lack of scientific literature and information about the effects occurring in the thin film at very high voltage. Fabricating and characterizing a HVTFT made of MOx would therefore bring scientific novelty and take advantage of the excellent properties of the channel technology to fabricate a HVTFT with high performance. We will describe how to build a HVTFT using this technology in the next chapter so that it can be implemented as a switch for dielectric elastomer actuators.

Table 3.6 – Comparison between the different channel technologies to fabricate a performant HVTFT

	Poly-Si	Organic	a-Si	MOx
Limit in operation voltage	-	-	+	+
Performance	+	-	-	+
HVTFT technological background	+	+	+	-
Scientific novelty	-	+	-	+

4 Concept and design of a HVTFT to drive DEAs

Summary

The objective of this chapter is to establish a concept and the design of a high voltage thin-film transistor (HVTFT) to drive arrays of dielectric elastomer actuators (DEAs)

We first describe the requirements for a HVTFT to be able to drive a DEA. We start by describing the circuit interconnecting the HVTFT and the DEA. We provide a table of requirements providing minimal and optimal parameters (Operation voltage, on-off ratio, on-current, voltage swing, flexibility, crystallinity) for a HVTFT leading to > 75% actuation strain of a DEA with a minimal time response of 100 ms [66] and a minimal driving voltage of 300 V [43].

Then, we discuss the design of the HVTFT by first identifying the amorphous oxide semiconductor (AOS) channel technology to use. We start by introducing AOSs followed by a description of two of the most successful technologies of AOSs, sputtered IGZO and solution processed ZTO. Solution processed ZTO was chosen because its electronic and crystalline properties can be easily tuned by control over the cations stoichiometry.

Finally, we present the complete HVTFT structure built around the zinc tin oxide (ZTO) semiconductor. Due to the high temperature required for the ZTO synthesis, the substrate used is polyimide. The HVTFT design combines a thick gate dielectric, and an offset gate > 50 µm. The gate dielectric is composed of a 100 nm thin layer of alumina (breakdown field E_{bd} = 7 MV cm^{-1}) and a 1 µm flexible Parylene-C layer (E_{bd} = 4 MV cm^{-1}). The use of a bilayer should decrease the probability of pinholes and passivate the HVTFT. To limit the high electric field effects such as channel length modulation (CLM), the HVTFT has a long channel of 500 µm with a W/L of 10.

4.1 Requirements on the HVTFT

In this section, we describe the requirements on a HVTFT to drive a DEA. We first determine the circuit required to control the DEA with the HVTFT. Based on this circuit, we discuss then the requirements on the on-off ratio, the on current, the voltage swing and other HVTFTs key parameters.

4.1.1 Circuit to drive a DEA with a HVTFT

Figure 4.1 shows three possible basic circuit configurations to drive DEA with HVTFTs. In the three figures, the DEA is represented by a capacitor. The three circuits are inverters, which means that a positive and a negative voltage at the gate lead respectively to a negative and positive response at the output. The inverters need to be able to drive the DEA. It means that a high voltage is applied to the circuit.

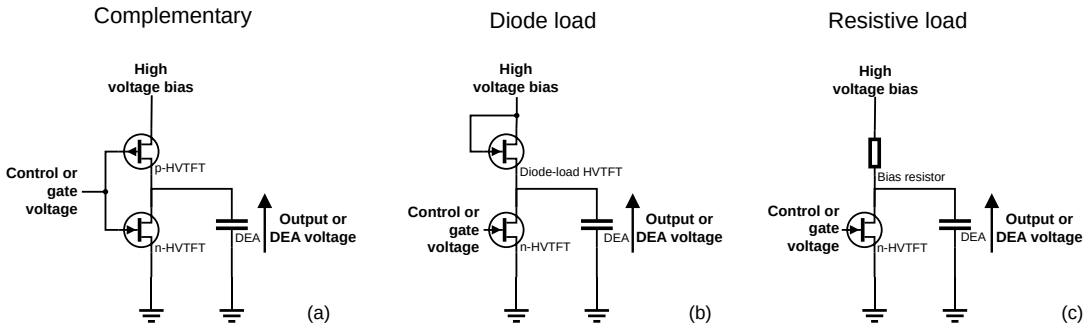


Figure 4.1 – Three inverter architectures to drive a HVTFT (a) Complementary inverter, (b) Diode-load inverter, (c) Resistive load inverter.

As a consequence, the complementary (Figure 4.1a) and the diode load (Figure 4.1b) circuit architectures are impossible as the gate of the pull-up transistor is referenced at the high voltage node. If the voltage across the DEA is at the high-voltage value, it means that the entire channel of the pull up HVTFT is at a high voltage, leading thus to a probable gate dielectric breakdown. As a consequence, to drive a high voltage DEA, we can only use the resistive-load structure shown in Figure 4.1c. The bias resistor is a passive component limiting the current flow, enabling to vary the output voltage with the switching of the channel of the HVTFT.

Figure 4.2 shows the working principle of the DEA-HVTFT circuit. When a gate voltage $V_g = V_t + V_{swing}$ is applied to the HVTFT, the HVTFT is on and dominates the bias resistor current and the voltage across the DEA is 0 V (Figure 4.2a). When a gate voltage $V_g < V_t$ is applied across the HVTFT, it is off and the bias resistor dominates the HVTFT current and the DEA charges. The voltage across the DEA is then the bias voltage of the circuit (Figure 4.2b).

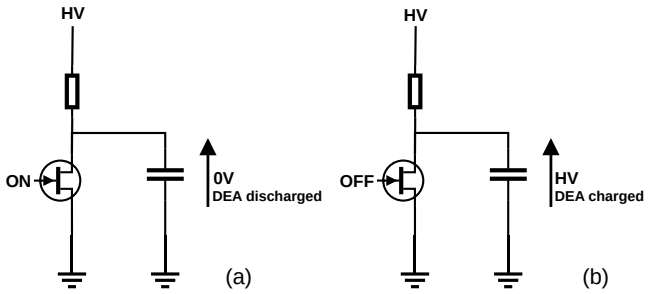


Figure 4.2 – Operation principle of a resistive loaded inverter driving a DEA. (a) When the gate of the HVTFT is biased, a current runs through the HVTFT channel and the DEA is discharged. (b) When the gate of the HVTFT is off, the HVTFT blocks the current and the DEA charges until reaching the high voltage (HV) value.

4.1.2 Achieving DEA actuation with minimal voltage variation

The circuit output voltage corresponds to the voltage across the DEA. It is modulated by the HVTFT. In this section, we show that only 50% of maximum actuation voltage is required to achieve 75 % actuation thanks to the non-linearity of the DEA strain response to the output voltage.

Considering that the maximum DEA actuation strain is less than 20% and that we neglect the stiffening impact of the electrodes, we can approximate the actuation strain-voltage relation with [6]:

$$s_z = -\frac{\varepsilon_m \varepsilon_0}{Y_m t_m^2} \cdot V^2 \tag{4.1}$$

where the elastomer has a Young's modulus Y_m and the compressive strain is s_z. Let s_{max} be the maximal DEA actuation strain before breakdown and V_{max} be the associated voltage. We assume that ε_m and Y_m are constant for any actuation voltage. We define the normalized strain as k_s and the normalized voltage as k_v with:

$$k_s = \frac{s_z}{s_{max}} = \left(\frac{V}{V_{max}}\right)^2 = k_v^2 \tag{4.2}$$

with $0 < k_s, k_v < 1$.

In order to switch the DEA on and off, we need to vary k_s between 0 and 1, which implies varying k_v between 0 and 1. However, the quadratic relation between these two parameters means that a small variation of voltage leads to more actuation strain at high voltage than it does at low voltage.

Figure 4.3 shows three normalized strain voltage relations: We can achieve an 80% normalized actuation strain. This can be achieved by sweeping the DEA voltage respectively between 0% and 90%(Figure 4.3a), 25% and 95%(Figure 4.3b), 45% and 100% of its maximal value. As we can see it here, there is a clear advantage in taking the last option in order to minimize the

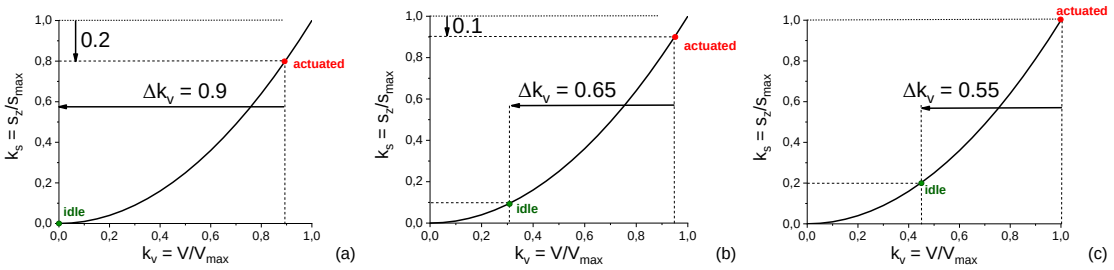


Figure 4.3 – Graphs describing the normalized strain-voltage relation of a DEA. 80% normalized actuation strain can be achieved by varying the DEA voltage (a) from 0% to 90%, (b) from 25% to 95%, (c)from 45% to 100% of its maximum value.

voltage operation range to have maximum actuation.

In order to minimize the voltage difference Δk_v for a given strain variation Δk_s of the DEA, the actuation voltage needs to be equal to the maximum voltage that can be applied to the DEA. Figure 4.4 shows the minimal voltage variation Δk_v as a function of the actuation strain range Δk_s of a DEA. This plot shows that until 75 % actuation strain, the strain is very sensitive to voltage variation, which corresponds to a tangent slope less than 1.

z

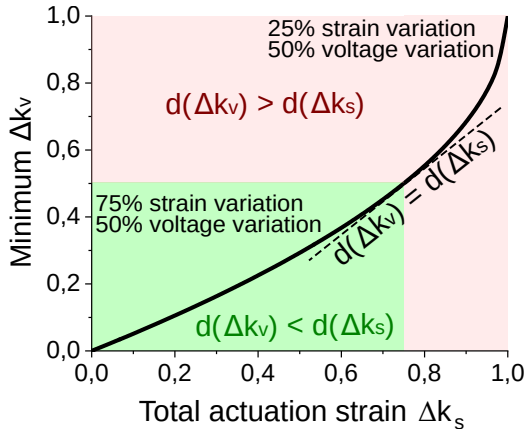


Figure 4.4 – Minimal variation of voltage required as a function of the actuation strain. Below 75% actuation strain the variation of voltage leads to a higher variation of strain. Above 75% actuation strain a variation of strain requires a higher variation of voltage

75% of the actuation strain can be achieved with 50% percent of voltage variation and the remaining 25% actuation strain is achieved within the remaining 50 % of voltage variation. Therefore, to achieve 75% of the strain actuation in the configuration shown in Figure 4.1c, we need to be able to vary the output node in the voltage range of 50% of V_{max} and V_{max}.

As an example, an actuator reaching a maximum actuation strain of 0.1 at 1 kV should be able

of a strain variation of 0.075 if the voltage is varied between 500 V and 1 kV.

A requirement for the HVTFT is to be able to switch the DEA by at least 75 % actuation strain. Based on this, we can estimate the required parameters for a HVTFT to control a DEA.

4.1.3 HVTFT requirements

Table 4.1 summarizes the table of requirements to build a HVTFT-DEA system based on the circuit presented in Figure 4.1c. In this section, we present and justify the requirements of each components, DEA, HVTFT, pull-up resistor. 75% of DEA actuation can be very efficiently achieved with 50% of voltage actuation, as we have seen in previous section, and is set as the minimum requirement. The maximal time response was defined according to the requiremnts for an application as haptic displays [66].

Table 4.1 – Requirements for a resistive load inverter based on a pull-up bias resistor, a control HVTFT and a DEA.

		Minimal	Maximal	Optimal
DEA	Normalized actuation strain	75%	-	100%
	Time response	-	100 ms	-
	Actuation voltage	300 V		-
HVTFT	Operation voltage	500 V*	-	> 1 kV
	On-off ratio	20	-	$2{\cdot}10^3$
	On-current	10 µA	-	1 mA
	Voltage swing	100 V*	-	5 V
	Flexibility	-	30 mm	1 mm
	Semiconductor microstructure		Amorphous	
	Channel length modulation (CLM)		Negligible	
Bias resistor	Resistance	-	200 M	20 M

* = Requirement defined initially by the project

The actuation voltage requirement of the DEA was based on the minimal operation voltage reported for DEAs by LMTS at the beginning of this thesis [43]. However, low-voltage DEAs are usually strain limited because of the electrodes stiffening impact. At LMTS, the standard electrode process leads to the fabrication of 2 µm thick carbon-PDMS electrodes [52], which prevent the lateral strain of 300 V DEAs to exceed 8% before dielectric breakdown [43].

Operation voltage

In the circuit of Figure 4.1c, the HVTFT drain-source electrodes are in parallel with the DEA. Consequently, the HVTFT has to withstand the DEA operation voltage. In the initial specifications, the minimum operation voltage was set at 500 V. However, most DEA require a voltage

higher than 1 kV to operate. Therefore, the HVTFT should optimally operate at voltages higher than 1 kV.

On-off current ratio

In the circuit of Figure 4.1c, we consider a resistor of resistance R, a DEA of capacitance C and a HVTFT with an on-current I_{on} and off-current I_{off} interconnected as shown Figure 4.1c. The circuit is biased by a high voltage power supply of value V_{dd}. We call V_{max} the output voltage when the DEA is actuated, i.e. when the transistor is off (open). We call V_{min} the output voltage when the DEA is in its discharged state, ie when the transistor is on (close). We call V_{sat} the transition between the linear and saturation region of the drain-source voltage of HVTFT in on-state. We assume ideal I-V characteristics with no high-voltage effects. The off-state resistance is defined as

$$R_{off} = \frac{V_{dd}}{I_{off}} \tag{4.3}$$

The on-state resistance is defined as:

$$R_{on} = \frac{V_{sat}}{I_{on}} \tag{4.4}$$

The output voltage in Figure 4.1c is obtained by assuming a voltage divider. When the DEA is actuating, the output voltage is V_{max}. When it is not, its voltage is V_{min} and:

$$V_{max} = \frac{R_{off}}{R + R_{off}} \cdot V_{dd} \tag{4.5}$$

$$V_{min} = \frac{R_{on}}{R + R_{on}} \cdot V_{dd} \tag{4.6}$$

$$V_{max} = \frac{1}{1 + \frac{R * I_{off}}{V_{dd}}} V_{dd} \tag{4.7}$$

$$V_{min} \approx \frac{1}{1 + \frac{R * I_{on}}{V_{sat}}} V_{dd} \tag{4.8}$$

In order to have $V_{max} \longrightarrow V_{dd}$, we need to have $\frac{RI_{off}}{V_{dd}} \longrightarrow 0$.

If we suppose that the DEA is charged when $V_{max} = 99\% V_{dd}$,

$$I_{off} < 10^{-2} \frac{V_{dd}}{R} \tag{4.9}$$

In order to have $V_{min} \longrightarrow 0$, we need to have $\frac{V_{sat}}{RI_{on}} \longrightarrow 0$.

If we suppose that the DEA is discharged when $V_{min} = 1\% V_{dd}$, then

$$I_{on} > 10^2 \frac{V_{sat}}{R} \tag{4.10}$$

By combining both equation, we need:

$$\left(\frac{I_{on}}{I_{off}}\right)_{100\%} > 10^4 \frac{V_{sat}}{V_{dd}} \tag{4.11}$$

If we now consider the case of 75 % actuation strain for the DEA, as presented in previous section, then, V_{max} needs, as before, to be equal to V_{dd}. V_{min} needs to be equal only to $50\% V_{dd}$.

From Equation 4.8 means that $\frac{1}{1+\frac{R*I_{on}}{V_{sat}}} < 0.50$. After calculation:

$$I_{on_{75\%strain}} > \frac{V_{sat}}{R} \tag{4.12}$$

By combining Equation 4.12 and Equation 4.9, we obtain:

$$\left(\frac{I_{on}}{I_{off}}\right)_{75\%} > 100 \frac{V_{sat}}{V_{dd}} \tag{4.13}$$

Table 4.2 shows the on-off ratio requirement as a function of the normalized DEA strain.

Table 4.2 – Minimal requirement on the on-off current ratio as a function of the bias voltage and the saturation voltage of the HVTFT

$\frac{I_{on}}{I_{off}}$ to achieve 100 % DEA strain

	V_{sat} = 50 V	100 V	200 V
V_{dd} = 500 V	1000	2000	**4000**
1000 V	500	1000	**2000**

$\frac{I_{on}}{I_{off}}$ to achieve 75 % DEA strain

	V_{sat} 50 V	100 V	200 V
V_{dd} = 500 V	10	20	**40**
1000 V	5	10	**20**

In Table 4.2, we consider as minimal (75% actuation strain) and optimal requirement (100% actuation strain) the values in bold.

On-current

The on-current needs to be scaled as a function of the resistance we aim at using. It has to respect these relations:

$$I_{on_{100\%strain}} > 100\frac{V_{sat}}{R} \tag{4.14}$$

or

$$I_{on_{75\%strain}} > \frac{V_{sat}}{R} \tag{4.15}$$

As we want a response time of at least 100 ms for the DEA, it means a time constant of at least be 20 ms should be obtained. We have seen that the DEA mechanical response is around 200 µs and that carbon polydimethylsiloxane (PDMS) electrodes can be designed to achieve an intrinsic resistivity providing an electrical time constant lower than 200 µs [49, 55].

As a consequence, if we neglect the electrodes resistance, the circuit resistance has to respect the following relation:

$$\tau_{circuit} = RC_{dea} < 20ms \tag{4.16}$$

i.e.

$$R < \frac{2 \cdot 10^{-2}}{C_{dea}} \tag{4.17}$$

where C_{dea} is the DEA capacitance. Combining Equation 4.14 and Equation 4.15 with Equation 4.17 leads to a condition on I_{on}:

$$I_{on_{100\%strain}} > 5000 \cdot V_{sat}C_{dea} \tag{4.18}$$

$$I_{on_{75\%strain}} > 50 \cdot V_{sat}C_{dea} \tag{4.19}$$

In Table 4.3, we consider as minimal (75% actuation strain) and optimal requirement (100% actuation strain) the worst case scenario in bold.

Gate voltage swing

The voltage swing is the voltage required by the gate of the HVTFT to switch the output voltage in Figure 4.1c. The specification in this project was to achieve < 100 V voltage swing. An optimal value would be 5 V a standard value for driving transistor logic gates.

Table 4.3 – Requirements on the on current as a function of the DEA capacitance and the saturation voltage of the HVTFT.

I_{on} to achieve 100 % DEA strain with 20 ms actuation time constant

	V_{sat} = 10 V	50 V	100 V	200 V
C_{DEA} = 100 pF	5 µA	25 µA	50 µA	**100 µA**
1 nF	50 µA	200 µA	500 µA	**1 mA**

I_{on} to achieve 75 % DEA strain with 20 ms actuation time constant

	V_{sat} = 10 V	50 V	100 V	200 V
C_{DEA} = 100 pF	50 nA	250 nA	500 nA	**1 µA**
1 nF	500 nA	2,5 µA	5 µA	**10 µA**

Bending curvature

Here, we define the bending curvature that the HVTFT should withstand without breaking down. A minimal value would correspond to reported the actuation curvature of DEA grippers like in [30], which value is below 3 cm. Ideally, the HVTFT could conform to any variety of shape down to 1 mm of radius of curvature.

Semiconductor microstructure

The semiconductor has to be amorphous in order to avoid high electric field effects due to grain boundaries.

4.2 Design of the amorphous oxide semiconductor channel

In this section, we will proceed to select an AOS material that meet the best the characteristics. We start by introducing the field of AOS and the cation tuning process, which enablies to obtain an amorphous metal oxide semiconductor film. We then compare two reference technologies, the sputtered IGZO and the sol-gel ZTO. Table 4.4 shows a comparison between two examples of these technologies and how they connect with the table of requirements. We choose to use ZTO as it presents excellent perspectives to print HVTFTs on foil and can be more easily tuned than indium gallium zinc oxide (IGZO).

Table 4.4 – Standard ZTO and IGZO TFT technologies vs table of requirements for the HVTFT

	Minimal	Optimal	Sputtered IGZO [1]	Sol-gel ZTO [88]
Operation volage	500 V*	> 1 kV	20 V	5 V
On-off ratio	20	$2{\cdot}10^3$	$5{\cdot}10^{7}$**	10^{8}**
On-current	10 µA	1 mA	0.5 mA	0.1 mA
Voltage swing	100 V*	5 V	30 V	20 V
Flexibility	30 mm	1 mm	Yes [78]	Yes [121]
Semiconductor cristal.	Amorphous		Amorphous	Amorphous
CLM	Negligible		None	None

* = Requirement defined initially by the project
** = This value drops by several orders of magnitude in HVTFTs

Table 4.4 shows the characteristics of IGZO and ZTO vs the requirements. We will describe these technologies later. The challenge of this thesis will be to increase the operation voltage of these devices without decreasing the on-off ratio, the on-current and the voltage swing.

4.2.1 Introduction on amorphous oxide semiconductors

In previous chapter, we have already mentioned that metal oxide (MOx) thin-film transistor (TFT) have critical advantages over silicon technologies. In particular, the possibility to fabricate amorphous materials, called AOS with high mobility is a key feature [1, 2, 78]. An explanation for electron mobility independence with microstructure. Figure 4.5 shows four different orbital structures. The orbitals of crystalline and amorphous silicon are shown in Figure 4.5a and b. The electron path is twisted for amorphous silicon and is a cause for low mobility if we compare to crystalline silicon. The orbitals of crystalline and metal oxides are shown in Figure 4.5c and d. The alteration of the crystalline structure does not affect the s-orbital overlaps. Consequently, metal oxide semiconductors can have a high mobility in amorphous state [117].

MOx semiconductors cover a wide range of materials and alloys including zinc oxide [122, 123], indium oxide [124], indium zinc oxide [125], indium gallium zinc oxide [126], zinc tin oxide [127], magnesium zinc oxide [105].

In previous chapters, it was mentioned that grain boundary avalanche effect causes failure in polycristalline silicon (poly-Si) HVTFTs at < 500 V. Consequently, polycrystalline semiconductors should be avoided for high voltage operation. Therefore, in the frame of this work, we have decided to go for an amorphous metal oxide alloy, which is going to be presented in the following section.

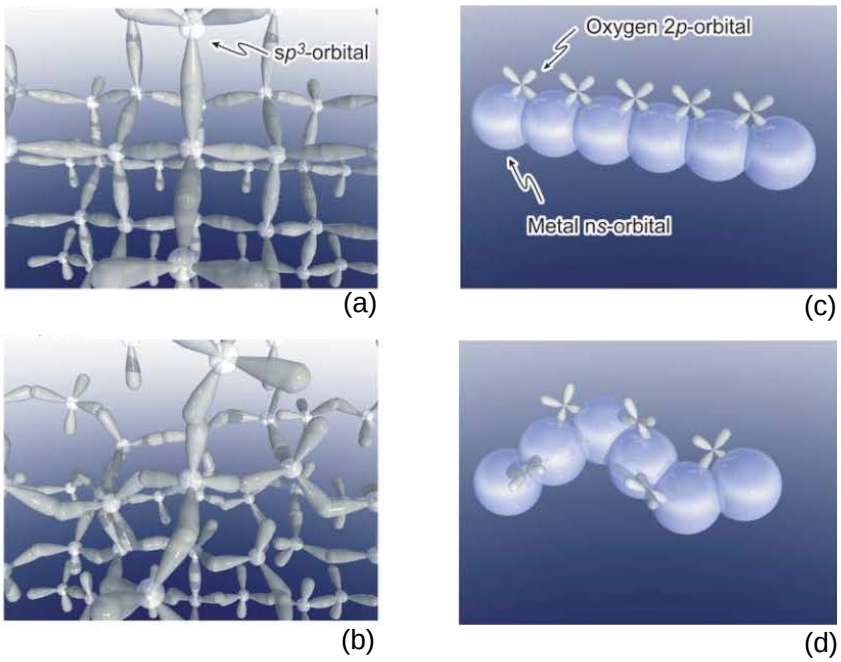


Figure 4.5 – Schematics of silicon and metal oxide orbitals. (a) Crystalline silicon. (b) Amorphous silicon. (c) Crystalline oxide semiconductor. (d) Amorphous oxide semiconductor. (adapted from [78])

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4.2.2 Zinc oxide based alloys

In single cation composition, zinc oxide was reported to be the best semiconductor available to fabricate TFTs [1]. An on-off ratio of 10^6, a voltage swing of 1 V and a mobility of 1 $cm^2 V^{-1} s^{-1}$ can be achieved. Zinc oxide has however a high concentration of traps and is mostly polycrystalline with a high concentration of grain boundaries [1, 127]. Amorphous zinc oxide has already been reported, however, it has never been used to our knowledge as a semiconductor channel [128]. In order to fabricate an amorphous material, a usual methodology is to combine several cations [1]. Tuning the cation composition enables also the optimization of the semiconducting properties of the material.

IGZO

The most used AOS today is indium gallium zinc oxide (IGZO). Compared to zinc oxide, IGZO has two additional cations: indium and gallium.

Figure 4.6a shows the transfer characteristics of IGZO TFTs with varying indium and gallium contents. Figure 4.6b shows two triangular color map showing respectively the influence of the indium, gallium and zinc stoichiometry on the mobility (and therefore on the on-current) and on threshold voltage [1].

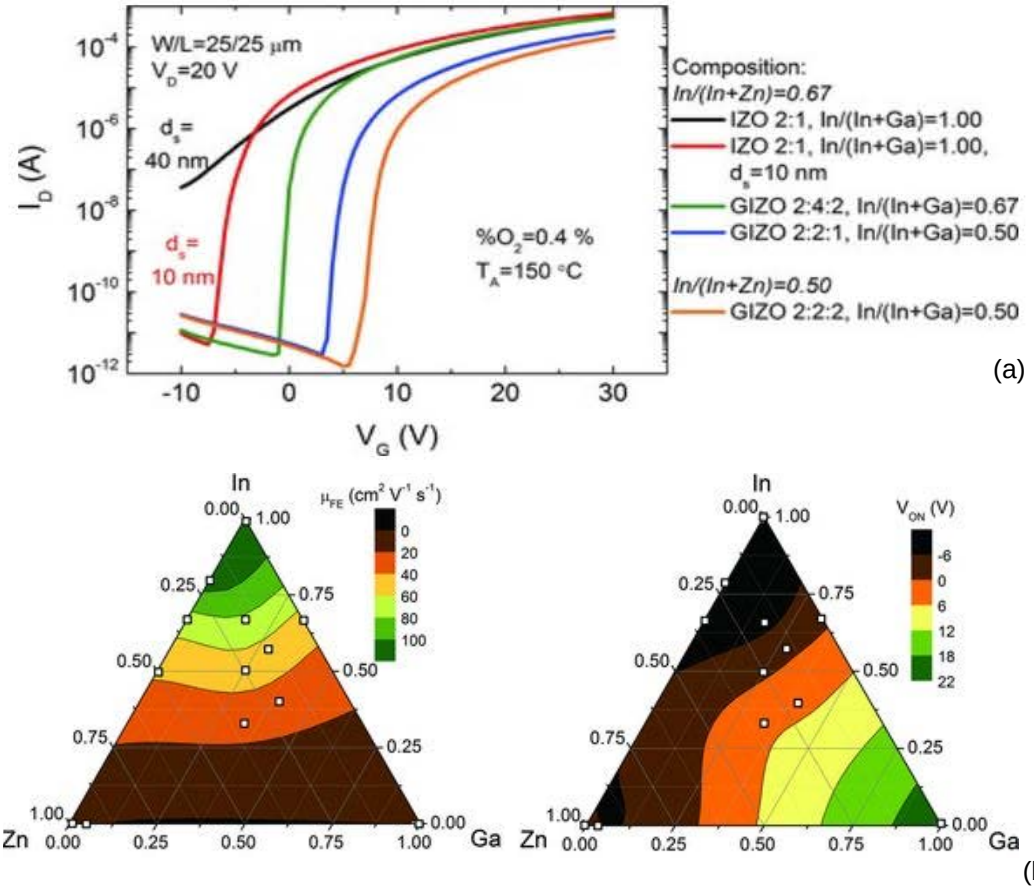

Figure 4.6 – Effect of cation tuning on IGZO TFTs. (a) IGZO transfer characteristics for different cation stoichiometry. (b) Effect of cation stoichiometry on mobility and threshold voltage (Adapted from [1]).

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Indium is a weak oxygen binder [1]. The presence of indium creates a larger electron path and oxygen vacancies, which results in an increased mobility and background charge carrier concentration. A too high concentration of indium leads to an overwhelming background carrier concentration, and, therefore, to a high off-current, a negative threshold voltage thus contributing to a decrease in the on-off current ratio [1].

In order to compensate for the high carrier concentration generated by indium, gallium is also included in the thin film. Gallium is a strong oxygen binder [1]. The addition of gallium leads to a decrease in background carrier concentration, thus leading to a decrease in the off-current and an increase in the threshold voltage. A too high addition of gallium has a negative impact on the mobility of IGZO and therefore on the off-current. Additionally the cation combination makes the film amorphous [1].

An optimal cation concentration balance exists for these thin films to achieve TFTs with excellent properties. As an example, with I:G:Z = 4:2:2, the on-off ratio of 10^8 and an on-current of 0.1 mA can be reached, with a gate swing of 10 V and a mobility was higher than 10 $cm^2 V^{-1} s^{-1}$ [1].

ZTO

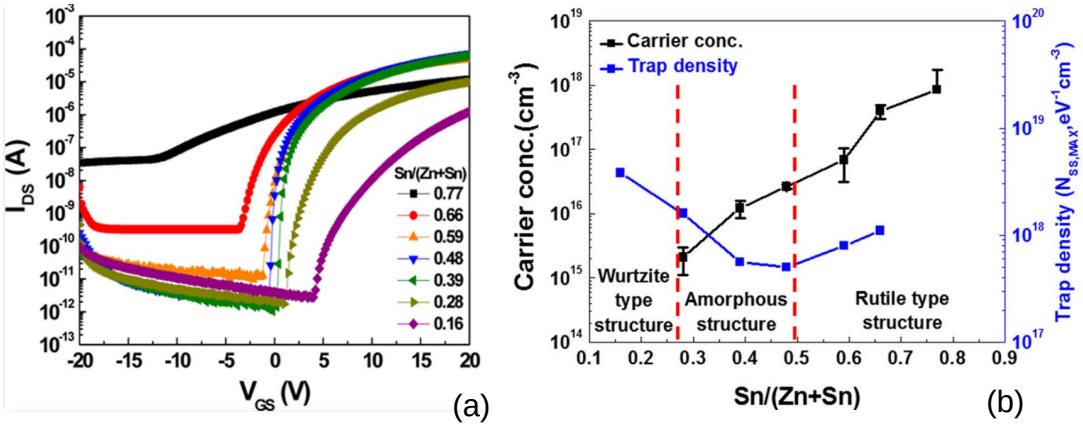

Figure 4.7 – Effect of cation tuning on ZTO TFTs. (a) ZTO transfer characteristics for different cation stoichimetries [1], and (b) effect of cation stoichiometry on cristallinity, carrier concentration and trap density (Adapted from [127]).

Due to its excellent performance, ZTO is one of the most promising solution-processed alternative to IGZO [129]. In particular, this alloy is gallium and indium-free, an advantage considering the scarcity and the cost of gallium and indium [130]. For HVTFTs, ZTO presents an additional advantage compared to IGZO: it is thermally stable, a property that should prevent the semiconductor from self-heating effects [131]. Solution-processed ZTO has been demonstrated with a mobility as high as 30 $cm^2 V^{-1} s^{-1}$ similar to what can be obtained with IGZO [88]. ZTO has another advantage: it is a binary alloy and its cristallinity as well as its electronic properties can be tuned by varying the zinc-tin stoichiometry. In a ZTO thin film, tin plays the role of the weak oxygen binder (higher mobility, higher on-current) and zinc the role of the strong oxygen binder (lower off-current, higher threshold voltage). The effect of tin can be improved by adding indium to the thin film leading to IZTO with a mobility > 100 $cm^2 V^{-1} s^{-1}$ and the effect of zinc can be improved by adding a strong oxygen binder such as gallium, scandium or yttrium (GZTO, YZTO or SZTO) [75, 132, 133].

Figure 4.7a presents different transfer characteristics with varying tin:zinc stoichiometry. Figure 4.7b shows the crystalline state and the trap and carrier concentration as a function of the tin:zinc stoichiometry [127]. ZTO is amorphous between 0.27 and 0.5 tin concentration. Beyond those values, ZTO is polycrystalline with the specific crystalline features of tin oxide or zinc oxide [127].

At a Z:T concentration of 1.7:1, the ZTO is amorphous and the TFT reported in [127] achieved on optimal on-off ratio of $5{\cdot}10^7$, an on-current of 0.1 mA corresponding, in this case, to a mobility of 4 $cm^2\,V^{-1}\,s^{-1}$. The threshold voltage was 0.8 V and the voltage swing was 20 V. In the case of the ZTO TFT reported with a mobility of 30 $cm^2\,V^{-1}\,s^{-1}$, Z:T = 2:1. the on-off ratio was 10^8 and the on-current also 0.1 mA [88]. The main difference came from the thin-film synthesis based on acetate precursors on silica substrate in Kim et al. [127] and based on chloride precursors on alumina thin film in Avis et al. [88].

Contrary other binary alloys such as IZO, ZTO is also one of the most stable alloys under bias stress, when the zinc concentration is dominating in the thin-film [134, 135].

4.2.3 Description of the sol-gel process of AOS

IGZO is essentially fabricated by sputtering [1, 88], while ZTO is mostly fabricated by sol-gel process [75, 88, 127, 132, 133]. The advantage of solution processed AOS, is that they can be manufactured over a large scale thanks to a variety of processes such as spincoating, printing or casting methods, whereas sputtering is usually limited by the wafer size and is less cost effective. In addition to this, DEAs are mostly fabricated with casting and printing methodologies. Being able to use the same types of processes for TFTs designed to drive such actuators would be of interest for better integration.

As we have seen in previous section, ZTO would be a good candidate for HVTFTs. The most frequent synthesis for ZTO semiconductor is the sol-gel route. The sol-gel route consists in the temperature reaction of chloride, acetates or nitride metal salts mixed with a solvent. When heated up to a certain reaction temperature, the chlorides or nitrides vaporize and the metal oxide network form. The precursor concentration and the deposition methodology on the substrate determines the quality and the thickness of the thin film. Figure 4.8 shows an example of sol-gel reaction between tin chloride and ethylene-glycol to form a tin oxide thin film. The chloride ions are separated from the tin by reacting with the hydrogen. They evaporate at with the organic chains at 250°C (first step of the sol-gel) and then, the hydroxides react and vaporize around 450°C (oxidation and second step of the sol-gel).

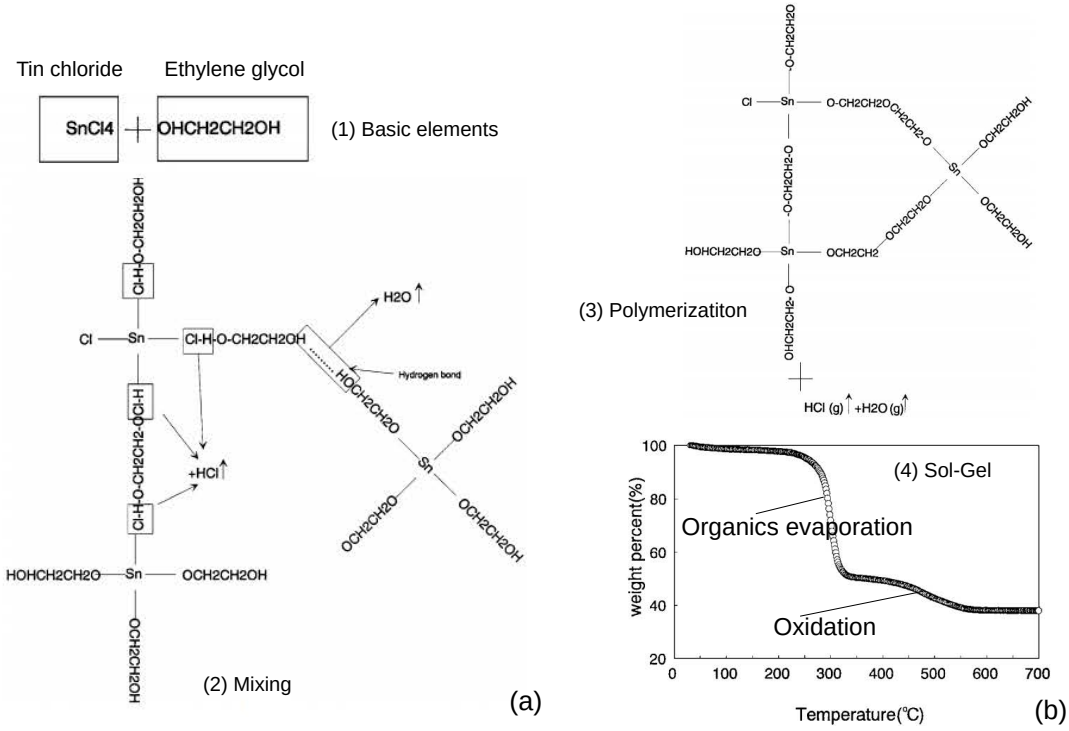

Figure 4.8 – Example of chloride based sol-gel process. (a) Tin chloride is first mixed with ethyleneglycol. During the mixing step, the chloride are separated from the metal, which bind to oxygens of ethylene glycol chain. By curing above 80°C, HCl and water are eliminated solidifying the thin film. (b)Thermogravimetric analysis of a sol-gel of metal oxide thin film. From the moment the film is solidified, the remaining HCl and the organics are eliminated at the first sharp mass loss between 250°C and 300°C. The metal oxide thin film is obtained between 450°C and 500°C at the second mass loss. (adapted from [136])

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4.2.4 In this work: Zinc tin oxide

In this thesis we use the solution processed ZTO based on the recipe presented by Avis et al [88] as it is the best compromise between simplicity (it uses only two cations) and good performance (amorphous thin film, high mobility, able of high on-off ratio and low voltage swing). We will keep a Z:T = 2:1 stoichiometry, the best configuration shown to achieve high performance AOS TFT [88, 127].

4.3 ZTO HVTFT architecture

In this section, we finalize the description of the HVTFT structure by describing the different layers and the geometrical parameters for the HVTFT. Figure 4.9 shows a cross-section and the design parameters of the HVTFT built around the ZTO sol-gel semiconductor. The HVTFT has an offset gate geometry with a dielectric bilayer composed of Parylene-C and alumina, both enabling operation above 500 V. The W/L is 10 for a channel length of 500 µm, which aim is to prevent high electric field effects. In this section, we first describe the geometry of the HVTFT, then, we present the substrate, the dielectric bilayer and the electrodes used.

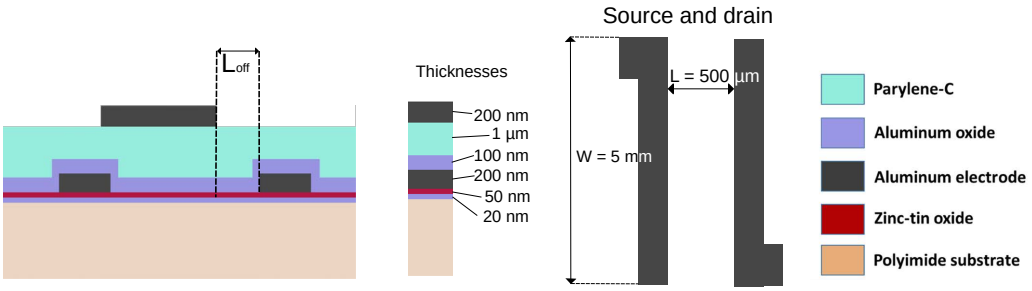

Figure 4.9 – Cross-section and architecture of the HVTFT.

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4.3.1 Electrodes architecture

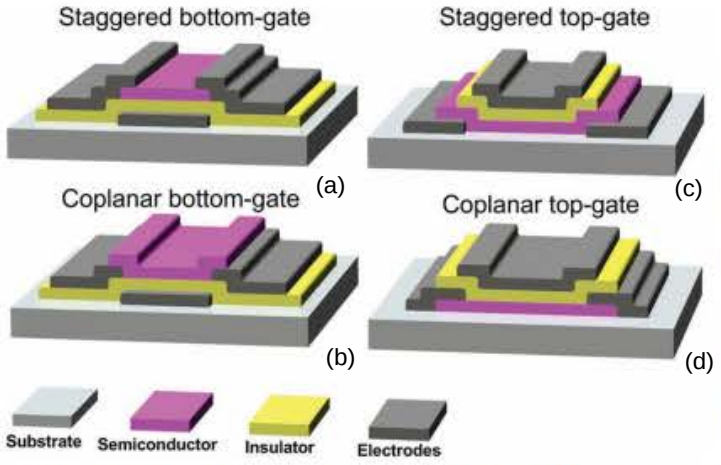

Figure 4.10 – TFTs with a (a) staggered bottom gate, (b) coplanar bottom-gate, (c) staggered top-gate and (d) coplanar top-gate architecture. (Adapted from [1])

Four different electrode architectures are possible for the HVTFT. Each one of them is described in Figure 4.10.

- **Bottom gate coplanar electrodes**: The gate, the source and the drain are deposited before the semiconducting layer, on top of the stack.
- **Bottom gate staggered electrodes**: The gate, is deposited first and the source and the drain are deposited on top of the semiconductor.
- **Top gate coplanar electrodes**: The gate, the source and the drain are deposited above the semiconductor, which is deposited first.
- **Top gate staggered electrodes**: The gate is deposited on top of the stack and the source and drain are deposited below the semiconductor.

A bottom gate configuration is practical if we use the substrate as the gate electrode and to ensure an excellent interface between semiconductor and dielectric. A top gate configuration is practical if the semiconductor requires process conditions that the other materials of the stack cannot withstand. Also, in a top gate electrode configuration, the dielectric layer serves as a passivation layer.

In order to avoid damages due to temperature of the sol-gel process (ZTO requires at least 400°C) on the other functional layers, we decided to deposit the semiconductor first. It is especially critical as we used Parylene-C as one of the dielectric layer, as will be discussed later. As a consequence, the only possible geometry is top-gate coplanar electrodes.

To increase the gate dielectric breakdown voltage we offset the gate from the drain by 150 µm to operate at 1 kV. A characterization of the effect of the offset gate on the HVTFT breakdown is provided in the next chapter.

Some high-electric field effects are due to the short-channel of the HVTFTs. It is particularly clear in Smith work, where channel length modulation accelerates the dielectric breakdown [103]. In Smith et al. [104], the maximum electric field induced by the voltage between the drain and the source at 400 V operation is 20 V/µm. In Avis et al. [88], the electric field at 5 V operation is 0.6 V/µm and enables operation without short channel effects. We scale our HVTFT so that it can hold 1 $V\mu m^{-1}$. we designed a 500 µm long channel with a 5 mm channel width (W/L = 10) in order to avoid short and narrow channel effect. Other channel lengths were tried such as 100 µm but showed very low performance and exhibited strong channel length modulation.

4.3.2 Substrate

The substrate has to respect two main requirements. It has to withstand a temperature > 400 °C required for sol-gel process and, according to the specifications defined in Table 4.1, it has also to be bendable with a radius of curvature < 30 mm.

A wide choice of substrates has been reported in [137]. Due to the high temperature required

by the semiconductor process, polymeric substrate with glass transition temperature < 300 °C like PET and PEN are excluded.

Flexible glass can withstand very high process temperatures (> 500 °C) and its oxide structure makes it an excellent environmental barriers. However it is fragile, expensive and 50 µm sheets fracture under 30 mm radius of curvature [138].

Polyimide (PI) is a good compromise between flexible glass and polyethylene terephthalate (PET). Sheets of PI can bend at low radii of curvatures < 50 mm, compatible with high-temperature processes. Some PI can be used at temperature > 500 °C [139]. It is a polymer, and, therefore, requires an additional passivation and a buffer layer to process an AOS on top. Additionally, PI can be used as a frame for DEAs [140] and SMD components can be soldered on top of it using standard soldering.

As a consequence, we decided to select PI as the substrate to build our HVTFTs on.

4.3.3 Dielectric

Selection of the gate dielectric material

Table 4.5 – Comparison between dielectric materials typically used for ZTO TFTs and comparison between the different processes used to deposit them (adapted from [3–5]

Metal oxide dielectrics: materials			
	K constant	Breakdown field (MV/cm)	HVTFT FoM (Jain [3])
Alumina	9	7	441
Silica	4	10	400
Hafnia	40	3	360
Zirconia	23	3	207
Metal oxide dielectrics: process			
	Coverage	Interfacial defects	Thickness uniformity
Sputtering	+	- - -	+
Oxidation of metal	+	+	+
MOCVD	+++	++	++
ALD	+++	++	+++

The figures of merit of a dielectric are its breakdown field and its relative dielectric constant. The breakdown field of a dielectric determines the maximum breakdown voltage a dielectric can withstand at a fixed thickness and the dielectric constant directly relates to the transconductance. There is a relation between a dielectric constant and the breakdown strength with the relationship established by Jain et al. (see Figure 4.11 [3]):

$$J = \varepsilon_r \cdot E^2_{bd_{MV/cm}} < 400 \tag{4.20}$$

J is called Jain's constant, a figure of merit judging both the dielectric breakdown and the dielectric constant (for transconductance) for HVTFTs.

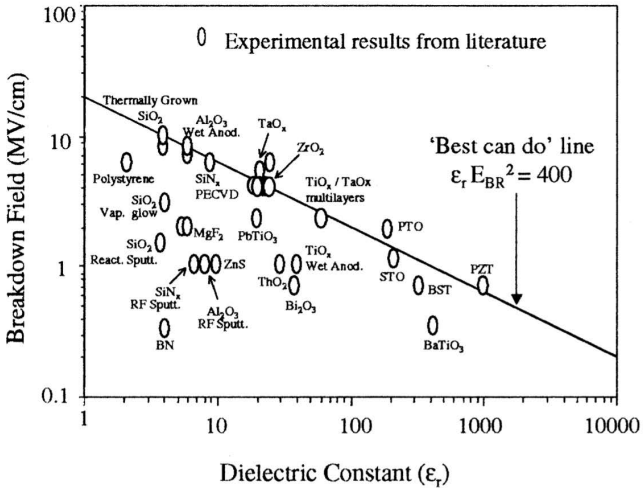

Figure 4.11 – Theoritical limit for dielectric constant and breakdown field from [3]. Jain's constant reach a theoritical limit at 400 and there is a trade-off between the dielectric constant and the breakdown field at this value.

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Figure 4.11 shows a plot with different dielectrics on a breakdown-field-dielectric constant chart [3] and Table 4.5 shows typical dielectrics implemented in ZTOs TFTs. In ZTO TFTs, alumina [88, 129, 141], zirconia [142, 143], hafnia, silica [127, 134] as a gate dielectric. The dielectrics classically used for HVTFT have high Jain's constant around the theoritical maximum, 400: Silicon nitride has a Jain's constant of 390, alumina(E_{bd} = 7 MVcm^{-1} ; ε_r = 9), used as a dielectric in CdSe HVTFT and in AOS TFTs [1, 75] has a Jain's constant of 440 (E_{bd} = 7 MVcm^{-1} ; ε_r = 9). Finally, the Parylene-C (E_{bd} = 4 MVcm^{-1} ; ε_r = 3), used in the work of Smith et al. [103, 104] is to our knowledge, the flexible polymer with the highest Jain's constant (48), due to its high 4 MVcm^{-1} breakdown field.

An additional feature we are looking for, is the compatibility of the ZTO layer with the dielectric deposited. It means achieving a good coverage to avoid pinholes, to avoid interfacial defects damaging the conduction, and have a good thickness uniformity over a large area. These parameters depend usually on the deposition process used (see Table 4.5 [4]). Metal oxide dielectrics can be deposited by sputtering, metal oxidation, metal organic chemical vapor deposition (MOCVD) and atomic layer deposition (ALD). Table 4.5 reports a comparison between the different deposition methodologies. The one enabling the best coverage, the least amount of interfacial defects and thickness uniformity is ALD [4]. ALD is a methodology enabling deposition of monolayers of atoms one by one to form the dielectric.

We select ALD Alumina as a first dielectric layer to serve as an interface between the semicon-

ductor and the dielectric. Alumina has a Jain constant of 440 , making it an excellent material with good breakdown capabilities and a decent dielectric constant, 9. The use of this material provides stable AOS TFT characteristics [88, 132]. Alumina was combined with another dielectric, a flexible one so that the dielectric has a high breakdown voltage above 100 V. We added a layer of Parylene-C on top of the Aluminum layer to form a dielectric stack. Compared to other dielectrics, Parylene-C has the advantage of being flexible at a thickness above 100 nm with a Jain constant of 50 (Ebd = 4 MV.cm-1 ; Eps = 3), caused by a high breakdown field. Parylene-C can also act as an excellent passivation layer. The drawback of Parylene-C is its low dielectric constant leading to low dielectric surface capacitance in a TFT structure.

Additional advantages in the use of multi-layers dielectrics

Using several material layers leads to the combination of their properties: The breakdown voltage sum up and the equivalent dielectric constant $\varepsilon_{r_{eq}}$ of the total material is obtained from the equivalent capacitance of two capacitors 1 and 2 in serie:

$$\varepsilon_{r_{eq}} = \frac{t_{tot}}{\frac{t_1}{\varepsilon_{r_1}} + \frac{t_2}{\varepsilon_{r_2}}} \tag{4.21}$$

where t_{tot}, t_1, t_2 are the total thickness, the thickness of material 1 and 2, respectively, and ε_{r_1} and ε_{r_2} the relative dielectric constants of material 1 and 2.

An advantage in the use of multilayer materials as HVTFT dielectric is the decrease in the probability of pinholes presence probability. As increasing the length of the channel is critical to diminish the high electric field effects presented in part, it also means that a larger area is covered by the gate, therefore the probability of pinholes presence is higher, which can be compensated by the use of stacked dielectric multilayers.

4.3.4 Electrodes

A high contact resistance between the electrodes and the semiconductor causes self-heating and hot carriers generation at high voltage. To avoid such an effect the electrodes need to be made of a metal with a workfunction of the same magnitude to the electron affinity (or conduction band distance to vacuum level) of the semiconductor. Zinc tin oxide has an electron affinity varying from 4 to 4.5 eV depending on its stoichiometry [144]. Among classical metals, the one perfectly fitting this interval is aluminum (workfunction between 4 and 4.2 eV). We will then use aluminum for the material of the electrodes.

Conclusion

In this chapter, we have presented a concept and a design for a high voltage thin film transistor (HVTFT). First, we presented the requirements of the HVTFT to switch a DEA efficiently. Then, we discussed our choice of amorphous oxide semiconductor, zinc tin oxide. Finally, we introduced the architecture of the HVTFT around the ZTO semiconductor. The ZTO HVTFT is made of a top-gate coplanar electrode structure, a solution-processed amorphous zinc tin oxide channel, a gate dielectric bilayer composed of alumina and Parylene-C at the interface of the ZTO layer. The HVTFT will be fabricated on polyimide, a substrate able to resist the high temperature required for the ZTO sol-gel process.

The next chapter will be focused on the experimental demonstration and characterization of the HVTFT. Characterizations of the ZTO semiconductor films and transistors will be presented, demonstrating their characteristics are suitable to drive DEAs. We will also develop a LT-Spice circuit model of the HVTFT. Ultimately, we will propose an optimization of ZTO thin film by doping with a strong oxygen binder, yttrium, for enhanced transistor characteristics at very high voltage.

5 Fabrication, characterization and optimization of ZTO HVTFTs

Summary

The objective of this chapter is to characterize the first high voltage thin-film transistor (HVTFT) operating at 1 kV made with an amorphous oxide semiconductor (AOS) channel, zinc tin oxide (ZTO).

We start this chapter by validating the synthesis of ZTO with the characterization of the sol-gel reaction by thermogravimetric analysis (TGA) and differencial scanning calorimetry (DSC). The ZTO synthesis was based on chloride precursors, which react between 400°C and 550°C. We demonstrated by X-ray photoelectron spectroscopy (XPS) that the thin film synthesized is mostly composed of zinc, tin and oxygen and that more than 80% of the oxygen bonds are metal oxide bonds. Then the amorphous character of the thin film was confirmed, a key requirement to avoid grain-boundaries effects in the thin film semiconductor.

Then we describe the architecture and process flow of the ZTO HVTFT. We characterized TFTs and HVTFTs made of ZTO with and without an offset gate and with and without an extra-Parylene-C layer at the gate dielectric. The different devices exhibited similar saturation mobility of about 0.1 $cm^2 V^{-1} s^{-1}$. The devices without parylene-C and no offset gate could operate up to 10 V. The devices with Parylene-C and no offset gate could operate up to 100 V. The devices with Parylene-C and with a 150 µm offset gate could operate up to 1 kV, an unprecedented operation voltage for thin-film transistors (TFTs). An equivalent DC-circuit model is proposed for the HVTFT taking into account the high electric field effects.

Finally, we optimized the HVTFT electrical properties by doping the semiconductor with 5% yttrium. It resulted in an increase of mobility from 0.1 to 1 $cm^2 V^{-1} s^{-1}$. The high electric field effects such as space charge limited current (SCLC) and potential barrier were strongly attenuated thanks to yttrium doping of ZTO.

The results presented in this chapter were included in a journal paper in *Advanced Materials* [24] and a proceedings of *the International Conference on Solid-State Sensors, Actuators and*

Microsystems [145].

5.1 Validation of amorphous zinc tin oxide synthesis

In this section we demonstrate the successful synthesis of the AOS zinc tin oxide by a sol-gel process. In order to characterize the reaction temperatures and events, we analyzed the TGA and the DSC of the sol-gel reaction. Then, we proved that the ZTO was composed of zinc, tin and oxygen without precursor residuals by measuring the XPS spectrum of ZTO. We showed that the alloying process was complete by deconvoluting the metal-oxide spectrum from the oxygen peak. Finally, we showed that synthesized thin-film was amorphous by X-ray diffraction (XRD) characterization.

5.1.1 Characterization of the sol-gel reaction by TGA and DSC

To characterize the reaction temperature of the sol-gel process, we performed a TGA and a DSC analyses. A TGA is a measure of a mass-loss with increasing temperature of a sample. Sharp mass-losses are characteristic of sol-gel reaction. A DSC probe measures the heat flow in the sample, while the temperature increases. A crystallization is usually triggering a strong exothermal peak that can be detected by DSC.

The precursors were commercial zinc chloride and tin chloride from Sigma-Aldrich. The solvent was a mix of acetonitril and ethyleneglycol from Sigma-Aldrich. The solute concentration was 0.2 M. Zn:Sn = 2:1, the ideal stoichiometry mentioned in several reports for ZTO [88, 127, 135]. The solute was dissolved in 65% ethyleneglycol and 35% acetonitril. The role of ethyleneglycol was to increase the viscosity of the precursor solution. This solution was based on the one described by Avis et al. [88].

The TGA and DSC ZTO samples were prepared as follows. First, acetonitril and ethyleneglycol were mixed together at room temperature. The solute were added and stirred for 24 hours at room temperature under air. When the solution became homogeneous, it was annealed for 24 hours in air at 120°C to evaporate most of the liquid until obtaining a paste. The paste was then put in the TGA scale. The TGA and DSC data were acquired by sweeping the temperature from 25°C to 800°C. The TGAs and DSCs data were acquired by Mathilde Rieu (Ecole des Mines de Saint-Etienne).

Figure 5.1 shows the TGA and DSC curves as a function of temperature. On this curve, we read 4 different events, 3 from the TGA and 1 from the DSC:

1. The first one occurs from room temperature to 100°C. It could be indicating evaporation of humidity;
2. The second event occurs from 230 to 300°C and corresponds to the evaporation of organic species and HCl;
3. The third event occurs from 400°C to 550°C and corresponds to the oxide formation, and the evaporation of the last chloride species;

4. The fourth event is a peak in the DSC centered at 540 °C. It might be caused by a crystallization event in the zinc tin oxide thin film as observed in [131, 146].

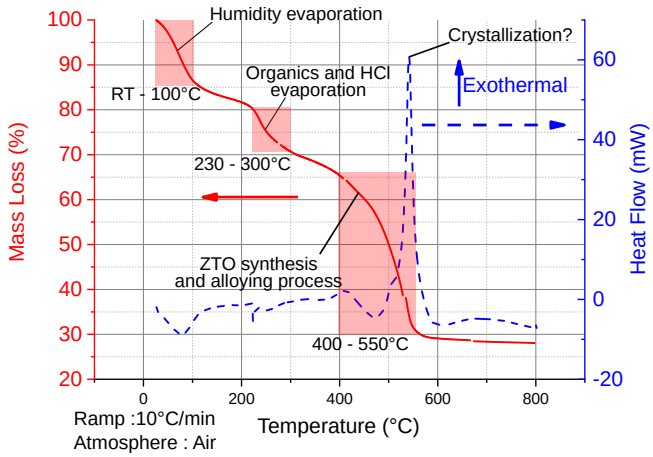

Figure 5.1 – Thermogravimetric analysis and differential scanning calorimetry of the precursor solution for ZTO. The precursor solution is made of zinc chloride and tin chloride dissolved in acetonitril (35% volume) and ethyleneglycol (65% volume). The solute has a total concentration of 0.2 M and Zn:Sn = 2:1.

From that, we can conclude that ZTO formation occurs between 400°C and 550°C. However zinc, tin or both oxides appear to form poly-crystals around 540°C.

5.1.2 Characterization of the zinc tin oxide chemical composition by XPS

We verify the synthesis of ZTO at 450°C by XPS. An XPS analysis measures the photoelectrons emitted by the surface of a sample after X-Ray exposure. The energy spectrum of the detected photoelectrons directly correlates with a specific material and its relative quantity in a sample.

We deposited the ZTO precursors on a 10 cm in diameter polyimide foil (Upilex-S, UBE) coated with a 20 nm ALD alumina film by spin-coating at 2000 rpm to obtain a 40 nm thick film (confirmed by ellipsometry). The film was annealed at 120°C. The film was analysed before and after curing at 450°C. This type of polyimide can withstand a very high temperature > 500°C. However, we have noticed in our experiments that it was starting to deform from 450°C, making processing of HVTFTs impossible above this temperature.

In order to analyse the zinc tin oxide molecular bonding we analysed the oxygen XPS spectra of the surface of the zinc tin oxide thin film and of the bulk of the zinc tin oxide thin film. The bulk measurement was taken 10 nm below the surface. The oxygen spectrum bears the essential part of the information on the alloying process. The oxygen spectrum was deconvoluted at 529.5-530.5 eV, 531.4 eV and 532.5 eV for the respective identification of the metal oxide bonds, the oxygen vacancies and the carbon-oxide bonds. A MOx bond represents a covalent bond between the metal and the oxygen. Oxygen vacancies can play different roles in a AOS

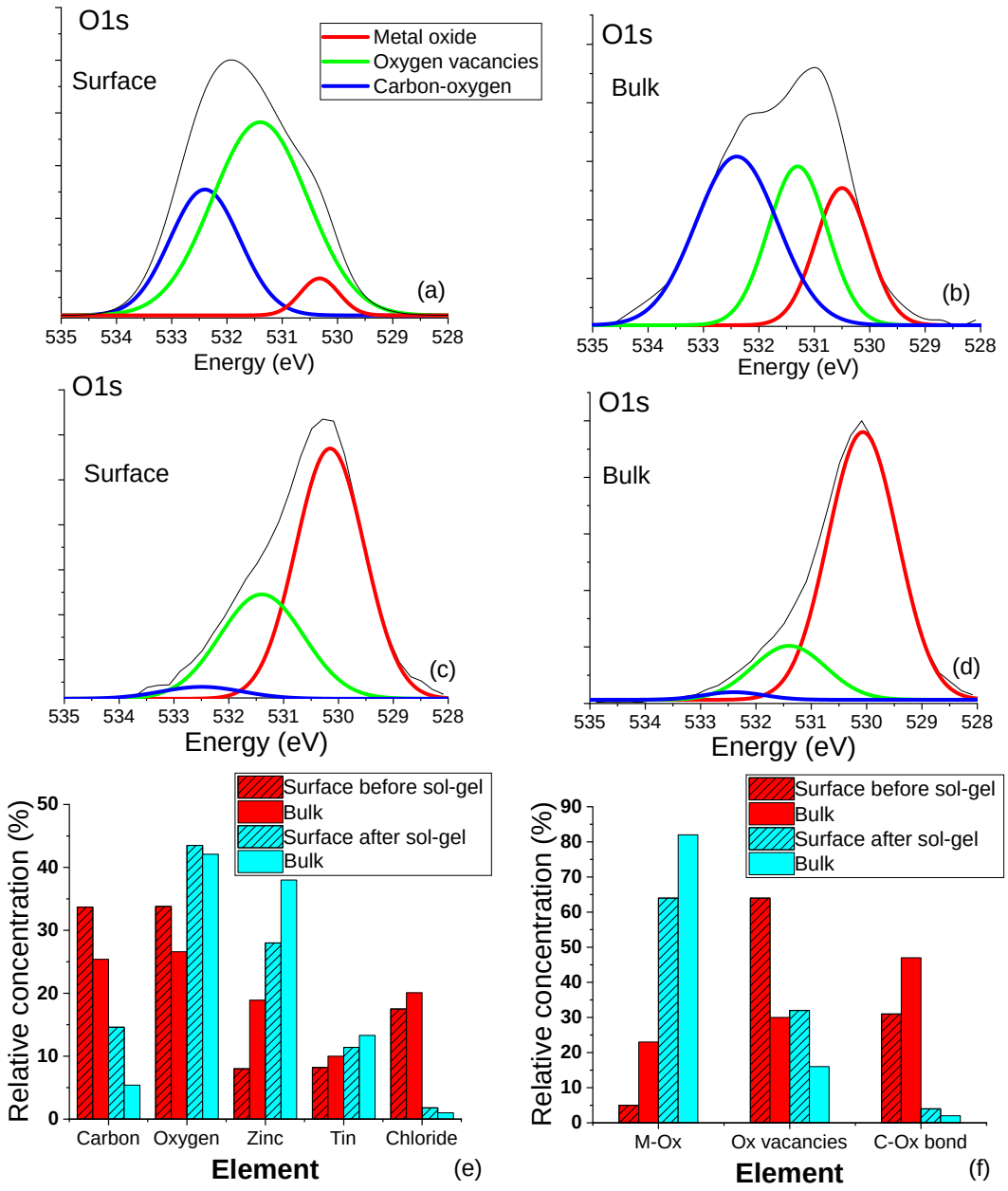

Figure 5.2 – Surface and bulk XPS spectra of ZTO for compositional analysis before and after sol-gel, (a) and (b) Oxygen (O1s) spectra before sol-gel respectively at the surface and 10 nm below the surface of ZTO, (c) and (d) Oxygen (O1s) spectra after sol-gel respectively at the surface and 10 nm below the surface of ZTO, (e) Summary of the relative concentration of carbon elements (contaminants or from organics), oxygen, zinc, tin and chloride elements, (f) Summary of the relative concentration of metal oxides, oxygen vacancies and carbon-oxygen groups obtained by deconvolution of peaks (a), (b) and (c).

thin film, depending on the size of the vacancy site [147]. They can play the role of shallow donors, leading to an increase in mobility [127], electron traps, leading to a drop in mobility and SCLC [91, 127]. The absence of oxygen coordination due to incomplete alloying can also lead to the formation of electron traps [148].

Before sol-gel: Figure 5.2a and b present the surface and bulk oxygen XPS spectrum before the sol-gel process. We can see that the carbon-oxygen bonds and the oxygen vacancies are more abundant than the metal oxide bonds: 5% of the oxygen signal at the surface and 23% in the bulk. It is coherent as the main oxygen contributions are coming from organic ethyleneglycol ($C_2H_6O_2$) and acetonitril (C_2H_3N) including hydroxide bonds and carbon-oxygen bonds. As the alloying process has not started, very few oxygen atoms contribute at this stage to a metal-oxide alloy. The high abondance of oxygen vacancy or hydroxides at the surface (60%) vs the bulk (30%) might be due to the humidity and contaminants adsorbed by the thin-film.

After sol-gel: Figure 5.2c and d present respectively the surface and bulk oxygen XPS spectrum after the sol-gel process. We notice in both cases that the deconvoluted metal-oxide spectrum is dominating the other spectra (62% concentration at the surface and 83% in the bulk), demonstrating thus the formation of the ZTO thin film. The deconvoluted spectrum of the carbon-oxide bond is almost negligible, demonstrating the absence of remaining organic species, confirming thus the TGA. Like before, the spectrum for oxygen vacancies/hydroxides is twice larger at the surface (33%) than in the bulk (15%).

In Figure 5.2e, we plotted a summary of the relative stoichiometry of the elements present in the thin film. In particular, the chlorides and the carbon have almost disappeared after the thermal annealing at 450°C, and this, in conjugation with the abundant metal oxide peaks in the oxygen spectra, demonstrates that the sol-gel process resulted in the synthesis of the ZTO thin film.

5.1.3 Validation of amorphicity by XRD analysis

In the previous chapters, we have seen that a semiconductor for HVTFT should not be polycrystalline to avoid grain boundaries. We characterized the ZTO thin film by XRD on polyimide. Figure 5.3 reports the XRD spectrum of the ZTO thin film on polyimide. These measurements were realized by Ivan Marozau (CSEM-Neuchâtel). In this figure, the XRD spectrum of the substrate is plotted in parallel to the one of the ZTO thin-film. We see that no crystalline peak is apparent in the spectra demonstrating thus that the ZTO thin film synthesized at 450°C is amorphous.

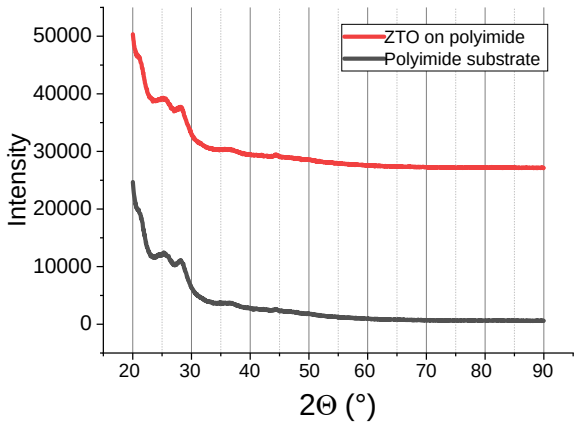

Figure 5.3 – X-ray diffraction spectrum of ZTO on polyimide substrate after sol-gel synthesis. The spectrum of the polyimide substrate is used as a reference. No peak characterizing a crystalline phase of the ZTO thin film appears on the spectrum. Therefore the film is amorphous.

5.1.4 Discussion

The synthesis of an amorphous ZTO thin film has been demonstrated. We first showed the successful sol-gel reaction of zinc and tin chloride precursors in acetonitril and ethyleneglycol with a TGA and DSC. This curve is similar to what has been reported in the literature for chloride precursor synthesis [136]. It highlights three different mass-loss events: humidity evaporation up 100°C, organic species evaporation between 230°C and 300°C and metal oxide synthesis between 400°C and 550°C. We have proven by XPS that the ZTO was already synthesized at 450°C, when deposited on alumina coated polyimide (PI). The metal-oxide concentration relative to the oxygen vacancy concentration differs slightly from the one reported in the literature at this stoichiometry. Kim et al. reported 15% oxygen vacancy concentration and 25% carbon-oxide concentration for 60% metal oxide for the same synthesis temperature [127]. Compared to it, our thin films have a remarkably low concentration of C-Ox bonds (< 5%) after the reaction but the amount of oxygen vacancy at the surface of the thin-film is twice higher. The reason could be coming from the different zinc precursors, as Kim et al. used zinc acetate, when we used zinc chloride [127]. The high number of oxygen

vacancies could be also attributed to an incomplete alloying process, as the mass loss occurs up to 550°C in the TGA as suggested in [149].

5.2 HVTFT process flow

In this section, we describe the fabrication of a 1 kV thin ZTO HVTFT on polyimide foil. The process flow is shown in Figure 5.4. We describe each process step to achieve a working device.

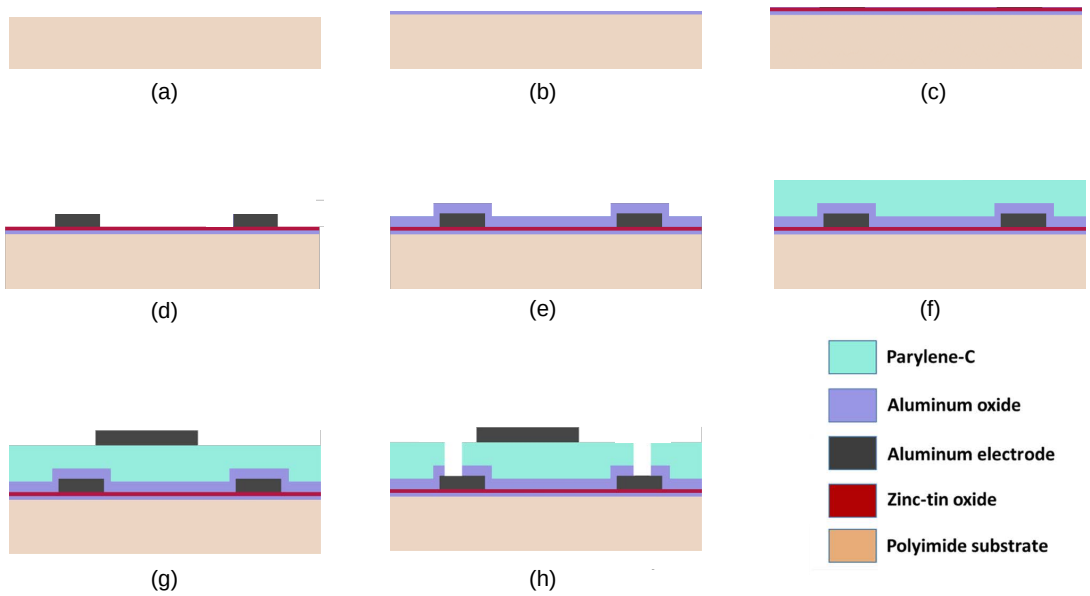

Figure 5.4 – HVTFT process flow. (a) Substrate preparation (Upilex-S), (b) Substrate passivation (Alumina), (c) Semiconductor deposition (ZTO), (d) Source and drain deposition (Aluminum), (e) Dielectric layer 1 deposition (Alumina), (f) Dielectric layer 2 (Parylene-C), (g) Offset gate alignment and deposition (Aluminum), (h) Source and drain contacts opening.

5.2.1 Substrate and alumina coating

50 µm thick Upilex-S (UBE) was used as the substrate. Upilex-S is a polyimide substrate made to withstand high temperature. The glass transistion temperature of Upilex-S is higher than 500°C [139]. However, experimental testing showed that the film starts to buckle and deform at t > 450°C. The roughness of Upilex is 2 nm, which is twice lower than for standard polyimide. We coat the Upilex foil with a 20 nm Al_2O_3 layer deposited by atomic layer deposition (ALD). ALD is performed under vacuum at 200 °C in a Beneq TFS200 reactor using trimethylaluminium (TMA) and H_2O as the precursors. The thickness of the layers characterized by ellipsometry was of 20 nm. Al_2O_3 serves as a passivation layer, preventing humidity and gas absorption from the back-channel of the HVTFT, to which ZTO is sensitive [150]. It also serves as a buffer layer for the ZTO semiconductor to grow, enabling a high concentration of oxygen atoms on top of the substrate compared to other materials such as silica [88]. Before semiconductor deposition, the substrate with its passivation layer are plasma treated to improve wettability. The plasma uses oxygen, the time of exposure is 30 s and the power is 50 W.

5.2.2 Semiconductor deposition

The synthesis of ZTO was based on the process described in the previous section. The precursor solution is made of zinc chloride and tin chloride dissolved in acetonitril (35% volume) and ethyleneglycol (65% volume). The solute has a total concentration of 0.2 M and Zn:Sn = 2:1. The ZTO precursors are deposited by spin-coating at 2000 rpm and cured first at 120°C for 1 hour (No ramp) in air. The sol-gel reaction is triggered by curing at 450°C during 1 hour in air (No ramp). The resistivity of the semiconductor was measured and is in the order of 40 Ωm, a typical value for semiconductors, demonstrating that this material can conduct electrons.

5.2.3 Dielectric deposition

The gate dielectric is a bilayer composed of a first layer of Al_2O_3 (100 nm) and a layer of Parylene-C (1 µm). The equivalent dielectric constant is ε_{eq} = 3.2, logically similar to the one of parylene-C, 10 times thicker than Al_2O_3. Al_2O_3 is deposited by ALD. ALD is performed under vacuum at 200 °C in a Beneq TFS200 reactor using TMA and H_2O as the precursors. Parylene-C is deposited by chemical vapor deposition with a COMELEC c-30-s machine at room temperature.

5.2.4 Electrodes deposition

The electrodes were deposited by e-beam evaporation through a shadow-mask in stainless steel of 50 µm thickness from PCB-pool. The alignment of the gate mask was made under an optical microscope to align the offset gate with the rest of the structure.

5.2.5 Post-annealing bake

Gupta et al. showed that a post annealing bake at 150°C step was necessary to increase the performance of a AOS semiconductor [151]. From our experiment, we saw that the absence of such a post-annealing bake step led to non-functional HVTFTs. The TFTs with no annealing have a conductive channel, not switching. The switching effect appears with the decrease of conduction after 120°C annealing. The best results we obtained were after 150°C annealing.

5.3 Transistor electrical characteristics: Results and discussion

In this section, we demonstrate the operation of the first 1 kV ZTO HVTFT. We characterize the HVTFT and compare it with its low-voltage counterparts in order to be able to analyze the effects specific to our process from the one related to the HVTFT. Figure 5.5 shows a picture with arrays of HVTFT fabricated on foil and a description of a HVTFT without (Figure 5.5b) and with an offset gate (100 µm offset gate in Figure 5.5c).

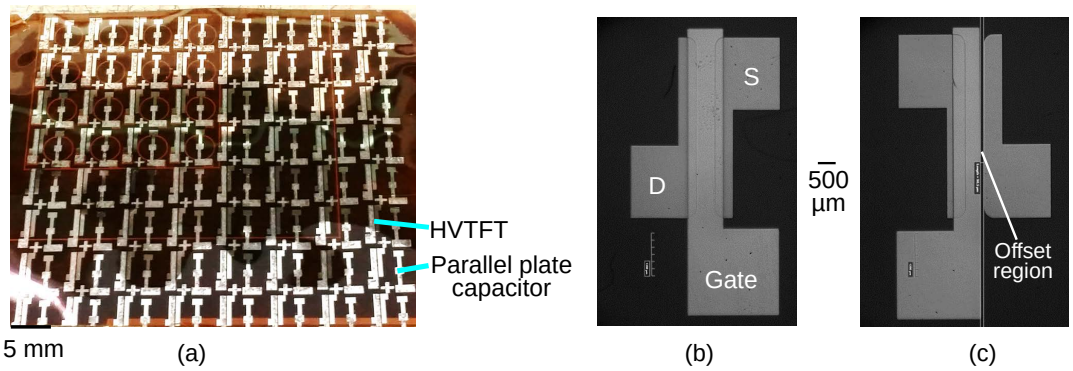

Figure 5.5 – Picture of the fabricated HVTFT (a) An array of HVTFTs, (b) A HVTFT with no offset gate, (c) a 100 µm offset gate.

5.3.1 Characterization setup

A dedicated setup to characterize HVTFTs was developed. It can apply drain voltage from 0 to 2 kV and gate voltage from 0 to 200 V. Figure 5.6a shows a picture of a HVTFT batch probed on the high voltage setup. Figure 5.6b shows a picture of the setup hardware. A first generation only included two positive voltage DC-DC converters and a current detector. Only positive voltage characteristics were possible. The second generation included positive and negative voltage power supplies and a voltage detector was added to measure the voltage between the drain and the source of the HVTFT. The hardware (Figure 5.6b) was developed in collaboration with Aymeric Schafflützel (CIFOM) and Olexandr Gudozhnik (EPFL-LMTS). The plans of the current detector had been developed by Dan Courtney (EPFL-LMTS) for a previous project. I designed the software (Figure 5.6c) on labview to communicate and interpret information from the DAQ.

The high voltage power supplies are made of commercially available regulated power supplies (EMCO-20P for the 2 kV and EMCO-02P for the 200 V power supply) including DC-DC converters transforming a control voltage from 0 to 5 V into a proportional high-voltage signal from 0 to 200 V (resp. 0 to 2 kV). In the latest version of the characterization box, negative DC-DC converters are also included to apply gate and drain voltage < 0 V. In order to measure the output current (drain-source current) we used a current to voltage amplifier made to measure a current range from 10 nA to 1 mA. The current detector integrates operational amplifiers, photodiodes, separating the high-voltage bias from the low-voltage measurement section.

Five different gains are available to be able to detect low to high currents. The voltage detector is made of a high-voltage follower in parallel to a high impedance (10 GΩ) voltage divider. It enables the detection of the voltage applied across the transistor channel, which has been particularly useful to detect the voltage across the dielectric elastomer actuator (DEA).

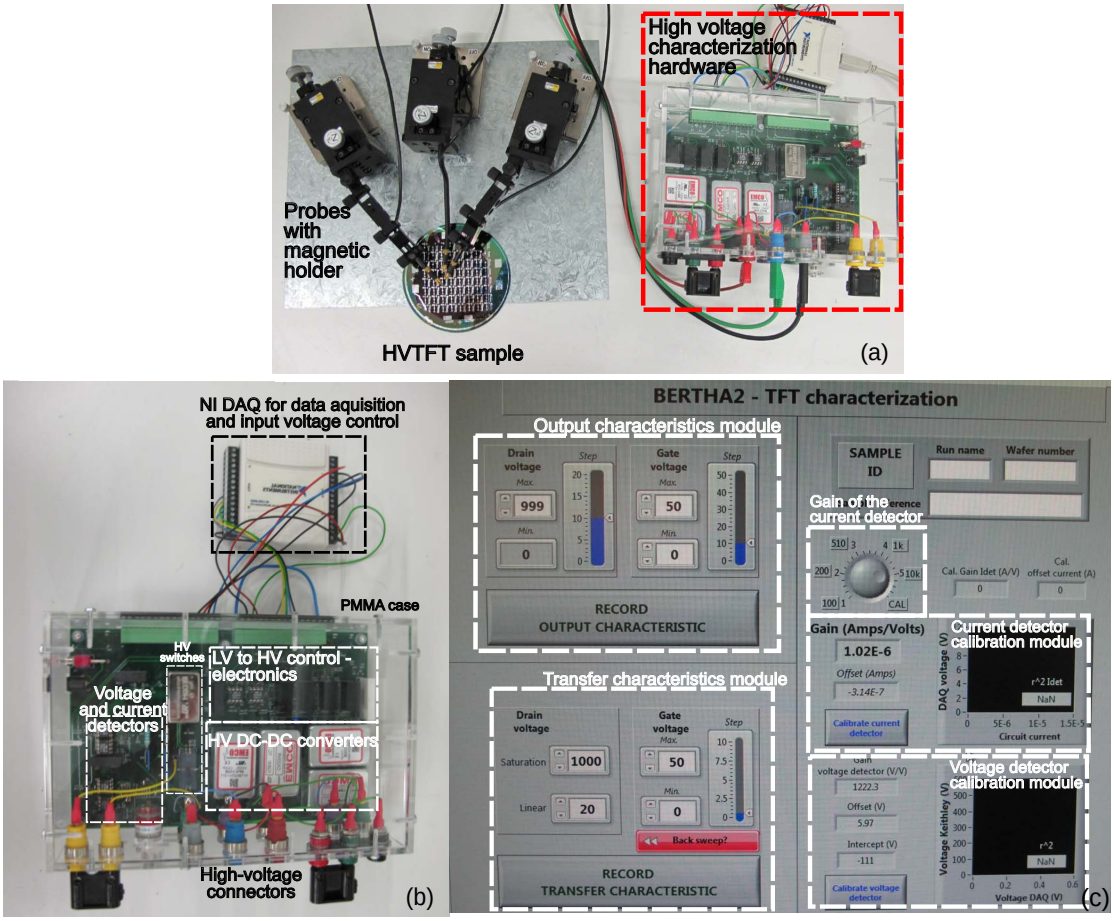

Figure 5.6 – High-voltage characterization setup: (a) Picture of the high voltage characterization setup measuring a probed HVTFT, (b) Picture and description of the different building blocks of the high voltage characterization setup harware, (c) Picture and description of the front-end pannel of the Labview-based software made to communicate to the high voltage characterization setup.

The circuits of the characterization setup, the voltage and the current detector are shown Figure 5.7 and Figure 5.8. The voltage applied by the DC-DC converter is controlled by a DAQ from National intruments, enabling the application of a very accurate analog voltage between 0 and 5 V. The DAQ can also detect a 0-12 V signal coming from the current and the voltage detectors. The software program converts the voltage signal back to the real voltage and the real current across the transistor channel. In order to measure very accurate data, two calibration modules for the voltage and current detector have been implemented in the software (see Figure 5.6c).

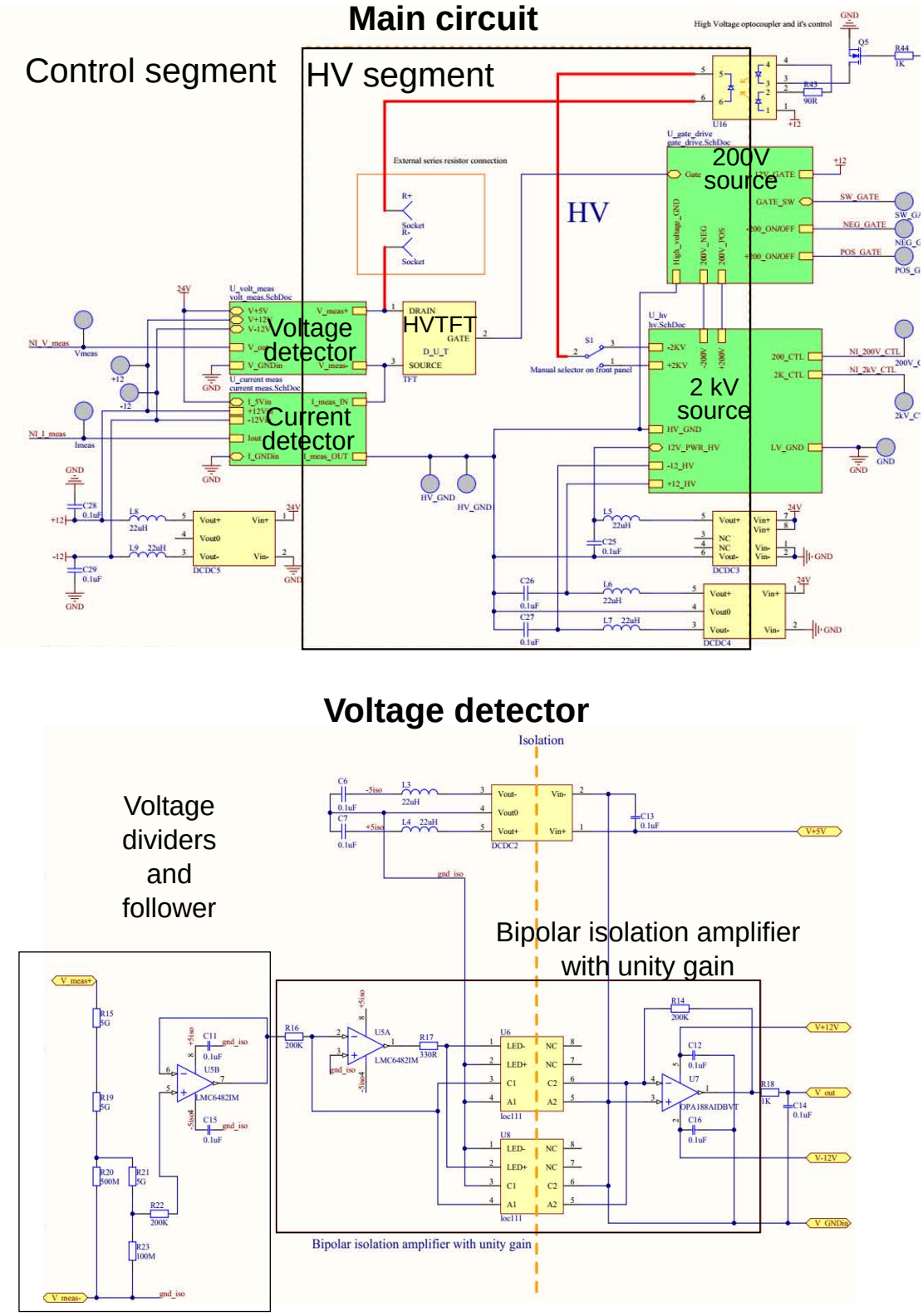

Figure 5.7 – Circuit of the high-voltage characterization setup (Part 1).

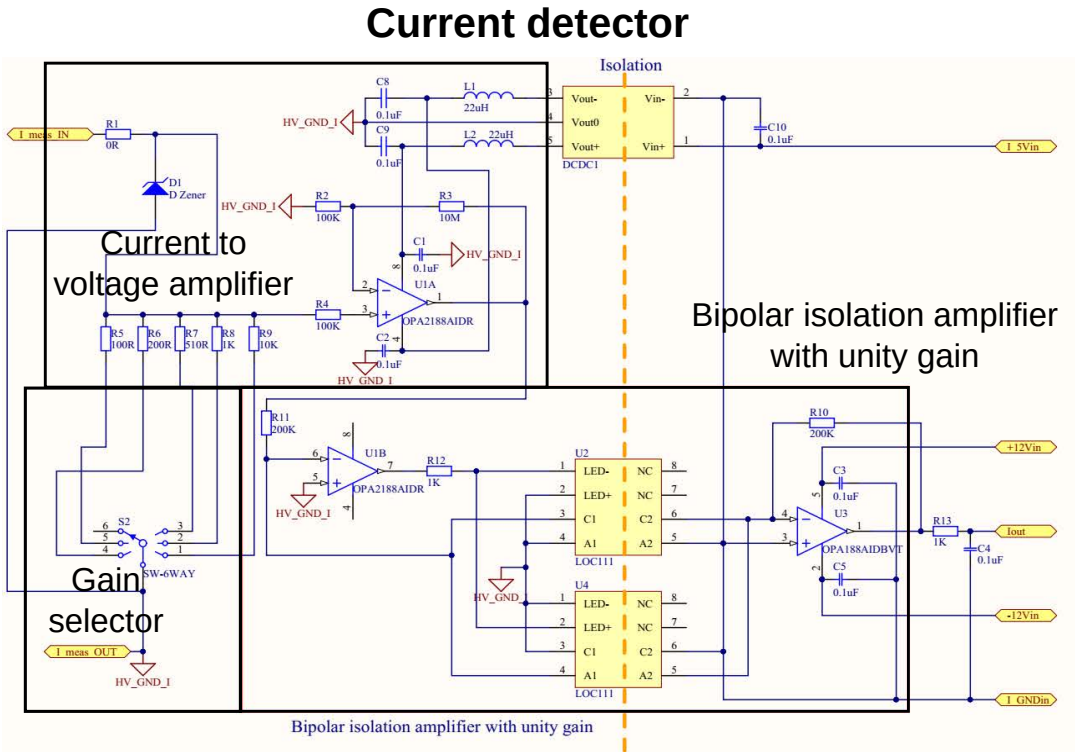

Figure 5.8 – Circuit of the high-voltage characterization setup (Part 2).

The high voltage segments are separated from the low-voltage control segments by bipolar isolation amplifier with LEDs transmitting optically the detected signals to the DAQs. Additionally, high voltage optocouplers have been implemented to switch on and off in several µs the gate and drain voltage signal for transient characteristics measurements.

5.3.2 Analysis methodology

The breakdown voltage is measured on an output characteristics such as shown in Figure 5.9a. The gate voltage V_{gs} was set at 0 V. The drain voltage V_{ds} was then swept from 0 V to breakdown voltage. The breakdown voltage is defined by the sudden increase of the drain current I_{ds} out of the output characteristics linear fit (Ohmic curve if the gate voltage is under threshold at 0 V or saturation curve if the gate voltage is above threshold at 0 V). The mobility and threshold voltage fits were obtained from the methodology described in Figure 3.2 previously. We only extract the saturation mobility as the presence of the offset gate makes the measurement of the linear and the field effect mobility unreliable. An example of such an extraction is provided Figure 5.9b. The case taken is a transfer characteristics of an HVTFT operating at 1 kV. The mobility is extracted from the slope of the curve obtained by linear fit. The threshold voltage is obtained from the junction between the gate voltage axis and the fitting curve. We only considered linear fits with $r^2 > 0.99$.

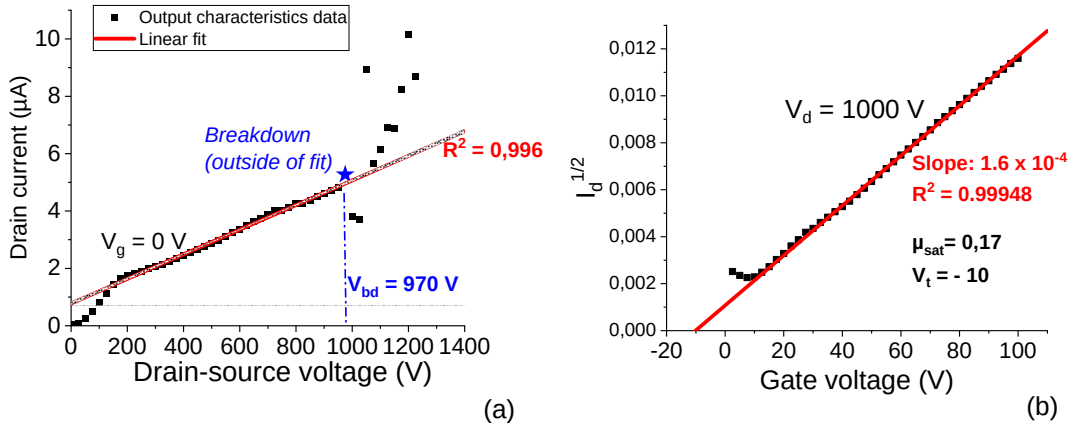

Figure 5.9 – (a) Example of output characteristics with breakdown voltage analysis. The fit is made on the post-linear region of the curve. The first current value outside the fit at high voltage is defined as the breakdown voltage of the transistor. (b) Example of transfer characteristics with square root of I_d represented in the y-axis. The saturation mobility is extracted from the slope of the fitted curve and the threshold voltage is obtained at the junction between the x-axis and the fitting curve.

To represent the data, at least five transistors were tested per foil. The error is represented by the standard deviation over one foil composed of these transistors. The results were reproduced over three runs for the ZTO HVTFTs operating at 1 kV.

5.3.3 HVTFT characteristics

First we characterize the breakdown voltage as a function of the offset gate length. After that, we measure the output and transfer characteristics for TFTs operating at 10 V, 100 V and a HVTFT operating at 1 kV. The yield of the ZTO HVTFTs with Parylene-C with and without offset gate was higher than 90%. The yield of the ZTO TFTs with no Parylene-C was less than 20%. This was mainly due to short circuits between the channel and the gate probably caused by pinholes.

Breakdown voltage

The breakdown voltage of the HVTFTs was first characterized as a function of the dielectric and the offset-gate geometry.

Figure 5.10 shows the measured breakdown voltage as a function of the offset gate length. The breakdown voltage of the HVTFTs without Parylene-C and a fully overlapping gate is in the order of 65 V. The addition of Parylene-C in the gate dielectric layer leads to an increase of the breakdown voltage to 430 V. An offset gate of 50 µm leads to a breakdown voltage of 800 V. The increase to 100 µm leads to a breakdown voltage of 920 V. Finally, a 1.1 kV breakdown voltage

of 1.1 kV was achieved for HVTFTs with a 150 µm offset gate.

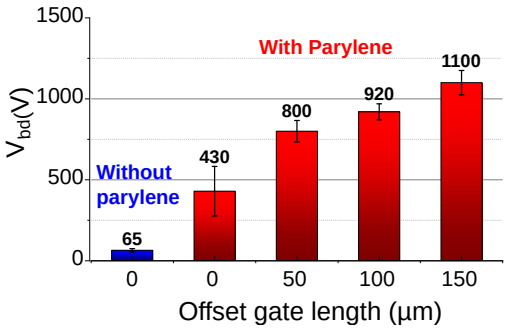

Figure 5.10 – Characterization of the breakdown voltage as a function of the offset gate length. The value for a TFT without Parylene-C is put as a reference. The error bar represents the standard deviation.

We notice that the presence of the Parylene-C leads to a 370 V increase of breakdown voltage contribution. The offset gate leads to a 570 V increase of breakdown voltage for a 150 µm offset gate. The breakdown voltage trend with increasing offset gate is similar to the one shown by Unagami et al. [100]. The initial increase is high and then it slightly increases for higher offset distance values. The breakdown events occur at the edge between the gate and the channel, suggesting a gate dielectric breakdown.

IV characteristics

We characterized the output and transfer characteristics of the HVTFTs and compared it with TFTs fabricated with and without Parylene-C but no offset gate. The procedure is the following one. We incremented the gate voltage by 10 V steps for the samples with Parylene-C samples and 2 V steps for the samples without Parylene-C. For a given gate voltage, the drain voltage was swept from 0 to 10 V for the samples without Parylene-C and no offset gate, 0 to 100 V for the samples with Parylene-C and no offset gate, and from 0 to 1 kV for the HVTFTs with Parylene-C and an offset gate of 150 µm. For the transfer characteristics, we fixed the drain-source voltage at 10 V for the TFT with no Parylene-C and no offset gate, we fixed it at 100 V for the TFTs in Parylene-C without an offset gate, and at 1 kV for the HVTFTs with Parylene-C and an offset gate of 150 µm. The drain voltage was swept from 0 to 10 V (No Parylene-C, no offset gate) and 0 to 100 V for both the other cases. Figure 5.11 shows the output characteristics for the TFT operating at 10 V with no Parylene-C, at 100 V with only Parylene-C and at 1 kV with Parylene-C and an offset gate of 150 µm.

Figure 5.12 shows the transfer characteristics for a TFT operating at 10 V with no Parylene-C, a TFT at 100 V with Parylene-C and no offset gate and the HVTFT operating at 1 kV with Parylene-C and an offset gate of 150 µm.

Table 5.1 summarizes the extracted HVTFTs parameters with the requirements. We analysed

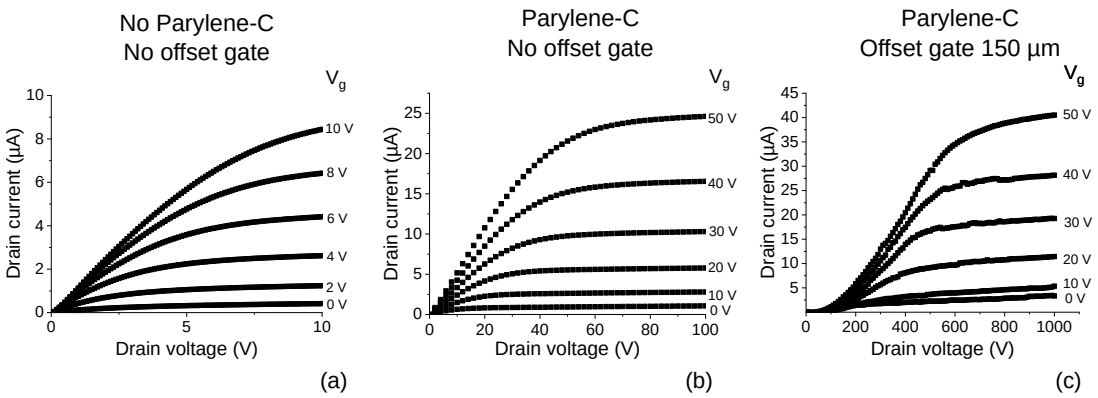

Figure 5.11 – Output characteristics of ZTO TFTs. (a) TFT without Parylene-C, (b) TFT with Parylene-C and (c) HVTFT with Parylene-C and 150 µm offset gate.

the key parameters extracted from the output and transfer characteristics shown in Figure 5.11 and in Figure 5.12. The on-off ratio for the low-voltage TFT without Parylene-C and no offset-gate is 1000 for a 15 V gate voltage swing. The on-off current ratio is 100 for the Parylene-C TFT and no offset gate over a 50 V gate voltage swing. The on-off ratio of the HVTFT with Parylene-C and offset gate (150 µm) is 20 over 85 V. In order to extract the mobility we used C_{ox} =3 nF cm^{-2} for the dielectric bilayer and C_{ox} = 60 nF cm^{-2} without the Parylene-C layer.

The saturation mobility of the TFT without Parylene-C was 0.1 ± 0.03. The saturation mobility of the TFT with Parylene-C was 0.3 ± 0.2 cm^2 V^{-1} s^{-1}. The saturation mobility of the TFT with Parylene-C was 0.1 ± 0.02 cm^2 V^{-1} s^{-1}. As the interface between the gate dielectric and the gate electrode did not change, it is coherent to obtain similar mobilities for each case. The lower mobility than reported in literature for ZTO by a high concentration of electron traps in the ZTO thin film as mentioned in previous section [147, 148].

The threshold voltage was of about -4 V for TFTs with no Parylene-C, -10 V for TFTs with Parylene-C and no offset gate. The threshold voltage of the HVTFT with Parylene-C and an offset gate at 150 µm was of the order of - 10 V. However, the current response as a function of the gate voltage starts to increase between 0 and 10 V, suggesting the methodology applied to extract the threshold voltage at low-voltage operation might not be appropriate for the characterization of this parameter at high voltage.

The differences between the HVTFT and the low voltage TFT characteristics are mostly due to the effects occurring at very high voltage (> 400 V)

The addition of Parylene-C causes an increase in the on-resistance and a decrease in transconductance as seen in the characteristics shown in Figure 5.11 and in Figure 5.12. The pre-saturation region of the HVTFT is non linear for V_{gs} > 30 V. In the transfer characteristics, the off-current reaches higher values due to the linear dependency of the off-current with the voltage. It is very interesting to see that the application of a high voltage drastically and irre-

Table 5.1 – Comparison of the HVTFTs experimental results for ZTO TFT with no Parylene-C and no offset gate, ZTO TFTs with Parylene-C and no offset gate and ZTO HVTFTs

	Minimal	Optimal	TFT	TFT with Par	HVTFT
Operation voltage	500 V*	> 1 kV	10 V	100 V	1 kV
On-off ratio	20	$2{\cdot}10^3$	10^3	100	20
On-current	10 µA	1 mA	10 µA	20 µA	0.1 mA
Voltage swing	100 V*	5 V	17 V	50 V	85 V
Semiconductor cristal.	Amorphous		Amorphous	Amorphous	Amorphous
CLM	Negligible		Negligible	Negligible	Negligible

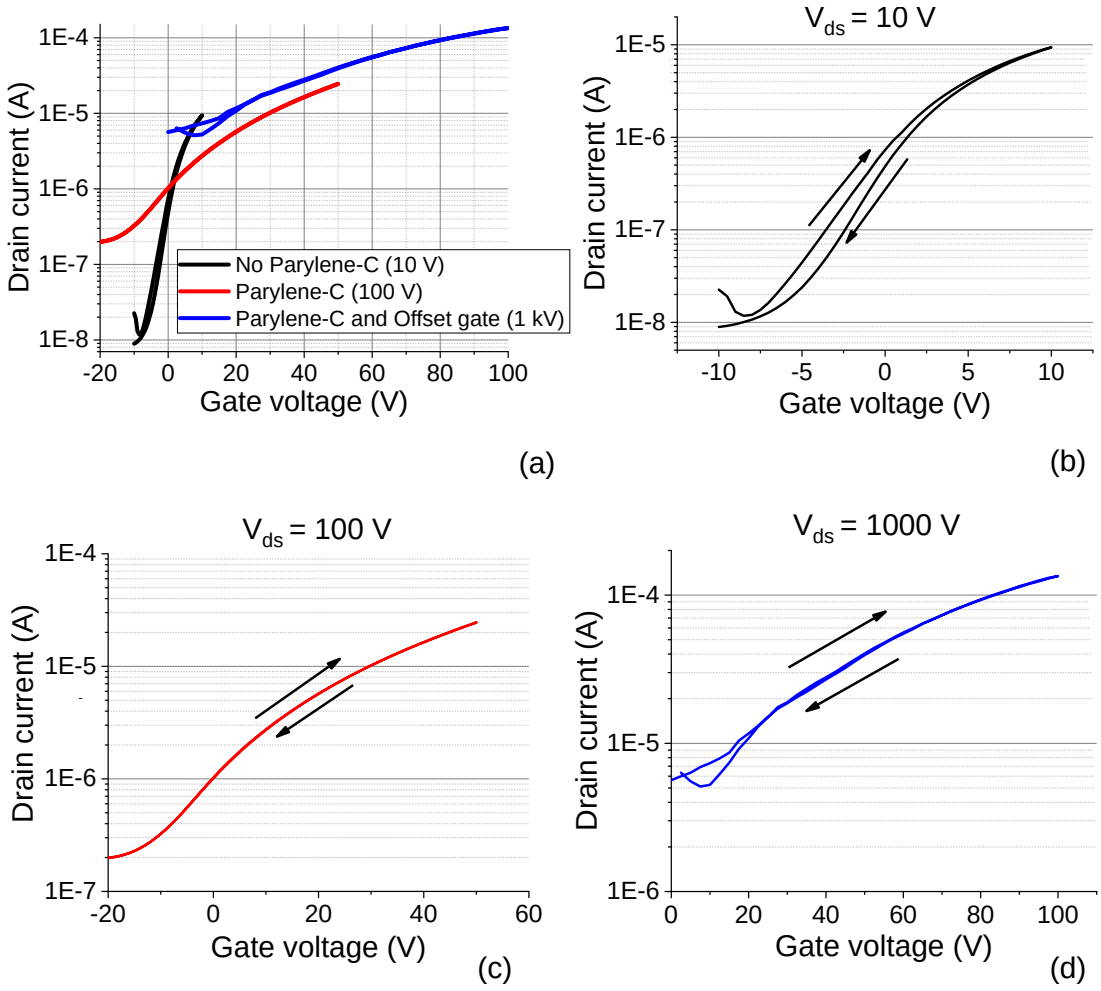

Figure 5.12 – Transfer characteristics of ZTO TFTs. (a) Summary for the three TFTs.(b) TFT without Parylene-C and no gate offset. (c) TFT with Parylene-C and no gate offset. (d) HVTFT with Parylene-C and a 150 µm offset gate.

versibly shifts positively the on-set point of the output characteristics, showing thus almost no more switching at lower drain voltage. This effect is a combination between the space-charge limited current (SCLC) and the potential barrier characterized by V_x.

V_x is defined as shown in Figure 5.13. For a gate offset of 150 µm V_x is equal to 130 ± 30 V. In its "linear" region, the curve has a quadratic shape, an evidence for the HVTFT being in the space-charge regime (see Figure 5.13b). SCLC seems to appear only for HVTFT, suggesting that, like reported in the literature, it is caused by the presence of the gate offset and by the apparition of novel traps near the gate edge [91, 103, 104] .

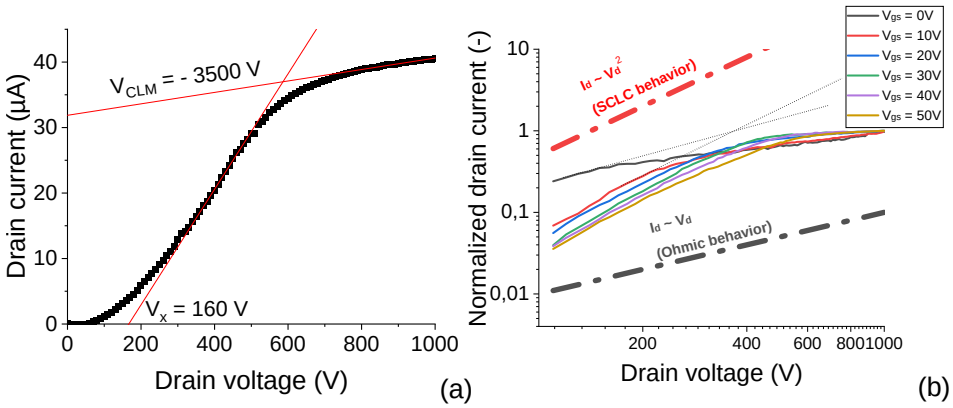

Figure 5.13 – Output characteristics of ZTO HVTFTs showing (a) The curve for Vg = 50 V with extracted potential barrier voltage value (V_x) by linear fit before the saturation region and channel length modulation voltage by linear fit in the saturation region V_{CLM}. (b) Every curve of the output characteristics, normalized by its maximum current in a logarithmic chart representation. Space charge limited current is characterized by the slope of the curves in this chart before saturation. As an indication, in dashed lines, trends for space-charge limited current behavior (in red) and ohmic current behavior (in black) have been plotted.

Another interesting feature is the limitation of channel length modulation (CLM) as the saturation current stays remarkably stable in saturation region especially compared to organic semiconductors. The value of early voltage was very high (in the order of 3500 V as shown in Figure 5.13 a), demonstrating that the choice of a metal oxide semiconductor with a long channel of 500 µm leads to a high-voltage thin film transistor with negligible channel length modulation.

In summary, we have demonstrated the first AOS HVTFT operating at 1 kV. The high voltage effects considerably reduce its performance in term of on-off ratio, voltage swing and space-charged limited current compared to its low-voltage counterparts. The long channel length protected the HVTFT from channel length modulation.

5.3.4 Discussion

Our HVTFTs present a very high on-current of almost 100 μA at 80 V and an unprecedented 1 kV operation voltage. What we notice first is the predicted degradation due to the parylene-C dielectric on the TFT and the HVTFT transconductance and on-resistance. Surprisingly, the addition of the Parylene-C layer does not seem to affect the value of the on current of the transistor. However, the voltage swing required to turn on the TFT and the HVTFT increases considerably. The most problematic effect is the high off-current value (respectively 10 nA, 200 nA and 5 μA) in the TFTs and the HVTFTs. Literature reports ZTOs TFT with off-current values lower than 1 pA [1, 88]. The high off-current could be caused by two reasons: The intrinsic conduction in the bulk of the HVTFT semiconductor or a negative threshold voltage caused by a too high charge carrier concentration.

The detection of traces of chlorides in the XPS (Figure 5.2e) and the 450 °C sol-gel temperature used suggest that the alloying process of ZTO is incomplete (as assessed in the TGA in Figure 5.1), leading to high concentration of oxygen vacancies (see Figure 5.2f), which can be a cause of high charge carrier concentration and high off current.

At low gate voltage, the effect of the offset gate leads to the increase of the on-resistance, a predictable effect, as, under low electric fields, the offset acts as a serie resistance. It is interesting to note that the dielectric bilayer suppresses the hysteresis behavior in the transfer characteristics observed in Figure 5.12b, an indication that charge trapping is minimal in the HVTFT dielectric.

5.4 Modeling the HVTFT

In this section, we propose an equivalent DC-circuit model for the HVTFT. First, we took a basic c-Si MOSFET model from LT-Spice libraries and we matched the extracted data from the characterizations presented in the previous section. Afterwards, we modified the circuit equivalent model to take into account the effect of the high voltage and the offset gate on the electrical characteristics of the HVTFT.

5.4.1 LT-spice model for the HVTFT

We first suggest an equivalent DC-circuit modeling for the HVTFT using a circuit modeling software LT-Spice from Analog Devices. To model simply the TFT, we used a basic metal oxide semiconductor field effect transistor (MOSFET) model available. Table 5.2 shows the model inputs, which were implemented in the MOSFET model. The geometrical parameter, width and length of the channel are those of the fabricated TFTs. The oxide capacitance and the threshold voltage were taken from the experimental data. The HVTFTs conduction occurs at the channel interface. We have to also consider parallel conduction occurring in the non-activated part of the semiconductor. We call this parameter the bulk resistance. A linear fit of the HVTFT output characteristics at 0 V gate voltage provides a value for the parallel resistance of 1 GΩ. The electron mobility was manually fitted in the software. For the mobility we used 0.1 $cm^2 V^{-1} s^{-1}$ for the TFT with no Parylene-C, 0.4$cm^2 V^{-1} s^{-1}$ for the Parylene-C TFT and the HVTFT with the offset gate.

Table 5.2 – TFT model inputs

	TFT	**TFT with Par**	**HVTFT**
Width (mm)	5	5	5
Length (µm)	500	500	350
Cox (nF/cm²)	60	3	3
V_{CLM} (V)	3500	3500	3500
Threshold voltage (V)	- 4	- 10	- 10
Bulk resistance (GΩ)	1	1	1
Mobility ($cm^2 V^{-1} s^{-1}$)	0.1	0.4	0.4

Figure 5.14 shows the transfer characteristics obtained for the TFT simulation. In the case of the HVTFT with an offset gate of 150 µm and Parylene-C, we plotted the simulation curve down to its threshold voltage. From Figure 5.14b, c and d, we see that the curve from the model fits well for the region above threshold value. Around gate threshold, the difference might be due to a variation of the bulk resistance between the samples. For the HVTFT Figure 5.14d, the fit drops is satisfying down to 0 V. To summarize the LTspice circuit model described by Figure 5.14a with the parameters shown in Table 5.2 describes well the behavior of our ZTO TFTs and HVTFTs when the drain voltage is held in the saturation region.

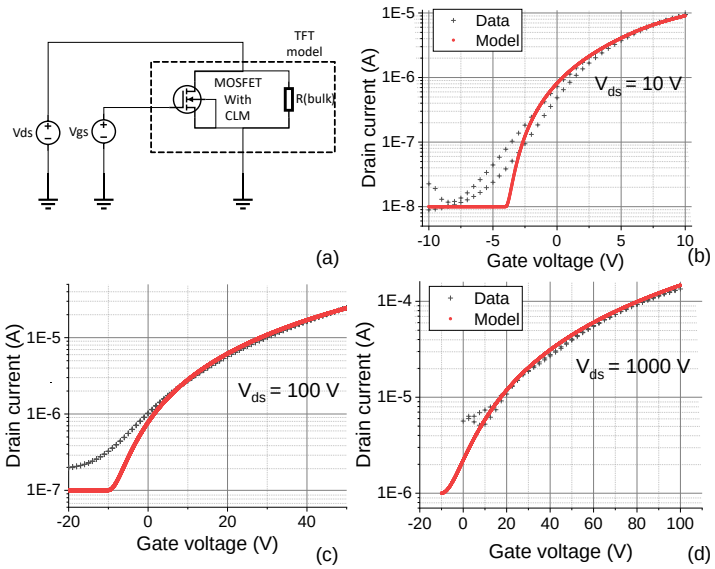

Figure 5.14 – (a) Equivalent circuit for the TFT model: The TFT is approximated by a c-Si MOSFET submitted to channel length modulation and a parallel resistance describing the intrinsic conduction below the material interface. Comparison between the transfer characteristics data points and simulation of (b) TFT without Parylene-C, (c) TFT with Parylene-C and (d) HVTFT with Parylene-C and 150 µm offset gate.

Figure 5.15 shows the simulated output characteristics for the TFTs and HVTFTs. In Figure 5.15b and c, we observe slight differences between the TFTs without an offset gate. The model curve for the TFT without Parylene fits well the data especially for gate voltage > 4 V values. We notice that the linear region of the model for the TFT with Parylene-C TFT with no offset gate has a larger slope for all V_{gs} than the data in the pre-saturation region in Figure 5.15c. The difference is probably coming from the contact resistance between the aluminum electrodes and the channel, a parameter that has not been taken into account in the model.

In the case of the HVTFT with Parylene-C and offset gate as shown in Figure 5.15d, the data of the model fit well the data in the saturation region. However they do not fit in the pre-saturation region. The reason for this absence of fitting is due to the fact we do not consider the high electric field effects in our model. The channel in the offset region is an intrinsic region, therefore it should be equivalent to a resistive load. In addition we have to consider the shift in the onset current due to V_x as seen earlier.

Therefore, we implemented two additional elements to symbolize the not-gated region. The channel is represented by a resistor, whose value is a second fitting parameter (due to SCLC, under high electric fields, the equivalent resistance is a function of the number of charges in the materials rather than a function of the resistivity). The threshold voltage of the diode is the experimental value obtained for V_x, 150 V for an offset gate of 150 µm. The modeled output characteristics is plotted in Figure 5.16b. The offset resistance value is 10 MΩ. The

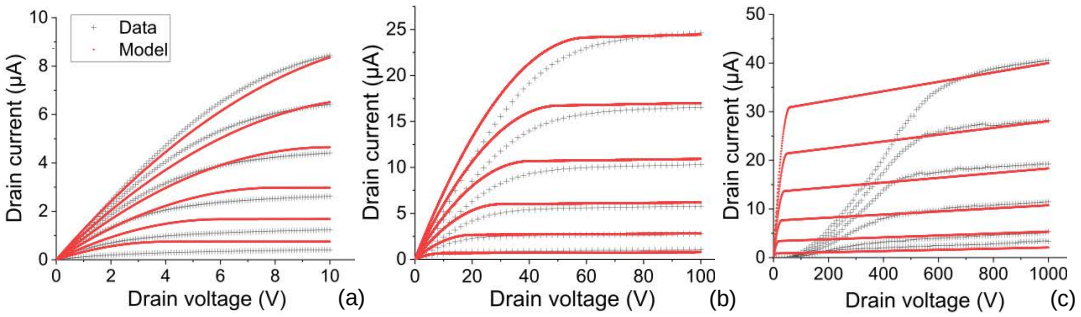

Figure 5.15 – Comparison between the output characteristics data points and simulation of (a) TFT without Parylene-C (gate voltage step: 2 V. Min voltage: 0 V), (b) TFT with Parylene-C and no offset gate (gate voltage step: 10 V. Minimum gate voltage: 0 V) and (c) HVTFT with Parylene-C and 150 µm offset gate (gate voltage step: 10 V. Minimum gate voltage: 0 V).

fitting between the model and the experimental data is better than before, but still imperfect, considering we are neglecting the non-linear relation between the HVTFT drain current and the HVTFT drain voltage in the pre-saturation region. In particular, the saturation voltage of the model does not match the saturation voltage of the data output characteristics.

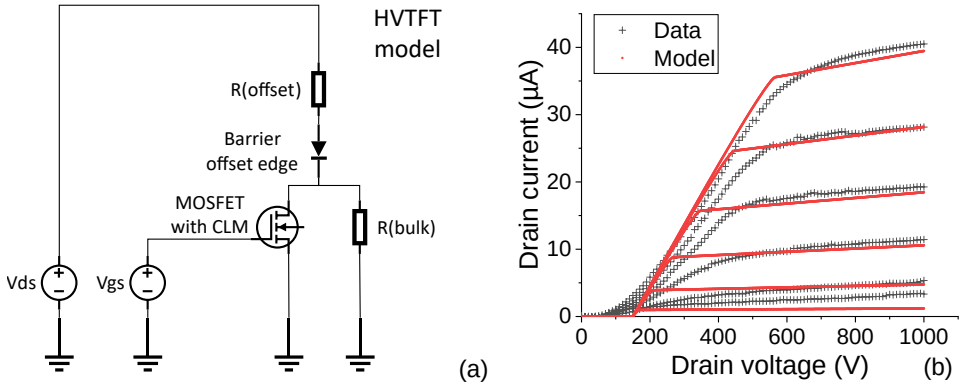

Figure 5.16 – (a) Schematics of the LTspice model for the HVTFT. Compared to before we add the offset contribution by approximating it with a diode of threshold voltage V_x in serie with a resistor symbolizing the non-gated part of the channel (gate voltage step: 10 V. Minimum gate voltage: 0 V) .

To conclude, this model is good enough to get an estimation with circuit behaviours with HVTFTs but is inaccurate to explain some major physical phenomena such as SCLC occurring in the HVTFT channel. A model specifically made for AOS such as a-IGZO might provide more accurate results [152].

5.5 Optimization of ZTO by yttrium doping

In the last section of this chapter, we briefly present an optimization of the HVTFT electrical properties by doping ZTO with yttrium. We first explain the benefit of doping ZTO with yttrium, a strong oxygen binder. After that, we discuss the transfer and output characteristics at V_{ds} = 500 V of ZTO and YZTO HVTFTs. We finally discuss the correlation between the decrease of the high voltage effects and yttrium doping of ZTO.

5.5.1 Adding Yttrium in the ZTO semiconductor

As a reminder, ZnO can be doped using two types of metal cations: weak oxygen binders (Sn, In...) as mobility enhancers and strong oxygen binder (Ga, Y...). Strong oxygen binders decrease the total charge in the semiconductor, leading to lower off-current and steeper gate voltage swing. As the ZTO HVTFT has a high off-current in the order of several µA, we added a strong oxygen binder into the alloy, yttrium, to increase the on-off current ratio by reducing the off-current [132, 153]. Low concentration of yttrium specifically increases the number of electron donors, preventing loss of mobility.

We choose to dope the ZTO thin film with yttrium, a strong oxygen binder. Compared to other strong oxygen binders such as gallium, yttrium is an excellent amorphicizing element [153]. Also yttrium suppresses the formation of ionized oxygen vacancies [132], decreasing the total charge of the material. This effect is very interesting for the ZTO HVTFTs, as a decrease of the material charge leads to the decrease of the SCLC effect [114] as well as to a drop in the off-current [154, 155]. In addition, yttrium has been reported to be acting as a donor when doping ZTO with a < 3% concentration [132].

5.5.2 Synthesis

A 3% and 5% concentration of yttrium was added to the ZTO semiconductor. Yttrium chloride was added to zinc and tin chloride (Sigma-aldrich). The relative concentration of ethylene-glycol and acetonitril were respectively 65% and 35%. The film was spin-coated at 500 rpm on polyimide (Upilex 50S) coated with ALD Al_2O_3. The film was coated at 500 rpm for the following reasons: In the new batches, at the end of this project led to the formation of thin film with a thickness < 10 nm after the sol-gel reaction for a 2000 rpm spin-coating speed. We decreased the spinning speed down to 500 rpm to achieve again 40 nm thickness ZTO semiconductors. The sol-gel reaction was triggered by first drying the thin-film by an annealing at 120°C for one hour and then at 450°C in air for 1 hour.

Figure 5.17 shows the XPS oxygen spectra for the ZTO, the $Y_{3\%}$ZTO and the $Y_{5\%}$ZTO thin films. We deconvoluted the oxygen vacancy spectrum (531.4 eV) and the metal-oxide spectrum (529-530 eV). The graph shows a slight increase in the concentration of oxygen vacancies with increasing yttrium concentration: 12% for ZTO, 19% for $Y_{3\%}$ZTO and 23% for $Y_{5\%}$ZTO.

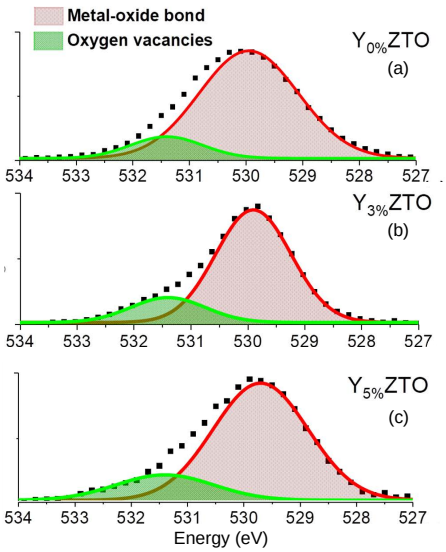

Figure 5.17 – Oxygen XPS spectra of bulk (a) ZTO, (b) $Y_{3\%}$3%ZTO and (c) $Y_{5\%}$ZTO.

This increase could be a consequence of the increase in structural disorder due to yttrium doping [132]. These oxygen vacancies can play the role of a deep trap as yttrium inhibits electron donors [132, 147, 148]. If its traps behave as an acceptor, it could contribute in neutralizing the thin-film decreasing thus the SCLC [91, 114, 132]

5.5.3 Fabrication and electrical characterization of ZTO and YZTO HVTFTs

The HVTFTs structures were built as described in the process-flow presented in section 5.2. The offset gate length was 50 µm. Figure 5.18 shows the output characteristics of ZTO and YZTO HVTFTs up to 500 V drain voltage. Figure 5.19 presents the transfer characteristics of the HVTFTs at 500 V.

From the transfer characteristics, we extract a mobility of 0.10 ± 0.08 cm²/Vs for ZTO, 0.30 ± 0.2 cm²/Vs for $Y_{3\%}$ZTO and 0.80 ± 0.30 cm²/Vs for $Y_{5\%}$ZTO. The on-off ratio is respectively 30 for ZTO, 100 for $Y_{3\%}$, ZTO and 1000 for $Y_{5\%}$ with on-currents in the order of 0.1 mA for the three types of HVTFTs for an 85 V gate voltage swing.

In the output characteristics, we see that the ZTO, $Y_{3\%}$ZTO and $Y_{5\%}$ZTO curves are saturating, showing we can neglect channel length modulation. We notice that the saturation voltage drops with increasing Y concentration. This drop could be caused by an attenuation of the SCLC effect and a decrease in the potential barrier at the offset edge.

There is a correlation between the increase of oxygen vacancies and the attenuation of the SCLC. The charge carrier creation due to the oxygen vacancies could be filling the traps created at the edge of the offset by the high potential applied.

To summarize, adding 5% concentration of yttrium in a ZTO HVTFT increases the field effect performance at high voltage, thus enhancing the characteristics of AOS HVTFT. Further optimization can be done by determining the optimal concentration of yttrium for the HVTFT to be stable. The yield of the devices was in the order of 50 % per wafer and failure came from dielectric-channel short-circuit.

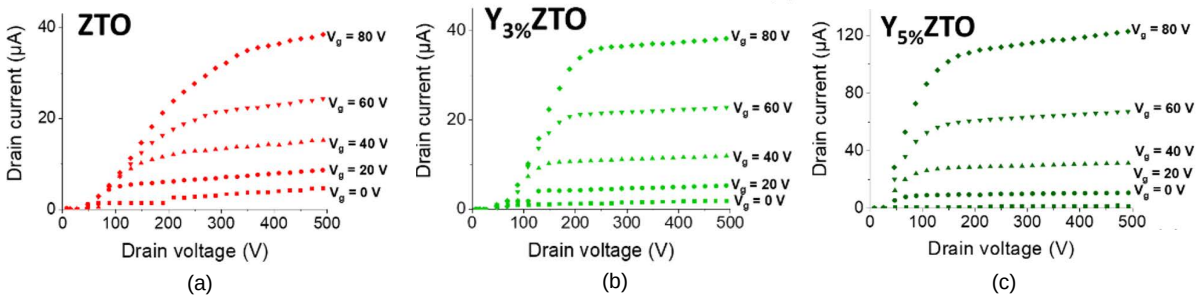

Figure 5.18 – Output characteristics of ZTO, Y3%ZTO and Y5%ZTO with a 50 µm offset gate and Parylene-C as a gate dielectric.

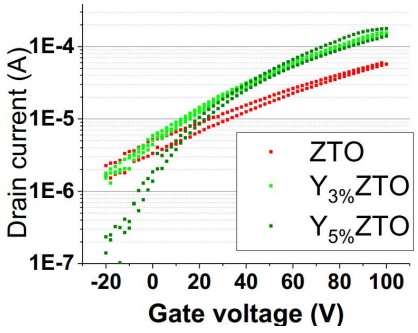

Figure 5.19 – Transfer characteristics of ZTO at V_{ds}, Y3%ZTO and Y5%ZTO with a 50 µm offset gate and Parylene-C as a gate dielectric.

5.6 Perspectives: Fully inkjet printed HVTFTs

Fully printing HVTFTs would enable to achieve highly scalable, cost effective components over large flexible surfaces. As every functional layers of DEAs can already be printed [43, 156–158], being able to print both the driving electronics and the actuators would enable a new level of scalability. Inkjet printing brings an additional level of freedom as materials can be locally patterned thanks to its digital character.

Sol-gel metal oxide semiconductors are materials that have already been implemented in high mobility fully printed thin film transistor [159]. The recipe we use to synthesize ZTO HVTFTs has already been demonstrated for inkjet printing [75]. Metal electrodes for the source, the drain and the gate could be made of metallic nanoparticle inks (Figure 5.20 shows a HVTFT printed in our laboratory with gold electrodes printed by aerosol-jet). However, the available printable metals are silver, gold and copper have work functions > 4.2 eV, the electron affinity of ZTO, which leads to Schottky contact barriers. Alternatively, we could synthesize by sol-gel indium tin oxide electrodes, a standard electrode technology for transparent conductive oxide in solar-cells. The most challenging step would be to print a reliable dielectric with a low pinhole concentration, breaking down under a high electric field. The most promising metal oxide dielectrics for high voltage electronics are alumina and zircona [88, 159] as they both have high breakdown fields and dielectric constant. It will be of particular importance to control the various effects specific to printing such as the substrate-solvent interaction and coffee ring effects for a multilayer stack.

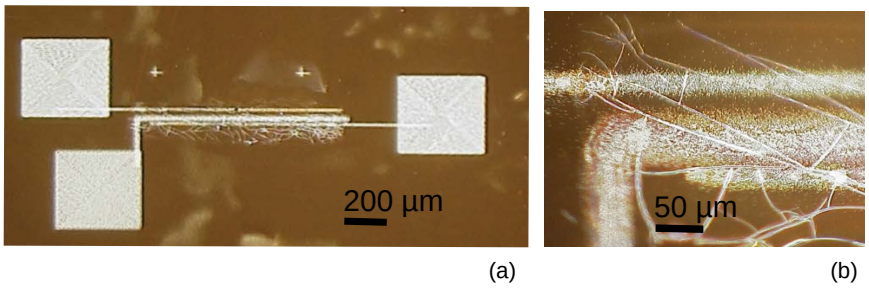

Figure 5.20 – Picture of a fully printed HVTFT (a) Overall device and (b) detail over the offset gate.

Conclusion

In this chapter, we have demonstrated the first ZTO HVTFTs operating at 1 kV. We first validated the synthesis of ZTO through different material characterizations (TGA, DSC, XPS, XRD). Then we presented the process flow of the HVTFT. The transistor showed operation at 1 kV with a dielectric stack made of 1 µm thick Parylene-C film on top of a 100 nm thick Alumina film and an offset gate geometry (150 µm). We provided an equivalent circuit model on LT-Spice considering every modifications in the HVTFT characteristics due to the high electric field effects. Finally, we optimized the HVTFT by doping it with Yttrium, which decreased the off-current to 100 nA and increased the on-off ratio to 10^3. The results are summarized in Table 5.3.

Table 5.3 – Table comparing HVTFTs with requirements

	Minimal	Optimal	ZTO HVTFT	YZTO HVTFT
Operation volage	500 V	> 1 kV	1 kV	500 V
On-off ratio	20	$2{\cdot}10^3$	20	$1{\cdot}10^3$
On-current	10 µA	1 mA	0.1 mA	0.1 mA
Voltage swing	100 V	5 V	85 V	85 V
Semiconductor cristal.	Amorphous		Amorphous	Amorphous
CLM	Negligible		Negligible	Negligible

In the following chapters, we will demonstrate that the ZTO (in chapter 6) and the YZTO (in chapter 7) HVTFTs can be used to drive DEAs. For this, we will integrate those transistors with matrices of DEAs and demonstrate that each actuator can be controlled independently by turning on and off the HVTFTs.

6 Integration of HVTFTs with DEAs

Summary

This chapter covers the first demonstration of integration of high voltage thin-film transistors (HVTFTs) with dielectric elastomer actuators (DEAs).

We first show the design, the fabrication and the characterization of diaphragm DEAs deflecting out of plane. The fabricated DEAs have radii of 2 mm and vertically deflect > 300 µm under a backpressure of 50 mbars.

Then, we recall the working principle of the circuit combining HVTFTs and DEAs. A HVTFT on and off leads respectively to a discharged and charged DEA. We motivate the choice of a 200 MΩ bias resistor to limit the current in the circuit based on the model developed in chapter 5.

Afterwards, we present the assembly of 4x4 arrays (see Figure 6.1) of DEAs-HVTFTs and we characterize it. Only a 30 V gate voltage swing is required to deflect the DEA by 350 µm under a circuit bias voltage of 1.4 kV. Operation under static bending down to 5 mm radius of curvature was ultimately shown suggesting that the HVTFTs could be used for soft robots made of DEAs.

The results presented in this chapter were included in a journal paper in *Advanced Materials* [24] and a proceedings of *the International Conference on Solid-State Sensors, Actuators and Microsystems* [145].

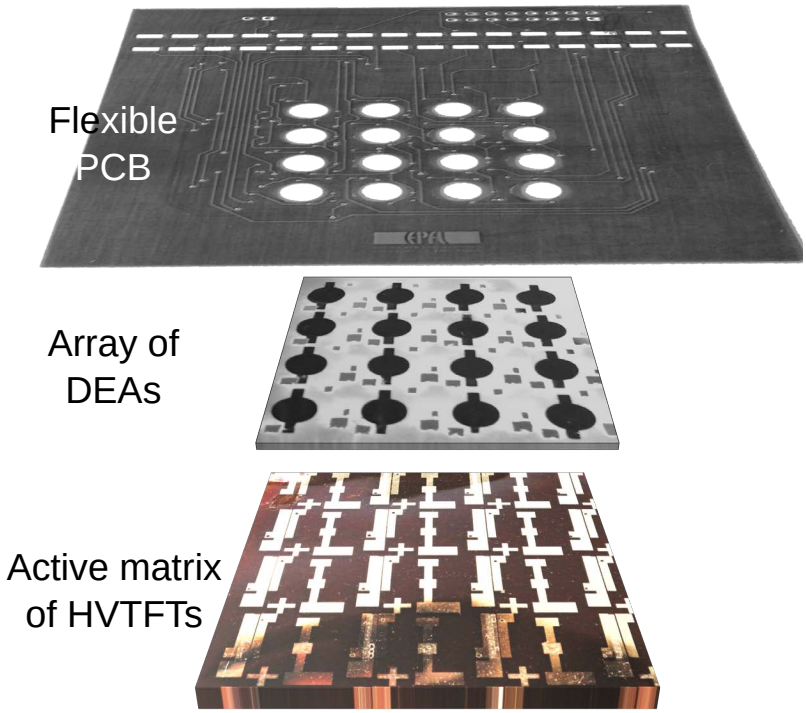

Figure 6.1 – Exploded view of the 3 structural elements of a 4x4 haptic display demonstrator: A matrix of HVTFTs, a matrix of DEAs and a flexible PCB for interconnections.

6.1 DEA design and fabrication

In this section, we show the design and characterization of the DEAs we will use for the HVTFT-DEA proof of concept. The DEAs are deflecting out of plane with a displacement > 300 µm. In particular, we discuss the thickness of the DEA membrane as a function of the back-pressure require to reach maximum actuation at 1 kV. We then present the fabrication process and the characterization of the DEAs.

6.1.1 Operation

In order to operate a DEA as an out-of plane actuator, we constrain its active region within a non-extensible flexible frame. The DEA in-plane expansion leads then to out-of-plane deflection as shown in Figure 6.2. A simple theoretical model has been established by Rosset

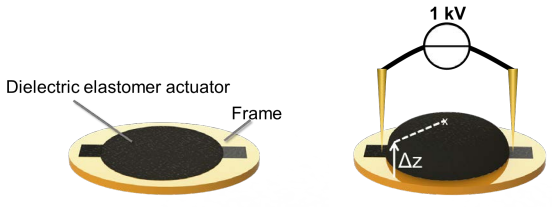

Figure 6.2 – Description of a DEA deflection, when its active region is constrained within a frame.

et al. in order to predict the deflection of the DEA with the following analytical expression when the DEA strain is less than 20% [6, 33]:

$$p = \frac{8(1-0.24\nu)Yt_0}{3(1-\nu)(r^2+z^2)^2}z^3 + 4\frac{\sigma_0 t_0 r^2}{r^2+z^2}z - 4\frac{\epsilon_0\epsilon_m}{t_0 r^2}zV^2 \tag{6.1}$$

Where p is the pressure applied at the back of the DEA diaphragm. ν and Y are respectively the Poisson ratio and the Young's modulus of the DEA membrane. r is the radius of the DEA membrane. t_0 is the initial thickness of the membrane and σ_0 is the initial stress in the membrane (usually due to prestretch). z is the vertical deflection of the DEA and V is the voltage applied across it. This formula is the sum of three different contributions, the mechanical reaction of the membrane one, the mechanical stress inside the membrane and the electrostatic actuation. Every one of these terms is connected to the material and the geometrical properties of the DEAs. Actuation and prestretch lead to a reduced membrane thickness that can be derived from [160]:

$$t = \frac{t_0 r^2}{r^2+z^2} \tag{6.2}$$

Using Equation 6.1 and Equation 6.2, we can now determine the geometry of the DEA in order

to achieve maximum actuation at 1 kV.

6.1.2 Design

We modeled 4 mm diameter circular DEA suspended over a frame made of polyimide with 5 mm holes. A 1 mm margin is taken to avoid sticking a portion of the active region to the frame, a cause for premature breakdown. We apply a constant back-pressure below the DEA diaphragm to inflate it. The back-pressure has three effects: (1) It orientates the DEA and enables it to operate in deflection-mode rather than in buckling mode, (2) it prestretches the DEA and (3) it increases the force of the taxel.

We choose to use polydimethylsiloxane (PDMS) as the membrane material. Assuming a a breakdown field in the order of 100 V/µm, the membrane's thickness under back-pressure and actuation at 1 kV has to be higher than 10 µm. To determine the PDMS membrane thickness, we compute together Equation 6.2 and Equation 6.1. For PDMS, the model's parameters are summarized in Table 6.1. We added parameters for the electrodes in order to describe the effects of the stiffening impact over the system as was shown in [73].

Table 6.1 – Analytical model parameters to determine DEA initial membrane thickness and active area diameter

Name	Symbol	Value
Young's modulus	Y	1 MPa
Poisson's ratio	ν	0.5
Prestretch	σ_0	0 Pa
Active region radius	r	2 mm
Equilibrium thickness	t	10 µm
Relative permittivity	ε_m	2.7
Electrodes thickness	t_e	2 µm
Electrodes Young's modulus	Y_e	1 MPa
Voltage applied	V	input
Backpressure	p	input
Initial thickness	t_0	output
Deflection	z	output

The results of the simulation are plotted in Figure 6.3. Figure 6.3a shows the initial thickness of the DEA membrane to reach a 10 µm membrane thickness under 1 kV actuation as a function of the applied backpressure. Figure 6.3b and c show the deflection-voltage curves of such DEAs respectively without and while considering the stiffening impact of the electrodes.

Without prestretch, the maximum deflection decreases with increasing back-pressure (i.e. increasing thickness from Figure 6.3a) The stiffening impact of the electrodes considerably decreases the 12 µm (10 mbars) and 14 µm (20 mbars) membranes. For a 20 µm thick membrane (100 mbars), the model is not converging towards a coherent value above 800 V as the DEA

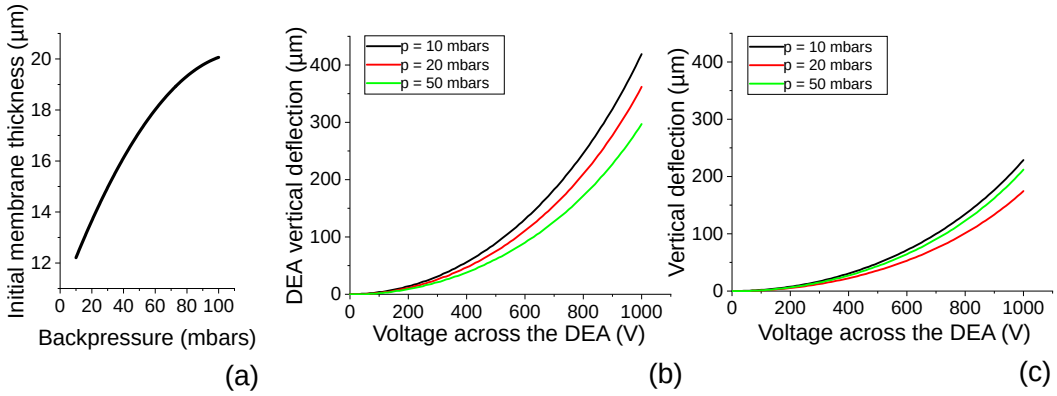

Figure 6.3 – (a)Initial membrane thickness vs backpressure required to achieve 1 kV maximum actuation voltage. Simulated deflection-voltage characteristics with varying initial membrane thickness and backpressure achieving 10 µm membrane thickness under 1 kV actuation (b) without and (c) with stiffening impact of 2 µm thick carbon-black electrodes.

gets beyond a half-sphere case. From Figure 6.3c, the best configuration appears to be either the 12 µm (10 mbar) membrane or the 17 µm membrane (50 mbar), both deflecting > 200 µm at 1 kV. From experience, we noticed that the application of 10 mbars to a membrane does not provide enough prestretch to avoid certain instabilities such as residual wrinkles due to Müllins effect [161, 162]. Therefore, for this demonstrator, we prefered to use the 50 mbars solution, ie the 17 µm membrane. The electrode radius also plays a role in the vertical de-

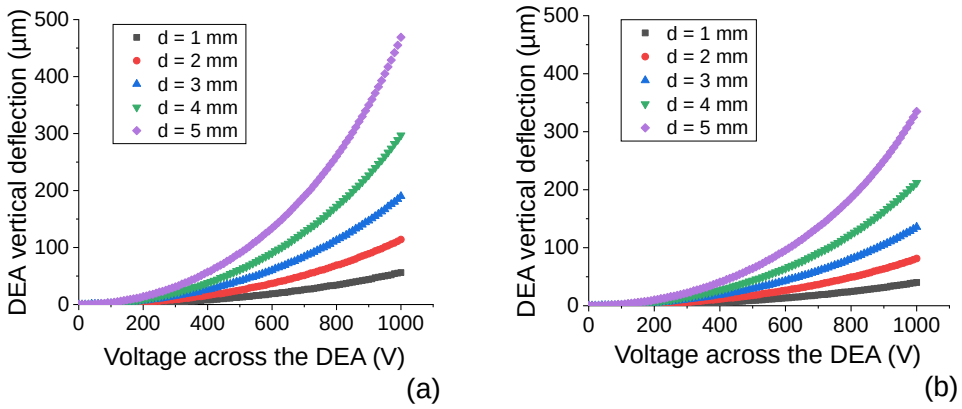

Figure 6.4 – Simulated deflection-voltage characteristics with varying active region diameter (a) without and (b) with stiffening impact of 2 µm thick carbon-black electrodes. The DEA initial thickness is 17 µm and the backpressure is 50 mbars

flection. In order to investigate its contribution, we plot the deflection of a 17 µm under 50 mbars backpressure with varying electrode width. The larger the electrode is, the larger the deflection gets. However, the width increase leads also to a stronger thickness decrease, which

decrease the breakdown voltage of the DEA.

6.1.3 Fabrication

We fabricated 4 mm wide circular DEAs with a 17 µm thick membrane with no initial prestretch. The DEA shall operate with a back-pressure of 50 mbar.

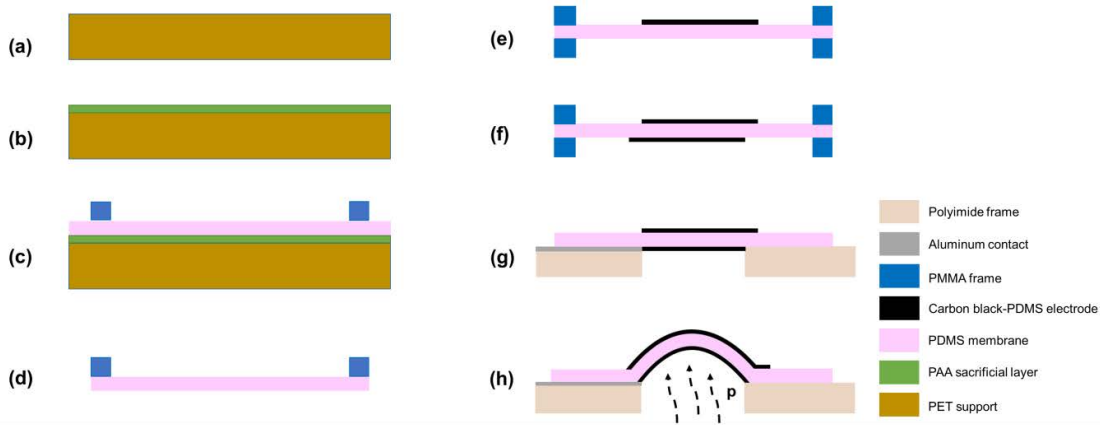

Figure 6.5 – Process-flow to fabricate deflection DEAs on polyimide frame

The fabrication protocol is described below and is strongly inspired from Rosset et al. [73]:

(a) We use a polyethylene terephthalate (PET) A4 sheet (125 µm thick) to serve as the support of the PDMS membrane.

(b) We deposit by blade-casting with a commercial applicator (Zehntner ZAA 2300) a poly(acrylic acid) (PAA) layer. The PAA is dissolved in isopropanol. We let the sheet at room temperature under air to evaporate for 10 minutes.

(c) The PDMS we use for the membrane is made of commercial Sylgard 186 (Dow Corning). The PDMS precursors are dissolved in OS-2 (Dow Corning) with a 38% solvent concentration over the total concentration. We deposit a uniform layer of PDMS by blade-casting with a commercial applicator (Zehntner ZAA 2300). The effective gap between the substrate and the doctor blade is 35 µm and the sweeping speed is 2 mm/s. We cure the membrane for 1 hour at 80 °C in air. We stick PMMA circular frame over the A4 membrane with dry adhesive (ARclear). The diameter of each frame is 5 mm. The substrate is cut with scissors around each frames.

(d) We release each membrane from its PET support. They remain suspended thanks to the PMMA frame. The release is done by putting the assembly in boiling water to dissolve the PAA. The thickness obtained after release has been measured by laser interferometry is 16 ± 1 µm.

(e) We prepare a mixture composed of a mix of PDMS (Bluestar LSR 4305) and carbon black(Akzo-Nobel Ketjenblack EC-300J) diluted in isopropanol to print stretchable electrodes.

The massic concentration of carbon black vs PDMS and of isopropanol:PDMS are respectively 1:10 and 2:1. After mixing, the mixture is applied to a pattern defined in a steel cliché (in our case, a 4 mm diameter circle). The pattern is then transfered to the PDMS membrane thanks to a pad-printer (Teca-Print). The ink is cured for 1 hour at 80 °C leading to ink drying and PDMS cross-linking.

(f) Using the same methodology as in (e), after aligning, we transfer the back-side electrode to define the active region. The ink is cured for 1 hour at 80 °C leading to ink drying and PDMS cross-linking. Figure 6.6 shows fabricated test DEAs in 2x2 matrices.

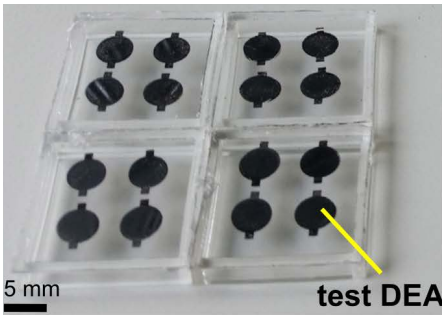

Figure 6.6 – Test DEAs before being suspended to polyimide foils

(g) The DEA is transfered from the PMMA frame to the 50 µm polyimide substrate (Upilex-50S from Goodfellow). Previous to transfer, a 5 mm diameter circular hole was laser cut with a CO_2 in the polyimide (PI) foil in order to suspend the active region of the DEA. The adhesion is achieved by depositing a dry-adhesive foil (ARclear) on the PI before DEA transfer. The backside electrode is connected to an Aluminum back electrode on the PI foil for electrical contact.

(h) A constant compressed-air back-pressure of 50 mbar is applied and regulated by an automatic pump (Fluigent MFCS-8C) to prestretch and orientate the DEA out-of-plane.

In the next subsection, we characterize the DEA fabricated by this methodology.

6.1.4 Characterization

The deflection of the DEAs were measured using a laser-displacement sensor (Keyence, LK-HD 500) pointed on the highest point of the DEA bubble. The voltage was ramped using an EMCO-20 2 kV power supply in order to measure the deflection-voltage characteristics. On Figure 6.7b, we plot the fabricated DEA deflection voltage characteristics. The DEA reaches a 375 µm displacement at 1000 V, which follows the the trend of the simulation for the 5 mm diameter electrodes. We notice that the DEA characteristics approach more the 5 mm electrode diameter curves rather than the 4 mm ones. The proportion of DEAs operating was > 90% for a 4x4 DEA chip. Failure is caused by premature breakdown. This could be due to various factors including inaccuracies in the definition of the circular patterns, the fact that the region

that is pushed by the back-pressure has a 5 mm diameter, when the electrodes have only a 4 mm diameter active region. The DEA breaks down around 1050 V. Those DEAs have the appropriate operation voltage to be combined with the HVTFT at 1 kV.

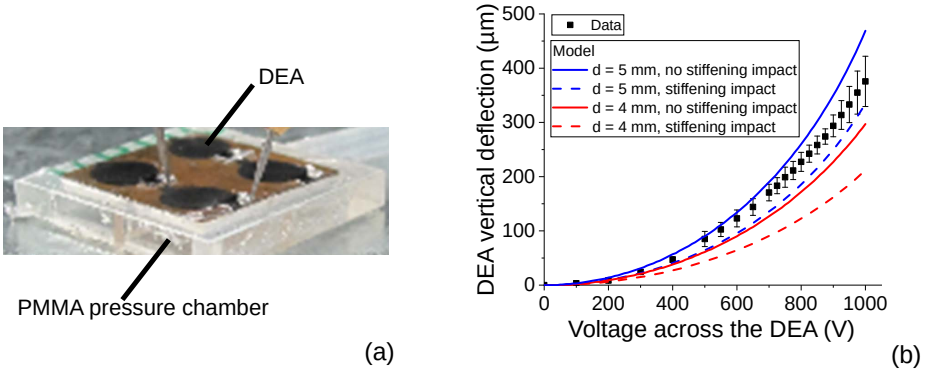

Figure 6.7 – (a) DEA constrained in a polyimide frame, as characterized and (b) deflection voltage characteristics. The dots represent averaged measured data points. The dashed and continuous lines represent simulated curves with the model shown before. The error bars represent the standard deviation of the different samples in 1 run.

6.2 Circuit design to address DEAs with HVTFTs

6.2.1 Circuit architecture

As we saw in Chapter 4, three components are included in the basic resistive-load inverter to drive a DEA: The bias resistor, the HVTFT, a DEA. The circuit of DEAs driven by HVTFTs is shown in Figure 6.8a.

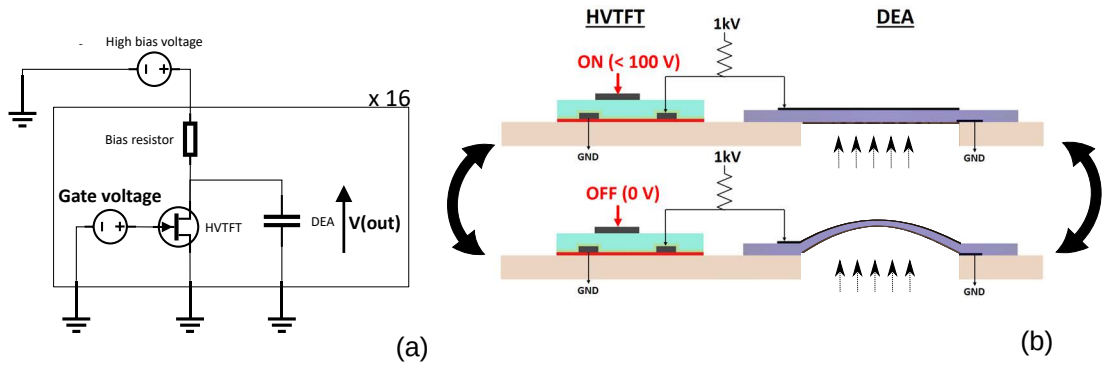

Figure 6.8 – (a)Circuit and (b) operation principle of a DEA based haptic display addressed by HVTFTs. The gate voltage controls the output voltage, across the DEAs, thus controlling the actuation.

We consider one common high-voltage power supply and one common ground biasing the entire circuit. Each DEA state is controlled by the voltage division between the bias resistor and the HVTFT, variating the output voltage between its discharged and charged value. The voltage division is controlled by the channel conduction of the HVTFT, and therefore by the gate voltage value. Figure 6.8b shows the working principle of one DEA-HVTFT cell. When the HVTFT is blocking or off (i.e. the gate voltage is 0 V), the DEA is charged. When the HVTFT is passing or on (i.e. the gate voltage is at its on-value), the DEA is discharged. Each taxel can be controlled independently by using this principle. A matrix can refresh in an infinite variety of configuration, this way with a sum of actuated taxels forming shapes and patterns. In addition, a precise control over the gate voltage in the subthreshold regime would lead to a precise control over the DEA deflection, enabling gradient and complex reconfigurable surfaces. Our circuit design parameters are constrained by the HVTFT we designed in Chapter 5. As the HVTFT maximum operation voltage is 1 kV, each DEA has to reach their maximum actuation at around 1 kV. The on-off ratio, the mobility, the dielectric capacitance and the high-voltage effects in the HVTFT constrain the choice of resistance of the bias resistor.

6.2.2 Choice of bias resistor

We recall from Chapter 4 that we can vary the DEA actuation strain by 75 % of its maximum value if we vary the voltage between 500 V and 1 kV in the particular case of a 1 kV DEA. We use the LTspice model presented in Figure 5.16 page 87 for the HVTFT. We implement this

model in Figure 6.8a in order to determine a value for the bias resistor that enables the DEA be switched on and off by the HVTFT.

We simulate on LTspice the output voltage across the DEA as a function of the gate voltage of the HVTFT for different bias resistance values (1, 10, 100, 1000 MΩ) under constant 1 kV voltage. The voltage across the DEAs have to be > 1 kV but less than breakdown voltage (1050 V) at 0 V gate voltage (DEA charged state, blocking HVTFT) and < 500 V at 0V < V_g < 100 V (DEA discharged state, passing HVTFT). We plot the result in Figure 6.9a. For low bias resistance (1 and 10 MΩ) value, the DEA is charged at 0 V gate voltage. However, it does not discharge sufficiently: At high gate voltage the curves are saturating at an output voltage value > 450 V. For high bias resistance (100 and 1000MΩ), the output voltage at high gate voltage is lower than 450 V. However the output voltage at low gate voltage is lower than 1000 V indicating the DEA is not charging enough in this configuration.

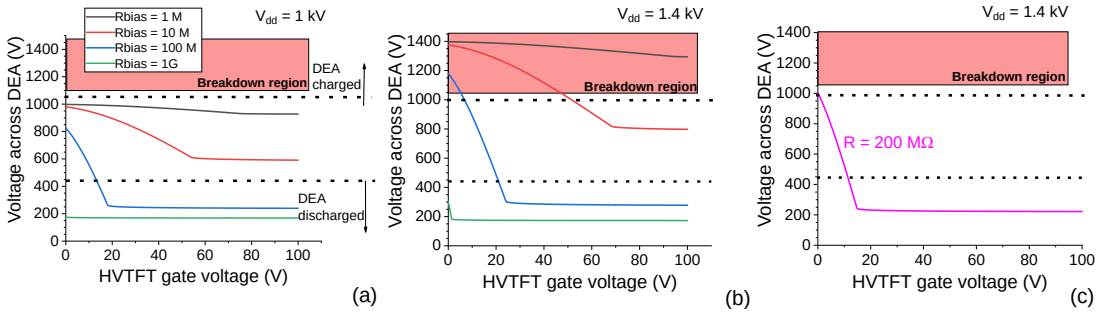

Figure 6.9 – Modeling of DEA switching characteristics with a HVTFT for different bias resistor at (a) 1 kV bias voltage, (b) 1.4 kV bias voltage. (c) Modeling of DEA switching characteristics with a HVTFT with a bias resistor of 200 MΩ, the optimized value to obtain a switching > 80 %.

We increase the bias voltage to 1.4 kV in order to achieve switching of the DEA voltage in order to achieve complete switching of the DEA. We plot the simulation result in Figure 6.9b. for the same bias resistance value as before. In this case, we see that the characteristic curve for a 100 MΩ bias resistance takes its output values above 1 kV when the HVTFT is off and below 450 V when the HVTFT is on. However the output voltage crosses the breakdown region of the DEA. By optimizing the value of the bias resistor, we obtain the curve in Figure 6.9c for a 200 MΩ resistor. Here, the output voltage is slightly above 1 kV when the HVTFT is off and below 450 V when the HVTFT, suggesting the DEA would switch on and off with a strain variation > 80 % in such a configuration.

Therefore, in order to drive the proof of concept, we use a bias voltage of 1.4 kV with a bias resistor of 200 MΩ with the fabricated HVTFT and DEA presented in previous chapter and section.

It is interesting to note that the choice of the bias resistance could be multiple and essentially depend on the increase in the bias voltage. A lower bias resistor would be interesting for the circuit speed, but would lead to the requirement of higher gate voltage swing to switch on and

off the DEA. A higher resistance value would lead on the other hand to a very low gate voltage swing, but would require to highly increase the bias voltage in addition of the circuit being slower.

6.3 Proof of concept design, fabrication and characterization

6.3.1 Design

An exploded view of the assembly is shown in Figure 6.10. The proof of concept was designed to demonstrate that we can integrate and drive independently DEAs with HVTFTs in a flat and bent configuration. Each cell had a 8 mm pitch, the minimal dimensions to respect PCB design rules at 1 kV. A spacer was put at the base of the device to isolate the HVTFTs substrate from the pressure chamber, The HVTFTs were processed and deposited before the DEA for easier contact with the PCB. The PCB on top enabled interconnections between the different components and external power supplies and the bias resistors. The bias resistors spots were aligned at the back of the PCB as shown in Figure 6.10.

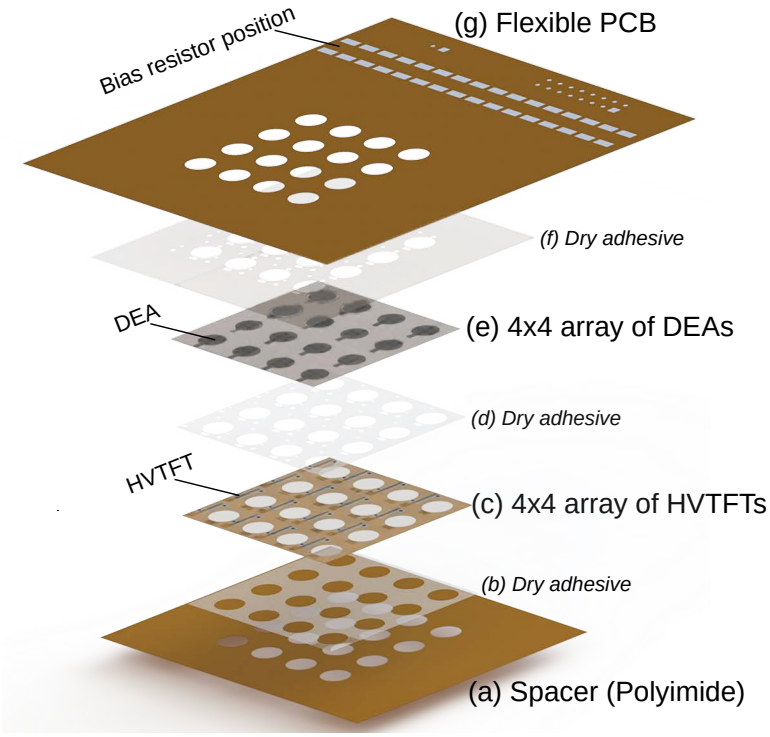

Figure 6.10 – Haptic display proof of concept exploded view.

6.3.2 Process

A step-by-step description of the process is shown in Figure 6.11. We first take a polyimide spacer (Upilex 50-S), marked by laser engraving (Trotec speedy-300) to define the position of the HVTFTs (Figure 6.11a). We align and put dry adhesive (Adhesive Research AR-clear 8932EE) at this position (Figure 6.11b). The 4x4 HVTFT (Figure 6.11c) was attached to the spacer (Figure 6.11d). A stencil mask from a dry adhesive film (Figure 6.11e), patterned with a CO2 laser (Trotec speedy-300) was laminated on it.

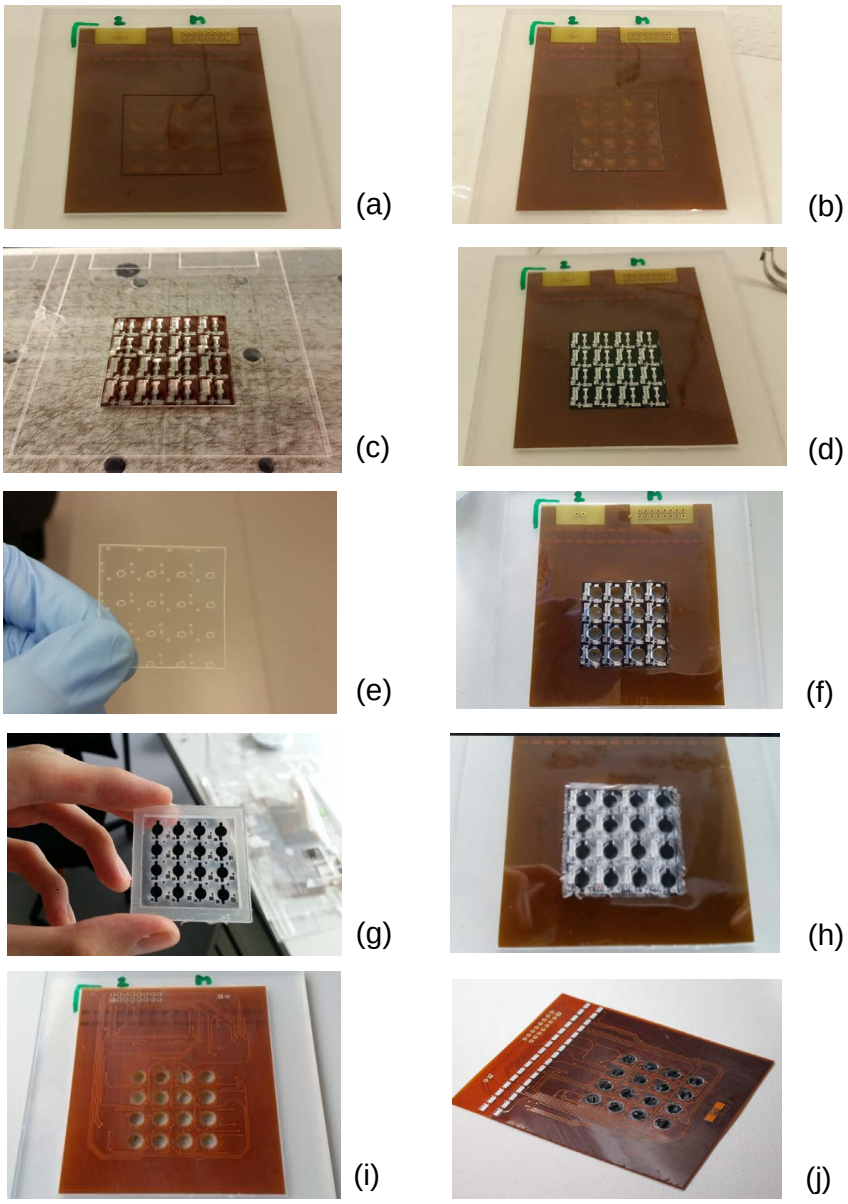

Figure 6.11 – Pictures of the demonstrator assembly step by step

Conductive silver glue (Henkel-CE3103WLV) was stenciled through the dry adhesive mask to define source, drain, gate and backside DEA electrode contacts. The assembly was then cured for 3 hours at 80 °C to solidify the conductive glue. 5 mm diameter holes were laser drilled between each TFT with an 8 mm pitch to suspend the actuators(Figure 6.11f). Holes at the position of the HVTFTs contact were laser-drilled in the DEA array to ensure electrical connection with the PCB (Figure 6.11g). The DEAs were then aligned and stuck on the TFTs layer(Figure 6.11h). We then prepare the designed flexible PCB (beta-layout) made in

polyimide (Figure 6.11i). We apply a stencil mask made of dry adhesive at the position of the via connecting the source, drain, gate of the TFT, the top and back electrodes of the DEA. Silver glue (Henkel-CE3103WLV) was stenciled to make the contact. The PCB was aligned and laminated on the assembly (Figure 6.11j). The whole device was annealed at 80 °C for 3 hours under air to solidify the conductive glue. The 200 MΩ bias resistors were then surface mounted as well as the external cables for the connection. Finally, the assembly is then mounted on a 3d-printed flexible chamber in order to be able to provide a back-pressure to each DEA diaphragm.

6.3.3 Challenges

To avoid short circuits, the via connection maximal diameter was 300 µm. Each taxel had therefore five 300 µm wide connection points: The source, the drain, the gate, the DEA top electrode, the DEA bottom electrode. Therefore the proper alignment of the 16 structures means aligning 80 connection points with the PCB vias. In order to have the most accurate alignment, an alignment stage (see Figure 6.12a) with vacuum and two cameras was fabricated in order to deposit the PCB and interconnect each structure. The stage was fabricated with the kind help of Nadine Besse and Anthony Ruch (EPFL-LMTS). In Figure 6.12b, we see that the PCB via are not well aligned and are overlapping sources and gates in HVTFTs leading to device failure. An excellent alignment is shown in Figure 6.12c, where every via is connected to a single electrode.

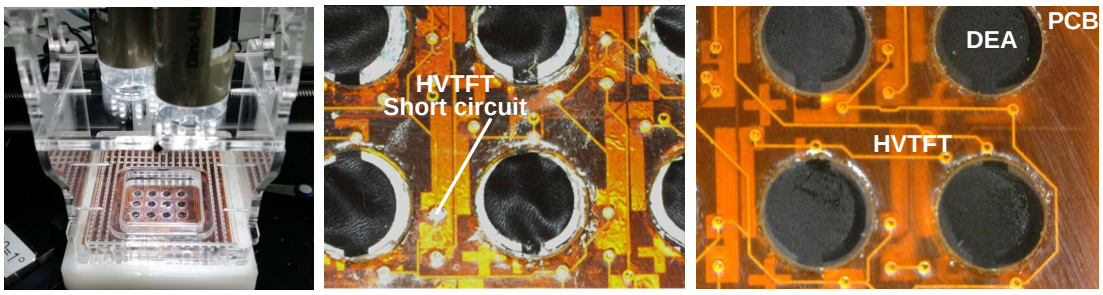

Figure 6.12 – (a) Alignment setup for the assembly of the demonstrator. It is composed of two USB camera in focus with a stage enabling alignment of the different layers with a vacuum. (b) Picture of a badly aligned PCB. The DEA are misaligned with the holes and the sources and gates of the HVTFT are short circuited. (c) Good alignment with properly interconnected HVTFTs and DEAs.

Another problem came from the patterning of dry adhesive to fabricate stencil masks. When laser cutting through it, it is common that the PDMS glue melts and sticks on the cover, making it difficult to remove without partially delaminating the dry-adhesive. As a consequence short circuits appear due to the overlapping of the conductive glue over two connections, or open circuit by removing the conductive glue from a via. In order to avoid such effect, we hardened

the PDMS by putting it for 1/2 hour at -20°C. After this extra cooling step, the dry adhesive does not delaminate anymore.

6.3.4 Deflection response to the gate voltage

The circuit driving each DEA has been described in Figure 4.1 We applied a fixed 1.4 kV drain-source voltage from the high voltage power supply. The transistor was probed at the output of the resistance. Its source was grounded and its gate voltage increments. We measured the DEA output voltage with our electrical characterization setup and the DEA deflection with a laser-displacement sensor (Keyence, LK-HD 500).

Result

We successfully demonstrated the independent operation of the DEA taxels integrated with the HVTFTs with the device shown in Figure 6.13.

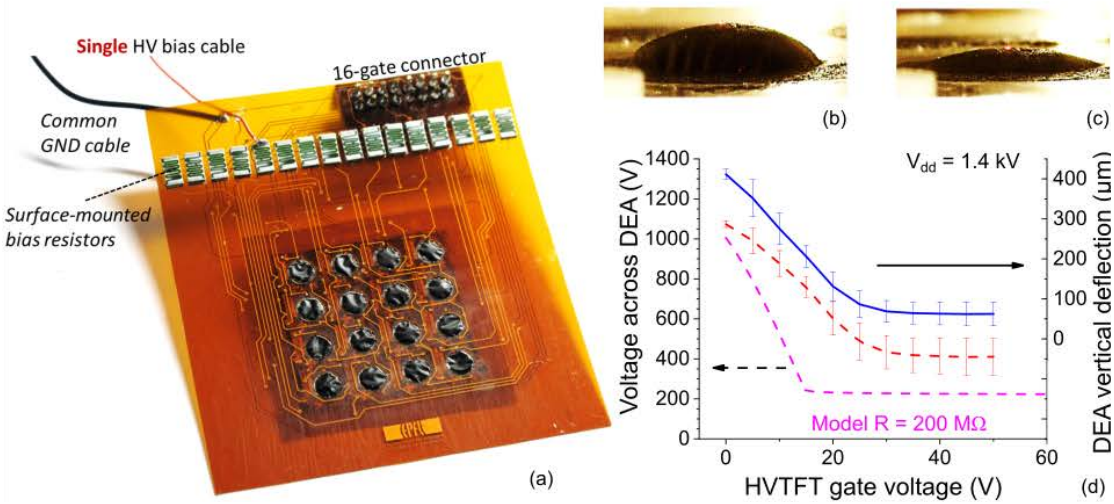

Figure 6.13 – (a)Assembled DEA-HVTFT proof of concept. (b and c) are side-pictures of respectively the DEA charged and discharged. (d) Characterization of DEA deflection and voltage controlled by HVTFTs gate voltage. the dashed curves are voltages and the continuous curve is the deflection. The error bars represent standard deviation. Video at [163]

As shown in Figure 6.13d the output voltage is 1.05 kV (DEA charged: Figure 6.13b) when the HVTFT is off and the turn-on voltage is 30 V for an output voltage of 400 V when the HVTFT is on(DEA discharged: Figure 6.13c). Despite the high output voltage of 400 V when the HVTFT is on, the DEA deflection drops from 400 µm down to 60 µm (on the scale of Figure 6.7) with an effective displacement of 340 µm. The deflection swing is 15 V/µm, demonstrating thus that we achieve more than 80 % DEA maximum actuation deflection (here, 85 %). We measured an on and off time response in the order of 50 ms, logically circuit limited, as it matches the RC constant of the bias resistor and the DEA. We notice a difference between the trend of the

model and the trend of the characteristics in Figure 6.13d. This difference could be caused by the model not taking into account space charge limited current, and repeating poorly the trend of the HVTFT characteristics at lower drain-source voltage (see Figure 5.16 page 102). A higher offset resistance increases the voltage across the DEA when the HVTFT is in on state acting thus as a voltage divider.

6.3.5 Operation under bending

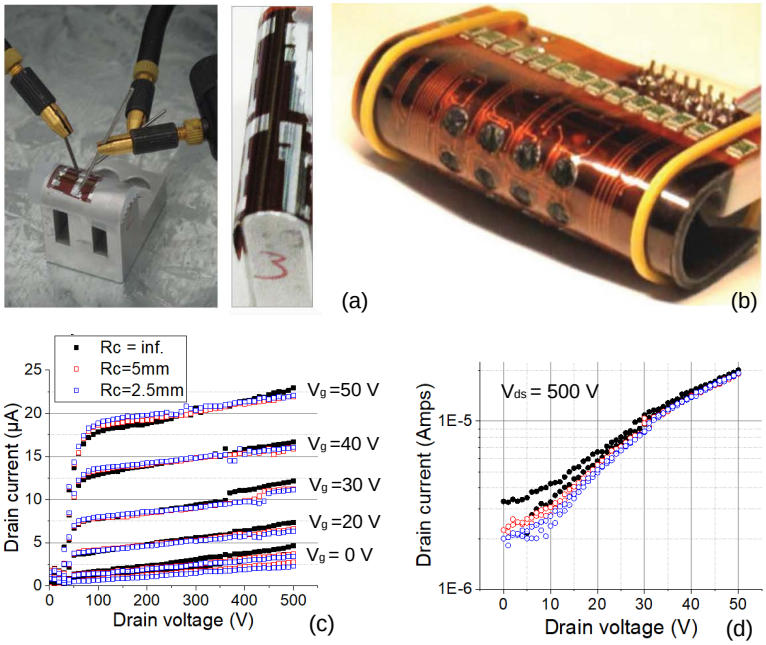

Figure 6.14 – (a)Picture of statically bent HVTFTs on a cylinder. (b)Demonstrator bent with a radius of curvature of 5 mm. Operation under bending is shown at the end of the video in [163] (c) Output and (d) transfer characteristics of the HVTFTs at 500 V under flexure.

We demonstrated that the display is operating down to a radius of curvature of 5 mm. In order to quantify the operation of the HVTFTs, we measured the evolution of the HVTFT characteristics under static bending.

The HVTFTs were diced by laser cutting. We took half metallic cylinders to bend the thin film transistors. We manually probed the devices on those cylinder. The tested radii of curvatures are 1 cm, 5 mm, 2.5 mm and 1 mm. We first measured the high voltage output characteristics of the devices then the transfer characteristics of the devices. The results are plotted on Figure 6.14. We successively measured the characteristics perpendicular and parallel to the channel length. The HVTFTs devices are still functional for a radius of curvature down to 2.5 mm in any type of bending orientation. We see that microcracks appear on the structure when this one is bent. Concerning the results, we notice a bigger characteristic degradation from the parallel case than the perpendicular case. In the parallel case, the cracks

are appearing across the width of the channel, which means it is cut, whereas across the channel length in the other case. In the perpendicular case, there are portions of the channel that remain continuous between the source and drain, and therefore, still operate fully, even at a bending radius of 2.5 mm. Every device breaks at a bending radius of 1 mm.

It has been suggested by Smith et al. that bending leads to lower damages in the electrical characteristics of HVTFT than their low voltage counterparts. Indeed, the traps generated by flexure would be emptied by the application of a high electric field across the channel [104]. Placing these devices at the neutral plane would probably enable operation at reduced radius of curvature.

Conclusion

The key novelties presented in this chapter is the first integration of HVTFTs with DEAs. Switching DEAs with integrated flexible HVTFTs has been demonstrated for the first time with a 30 V gate voltage swing only. The addressing of 4x4 matrix of DEA has been achieved with only a single 1.4 kV high-voltage bias line. The DEA operation has been demonstrated under static bending down to a 2.5 mm radius of curvature demonstrating thus that our approach could be use for bending soft robots made of DEAs such as grippers.

We summarize the parameters of the demonstrator towards a haptic display by comparing them to the requirements described in Chapter 4. Our devices respect all minimum requirements. Increasing the operation voltage, the on-off ration and decrease the high electric field effects of the HVTFT, are necessary steps to approach the optimal requirements. We have suggested a material solution based on the inclusion of a third cation in previous chapter (Yttrium). A geometrical solution could also be found by including a field plate [91, 104], a solution reducing however the on-current of the HVTFT and its breakdown voltage [87].

Table 6.2 – Comparison between the fabricated demonstrator parameters with the requirements.

		Minimal	Optimal	Our demonstrator	Comments
DEA	Normalized actuation strain	80%	100%	85%	
	Time response	100 ms	100 µs	50 ms	Circuit limited
	Actuation voltage	500 V	5 kV	1.05 kV	
HVTFT	Operation voltage	500 V	5 kV	1.05 kV	
	Breakdown voltage	> 500 V	> 5 kV	1.1 kV	
	On-off ratio	10	10000	20	
	On-current	5 mA	2.5 µA	100 µA	20 µA at Vg = 30 V
	Voltage swing	100 V	1 V	30 V	Can be reduced with R_{bias}
	Flexibility	30 mm	1 mm	2.5 mm	Static bending
Bias resistor	Resistance	200 M	200 k	200M	

7 Switching and logic in DEAs thanks to HVTFTs and triboelectric sensors

Summary

In this chapter, it is demonstrated that the use of self-powered triboelectric sensors can be of interest to control the gate voltage of high voltage thin-film transistors (HVTFTs) in order to actuate dielectric elastomer actuators (DEAs) with low-voltage input signals.

First we compare two different ways to control DEAs with mechanical sensors: directly connected and with an intermediate HVTFT. The direct connection approach has drawbacks as the DEA requires a high voltage of more than 500 V, whereas the HVTFT only requires 30 V to switch on and off a 1 kV DEA. Historically, two types of sensors have been used to control DEAs: stretchable resistors [164] and triboelectric sensors [165]. As triboelectric sensors have the advantage of being self-powered, we use them to demonstrate the HVTFT can be used to transfer a low-voltage sensing signal to the DEA.

Afterwards, we demonstrate this concept by amplifying the signal of a triboelectric bending sensor through the HVTFT in order to control a DEA. The output current sensitivity to the sensor's bending angle was 400 nA/°. We were able to demonstrate the driving of a DEA straining accordingly to the bending motion of the triboelectric sensor.

Finally, we fabricated a high-voltage flip-flop composed of two triboelectric sensors with opposite polarity connected in parallel to the gate of the HVTFT. The triboelectric devices were able to latch 40 V peak to peak signals for several seconds at the gate of the HVTFT. The HVTFT was able to maintain two stable states in a 300 V DEA with a 5% lateral strain difference.

7.1 Introduction on switching DEAs with triboelectric sensors

In this section, we show the advantages of controlling the actuation voltage of a DEA with an intermediate HVTFT transmitting the signal of a triboelectric sensor. We compare the advantages of switching the DEA directly and with an intermediate HVTFT. We also discuss the use of a triboelectric device compared to stretchable resistors, previously used to switch DEAs on and off, dielectric elastomer switches (DES). Implementing such sensors would lead, for instance to DEAs based grippers able to close when an object collides inside, microfludic pump opening when liquid is detected at the gate of a chamber, or a haptic display detecting finger pressure and interacting with its user.

7.1.1 Switching DEAs with sensors directly connected to the actuator

Up to date, it has been possible to control directly DEA actuation with mechanical sensors by using stretchable resistors, also called dielectric elastomer switch (DES) [164]. This approach led to logic gates combining actuation and sensing to create logic signals [166]. Recently, another work reported the use of triboelectric generators (TrEGs) to switch on DEAs [165]. Figure 7.1 shows the operation principle of a DES and a TrEG, when connected directly to a DEA.

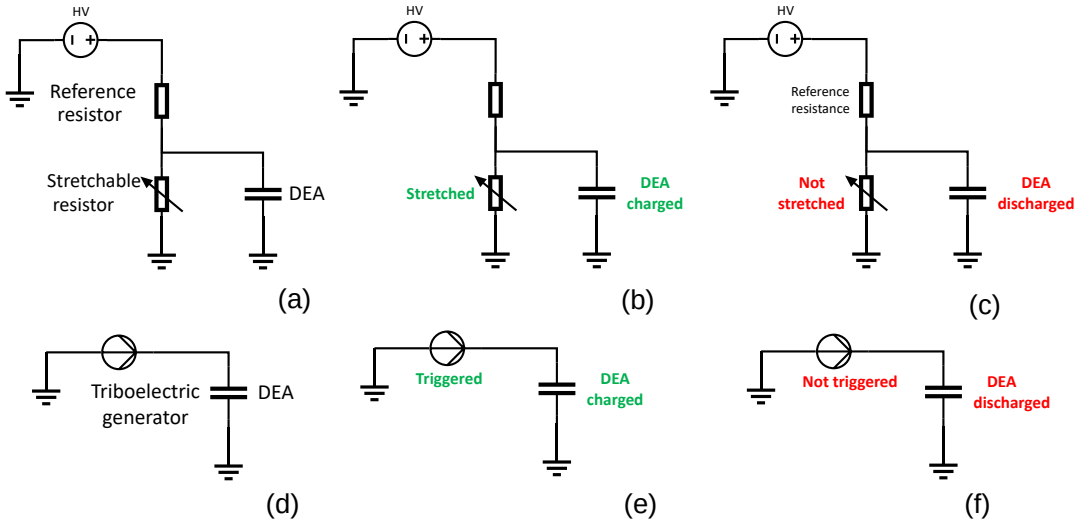

Figure 7.1 – (a) Circuit for a stretchable resistor or DES driving a DEA. (b) When the stretchable resistor is stretched, it is acting as an open switch and the DEA is charged. (c) When the stretchable resistor is not stretched, it is acting as a close switch and the DEA is discharged. (d) Circuit for a triboelectric sensor charging a DEA. (e) When the triboelectric device is triggered the DEA charges. (f) When the triboelectric sensor is not triggered, the DEA is discharged. Adapted from [164, 165]

A DES can be fabricated from DEA carbon-based stretchable electrodes [164, 167]. When the DES is not stretched, a continuous conductive electron path exists and the resistance is low,

typically in the order of 1 MΩ and the DEA is discharged. When the DES is stretched, there is no more percolation between the carbon particles and the resistance is higher than 1 GΩ [164].

A TrEG is an energy harvesting device generating an electrical potential from the charges produced by the friction between two materials of opposite electronegative/positive polarity. TrEGs can generate high open-circuit voltage higher than 1 kV. DEAs being capacitors, a TrEG connected to it in serie can generate its open-circuit output voltage, 1.6 kV in the case reported in [165].

These devices have specific advantages. A stretchable resistor can be designed simply and combined with the DEA electrode processes. The TrEG is self-powered and can generate tens to thousands of volts in open-circuit configuration.

However, for both of these technologies, being directly connected to the DEA presents several drawbacks. The DES cannot withstand more than several tens of cycles because of the damages due to the very high voltage applied to the DEA leading to spark erosion [167]. The voltage generated by the TrEG depends highly on the output load impedance of the circuit. As a consequence, the voltage generated across the DEA depends on the DEA capacitance, therefore its active region area and the thickness of the membrane [165].

7.1.2 Switching DEAs with intermediate HVTFTs amplifying the sensor signal

In previous chapter, we have seen that we only needed to switch the gate voltage of the DEA by 30 V to control the actuation of a 1 kV DEA. Therefore, connecting a sensor able to produce a 30 V swing to the HVTFT gate would enable full control of DEA actuation. Figure 7.2 shows an example of such a configuration where the DES or the triboelectric sensor are driving the gate of the HVTFT. Such configurations solve several problems: In the case of the DES, the resistor is only submitted to 30 V, which would probably increase its durability, by decreasing the heating and degradation effects that were previously due to the application of a high voltage. In the case of the triboelectric sensor, requiring only 30 V open-circuit voltage enables to reduce the size of the device to charge a DEA [168]. Additionally, the voltage generated only depends on the HVTFT gate impedance and not anymore on the DEA output load. It implies that DEAs can be designed independently from the TrEG. We have summarized this comparison in Table 7.1.

Table 7.1 – Comparison between dielectric elastomer switches and triboelectric sensors to drive a DEA.

	Directly connected to a DEA		**With an intermediate HVTFT**	
	DES	TrEG	DES	TrEG
Self-powered	No	**Yes**	No	**Yes**
Output independent from load	**Yes**	No	**Yes**	**Yes**
Durability	Low	**High**	**Fair**	**High**

Compared to DES, a triboelectric sensor presents interesting perspectives to drive a DEA as it does not require an external power supply to control the gate of the HVTFT. As a consequence, we will demonstrate the amplification of a sensor signal with the HVTFT to drive a DEA with triboelectric sensors.

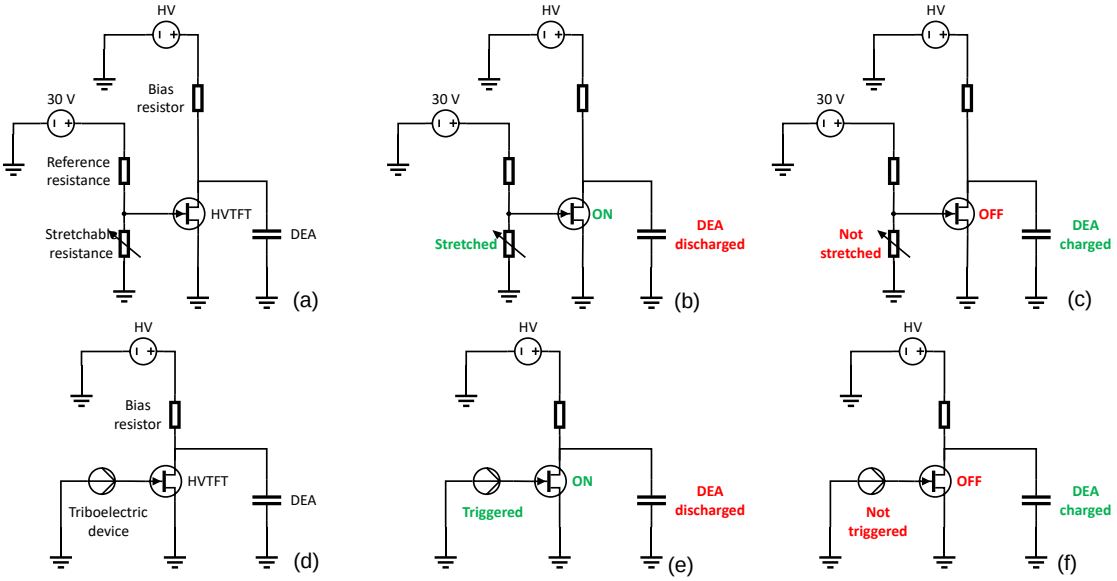

Figure 7.2 – (a) Circuit for a stretchable resistor or DES driving a HVTFT to control a DEA. (b) When the stretchable resistor is stretched, the HVTFT is on the DEA is discharged. (c) When the stretchable resistor is not stretched, the HVTFT is on and the DEA is discharged. (d) Circuit of a triboelectric sensor charging the gate of a HVTFT to control a DEA. (e) When the triboelectric device is triggered the HVTFT is on and the DEA is discharged. (f) When the triboelectric is not triggered the HVTFT is off and the DEA is charged.

7.1.3 Introduction to triboelectric sensors

In triboelectric sensors, charge generation occurs by contact electrification of two electropositive/negative materials: When the two materials are in contact, electrons transfer from the electropositive to the electronegative material. The separation of the materials leads to the apparition of opposite charges on the other side of the material to compensate for the electric charges transferred. These charges imply a voltage that can be measured across the triboelectric device. Two of the main operation modes are the lateral sliding mode and the vertical contact-separation mode [168–170].

Triboelectric sensors can be used for mechanical energy harvesting but also as very sensitive self-powered mechanical sensors [171]. By combining materials with large electronegativity/positivity, a triboelectric sensor can produce very high open-circuit voltage higher than 100 V [165]. Additionally, TrEGs can be made with very simple, a cost efficient processes such as casting [172] and a wide choice of materials [168]. As a comparison, piezoelectric sensors

hardly achieve more than 100 V operation voltage with flexible materials such as PVDF. To achieve high voltage, the process is more complicated and electric poling is required for dipole alignment to achieve higher performance [173]. For PVDF the open-circuit voltage reported can be in the order of tens of volts but rarely exceeds 100 V without loading the thin film with eg $BaTiO_3$ nanoparticles [174, 175].

Triboelectric sensors can be adapted to a wide variety of scenarii. Wang et al. reviewed in 2015 a high number of applications where triboelectric devices could be used as active sensors [168]. These applications include pressure sensing (sensitivity: 40 $mVPa^{-1}$), acoustic sensing (sensitivity 10 VPa^{-1}), acceleration sensing (sensitivity 15 Vg^{-1}) as well as gas, chemical and displacement sensing.

7.2 Amplifying the signal of a triboelectric device with a HVTFT to drive a DEA

7.2.1 Working principle

In this section, we use a TrEG device operating in bending motion to drive a HVTFT and through it, a DEA.

In order to switch HVTFTs with triboelectric devices, we exploit the polarity and the high voltage generation of the triboelectric device in a high impedance circuit. The gate of the HVTFT is equivalent to a capacitor of high impedance because of the thick gate dielectric leading to low gate capacitance and negligible leakage current between the gate and the source.

Figure 7.3 shows the operation principle of the bending triboelectric when the device is connected to the gate of the thin-film transistor (TFT). When the triboelectric is bent, it generates a negative potential across the gate and the HVTFT is off. When the device returns to initial position, the contact separation generates a positive voltage and the HVTFT is on.

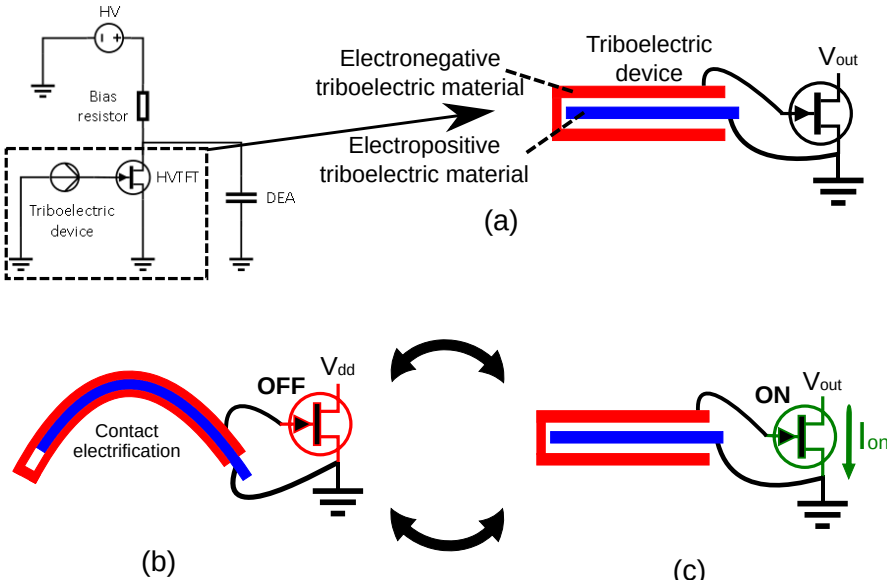

Figure 7.3 – (a) Circuit of a bending triboelectric device driving the gate of the HVTFT. (b) When the TrEG is bent, the HVTFT is off. (c) When the TrEG is not bent, the HVTFT is on.

7.2.2 Devices

The ZTO HVTFT and the DEA implemented are the same as those described in chapters 5 and 6. The DEA has not been constrained to a polyimide frame and actuates in-plane. The triboelectric devices were fabricated by Rubaiyet Haque (EPFL-LMTS) and its characteristics

and fabrication process have been reported in [170]. The device has been fabricated to operate at the same time in vertical contact separation and in lateral sliding mode. When the device is bent, the triboelectric layers enter into contact together and further bending leads to friction between them. Under arm bending the triboelectric device provides an open-circuit voltage signal varying from -100 V to +50 V between the bent and the idle position. The band total area is 72 cm^2, the electronegative layer is made of a 60 µm thick blade-casted polydimethylsiloxane (PDMS) (Sylgard 186) and the electropositive layer is made of a blade-casted 50 µm thick polyurethane (PU) (MM4520). A spacer of PDMS was added so that the gap between the triboelectric active layers is 200 µm. The electrode on PDMS to collect the charges is made of conductive textile and the electrode on PU is made of a carbon-black-PU mixture to adhere well to the polyurethane. Alternatively, a band using teflon instead of PDMS has been used as a flexible, non-stretchable device. A cross-section and a picture of the triboelectric devices are available in Figure 7.4

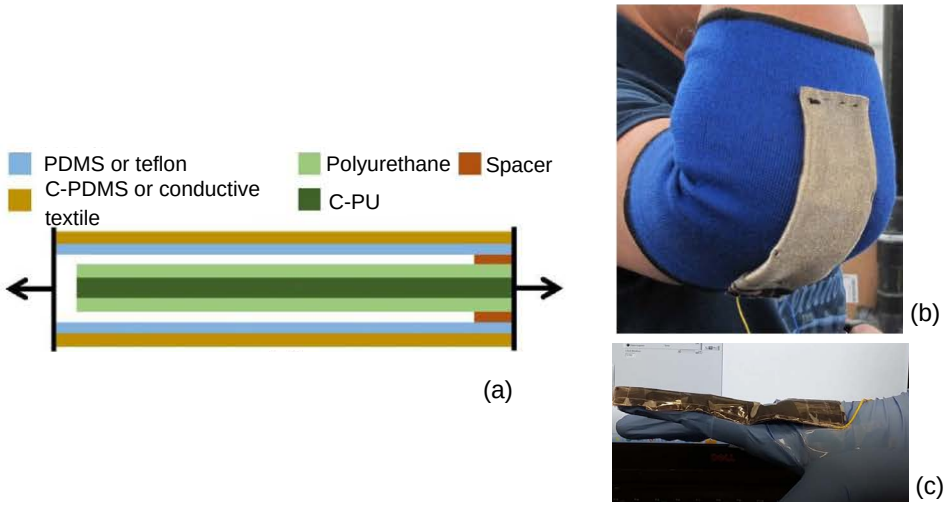

Figure 7.4 – (a) Cross-section of the triboelectric band. (b) Triboelectric band implemented to an arm band. (c) Triboelectric band integrated to a finger gloves. (adapted from [170])

7.2.3 Results

We were able to control the HVTFT drain-source current by finger bending. Figure 7.5 shows the HVTFT characteristics, when driven by the TrEG.

In Figure 7.5b, we plotted the HVTFT drain current as a function of the TrEG bending angle. The bias voltage applied to the HVTFT was 600 V. The output current was measured at the source of the HVTFT without additional circuits.

The TrEG bending angle was measured at the junction between the proximal and intermediate phalanx. In this configuration, we are able to detect the motion with a sensitivity around 400 nA/° showing that not only switching of the HVTFT is possible with a triboelectric device

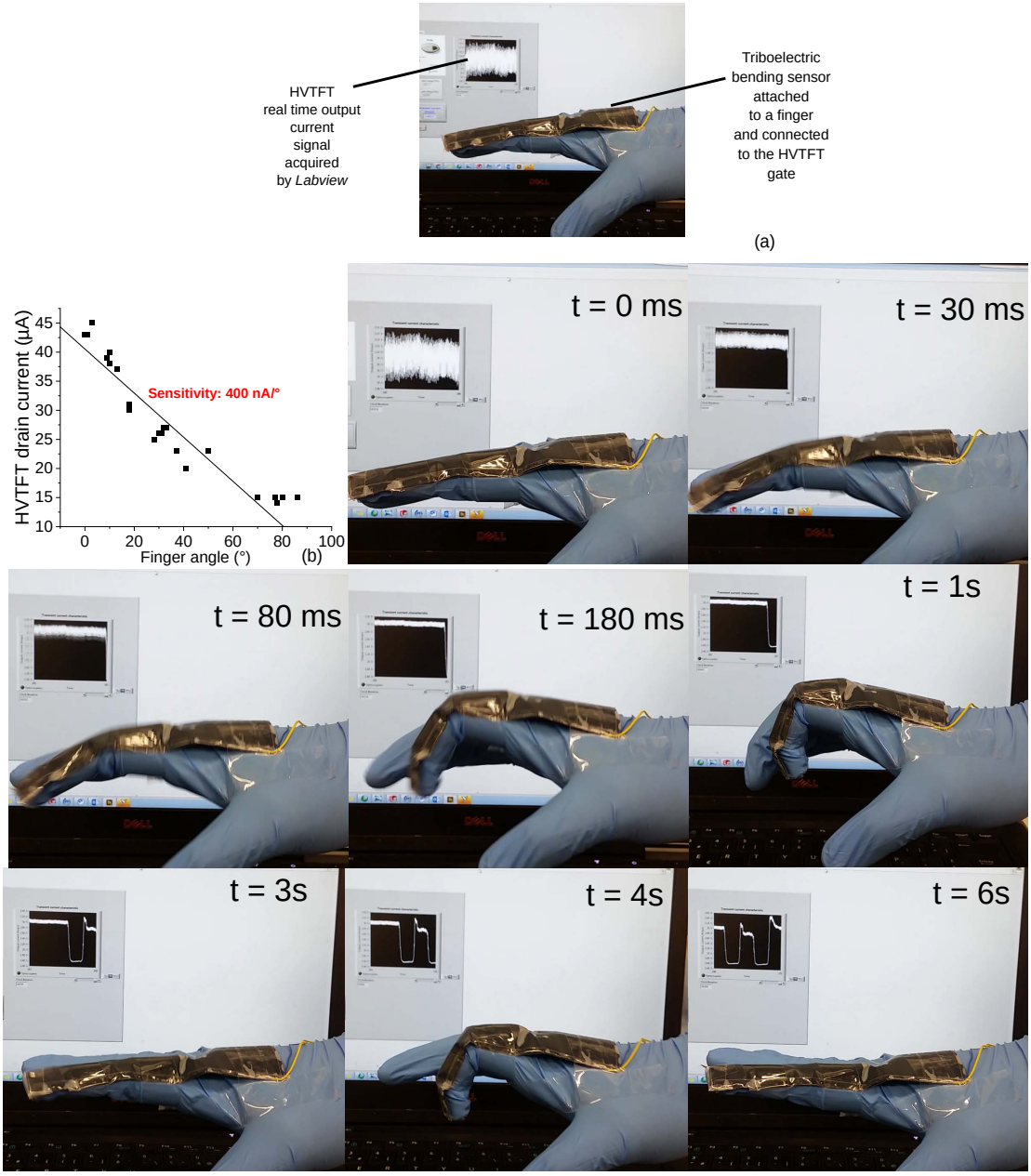

Figure 7.5 – (a) Picture describing the system composed of the triboelectric device connected to the HVTFT of which we see the transient drain-source voltage signal. (b) Output current of the HVTFT as a function of the finger angle. Each sample were obtained from the same triboelectric device and the HVTFT. (c) Sequence of HVTFT switching with a triboelectric sensor.

but also analog control of the HVTFT output. In Figure 7.5c, we can see that the response time of the HVTFT to the bending motion is less than 30 ms and limited by the speed of the finger.

We then connected a triboelectric device to a DEA circuit as shown in Figure 7.3 and we demonstrated that we were able to control the actuation with the triboelectric device. As the motion of the DEA is difficult to see on a picture, a video validating this experiment can be downloaded from [176].

To summarize, we have demonstrated that we could use a triboelectric bending sensor to switch the gate voltage on and off and to amplify a sensing signal to drive a DEA. The output current of the HVTFT has analog sensitivity to the triboelectric input signal enabling analog control of DEAs.

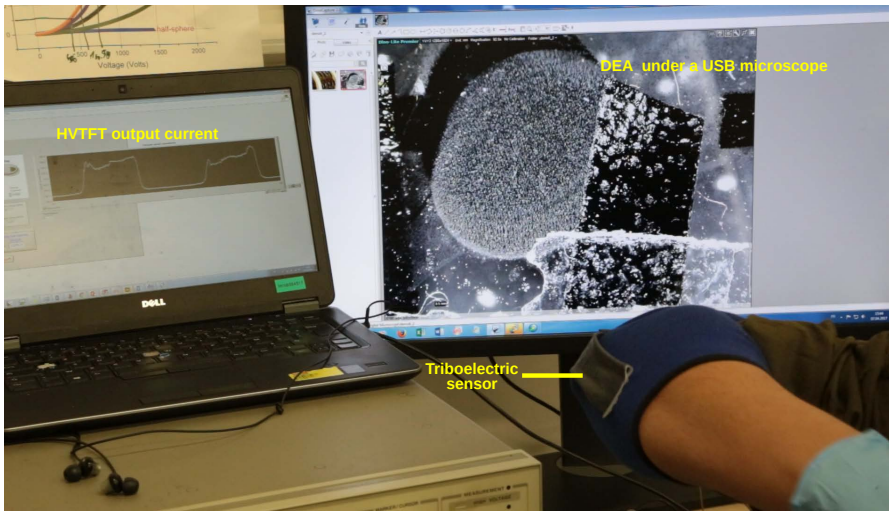

Figure 7.6 – Picture of the experimental setup providing the HVTFT transient current characteristics, the triboelectric device and the DEA connected at the output projected on a computer screen thanks to a USB microscope. Video: [176].

7.3 A high voltage flip-flop gate to drive DEAs

7.3.1 Working principle

In open circuit configuration, a TrEG in contact separation mode generates a voltage when pressed, and holds a voltage of opposite polarity when released. Depending if we are measuring the voltage between the electropositive and the electronegative material or inversely, we can produce a voltage of negative or positive polarity. Putting in parallel two triboelectric pads of opposite polarity to a capacitor would constitute a device able to hold two voltage signals of opposite polarity. Connected to the gate of a HVTFT, this enables a transistor with two electronic stable states, equivalent to a set-reset flip-flop. Table 7.2 shows the output logic states of a flip-flop as a function of its set and reset inputs.

Table 7.2 – Logic states of a set-reset flip-flop

Set	Reset	Output
1	0	1
0	1	0
0	0	Previous
1	1	Indeterminate

Figure 7.7 describes the circuit architecture and the working principle of such a flip-flop. When the set triboelectric is pressed and released, the gate holds the charge and the transistor channel is closed. The charge is then held until the reset is pressed and released, generating a negative potential at the gate of the transistor. The channel is then open. When no action is performed on the triboelectric devices, then the previous state triggered is kept in memory until charge dissipation through the triboelectric device or the HVTFT. When the set and the reset triboelectric devices are triggered together then the dominant one is the one generating more charges. It is a scenario that can vary with the triboelectric architecture and the triggering condition and it is therefore not possible to predict a defined on or off state for the HVTFT in this case. As shown in Figure 7.7a, we can connect this logic gate to a DEA. With the flip-flop we would be able to induce electrical bistability to the DEA. This is very interesting for systems requiring DEA bistability as mechanical bistability requires specific frame and membrane scaling and processing, which can be complicated to achieve.

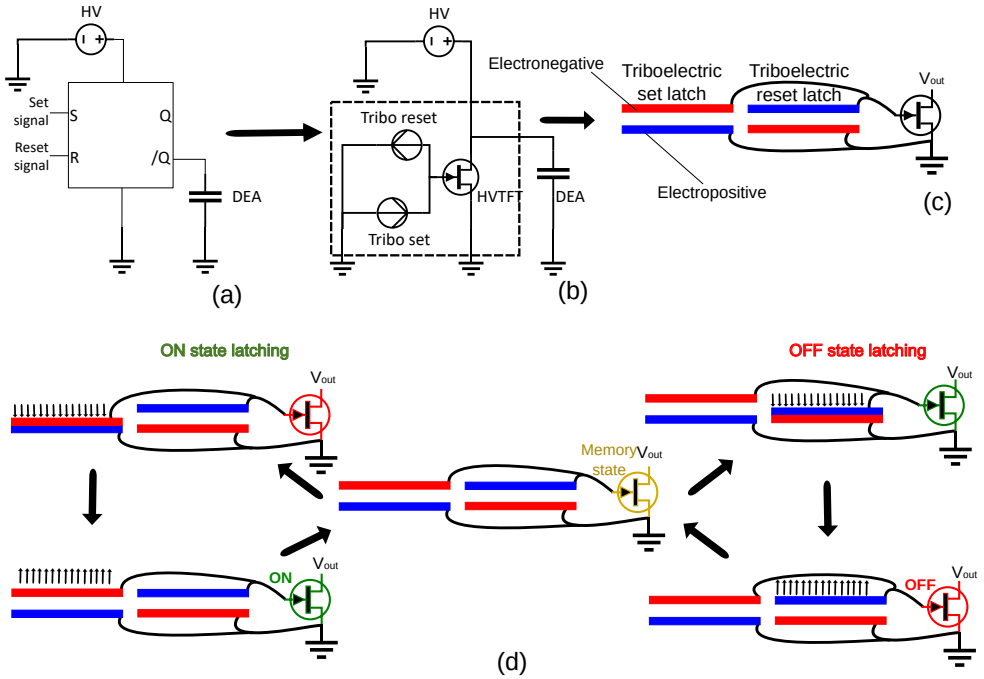

Figure 7.7 – (a) Circuit representing a flip-flop driving a DEA. (b) Equivalent circuit of the flip-flop composed of two triboelectric devices and a HVTFT driving a DEA. (c) The two triboelectric are made of two triboelectric in different polarities. (d) Working principle of the high voltage flip-flop. When the two triboelectric devices are idle, the previous state remains in memory. The on-state and off-state are respectively latched by pressing the set and reset triboelectric devices.

7.3.2 Devices

The HVTFT is made of YZTO HVTFT as described in chapter 5 and the DEA operate at 300 V. The latter, which has been fabricated by Xiaobin Ji (EPFL-LMTS) following the process described in [74]. The DEA has a 4 µm thick membrane and CNT based electrodes. The tapping triboelectric device has been fabricated by Rubaiyet Haque following the process described in [170]. The electronegative layer is a PDMS layer and the electropositive layer is in PU, fabricated identically as before [170]. The electrodes are made of carbon-black silicone. In contact separation mode, the triboelectric device switches between -200 V and 200 V in open circuit configuration. The active area is 25 cm^2. The cross-section and a picture of a triboelectric pad is shown in Figure 7.8.

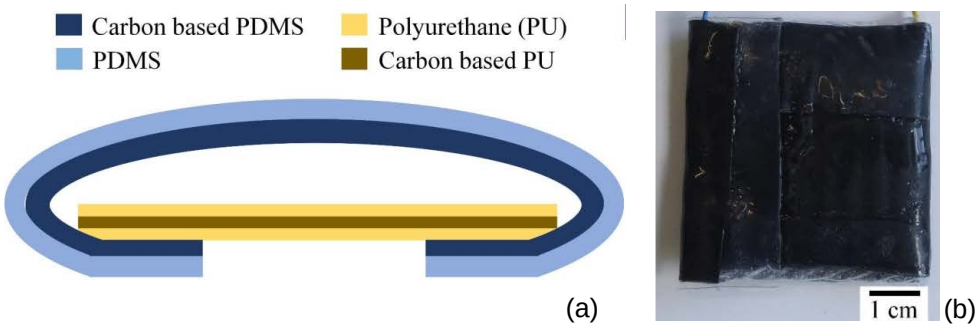

Figure 7.8 – (a) Cross-section of a triboelectric pad used as the set or the reset triboelectric device. (b) Picture of a triboelectric pad.

7.3.3 Results

Figure 7.9 reports the circuit architecture and chronograms for the output voltage controlled by the set-reset flip-flop. A constant 500 V is applied to the circuit with a 1 GΩ bias resistor for the HVTFT control. No power supply is used at the gate node, which means that only the triboelectric devices play a role in the HVTFT electrical conduction modulation.

As reported in Figure 7.9b and c it is possible to control the output voltage of the circuit by latching the triboelectric gate in on or off state. We see that the reset output voltage is around 460 V and the set voltage varies between 120 V and 170 V. The small spikes that we can see before releasing correspond to an excess of charge being generated at the gate due to the pressing of the triboelectric device. We see in each cycle represented in Figure 7.9 that we can discriminate the different phases of the latching mechanism, the pressing and the release of the triboelectric device. The set and reset time constants after triboelectric release are identical at 100 ms and, in this configuration, is circuit limited. With no bias resistor, the time response of the HVTFT is less than 10 ms, the time resolution limit of our characterization tool. The latching effect disappears after 4.5 s, probably because of leakage through the triboelectric devices and the HVTFT. The voltage generated at the gate by one single triboelectric device is in the order of ±140 V. However, connected in parallel, the peak voltage of one triboelectric

device is in the order of ±40 V. This loss is caused by the capacitive division between the two triboelectric devices. In order to avoid a voltage reduction caused by this division, the solution would be to increase the difference of capacitance for each triboelectric device between its contact electrification and its idle position. Ideally a triboelectric device in single electrode operation mode (0 capacitance in idle position) would be ideal to avoid the set and reset triboelectric latches to interact with one another [165].

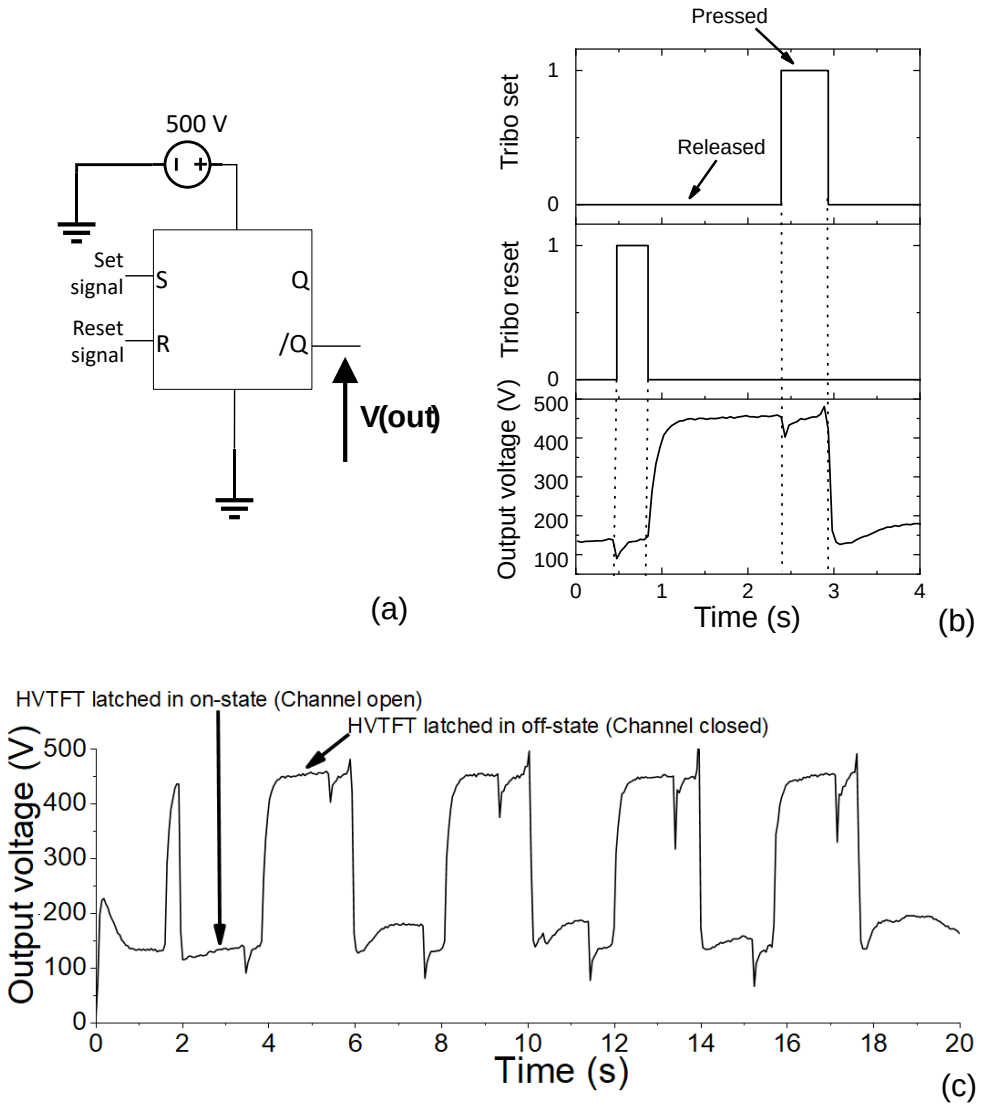

Figure 7.9 – (a) Circuit schematics of the high voltage flip-flop composed of one HVTFT and two triboelectric sensors. (b) Chronogram showing bistable latching. The triboelectric input signal reported have been manually plotted. (c) Chronogram of 4 latching bistable cycles.

Finally, we demonstrated the DEA latching with the high voltage flip-flop. The first experiments showed we were able to latch the DEA with a 5% linear actuation strain between 100 V and 300 V actuation voltage. Experiments quantifying the strain vs the triboelectric stimuli are still

ongoing and more will be performed to investigate the effects of the different triboelectric devices input parameters (speed, compression force...) on the output parameters.

Conclusion

In this chapter, we proposed to use the HVTFT as a mechanical sensor amplifier and as a high-voltage flip-flop to switch a DEA. Triboelectric sensors were implemented to demonstrate this idea. Sensor amplification was demonstrated with a triboelectric bending sensor generating an open-circuit voltage of 100 V and we showed it was able to control a 1 kV DEA actuation. Secondly, we demonstrated a high-voltage flip-flop composed of two parallel triboelectric sensors of opposite polarity connected the gate of a HVTFT. When the set triboelectric was released, the HVTFT channel was open and when the reset tribolectric device is released, the HVTFT was closed. The time constant is 100 ms and we showed we were able to switch the output voltage of a 500 V HVTFT inverter from 460 V down to 120 V and hold the state for more than 4 s. We were able to drive a 300 V DEA by controlling it with a 5% linear strain difference between on and off state.

Our approach is very innovative as neither the sensing nor the latching effect require additional electronic components to be operating and can therefore be used to drive high impedance and high voltage devices. The minimization of the size of the triboelectric devices and their integration with HVTFTs would lead to novel soft robots based on DEAs. An optimization of the HVTFTs voltage swing to switch on and off might be of interest for future work. The smaller the swing the higher the system will be able to react to very small objects or organisms triggering the triboelectric sensor. This chapter demonstrated that the HVTFTs developped in this thesis are not only good for addressing but can also be used to amplify and treat sensing signals.

8 Conclusion

8.1 Summary

For the first time, a Metal-Oxide HVTFT operating at 1 kV has been demonstrated. Their implementation with soft actuators operating at more than 500 V has been demonstrated, enabling actuation control with a voltage swing of only 30 V. Also, a high voltage flip-flop logic gate made of triboelectric sensors and a HVTFT has been demonstrated driving a DEA.

These three major breakthroughs were possible thanks to the design, the fabrication, and the integration of the HVTFT developped in the frame of this thesis. This thesis impacts both the fields of HVTFTs and DEAs by demonstrating the ability to address and control large arrays of high voltage soft actuators with an active matrix of flexible HVTFTs.

On the HVTFT part, the results of this work show that HVTFTs made of amorphous oxide semiconductor (AOS) are a powerful alternative to amorphous silicon (a-Si) at very high voltage > 500 V. Contrary to a-Si HVTFTs, zinc tin oxide (ZTO) and yttrium zinc tin oxide (YZTO) HVTFTs can achieve high on-current higher than 100 µA and, through optimization, can achieve a mobility in the order of 1 $cm^2 V^{-1} s^{-1}$.

This thesis has also an impact on the DEA field. With the HVTFT, the external bulky circuits required to drive high-voltage DEAs can be suppressed. From now on, it is possible to design matrices of HVTFTs to control large arrays of DEAs for applications such as haptic displays or soft robots. Each HVTFT requires only 30 V to switch on and off one DEA, a switching voltage that can be easily controlled with compact external electronics.

Finally, we have proven that a high-voltage latch gate could be fabricated by combining a HVTFT with two triboelectric sensors, enabling thus a bistable control of DEAs. This combination is interesting as two triboelectric devices can control the HVTFT gate voltage without the need of external sources and circuit. For DEAs, it means that we can achieve bistability without requiring mechanical tuning of the frame and the membrane.

8.1.1 Zinc tin oxide HVTFTs operating at 1 kV

Main results

In this thesis, we successfully developed arrays of HVTFT with amorphous ZTO channel semiconducting technologies. The device has a top-gate coplanar electrodes geometry and is built on flexible polyimide substrate passivated with a thin alumina layer. The semiconductor is a sol-gel processed ZTO layer spin-coated and cured at 450 °C based on chloride precursors. The HVTFT has a W/L ratio of 10 and the channel length is 500 µm long to avoid short and narrow channel effects. The source, drain and gate are made of aluminum. The gate dielectric is made of a bilayer composed of 100 nm alumina and 1 µm parylene-C. The gate is offset from the drain by 150 µm. The HVTFT breaks down at 1.1 kV and we validated operation at a voltage of 1 kV with an on-off current ratio of 20, a threshold voltage between -10 V and 0 V and a mobility in the order of 0.1 $cm^2 V^{-1} s^{-1}$. Several high voltage effects causing performance degradation were identified: A potential barrier at the offset edge, space-charge limited current, channel length modulation and high leakage current > 1 µA. We suggested a LTspice model of the HVTFT to be used in a circuit model. Optimization of the device was done by yttrium doping of the ZTO thin film. At 5% doping, the off-current dropped from several µA for ZTO to 100 nA for YZTO and space charge limited current and the potential barrier were reduced, enhancing device performances.

Impact statement

This work demonstrates that HVTFT made of AOS can operate up to 1 kV, an unprecedented high voltage while operating with high on-currents, tens of µA. It is an important step in the HVTFT field as AOS enables high on-current and high breakdown voltage HVTFTs. Using a solution-processed ZTO semiconductor for HVTFTs is the first step towards printed HVTFTs.

Outlook

Future work in this thematic includes further improvement of the HVTFTs performance at very high voltage: the off-current needs to be decreased below 1 nA to limit circuit power consumption. This can probably be achieved by further optimizing the cation stoichiometry of zinc, tin and yttrium for the YZTO semiconductor to achieve lower off-current without decreasing the on-current. The voltage swing needs to be decreased to switch the HVTFT < 1 V to be directly combined with digital electronics. In order to drop the voltage swing, we need to replace the Parylene-C with flexible higher-K dielectrics such as PDMS with ionic interpenetrated networks [177] for which the first tests we performed showed promising results. Finally, in order to decrease the high electric field effects, especially, the space-charge limited current and the potential barrier at the offset, the geometry of the HVTFT needs to be optimized by adding a field plate or by designing a dual bottom-top gate HVTFT. Also, fully printing HVTFTs would enable to achieve highly scalable, cost effective components over large

flexible surfaces. One could ultimately print the HVTFTs on the DEA frame and interconnect them together.

8.1.2 Addressing a matrix of DEAs with integrated HVTFTs

Main results

In this thesis, we successfully integrated an active matrix of HVTFT to drive a 4x4 array of DEA out-of-plane actuators. The 4x4 HVTFT and DEA matrices were stacked together and interconnected with a flexible PCB. The entire device is sealed over a 3D-printed flexible pressure chamber. The DEA are made of a 17 µm layer of PDMS encapsulated between circular carbon electrode with a 2 mm radius. A back-pressure of 50 mbars is applied to have an initial prestretch and to reach a maximum actuation at 1 kV with a breakdown at 1.1 kV. Each cell is a resistive load inverter made of a pull-up resistor (200 MΩ) and the pull-down HVTFT. The entire device is biased with a 1.4 kV power line. The HVTFTs can drive each actuator within a 30 V gate voltage swing enabling a vertical deflection of 340 µm. The time response of the system is 50 ms. The assembly operates down to a 2.5 mm radius of curvature in static bending.

Impact statement

This work on HVTFT integration with DEAs paves the way towards new devices based on multiple DEAs. With the ability to integrate low control voltage switches with DEAs allows us to envision devices enabling the independent control of matrices of hundreds or thousands of high voltage DEAs for, as an example, fast haptic display technologies.

Outlook

To go even further and to design Braille displays, miniaturization of DEAs and HVTFTs will be required (from 5 mm to 1.5 mm). On the HVTFTs side miniaturization will increase the applied electric field across the channel leading to higher high voltage effects and new problems like channel length modulation and punch-through effects [103]. On the DEA side, optimization will be required to increase the actuator displacement, by decreasing the active area. Also, at this miniaturization level, the circuit tracks of a PCB should have a high density. A circuit design optimization will be required to avoid breakdown between the high voltage and the low voltage tracks of the PCB. Finally, in order to integrate the HVTFTs on the frame of soft robots such as dielectric minimal energy structure (DEMES), we will need to test dynamically the evolution of the HVTFT characteristics in a cycling bending setup. In order to design a haptic display based on the concept we presented in this thesis, we will need to increase the blocking force of the DEAs by rigid [69] or liquid coupling [67], by combining them with spring structures [70] or by using DEAs stacks enabling higher force [36].

8.1.3 Triboelectric control of the HVTFT channel

Main results

Finally, we demonstrated that the DEAs charge could be controlled by a triboelectric signal thanks to HVTFTs. The triboelectric devices were assembled with the HVTFTs in two different configurations, the sensing and the flip-flop configuration. In the sensing configuration, only one triboelectric sensor connected to the HVTFT gate is required. The interaction with the triboelectric device directly controls the HVTFT gate voltage and therefore the channel current. We validated this operation mode by activating the HVTFT channel, charging and discharging a DEA. Small modulation of the input mechanical signal on the triboelectric device, like small bending, can be detected if the gate voltage is in the subthreshold region of the HVTFT characteristics and analog control is possible. The second operation mode was the flip-flop mode. We designed a high-voltage flip-flop with two contact-separation triboelectric pads and a HVTFT. The flip-flop keeps in memory the last signal triggered. The two triboelectrics were connected to the gate in parallel. The first triboelectric generates a negative signal (an off signal) that maintains the HVTFT in off-state and the DEA charged. The second triboelectric generates a positive signal (an on signal) that maintains the HVTFT in on-state and the DEA discharged. As the circuit at the gate is open, the triboelectric charges remain until dissipation. We were able to latch the channel of a 500 V YZTO HVTFT in on and off state for a maximum of 4 s and to control a DEA charge within this time-frame. The two triboelectric devices in parallel reproduce the effect of a set-reset flip-flop without requiring additional electronics. The assembly was then demonstrated to be able to latch the DEA in two stable positions with 5% linear strain variation for several cycles.

Impact statement

This work demonstrates that we can use the HVTFT to communicate to the DEA a signal coming from a triboelectric device. It also shows that self-powered triboelectric generators can be used to control the state of a DEA, enabling to drive numerous DEAs with one power supply and no external switching circuit. These results are promising for DEAs for soft-locomotion and for implementing sensors in soft-robots and grippers made of DEAs.

Outlook

In order to optimize the voltage applied at the gate of the HVTFTs by the triboelectric devices, we need to avoid capacitive division between the two triboelectric generators and the HVTFTs. In order to avoid this, we need the capacitance of the triboelectric devices to be negligible when the devices are passive so that the voltage is only controlled by the HVTFT gate. Also, we need to design triboelectric devices with a higher capacitance in trigger state than the HVTFTs. For further integration, it could be interesting to fabricate together the DEA and the triboelectric device in the same process.

8.2 Perspectives

The proofs of concept of this PhD thesis demonstrated that HVTFT can be integrated with DEAs to fabricate complex flexible devices requiring several independent actuators. From this principle, novel devices can be fabricated based on DEAs and HVTFTs integration.

Adding collision and pressure sensor inside DEA grippers would enable catching and immobilizing small bodies displacing fast but unable of high forces such as flies or mosquitoes. The integration and application of the work we presented in the last chapters would enable the creation of such a device. A concept for such a device is shown in Figure 8.1. The idea behind this device is to use the triboelectric device in a single electrode latching configuration. When an electropositive or negative object hits the triboelectric sensing layer, charges are created at the gate of the HVTFT triggering the bending of the DEA in a gripper configuration and holding bending until the triboelectric charges dissipate releasing thus the actuator.

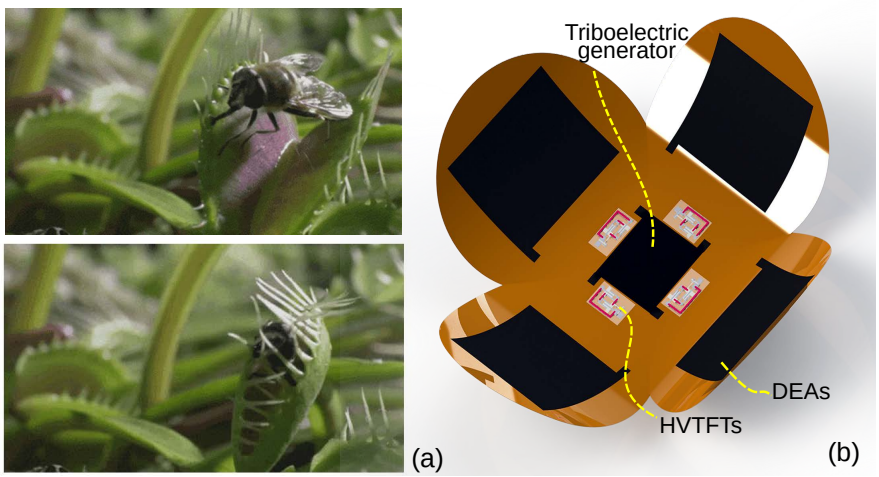

Figure 8.1 – (a) Picture of a Venus flytrap closing on a fly. (b) Concept of DEA flytrap made of integrated DEAs grippers controlled by the HVTFTs transfering the sensing signal on the triboelectric generator.

Being able to control DEAs with triboelectric sensor signals would enable unprecedented automated systems able to interact with their environment autonomously. This implies the ability to integrate together DEAs, HVTFTs and the triboelectric sensor. Applications could include grippers behaving like Venus Flytraps as shown in Figure 8.1, ie automatically closing on an object entering in contact with its interior. We would integrate a triboelectric device at the center of the "flower" composed of four DEAs driven by integrated HVTFTs. The collision of a body would trigger the triboelectric device, latching the HVTFT and closing the DEAs "flower".

We could also imagine a peristaltic pump made of a sequence of zipping actuators [35] transporting a liquid from one chamber to another. The closing of one DEA valve would trigger the triboelectric sensor leading to the opening of the next DEA valve in the sequence.

Also automated soft locomotion could be done by detecting the DEA motion. We could imagine a wheel based on [178] automatically rolling on the ground instead of high-voltage rails or a 4-legged robot as in [34], where the motion of one leg triggers the motion of the next one.

The main challenges to achieve soft robots made of DEAs-HVTFTs would be (1) to decrease the voltage swing of the HVTFT, so that it switches on and off for very small variations of input signal (e.g. triboelectric voltage), (2) to determine a good trade-off for the DEA ground electrodes area and the triboelectric detection electrodes, (3) to fabricate a triboelectric device able to generate an open circuit voltage > 30 V with high sensitivity detection and (4) fabricate a DEA with low actuation voltage and high blocking force.

8.3 Concluding remarks

An integrated high voltage driving electronics is a necessity in the field of high voltage actuators to design systems requiring tens to thousands of independent actuators. It is also capital to interface low voltage sensors with these high voltage actuators to design compact, complex, automated machines for practical applications. The field of dielectric elastomer actuators, in particular, will expand as more and more high voltage components such as high voltage thin film transistors, and diodes get developed, optimized and integrated. The novel technology described in this work is pioneer in integrating an array of high voltage actuators and thin film transistors. Additionally, being able to use the combination of a HVTFT and triboelectric devices as latch logic gates to induce electrical bistability in DEAs enables a wide range of new applications e.g. in the field of grippers or automated soft locomotion.

As a consequence, this PhD thesis on HVTFTs opens unique new perspectives not only in the field of dielectric elastomer actuators and thin film transistors, but also in the field of soft robotics and active displays.

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List of Abbreviations

a-Si	amorphous silicon
AFM	atomic force microscopy
ALD	atomic layer deposition
AOS	amorphous oxide semiconductor
CdSe	cadmium selenium
CMOS	complementary metal oxide semiconductor
CVD	chemical vapor deposition
DEA	dielectric elastomer actuator
DES	dielectric elastomer switch
DSC	differencial scanning calorimetry
EDXS	electron dispersive X-ray spectroscopy
eg	exampli gratia
FET	field effect transistor
HV	high voltage
HVOTFT	high-voltage organic thin film transistor
HVTFT	high voltage thin-film transistor
IGZO	indium gallium zinc oxide
LCD	liquid crystal display
MEMS	microelectromechanical systems
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transistor
MOx	metal oxide
OLED	organic light emitting diode

PAA	poly(acrylic acid)
PDMS	polydimethylsiloxane
PET	polyethylene terephthalate
PhD	doctor of philosophy
PI	polyimide
poly-Si	polycristalline silicon
PU	polyurethane
SCLC	space charge limited current
TEM	transmission electron microscopy
TENG	triboelectric nanogenerator
TFT	thin-film transistor
TGA	thermogravimetric analysis
TMA	trimethylaluminium
TrEG	triboelectric generator
VHB	Very High Bond
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
YZTO	yttrium zinc tin oxide
ZTO	zinc tin oxide

List of publications

Journal articles

- Marette, A., Poulin, A., Besse, N., Rosset, S., Briand, D., Shea, H. (2017). Flexible zinc–tin oxide thin film transistors operating at 1 kV for integrated switching of dielectric elastomer actuators arrays. Advanced Materials, 29(30).

In preparation

- Marette, A., Shea, H., Briand, D., Yttrium zinc tin oxide high voltage thin-film transistors. (Manuscript in preparation)

- Marette, A., Haque, R., Ji, X., Shea, H., Briand D., A high voltage flip-flop gate made of triboelectric devices and thin film transitors to drive dielectric elastomer actuators. (Manuscript in preparation)

Conference proceedings

- Marette, A., de Saint-Aubin, C., Rosset, S., Briand, D., Shea, H. (2017, June). Full integration of a dielectric elastomer actuator with a flexible 1 kV thin-film transistor. In Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS), 2017 19th International Conference on (pp. 2063-2066). IEEE. **Best paper and poster award**.

Oral presentations

- Marette, A., Rosset, S., Shea, H., Briand, D. (2017, December). Solution processed Y-doped zinc tin oxide with superior performance at very high-voltage. In Materials Research Society fall meeting (MRS fall 2017).

- Marette, A., Briand, D., Poulin, A., Rosset, S., Shea, H. (2016, November) Flexible zinc-tin oxide thin-film transistors operating at 1kV to drive soft actuators. In Materials Research Society fall meeting (MRS fall 2016).

- Marette, A., Briand, D., Poulin, A., Rosset, S., Shea, H. (2016, May) Solution-processed zinc-tin oxide thin-film transistors operating at 1kV on flexible substrate. In European Materials Research Society spring meeting (EMRS spring 2016).

Poster presentations

- Marette, A., Khan, S. Poulin, A., Shea, H., Briand, D. (2017, September). Printing flexible ZTO thin film transistors for high-voltage applications. In The Swiss Conference on Printed Electronics and Functional Materials (Swiss e-print 2017).
- Marette, A., Poulin, A., Besse, N., Schlatter, S. Rosset, S., Briand, D., Shea, H. (2017, June). A flexible 4x4 array of 1 kV dielectric elastomer actuators driven by an integrated matrix of high-voltage thin film transistors. In International conference on Electromechanically Active Polymer (EAP), transducers and artificial muscles (EuroEAP 2017).
- Marette, A., Poulin, A., Rosset, S., Briand, D., Shea, H. (2016, June).Flexible 1kV thin-film transistor driving out-of-plane dielectric elastomer actuator. In International conference on Electromechanically Active Polymer (EAP), transducers and artificial muscles (EuroEAP 2016).
- Marette, A., Poulin, A., Shea, H., Briand, D. (2015, September). Solution processed metal oxide TFT for high voltage electrostatic actuation. In The Swiss Conference on Printed Electronics and Functional Materials (Swiss e-print 2015). **Best poster award**.

Curriculum Vitae

Alexis Marette
14 rue Louis Bourguet
2000 Neuchâtel

+41 7 87 659 515
alexis.marette@epfl.ch

Education

2014-2018	**PhD** in Microengineering at Ecole Polytechnique Fédérale de Lausanne (EPFL), Neuchâtel, Switzerland. Title: *High voltage metal oxide thin film transistors to drive arrays of dielectric elastomer actuators.* *Directors: Prof. Herbert Shea, Dr. Danick Briand*
2010-2013	**Engineering diploma (Bachelor and Master of Science)** in Physics, Electronics and Materials at Grenoble-INP Phelma, Grenoble, France
2008-2010	**Preparatory classes (CPGE)** in Mathematics, Physics and Engineering at Lycée Rabelais, Saint Brieuc, France

Professional experience

2013-2014	**Internship** on biodegradable flexible sensors and electronics at EPFL, Neuchâtel (SAMLAB) *Supervisor: Dr. Danick Briand*
2013	**Master project** on microfluidic chip design for C. Elegans micro-embryo imaging at EPFL, Lausanne(LMIS-2). *Supervisor: Dr. Matteo Cornaglia*
2012	**Internship** on optical bandgap simulation in photonic crystals at Trinity College, Dublin. *Supervisor: Dr. Tatiana Perova*

Language skills

French: Native, **English**: Fluent, **German**: Fluent, **Italian**: Beginner

Technical skills

Engineering	Cleanroom microfabrication, Thin-films, Photolithography, Inkjet printing
Programming	C, Labview, Matlab
CAD	Solidworks
Office	LaTeX, Origin

Awards and distinctions

- **Best paper and poster award**: International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers '17).
- **Best poster award**: The Swiss Conference on Printed Electronics and Functional Materials (Swiss e-print 2015).

Selected publications

A. Marette, A. Poulin, N. Besse, S. Rosset, D. Briand, and H. Shea, "Flexible Zinc–Tin Oxide Thin Film Transistors Operating at 1 kV for Integrated Switching of Dielectric Elastomer Actuators Arrays," Advanced Materials, vol. 29, no. 30, Aug. 2017.

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G. Mattana, D. Briand, A. Marette, A. Vásquez Quintero, and N. F. de Rooij, "Polylactic acid as a biodegradable material for all-solution-processed organic electronic devices," Organic Electronics, vol. 17, Feb. 2015.