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Tunable RF Phase Shifters Based on Vanadium Dioxide Metal Insulator Transition

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ABSTRACT This paper presents the design, fabrication, and electrical characterization of a reconfigurable RF capacitive shunt switch that exploits the electro-thermally triggered vanadium dioxide (VO_2) insulator to metal phase transition. The RF switch is further exploited to build wide-band RF true-time delay tunable phase shifters. By triggering the VO_2 switch insulator to metal transition (IMT), the total capacitance can be reconfigured from the series of two metal–insulator–metal (MIM) capacitors to a single MIM capacitor. The effect of bias voltage on losses and phase shift is investigated, explained, and compared to the state of the art in the field. We report thermal actuation of the devices by heating the devices above VO_2 IMT temperature. By cascading multiple stages a maximum of 40° per dB loss close to 7 GHz were obtained.

INDEX TERMS Vanadium dioxide, phase transition, RF switch, true-time delay, phase shifter, tunable capacitor.

I. INTRODUCTION

Phase shifters are key components for beam-steering implementations, smart adaptive antennas and scanning applications for wideband communications and remote sensing systems. Phase shifter based on ferroelectric technology have been shown to offer interesting RF performances in terms of tunability, losses and power consumption [1], [2]. In parallel RF distributed MEMS transmission lines (DMTL) have been proven to be a very interesting solution to achieve a high phase shift over a wider frequency band if compared to traditional solid-state implementations (PIN diodes, GaAs FET), with a DC power consumption limited to tenths of milliwatts [3].

Strongly correlated functional oxides exhibiting metal to insulator transition have recently emerged in research as promising materials for a large number of applications, including steep-slope transistors [4], RF switches [5], [6], reconfigurable filters [7], [8] and antennas [9]. Vanadium dioxide (VO_2) has proven to be one of the most interesting among such materials thanks to its large contrast in conductivity between its two states and the possibility of inducing the phase transition by electrical excitation [10].

Compared to MEMS switches, VO_2 switches offer clear advantages such as an easier integration in microelectronic technological processes, smaller footprint and a three order of magnitude faster switching time [11]. A switched line phase shifter with thermally actuated VO_2 switches has been previously demonstrated in microstrip technology [12].

In our previous work [13] we presented for the first time a shunt capacitive switch reconfigurable by means of electrically triggered VO_2 phase transition to build true-time delay phase shifters by periodically loading a coplanar waveguide (CPW) with capacitive switches (Fig. 1). We validated the concept by fabricating, designing and characterizing an 819 μm long unit. In this work, we show improved results for thermally actuated cells by demonstrating up to 40° phase

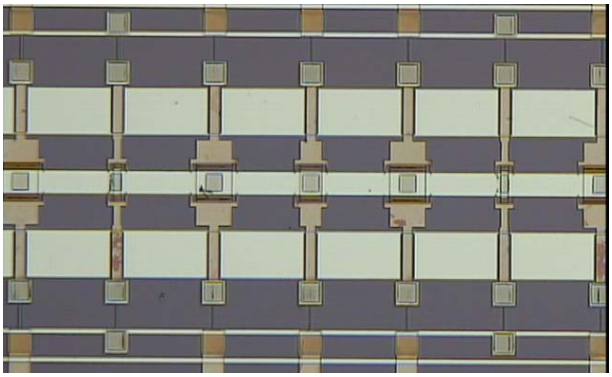

FIGURE 1. Optical image of the CPW phase shifter showing the cascaded VO_2-based capacitive shunt switches designed to achieve 3-bits phase states.

shift per dB loss at 7 GHz in a 6-cell phase shifter. We furthermore present two possible scheme to bias cascaded cells to obtain a multi-state tunable phase shift.

II. RECONFIGURABLE CAPACITIVE SHUNT SWITCH

The reconfigurable capacitive shunt switch consists of two fixed MIM capacitors in series, C_S and C_G, where the first can be short-circuited by actuating a VO_2 two-terminal switch (Fig. 2). Below the phase-transition temperature and when no bias is applied, the VO_2 is in its insulating state so that the switch exhibits a high resistance level and can be considered as an open circuit. The two capacitors are then electrically in series, offering an equivalent capacitance $C_{TOT} = C_G \cdot C_S/(C_G + C_S)$. Whenever a bias larger than the switch actuation voltage is applied, the VO_2 film phase changes to its conductive state and the switch exhibits a low resistance value. In this configuration, the C_S capacitor is short-circuited by the switch and the equivalent capacitance between the signal and the ground line will be simply C_G. In this way the VO_2 switch allows reconfiguring the loading capacitance between C_G and C_{TOT}.

The VO_2 switch can be electrically actuated by means of a bias line decoupled from the RF signal using a resistor fabricated with a 25 nm-thick Chromium (Cr) film. The switch resistance is in the high state until a critical DC power is achieved, which triggers a steep insulator to metal transition (Fig. 3). In order not to affect the RF performance, the switch dimensions are chosen to obtain a high value of resistance in the off-state (> 1 kΩ) and low value in the on-state ($\sim 1\ \Omega$), while keeping a reasonably low actuation voltage. Thus, given a 200 nm VO_2 thickness, the switch was designed with a width of 30 μm and a length of 1 μm.

III. FABRICATION

The phase shifter was fabricated using standard microelectronics processes starting with a high-resistivity 525 μm thick silicon substrate passivated with 500 nm LPCVD-deposited SiO_2 (Fig. 4). The VO_2 film was prepared by reactive magnetron sputtering deposition starting from a Vanadium target, as described in [4]. After the deposition, a resistivity ratio between insulating and conducting phase higher than 3 decades was measured with Van der Pauw measurements performed at different temperatures (Fig. 5). The film was then patterned by using photolithography and wet etching. The bias resistors were realized by lift-off of a 25 nm thick Cr film. A 200 nm thick Al film was subsequently deposited and patterned with lift-off to act as bottom metal. A 200 nm thick SiO_2 film was sputtered as insulating layer and as a dielectric for MIM capacitors. Vias were opened by photolithography and dry etching. A final 800 nm thick Al top metal layer was deposited to create the CPW and the contacts on the bottom metal bias lines.

IV. UNIT CELL PERFORMANCE

The CPW was designed with a signal line width (w) of 100 μm and a ground plane spacing (g) of 150 μm to obtain an unloaded characteristic impedance of 65 Ω. The design of the unit cell for the phase shifter was done following the method described in [14] in order to maximize the phase shift for the minimum insertion loss (*IL*). Starting from the chosen values of characteristic impedances in the ON and OFF state, respectively $Z_{ON} = 42\ \Omega$ and $Z_{OFF} = 58\ \Omega$, and having chosen the Bragg frequency to be three times the frequency of design for the phase shifter, for a design frequency of 10 GHz the required unit cell length (*CL*) was calculated to be 819 μm. The computed capacitances were $C_{ON} = 143$ fF and $C_{OFF} = 26$ fF resulting in a capacitance ratio of 5.5. Thus the MIM capacitances for the reconfigurable capacitive shunt switch are calculated as $C_S = 31.7$ fF and $C_G = 143$ fF. A schematic of the mask of the single cell is shown in Fig. 6.

The device was characterized by using an Anritsu VectorStar MS4647B Vector Network Analyser to measure *S*-parameters, a HP 4155B Semiconductor Parameter Analyser to provide the bias to operate the VO_2 switches and a Cascade Summit prober with a thermo-chuck to control the substrate temperature.

Fig. 7 shows a comparison between Ansys HFSS simulations of *S*-parameters and measurements with no bias applied at 20°C (OFF state) and 100°C (ON state), well above the phase transition temperature where the VO_2 film becomes fully conductive (see Fig. 5). When the switches are turned off (20 °C and no bias) the insertion loss is 0.43 dB at 10 GHz, while in the ON state the insertion losses are increased both in simulation and measurements. The discrepancy between measured and simulated values can be attributed to resistive losses along the line and in the VO_2 switch for the ON state, besides extra reflection due to parasitic capacitances caused by biasing lines not included in the simulations.

The devices were measured for different bias values above the actuation voltage of the VO_2 switches (Fig. 8). While the insertion loss seems to increase by increasing the bias, the loss at the design frequency is improved when the switch is at its lowest possible resistance value, obtained measuring at 100 °C. This behavior can be explained looking at

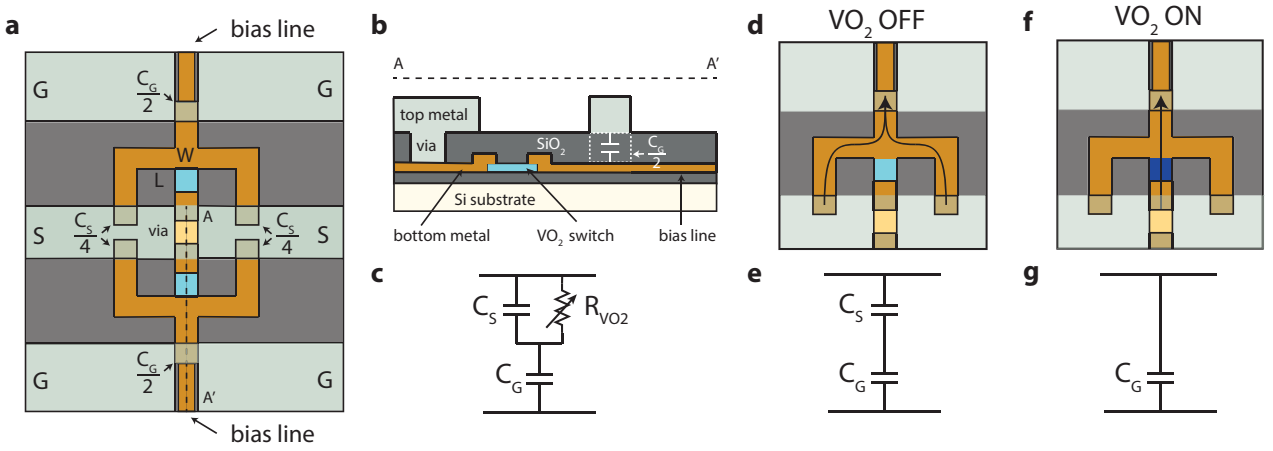

FIGURE 2. **a) Schematic of the reconfigurable capacitive shunt switch. A via connects the signal top metal line with a metal line underneath in contact with a VO_2 switch. Four MIM capacitors ($C_S/4$), two per side, lay between the signal line and the underneath metal, whilst other two MIM capacitors ($C_G/2$), one per side, lay between the ground planes and the underneath metal. b) Cross-section beween signal and ground plane highlighting the via between the two metals, the VO_2 switch and the capacitance $C_G/2$. c) Equivalent circuit of the capacitive divider, with the VO_2 switch modeled as a variable resistor R_{VO2}. d) Preferential path seen by the signal when the VO_2 is in insulating phase, with an equivalent capacitance given by the series of C_S and C_G. e) Equivalent circuit for the insulating phase, where the switch can be modeled as an open switch ($R_{VO2} > 1$ kΩ). f) When the VO_2 film is in its conducting phase the capacitors $C_S/4$ are short-circuited by the switch ($R_{VO2} \sim 1\Omega$) and g) the equivalent capacitance seen between signal and ground equals C_G.**

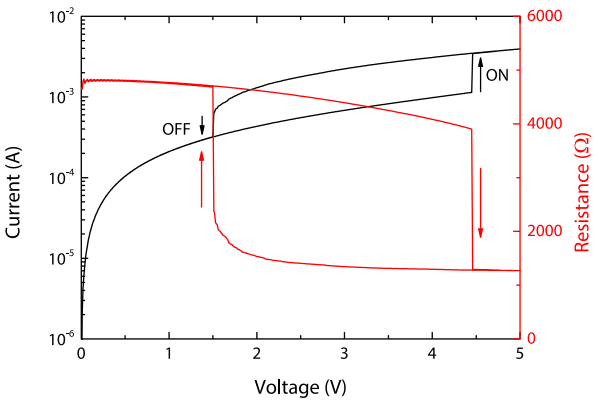

FIGURE 3. **Current versus voltage electrical characteristic and extracted resistance of the VO_2 switch with an integrated serpentine resistor of 1.2 kΩ in series. The arrows indicates the insulator-metal transition and metal insulator transition.**

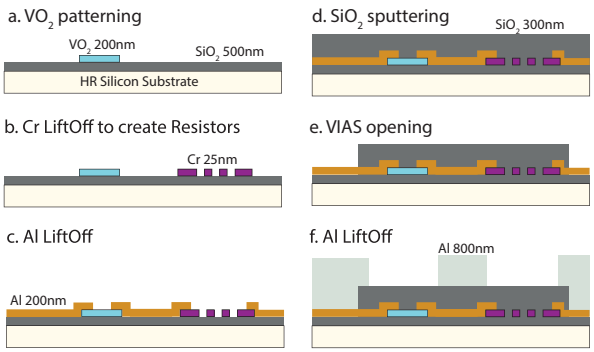

FIGURE 4. **Fabrication process of the capacitive shunt switch with VO_2 switches and integrated bias resistors.**

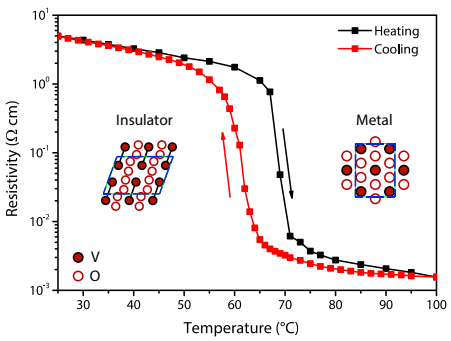

FIGURE 5. **Dependence of resistivity on temperature for the deposited VO_2 film.**

the losses not due to reflection. While in the OFF state the insertion losses and no-reflection losses are almost coincident, indicating a good match, in the ON state the behavior depends on the bias. At 20 V the *IL* and total losses are similar, while at 30 V and 40 V a considerable part of the *IL* is due to the mismatch. At 100 °C the *IL* are lower than at the considered bias points and the no-reflection losses are minimized, showing better accordance with the FEM simulations.

The measured phase shift with respect to the OFF state increases with the applied bias but tends to saturate around 5 GHz for 40 V bias, while at 100 °C it is linear over the considered frequency band (Fig. 9). The phase shift per dB loss shows as well that the best trade-off is obtained for higher bias and indicates that best performances are obtained at 100 °C, where a maximum of 16° per dB loss is obtained slightly below the design frequency.

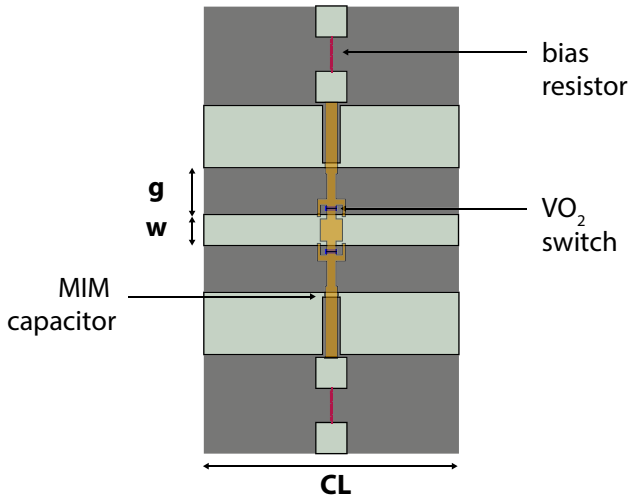

FIGURE 6. Schematic of the unit cell with indicated dimensions $w = 100$ μm, $g = 150$ μm and $CL = 819$ μm.

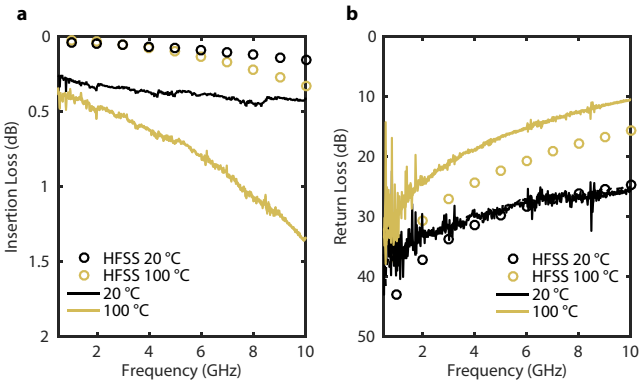

FIGURE 7. (a) Insertion Loss and (b) Return Loss of the measured unit cell at 20 °C and 100 °C. Circles correspond to ANSYS HFSS simulations. The simulations have been performed using the VO_2 resistivity measured at 20 °C for the OFF state and 100 °C for the ON state.

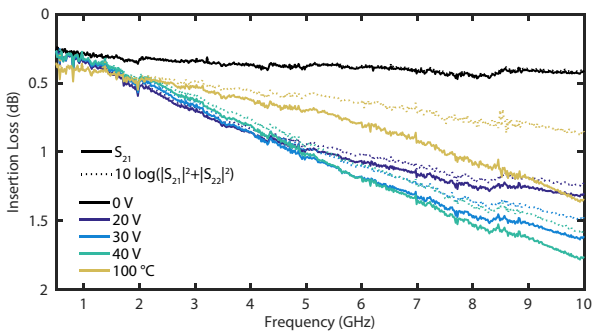

FIGURE 8. Insertion loss (continuous lines) and no-reflection losses (dotted lines) versus frequency, measured at 20 °C substrate temperature for 0 V, 20 V, 30 V and 40 V bias voltage and at 100 °C with no applied bias.

The limited performance of the device when electrically actuated suggests that for the applied bias voltages, the conduction channel in the VO_2 switch does not extend to the entire film width [15] and the resulting resistance is still not low enough to grant a full capacitance reconfiguration and to prevent significant RF losses. We can assume that by applying a larger bias voltage, thus by injecting a larger current, the performance will converge to the one measured at 100 °C.

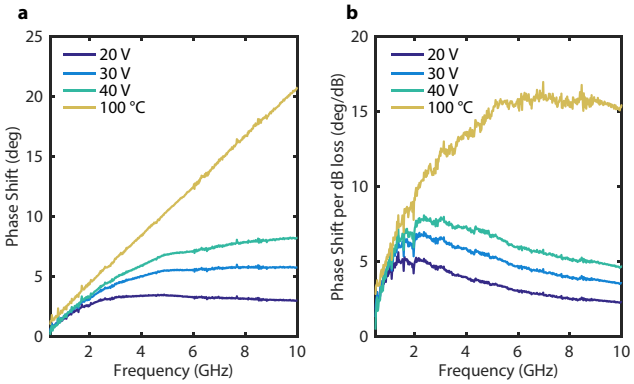

FIGURE 9. (a) Phase shift and (b) phase shift per dB loss extracted from *S*-parameter measurements at 20 °C for 0 V, 20 V, 30 V and 40 V bias voltage at and at 100 °C with no applied bias.

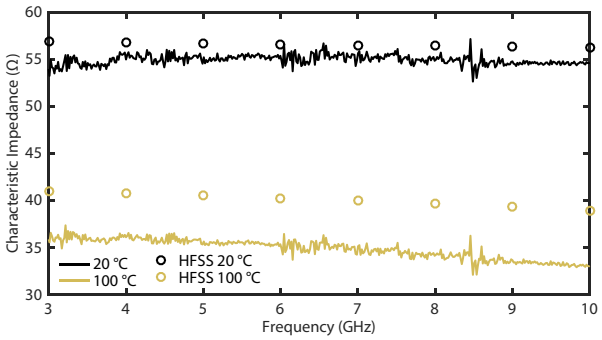

FIGURE 10. Equivalent characteristic impedance of the unit cell, extracted from measurements at room temperature and at 100 °C (solid lines), and from ANSYS HFSS simulations (circles).

The equivalent characteristic impedance of the loaded line was calculated using the method proposed in [16] and it is shown in Fig. 10. In the OFF state the extracted characteristic impedance is about 55 Ω at 10 GHz, not far from the simulated value of 56 Ω. In the ON state at 100 °C the extracted characteristic impedance is lower than the simulated one, in accordance with the larger measured phase shift and larger insertion loss due to reflection.

V. PHASE SHIFTER

In order to improve the performance, new devices were fabricated starting from a 300 nm thick VO_2 film deposited by Pulsed Laser Deposition (Solmates SMP 800) in oxygen atmosphere of a V_2O_5 target. The bottom metal was realized with Ti/Al respectively 20 nm and 800 nm thick, while the top-metal was made of a 2 μm thick Al film. The thicker VO_2 and metal layers provide lower resistive loss compared to the previously used process. The design of the cell was slightly varied and a tapered ground plane was

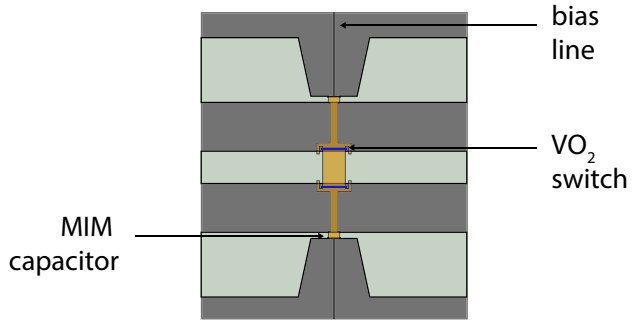

FIGURE 11. Schematic of the improved phase-shifter unit cell with tapered ground plane in proximity of the biasing line.

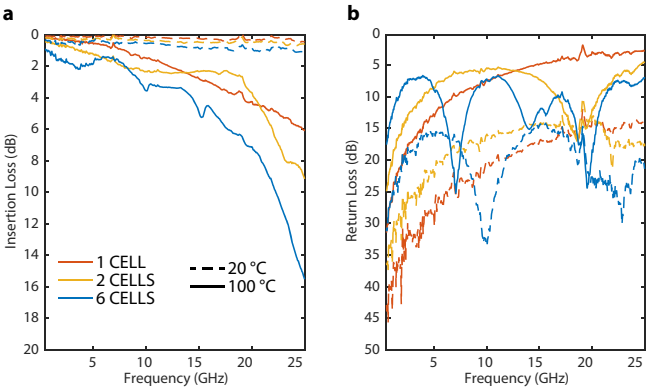

FIGURE 12. Measured (a) insertion loss and (b) return loss for 1,2 and 6-stage phase shifter with all stages in off-state (measured at 20 °C, dashed line) and all stages in on-state (measured at 100 °C, solid line).

designed to minimize the parasitic capacitance between the biasing line and the ground plane itself. The cell length and capacitors dimension were kept the same. The VO_2 switch width was increased to 70 μm, while the length was kept 1 μm. A schematic of the mask of the new single cell is shown in Fig. 11.

In Fig. 12 we report the S-parameter in OFF and ON states (measured with no applied bias at temperatures of 20°C and 100°C, respectively) of three different phase shifters composed by one, two and six cells. Fig. 13 shows that by cascading multiple stages a larger phase shift can be obtained and an improved phase shift per dB loss of 40° is achieved since reflection losses do not sum up from stage to stage.

VI. MULTISTAGE ACTUATION

To obtain the desired phase shift we can cascade multiple unit cell in a CPW. We propose two different biasing schemes to control each cell (Fig. 14). In the first scheme, the actuation voltage of the VO_2 switch of each stage is set to a specific value by engineering the corresponding biasing resistor value. The actuation is then performed using the RF signal line as bias line and a common DC ground line for all the stages. When a certain DC bias is applied to the signal line the obtained phase shift will be deriving from the stages with actuation threshold below the applied bias. Increasing

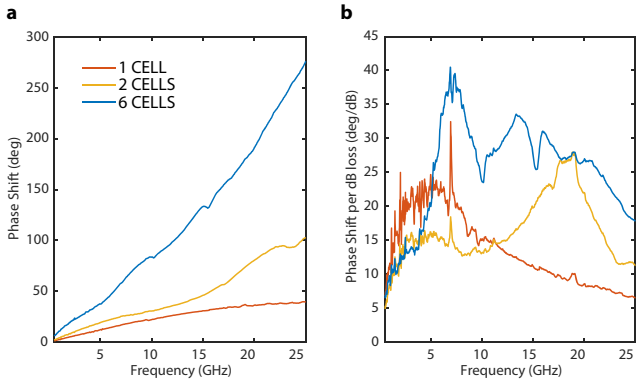

FIGURE 13. (a) Phase shift and (b) phase shift per dB loss for 1,2 and 6-stage shifter between the two extreme states: all stages in off-state at 20 °C and all in on-state at 100 °C.

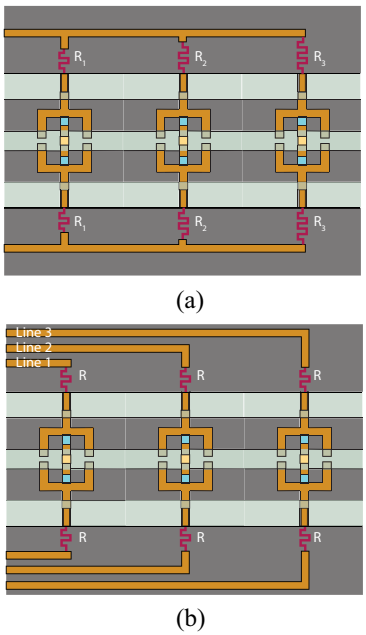

FIGURE 14. a) Biasing schemes with single bias line but different resistor values for each stage to modify the threshold voltages of the VO_2 switches and (b) scheme with separate biasing "bit" line for each stage.

the bias, other stages will be actuated and the phase shift will increase. In the second scheme, separate bias "bit" lines are created for each stage or set of stages and the RF signal line is used as a DC ground: when a bit line is set to a voltage higher than the switch threshold voltage, bit to "1", the corresponding stage will turn ON and provide a phase shift.

Using this latter "multi-bit" scheme we can make predictions on a phase shifter desing by matematically cascading the S-parameter of the unit cell shown in Fig. 12. Considering a phase shifter made out of three of this cell, each one controllable with a separate bit line, we show in Fig. 15 the calculated losses for the phase shifter in four configuration, all stages OFF (000), first stage ON (100), first two stages ON (110), all stages ON (111). Fig. 16 report the obtained phase shift with respect to the all OFF (000) state.

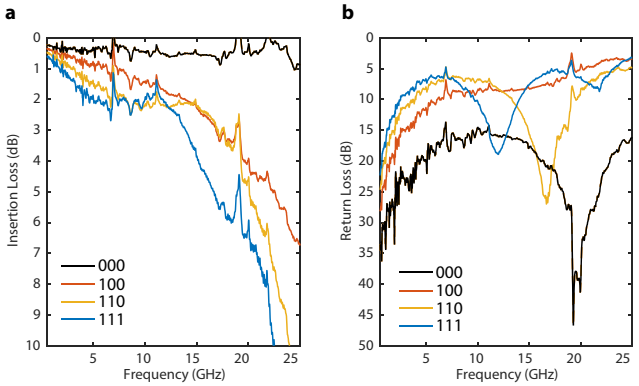

FIGURE 15. Predicted (a) insertion loss and (b) return loss for a 3-stage phase shifter biased with three bit lines in four different configuration, where bit "0" stands for OFF state of the cell and bit "1" stands for ON state.

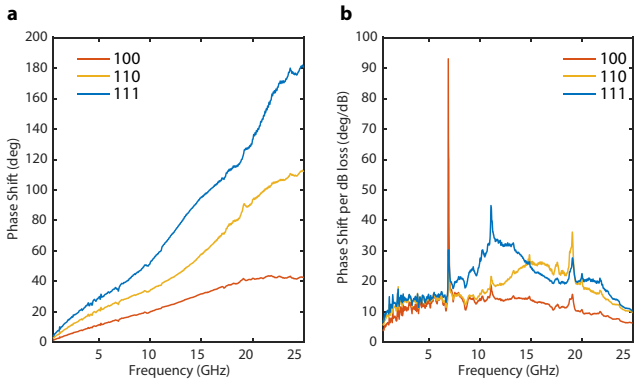

FIGURE 16. Predicted (a) Phase shift and (b) phase shift per dB loss of a 3-stage phase shifter biased with three bit lines for the indicated bits states compared to the all OFF state (000).

As expected, when turning ON more stages the phase shift increases and the phase shift per dB loss is maximized.

VII. CONCLUSION

We reported a VO_2-based capacitive shunt switch as fundamental building block that can be cascaded to obtain TTD phase shifters. The working principles as well as the fabrication method have been presented and validated by simulating, designing, fabricating and characterizing a unit cell. The extracted considerable insertion losses are largely due to the impedance mismatch and could be easily reduced by improving the MIM capacitors design. The measurements at different bias voltage and at high temperature have revealed the need of a better optimization of the VO_2 switch in order to have lower resistance values in the electrically actuated ON state so to match the good performance obtained at high temperatures.

A 6-stage phase shifter was fabricated and measured. A 40° phase shift per dB loss was achieved around 7 GHz, showing that the VO_2-based reconfigurable capacitive switches can offer a unique opportunity to build ultrafast and reliable phase shifters. Moreover, we presented two possible biasing strategies for multistage actuations to achieve a tunable phase shift by controlling it with either several bits line or with a single analog one. VO_2 based phase shifters are realized with an easier and cheaper fabrication process with respect the RF MEMS counterpart and have 100 to 1000 time faster switching time, which makes them interesting for fast airborne applications. Actuation voltages can be potentially lower than RF MEMS ones while the insertion loss is expected to decrease by further improving the VO_2 material properties and design implementation.

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