PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of

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IGCT Switching Behaviour Under Low Current Conditions

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Abstract

As MVDC technology is slowly finding its way into the area of energy distribution, there is a need for reliable, efficient, compact and low maintenance medium voltage DC-DC converters, as a counterpart to AC transformers. Given the typical operating conditions and the design practices, IGCT manufacturers have paid, so far, little attention to the switch's behaviour under low loads (below 10% of the device rated current) and this information is mostly unavailable in the datasheets. Low current turn-off performance of the IGCT, typical to some resonant converters, is explored throughout this paper, supported by TCAD simulations and test results obtained from a dedicated test setup. These tests show the prolonged duration of the turn-off process as the turn-off current decreases, which must be correctly taken into account during converter design.

1. Introduction

Motivation in exploring the Integrated Gate Commutated Thyristor (IGCT) technology for DC-DC conversion, comes from the increased research interests in MVDC power distribution networks, where these converters will perform the role of a DC transformer. Typical applications examples are marine [1], wind-park collection grids [2], large PV generation [3] and various industrial facilities. As these MVDC power distribution networks are still in an early evaluation and planning phase, there is a great research opportunity to develop novel and flexible conversion technologies to enable further practical realizations.

Lot of research has already been done in the field, mostly based on Insulated Gate Bipolar Transistor (IGBT) technology [4], [5] due to its popularity and availability. Promising alternative to IGBTs is found in IGCT technology that has already proven itself in the applications such as medium voltage inverters [6] and rectifiers [7]. It is already a mature technology found in the grid interties, metal drives, solid state breakers [8] etc. with over 1GW of installed power in various pieces of equipment [6]. Common aspect for all these applications is the hard switching of the semiconductor device under large currents and switching frequencies up to 900Hz. Successful demonstration of implementing the IGCT in three phase dual active bridge topology is presented in [9] with suggested further improvements in terms of power losses and efficiency.

Despite IGBT being preferred switching device in most of the proposed converter topologies, IGCT as a switching element offers some advantages over IGBT [10] as they have been mostly optimized for hard switched conditions considering high current values. Given its thyristor structure, conduction losses of the IGCT are noticeably lower when compared to the IGBT of the same ratings; turn-on losses can be neglected most of the time (due to inductive load current) while turn-off losses are comparable to that of IGBT. Other positive aspects are high short-circuit capability, high reliability and large Safe Operating Area (SOA) as well as better utilization of the silicon surface for the same type of packaging, allowing IGCT higher current carrying capability (full circular surface of silicon opposed to a number of IGBT rectangular dies on a round surface of a package). Considered negative aspects include rather large gate driver circuit and inability to control di/dt during turn-on which leads to the requirement of the clamp circuit for hard switching applications, further increasing number of components needed for the final converter circuit. However, the di/dt clamping inductor offers an advantage as it helps in limiting the short circuit current.

Resonant converter topologies (e.g. [11] and [12]) present the opportunity for the IGCT to further maximize its performance: low current turn-off could lead to significant decrease in accompanying energy losses, leaving it only with conduction losses which are already the lowest among the similar switching devices. Resonant operation allows reconsidering the structure and the role of the clamp circuit due to the presence of the resonant tank on the load side which already lowers the turn-on di/dt, inherently protecting the free-wheeling diodes. All being said brings the need to investigate the IGCT at low current switching conditions in order to gain knowledge and deeper understanding of switching transients duration, di/dt values, SOA conformity and switching energy losses in hard switching low current turn-off operation. This paper focuses exactly on this topic, presenting the results from Technology Computer-Aided Design

ISBN 978-3-8007-4646-0

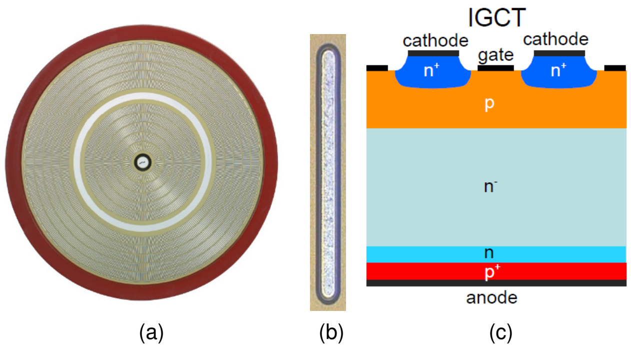

Fig. 1: a) GCT wafer, top view b) GCT finger, top view c) GCT simulation geometry, vertical cross section.

(TCAD) simulations along with the experimental results from the commissioned test setup. Detailed simulation results are presented in section 2 while the description of the test setup and experimental results are given in sections 3 and 4.

2. TCAD Simulations

TCAD model of the test IGCT was implemented in the Synopsis Sentaurus TCAD simulation package capable of accurately predicting semiconductor behavior under different user specified loads. The tool is based on the finite element method for solving the fundamental partial differential equations representing the silicon wafer in a semiconductor device e.g. transport and diffusion equations. One of the advantages of the package, interesting for this paper, is the ability for the user to define SPICE based description of the circuit around the TCAD modelled device in order to predict the behaviour of the given device under the specific circuit conditions. This fact is used to obtain the first turn-off waveforms of the IGCT under test and later compare the simulation data to the actual experiment.

IGCT is simulated in the typical double pulse circuit environment (presented in Fig. 9), with the parameters given in Table 1, in order to mimic the actual test setup conditions to the most realistic extent. The model of the semiconductor is the detailed geometry simulated in finite element manner. The difference between the actual test setup and the simulation is that the simulation's freewheeling diode D_{FW} and the clamp circuit diode D_{CL} are implemented as the ideal diodes.

Figures 1a-1c roughly show the steps in modelling of the semiconductor geometry. GCT wafer (Fig. 1a) consists of many GCT fingers (Fig. 1b) spread across the circular surface of the wafer. Modelling of all the fingers would be very time consuming and would not considerably improve the accuracy of the model; instead, only one GCT finger is modelled and simulated in 2D with half the geometry and symmetrical boundary condition along left and right edges (Fig. 1c). By using proper upscale coefficients, all the values of interest for the full GCT wafer are obtained.

Simulations are performed to test the turn-off behaviour at different low current levels, two temperatures of 30°C and 115°C and the fixed value of the DC-link voltage of 2500V. Different temperatures were used in order to simulate the switch's behaviour during start up (30°C) and under normal operating conditions (115°C). Turn-off current and voltage waveforms, under hard switching conditions, of the Device Under Test (DUT) are presented in Fig. 2 and Fig. 4. Current and voltage waveform pairs representing one turn-off event at the given value of the turn-off current are plotted using the same color for easier identification. Fig. 2 and Fig. 4 clearly show the shortening trend of the turn-off transient with increasing values of the turn-off current, influenced by the rising dV/dt between anode and cathode of the IGCT (directly proportional to the turn-off current). Parameter used to evaluate this trend is turn-off delay time (t_{DOFF}) and it is defined as the elapsed time between the moment of turn-off electrical command signal and the moment when anode current falls to the 40% of its starting value [13]. The electrical command signal is not explicitly shown in Fig. 2 and Fig. 4 but the waveforms are aligned so that this signal falls to -20V at 0.1 μs on the time axis. Fig. 6 shows the values extracted directly from the simulated waveforms from Fig. 2 and Fig. 4 along with the fitted curve to represent the sample and visually present the trend. Figures also show the strong influence of the working temperature on t_{DOFF}.

Fig. 3 and Fig. 5 show the power losses waveforms for the full set of turn-off currents used in simulations

Table 1: Double pulse test circuit parameters

Parameter	Value	Parameter	Value
D_{CL}	5SHX 1445H	C_{DC}	2.6mF
C_{CL}	$8\mu F$	L_{LOAD}	5.4mH
R_{CL}	2Ω	IGCT	5SHX 1445H
L_{CL}	$9\mu H$	D_{FW}	5SDF 0545F
		L_{σ}	500nH

Table 2: Reverse conducting IGCT data

	IGCT	Reverse Diode
Manufacturer	ABB	ABB
Model	5SHX 1445H	5SHX 1445H
Forward blocking voltage	5500V	5500V
V_{DC}	3300V	-
I_{TGQM}	900A	-
I_{FAVM}	-	170A
Treshold Voltage	1.65V	2.53V
Slope Resistance	$2m\Omega$	$4.3m\Omega$

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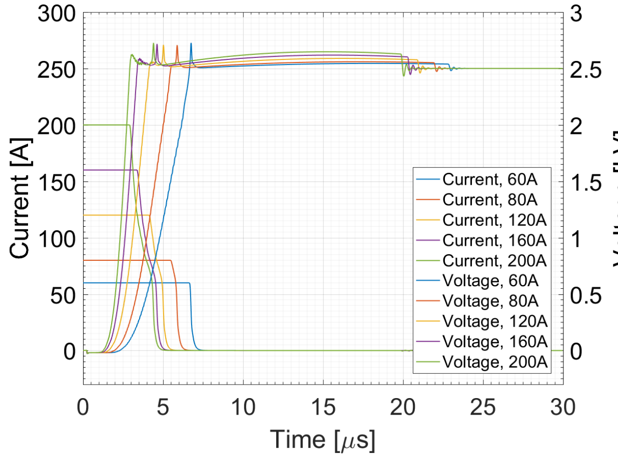

Fig. 2: IGCT turn-off current and voltage waveforms, 30°C.

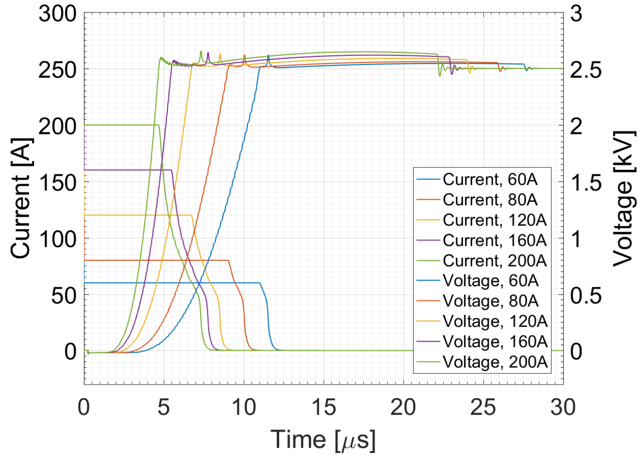

Fig. 4: IGCT turn-off current and voltage waveforms, 115°C.

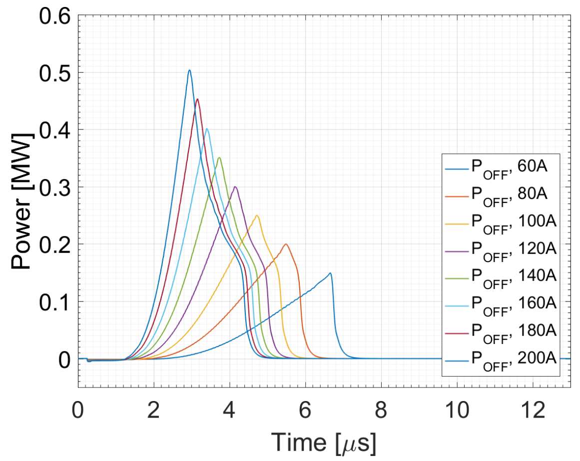

Fig. 3: IGCT turn-off power losses, 30°C.

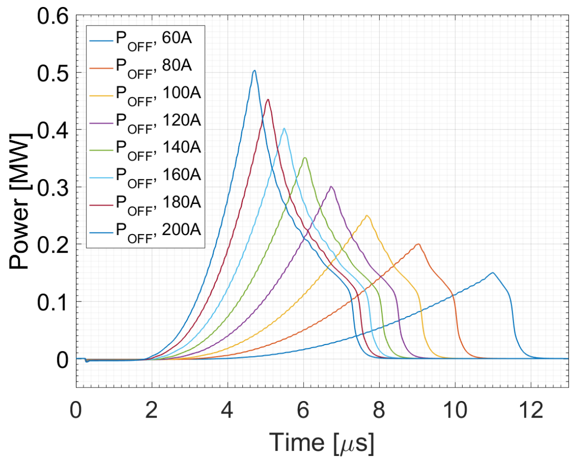

Fig. 5: IGCT turn-off energy losses, 115°C.

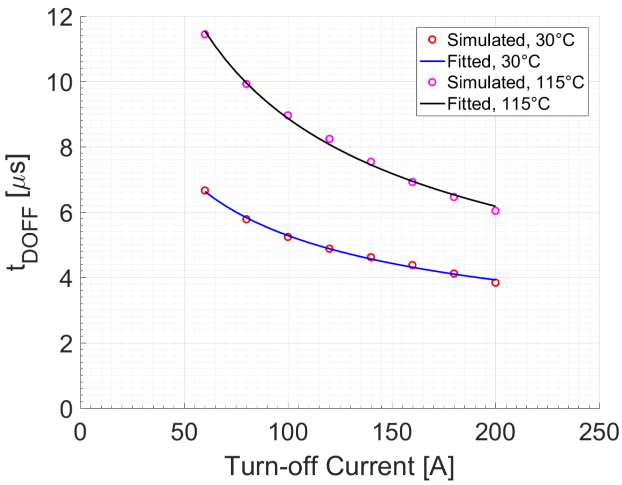

Fig. 6: t_{DOFF} estimated from the TCAD simulations.

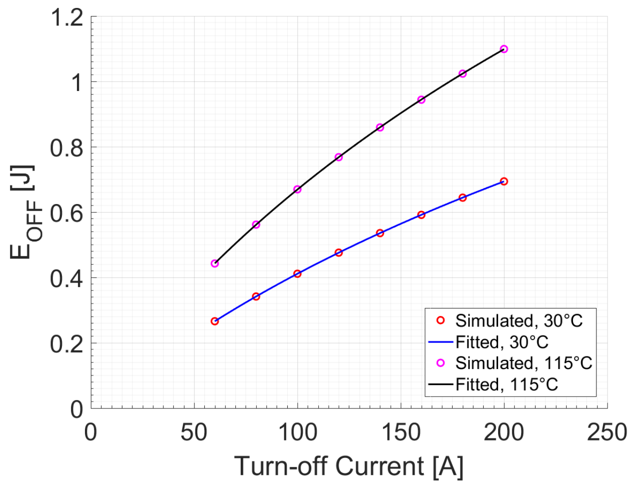

Fig. 7: IGCT turn-off energy losses.

while Fig. 7 shows the estimation of the energy lost during each of these switching events. Fitted curves are also given in the figure clearly showing the direct proportionality of the switching energy to the level of the turn-off current. Significant influence of the temperature is also observed. One of the design goals in the process of the DC-DC converter synthesis is to minimize the turn-off losses of the semiconductor devices and Fig. 7 suggests that this can be achieved by choosing low turn-off current value. Direct result of this requirement

Fig. 8: Multifunctional IGCT test setup.

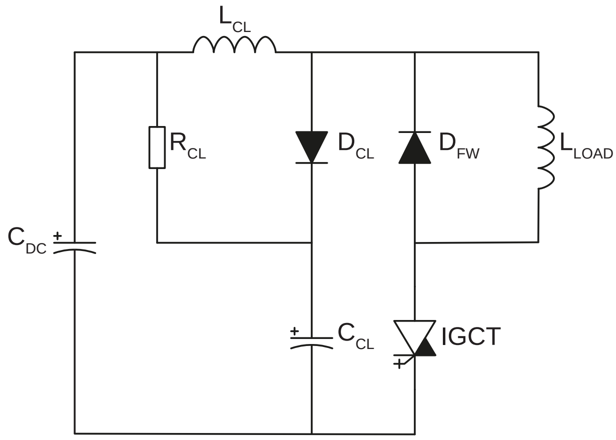

Fig. 9: Test setup configuration for double pulse test.

is prolonged t_{DOFF}; on the other hand, this parameter should not be allowed to be too long, so that reasonable dead time for the complementary switch could be defined (in order to avoid direct DC-link short circuit as well as ensuring continuation of the intended operation of the converter). At relatively low operation frequencies, this fact is of no significant concern but as the operational frequency increases, dead time (directly influenced by t_{DOFF}) presents itself as the limiting factor.

3. IGCT Test Setup

Test setup given in Fig. 8 has been designed and implemented for the purposes of verifying the simulation results and testing the IGCT switching devices under different working conditions (both hard-switching and resonant-switching). One of the functionalities of the setup is ability to run the industry standard double pulse test used for gaining detailed practical insight into the device's turn-on and turn-off behaviour, SOA conformity and switching energy losses. Typical electrical diagram of the circuit used for the double pulse test is presented in the Fig. 9 (one out of four possible modes of use of test setup) and the actual circuit parameters are given in the Table 1.

Circuit configuration for double-pulse test is fairly standard, with additional clamp circuit that limits the di/dt during the IGCT turn-on transient protecting the free-wheeling diode in the process. Added value of this kind of clamp circuit is that the significant part of the energy collected in the clamping inductor at the moment of turn-off is fed back to the DC-link through the clamping capacitor. This assembly allows for testing both turn-off and turn-on transients by applying one long on-pulse to the switch in order to build up the current to the desired level followed by two short off and on pulses. Hard turn-on of the IGCT is not of the interest in this paper, therefore it is neither presented nor discussed. Typical datasheet values of the reverse conducting IGCT used in the test setup are given in Table 2. Maximum DC operating voltage of the test setup is 5000V, and is provided from the external power supply. All semiconductor devices are water cooled by dedicated de-ionized water cooling unit. Various load inductances can be connected into the circuit, providing great flexibility during testing.

4. Experimental Results

Experiments were performed on the IGCT test setup to match conditions of the TCAD simulation for the comparison (2500V DC-link, 30°C) and Fig. 10 shows current and voltage waveforms of interest. Heating elements were not installed in the test setup and the experiment was not performed at the semiconductor temperature of 115 °C. Waveforms are aligned so that the electrical turn-off command (not shown on Fig. 10) happens at 0.1 μs as in the TCAD simulations. Faster turn-off transients are noticed when compared to the Fig. 2 and the behaviour is described by turn-off delay time t_{DOFF} (as defined previously) presented in the Fig. 12. Higher turn-off current causes shorter t_{DOFF} as predicted by the TCAD simulations with generally lower values obtained from the test data compared to the simulations.

Turn-off power loss waveforms are given in the Fig. 11 while Fig.13 shows the estimated turn-off energy lost during the transition period. Trend of rising turn-off

ISBN 978-3-8007-4646-0

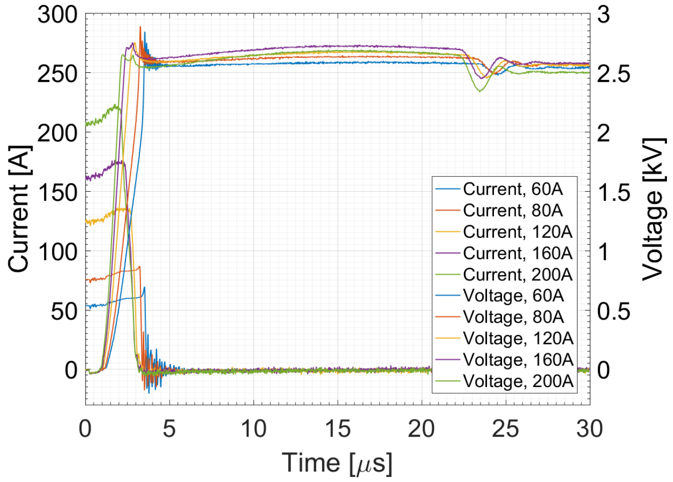

Fig. 10: IGCT turn-off current and voltage waveforms, 30°C.

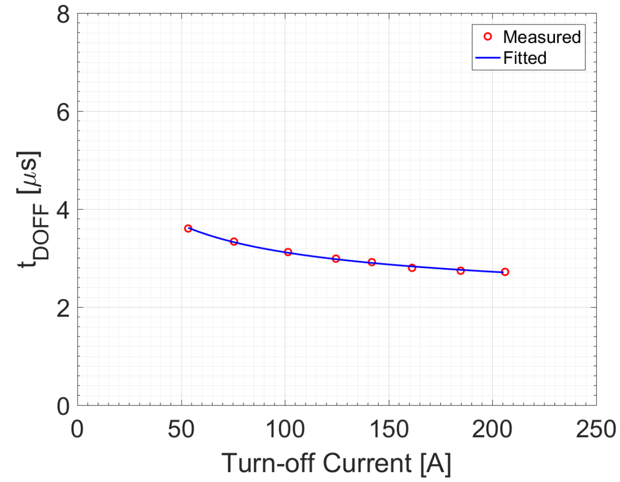

Fig. 12: t_{DOFF} estimated from the experiment.

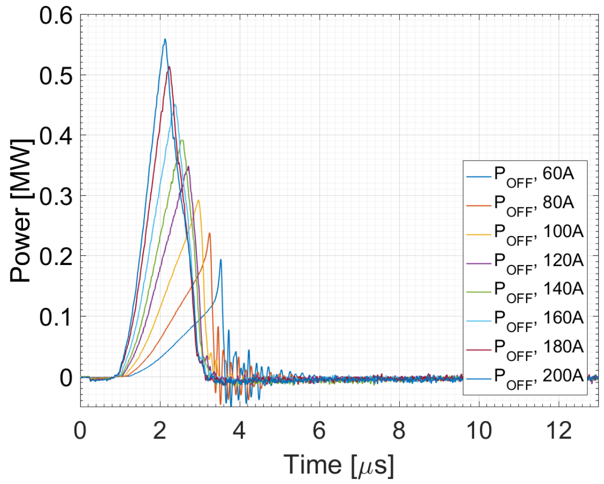

Fig. 11: IGCT turn-off power losses.

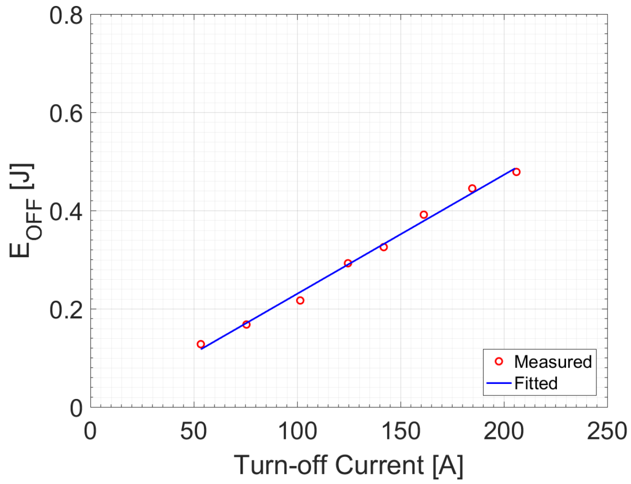

Fig. 13: IGCT turn-off energy losses, 30°C.

energy losses with increasing turn-off current is evident here as well and the difference with the TCAD obtained values is attributed to the shorter turn-off periods of a device under test. Thus, the trade-off between turn-off duration under low switching current and decrease of switching energy loss needs to be carefully considered during application of IGCT under these conditions.

5. Conclusion

The prospect of low overall energy losses of the IGCT opens the opportunity of increasing its switching frequency allowing for the decrease in volume of the surrounding passive components of the high power DC-DC converters. TCAD simulation results and experiments performed on the dedicated test setup show that low turn-off currents affect the duration of turn-off process prolonging it as the turn-off current decreases (Fig. 6 and Fig. 12). At the same time, turn-off energy losses decrease with the decreasing turn-off current of the IGCT (Fig. 7 and Fig. 13). Conflicting requirements of the low turn-off losses and short turn-off delay times have to be optimized and parameters (I_{OFF} and dead time) carefully chosen for the particular converter design to guarantee efficient and safe operation of the converter during its lifetime. Worst case scenario curves for the t_{DOFF} and E_{OFF} are to be used in the design process while the typical ones should be employed when estimating the efficiency of the converter designs with the selected IGCT device. In collaboration with the manufacturer, technology curve of the IGCT of choice can be tailored to fulfill the requirements set forth by the designer.

Acknowledgment

The work presented in the paper is supported in part by the Swiss National Science Foundation under the project number 200021_165566 and in part by ABB Semiconductors, Lenzburg, Switzerland.

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