Galvanically Isolated Modular Converter

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"There's never enough time to do all the nothing you want"
B. Watterson

Abstract

The ever increasing penetration of renewable energy systems in the distribution grids will inevitably require profound changes in the grid infrastructure. One emerging direction, the medium voltage dc (MVdc) grids, is the cornerstone of this work. They are foreseen for offshore wind parks and onshore large scale renewables collection grids, future on-board ship power systems, repurposed ac lines with increased transport capacity, etc. The shift to dc offers energy savings and reduced impact on the landscape. This thesis provides insights on the presumed most suitable conversion topology between a MVdc and a LVac grid, which is not expected to disappear in the near future. The conversion is characterized by a large voltage ratio between the two terminals. A modular multilevel converter (MMC) with an integrated magnetic component, the galvanically isolated modular converter (GIMC), is proposed and preferred for efficiency and cost reasons over a solid-state transformer, whose efficiency is heavily penalized by the inverter stage on the low voltage side.

The thesis opens on a detailed benchmark of the performances of various control, modulation and branch balancing methods, with a focus on medium voltage applications. Extensive simulations are carried out to support the discussion. In case of an application with fast dynamics, the closed-loop control method, comprising energy balancing controllers, offers by far the best performances. For the modulation and branch balancing methods, it was concluded that, as long as both the number of cells per branch and average cell switching frequency are not very low, PWM methods based on the reference branch voltage, rather than the number of inserted cells per branch, feature lower voltage errors.

From there, the two GIMC variants sharing the same three-windings transformer, the interleaved GIMC and stacked GIMC, are analyzed. This solution does not suffer from dc bias in the magnetic device, unlike the open-end windings MMC. Since the obtained model is identical to the one for the conventional dc/3-ac MMC, the same control algorithms can be applied without restriction. The volume and efficiency comparison against the conventional case with discrete air-core inductors, supported by FEM simulations, quantifies the benefits of the proposal. It is concluded that the gains are marginal for the considered modest power ratings (0.5 MVA). However, the magnetic design is considerably simplified. Larger gains are expected for designs with higher branch inductance values, since the stacking of the primary windings gives easy access to high leakage inductances.

A generic and versatile losses estimation method for modular converters is introduced. Compared to detailed switched simulations, the simulation times are improved by two orders of magnitude, if the assumptions to neglect the branch current ripple and branch capacitor voltage spread hold. The estimation error is below 2 % in the considered comparison.

At last, the design of a 0.5 MVA converter prototype connected to 10 kV_{dc} with 96 cells is presented. The cell, with a dedicated Flyback-based auxiliary cell power supply from its dc-link and protection circuits for a cell bypass in case of over-current or -voltage, along with the electric design of the cabinet hosting one converter phase-leg, are verified experimentally. The cell and phase-leg layout provide a platform for further research activities.

Keywords modular multilevel converter, medium voltage dc grid, power electronics, control, modulation, finite element modeling

Résumé

La pénétration toujours plus importante des énergies renouvelables dans les réseaux de distribution requiert de profonds changements dans leur infrastructure. Les réseaux continus moyenne tension (MVdc), au fondement de ce travail, en sont un exemple. Ils sont envisagés pour le raccordement de parcs éoliens en mer ou d'énergies renouvelables à grande échelle, la distribution électrique à bord des navires, la conversion de lignes alternatives pour en augmenter la capacité, etc. La transition vers le continu permet des économies d'énergie et une réduction de l'impact sur le paysage. Cette thèse étudie la structure de conversion la plus à même entre un réseau MVdc et un réseau ac basse tension, dont la disparition n'est pas envisagée dans un futur proche. La conversion se distingue par un grand rapport de tension entre les deux terminaux. Un convertisseur modulaire multiniveaux (MMC) avec un élément magnétique intégré, nommé convertisseur modulaire à isolation galvanique (GIMC), est introduit et préféré à un convertisseur avec étage intermédaire moyenne fréquence pour des raisons de rendement et de coûts, l'onduleur du côté basse tension pénalisant fortement son rendement.

La thèse débute par une comparaison détaillée des performances des techniques de contrôle, de modulation et d'équilibrage pour des applications moyenne tension. De nombreuses simulations sont effectuées pour étayer l'argumentaire. La méthode qui comprend le contrôle en boucle fermée de l'équilibrage des énergies internes offre de loin les meilleures performances. De fait, elle est particulièrement adaptée aux applications hautement dynamiques. En ce qui concerne les méthodes de modulation et d'équilibrage, pour autant que le nombre de cellules par branche et la fréquence moyenne de commutation par cellule ne soient pas trop bas, les modulations PWM avec référence de tension, plutôt que nombre de cellules insérées, présentent les plus faibles écarts de tension.

De là, deux variantes du GIMC, entrelacée et superposée, qui partagent le même transformateur à trois enroulements sont analysées. Au contraire du MMC à enroulements ouverts, la solution proposée ne souffre pas de composante continue dans le matériau magnétique. Puisque les modèles obtenus sont identiques avec celui d'un MMC conventionnel, les mêmes approches de contrôle peuvent être appliquées sans limitation. La comparaison du volume et du rendement de l'élément magnétique intégré avec le MMC conventionnel et ses inductances à l'air est réalisée avec l'appui de simulations par éléments finis. Les gains obtenus sont marginaux pour le niveau de puissance considéré (0.5 MVA). Cependant, la conception du composant magnétique est considérablement simplifiée. Des gains supérieurs sont attendus pour des systèmes avec une plus grande inductance de branche, puisque de grandes inductances de fuite sont aisément atteignables via l'empilement des enroulements primaires.

Une méthode générique et flexible d'estimation des pertes pour convertisseurs modulaires est proposée. Les temps de simulation comparés à un modèle détaillé sont réduits d'un facteur supérieur à cent, à condition que les hypothèses de négliger l'ondulation du courant de branche et la dispersion des tensions des condensateurs restent raisonnables. Dans les comparaisons, la différence est inférieure à 2 %.

Finalement, la conception d'un démonstrateur de 0.5 MVA connecté à un bus 10 kV_{dc} avec 96 cellules est présentée. La cellule, avec son alimentation Flyback et les circuits de protection pour la court-circuiter en cas de surcourant ou surtension, de même que la conception électrique d'une armoire contenant une phase du convertisseur, sont vérifiées expérimentalement. Cet ensemble consitue une plateforme pour de futures recherches.

Mots-clés convertisseur modulaire multiniveaux, réseau continu moyenne tension, électronique de puissance, contrôle, modulation, simulation par éléments finis

Acknowledgments

"In nature, nothing exists alone"
R. Carson

Unsurprisingly, this thesis is no exception. I'd like to take the time to thank all the people who have directly or indirectly contributed to this work or to the well-being of its author.

Four years ago, I was given the opportunity to start a PhD in the newly created Power Electronics Laboratory (PEL), under the direction of Prof. Dražen Dujić. What a journey it has been! Prof. Dražen Dujić provided valuable advice and steady support to my research. I was given a lot of freedom regarding the orientation to give to my work, which I considered as a benefit of joining a lab in ramp-up phase. This allowed me to explore and broaden the spectrum of my views on the power electronics field, but not only.

I'm grateful to the members of the jury, Prof. Mario Paolone from the DESL at EPFL, Prof. Alfred Rufer from EPFL, Prof. Marc Hiller from the Electrotechnical Institute at KIT and Dr. Tobias Geyer from ABB Corporate Research Center in Baden-Dättwil, for accepting to evaluate this work.

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I'd like to express my sincere gratitude to Prof. Alfred Rufer, Dr. now Prof. Philippe Barrade and the assistants of the former LEI, who all completed their PhDs in the meantime. You passed me the virus for power electronics during my undergraduate studies, and you had a very positive impact on my young scientific mind.

I was pleased to be allowed to spend 5 months in industry at ABB, in the Power Grids division in the Grid Integration R&D team in Turgi, Switzerland. I would like to thank Lukas Ramming, Dr. Jürgen Steinke and Prof. Dražen Dujić to make this happen. I'd like to thank all the members from the R&D team for their warm welcome, in particular Dr. Michail Vasiladiotis, with whom I had close interactions. It was a precious experience.

I'm thankful to Pedro and Miodrag for the meticulous proofreading of this thesis.

Thanks to all the people who worked shortly on the MMC prototype at my side: Emilien Coulinge, Nikolas Zbären, Julien Gasser, Julien Orsinger, Mathieu Grossenbacher, Marko P. and Didier Ansermet. Karim Collomb from the workshop desserves a special note for the assembly of the drawers and enclosures inside the MMC cabinets. Now, Stefan, Miodrag and Milan, the floor is yours to finalize the MMC platform and get it up and running!

Thanks also to the whole PEL crowd in everlasting growth since I joined. We had nice discussions during the breaks, conference travels and lab events far from the campus. I wish the spirit from the early days of PEL would persist.

Pour finir, merci à ma famille, ce petit noyau de personnes si importantes. Vous avez enduré mes hauts et bas, sans trop vous plaindre. Voici venu le temps pour moi de finir mes études et d'explorer de nouveaux horizons. Enfin, certains diront…

Lausanne, March 2018

List of Abbreviations

ac	alternate current
ACPS	auxiliary cell power supply
ANPC	active neutral point clamped (NPC)
APOD-PWM	alternative phase opposition disposition PWM
BESS	battery energy storage system
CCC	circulating current control
CCSC	circulating current suppression controller
CHB	cascaded H-bridge
CM	common mode
CTI	comparative tracking index
DAB	dual active bridge
DAB3	three-phase DAB
dc	direct current
dc/3-ac	direct to three-phase
DCM	discontinuous conduction mode
DDSRF	double decoupled synchronous reference frame
DFIG	doubly-fed induction generator
DSOGI	double second-order generalized integrator
DVC	direct voltage control
eRSA	enhanced RSA
ESR	equivalent series resistance
FACTS	flexible ac transmission systems
FC	flying capacitor
FEM	finite element modeling
FFT	fast Fourier transform
FTB	flux tolerance-band
GD	gate driver

GIMC	galvanically isolated modular converter
HVdc	high voltage dc
iGIMC	interleaved GIMC
KVL	Kirchhoff's voltage law
LCC	line-commutated converter
LDO	low-dropout
LFT	line frequency transformer
LS-PWM	level-shifted PWM
LUT	look-up table
LVac	low voltage ac
LVdc	low voltage dc
MAF	moving average filter
MFT	medium frequency transformer
MMC	modular multilevel converter
MV	medium voltage
MVac	medium voltage ac
MVdc	medium voltage dc
NLM	nearest level modulation
NPC	neutral point clamped
NPP	neutral point piloted
OEW	open-end windings
OPP	optimized pulse pattern
OVC	over-voltage category
PCB	printed circuit board
PCC	point of common coupling
PD	partial discharge

PD-PWM	phase-disposition PWM
PEBB	power electronics building block
PHSP	pumped-hydro storage plant
PI	proportional integral
PLL	phase-locked loop
PoD	pollution degree
POD-PWM	phase opposition disposition PWM
PR	proportional resonant
PS-PWM	phase-shifted PWM
PWM	pulse-width modulation
RES	renewable energy sources
RSA	restricted sorting algorithm
SCR	short-circuit ratio
SFC	static frequency converter
sGIMC	stacked GIMC
SHE	selective harmonic elimination
SOA	safe operating area
SOGI	second-order generalized integrator
SST	solid-state transformer
STATCOM	static synchronous compensator
SVM	space-vector modulation
TVS	transient-voltage-suppression
UVLO	undervoltage lockout
VSC	voltage-source converter
VSM	virtual submodule

List of Symbols

C_{br}	Branch capacitance
C_{cell}	Cell capacitance
I_{dc}	Dc current
L_{μ}	Magnetizing inductance
L_{σ}	Leakage inductance
L_{br}	Branch inductance
L_{p}	Self inductance
M_{br}	Branch mutual inductance
N_{cells}	Number of cells per branch
N_{lvl}	Number of levels in the phase switching pattern
P	Active power
Q	Reactive power
R_{br}	Branch resistance
R_{esr}	Equivalent series resistance
S	Apparent power
V_{B}	Dc bus voltage
V_{dc}	Dc voltage
W_{0}	Initial branch energy
ΔW_{br}	Branch energy variation
$\Delta\psi$	Volt-second ripple
$\hat{.}$	Peak value
ω	Fundamental grid angular frequency
ϕ	Load angle
$\|\|.\|\|$	ℓ^2-norm
abc	Ac grid phase number
e_{B}	Summed phase-leg emf voltage
e_{L}	Differential phase-leg emf voltage
e_{p}, e_{n}	Branch emf voltages
$f_{\mathrm{sw,app}}$	Apparent switching frequency
f_{sw}	Switching frequency
f_{g}	Fundamental grid frequency
i_{B}	Dc bus current

i_μ	Transformer's magnetizing current
i_{circ}	Circulating current
i_g	Grid current
i_p, i_n	Branch currents
k_{ac}	Ac grid voltage over dc voltage ratio
m_p, m_n	Branch modulation indices
n_{dc}, n_{ac}	Equivalent numbers of inserted cells seen from the dc and ac terminals
n_p, n_n	Numbers of inserted cells per branch
p_Δ	Differential phase-leg power
p_Σ	Summed phase-leg power
p_p, p_n	Branch powers
v_L	Ac phase voltage
v_{CM}	Common mode voltage
v_g	Ac grid voltage
$v_{C\Sigma p}$, $v_{C\Sigma n}$	Summed branch capacitor voltages
$v_{C\Sigma}^{\Delta}$	Differential phase-leg capacitor voltage
$v_{C\Sigma}^{\Sigma}$	Summed phase-leg capacitor voltage

Contents

1 Introduction

1.1 Background and motivation

1.1.1 Swiss energy landscape

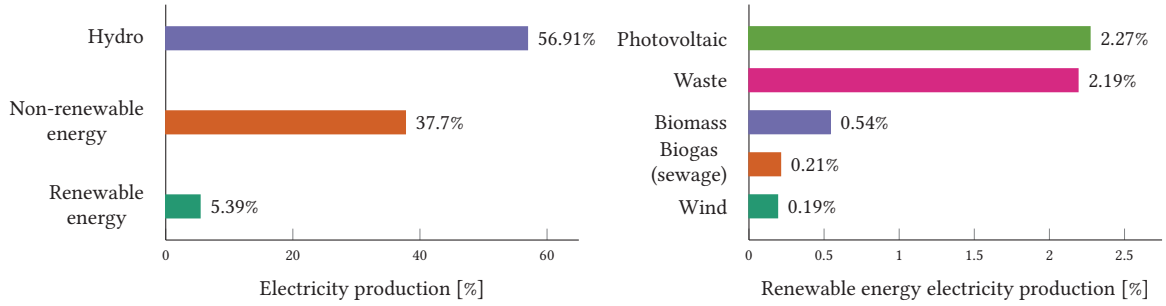
Switzerland has engaged an energy turnaround process, with a complete nuclear phase out by 2050. This process is elaborated in the *Energy Strategy 2050* [1], which is providing the legal framework supporting the transition as well as a planning of the resources / needs with incremental objectives. In the following, the discussion will restrain on the electrical energy, even though the strategy considers all forms of energy.

In 2016, the annual swiss electricity consumption was just below 60 TWh [2]. The actual share of nuclear power (~ 40 %) is expected to be replaced with renewable energy sources (RES)[1], assuming no increase in the electrical energy consumption, thanks to increased efficiency enabled by technological advances. This last statement, however, might be compromised if a large shift towards e-mobility happens in parallel. Since the hydro power potential for new large-scale installations or extensions of existing ones is limited [3], this implies an increase by a factor 10 of the share of renewables. The current energy split is presented in **Tab. 1.1** and illustrated in **Fig. 1.1**.

Tab. 1.1 Electricity production in Switzerland in 2016. Data from [2].

Source	**Production** [TWh]	**Share** [%]
Hydro	33.40	56.91
Non-renewable energy	22.13	37.70
Photovoltaic	1.33	2.27
Waste	1.26	2.15
Biomass	0.34	0.57
Biogas (sewage)	0.12	0.21
Wind	0.11	0.19
Total	58.69	100

[1] Such as wind, photovoltaic, etc. Hydro is counted separately.



(a) (b)

Fig. 1.1 Electricity production in Switzerland in 2016. Data from [2].

1.1.2 Swiss electrical grid infrastructure

Comprising 6700 km of transmission lines (220 or 380 kV, 50 Hz), the swiss grid infrastructure is aging: two-thirds of today's grid was built around the 1960s. In addition, newly built or upgraded large-scale pumped-hydro storage plants (PHSPs) (cf. **Tab. 1.2**) were recently commissioned, are approaching commissioning or are still waiting for project approval, totalizing investments of CHF 6 billions. Consequently, new infrastructures are required to handle non-planned power flows and avoid line congestions at the transmission level [4].

Tab. 1.2 Large PHSPs (> 100 MW) in Switzerland. Data from [5].

Plant	**Installed power** [MW]	**Commissioning** (last)
Limmern	1000	2017
Lago Bianco	1000	under regulatory review
Nant de Drance	900	2019
Grimsel 3	660	under regulatory review
Hongrin-Léman	437	2016
Grimsel 2	347	2013
Robiei	140	2016
Mapragg	159	1977
Tierfehd (Umwälzwerk)	140	2010

The situation is slightly different for the distribution grid, which is experiencing tremendous changes. The traditional power flow, from transmission to distribution transformers to the end users, is about to definitively belong to the past due to the increased penetration of renewables. There is a need for new regulations and standards to coordinate the functions and ancillary services provided by the power electronics interfaces that enable the penetration of renewable energy sources. From a grid operator point of view, a better knowledge of the distribution grid is required, since the behavior from a pure load to a mix of loads and sources is definitively happening, with an even accelerating pace, pushing the present way of operation to its limit.

However, this is not considering future strategic expansions. To fulfill the objectives of the Energy Strategy 2050, profound changes beyond smart metering are needed in the electrical grid. Some large-scale distributed energy resources will have to be deployed. Due to limited space, large-scale

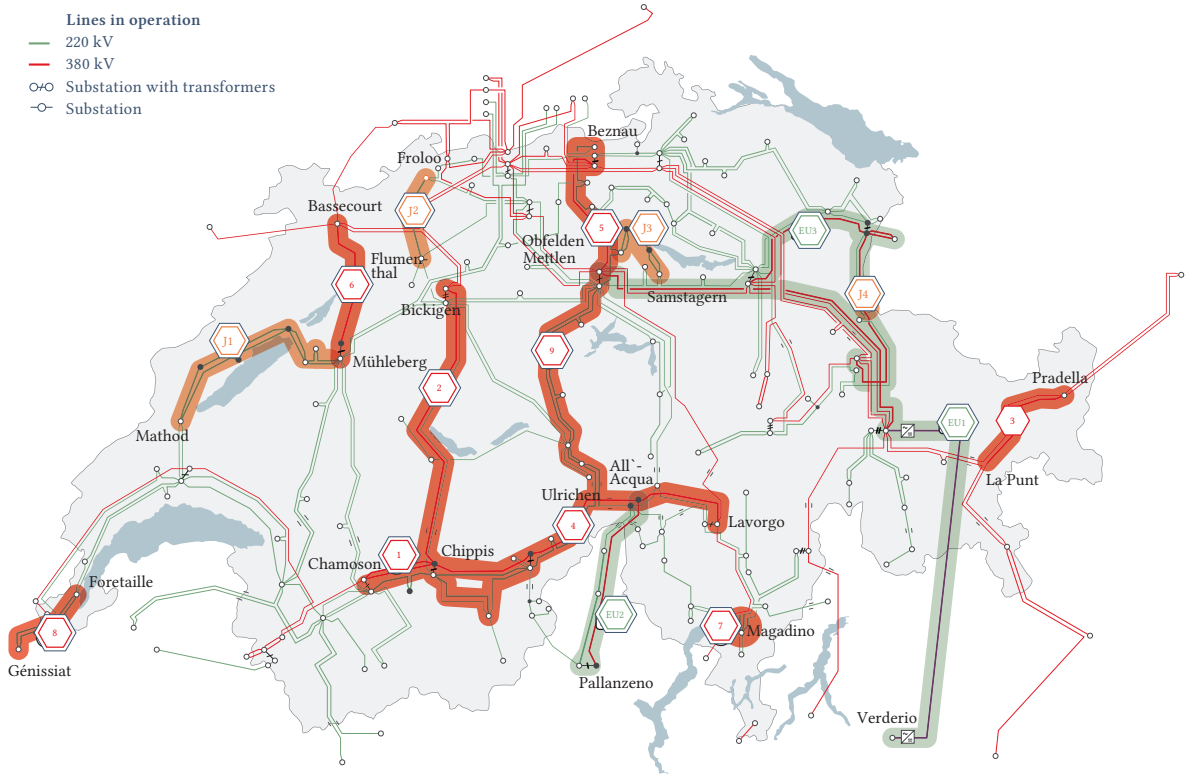


Fig. 1.2 SwissGrid expansion prospects (adapted from [4]).

installations might be limited to a few tens of MW in Switzerland. Consequently, they're expected to be connected to the medium voltage grid. Aware of the low public acceptance and lengthy authorization process for overhead alternate current (ac) lines, due to their large impact on the landscape and the existing built environment, medium voltage dc (MVdc) transmission with underground cables might present a feasible alternative.

1.1.3 Future prospects

Nowadays, there is a noticeable push towards direct current (dc) systems: datacenters are equipped with low voltage dc (LVdc) distribution, 1500 V_{dc} is the new standard for large-scale PV plants [6]–[8], LVdc ships are already on the market [9]. Among various dc technologies, both the academia and the industry have an increasing interest towards MVdc [10], where its use is foreseen for renewable energy collection grids, next generation marine distribution system, etc. In all cases, the justification for the move to dc is an efficiency increase, with potential system simplifications. However, some elements, such as the dc breaker [11], are still missing, slowing down the expansion of MVdc. From a research perspective, this field offers many opportunities, from system stability [12] to new components design/use, including the development of new converter topologies.

The three different dc line configurations are shown in **Fig. 1.3**. In the symmetric monopolar case, the two dc conductors are isolated for half the dc voltage, with or without grounding on the dc side. In the asymmetric monopolar dc link, a single conductor requires isolation for the full dc voltage. The solution with ground return is cheaper, but requires a special authorization. The main advantage

of an asymmetric monopolar dc link is that it can be easily upgraded to a bipolar configuration. The last configuration, the bipolar dc link, allows for reduced operation as an asymmetric monopolar dc link in case of defect or maintenance in one converter station, assuming that the dc current can return through the ground path. Note that for both asymmetric monopolar and bipolar dc links the transformers has to be designed for the dc stress between the primary and the secondary, as one dc terminal end and not its midpoint is grounded.

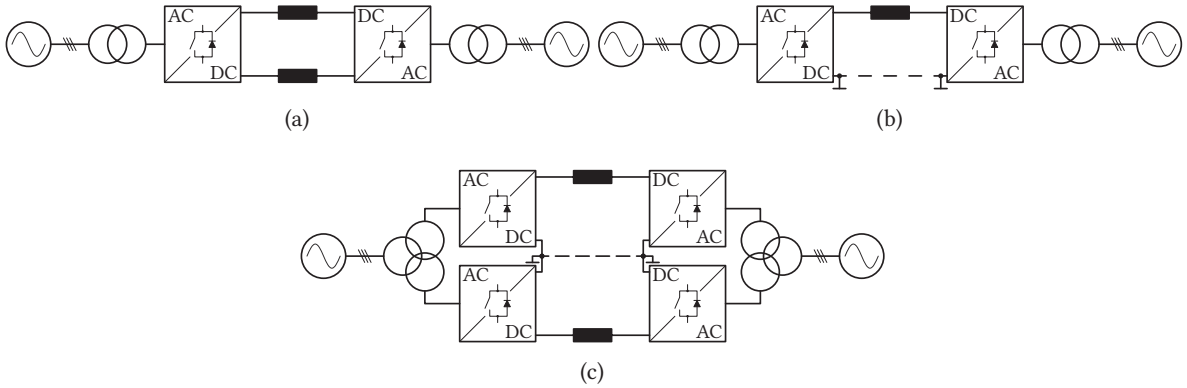


Fig. 1.3 Dc line configurations: (a) symmetric monopolar, (b) asymmetric monopolar and (c) bipolar. For the last two, either ground or metallic return are considered, depending on whether a dc ground current is allowed or not.

1.2 Scope and main contributions of the thesis

This work focuses on the interconnection of a MVdc grid or line with an existing low voltage ac (LVac) grid, which could represent a microgrid or a group of hotel loads, as shown in **Fig. 1.4**. A symmetric monopolar dc line is considered. The conversion is characterized by a large voltage ratio ($\geq$ 10) between the two grids. Since no MVdc voltage levels are defined by standards or common agreement by the industry, the solution has to be able to stretch in a range from 5 kV up to ($\pm$) 50 kV. Also, galvanic isolation is desired for safety purpose. Since it is a grid-connected application, the high efficiency target dominates the power density and converter footprint, as opposed to an on-board application, where volume/weight targets dominate.

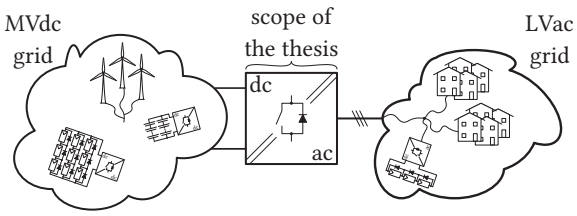


Fig. 1.4 Scope of the thesis: interconnection of a MVdc grid with a LVac grid (radial structure).

The main contributions of the thesis are:

1. A careful assessment on the control method for a direct to three-phase (dc/3-ac) modular multilevel converter (MMC) for medium voltage applications supported by extensive simulations

on a common scenario. With six key metrics, critical conclusions are drawn regarding the best suited control method for this voltage range.

2. A critical comparison of the modulation and branch balancing methods for a dc/3-ac MMC with voltage error minimization.

3. Two converter topologies presented in the literature and using the same integrated magnetic component that merges the discrete branch inductors and the line frequency transformer (LFT) without suffering from design constraints (namely a dc bias) nor operation limitations (free common mode (CM) and harmonic circulating current injection) are unified under the galvanically isolated modular converter (GIMC) designation. The benefits originating from this integration are evaluated in terms of volume and efficiency.

4. The introduction of a very fast (over two orders of magnitude faster than a detailed switched model simulation) cell loss estimation method for modular converters, which is flexible regarding the cell type, CM voltage injection method and harmonic content of the circulating current, as long as two simplifying assumptions hold.

5. The design of a medium voltage MMC cell with a Flyback-based auxiliary cell power supply (ACPS) using a planar transformer with printed circuit board (PCB) integrated windings, bypass functions for preserving the integrity of the cell in case of component failure or unexpected conditions (over-current or -voltage), and proper electrical design of the phase-leg cabinets.

1.3 Structure of the thesis

The thesis is organized as follows.

Chapter 2 presents an overview of the state-of-the-art converter topologies in the medium and high voltage ranges. The general trend shows a noticeable shift towards highly modular conversion structures. Building on this observation, and considering the selected application in this work, the best candidate is selected: a dc/3-ac MMC with (conventional) or without (the GIMC proposal) discrete branch inductors.

Chapter 3 presents the modeling of the dc/3-ac MMC. As a result, thanks to the introduction of two linear mappings, a model that decouples the dc from the ac terminals is derived. The modeling part streamlines the two subsequent chapters focusing on the control and modulation of an MMC. The branch power equations provide appreciable insights on the low-order harmonic content of the branch quantities (branch current, summed capacitor voltages, modulation indices, ...) and support the optimization of the harmonic circulating current injection, the converter energy requirements and the converter safe operating area (SOA).

Chapter 4 provides a thorough assessment of the control performances from methods proposed in the literature, with a specific focus on medium voltage applications, that greatly differ from high voltage dc (HVdc) in terms of converter sizing, voltage resolution and desired dynamics. An extensive set of time domain simulations is carried out on an average model based on the ratings of the converter prototype. Each control method is evaluated along six key performance indicators and it is concluded that the closed-loop control method offers the best performances among them.

Chapter 5 performs a systematic and critical review of the modulation and branch balancing methods for the dc/3-ac MMC. Several implementation details and pecularities are discussed. The best performing pulse-width modulation (PWM) methods, phase-disposition PWM (PD-PWM) with enhanced RSA (eRSA) for the $N_{\text{cells}} + 1$ modulation, and phase-shifted PWM (PS-PWM) with local proportional controllers for balancing for the $2N_{\text{cells}} + 1$ modulation, are advised, since they feature the lowest voltage errors.

Chapter 6 critically analyzes the proposals where the LFT has been integrated within the MMC phase-legs. In order to overcome the highlighted drawbacks of these topologies, the need for a three-windings transformer is outlined. The modeling of the topology based on such a transformer, the GIMC, through its two variants: (i) the stacked GIMC (sGIMC) and (ii) the interleaved GIMC (iGIMC), shows no difference compared to the MMC modeling. Consequently, the same control algorithms are applied to the GIMC without restriction.

Chapter 7 quantifies the benefits of the GIMC three-windings transformer with integrated branch inductors compared to the conventional dc/3-ac MMC with discrete branch inductors, with a focus on the volume and efficiency of the magnetic components. The integration of the branch inductors offers interesting volume reduction and efficiency increase by saving 500 W of losses for a 0.5 MVA converter, which corresponds to an efficiency increase of 0.1 %.

Chapter 8 introduces a generic cell losses estimation method, the virtual submodule (VSM) method, for modular converters, characterized by a two orders of magnitude computation time improvement compared to detailed switched model simulations. Unlike conventional converter topologies, the need for a loss evaluation in closed-loop is motivated by the possibility to shape/need to control the harmonic content of the circulating current. As long as the two assumptions hold, (i) a negligible branch current ripple and (ii) a negligible branch capacitor voltage spread, the estimation error compared to detailed switched models remained below 2 %.

Chapter 9 summarizes the development around the MMC cell design and the medium voltage prototype, from cell concept through a Flyback-based ACPS and phase-leg cabinet layout, which compliance with the IEC 61800-5 standard was verified with ac dielectric withstand tests.

Chapter 10 concludes the work and outlines future research perspective in the area.

1.4 List of publications

Conference papers:

C1. A. Christe and D. Dujić, "State-space modeling of modular multilevel converters including line frequency transformer," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sep. 2015, pp. 1–10

C2. A. Christe and D. Dujić, "On the integration of low frequency transformer into modular multilevel converter," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2015, pp. 3585–3592

C3. E. Coulinge, A. Christe, and D. Dujic, "Electro-thermal design of a modular multilevel converter prototype," in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics,*

Intelligent Motion, Renewable Energy and Energy Management, May 2016, pp. 1–8

C4. A. Christe, E. Coulinge, and D. Dujic, "Insulation coordination for a modular multilevel converter prototype," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sep. 2016, pp. 1–9

C5. A. Christe and D. Dujic, "Virtual submodule concept applied to the modular multilevel converter," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2017, pp. 1–8

C6. A. Christe and D. Dujic, "Novel insight into the output current ripple for multilevel and multiphase converter topologies," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jul. 2017, pp. 1–8

Journal papers:

J1. A. Christe and D. Dujic, "Galvanically isolated modular converter," *IET Power Electronics*, vol. 9, no. 12, pp. 2318–2328, 2016

J2. A. Christe and D. Dujic, "Virtual submodule concept for fast semi-numerical modular multilevel converter loss estimation," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5286–5294, Jul. 2017

J3. A. Christe, M. Petkovic, and D. Dujic, "Flyback-based auxiliary cell power supply with multiple isolated outputs for a medium voltage modular multilevel converter," *IET Power Electronics (under review)*, 2018

J4. A. Christe and D. Dujic, "Modular multilevel converter control methods performance benchmark for medium voltage applications," *IEEE Transactions on Power Electronics (under review)*, 2018

Other publications, not directly related to the scope of the thesis:

O1. U. Javaid, A. Christe, F. D. Freijedo, *et al.*, "Interactions between bandwidth limited CPLs and MMC based MVDC supply," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2017, pp. 2679–2685

O2. M. Vasiladiotis, A. Christe, T. Geyer, *et al.*, "Decoupled modulation concept for three-to-single-phase direct ac/ac modular multilevel converters for railway interties," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Sep. 2017, P.1–P.9

O3. M. Vasiladiotis, A. Christe, and T. Geyer, "Model predictive pulse pattern control for modular multilevel converters," *IEEE Transactions on Industrial Electronics (under review)*, 2018

2
State-of-the-art

This chapter provides an overview of the converter topologies for medium and high voltage applications. The requirements for the considered MVdc application are presented, followed by the choice of the most suitable converter topology for dc/3-ac conversion with a large voltage ratio between the MVdc and LVac terminals.

2.1 Converter topologies overview

Multilevel converter topologies enabled and supported the continuous development of medium and high voltage applications over the last 40 years. They were initially developed for high power applications with limited semiconductor blocking voltages. Today, they are essential for numerous industrial and utility applications. Still, further technological developments are possible and needed to support the profound transformations of the electrical energy systems.

2.1.1 High voltage dc transmission

Dc is more efficient for the transport of electrical energy over long distances. It was already the case in the late 19^{th} century with the Thury systems [13], whose best demonstration was a dc link between Moutiers (CH) and Lyon (FR): a capacity of 20 MW over 230 km at 125 kV_{dc}, operated between 1906 and 1936. However, simple and efficient conversion solutions were missing, since there were several limitations with series-connected dc machines. From an economic point of view, even though the base cost for a dc terminal is higher than an ac one, the lower transmission losses lead to a so-called break even distance, from where a dc transmission is a better choice (cf. **Fig. 2.1**). Depending on the technology and transmission type (overhead line, underground or subsea cable), different break even distances are obtained, typically around 50 km for subsea cables and 600 km for overhead lines. In addition, the line capacitance reduces the transmission power of very long overhead ac lines [14] and causes a large charging current for underground ac cables [15].

The HVdc applications saw the emergence of three different converter topologies over the last half century, branded under the names:

HVdc classic Mercury arc valve and then thyristor based line-commutated converters (LCCs) were used in the early days of HVdc (cf. **Fig. 2.2(a)**). They feature a dc current link and require large filters to operate, as well as a stiff ac grid. The first commercial installation was completed in 1954 in Gotland, Sweden [16]. Nowadays, LCCs dominate the high power and ultra high voltage range.

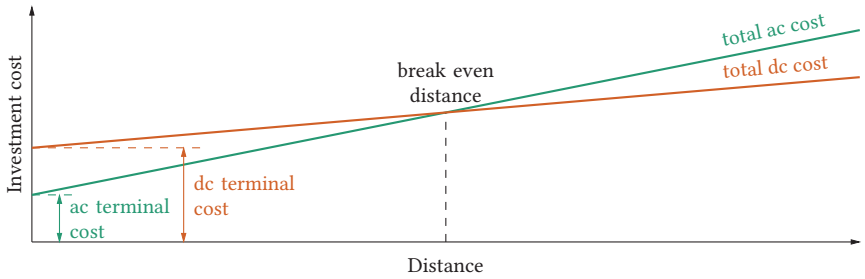


Fig. 2.1 Cost comparison between ac and dc transmission. The slope of the ac transmission is higher due to a higher loss factor compared to the dc transmission.

HVdc light As an improvement, two- or three-level voltage-source converters (VSCs) were introduced in the late 90s (cf. **Fig. 2.2(b)**) and are based on the IGBT technology. As opposed to LCC, they feature a dc voltage link, implying faster power reversal capability, since the dc lines doesn't have to be discharged, reactive power control capability and black start capability, which is needed for offshore applications. Smaller filters compared to LCC are used, quick power restoration after a blackout is possible, as well as weak ac grid connection. The series-connection of semiconductors constraints the maximum achievable switching frequency below 1 kHz. The first commercial installation was completed in 1999 in Gotland, Sweden [17].

HVdc plus The last improvement was introduced by Marquardt in 2002 with the MMC [18] (cf. **Fig. 2.2(c)**). Unlike previous solutions, MMC does not require series-connected semiconductor devices but series-connected cells. It enables both multilevel and high apparent switching frequency operations. As a consequence, filtering needs are partially, if not totally, removed. Harmonic filters, especially for high power applications, are very bulky when the cut-off frequency is low. Also, depending on the cell type, the fault blocking can directly be handled by the converter without a need for an external dc breaker. The first commercial installation was completed in 2010 in San Francisco, USA, with the Trans Bay Cable project [19].

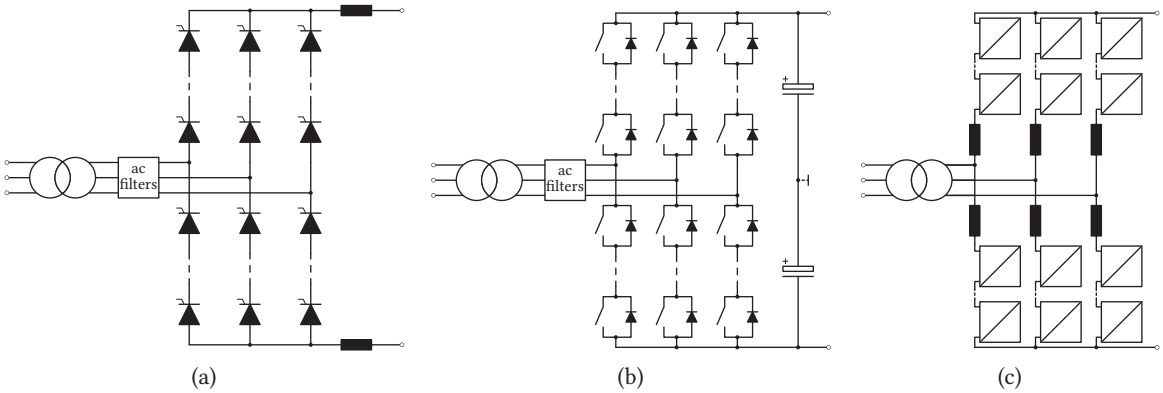


Fig. 2.2 HVdc technology evolution: (a) monopolar LCC, (b) two-level VSC and (c) MMC.

A comparison between the three HVdc technologies is presented in **Tab. 2.1**. Apart from the maximum ratings and losses, VSC and MMC show great similarities. It is also clear that LCC based HVdc will keep some market share, due to its unequaled efficiency and higher dc voltage, positioning it as the best solution for bulk power transmission over long distances.

Tab. 2.1 HVdc technologies comparison.

Property	LCC	VSC	MMC
Maximum dc voltage	±800 kV	±320 kV	±640 kV
Maximum converter rating	6.4 GW	2.4 GW	3.2 GW
Substation losses (at nominal power)	0.8 %	1.7 %	1 %
P control	Continuous	Continuous	Continuous
Q demand	50 % of the power transfer	0	0
Q control	Discrete or continuous	Continuous	Continuous

The high availability of HVdc links is supported by the possibility to continue the operation of a converter even with failed semiconductor(s) and/or cell(s) in a certain measure, depending on the redundancy concept applied. For a reliable operation with series-connected semiconductor devices, it has to be ensured that they fail in short-circuit state. This implies the use of press-pack semiconductor devices rather than modules. For both thyristors (light-triggered devices are normally used) and IGBTs, static (in OFF-state) and dynamic (during switching) voltage sharing have to be achieved (cf. **Fig. 2.3**). All these topologies are considered modular and scalable. For LCC and VSC, the number of stacks[1] can be varied to accommodate different dc link voltages. For MMC, this is done by varying the number of series-connected cells. For power scaling, semiconductor devices with various current capabilities (but if possible with same diameter for minimal implications on the mechanical design) are appropriately selected.

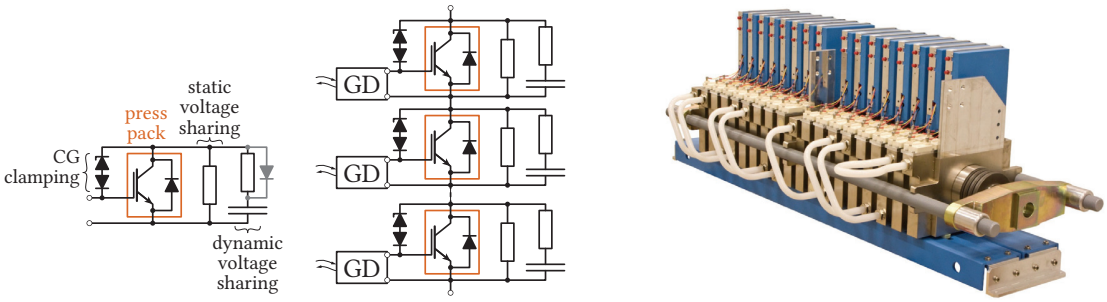


Fig. 2.3 Series-connected IGBTs with press-pack semiconductor devices [20]: (a) snubber circuits for static and dynamic voltage sharing, (b) IGBT stack and (c) ABB IGBT stack realization for MMC from [21].

HVdc enables the interconnection of asynchronous grids, and depending on the converter topology provides ancillary services, such as voltage control, power oscillation damping, and black start capability. With the increase of offshore wind farms projects, or need for large urban areas infeeds, HVdc projects are flourishing around the world, with an estimated compound annual growth rate (CAGR) of 8.8 % over the next decade [22].

[1] A stack is a mechanical arrangement comprising several series-connected semiconductor devices.

2.1.2 Medium voltage drives

Power electronics enabled variable speed operation of ac drives. The achievable performances with two-level converters are sufficient for low to medium power applications in the low voltage range with a high simplicity. When moving to larger powers and voltages, two major challenges are faced: (i) the limited switching frequency imposed by the semiconductor technology in combination with the blocking voltage class and (ii) the issue with large dv/dt at the motor terminals in case of series-connection of semiconductor devices (a dv/dt filter might not suffice to protect the machine windings).

Multilevel converter topologies emerged from the late seventies, e.g., neutral point piloted (NPP) [23], neutral point clamped (NPC) [24], [25], flying capacitor (FC) [26] or a combination of the last two [27], as a solution to the above mentioned problems. Some of these topologies are presented in **Fig. 2.4**. Regenerative braking is possible if an active front-end is selected instead of a diode rectifier[2]. By essence, these topologies are not modular beyond phase modularity and considered monolithic with limited scalability in terms of dc-link voltage (either by a change of semiconductor blocking voltage class or use of series-connected semiconductor devices, implying a complete redesign of the power electronics building block (PEBB)), while power scaling is obtained by paralleling units. Also, high voltage high power semiconductors ($\geq 3.3\,\mathrm{kV}$) are thermally constrained to a low switching frequency (mainly hard switching transitions), limiting the harmonic performance of these topologies.

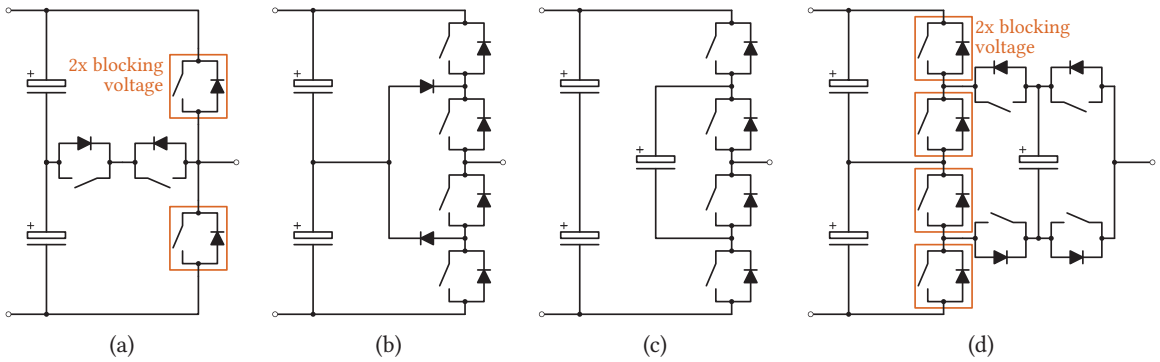


Fig. 2.4 Conventional industrial grade multilevel converters phase modules: (a) 3L NPP, (b) 3L NPC, (c) 3L FC and 5L active NPC (ANPC).

An improvement was introduced in [28] with the cascaded H-bridge (CHB) *Robicon* drive, where the multilevel output voltage is obtained by the series connection of H-bridge cells supplied by a multipulse transformer (cf. **Fig. 2.5(a)**). This drive is modular, since each cell is identical, scalable, since the number of series-connected cells is varied depending on the desired / required output voltage, and also fault tolerant (if included in the design), thanks to the neutral shift technique [29], [30]. The multipulse transformer, which is bulky and complex, due to the high number of secondaries, but fairly cheap, has however to be redesigned for each cell number configuration. Note that the windings configuration is similar to multipulse diode rectifiers and allow a grid friendly operation on the supply side [31]. Since then, CHB drives have been widely adopted by the industry (Siemens, Hitachi, Rockwell, WEG, ABB, etc.).

[2] Thyristor rectifiers are never used in these applications, since they do not offer significant advantages compared to diode rectifiers (slow dynamics and no need for a variable dc-link voltage).

Following the introduction of MMC, its use has also been extended to drives (cf. **Fig. 2.5(b)**), where the low speed range requires a special operating mode that injects a high frequency CM current, which is required to avoid an oversizing of the branch capacitor / large voltage ripples in the cell capacitor voltages [32]–[34]. The main advantage of an MMC drive over a CHB drive is that the complex multipulse transformer is replaced by a conventional 12/24/36-pulse transformer. For the moment, the market penetration of MMC in the drive area remains small.

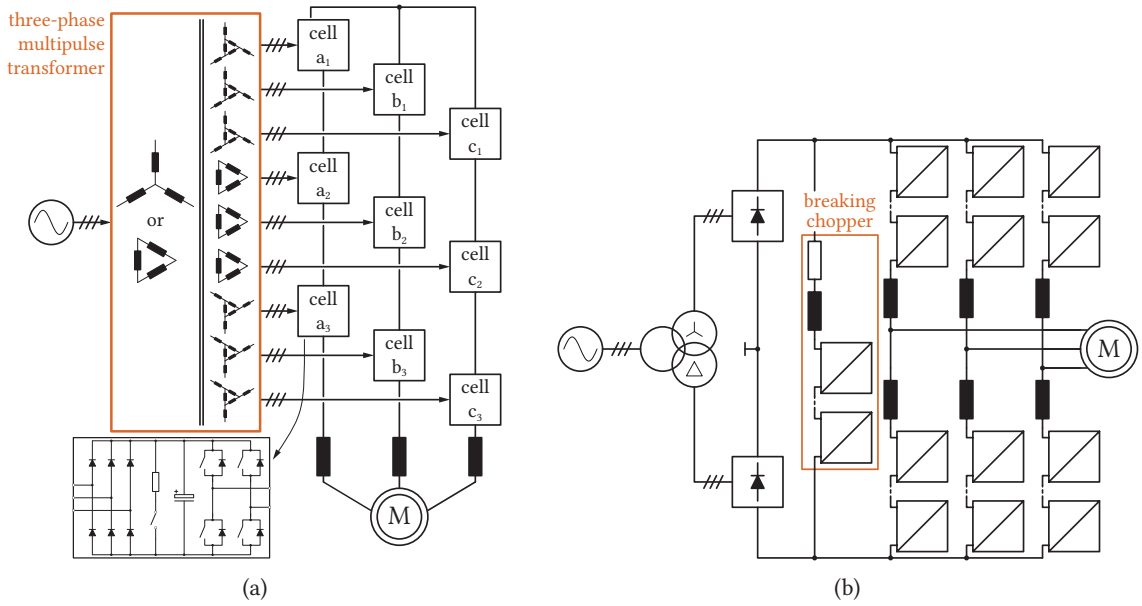


Fig. 2.5 Cascaded cells drives: (a) 9 cells CHB *Robicon* drive and (b) MMC drive with 12-pulse rectifier, both with unidirectional power flow (non-regenerative braking, with breaking chopper in each cell and central breaking chopper, respectively). Note that regenerative braking is also possible, with bidirectional cells and active front end, respectively.

medium voltage (MV) drives cover a voltage range from 2.3 kV to 13.8 kV, powers from a few hundreds of kW to few dozens of MW (discarding LCI), as seen from **Tab. 2.2**. Their applications are found in the heavy industry (mining, oil and gas, metal, ...), process industry, marine propulsion, etc.

2.1.3 Solid-state transformers

The concept of solid-state transformer (SST) has emerged on the premise that the power density of converters can be increased when the frequency at which the conversion and galvanic isolation are performed is increased (between a few hundreds Hz to few tens of kHz, compared to 50 or 60 Hz). This statement is true, as long as isolation requirements don't become the dominant factor of the transformer design.

Depending on the application requirements (uni- or bi-directional power flow), the conversion chain might differ. Usually, the complete conversion chain comprises several stages, meaning that the least efficient conversion stage will strongly impact the overall efficiency, no matter how high the efficiencies of the other stages are. As an illustration, the conversion chain for a traction application is shown in **Fig. 2.6**. The so-called input-series output-parallel (ISOP) concept is used to benefit from a

Tab. 2.2 MV drives offerings by ABB, Siemens and GE.

	Topology	Model	Output voltage range [kV]		Power range [MVA]		Semiconductor technology
ABB	3L NPC	ACS1000	2.3	4.16	0.315	5	IGCT
		ACS6000	2.3	3.3	5	36	IGCT
	5L ANPC	ACS2000	4	6.9	0.25	3.68	IGBT
	5L H-bridge	ACS5000	6	13.8	2	36	IGCT
	CHB	ACS580MV	6	11	0.2	6.3	IGBT
Siemens	3L NPC	GM150	2.3	4.16	1	24	IGBT / IGCT
		SM150	3.3	4.16	2	31.5	IGBT / IGCT
	CHB	GH180	2.3	11		24.4	IGBT
	MMC	GH150	4	7.2	4	30	IGBT
	3L NPC / MMC	SM120 CM	3.3	7.2	4	13.3	IGBT
GE	nested NPP	MV6	3.3	13.8	0.1	6	IEGT
	unknown	MV7	3.3	13.8	6	100	IGBT

voltage summation on the high voltage side with series-connection of the PEBBs, while their outputs are all connected in parallel on the low voltage side.

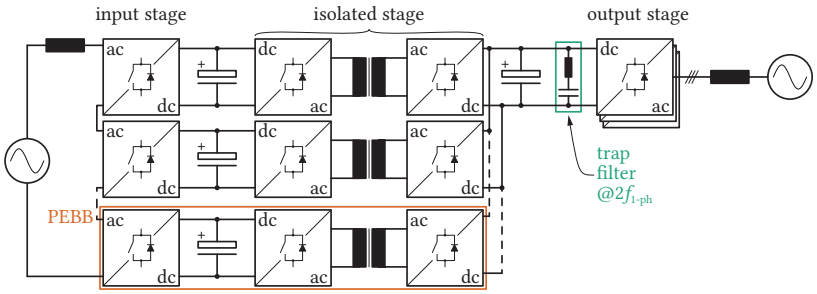


Fig. 2.6 SST from single-phase medium voltage ac (MVac) to LVac, typically found in traction applications. The three-stage conversion chain comprises: (i) an ac/dc active rectifier input stage with a CHB, (ii) a dc/dc isolated stage and (iii) a dc/ac inverter stage for the drive(s) supply.

The isolation stage can be realized with different topologies, either resonant or non-resonant. Non-resonant topologies are characterized by a fully controlled operation (both the power flow and output voltage are controlled), while resonant topologies feature a self regulating behavior (depending on the input-to-output voltage difference, the resonant tank gain will slightly change) and are mostly operated in open-loop. Some of them are presented in **Fig. 2.7**. An efficient high frequency operation is supported by soft-switching conditions. The DAB is the most well-known isolated dc/dc converter topology. Proposed in [35], its modes of operation (phase-shift and/or duty cycle modulation) have been developed in [36]. In general, the leakage inductor L_σ is kept as low as possible for minimizing the reactive power flow (i.e. larger current, meaning losses). However, controllability has to be maintained, implying a lower bound on L_σ, since the resolution on the phase-shift angle is directly determined from the maximum achievable time resolution in the control platform. Compared to the DAB, the DAB3 features a lower ripple on the dc-link, at the expense of a more complex angle step implementation (the almost hexagonal current trajectory in $\alpha\beta$ plane has to remain centered at origin [37]). For the resonant topologies, the number of possible combinations explodes with the number

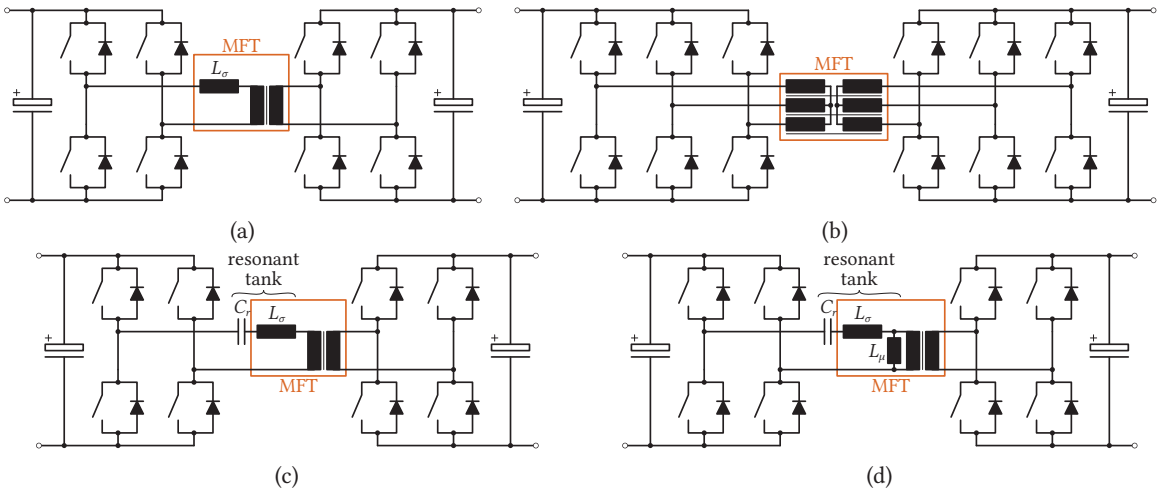


Fig. 2.7 Isolated dc/dc conversion stages using a medium frequency transformer (MFT): (a) dual active bridge (DAB), (b) three-phase DAB (DAB_3), (c) series-resonant and (d) *LLC* resonant.

of elements in the tank (cf. [38] for resonant tanks with three elements). Some combinations have little interest in comparison to others. Please note that even if the content presented here was limited to dc/dc isolated stages, ac/dc isolated stages with a cyclo-converter alike or unfolder behavior also exist. A thorough review of the various SST topologies and applications is available in [39].

While some impressive prototypes have demonstrated the technology for grid [40], [41] and traction applications [42], no commercial product for MV applications has hit the market at the moment. Today, the MFT design still remains the bottleneck of that technology, although some works show advances on the topic [43]. The scalability of such converters is compromised by the isolation requirements that change with the input voltage. Besides technical drawbacks/limitations, the cost of SSTs lies in a range of 5 to 10 times the equivalent state-of-the-art solution for comparable functionalities [44].

2.1.4 Other applications

Some other relevant applications in the medium/high power range could also be mentioned. In particular, flexible ac transmission systems (FACTS), battery energy storage systems (BESSs), static frequency converters (SFCs) and PHSPs.

FACTS are defined as ac transmission systems incorporating shunt or series-connected power electronic and static devices to enhance the controllability and increase the power transfer capability [45]. Among them, static synchronous compensators (STATCOMs) are able to perform reactive power compensation, transient stability enhancement, power oscillation damping and VAr reserve control (cf. **Fig. 2.8**). In [46], the intra branch balancing capability between the single-star [47] (through zero-sequence voltage injection) and delta-connected MMC [48] (through zero-sequence circulating current injection) were compared and it was concluded that the latter has a higher balancing capability.

The perspective to enhance the operation of STATCOMs with energy storage for frequency stabilization [49], or peak shaving / load balancing / emergency power source instead of diesel generators with BESSs (cf. **Fig. 2.9**), depending on the desired time scale for compensation, is promising, even though has not found any commercial application yet. The latter are used in combination with a large-scale

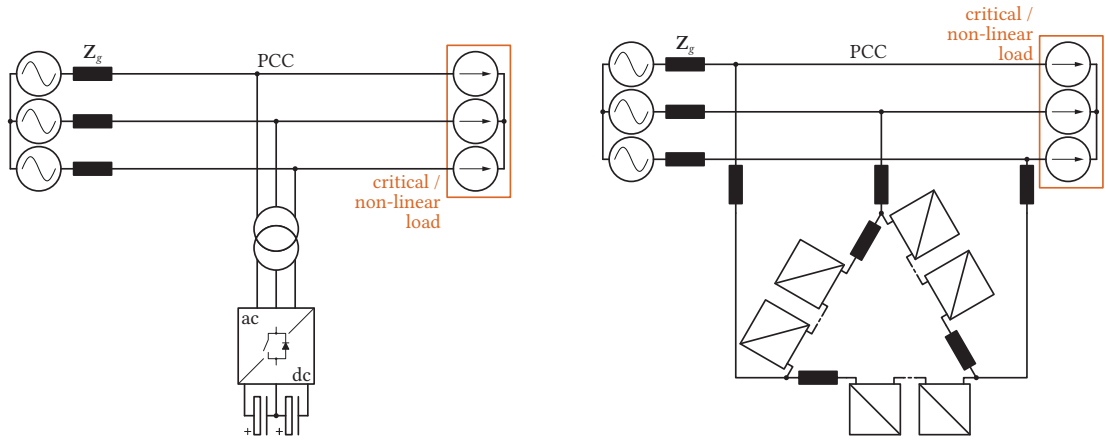


Fig. 2.8 STATCOM: (a) VSC-STATCOM with dc-link and (b) delta-connected MMC with bipolar cells.

RES, or as support for very weak grids / microgrids. The largest BESS was commissioned in 2017 in Australia [50] (100 MW, 129 MWh), outpassing the one installed in Fairbanks, Alaska [51] (46 MW for 5 min). Despite the proposition of the split battery energy storage [52], at this time no product or pilot installation is known to the author. In [53], CHB and MMC BESSs have been compared, and it was found that CHB solution requires less cells (i.e. a lower semiconductor count), features higher efficiency and better battery handling.

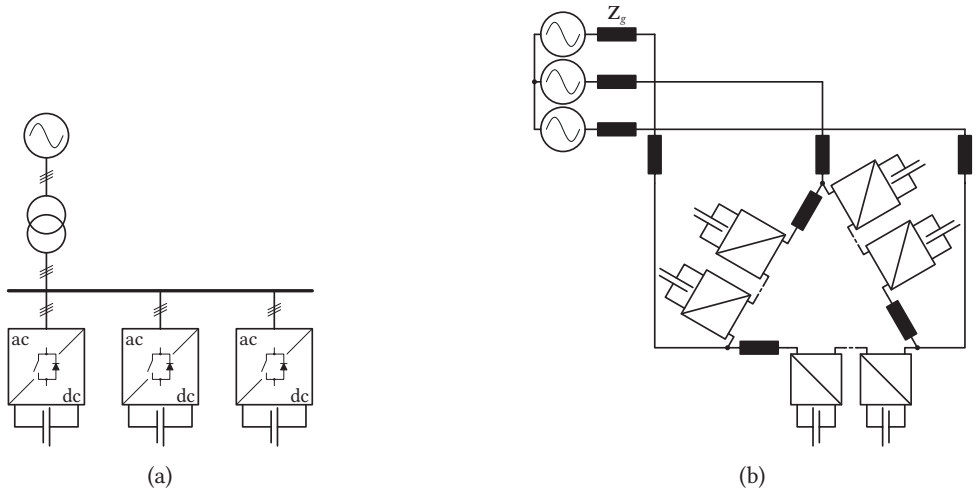


Fig. 2.9 BESS: (a) VSC-BESS with a step-down transformer and LVac feeder and (b) delta-connected MMC with bipolar cells and integrated split energy battery storage (note that filters or interface converters are required to protect the battery cells from high frequency current ripples).

SFCs are found in grid (from 50 to 60 Hz) and railway interties (from the three-phase 50 or 60 Hz utility grid to the single-phase 16.7, synchronous or asynchronous, 50 or 60 Hz traction supply line). Over the last few years, they experienced a technological evolution with the direct ac/ac MMC in place of the conventional back-to-back solution (cf. **Fig. 2.10**) [54].

PHSPs can be enhanced by variable-speed operation, which enables the operation of the pump-

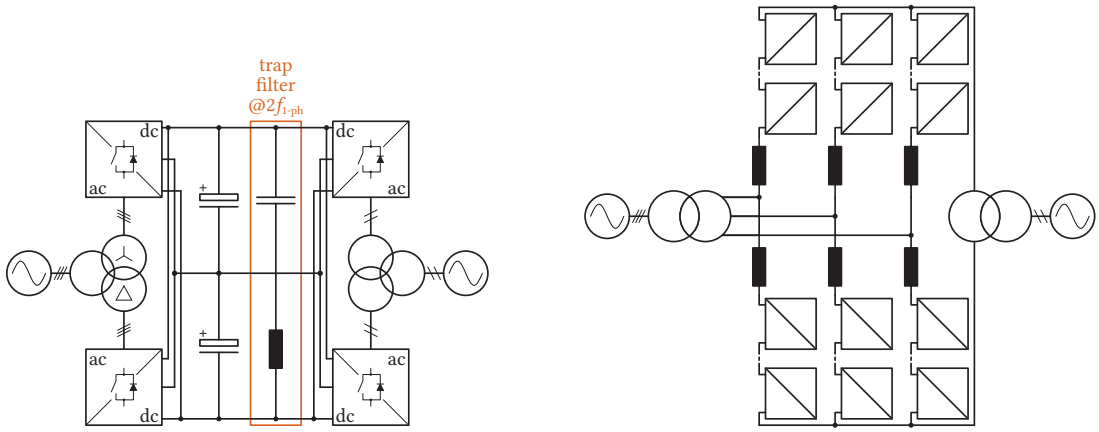


Fig. 2.10 SFC for railway interties: (a) old solution equipped with 3L-NPC legs and bulky trap filter on the dc-link tuned at twice the single-phase frequency and (b) new solution with direct ac/ac MMC and bipolar cells.

turbine at its best efficiency point, taking into account the hydraulic conditions (head and discharge), irrespectively of the grid frequency. Two configurations are possible (cf. **Fig. 2.11**): (i) partially rated converter (20-30 %) with doubly-fed induction generator (DFIG) and (ii) full-scale converter with synchronous machine. While DFIG is the most widely adopted solution for wind turbines, at considerably lower powers and voltages (< 10 MW), the ratings of a PHSP unit is in the few hundreds of MW range. Also, special operating conditions, such as the start-up in pump mode, are challenging. A fundamental contribution in DFIG for PHSP is found in [55]. Regarding the second configuration, a single full-scale converter installation in Grimsel is in operation at the moment, providing flexible operation in pump mode from 60 to 100 MW, while being bypassed in turbine mode [56]. In this installation, 3L back-to-back converters with a limited ac voltage (3.3 kV) are used, so that a machine-side transformer is also required. An interesting perspective with the use of a back-to-back MMC instead of the conventional solution, with the removal of the machine-side transformer, has been proposed in [57]. However, no proper in-depth analysis and comparison against the DFIG is presently available in the literature.

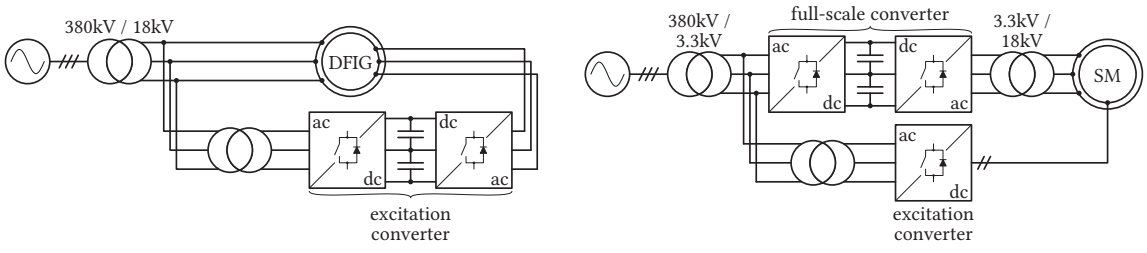


Fig. 2.11 Variable-speed PHSP configurations: (a) DFIG with rotor excitation fed by a frequency converter and (b) synchronous machine fed by a full-scale frequency converter. 18 kV is an upper limit for generator voltages.

2.1.5 Discussion

From the above paragraphs, a general and clear trend towards highly modular and scalable converter topologies is identified. The advantages offered by MMCs and alike topologies, such as excellent harmonic performance, high efficiency, high controllability, straightforward scalability, fault tolerant and fault blocking capabilities, are overcoming the drawbacks of more complex control algorithms, large communication network and potentially larger converter footprint. This observation is confirmed by the widespread adoption of these topologies by the industry. Versatile hardware platforms, e.g., a unipolar and bipolar cell, that can be used for multiple applications, is a decisive advantage, reducing converter development times, allowing for more focus on the application control, etc. provided that the high initial development costs are bearable.

2.2 Existing MVdc projects and products

At the time of writing, a few MVdc projects are reported. In 2000, ABB commissioned in Tjæreborg (Denmark) a 4.3 km/$\pm 9\,\mathrm{kV_{dc}}$ link transferring 7.2 MW using the HVdc light technology [58]. In France, in the frame of a tidal power demonstrator project, a 16 km/$10\,\mathrm{kV_{dc}}$ link transfers 1 MW [59]. In China, 29.2 km MVac links connecting an oil platform to the shore were repurposed to $\pm 15\,\mathrm{kV_{dc}}$ links transferring 8 MVA (unidirectional power transfer with diode front-end) [60]. Also, Siemens is offering MVdc Plus [61] (distance up to 200 km, voltage up to $\pm 50\,\mathrm{kV_{dc}}$ and power transfer up to 150 MW) and RXPE is advertising Smart VSC-MVDC transmission [62] (distance up to 100 km, voltage up to $50\,\mathrm{kV_{dc}}$). Also, the project AngleDC looks at the conversion of an existing double $29\,\mathrm{kV_{ac}}$ line to $\pm 27\,\mathrm{kV_{dc}}$ between the Isle of Anglesey and North Wales, aiming to increase the transmission power [63].

2.3 Topology selection

According to the scope of the thesis (cf. **Fig. 1.4**), the converter topology should accommodate a wide dc voltage range and comprise galvanic isolation. The high efficiency requirement eliminates SST based solutions, for the reason that the inverter stage on the low voltage side is not expected to be highly efficient, due to the large current amplitude [44]. Based on these considerations, the most suitable solution is to combine an MMC with a LFT for voltage adaptation. The transformer might not or might integrate the branch inductors, as it is proposed with the GIMC in this thesis (cf. **Fig. 2.12**). The MMC doesn't require a high semiconductor switching frequency, all semiconductors are on the low current side, the topology is redundant so high availability is obtained. This solution fulfills all the requirements with a minimum number of conversion stages.

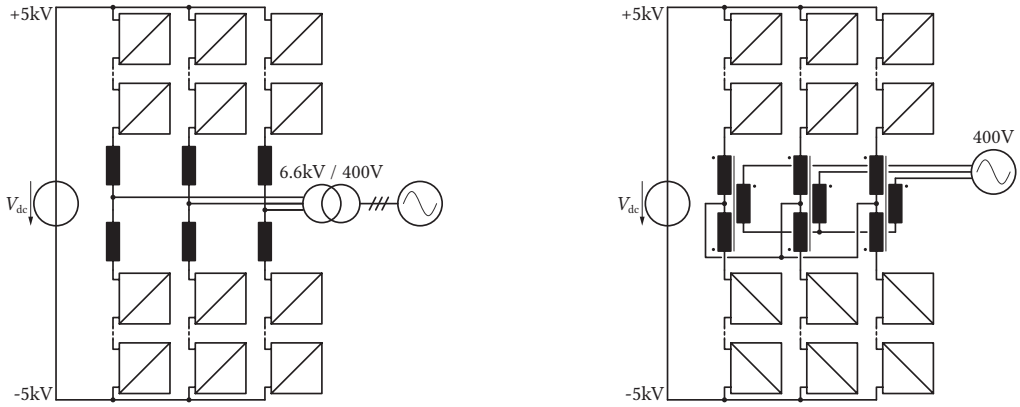


Fig. 2.12 Topology selection for the two stage conversion combining: (a) an MMC and an external LFT and (b) an MMC and a three-winding transformer with integrated branch inductors (GIMC).

3

Modular multilevel converter modeling

This chapters presents the modeling of the dc/3-ac MMC. Two linear mappings transform the branch voltages and currents into suitable bases for their control, that will be the focus of the following chapter, and permit the derivation of a decoupled model of the MMC between the dc and ac terminals. The power equations provide insight in the harmonic content of the branch quantities, e.g., the branch currents, summed capacitor voltages and modulation indices, and are fundamental to formulate the optimal circulating current injection. Finally, the converter energy requirements and SOA are derived for different scenarios.

3.1 Preliminary considerations

3.1.1 Layout and nomenclature

A dc/3-ac MMC is presented in **Fig. 3.1**. A branch (or arm or chainlink) comprises N_{cells} series-connected cells (or submodules) and a branch inductor L_{br} for the control of the branch current i_{br}. Two branches form a phase-leg.

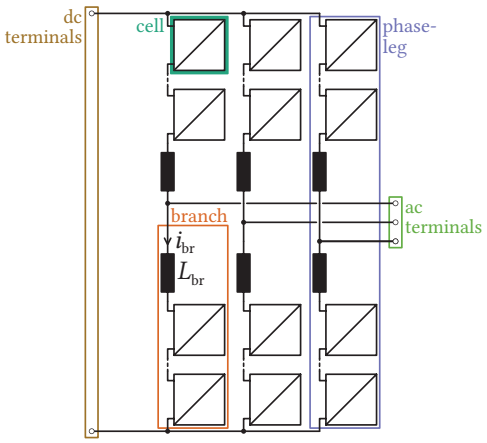
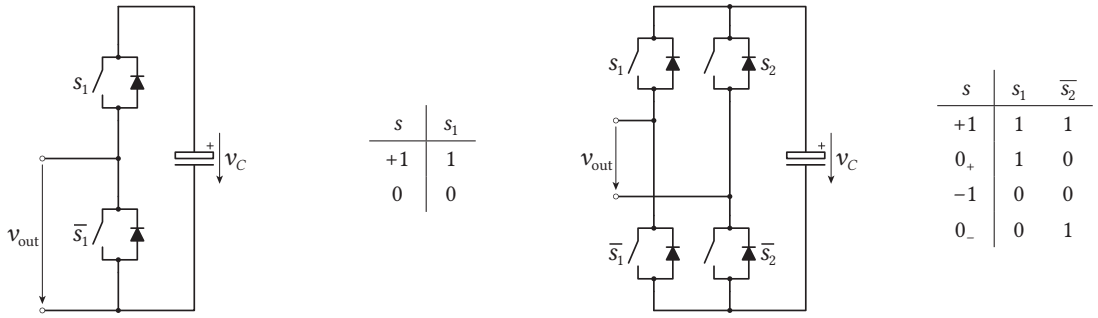


Fig. 3.1 MMC nomenclature.

3.1.2 Cell types

The MMC was originally proposed with unipolar cells (cf. **Fig. 3.2(a)**), as efficiency was the main objective. However, with time, the opportunity to embed a fault blocking capability inside the converter has become increasingly attractive. This was partly motivated on one hand by the fact that multi-terminal dc grids where not initially foreseen (only point-to-point dc connections were built, requiring a complete link shutdown and opening of the ac breakers in $\approx 60\,\text{ms}$[1] in case of fault) and on the other hand that dc breakers are neither simple to build nor come at an acceptable cost level. In order to maintain the loss increase below 150 % for bipolar cells (cf. **Fig. 3.2(b)**) compared to unipolar cells, the maximum modulation index should be kept below $\sqrt{2}$ [64]. Consequently, the maximum advised branch voltages are shown in **Fig. 3.3**.

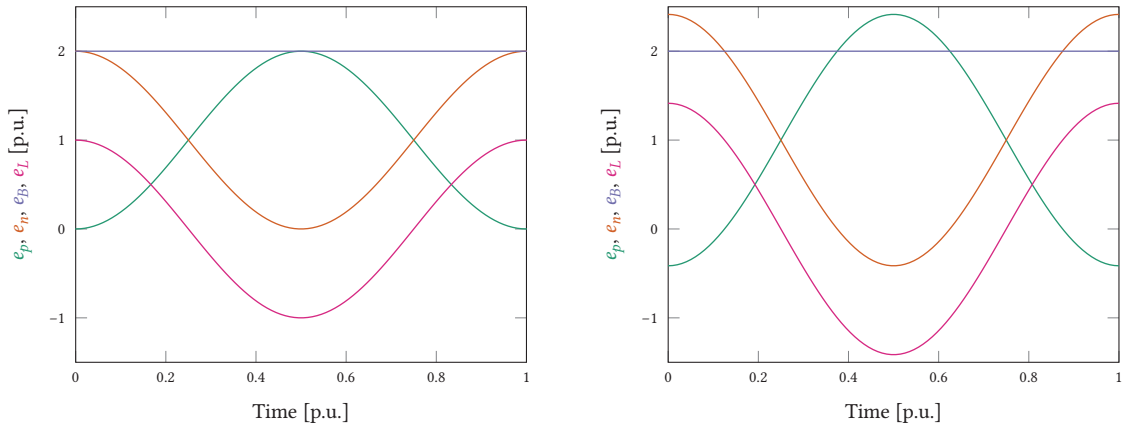


s	s_1
+1	1
0	0

s	s_1	$\overline{s_2}$
+1	1	1
0_+	1	0
−1	0	0
0_-	0	1

(a) (b)

Fig. 3.2 Basic cell types: (a) two-level unipolar cell with its switching table and (b) three-level bipolar cell with its switching table. Note that the switching combinations for the bipolar cell are given for s_1 and $\overline{s_2}$ rather than s_1 and s_2.



(a) (b)

Fig. 3.3 Maximum advised branch voltage limits: (a) unipolar cell and (b) bipolar cell. $e_{p/n}$ are the positive and negative branch voltages, e_B the dc bus voltage, defined as $e_B = e_p + e_n$, and e_L the ac phase voltage, defined as $e_L = (-e_p + e_n)/2$. The voltage base value is $V_{\text{dc}}/2$.

Other cell types have been proposed in the literature, such as the clamp-double cell (cf. **Fig. 3.4(a)**) [65] or semi-full-bridge cell (cf. **Fig. 3.4(b)**) [66], with the objective of achieving a fault blocking

[1] During this time, the converter has to withstand the surge current.

capability with a reduced semiconductor device count compared to a full-bridge cell. The clamp-double cell is not able to produce a negative voltage irrespectively of the branch current polarity. In contrast, the semi-full-bridge cell is able to produce a negative voltage irrespectively of the branch current polarity, thanks to the bidirectional switching in place of the diode.

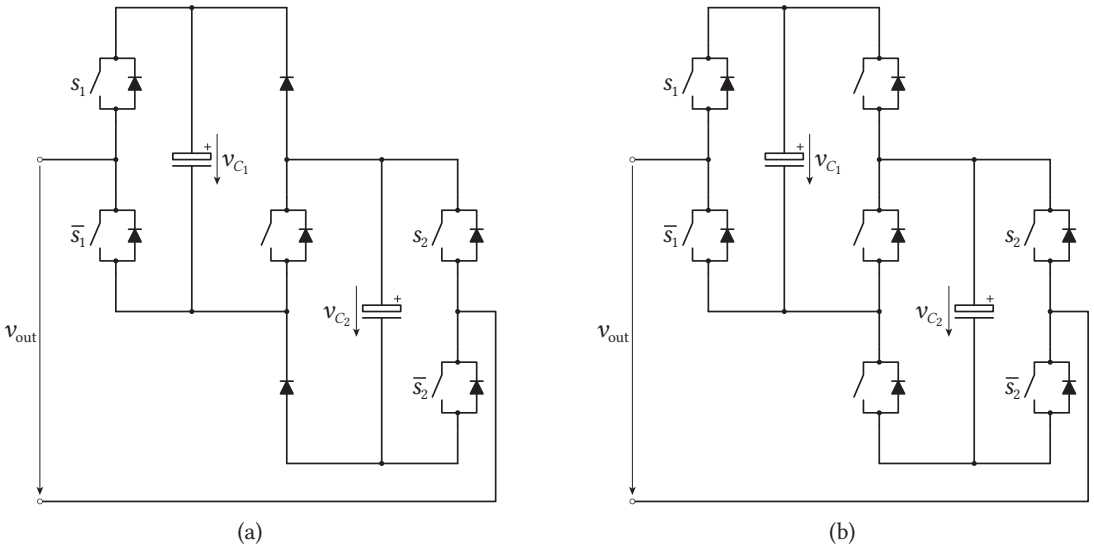


Fig. 3.4 Other cell types with fault blocking capability: (a) clamp-double cell, (b) semi-full-bridge cell.

Considering these limitations, the mixing of the two basic cell types [67], with at least half full-bridge cells to provide the fault blocking capability, is introduced. The maximum possible over-modulation for the full-bridge cells (i.e. pushing the phase voltage above $\pm V_{\text{dc}}/2$) is limited, else the stored energy between the half- and full-bridge cells would diverge [68]. In addition, it was recently shown in [69] that despite limiting the over-modulation depth, energy imbalances might still occur within a fundamental cycle, resulting in different stresses between the sets of cells.

Multilevel cells have also been proposed [70]. However, this implies an increased complexity of the cell design and in case of a faulty cell a potentially substantial number of levels might be lost.

3.2 Modeling

To derive the relevant equations governing the MMC dynamics, a single-phase MMC phase-leg (cf. **Fig. 3.5**) is analyzed. The branch can either be modeled with an average or a switched model without impact on the derivations that follow.

The branch dynamic equations are the following for each Kirchhoff's voltage law (KVL) loop:

$$\frac{V_{\text{dc}}}{2} = e_p + L_{\text{br}}\frac{\mathrm{d}}{\mathrm{d}t}i_p - M_{\text{br}}\frac{\mathrm{d}}{\mathrm{d}t}i_n + R_{\text{br}}i_p + L_g\frac{\mathrm{d}}{\mathrm{d}t}\Big(i_p - i_n\Big) + R_g(i_p - i_n) + v_g + v_{\text{CM}} \tag{3.1a}$$

$$\frac{V_{\text{dc}}}{2} = e_n + L_{\text{br}}\frac{\mathrm{d}}{\mathrm{d}t}i_n - M_{\text{br}}\frac{\mathrm{d}}{\mathrm{d}t}i_p + R_{\text{br}}i_n - L_g\frac{\mathrm{d}}{\mathrm{d}t}\Big(i_p - i_n\Big) - R_g(i_p - i_n) - v_g - v_{\text{CM}} \tag{3.1b}$$

where the subscripts p and n correspond to the positive and negative branch, respectively, e_x is the controlled voltage source that corresponds to the sum of the inserted cell voltages within a branch:

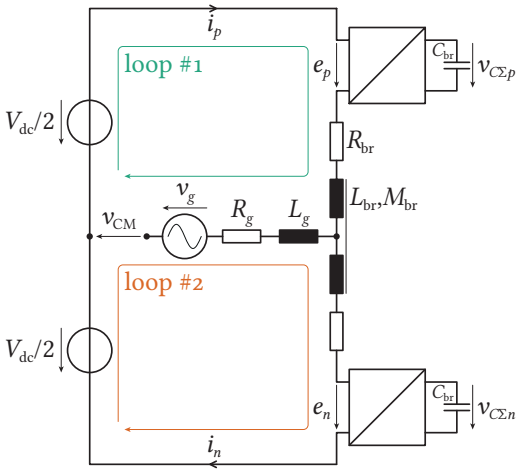


Fig. 3.5 Single-phase MMC, where the ac connection is assumed to be a star. The branch inductors are coupled with a coupling factor $k_{\text{br}} = M_{\text{br}}/L_{\text{br}}$. The strings of cells are represented by a single element, whose terminal voltages are $e_{p/n}$, without loss of generality whether an average or detailed switch model is used.

$e_x = \sum_{i=1}^{N_{\text{cells}}} s_{xi} v_{Cxi}$, with s_{xi} the cell switching function and v_{Cxi} the cell capacitor voltage for a switched branch model or $e_x = m_x v_{C\Sigma x}$ for an average branch model with m_x the modulation index, v_g the grid voltage, v_{CM} the common-mode voltage (both low and high frequency components, so that the impact of other phases is captured).

Equations (3.1) in the *pn* frame are not really insightful regarding the control of an MMC. For that reason, two linear mappings are performed [71]. They'll reveal a decoupling between the terminal quantities and also feature frequency specific contents. The respective sum and difference of (3.1) reveal a decoupling between the dc and ac quantities. In (3.2), the sum and difference of the branch voltages control independently the power exchange at both terminals, the cells acting as energy buffers.

$$V_{\text{dc}} = (e_p + e_n) + (L_{\text{br}} - M_{\text{br}})\frac{\mathrm{d}}{\mathrm{d}t}\big(i_p + i_n\big) + R_{\text{br}}(i_p + i_n) \tag{3.2a}$$

$$0 = (e_p - e_n) + (L_{\text{br}} + M_{\text{br}} + 2L_g)\frac{\mathrm{d}}{\mathrm{d}t}\big(i_p - i_n\big) + (R_{\text{br}} + 2R_g)(i_p - i_n) + 2v_g + 2v_{\text{CM}} \tag{3.2b}$$

From (3.2), new variables are defined:

$$\begin{bmatrix} i_{\text{circ}} \\ i_g \end{bmatrix} = \begin{bmatrix} 1/2 & 1/2 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} i_p \\ i_n \end{bmatrix} \quad \leftrightarrow \quad \begin{bmatrix} i_p \\ i_n \end{bmatrix} = \begin{bmatrix} 1 & 1/2 \\ 1 & -1/2 \end{bmatrix} \begin{bmatrix} i_{\text{circ}} \\ i_g \end{bmatrix} \tag{3.3a}$$

$$\begin{bmatrix} e_B \\ e_L \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ -1/2 & 1/2 \end{bmatrix} \begin{bmatrix} e_p \\ e_n \end{bmatrix} \quad \leftrightarrow \quad \begin{bmatrix} e_p \\ e_n \end{bmatrix} = \begin{bmatrix} 1/2 & -1 \\ 1/2 & 1 \end{bmatrix} \begin{bmatrix} e_B \\ e_L \end{bmatrix} \tag{3.3b}$$

where i_{circ} is the circulating current, i_g the phase current, e_B the bus voltage and e_L the phase voltage. With the newly defined variables, (3.2) become:

$$V_{\text{dc}} = e_B + 2(L_{\text{br}} - M_{\text{br}})\frac{\mathrm{d}}{\mathrm{d}t} i_{\text{circ}} + 2R_{\text{br}} i_{\text{circ}} \tag{3.4a}$$

$$0 = -e_L + \left(\frac{L_{\text{br}} + M_{\text{br}}}{2} + L_g\right)\frac{\mathrm{d}}{\mathrm{d}t} i_g + \left(\frac{R_{\text{br}}}{2} + R_g\right) i_g + v_g + v_{\text{CM}} \tag{3.4b}$$

or in state-space form:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{circ}} \\ i_g \end{bmatrix} = \begin{bmatrix} -\frac{R_{\mathrm{br}}}{L_{\mathrm{br}}-M_{\mathrm{br}}} & 0 \\ 0 & -\frac{\frac{R_{\mathrm{br}}}{2}+R_g}{\frac{L_{\mathrm{br}}+M_{\mathrm{br}}}{2}+L_g} \end{bmatrix}\begin{bmatrix} i_{\mathrm{circ}} \\ i_g \end{bmatrix} + \begin{bmatrix} \frac{1}{2(L_{\mathrm{br}}-M_{\mathrm{br}})} & 0 \\ 0 & \frac{1}{\frac{L_{\mathrm{br}}+M_{\mathrm{br}}}{2}+L_g} \end{bmatrix}\begin{bmatrix} V_{\mathrm{dc}} - e_B \\ e_L - v_g - v_{\mathrm{CM}} \end{bmatrix} \tag{3.5}$$

The controllable variables (through the respective branch modulation indices / insertion indices) are the bus voltage e_B and the phase voltage e_L. It is important to note that the branch inductor coupling has an opposite effect on the circulating and the phase current. If the coupling factor is positive ($k_{\mathrm{br}} = M_{\mathrm{br}}/L_{\mathrm{br}}$), the filtering of the phase current is favored over the filtering of the circulating current, and vice versa (cf. the second term of the right-hand side of (3.5)).

The branch capacitor voltages dynamics are defined by:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} v_{C\Sigma p} \\ v_{C\Sigma n} \end{bmatrix} = \frac{1}{C_{\mathrm{br}}}\begin{bmatrix} m_p & 0 \\ 0 & m_n \end{bmatrix}\begin{bmatrix} i_p \\ i_n \end{bmatrix} \tag{3.6}$$

Similar to the definitions of the bus and phase voltages in (3.3), the branch capacitor voltages are transformed into:

$$\begin{bmatrix} v^{\Sigma}_{C\Sigma} \\ v^{\Delta}_{C\Sigma} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ -1/2 & 1/2 \end{bmatrix}\begin{bmatrix} v_{C\Sigma p} \\ v_{C\Sigma n} \end{bmatrix} \quad \leftrightarrow \quad \begin{bmatrix} v_{C\Sigma p} \\ v_{C\Sigma n} \end{bmatrix} = \begin{bmatrix} 1/2 & -1 \\ 1/2 & 1 \end{bmatrix}\begin{bmatrix} v^{\Sigma}_{C\Sigma} \\ v^{\Delta}_{C\Sigma} \end{bmatrix} \tag{3.7}$$

This linear mapping allows one to compare the amount of stored energy between the phase-legs (via $v^{\Sigma}_{C\Sigma}$) and between the positive and negative branches within the same phase-leg (via $v^{\Delta}_{C\Sigma}$). This forms the foundation of the so-called *energy balancing* control, which is specific to the MMC.

The modulation indices can be also transformed as to obtain:

$$\begin{bmatrix} m_{\Sigma} \\ m_{\Delta} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ -1/2 & 1/2 \end{bmatrix}\begin{bmatrix} m_p \\ m_n \end{bmatrix} \quad \leftrightarrow \quad \begin{bmatrix} m_p \\ m_n \end{bmatrix} = \begin{bmatrix} 1/2 & -1 \\ 1/2 & 1 \end{bmatrix}\begin{bmatrix} m_{\Sigma} \\ m_{\Delta} \end{bmatrix} \tag{3.8}$$

The dynamic evolution of the transformed branch capacitor voltages follows:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} v^{\Sigma}_{C\Sigma} \\ v^{\Delta}_{C\Sigma} \end{bmatrix} = \frac{1}{C_{\mathrm{br}}}\begin{bmatrix} m_{\Sigma} & -m_{\Delta} \\ m_{\Delta} & -m_{\Sigma}/4 \end{bmatrix}\begin{bmatrix} i_{\mathrm{circ}} \\ i_g \end{bmatrix} \tag{3.9}$$

Finally, a decoupled MMC model is obtained in **Fig. 3.6** from (3.5) and (3.9).

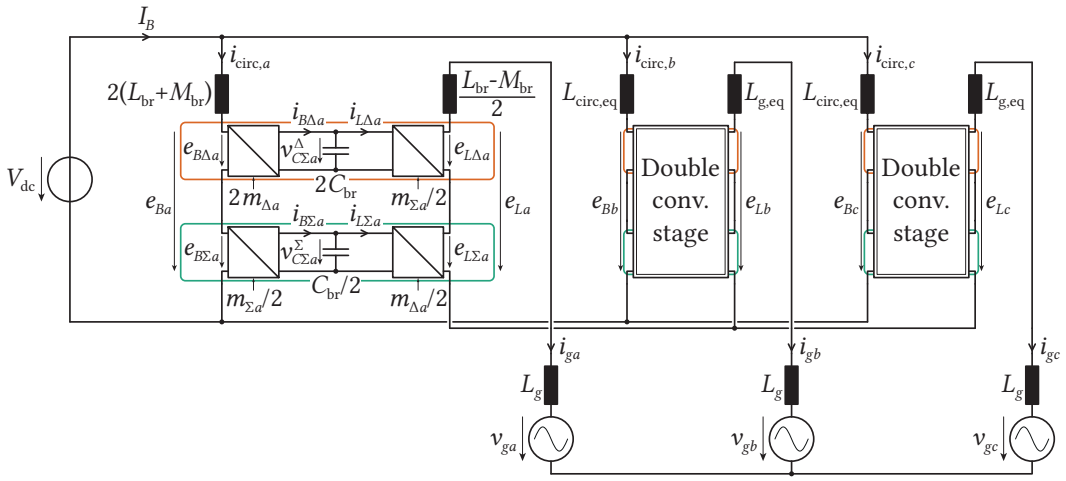


Fig. 3.6 Decoupled dc/3-ac MMC model: main (Σ) and secondary (Δ) power flow paths. The equivalent circulating and phase inductances are defined as $L_{\text{circ,eq}} = 2(L_{\text{br}} + M_{\text{br}})$ and $L_{\text{g,eq}} = \frac{L_{\text{br}}-M_{\text{br}}}{2}$. Note that the equivalent resistances have been omitted, but are obtained by substituting L by R.

3.3 Branch power equations

The branch power equations are extremely insightful regarding the internal control (especially the energy balancing) and the possible optimizations of the internal variables of an MMC. Several works have been reported in the literature, where initially the branch impendance (L_{br}, R_{br}) effect was neglected [72], [73] and further included for sake of completeness [74]. In every case, the principle is that, under the assumptions of a closed-loop controlled operation without branch energies imbalances, the expected (or reference) variables correspond to their measurements. As a consequence, for a given operating point, the branch currents and voltages can be reconstructed from the external variables.

The single-phase MMC is slightly modified compared to the previous section, since the focus is on the branch power and energies (cf. **Fig. 3.7**), making any complex grid modeling irrelevant.

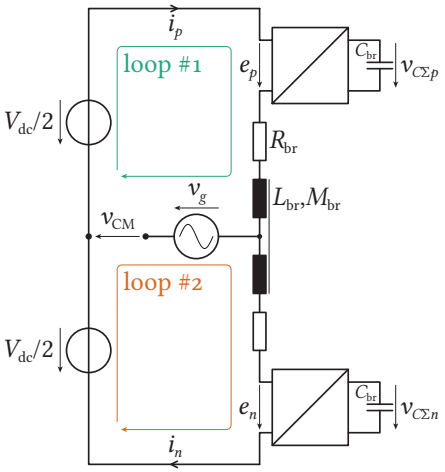


Fig. 3.7 Single-phase MMC with simplified ac side representation for the power equations.

3.3.1 Mathematical derivation

The derivation starts from the expressions of the branch voltage ($e_{p/n}$) and current ($i_{p/n}$). The first input is the branch voltage, which is nothing but a rearrangement of the KVL (3.1). The second input is the branch current, that contains a dc term, responsible for the power exchange with the dc terminals, a fundamental ac term, for the power exchange with the ac terminals, and a circulating current, whose harmonic content can be freely chosen, as it is a purely internal quantity.

$$e_{p/n}(t) = \frac{V_{\mathrm{dc}}}{2} \mp \left(v_{\mathrm{g}}(t) + v_{\mathrm{CM}}(t)\right) - \left(R_{\mathrm{br}} i_{p/n}(t) + L_{\mathrm{br}} \frac{\mathrm{d}}{\mathrm{d}t} i_{p/n}(t) - M_{\mathrm{br}} \frac{\mathrm{d}}{\mathrm{d}t} i_{n/p}(t)\right) \tag{3.10a}$$

$$i_{p/n}(t) = \frac{I_{\mathrm{dc}}}{3} \pm \frac{i_{\mathrm{g}}(t)}{2} + i_{\mathrm{circ}}(t) \tag{3.10b}$$

where

$$V_{\mathrm{dc}} \qquad \text{the dc-link voltage} \tag{3.11a}$$

$$v_{\mathrm{g}}(t) = k_{\mathrm{ac}} \frac{V_{\mathrm{dc}}}{2} \cos\left(\omega t - \frac{2\pi(k-1)}{3}\right) \qquad \text{the ac grid voltage} \tag{3.11b}$$

$$v_{\mathrm{CM}}(t) = \sum_i \hat{v}_{\mathrm{CM},i} \cos(i3\omega t) \qquad \text{the CM voltage} \tag{3.11c}$$

$$I_{\mathrm{dc}} \qquad \text{the dc-link current} \tag{3.11d}$$

$$i_{\mathrm{g}}(t) = \hat{i}_g \cos\left(\omega t + \phi - \frac{2\pi(k-1)}{3}\right) \qquad \text{the ac grid current} \tag{3.11e}$$

$$i_{\mathrm{circ}}(t) = \sum_{6\nmid l} \hat{i}_{\mathrm{circ},l} \cos\left(l2\omega t + \theta_l - \frac{2\pi(k-1)}{3}\right) \qquad \text{the circulating current} \tag{3.11f}$$

with $k \in \{1, 2, 3\}$ the phase number. The CM voltage and circulating current are generic functions with specific harmonic contents. The CM harmonics are all the triplen harmonics of the grid frequency ω. The circulating current harmonics are all even harmonics except the multiple of 6. Generally speaking, odd harmonics might be considered, but they would impair the vertical energy balance, which is not desired in steady-state. This limits the use of odd harmonics in the circulating current to transients, i.e. when the vertical energy balance has to be restored. The circulating currents should cancel each other at the dc, implying a phase-shift of $2\pi/3$ between the phase-legs.

The branch power expressions ($p_{p/n}(t) = e_{p/n}(t) i_{p/n}(t)$) are given as:

$$\begin{aligned} p_{p/n}(t) = {} & \frac{V_{\mathrm{dc}} I_{\mathrm{dc}}}{6} \pm \frac{V_{\mathrm{dc}} i_{\mathrm{g}}(t)}{4} + \frac{V_{\mathrm{dc}} i_{\mathrm{circ}}(t)}{2} \mp \frac{I_{\mathrm{dc}} \left(v_{\mathrm{g}}(t) + v_{\mathrm{CM}}(t)\right)}{3} - \frac{i_{\mathrm{g}}(t) \left(v_{\mathrm{g}}(t) + v_{\mathrm{CM}}(t)\right)}{2} \\ & \mp i_{\mathrm{circ}}(t) \left(v_{\mathrm{g}}(t) + v_{\mathrm{CM}}(t)\right) - \left(R_{\mathrm{br}} i_{p/n}(t)^2 + L_{\mathrm{br}} i_{p/n}(t) \frac{\mathrm{d}}{\mathrm{d}t} i_{p/n}(t) - M_{\mathrm{br}} i_{p/n}(t) \frac{\mathrm{d}}{\mathrm{d}t} i_{n/p}(t)\right) \end{aligned} \tag{3.12}$$

The branch powers can be transformed similarly to the sum of capacitor voltages: $p_\Sigma = p_p + p_n$ and $p_\Delta = (-p_p + p_n)/2$. Note that p_Σ only contains even harmonics, while p_Δ only contains odd harmonics.

$$p_\Sigma(t) = \frac{V_{\mathrm{dc}} I_{\mathrm{dc}}}{3} + V_{\mathrm{dc}} i_{\mathrm{circ}}(t) - i_{\mathrm{g}}(t) \left(v_{\mathrm{g}}(t) + v_{\mathrm{CM}}(t)\right) - 2\Big[R_{\mathrm{br}} \left(i_p(t)^2 + i_n(t)^2\right)$$

$$+ L_{\mathrm{br}}\left(i_p(t)\frac{\mathrm{d}}{\mathrm{d}t}i_p(t) + i_n(t)\frac{\mathrm{d}}{\mathrm{d}t}i_n(t)\right) - M_{\mathrm{br}}\left(i_p(t)\frac{\mathrm{d}}{\mathrm{d}t}i_n(t) + i_n(t)\frac{\mathrm{d}}{\mathrm{d}t}i_p(t)\right)\Bigg] \tag{3.13a}$$

$$p_\Delta(t) = -\frac{V_{\mathrm{dc}}\, i_g(t)}{8} + \frac{I_{\mathrm{dc}}\left(v_g(t) + v_{\mathrm{CM}}(t)\right)}{6} + \frac{i_{\mathrm{circ}}(t)\left(v_g(t) + v_{\mathrm{CM}}(t)\right)}{2} \tag{3.13b}$$

In order to ensure a zero net power transfer to the cells in steady-state, the branch power expressions, or p_Σ, should have a zero mean, i.e. their dc terms should cancel each other. This allows one to set the dc current, whose negative root is selected [75]:

$$0 = \frac{V_{\mathrm{dc}} I_{\mathrm{dc}}}{3} - \frac{\hat{i}_g^2 R_{\mathrm{br}}}{4} - \frac{\hat{i}_g \hat{v}_g \cos(\phi)}{2} - \frac{2R_{\mathrm{br}} I_{\mathrm{dc}}^2}{9} - 2R_{\mathrm{br}} i_{\mathrm{circ}}(t)^2\Big|_{\mathrm{dc}} \tag{3.14}$$

where $i_{\mathrm{circ}}(t)^2\Big|_{\mathrm{dc}} = \frac{1}{2}\sum_{6\nmid l} \hat{i}_{\mathrm{circ},l}^2$[2]. Note that due to R_{br}, there is a coupling between I_{dc} and $i_{\mathrm{circ}}(t)$, which will prove to be problematic later. It follows that:

$$I_{\mathrm{dc}} = \frac{3\left[V_{\mathrm{dc}} - \sqrt{V_{\mathrm{dc}}^2 - 2R_{\mathrm{br}}\left(2\hat{i}_g\hat{v}_g\cos(\phi) + R_{\mathrm{br}}\left(4\sum_{6\nmid l}\hat{i}_{\mathrm{circ},l}^2 + \hat{i}_g^2\right)\right)}\right]}{4R_{\mathrm{br}}} \tag{3.15}$$

The next step consists in obtaining the low frequency dynamics of the capacitor voltages by time integration of $p_{p/n}(t)$. The complete analytical expressions won't be shown here, but can be easily retrieved with a symbolic calculation software.

$$\Delta W_p(t) = \int p_p(t)\mathrm{d}t \tag{3.16a}$$

$$\Delta W_n(t) = \int p_n(t)\mathrm{d}t \tag{3.16b}$$

From there, the summed capacitor voltages evolution is retrieved.

$$v_{C\Sigma 0} = V_{\mathrm{dc}} - \frac{2R_{\mathrm{br}} I_{\mathrm{dc}}}{3} \Longrightarrow W_0 = \frac{1}{2} C_{\mathrm{br}} v_{C\Sigma 0}^2 \tag{3.17a}$$

$$v_{C\Sigma p/n}(t) = \sqrt{\frac{2\left(W_0 + \Delta W_{p/n}(t)\right)}{C_{\mathrm{br}}}} = \sqrt{v_{C\Sigma 0} + \frac{\Delta W_{p/n}(t)}{C_{\mathrm{br}}}} \tag{3.17b}$$

The final step is to determine which modulation index corresponds to the evaluated operating point.

$$m_p(t) = \frac{e_p(t)}{v_{C\Sigma p}(t)} \qquad m_n(t) = \frac{e_n(t)}{v_{C\Sigma n}(t)} \tag{3.18}$$

The power analysis method is powerful, since harmonics and parasitic components can be integrated in a transparent manner, at the expense of a higher mathematical burden. It allows one to evaluate the SOA of a converter, since the bounds can be easily evaluated (average capacitor voltage ripple,

[2] Recalling the trigonometric identity $[A\cos(x)]^2 = \frac{A^2}{2}[1 + \cos(2x)]$.

maximum branch current, discontinuous modulation limits), to size the required branch capacitor, etc. Still, the dynamic transients are not captured by the method (which only considers steady-state operation), meaning that even though some operating points were identified within the SOA, they might not be reached without a violation of the predefined bounds, due to the control system response or capacitor voltage spread if a very low cell switching frequency is selected.

3.3.2 Circulating current optimization

Several works explored the various possibilities offered by the circulating current optimization, which aims to set $p_{\Sigma}(t) = 0$, or at least cancel its low order harmonics. As a result, tighter margins between the average branch capacitor voltages and ac peak voltage are possible. This might be expressed differently as a reduction of the branch capacitance requirement for steady-state operation. In [76], for the first time, it was stated that the addition of a 2^{nd} harmonic circulating current with a magnitude of 50 % of the fundamental ac branch current was able to reduce the capacitor voltage ripple. In [72], simplified expressions for $i_{\text{circ}}(t)$ were presented, achieving the same effect. In [77], the benefit of the 2^{nd} harmonic circulating current through the shaping of the capacitor voltage ripple and consequently the extension of the voltage range was nicely illustrated. Reference [78] proposed an optimization of the circulating current for the minimization of the capacitor voltage ripple / minimized cell capacitance requirement with constraints on the branch RMS current. In [79], both a 2^{nd} and 4^{th} harmonic circulating currents are considered when a 3^{rd} harmonic CM voltage is used to extend the linear modulation range.

This section uses the generic notation introduced previously and shows that each of the proposals [72], [76], [79] are particular cases of a more generic problem.

In the next paragraphs, the impact of the circulating current and CM injection will be compared for various cases. The parameters for the converter model are listed in **Tab. 3.1**. The load angle ϕ takes the values $\left[0,\ \pi/3,\ \pi/2\right]$ for each 20 ms interval.

Tab. 3.1 System parameters for the power equations analysis comparison.

V_{dc}	10 kV	C_{br}	118.75 µF	S	0.5 MVA	f_g	50 Hz	k_{ac}	0.85

3.3.2.1 No circulating current and no passives

The results of the power equation analysis for the case without circulating current ($i_{\text{circ}}(t) = 0$) nor passives (R_{br}, L_{br} and M_{br}) are shown in **Fig. 3.8**. The branch voltages are symmetric sinusoids, as the contributions from L_{br} and M_{br} are neglected. The dc current is obtained from (3.14) with $R_{\text{br}} = 0$.

$$I_{\text{dc}} = \frac{3\hat{i}_g\hat{v}_g\cos(\phi)}{2V_{\text{dc}}} \tag{3.19}$$

As a consequence, the branch current waveforms only contain a fundamental ac component offset by the third of the dc current. The use of a CM voltage (here a 3^{rd} harmonic sine) lowers the peak-to-peak fundamental ac component of the branch voltage, leading to a reduction of the branch modulation indices.

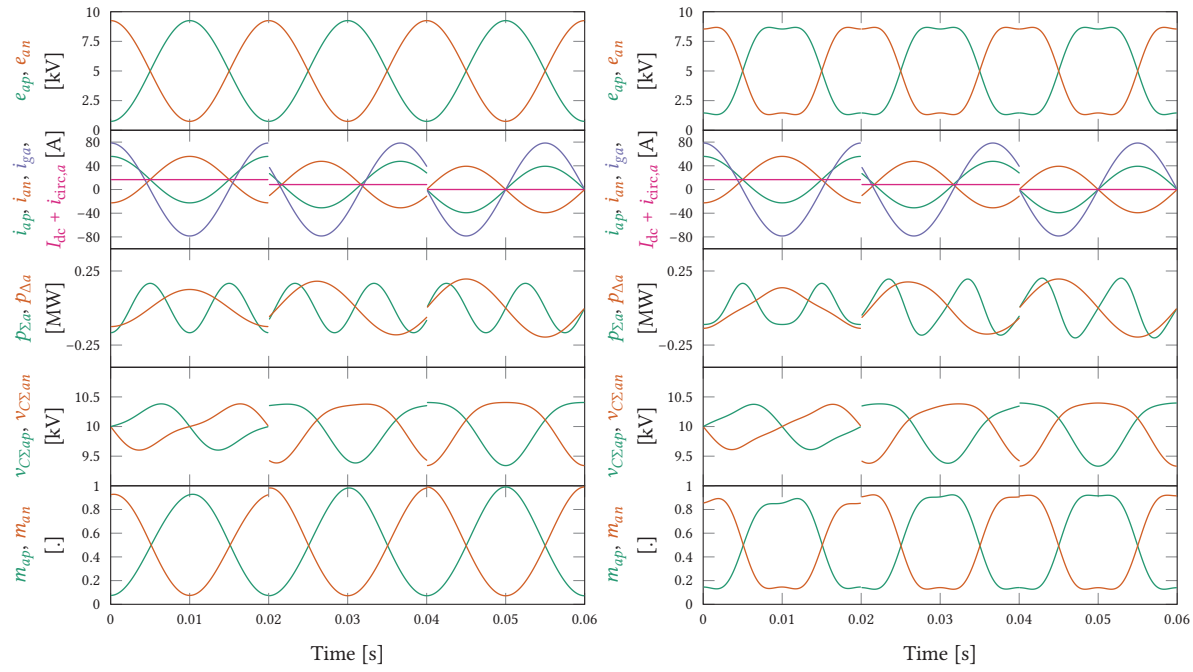


Fig. 3.8 MMC power equation analysis results in phase-leg a with $\phi = [0,\ \pi/3,\ \pi/2]$ for each interval of 20 ms: (a) without CM and (b) with CM injection.

3.3.2.2 No CM voltage and no passives

In the case there is neither CM voltage nor passives, the branch power sum (3.13) simplifies to:

$$p_{\Sigma}(t) = \frac{V_{dc} I_{dc}}{3} + V_{dc}\, i_{circ}(t) - \frac{\hat{i}_g \hat{v}_g \cos(\phi)}{2} - \frac{\hat{i}_g \hat{v}_g \cos(2\omega t + \phi)}{2} = 0 \tag{3.20}$$

The solution is straightforward. On one hand, the dc terms should cancel each other. On the other hand, a circulating current is used to cancel the harmonic term.

$$I_{dc} = \frac{3\hat{i}_g \hat{v}_g \cos(\phi)}{2V_{dc}} \tag{3.21a}$$

$$i_{circ}(t) = \frac{\hat{i}_g \hat{v}_g \cos(2\omega t + \phi)}{2V_{dc}} \tag{3.21b}$$

A 2nd harmonic circulating current will allow to set $p_{\Sigma}(t) = 0$. Note that, as stated in [76], the magnitude of the circulating current $\hat{i}_{circ,2}$ is approximately $\hat{i}_g/4$, since $\hat{v}_g \approx V_{dc}/2$. Similar findings were presented in [72]. Consequently, two new terms originating from $i_{circ}(t)\hat{v}_g \cos(\omega t)$ appear in $p_{\Delta}(t)$ with the addition of a second harmonic circulating current:

$$p_{\Delta}(t) = \frac{I_{dc}\hat{v}_g \cos(\omega t)}{3} - \frac{\hat{i}_g V_{dc} \cos(\omega t + \phi)}{4} + \frac{\hat{i}_g \hat{v}_g^2 \cos(3\omega t + \phi)}{4V_{dc}} + \frac{\hat{i}_g \hat{v}_g^2 \cos(\omega t + \phi)}{4V_{dc}} \tag{3.22}$$

The result is shown in **Fig. 3.9(a)**.

3.3.2.3 CM voltage and no passives

In the case a CM voltage is present and that the passives are neglected, the branch powers sum (3.13) simplifies to:

$$p_\Sigma(t) = -\hat{i}_g \cos\big(\omega t + \phi\big) v_{\mathrm{CM}}(t) - \frac{\hat{i}_g \hat{v}_g \cos\big(\phi\big)}{2} - \frac{\hat{i}_g \hat{v}_g \cos\big(2\omega t + \phi\big)}{2} + i_{\mathrm{circ}}(t) V_{\mathrm{dc}} + \frac{I_{\mathrm{dc}} V_{\mathrm{dc}}}{3} = 0 \tag{3.23}$$

As $R_{\mathrm{br}} = 0$, the solution for I_{dc} is identical to (3.21a). The circulating current expression is:

$$i_{\mathrm{circ}}(t) = \frac{\hat{i}_g \Big[2\cos\big(\omega t + \phi\big) v_{\mathrm{CM}}(t) + \hat{v}_g \cos\big(2\omega t + \phi\big)\Big]}{2V_{\mathrm{dc}}} \tag{3.24}$$

The result is identical to [79]. The order of $i_{\mathrm{circ}}(t)$ depends on the harmonic expansion of $v_{\mathrm{CM}}(t)$. For example, with a 3^{rd} harmonic CM injection, 2^{nd} and 4^{th} harmonic circulating currents are used.

$$\begin{aligned} p_\Delta(t) = &-\frac{2I_{\mathrm{dc}} \hat{v}_g \cos(\omega t)}{3} + \frac{\hat{i}_g V_{\mathrm{dc}} \cos\big(\omega t + \phi\big)}{2} - 2\hat{v}_g \cos(\omega t) i_{\mathrm{circ}}(t) - \frac{2I_{\mathrm{dc}} v_{\mathrm{CM}}(t)}{3} \\ &- 2v_{\mathrm{CM}}(t) i_{\mathrm{circ}}(t) \\ = &-\frac{2I_{\mathrm{dc}} \hat{v}_g \cos(\omega t)}{3} + \frac{\hat{i}_g V_{\mathrm{dc}} \cos\big(\omega t + \phi\big)}{2} - \frac{2I_{\mathrm{dc}} v_{\mathrm{CM}}(t)}{3} \\ &- \frac{\hat{i}_g \Big[2\cos\big(\omega t + \phi\big) v_{\mathrm{CM}}(t) + \hat{v}_g \cos\big(2\omega t + \phi\big)\Big] \Big[\hat{v}_g \cos(\omega t) + v_{\mathrm{CM}}(t)\Big]}{V_{\mathrm{dc}}} \end{aligned} \tag{3.25}$$

The result is shown in **Fig. 3.9(b)**.

3.3.2.4 Passives included

In case passives are included, no analytical solution exists. In the case no CM voltage is used, the sum of branch powers equals:

$$\begin{aligned} p_\Sigma(t) = &\frac{\hat{i}_g^2}{4}(L_{\mathrm{br}} + M_{\mathrm{br}})\omega \sin\big(2\omega t + 2\phi\big) - \frac{2I_{\mathrm{dc}}}{3}(L_{\mathrm{br}} - M_{\mathrm{br}})\frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{circ}}(t) - \frac{4R_{\mathrm{br}} I_{\mathrm{dc}} i_{\mathrm{circ}}(t)}{3} \\ &- 2(L_{\mathrm{br}} - M_{\mathrm{br}})\frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{circ}}(t) i_{\mathrm{circ}}(t) - \frac{R_{\mathrm{br}} \hat{i}_g^2}{4} - \frac{R_{\mathrm{br}} \hat{i}_g^2 \cos\big(2\omega t + 2\phi\big)}{4} - \frac{\hat{i}_g \hat{v}_g \cos\big(\phi\big)}{2} \\ &- \frac{\hat{i}_g \hat{v}_g \cos\big(2\omega t + \phi\big)}{2} - \frac{2R_{\mathrm{br}} I_{\mathrm{dc}}^2}{9} + \frac{I_{\mathrm{dc}} V_{\mathrm{dc}}}{3} - 2R_{\mathrm{br}} i_{\mathrm{circ}}(t)^2 + i_{\mathrm{circ}}(t) V_{\mathrm{dc}} \end{aligned} \tag{3.26}$$

One one hand, due to R_{br}, the expressions for I_{dc} and $i_{\mathrm{circ}}(t)$ are coupled. If $R_{\mathrm{br}} \approx 0$, which is an acceptable simplification since it only contributes to the losses of the system, the expression for p_Σ simplifies to:

$$\begin{aligned} p_\Sigma(t) = &\frac{\hat{i}_g^2}{4}\left(L_{\mathrm{br}} + M_{\mathrm{br}}\right)\omega \sin\big(2\omega t + 2\phi\big) - 2\left(L_{\mathrm{br}} - M_{\mathrm{br}}\right)\left[\frac{I_{\mathrm{dc}}}{3} + i_{\mathrm{circ}}(t)\right]\frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{circ}}(t) \\ &- \frac{\hat{i}_g \hat{v}_g \cos\big(\phi\big)}{2} - \frac{\hat{i}_g \hat{v}_g \cos\big(2\omega t + \phi\big)}{2} + \frac{I_{\mathrm{dc}} V_{\mathrm{dc}}}{3} + i_{\mathrm{circ}}(t) V_{\mathrm{dc}} \end{aligned} \tag{3.27}$$

On the other hand, by looking at (3.27), the non-existence of an analytical solution is manifest.

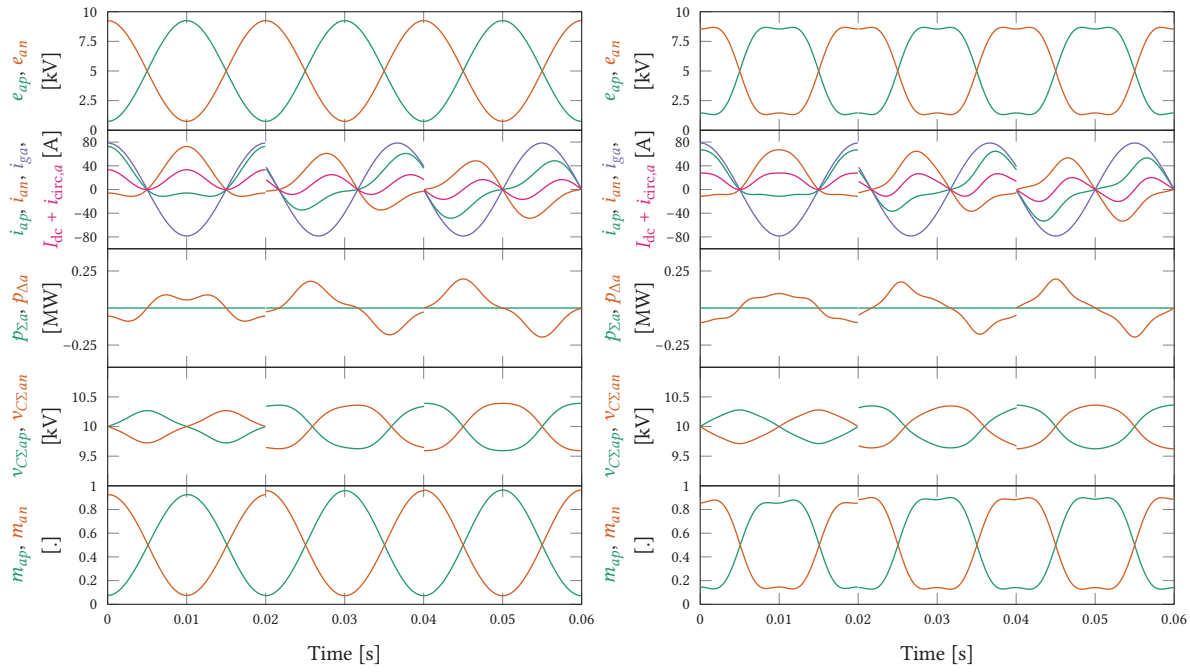


Fig. 3.9 MMC power equation analysis results in phase-leg a with $\phi = [0, \pi/3, \pi/2]$ for each interval and circulating current injection: (a) without CM and (b) with CM injection. In both cases, $p_\Sigma(t) = 0$, so the compensation is effective.

3.4 Branch capacitance selection

The branch capacitor voltage ripple is central in the voltage generation capability of an MMC, in the sense that the required branch voltage must be always smaller than the sum of capacitor voltages. On the one hand, it is desirable for power density and cost reasons to minimize the branch capacitance. On the other hand, larger cell capacitance designs provide more robust converter behavior, especially for fault ride through and fast power transients.

Numerous publications [73], [74], [78], [80], [81] have dealt with this question, and there is a general agreement that the energy requirement for a dc/3-ac MMC is approximately 45 kJ/MVA with a voltage ripple factor $\varepsilon_{v_{C\Sigma}} = 10\,\%$.

Unlike what is claimed in [18], [81], [82], it is visible from **Fig. 3.10** that the branch energy ripple, is not symmetrical around its average ($\Delta W_{\mathrm{br},+} \neq \Delta W_{\mathrm{br},-}$) for the cases for $\phi \neq \{0, \pi\}$ or without circulating current injection, meaning that the peak-to-average branch energy ripple, and not the peak-to-peak branch energy ripple, shall be used to determine the branch energy requirement. In case the branch impedance (L_{br}, R_{br}) is discarded, the maximum energy ripples are obtained for $\phi = \pm\pi/2$. Else, the maximum is slightly shifted from $\pm\pi/2$. The peak to average energy ripple has to be buffered by the branch capacitance, i.e.

$$\Delta W_{\mathrm{br},+} = \frac{1}{2} C_{\mathrm{br}} v_{C\Sigma,\max}^2 - \frac{1}{2} C_{\mathrm{br}} v_{C\Sigma 0}^{\star 2} \qquad \rightarrow \qquad C_{\mathrm{br}} = \frac{2\Delta W_{\mathrm{br},+}}{\left[(1 + \varepsilon_{v_{C\Sigma}})^2 - 1\right] v_{C\Sigma 0}^{\star 2}} \tag{3.28a}$$

$$\Delta W_{\mathrm{br},-} = \frac{1}{2} C_{\mathrm{br}} v_{C\Sigma 0}^{\star 2} - \frac{1}{2} C_{\mathrm{br}} v_{C\Sigma,\min} \quad \rightarrow \quad C_{\mathrm{br}} = \frac{2\Delta W_{\mathrm{br},-}}{\left[1 - (1 - \varepsilon_{v_{C\Sigma}})^2\right] v_{C\Sigma 0}^{\star 2}} \tag{3.28b}$$

From (3.28), it is found that the branch energy requirement is determined by the energy ripple below the average, $\Delta W_{\mathrm{br},-}$, since $\left[1 - (1 - \varepsilon_{v_{C\Sigma}})^2\right] < \left[(1 + \varepsilon_{v_{C\Sigma}})^2 - 1\right]$.

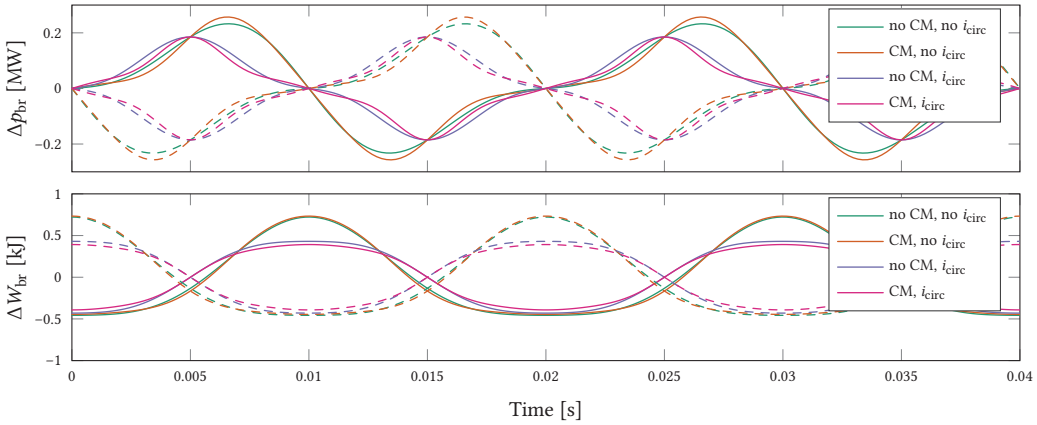


Fig. 3.10 Branch power (top plot) and energy (bottom plot) ripples for the prototype converter ratings with $k_{\mathrm{ac}} = 0.9$, $\phi = -\pi/2$ and the branch impedance neglected (marginal contribution). The plain lines correspond to the positive branch, while the dashed ones to the negative branch. The worst case is in red, with CM injection and no harmonic circulating current injection.

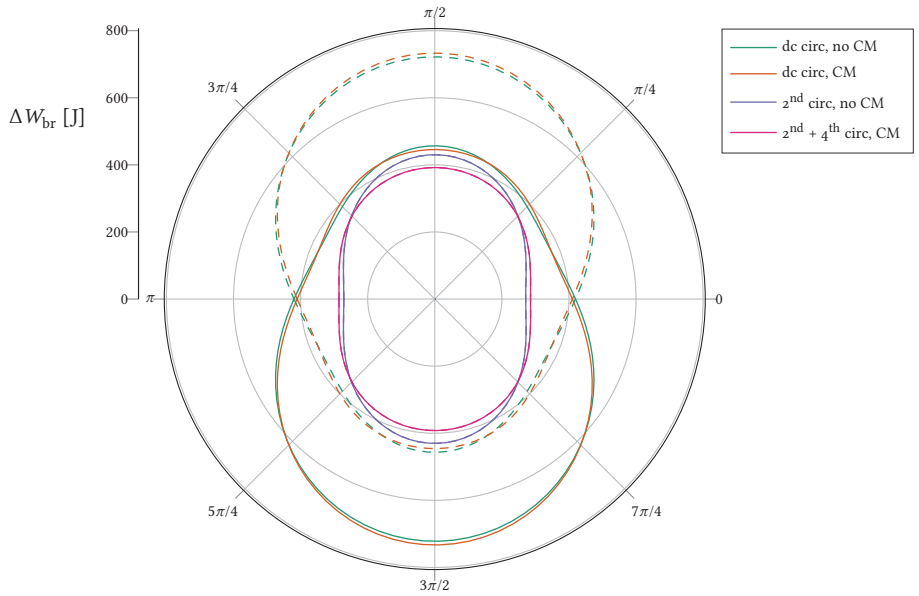


Fig. 3.11 Polar plot of the peak-to-average branch energy ripples. The plain lines correspond to $\Delta W_{\mathrm{br},p+}$, while the dashed ones to $\Delta W_{\mathrm{br},p-}$. It is clear that the peak-to-peak energy ripples for the cases without circulating current harmonic injection are only symmetrical for $\phi = \{0, \pi\}$ (at their crossings).

Tab. 3.2 summarizes the converter energy requirements derived from **Fig. 3.11**. For steady-state operation, the injection of a circulating current permits a reduction of the energy requirement by around 60 %. **Fig. 3.12** presents the summed branch capacitor voltage ripples for different power

factor and each of the four analyzed cases. Note that the choice of the CM injection methods has barely no impact, since min/max CM injection [83] leads to 0.19 kJ/MVA more energy requirement, while flat-top CM injection [84] leads to 0.12 kJ/MVA less.

Tab. 3.2 Converter energy requirements summary for $k_{ac} = 0.9$, $v^{\star}_{C\Sigma 0} = V_{dc}$ and $\varepsilon_{v_{C\Sigma}} = 10\,\%$.

Case #	CM	2^{nd} (+ 4^{th}) harmonic	Energy requirement [kJ/MVA]
1	○	○	45.6
2	○	●	46.3
3	●	○	27.2
4	●	●	24.8

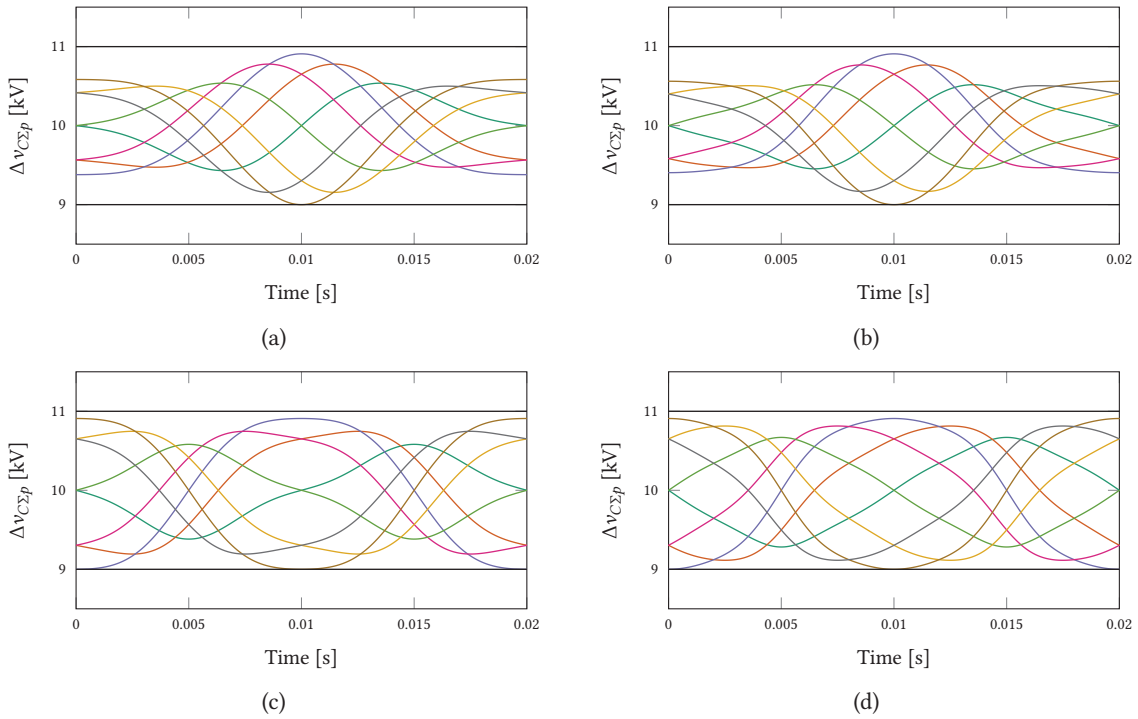


Fig. 3.12 Summed branch capacitor voltage ripples for different C_{br} sizing for $k_{ac} = 0.9$, $v^{\star}_{C\Sigma 0} = V_{dc}$, $\varepsilon_{v_{C\Sigma}} = 10\,\%$, $\phi \in \{-\pi, -3\pi/4, -\pi/2, -\pi/4, 0, \pi/4, \pi/2, 3\pi/4\}$: (a) case 1 ($C_{br} = 75\,\mu F$), (b) case 2 ($C_{br} = 76.07\,\mu F$), (c) case 3 ($C_{br} = 44.47\,\mu F$) and (d) case 4 ($C_{br} = 40.91\,\mu F$) as defined in **Tab. 3.2**. In each case, the lower bound is exactly hit for $\phi = -\pi/2$.

In practice, such savings might not be achievable, since transient responses (the converter shall not trip) or low cell switching frequencies (high branch capacitor voltage spread) impose higher constraints on the converter energy requirements. However, the converter energy requirement can be simply lowered by increasing $\varepsilon_{v_{C\Sigma}}$ and the average summed branch capacitor voltage (minimum value given in (3.17a)) at the expense of an increase of the switching losses.

3.5 Safe operating area

The SOA is defined by three sets of constraints: (i) the modulation index is bounded by 0 and 1 for unipolar cells, (ii) the maximum branch current is bounded to 75 A (thermal limit for the converter prototype) and (iii) the capacitor voltage ripple should not exceed ±10 % of the dc bus voltage. **Fig. 3.13** shows the resulting SOA for various MMC operating conditions, i.e. with dc or dc plus $2^{\text{nd}}/4^{\text{th}}$ harmonic circulating current injection and with or without CM voltage injection. It is observed that the CM injection enables a significant extension of the SOA in the positive reactive power area ($\phi \in [0,\ \pi]$), thanks to the modification of the branch voltage waveform that displaces the intersection between the summed branch capacitor voltage and the branch voltage. In the active power area, the SOA is constrained by the maximum branch current, hence a purely dc circulating current with a lower peak value is beneficial. The constraints on the boundary of the SOAs for two load angles, $\phi = \{0,\ \pi/2\}$ are displayed in **Fig. 3.14**.

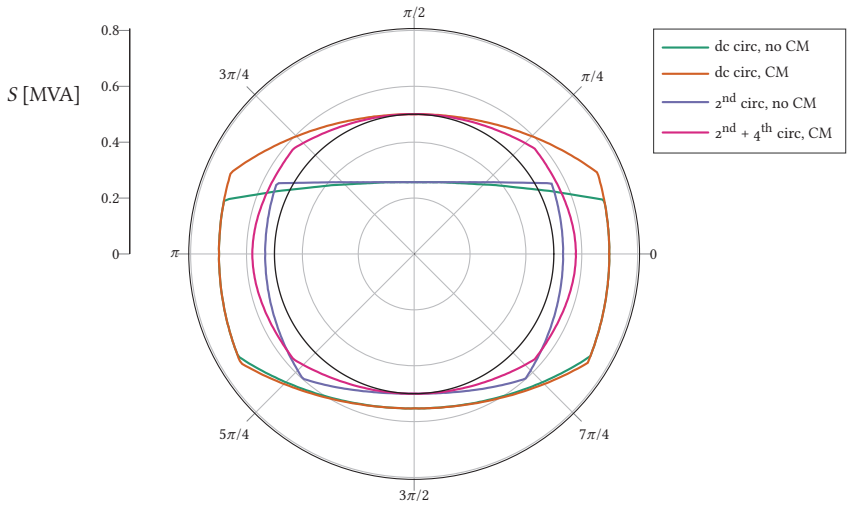


Fig. 3.13 MMC SOAs derived from the power equations without passives. The black circle corresponds to $S = 0.5$ MVA.

Note that the effective SOA is reduced due to the branch impedance voltage drop and ripples in the capacitor voltages and branch currents. Also, margins with respect to transients during step changes will further reduce the real SOA of the converter.

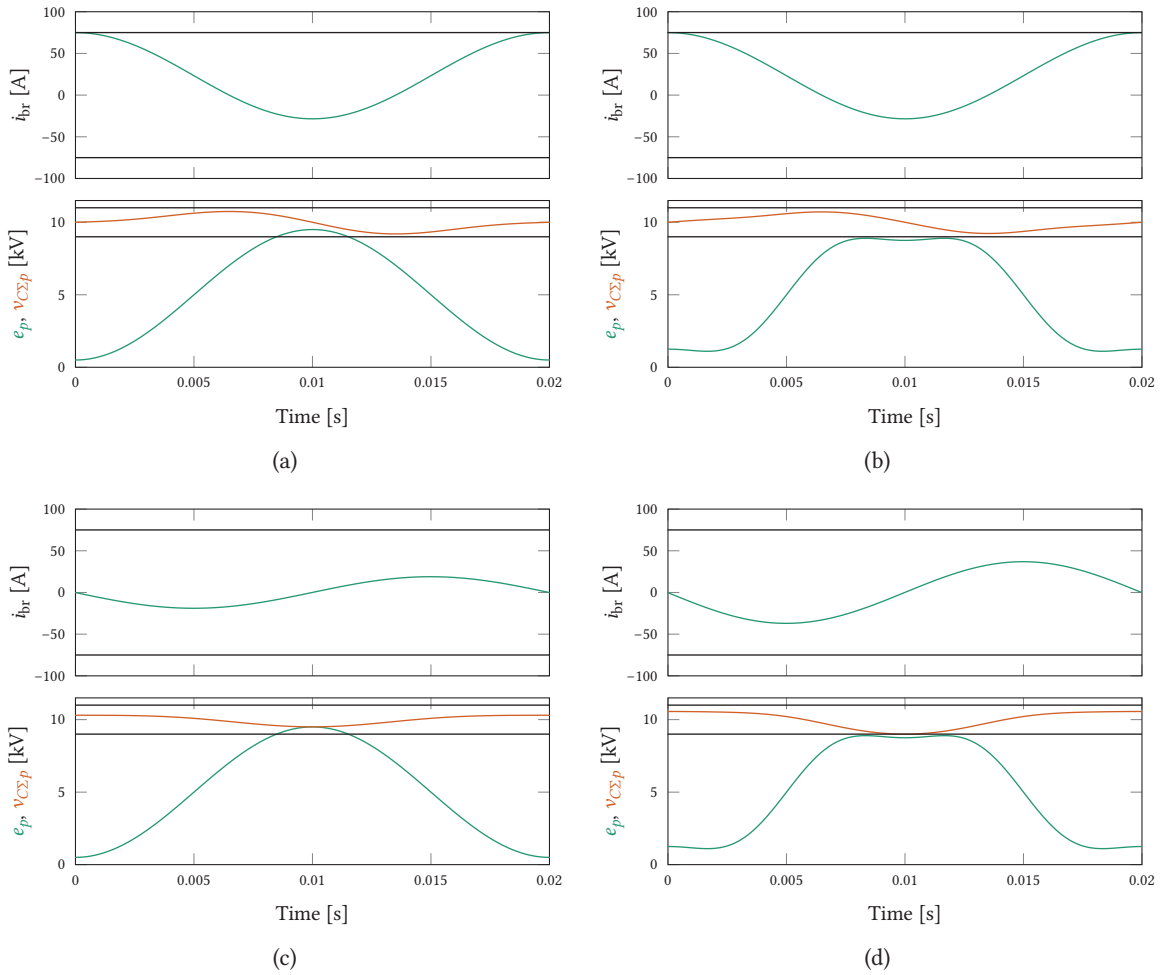


Fig. 3.14 SOA boundary limits: (a) $\phi = 0$, dc circ, no CM, (b) $\phi = 0$, $2^{\text{nd}} + 4^{\text{th}}$ circ, CM, (c) $\phi = \pi/2$, dc circ, no CM and (d) $\phi = \pi/2$, $2^{\text{nd}} + 4^{\text{th}}$ circ, CM. The black lines indicate the branch current and summed capacitor voltage ripple limits, respectively. The active constraint is the branch current in (a) and (b), the modulation index in (c) and the summed branch capacitor voltage ripple in (d).

3.6 Discussion

The reduction of the capacitor voltage ripples through optimization of the circulating current theoretically enables reduced branch capacitance designs. However, this has to be balanced with the fact that the behavior and response under faults or transients, as well as for operation at low apparent branch switching frequency, might not be properly handled by the resulting design, necessitating more conservative designs.

This section has shown that a mathematical solution might not always be found depending on the level of simplification. Consequently, numerical methods with relaxed constraints (such as $p_\Sigma \approx 0$) minimizing the branch current RMS value should be favored. Looking at the problem from a control perspective, there is an interest to embed the circulating current generation within the control algorithm. In that regard, the relevance of an (exact) analytical expression is of little relevance. Instead, a real-time calculation of the circulating current injection is much more attractive. Such

considerations will be addressed in **Sec. 4.2.2.2**.

In all cases, with circulating current injection, the RMS value of the branch current increases and additional terms appear in $v_{C\Sigma}^{\Delta}$. But by lowering the harmonic content in $v_{C\Sigma}^{\Sigma}$, there is a visible impact at the converter terminals, since this will translate into a reduction of the harmonic content in the terminal currents.

4

Modular multilevel converter control methods

Numerous works have focused on the control of the dc/3-ac MMC and its variants. This chapter restrains the analysis to the dc/3-ac MMC (or double-star MMC). A thorough comparison of the control methods performance for a medium voltage converter is carried out in this chapter, highlighting the advantages and drawbacks of each method and eventually summarizing the findings according to a set of predefined criteria.

4.1 Simulation models

Prior to the presentation of the control and modulation methods, appropriate and flexible converter models are required. The control methods will be evaluated with an average MMC model in order to avoid the influence or impact of the choice of the modulation method. The modulation methods will be evaluated with a switched MMC model with the same control method in order to avoid a possible bias in the results, originating from differences in the control method.

The average branch model is inspired from [85], [86]. In this work, quantization effects are neglected, even tough they might not be completely negligible, especially at low average branch switching frequencies / low cell number [87]. The time delays, which play a fundamental role in the limitation of the control gains, are modeled by a pure time delay with a total value T_d. The average branch model is shown in **Fig. 4.1**.

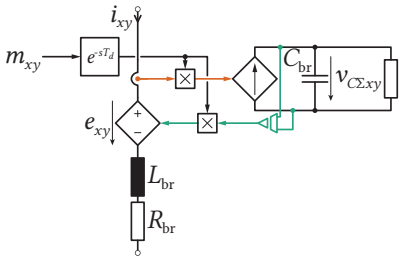


Fig. 4.1 Average branch model considering time delay with $x \in \{a,\ b,\ c\}$ and $y \in \{p,\ n\}$.

For the switched model, it is interesting to avoid a tight dependency with N_{cells}, since it might be relevant to modify it. This can be solved thanks to the vectorization capability of the simulation software. It implies to develop vectorized modulators and sorting algorithms, which will be explained later in **Chap. 5**. The vectorized branch switched model is shown in **Fig. 4.2**. In order to adapt to the communication layout, which might change depending on the choice of the modulation method, the

dimensions of the signals might vary and ranges are provided. Note also that the central and branch controllers might in fact be at the same location.

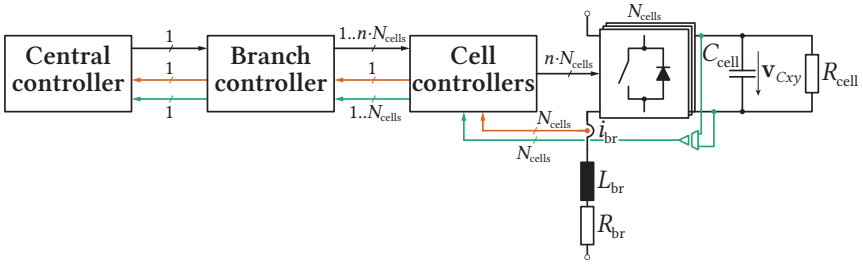


Fig. 4.2 Vectorized branch switched model along with the different control level / entities and signal dimensions.

4.2 Control methods

Numerous control methods for dc/3-ac MMC have been proposed over the years. On one hand, regarding the *external* state variables (ac grid current and dc voltage control), conventional control structures are used, where all the knowledge from VSC control can be applied. On the other hand, the control of the *internal* state variables (capacitor voltages / balancing of energies and circulating currents), specific control algorithms have been developed.

Two operating modes are distinguished, depending on the nature of the source connected on the dc side. In inverter mode (also called current source mode), the dc side voltage is assumed to be stiff (i.e. controlled by another entity), justifying the absence of dc voltage control in the MMC. In rectifier mode (also called voltage source mode), the MMC controls also the dc voltage. Note that these operation modes are not limited to one power flow direction, but depend on the nature of the source / system to which the converter is connected.

Depending on how the sum of branch capacitor voltages is used to define the branch modulation / insertion index, such as whether it is based on measurements or estimated values, the control methods for MMC can be classified.

In this section, the external state variables control will be presented first, followed by the internal state variables control and the control methods regarding the computation of the modulation indices. Then, a comparison of the achievable dynamics, with medium voltage applications in mind, will be performed and the results discussed. This review and performance comparison will be of high importance for the material presented in **Chaps. 6** and **7**, where topological variations of the MMC with integrated branch inductors are presented and evaluated for MVdc applications.

4.2.1 External state variable control

Most of the control concepts applied in this paragraph, unless otherwise specified, can be found in [88], [89]. Rather than simply reviewing them, an extended number of PLECS simulations are developed as the base for a performance evaluation of these various schemes.

4.2.1.1 Power references

The power references are handled in an open-loop fashion. The references are eventually low-pass filtered in order to smoothen the transients (cf. **Fig. 4.3**). Depending on the operating mode, either the active power reference $P^\star$ or the dc voltage $V_B^\star$ in combination with the direct voltage control (DVC) is used. In any case, the reactive power component is kept for any grid ancillary / support feature.

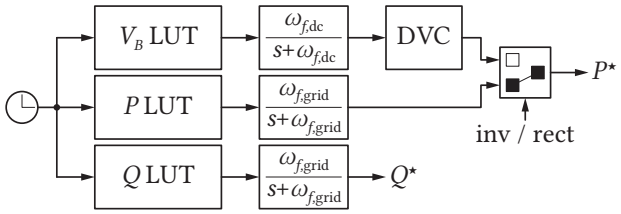


Fig. 4.3 Power references, with a signal selector depending on the operating mode.

Depending on the choice of reference frame for the grid current controller, the grid current references are determined as follows. In dq frame, the following holds[1]:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \frac{3}{2}\begin{bmatrix} v_{gd} & v_{gq} \\ -v_{gq} & v_{gd} \end{bmatrix}\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} \longrightarrow \begin{bmatrix} i_{gd}^\star \\ i_{gq}^\star \end{bmatrix} = \frac{2}{3}\frac{1}{v_{gd}^2 + v_{gq}^2}\begin{bmatrix} v_{gd} & -v_{gq} \\ v_{gq} & v_{gd} \end{bmatrix}\begin{bmatrix} P^\star \\ Q^\star \end{bmatrix} \tag{4.1}$$

Alternatively, since the phase-locked loop (PLL) usually tracks v_{gq} to be zero, the expressions might be simplified to:

$$\begin{bmatrix} i_{gd}^\star \\ i_{gq}^\star \end{bmatrix} = \frac{2}{3\hat{v}_g}\begin{bmatrix} P^\star \\ Q^\star \end{bmatrix} \tag{4.2}$$

with $\hat{v}_g$ the peak magnitude of the grid voltage.

In $\alpha\beta$ frame, the following holds:

$$\begin{bmatrix} P^\star \\ Q^\star \end{bmatrix} = \frac{3}{2}\begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ -v_{g\beta} & v_{g\alpha} \end{bmatrix}\begin{bmatrix} i_{g\alpha}^\star \\ i_{g\beta}^\star \end{bmatrix} \longrightarrow \begin{bmatrix} i_{g\alpha}^\star \\ i_{g\beta}^\star \end{bmatrix} = \frac{2}{3}\frac{1}{v_{g\alpha}^2 + v_{g\beta}^2}\begin{bmatrix} v_{g\alpha} & -v_{g\beta} \\ v_{g\beta} & v_{g\alpha} \end{bmatrix}\begin{bmatrix} P^\star \\ Q^\star \end{bmatrix} \tag{4.3}$$

4.2.1.2 Grid current control

Either proportional integral (PI) in dq-frame(s) or proportional resonant (PR) [90] in $\alpha\beta$-frame are controller structures able to achieve the tracking of ac grid current references with zero steady-state error. The main advantage of PR controllers is their inherent ability to control both positive and negative sequence at the same time, while two different sets of PI controllers in dq frames at $\pm\omega$ are required to achieve the same functionality.

[1] Amplitude invariant coordinate transformations are applied.

PI controller in dq-frame The controller action is formulated as:

$$\mathbf{e}^{\star}_{L,dq} = \underbrace{\left(K_{p,\mathrm{gcc}} + \frac{K_{i,\mathrm{gcc}}}{s}\right)}_{G_{\mathrm{PI}}(s)}(\mathbf{i}^{\star}_{g,dq} - \mathbf{i}_{g,dq}) + j\omega\left(L_g + L_{\mathrm{br}}/2\right)\mathbf{i}_{g,dq} + F(s)\mathbf{v}_{g,dq} \tag{4.4}$$

where

$$K_{p,\mathrm{gcc}} = \alpha_{\mathrm{gcc}}\left(L_g + L_{\mathrm{br}}/2\right) = \alpha_{\mathrm{gcc}}L_{\mathrm{eq}} \qquad K_{i,\mathrm{gcc}} = \alpha_{\mathrm{gcc}}\left(R_g + R_{\mathrm{br}}/2 + R_a\right) = \alpha_{\mathrm{gcc}}(R_{\mathrm{eq}} + R_a) \tag{4.5}$$

with R_a the active damping term and $F(s)$ an (optional) low-pass filter to remove harmonics in $\mathbf{v}_{g,dq}$. Its scheme is shown in **Fig. 4.4**.

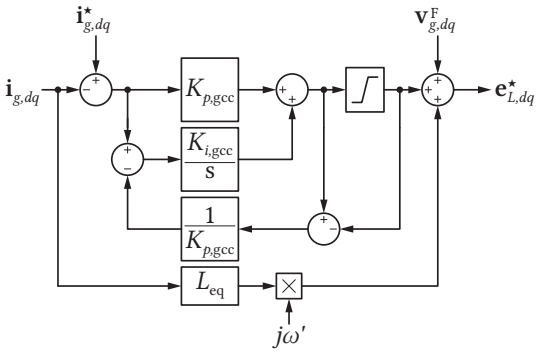


Fig. 4.4 Grid current control in dq frame with saturation and anti-windup (for the positive sequence). The coordinate transformations are omitted. The time delay compensation is performed on the $dq \rightarrow abc$ transformation on $\mathbf{e}^{\star}_{L,dq}$ with the addition of ϕ' to the grid angle θ' (phase advance).

The controller bandwidth is selected such that:

$$\alpha_{\mathrm{gcc}} \leq \begin{cases} 0.1\omega_s & \text{if } R_a = 0 \\ 0.04\omega_s & \text{if } R_a = \alpha_{\mathrm{gcc}}L_{\mathrm{eq}} - R_{\mathrm{eq}} \end{cases} \tag{4.6}$$

with ω_s the sampling frequency.

PR controller in $\alpha\beta$-frame The controller action is formulated as:

$$\mathbf{e}^{\star}_{L,\alpha\beta} = \underbrace{\left(K_{p,\mathrm{gcc}} + K_{h,\mathrm{gcc}}\frac{s\cos(\phi'_h) - h\omega_1\sin(\phi'_h)}{s^2 + (h\omega_1)^2}\right)}_{G_{\mathrm{PR}}(s)}\left(\mathbf{i}^{\star}_{g,\alpha\beta} - \mathbf{i}_{g,\alpha\beta}\right) + F(s)\mathbf{v}_{g,\alpha\beta} \tag{4.7}$$

where $\phi'_h = h\omega_1 T_d$ (with usually $T_d = 1.5T_s$ for PWM and computation delays) and h the harmonic order. The selection of the controller gains follows:

$$K_{p,\mathrm{gcc}} = \alpha_{\mathrm{gcc}}\left(L_g + L_{\mathrm{br}}/2\right) \qquad K_{h,\mathrm{gcc}} = 2\alpha_{h,\mathrm{gcc}}K_{p,\mathrm{gcc}} \tag{4.8}$$

Its block diagram is shown in **Fig. 4.5** and its implementation in **Fig. 4.6**.

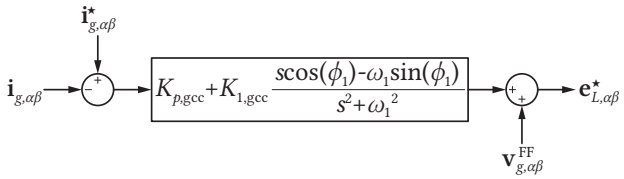


Fig. 4.5 Grid current control in $\alpha\beta$ frame. The coordinate transformations are omitted. The time delay compensation is performed with a lead-lag by setting ϕ_h' to a non-zero value. Note that a phase advance is added on the feed-forward term ($\mathbf{v}^{\mathrm{FF}}_{g,\alpha\beta}$), which plays an important role at grid synchronization.

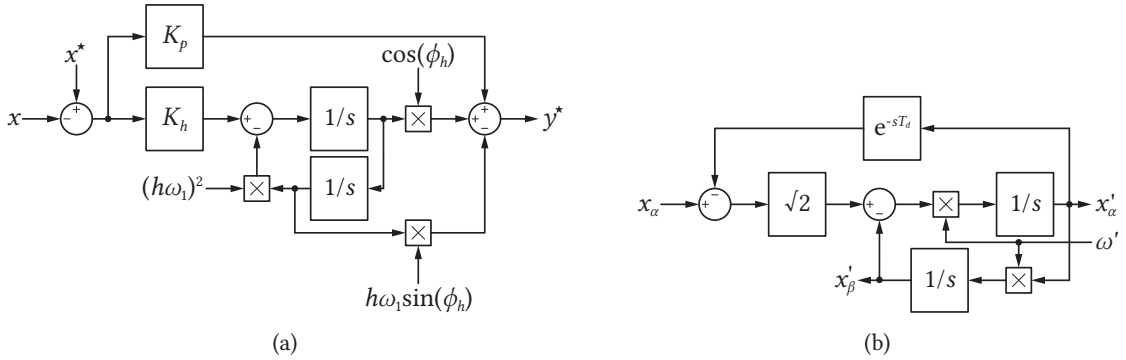


Fig. 4.6 Implementation details: (a) frequency adaptive PR controller with time delay compensation and (b) phase-advance in $\mathbf{v}^{\mathrm{FF}}_{g,\alpha\beta}$ with delayed feedback in second-order generalized integrator (SOGI).

4.2.1.3 Phase-locked loop

The role of the PLL is to achieve a tracking of the grid angle and retrieve the grid frequency. A standard dq-PLL is used, in combination with an optional low-pass filter to get rid of undesired harmonics (i.e. ac part of the dq signals), as shown in **Fig. 4.7**. There is a trade-off between the filter cut-off frequency and the PLL dynamics. An integral part in the PLL is required in order to properly drive the grid angle error to zero after a frequency variation. The PLL is at least one decade slower than the grid current control loop.

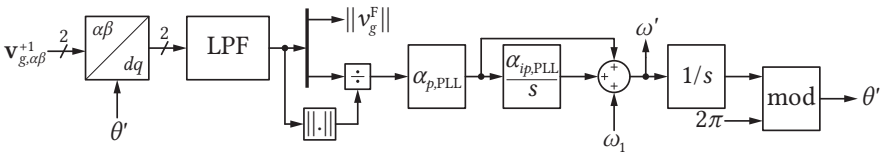


Fig. 4.7 PLL in dq frame, with optional low-pass filter on the dq signals, and amplitude normalization in order to maintain the same dynamics regardless of the magnitude of the grid voltage. ω' and θ' are the estimated signals provided by the PLL. ω_1 is only there to reduce the pull-up time at the startup.

The handling of faults and unbalances (i.e. non-zero negative-sequence component) is performed with a special decoupling network (double decoupled synchronous reference frame (DDSRF) [91] or double second-order generalized integrator (DSOGI) [92]), whose structures are shown in **Fig. 4.8**. The cancellation of harmonics is inherent of the structures, since there is a low-pass filter in the path for the DDSRF, and through the adaptive filtering structure of SOGI. Consequently, the low-pass filter in the dq-PLL is discarded.

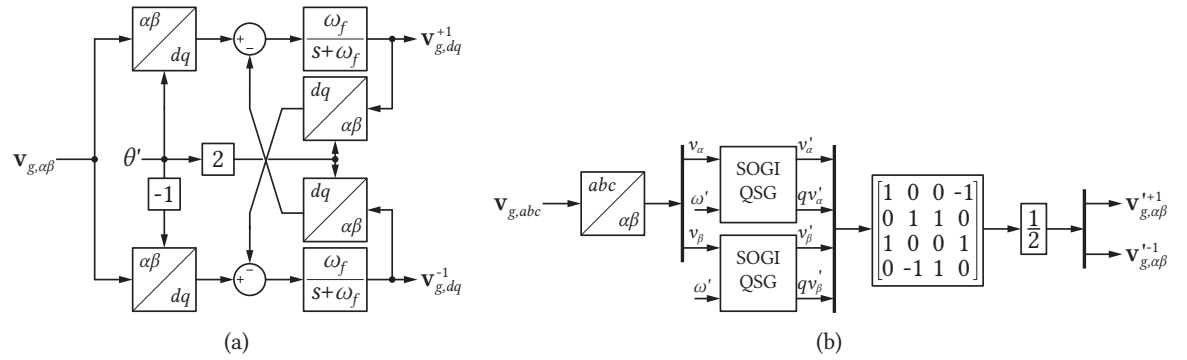


Fig. 4.8 Positive- and negative-sequence components identification schemes: (a) DDSRF, where θ' is the angle provided by the PLL and (b) DSOGI, where ω' is the grid frequency provided by the PLL. QSG stands for quadrature signal generator. Identical dynamics between DDSRF and DSOGI are obtained if $\omega_f = \omega_1/\sqrt{2}$, however the former depends on θ', which exhibits higher dynamics during faults than ω' [93].

4.2.1.4 Dc voltage control

A dc voltage controller is only present in rectifier mode, where the converter is normally expected to regulate the dc voltage. It is preferred to control the dc energy rather than the dc voltage in order to avoid dependency with the dc voltage magnitude [94]. A low-pass filter is added on the measurement to avoid transferring undesired harmonics to the ac grid, which would lead to oscillations in the active power. The DVC scheme is illustrated in **Fig. 4.9**.

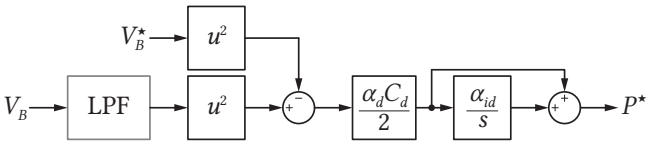


Fig. 4.9 DVC implementation.

4.2.2 Internal state variable control

4.2.2.1 Energy controllers

The energy balancing is a control action that ensures an equal distribution of the average stored energy within the converter, i.e. that the energies among the branches are similar [95]. Two mechanisms are present: (i) horizontal balancing and (ii) vertical balancing. Their control implementation has been widely discussed in the literature: in [96], the horizontal balancing is performed in $dq0$ frame at twice the grid frequency, in [97], the energies are controlled in $\alpha\beta0$ coordinates with PI controllers. The balancing action shall not be visible at any converter terminal, i.e. the balancing process remains unseen from outside the converter.

Horizontal balancing The horizontal balancing ensures an equal partition of the average stored energy among the three phase-legs. It modifies the sharing of the dc current among the phase-legs and interacts with the dc part of the branch voltages, which appears with the same sign for both

the positive and negative branch, leading to identical energy variation for both branches within the same phase-leg. The lowest possible value for $v_{C\Sigma 0}^{\Sigma}$ is given in (3.17a), since for a dc/3-ac MMC it is assumed that there is a sufficient voltage margin between the dc terminal voltage and maximum ac peak-to-peak voltage. However, in such a case there is no margin against dc overvoltages. For control purpose and transients handling, there are incentives to increase $v_{C\Sigma 0}^{\Sigma\star}$. Still, its value shall not be increased too much, since efficiency constraints (higher $v_{C\Sigma 0}^{\Sigma\star}$ implies higher switching losses) and limitations from the hardware capability (maximum cell voltage) have to be accounted for. The horizontal balancing scheme is presented in **Fig. 4.10**, where $\alpha\beta 0$ frame is selected. The zero-sequence component corresponds to the total energy control, while the $\alpha\beta$ ones correspond to the energy imbalance between the phase-legs. Hence, the reference for the $\alpha\beta$ components is $[0;\ 0]$.

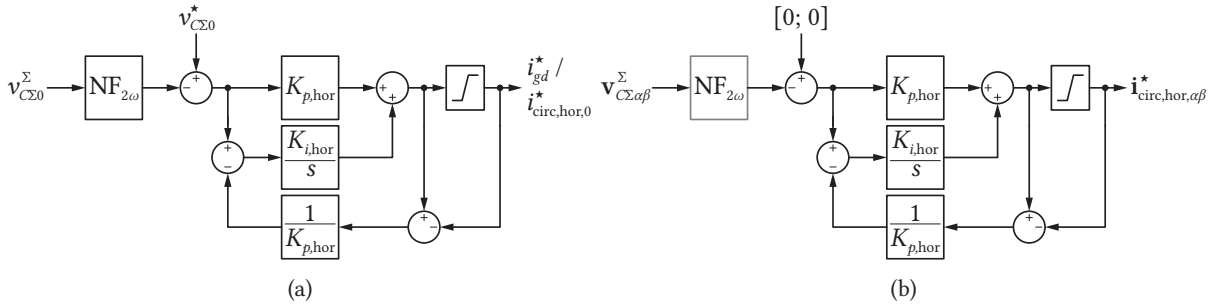


Fig. 4.10 Horizontal balancing in $\alpha\beta 0$ frame: (a) zero sequence component corresponding to the total energy control (with recommended notch filter especially in the case of grid faults/imbalances) and (b) $\alpha\beta$ components corresponding to the phase-leg imbalances (with optional notch filter). In inverter mode, the zero-sequence reference is fed to the circulating current controller, while in rectifier mode it is fed to the grid current controller.

Vertical balancing The vertical balancing ensures an equal distribution of the stored energy between the positive and negative branch of the same phase-leg. It introduces an ac component at fundamental frequency that interacts with the ac component of the branch voltage. Power shifting between the positive and negative branch is achieved due to opposite signs of the grid voltage component in the branch voltage. In normal operation, different energy levels between the positive and negative branch are not desired. Hence the reference is set to $[0;\ 0;\ 0]$. The notch filters at fundamental frequency ensure that the controller outputs do not feature fundamental frequency components. This permits the cancellation at the dc terminals of the circulating currents, which is achieved by inducing reactive power flows in the other two phase-legs using the orthogonality principle in the matrix $\mathbb{M}$ [98].

$$\mathbb{M} = \begin{bmatrix} \cos(\theta_L) & \frac{-\sin(\theta_L)}{\sqrt{3}} & \frac{\sin(\theta_L)}{\sqrt{3}} \\ \frac{\sin(\theta_L - 2\pi/3)}{\sqrt{3}} & \cos(\theta_L - 2\pi/3) & \frac{-\sin(\theta_L - 2\pi/3)}{\sqrt{3}} \\ \frac{-\sin(\theta_L + 2\pi/3)}{\sqrt{3}} & \frac{\sin(\theta_L + 2\pi/3)}{\sqrt{3}} & \cos(\theta_L + 2\pi/3) \end{bmatrix} \tag{4.9}$$

where θ_L is the angle of $\mathbf{e}_L^{\star}$. The vertical balancing control scheme is presented in **Fig. 4.11**. The meaning of the matrix $\mathbb{M}$ is illustrated in **Fig. 4.12**.

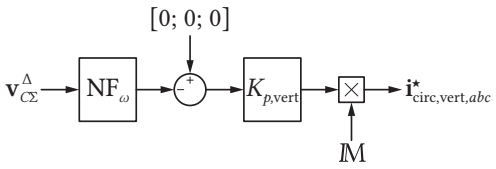


Fig. 4.11 Vertical balancing in abc frame, with notch filter at fundamental frequency and $\mathbb{M}$ the matrix that creates reactive power flows in the neighbouring phase-legs when a non-zero circulating current for vertical balancing is required in one phase-leg.

Fig. 4.12 Reactive currents creation to achieve cancellation on the bus: (a) positive case and (b) negative case of a required action for the vertical balancing in phase-leg a. The quadrature in phase-legs b and c is clearly visible.

Remark The notch filters are implemented with a SOGI structure (cf. **Fig. 4.13**), since the transfer function

$$G_{\mathrm{SOGI}}(s) = \frac{x'(s)}{x(s)} = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \tag{4.10}$$

is a frequency adaptive bandpass filter. The quadrature signal qx' is discarded and of no use.

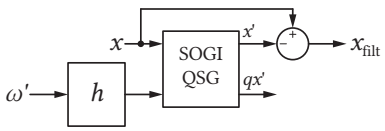


Fig. 4.13 Frequency adaptive notch filter based on SOGI.

4.2.2.2 Circulating current control

While the control of the circulating currents was not considered in a first place (with very low L_{br}), it has become clear that for larger values of L_{br}, also to better control the harmonic content of the branch current and eventually the branch energies, the use of a circulating current controller would be beneficial / mandatory.

The circulating current is known to naturally feature in steady-state even harmonics (especially 2^{nd} and 4^{th}) due to the capacitor voltages mismatch between the positive and negative branch and odd harmonics during transients for the re-balancing of the branch energies (vertical balancing). Consequently, the circulating current controller, in its minimum configuration, should aim at suppressing

the undesired harmonics in the circulating current. This is what the circulating current suppression controller (CCSC) initially proposed in [99] aims at. The circulating currents were transformed in a dq frame rotating at $-2\omega_1$ (negative sequence). Further improvements can be achieved by increasing the number of harmonic components controlled (such as the 4^{th} one) [100].

Alternatively, the circulating currents are transformed in $\alpha\beta$ frame (the zero sequence responsible for power exchange with the dc terminals is left uncontrolled) and controlled with multiple PR controllers (on 2^{nd} and 4^{th} harmonic for good results), as shown in **Fig. 4.14**.

For any control method that doesn't rely on energy or voltage controllers, the odd harmonics (especially the fundamental) of the circulating current is left uncontrolled, else the re-balancing and long term stability would be compromised. For closed-loop modulation, where energy controllers are present, a control of the fundamental circulating current is added for improved vertical balancing performance.

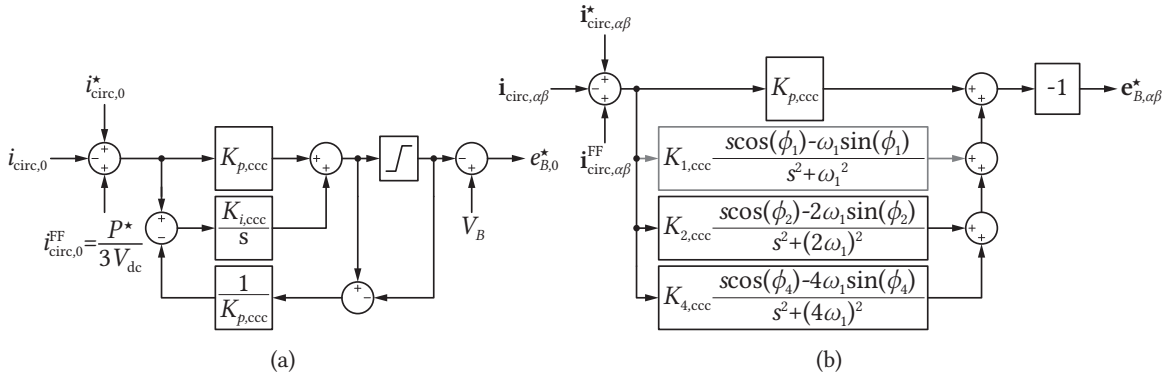
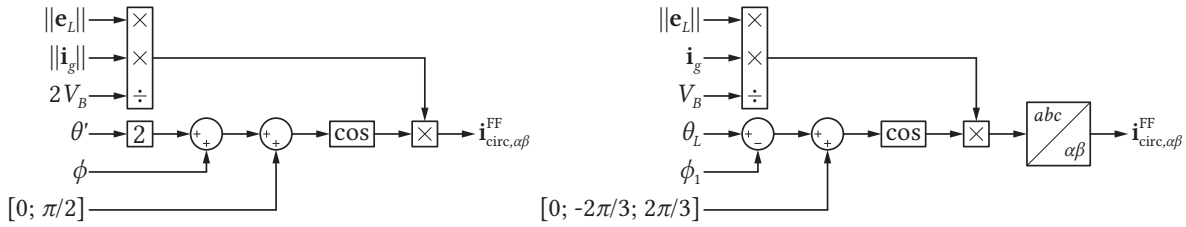


Fig. 4.14 Circulating current control in $\alpha\beta 0$ frame, with dc, fundamental, 2^{nd} and 4^{th} harmonics tracking and active power feed-forward, which provides better dc side dynamics in inverter mode. (a) shows the control scheme for the zero-sequence component, while (b) the scheme for the $\alpha\beta$ components. $\mathbf{i}^{\text{FF}}_{\text{circ},\alpha\beta}$ is used for capacitor voltage ripple reduction by injecting appropriate harmonics in the circulating current. Note that the fundamental harmonic tracking is turned-off for any modulation method apart closed-loop modulation, since uncontrolled fundamental circulating currents are introduced to naturally achieve vertical balancing.

It is generally desired to use a filtered active power feed-forward ($i^{\text{FF}}_{\text{circ},0} = P^{\star\text{F}}/(3V_{\text{dc}})$ or just the instantaneous active power ($i^{\text{FF}}_{\text{circ},0} = P/(3V_{\text{dc}})$ in case the grid current control is slow. An optional second harmonic circulating current ($\mathbf{i}^{\text{FF}}_{\text{circ},\alpha\beta}$) is added with the scheme of **Fig. 4.15**. There, despite only considering a 2^{nd} harmonic component, the ripple reduction is still achieved ($v^{\Sigma}_{C\Sigma}$ tends to a dc value).

4.2.3 Common mode injection methods

The extension / maximization of the dc bus utilization of a converter through zero-sequence (CM) signal is interesting if the application permits CM voltage. This is achieved by modifying the zero space vector distribution, as it does not change the output converter flux in $\alpha\beta$ frame. Several methods have been proposed in the literature, and the discussion is restricted to the three methods for continuous modulation: (i) third harmonic injection, (ii) min/max injection [83] and (iii) flat-top modulation [84]. In all cases, the maximum modulation index is $2/\sqrt{3}$, which corresponds to an increase by 15.5 %



x

Fig. 4.15 Second harmonic circulating current injection (negative sequence) for capacitor voltage ripple reduction: (a) implementation that only considers the $\alpha\beta$ components, where $\phi = \text{atan}(Q^\star/P^\star)$, and (b) instantaneous power mode in [72] where the zero sequence component is discarded (usually the active power feed-forward is faster). Note that there shouldn't be any phase advance in the feed-forward term, hence $\phi_1 = \omega_1 T_d$ is subtracted to $\theta_L = \text{atan}\left(e^\star_{L,\beta}/e^\star_{L,\alpha}\right)$.

compared to the sinusoidal modulation. The flat-top common mode injection method is optimal, as the modulation index is $m\sqrt{3}/2$ at its peak, hence the CM signal amplitude is minimal. The obtained waveforms at the edge of continuous modulation are presented in **Fig. 4.16**.

$$m_{\text{CM},3^{\text{rd}}} = -\frac{m}{6}\cos(3\omega t) \tag{4.11a}$$

$$m_{\text{CM,min/max}} = -\frac{\max(m_a^\star, m_b^\star, m_c^\star) + \min(m_a^\star, m_b^\star, m_c^\star)}{2} \tag{4.11b}$$

$$m_{\text{CM,flattop}} = -\sum_{i=a}^{c} \max\left\{\min\left\{m_i^\star, m\sqrt{3}/2\right\}, -m\sqrt{3}/2\right\} \tag{4.11c}$$

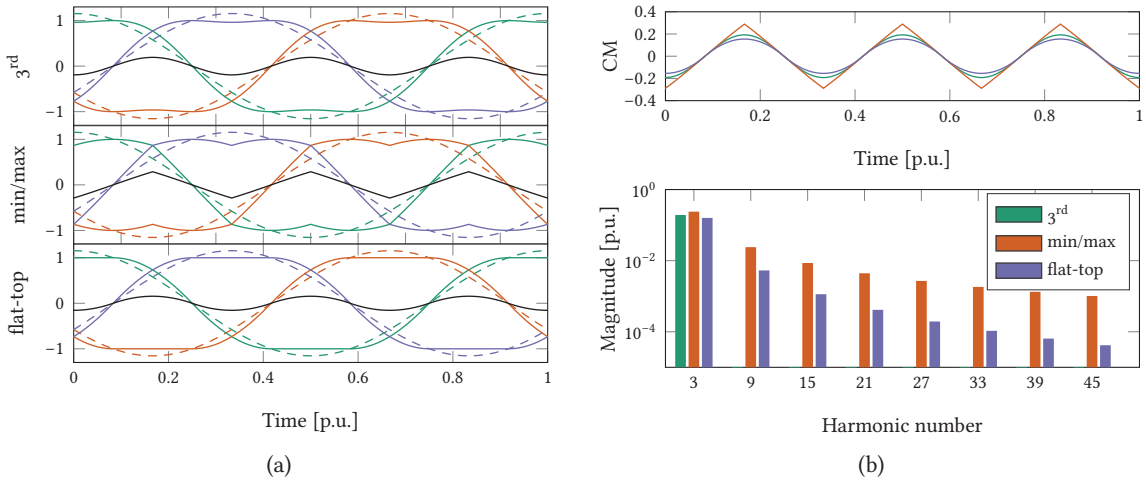


Fig. 4.16 Common mode injection methods for $m = 2/\sqrt{3}$: (a) modulation index waveforms (fundamental in dashed lines, common-mode in black) and (b) normalized harmonic distribution. The flat-top modulation features the lowest peak-to-peak common mode voltage and the magnitude of the harmonics decays faster compared to the min/max method.

4.2.4 Modulation index calculation

Normally, as in any converter, the modulation indices are computed with respect to the (measured) summed branch capacitor voltages. It allows one to compensate for the eventual low order harmonics. However, in the case of MMC, it was found that there might be some advantages offered by not using the measured summed branch capacitor voltages as is, i.e. by replacing the measurements by desired, estimated or filtered values. For these cases, no energy controllers are required. In order to allow the branch energies to re-balance, the circulating current control (CCC) shouldn't include an integrator on the dc component, nor a resonant part on the fundamental frequency.

The calculation of the modulation indices is done according to **Fig. 4.17**, where the matrix $\mathbb{T}$ is expanded from (3.8).

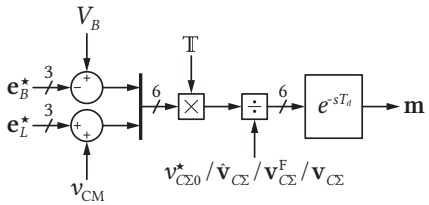


Fig. 4.17 Modulation indices calculation, where the term in the division is adapted depending on the modulation method.

A thorough comparison of the achievable dynamic and harmonic performances is presented in the next section, just after the presentation of their expressions.

Direct modulation The capacitor voltages / branch energy are not controlled, since they're re-balancing themselves. A formal proof regarding the self-balancing was presented in [101]. The branch modulation indices are calculated from their desired (dc) average value:

$$\mathbf{m}_p = \frac{V_{\mathrm{dc}}/2 - \mathbf{e}_B^\star/2 - \mathbf{e}_L^\star}{v_{C\Sigma 0}^\star} \tag{4.12a}$$

$$\mathbf{m}_n = \frac{V_{\mathrm{dc}}/2 - \mathbf{e}_B^\star/2 + \mathbf{e}_L^\star}{v_{C\Sigma 0}^\star} \tag{4.12b}$$

where $v_{C\Sigma 0}^\star = v_{C\Sigma 0}^{\Sigma\star}/2$. As a consequence, since the required control action for the circulating current control is assumed to be small (in steady-state), the modulation indices are almost only constructed from the phase voltage component.

Open-loop control The open-loop control was proposed in [102] as an improvement of the direct modulation. The motivation was double: (i) to reduce the delays associated with the retrieval of the summed branch capacitor voltages and (ii) to lower the number of exchanged data between the cells and the central controller. The common denominator from the direct modulation is replaced with the branch capacitor voltage estimates (denoted with $\hat{\cdot}$ hereafter). Therefore, the ripples are captured effectively in steady-state, which is beneficial for harmonics rejection. The branch modulation indices

are calculated as:

$$\mathbf{m}_p = \frac{V_{\mathrm{dc}}/2 - \mathbf{e}_B^\star/2 - \mathbf{e}_L^\star}{\hat{\mathbf{v}}_{C\Sigma p}} \tag{4.13a}$$

$$\mathbf{m}_n = \frac{V_{\mathrm{dc}}/2 - \mathbf{e}_B^\star/2 + \mathbf{e}_L^\star}{\hat{\mathbf{v}}_{C\Sigma n}} \tag{4.13b}$$

where $\hat{\mathbf{v}}_{C\Sigma p}$ and $\hat{\mathbf{v}}_{C\Sigma n}$ are obtained from **Fig. 4.18**. The band-pass filters are implemented with a low frequency selectivity with $\alpha_f = 50$ rad/s (similar to the PLL bandwidth), as it can be seen in cf. **Fig. 4.19**. Consequently, the filters are not dependent on the frequency retrieved from the PLL, but simply from the center grid frequency ω_1.

$$\mathrm{BPF}_h(s) = \frac{\alpha_f s}{s^2 + \alpha_f s + (h\omega_1)^2} \tag{4.14}$$

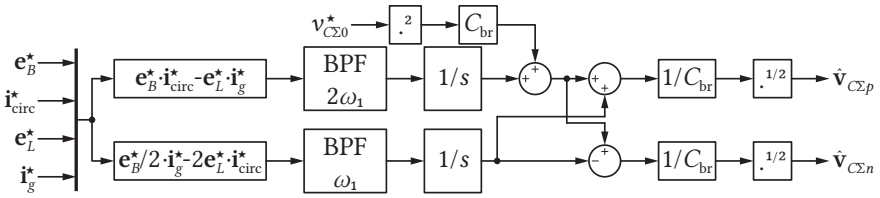


Fig. 4.18 Open-loop modulation: estimation of the sum of capacitor voltages. Note the scaling of $\mathbf{e}_B^\star$ due to different definition. The time-delay compensation is inherently achieved if the reference signals are properly handling delay compensation.

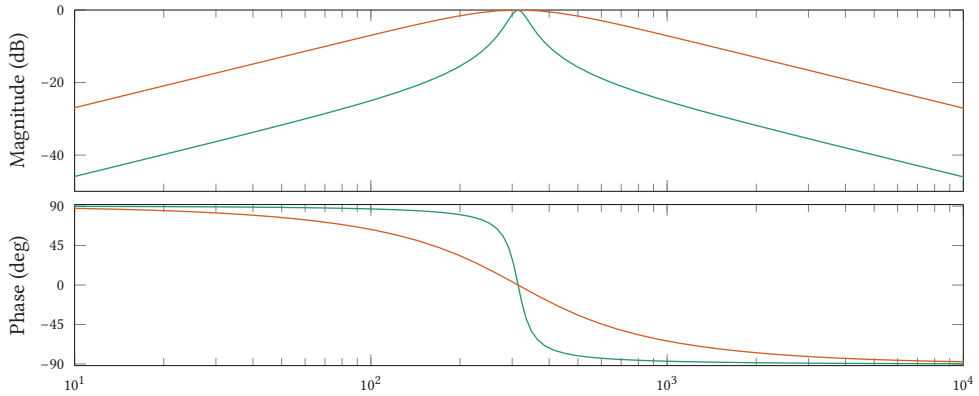


Fig. 4.19 Band-pass filter with low selectivity (in red) compared to a regular SOGI tuning with $k = \sqrt{2}$, center frequency at 100π rad/s (in green).

The formal asymptotic stability was proven in [103]. Note that in this case an active damping contribution for the circulating current control was added, hence the approach is not fully open-loop anymore.

Hybrid voltage control Instead of the summed capacitor voltages estimates, the voltage ripples are retrieved from the measurements, while the dc part is selected the same way as for the direct modulation ($\mathbf{v}^{\mathrm{F}}_{C\Sigma p/n} = V^\star_{C\Sigma 0} + \tilde{\mathbf{v}}_{C\Sigma p/n}$). It is a compromise between the direct modulation and open-loop

control, since it enables the rejection of harmonics at the terminals and achieves asymptotic stability (proven in [104]). Since the measurements are used as an input in **Fig. 4.20**, delay compensation has to be implemented in the filters.

$$\mathbf{m}_p = \frac{V_{\mathrm{dc}}/2 - \mathbf{e}_B^\star/2 - \mathbf{e}_L^\star}{\mathbf{v}_{C\Sigma p}^{\mathrm{F}}} \tag{4.15a}$$

$$\mathbf{m}_n = \frac{V_{\mathrm{dc}}/2 - \mathbf{e}_B^\star/2 + \mathbf{e}_L^\star}{\mathbf{v}_{C\Sigma n}^{\mathrm{F}}} \tag{4.15b}$$

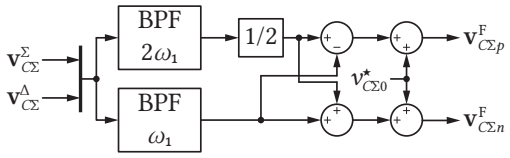


Fig. 4.20 Hybrid modulation.

Closed-loop control The modulation indices are computed with respect to the actual (measured) summed branch capacitor voltages, which have to be communicated to the central controller.

$$\mathbf{m}_p = \frac{V_{\mathrm{dc}}/2 - \mathbf{e}_B^\star/2 - \mathbf{e}_L^\star}{\mathbf{v}_{C\Sigma p}} \tag{4.16a}$$

$$\mathbf{m}_n = \frac{V_{\mathrm{dc}}/2 - \mathbf{e}_B^\star/2 + \mathbf{e}_L^\star}{\mathbf{v}_{C\Sigma n}} \tag{4.16b}$$

4.3 Control method benchmark

A fair comparison between the different modulation index calculation methods is performed with identical controller tunings. The system and control parameters are given in **Tab. 4.1** and **Tab. 4.2**, respectively. A strong ac grid is considered (infinite short-circuit ratio (SCR)). In case of weak grids (SCR < 10), the voltage at the point of common coupling (PCC) should be controlled (closed-loop reactive power control). Such a case was not considered relevant regarding the objectives of the comparison, since the control of external state variables is of less importance. The key parameters or indicators for the comparison are: the power transient dynamics, harmonic content and capacitor voltage bounds violation (set to ±10 % of their reference value, which is in the end quite similar to knowing whether discontinuous modulation is hit or not). The two converter modes, inverter mode (or current source mode from the dc side) and rectifier mode (or voltage source mode from the dc side), are analyzed separately.

4.3.1 Inverter mode

When an MMC is used as an inverter, the dc voltage is assumed to be stiff (normally regulated by some other entity), as illustrated in **Fig. 4.21**. The full control scheme is shown in **Fig. 4.22**.

Tab. 4.1 System parameters.

Parameter	Value
V_{dc}	10 kV
$f_{\mathrm{sw,app}}$	5 kHz
T_d	$1.5/f_{\mathrm{sw,app}}$
L_{br}	2.5 mH
R_{br}	0.1 Ω
C_{br}	118.75 µF
$\hat{v}_g$	4.25 kV
f_g	50 Hz
L_g	0 H
R_g	0 Ω

Tab. 4.2 Controller parameters.

Controller	Parameter	Value
PLL	$\alpha_{p,\mathrm{PLL}}$	50 rad/s
	$\alpha_{ip,\mathrm{PLL}}$	10 rad/s
GCC	α_{GCC}	$2\pi f_{\mathrm{sw,app}}/10$
	$\alpha_{h,\mathrm{GCC}}$	200 rad/s
CCC	α_{CCC}	$\alpha_{\mathrm{GCC}}/2$
	$\alpha_{h,\mathrm{CCC}}$	100 rad/s
DVC	α_d	50 rad/s
	α_{id}	25 rad/s
ΣVC	α_{hor}	$\alpha_{\mathrm{CCC}}/10$
	$\alpha_{h,\mathrm{hor}}$	1 rad/s
ΔVC	α_{vert}	$\alpha_{\mathrm{CCC}}/10$
LPF	$\alpha_{v^\star_{C\Sigma 0}}$	20 rad/s
BPF	α_f	50 rad/s

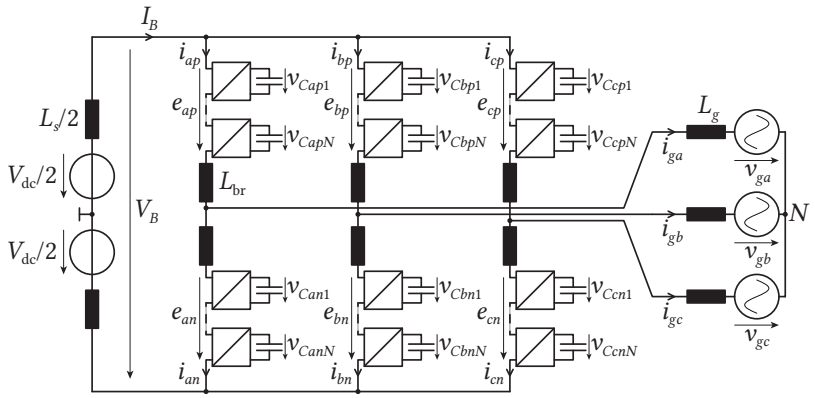


Fig. 4.21 MMC for inverter mode.

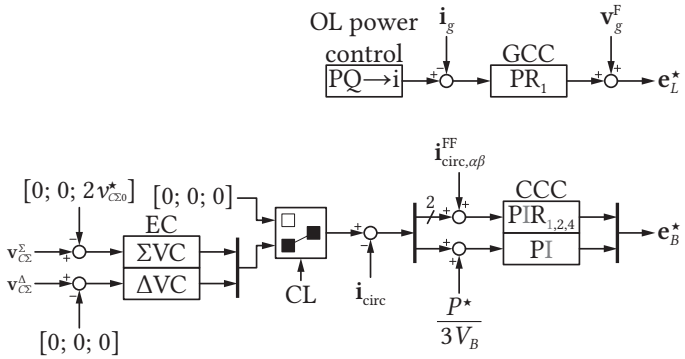


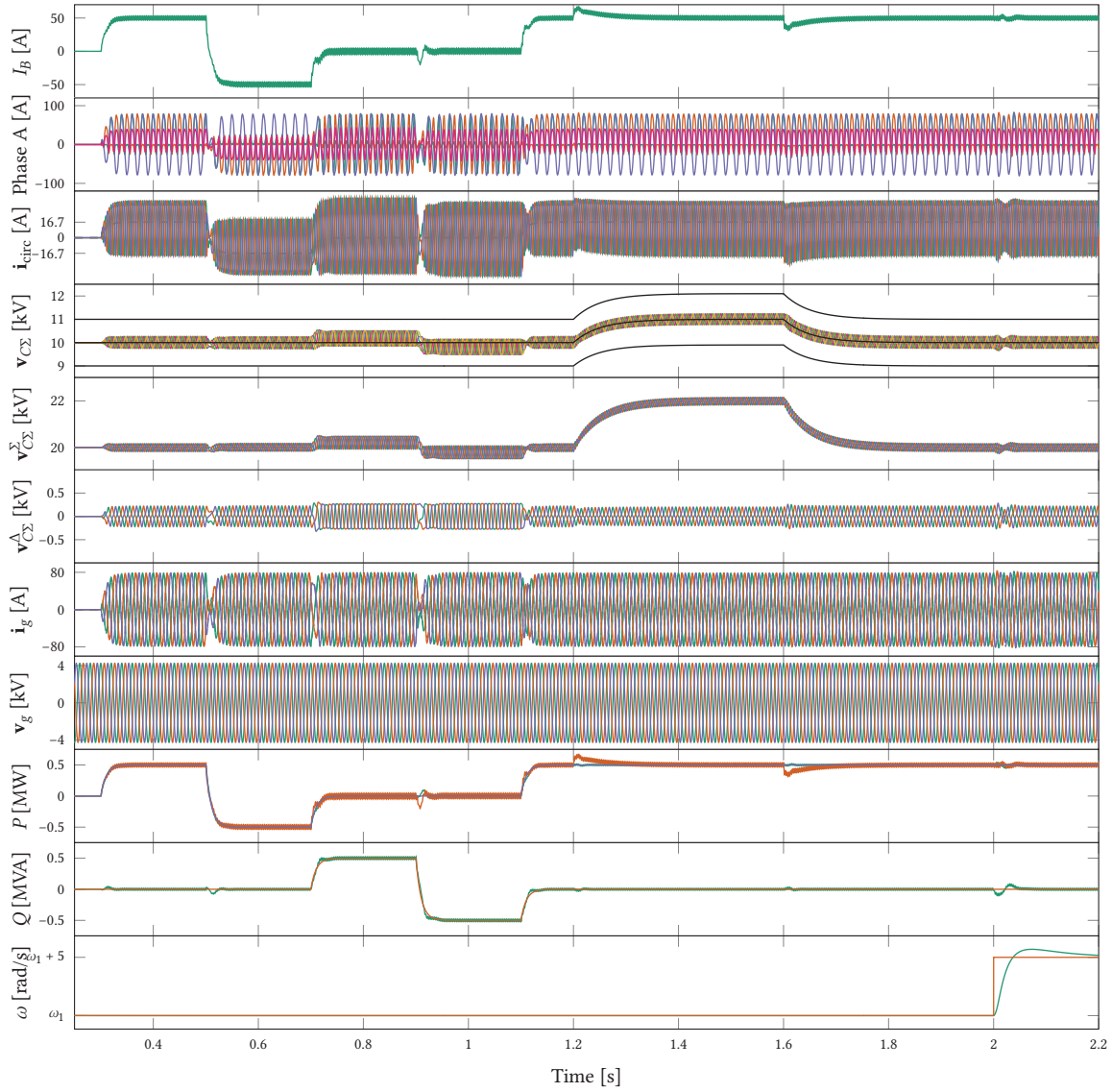
Fig. 4.22 Overall control scheme in inverter mode. EC stands for energy control, CCC for circulating current control, OL for open-loop and GCC for grid current control. CL is the signal switch that depends whether the closed-loop control is used or not.

Six cases are compared. The configurations are summarized in **Tab. 4.3**. Regarding the color scheme

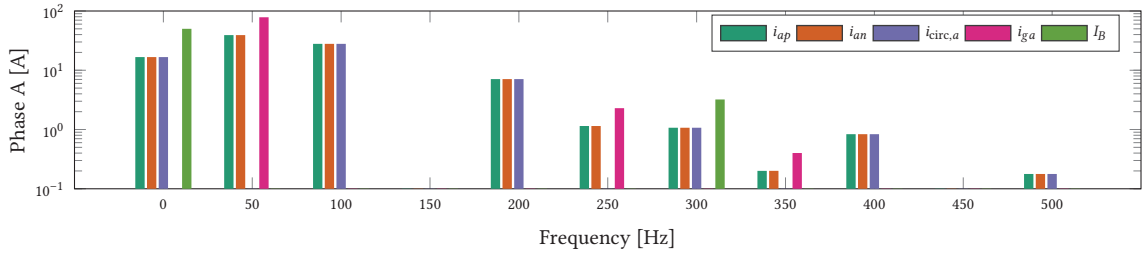
for the phase A current plots, i_{ap}, i_{an}, i_{ga} and $i_{\text{circ},a}$.

Tab. 4.3 Control method comparison configurations in inverter mode. A filled dot corresponds to the presence of a CCC, CM voltage or 2nd harmonic circulating current injection, and the absence for an unfilled one.

Case #	Control method	CCC	CM	2nd harmonic	Figure
1	Direct modulation	○	○	○	**Fig. 4.23**
2	Direct modulation	●	○	○	**Fig. 4.24**
3	Direct modulation	●	○	●	**Fig. 4.25**
4	Open-loop control	●	○	○	**Fig. 4.26**
5	Hybrid voltage control	●	○	○	**Fig. 4.27**
6	Closed-loop control	●	○	○	**Fig. 4.28**

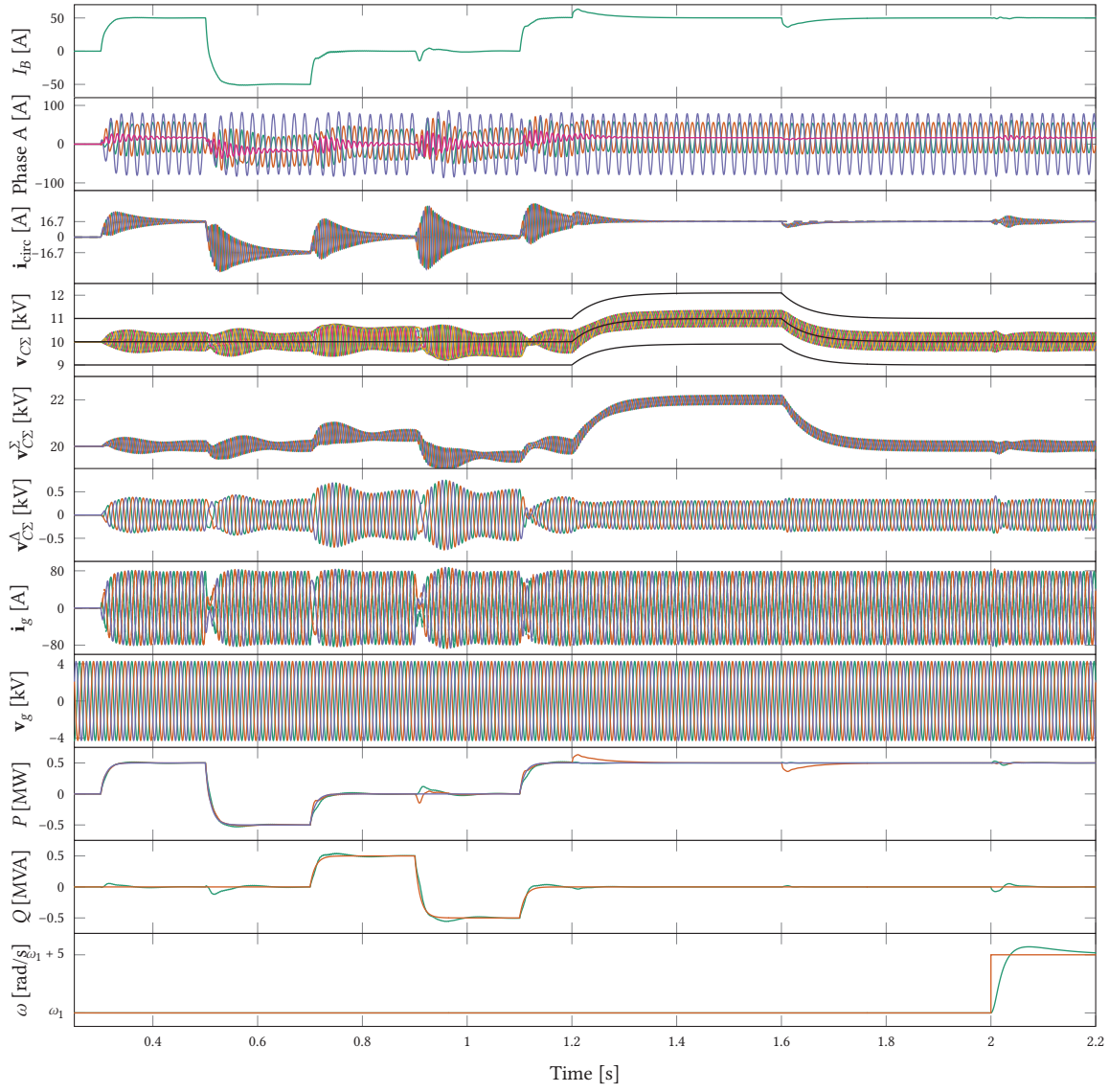


(a)

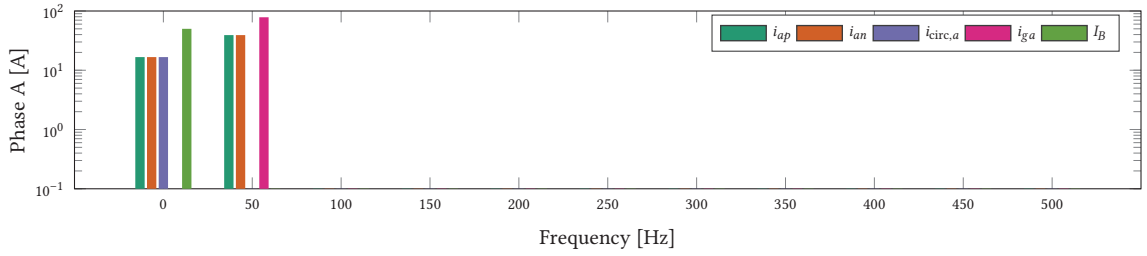


(b)

Fig. 4.23 Case 1 inverter mode: (a) time domain waveforms and (b) FFT in a 2 periods window between 1.9 and 1.94 s. Low order harmonics are present in the bus current (6^{th}) and grid currents (5^{th} and 7^{th}), since the capacitor voltage ripples are not compensated for. On the other end, the capacitor voltage ripples are very low. During Q steps, i.e. for $t \in [0.7,\ 1.1]$ s, $v^{\Sigma}_{C\Sigma 0}$ settles to a different value than $v^{\Sigma\star}_{C\Sigma 0}$.

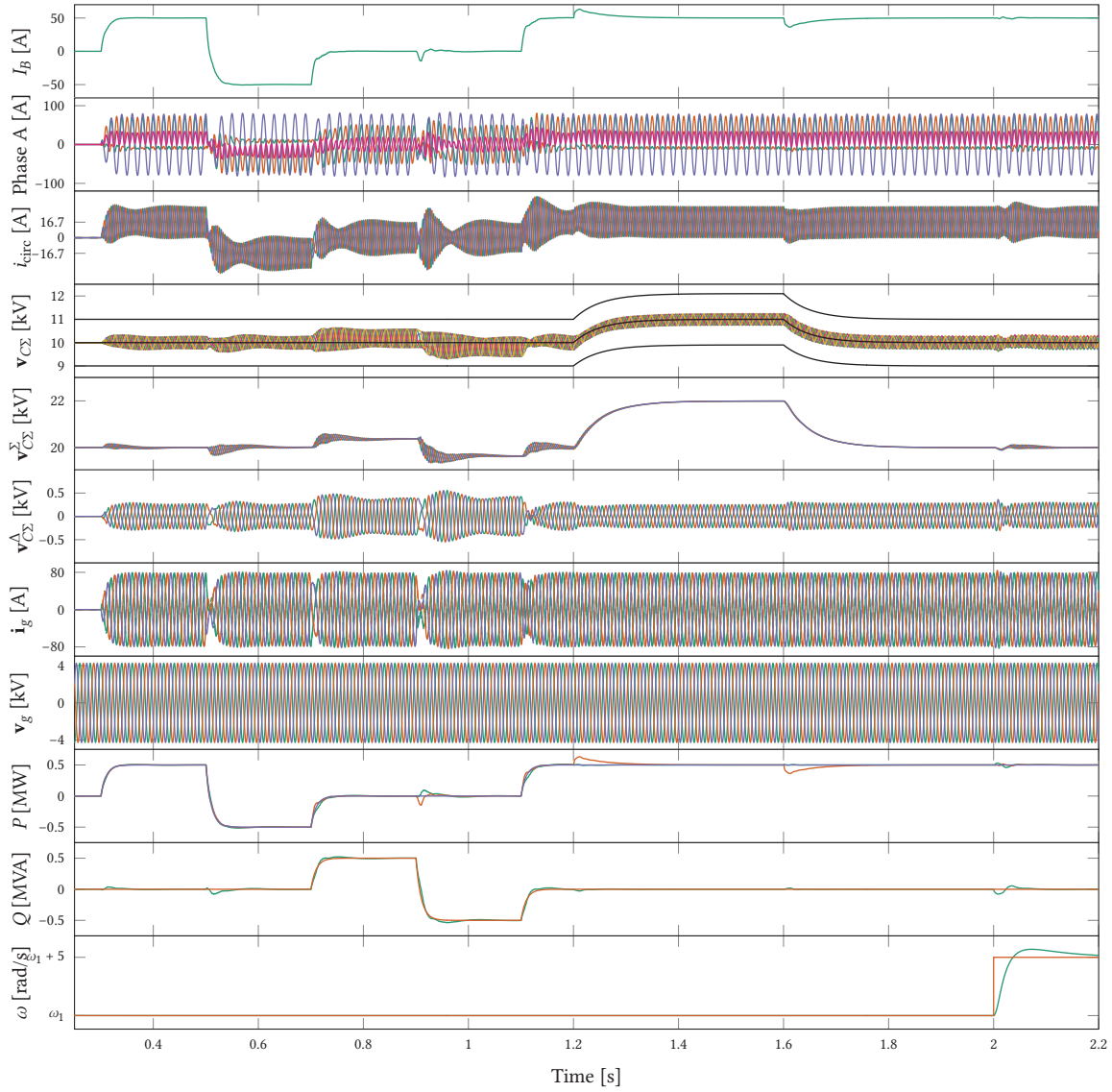


(a)

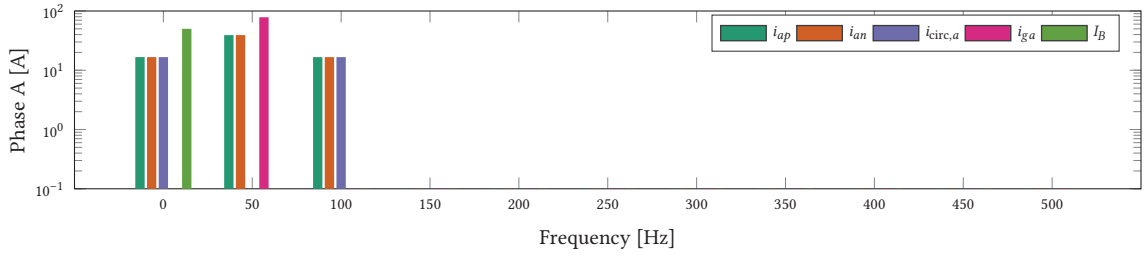


(b)

Fig. 4.24 Case 2 inverter mode: (a) time domain waveforms and (b) FFT in a 2 periods window between 1.9 and 1.94 s. The resonant part of the CCC is not tuned very aggressively and it is observed that the harmonic content in the circulating current decays slowly. The power references are low-pass filtered with $\omega_{f,\text{grid}} = 100$ rad/s. Low order harmonics are removed.

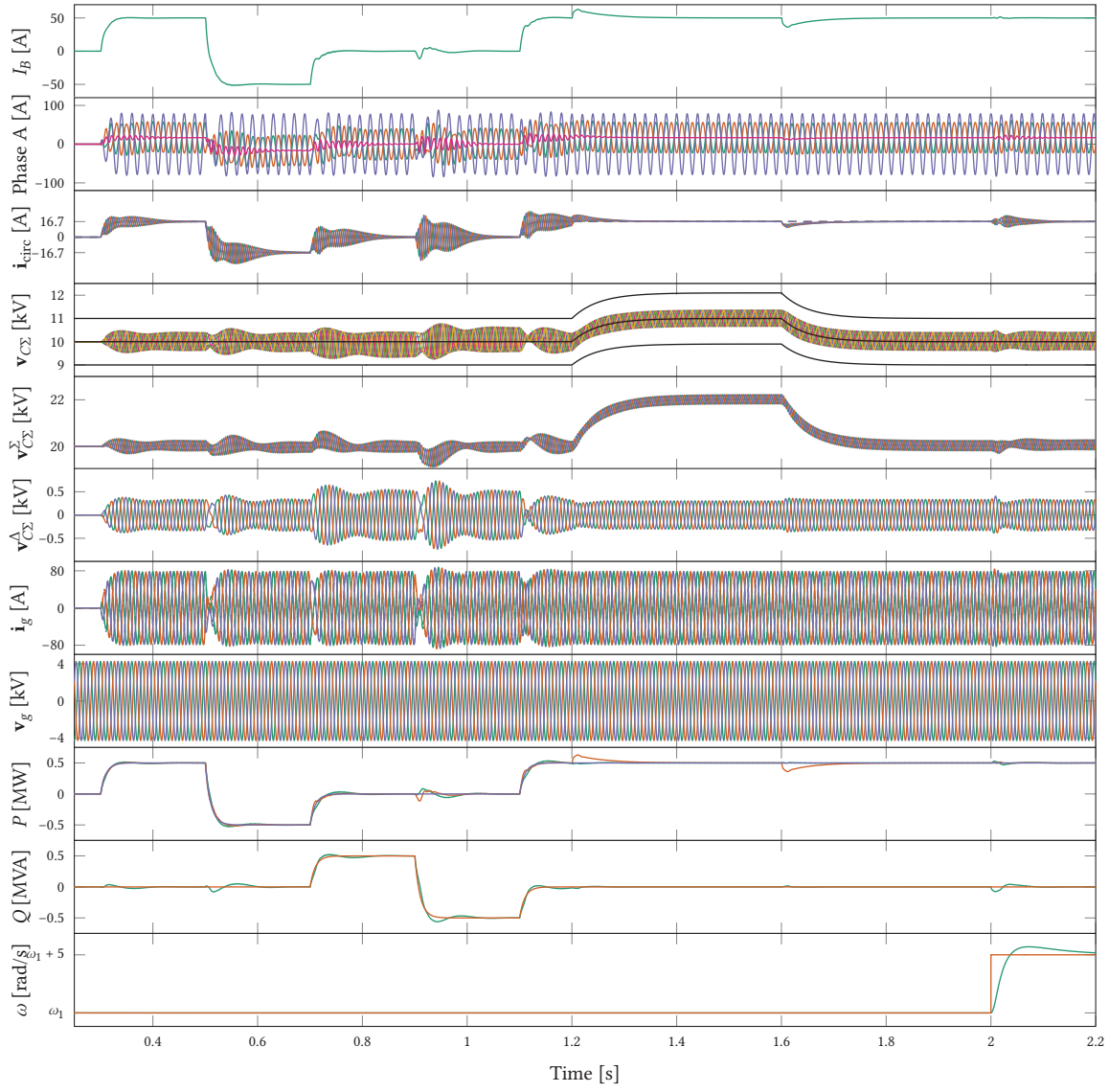


(a)

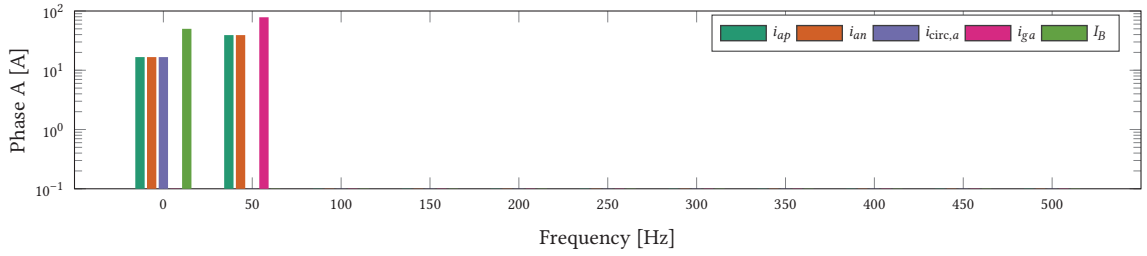


(b)

Fig. 4.25 Case 3 inverter mode: (a) time domain waveforms and (b) FFT in a 2 periods window between 1.9 and 1.94 s. The power references are low-pass filtered with $\omega_{f,\text{grid}} = 100$ rad/s. The dynamics are unchanged, but harmonics in $\mathbf{v}^{\Sigma}_{C\Sigma}$ are almost completely removed thanks to the voltage ripple reduction in $v^{\Sigma}_{C\Sigma}$ (leaving only the ones originating from $v^{\Delta}_{C\Sigma}$).

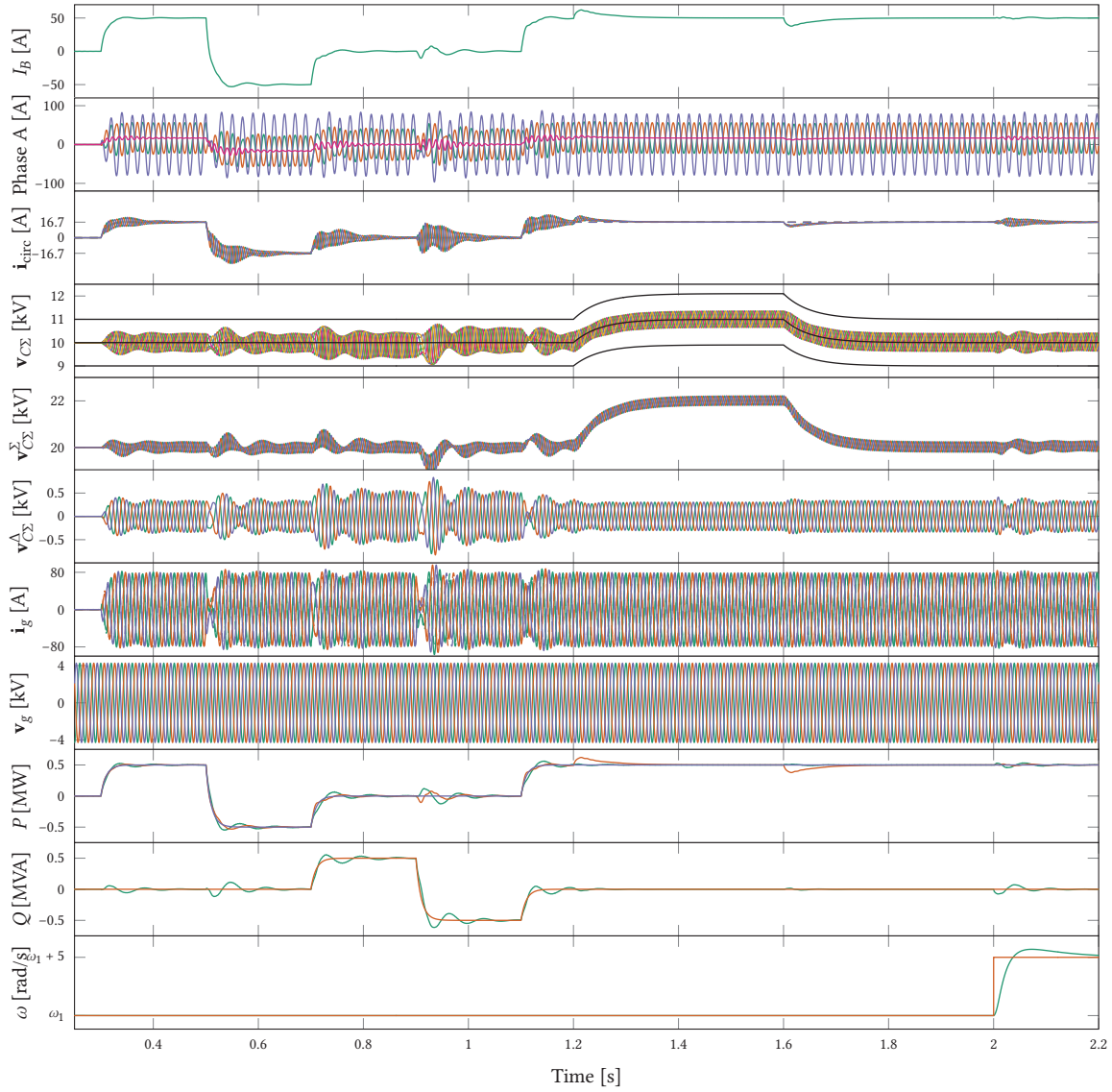


(a)

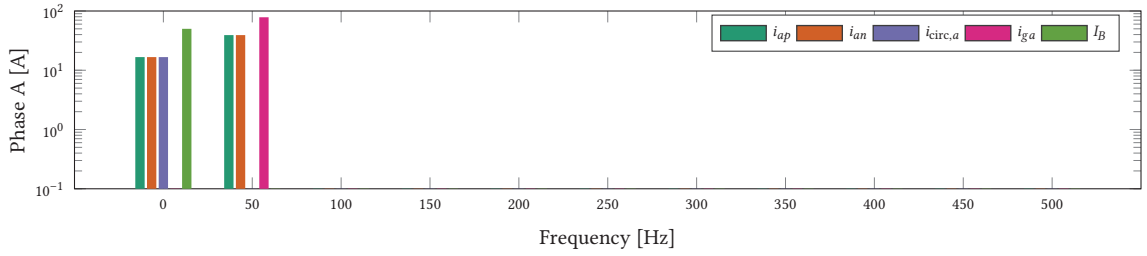


(b)

Fig. 4.26 Case 4 inverter mode: (a) time domain waveforms and (b) FFT in a 2 periods window between 1.9 and 1.94 s. The power references are low-pass filtered with $\omega_{f,\text{grid}} = 100$ rad/s. The dynamics are similar to the direct modulation, with the different that unwanted harmonics are removed.

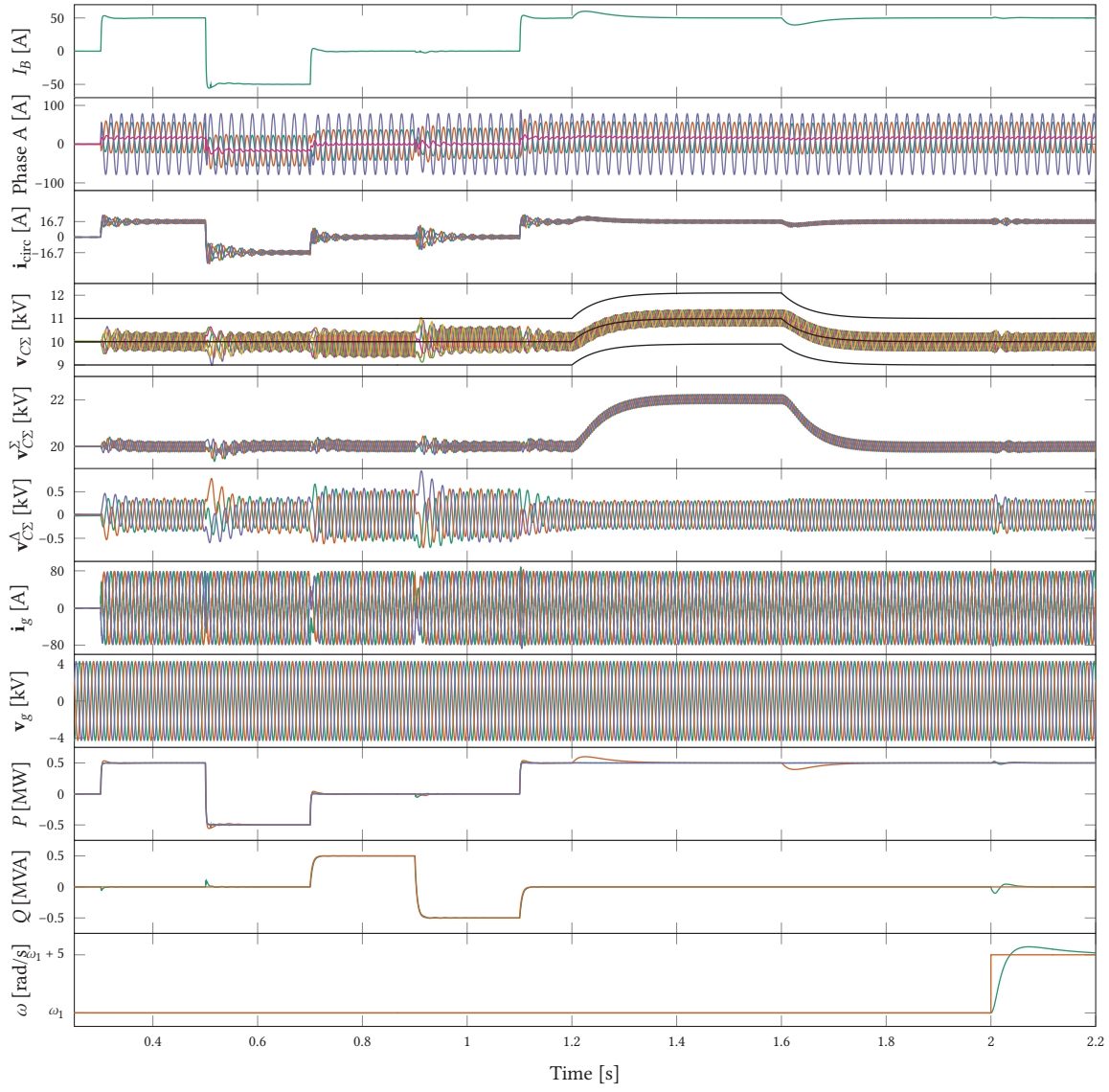


(a)

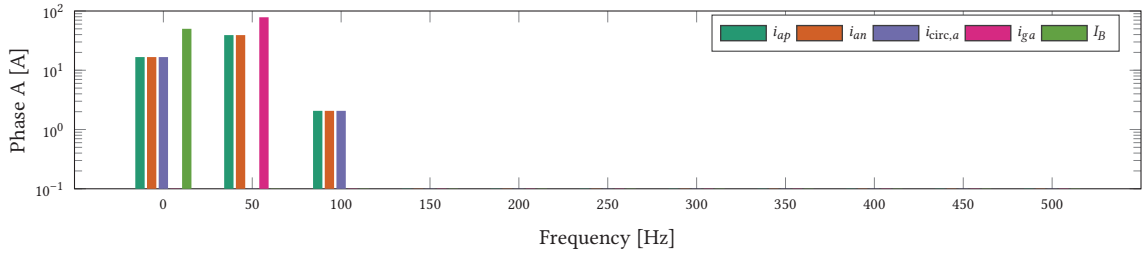


(b)

Fig. 4.27 Case 5 inverter mode: (a) time domain waveforms and (b) FFT in a 2 periods window between 1.9 and 1.94 s. The power references are low-pass filtered with $\omega_{f,\text{grid}} = 100$ rad/s. It is observed that the reactive current step response is very sluggish. The harmonic performance compared to direct modulation is improved, since unwanted harmonics are not present in the observed currents.



(a)



(b)

Fig. 4.28 Case 6 inverter mode: (a) time domain waveforms and (b) FFT in a 2 periods window between 1.9 and 1.94 s. The circulating current is not free of harmonics since no filter is placed on $\mathbf{v}^{\Sigma}_{C\Sigma\alpha\beta}$ (this explains the remaining harmonics on the 2nd). The power references are low-pass filtered with ω_{grid} = 100 rad/s. The dynamic limits for the power reference filters are $\alpha^{P}_{f,grid}$ = 900 rad/s and $\alpha^{Q}_{f,grid}$ = 250 rad/s.

4.3.2 Rectifier mode

When an MMC is used as an active rectifier, the dc voltage has to be regulated by the converter, as illustrated in **Fig. 4.29** and the load is modeled by a current source. The full control scheme is shown in **Fig. 4.30**. In rectifier mode, due to the deviation of the dc voltage on active power changes, it is very likely to be unable to synthesize the required voltage. For that reason, either the reference capacitor voltage $v^{\star}_{C\Sigma 0}$ is set higher than the maximum dc voltage or is set to follow the dc voltage. In the latter scenario, sufficient margin between the maximum ac grid voltage and minimum dc voltage has to be present.

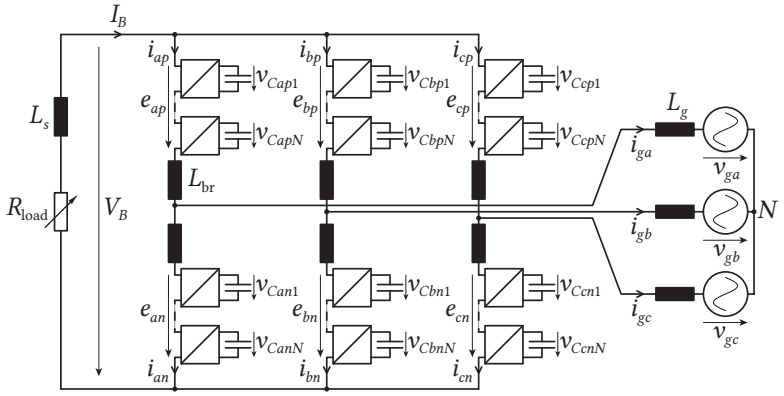


Fig. 4.29 MMC for rectifier mode.

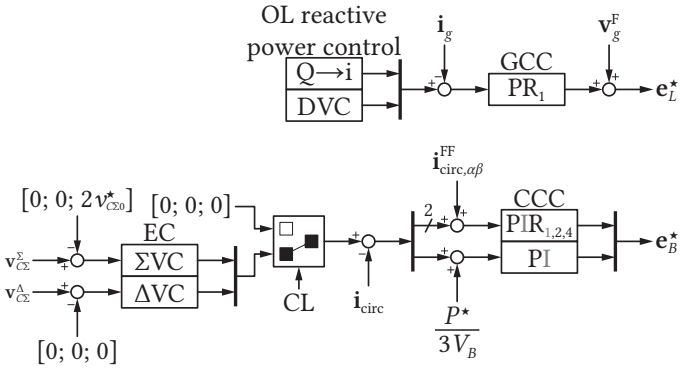


Fig. 4.30 Overall control scheme in rectifier mode.

Three cases are evaluated and the configurations are listed in **Tab. 4.4**.

Tab. 4.4 Control performance in rectifier mode.

Case #	Control method	CCC	CM	2nd harmonic	Load	Figure
1	Closed-loop control	●	○	○	Open-circuit	**Fig. 4.31**
2	Open-loop control	●	○	○	Current source	**Fig. 4.32**
3	Closed-loop control	●	●	●	Resistive load	**Fig. 4.33**

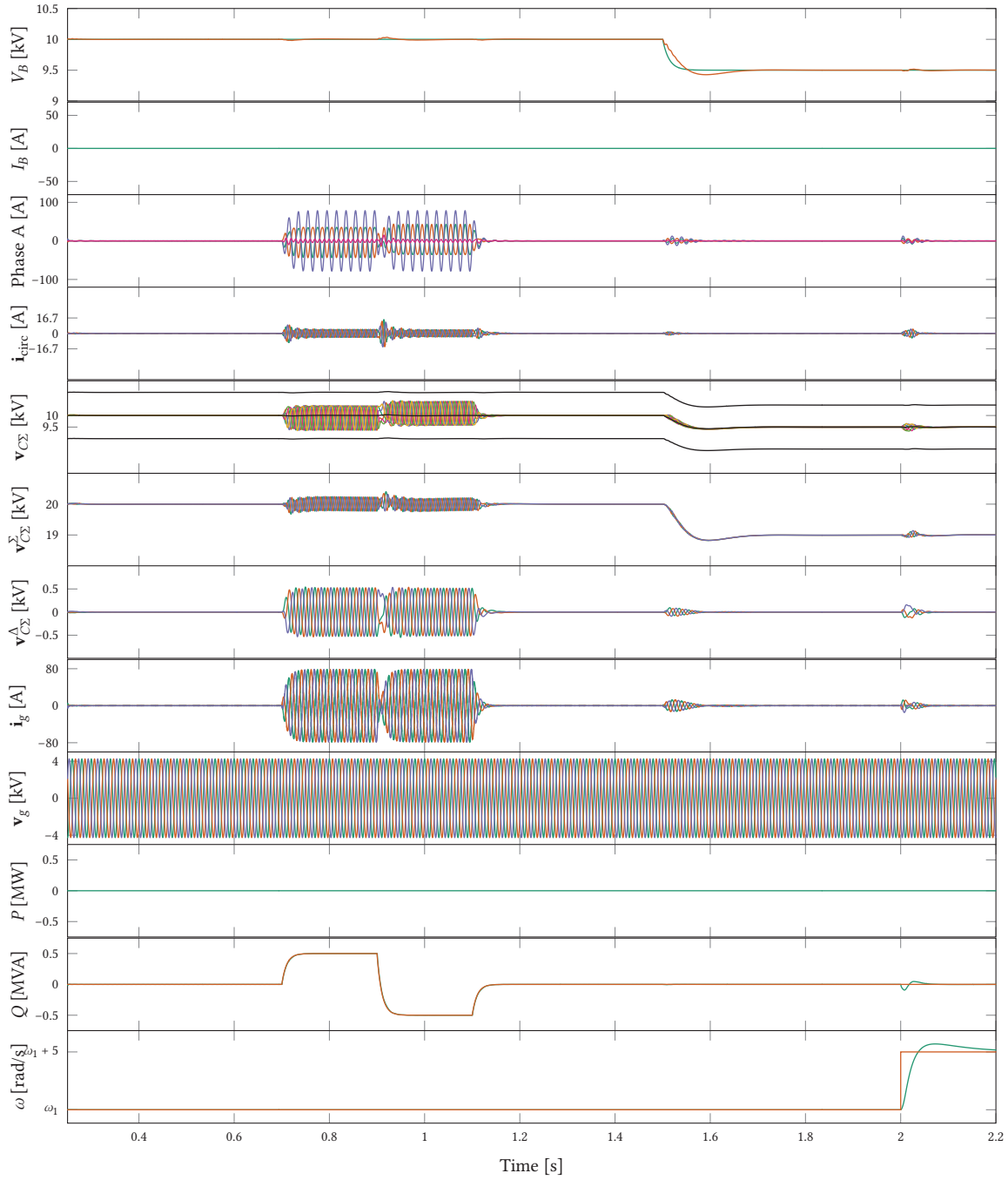


Fig. 4.31 Case 1 rectifier mode. The simulation is stable and the circulating currents cancellation at the dc terminals is verified. Since the dc terminal is unloaded, the active power remains 0 all the time (only the converter losses have to be supplied).

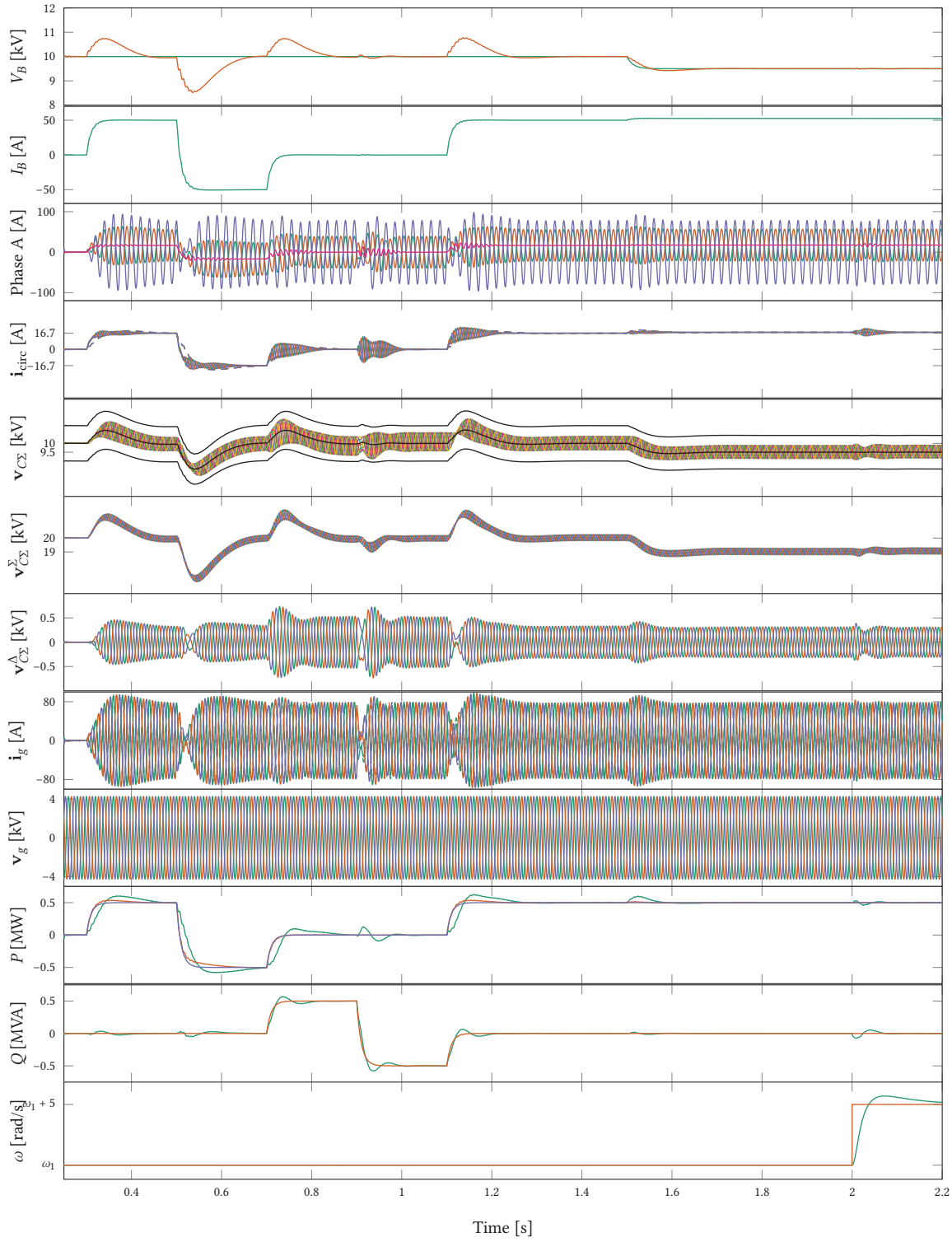


Fig. 4.32 Case 2 rectifier mode. A 30 µF capacitor is added in parallel to the current source (matching $P^\star$) on the dc side and $v^\star_{C\Sigma 0}$ is set to V_B.

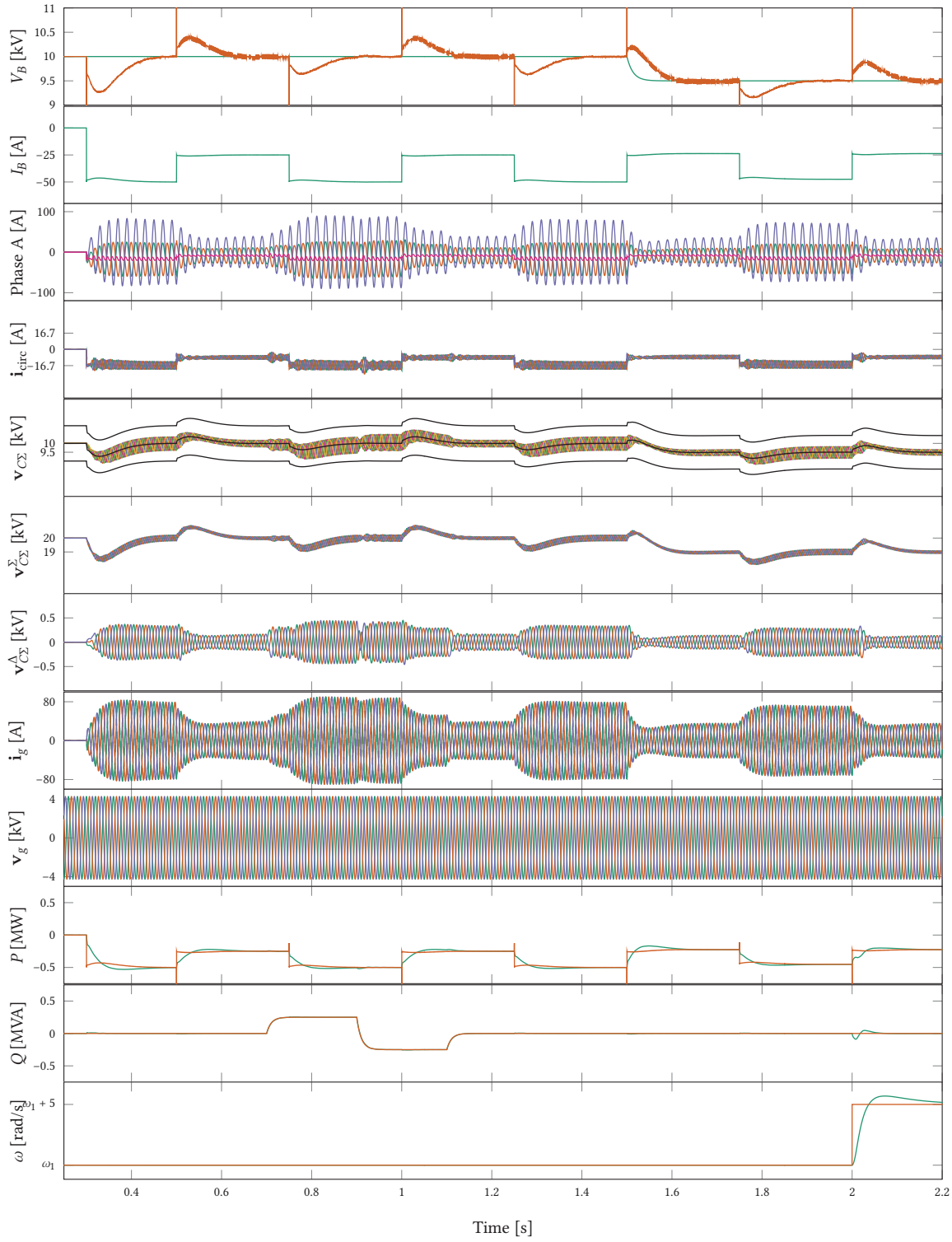


Fig. 4.33 Case 3 rectifier mode. Since the R part of the load varies instantly, the active power drawn from the ac grid is compensating for the required charge or discharge of $v^{\Sigma}_{C\Sigma 0}$.

4.4 Discussion

All in all, the MMC control dynamics and harmonic performances have been compared. The comparative performances according to six criteria are summarized in **Fig. 4.34**. Generally speaking, the reactive power steps are more difficult to track than the active power transients, as the voltage margin is tight in case of $Q^\star > 0$. When the capacitor voltages are not actively controlled (i.e. direct modulation, open-loop control and hybrid voltage control), inferior dynamic performances are observed, even though being asymptotically stable (the system converges after some time, but this time is quite long). In particular, the use of filters to extract the ripple component from the summed branch capacitor voltages is detrimental for the hybrid voltage control method. While these dynamics might be acceptable for specific applications like HVdc where a slow converter response is desired, they aren't suited for dynamic applications that are expected in the medium voltage range. As a conclusion, the closed-loop control is the method of choice for dynamic applications.

Note that grid unbalances and fault conditions have not been discussed here. In [105], the impact of grid unbalances on the branch capacitor voltage ripples is calculated.

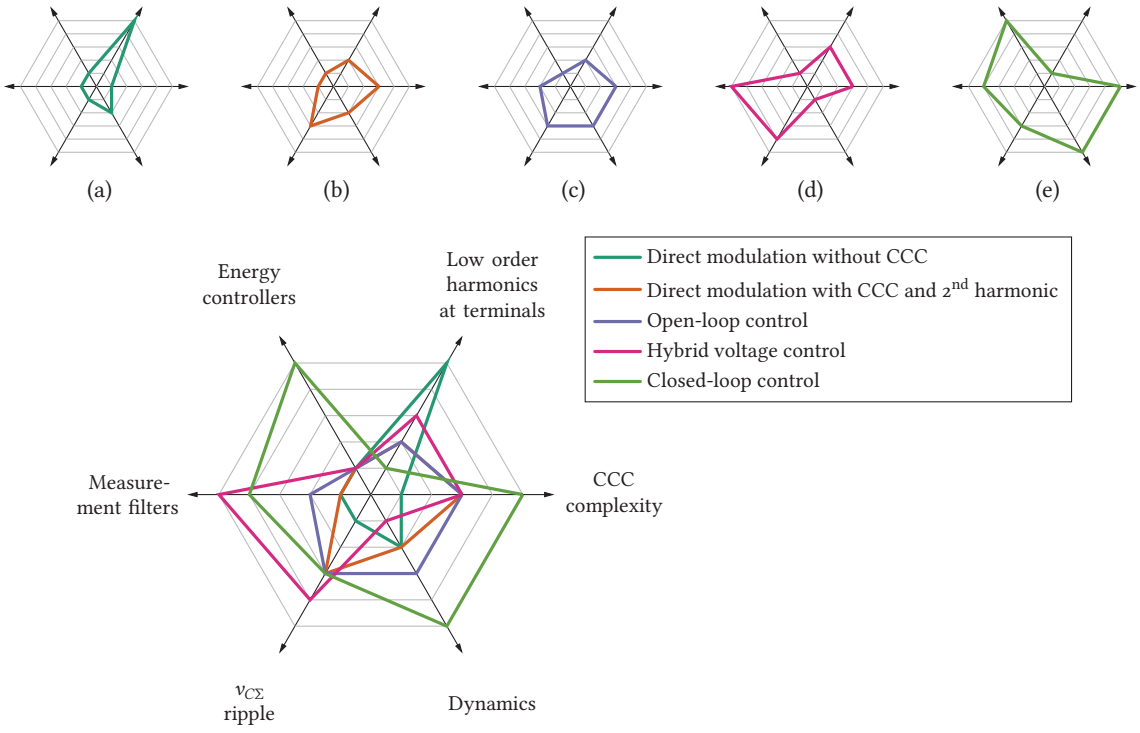


Fig. 4.34 Control methods benchmark in inverter mode: (a) – (e) individual control method performance and (f) converter performance comparison. The axis scale ranges from *small* (at the center) to *large*.

5

Modular multilevel converter modulation and branch balancing methods

The control method performances for a medium voltage dc/3-ac MMC have been assessed in the previous chapter. Moving towards a more detailed switched converter model, modulation and branch balancing methods aim at reproducing as accurately as possible the reference generated by the control algorithm. Several implementation peculiarities and subtleties are discussed in this chapter. Eventually, the most suitable modulation and branch balancing methods are discussed at the end of the chapter.

5.1 Modulation methods

Unlike conventional converter topologies, the combination of the branch switching patterns in order to obtain the bus (towards the dc terminals) and phase (towards the ac terminals) switching patterns complicates the implementation of the conventional multilevel modulation schemes, but at the same time opens door for new combinations / optimizations. This section presents the modulation methods for a dc/3-ac MMC, which are listed in a structured manner in **Fig. 5.1**.

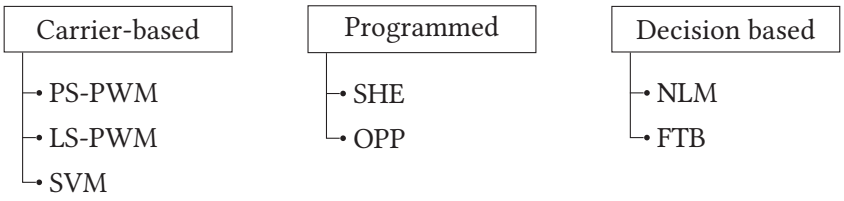


Fig. 5.1 Modulation methods classification.

The modulation can be performed either at the branch level, where the input signal is the branch modulation index, or at the phase-leg level, where the input signals are the bus and phase voltages. They'll be further referred to as branch and phase-leg modulation. Depending on the cell type, and assuming ideal cell capacitor voltages equal to $V^{\star}_{C\Sigma 0}/N_{\text{cells}}$, the maximum number of levels can be analyzed and compared for different modulation schemes.

Unipolar cells Two different maximum numbers of output levels on the ac side can be obtained, either $N_{\text{cells}} + 1$ or $2N_{\text{cells}} + 1$. The two methods are shown in **Fig. 5.2**. In the first case, the observed inserted number of cells on the dc side remains *almost* constant and equal to n_{dc}, as n_p and n_n are

changing *almost* simultaneously in opposite directions[1]. In the second case, the observed inserted number of cells on the dc side will be constantly oscillating between $n_{\mathrm{dc}} - 1$, n_{dc} and $n_{\mathrm{dc}} + 1$, as n_p and n_n are changing only one at a time. This impacts the circulating current harmonic content, which will be excited with *high* frequency, hence a higher branch current ripple will be observed with $2N_{\mathrm{cells}} + 1$ modulation, even though the ac output current quality is improved. When $n_p + n_n = N_{\mathrm{cells}} \pm 1$, the corresponding level is called a *redundant level*. It can always be synthesized by two combinations of n_p and n_n, assuming $N_{\mathrm{cells}} - n_p - n_n \in \{+1, 0, -1\}$. With an odd N_{cells} and $N_{\mathrm{cells}} + 1$ modulation, it is impossible to generate a 0 output in the phase voltage without CM, which makes such configuration less attractive.

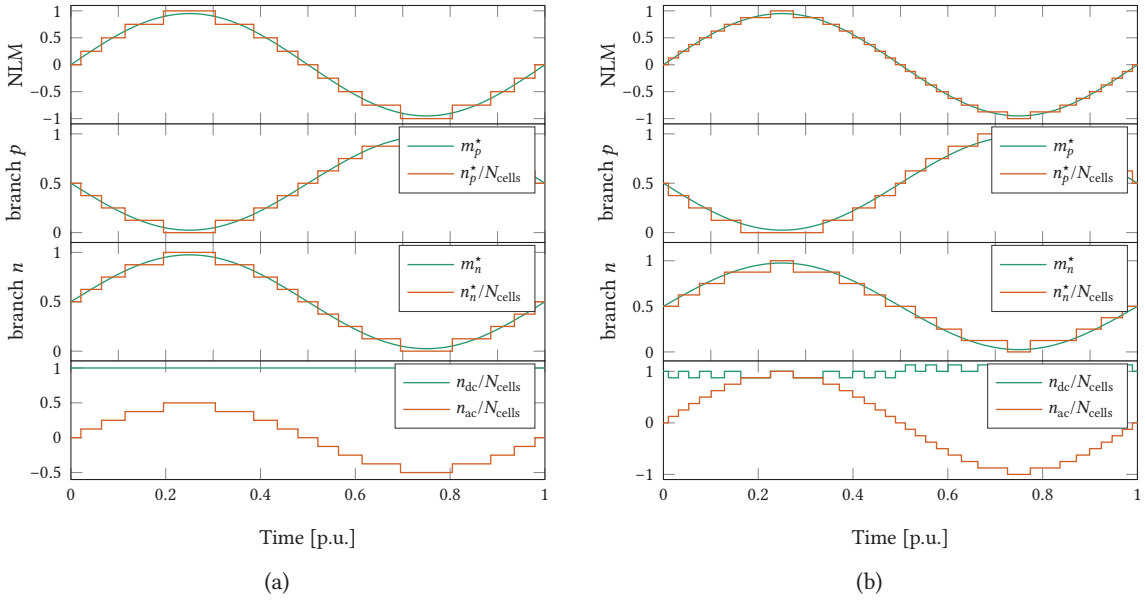


Fig. 5.2 Idealized MMC modulation principle for $N_{\mathrm{cells}} = 8$ (unipolar cells) and $M = 0.95$ with $n_{\mathrm{dc}} = n_p + n_p$ and $n_{\mathrm{ac}} = (-n_p + n_n)/2$: (a) $N_{\mathrm{cells}} + 1$ modulation and (b) $2N_{\mathrm{cells}} + 1$ modulation. Note that the distribution of the switching events between the positive and negative branch for $2N_{\mathrm{cells}} + 1$ is subject to an additional control action, as with the distribution shown the circulating current would experience its largest deviation.

Bipolar cells Apart from the recommended constraint of the ratio between the ac and dc terminal voltages to $\sqrt{2}$ to limit the loss increase to ~ 150 % compared to unipolar cells (cf. **Sec. 3.1.2**), the same analysis as for unipolar cells can be performed for bipolar cells.

Remark The difference in the number of cells per branch between a medium voltage and a high voltage MMC strongly impacts the harmonic performance of a converter, hence while some differences between modulation methods might be tight / negligible for a converter with $N_{\mathrm{cells}} > 100$, this is completely different for $N_{\mathrm{cells}} < 20$.

[1] The use of *almost* is due to the required control action for the circulating current as well as v_{CM}.

5.1.1 Staircase / nearest level modulation

Staircase, or nearest level modulation (NLM), is based on a rounding principle in order to determine the number of inserted cells per branch. For a desired branch voltage $e^\star$, the number of inserted cells is defined as $n^\star = \text{round}(N_{\text{cells}} e^\star / v_{C\Sigma})$. As a direct consequence, the cell switching frequency is close to the line frequency for dc/3-ac MMC[2]. A low cell switching frequency, with a low implementation complexity (there is no carrier) is obtained. However, the modulation methods suffers from poor harmonic performance. If the reference modulation indices are not purely sinusoidal, odd harmonics will appear in the output waveform. Also, the choice of the sampling frequency is not straightforward, since the zeros of the branch current ripple are not equally spaced in time. This aspect is discussed in [106], [107].

$N_{\text{cells}} + 1$ modulation Each branch is modulated separately. In absence of a signal for the circulating current, the switching events in the positive and negative branch coincides. **Fig. 5.3** illustrates the resulting insertion indices and switching patterns for two different values of N_{cells}. When N_{cells} is even, $n_{\text{ac}} = 0$ exists, while in case N_{cells} is odd that level does not exist.

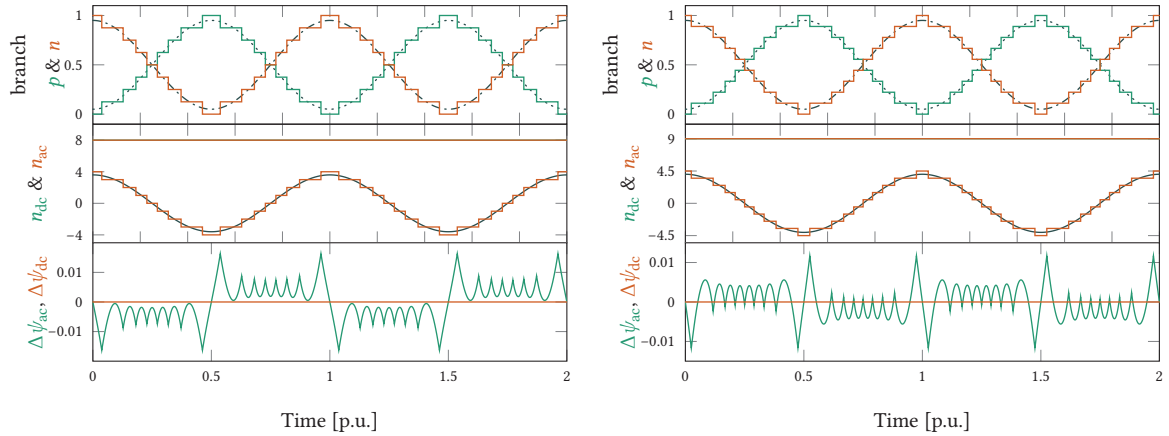


Fig. 5.3 Idealized $N_{\text{cells}} + 1$ NLM for unipolar cells with $M = 0.9$: (a) $N_{\text{cells}} = 8$ and (b) $N_{\text{cells}} = 9$. The volt-second errors are defined as $\Delta\psi_{\text{ac}} = \int m_{\text{ac}} - n_{\text{ac}}/N_{\text{cells}} \mathrm{d}t$ and $\Delta\psi_{\text{dc}} = \int m_{\text{dc}} - n_{\text{dc}}/N_{\text{cells}} \mathrm{d}t$.

$2N_{\text{cells}} + 1$ modulation As mentioned in the introduction of the section, the $2N_{\text{cells}} + 1$ modulation with NLM is a phase-leg modulation. From a logical point of view, $2N_{\text{cells}} + 1$ levels can be obtained by assigning a floor and ceiling function to each branch instead of the round function. However, in that case, the distribution of the redundant levels follows **Fig. 5.2**(b). There is a need for a logic in the selection of the redundant levels. Two methods are proposed: (i) alternate distribution of the $N_{\text{cells}} + 1$ and $N_{\text{cells}} - 1$ level and (ii) hysteresis control depending on the sign of the dc volt-second error, which should be centered around 0. A possible way to evaluate the performance of a modulation method is to look at its flux error, i.e. the time integral of the difference between the desired output and its

[2]More precisely, it is slightly below the line frequency for no CM injection and lower than unity modulation depth, and slightly above the line frequency otherwise. All this is valid only if no additional switching events are required from the branch balancing algorithm

actual value. With NLM, it is clear that the flux error will be larger when the slope of the reference signal decreases. Results are shown in **Fig. 5.4**.

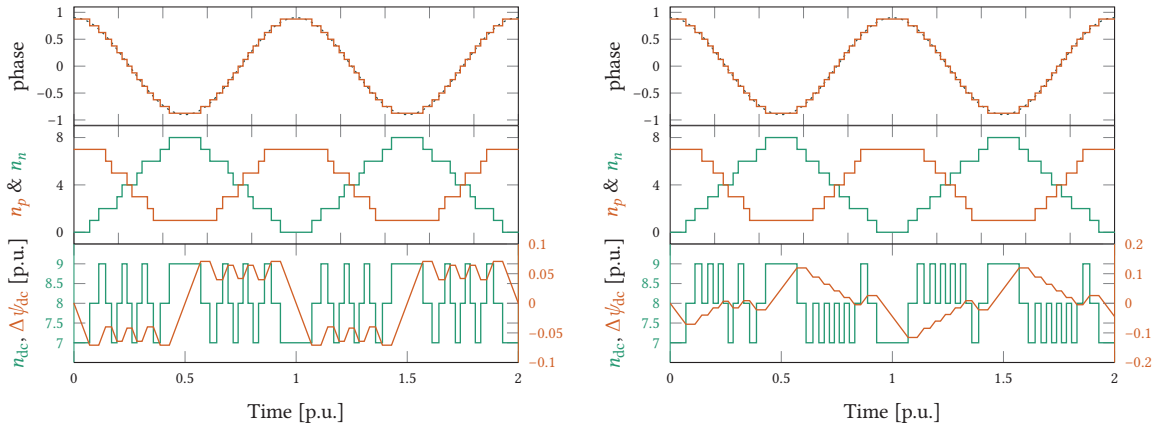


Fig. 5.4 Idealized $2N_{cells} + 1$ NLM for $N_{cells} = 8$ (unipolar cells) with $M = 0.9$: (a) alternate distribution of the redundant levels and (b) hysteresis control of $\Delta\psi_{dc}$.

Tolerance-band modulation As an enhancement, switching events can be introduced when the flux error exceeds a certain defined bound. This concept was proposed in [108] with the flux tolerance-band (FTB) modulation. By essence, it is a per phase correction, meaning that the switching events are not *synchronized* between the phases.

5.1.2 Carrier-based modulation

Three well-known level-shifted PWM (LS-PWM) methods are defined depending on their carriers disposition:

1. PD-PWM: all carriers are in phase, as shown in **Fig. 5.5(a)**.
2. Phase opposition disposition PWM (POD-PWM): the lower set of carriers is phase-shifted by 180° compared to the upper one, as shown in **Fig. 5.5(b)**.
3. Alternative phase opposition disposition PWM (APOD-PWM): the neighbouring carriers are phase-shifted by 180°, as shown in **Fig. 5.5(c)**.

Note that the resulting switching pattern with APOD-PWM is identical to PS-PWM (**Fig. 5.5(c)** vs **Fig. 5.5(d)**). These modulation methods can either be performed at a branch or phase-leg level. Out of these methods, PD-PWM has the best harmonic performance for identical apparent switching frequencies [109], as shown in **Fig. 5.6**.

In the case of multilevel modulation, one interesting geometrical property can be advantageously used in order to reduce the modulation complexity when the modulator is implemented at a branch level or in a centralized controller and that the distribution of the switching signal is performed with a sorting algorithm. The single-carrier principle has already been presented in the literature for PD-PWM in [110], [111]. However, the simplification is not restricted to PD-PWM. The multilevel

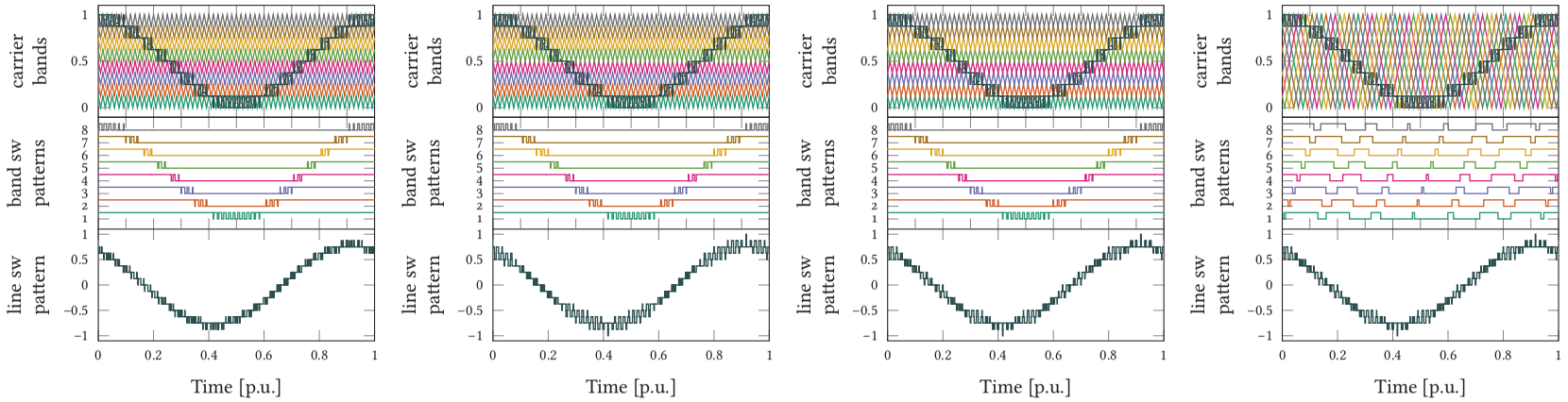


Fig. 5.5 Multilevel PWM methods for $N_{\text{cells}} = 8$ (unipolar), $M = 0.9$ and $f_{\text{sw,app}} = 60 f_g$: (a) PD-PWM, (b) POD-PWM, (c) APOD-PWM and (d) PS-PWM. Only PD-PWM utilizes the two nearest voltage levels in the line-to-line switching pattern. Note that the band / carrier switching patterns are not (necessarily) the switching signals assigned directly to the cells, as the branch balancing algorithms have not been discussed so far.

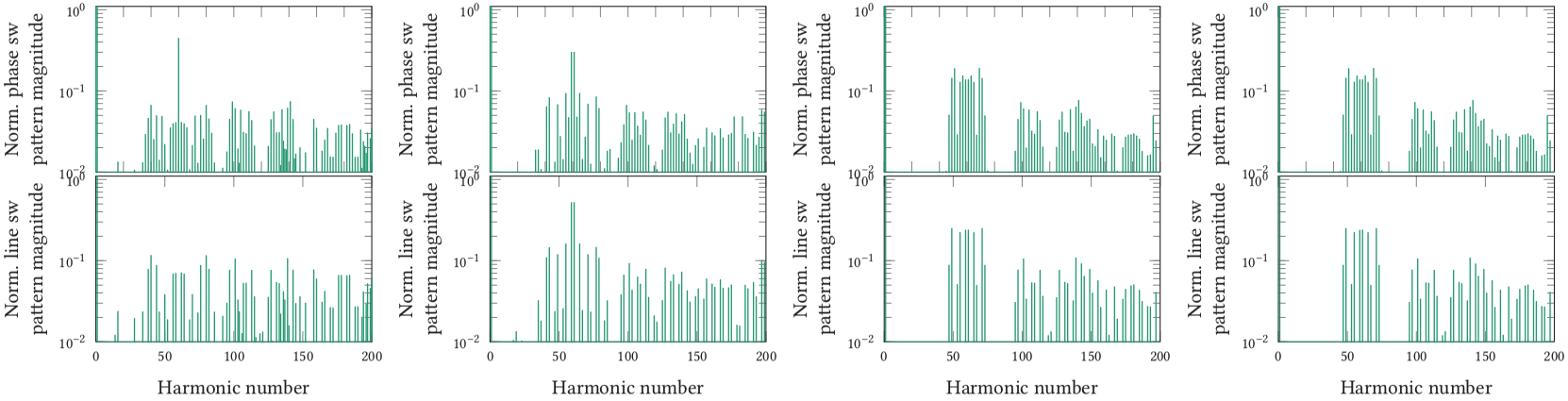


Fig. 5.6 Multilevel PWM spectra for $N_{\text{cells}} = 8$ (unipolar), $M = 0.9$ and $f_{\text{sw,app}} = 60 f_g$: (a) PD-PWM, (b) POD-PWM, (c) APOD-PWM and (d) PS-PWM.

PWM switching pattern is obtained by the summation of individual two-level patterns, with each carrier band defined between two neighbouring levels in $\left[0 \quad 1/N_{\text{cells}} \quad \ldots \quad 1\right]$. Each carrier band is *active* only when the reference is between its upper and lower bound limits. At band crossings, the regular switching sequence +1/ − 1/ + 1 is replaced by consecutive identical switching events (+1/ + 1 or −1/ − 1). Hence, with only two signals, the complete multilevel switching pattern can be retrieved: (i) a quantizer signal, which corresponds to a floor function and tracks the band changes and (ii) a modified reference signal, defined by $mN_{\text{cells}} - \text{floor}(mN_{\text{cells}})$. The last step consists of selecting the correct carrier. While it is trivial for PD-PWM, in the cases of POD-PWM and APOD-PWM the carrier polarity changes between the upper and lower set of carrier bands or at every carrier band change, respectively. The implementation is shown in **Fig. 5.7**, while examples for each modulation method are presented in **Fig. 5.8**.

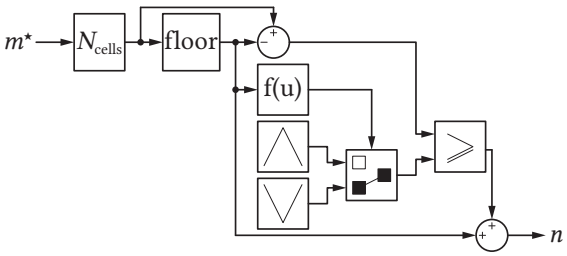


Fig. 5.7 General single-carrier principle for any multilevel PWM method, where only f(u) has to be adapted to account for the carriers disposition.

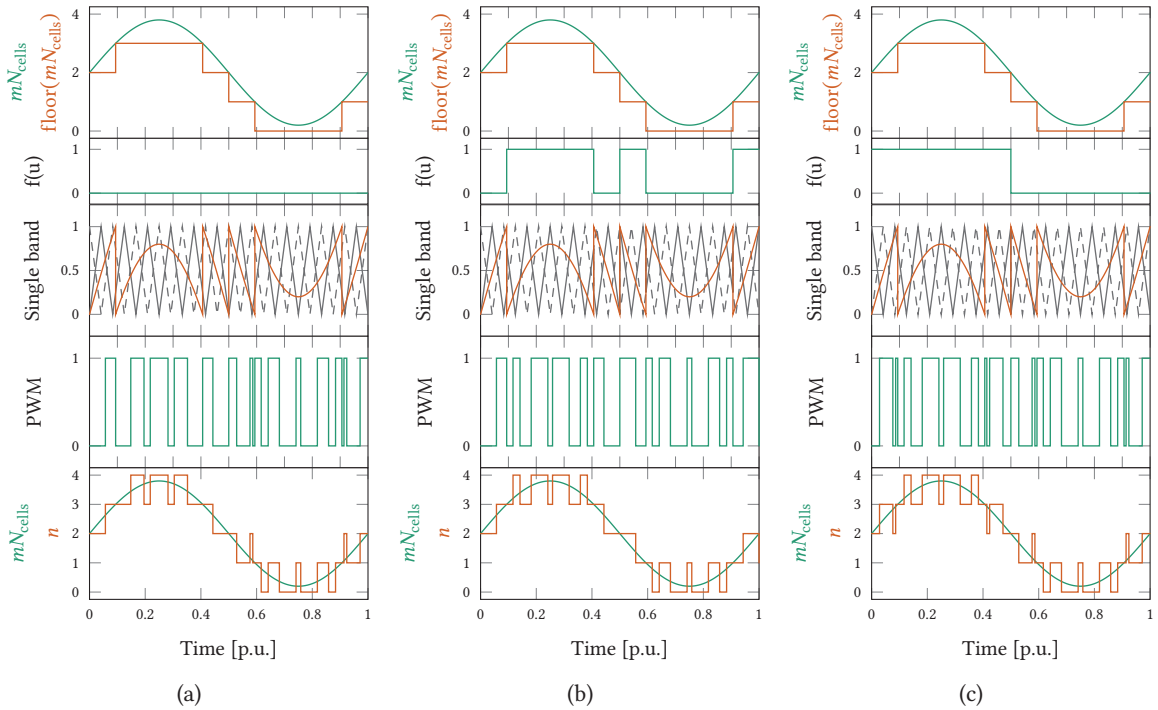


Fig. 5.8 Single carrier band PWM for $f_{\text{sw,app}} = 12f_g$, $M = 0.9$ and $N_{\text{lvl}} = 5$: (a) PD-PWM, (b) APOD-PWM or PS-PWM and (c) POD-PWM. The active carrier is shown in plain lines, while the inactive one in dashed lines.

In the following, the cases of unipolar and bipolar cells will be analyzed separately.

Unipolar cells The results with ideal capacitor voltages for PS-PWM and PD-PWM are illustrated in **Fig. 5.9** and **Fig. 5.10**. The configuration of the carrier phase-shifts are summarized in **Fig. 5.11**, where f_{car} is the individual carriers frequency and Δt_{pn} represents the phase-shift (in [s]) between the positive and negative branch sets of carriers. In order to obtain the phase switching pattern, since $\mathbf{e}_L = (-\mathbf{e}_p + \mathbf{e}_n)/2$, the positive branch carriers have to be mirrored down. As reported in [112], such an implementation for $2N_{\text{cells}} + 1$ modulation with PD-PWM is improper and leads to an identical harmonic performance as with PS-PWM (the same phase switching patterns are obtained). Instead, $2N_{\text{cells}}$ independent and stacked carriers (at the phase-leg level) should be considered, with the addition of a switching event distribution algorithm for the redundant levels (e.g., a finite state machine).

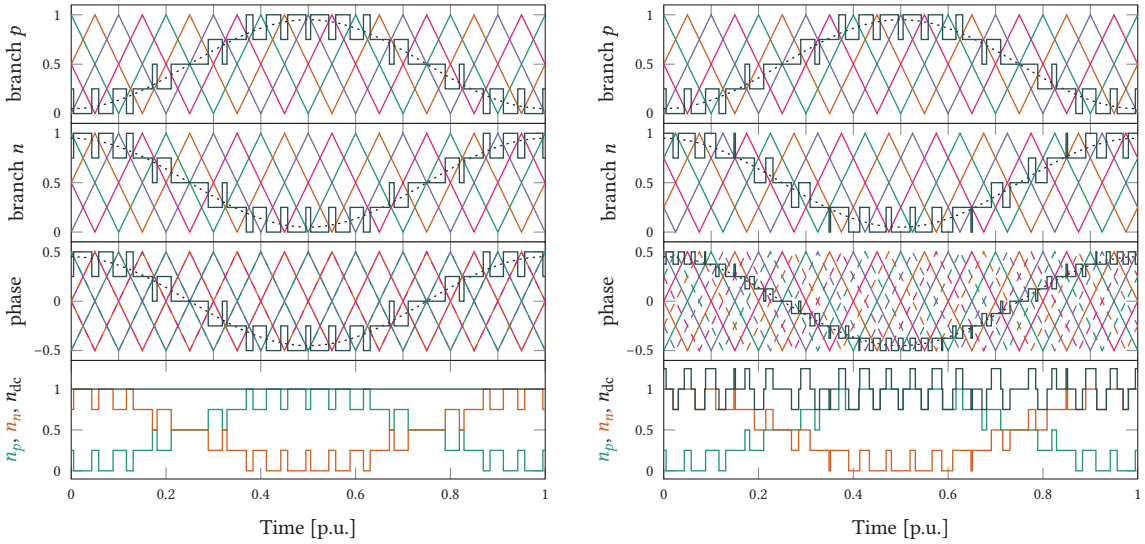


Fig. 5.9 Idealized PS-PWM for $N_{\text{cells}} = 4$ (unipolar cells), $M = 0.9$ and $f_{\text{sw,app}} = 20 f_g$: (a) $N_{\text{cells}} + 1$ with $\Delta t_{pn} = 0$ and (b) $2N_{\text{cells}} + 1$ with $\Delta t_{pn} = 1/(2 f_{\text{sw}} N_{\text{cells}})$. In the phase plots, the carriers from the positive branch are flipped (as $e_L = (-e_p + e_n)/2$) and the ones from the negative branch are shown with dashed lines. The redundant levels are automatically distributed between the positive and negative branch in case of $2N_{\text{cells}} + 1$ modulation, as it can be seen on the bus switching pattern.

Bipolar cells Unipolar modulation is selected instead of bipolar modulation (i.e. the state $s = 0$ is used). First, the analogy between the so-called double-frequency PWM and PS-PWM is recalled (cf. **Fig. 5.12**). Bipolar cells have a redundant 0 state that PD-PWM doesn't take advantage intrinsically. Naturally, one pair of switches (s_1 and $\overline{s_1}$ or s_2 and $\overline{s_2}$) are only switched for half a period (assuming a purely sinusoidal reference signal). In **Fig. 5.13**, the switching events between $\{s_1, \overline{s_1}\}$ and $\{s_2, \overline{s_2}\}$ are redistributed. The states +1 and −1 are doubled to avoid transition of the same leg for two consecutive switching events. The semiconductor switching frequency is maintained at half the carrier frequency, and similar semiconductor stresses as with PS-PWM are obtained.

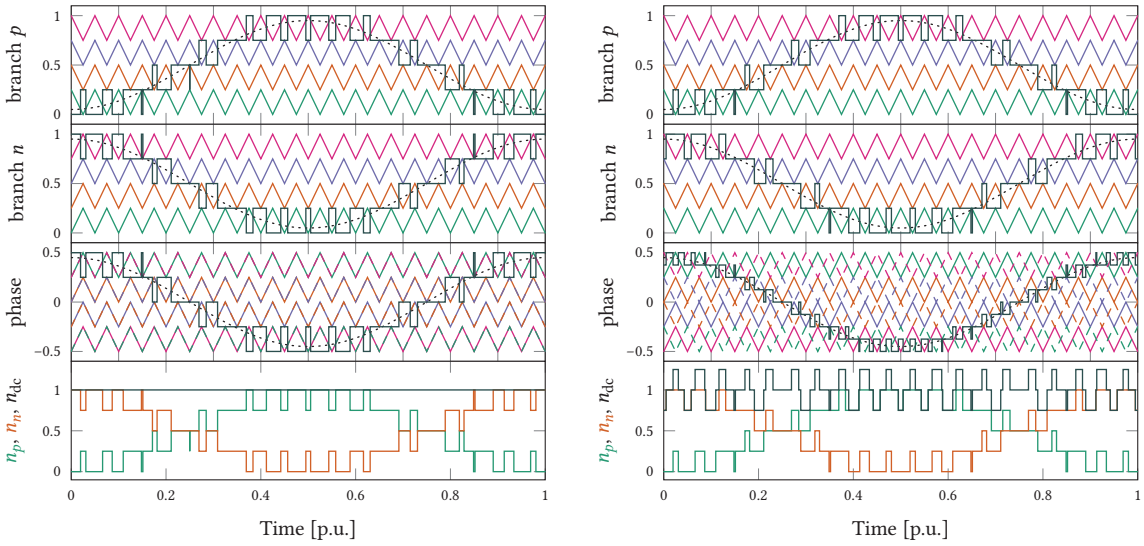


Fig. 5.10 Idealized PD-PWM for $N_{cells} = 4$ (unipolar cells), $M = 0.9$ and $f_{sw,app} = 20 f_g$: (a) $N_{cells} + 1$ with $\Delta t_{pn} = 1/(2 f_{sw})$ and (b) $2N_{cells} + 1$ with $\Delta t_{pn} = 0$. In the phase plots, the carriers from the positive branch are flipped (as $e_L = (-e_p + e_n)/2$) and the ones from the negative branch are shown with dashed lines. It is clear that the $2N_{cells} + 1$ implementation is incorrect, as it is reducing to PS-PWM for the phase switching pattern, as stated in [112], while the bus switching patterns remain different, as they're the sum of two PD-PWM patterns.

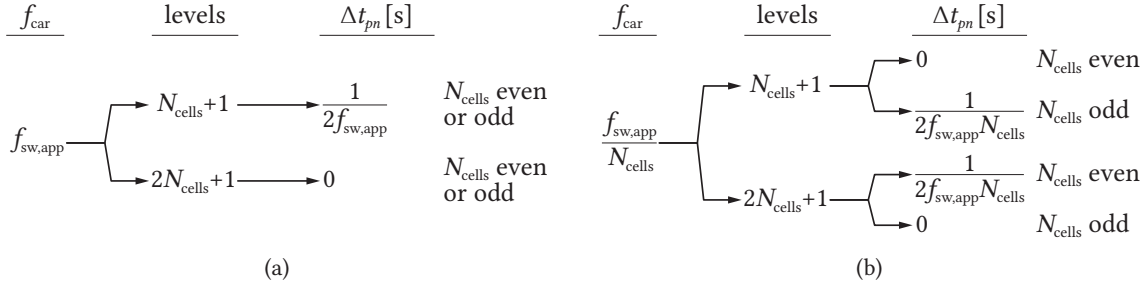


Fig. 5.11 Multilevel phase-shifts configurations for: (a) PD-PWM and (b) PS-PWM, considering a branch modulation. By doing so, $2N_{cells} + 1$ modulation with PD-PWM is improper.

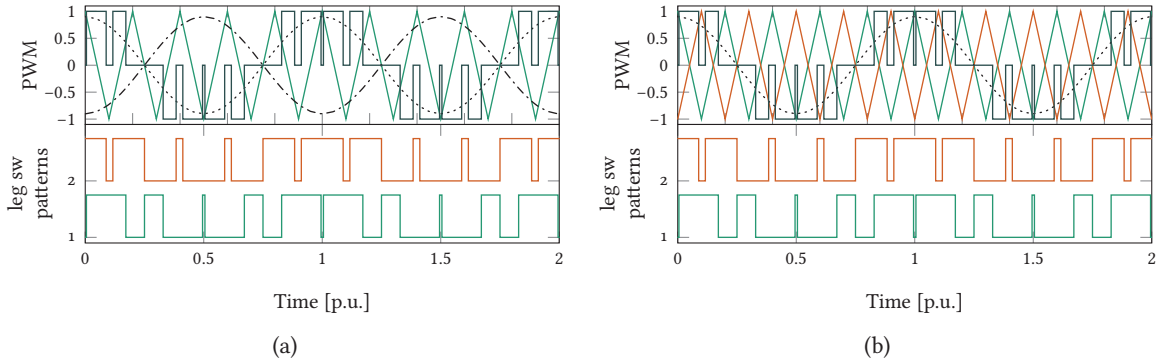


Fig. 5.12 Bipolar cell modulation analogy for $M = 0.9$ and $f_{sw,app} = 10 f_g$: (a) PWM with double frequency (two reference signals) and (b) PS-PWM modulation (two phase-shifted carriers). Note that for the cell switching patterns the signals for s_1 and $\overline{s_2}$ are provided. The leg switching frequencies are $f_{sw} = f_{sw,app}/2$.

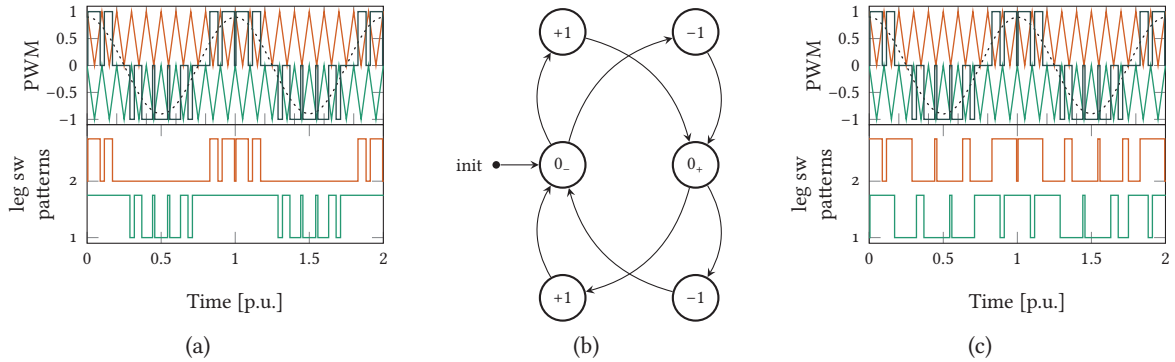


Fig. 5.13 PD-PWM for bipolar cells for $M = 0.9$ and $f_{sw,app} = 10 f_g$: (a) standard implementation, (b) finite state machine to equally distribute the switching events between the two legs (the (natural) initial cell state is 0_-) and (c) modified PD-PWM modulation. In the standard implementation, the legs feature an alternation of switching events at frequency at $f_{sw} = f_{sw,app}$ and no switching events, with a duty-cycle of 0.5. This leads to semiconductor thermal cycling. With the redistribution (i.e. equalization) of the switching events, the legs feature a constant switching frequency of $f_{sw} = f_{sw,app}/2$. The redistribution of the switching events achieves a constant leg switching frequency equal to its average, hence the semiconductor thermal cycling is reduced. Note that for the cell switching patterns the signals for s_1 and $\overline{s_2}$ are provided.

5.1.3 Space-vector modulation

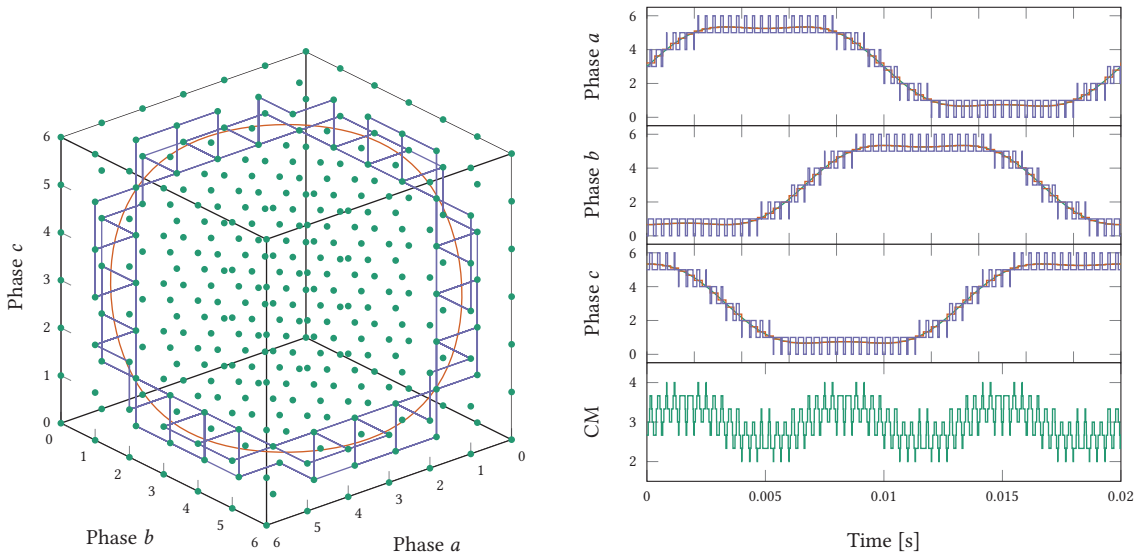
Initially presented in [83] for two-level inverters, the space-vector modulation (SVM) has been extended to multilevel inverters. A 3D SVM implementation according to [113] is followed. The result is shown in **Fig. 5.14**. This is the modulation method initially used in [114]. Apart from the equal split of the first and last duty-cycle in the switching sequence (i.e. min/max CM injection, as presented in **Sec. 4.2.3**), the reference signals also have to be centered within the carrier band [115], as shown in **Fig. 5.15**. SVM has been little explored for MMC, even though advanced CM generation has been introduced recently in [116].

5.1.4 Programmed modulation

In industrial medium voltage applications, the number of cells per branch might be very low. In order to maintain a good harmonic performance without compromising the converter's efficiency, i.e. by keeping a low cell switching frequency, optimized pulse pattern (OPP) and selective harmonic elimination (SHE) are two programmed methods of choice. In both cases, the number of switching angles (minus one for setting the fundamental) in a quarter of a period[3] forms the degrees of freedom available for optimization. The difference between OPP and SHE is that the (offline) optimization formulates user definable constraints on specific harmonics for OPP, while it aims at completely canceling low order harmonics (one per available switching angle) with SHE.

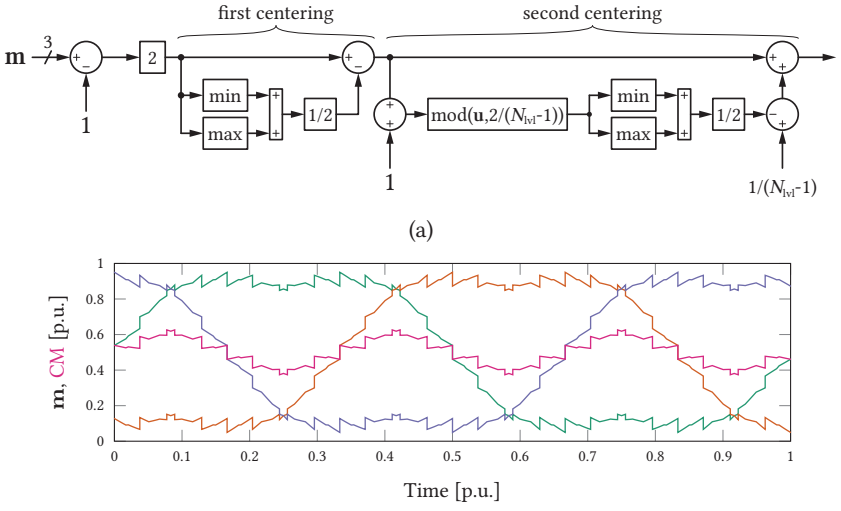
However, both of these modulation methods have been overlooked in the literature, especially when it comes to closed-loop control of the output current. The interested reader is invited to consult [117] that deals with this particular aspect of OPPs, which covers partly the work carried out by the author

[3]Half-wave symmetry ensures no even harmonics are present in the resulting pattern.



(a) (b)

Fig. 5.14 3D SVM for $N_{\text{lvl}} = 7$, $M = 0.9$, 3rd harmonic injection and $f_{\text{sw,app}} = 3\,\text{kHz}$: (a) 3D normalized domain, with each of the $7^3 = 343$ switching combinations represented by a green dot, the reference signal in red and the switching sequence in blue, and (b) resulting patterns.



(a)

(b)

Fig. 5.15 3D SVM with centered space vector for $N_{\text{lvl}} = 7$ and $M = 0.9$: (a) centering method and (b) corresponding references.

at ABB Switzerland Ltd., in Turgi. As this is an industry specific topic, it will not be further discussed in this thesis.

Remark In $N_{\text{cells}} + 1$ modulation with an odd N_{cells}, there is a fixed switching event imposed at the zero crossing of the phase waveform. This means there is no additional degree of freedom (or switching transition) compared to the even case $N_{\text{cells}} - 1$, e.g., $N_{\text{cells}} = 5$ versus $N_{\text{cells}} = 4$.

5.2 Branch balancing methods

A basic requirement for a stable converter operation and the validity of the average MMC modeling is that the capacitor voltages within a branch should be balanced, i.e. kept closely altogether. The *degree of closeness* depends on the cell switching frequency and is hardly quantifiable. This is generally a desired feature for cascaded converters, as large cell capacitor voltages spread leads to unequal thermal stresses, which is undesirable. Also, a larger voltage spread means a less *accurate* modulator, i.e. the difference between the desired and actual branch voltage increases. Consequently, a larger control action for compensation is required.

5.2.1 Sequencing

The sequencing principle is similar to the coarse step modulation for pulsed power [118]. All the cells are inserted / bypassed in a predefined order. Indeed, the assignment of the switching signals is identical to PS-PWM with non-integer frequency ratio between the grid and carrier frequencies (cf. **Fig. 5.16**). Consequently, similar self-balancing properties are observed.

This branch balancing algorithm was used in [119] in combination with SHE modulation.

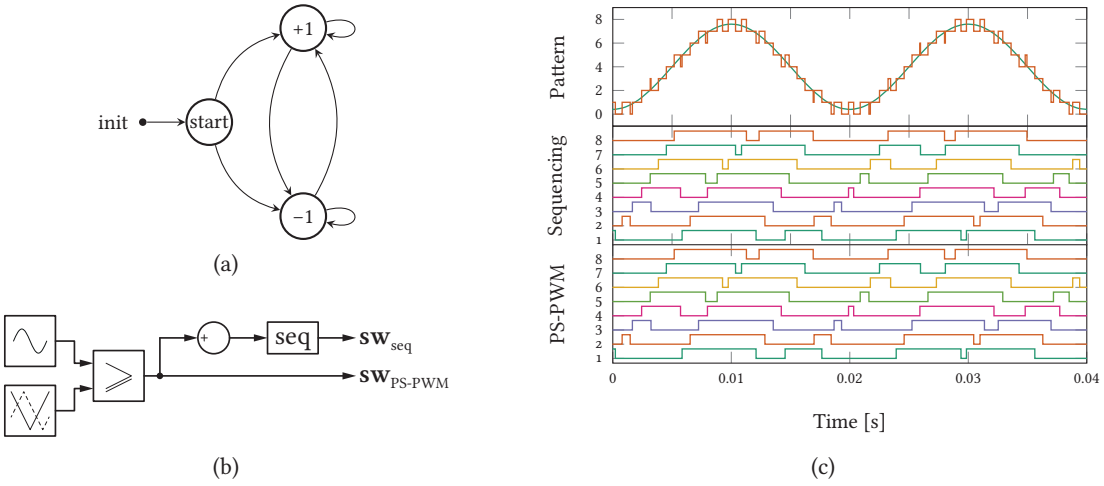


Fig. 5.16 Sequencing balancing method: (a) finite state-machine, (b) comparison configuration and (c) comparison results for $N_{cells} = 8$, ideal sinusoidal reference and $f_{sw,app} = 945\,\text{Hz}$.

5.2.2 Sorting

This was the original proposal from Marquardt [18]. The idea is rather simple, and is based on the net energy transfer to a cell. The objective is to make the cell capacitor voltages converge, i.e. to discharge the cells that are charged the most and to charge the ones that are charged the least. The vector of measured capacitor voltages is first sorted, as shown in **Fig. 5.17**.

Depending on the polarity of the branch current and cell state s, the inserted cell capacitor is either charged or discharged, as shown in **Tab. 5.1** that lists all the possible combinations. By sorting the

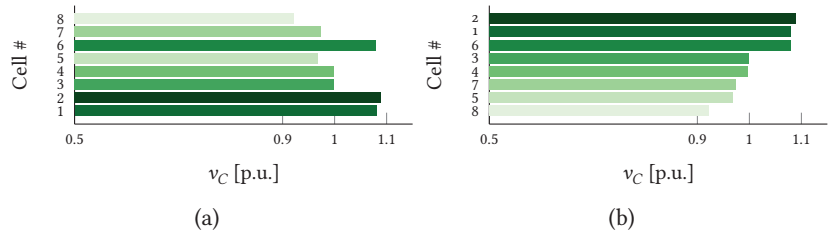


Fig. 5.17 Sorting principle for $N_{\text{cells}} = 8$: (a) before sorting and (b) after sorting (in ascending order).

Tab. 5.1 Net energy transfer to a cell, neglecting its internal losses.

s	$i_{\text{br}} \geq 0$	$i_{\text{br}} < 0$
+1	$v_C \nearrow$	$v_C \searrow$
0	$v_C \rightarrow$	$v_C \rightarrow$
−1	$v_C \searrow$	$v_C \nearrow$

cells depending on their states ($s \in \{0, +1\}$ for unipolar cells and $s \in \{-1, 0, +1\}$ for bipolar cells[4]) and charging level (v_C), it is possible to determine which set of cells should be used at a given instant, while maintaining the charge level of all the cells within a branch around the same level (i.e. the branch average voltage, which contains low order harmonics: dc, fundamental ac, twice fundamental, etc.).

An improvement of the method, which will be further referred to as restricted sorting algorithm (RSA), was presented in [99]. The idea is to avoid group permutations between inserted and bypassed cells, i.e. for each switching transition the best cell is selected. The logic for the RSA is shown in **Tab. 5.2**. The condition $\mathrm{d}n_{\text{br}} = 0$ is always reached assuming that the number of inserted cells per branch, n, is properly bounded. The difference between the two algorithms is shown in **Fig. 5.18**. It is clear that the behavior of RSA is much more desirable than the one with simple sorting.

5.2.3 Phase-shifted carriers

PS-PWM has an inherent branch balancing capability when the switching frequency is not an integer multiple of the grid frequency. While a formal proof was presented in [120], the concept can be grasped intuitively: in order to achieve the balancing of the capacitor voltages within a branch, the insertion / bypass times have to be *shuffled*, else the cells will experience different power transfer over a long horizon and their voltages will diverge.

However, a proper frequency ratio that achieves self-balancing is not always desired from the point of view of harmonics. Additionally, during changes of $v^{\star}_{C\Sigma 0}$, the self-balancing property is compromised. For these reasons, it is recommended to augment the PS-PWM modulation with a balancing algorithm, as shown in **Fig. 5.19**. This is a proportional controller with gain k_{bal}, whose action doesn't contribute to the total energy control ($\sum_{i=1}^{N_{\text{cells}}} k_{\text{bal}} \Delta v_{Ci} = 0$). Such a controller is very similar to what is used for the cell balancing of a cascaded H-bridge converter [121] and was initially proposed for MMC in [122]. Note that the balancing method based on a moving average filter (MAF) is less sensitive to communication delays between a central controller or hub and the cells, thus is more suitable for distributed modulation.

Compared to a sorting algorithm balancing method, PS-PWM balancing suffers from very limited balancing capability at no load (i.e. when $i_{\text{br}} \approx 0$). This drawback might be problematic depending on the application. A possible workaround would be to inject a circulating current in order to increase the branch current.

[4]For multilevel cells, the sets are extended, but the principle remains the same.

Tab. 5.2 RSA decision table for: (a) unipolar and (b) bipolar cells. $ is the set of cells for each state. dn is the difference w.r.t. the previous number of inserted cells per branch. The algorithm is looped until $dn_{br} = 0$ at each switching update instant.

(a)

	$i_{br} \geq 0$	$i_{br} < 0$
$dn = +1$	min(${0})	max(${0})
$dn = -1$	max(${+1})	min(${+1})

(b)

		$i_{br} \geq 0$	$i_{br} < 0$
$dn = +1$	${−1} ≠ ∅	min(${−1})	max(${−1})
	${−1} = ∅	min(${0})	max(${0})
$dn = -1$	${+1} ≠ ∅	max(${+1})	min(${+1})
	${+1} = ∅	max(${0})	min(${0})

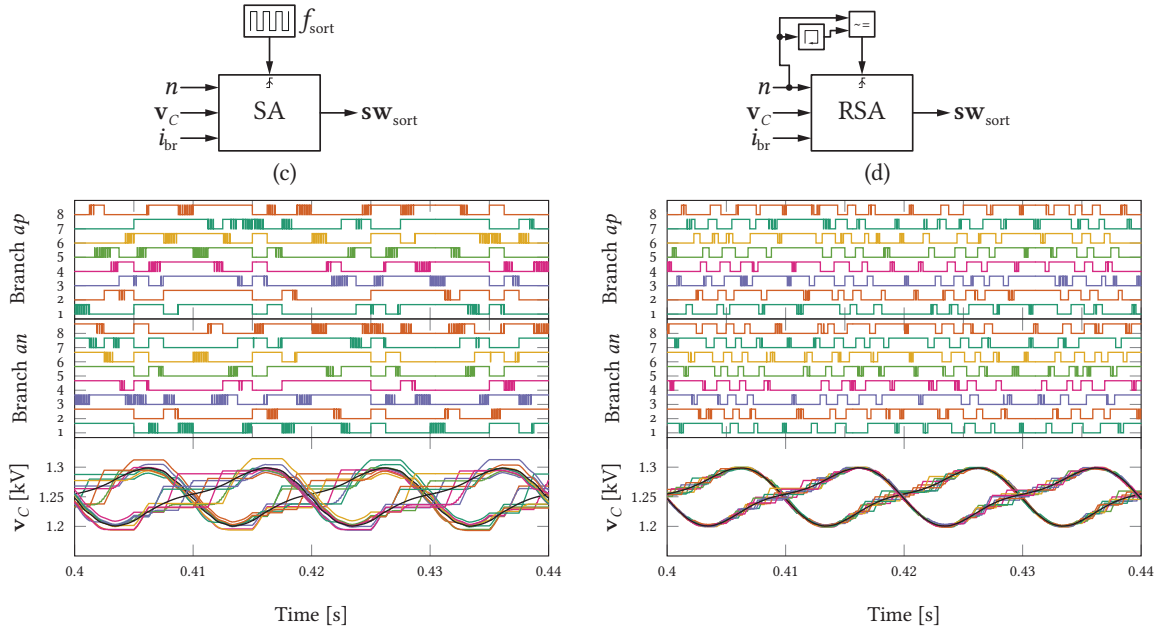


Fig. 5.18 Comparison between simple sorting and RSA with $N_{cells} = 8$, PD-PWM and $f_{sw,app} = 5\,kHz$: (a) the simple sorting algorithm is triggered at $f_{sort} = 400\,Hz$ and (b) RSA triggered when n changes. The average branch capacitor voltages are shown in black. With simple sorting, the average cell switching frequency is 800 Hz. With RSA, the average cell switching frequency is 668.75 Hz. With RSA the cell switching frequency is both deterministic and constant, which is not the case for simple sorting. In any case, the average cell switching frequency is higher than $f_{sw,app}/N_{cells} = 625\,Hz$, due to transitions between carrier bands.

5.2.4 Carrier swap

Used for comparison in [123], this balancing method is a hybrid between level-shifted and phase-shifted carrier. In **Fig. 5.20**, two possible implementations, (i) with sawtooth carrier swapping and (ii) with triangle carrier swapping, are presented. Depending on the choice of n_{swap} (the number of carrier periods before swapping), the switching patterns might not be simply phase-shifted among the cells, especially with sawtooth carrier swapping.

Simulation results are presented in **Fig. 5.21**. The voltage spread is by far the largest of all the previously presented method, despite a larger average cell switching frequency (due to the swapping

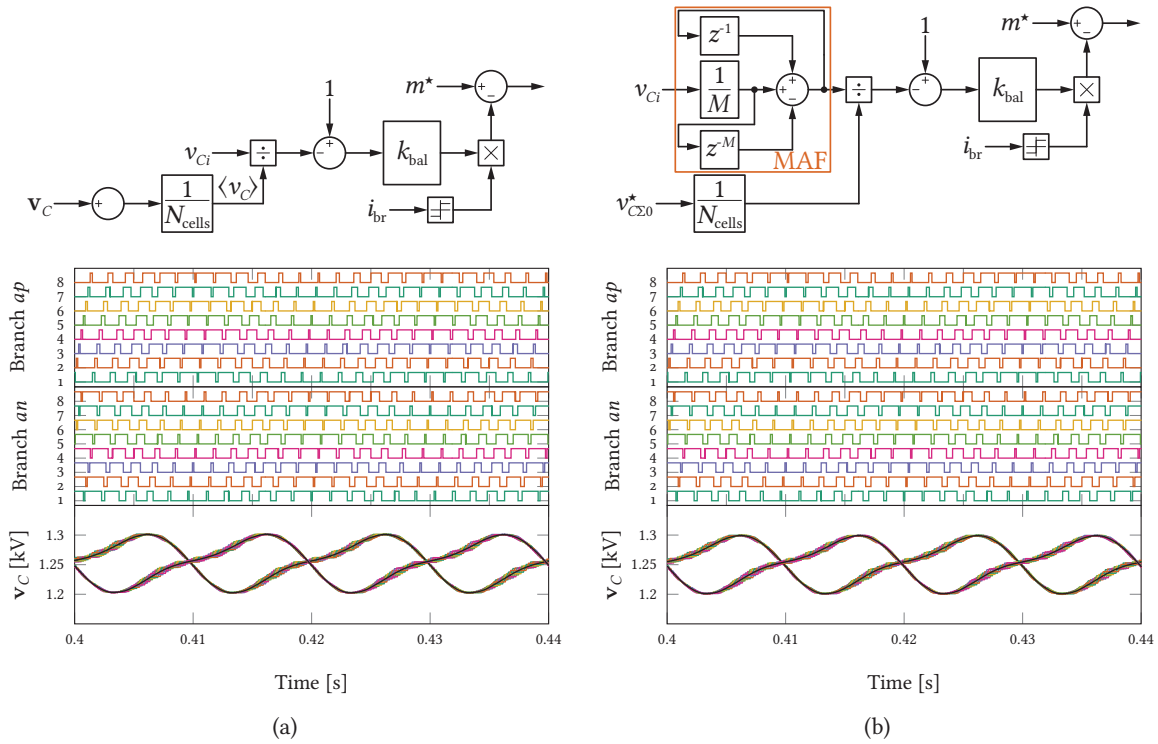


Fig. 5.19 PS-PWM balancing with $N_{\text{cells}} = 8$, $f_{\text{sw,app}} = 5\,\text{kHz}$ and $k_{\text{bal}} = 0.1$: (a) balancing algorithm using the instantaneous branch average voltage $\langle v_C \rangle$ and (b) balancing algorithm using the reference capacitor voltage and a discrete MAF with $M = \text{floor}(f_{\text{sw,app}}/f_g)$. In both cases, the average cell switching frequency is 662.5 Hz.

of carriers causing additional switching events). Also, the switching pulses are far from being well distributed among the cells within a branch, leading to an uneven distribution of the stresses among the cells. For these reasons, this balancing method is not recommended.

5.2.5 Additional features

Additional switching actions when a cell capacitor voltage exits predefined voltage bounds (hardware limit or voltage spread limitation) might be desirable for cases with very low cell switching frequency, i.e. with large conduction times.

RSA with very low average cell switching frequency With low average cell switching frequency, the cell capacitor voltages spread becomes large. In such a case, the RSA is not able to maintain the cell capacitor voltages within reasonable bounds. It is much desirable from a harmonic point of view to ensure that the cell capacitor voltages remain within a predefined range, hence limiting the voltage error. The addition of a tolerance band $(1 \pm k_{\text{max}})v^{\star}_{C\Sigma 0}/N_{\text{cells}}$ constraint on the cell voltages enables the exchange of conducting cells in case of bound violation (cf. **Fig. 5.22**). The method was initially presented in [108]. Note that the switching frequency is not maintained constant, especially on transients. The simulation results are presented in **Fig. 5.23**.

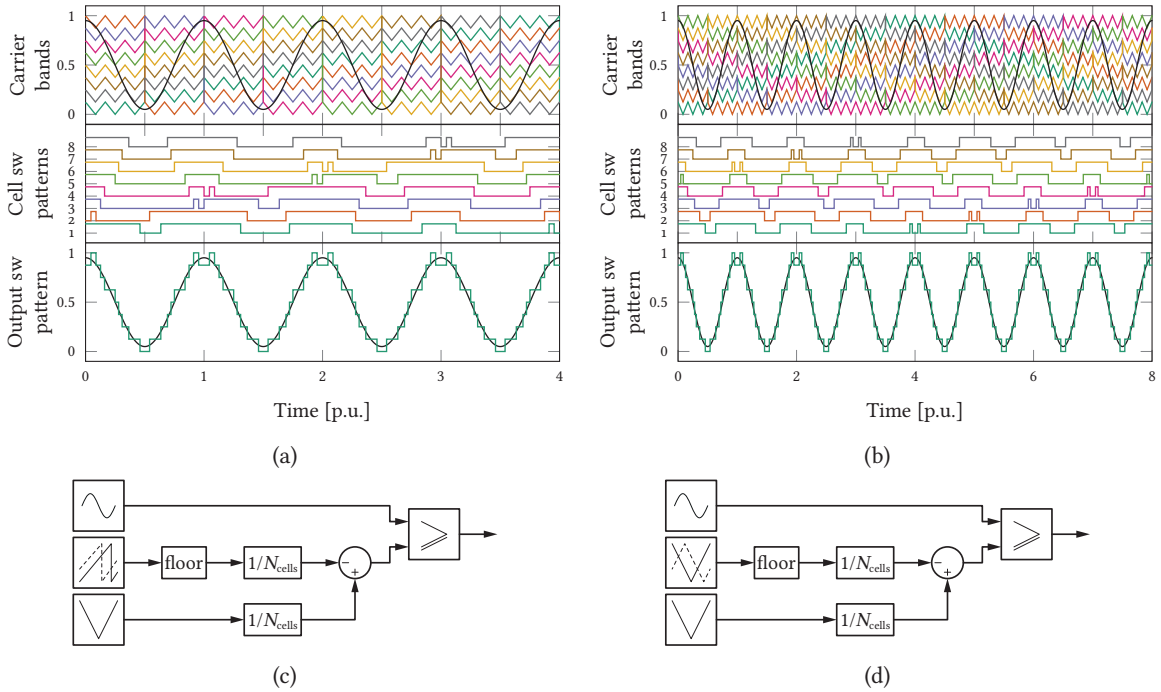


Fig. 5.20 Carrier swapping principle for $N_{\text{cells}} = 8$ (unipolar cells), $f_{\text{sw}} = 6f_g$ and $n_{\text{swap}} = 3$ applied to PD-PWM: (a) sawtooth carrier swapping and (b) triangle carrier swapping. Their respective implementations are shown in (c) and (d). By construction, the swapping cycle is double for the triangle carrier swapping compared to the sawtooth carrier swapping. Both methods leads to the same resulting switching pattern, as the meshes of carriers are identical.

Enhanced RSA (eRSA) with voltage error mitigation The voltage error due to the use of the number of inserted cells n regardless of their voltage value leads to voltage error between the reference branch voltage and actual one. Instead of using a sorting algorithm that takes as an input the number of inserted cells n, it'd be advantageous to compute the duty-cycle for the PWM switching cell for each half carrier period. This means each cell duty-cycle (either 0 or ±1 for the permanently inserted cells and d for the PWM switching cell) prior of the gate signals generation (cf. **Fig. 5.24**). Note that such an enhancement only makes sense for the closed-loop control (cf. **Sec. 4.2.4**).

Predictive methods All the previous presented methods are relying on a sampled value of v_{Cxyz} (with a time delay), but do not account for its evolution over the next time interval over which the switching signals are assigned. In [124], a predictive sorting algorithm is proposed. The objective is to evenly distribute the charge transfer among all cells of a branch. An average cell switching frequency of 130 Hz was obtained, however circulating current control capability was lost, necessitating the use of a main-circuit filter.

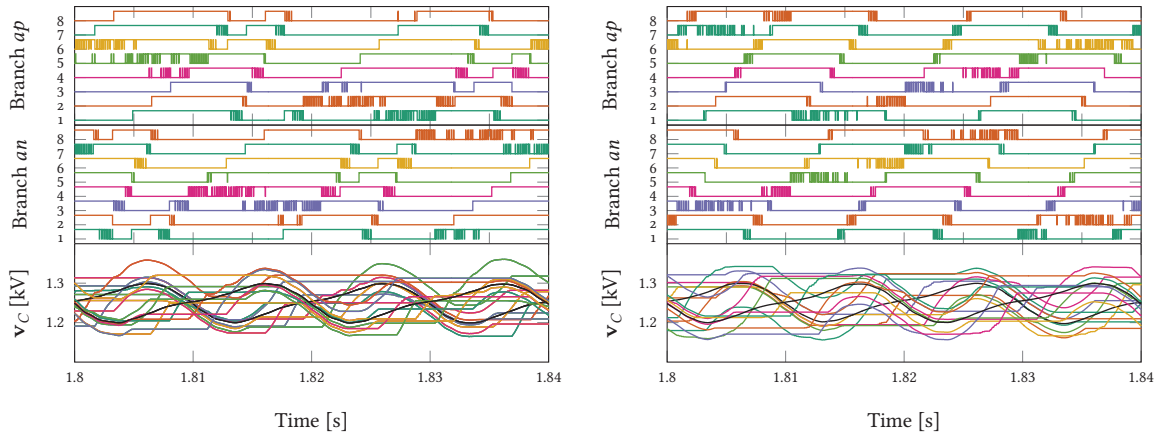


Fig. 5.21 Carrier swapping performance with $N_{\text{cells}} = 8$, $f_{\text{sw,app}} = 5\,\text{kHz}$ and $n_{\text{swap}} = 8$: (a) sawtooth carrier swapping and (b) triangular carrier swapping. The average cell switching frequency is 730 Hz.

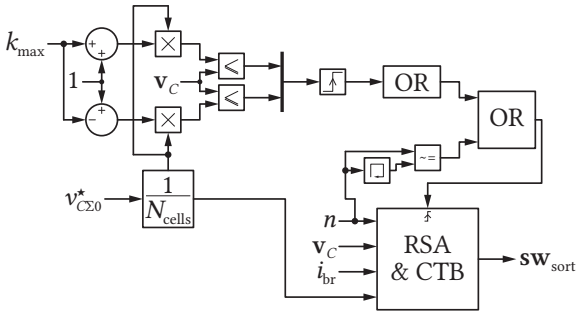


Fig. 5.22 RSA augmented with cell voltage tolerance band constraint.

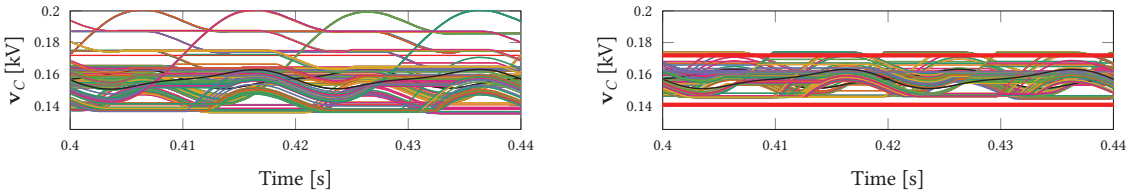


Fig. 5.23 RSA limitations with low average cell switching frequency for NLM with $N_{\text{cells}} = 64$: (a) RSA without cell voltage constraint, $\bar{f}_{\text{sw,avg}} = 43\,\text{Hz}$, and (b) RSA augmented with cell voltage constraint ($k_{\text{max}} = 0.1$), $\bar{f}_{\text{sw,avg}} = 53\,\text{Hz}$. The cell capacitor voltages are sampled at a fixed frequency $f_{\text{samp}} = 6\,\text{kHz}$, hence the voltage bounds are most of the time not exactly respected.

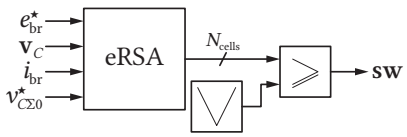


Fig. 5.24 ERSA scheme with voltage error mitigation.

5.3 Discussion

In **Figs. 5.25** and **5.26**, PS-PWM with a MAF and eRSA are compared for both $N_{\text{cells}} + 1$ and $2N_{\text{cells}} + 1$ modulations. For $N_{\text{cells}} + 1$ modulation, **Fig. 5.25(b)** gives the best results: low sensitivity to double switching despite a low average cell switching frequency, lowest ripple on the dc current. For $2N_{\text{cells}} + 1$, **Fig. 5.26(a)** gives the best results. As already mentioned, the branch current ripple is significantly inferior with $N_{\text{cells}} + 1$ modulation compared to $2N_{\text{cells}} + 1$. Overall, the lowest current ripple is obtained with $N_{\text{cells}} + 1$ and eRSA. Even though the ripple content of the grid current is fairly similar to **Fig. 5.26(a)**, wide differences are observed in the dc current ripple. It is concluded that the quality of the obtained waveforms does not depend on the number of levels in the bus and phase voltages, but rather on the way the switching pulses are distributed. As a complement, the branch voltage errors are shown in **Fig. 5.27**. The branch voltage errors are similar in terms of range with a peak value around 3 % of the nominal cell voltage, but feature a high frequency ripple in the case of PS-PWM.

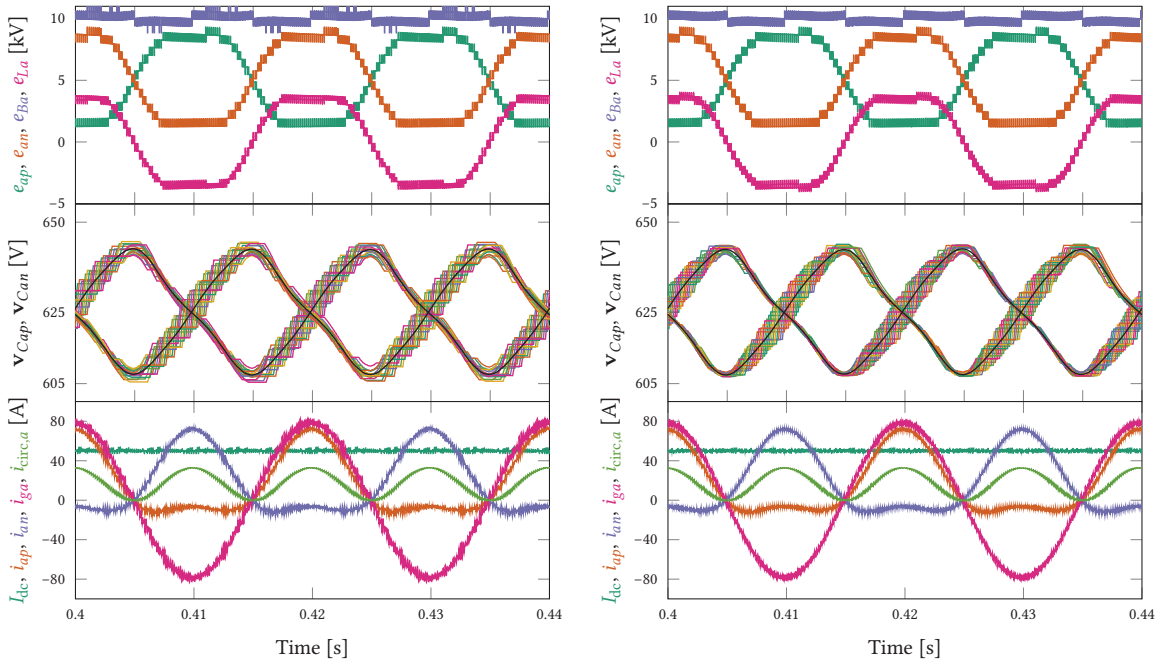


Fig. 5.25 Switched model performance comparison in inverter mode with $\overline{f_{\text{sw,br}}} = 6\,\text{kHz}$ and $N_{\text{cells}} + 1$ modulation: (a) PS-PWM with MAF and (b) eRSA. The control parameters are identical to **Tab. 4.2** and the respective phase-shifts from **Fig. 5.11**.

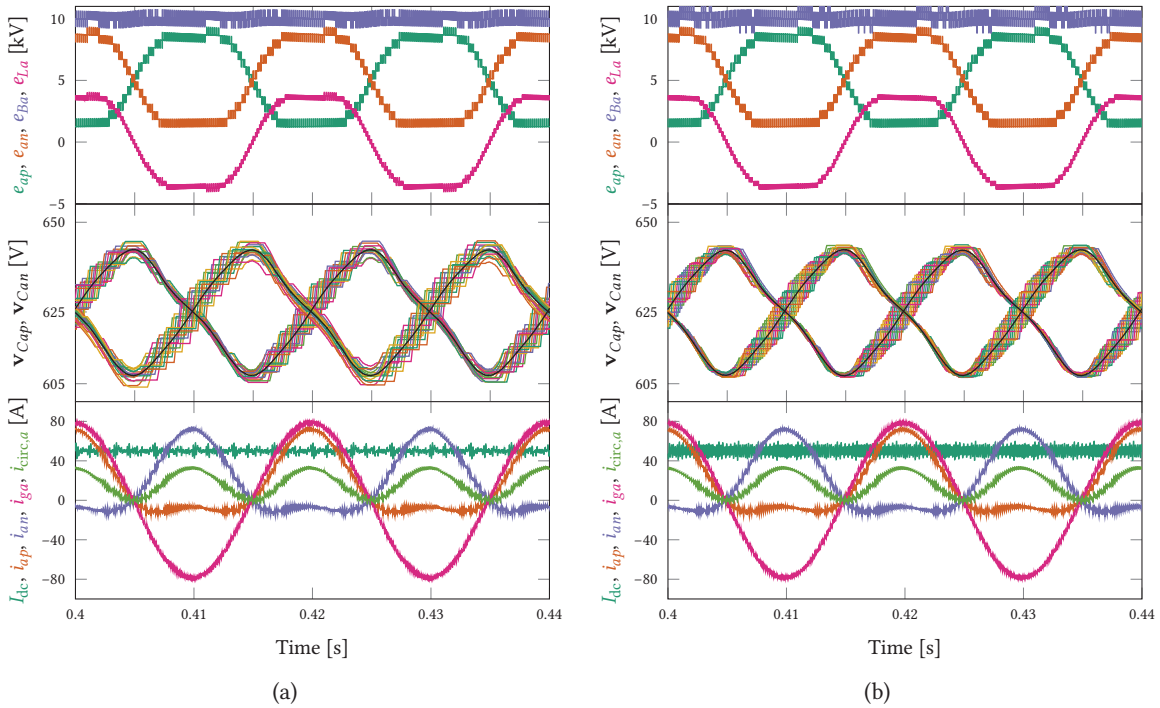


Fig. 5.26 Switched model performance comparison in inverter mode with $\overline{f_{sw,br}}$ = 6 kHz and $2N_{cells}$ + 1: (a) PS-PWM with a MAF and (b) eRSA. The control parameters are identical to **Tab. 4.2** and the respective phase-shifts from **Fig. 5.11**.

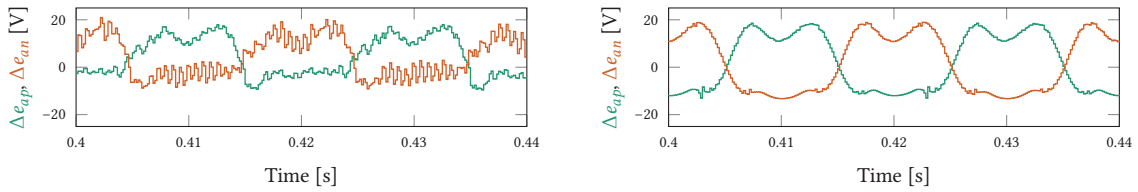


Fig. 5.27 Branch voltage error with periodic average and delay compensation for the operating point corresponding to **Figs. 5.25** and **5.26**: (a) PS-PWM with MAF and $2N_{cells}$ + 1 modulation and (b) eRSA with N_{cells} + 1 modulation.

6

The galvanically isolated modular converter

In the application foreseen in this work, which aims at dc/3-ac conversion between a $10\,\mathrm{kV_{dc}}$ *grid and a* $400\,\mathrm{V}$, $50\,\mathrm{Hz}$ *utility network, the large voltage step requires the use of a LFT for the voltage adaptation. The integration of the transformer within the MMC structure offers interesting perspectives, and this chapter derives two GIMC structures that are appropriate for its integration.*

6.1 Low frequency transformer integration

The conventional case, displayed in **Fig. 6.1**, consists of an MMC with an external LFT. It'll be considered as the basis upon which the integration of the LFT inside the MMC phase-leg is evaluated. This integration offers interesting perspectives when compared to the conventional case: the branch inductors are substituted with the leakage inductances of the LFT (hence no loss of controllability), the volume occupied by the magnetic components is potentially lower at the system level, combined with an eventual loss reduction.

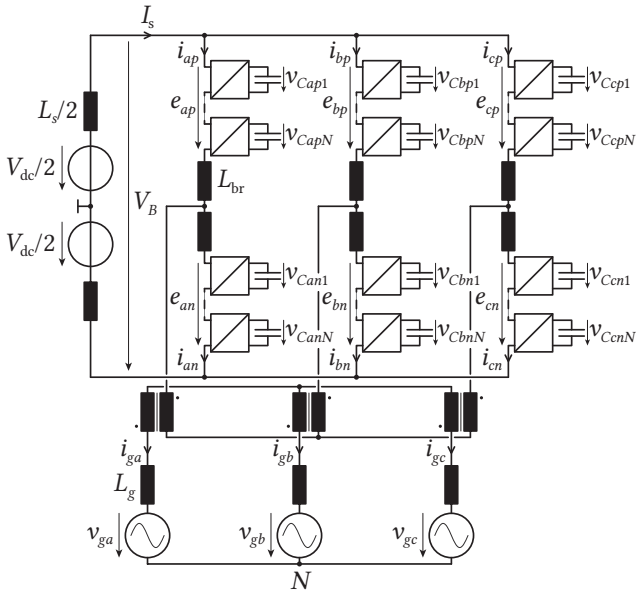


Fig. 6.1 Dc/3-ac MMC with external LFT.

Recently, several proposals have been made towards this direction. They will be critically presented, and the general requirements for a dc bias free magnetic structure will be derived.

6.1.1 Open-end windings MMC

6.1.1.1 Operation

A topology based on an open-end transformer was presented in [125], [126]. It will be further referred to as the open-end windings (OEW) MMC. Its scheme is presented in **Fig. 6.2(a)**. The operation differs from a classical dc/3-ac MMC, since the transformer's primary winding is series connected with the branches. This implies that the two branch currents are identical. In addition, each open-end terminal is swinging from the positive to the negative terminal. An illustration of the difference in operation is presented in **Fig. 6.3**, where:

$$e_p(t) = \frac{[1 - M\cos(\omega t)]\, V_{\mathrm{dc}}}{2} \qquad e_n(t) = \frac{[1 + M\cos(\omega t)]\, V_{\mathrm{dc}}}{2} \qquad \text{for the dc/3-ac MMC} \tag{6.1a}$$

$$e_{1O}(t) = \frac{M\cos(\omega t) V_{\mathrm{dc}}}{2} \qquad e_{2O}(t) = \frac{-M\cos(\omega t) V_{\mathrm{dc}}}{2} \qquad \text{for the OEW MMC} \tag{6.1b}$$

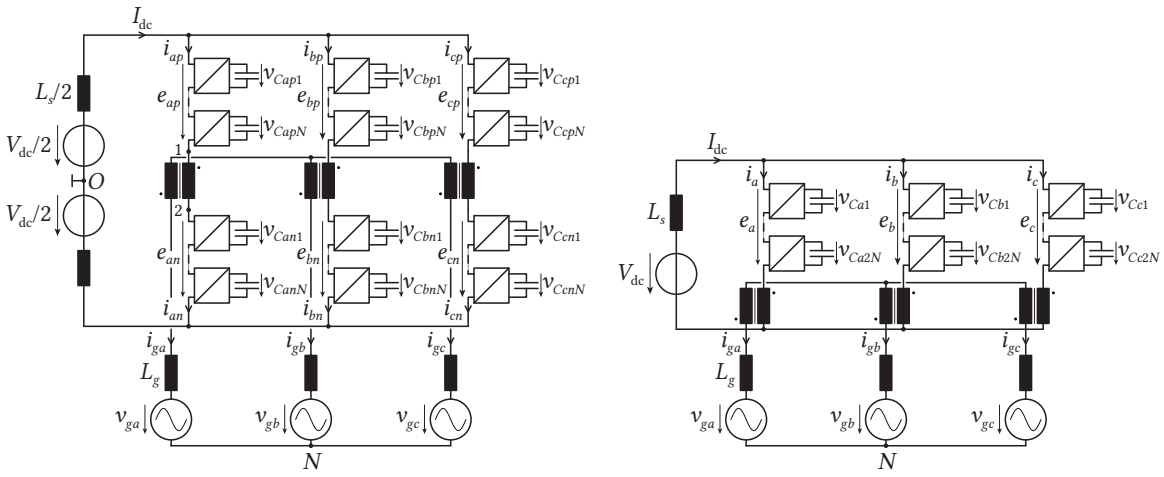


Fig. 6.2 OEW MMC: (a) original scheme as in [125], [126] and (b) re-drawn equivalent scheme with a single branch per phase.

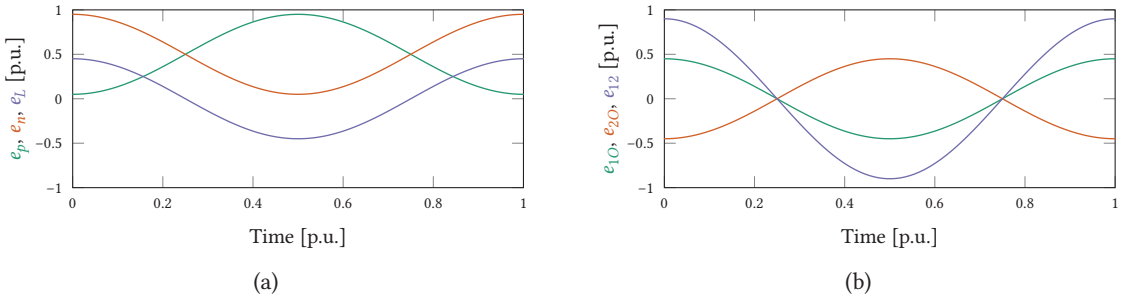


Fig. 6.3 Illustrative converter operation: (a) MMC and (b) OEW MMC, where 1 is the positive primary terminal, 2 the negative one and O the dc midpoint. The voltage base value is V_{dc}.

It follows that the voltage magnitude across the primary side of the LFT is double with the OEW

MMC ($e_{12} = e_{1O} - e_{2O}$) compared to the dc/3-ac MMC ($e_L = (-e_p + e_n)/2$). It is observed that the two branches within the same phase-leg receive the same modulation index. This motivates the merging of the branches into one in **Fig. 6.2(b)**. This reduction has implications on the control algorithm that will be discussed shortly after.

The comparison, and eventual advantage over a dc/3-ac MMC, cannot be solely based on the voltages across the primary side of the LFT. If one OEW MMC branch blocking capability is kept equal to one phase-leg blocking capability for the dc/3-ac MMC for the analysis, the branch current of the OEW MMC is expressed as:

$$i_{\mathrm{br}}(t) = \frac{I_{\mathrm{dc}}}{3} + \hat{i}'_g \cos(\omega t + \phi) + \hat{i}_\mu \cos\left(\omega t - \frac{\pi}{2}\right) \tag{6.2}$$

Both the dc and ac parts of the branch current are identical to the dc/3-ac MMC, assuming identical dc voltages. There is no ½ scaling of the grid current for the OEW MMC, but since the peak primary voltage is twice compared to the dc/3-ac MMC, they are identical magnitude wise. This means the branch requirements in terms of blocking voltage capability and current ratings for the OEW MMC branch is identical to one phase-leg of a dc/3-ac MMC.

A major drawback of the OEW MMC is that a dc current flows through the primary windings. This dc current impact cannot be mitigated by control means, since it is responsible for the active power transfer from the dc to the ac terminals. As a consequence, the transformer has to be designed accounting for this bias (cf. **Fig. 6.4**). In other words, it results in a poor magnetic material utilization, and an air-gap might be required, implying significantly higher leakage flux compared to an ungapped transformer.

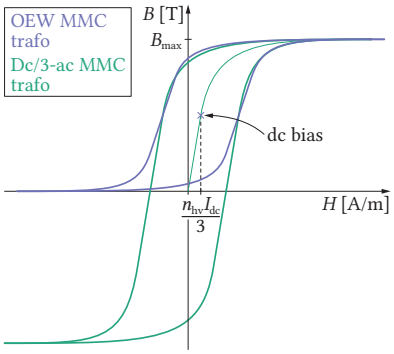


Fig. 6.4 Dc bias in the magnetic material for a positive power transfer from the dc to the ac terminals. In case of a negative power transfer, the *BH* curve would be shifted down. n_{hv} is the number of turns on the primary side of the transformer.

The OEW MMC suffers from further limitations. CM injection is not possible, as there is a path for the zero-sequence current that overlaps with the dc terminal current path. Harmonic circulating current injection is not possible either, as low order harmonics would appear at the ac terminals.

6.1.1.2 Power equations

The power equations can be derived based on the closed-loop steady-state variables. The branch current is ideally composed of a dc and fundamental ac component. The branch voltage is obtained

from the KVL:

$$i_{\mathrm{br}}(t) = \underbrace{\frac{I_{\mathrm{dc}}}{3}}_{\text{dc magn. current}} + \hat{i}'_g \cos\left(\omega t + \phi + \frac{2\pi(k-1)}{3}\right) + \underbrace{\hat{i}_\mu \cos\left(\omega t - \frac{\pi}{2}\right)}_{\text{ac magn. current}} \tag{6.3a}$$

$$e_{\mathrm{br}}(t) = V_{\mathrm{dc}} - \hat{v}'_g \cos\left(\omega t + \phi + \frac{2\pi(k-1)}{3}\right) - \underbrace{\left(R_{\mathrm{br}} i_{\mathrm{br}} + L_{\mathrm{br}} \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{br}}\right)}_{\text{branch impedance}} \tag{6.3b}$$

Then the (simplified) branch power equation is obtained as (for the phase $k = 1$):

$$p_{\mathrm{br}}(t) = \frac{I_{\mathrm{dc}} V_{\mathrm{dc}}}{3} - \frac{\hat{i}'_g \hat{v}'_g \cos(\phi)}{2} - \frac{\hat{i}'_g \hat{v}'_g \cos(2\omega t + \phi)}{2} - \frac{I_{\mathrm{dc}} \hat{v}'_g \cos(\omega t)}{3} + \hat{i}'_g V_{\mathrm{dc}} \cos(\omega t + \phi) \tag{6.4}$$

The branch energy ripple is given by:

$$\Delta W_{\mathrm{br}}(t) = -\frac{\hat{i}'_g \hat{v}'_g \sin(2\omega t + \phi)}{4\omega} - \frac{I_{\mathrm{dc}} \hat{v}'_g \sin(\omega t)}{3\omega} + \frac{\hat{i}'_g V_{\mathrm{dc}} \sin(\omega t + \phi)}{\omega} \tag{6.5}$$

Finally, the summed branch capacitor voltage and modulation index can be obtained in a similar manner as for the dc/3-ac MMC (cf. **Sec. 3.3**). The analysis result is shown in **Fig. 6.5**, with the parameters from **Tab. 6.1** and three different load angles. The summed branch capacitor voltages contain both fundamental and second harmonic ripple components.

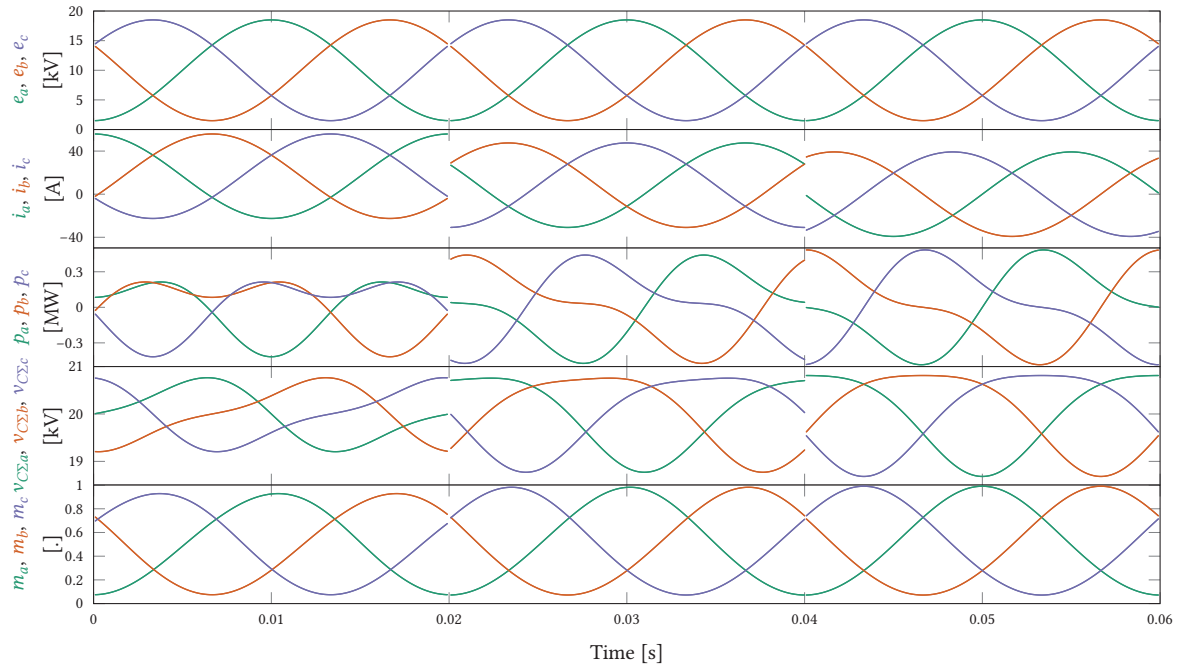


Fig. 6.5 OEW MMC power equation result for $S = 0.5\,\mathrm{MVA}$ with $\phi = [0,\ \pi/3,\ \pi/2]$ for each interval of 20 ms.

Since there is no possibility to shape the summed branch capacitor voltages through circulating current injection, direct modulation is expected to perform poorly for the OEW MMC. Note that the branch currents are identical to the positive branch currents of the dc/3-ac MMC in **Fig. 3.8(a)**.

Tab. 6.1 System parameters for the power equations analysis of the OEW MMC.

V_{dc}	10 kV	C_{br}	59.375 µF	S	0.5 MVA	f_g	50 Hz	k_{ac}	0.85

6.1.1.3 Control

In essence, the OEW MMC is a single star MMC. This has two implications: (i) the branch energy balancing control has to be redesigned and (ii) both the dc and ac currents are controlled through the branch current. In addition, the severe limitations of the OEW MMC (no CM nor harmonic circulating current injection) have to be accounted for.

The branch energy balancing control is modified, since the vertical balancing control is nonexistent. The balancing action has to be performed only through dc current components, else unwanted harmonics would appear at the ac terminals. This implies to filter the summed branch capacitor voltages in order to extract their dc component prior to their control in $\alpha\beta 0$ frame.

The branch currents are controlled in $\alpha\beta 0$ frame. The grid current reference is obtained from the desired active and reactive powers at the PCC. Dc contributions for the balancing control, ac components at fundamental frequency for the ac power control as well as two feed-forward terms, the dc current corresponding to the active power exchange and the magnetizing current, are collected to form the branch current reference. Given the multi-frequency content of the branch current spectrum, PI plus multi-resonant controllers are used.

$$\mathbf{i}^{\mathrm{FF}}_{\mu,\alpha\beta} = \frac{1}{\omega L_\mu}\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\mathbf{v}^{\mathrm{F}}_{g,\alpha\beta} \tag{6.6}$$

It is found that the circuit configuration is highly sensitive to CM harmonics in the branch currents. Thus, the zero-sequence control is augmented with a third harmonic resonant controller.

The control diagram for the inverter mode is shown in **Fig. 6.6**.

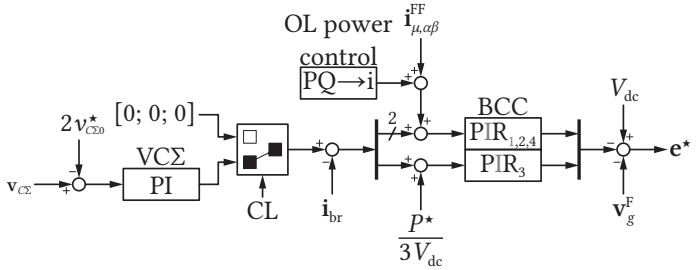


Fig. 6.6 OEW MMC control diagram in inverter mode.

The result for the average model simulation with closed-loop control is shown in **Fig. 6.7**. The circuit and control parameters are listed in **Tab. 6.2** and **Tab. 6.3**, respectively.

6.1.1.4 Topological improvement

In [127], an improvement to overcome the main drawback of the OEW MMC was proposed, with either a transformer zig-zag windings on the primary side (cf. **Fig. 6.8(a)**, which is identical to the

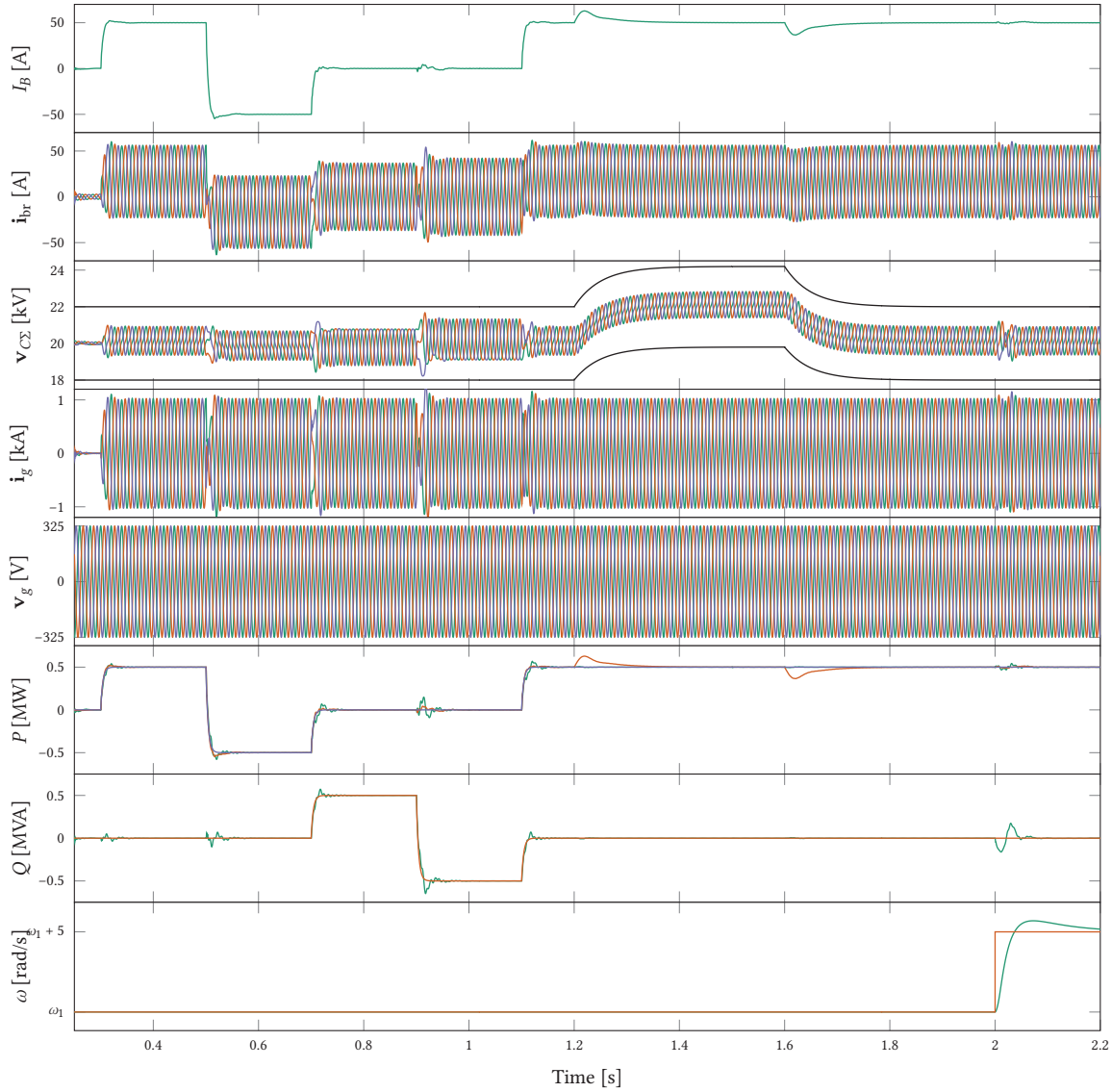


Fig. 6.7 OEW MMC in inverter mode with closed-loop control. For $t \in \{0.3\,\text{s}, 1.1\,\text{s}\}$, P and Q are stepped to S_{nom} and inversed. Between $t = 1.2\,\text{s}$ and $t = 1.6\,\text{s}$, $v_{C\Sigma 0}^{\Sigma\star}$ is varied. Finally, at $t = 2\,\text{s}$, ω is increased by 5 rad/s.

half-wave bridge MMC originally proposed in [128]) or the addition of dc cancellation windings (cf. **Fig. 6.8(b)**). In any case, the transformer complexity has to be significantly increased and no change in the dynamic response is observed when compared to the base case presented in **Sec. 4.3.1**.

6.1.1.5 Discussion

While the OEW MMC proposal looks highly interesting at first sight, it is clear that the open-end transformer configuration comes at the expense of severe design constraints, since a dc current bias has to be considered for the transformer design, and operation limitations as well, since the CM voltage and harmonic circulating current injections are not possible. Despite addressing this issue

Tab. 6.2 System parameters for the OEW MMC.

Parameter	Value
V_{dc}	10 kV
$f_{\mathrm{sw,app}}$	5 kHz
T_d	$1.5/f_{\mathrm{sw,app}}$
L_{br}	2.5 mH
R_{br}	0.1 Ω
C_{br}	59.375 µF
$\hat{v}_g$	325 V
f_g	50 Hz
L_g	0 H
R_g	0 Ω
L_μ	10 H
L_σ	0 H
$n_{\mathrm{HV}}/n_{\mathrm{LV}}$	26 : 1

Tab. 6.3 Controller parameters for the OEW MMC.

Controller	Parameter	Value
PLL	$\alpha_{p,\mathrm{PLL}}$	50 rad/s
	$\alpha_{ip,\mathrm{PLL}}$	10 rad/s
BCC	α_{BCC}	$2\pi f_{\mathrm{sw,app}}/10$
	$\alpha_{h,\mathrm{BCC}}$	200 rad/s
VCΣ	α_{hor}	$\alpha_{\mathrm{CCC}}/15$
	$\alpha_{h,\mathrm{hor}}$	2 rad/s
LPF	$\omega_{f,\mathrm{grid}}$	250 rad/s

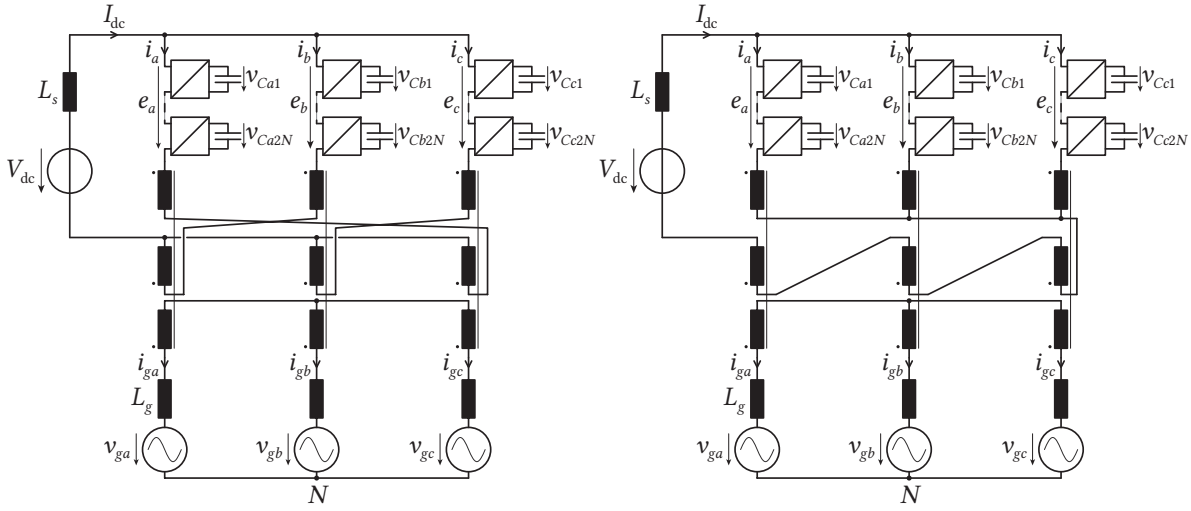


Fig. 6.8 OEW MMC topological improvements: (a) transformer with zig-zag windings and (b) transformer with dc cancellation windings. In both cases, the dc bias cancellation in the magnetic material is achieved.

by topological improvements, there is no clear advantage over the dc/3-ac MMC in terms of branch blocking voltage or current ratings, nor energy requirements.

6.1.2 Isolated dc/dc MMC

The topology was originally proposed as a high voltage isolated dc/dc converter in [129]. Unlike the OEW MMC, two branches from each converter side are coupled by a magnetic structure. This enables the cancellation of the dc component of the branch current inside the magnetic material (I_{dc1} and I_{dc2} have opposite signs), hence the magnetic material utilization is maximized. Note that in real operation, for balancing reasons and also due to transformer non-idealities, a small dc bias

component might remain in the transformer. An ac component, whose frequency is also a design parameter leading to energy requirement reduction, is circulated between the two branches of the same converter side and is used for power transfer between the two converter sides. Conceptually, it shares great similarities with the Front-to-Front MMC it inspired [130]. The scheme in **Fig. 6.9** shows the minimal configuration with two branches per dc terminal.

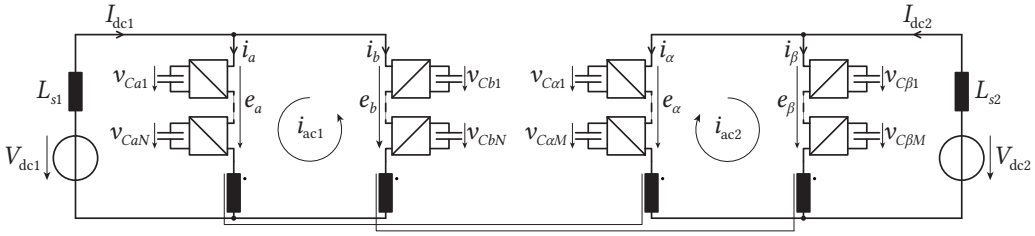


Fig. 6.9 Isolated dc/dc MMC.

6.1.3 General requirements for a dc free magnetic structure

Both the OEW MMC and the isolated dc/dc MMC are similar in terms of phase-leg structure, resulting in identical branch blocking voltage and current capability requirements. Also, no improvement over the energy storage requirement compared to a dc/3-ac MMC is obtained. Since the dc bias cancellation can not be achieved by control means (as this is the only frequency component able to exchange non-zero mean power with the dc terminals), a suitable windings configuration has to provide it. A multi-winding transformer is a good candidate. As shown in **Fig. 6.10**, depending whether the branches are parallel or series-connected, two different windings arrangements are used.

When the windings are parallel-connected (cf. **Fig. 6.10(a)**), the dc currents are summed at the star connection, implying a dc return, while the ac current is common to the two primary windings of each phase. When the windings are series-connected (cf. **Fig. 6.10(b)**), the opposite happens. The ac current flows out from the star connection, implying a star connection on the primary side, while the dc current is common. In that way, the dc flux cancellation in the magnetic material is effective. Unlike a zig-zag transformer, where the primary side only comprises three terminals with a "grounded" star, which translates into a single-star MMC, the identified multi-winding transformer configurations have six terminals on the primary side, which translates into a double-star MMC. In such a way, the severe limitations of the OEW MMC are avoided with the derived structures.

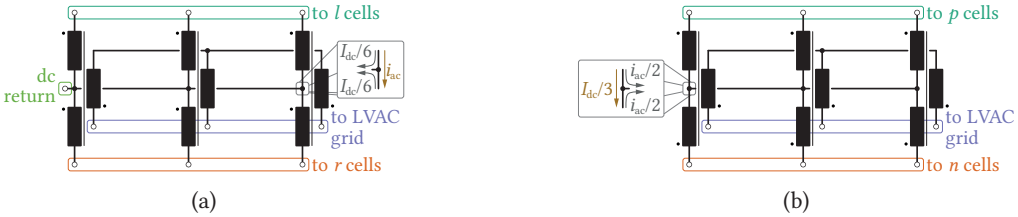


Fig. 6.10 Multi-winding transformer configurations to achieve the dc bias cancellation in the magnetic material, along with the current composition: (a) for the case of parallel-connected branches and (b) for the case of series-connected branches. The l and r cells are defined as the set of cells from the left and right parallel branch, as shown in **Fig. 6.11(a)**.

6.2 The galvanically isolated modular converter

6.2.1 Fundamental structures

Two converter structures employing the transformer configurations previously identified have been proposed in [131], [132] under the names "Modular Push-Pull PWM Converter" and "MMC applying a three-windings transformer", respectively. Their phase-legs are identical, with the difference that the primary winding midpoint is connected to the dc minus terminal in the first case and to a virtual star connection with the other midpoints of the other phases in the second. These converter structures will be further referred to as GIMC. The "folded" version will be referred to as the iGIMC and the "unfolded" one as the sGIMC (cf. **Fig. 6.11**). Note that only the iGIMC is suitable for DC/1-AC conversion with only two branches. No detailed studies of these topologies have been carried in the literature so far. The current and subsequent chapters aim at filling this gap.

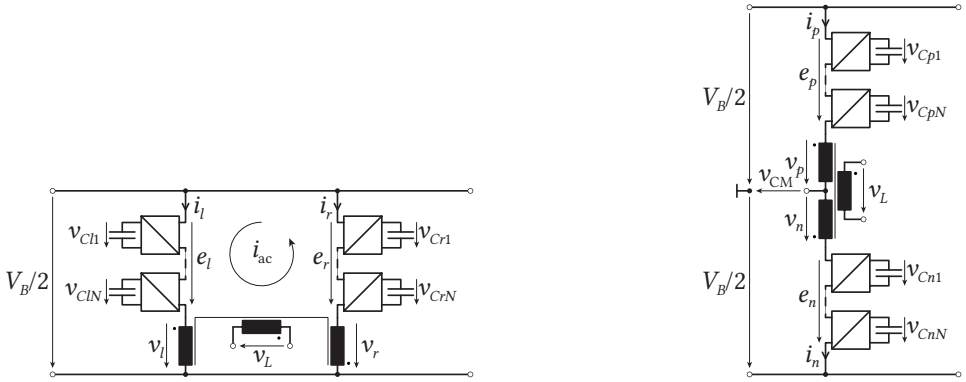


Fig. 6.11 GIMC phase-legs: (a) interleaved GIMC and (b) stacked GIMC, connected to a dc bus of $V_{\mathrm{dc}}/2$ and V_{dc}, assuming identical branch blocking voltages.

6.2.2 Modeling

The modeling is carried out separately for the two GIMC topologies, due to different transformer configurations. However, it'll be shown in a second step that the obtained state-space models share great similarities.

6.2.2.1 External circuits

The terminal circuits are common among the GIMC (cf. **Fig. 6.12**). They are described once (note that **Fig. 6.12(a)** and **Fig. 6.12(b)** are described by the same differential equation):

$$\frac{V_B}{2} = \frac{L_s}{2}\frac{\mathrm{d}}{\mathrm{d}t}I_B + \frac{R_s}{2}I_B + \frac{V_{\mathrm{dc}}}{2} \tag{6.7a}$$

$$v_L = L_g\frac{\mathrm{d}}{\mathrm{d}t}i_g + R_g i_g + v_g \tag{6.7b}$$

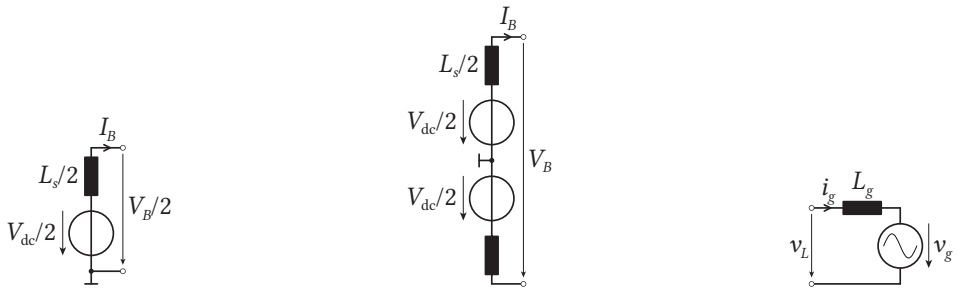


Fig. 6.12 External circuits: (a) dc side circuit for the iGIMC, (b) dc side circuit for the sGIMC and (c) common ac side circuit.

6.2.2.2 Three-winding transformer

To set the conventions, a three-winding transformer (cf. **Fig. 6.13**) is analyzed. Each GIMC variant will be then expressed by a simple mapping of the winding voltages and currents.

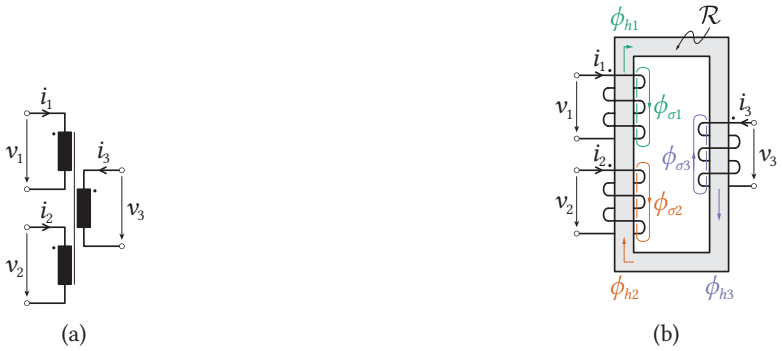


Fig. 6.13 Generic three-winding transformer: (a) electrical circuit with polarity convention and (b) magnetic circuit, with the core's reluctance $\mathcal{R}$.

Starting from the flux definitions:

$$\begin{bmatrix}\phi_1\\ \phi_2\\ \phi_3\end{bmatrix} = \begin{bmatrix}1 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & 1\end{bmatrix}\begin{bmatrix}\phi_{\sigma1}\\ \phi_{\sigma2}\\ \phi_{\sigma3}\end{bmatrix} + \begin{bmatrix}1 & 1 & 1\\ 1 & 1 & 1\\ 1 & 1 & 1\end{bmatrix}\begin{bmatrix}\phi_{h1}\\ \phi_{h2}\\ \phi_{h3}\end{bmatrix} \tag{6.8}$$

with $\phi_{\sigma x}$ the leakage flux and ϕ_{hx} the main flux ($\lambda_x = N_x\phi_x$). The flux linkages λ are obtained by multiplication per row with the turns number:

$$\begin{bmatrix}\lambda_1\\ \lambda_2\\ \lambda_3\end{bmatrix} = \begin{bmatrix}N_1 & 0 & 0\\ 0 & N_2 & 0\\ 0 & 0 & N_3\end{bmatrix}\begin{bmatrix}\phi_{\sigma1}\\ \phi_{\sigma2}\\ \phi_{\sigma3}\end{bmatrix} + \begin{bmatrix}N_1 & N_1 & N_1\\ N_2 & N_2 & N_2\\ N_3 & N_3 & N_3\end{bmatrix}\begin{bmatrix}\phi_{h1}\\ \phi_{h2}\\ \phi_{h3}\end{bmatrix} \tag{6.9}$$

The fluxes are replaced by their magnetic circuit equivalents ($\phi\_x = N_x \mathcal{P}\_ i_x$):

$$\begin{bmatrix} \lambda_1 \\ \lambda_2 \\ \lambda_3 \end{bmatrix} = \underbrace{\left(\begin{bmatrix} N_1^2 \mathcal{P}_{\sigma 1} & 0 & 0 \\ 0 & N_2^2 \mathcal{P}_{\sigma 2} & 0 \\ 0 & 0 & N_3^2 \mathcal{P}_{\sigma 3} \end{bmatrix} + \mathcal{P}_h \begin{bmatrix} N_1^2 & N_1 N_2 & N_1 N_3 \\ N_2 N_1 & N_2^2 & N_2 N_3 \\ N_3 N_1 & N_3 N_2 & N_3^2 \end{bmatrix} \right)}_{\mathbb{L}} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{6.10}$$

where $\mathcal{P}_h = 1/\mathcal{R}_h$. The self ($L_{xx}$) and mutual ($M_{xy}$) inductances are expressed through the inductance matrix:

$$\mathbb{L} = \begin{bmatrix} L_{11} & M_{12} & M_{13} \\ M_{21} & L_{22} & M_{23} \\ M_{31} & M_{32} & L_{33} \end{bmatrix} \tag{6.11}$$

which is symmetric, meaning $M_{xy} = M_{yx}$. The six inductances are expressed as:

$$L_{11} = N_1^2(\mathcal{P}_{\sigma 1} + \mathcal{P}_h) = L_{\sigma 1} + L_{h1} \tag{6.12a}$$
$$M_{12} = N_1 N_2 \mathcal{P}_h \tag{6.12b}$$
$$M_{13} = N_1 N_3 \mathcal{P}_h \tag{6.12c}$$
$$L_{22} = N_2^2(\mathcal{P}_{\sigma 2} + \mathcal{P}_h) = L_{\sigma 2} + L_{h2} \tag{6.12d}$$
$$M_{23} = N_2 N_3 \mathcal{P}_h \tag{6.12e}$$
$$L_{33} = N_3^2(\mathcal{P}_{\sigma 3} + \mathcal{P}_h) = L_{\sigma 3} + L_{h3} \tag{6.12f}$$

When inserted into the GIMC structure, the multi-winding transformer has two similar windings on the primary side. The turns numbers are defined as:

- $N_1 = N_2 = n_{\mathrm{HV}}$ for the primary side
- $N_3 = n_{\mathrm{LV}}$ for the secondary side

achieving the transformation ratio $n = n_{\mathrm{LV}}/n_{\mathrm{HV}}$. Consequently, the inductance matrix simplifies to:

$$\mathbb{L} = \begin{bmatrix} L_{\sigma,\mathrm{HV}} + L_{\mathrm{HV}} & L_{\mathrm{HV}} & M_{\mathrm{LV}} \\ L_{\mathrm{HV}} & L_{\sigma,\mathrm{HV}} + L_{\mathrm{HV}} & M_{\mathrm{LV}} \\ M_{\mathrm{LV}} & M_{\mathrm{LV}} & L_{\sigma,\mathrm{LV}} + L_{\mathrm{LV}} \end{bmatrix} \tag{6.13}$$

with $M_{\mathrm{LV}} = L_{\mathrm{LV}} n_{\mathrm{HV}}/n_{\mathrm{LV}}$ and $L_{\mathrm{LV}} = L_{\mathrm{HV}} n_{\mathrm{LV}}^2/n_{\mathrm{HV}}^2$. Finally, the terminal voltages are obtained by time derivation of the flux linkages, with the addition of the resistive voltage drops for each winding:

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} \lambda_1 \\ \lambda_2 \\ \lambda_3 \end{bmatrix} + \begin{bmatrix} R_{\mathrm{HV}} & 0 & 0 \\ 0 & R_{\mathrm{HV}} & 0 \\ 0 & 0 & R_{\mathrm{LV}} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \mathbb{L} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + \mathbb{R} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{6.14}$$

6.2.2.3 Interleaved GIMC

The mapping of the winding voltages and currents for the iGIMC compared to the generic case analyzed in **Sec. 6.2.2.2** to derive the inductance matrix of a three-winding transformer is given by:

$$v_1 = v_l \quad (6.15a) \qquad i_1 = i_l \quad (6.15d)$$
$$v_2 = -v_r \quad (6.15b) \qquad i_2 = -i_r \quad (6.15e)$$
$$v_3 = v_L \quad (6.15c) \qquad i_3 = -i_g \quad (6.15f)$$

The remaining two KVL equations to describe the phase-leg (cf. **Fig. 6.11(a)**) in addition to (6.15c) are:

$$\frac{V_B}{2} = e_l + v_l + v_{\mathrm{CM}} \quad (6.16a)$$
$$\frac{V_B}{2} = e_r + v_r - v_{\mathrm{CM}} \quad (6.16b)$$

The application of the mapping of (6.15) to (6.14) results into:

$$\frac{V_B}{2} = e_l + R_{\mathrm{HV}} i_l + (L_{\sigma,\mathrm{HV}} + L_{\mathrm{HV}}) \frac{\mathrm{d}}{\mathrm{d}t} i_l - L_{\mathrm{HV}} \frac{\mathrm{d}}{\mathrm{d}t} i_r - M_{\mathrm{LV}} \frac{\mathrm{d}}{\mathrm{d}t} i_g + v_{\mathrm{CM}} \quad (6.17a)$$
$$\frac{V_B}{2} = e_r + R_{\mathrm{HV}} i_r - L_{\mathrm{HV}} \frac{\mathrm{d}}{\mathrm{d}t} i_l + (L_{\sigma,\mathrm{HV}} + L_{\mathrm{HV}}) \frac{\mathrm{d}}{\mathrm{d}t} i_r + M_{\mathrm{LV}} \frac{\mathrm{d}}{\mathrm{d}t} i_g - v_{\mathrm{CM}} \quad (6.17b)$$
$$v_L = M_{\mathrm{LV}} \left(\frac{\mathrm{d}}{\mathrm{d}t} i_l - \frac{\mathrm{d}}{\mathrm{d}t} i_r \right) - (L_{\sigma,\mathrm{LV}} + L_{\mathrm{LV}}) \frac{\mathrm{d}}{\mathrm{d}t} i_g - R_{\mathrm{LV}} i_g \quad (6.17c)$$

The sum and difference of (6.17a) and (6.17b) provide the final set of differential equations with (6.17c):

$$V_B = e_l + e_r + R_{\mathrm{HV}} (i_l + i_r) + L_{\sigma,\mathrm{HV}} \left(\frac{\mathrm{d}}{\mathrm{d}t} i_l + \frac{\mathrm{d}}{\mathrm{d}t} i_r \right) \quad (6.18a)$$
$$0 = -e_l + e_r + R_{\mathrm{HV}} (-i_l + i_r) + (L_{\sigma,\mathrm{HV}} + 2L_{\mathrm{HV}}) \left(-\frac{\mathrm{d}}{\mathrm{d}t} i_l + \frac{\mathrm{d}}{\mathrm{d}t} i_r \right) + 2M_{\mathrm{LV}} \frac{\mathrm{d}}{\mathrm{d}t} i_g - 2v_{\mathrm{CM}} \quad (6.18b)$$
$$v_L = M_{\mathrm{LV}} \left(\frac{\mathrm{d}}{\mathrm{d}t} i_l - \frac{\mathrm{d}}{\mathrm{d}t} i_r \right) - (L_{\sigma,\mathrm{LV}} + L_{\mathrm{LV}}) \frac{\mathrm{d}}{\mathrm{d}t} i_g - R_{\mathrm{LV}} i_g \quad (6.18c)$$

6.2.2.4 Stacked GIMC

The mapping of the winding voltages and currents for the sGIMC compared to the generic case analyzed in **Sec. 6.2.2.2** to derive the inductance matrix of a three-winding transformer is given by:

$$v_1 = v_p \quad (6.19a) \qquad i_1 = i_p \quad (6.19d)$$
$$v_2 = -v_n \quad (6.19b) \qquad i_2 = -i_n \quad (6.19e)$$
$$v_3 = v_L \quad (6.19c) \qquad i_3 = -i_g \quad (6.19f)$$

The remaining two KVL equations to describe the phase-leg (cf. **Fig. 6.11(b)**) in addition to (6.19c) are:

$$\frac{V_B}{2} = e_p + v_p + v_{\mathrm{CM}} \quad (6.20a)$$

$$\frac{V_B}{2} = e_n + v_n - v_{\mathrm{CM}} \tag{6.20b}$$

The application of the mapping of (6.19) to (6.14) results into:

$$\frac{V_B}{2} = e_p + R_{\mathrm{HV}} i_p + (L_{\sigma,\mathrm{HV}} + L_{\mathrm{HV}}) \frac{\mathrm{d}}{\mathrm{d}t} i_p - L_{\mathrm{HV}} \frac{\mathrm{d}}{\mathrm{d}t} i_n - M_{\mathrm{LV}} \frac{\mathrm{d}}{\mathrm{d}t} i_g + v_{MO} \tag{6.21a}$$

$$\frac{V_B}{2} = e_n + R_{\mathrm{HV}} i_n - L_{\mathrm{HV}} \frac{\mathrm{d}}{\mathrm{d}t} i_p + (L_{\sigma,\mathrm{HV}} + L_{\mathrm{HV}}) \frac{\mathrm{d}}{\mathrm{d}t} i_n + M_{\mathrm{LV}} \frac{\mathrm{d}}{\mathrm{d}t} i_g - v_{MO} \tag{6.21b}$$

$$v_L = -R_{\mathrm{LV}} i_g + M_{\mathrm{LV}} \left(\frac{\mathrm{d}}{\mathrm{d}t} i_p - \frac{\mathrm{d}}{\mathrm{d}t} i_n \right) - (L_{\sigma,\mathrm{LV}} + L_{\mathrm{LV}}) \frac{\mathrm{d}}{\mathrm{d}t} i_g \tag{6.21c}$$

The sum and difference of (6.21a) and (6.21b) provide the final set of differential equations with (6.21c):

$$V_B = e_p + e_n + R_{\mathrm{HV}} \left(i_p + i_n \right) + L_{\sigma,\mathrm{HV}} \left(\frac{\mathrm{d}}{\mathrm{d}t} i_p + \frac{\mathrm{d}}{\mathrm{d}t} i_n \right) \tag{6.22a}$$

$$0 = -e_p + e_n + R_{\mathrm{HV}} \left(-i_p + i_n \right) + (L_{\sigma,\mathrm{HV}} + 2L_{\mathrm{HV}}) \left(-\frac{\mathrm{d}}{\mathrm{d}t} i_p + \frac{\mathrm{d}}{\mathrm{d}t} i_n \right) + 2M_{\mathrm{LV}} \frac{\mathrm{d}}{\mathrm{d}t} i_g - 2v_{MO} \tag{6.22b}$$

$$v_L = M_{\mathrm{LV}} \left(\frac{\mathrm{d}}{\mathrm{d}t} i_p - \frac{\mathrm{d}}{\mathrm{d}t} i_n \right) - (L_{\sigma,\mathrm{LV}} + L_{\mathrm{LV}}) \frac{\mathrm{d}}{\mathrm{d}t} i_g - R_{\mathrm{LV}} i_g \tag{6.22c}$$

6.2.3 Circuit simulations

The circuit simulations are performed on three-phase GIMC configurations (cf. **Fig. 6.14**). The transformers, appart from their connection points, share the same magnetic parameters (cf. **Tab. 6.4**). The similarities between the resulting models ((6.18) and (6.22)) are obvious, justifying to make no distinction between the two GIMC variants. The dc bias cancellation is effective, since there is no term $L_{\mathrm{HV}} \left(\frac{\mathrm{d}}{\mathrm{d}t} i_l + \frac{\mathrm{d}}{\mathrm{d}t} i_r \right)$ or $L_{\mathrm{HV}} \left(\frac{\mathrm{d}}{\mathrm{d}t} i_p + \frac{\mathrm{d}}{\mathrm{d}t} i_n \right)$, that would imply a dc flux in the magnetic material. As the obtained models are identical to a dc/3-ac MMC, the same control methods previously discussed in **Chap. 4** can be applied. Both sGIMC and iGIMC are operated in inverter mode (cf. **Sec. 4.3.1**), with the same branch ratings as the dc/3-ac MMC. This means the sGIMC is connected to a 10 kV dc bus, while the iGIMC is connected to a 5 kV one. For the same power, the bus current for the iGIMC is double compared to the sGIMC.

The results with closed-loop control shown in **Fig. 6.15** and **Fig. 6.16** confirm the dc bias free operation, since the magnetizing currents $\mathbf{i}_\mu$ are purely ac. The same scenario as in **Fig. 6.7** is applied. Note that the magnetizing currents are measured on the primary side, unlike the grid voltages and currents, which are measured on the secondary (low-voltage) side.

Tab. 6.4 GIMC transformer parameters.

$L_{\sigma,\mathrm{HV}}$	2.5 mH	$L_{\sigma,\mathrm{LV}}$	1 µH	$R_{\sigma,\mathrm{HV}}$	0.1 Ω	$R_{\sigma,\mathrm{LV}}$	0.01 Ω	L_μ	100 mH

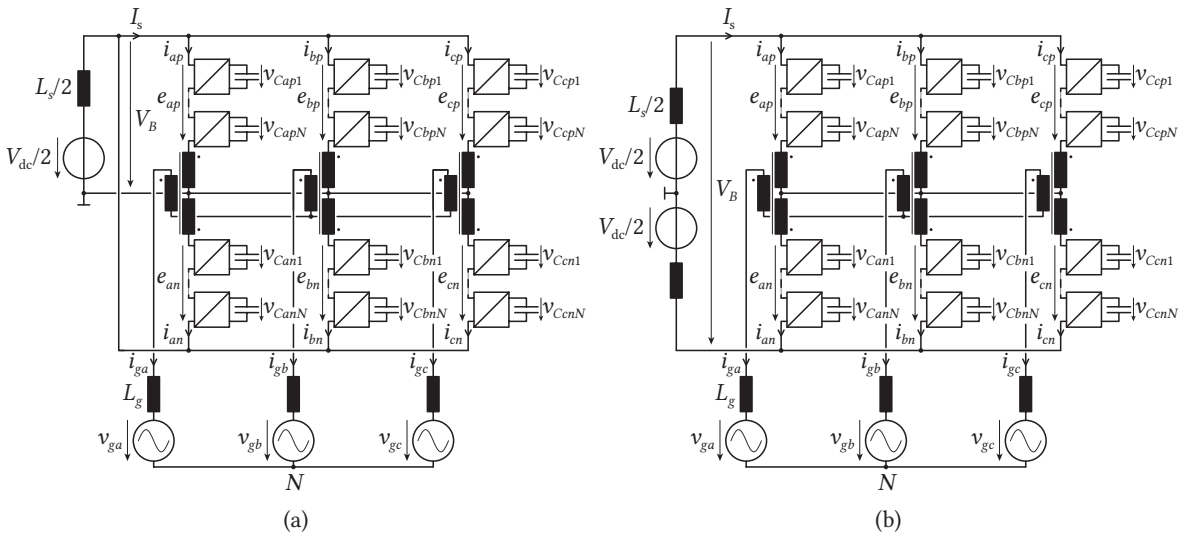


Fig. 6.14 Three-phase GIMC: (a) iGIMC and (b) sGIMC.

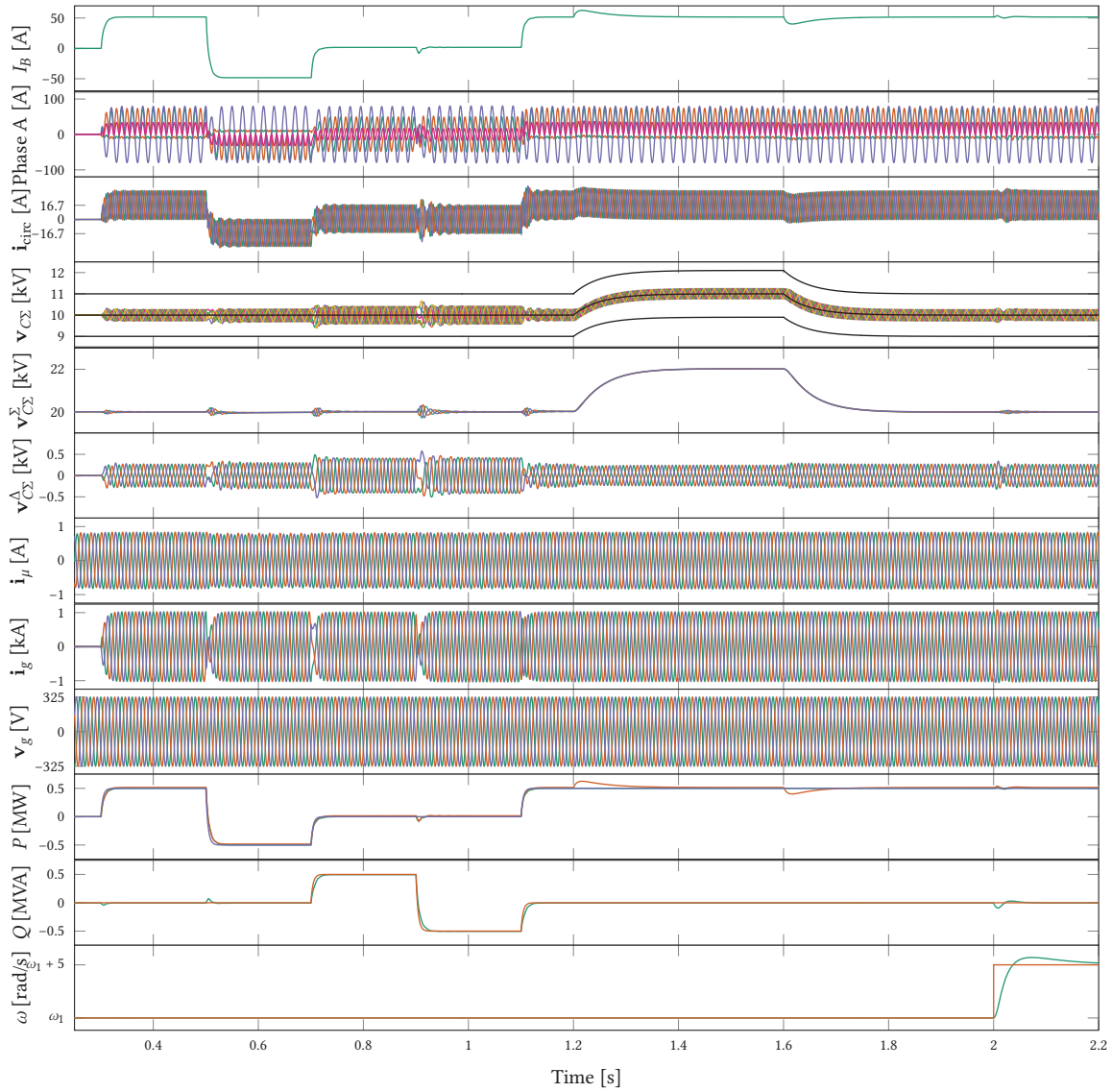


Fig. 6.15 sGIMC in inverter mode with closed-loop control and 2nd harmonic injection. For $t \in \{0.3\,\text{s}, 1.1\,\text{s}\}$, P and Q are stepped to S_{nom} and inversed. Between $t = 1.2\,\text{s}$ and $t = 1.6\,\text{s}$, $v^{\Sigma\star}_{C\Sigma 0}$ is varied. Finally, at $t = 2\,\text{s}$, ω is increased by 5 rad/s.

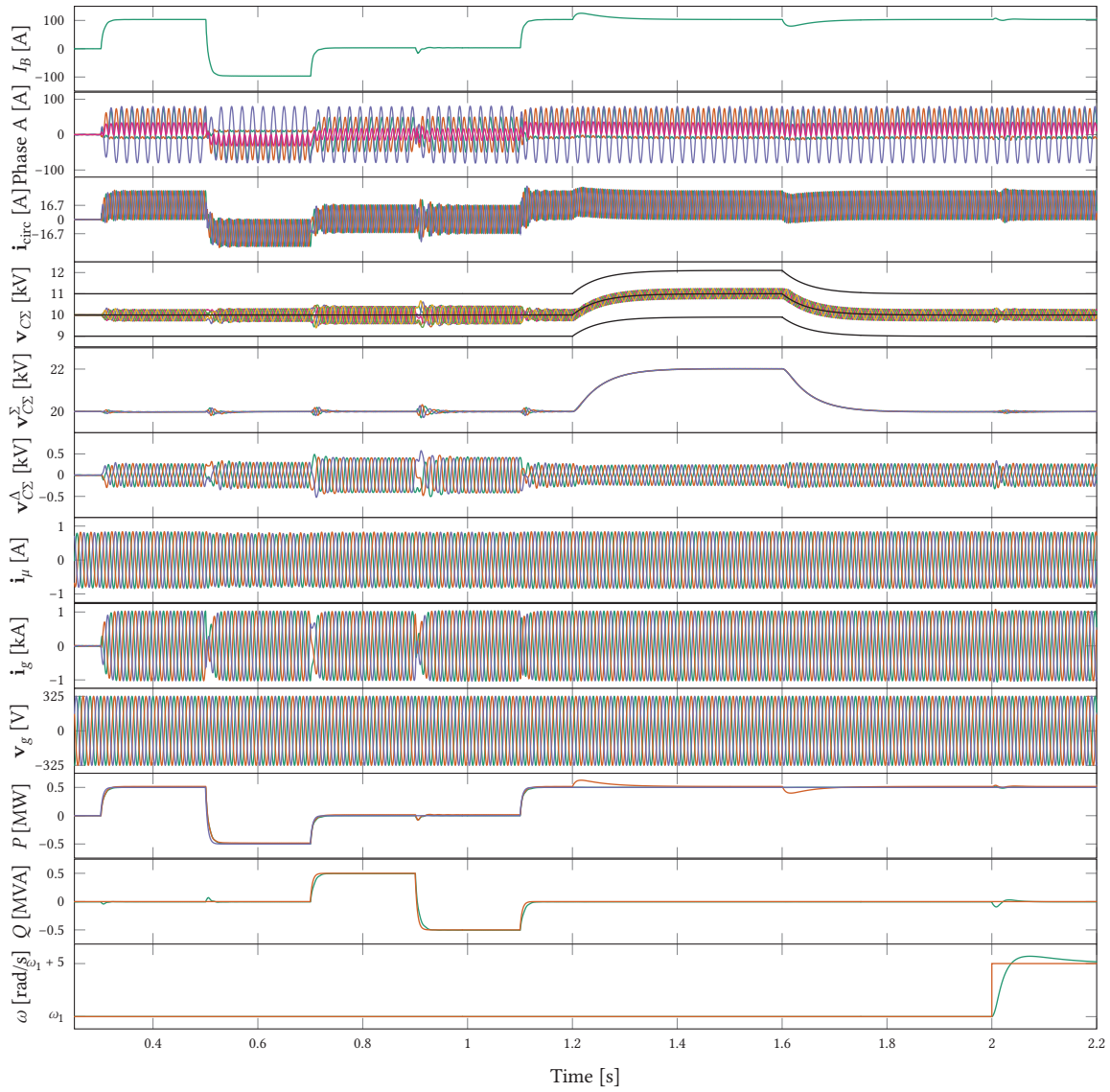


Fig. 6.16 iGIMC in inverter mode with closed-loop control and 2nd harmonic injection. For $t \in \{0.3\,\text{s}, 1.1\,\text{s}\}$, P and Q are stepped to S_{nom} and inversed. Between $t = 1.2\,\text{s}$ and $t = 1.6\,\text{s}$, $v^{\Sigma\star}_{C\Sigma 0}$ is varied. Finally, at $t = 2\,\text{s}$, ω is increased by 5 rad/s.

6.3 Discussion

This chapter has critically evaluated two proposals for the LFT integration. On one hand, the OEW MMC was questioned due to the presence of a dc bias in the transformer, which is detrimental for any practical implementation, and the impossibility to use CM or harmonic circulating current injection, which limits the SOA of the converter and offers no possibility to reduce the converter energy requirement. On the other hand, the isolated dc/dc MMC was much more interesting, since its configuration was suitable to achieve the dc bias cancellation in the transformer. Consequently, the requirements for a dc free magnetic structure were outlined. This resulted in the need for a three-winding transformer.

As a follow up, two sibling structures based on a three-windings transformer, the iGIMC and the sGIMC, were modeled. From the modeling point of view, no difference was found compared to the conventional dc/3-ac MMC, implying that the control algorithms discussed in **Sec. 4.2** can be applied to the GIMC without restriction. Due to its arrangement, the sGIMC is indeed particularly well suited for the considered application in this thesis (step down from dc to ac), while the iGIMC is better suited for step up operation. The gains provided by the integrated magnetic structure, the three-windings GIMC transformer, are evaluated in the next chapter.

7
Magnetic components sizing

This chapter provides the design and a comparison between the dc/3-ac MMC with air-core branch inductors and external LFT and the GIMC, where the branch inductors are merged with the leakage inductances of the multi-windings transformer. The focus is set on the volume and efficiency estimates, in order to assess the impacts on the system level design.

7.1 Branch inductor design

7.1.1 Requirements

For the dc/3-ac MMC, the branch inductors are realized with an air-core design, due to the presence of a dc bias. The MMC branch inductance value selection is not straightforward and little agreement exist regarding its sizing [80], [133], [134]. Criteria, such as 2nd harmonic current limitation (in case no circulating current controller is present), branch current controllability (in case a circulating current controller is present), dc fault current limitation (relevant only for non fault blocking cell types, cf. **Sec. 3.1.2**) and branch current ripple limitation, are generally considered. The target branch inductance value is $L_{\mathrm{br}} = 2.5\,\mathrm{mH}$. The corresponding branch current rise in case of a dc fault is $1\,\mathrm{kA/ms}$.

For a $0.5\,\mathrm{MVA}$ converter with $V_{\mathrm{dc}} = 10\,\mathrm{kV}$, the branch current rms value is $56.7\,\mathrm{A}$ ($16.7\,\mathrm{A}$ for the dc current and $50\,\mathrm{A}$ rms for half the ac current at $50\,\mathrm{Hz}$). As a consequence, for a current density $J = 2\,\mathrm{A/mm^2}$, the wire cross-section is rounded to $30\,\mathrm{mm^2}$. Enamelled bare wire with square cross-section is selected (conductor side length $d_{\mathrm{cond}} = 5.5\,\mathrm{mm}$). Only designs with less than $40\,\mathrm{V}$ turn-to-turn voltage were considered. With $d_{\mathrm{vert}} = 1\,\mathrm{mm}$ the vertical spacing distance (turn to turn voltage difference) and $d_{\mathrm{horiz}} = 5\,\mathrm{mm}$ the horizontal spacing distance (layer to layer voltage difference, requiring some isolation material layer plus spacers), the rectangle winding area is completely defined. Note that the wire isolation is already included in d_{vert} and d_{horiz}.

7.1.2 Design algorithm

In the literature, several empirical formulas for the inductance of a multi-layer solenoid have been proposed. The decision was made to use the Welsby's formula in the case of a rectangular winding cross-section as shown in **Fig. 7.1** [135]:

$$L_{\mathrm{Welsby}} = \frac{\mu_0 N^2 \pi a^2}{b} \frac{1}{1 + 0.9\frac{a}{b} + 0.32\frac{c}{a} + 0.84\frac{c}{b}}\,[\mathrm{H}] \tag{7.1}$$

where a is the mean coil radius, b the winding length and c the winding height.

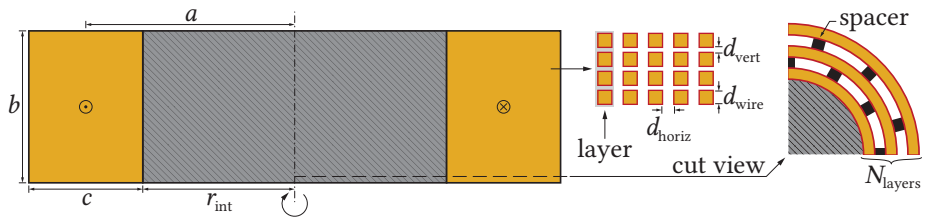


Fig. 7.1 Air-core inductor with rectangular winding cross-section. The cut view on one quarter of the cylinder presents the layer spacers for layer cooling and eventually isolation distance increase.

The air-core inductor is built around a drum, that serves as mechanical and mounting support. Thermal as well as short-circuit mechanical withstand constraints are not taken into account in the size estimation.

The expression (7.1) is evaluated for a set \$ = $\{N_{turns}, N_{layers}, r_{int}\}$. The variable r_{int} is preferred to a for the optimization set. The ranges are selected as: $N_{turns} = [10 : 850]$, $N_{layers} = [1 : 20]$ and $r_{int} = [1 : 0.1 : 200]$ (in [mm]). A subset for which L_{Welsby} is close to the design target inductance value is extracted and shown in **Fig. 7.2**. The best design in this subset is identified with the cost function:

$$J_{cost} = \sqrt{\left(\frac{l_{wire}}{10}\right)^2 + V_{tot}^2} \tag{7.2}$$

that finds the best compromise between the wire length (i.e. the dc resistance) and the total volume (including the drum). Only designs with equally distributed number of conductors per layer and constant horizontal spacing are considered.

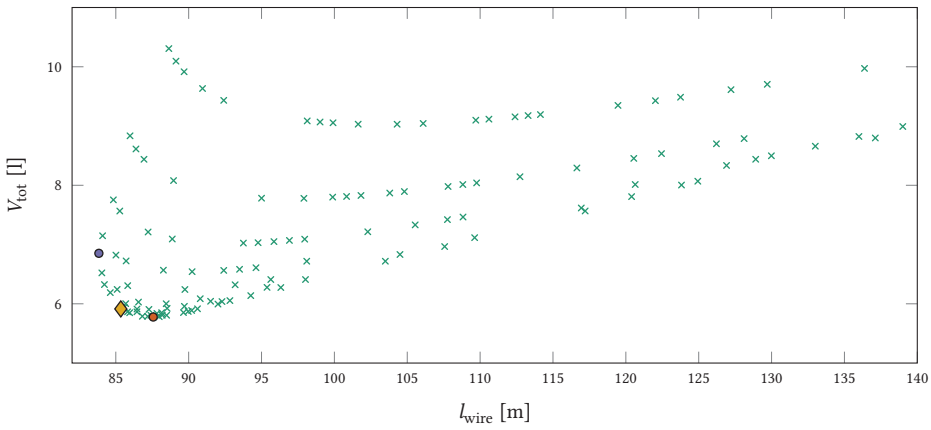


Fig. 7.2 V_{tot}–l_{wire} optimization result for the air-core branch inductor. A Pareto front is clearly visible. The design with the lowest dc resistance is shown with a blue dot, while the one with the lowest volume is shown with a red dot. The design that features the lowest value of the cost function defined in (7.2) is considered optimal and is marked with an orange diamond shape.

7.1.3 Design verification in finite element modeling (FEM)

The best design is {132, 12, 42.4 mm}, with a total volume slightly lower than 6 l. This design is verified in COMSOL Multiphysics©. The geometry is parametrized in a 2D axisymmetric model, reducing significantly the simulation times. Since (7.1) does not account for the packing factor, which depends on isolation requirements, r_{int} is adjusted first with a frequency study at 0.1 Hz. It is found that an inner radius of 46.9 mm is needed to reach the target inductance value (cf. **Fig. 7.3**). The magnetic flux density and magnetic field norm plots are shown in **Fig. 7.4**.

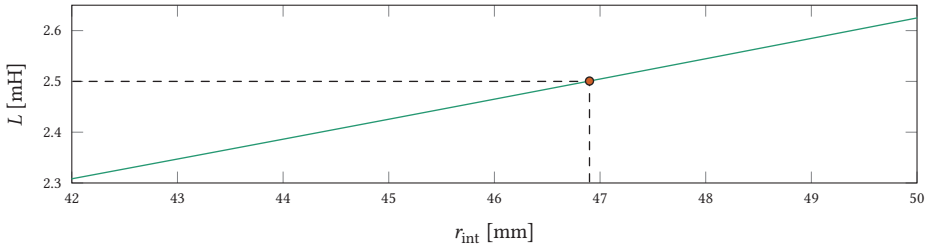
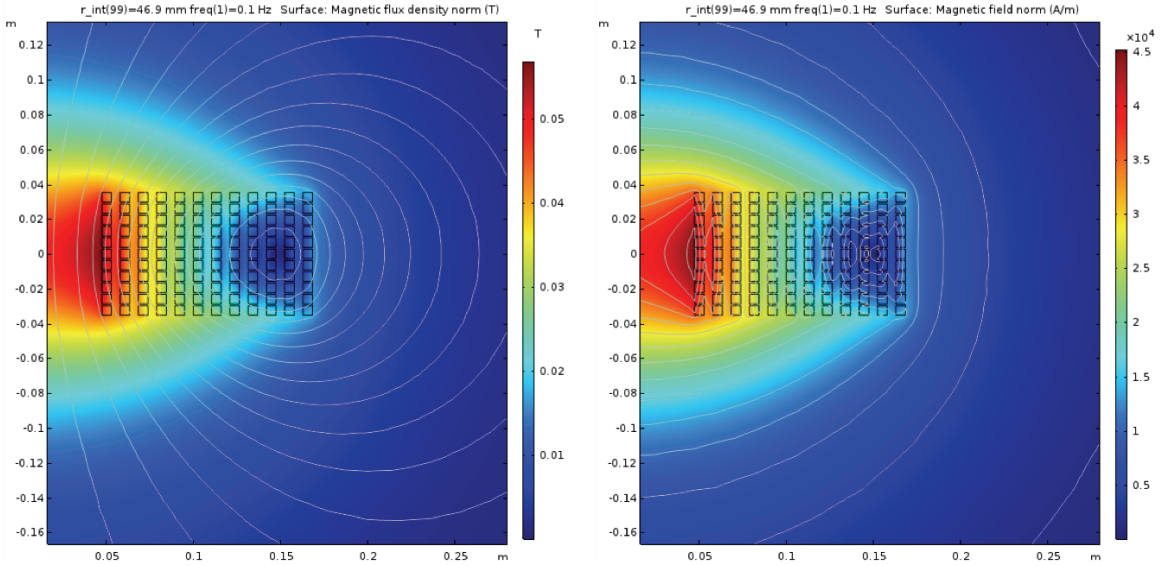


Fig. 7.3 Inner radius sweep result in COMSOL Multiphysics©. The required inner radius for obtaining 2.5 mH is 46.9 mm (shown in red).



(a) (b)

Fig. 7.4 Frequency study result in COMSOL Multiphysics© at 0.1 Hz for the optimal design: (a) magnetic flux density norm and (b) magnetic field norm.

Then, a frequency study with a frequency sweep $f \in 10^{[-1:.1:5]}$ Hz. **Fig. 7.5** shows the frequency evolution of the inductance value and ac resistance for the designed air-core inductor. The inductance value starts to drop at 100 Hz, with a reduction of 21.6 % at 100 kHz compared to the dc value. The ac resistance equals 49 mΩ until 100 Hz as well.

Fig. 7.6 shows the branch current fast Fourier transform (FFT) at nominal power. The copper losses

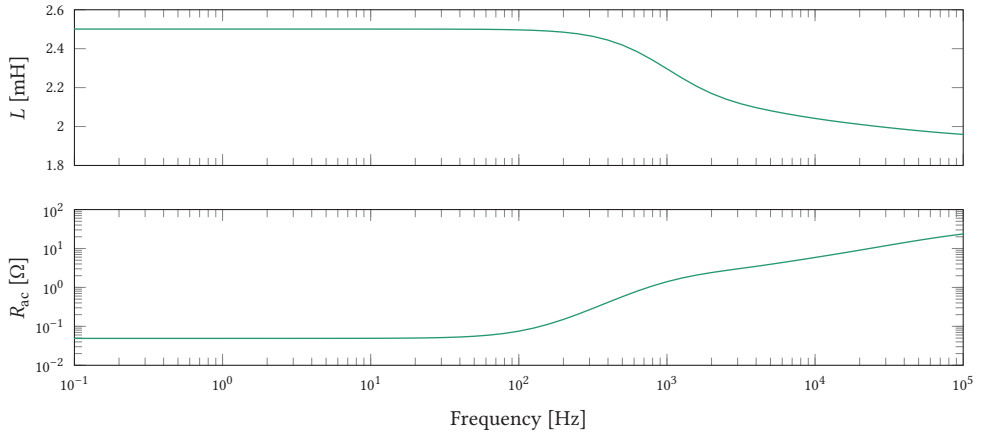


Fig. 7.5 Frequency study result in COMSOL Multiphysics© for the optimal design between 0.1 and 100 kHz. The dc resistance is 49 mΩ.

are defined as:

$$P_{\text{copper}} = \sum_i R_{\text{ac},i} i_{\text{FFT},i}^2 \tag{7.3}$$

The ohmic inductor losses are estimated at 130 W. In total, the ohmic losses in the six air-core branch inductors translate to 0.156 % losses (for a 0.5 MVA converter).

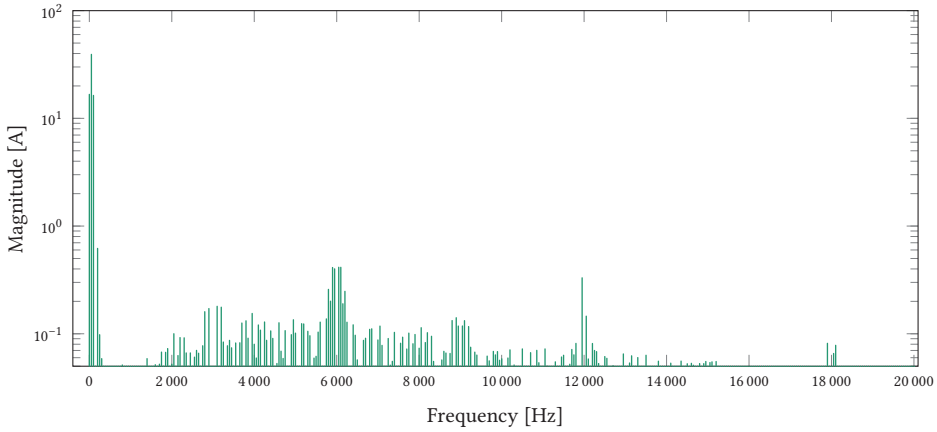


Fig. 7.6 Branch *ap* current FFT at nominal power, eRSA and $f_{\text{sw,app}} = 6$ kHz from **Fig. 5.25(b)**. There is a clear distinction in magnitude between the low order harmonics (that are controlled in closed-loop) and the high order harmonics due to the PWM.

7.2 LFT design

The LFT for the dc/3-ac MMC is designed for the minimum leakage inductance, since the branch current controllability is achieved through the air-core branch inductors. A three-limb dry-type transformer is considered (cf. **Fig. 7.7**). For such a power level, the short-circuit impedance is expected to be in the range of 5 – 6 % and above.

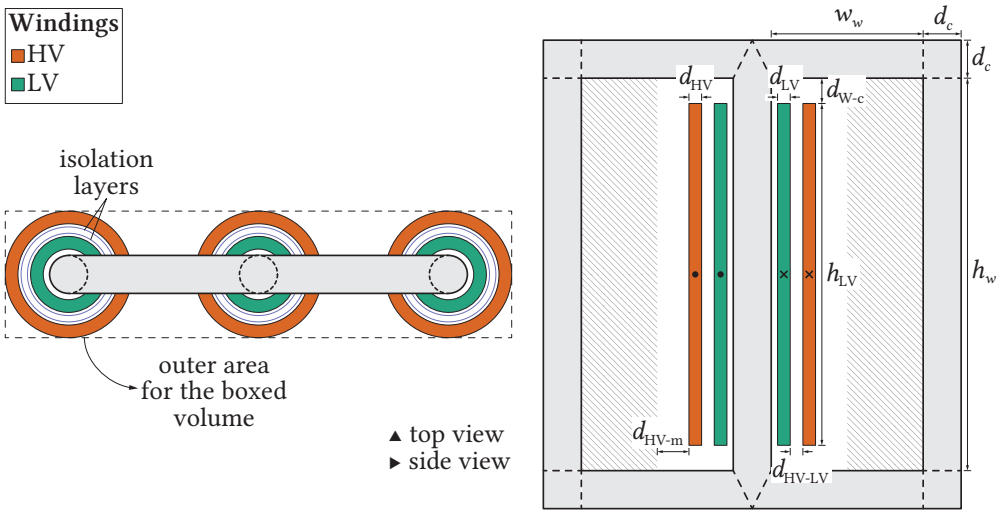


Fig. 7.7 Three-phase three-limb dry-type transformer geometry parametrization. The hatched areas in the right image are the areas reserved for the windings in phase *a* and *c*.

7.2.1 Design algorithm

Silicon steel (M19 from AK Steel) is chosen as core material. The maximum magnetic field density $B_{\max}$ is set to 1.2 T and the turn-to-turn voltage to 10 V, which is reasonable for enamelled or resin cast windings. The magnetizing current (and consequently the magnetizing inductance) are deduced accordingly. It is found that $i_\mu = 1.37\,\%$. The magnetic material properties and chosen operating point are shown in **Fig. 7.8**.

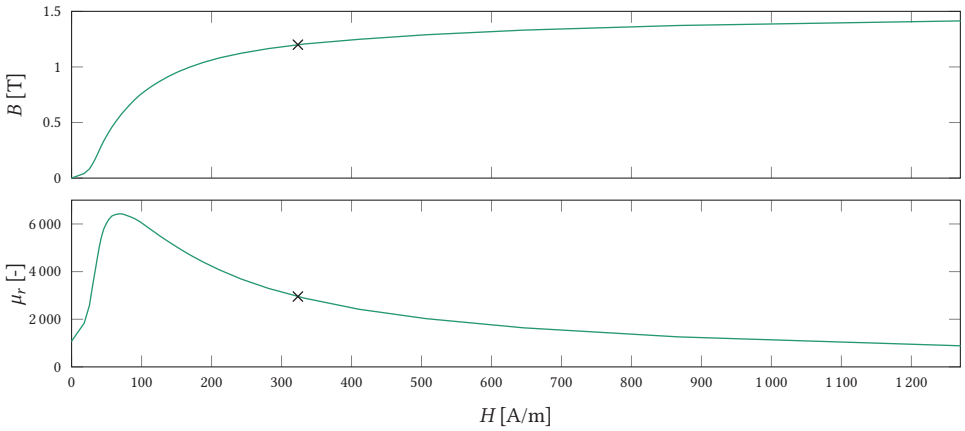


Fig. 7.8 Magnetic properties for the silicon steel M19 from AK Steel (non grain-oriented). For $B_{\max} = 1.2$ T, $\mu_r = 2953$.

The minimum core cross-section is given by (7.4), with 4.44 the factor for sinusoidal operation, with $f = 50$ Hz. The result transfers into a core diameter of $d_c = 218.6$ mm for a circular core cross-section. In practice, the core cross-section would be stepped, as to approximate a circular core cross-section.

$$A_c = \frac{V_{\text{t2t}}}{4.44 f B_{\max}} = 0.0375\,\text{m}^2 \tag{7.4}$$

The different segments of the core can be expressed by the following permeances:

$$\mathcal{P}_{\text{limb}} = \mu_0\mu_r\frac{A_c}{h_w} \quad (7.5a) \qquad \mathcal{P}_{\text{yoke}} = \mu_0\mu_r\frac{A_c}{w_w + d_c/2} \quad (7.5b) \qquad \mathcal{P}_{\text{corner}} = \mu_0\mu_r\frac{A_c}{\pi d_c/4} \quad (7.5c)$$

This allows to express the equivalent permeances for the middle and external paths:

$$\mathcal{P}_{\text{mid}} = \mu_0\mu_r\frac{A_c}{h_w + d_c} \quad (7.6a) \qquad \mathcal{P}_{\text{ext}} = \left(\frac{1}{\mathcal{P}_{\text{limb}}} + \frac{2}{\mathcal{P}_{\text{corner}}} + \frac{2}{\mathcal{P}_{\text{yoke}}}\right)^{-1} \quad (7.6b)$$

The core permeance seen from the middle winding is different from the external ones due to the yokes, hence the magnetizing currents will not have the same peak value in each phase of a three-limb transformer. They're expressed as:

$$\mathcal{P}_{c,\text{mid}} = \left(\frac{1}{\mathcal{P}_{\text{mid}}} + \frac{1}{2\mathcal{P}_{\text{ext}}}\right)^{-1} \quad (7.7a) \qquad \mathcal{P}_{c,\text{ext}} = \left(\frac{1}{\mathcal{P}_{\text{ext}}} + \frac{1}{\mathcal{P}_{\text{mid}} + \mathcal{P}_{\text{ext}}}\right)^{-1} \quad (7.7b)$$

By assuming $h_w = \alpha w_w$, with $\alpha \in \{2,\ 4\}$, the geometry of the transformer core simplifies to a single parameter left to be determined, the window area width w_w. The core permeance is defined as:

$$\mathcal{P}_{c,\text{mid}} = \frac{4\mu_0\mu_r A_c}{(6+\pi)d_c + (4+6\alpha)w_w} \quad (7.8a)$$

$$\mathcal{P}_{c,\text{ext}} = \frac{2\mu_0\mu_r A_c\left[(4+\pi)d_c + 4(1+\alpha)w_w\right]}{\left[(2+\pi)d_c + 2(2+\alpha)w_w\right]\left[(6+\pi)d_c + 2(2+3\alpha)w_w\right]} \quad (7.8b)$$

The ratio between the two permeances is given by:

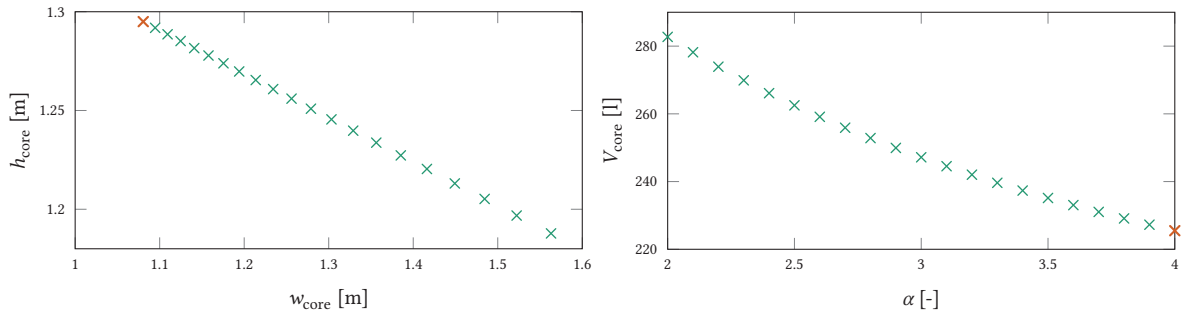
$$\frac{\mathcal{P}_{c,\text{mid}}}{\mathcal{P}_{c,\text{ext}}} = \frac{2\left[(2+\pi)d_c + 2(2+\alpha)w_w\right]}{(4+\pi)d_c + 4(1+\alpha)w_w} \quad (7.9)$$

The magnetizing current of 1.37 % of the nominal current translates into a magnetizing inductance on the primary side of $L_\mu = 12.6\,\text{H}$. This allows to determine the core size. From (7.8a), the window area width is expressed as:

$$w_w = \frac{4\mu_0\mu_r A_c - \mathcal{P}_c^\star(6+\pi)d_c}{(4+6\alpha)\mathcal{P}_c^\star} \quad (7.10)$$

with $\mathcal{P}_c^\star = L_\mu/n_{\text{HV}}^2$ the target core permeance (on the primary side). The current density for the low voltage windings is set to $2\,\text{A/mm}^2$ and $2.5\,\text{A/mm}^2$ for the high voltage one. The results are summarized in **Fig. 7.9**.

For low leakage inductances, the window area should be minimized. As a consequence, designs with a large α are favored. Another advantage is that the magnetizing inductance ratio (cf. (7.9)) remains below 1.3, hence limiting the magnetizing currents imbalance.

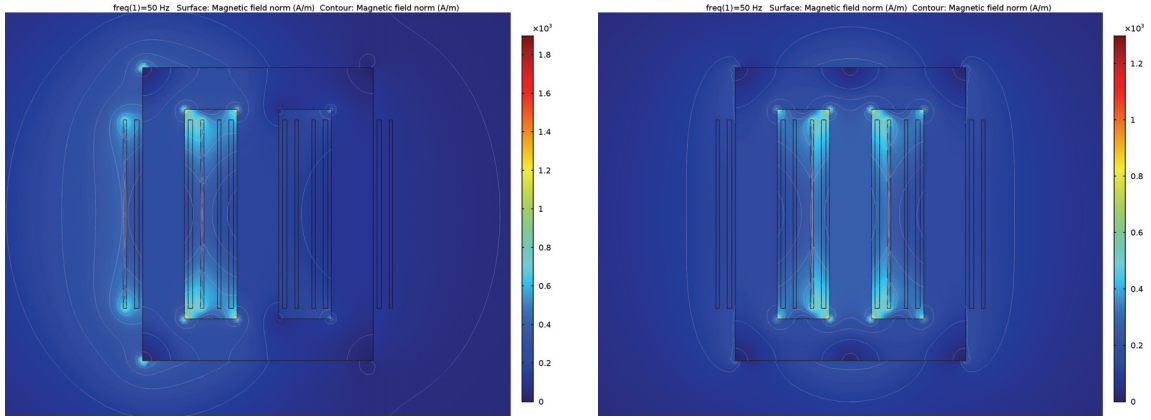


(a) (b)

Fig. 7.9 Three-phase transformer design result: (a) and (b) core volume vs. α. The selected design is indicated in red.

7.2.2 Design verification in FEM

The design with $w_w = 214.4\,\text{mm}$ and $\alpha = 4$ (red crosses in **Fig. 7.9**) is verified with 2D FEM, since it leads to the lowest core volume. The conductor diameters are $\varnothing_{\text{HV}} = 47\,\text{mm}$ ($n_{\text{layers}} = 3$), $\varnothing_{\text{LV}} = 190\,\text{mm}$ ($n_{\text{layers}} = 1$). The winding mean radii are $r_{\text{HV}} = d_c/2 + 75\,\text{mm}$ and $r_{\text{LV}} = d_c/2 + 25\,\text{mm}$. A first set of frequency studies at 50 Hz (with uniform μ_r in the core) is performed. It is found that the self inductances are {9.21, 11.863, 9.21} H for the left, middle and right winding. As expected, the middle and external magnetizing inductances are fairly close ($L_{\mu,\text{mid}} = 1.29 L_{\mu,\text{ext}}$), compared to the expected 1.27 ratio. It is found that the leakage inductances (primary excited and secondary shorted) are {5.42, 5.19, 5.42} mH, respectively. The magnetic fields norm plots for the short-circuit case in phases *a* and *b* (phase *c* is the mirrored version of phase *a*, for symmetry reason) are shown in cf. **Fig. 7.10**.



(a) (b)

Fig. 7.10 Leakage magnetic field norm plots at 50 Hz (in [A/m]) in COMSOL Multiphysics© with one primary winding supplied and corresponding secondary winding shorted: (a) left external winding and (b) middle winding. The same results are mirrored for the right external winding.

Two additional sets of simulations are carried out: (i) no-load test with time domain study with non-linear magnetic material (*BH* curve supplied) and (ii) short-circuit test with frequency domain study and linear magnetic material (constant μ_r). The results are shown in **Fig. 7.11**.

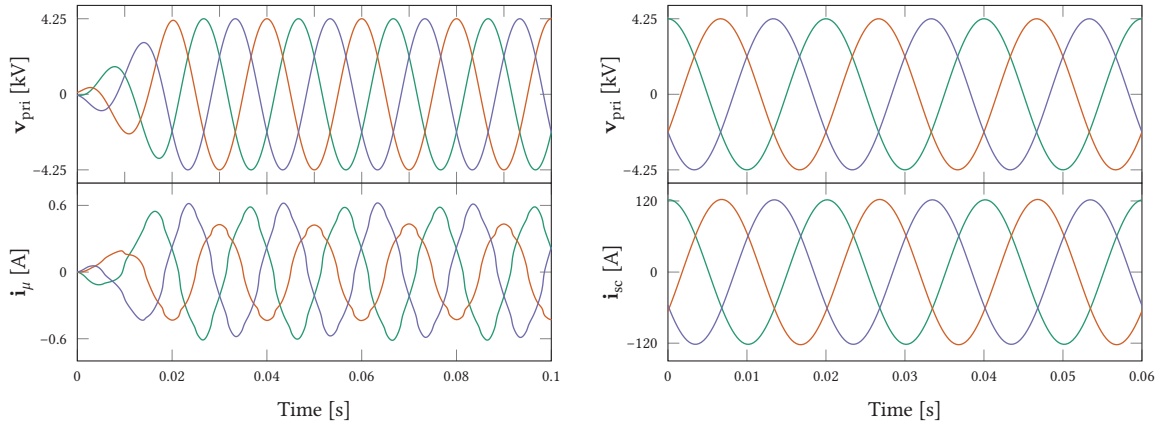


Fig. 7.11 Three-phase transformer additional simulations in COMSOL Multiphysics©: (a) no-load time-domain simulation with non-linear *BH* curve and secondaries open, (b) short-circuit phasor simulation at 50 Hz and secondaries shorted. The imbalance between the middle and external magnetizing inductances is visible through different peak magnetizing currents (with a 90° phase lead).

The total boxed transformer volume (cf. **Fig. 7.7** for the definition of the outer area) is 481.7 l. The primary dc resistance is 25.71 mΩ with $r_{\text{mean,HV}} = 16.34$ mm. The secondary dc resistance is 58.9 µΩ with $r_{\text{mean,LV}} = 113.4$ mm. The mean radii are defined to the center of the equivalent rectangular windings. The winding losses, in case only the component at 50 Hz is accounted for, are 79.08 W for the primary winding and 30.93 W for the secondary winding. In total, the winding losses contribute to 0.066 % losses (330 W for a 0.5 MVA converter). The core losses are estimated to be on par with the winding losses.

7.3 GIMC transformer design

The feasibility of high primary leakage transformer required for the GIMC is evaluated in this section. The magnetizing inductance target value is identical to the three-phase transformer previously designed. The only difference is that the leakage inductance must be large enough to maintain the branch current controllability. In order to achieve higher leakage, the primary windings are placed one on top of the other. Depending on their interleaving, the leakage inductance can be lowered to the design objective value (cf. **Fig. 7.12**).

The design with $w_w = 259.8$ mm and $\alpha = 4$ is verified with 2D FEM. Again, a high α parameter is favored, since it results in lower discrepancies between the magnetizing inductances ($L_{\mu,\text{mid}} \sim 1.28 L_{\mu,\text{ext}}$). Both non interleaved and interleaved primary windings are compared hereafter with the same core size.

7.3.1 Without interleaving

A GIMC transformer without interleaving of the primary windings (cf. **Fig. 7.12(a)**) is studied. A first set of frequency studies at 50 Hz (with uniform μ_r in the core) provide the self and leakage inductances

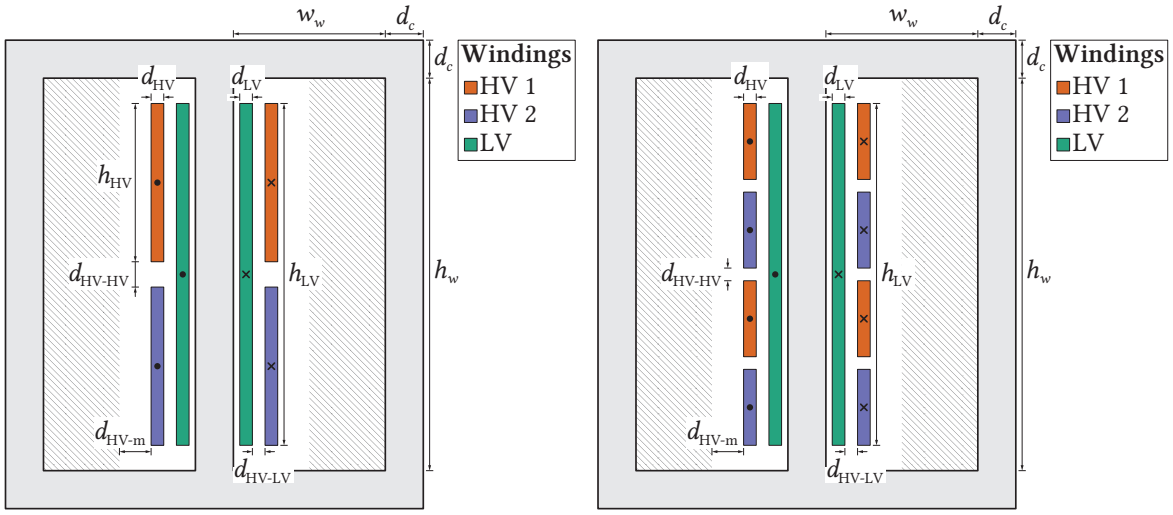


Fig. 7.12 GIMC transformer geometry: (a) without interleaving of the primary windings and (b) with interleaving of the primary windings. The hatched regions in the window areas correspond to the space reserved to the other phases windings.

with one winding shorted at a time. The inductances obtained with the FEM simulations are:

- The self inductances are {8.11, 10.35, 8.11} H for the left, middle and right winding.
- The leakage inductances with one primary winding supplied and the secondary shorted are {29.02, 36.96, 29.02} mH.
- The leakage inductances with one primary supplied and the other one shorted are {94.26, 126.92, 94.26} mH.
- The leakage inductances with one primary winding supplied and the other windings shorted are {83.33, 108.21, 83.33} mH.

The obtained values are much higher than the leakage inductances for the regular three-phase transformer with concentrated windings, since the contribution of the radial flux plays also a role (high for primary to primary inductance, medium for primary to secondary), instead of solely the axial flux. The magnetic field norm plots for each case in phases a and b (phase c is the mirrored version of phase a, for symmetry reason) are shown in **Fig. 7.13**.

7.3.2 With interleaving

A different realization of the GIMC transformer with interleaving of the primary windings (cf. **Fig. 7.12(b)**) is evaluated as well for comparison. A first set of frequency studies at 50 Hz (with uniform μ_r in the core) provide the self and leakage inductances with one winding shorted at a time. The inductances obtained with the FEM simulations are:

- The self inductances are {8.09, 10.33, 8.09} H for the left, middle and right winding.

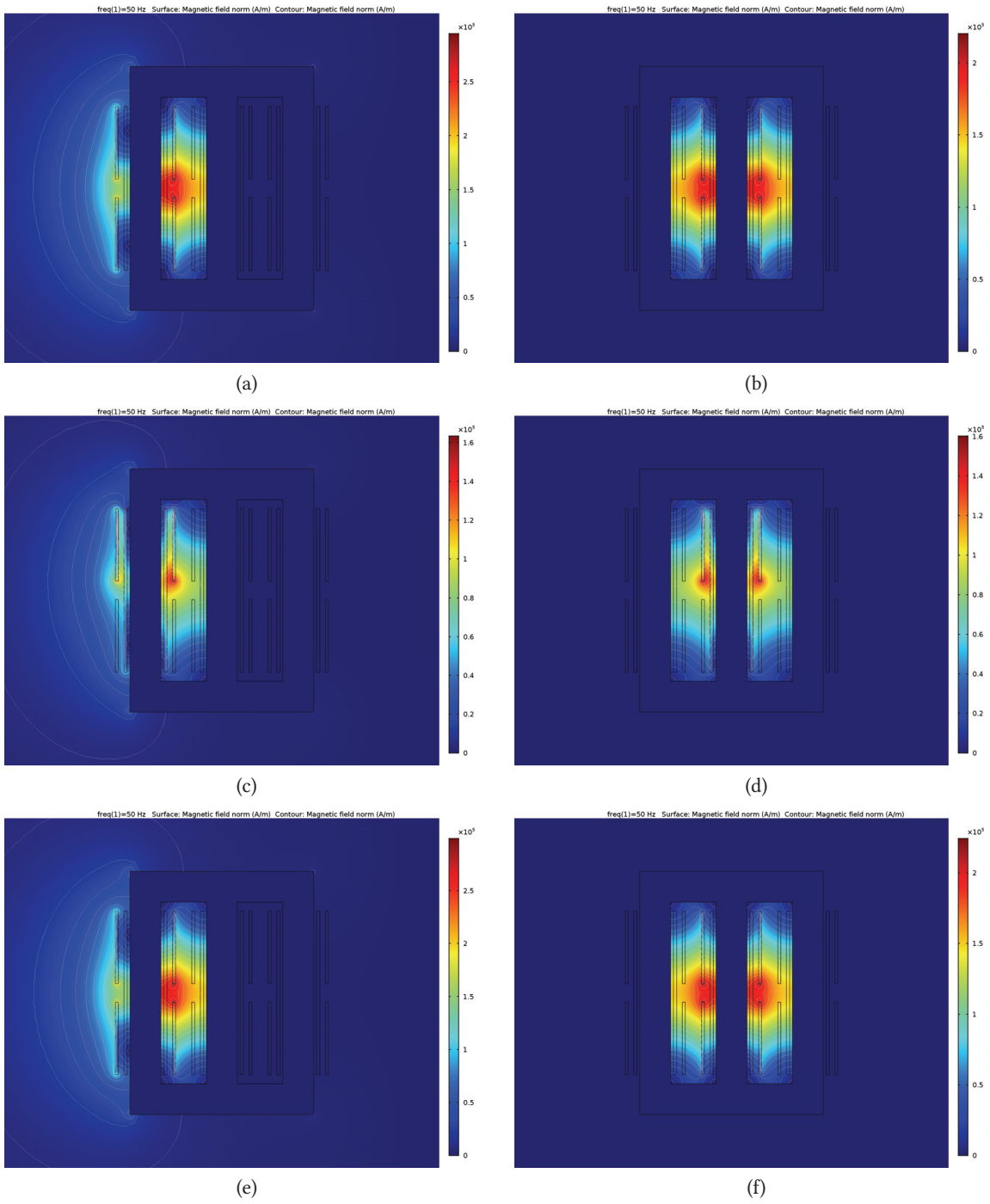


Fig. 7.13 Magnetic field norm plots at 50 Hz for the GIMC transformer without interleaving of the primary windings: (a) one primary winding supplied and the other shorted in phase *a*, (b) one primary supplied and the other shorted in phase *b*, (c) one primary winding supplied and the secondary shorted in phase *a*, (d) one primary supplied and the secondary shorted in phase *b*, (e) one primary and the two other windings shorted in phase *a* and (f) one primary and the two other windings shorted in phase *b*.

- The leakage inductances with one primary supplied and the secondary shorted are {12.05, 13.3, 12.05} mH.
- The leakage inductance with one primary supplied and the second primary shorted are {27.65, 33.73, 27.65} mH.
- The leakage inductances with one primary supplied and the other windings shorted are {25.57, 31.17, 25.57} mH.

The magnetic field norm plots for each case in phases *a* and *b* (phase *c* is the mirrored version of phase *a*, for symmetry reason) are shown in **Fig. 7.14**.

Two additional sets of simulations are carried: (i) no-load test with time domain study with non-linear magnetic material (*BH* curve supplied) and (ii) short-circuit test with frequency domain study and linear magnetic material (constant μ_r). The results are shown in **Fig. 7.15**.

The total boxed transformer volume (cf. **Fig. 7.7** for the definition of the outer area) is 573.1 l. The primary dc resistance is 32.11 mΩ with $r_{\text{mean,HV}} = 16.34$ mm. The secondary dc resistance is 58.9 μΩ with $r_{\text{mean,LV}} = 113.4$ mm. The winding losses, in case only the component at 0 and 50 Hz are accounted for, are 63.29 W for each primary winding and 30.93 W for the secondary winding. In total, the winding losses contribute to 0.095 % losses (472.53 W for a 0.5 MVA converter). The core losses are estimated to be on par with the winding losses.

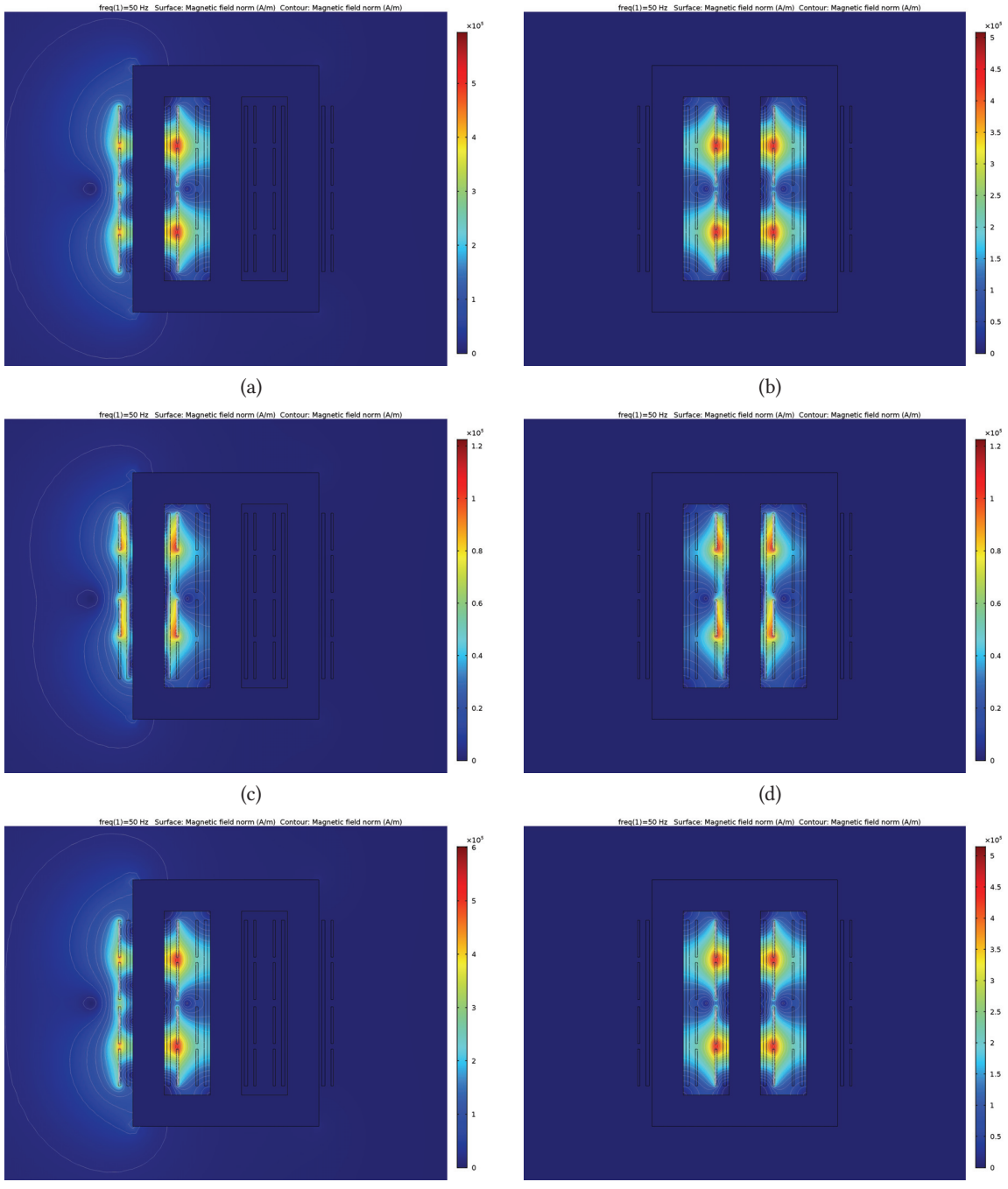


Fig. 7.14 Magnetic field norm plots at 50 Hz for the GIMC transformer with split windings and interleaving: (a) one primary winding supplied and the other shorted in phase *a*, (b) one primary supplied and the other shorted in phase *b*, (c) one primary winding supplied and the secondary shorted in phase *a*, (d) one primary supplied and the secondary shorted in phase *b*, (e) one primary and the two other windings shorted in phase *a* and (f) one primary and the two other windings shorted in phase *b*.

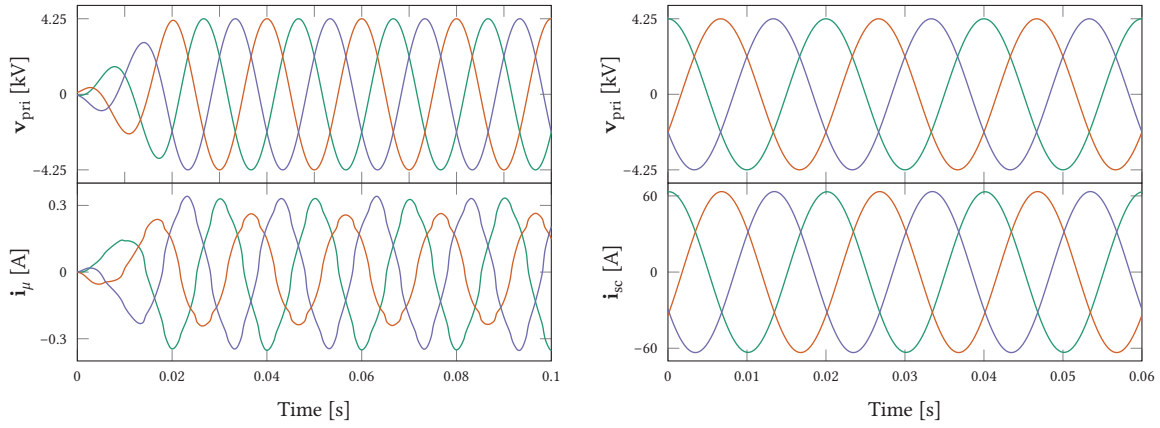


Fig. 7.15 GIMC transformer with interleaving additional simulations in COMSOL Multiphysics©: (a) no-load time-domain simulation with non-linear *BH* curve and secondaries open, (b) short-circuit phasor simulation at 50 Hz and secondaries shorted. The imbalance between the middle and external magnetizing inductances is visible through different peak magnetizing currents (with a 90° phase lead).

7.4 Discussion

In this chapter, the comparison between a dc/3-ac MMC with air-core branch inductors plus three-phase transformer and the GIMC with multi-winding transformer, where the branch inductors are realized through the leakage inductances of the primary windings, was performed. It was shown that the GIMC transformer with higher leakage is easily feasible by stacking the primary windings, without increasing the core size. The tuning of the leakage inductance is achieved by interleaving the primary windings, with more or less spacing between them, i.e. by varying the number of layers for the primary windings.

The comparison is summarized in **Tab. 7.1** in terms of numbers. While the transformer boxed volume is increased by a factor 1.2 for the GIMC transformer compared to the conventional three-phase transformer, the complete magnetic component volume is estimated to be lower for the GIMC than the dc/3-ac MMC, since no additional space has to be allocated for the six branch inductors[1]. In addition, the total losses for the GIMC are lower than for the three-phase transformer with air-core inductors, since the branch inductors were found way less efficient than the primary windings of the multi-winding transformer (factor 2.7 between the primary winding losses of the GIMC transformer, i.e. 63.3 W per branch, compared to the three-phase transformer and air-core branch inductor, i.e. 170 W per branch).

It is concluded that the integration of the branch inductor function inside the transformer with the GIMC provides a marginal volume reduction and large efficiency increase of the magnetic components. In total, the GIMC transformer contributes to 0.19 % losses, compared to 0.29 % for the dc/3-ac MMC. However, a refined study of the transformer design is required to obtain a more accurate comparison. Practically speaking, in case a drive line-up is considered, the branch inductors would occupy a separate cabinet, which could be omitted with the GIMC.

[1]The mechanical layout for respecting the electrical clearances and providing cooling would increase significantly the volume occupied by the branch inductors.

Tab. 7.1 Magnetic components comparison between the conventional dc/3-ac MMC with branch inductors and the GIMC with integrated branch inductors.

	Branch inductors		**Transformer**	
	volume	losses	volume	losses
dc/3-ac plus LFT MMC	6× 6 l	780 W (0.156 %)	481.7 l	660 W (0.132 %)
GIMC	-	-	573.1 l	945 W (0.19 %)

8

Virtual Submodule loss estimation method

The VSM is a generic loss estimation method that can be applied to other multilevel converter topologies besides the dc/3-ac MMC. Starting from the analytical expressions of the branch voltages and currents, which accurately describe their closed-loop steady-state waveforms, the other MMC key waveforms, such as the branch capacitor voltages and modulation indices, are derived in a similar manner as for the power equations in ***Sec. 3.3****. Combined with a modulation block that captures the switching pattern, each semiconductor current and voltage waveform is reconstructed with a model of the cell, which has to be adapted depending on its type. From there, the cell losses are calculated in a conventional way. An accurate estimation of the actual losses is obtained, with a two orders of magnitude improvement of the calculation time compared to a detailed switched model, which makes the VSM method particularly suitable for establishing a converter loss map over the whole SOA.*

8.1 Introduction

During the design phase of an MMC, an accurate loss evaluation of the cell plays an important role and supports the semiconductor device selection. Unlike classical topologies, the MMC features an additional degree of freedom, the circulating current, an internal quantity used to control the converter's internal energy balance. The circulating current can be shaped according to some control objective and its harmonic content is subject to variation, involving both dc and ac components of certain frequencies (cf. **Sec. 3.3.2**). Consequently, the harmonic content of the MMC key waveforms and the cell losses are also affected. In contrast to conventional converter topologies, it makes sense to calculate the losses in closed-loop operation, where the shape of the circulating current can be accurately determined. This is further motivated by the fact that the required branch inductance values for direct modulation operation, where the circulating current is not actively controlled, are much larger compared to the case with active circulating current control, as attested by the impedance comparison in [134], which revisited the findings from [136]. Hence, if the circulating current is actively controlled, the sensitivity to the choice of the branch inductance is significantly reduced, as it is almost fully decoupled from the shape of the circulating current, as long as the provided inductance allows to get control over the circulating current.

Regarding the modulation, two concurrent PWM methods are found in the literature: (i) based on LS-PWM combined with a sorting algorithm and (ii) based on PS-PWM with an inherent branch balancing capability if the switching frequency is not an integer multiple of the fundamental ac grid frequency [120]. With the latter method, some uncertainty stemming from the sorting algorithm has to be managed or circumvented, as the link between the apparent switching frequency (branch voltage waveform) and the cell switching frequency is not obvious. So far, the influence of the modulation

scheme and branch balancing method on the cell losses has not been evaluated in the literature. While the conduction losses depend on the operating point of the converter and thus cannot be reduced through control means once the circulating current harmonic content is set, the switching losses directly depend on the switching frequency experienced by each cell, its position inside the switching sequence and associated voltages and currents.

In the literature, the MMC semiconductor losses were obtained by simulation [137], [138] or numerically considering direct modulation for HVdc application in mind, with a dc circulating current and without considering the capacitor losses [139]. These works suffer either from a high computation burden, in case the losses are obtained from extensive switched model simulations, or from strong limitations concerning the modulation method, in case the computation is tailored to one particular modulation method.

In contrast, the proposed VSM loss estimation method allows for a fast estimation of the cell losses under different operating conditions, control schemes (e.g., effects of the circulating current injection strategy) and modulation methods, under the assumption of a stable operation of these schemes in steady-state. In addition, the principle can be applied to other cell types, by a adapting the VSM model, or multilevel converter topologies, as long as the two main assumptions introduced in the following section hold. The validity of this method is assessed with a thorough comparison of the results obtained from a fully switched converter model.

8.2 Idea and main assumptions

Switched model simulations, especially for an MMC with a large number of cells, are known to be time consuming. Two assumptions enable a significant complexity reduction:

1. The branch current ripple is small enough to be ignored (cf. **Fig. 8.1(a)**). It is not simple to model (or capture) in an efficient and accurate manner the branch current ripple, as discussed in [140] for conventional multi-level and -phase converters.
2. The branch capacitor voltage spread is ignored (**Fig. 8.1(b)**). As a good estimate, the voltage error is inferior to the peak-to-peak capacitor voltage ripple, which is $20\,\%V_{\mathrm{dc}}$ at max.

Otherwise, there will be an error coming from the non linearity of the switching losses. These two assumptions allow the substitution of the branch currents and voltages with their average. It implies that the branch inductance value and/or the apparent branch switching frequency are high enough. Both these conditions are generally valid in the case of MMC.

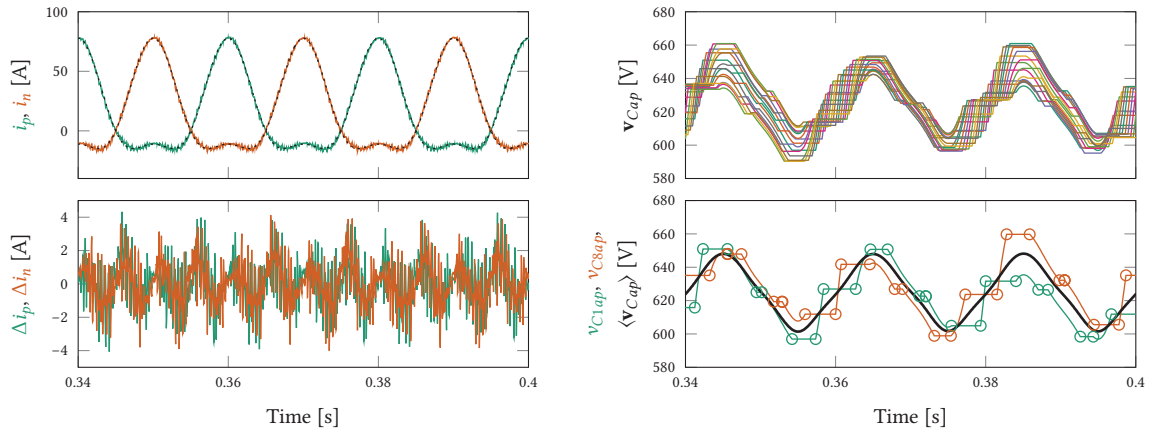


Fig. 8.1 Branch *ap* evaluation of the VSM assumptions over three fundamental grid periods obtained from a switched model with PS-PWM and $\phi = 0$: (a) branch current ($\Delta i_{p/n} = i_{p/n,\mathrm{sw}} - i_{p/n,\mathrm{VSM}}$) and (b) branch capacitor voltages. The switching events are marked with circles. Note that as the cell switching frequency (187.375 Hz) is not an integer multiple of the grid frequency, each cell capacitor voltage does not have the same periodicity as the grid frequency.

8.3 Analytical description of the MMC key waveforms

The analytical average model is based on the set of equations that has already been presented in **Sec. 3.3**. The model accounts for all parasitic elements in the circuit, especially the branch inductance L_{br}, which was the main motivation of [74] compared to the simplified models of [72], [73], as well as the circulating current in steady-state, where no large branch energy imbalances occur. Equations (8.1) are the starting point with the expressions for the branch voltage and current. Two scenarios for the branch voltage have to be accounted for in (8.1a), whether a CM voltage term made from a combination of one or more triplen harmonics is present or not. If yes, the linear modulation range is extended up to $k_{\mathrm{ac}} \approx 1.03$ due to the $2/\sqrt{3}$ over-modulation factor. In addition, two scenarios can be analyzed regarding the shaping of the circulating current in (8.1b): (i) no 2^{nd} harmonic circulating current, which corresponds to a circulating current suppression controller alike behavior and (ii) 2^{nd} harmonic circulating current injection, which was initially proposed in [72] to reduce the capacitor voltage ripple. Consequently, the branch current contains three terms: (i) a dc term, which corresponds to the active power exchange between the dc and ac grids, (ii) a fundamental frequency ac term, which corresponds to half the ac grid current i_g and (iii) an optional 2^{nd} harmonic circulating current term, with amplitude $\hat{i}_{\mathrm{circ},2}$ and phase $\theta_2 = \phi$.

$$e_{p/n} = \frac{V_{\mathrm{dc}}}{2}\left(1 \mp k_{\mathrm{ac}} \cos\left(\omega t - \frac{2\pi(k-1)}{3}\right) \mp v_{\mathrm{CM}}\right) - \left(R_{\mathrm{br}} i_{p/n} + L_{\mathrm{br}} \frac{\mathrm{d}}{\mathrm{d}t} i_{p/n}\right) \tag{8.1a}$$

$$i_{p/n} = \underbrace{\frac{I_{\mathrm{dc}}}{3}}_{\text{dc term}} \underbrace{\pm \frac{1}{2}\hat{i}_g \cos\left(\omega t + \phi - \frac{2\pi(k-1)}{3}\right)}_{\text{fundamental ac term}} \underbrace{+ \hat{i}_{\mathrm{circ},2} \cos\left(2\omega t + \theta_2 - \frac{2\pi(k-1)}{3}\right)}_{\text{optional } 2^{\mathrm{nd}} \text{ harmonic term}} \tag{8.1b}$$

where V_{dc} is the dc link voltage, $k_{\mathrm{ac}} = 2\hat{v}_g/V_{\mathrm{dc}}$ the voltage ratio between the three-phase and dc grids, ω the grid frequency, $k \in \{1, 2, 3\}$ the phase number, S the apparent power of the converter and ϕ the

load angle. The expressions for $\hat{i}_g$ and $\hat{i}_{\text{circ},2}$ are given in (8.2a) and (8.2b).

$$\hat{i}_g = \frac{2S}{3\hat{v}_g} = \frac{2S}{3k_{\text{ac}}V_{\text{dc}}/2} \tag{8.2a}$$

$$\hat{i}_{\text{circ},2} = \frac{\hat{v}_g\hat{i}_g}{2V_{\text{dc}}} = \frac{S}{3V_{\text{dc}}} \tag{8.2b}$$

The expression for the dc current is subject to a quadratic equation, whose negative root is generally selected [75].

$$I_{\text{dc}} = \frac{V_{\text{dc}} - \sqrt{V_{\text{dc}}^2 - 8R_{\text{br}}\left(\frac{\hat{v}_g\hat{i}_g}{2}\cos(\phi) + 2R_{\text{br}}\left(\frac{\hat{i}_g^2}{8} + \frac{\hat{i}_{\text{circ},2}^2}{2}\right)\right)}}{4R_{\text{br}}} \tag{8.3}$$

From there, subsequent derivations finally lead to the branch modulation index expressions $m_{p/n} = e_{p/n}/\langle v_{C\Sigma p/n}\rangle$. The relevant waveforms with a sweep of the branch inductance value are illustrated in **Fig. 8.2** for the parameters of **Tab. 8.1**.

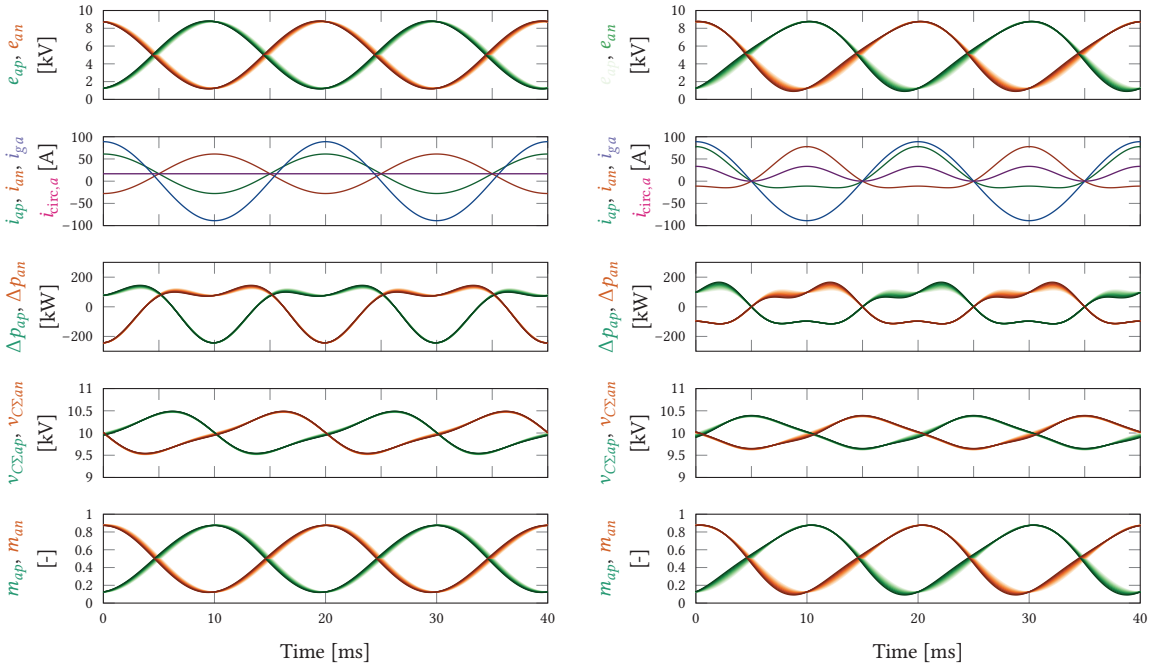


Fig. 8.2 Branch representative waveforms with: (a) dc circulating current and (b) dc plus 2$^{\text{nd}}$ harmonic circulating current injection. The branch inductance value is swept from 0 H (light shade) to 50 mH (dark shade) to highlight the impact of the branch inductance voltage drop. The currents are not impacted by L_{br}, as they are set for a given power transfer and no ripple is considered.

Tab. 8.1 System parameters for the VSM method based on the MMC prototype.

V_{dc}	10 kV	S	0.5 MVA	f_g	50 Hz	N_{cells}	16	R_{br}	0.1 Ω
k_{ac}	0.75	C_{cell}	1.9 mF	k_{dc}	1	L_{br}	10 mH	R_{esr} [a]	110 mΩ

[a]Per individual capacitor

8.4 Virtual submodule concept

Considering the operating principle of an MMC and the previously introduced assumptions, all the relevant waveforms are identical for each cell of the same branch. The modulation can be modified in order to capture and direct all the switching events to a single cell, as shown in **Fig. 8.3**. The VSM concept allows for significant simplifications, and its validity is restricted under the conditions already discussed. Thus, a slight deviation from a purely analytical method is required in order to compress multiple PWM signals into a representative train of pulses.

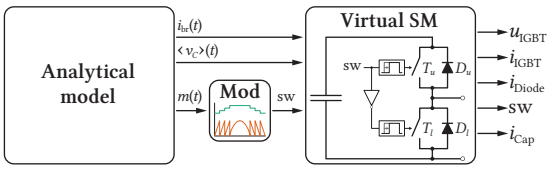


Fig. 8.3 Functional VSM concept, where the MOD block is implemented with a single carrier and a quantizer. It produces an output identical to a collection of all switching events from any modulation scheme.

Analytical model block The MMC key waveforms, i.e. the branch current, branch capacitor voltage and modulation index, are calculated with the converter analytical model. There, the harmonic content of these quantities can be adjusted to match the closed-loop steady-state obtained with the selected control method. The analytical expressions are evaluated over the simulation horizon and then loaded into 1D look-up tables (LUTs).

Mod block The modulation block is implemented with the single-carrier and quantizer, as illustrated in **Fig. 5.8**. This is an effective way to perform a multi-level modulation with a low computation burden. All switching events are compressed in a train of pulses.

VSM block The VSM constructs the signals that are routed to the loss tool according to the cell type. As the branch current, capacitor voltage, modulation index and switching sequence are used as inputs, the VSM implementation doesn't require modifications in order to account for changes in them. The switching instants are collected with the edge detection block (turn-ON and turn-OFF) and stored for further post-processing and loss calculations.

A detailed view of the complete VSM method is shown in **Fig. 8.4**. To verify the validity of this concept, a fully switched model of the MMC has been developed in PLECS, as presented next.

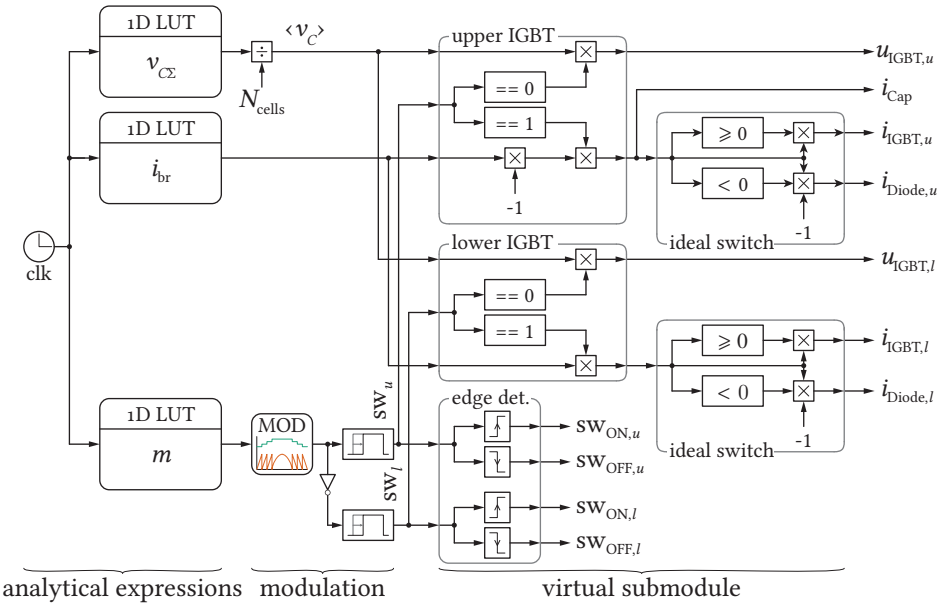


Fig. 8.4 Detailed VSM concept implementation for a unipolar cell. $v_{C\Sigma p/n}$, i_{br} and m are obtained from the analytical model.

8.5 MMC switched model

To compare the analytical method based on the VSM concept with realistic waveforms from a fully switched MMC model, circuit simulations are performed with PLECS / Simulink. The comparison is carried out with two modulation methods: (i) PD-PWM with the eRSA (cf. **Sec. 5.2.5**) and (ii) PS-PWM without branch balancing control (cf. **Sec. 5.2.3**), since the power set point is slowly ramped up. The considered apparent branch switching frequencies are 3 kHz for PD-PWM and 2.95 kHz for PS-PWM. This corresponds to a cell switching frequency of 187.5 Hz and 184.375 Hz, respectively. The closed-loop control as detailed in **Sec. 4.2.4** is applied.

The relevant waveforms from the analytical model and from the closed-loop switched model are compared for various load angles and the two considered circulating current injection strategies in **Fig. 8.5**. Aside from the branch current ripple and the capacitor voltage spread that cannot be captured in the analytical model, they are in very good agreement. This also demonstrates the performance of the control algorithm: a perfectly dc circulating current (**Figs. 8.5(a)** and **8.5(c)**) or a dc with superimposed 2$^{\text{nd}}$ harmonic circulating current (**Figs. 8.5(b)** and **8.5(d)**) are obtained in steady-state.

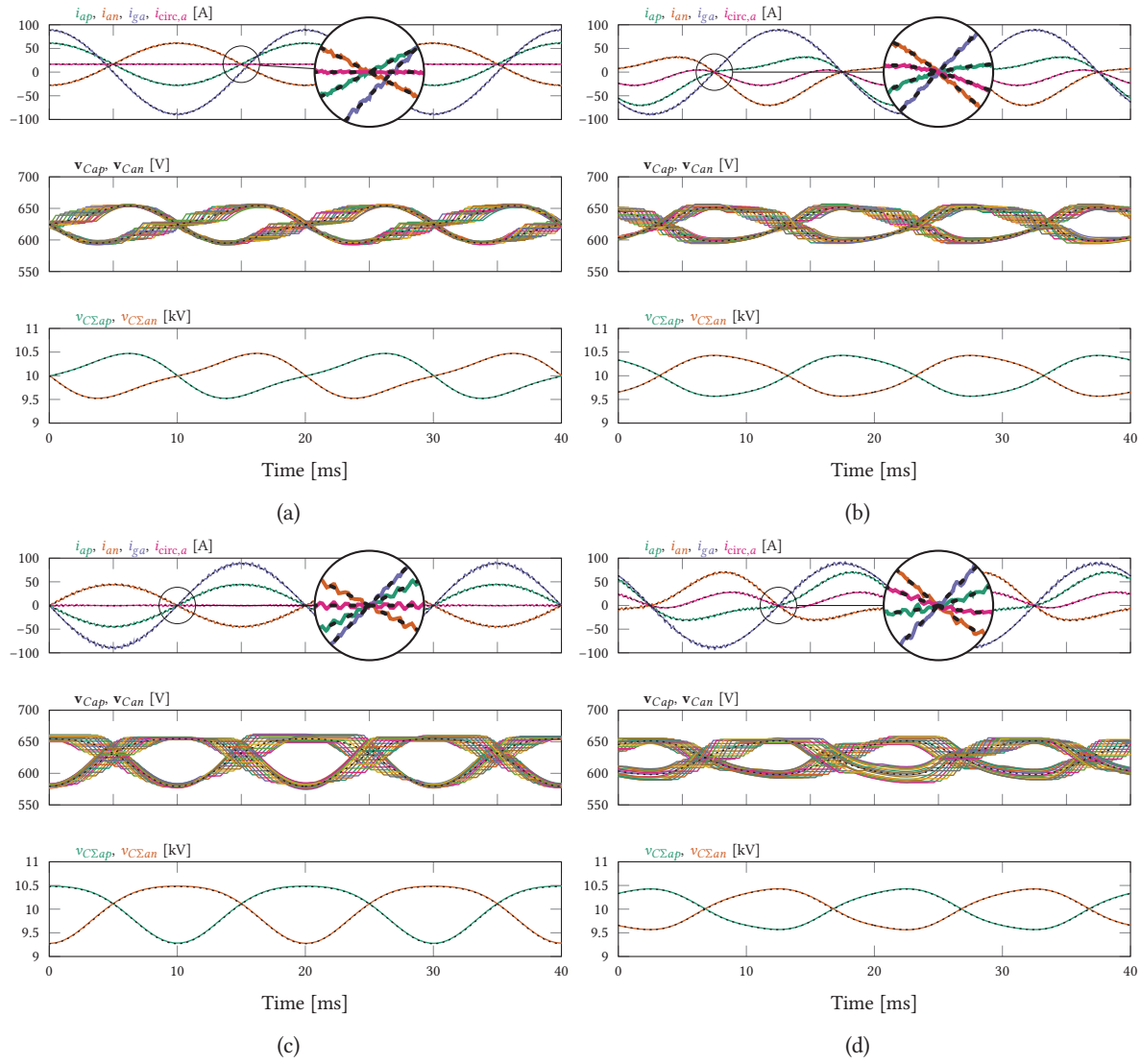


Fig. 8.5 Closed-loop responses (colored lines) versus analytical waveforms (dashed lines) in phase-leg a: (a) PD-PWM with dc circulating current for $\phi = 0$, (b) PD-PWM with dc plus 2$^{\text{nd}}$ harmonic circulation current for $\phi = 3\pi/4$, (c) PS-PWM with dc circulating current for $\phi = \pi/2$ and (d) PS-PWM with dc plus 2$^{\text{nd}}$ harmonic circulating current for $\phi = \pi/4$. The circles located at $t = 25$ ms are magnifications of the current crossings indicated by thin circles.

8.6 Loss tool

To compare the results, a common loss tool collects the waveforms of interest either from the VSM or the fully switched model. The input waveforms are sampled at 200 kHz. The waveforms of interest are: (i) the voltage across both upper and lower IGBTs, (ii) the current through the IGBTs and the diodes as well as the capacitor current and (iii) the switching instants, which are mandatory in order to determine the switching losses (functional description presented in **Fig. 8.6**). To evaluate the losses, either from the PLECS switched model, or the VSM concept, the relevant information is captured (e.g., turn-ON event, turn-OFF event, device voltage and current). The losses are split between conduction

and switching losses (turn-ON, turn-OFF and diode reverse recovery losses) and calculated using (8.4). As datasheet curves for the switching energies are used, the data points are interpolated for calculation - p^3 stands for piecewise cubic interpolation.

$$P_{\text{IGBT,cond.}} = i_{\text{IGBT,avg}} V_{\text{CE}} + i^2_{\text{IGBT,RMS}} R_{\text{IGBT,ON}} \tag{8.4a}$$

$$P_{\text{Diode,cond.}} = i_{\text{Diode,avg}} V_{\text{F}} + i^2_{\text{Diode,RMS}} R_{\text{Diode,ON}} \tag{8.4b}$$

$$P_{\text{IGBT,ON}} = \sum \frac{\text{p}^3(i_{\text{IGBT}}, E_{\text{IGBT,ON}}, i_{\text{IGBT,ON}}) u_{\text{IGBT,ON}}}{V_{\text{CS}} T_{\text{window}}} \tag{8.4c}$$

$$P_{\text{IGBT,OFF}} = \sum \frac{\text{p}^3(i_{\text{IGBT}}, E_{\text{IGBT,OFF}}, i_{\text{IGBT,OFF}}) u_{\text{IGBT,OFF}}}{V_{\text{CS}} T_{\text{window}}} \tag{8.4d}$$

$$P_{\text{Diode,rr}} = \sum \frac{\text{p}^3(i_{\text{IGBT}}, E_{\text{IGBT,rr}}, i_{\text{IGBT,ON}}) u_{\text{IGBT,ON}}}{V_{\text{CS}} T_{\text{window}}} \tag{8.4e}$$

where T_{window} is the window of time over which the losses are computed.

As a reminder, the 1.9 mF capacitor bank is realized with six 400 V electrolytic capacitors. Only ohmic losses from equivalent series resistance (ESR) are considered and used for the capacitor loss calculation in the loss tool.

$$P_{\text{cap}} = R_{\text{esr},eq} i^2_{\text{Cap}} \tag{8.5}$$

Different semiconductor devices can be easily compared, as they are loaded from a database - though based on data sheet parameters. Multiple simulation sweeps for each device are not required, as device specific parameters are not required for the simulation. Proper scalings and interpolations of the datasheet curves are built into the loss tool, aiming to minimize the errors due to the limited number of sampled points provided for the switching loss energies. Additional calculated data provided as outputs are also indicated at the bottom of the loss tool.

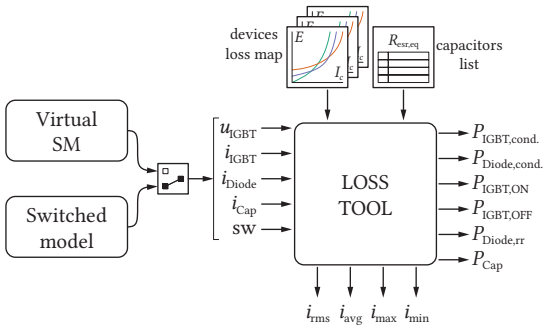


Fig. 8.6 Loss calculation tool diagram. The switch between the VSM and switched model symbolizes that the inputs of the loss tool (u_{IGBT}, i_{IGBT}, ...) are gathered from either model for the comparion. The outputs of the loss tool are the power losses of each component ($P_{\text{IGBT,cond.}}$, $P_{\text{Diode,cond.}}$, ...).

8.7 Verification and comparison

To provide a complete analysis of the error between the VSM method and the loss values obtained from the detailed switched model, extensive simulations for different operating points are carried

out. The semiconductor device is the Semikron SK 50 GH 12T4 T module [141], i.e. the same as in the MMC cell of the prototype (cf. **Sec. 9.3**). The losses are computed in the positive branch of phase-leg *a*, but any other branch could have been selected instead. The waveforms are recorded over ten fundamental ac grid periods before the loss tool is invoked, in order to mitigate the *instantaneous* loss difference between the cells. The average losses per cell are obtained from the VSM (representing a complete branch) by simple division by the number of cells in a branch.

As it can be seen in **Fig. 8.7**, the semiconductor losses (the same stands for capacitor losses) are well balanced across all the cells within a branch. Consequently, from this point on only the mean value is considered. A subset of results, with one load angle per modulation method and circulating current harmonic content, is presented in **Tab. 8.2**. As it can be seen, the semiconductor losses obtained using the VSM are in good agreement with each cell from the detailed switched model. The conduction losses are very accurately estimated by the VSM method, as based on the branch current RMS value, which is unaffected by the branch current ripple. The switching losses are less accurately estimated by the proposed method. The reason behind is that they depend on the instantaneous switched branch current and cell capacitor voltage. The accuracy dependency is inversely proportional to the apparent branch switching frequency. However, as the switching losses are few orders of magnitude smaller than the conduction losses, the overall semiconductor losses are in good agreement. The complete results, for each modulation method and circulating current injection strategy, are presented in **Fig. 8.8**. The left-hand side stacked bars correspond to the VSM method and the right-hand side stacked bars to the averaged semiconductor losses of the switched model. The split of different loss contributions in function of the load angle ϕ can be easily identified. At the same time, the loss split and the overall losses are almost identical to the results obtained from the VSM concept, demonstrating that the MOD block is able to correctly capture and compress the original switching patterns. Similarly, the averaged capacitor losses are presented in **Fig. 8.9**.

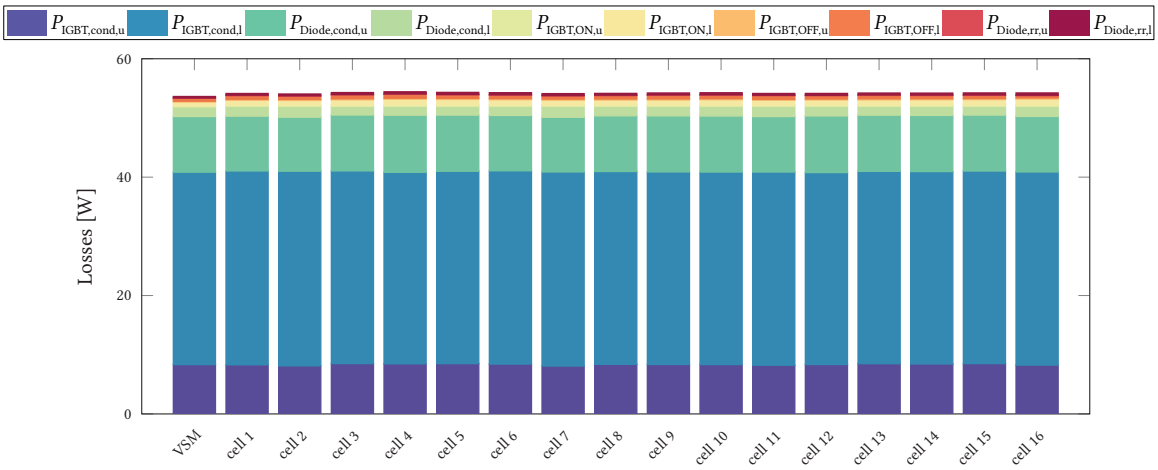


Fig. 8.7 Detailed semiconductor losses comparison for PS-PWM with DC circulating current and $\phi = 0$. Cell 1 to 16 are the individual semiconductor losses from the switched model.

The relative errors plots on the total averaged semiconductor and capacitor losses are presented in **Fig. 8.10** and are computed as:

$$\varepsilon = \frac{x_{\text{switched}} - x_{\text{VSM}}}{x_{\text{VSM}}} \cdot 100 \tag{8.6}$$

Tab. 8.2 Detailed loss numbers comparison between the VSM concept and the switched model for one operating point per modulation method and circulating current harmonic content: (a) PD-PWM and (b) PS-PWM. All the entries are in [W].

(a)

i_{circ}	dc		dc plus 2$^{\text{nd}}$	
Model	VSM	SW	VSM	SW
ϕ [rad]	0		$3\pi/4$	
$P_{\text{IGBT,cond,u}}$	8.34	8.36	9.21	9.19
$P_{\text{IGBT,cond,l}}$	32.50	32.58	4.73	4.77
$P_{\text{Diode,cond,u}}$	9.41	9.42	7.18	7.20
$P_{\text{Diode,cond,l}}$	1.64	1.64	28.06	27.89
$P_{\text{IGBT,ON,u}}$	0.16	0.20	0.69	0.71
$P_{\text{IGBT,ON,l}}$	0.63	0.87	0.26	0.32
$P_{\text{IGBT,OFF,u}}$	0.14	0.17	0.46	0.48
$P_{\text{IGBT,OFF,l}}$	0.50	0.58	0.15	0.19
$P_{\text{Diode,rr,u}}$	0.07	0.08	0.24	0.25
$P_{\text{Diode,rr,l}}$	0.23	0.31	0.11	0.13
$P_{\text{tot,semi}}$	53.62	54.21	51.08	55.46
P_{Cap}	26.03	26.13	26.12	25.98

(b)

i_{circ}	dc		dc plus 2$^{\text{nd}}$	
Model	VSM	SW	VSM	SW
ϕ [rad]	$\pi/2$		$\pi/4$	
$P_{\text{IGBT,cond,u}}$	11.56	11.73	7.51	7.48
$P_{\text{IGBT,cond,l}}$	11.57	11.55	28.30	28.29
$P_{\text{Diode,cond,u}}$	11.24	11.35	9.07	9.02
$P_{\text{Diode,cond,l}}$	11.26	11.12	4.55	4.48
$P_{\text{IGBT,ON,u}}$	0.49	0.47	0.27	0.25
$P_{\text{IGBT,ON,l}}$	0.49	0.47	0.66	0.64
$P_{\text{IGBT,OFF,u}}$	0.22	0.31	0.13	0.19
$P_{\text{IGBT,OFF,l}}$	0.22	0.33	0.35	0.40
$P_{\text{Diode,rr,u}}$	0.19	0.19	0.12	0.10
$P_{\text{Diode,rr,l}}$	0.19	0.18	0.23	0.22
$P_{\text{tot,semi}}$	47.43	47.71	51.19	51.08
P_{Cap}	36.03	36.59	26.11	25.99

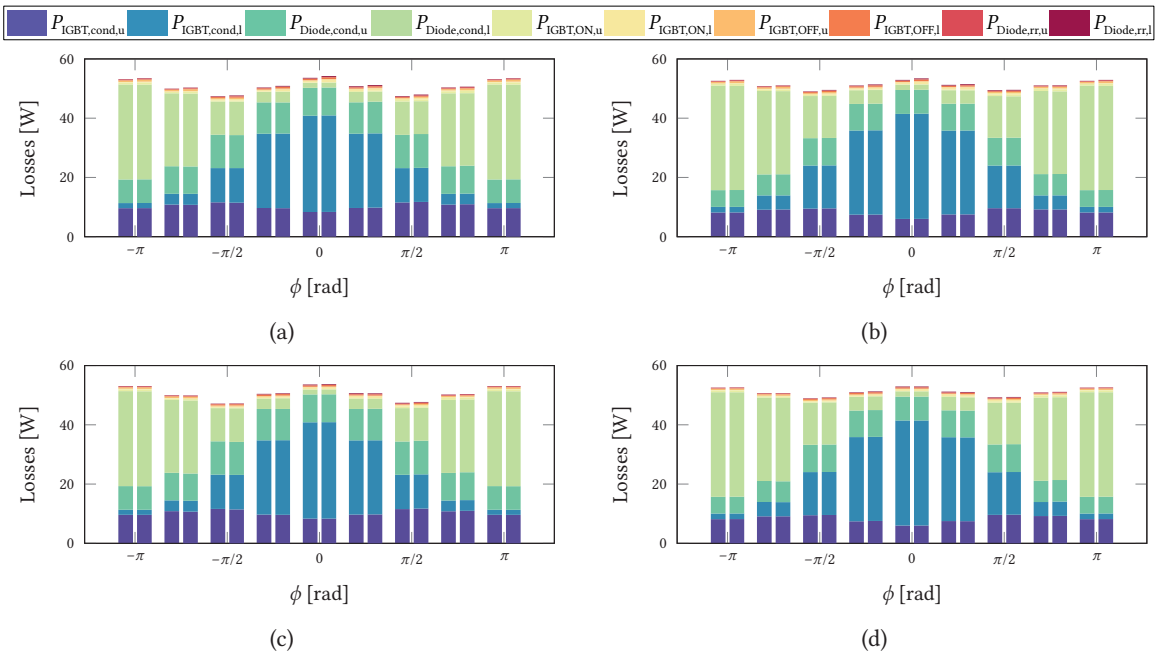


Fig. 8.8 Averaged semiconductor loss comparison between the VSM method (left side stacked bars) and the switched model (right side stacked bars): (a) PD-PWM with dc circulating current, (b) PD-PWM with dc plus 2$^{\text{nd}}$ harmonic injection circulating current, (c) PS-PWM with dc circulating current and (d) PS-PWM with dc plus 2$^{\text{nd}}$ harmonic injection circulating current.

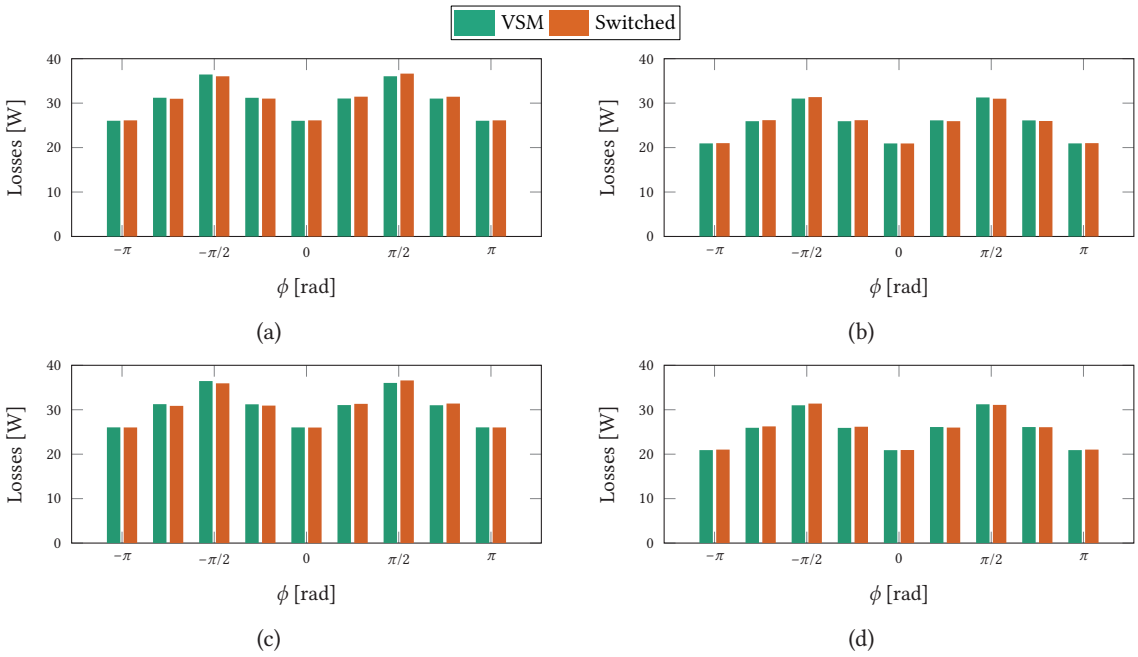


Fig. 8.9 Averaged cell capacitor bank losses comparison between the VSM concept (left side bars) and the switched model (right side bars): (a) PD-PWM with dc circulating current, (b) PD-PWM with dc plus 2nd harmonic injection circulating current, (c) PS-PWM with dc circulating current and (d) PS-PWM with dc plus 2nd harmonic injection circulating current.

Given the assumptions required for the VSM concept, a very good accuracy is obtained, as the loss estimation error is below 2 % for both semiconductor and capacitor losses. The source of this error comes from the branch current ripple and the cell capacitor voltage spread that are not captured by the VSM. These could be mitigated by an enhanced analytical description, which goes beyond the objectives of this work.

It is important to state that the branch current ripple envelope is not simply dependent on the instantaneous branch modulation index, apparent switching frequency and branch inductance value. Similarly, the capacitor voltage spread is not linearly proportional to the apparent branch switching frequency or average capacitor voltage ripple (as shown in **Fig. 8.1**).

The VSM allows for a very fast evaluation of the MMC cell's stresses, while considering directly the influence of the circulating current control strategy and impact of different modulation schemes. A benchmarking of the simulation times for obtaining the inputs of the loss tool (as the execution of the loss tool is negligible) between the VSM concept and a switched model has been performed on the same computer. The results are shown in **Fig. 8.11**.

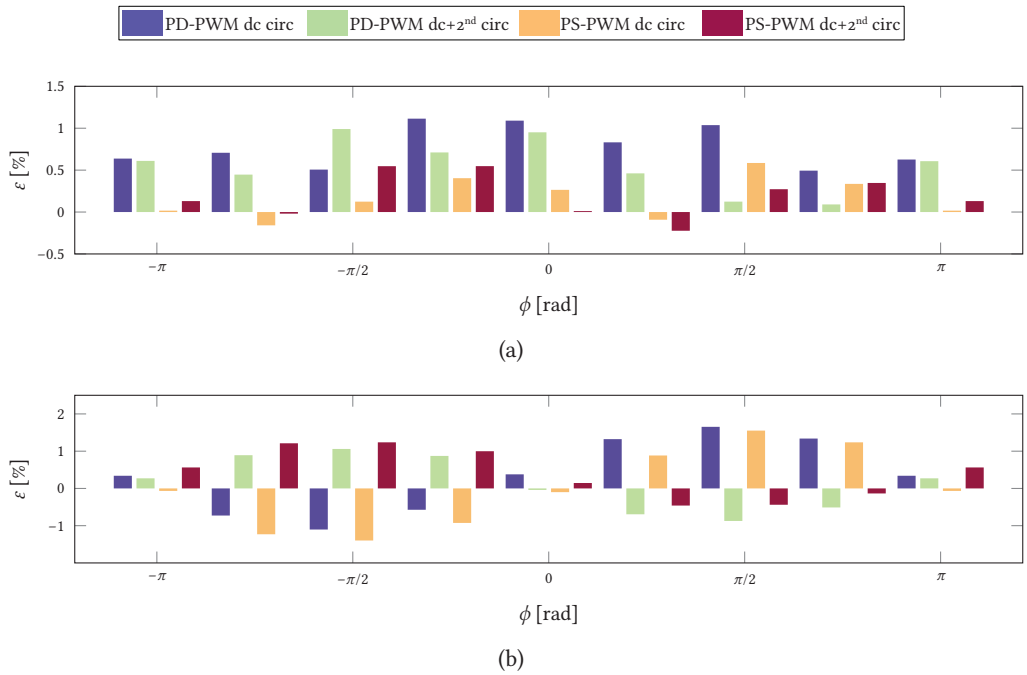


Fig. 8.10 Relative error plots for each modulation method and circulating current injection strategy: (a) semiconductor average losses and (b) capacitor average losses.

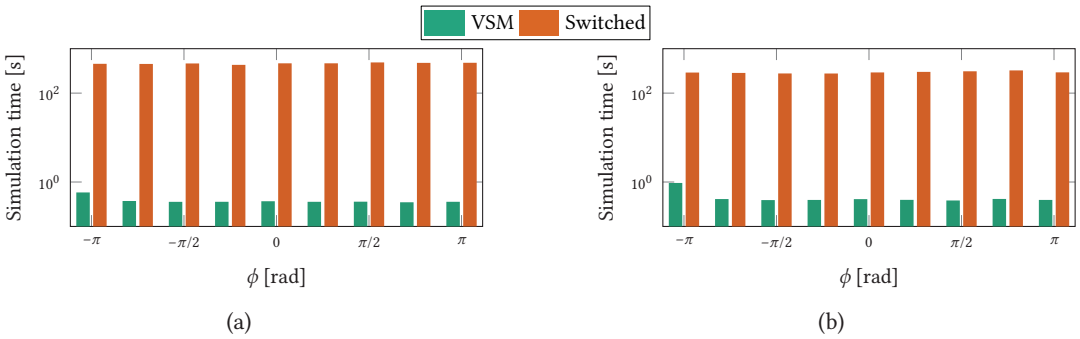


Fig. 8.11 Computational time benchmarking between the VSM method and the switched model: (a) PD-PWM with dc circulating current and (b) PS-PWM with dc circulating current. The time overhead for $\phi = -\pi$ corresponds to the loading time of the model in Simulink. The time overhead due to the sorting algorithm is clearly visible between PD-PWM and PS-PWM. Similar results are obtained for dc plus 2nd harmonic injection circulating current.

8.8 Discussion

Starting from a set of relatively simple branch current and voltage equations, with deterministic circulating current injection strategy enabled by a circulating current controller, the averaged MMC waveforms have been derived. Those waveforms have been used as inputs for the semiconductor loss tool in combination with the proposed VSM concept. The proposed concept has been compared with switched models of the MMC under two PWM modulation schemes: (i) PD-PWM and (ii) PS-PWM. A compression of a large number of switching pulses is required for the application of the VSM concept,

which can be easily realized with a quantizer and one suitable carrier. It has been shown that there is a good agreement between the predicted (analytically) and obtained (switched) converter waveforms in steady-state, under the conditions of limited voltage spread among the capacitor voltages of the same branch and limited branch current ripple (compared to the branch current average value). With a higher apparent branch switching frequency, the impact of the assumptions associated with the VSM method is expected to be reduced. Moreover, the loss difference is within the usual safety margin that is taken for any industrial grade product during the design process. The speed gain is in the range of 600 between the semi-numerical and switched simulations. This significant gain is a real advantage for the VSM concept, as a complete converter loss map for any possible operating point can be obtained almost instantaneously. The necessity to run loss calculation in closed-loop operation is fully justified by the particular role of the circulating current in an MMC, and with the aid of the VSM concept, this problem is significantly simplified without any loss of information.

9 Medium voltage MMC prototype design

MV converter designs require special components and arrangements due to the presence of higher voltages, even though the cell designed in this thesis is of modest ratings. The design description starts from the cell concept. After the semiconductor device selection, the Flyback-based ACPS with a planar transformer, instead of an externally supplied ACPS, is designed. Electrical tests of the cell verify the well functioning of its subcircuits. Finally, the cabinet layout, and its insulation coordination according to the IEC 61800-5 standard, are presented and its compliance is verified experimentally with a series of ac dielectric withstand tests.

9.1 Introduction

The MMC prototype, currently under development, has the following ratings:

- 0.5 MVA apparent power
- 10 kV MVdc connection
- Either 400 V, with the three-windings GIMC transformer, or 6 kV transformerless connection on the ac side
- 96 cells (16 per branch) with low-voltage semiconductor devices (1.2 kV)

Such a high number of cells was motivated by the high resolution waveform generation capability and flexibility for research, rather than designed for optimal efficiency.

9.2 Cell concept

The MMC cell concept is presented in **Fig. 9.1**. The cell functionalities are divided into four categories:

Power processing The semiconductor is an H-bridge module[1]. It can either operate as a unipolar or bipolar cell thanks to the hardware reconfiguration (HR). The cell capacitor bank is made out of six electrolytic capacitors[2], for a total cell capacitance C_{cell} of 2.25 mF.

[1] Semikron SK 50 GH 12T4 T, 1.2 kV/50 A.

[2] Exxelia Sic Safco Snapsic 4P 1.5 mF/400 V.

Control & communication The cell controller[3] handles the communication with the upper layer control (via Rx/Tx fiber optical links), measures the cell state (V_{cell}[4] and i_{br}[5] are required for the control), performs the decentralized modulation (via $\text{sw}_{\text{GD1..4}}$), monitors the cell condition (IGBT module temperature sensing with a thermistor, IGBT driver fault state assessment through the processing of $\text{fault}_{\text{GD1..4}}$ and $v_{\text{HB1..2}}$, ACPS failure with PS_{fail}).

Protection The protection part comprises a fast acting device with two anti-parallel thyristors[6] (THYB) and a slow (and permanent) bypass with a relay[7] (RELB). The protection is either activated from software (in case of gate driver (GD) fault, over-current, etc.) or self-triggered by the over-voltage detection (OVD) circuit (a chain of transient-voltage-suppression (TVS) diodes) of the cell terminal voltage. In case of ACPS failure, an energy buffer stores a sufficient amount of energy to achieve the cell bypass. In addition, a discharge relay ensures a finite discharge time of the remaining stored energy in the cell and closes when the ACPS shuts down.

Auxiliary cell power supply The ACPS is based on the Flyback topology and generates (isolated low) voltage levels for the cell controller (+5 V that is converted to +3.3 V with a low-dropout (LDO) regulator[8]), the protection circuit (+80 V, floating ground) and the IGBT GDs[9] (4× +15 V, 2× floating grounds for the high side IGBTs) from the cell voltage.

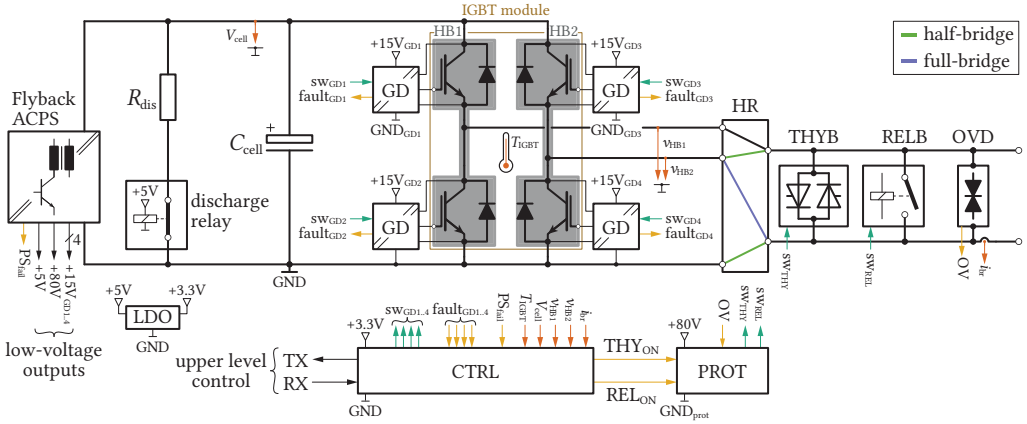


Fig. 9.1 MMC cell concept with only the main signals and elements to highlight its different functionalities.

Two boards, a power and a controller board, are assembled to form the MMC cell, as illustrated in **Fig. 9.2**. The realized cell with the two boards assembled is shown in **Fig. 9.3**. Details about the choice and sizing of the various cell components are presented in the subsequent paragraphs.

[3] TI Piccolo TMS320F28069.
[4] Resistive voltage divider and TI OPA328.
[5] Allegro ACS759.
[6] Semikron SK70 KQ, 1.2 kV/72 A_{rms}.
[7] KG K100.
[8] TI TPS73733.
[9] Broadcom ACPL-332J.

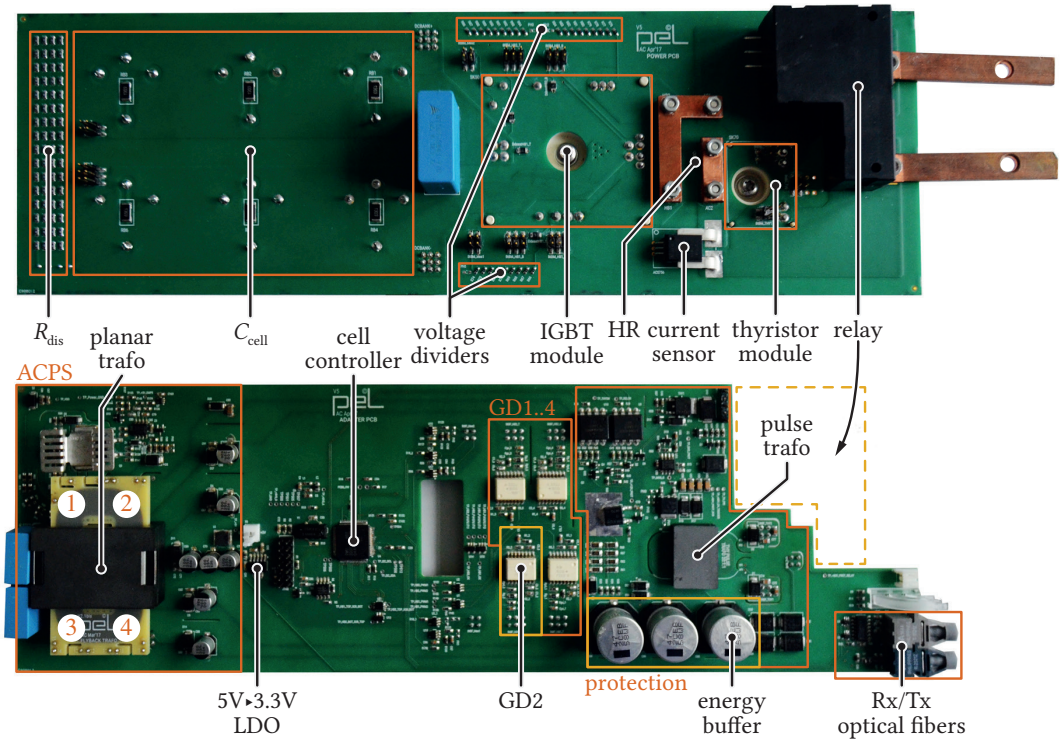


Fig. 9.2 MMC cell power (top) and controller (bottom) boards top view.

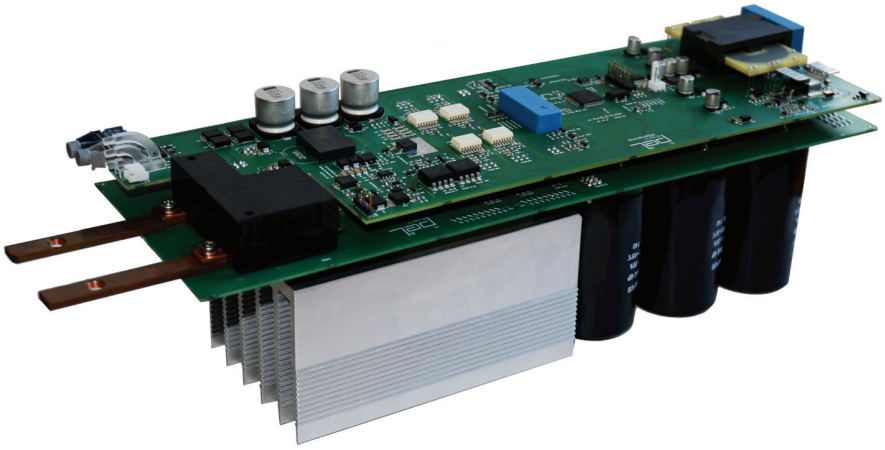


Fig. 9.3 Realized MMC cell, with the controller and power boards assembled.

9.3 Cell losses

A series of potential semiconductors, rated for 1.2 kV/50–70 A, have been evaluated with the VSM loss estimation method presented in **Chap. 8** (Infineon FF50R12RT4, Infineon F4-50R12KS4, Infineon F4-50R12KS4 B11, Semikron SK 50 GB 12T4 T, Semikron SK 50 GH 12T4 T, Semikron SKM50GB12T4, Semikron 26GH12T4V11). Besides the semiconductor losses, the packaging, and especially the matching package height for the anti-parallel thyristor module, were decisive, since the two semiconductor

devices are sharing the same heatsink. The adopted solution is a combination of the Semikron SK 50 GH 12T4 T (IGBT full-bridge module) and the Semikron SK70 KQ (thyristor module), both in Semitop package [142]. It was found that the semiconductor losses are below 55 W for an apparent branch switching frequency of 3 kHz, to which 35 W of losses from the cell capacitor bank shall be added. In total, the cells losses sum up to 8.64 kW of losses, which is 1.73 % of 0.5 MVA.

9.4 Branch capacitance selection

The converter energy requirements leading to the branch capacitance selection were discussed and compared in **Sec. 3.4**. For the converter prototype, a more conservative design was selected. A simplified expression considering a dc circulating current and neglecting the branch impedance voltage drop was derived in [18]:

$$\Delta W_{\text{cell}} = \frac{2}{3}\frac{S}{m\omega N_{\text{cell}}}\left[1-\left(\frac{m\cos\phi}{2}\right)^2\right]^{3/2} \Longrightarrow C_{\text{cell}} = \frac{\Delta W_{\text{cell}}}{2\varepsilon V_{\text{cell}}^2} \tag{9.1}$$

where S is the nominal apparent power, m the modulation index at nominal output voltage, ω the line frequency, ϕ the load angle and ε the voltage ripple coefficient. Equation (9.1) is maximum for $\phi = \pm\pi/2$ (cf. **Fig. 9.4**). With $\varepsilon = 5\,\%$, it is found that $C_{\text{cell}} = 1.9\,\text{mF}$ ($C_{\text{br}} = 118.75\,\mu\text{F}$, corresponding to an energy requirement of 71.25 kJ/MVA). The installed cell capacitor value is $3 \times 1.5\,\text{mF}/2 = 2.25\,\text{mF}$.

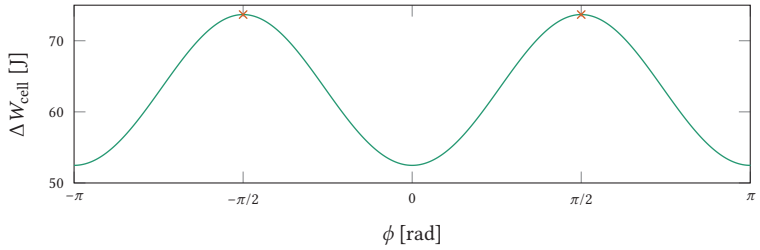


Fig. 9.4 Evaluation of (9.1) for the MV MMC prototype with $S = 0.5\,\text{MVA}$ and $m = \hat{v}_{\text{ac}}/(V_{\text{dc}}/2) = 0.9$.

The corresponding converter SOAs are shown in **Fig. 9.5**. Compared to the one obtained with the minimum converter energy requirement in **Sec. 3.5**, they are extended beyond the circle $S = 0.5\,\text{MVA}$, irrespectively of the CM and harmonic circulating current injection method.

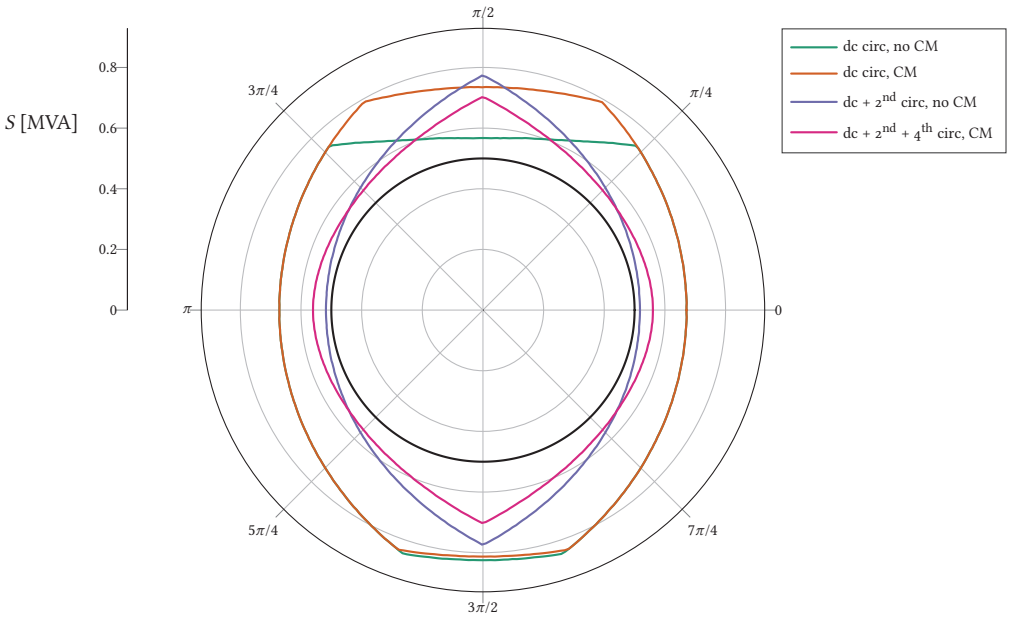


Fig. 9.5 MMC SOAs derived from the power equations without passives with $C_{\text{br}} = 118.75\,\mu\text{F}$ ($C_{\text{cell}} = 1.9\,\text{mF}$). The black circle corresponds to $S = 0.5\,\text{MVA}$.

9.5 Auxiliary cell power supply

The cell's controller, IGBT GD and protection circuits require (isolated) low-voltage supplies. Providing a low-voltage supply from ground (i.e. across a medium voltage isolation barrier), such as inductive power transfer [143] or inductive loop supply [144], is difficult due to the high voltage isolation requirements. For this reason, externally supplied ACPSs are often discarded in favor of internally supplied ACPSs (the power is tapped from the cell's capacitor bank), especially when cost constraints are tight. Several solutions have been proposed in the literature: tapped-inductor Buck converter [145] or series-connected Flyback for medium voltage cell [146]. From all these proposals, a Flyback converter supplied from the cell's capacitor is the simplest solution, as multiple secondary supply outputs can be easily achieved with a single switch. It greatly simplifies the isolation requirements in the surroundings of the cell. As a drawback, the MMC cells have to be energized from an external source (passive charging in open-loop) until the ACPSs start, followed by an activation of the distributed controllers, thus enabling active charging (in closed-loop). For the MMC cell discussed here, a Flyback-based ACPS with multiple outputs is selected.

9.5.1 Flyback specifications

This can be realized at once with a transformer[10] with multiple outputs (cf. **Fig. 9.6**). The transformer described and designed has six sets of secondary windings:

- $1\times$ 5 V, 4 W for the controller supply ($V_{+5\,\text{V}}$). This output is tightly regulated in closed-loop. In

[10] Even though the magnetic circuit in a Flyback converter is actually a multi-winding inductor, for the sake of brevity and schematic representation, it will be referred to as a multi-winding transformer.

practice, this is a tapped winding with the +15 V winding used to power the TI UCC28C44 chip [147]. The cell's ground potential is common with the cell controller's ground.

- 4× 15 V, 1.5 W for the IGBT GDs ($V_{GD1..4}$). An additional 900 V isolation is required between the upper and lower GDs windings.
- 1× 80 V, 15 W for 15 s operation when activated for the protection circuit (V_{prot}). The voltage is on purpose high in order to obtain a sufficiently large energy buffer with a relatively low storage capacitance value ($E \propto V^2$ – $E \propto C$ trade-off).

Due to the operating principle of the Flyback converter, a general 900 V isolation [148] is required between the primary and each secondary winding. Additionally, the start-up voltage is set to approximately 200 V (one third of the nominal operating voltage).

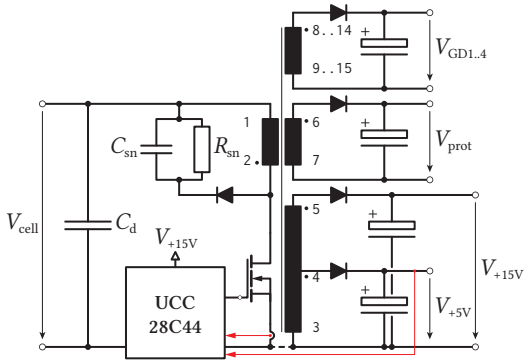


Fig. 9.6 Simplified Flyback circuit with seven sets of windings, where the bias circuit and additional filtering elements have been omitted. Each IGBT GD is supplied by a separated winding.

The cells are first charged passively from the outside (e.g., with an inrush current limiting resistor from the ac side). In that way, it only gets charged to the peak of the ac voltage, which roughly corresponds to approximately 45 % of the nominal cell voltage. As a consequence, in order to enable the active charging (in closed-loop), the ACPS should start its operation at a relatively low voltage. The minimum cell voltage at which the ACPS is expected to start is set to $V_{cell,min}$ = 200 V. The nominal cell voltage is $V_{cell,nom}$ = 625 V (considering a connection with a 10 kV_{dc} bus, with 16 cells per branch). The maximum cell voltage, related to the threshold voltage at which the cell's bypass gets activated for preserving its components (both the IGBTs and capacitors), is set to $V_{cell,max}$ = 900 V. The estimated ACPS input power is 20 W. The specifications for the planar transformer are summarized in **Tab. 9.1**. The detailed electrical design of the ACPS is presented in **App. A**.

Tab. 9.1 Technical specifications per winding for the planar transformer.

Winding	Voltage			Power
	Min.	Nom.	Max.	
pri	200 V	625 V	900 V	≈ 20 W
prot.		80 V		15 W during 15 s
+5 V		5 V		4 W
+15 V		15 V		1 W max
GD (4x)		15 V		1.5 W each

9.5.2 Planar transformer testing

A planar transformer with PCB integrated windings is chosen over a wound one to minimize the electrical parameters mismatch betweeen the 96 cells. The design procedure is detailed in **App. B**. The realized transformer (cf. **Fig. 9.7**) is tested first separately in order to verify that it is compliant with the design objectives. 125 custom gapped cores (gap on the center leg of the E core, as shown in **Fig. B.1**) were ordered from Cosmo Ferrites. Grinding and glueing of the ferrite cores was preferred over shimming and clamping for its increased flexibility and precision (no dependency on the isolated sheet's thickness).

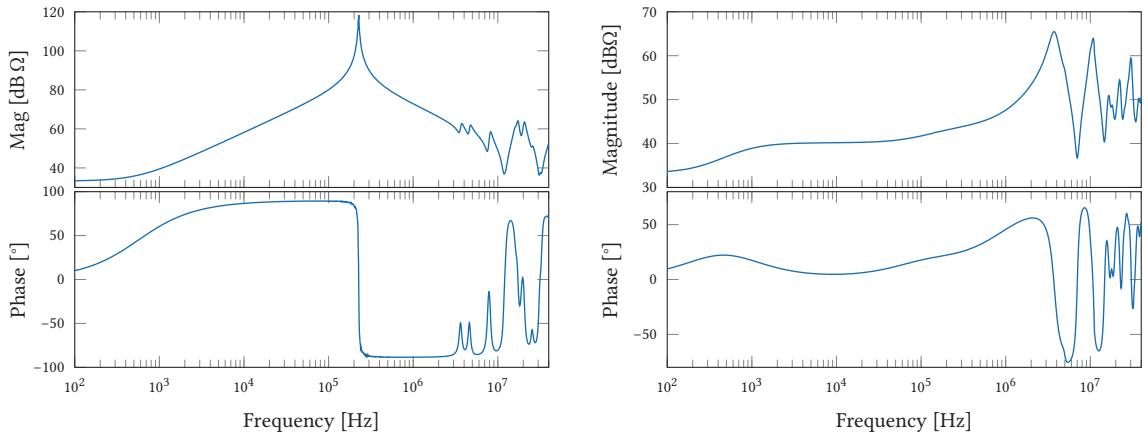
(a) (b)

Fig. 9.7 Realized planar transformer: (a) separate elements before assembly and (b) assembled transformer. The PCB is 61.6 mm × 34.1 mm × 3 mm and the ferrite core 43.2 mm × 27.8 mm × 13.6 mm. The total planar transformer footprint is 61.6 mm × 43.2 mm. The pin numbers on the planar transformer PCB are matching the ones in **Fig. 9.6**.

Impedance measurements The transformer is measured with an Omicron Bode 100 network analyzer. The results are shown in **Fig. 9.8**. In the low frequency region ($f < 1\,\text{MHz}$), the characteristic is dominated by the core geometry and the air-gap, while in the high frequency region the characteristic is dominated by the parasitic elements in the PCB integrated windings. The transformer design experiences a main resonance at 228 kHz (which corresponds to a capacitance of 37.5 pF).

The gapping manufacturing repeatability process has been assessed by measuring the magnetizing inductance at 20 kHz for all 125 cores. The mean value is 12.9 mH ($\sigma = 0.18\,\text{mH}$), which is slightly higher than the target value of 12.5 mH, since the glueing process adds an additional air-gap on the outer legs, resulting in a small drop in L_p.

AC dielectric withstand test The planar transformer's PCB is tested in a Faraday cage with a single-phase high step-up line frequency test transformer (capable of generating voltages up to 100 kV) and an Omicron MPD600 partial discharge (PD) measurement system in order to see if any breakdown occurs in the substrate. As the primary layer is spread among five layers distributed almost symmetrically inside the layer stack, it is sufficient to perform a single test where the primary winding is shorted and all secondary windings are shorted together and tied to the same potential. A trapezoidal voltage profile according to the IEC 61800-5 standard [149] is applied and the results are shown in **Fig. 9.9**. Since the detected peak charge 2 pC is below the 10 pC threshold, the test is passed.



(a) (b)

Fig. 9.8 Transformer impedance measurements with an Omicron Bode 100 network analyzer from 100 Hz to 40 MHz: (a) open-circuit test (all secondaries open), giving L_p = 12.99 mH (R_s = 48.12 Ω) at 20 kHz and (b) short-circuit test (all secondaries shorted), giving L_σ = 88.21 µH (R_σ = 102.64 Ω) at 20 kHz. The curves are obtained with 1601 logarithmically spaced frequency points.

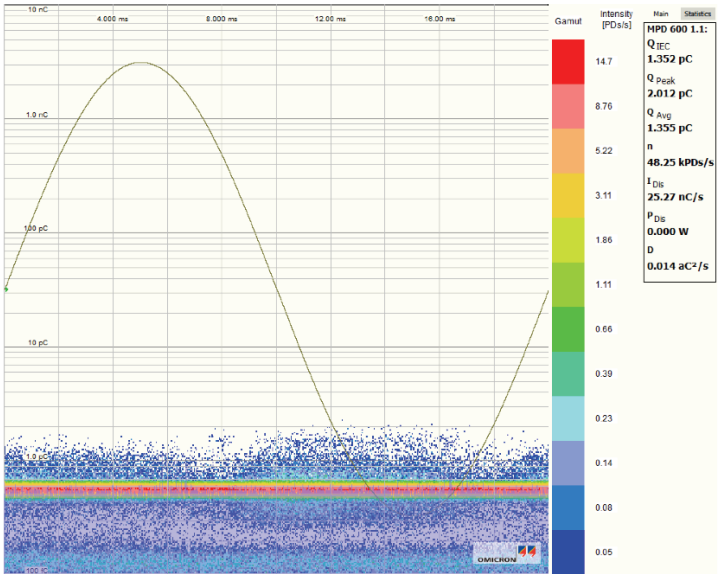


Fig. 9.9 AC dielectric withstand test results. A full 50 Hz period allows to potentially identify a higher level of PD at high dv/dt. Additional statistics are provided in the top right corner.

9.5.3 ACPS testing

The designed planar transformer is inserted on the MMC cell inside the ACPS circuit as shown in **Fig. 9.2**.

Start-up test The start-up of the ACPS was performed with a cell voltage stepped from 0 V to its nominal value in **Fig. 9.10(a)** (due to the limited dv/dt from the Delta SM 660-AR-11 power supply that emulates the cell charging, whose final part is visible in the picture). Due to the undervoltage

lockout (UVLO), the PWM controller starts its operation once the PWM controller voltage V_{DD} reaches 14.5 V. Then a soft start is initiated and the gate pulses are released. V_{DD} is slowly charged once the +15 V output gets energized.

Steady-state operation and efficiency The steady-state operation at nominal cell voltage of the ACPS is reported in **Fig. 9.10(b)**. The outputs are within their ripple limits and a small jitter is observed at the switching instants. The efficiency was measured to 89.4 %, which is higher than the usual Flyback efficiency (around 80 %).

Shutdown test The shutdown test was performed with a cell voltage step from its nominal value to 0 V. As long as V_{DD} is higher than its UVLO turn-off threshold (9 V), the ACPS continues its operation, despite not being able to maintain the controlled output to +5 V with $D = 0.5$ when the cell voltage is below 178 V. The result is shown in **Fig. 9.10(c)**. The slow $\mathrm{d}v/\mathrm{d}t$ of the cell voltage is again limited by the power supply used to emulate the cell voltage. The complete shutdown time is around 500 ms. Once the ACPS stops its operation, a string of discharge resistors (R_{dis} in **Fig. 9.1**) ensures a finite converter discharge time.

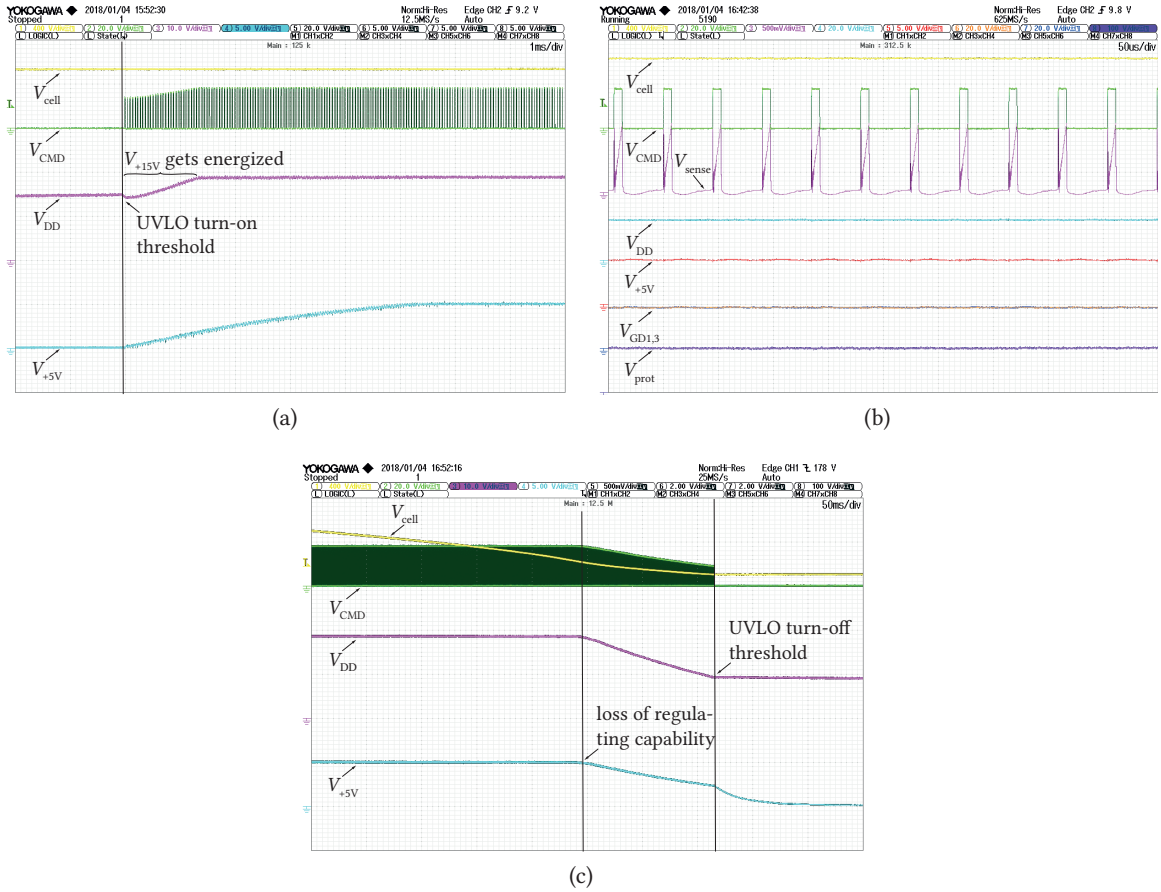
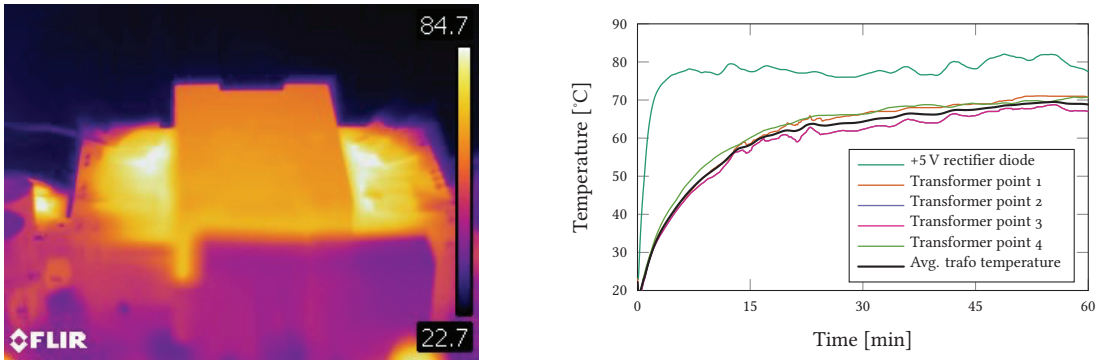


Fig. 9.10 ACPS operation modes: (a) start-up, (b) steady-state operation at nominal cell voltage with each winding loaded as in **Tab. 9.1** and (c) shutdown. V_{sense} is the voltage across the 1.5 Ω sensing resistor, i.e. the image of the primary current.

Thermal measurements The thermal measurements are presented as an overall view of the ACPS, where the temperature was observed with a FLIR E60 infrared camera in **Fig. 9.11(a)**. Additionally, the temperature at five specific locations on the ACPS (as shown in **Fig. 9.2**, plus the diode on the +5 V output) were recorded over the span of one hour of operation at nominal cell voltage from cold start. The results are shown in **Fig. 9.11(b)**. Certain measurements points on the transformer experience EMI and consequently differ one from another. As a consequence, it was decided to include an average of the measurements, which can represent the transformer temperature in a better way.



(a) (b)

Fig. 9.11 Thermal measurement: (a) infrared thermal camera capture after one hour of operation and (b) thermocouples measurements on four different points on the transformer PCB and on the $V_{+5\,\mathrm{V}}$ rectifier diode.

9.6 Cell testing

Two basic tests are performed on the MMC cell besides the ACPS operation verification. This is not a thorough testing of the cell. Besides operation at full load and maximum voltage for both cell types, thermal testing and current sharing between the two parallel half-bridge modules should be verified in priority as follow-ups.

9.6.1 Power stage testing

The first test verifies the operation in full-bridge cell type. The capacitor bank is supplied with a Delta SM 660-AR-11 power supply. The full-bridge is operated in open-loop with a sinusoidal reference at 50 Hz and a fixed modulation index of 0.5, supplying an inductive load (7.86 mH/0.2 Ω at 50 Hz). The switching frequency for each leg is set at 1 kHz (2 kHz effective switching frequency seen by the load in unipolar modulation). The result with $V_{\mathrm{cell}} = 250\,\mathrm{V}$ is shown in **Fig. 9.12**, with a peak load current of 4.9 A.

9.6.2 Protection testing

The second test focuses on the activation of the protection circuit. The cell terminals are supplied with a dc voltage source in series with a load resistor. The protection firing sequence is shown in **Fig. 9.13**. Once the relay bypass command is issued ($\overline{\mathrm{REL}_{\mathrm{ON}}}$), firing pulses at 10 kHz with a 10 % duty-cycle to

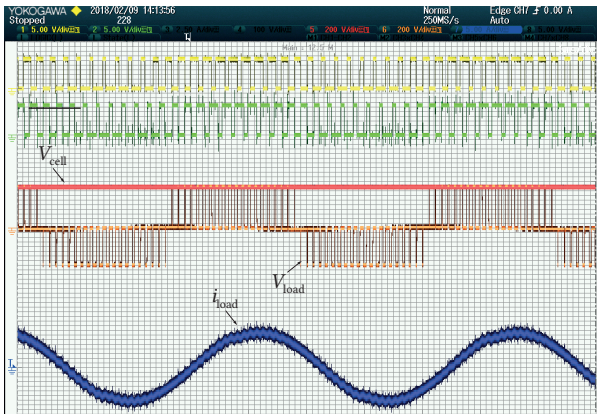


Fig. 9.12 Cell testing in full-bridge type supplying an inductive load. The first two signals from the top are the gate signals s_1 and s_4 from the diagonal IGBTs.

trigger the thyristor module are released through the PCB integrated pulse transformer, same as the relay command signal (the relay closing time is approximately 8.5 ms after the command signal is received).

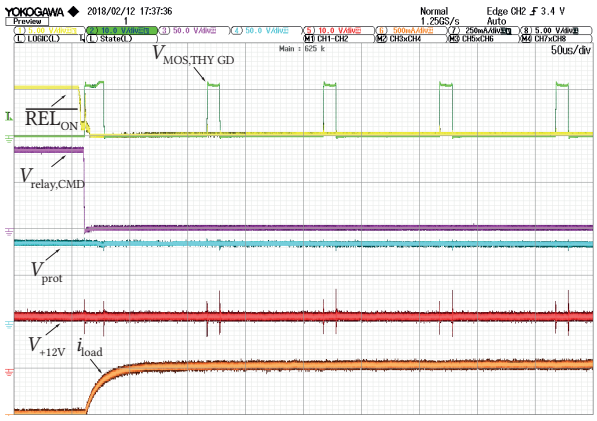


Fig. 9.13 Cell protection firing sequence. The $V_{+12\,V}$ signal is the supply voltage for the protection circuit electronics, while the protection's energy storage is supplied with 80 V.

9.7 Electrical cabinet layout

Considering the connection to $10\,kV_{dc}$, several design constraints have to be satisfied, related to the choice of cooling medium, the insulation concept, clearance and creepage distances, as well as selection of suitable materials and arrangements of the different sub-assemblies that contribute actively to meeting the standards. Various norms and standards have been consulted (e.g., UL 840 [148], IEC 61800-5-1 [149]) to identify the applicable requirements and constraints, keeping in mind the laboratory use of the equipment, the presence of already installed protection equipments and controlled environmental conditions. Design tools, such as FEM[11], are used for simulation and design optimization, prior to the experimental verification with a high voltage test equipment.

[11] All FEM simulations in this section are performed with the software ANSYS Maxwell from the company ANSYS Inc.

Unlike industrial MMC converters, where an horizontal disposition of the branches is generally chosen for easier voltage scalability and increased power density (e.g., [150]), the converter prototype is designed such that one phase-leg fits in one standard IT cabinet (for cost reasons). Also, forced air cooling rather than water cooling was selected. Details about the complete cooling concept are presented in [151].

9.7.1 System level considerations

The schematic of the complete laboratory system is shown in **Fig. 9.14**. The 10 kV_{dc} supply is provided through a laboratory installed step-up transformer (vector group Yd11y0) and a 12-pulse diode rectifier, while the 400 V_{ac} output connection is available for load or grid connections after the three-windings GIMC transformer. Alternatively, a direct access to the MVac output is possible by substitution of the output transformer with conventional branch inductors. The complete prototype is realized in a modular fashion and partitioned into five cabinets. The focus is set on the three phase-leg cabinets, and discussion related to the other parts of the system are omitted. Considering the IEC 61800-5-1 standard, the nature of the installation with no direct connection or exposure of the circuit to the direct transient over-voltages and the choice of forced air cooling with air from indoor, over-voltage category (OVC) 1 and pollution degree (PoD) 1 should suffice design. Nevertheless, as this is a laboratory prototype for multipurpose use, more stringent OVC2 and PoD2 are selected. Four insulation zones are identified, each one characterized by different working voltages, materials and requirements for insulation coordination. They are graphically presented in **Fig. 9.15**.

Zone 1 insulation coordination inside the cell's enclosure. The nominal cell capacitor voltage ($V_{cell,nom}$) is 625 V_{dc}, with a maximum voltage of 900 V_{dc} ($V_{cell,max}$) before the trigger of the protective cell bypass. The system voltage is 1 kV_{ac}.

Zone 2 insulation coordination between the cells within a branch. Due to the connection of the cells, the maximum voltage between two adjacent cells is different on the horizontal and vertical axes. It is equal to $V_{cell,max}$ and $4V_{cell,max}$, respectively. They correspond to system voltages of 1 kV_{ac} (no interpolation allowed) and 3.6 kV_{ac}.

Zone 3 insulation coordination between a branch and the surrounding cabinet (at ground potential). This also includes any passages made available for cables routing. The system voltage considered for insulation coordination is 6.6 kV_{ac}.

Zone 4 insulation coordination related to the low voltage circuits, such as control boards or auxiliary power supply systems. The nominal voltage is 400 V_{ac}.

9.7.1.1 Zone 1 - MMC submodule

Each cell is enclosed in a metallic box, providing shielding, protection and shaping of the surrounding E-field. Each cell defines the enclosure potential, which is referenced to the negative capacitor bank terminal. It effectively floats on a potential with respect to the external system ground. As the cell is a low voltage circuit, both UL 840 and IEC 61800-5-1 are considered. Yet, with IEC 61800-5-1 being a safety standard, it is more relevant for the design outside the cell. By considering a maximum expected

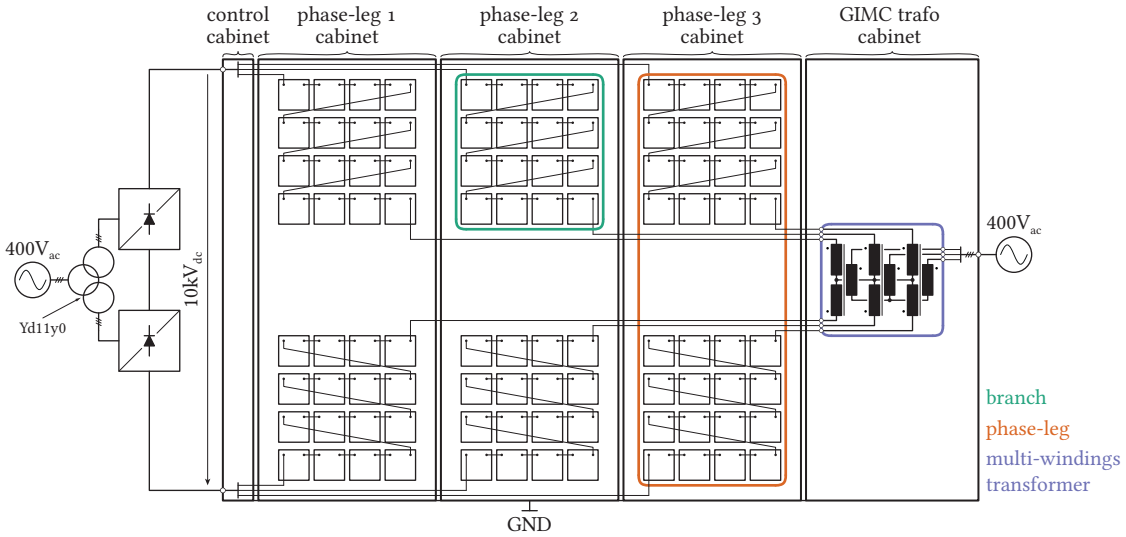


Fig. 9.14 MMC prototype converter simplified layout and connection to the laboratory infrastructure.

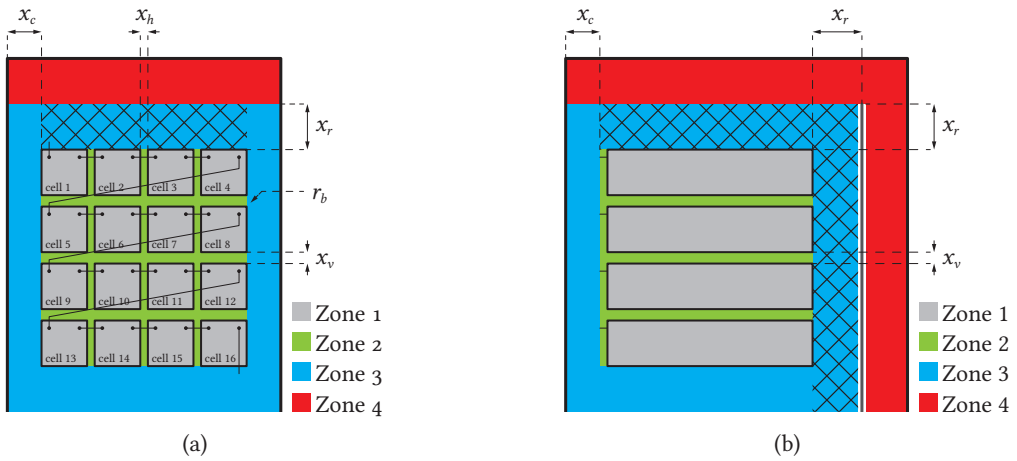


Fig. 9.15 System partitioning and definition of the four insulation coordination zones inside one phase-leg cabinet: (a) front view and (b) side view. The relevant distances are also indicated, and x should be substituted with d_{L} and d_{C} for clearance and creepage distances, respectively. The hatched areas correspond to required reinforced isolation.

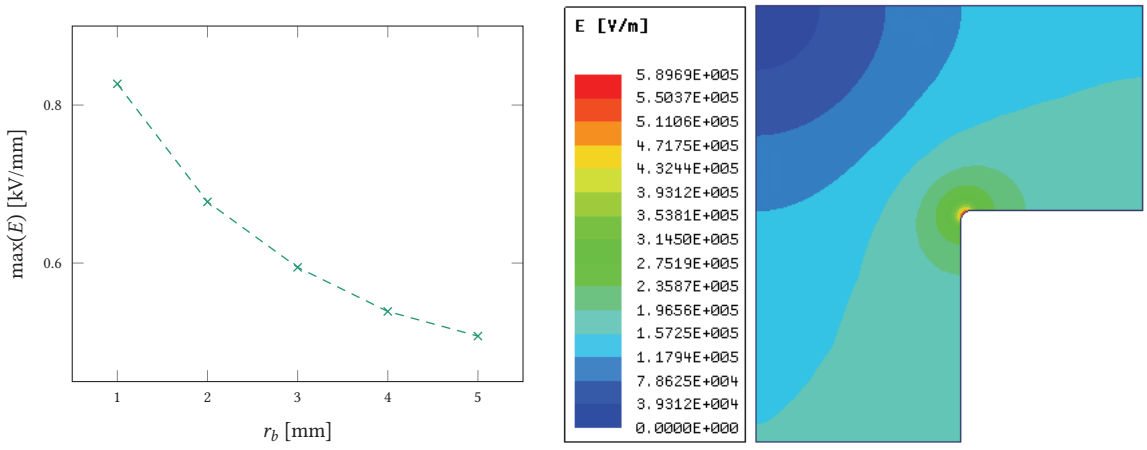
voltage inside the cell of $V_{\mathrm{cell,max}}$, OVC2 and FR-4[12] for printed circuit board (insulating material group IIIa, comparative tracking index (CTI) between 175 and 200), the minimum clearance and creepage distances are determined and applied, respectively (cf. **Tab. 9.2**). The complete cell assembly is placed inside a custom protruded aluminum enclosure, designed to provide a mechanical support, a defined air channel, and a shaping of the E-field at the corners below the critical levels considering air insulation inside the cabinet (maximum theoretical air breakdown threshold of 3 kV/mm). In **Fig. 9.16(a)**, the enclosure corner radius r_b is varied from 1 to 5 mm and multiple FEM simulations are performed to verify that the maximum E-field is below the critical value. The E-field magnitude for the final design with r_b = 3 mm is presented in **Fig. 9.16(b)** (constraint from the box manufacturing

[12]Glass-reinforced epoxy laminate material.

process, since r_b = 1 mm would have sufficed).

Tab. 9.2 Summary of Zone 1 isolation distances requirements.

Variable	Minimal value [mm]
$d_{\text{L,cell PCB}}$	3
$d_{\text{C,cell PCB}}$	6.3



(a) (b)

Fig. 9.16 FEM E-field magnitude near the top corner: (a) evolution of max(E) when r_b is varied from 1 to 5 mm and (b) E-field magnitude with r_b = 3 mm plus 62 mm distance to the ground.

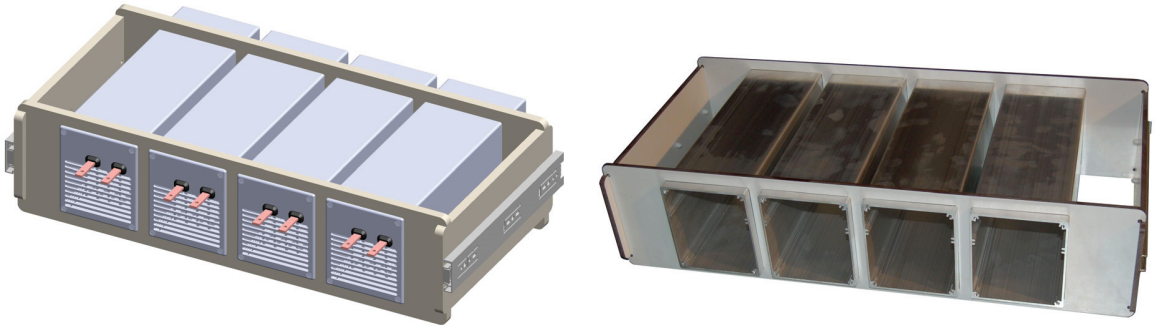
9.7.1.2 Zone 2 - MMC branch

All 16 cells of one branch are arranged into a 4 × 4 matrix, as shown in **Fig. 9.15(a)**. Due to this arrangement, the horizontal and vertical potential differences during operation between two adjacent cells are not the same. As previously stated, they equal $V_{\text{cell,max}}$ and $4V_{\text{cell,max}}$, respectively. This has been taken into account during the design of the cell enclosure and for the choice of the clearance distances. Even though IEC61800-5-1 considers non-homogeneous E-field distribution, care is taken to avoid sharp edges on the enclosure and avoid excessive E-field values (namely mitigate the peak effect). Additionally, to provide mechanical support to the cells, easy installation and quick removal from the cabinet, the cells are grouped in a drawer alike sub-assembly that consists of four cells, as shown in **Fig. 9.17**. The material used for the drawer is a melamine / paper-based laminate[13] (insulating material group I, CTI of 600), which was helpful to reduce creepage distances in the design. As each drawer has metallic sliding rails for easy mounting, the insulation coordination must consider not only the distances relevant for the Zone 2, but also nearby Zone 3.

The constraints are presented in **Tab. 9.3** and have been verified using FEM simulations. To define the exact shape of the cell enclosure, the corner's radius has been optimized to shape the surrounding E-field. At the same time, horizontal and vertical distances for mechanical integration have been verified with respect to the maximum E-field values observed at relevant points. FEM simulations

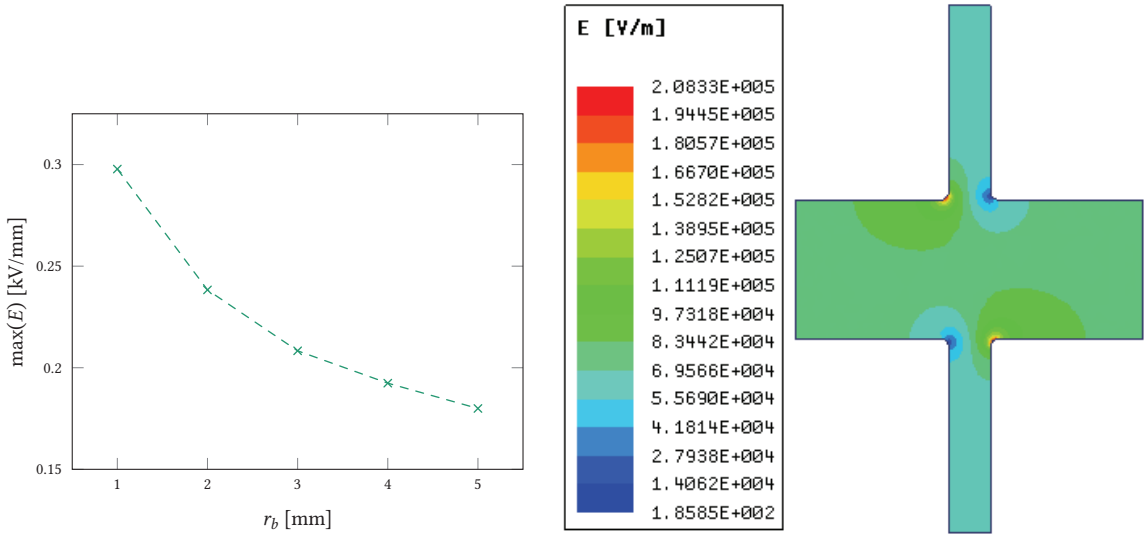
[13] Melaminkaschiertes Hartpapier (MKHP).

have been carried out with an excitation voltage equivalent to 1.1 kV_{ac} and 4 kV_{ac} for horizontal and vertical clearances, respectively, according to the IEC61800-5-1 standard for AC test requirements. FEM simulation results are shown in **Fig. 9.18(a)**, from where it can be seen that the maximum values of E-field are substantially below the air breakdown level when r_b is varied from 1 to 5 mm. The E-field magnitude for the final design with r_b = 3 mm is presented in **Fig. 9.18(b)**.



(a) (b)

Fig. 9.17 Drawer sub-assembly containing four cells: (a) CAD drawing and (b) realization.



(a) (b)

Fig. 9.18 FEM E-field magnitude: (a) evolution of max(E) in function of the enclosure corner radius r_b and (b) E-field magnitude around four cell enclosures with r_b = 3 mm.

Tab. 9.3 Summary of Zone 2 isolation distances requirements.

Variable	**Minimal value** [mm]
$d_{L,h}$	6.8
$d_{C,h}$	3.2
$d_{L,v}$	30
$d_{C,v}$	12.5

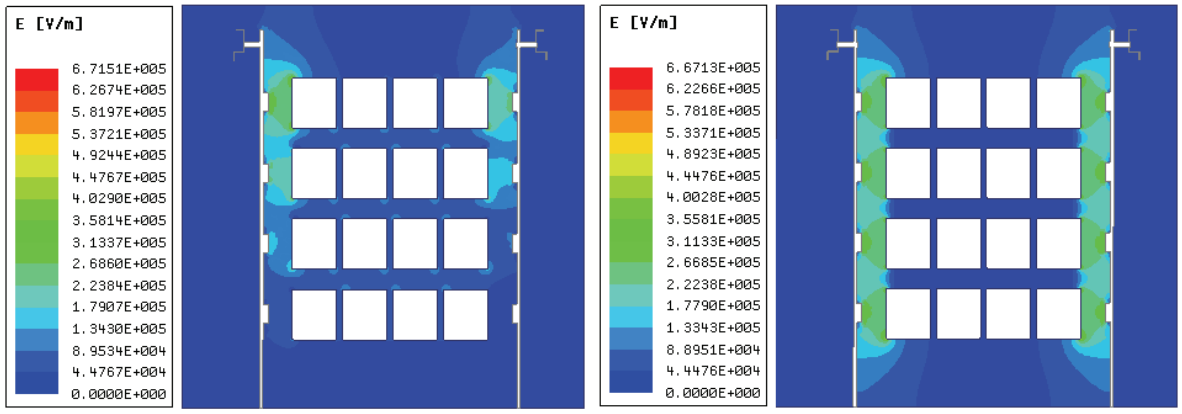
9.7.1.3 Zone 3 - MMC phase-leg

Since various metallic parts of the cabinet are at the ground potential with respect to the floating cells, the full system voltage rating must be taken into account. A basic insulation is sufficient for most of the Zone 3, considering the space between the branch assembly (live parts) and cabinet side walls at ground. The metallic sliding rails, mounted on the sides of each drawer, are the closest ground points from the live parts (cells). However the presence of low voltage circuits, such as a controller on top of the cabinet, requires reinforced or double insulation to be deployed. This is illustrated in **Fig. 9.15**, where the hatched areas of Zone 3 are those where reinforced insulation is required.

The constraints are presented in **Tab. 9.4** and have been verified using FEM simulations. Theoretically, there are $2^{16} = 65536$ cases that should be tested, however this number is way too large. The simulation results are shown in **Fig. 9.19** under the condition of the complete branch assembly (16 cells) only for symmetry reason, with an excitation voltage equivalent to 11 kV_{ac} (level required for ac test in case of basic insulation). As it can be seen, the values of the E-field observed near the mounting rails are sufficiently below the air breakdown level.

Tab. 9.4 Summary of Zone 3 isolation distances requirements.

Variable	**Minimal value** [mm]
$d_{\mathrm{L},c}$	60
$d_{\mathrm{C},c}$	50
$d_{\mathrm{L},r}$	102



(a) (b)

Fig. 9.19 Cabinet level FEM E-field magnitude simulations with: (a) 16 cells inserted (1 out of 2^{16} combinations) and (b) 16 cells bypassed (all clamped to the positive dc terminal). Only the upper branch is displayed, as similar results would be observed in the lower one due to geometry symmetry.

9.7.2 Final design

The manufacturing capabilities, required distances for handling as well as internal cabinet dimensions influenced the final design, which is summarized in **Tab. 9.5**. The selected cabinet (1970 mm × 800 mm

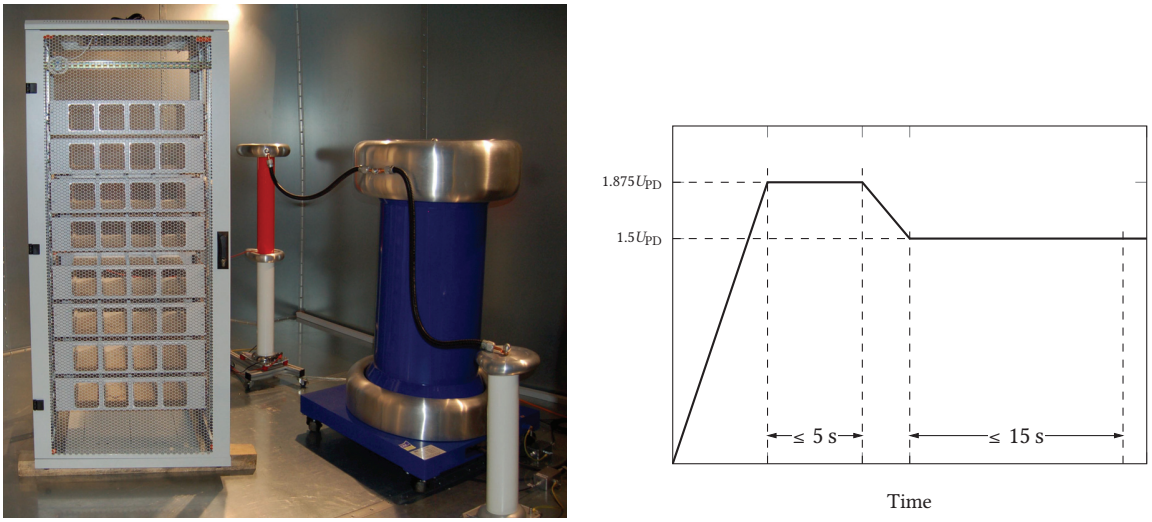
× 800 mm) is equipped with a meshed front door and an air chimney at the back for forced air cooling.

Tab. 9.5 Mechanical design summary. The distances concerning the PCB part of the cell are of less relevance and were intentionally omitted in this table.

Variable	**Minimal value** [mm]	**Actual design value** [mm]
r_b		3
$d_{\mathrm{L},h}$	6.8	15
$d_{\mathrm{C},h}$	3.2	15
$d_{\mathrm{L},v}$	30	50
$d_{\mathrm{C},v}$	12.5	275
$d_{\mathrm{L},c}$	60	81.5
$d_{\mathrm{C},c}$	50	93
$d_{\mathrm{L},r}$	102	120

9.7.3 Experimental verification

To verify the design, several tests are performed using the available high voltage test setup for ac dielectric withstand and PD measurements rated for 100 kV, 20 kVA [152]. The measurements were performed with Omicron MPD600 [153]. The inside of the Faraday cage is shown in **Fig. 9.20(a)**, with the high voltage step-up transformer, damping resistor, parallel capacitor to the device under test, which is the phase-leg MMC cabinet. The device was calibrated at 1 pC and the setup has a noise level below 100 fC. For each test, the voltage profile follows **Fig. 9.20(b)** with the appropriate U_{PD}. Please note that U_{PD} is equal to the recurring voltage of the system.



(a) (b)

Fig. 9.20 Ac dielectric withstand test configuration: (a) setup inside the Faraday cage and (b) voltage profile for the tests. The PDs are recorded on the second flat section (≤ 15 s) as specified in IEC 61800-5.

A series of tests were performed on the prototype:

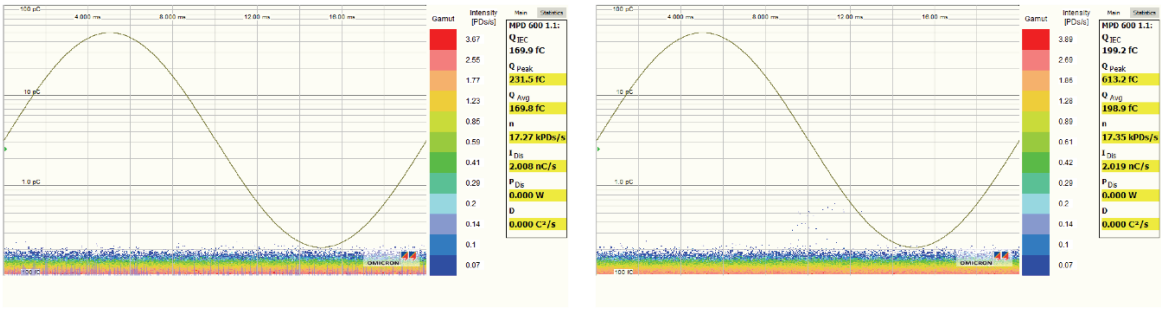
Test 1: Two adjacent cells of the same drawer This is the most critical test at the drawer level.

Other tests were performed, but their results are not shown here. A working voltage of 1 kV_{ac} is considered. The PD test result is presented in **Fig. 9.21(a)**. As it can be read on the image, Q_{Peak} = 231.5 fC, which is below the 10 pC limit specified by the standard.

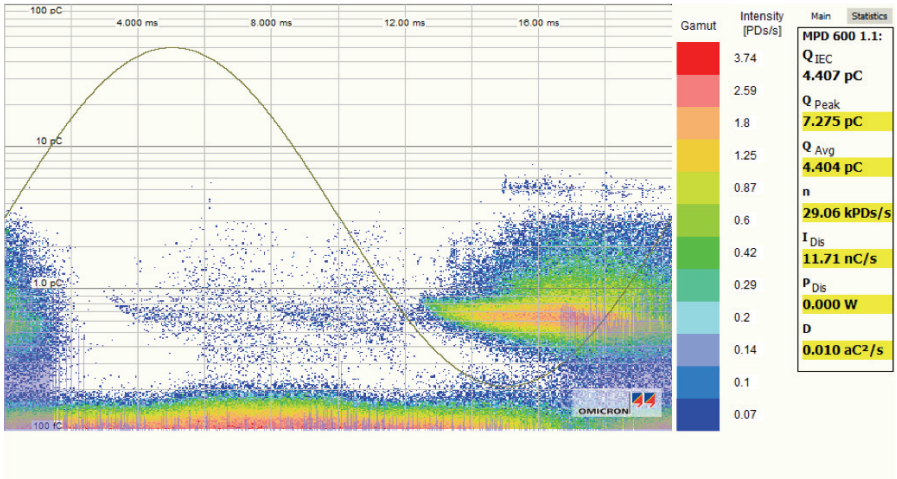
Test 2: enclosure to sliding rail (at ground) The drawer is designed such that the creepage and clearance distances between one sliding rail and the closest cell has to withstand the full input dc voltage. As is can be seen on **Fig. 9.17(b)**, the sliding rail is mounted on the drawer's vertical panel. The PD test result is presented in **Fig. 9.21(b)**. As it can be read on the image, Q_{Peak} = 613.2 fC, which is way below the 10 pC limit specified by the standard.

Test 3: phase-leg to cabinet frame (at ground) All cells are connected together (at the same potential), as at any point in time one cell or a group of cells can be at the maximum potential, depending on the branch insertion index. The PD test result is presented in **Fig. 9.21(c)**. As it can be read on the image, Q_{Peak} = 7.275 pC, which is below the 10 pC limit specified by the standard.

It is concluded that the insulation coordination design is compliant with the IEC standard.



(a) (b)



(c)

Fig. 9.21 Ac dielectric withstand test results: (a) PD histogram for test 1, U_{PD} = 1 kV_{ac}, (b) PD histogram for test 2, U_{PD} = 9.3 kV_{ac} and (c) PD histogram for test 3, U_{PD} = 9.3 kV_{ac}.

10
Summary, overall conclusions and future works

Nothing went according to the initial plan, but it's alright. Research is not meant to be planned in advance.

10.1 Summary and contributions

In this thesis, the interface between a MVdc grid and a LVac grid has been studied. The choice to use an MMC with an integrated magnetic component, namely the GIMC, was supported by efficiency and cost reasons. The conversion is characterized by a large voltage ratio between the two terminals, necessitating a transformer for voltage adaptation. Such a converter should ease the adoption of MVdc links that are compatible with the existing ac infrastructure. The thesis has covered several aspects, ranging from control to cell design, in five directions which are summarized hereafter.

The control methods give access to different levels of performance for the same converter design. The rigorous benchmarking of these methods provided in **Chap. 4** should support their selection in further applications. It is undeniable that the circulating current control is mandatory, since it provides a way to get control over the low order harmonics at the terminal. Estimation or filter methods feature good steady-state performances, as the harmonic content of the summed capacitor voltage ripples is properly reconstructed. However, their performance during transients is sensitive to filter design and this raises the question of their robustness against fast operation point changes. Limitations of the dynamics might not be acceptable for medium voltage applications. Finally, the closed-loop control method offers the best performances and transient response, thanks to the horizontal and vertical balancing controls, at the expense of a higher communication bandwidth requirement. A trade-off between the control algorithm complexity and achievable performances is observed.

The modulation methods were compared in **Chap. 5**. Ideally, the branch or phase-leg voltage reference provided by the control algorithm should be approximated as well as possible by the actual branch or phase-leg voltage, otherwise an additional control action is necessary for correction. The modulation can be performed at two levels: (i) the branch and (ii) the phase-leg level. The branch level modulation is easier to perform, but the resulting switching patterns seen from each converter terminal result from the combination of at least two branch switching patterns. The phase-leg level modulation is more complex, can require additional intelligence to equally distribute the switching events between the two branches from the same phase-leg and has implications on the way the circulating current control is/can be performed, but usually leads to better harmonic performance and straightforward switching patterns at the terminals. However, this approach was not selected in this thesis, since

the benefits are less visible considering the relatively high number of cells per branch for an MV application and the lack of necessity for a low cell switching frequency operation. As long as the number of cells is high enough, $N_{\text{cells}} + 1$ modulation over $2N_{\text{cells}} + 1$ modulation is favored, since it is not advisable to have a high branch current ripple, which is also partly transferred to the dc terminal and implies larger branch inductance value to mitigate the peak-to-peak current ripple. The branch balancing methods proved to be very important in order to close the gap with the modulation method's harmonic performance in the ideal case. This was supported by the voltage error reduction that was achieved by substituting the number of inserted cells per branch with the average branch voltage.

The prospect to integrate the branch inductors inside a unique magnetic structure was the motivation for the work around the LFT integration within the MMC branches in **Chap. 6**. After a brief overview of the structures proposed in the literature, the need for a three-windings transformer was derived. From there, two sibling converter structures, the iGIMC and sGIMC, were derived and modeled. No difference was found with the classical dc/3-ac MMC, whose modeling was carried out in **Chap. 3**. Following the design of the magnetic components in **Chap. 7**, it was found that the integration of the branch inductors inside a three-windings transformer, i.e. the GIMC proposal, offers limited volume and efficiency improvements, at least for the ratings of the prototype converter. These gains would have to be more closely assessed, whether they're worth and sufficient from an industrial perspective. For instance, the leakage inductance for the GIMC transformer with stacked primary windings was easily reaching high values, meaning that such an integrated magnetic structure might provide higher benefits for designs that require a larger branch inductance value.

The estimation of the cell losses of a modular converter is relevant in its design phase and supports the semiconductor device selection. Unlike conventional converter topologies, the existence of a circulating current, whose harmonic content can be shaped/altered by control means, requires to perform the loss estimation in closed-loop. Since detailed time-domain simulations are time consuming, especially in the case losses at several operating points have to be evaluated, it was proposed in **Chap. 8** to use a semi-numerical methods that achieves a two order of magnitude improvement for the procurement of the cell losses. The obtained estimation is valid as long as the omission of the branch current ripple and capacitor voltage spread remain acceptable assumptions. The method is versatile, in the sense that variations in the harmonic content of the CM voltage as well as the circulating current are handled by the mathematical model, while cell type variations are handled by the VSM model that reconstructs the waveforms seen by the semiconductors devices and cell capacitor. It was found by comparison with detailed switched model simulations that the relative error is below 2 %, i.e. within the design margin.

At last, the construction of a realistically sized converter prototype in the MV range was presented in **Chap. 9**. This is not an easy task, that necessitates various competencies, from mechanics to embedded systems, and turns out to be time and resource consuming, but undeniably a great learning and engineering experience, where ingenuity is only bounded by the available time. The MMC cell design has been entirely presented. Unlike some cells from small-scale prototypes, the designed cell comprises all the bypass and detection circuits dedicated to its protection, in case of over-currents and -voltages. The Flyback-based ACPS from the dc-link supplies the low voltage electronics of the cell, is simple, reliable and cost effective for a prototype with a large number of cells. The phase-leg layout followed the standard IEC 61800-5, whose compliance was verified by a set of ac dielectric withstand test in the high voltage test equipment of the lab.

10.2 Overall conclusions

MMCs are making their way through the power electronics landscape, as seen in **Chap. 2**. Derived from designs for HVdc transmission, where they were first commercialized, more and more applications in the MV range are emerging, aiming at larger voltage levels than the conventional multilevel converters that were introduced over the last 35+ years. With a greater integration, e.g., by merging the branch inductors and the output transformer, improvements visible at the system level in terms of power density are possible. As such, the two GIMC variants address different voltage ratio configurations: the sGIMC is particularly suited for a step down conversion from a higher voltage dc link to a lower ac link, while the iGIMC is better suited for a step up conversion from a lower voltage dc link to a higher voltage ac link.

The relevance of MVdc grids is supported by the recent offering of such platforms by the industry, e.g., Siemens MVDC Plus [61] in October 2017, highlighting a technology readiness.

10.3 Future works

Future works, attractive from the point of view of the author, are briefly described in the following non-exhaustive list.

10.3.1 MVdc grid and components

Many components, such as the dc breaker in case the converter topology itself is not fault tolerant, and converter topologies, for interconnecting different dc voltage level, are required for MVdc grids to be a viable addition to the existing distribution system. A special focus should be put on a search of coherent and reasonable solutions, meaning that efficiency, feasibility, but also features (control features, behavior) shall remain at the center of concerns.

There is also an underlying need for some agreements in terms of voltage level standards, in order to prevent MVdc grids to become closed and proprietary grids, tightly bound to a unique system provider and incompatible with each others. In other words, to avoid the mistakes from the railroad electrification, initiated without coordination more than one century ago.

10.3.2 Impedance modeling

The shift towards power systems with a high penetration of power electronics interfaces require that each additional element is *compatible* with the existing infrastructure, without compromising its stability. A good example is the railway supply grid, where such a high penetration started in the 1990s. On April 9th, 1995, resonances between locomotives in the S-Bahn Zürich triggered their protective equipments. In the press, the event was reported as *mysterious*. Such unavailability of services is not desired, and very conservative compliance rules, in the form of spectral signature requirements for the traction converters, had to be put in place in order not to compromise the stability of the railway supply grid. Similar requirements will very likely spread to other applications, hence a better understanding of the ways to shape the impedance signature of a converter and also

the impact of the control method selection are seen as valuable future research. Most of the analytical results are obtained by (simplified) average model, so that the effect of the modulation methods, especially the non PWM ones, might impair the theoretical findings. In [154], for example, the dc-side impedance curves were obtained with average model simulations.

10.3.3 Modulation

In MMCs, the switching patterns seen from the terminals is a combination of the switching patterns of at least two branches. Few papers have discussed the phase-leg modulations. However, a non negligible improvement potential is seen over there, especially considering that such modulation methods are supporting a reduction of the average cell switching frequency. In terms of semiconductor losses and for a given cell design (blocking voltage and current capability), only the switching losses, through an average cell switching frequency reduction, can provide efficiency increases. By nature, such modulation methods are centralized. For converter designs with a low number of cells per branch, as the ones in the MV ranges, centralized phase-leg modulations are pertinent.

Appendices

A
Flyback ACPS electrical design

For the sake of simplicity, the following developments consider only one secondary. All the results presented in this section can be extended to the case with six (or more) outputs.

A.1 Duty cycle and primary inductance

The maximum duty cycle, $D_{\max} = 0.5$ is set by the PWM controller, which operates in discontinuous conduction mode (DCM). This condition, combined with the minimum cell voltage, gives the turns ratio between the primary and the secondary winding. For the calculation, the protection winding was taken, but the same holds for any other winding:

$$D_{\max} = \frac{V_{\text{prot}} N_p}{V_{\text{prot}} N_p + V_{\text{cell,min}} N_{s,\text{prot}}} = 0.5 \longrightarrow \frac{N_p}{N_{s,\text{prot}}} = \frac{5}{2} \tag{A.1}$$

The condition on the turns ratio and maximum cell voltage gives the minimum duty cycle:

$$D_{\min} = \frac{V_{\text{prot}} N_p}{V_{\text{prot}} N_p + V_{\text{cell,max}} N_{s,\text{prot}}} = \frac{2}{11} \simeq 0.182 \tag{A.2}$$

Additionally, the nominal duty cycle is estimated to $D_{\text{mean}} = 0.242$, which is relevant for evaluating the magnetic field density norm and eventual saturation level in the transformer core. The primary inductance to be matched is defined in (A.3). This value is relevant for the choice of the semiconductor's current rating.

$$L_p = \frac{V_{\text{cell,min}}^2}{D_{\max}^2} 2 P_{\text{in}} f_{\text{sw}} \tag{A.3}$$

The obtained primary inductance is $L_p = 12.5\,\text{mH}$ with $f_{\text{sw}} = 20\,\text{kHz}$, which was found by trade-off between the efficiency, power density and high voltage MOSFET switching losses.

A.2 Semiconductor device sizing

The semiconductor device selected for this application is an N-chanel enhancement mode MOSFET. The drain to source voltage reflected from the secondary to the primary winding that the MOSFET has to withstand is [155]:

$$V_{\text{DS}} = 1.3 \left(V_{\text{cell,max}} + V_L \right) + \left(\frac{N_p}{N_s} \right) \left(V_{\text{out}} + V_D \right) \tag{A.4}$$

The worst case scenario is at $V_{\text{cell,max}}$ input voltage and the highest reflection voltage comes from the +5 V output. V_L is the voltage spike due to the leakage inductance and is estimated at 30 % of the input voltage. From (A.4), the maximum voltage that the MOSFET has to withstand is 1.41 kV. The current rating of the switch is:

$$I_{\text{DS,pk}} = \frac{V_{\text{cell,min}} D_{\text{max}}}{L_p f_{\text{sw}}} = 0.4\,\text{A} \tag{A.5}$$

The selected semiconductor device is the 1.5 kV/2 A 2SK4177 MOSFET from ON Semiconductor. The 2SK4177 comes in a TO-263-2L package, which perfectly conforms to the space constraints.

A.3 MOSFET driving

The selected MOSFET has a gate capacitance $Q_{\text{g(on)}} = 39\,\text{nC}$. The peak gate current is limited by an additional gate resistor, so that it remains below one third of the maximum current that the PWM controller can output ($I_{g,\text{max}} = 1\,\text{A}$). Taking into account the 10 Ω impedance to rail of the controller, a safe choice is around 35 Ω. For the discharge, the sink to ground can take much higher current, so a small 15 Ω is put in series with a Schottky diode on the return path, all in parallel with 35 Ω resistor.

A.4 Snubber circuit

In order to protect the MOSFET from voltage spikes, which occur due to the leakage inductance of the transformer, a RCD snubber circuit is used. The snubber resistor R_{sn} and capacitor C_{sn} values are obtained from (A.6a) and (A.6b) according to [156]. The snubber voltage V_{sn} is taken as 2 – 2.5 times of the reflected output voltage $V_{\text{ro}} = 240\,\text{V}$ (slightly higher than $(N_{\text{pri}}/N_{+5\,\text{V}})V_{+5\,\text{V}}$ due to the leakage inductance. The leakage inductance is considered to be 3 % of the magnetizing inductance, i.e. $L_\sigma = 375\,\mu\text{H}$. The snubber voltage ripple ΔV_{sn} should not be greater than 10 – 15 %.

$$\frac{V_{\text{sn}}^2}{R_{\text{sn}}} = \frac{1}{2} f_{\text{sw}} L_\sigma I_{\text{DS,pk}}^2 \frac{V_{\text{sn}}}{V_{\text{sn}} - V_{\text{ro}}}$$

$$\Delta V_{\text{sn}} = \frac{V_{\text{sn}}}{C_{\text{sn}} R_{\text{sn}} f_{\text{sw}}}$$

$$R_{\text{sn}} = \frac{V_{\text{sn}}^2}{\frac{1}{2} f_{\text{sw}} L_\sigma I_{\text{DS,pk}}^2 \frac{V_{\text{sn}}}{V_{\text{sn}} - V_{\text{ro}}}} \tag{A.6a}$$

$$C_{\text{sn}} = \frac{V_{\text{sn}}}{R_{\text{sn}} \Delta V_{\text{sn}} f_{\text{sw}}} \tag{A.6b}$$

As a result, the values of the snubber resistor and capacitor are 192 kΩ and 2.7 nF. The snubber diode is BYG10Y, with $V_{\text{RRM}} = 1.6\,\text{kV}$.

A.5 Start-up circuit

A bias circuit powers the PWM controller from the dc-link until the +15 V output gets activated (the turn-on threshold for the PWM controller is 14.5 V, while the turn-off threshold is 9.5 V). The bias circuit is sized so that V_{DD} rises in 1 s. The resistor and capacitor R_{in} and are obtained with (A.7).

$$V_{\mathrm{DD}} = V_{\mathrm{cell,min}} \left(1 - e^{-\frac{t}{R_{\mathrm{in}} C_{\mathrm{in}}}} \right) \tag{A.7}$$

It follows that $R_{\mathrm{in}} = 1.4\,\mathrm{M\Omega}$ and $C_{\mathrm{in}} = 1\,\mu\mathrm{F}$. A 18 V Zener diode prevents V_{DD} from exceeding the controller limit.

A.6 Output filtering and rectification diodes

Since $V_{+5\mathrm{V}}$ is supplying the cell controller, the voltage ripple on this output must be lower than specified by the cell controller. For this reason, a maximum of 1 % $\Delta V_{\mathrm{pk,pk}}$ is allowed, i.e. 50 mV. According to [157]:

$$C_{\mathrm{out,min,+5\,V}} = \frac{I_{\mathrm{out,max,+5\,V}}(1 - D_{\mathrm{min}})}{f_{\mathrm{sw}} \Delta V_{\mathrm{pk,pk}}} \tag{A.8}$$

This leads to $C_{\mathrm{out,min,+5V}} = 0.6\,\mathrm{mF}$. The actual filter capacitance is increased to 3 mF for safety margin.

For the +15 V output, no large capacitance is needed, since the power consumption is low. $C_{\mathrm{out,+15\,V}}$ is set to 11 µF.

The current flowing through the GD outputs is approximately 100 mA and the maximum ripple allowed is $\Delta V_{\mathrm{pk,pk}} = 100\,\mathrm{mV}$. For the GD outputs, the minimum capacitance is $C_{\mathrm{out,min,GD}} = 43\,\mu\mathrm{F}$. The actual filter capacitance is increased to 100 µF for safety margin.

The protection output is not requiring any filtering, since a larger energy buffer (required to activate the permanent bypass in case of supply loss) is present on the receiver end.

The output rectifier diodes used are MURS340 for the $V_{+5\,\mathrm{V}}$ output and MURS160 for all the other outputs. The reason for this choice is the current rating of MURS340 and MURS160 of 1 A and 3 A, respectively. These ratings are high enough compared to the output current flowing through them, which is in range of 67 – 800 mA, according to **Tab. 9.1**.

A.7 MMC cell controller

The local cell controller handles the communication with the upper layer control (through Rx/Tx signals), performs the PWM modulation for generating the IGBT gate signals, monitors the cell state and eventually issue a bypass command in case of fault. It is supplied by the +5V output, which has to be tightly regulated. This output is chosen as the controlled output, while the other outputs are cross-regulated. As the input voltage and load vary over a wide range, an IC performing a current mode control is chosen. The dual control loop is the following: a fast inner control loop acts on the

switch current (feedback of the primary current with a sensing resistor) and a slower outer control loop acts on the voltage (feedback of the +5 V controlled output voltage with a resistive divider). Since both the input and +5 V output share the same ground, there is no need for an isolated feedback of the controlled voltage.

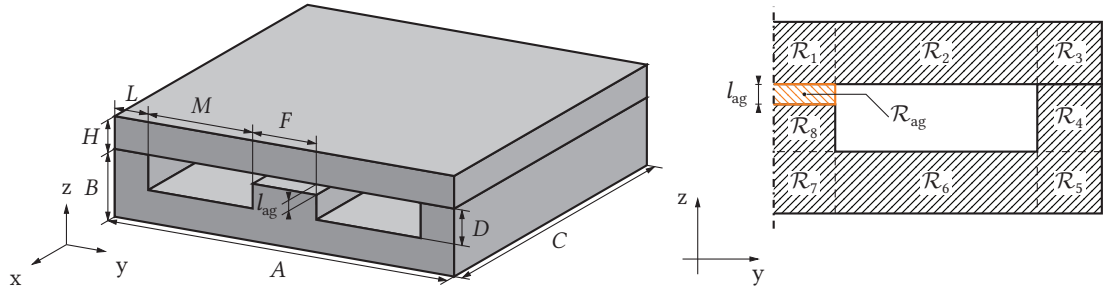
B

Flyback ACPS planar transformer design

The transformer to be designed comprises seven windings in total (cf. ***Fig. 9.6****). The use of PCB integrated windings allows for very compact transformer design, which means cores with small window heights are well suited. Moreover, all units will have almost identical electrical parameters. The design presented in this paper has considered the following manufacturing minimum requirements: (i) track width of* 200 µm *and (ii)* 200 µm *track spacing if the tracks belong to the same net (i.e. winding). The main impact of those constraints results in the maximum achievable number of turns per layer, or in the minimum number of layers per winding.*

B.1 Reluctance model

A combination of a ferrite planar E-core and its matching I-core is selected in order to obtain a design with a reasonable window height utilization. An air-gap is considered on the center limb, where the majority of the magnetic energy is stored during the power transfer from the primary to the secondaries. The PCB containing the windings is placed at the bottom of the window area (the furthest from the air-gap) in order to minimize the winding losses [158]. The core geometry and its parametrization are presented in **Fig. B.1(a)**.



(a) (b)

Fig. B.1 Ferrite core: (a) geometry parametrization and (b) magnetic circuit partitioned into reluctances. For symmetry reasons, only its half is represented.

The detailed expressions for each reluctance according to the partitioning in **Fig. B.1(b)** are given in (B.1). The core reluctance expressions follow [159].

$$\mathcal{R}_1 = \frac{\frac{\pi}{8}(H + F/2)}{\mu_0 \mu_r (I_{p,\max}) C (H + F/2)/2} \tag{B.1a}$$

$$\mathcal{R}_2 = \frac{M}{\mu_0\mu_r(I_{p,\max})CL} \tag{B.1b}$$

$$\mathcal{R}_3 = \frac{\frac{\pi}{8}(H+L)}{\mu_0\mu_r(I_{p,\max})C(H+L)/2} \tag{B.1c}$$

$$\mathcal{R}_4 = \frac{D}{\mu_0\mu_r(I_{p,\max})CL} \tag{B.1d}$$

$$\mathcal{R}_5 = \frac{\frac{\pi}{8}((B-D)+L)}{\mu_0\mu_r(I_{p,\max})C((B-D)+L)/2} \tag{B.1e}$$

$$\mathcal{R}_6 = \frac{M}{\mu_0\mu_r(I_{p,\max})C(B-D)} \tag{B.1f}$$

$$\mathcal{R}_7 = \frac{\frac{\pi}{8}((B-D)+F/2)}{\mu_0\mu_r(I_{p,\max})C((B-D)+F/2)/2} \tag{B.1g}$$

$$\mathcal{R}_8 = \frac{D-l_{\text{ag}}}{\mu_0\mu_r(I_{p,\max})C(F/2)} \tag{B.1h}$$

$$2\mathcal{R}_{\text{core}} = \sum_{i=1}^{8}\mathcal{R}_i \tag{B.1i}$$

The air-gap reluctance $\mathcal{R}_{\text{ag}}$ accounts for the fringing flux (the effective air-gap is larger than the core's cross-section at the air-gap) as presented in [160]. The original concept for accounting for the fringing flux in gapped inductors was presented in 2D in [161]. Starting from a basic air-gap geometry illustrated in **Fig. B.2(a)**, it's equivalent reluctance is calculated using the Schwarz-Christoffel transformation, resulting in:

$$\mathcal{R}_{\text{basic}} = \frac{1}{\mu_0\left[\frac{w/2}{l}+\frac{2}{\pi}\left(1+\ln\frac{\pi h}{4l}\right)\right]} \tag{B.2}$$

From there, more complex air-gap geometries can be obtained by an arrangement of basic air-gap geometries. In [160], an extension to pseudo 3D is made by combining the modified reluctances in two orthogonal planes whose intersection is parallel to the air-gap flux.

The combination of basic reluctances results into the following reluctance expressions on zy (cf. **Fig. B.2(b)**) and zx planes (cf. **Fig. B.2(c)**):

$$\mathcal{R}'_{\text{zy}} = \frac{1}{\mu_0\left[\frac{F/2}{l_{\text{ag}}}+\frac{2}{\pi}\left(1+\ln\frac{\pi(D-l_{\text{ag}})}{4l_{\text{ag}}}\right)\right]} \tag{B.3a}$$

$$\mathcal{R}'_{\text{basic,down}} = \frac{1}{\mu_0\left[\frac{C/2}{l_{\text{ag}}/2}+\frac{2}{\pi}\left(1+\ln\frac{\pi(B-l_{\text{ag}}/2)}{2l_{\text{ag}}}\right)\right]} \quad \mathcal{R}'_{\text{basic,up}} = \frac{1}{\mu_0\left[\frac{C/2}{l_{\text{ag}}/2}+\frac{2}{\pi}\left(1+\ln\frac{\pi H}{2l_{\text{ag}}}\right)\right]}$$

$$\mathcal{R}'_{\text{zx}} = \frac{\mathcal{R}'_{\text{basic,up}}+\mathcal{R}'_{\text{basic,down}}}{2} \tag{B.3b}$$

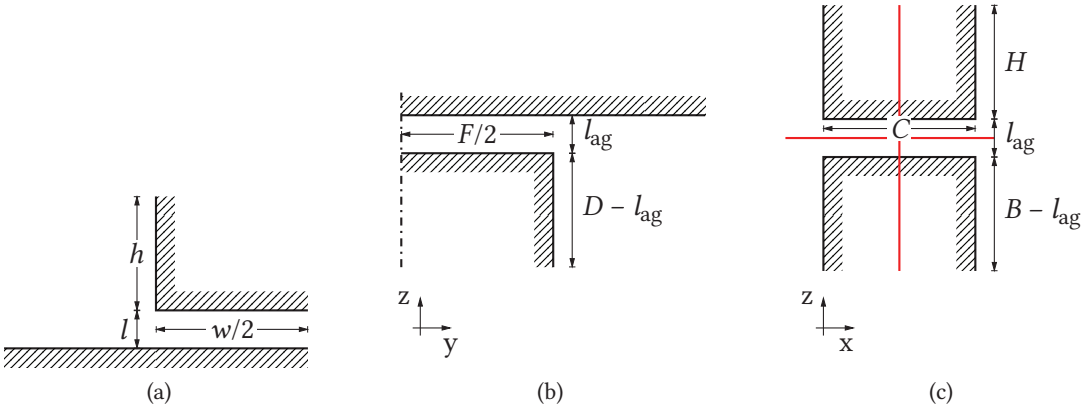


Fig. B.2 Air-gap 2D modeling: (a) basic air-gap geometry with an half-infinite plane, on which the Schwarz-Christoffel transformation is applied, (b) air-gap seen from the zy plane, which directly corresponds to $\mathcal{R}_{basic}$ and (b) the zx plane, where four $\mathcal{R}_{basic}$ are combined according to the red separations.

Finally, the air-gap reluctance with fringing flux is given by:

$$\mathcal{R}_{ag} = \sigma_{zy}\sigma_{zx}\frac{l_{ag}}{\mu_0 C(F/2)} \tag{B.4}$$

where

$$\sigma_{zy} = \frac{\mathcal{R}'_{zy}}{\frac{l_{ag}}{\mu_0(F/2)}} \quad \text{and} \quad \sigma_{zx} = \frac{\mathcal{R}'_{zx}}{\frac{l_{ag}}{\mu_0 C}} \tag{B.5}$$

The total circuit reluctance is given as a function of the air-gap length:

$$\mathcal{R}_{tot}(l_{ag}) = \frac{1}{2}\left(2\mathcal{R}_{core} + \mathcal{R}_{ag}\right) \tag{B.6}$$

Tab. B.1 Planar transformer design inputs.

L_p	$V_{cell,max}$	D_{min}	k_{sat}	f_{sw}	$S_{Cu,min}$
12.5 mH	900 V	0.182	0.725	20 kHz	35 × 200 µm

B.2 Design algorithm

The design specifications are summarized in **Tab. B.1**. The first element to be evaluated is the minimum allowable number of turns on the primary winding so that the maximum flux density in the core remains way below saturation ($B_{max} = k_{sat}B_{sat} < B_{sat}$). Note that k_{sat} can be relatively high without affecting the performance of the converter at nominal cell voltage, since both the peak primary current and the duty cycle (close to D_{mean}) are decreasing.

$$B_{max} = \frac{\phi_1}{2A_8} = \frac{L_p I_{p,max}}{N_p 2A_8} = \frac{V_{cell,max} D_{min} T_{sw}}{N_p 2A_8}$$

$$\rightarrow N_{p,\min} = \text{ceil}\left(\frac{V_{\text{cell,max}} D_{\min} T_{\text{sw}}}{2A_8 B_{\max}}\right) \tag{B.7}$$

where $2A_8 = FC$ is the core center limb's cross-section, L_p the desired primary side main inductance, $I_{p,\max}$ the maximum peak primary current, N_p the turns number of the primary winding, $V_{\text{cell,max}}$ the maximum cell voltage, $D_{\min}$ the minimum switch duty cycle (corresponding to $V_{\text{cell,max}}$) and $T_{\text{sw}} = 1/f_{\text{sw}}$. The primary inductance value is matched by adjusting the air-gap length:

$$L_p = \frac{N_p^2}{\mathcal{R}_{\text{tot}}(l_{\text{ag}})} \tag{B.8}$$

Notably, for costs reasons, the number of turns (i.e. indirectly the number of layers in the PCB) should be kept at a minimum. This means the smaller core sizes (e.g. 1804), for which $N_{p,\min}$ will be inevitably large in order to prevent the core's saturation, are discarded. On the other hand, large core sizes (e.g. 6450) require low $N_{p,\min}$, but are discarded due to space constraint.

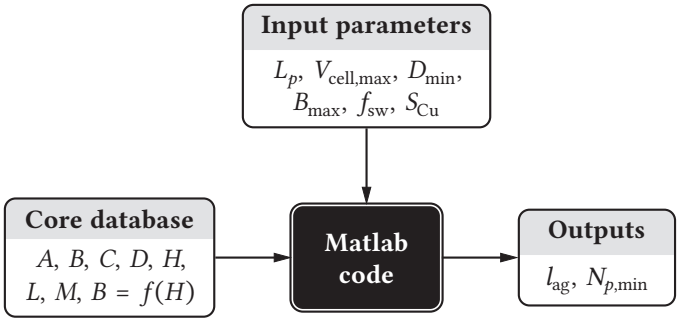


Fig. B.3 Planar transformer design tool.

A transformer design tool encompassing the above discussed design steps is built (cf. **Fig. B.3**). The core database comprises the core's geometry parameters as well as the material's *BH* curve, from which the relative permeability is derived. The input parameters are specific to the desired design.

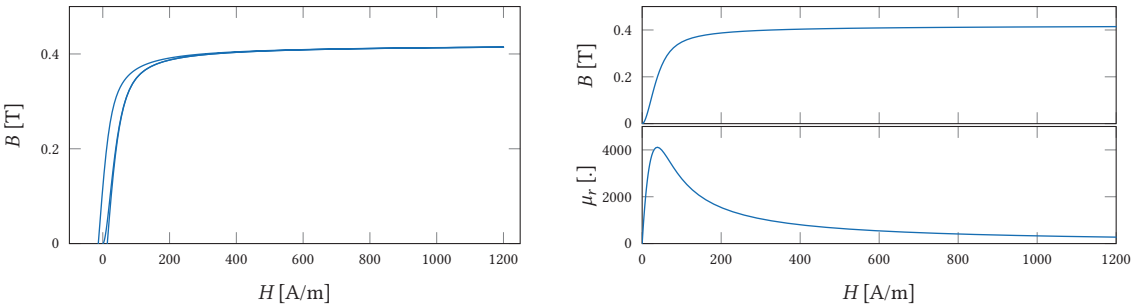
B.3 Design results

The core database is built with planar EI cores from Cosmo Ferrites [162]. The selected ferrite material is CF297, whose *BH* curve is shown in **Fig. B.4(a)**. The choice was based on the material availability from the supplier. The fitted Jiles-Atherton [163] parameters are indicated in **Tab. B.2**. Its *BH* and corresponding relative permeability curves are shown in **Fig. B.4(b)**. The design results are shown in **Fig. B.5**. For the selected design, the inductance contribution from the core and the air-gap are given by:

$$L_{p,\text{core}} = \frac{N_p^2 \mathcal{R}_{\text{core}}}{\mathcal{R}_{\text{tot}}^2} = 565\,\mu\text{H}$$

$$L_{p,\text{ag}} = \frac{N_p^2 \mathcal{R}_{\text{ag}}}{\mathcal{R}_{\text{tot}}^2} = 11.9\,\text{mH}$$

meaning that the influence of the peak primary current on the primary inductance value is negligible, as the magnetic energy is to the great extent stored in the air-gap.



(a) (b)

Fig. B.4 CF297 magnetic material: (a) *BH* curve and (b) magnetization and derived relative permeability curves, at 25°C.

Tab. B.2 Jiles-Atherton fitted parameters for CF297 ferrite material.

M_s	k	a	c	α
332327	14.47	13.55	$6 \cdot 10^{-6}$	$5.83 \cdot 10^{-9}$

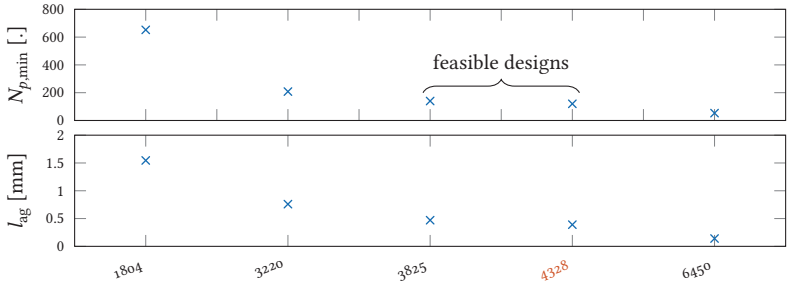


Fig. B.5 Design algorithm results for a range of planar EI cores. The selected core combination (4328) is indicated in red. $N_{p,\min} = 120$ and $l_{ag} = 390\,\mu m$.

Tab. B.3 Turns numbers for the selected design.

Primary	**Protection**	**+5 V winding**	**+15 V winding**	**GD**
120	48	3	9	9

The turns numbers for the other windings are given by:

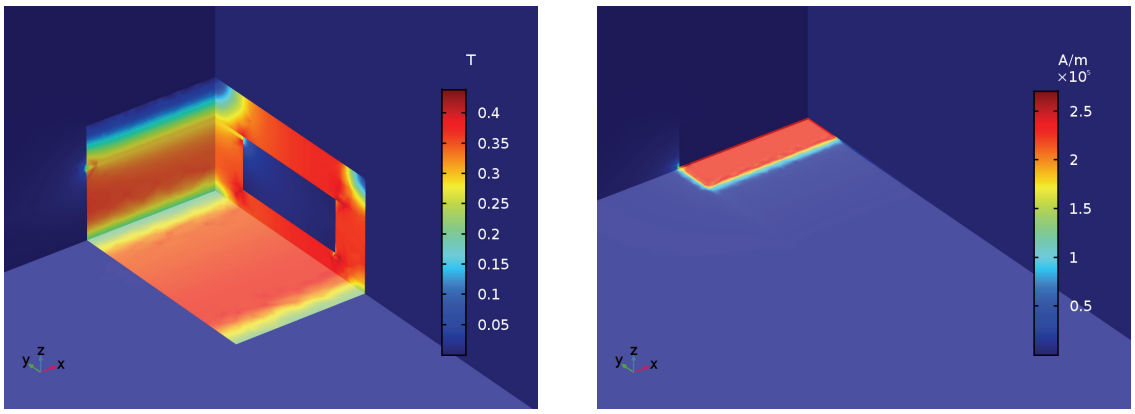
$$\frac{x}{N_{s,x}} = \frac{80\,\mathrm{V}}{N_{s,80}} \tag{B.9}$$

where $x = \{V_{+5\,\mathrm{V}},\ V_{+15\,\mathrm{V}}\}$. Finally, the turns numbers are summarized in **Tab. B.3**.

B.4 FEM

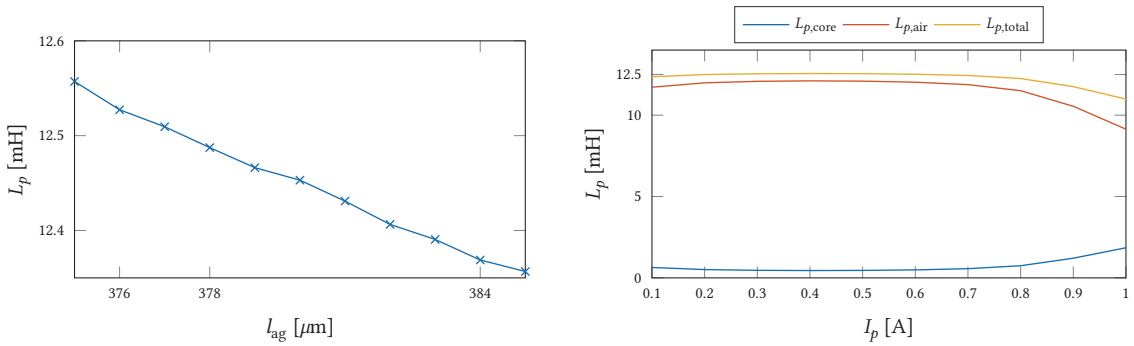
In order to accurately capture the fringing effect, a 3D FEM model is built in Comsol Multiphysics® in order to verify the magnetic characteristics of the design. Even though 3D simulations come with

a large computation overhead compared to 2D ones, they're necessary to avoid ~ 4.5 % difference in the air-gap length (observed for the selected design) in case only the fringing flux in zy plane is accounted for. The primary windings are lumped in one single conductor whose dimensions are the ones of the PCB where the windings have been integrated. The air-gap length is set to the designed value. For the first FEM simulation, the coil excitation is set to the maximum primary peak current (during the start-up with $D = 0.5$). The result is shown in **Fig. B.6**. The obtained inductance value matches the analytical model with a relative error $\varepsilon = -2\,\%$. In a second FEM simulation, the air-gap length is swept from 375 to 385 µm with the maximum peak primary current (cf. **Fig. B.7(a)**). it is found that $l_{ag} = 377.5\,\mu m$ reaches exactly the target L_p. For the third FEM simulation, the primary peak current is swept from 0.1 to 1 A with 0.1 A step in order to observe the variation of the primary inductance with respect to the cell voltage variation. As the magnetic energy is mainly stored in the air-gap, the variation of the primary inductance value is barely existent (cf. **Fig. B.7(b)**).



(a) (b)

Fig. B.6 3D FEM fields: (a) magnetic field density (in [T]) with three orthogonal cut planes in the middle of the ferrite core (center at coordinate $(C/2, A/2, (B-D)/2)$) and (b) magnetic field norm (in [A/m]) for $I_{pri} = 0.8$ A with three orthogonal cut planes in the middle of the air-gap (center at coordinate $(C/2, A/2, B - l_{ag}/2)$). By integration of the magnetic energy, $L_{p,core} = 750\,\mu H$ and $L_{p,air} = 11.5$ mH, resulting in $L_p = 12.25$ mH.



(a) (b)

Fig. B.7 3D FEM primary inductance variation: (a) over a sweep of the air-gap length from 375 to 385 µm with a primary current of 0.8 A and (b) over a sweep of the peak primary current from 0.1 to 1 A with 0.1 A step.

B.5 Planar transformer layout

The planar transformer layout is designed in Altium Designer®. The windings are drawn thanks to the user script PlanarTXv0.7 tool. The tracks are spread across 12 layers.

The need for HV isolation between winding sets results in creepage / clearance distances that have to be met in the PCB. The standard UL840 [148] is followed, considering a pollution degree 2 and an overvoltage category II. It is allowed to interpolate the values from the standard. While BT-epoxy laminates (like G200 from Isola Group [164]) offer superior dielectric properties, they're generally not stocked by PCB manufacturers and can't be requested for low order quantities. The laminate belongs to the material group IIIa (high CTI). The minimum creepage and clearance distances are presented in **Tab. B.4**.

Tab. B.4 Minimum distances between two sets of windings: (a) creepage and (b) clearance. The distances are in [mm] for 900 V maximum operation voltage.

(a)

Set	pri	+5/15 V	prot	GD1	GD2	GD3	GD4
pri	0	9	9	9	9	9	9
+5/15 V		0	9	9	0	9	0
prot			0	9	9	9	9
GD1				0	9	9	9
GD2					0	9	0
GD3						0	9
GD4							0

(b)

Set	pri	+5/15 V	prot	GD1	GD2	GD3	GD4
pri	0	2.625	2.625	2.625	2.625	2.625	2.625
+5/15 V		0	2.625	2.625	0	2.625	0
prot			0	2.625	2.625	2.625	2.625
GD1				0	2.625	2.625	2.625
GD2					0	2.625	0
GD3						0	2.625
GD4							0

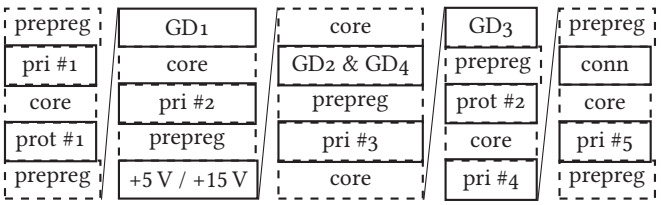


Fig. B.8 PCB layer stack with constant 200 µm fiberglass layers (either core or prepreg) between copper layers. The two prepreg layers on top and at the bottom are required to cover the vias around the center limb for layers connections, as their spacing is way too small compared to the required clearance in air.

The final PCB dimensions are 61.6 mm × 34.1 mm × 3 mm. The layer stack is shown in **Fig. B.8**, while the layers layout is shown in **Fig. B.9**. The copper layers spacing is selected according to the dielectric properties of the substrate and the minimum isolation voltage required for the design. As the primary winding is spread across 5 layers in order to comply with the manufacturing constraints regarding the minimum track width and track spacing, a full voltage isolation is required between each neighboring layer. Consequently, a 200 µm layer spacing is selected. A radiography to highlight one slice of the PCB in zx plane is shown in **Fig. B.10**.

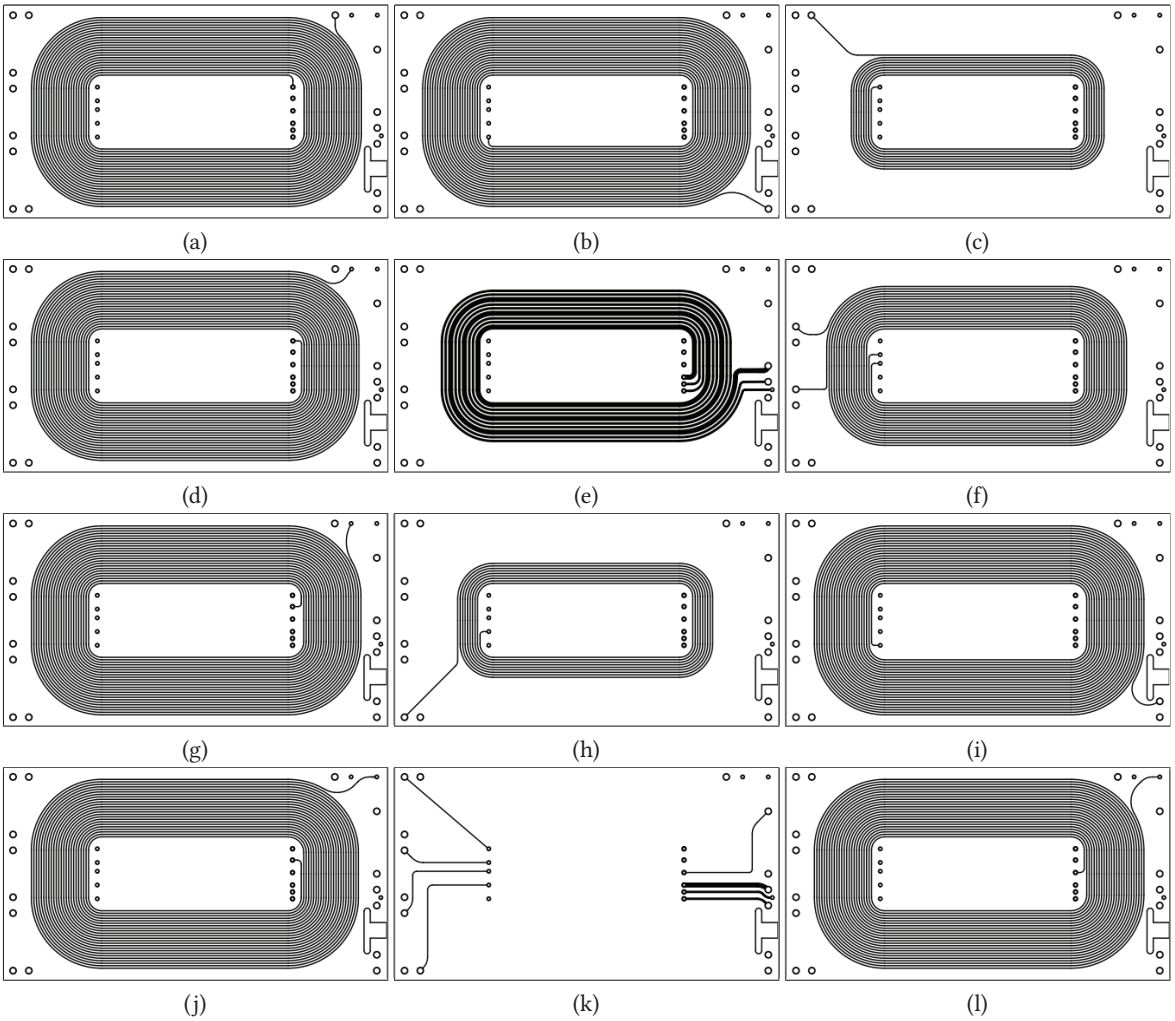


Fig. B.9 Flyback trafo PCB layers: (a) primary layer #1, (b) protection layer #1, (c) GD3, (d) primary layer #2, (e) +5 V / +15 V, (f) GD2 & GD4 (bottom switches), (g) primary layer #3, (h) GD1, (i) protection layer #2, (j) primary layer #4, (k) connections and (l) primary layer #5. The 15 transformer pins are numbered clockwise from 12 o'clock. All vias not used as electrical connections (pin #1 to #15) are blind vias, as clearances cannot be met around the central opening for the ferrite core.

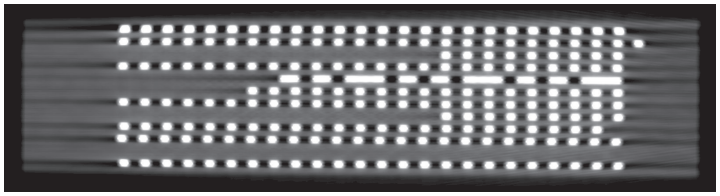


Fig. B.10 Planar transformer PCB windings cut view is in the zy plane, in the middle of the bottom horizontal section of **Fig. B.9**, obtained by a micro Computed Tomography (CT) scanner [165]. Only 11 copper layers are visible here, since the connection layer ((k) in **Fig. B.9**) has no track in the region of the cut.

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REVIEW

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