A Reconfigurable Heterogeneous Microserver Architecture for Energy-efficient Computing

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Extended Abstract

Using microserver-based system architectures for scale-out applications in cloud computing and HPC could provide a significant advantage in energy-efficiency and TCO, as they offer performance, scalability and high integration density. Specialized server architectures and GPU-based hardware accelerators are increasingly used instead of traditional, CPU-based architectures to achieve higher performance and better energy efficiency. Recently, FPGA-based acceleration is being on the rise due to novel programming models. In this work we propose a scale-out solution for high-density, heterogeneous microservers integrating a high-speed, low-latency communication infrastructure.

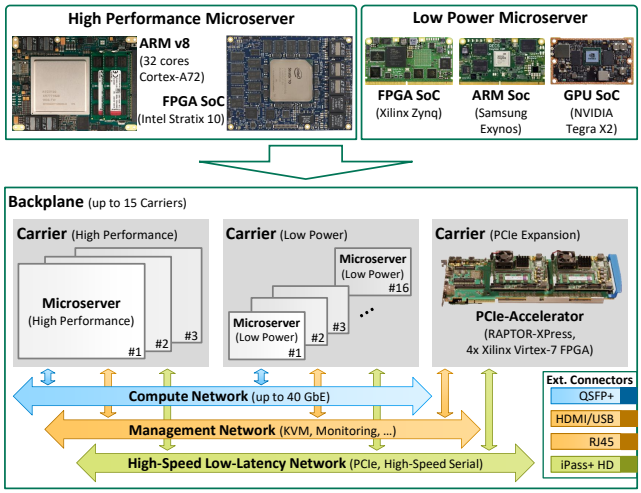

Figure 1: Heterogeneous, modular microserver architecture including GPU and FPGA acceleration

The presented next-generation modular microserver incorporates a broad spectrum of heterogeneous target architectures, making it a versatile platform for a wide range of applications. Specifically, state-of-the-art x86 processors, 64-bit ARM SoCs and server processors, FPGAs, GPUs and others can be integrated. All major processing architectures (CPU, GPU and FPGA) are available in a high-performance as well as a low-power variant. In addition, a custom PCIe-based accelerator card with up to 4 FPGAs has been integrated into our platform. These PCIe-based accelerators can be interconnected to each other to form a unique, densely coupled FPGA cluster. The server architecture permits sharing a PCIe device across multiple microservers or a dynamic assignment of PCIe devices to a dedicated microserver. In contrast to existing microserver platforms that support only homogeneous populations, the proposed modular microserver enables a seamless combination of all these technologies in a single enclosure. This allows for fine-tuning the platform towards a specific application, offering a densely coupled, highly integrated heterogeneous server architecture including a scalable, high-speed, low-latency communication infrastructure. The platform targets form factors on microserver-, baseboard-, backplane-, and chassis-level that match the requirements of today's data centers, enabling hot-swapping and hot-plugging of system components as well as easy integration into existing data center racks.[1]

One of the greatest challenges in using heterogeneous server architectures is to program the different kinds of target devices efficiently. As a common programming language, all integrated computation nodes support OpenCL. This includes our custom FPGA-platform RAPTOR-XPress, which comes with a comprehensive software environment and is fully integrated into the Xilinx® SDAccel™ design flow.

Our current work is to extend this design flow to enable communication between multiple FPGAs in a tightly coupled cluster via high-speed serial transceivers. Several benchmark applications are used to assess the performance, scalability and energy efficiency of different applications, e. g. Locality Sensitive Hashing for DNA-processing in biocomputing appliances. These algorithms will be implemented using OpenCL on every compute platform and compared with optimized implementations based on, e.g., OpenMP, VHDL and CUDA. All FPGA implementations will use the high-speed communication infrastructure of the RAPTOR-XPress and will be partitioned across multiple FPGAs.

Summary The introduced novel server architecture provides heterogeneous computation nodes for an application-driven, configurable high-speed communication infrastructure, which enables easy usage of hardware accelerators, especially multiple, tightly coupled FPGAs via OpenCL.

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Keywords

HPC, Cloud Computing, Heterogeneous Microserver, Accelerator, OpenCL, High-Speed Low Latency Communication, Energy Efficiency, Scale-Out Server

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