

## Towards flexible organic thin film transistors (OTFTs) for biosensing

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We have studied parylene-N and parylene-C for their use as substrates and gate dielectrics in OTFTs. Parylene-N films with a thickness of 300 nm show the required dielectric properties, as verified by breakthrough-voltage measurements. The surface roughness measured for 300 nm thick parylene-N films is 4–5 nm. However, initial growth of parylene depends on the subjacent surface. This results in different thicknesses on Au electrodes and substrate materials for thin films. Capping of micro-patterned Au-electrodes with a thin Al layer *via* lift-off results in homogenous parylene film thickness on the whole sample surface. OTFTs are fabricated on glass with parylene-N as a gate dielectric and pentacene as a semiconductor. The electrodes are patterned by photolithography enabling micrometer sized features. The contact resistance is extracted by variation of the channel length. Modification of the parylene dielectric layer surface by plasma treatment with oxygen after deposition allows shifting of the threshold voltage to more positive values, however at the cost of increasing hysteresis. OTFTs fabricated on thin parylene-C films can be peeled off and could result in flexible devices employing parylene-C foil as a substrate. For a foil thickness of 3–4  $\mu\text{m}$ , operational devices can be bent down to radii less than 1 mm, *e.g.* in the range of cannulas. Operation of such OTFTs with parylene-C as a gate dielectric in liquids is demonstrated. The OTFT current can be modulated by the potential in the electrolyte as well as by the bottom gate potential. This allows for application of such OTFTs as sensors in medical devices.

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### Introduction

Application of organic materials as active materials in sensors is an emerging field of research. Here, especially the possibility to choose biocompatible materials and to construct mechanical flexible devices allows us to potentially outperform the established inorganic semiconductor technology for practical applications, for example in medical applications.<sup>1</sup> The organic semiconductor pentacene is known to support the growth of neural networks, thus it can be considered biocompatible for at least several days.<sup>2</sup> Parylene, another commonly employed material in organic electronics, is FDA approved for implants. Furthermore, it offers good dielectric properties and can be deposited *via* chemical vapour deposition (CVD) at room temperature forming insulating layers for *e.g.* gate dielectrics. By careful choice of the employed materials biodegradable devices could be achieved.<sup>3</sup> The low energy cost for production is another advantage of organic materials.

A number of sensors utilising organic semiconductors have been demonstrated.<sup>4</sup> One architecture family is the organic electrochemical transistor (OECT), which can be used for enzymatic sensing<sup>5</sup> and barrier tissue evaluation.<sup>6</sup> The sensing

relies on a dedoping mechanism of the active material. Another principle is based on the classical field effect transistor.<sup>7</sup> Here, charge carrier accumulation is controlled *via* a gate field. The accumulated charge carriers are transported through the channel *via* an additional source–drain voltage, resulting in an on-state current. Detection of targets relies on the shift of the threshold voltage induced by adsorption of charged particles or by changes of the chemical potential at the transistor–sample interface. These principles have been developed for CMOS technology,<sup>8</sup> and have also been successfully applied to other materials *e.g.* diamond.<sup>9</sup> Similarly, sensors of this type based on organic semiconductors are able to detect pH,<sup>10</sup> penicillin,<sup>11</sup> biotin,<sup>12</sup> trimethylamine<sup>13</sup> and DNA.<sup>14,15</sup> In the later case, the probes were covalently bound to the organic semiconductor, highlighting the advantage of easy ways to functionalise the sensor surface.<sup>15</sup> Another interesting approach is the formation of a lipid bilayer on the sensor, which allows the incorporation of biological receptors at the sensor surface.<sup>16</sup> In the line of sensors employing organic semiconductors, we demonstrated a transducer resembling the architecture of conventional double-gate thin film transistors (DGTFTs).<sup>17</sup> To realise this experiment, it was essential to identify tetratetracontane (TTC) as a top gate dielectric.<sup>18</sup>

Our transducers are able to detect the adsorption of fatty acids onto the sensor *via* a threshold-voltage shift both in top gate as well as in bottom gate sweeps. A main drawback of our

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previous work is that it still utilises a silicon chip for the bottom gate and the bottom gate dielectric. Although tissue is soft, Si is brittle, so interfaces between biological samples and the sensor pose sources of inflammation due to mechanical stress.<sup>19</sup>

Furthermore, in setups with optical microscopes working in transmission, a transparent device is mandatory.

Here, we report our progress on the fabrication of flexible and micro-patterned OTFTs for biosensors based on pentacene as an organic semiconductor.

## Experimental results

Parylene, a widely used dielectric in organic electronics,<sup>20,21</sup> is chosen as the dielectric. It offers many advantages, such as high dielectric strength, mechanical flexibility and good optical transparency. It can be easily deposited on glass slides for transparent devices. Peeled off, parylene itself can also serve as the substrate. This results in flexible devices, which are already used for fabrication of electrode arrays for *in vivo* recordings.<sup>22</sup> It has also been shown that one can conduct photolithography on parylene, which enables the fabrication of micro-patterned electrode structures on parylene.<sup>23</sup>

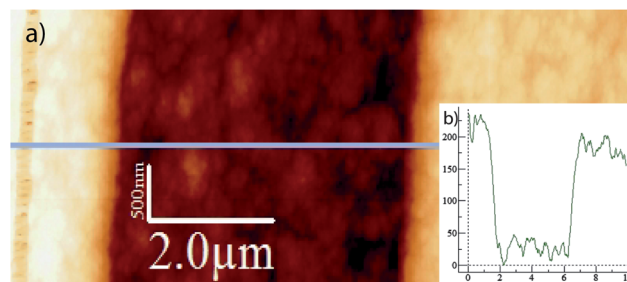
### Growth study of parylene

The gate dielectric is a critical part of the device;<sup>24</sup> here, thin films with good dielectric properties are required.<sup>25</sup> Consequently the dielectric materials, namely two variants of parylene, parylene-N and parylene-C, are studied first. Both are deposited *via* CVD at temperatures ranging from 8 °C to 15 °C.

A capacitor structure with an area of 2 mm × 2 mm and the dielectric layer in between Au electrodes was used to test for stability against breakthrough due to the applied voltages. The parylene film thickness was evaluated with a DekTak 6M. Parylene-N films of a thickness of 400 nm withstand an applied voltage of at least 60 V. Working OTFTs can be fabricated with dielectric layers from 300 nm onwards. In contrast, parylene-C films of a thickness of 600 nm withstand only 20 V or less. Thus parylene-N was chosen, since it allows for thinner dielectric layers.

A surface roughness (rms) of less than 1 nm is preferable for the preferred pentacene thin-film phase growth. Thus parylene-N and -C films are evaluated for their surface roughness using a Veeco Dimension 3100 AFM. The AFM micrographs were evaluated using the WSxM software.<sup>26</sup> For parylene-N, a surface roughness of 4–6 nm is typical for a 300 nm thick film.

Evaluation of the dielectric layer surfaces by AFM shows that the thickness of the parylene-N layer is significantly lower on the Au electrodes than on the surrounding parylene substrate (see Fig. 1). The same result is observed for different substrates like borosilicate-glass or silicon-oxide. Since the Au electrodes are higher than the surrounding substrate surface, one would expect the parylene surface to appear higher on the Au electrodes than on the substrate. This is in contrast to the measured lower height on the Au electrodes. Once 6 nm of Al is evaporated on top of a 25 nm Au electrode, patterned by photolithography, the grown parylene film is homogenous on the whole sample.



**Fig. 1** Parylene-N on Au. (a) AFM micrograph of parylene-N grown on a 4 μm Au electrode on silicon dioxide. (b) Height profile extracted from the line indicated in (a).

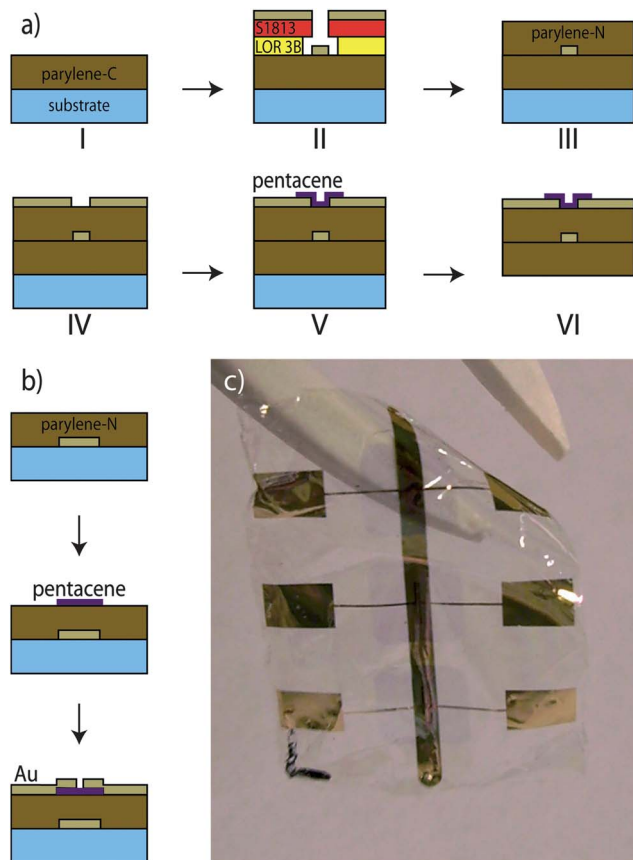
Such parylene-N films are employed as gate dielectrics for the fabrication of OTFTs.

### OTFT fabrication and characterisation

OTFTs are fabricated on thin parylene-C foils as well as on glass slides. The latter offer a smooth substrate surface, which is beneficial for AFM studies. Furthermore, some OTFTs are fabricated with electrodes defined by shadow masks and photolithography. While photolithography allows for micro-patterned electrode structures, shadow masks have restrictions in feature size and obtained structures. However, patterning by shadow masks is a solvent free process and it features faster fabrication compared to photolithography.

The substrates (glass slides) are cleaned in acetone, isopropanol and purified water in an ultrasound bath for 10 min each. For flexible device configurations, a parylene-C (Plasma-Parylene Systems GmbH) layer with a thickness of 2–4 μm is deposited onto glass substrates *via* CVD in a home-built CVD-chamber (Fig. 2a I). For the gate, 30 nm of Au and 6 nm of Al are deposited using an e-beam UHV evaporation system. The gate is patterned either by a lift-off process (II) or by evaporation through a shadow mask. For micro-patterned gates, the Al-capping ensures homogenous parylene film growth on the whole sample surface. A 3 nm Ti sticking layer is added for samples produced directly on the glass slides. Parylene-N is deposited to a thickness of 400 nm as a gate dielectric (III). For micro-patterned OTFTs, 30 nm of Au is patterned as the source and drain electrodes *via* a subsequent lift-off process (IV). This is followed by the deposition of 30 nm of pentacene (Sigma Aldrich, triple sublimed grade) (V). This results in micro-patterned, bottom contact OTFTs. Alternatively, 30 nm of pentacene is deposited first, and the source and drain electrodes (30 nm of Au) are evaporated through a shadow mask (see Fig. 2b). This way, top contact OTFTs are fabricated.

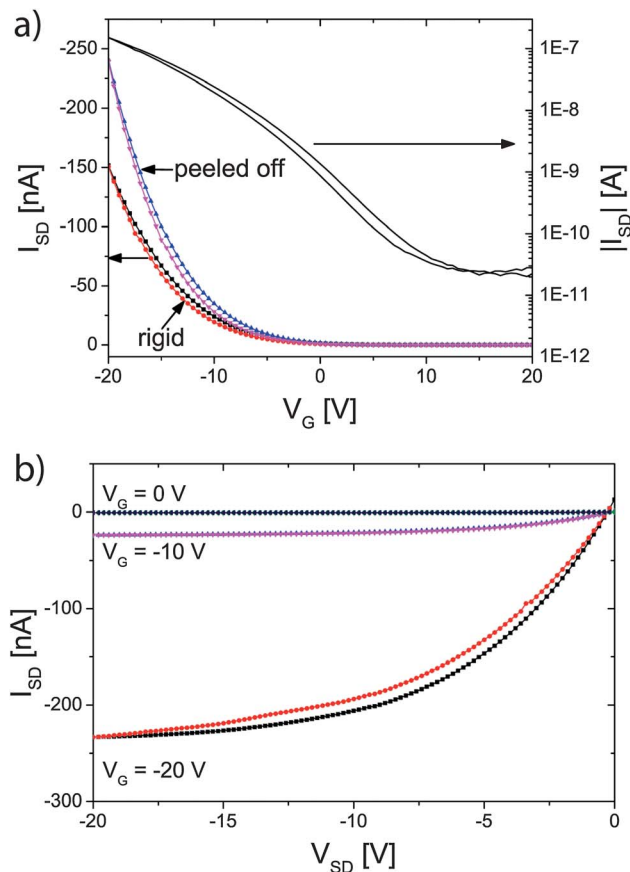
The OTFTs are measured under ambient conditions employing a Keithley 2612 Source Measure Unit. In general, they show saturation mobility on the order of 10<sup>-3</sup> cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, extracted from the slope of the square root of the current *versus* the gate voltage in the saturation regime. Since the saturation mobility is directly proportional to the current, it must be as high as possible for good signal strength. Among different devices the threshold voltage varies from 0 V to -15 V. The



**Fig. 2** Fabrication pathways. (a) Processing steps for bottom contact OTFTs with electrode structures patterned by photolithography. For the lift-off process a bilayer photoresist with LOR-3B and S1813G2 was spun onto the samples. (b) Processing steps for the production of top contact OTFTs. (c) Photograph of three top contact OTFTs fabricated on a thin parylene-C foil.

threshold voltage should be close to 0 V, because the threshold voltage has to be compensated by the voltage applied to the bottom gate in our DGTFT sensors. This was achieved in some devices. For the previously demonstrated Si-oxide based transducers, the threshold voltage was always more negative with values between  $-14$  V and  $-30$  V.<sup>17</sup> The hysteresis can be as small as 1 V ranging up to 10 V. A typical device example is given in Fig. 3. The threshold voltage can be moved towards positive threshold voltages by modifying the parylene surface with oxygen groups. We use an oxygen plasma treatment, which replaces the previously reported UV-treatment.<sup>28</sup> The samples are subjected to an oxygen plasma treatment in a LabAsh 100 at 2 torr oxygen pressure and 53 W incident power before deposition of pentacene. An increasing shift of the threshold voltage towards more positive voltages with increasing treatment times is observed. However, any plasma treatment increases the hysteresis (see Table 1).

When different channel lengths are fabricated in one step, one can extract the contact resistance. The contact resistance can limit the current through the channel resulting in a lower saturation mobility of the device. For the electrode structures, patterned by photolithography, different channel lengths at a constant channel width of 1 mm are realised. 10  $\mu\text{m}$ , 6  $\mu\text{m}$ , 4  $\mu\text{m}$



**Fig. 3** Transistor characteristics. (a) Gate sweeps of a transistor fabricated on a thin parylene-C foil. The black (squares) and red (circles) lines are the forward and backward sweeps before taking the OTFT off the rigid support, the blue and magenta ones are the corresponding sweeps of the flexible device after peeling off. The black curves belonging to the logarithmic scale give the situation before the peel off. (b) Source-drain voltage sweeps of the transistor in the rigid situation.

and 2  $\mu\text{m}$  are chosen as channel lengths. These dimensions allow for a high number of individual sensors on a small area. The resistance for the different channel lengths can be obtained from the linear slopes of the conductance in source-drain

**Table 1** Threshold voltage shift upon functionalisation of the dielectric surface by an oxygen plasma treatment (before deposition of the pentacene). The threshold voltage is extracted from the backward sweeps at a source-drain voltage of  $-20$  V and a gate voltage of up to  $-32$  V. The extracted data for two batches are shown. On parylene-N, hole mobilities of pentacene of  $0.55$   $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$  have been reported, which have been measured at higher voltages<sup>27</sup>

Treatment time [s]	Saturation mobility [ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ ]	Threshold voltage [V]	Hysteresis [V]
0	$1.3 \times 10^{-3}$	$-4.0$	7.1
3	$0.2 \times 10^{-3}$	$-1.8$	22.0
6	$1.3 \times 10^{-3}$	2.7	20.8
9	$1.6 \times 10^{-3}$	7.9	11.3
0	$8.8 \times 10^{-4}$	$-1.3$	2.6
2	$9.1 \times 10^{-4}$	9.5	17.0
4	$1.9 \times 10^{-4}$	3.7	19.3
6	$2.2 \times 10^{-4}$	7.3	22.0

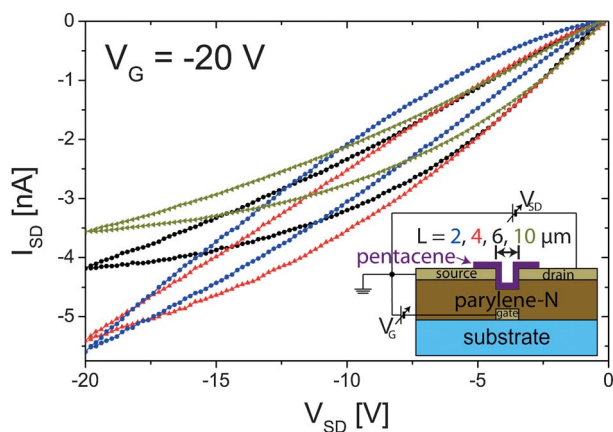
voltage sweeps. Extrapolation to zero channel length allows us to obtain the contact resistance.<sup>29</sup> This results in a contact resistance of 3 GΩ for a 1 mm wide channel. A pronounced nonlinearity at low source–drain voltages is observed (see Fig. 4).

For the flexible configuration the finished devices produced on a parylene-C film are placed in a water bath. After soaking for 1 to 3 hours, the adhesion of the parylene films is reduced and the OTFTs are peeled off (Fig. 2a VI and c).

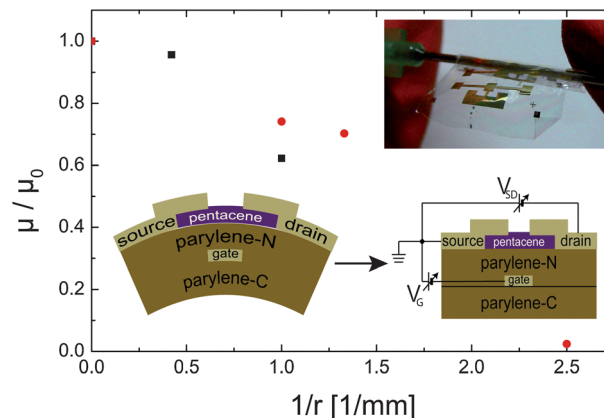
The electrical characteristics are recorded before and after they were stripped off their rigid support. All device characteristics change after the transistor is peeled off the rigid support, presumably due to the mechanical stress. Remarkably, in some cases some or all of the figures of merit are better after the transistor is peeled off. For the OTFT shown in Fig. 3, the saturation mobility increased from  $7 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  to  $1 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , when the OTFT was peeled off.

Once the devices are bent to a radius of a few mm, a decrease of the electrical properties can be observed. In terms of saturation mobility the transistors retain above 60% of their original performance for a bending radius of 1 mm. For a sample of a thickness of 3 μm, the transistor can be bent around a cannula with a radius of 800 μm, still showing transistor behaviour at a decreased performance afterwards. In contrast, if wrapped around a cannula with a radius of 400 μm, the transistor still shows an on- and off-state, but the electrical characteristics of a gate sweep deviate from the standard curve. Thus, one can expect the devices to stay operational if wrapped around a cannula with a radius of 800 μm (see Fig. 5). This would allow for the intended use in medical treatment, for example for medication triggered by transducer signals.

To demonstrate that such a device will be applicable as a biosensor, operation with the OTFT channel immersed in 10 mM PBS buffer is tested. While in initial tests the parylene-N layers have shown good dielectric properties immersed in electrolytes, the parylene-N layer is found to have an insufficient reliability in longer measurements. Thus we use parylene-C as the dielectric for the sensing devices. While the film thickness



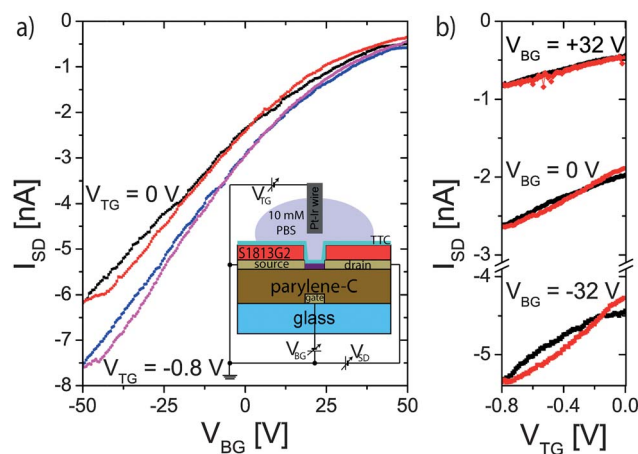
**Fig. 4** Source–drain voltage sweeps for different channel lengths. The curves are colored in blue (circles) for the 2 μm, in red (upward facing triangles) for the 4 μm, in black (squares) for the 6 μm and in yellow (sideward facing triangles) for the 10 μm long channel.



**Fig. 5** Bending of the flexible transistors. Decrease of the saturation mobility after bending the OTFT to small radii. The inset shows an OTFT wrapped around a cannula.

of the dielectric layer has to be increased with respect to parylene-N, the results of processing and OTFT performance can be transferred. A 2 μm thick parylene-C layer serves as the bottom gate dielectric. To cap the source and drain contacts, a photoresist with good dielectric properties (S1813G2) is spun onto the finished micro-patterned OTFTs and baked at 120 °C for 10 min. It is patterned using photolithography, such that only the channel region is reopened again. A layer of 50 nm of TTC is deposited on the top. This leaves the pentacene in the channel region capped with 50 nm of TTC.

A droplet of 10 mM PBS buffer (degassed) is put on the transistor and is brought into contact with a Pt–Ir wire, which is glowing out with a Bunsen burner before the measurement. Gate sweeps with both bottom and top gate are performed at different fixed potentials of the other electrode. The



**Fig. 6** Transistor operation in 10 mM PBS buffer solution. (a) Bottom gate sweeps at fixed top gate potential. For a more negative top gate potential, additional charge carriers are accumulated, resulting in an increase in the current. (b) Top gate sweeps at fixed bottom gate potential. The response of the top gate is modulated by the bottom gate. For positive bottom gate potentials, the semiconductor gets more depleted reducing the response to the top gate voltage and conversely for more negative bottom gate voltages. Thus, the sensitivity of the device can be tuned by the bottom gate.

source–drain voltage is set to  $-0.6$  V. The leakage current through the bottom gate dielectric is negligible and for the top gate dielectric, the source–drain current is corrected for the gate leakage current, as previously reported.<sup>17</sup> The transistors can be measured several hours, until finally breakdown of the top gate dielectric occurs.

The transistor current can be clearly modulated by the bottom as well as the top gate potential (see Fig. 6). The extracted transconductance from the bottom gate sweeps is  $4.0 \times 10^{-11} \text{ A V}^{-1}$ ,  $8.0 \times 10^{-11} \text{ A V}^{-1}$  and  $9.0 \times 10^{-11} \text{ A V}^{-1}$  for  $+32$  V,  $0$  V and  $-32$  V bottom gate potential, respectively. For the top gate it is  $4.5 \times 10^{-10} \text{ A V}^{-1}$ ,  $8.0 \times 10^{-10} \text{ A V}^{-1}$  and  $10.0 \times 10^{-10} \text{ A V}^{-1}$  at  $+32$  V,  $0$  V and  $-32$  V bottom gate potential, respectively. The ratio of the top gate to the bottom gate transconductance calculated from these values is *ca.* 11.

## Discussion

The disturbed growth of parylene films on the bare Au electrodes gives rise to sharp flanks at the rims of the underlying electrodes at least for thin films. This distorted growth of parylene on certain metals is described in the literature. Inhibition of parylene growth on Au seems to be dependent on the precise Au surface, since inhibition has not been reported in at least one case.<sup>30</sup> A capping of the Au electrode surface with a thin Al layer gives rise to homogenous parylene film growth on the whole sample surface for micro-patterned devices. For thin dielectric layers (300 nm), the thin Al top layer in the micro-patterned gate electrode is necessary to avoid the distorted parylene growth on the gate. For thicker layers ( $\mu\text{m}$ ), these deviations may not be relevant.

The shift of the threshold voltage to more positive values and increase of the hysteresis due to the addition of oxygen groups to the surface are established effects.<sup>28</sup> The oxygen plasma treatment instead of UV-ozone assisted reactions may further roughen the surface in comparison. Since parylene is known to degrade under UV irradiation, the plasma approach may be more gentle, since the UV degradation weakens the dielectric properties of parylene.<sup>31</sup> Both treatments can also be used as a starting step for introducing functionality to the surface.<sup>32</sup>

The contact resistance of  $3 \text{ G}\Omega$  extracted for our devices is high in comparison with values found in the literature. While contact resistance is reported to decrease with increasing gate voltages,<sup>29</sup> this may not be feasible in every application. A Schottky barrier can give rise to the observed nonlinearity in conductance at low source–drain voltages. Also trap states may give rise to such effects.<sup>33</sup> A decrease can be expected if the electrode surface is treated with a functional layer.<sup>34,35</sup>

When the transistors are peeled off, some devices improve while some degrade. This is encouraging since it indicates that a controlled peel-off process may result in devices as good as on solid support. The mechanism that changes the performance is complex and may range from loss of material up to strain induced phase transitions.<sup>36</sup>

Degradation of OTFTs at controlled bending radii is a well-known effect, which is attributed to the displacement of molecules within the thin film.<sup>37</sup> The degradation can be averted if

the organic semiconductor is placed in a neutral strain position. This reduces the strain acting on the thin film.<sup>38</sup> However, this may not be possible in sensor applications. Here, the organic semiconductor is separated from the test sample only by a thin capping layer, or it is even in direct contact with the sample.

In liquids, the OTFTs show stable performance for several cycles and the gate leakage current in the case of the bottom gate dielectric is negligible. The transconductance extracted for the sweep of the bottom and the top gate at  $+32$  V,  $0$  V and  $-32$  V differ by a factor of 11. The expected factor is given by the ratio of the capacitances of the top-gate dielectric (50 nm of TTC;  $\epsilon_r = 1.3$ ) and the bottom gate dielectric (2  $\mu\text{m}$  parylene-C;  $\epsilon_r = 2.95$ ). This ratio is calculated to  $C_{\text{TTC}}/C_{\text{parylene-C}} = 17.7$  and fits reasonably well to the extracted ratio of the top- and bottom-gate's transconductances, as deduced from the theory of DGTFTs. The modulation of the current by the top gate is the principle of our sensor mechanism.<sup>17</sup>

## Conclusions

The use of parylene as a substrate and dielectric enables the production of flexible OTFTs of just a few  $\mu\text{m}$  thickness. The electrodes can be micro-patterned by lift-off, which is a parallelisable technique that allows for high throughput processing. The materials utilized in production of the devices are all biocompatible. This is mandatory for interfacing with tissue. Especially the possibility of wrapping the OTFTs around cannulas, with the transistors staying operational, already shows possible future applications. The processes involved in the change of the device characteristics upon taking the OTFTs off the rigid support are certainly worth further attention. Operation of such devices fabricated on glass in PBS buffer solution is demonstrated. This further points to future applications of such devices as biosensors. The presented devices serve as the starting point for our ongoing work to realise flexible and optical transparent biosensors.

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