Analysis and Design of Current-fed Wireless Inductive Power Transfer Systems

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Abstract

Analysis and Design of Current-fed Wireless Inductive Power Transfer Systems

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Wireless Inductive Power Transfer (IPT) technology promises a very convenient, reliable, and safe way of transferring power wirelessly. Recent research on IPT establishes its indispensable role and suitability in electric vehicle (EV) applications. Efficient design of both converters and IPT coils are essential to make this technology feasible for mass deployment. The existing research on IPT is mainly based on power converters derived from voltage-source inverter (VSI) topologies, where feasibility of current-source inverter (CSI) has received very limited attention. Considering certain limitations of voltage-fed converters, this research is focused on the concept study and feasibility analysis of current-fed power electronics for IPT systems, where the primary application is EV charging.

CSI leads to parallel *LC* resonance in the primary side of IPT. The advantages of the parallel tank networks include lower inverter device current stress, very close to sinusoidal coil current, soft-switching of inverter devices, and natural short circuit protection during fault etc. Considering these merits, a new IPT topology is proposed in this thesis, where the inverter is full-bridge CSI and the compensations in primary and secondary sides are parallel and series types, respectively. Compared with the existing IPT topology with current-fed push-pull inverter, the proposed system does not have startup and frequency bifurcation issues. However, due to weak coupling between IPT coils, the primary side parallel capacitor experiences high voltage stress in higher power levels, and this voltage directly appears on inverter devices. To overcome this, a modified IPT topology fed from a CSI is proposed, where the primary compensation is parallel-series type and secondary compensation is series type. Detailed steady-state operation, converter design, soft-switching conditions, small-signal modelling, and closed-loop control are reported for both the topologies. To verify analytical predictions, numerical simulation is performed in PSIM 10 and experimental results obtained from a 1.6*k*W lab-built prototype are reported.

Considering the requirement of bi-directional power flow capability to support energy injection from vehicle to grid (V2G) for future smart-grid applications, a new bidirectional IPT topology with current-

fed converter is proposed. It has current-sharing feature in grid side converter and voltage doubling feature in vehicle side converter. This is the first attempt to implement bidirectional IPT with current-fed circuit and demonstrate grid to vehicle (G2V) and V2G operation. Keeping inverter output power factor lagging, ZVS turn-on of the inverter devices are always ensured irrespective of load variation. Detailed steady-state operation and converter design for both G2V and V2G modes are reported. Experimental results obtained from a 1.2*k*W lab-prototype are reported to verify the analysis and performances of bidirectional IPT circuit.

The last part of this thesis addresses the possible improvements on reducing the number of power conversion stages to achieve higher system efficiency, compact size and reduced cost. This is usually done by using direct ac-ac converter as the primary side converter of IPT. Existing single stage IPT topologies are derived from VSI topology. From source side, these topologies have buck derived structure; therefore, none of them draw high quality current from source. In this thesis a new single stage IPT topology is proposed, which has boost derived structure and thereby capable of maintaining unity power factor at source. Dynamic load demand, source current waveshaping and effective wireless power transfer are achieved with two-loop control method. Experimental results obtained from a 1.2*k*W grid-connected lab-prototype are reported to justify the suitability of this single-stage IPT topology for practical use.

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Table of Contents

List of Tables

List of Figures

List of Abbreviations

ac	Alternating Current – represents alternating quantities
CSI	Current-Source Inverter
CPT	Capacitive Power Transfer
dc	Direct Current – represents constant quantities
EMI	Electromagnetic Interference
EV	Electric Vehicle
G2V	Grid to Vehicle
IGBT	Insulated-Gate Bipolar Transistor
IPT	Inductive Power Transfer
LC	Inductor-Capacitor
LCL	Inductor-Capacitor- Inductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
PFC	Power Factor Correction (or Corrected)
P/P	Parallel/Parallel
P/S	Parallel /Series
PWM	Pulse Width Modulation
RV-IGBT	Reverse-Blocking Insulated-Gate Bipolar Transistor
RC	Receiver Coil (*same as* Secondary Coil)
RMS	Root mean square
S/P	Series/ Parallel
S/S	Series/Series
SSM	Small-Signal Model (Modelling)
UPF	Unity Power Factor
TC	Transmitter Coil (*same as* Primary Coil)
THD	Total Harmonic Distortion
V2G	Vehicle to Grid
VSI	Voltage-source Inverter
WPT	Wireless Power Transfer
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching

List of Symbols

C_2	RC side series compensation capacitor
C_o	Output dc capacitor
C_p	TC side parallel capacitor in *CLC* tank
C_s	TC side series capacitor in *CLC* tank
C_t	TC side parallel capacitor in (*L*)(*C*) tank
D	Duty cycle of inverter
f_o	Resonance frequency in Hz
i_1	TC current
i_2	RC current
i_d	Input dc current
i_o	Output current
k	Coefficient of coupling between TC and RC
L_1	Self-inductance of TC
L_2	Self-inductance of RC
L_d	Input dc inductor
L_{k1},	Leakage inductance of TC coil in transformer equivalent circuit
L_{k2}	Leakage inductance of RC coil in transformer equivalent circuit
L_m	Magnetizing inductance in transformer equivalent circuit
M	Mutual inductance between TC and RC
v_d	Input dc voltage
v_i	Output voltage of inverter
v_o	Output voltage
ω_o	Resonance frequency in rad/sec

Chapter 1 Introduction

1.1 Background

At present, worldwide on-road transportation primarily relies on petroleum. This causes the emission of enormous amount of greenhouse gases, thereby making it harder to satisfy stringent environmental regulations [1]. Also, the petroleum reserve throughout the globe is quite limited. Therefore, to conserve energy and protect the environment, the electrification of transportation has been carried out in the last few decades [2]. Transportation electrification enables the utilization of energy not only from fossil fuels but also from renewable energy sources, such as hydropower, solar-PV, and wind power.

In traction applications, the electrification of rail roads has been fully achieved in the past many years. However, there are some obvious challenges for large scale deployment of electric vehicles (EVs). These are as follows:

1) A high power and large capacity battery pack is usually required as an energy storage unit for an EV to operate up to a satisfactory distance. Therefore, the mass deployment of EVs was never realized in spite of several government initiatives such as subsidy and tax incentives [3]. The major limitation of EVs is the requirement of storing energy in a battery which has a high energy density, high power density, affordable cost, long cycle life time, good safety, and reliability. The most competitive solution for EV is Li-ion batteries, which has an energy density of about 90-100Wh/kg, whereas for gasoline it is about 12000Wh/kg [3], [4]. Therefore, for a given distance, an EV requires a large and very expensive battery, which is too heavy and too expensive as compared to gasoline.
2) Recharging an EV battery takes at least about half-hour to several hours depending on the power level of the attached charger, which is a lot more time than that required for refuelling gasoline cars. Therefore, EVs cannot get ready immediately if the battery charge is over. This is a practical issue since people may forget to recharge the EV and face difficulty when they need to use the vehicle.
3) Charging cables of EV are inconvenient and may lead to tripping, leakage due to aging of cracked old cables, and other additional hazards especially in cold zones. Also, people may have to brave the wind, rain, ice, or snow to plugin, riding the risk of an electric shock.

1.2 Wireless Power Transfer

In recent years, research on wireless power transfer (WPT) technology has gained significant popularity due to the availability of high power and high switching frequency semiconductor devices. The advantages of this technology are as follows [3], [5]:

1) Very convenient, safe and reliable due to elimination of direct electrical contact.
2) The power transfer is unaffected in hostile environments such as snow, water, dirt, wind, and chemicals.
3) It provides galvanic isolation.

Besides these general advantages, the WPT technology has merits which are specific to particular applications. In biomedical implants, for e.g., in heart pump battery recharging, WPT technology is the most practical and convenient [6] [5]. Similarly, WPT has found wide acceptance for recharging batteries of electronic gadgets, lighting, chemical plants, and underwater vehicles, etc. due to its flexible usage and the ability to prevent damages to the charging port.

Implementation of wireless charging in EV applications provides remarkable outcomes. Along with the aforementioned merits, it can reduce the battery storage requirement to 20% through opportunistic charging techniques [3], [7]. For EVs, opportunistic charging is possible by placing the wireless chargers in different parking areas, for e.g., home, office, service, shopping complexes and other general parking areas. Also, these chargers can be installed in the traffic signal areas for quick recharging. For recharging electric buses it can be installed in bus terminals, bus-stops and traffic signals. These types of chargers are called static WPT chargers. Intense research is being carried on dynamic WPT technology, where the EV battery can recharge while the vehicle is running [8], [9]. However, there are several challenges, both at the technical level and infrastructural or initial investment level. Therefore, taking into view the practical issues of using WPT technology, this thesis focuses only on static WPT technology.

1.3 Types of WPT Technologies

In this section a brief overview and qualitative comparison of all the possible WPT technologies are reported. Based on this study, the most effective technology is selected for medium power

(fraction of *k*W to several *k*W) and mid-range airgap (about 100mm-350mm) applications, which are especially suitable for EV battery charging.

1.3.1 Inductive WPT

Inductive charging systems generally consist of a primary side power converter, an inductive interface transformer, and a secondary converter [10]. The interface transformer is separable along the magnetic circuit so that one of the windings can be physically removed, eliminating the need for ohmic, i.e., metal-to-metal, contact of electric wires. In such a transformer, the shape and location of the magnetic core material and windings are very important design choices. This technology is already implemented in EV charging systems such as the GM EV1 [7] as shown in Fig. 1.1. The charging paddle (the primary coil) of the inductively coupled charger is sealed in epoxy as it is done in the secondary. The paddle inserted into the centre of the secondary coil permitted charging of the EV1 without any contacts or connectors at either 6.6 kW or at 50 kW. As it depicts in Fig. 1.1, this system is connector-less, but not wireless.

Fig. 1.1 Inductive charger paddle (left) and electric vehicle charging through the paddle (right) [7]

1.3.2 Capacitive Power Transfer

Wireless capacitive power transfer (CPT) technology has been proposed recently as an alternate wireless power transfer solution [11]. Fig. 1.2 shows a typical CPT system fed from a half bridge voltage source inverter and the primary and secondary side compensation networks are *LCL* and *LC* types, respectively. As shown in in Fig. 1.2, the CPT interface is constructed around a pair of coupling capacitors. The operating principle is same as usual parallel capacitors, where the dielectric medium is only air. Inductive coupling requires a magnetic core in order to provide good coupling and in some cases shielding in order to prevent EMI. With increasing operating frequency, CPT may

compete inductive coupling, as the former can offer equally good galvanic isolation and does not require a costly, high-frequency rated magnetic core. This technology finds suitable applications in low power level such as biomedical implants, or in charging of space-confined systems such as robots or mobile devices [11], [12], [3], etc. Its design flexibility and low cost make it ideal for power delivery in reconfigurable and moving systems, such as robot arms, latches, and in-track-moving systems [11]. However, owing to lower power density, the CPT technology is not preferred for higher power applications such as EV charging [7].

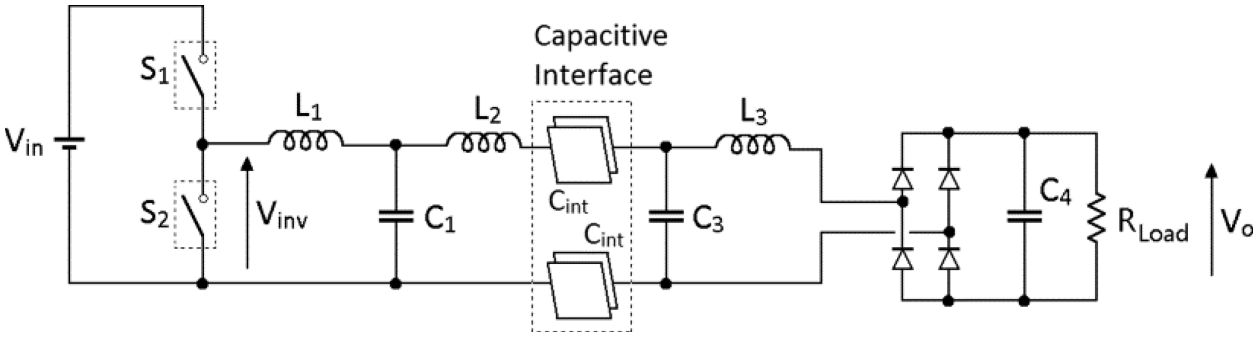


Fig. 1.2 A typical CPT system with LCL compensation in primary side and LC compensation in secondary [11]

1.3.3 Resonant Inductive Power Transfer

In inductive coupling technology, if a significant amount of airgap is introduced then the power transfer between the primary to secondary coil becomes ineffective. This fact is illustrated using a simple two winding coupled inductor model shown in Fig. 1.3. The mutual inductance, M reduces very fast with increase in airgap between the coils. Therefore, to have significant amount of induced voltage ($=\omega M i_1$) in the secondary side, the operating frequency (ω) and primary coil current (i_1) must be high. Owing to wide availability of high voltage, high current, and high switching frequency semiconductor devices, ω can be ranging from kHz to hundreds of kHz. However, high leakage impedance of primary coil introduces another difficulty to drive significant amount of current (i_1) through coil. A reactive power compensation circuit can be places in primary side to drive higher coil current. Therefore, the primary side converter does not need to feed high voltage to coil. Although, with these arrangements, it is possible to induce sufficient amount of voltage at secondary coil, but most of it is dropped across the high secondary leakage impedance. Therefore, another reactive power compensation is also required in the secondary side to transfer power effectively. Usually, these compensation elements in both the sides resonate with the coil inductances; therefore, this technology is called resonant inductive power transfer (RIPT). This

technology is pioneered and patented by Nikola Tesla [13]. This technology is most suitable for transferring power with airgap from few mm to hundreds of mm, where the power level varies from fraction of watt to hundreds of *k*W. Owing to high power density, high efficiency, wide power range, and acceptable airgap length, RIPT technology is most demanding among all other WPT technologies [14] - [37]. It finds applications in EV charging, electronic gadgets, implants, chemical factory, underwater vehicles, and lightings etc [3], [5], [6]. In the literature, this technology is often called as inductive power transfer (IPT) and throughout this thesis it is named as IPT.

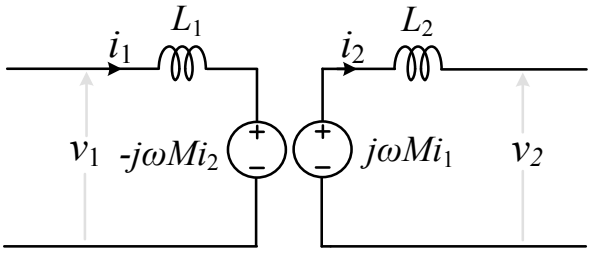


Fig. 1.3 Two winding coupled inductor model

1.3.4 Resonant Antennae Power Transfer

Resonant Antennae Power Transfer (RAPT) is also pioneered and patented by Nikola Tesla, and has recently been studied by MIT [13] and Intel. The fundamental operating principle of this technology is similar to IPT. RAPT uses two, or more resonant antennae tuned to the same frequency. The resonant capacitances and inductances are integrated into the antennae. These systems often have large WPT coils (antennae), often helical with controlled separation between the turns to obtain a distributed and integrated, resonant capacitance. The airgap length can be much longer than IPT system due to use of high quality factor coils and high frequency of operation. Acceptably, efficient power transfer is possible at distances up to approximately 10 meter and operating frequency is in the *M*Hz range [38]. However, for several kW power transfer with airgap suitable for EV applications, this RAPT technology is essentially same as IPT technology.

1.4 Detailed Literature Review of IPT

Considering the advantages of IPT technology, a detailed theory of it is reported. The basic operating principle is like a two-winding transformer (or a coupled inductor), where the

magnetizing inductance (or coil coupling factor) is much lower than conventional iron core transformer (or inductor) [7]. From Fig. 1.3 coupled inductor model, the voltage across primary and secondary terminals are given as

$$v_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \tag{1.1}$$

$$v_2 = L_2 \frac{di_2}{dt} + M \frac{di_1}{dt} \tag{1.2}$$

where, $M=k\sqrt{L_1 L_2}$; k is the coefficient of coupling between TC (primary) and RC (secondary); L_1 and L_2 are self-inductances of primary and secondary coils, respectively. For a given primary coil current, I_1, the open circuit induced voltage, and short circuit current through L_2 are given as

$$V_{\text{oc}} = \omega M I_1 , \qquad I_{\text{sc}} = \frac{V_{\text{oc}}}{\omega L_1} = I_1 \frac{M}{L_2}. \tag{1.3}$$

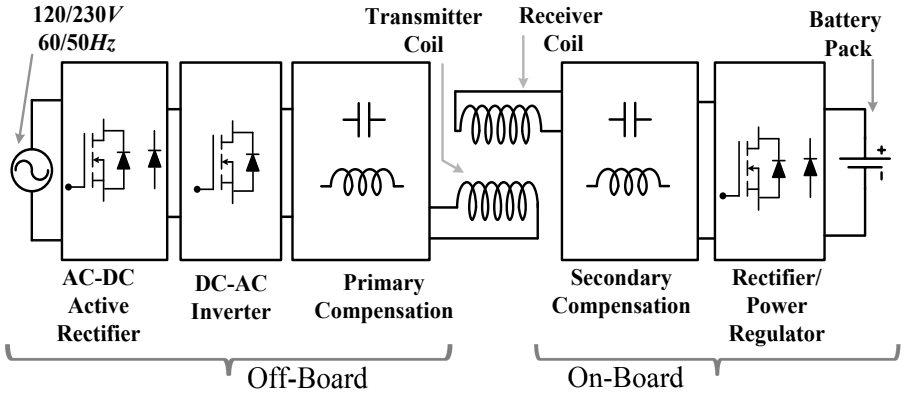


Fig. 1.4 A typical electric vehicle wireless charging system

When the system is tuned at resonance frequency with compensation capacitors, the available power is derived as [7]

$$P = \frac{V_{\text{oc}}^2}{R} = \omega \frac{M^2}{L_2} {I_1}^2 Q = \omega L_1 I_1 I_2 \frac{M^2}{L_1 L_2} Q \tag{1.4}$$

where, $Q= \omega L_2 / R$ and R is load resistance.

A number of IPT topologies are reported in the literature based on compensation topologies, power converter topologies and IPT coils etc. Generally, all these IPT system follows a similar power conversion stages as shown in Fig. 1.4. Generally, the input is line frequency ac, which is rectified

by active rectifier to draw power at unity power factor (UPF). Next, dc-ac inverter injects high frequency ac to primary compensation network. In the secondary side, the power is extracted effectively using another compensation network. Finally, this ac power is rectified either by active or passive rectifiers. A detailed study of existing IPT systems are included here, and to make it concise, descriptions are reported based on different classifications.

1.4.1 Classifications Based on Compensation Topologies

The existing IPT topologies can be broadly classified based on basic series and parallel compensations or combinations of these basic compensations.

1.4.1.1 Basic Compensation Topologies

With an airgap ranging from 150mm to 300mm for EV battery charging applications, the TC to RC coupling is generally very low (typically below 0.3) and compensation both in the TC and RC side is mandatory. By adding one capacitor in each side of the coils, four basic types of compensation networks are formed as shown in Fig. 1.5. Several papers provides detailed study these networks, especially for the series-series (S/S) [14] - [23] and series-parallel (S/P) [3], [24] -[26]. From Fig. 1.5, it is clear that the selection of inverter type is dependent on TC tank network. When the TC side compensation is series type, the inverter is VSI whereas, the inverter is CSI when TC side compensation is parallel type.

S/S topology is the simplest to design, where compensation is load and coupling independent. However, during no load or light load, the series RC tank network provides almost zero reflected impedance to TC coil. Therefore, the VSI output current surges when RC is uncoupled to TC and the system becomes unstable [39]. This issue is generally taken care with very fast closed loop control. The parallel *LC* tank at RC side in S/P compensation always reflects some impedance to TC coil; hence, current surge does not arise. However, surge current will also appear at VSI output for this case, if RC coil is moved out. As per the study, S/S topology provides higher efficiency than the S/P topology in a wide range of load resistance [14], [22], [40]. Moreover parallel-compensated system has a large reactive current in the receiver coil and the reactive power is reflected to the primary side [41]. Considering all these issues, most of the IPT topologies uses S/S compensation for EV charging applications.

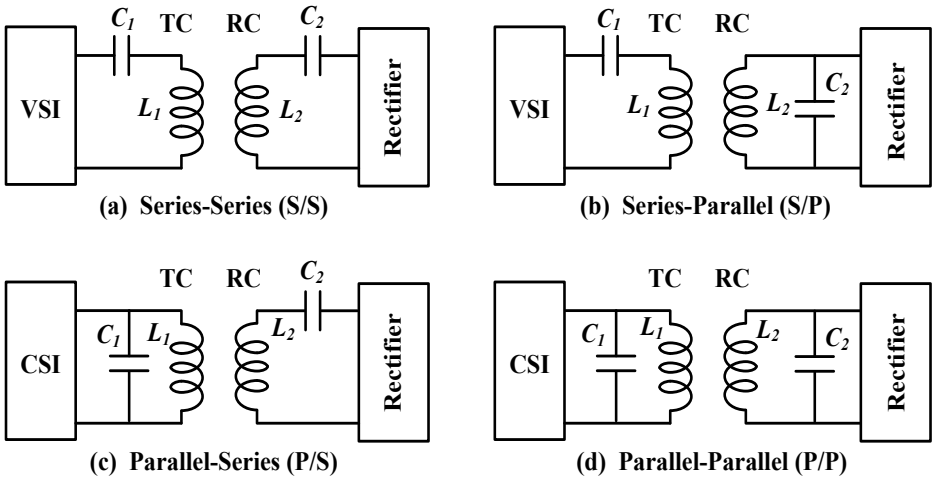


Fig. 1.5 Basic compensation topologies for IPT circuit (a) Series-Series (S/S); (b) Series- Parallel (S/P); (c) Parallel- Series (P/S); (d) Parallel- Parallel (P/P)

The P/S and P/P compensation networks are realized with CSI as inversion stage. Generally a dc link inductor is required to function CSI [5], [34]- [37] . Because, the previous stage PFC output is generally stiff voltage; hence, this dc link inductor is an extra bulky component and research on P/S and P/P compensation networks were quite limited to only low power. However, in an applications where stiff current is readily available these compensation topologies are comparatively more suitable than the S/S and S/P topologies. The major advantages of these topologies are as follows:

1) High magnitude TC current circulates through the parallel capacitor without flowing through the devices [5]. In other words, like in the series compensation, the capacitor nullifies the effect of coil leakage impedance, in parallel compensation the effective magnetizing impedance become very high. Therefore, parallel tank provides lower current stress on inverter devices;

2) The coil current corresponding to a parallel tank is very close to sinusoidal, because higher order harmonic currents predominantly flow through the lower impedance offered by the capacitor;

3) Unlike S/S and S/P compensations, in P/S and P/P compensation the inverter output never gets shorted during coil uncoupled condition. Moreover, just like open circuiting the inverter output of VSI does not harm the circuit, short circuiting the output of CSI does not damage any components.

1.4.1.2 Combinations of Basic Topologies

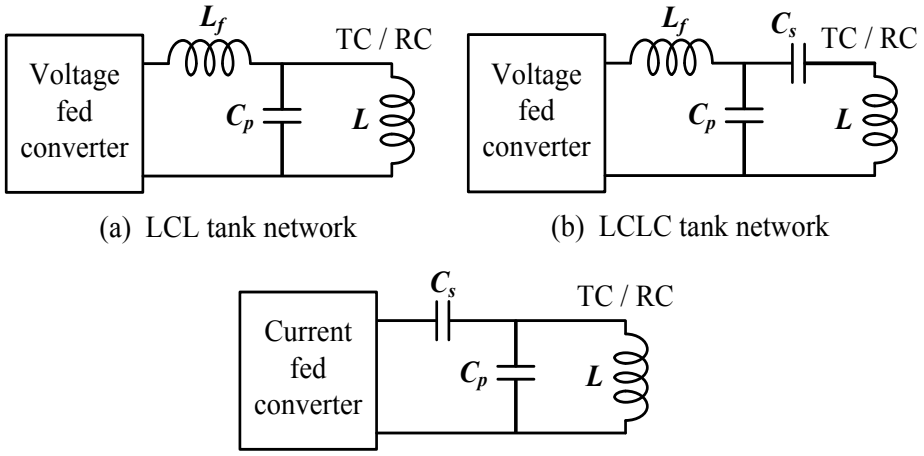


Fig. 1.6 Combination of basic compensation topologies, (a) *LCL* tank; (b) *LCLC*; (c) Series parallel (SP) tank

Considering the merits and demerits of the basic compensation techniques, several complex combinations of these four basic topologies are reported to achieve improved performances. Fig. 1.6 shows those compensation networks which are most frequently reported for their added advantages. Fig. 1.6 shows three general compensation network diagrams. Any of them could be selected either TC or RC compensation network. Often, one side tank network is selected from one of these three topologies and the other side is selected as simple series or parallel compensation network. It is clear from here that there are several IPT topologies possible based on the combinations of these compensation networks. In fact, as per the existing research of IPT topologies are concerned, almost all these possible networks are already studied or being studied. Considering the focus of this thesis is to present a detailed study of current- fed IPT topologies, only the important key points of each of these topologies are presented.

Fig. 1.6a *LCL* tank network is very common for its simple yet comparatively improved performances over simple parallel or series tank [39], [42] - [46]. It includes the advantages of parallel *LC* tank networks while eliminating the limitations of series tank. Unlike parallel tank, this topology is fed from VSI; hence, bulky dc link inductor is eliminated. However, a light weight inductor, L_f in the high frequency tank network is required. Unlike the dc inductor used in CSI fed parallel tank, L_f carries ac current and is highly sensitive to effective power transfer; therefore, L_f requires high precision, which incurs additional cost. When *LCL* tank is used at TC side, it does

not create instability issue like series tank during no load conditions [39]. This tank is well used for bi-directional IPT applications [42], [43].

Y. Yao *et.al.* [44] reports that the VSI output current with T type compensation topology contains significant amount of lower order harmonics (3^{rd}, 5^{th}, and 7^{th} etc.) and they have 90^0 phase differences from their respective harmonic voltages, for e.g., 3^{rd} harmonic current and voltage has 90^0 phase difference. Therefore, although the fundamental component voltage and current are in same phase, but significant harmonic content in current deviates UPF operation of inverter significantly. Although, this fact is very well visible in several reported works, but [44] reports the details impedance analysis to justify this fact. Therefore, UPF operation with *LCL* tank is not as significant as the parallel compensated primary topology, where the inverter output voltage is very close to sinusoidal. From [5], [34], [35] it is evident that the parallel tanks are mostly attempted to operate at ZPA point.

In *LCL* topology adding one extra capacitor in series with the coil makes *LCLC* tank as shown in Fig. 1.6b [27], [47]. Even though the analysis of this topology is similar to *LCL* tank, but this is an improved version. In transmitter side this extra capacitor directly reduces the coil leakage impedance. This improves power transfer capability [48]. In the receiver side this tank is used to achieve a unit power factor pickup [41].

The Fig. 1.6c compensation network is suitable in the TC side when the inverter is current-fed type. This compensation network is termed as series–parallel–series (SPS) topology in [24]. However, this converter is tested with voltage source inverter where an extra inductor is added in series with series capacitor, C_s to make it compatible with VSI. This compensation in TC side and series *LC* compensation in RC side have the capacity to deliver rated power with wider coil misalignments [24].

1.4.2 Classifications Based on Power Converter Topologies

The input power of IPT inverter is usually supplied from a dc source, such as PV modules or a rectified ac grid as shown in Fig. 1.4. The purpose of this converter is to feed high frequency ac to primary resonant tank, and maintain load power to desired level. A number of IPT power converter topologies are reported in literature, and these are classified as follows.

1.4.2.1 VSI Topologies

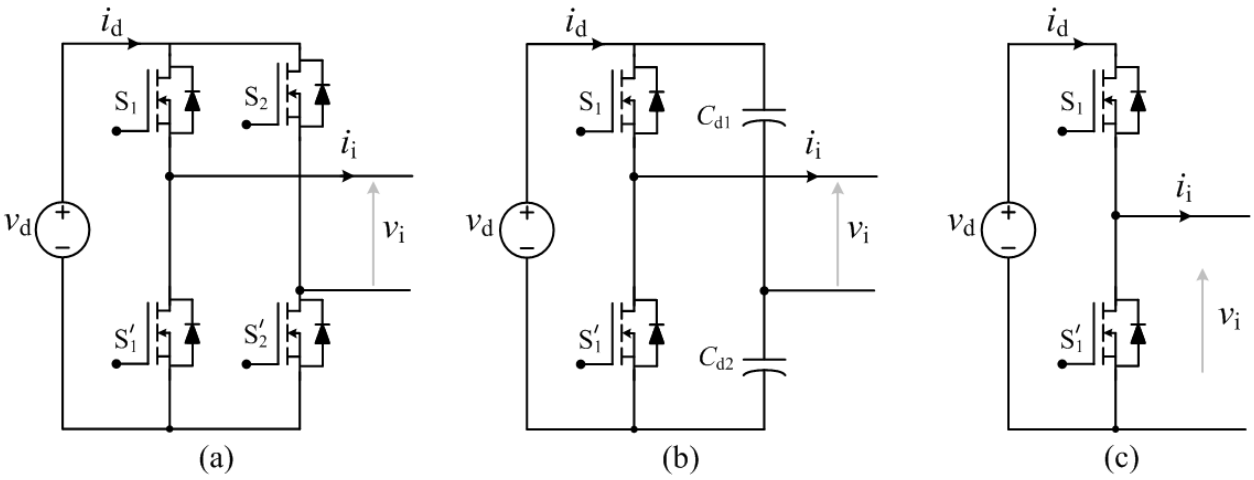


Fig. 1.7 (a) Full-bridge, (b) half-bridge, and (c) semi-bridgeless VSI topologies for IPT systems

The voltage-fed H-bridge and half-bridge power converters are shown in Fig. 1.7a [14] - [26] and Fig. 1.7b [25], respectively. The half-bridge converter employs two capacitors in the second leg to provide the neutral point of input dc voltage. Compared with H-bridge converter, a half-bridge converter is simpler in controlling and reduces the number of switching devices, which reduces switching losses. However, the output voltage of the neutral point between two capacitors is normally unbalanced during the switching process of two switches. Another limitation of the half-bridge topology is that the converter can only generate ac output with the amplitude of $\pm v_d/2$, which limits its application only in lower power. Therefore, in practice, H-bridge converters are preferable in most of applications.

In IPT systems series, *LCL*, or *LCLC* can be used as compensation network with VSI. For full bridge VSI, usually, there are four hard switching states and four soft switching states within an output voltage cycle [25]. To control the output power, another power converter can also be used in the secondary side. If another H-bridge converter is employed in the secondary side, it becomes bidirectional IPT system. The power level, power flow direction and input power factor can be controlled by adjusting the phase shift angle between two converters [42], [43]. Fig. 1.7c shows a semi-bridgeless VSI, which is reported to have very high efficiency (94.4% at1 *k*W) with phase shift control [49].

1.4.2.2 Direct Ac-ac Converter Topologies

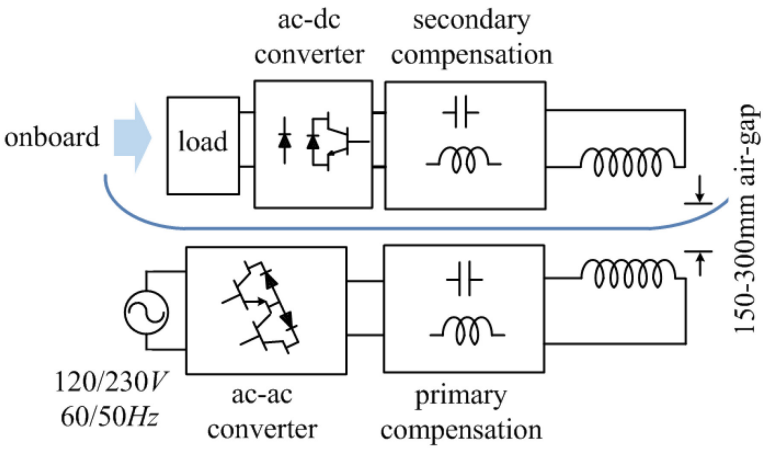


Fig. 1.8 IPT topology with single stage direct ac-ac converters

To improve overall efficiency and reduce component count of the complete converter system, direct ac-ac converter is reported to generate switching frequency ac, directly from line-frequency ac [27] - [33]. Therefore, compared with two stage power conversion, it is a single-stage power conversion as shown in Fig. 1.8. Also, short-lived bulky dc link capacitor is removed from the circuit. Usually, the conductive charging of EV batteries are more efficient and less expensive compare with the wireless inductive method, mainly due to higher copper loss and expensive materials used in IPT coils. Successful implementation of direct ac-ac converter can compensate those two demerits of the existing multi-stage IPT power supplies. However, there are some obvious limitations of IPT topology with direct ac-ac converters such as

1. the components are required to be rated for peak power, where the rating of the components in the tank network including IPT pads are quite high due to poor coil coupling, and
2. since, the grid current is not directly controlled; hence, high quality source current is not ensured.

Considering the limitations, these topologies could be more suitable for low power applications viz. electronic gadgets, body implants and other low power industrial applications. This is because the IPT circuit components can easily handle the peak power of such low power, while keeping the converter cost low due to less number of components. For Higher power applications such as EVs, along with cost and efficiency the source current quality is very important, which only the IPT topology with conventional multi-stage power conversion ensures through PFC.

1.4.2.3 Current Source Inverter Topologies

Occasionally, current source inverter (CSI) is also used in IPT systems [5], [34], [35], [36], [37]. Fig. 1.9 shows the existing IPT systems fed from a current-fed push-pull inverter, where the transmitter coil tank network is parallel *LC* type. Following merits of these systems are reported in literature:

1) Suitably designed parallel capacitor supplies the reactive power consumed by TC without flowing through the inverter devices. Therefore, the inverter device current is lower;
2) Coil current quality with the presence of parallel capacitor is almost sinusoidal, because the higher order harmonics primarily passes through this capacitor;
3) Achieves soft-switching of all the inverter devices;
4) In CSI topology the inductor in dc link limits short circuit current during fault.

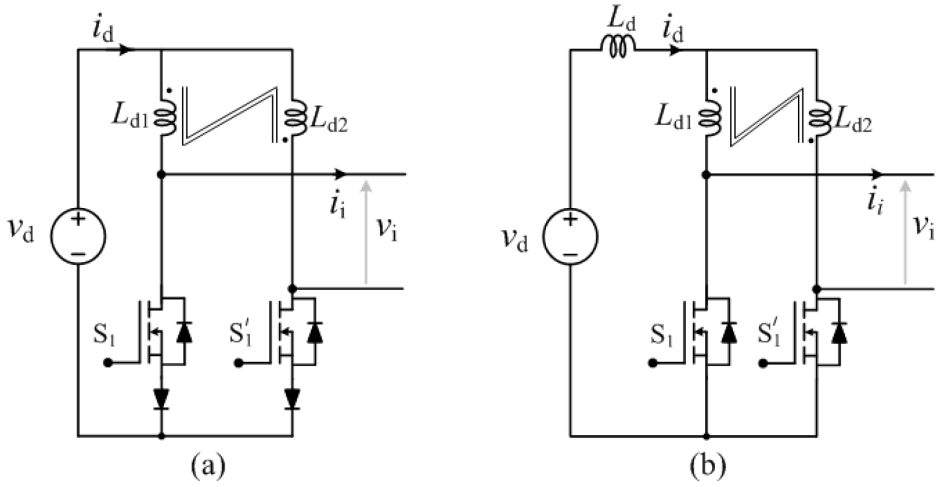


Fig. 1.9 Existing IPT topology using current-fed push-pull inverters (a) without extra input inductor and with reverse voltage blocking devices (b) with extra input inductor and without reverse voltage blocking devices

However, there are some demerits of these systems, which are listed as follows:

1) Bulky dc link inductor is needed to get stiff dc current at the inverter input. However, in an application where stiff dc current input is readily available such as solar cell output, there this topology will find suitable application.
2) Parallel resonant tanks are reported to load dependent; therefore, complex control is required to tune inverter switching frequency to tank resonance frequency. This dynamic

tuning is usually carried out either by adopting variable frequency control of inverter, or by varying tank capacitances dynamically.

3) Owing to this control of inverter, the dynamic load demand is generally met by additional dc-dc chopper connected before the load, thereby increasing power conversion stages.

4) Variable frequency control experiences converter start-up problems and frequency bifurcation (i.e., multiple operating frequencies) issues.

Owing to these limitations, current source inverters are only reported for low power applications such as body implants.

1.4.3 Classifications Based on IPT Coils

Unlike the traditional inductors or transformers, the IPT coils are usually planer type. These coils are generally two types i.e., unipolar and bipolar.

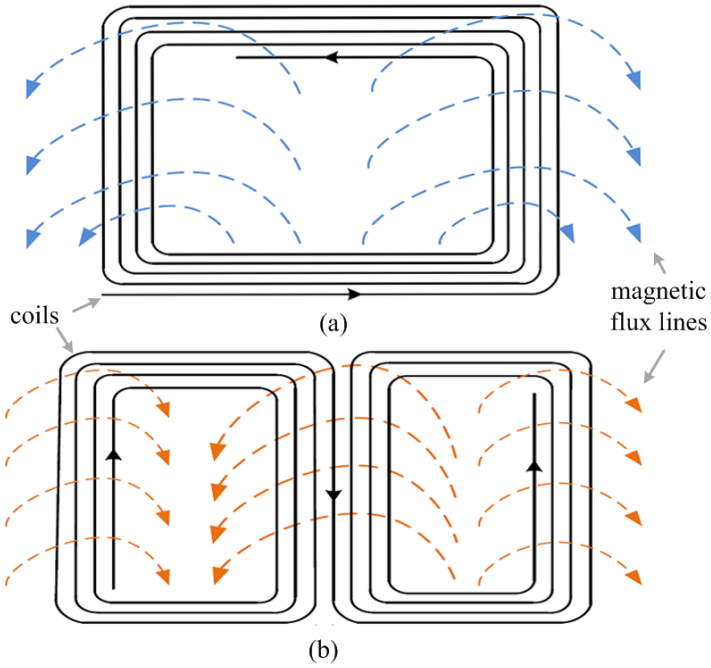


Fig. 1.10 Wireless IPT coil types (a) unipolar (b) bipolar [50]

1.4.3.1 Unipolar IPT Coils

Usually, practical IPT coils for EV are either rectangular or circular with the form of a flat Archimedean spiral placed on magnetic material. Fig. 1.10a show a typical circular shaped wireless IPT coil [46], [50]. Other types of coil structures include U, I, and E etc [16]. These

systems have evolved from essentially track-based designs to concentrated couplers [51]. Usually, these coils are placed on top of a solid ferrite plate. It helps to improve coefficient of coil coupling and reduces EMI [22], [48]. However, these designs are comparatively fragile and expensive due to the geometry of the large ferrite plate, which is required to achieve the desired flux path. In addition, designs using E-cores are necessarily thick, which compromises the ground clearance of the EV [7], [52]. To overcome these limitations, a new IPT coil with arrays of small ferrite plates have been reported in [52]. To reduce ac resistance of IPT coils, litz wires are often used to improve efficiency.

1.4.3.2 Bipolar IPT Coils

Fig. 1.1b shows a multi-coil coupler, which is commonly known as a bipolar coil [53]. Its operation may be visualized by considering two coils lying on the striated ferrite such that the line of centres is along the direction of the ferrite. Since, this structure has comparatively more closed path for the magnetic flux; therefore, coefficient of coupling is relatively more than unipolar arrangement. Although, in this diagram both the loops of bipolar coil carry same current, they can be controlled to carry different current with the help of two power converters [54]. The bipolar structures have higher tolerance to coil misalignment, compared with unipolar coils.

1.5 Research Problem and Objectives

Wireless inductive charging technology has a great potential for successful deployment of EVs on a large scale. The opportunistic charging technique realized by IPT is capable of reducing the battery size significantly as compared to conventional systems. Although, several prominent research groups are actively working to make IPT feasible for practical use, several aspects of this technology require further improvement. The possible improvement areas are i) power converter and compensation network design, ii) control of the overall system, iii) wireless coil design, iv) construction of the road embedded coils, and iv) EMI and safety aspects. All these areas require extensive research and improvements to successfully implement IPT technology in EVs. This research work primarily deals with power converter design, compensation network design, and closed loop control aspects.

Almost all the existing power converters for driving the IPT coils are VSI based. VSI leads to the selection of i) series *LC*, ii) *LCL,* or iii) *LCLC* tanks in primary side. A series *LC* compensated

primary fed from a VSI experiences severe instability during light load, or in the absence of a secondary coil. Also, owing to its series structure, it draws high amplitude primary coil current from VSI. Although *LCL* or *LCLC* tank, fed from a VSI, does not experience these issues and has high tolerance to coil misalignments, they draw non-sinusoidal current from the inverter. This leads to higher VA loading and subsequent higher power loss in the inverter. Although the extra ac inductor in these tanks is quite small, it is highly sensitive to effective wireless power transfer. Therefore, this inductor must be designed and manufactured with very high precision, which incurs additional cost. Considering these limitations, this thesis fully focuses on concept study and feasibility analysis of current-fed power electronics for IPT system, where the primary application is EV charging. The objectives of this thesis are as follows:

1) Study of possible improvements in power converters and compensation techniques for medium power IPT applications (i.e., fraction of *k*W to several *k*W);
2) Proposing new converters and compensation topologies to make this technology more practical;
3) Report the detailed steady-state performance, converter design, and soft-switching of switching devices;
4) Analyze and propose simple and effective control techniques for the IPT topologies and report complete dynamic modelling and closed-loop control;
5) Develop scale-down prototypes for all the proposed IPT topologies to verify mathematical analysis and simulations with experimental results.

1.6 Methodology

To achieve the objectives within the given time limit, the following methodology has been adopted:

Report a comprehensive study of existing power converters and compensation topologies for IPT systems, and identify merits and demerits

Considering the fact that an extensive study of voltage-source converter topologies has already been carried out, and feasibility of current-fed topologies received very limited attention, perform a systematic study on possible use of current-fed converters

Based on the merits and demerits of current-fed converters, propose new converter topologies, modulation, and control techniques to make it more acceptable for practical use

Perform preliminary simulation on a suitable platform to find the suitability of the proposed system

Analyze comprehensively to find out all justification of successes or failures in achieving desired results

Modify converter topology or modulation and control schemes to achive desirded results

Verify the results with the help of mathematical expressions, and also through simulation results

If the mathematical model and sumulation results have acceptable agreement, then build a scale-down lab prototype and verify analytical and simulation results with experimental results

1.7 Thesis Contributions

The major research contributions of this thesis are as follows:

i. In Chapter 1, a comprehensive literature study on IPT technology has been provided, and several possible merits and demerits of power converters have been identified. For higher power IPT applications, limitations of existing current-fed converters are analysed. The

major issues include a) converter start-up, b) frequency bifurcation, and c) short-circuiting parallel capacitor at the primary side.

ii. In Chapter 2, a new parallel *LC* tuned IPT topology, fed from a full-bridge CSI, has been proposed, where the secondary side has series *LC* compensation. The system is controlled through fixed frequency variable duty cycle modulation and does not experience any start-up and frequency bifurcation issues. The full-bridge inverter structure enables the increase of power level. Reverse voltage blocking devices in inverter eliminates short-circuit path of parallel capacitor. The steady-state operation, converter design, and soft-switching criteria are reported in detail. Simulation results obtained from PSIM 10 have been included to verify the analysis and performance of the proposed topology. A 420W scale-down lab-prototype has been developed and experimental results have been included to verify analysis and simulation. However, one limitation of this topology is that the required voltage rating of inverter devices is quite high as the primary coil voltage directly appears across the inverter.

iii. In Chapter 3, considering the limitation of parallel *LC* tank at primary side for higher power applications, a modified parallel-series (*CLC*) compensation technique has been proposed. The extra capacitor in series with the primary coil directly reduces the coil leakage inductance. Therefore, keeping all the merits of earlier topology, this topology reduces the CSI voltage stress significantly, thereby making it more suitable for EV applications. A detailed report of the steady-state operation, converter design, and soft switching conditions has been provided. Both simulation and experimental results have been included to verify the expected improvements.

iv. In Chapter 4, small-signal modelling and closed-loop control of both the current-fed IPT topologies is provided. The control goals are achieved through two-loop method, where the inner input current loop controls the source current, and outer output current loop meets load requirements. Compared with existing frequency modulation technique, this control technique is based on duty cycle modulation, which is simple and easier to implement. However, fixed frequency control of these parallel resonant tanks cannot maintain ZPA operation of the inverter due to load-dependent resonance. Therefore, a new load-independent resonant tank design has been proposed, where ZPA operation is always

maintained to ensure least VA loading on inverter. Experimental results obtained from a 1.6*k*W lab-prototype validates the proposed load-independent ZPA design, small signal modelling and closed loop control of the converter.

v. In Chapter 5, considering the need for V2G operation of EVs for future smart grid applications, a new bidirectional IPT topology has been proposed for the first time using current-fed converter technology. It has current-sharing feature in grid side converter, and voltage doubling feature in vehicle side converter. A detailed report of the steady-state operation, converter design, and soft-switching conditions is provided for both G2V and V2G power transfer. A 1.2kW bi-experimental set-up has been developed and detailed experimental results have been included to bidirectional power transfer.

vi. In Chapter 6, the necessary requirement for current-fed technology in single-stage IPT systems is established. Existing single-stage IPT topology, derived from VSI, fails to draw high quality current from the grid. A new single-stage IPT topology using current-fed direct ac-ac converter has been proposed and analyzed to justify the claims. A detailed report on the steady-state operation, converter design, and soft switching conditions is provided. Complete control is carried out through two loop control method, where the inner loop maintains high quality source current, and outer loop meets dynamic load demand. Experimental results obtained from 1.2*k*W grid-connected lab-prototype verifies all the analysis and performance of the closed loop system.

vii. All these studies and results conclude that current-fed technology is also a viable solution for wireless inductive power transfer for medium power applications.

However, there are some limitations of this research work. IPT coil design and optimization of coil size and volume have not been carried out. Subsection 1.4.3 of literature review provides a number of references to find the details of coil design aspects. This research work has selected some suitable and simple coil structures from those references and has verified the performances of proposed converters. Also, the impact of the magnetic field on foreign objects (e.g., humans, animals, or any equipment) has not been considered in this thesis. It is already proven that the leakage magnetic flux of the IPT coils can be kept well within the specified limit with the use of proper aluminum shielding [52].

1.8 Thesis Outline

The contents of the thesis are organized as follows:

In Chapter 2, a new current-fed IPT topology is reported, where the TC and RC side resonant tanks are *LC* parallel and *LC* series types. Steady-state operation, converter design, ZCS turn-off conditions, and IPT coil selection are reported, where the CSI devices are given bipolar PWM pulses. Both simulation and experimental results are demonstrated to validate the analysis.

In Chapter 3, an improved current-fed IPT topology is proposed, where the primary side tank is parallel-series (*CLC*) type and secondary side is series *LC* type. Steady-state operation, performance improvements, converter design, and ZVS conditions are reported. Through a comparative study with the previous topology, the improvements are highlighted. Simulation and experimental results are included to verify the performance improvements.

In Chapter 4, complete small-signal modelling and closed-loop control is reported for both the current-fed IPT topologies, where the inverter devices are given unipolar PWM pulses. To reduce the control effort of inverter, a load independent tuning technique is reported for both the topologies; therefore, the control is fully focused on meeting load demand and achieving soft-switching characteristics. Experimental results of both the CSI IPT topologies are reported to verify ZPA operation and closed-loop control.

In Chapter 5, a new bidirectional IPT topology with CSI is proposed. Steady-state operation, and converter design is reported for the G2V and V2G operating modes. Also, ZVS conditions of both the primary and secondary side converter devices are established for both operating modes, where the control is carried out with frequency modulation of inverter. Experimental results are included for both G2V and V2G operations to justify the suitability of the proposed bidirectional IPT topology.

In Chapter 6, a single-stage IPT topology with current-source ac-ac converter is proposed to achieve UPF at source. The chapter establishes the necessary requirement of current-fed technology in single-stage IPT to achieve PFC. Detailed steady-state operation, dynamic modelling through transfer-function derivation, and closed loop control is reported. Experimental results are reported to verify the closed performance of the converter.

In Chapter 7, conclusions and summary of thesis are presented along with guidelines for future work.

1.9 Conclusions

This chapter establishes the indispensable role and appropriateness of the wireless power transfer technology in EV applications. Based on the study of several WPT technologies, IPT technology has been found to be the most appropriate option for EV charging in terms of efficiency, power level, and power density. Although, dynamic IPT technology promises immense benefits with regard to battery size reduction, it has great challenges both at the technical level (e.g., coil misalignment, fast control, and EMI exposure to living objects) and at infrastructural level (e.g., new road construction with IPT coils, heavy initial investment, high operating costs etc.) Therefore, static wireless IPT system is a viable option for EVs, which can be installed in the parking spaces (e.g., home, office, shopping centers, streets, etc.), as well as at bus-stops, bus-terminals, and traffic signal areas.

To make IPT practical for use in EVs, several areas of the technology must be improved. This thesis essentially focuses on the improvement of power converter topologies, compensation networks, and closed-control techniques. Existing research in these areas is mainly addressed with VSI, and the compensation is either series *LC*, *LCL* or *LCLC*. Several merits and limitations of these compensation networks are reported in detail. Examining these factors, and considering the limited study of current-fed technology in IPT applications, this thesis fully focuses on concept study and feasibility analysis of current-fed power electronics, where the primary application is EV charging.

Chapter 2 H-bridge Current-Fed IPT Topology with (*L*)(*C*) Transmitter and (*LC*) Receiver Tank

In this Chapter, a detailed discussion of the limitations of existing current-fed IPT topologies in higher power applications are reported. Based on this understanding, a new current-fed IPT topology is proposed, analysed, and designed in detail.

2.1 Introduction

The literature review section consists of a general study on existing current-fed IPT topologies. A more detailed study is carried out to find the reasons for not using these topologies in higher power applications. Fig. 2.1a shows dc-ac and ac-dc stages of a current-fed push-pull current doubler circuit based IPT system [5], [55]. Fig. 2.1b shows another existing push-pull converter circuit which requires several bulky reactive components for operation [5], [37], [56]. The dc inductor (L_d) and phase splitting transformer (L_{d1} and L_{d2}) are used to generate square wave current for resonant tank, while devices S_1 and S_1' operate under ZVS conditions. Both the converters select parallel resonant tank in the primary side, which leads to lower current stress on devices S_1 and S_1' and provides very close to sinusoidal profile of primary coil current. Also, input inductor limits the short-circuit current during inverter fault. Furthermore, only two controlled devices or MOSFETs are required in the converter circuit. The gate driver circuit is very simple because the source terminals of both the MOSFETS are connected to a common point as dc input ground terminal [57], [58], [59]. Generally, these converters are controlled through variable switching frequency fixed duty cycle method. The switching frequency is solely determined by the inverter output voltage, v_1 and is done by sensing zero crossing of v_1. This helps to achieve both ZVS turn-on and turn-off of both the devices.

However, the major limitation of this control method is to start-up the converter since there is zero voltage at inverter output [5]. The number of inductive elements for both topologies are high [56]. Also, the zero crossing of inverter output voltage is a single operating point. Therefore, exact detection of that point and turning on one MOSFET and turning off the other MOSFET without a delay in sensor and control is a challenge. If this control is not accurate, then in the Fig. 2.1b circuit, the parallel capacitor gets short circuited through a MOSFET and body diode of other MOSFET

[5]. However, this is not a major problem if the inverter output voltage is low and operating switching frequency is low enough such that control circuit delay is negligible. Fig. 2.1a clearly shows this point: when amplitude of v_1 is low, zero crossing detection error does not lead to a significant voltage rise of v_1. However, in higher power applications the inverter output voltage amplitude is high, and it rises sharply after zero crossing. Therefore, if the MOSFETs are not turned-on and turned-off exactly at zero crossing, then the tank capacitor will be short circuited through MOSFET and body diode. This will result in significant power loss. For these reasons, the application of these topologies is generally limited to low power applications such as body implants [56].

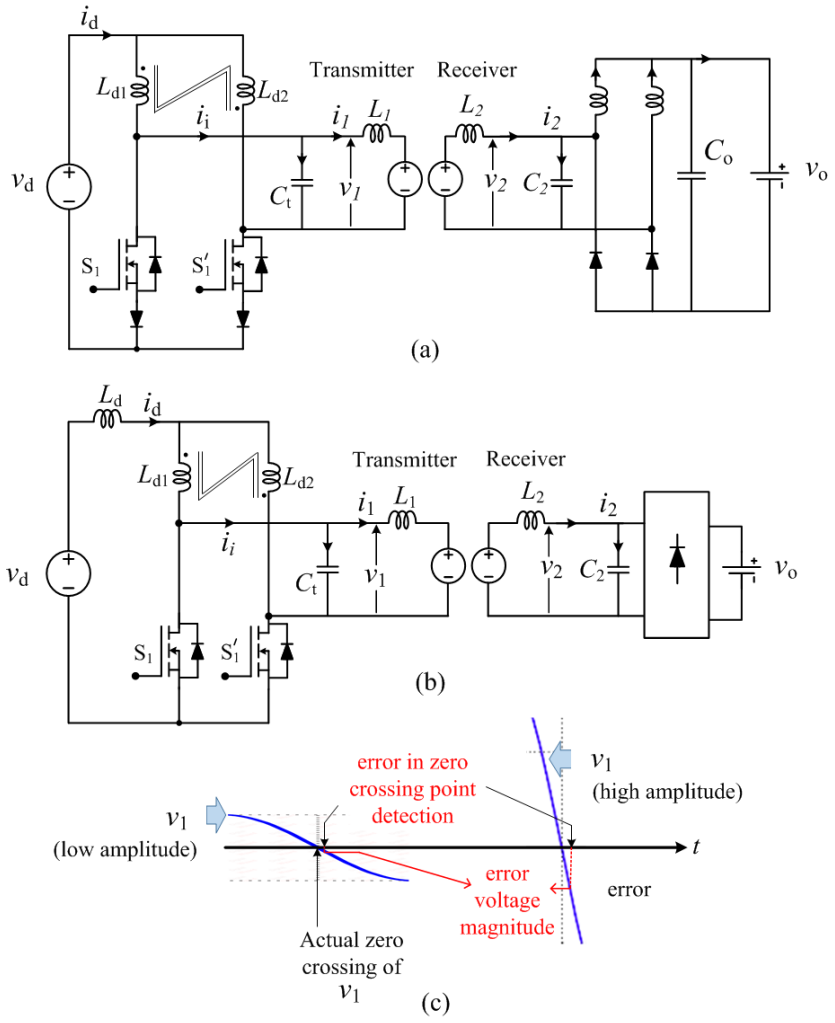


Fig. 2.1 IPT with current-fed push-pull current doubler converter (a) without dc inductor, L_d, [5], [55], (b) with DC inductor, L_d [5], [37], [56] (c) limitation of ZVS push-pull converter with zero crossing detection technique for higher power applications.

Considering these limitations, a new resonant converter using a full-bridge CSI topology has been proposed next. The full-bridge structure makes the system scalable for higher power. Reverse voltage blocking devices in the inverter disables the short-circuit path of the parallel capacitor. Also, fixed frequency variable duty cycle modulation eliminates frequency-bifurcation problems.

2.2 Proposed IPT Topology

Fig. 2.2a shows the complete dc-dc stage circuit diagram of the proposed IPT topology with current-fed H-bridge inverter. The input current, I_d can either be output of a stiff current source viz. a solar cell or the output of a PFC rectifier connected with an inductor, L_d. For simplicity, in this research the stiff current, I_d is generated using inductor, L_d connected with a voltage source, V_d as shown in Fig. 2.2a. Considering the switching frequency of inverter is significantly high and the inductor, L_d is sufficiently large, the full bridge inverter injects a square wave current, I_i to the transmitter resonant network. Transmitter coil inductance, L_1 with capacitor, C_t makes a parallel resonant tank network on the transmitter side. Because of air core, the value of the mutual inductance, M is much lower than the conventional iron core coupled inductor. Therefore, to transfer a significant amount of active power through the air, the required transmitter coil current must be high enough such that sufficient amount of voltage in the receiver coil ($=\omega M I_1$) is induced. To reduce the CSI device current stress, the selection of the capacitor, C_t must be such that the reactive component of the transmitter coil current circulates through C_t and inverter devices supply only the active component of current.

The purpose of the series diodes [D_1, D_1', D_2, D_2'] is to prevent short circuit of capacitor, C_t through inverter devices and body diodes of the devices. For example, when device S_1 and S_2' are ON and if the voltage across C_t is negative then C_t will be short circuited through $S_2' - D_2$. However, if the inverter output voltage and current are in same phase then there is no need of these series diodes. But in practice, circuit parameter changes and mutual inductance deviates from designed value. Therefore, power factor deviates from unity. Although, with reverse blocking IGBTs (RV-IGBT), these diodes can be eliminated, but at present RV-IGBTs are mostly under development and lacks in wide range of availability. Thus, this research chooses MOSFET-diode combination to verify the performance of the proposed system.

A series capacitor, C_2 is connected to achieve the desired resonance in receiver coil. Thus, the large voltage drop due to the receiver coil inductance, L_2 is compensated. This *LC* series compensation at the secondary side (receiver) ensures least number of components. This merit is especially applicable when receiver circuitry is placed in moving system such EVs. Finally, diode-bridge rectifies the receiver coil current and charges the battery.

The parallel-parallel compensation topology is also a viable solution for WPT. However, parallel topology in the receiver side suffers from circulating current [41] and this leads to higher copper loss in the receiver coil. Also, parallel compensation on the receiver side leads to inductive filter after the diode bridge rectifier. This will increase on-board charger weight as well needs secondary snubbers to limit ringing and diode voltage stress.

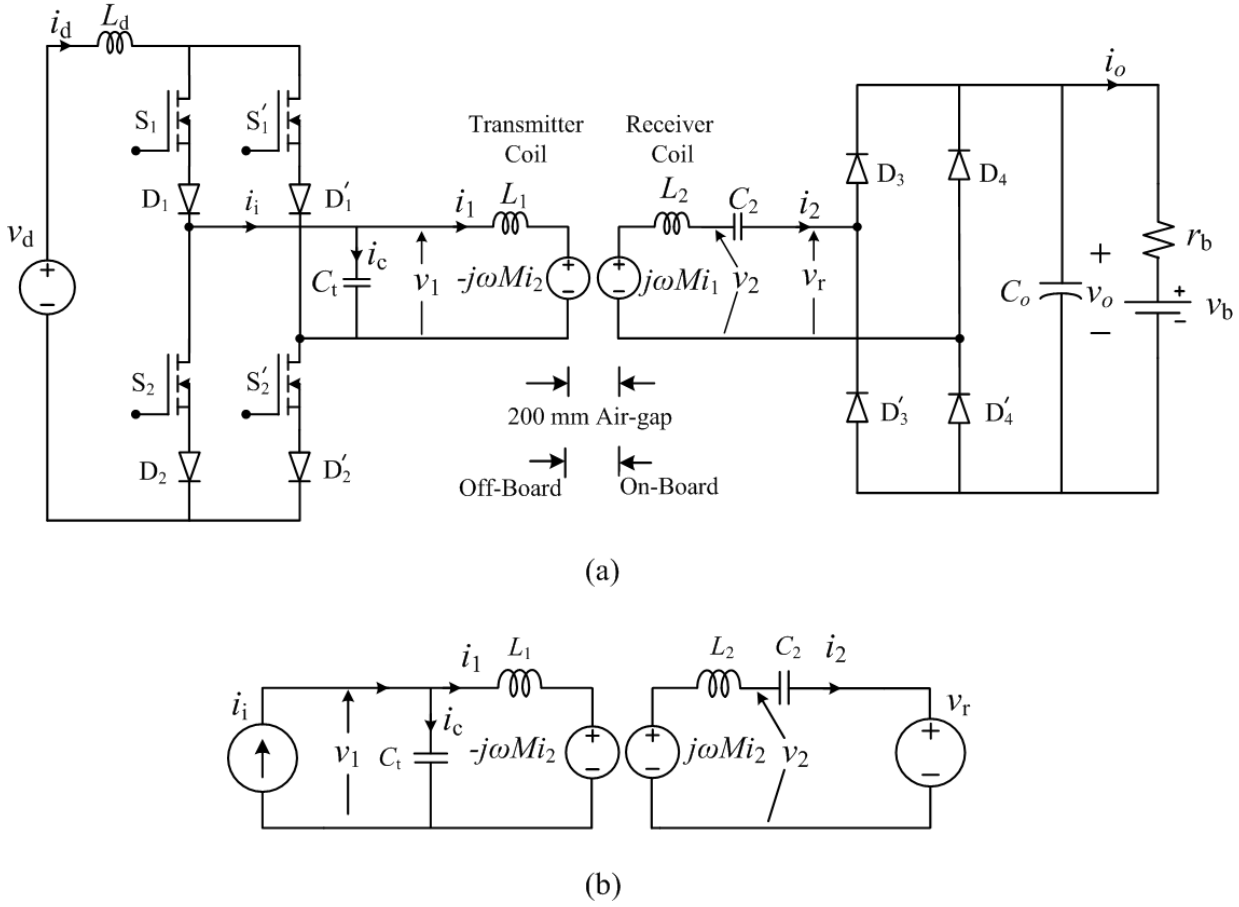


Fig. 2.2 (a) Wireless power transfer (dc-dc conversion) stage using full bridge current-fed converter; (b) ac equivalent circuit of the proposed current-fed WPT.

Referring to Fig. 2.2a when S_1 is ON, current, i_d must get continuous path either through S_2 or S_2'. This is ensured by providing slight overlap between switching signals of S_2 and S_2'. Similarly,

sufficient overlap is maintained between S_1 and S_1' such that current i_d always gets a continuous path [60]. Steady state operation and analysis of the converter is discussed next.

2.3 Steady State Operation

The steady state operation and operating voltage and current waveforms of circuit components for one inverter switching cycle is detailed here. To explain the operation, consider that the power factor at inverter output is leading i.e. voltage, v_1 lags the current, i_i. This is the normal operating condition and it is derived mathematically in the following subsections. This operation ensures soft-switching of all the inverter devices at turn-off.

Interval 1 [t_0 - t_1]: Consider that at time instant t_0, diagonal device pair of the inverter S_1 and S_2' are conducting. During time interval, t_0 to t_1, devices S_1 and S_2' take the complete inverter current and off-diagonal device pair S_1' and S_2' blocks a voltage of same magnitude as inverter output voltage, v_1 as shown in Fig. 2.3a. During time interval t_0 to t_1, the receiver coil current, I_2 is positive and diode pair D_3, D_4' conducts and feeds the output filter capacitor, C_o as shown in the equivalent circuit Fig. 2.3b

Interval 2 [$t_1 - t_2$]: At $t=t_1$, gating signal of device pair S_1' and S_2 becomes high and immediately these devices commutate the device pair S_1 and S_2'. This is because the voltage across S_1' and S_2 is already positive. At this instant, inverter output current, i_i changes polarity but since, the voltage, v_1 lags i_i, the voltage polarity remains same as shown in Fig. 2.3a. A negative voltage with same magnitude as v_1 appears across the device diode pairs (S_1, D_1 and S_2', D_2') and the diodes D_1 and D_2' block this negative voltage as shown in Fig. 2.3a. With the change in inverter current polarity, receiver side diode pair D_3', D_4 are reverse biased and D_3, D_4' start conduction as shown in Fig. 2.3c.

Interval 3 [$t_2 - t_3$]: At time instant t_2, gating signal of device S_1 and S_2' is withdrawn. Consider that the time lag of inverter output voltage v_1 from current i_i is more than the overlap time of the devices. The device pair S_1' and S_2 keep on conducting in the interval t_2 to t_3 and the diode pair D_1 and D_2' continue blocking the negative voltage as shown in the Fig. 2.3a. In this interval rectifier diodes D_3 and D_4' keep on conducting as shown in equivalent circuit Fig. 2.3d.

Interval 4 [$t_3 - t_4$]: At instant t_4 inverter output voltage, v_1 changes polarity. However, devices S_1 and S_2' are already turned-off at time instant t_2. Therefore, S_1' and S_2 keep on conducting and

they take complete inverter current, i_d throughout the interval $t_4 - t_5$. In this interval a positive voltage with same magnitude as inverter output voltage, v_1 appears across the device-diode pairs (S_1, D_1 and S_2', D_2'). Devices S_1 and S_2' block this positive voltage as shown in Fig. 2.3a and Fig. 2.3d. At instant t_4, gating signal of devices S_1 and S_2' becomes high and they immediately take over the complete inverter current. At this point receiver coil current polarity also changes and the rectifier diodes D_3, D_4' on the receiver side come into conduction. The typical voltage and current profiles of different circuit elements for one complete inverter switching cycle is shown in Fig. 2.3a and this repeats in every switching cycle.

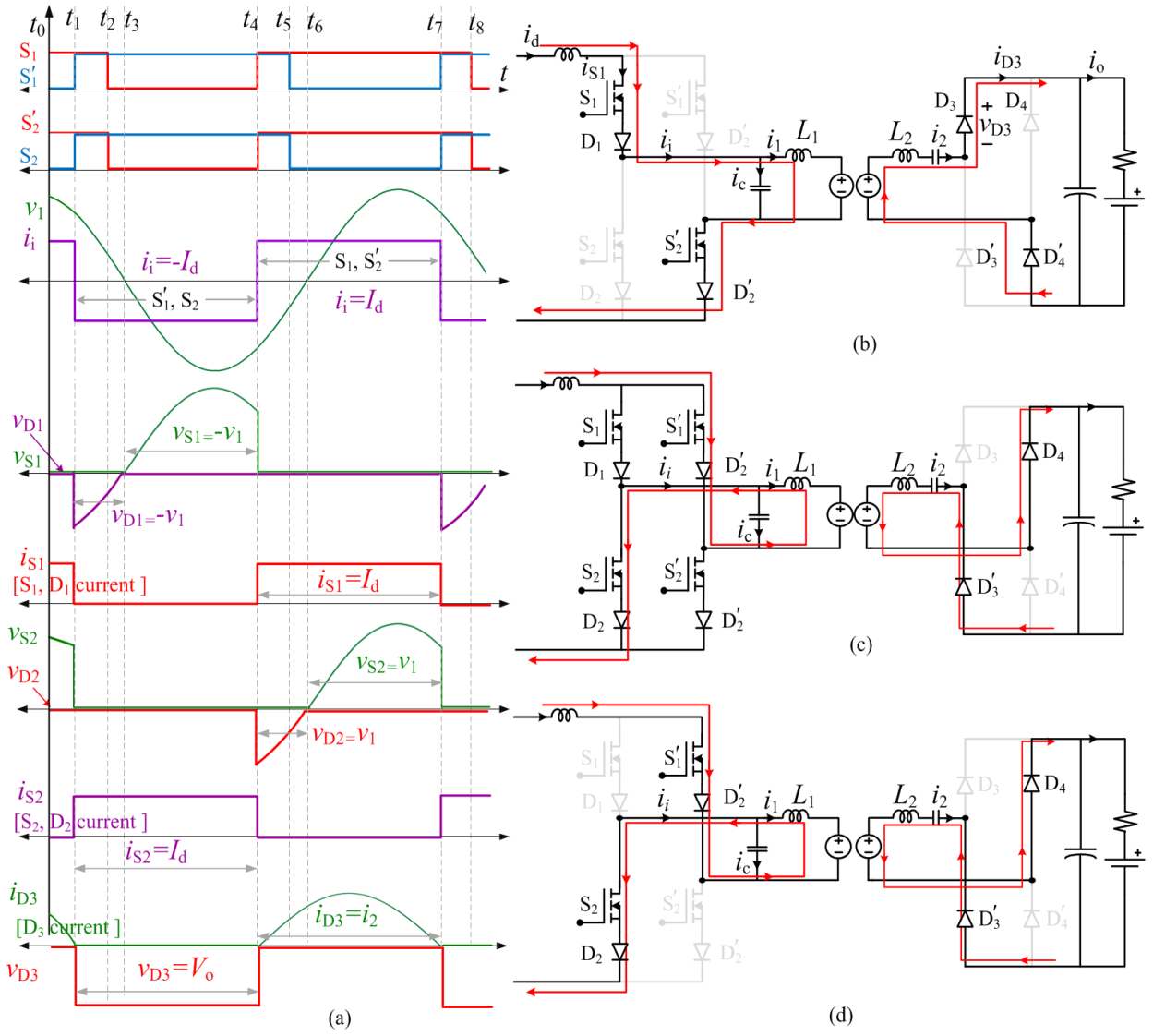


Fig. 2.3 Operating waveforms and corresponding equivalent circuits of the proposed WPT.

2.4 Converter Design

Converter design involves design of compensation capacitors in both the side of the coils to compensate high volume of reactive power consumed by the coils. Also, determination of voltage and current stress of each component for a given input and output specifications are required for proper selection of components.

2.4.1 Selection of Capacitances

The main motivation of adding compensation capacitors in both transmitter and receiver side is to reduce volt-amp (VA) burden of the converters. In this research, the transmitter side compensation ensures least inverter current stress for a given load whereas in the receiver side the compensation provides maximum output voltage.

Applying Kirchhoff's current law (KCL) at inverter output, the inverter current is given as

$$I_{\mathrm{i}} = I_1 + I_{\mathrm{c}}\,, \tag{2.1}$$

where, I_{c} is capacitor C_t current. Replacing the currents with branch voltage and impedance, (2.1) is modified as

$$I_{\mathrm{i}} = \frac{1}{\omega L_1}\left[\omega M I_2 + jV_1(\omega^2 C_{\mathrm{t}} L_1 - 1)\right], \tag{2.2}$$

where, $\omega=2\pi f$ is the frequency of fundamental component, transmitter to receiver coil turns ratio is 1. Due to passive rectification, the rectifier input voltage and currents are in same phase. In this analysis receiver coil current I_2 is considered as reference phasor. From Fig. 2.2a, it is clear that without capacitor, C_{t}, the required high amount of transmitter coil current would pass through CSI devices. The magnitude of CSI output current is minimized by selecting C_{t} such that second part of (2.2) is removed.

In the receiver side, voltage injected at the input of the diode bridge is given as

$$V_{\mathrm{r}} = j\omega M I_1 - I_2\left[j\omega L_2 + \frac{1}{j\omega C_2}\right], \tag{2.3}$$

where, C_2 is receiver side series compensation/resonance capacitor. The value of C_2 is chosen such that voltage, V_{r} is maximum. This is achieved by removing the second part of (2.3). From (2.3) and (2.3) required capacitances are calculated as

$$\omega_{\mathrm{t}} = \frac{1}{\sqrt{C_{\mathrm{t}} L_1}}, \qquad \omega_{\mathrm{r}} = \frac{1}{\sqrt{C_2 L_2}}. \tag{2.4}$$

Effective power transfer is achieved by equalizing inverter switching frequency, ω_{s} (=$2\pi f_{\mathrm{s}}$), transmitter coil resonance frequency, ω_{t} and receiver coil resonance frequency, ω_{r}.

2.4.2 Derivation of Device Voltage and Current Ratings

For simplicity, coil resistance and device losses are neglected which is reasonable since voltage drop across coil is mainly due to inductance. It is clear that the reverse blocking voltage rating of the diodes, D_3, D_4, D_3' and D_4' are the same as battery voltage, V_{b}. The current wave-shape of the receiver coil is sinusoidal since, it passes through the series resonating circuit. Therefore, the peak and RMS current rating of the rectifier diodes are given as

$$\hat{I}_{\mathrm{D}} = \frac{\pi}{4} I_{\mathrm{o}}, \qquad I_{\mathrm{D}} = \frac{\pi}{2\sqrt{2}} I_{\mathrm{o}}, \tag{2.5}$$

where, I_{o} is average battery charging current. Transmitter side device and diode current rating are the same as dc link current, I_{d}. Peak voltage rating of the devices and series diodes are dependent on peak voltage across capacitor, C_{t}. Fig. 2.2b shows ac equivalent of the proposed current-fed WPT circuit. The active load i.e. battery is replaced by its ac equivalent voltage V_{r}. Since, the internal resistance of rechargeable battery is of the order of $m\Omega$ or a fraction of ohm and the voltage drop across it is much less compared with the battery voltage, it is not included in the derivation. Although V_{r} waveshape is square wave but only its fundamental component is involved in active power transfer, since current, I_2 is sinusoidal. Applying power balance and using Fourier analysis, RMS value of equivalent load voltage and receiver coil current are derived as

$$V_{\mathrm{r}} = \frac{2\sqrt{2}}{\pi} V_o, \quad I_2 = \frac{\pi}{2\sqrt{2}} I_o. \tag{2.6}$$

Applying Kirchhoff's voltage law (KVL) in the receiver side loop, transmitter coil current is calculated as

$$I_1 = -j \frac{2\sqrt{2}}{\pi} \frac{V_{\mathrm{o}}}{\omega_{\mathrm{s}} M} + \frac{\pi}{2\sqrt{2}} \frac{I_{\mathrm{o}}}{\omega_{\mathrm{s}} M} \left(\omega_{\mathrm{s}} L_2 - \frac{1}{\omega_{\mathrm{s}} C_2} \right) \tag{2.7}$$

Applying KVL and KCL in transmitter side and using (2.6) and (2.7), RMS value of the fundamental CSI output voltage and current are derived as

$$V_1 = \frac{2\sqrt{2}}{\pi}\left(\frac{L_1}{M}\right)V_o - j\frac{\pi}{2\sqrt{2}}.I_o\left\{\omega_s M - \frac{L_1}{M}\left(\omega_s L_2 - \frac{1}{\omega_s C_2}\right)\right\} \tag{2.8}$$

$$I_i = \frac{\pi}{2\sqrt{2}}I_o\left[\omega_s{}^2 M C_t - \frac{L_1}{M}\omega_s C_t\left(\omega_s L_2 - \frac{1}{\omega_s C_2}\right) + \frac{1}{\omega_s M}\left(\omega_s L_2 - \frac{1}{\omega_s C_2}\right)\right] + j\frac{2\sqrt{2}}{\pi}\frac{V_o}{\omega_s M}(\omega_s{}^2 C_t L_1 - 1) \tag{2.9}$$

From (2.7) and (2.8) it is clear that for a given output voltage and current, transmitter coil will draw more current with lower mutual coupling (M) and this leads to higher voltage across transmitter coil. Also at proper LC tuning i.e. $\omega_s L_2 = \frac{1}{\omega_s C_2}$, (2.8) and (2.9) can be simplified but due to presence of the factor $\frac{L_1}{M}$ this simplification is not done. This is because in a loosely coupled system this factor is generally much greater than unity and a slight mismatch in L-C tuning leads to large mismatch between simplified equations and actual equations. From (2.8) and (2.9), CSI peak device voltage and both peak and RMS current ratings are derived as,

$$\hat{V}_{sw} = \hat{V}_1, \qquad \hat{I}_{sw} = \hat{I}_i. \tag{2.10}$$

2.4.3 Soft-switching of Inverter Devices

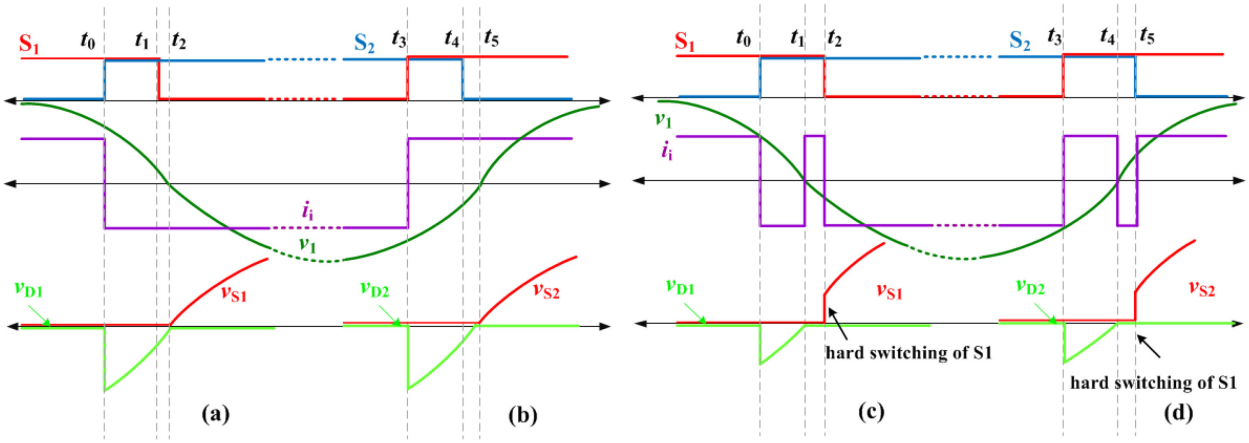


Fig. 2.4 Turn off characteristics **(a)** and **(b)** soft-switching of device S_1 and S_2 **(c)** and **(d)** hard-switching of device S_1 and S_2.

From (2.8) and (2.9), it is clear that inverter output voltage, v_1 lags the current, i_i when LC tuning is perfect. However, if the circuit is not exactly tuned to its resonance frequency then depending upon the parameter values and load, the inverter power factor can be lagging or unity. In the proposed topology, leading and lagging power factor at inverter output enables soft switching of

inverter devices during turn-off and turn-on respectively. Though the turn on loss of a power MOSFT is higher than the turn-off loss but considering the proposed topology is more suitable with RV-IGBT, turn-off soft switching is discussed here.

Fig. 2.4a shows soft-switching of device S_1. At instant t_0, gating signal of S_2 is high and since, the voltage across S_2 is positive before instant t_0, it takes the inverter current. Owing to leading power factor at inverter output, the current changes polarity before the voltage as shown in Fig. 2.4a. During overlap region (t_0 - t_1), device S_1 and diode D_1 together gets negative voltage and the diode blocks this negative voltage as shown in Fig. 2.4a. Considering the power factor angle at inverter output is greater than the switching overlap angle, diode D_1 keeps on blocking negative voltage during the interval (t_0 - t_1). At instant t_1, the gate pulse of device S_1 is withdrawn and S_1 turn-off at zero current. At instant t_2, inverter output voltage polarity reverses and a positive voltage appears across S_1 and D_1. Device S_1 blocks this positive voltage. Similarly, turn-off characteristics of device S_2 is shown in Fig. 2.4b. At instant t_3 diode D_2 blocks the negative voltage and the current through device S_2 becomes zero as shown in Fig. 2.4b. At instant t_4, gate pulse of device S_2 is withdrawn and it turns-off at zero current.

Fig. 2.4c and Fig. 2.4d show the turn-off characteristics of S_1 and S_2 when the soft-switching condition is not maintained. At instant t_1, inverter output voltage changes polarity and a positive voltage appears across device -diode pair S_1-D_1 as shown in Fig. 2.4c. However, the gating signal of device S_1 is still high and S_1 immediately takes inverter current. At instant t_2 gating signal of S_1 become low and it experiences hard turns-off. Because of the sinusoidal profile of the inverter output voltage, this turn-off occurs at lower voltage. Similar characteristics are observed for other devices as shown in Fig. 2.4d. Therefore, in the proposed topology confirmed soft switching is conditional and it occurs near 50% duty cycle and in other points it depends on relative magnitude of inverter output power factor angle and overlap duration of CSI devices.

2.5 IPT Coil Design

Although, this research mainly focuses on designing novel power converter not on coil design, but to verify the converter performance, coil design is an integral part. This section provides a general idea of IPT coil and coil structures and later a suitable coil is selected to verify the performance of proposed converter. The regular 2-winding transformer or coupled inductors

cannot be used here. The IPT coil geometry widely varies from conventional magnetic structures to achieve high coupling inductance with a large airgap. Also, additional design challenges include coil misalignments, especially when one or both coils are in motion.

2.5.1 Selection of Coil

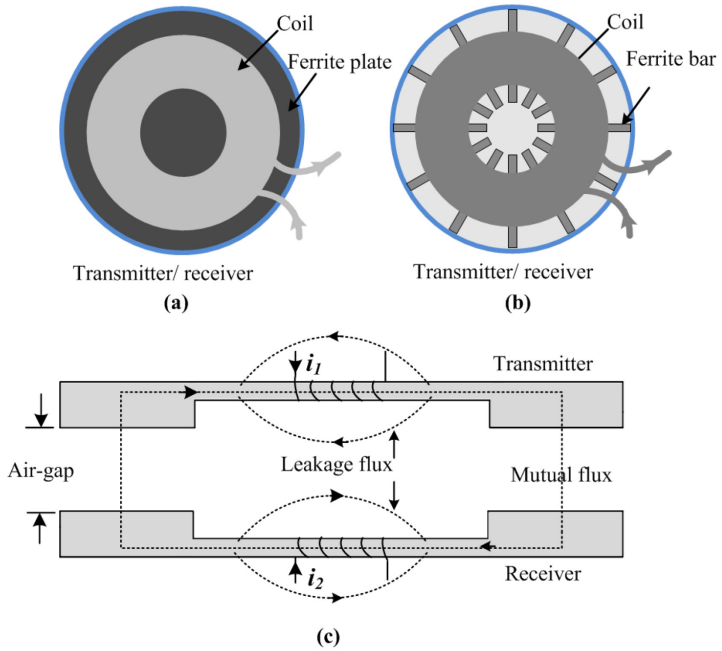


Fig. 2.5 2-D structure and different flux guided IPT pads (a) Circular with solid ferrite core, (b) circular with ferrite bars, and (c) UU type IPT pad

Magnetic coupling is an important factor in designing a wireless IPT system. Generally, IPT pads are classified as IPT pad without ferromagnetic core and IPT pad with ferromagnetic core i.e. IPT pad with flux guided material. Though the IPT pad with ferrite core is comparatively expensive but it has some advantages. The major advantage of having ferrite core is to minimize magnetic field emissions around the coils by reducing the stray or fringe fields because ferrites keep the magnetic field in between the coils. Various types of flux guided IPT pads using ferrite blocks or bar are discussed in [9], [14], [16], [52], [53], [61] - [65]. Fig. 2.5a and Fig. 2.5b show circular IPT pad and Fig. 8c shows a UU type of IPT pad. Fig. 2.5a circular pad is developed with solid ferrite plate where Fig. 2.5b is pad is an improved structure for EV applications. Fig. 2.5b structure is extensively used by University of Auckland and Oak Ridge National Laboratory (ORNL) researchers [14], [52], [66] whereas Fig. 2.5c structure is extensively used both commercially and in research by Korea Advanced Institute of Science and Technology (KAIST) [16]. Detailed

design process of these pads are presented in [16], [52]. In this research, UU type core is selected for its simple structure and easy to implement. This IPT pad is used in the experiment to verify the operation of the proposed topology. The coil design and size optimization of the pads are detailed in [16], [9].

2.5.2 Coil Characteristics

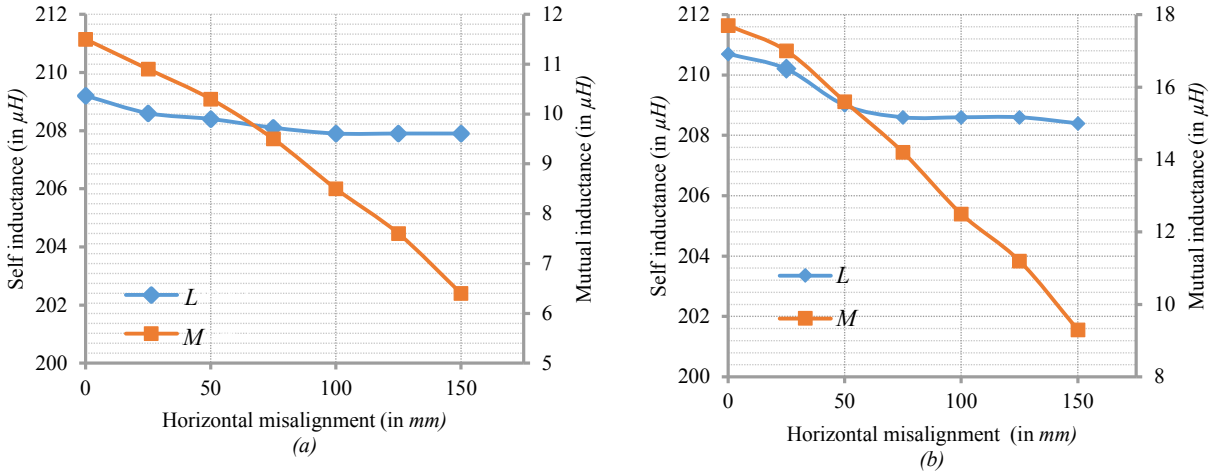


Fig. 2.6 Experimental results: self and mutual inductance of the IPT pad with fixed vertical distance *(a)* 200*mm* *(b)* 150*mm*

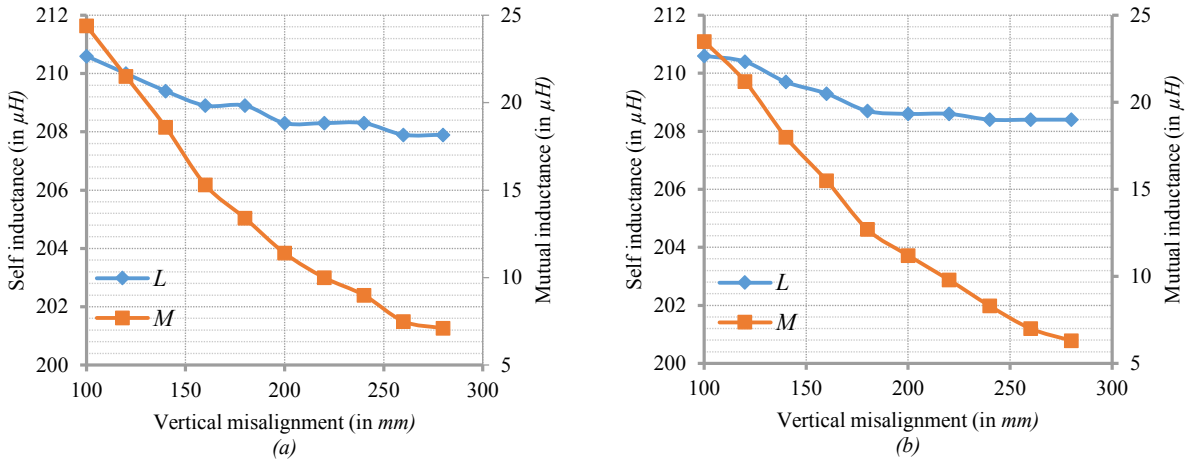


Fig. 2.7 Experimental results: self-inductance and mutual inductance of the IPT pad with fixed horizontal misalignment *(a)* 0 *mm* *(b)* 50 *mm*

Fig. 2.6 shows the variation of self and mutual inductance of the IPT pad when the horizontal misalignment is variable and vertical misalignments are fixed to 200mm [Fig. 2.6a] and 150mm [Fig. 2.6b]. Fig. 2.7 shows the change in self and mutual inductance with varying vertical

misalignment and a fixed horizontal misalignment 0 mm [Fig. 2.7a] and 50mm [Fig. 2.7b]. From these results, it is clearly understood that the change in self-inductance is very slow with change in pad misalignment whereas the change in mutual inductance is much faster. In Fig. 2.5c, the flux generated due to current flow in transmitter coil (TC) have two possible flux paths. One is through transmitter core – air - transmitter core and the other one is through transmitter core – air - receiver core – air - transmitter core. The reluctance of the second parallel flux path increases with the increase in air gap between transmitter and receiver coils (RC) resulting in slight reduction in TC self-inductance. Also, increase in air gap directly leads to increase in reluctance to the mutual flux. Therefore, mutual inductance sharply reduces with increase in air gap. Coil to Coil Efficiency

The predominant loss in these large air gap coils is the copper loss. From TC current and RC current expressions given in (2.6) and (2.7), the copper loss in the coils is calculated as,

$$P_{\mathrm{cu1}} = \frac{8}{\pi^2} \times \left(\frac{V_o}{\omega_s M}\right)^2 r_1 , \tag{2.11}$$

$$P_{\mathrm{cu2}} = \frac{\pi^2}{8} \times {I_o}^2 r_2 , \tag{2.12}$$

where, r_1 and r_2 are transmitter and receiver coil ac resistances, respectively. Using (2.11) and (2.12), the coil-to-coil efficiency is calculated as,

$$\eta_{\mathrm{coil}} = \frac{1}{1 + \frac{8}{\pi^2}\frac{V_o}{I_o(\omega_s M)^2} r_1 + \frac{\pi^2}{8}\frac{I_o}{V_o} r_2} . \tag{2.13}$$

From (2.13), it is clear that coil-to-coil power transfer efficiency increases with increase in impedance due to mutual coupling ($M \times \omega_s$) and reduction in coil ac resistance. For a given system, all parameters in (2.13) other than charging current are known. Therefore, the optimum charging current for maximum coil-to-coil power transfer efficiency and corresponding maximum efficiency are given as,

$$I_{\mathrm{o\,max}} = \frac{8}{\pi^2}\frac{V_o}{M\omega_s}\sqrt{\frac{r_1}{r_2}}, \tag{2.14}$$

$$\eta_{\mathrm{coil\,max}} = \frac{1}{1 + 2\frac{\sqrt{r_1 r_2}}{M\omega_s}} . \tag{2.15}$$

2.6 Simulation Results

The IPT circuit shown in Fig. 2.2a is simulated using PSIM 9.3 to verify the concept, proposed operation, and mathematical analysis. Selected circuit parameter values for the simulation have been listed in Table 2.1. Two sets of simulation results are presented in this section where one set is with the same circuit parameters as 420W lab-prototype and the other set is for a type I charger with 1 *kW* power output [67]. This power level is suitable for solar to EV charging and slow EV charging at residential area (overnight) or official area [67]. For 420W power output the simulation circuit parameters are listed in second column of Table 2.1 and for 1 *kW* the parameters are listed in third column. To control the battery charging current, fixed switching frequency and variable duty cycle control is adopted in the inverter. Details of small signal modelling and closed loop control is reported in Chapter 4.

2.6.1 Comparison with VSI Topology

Table 2.1. Selected circuit parameters

Parameters	Selected Values (for 420W lab prototype)	Selected Values (Proposed topology P_o= 1kW load) [48]	Selected Values (Voltage-fed *LCL* topology P_o= 1kW) [68]
Input DC voltage, v_d	500 *V*	380V	380V
DC link inductor, L_d	4 *mH*	4 *mH*	250 *μH* (output side dc link)
Self-inductance, L_1, L_2	225.8 *μH*, 226.3 *μH*	177 *μH,* 177 *μH*	31 *μH,* 15.5 *μH*
Mutual inductance, *M*	40.9 *μH*	39 *μH* (22% coupling)	4.8 *μH* (22% coupling)
Resonating capacitors, C_t, C_2	47 *nF*, 47 *nF*	228 *nF*, 228 *nF*	1.307 *μF*, 1.69 *μF*
Switching frequency, f_s	46.7 *kHz*	25 *kHz*	25 *kHz*
Battery voltage, v_b	42 *V* DC	100 *V* DC	100 *V* DC
Battery internal resistance,	100 *mΩ*	200 *mΩ*	200 *mΩ*
Output filter capacitor, C_o	350 *μF*	350 *μF*	350 *μF*
Coil turns ratio	1:1	1:1	1:0.7

To verify the suitability of the current-fed topology a comparison is done with a voltage-fed topology based on power loss distribution. In this research voltage-fed inverter with *LCL* transmitter and series *LC* receiver is considered. Although the series (LC) transmitter and (LC) receiver topology requires least component count but because of instability issues reported in [17],

[39], [42] this topology is not considered here. Presence of *LCL* resonant tank after the voltage-fed inverter facilitates soft switching during turn-on of inverter devices [39], [42]. The circuit parameters for *LCL* topology are from [68] and a slight modification of TC to RC turn ratio is done from 1: 0.88 to 1: 0.7 to feed the same 100V battery.

Table 2.2. Comparison of relative loss distribution between proposed topology and voltage-fed *LCL* topology

Parameters	Proposed topology P_o=1kW	Voltage-fed *LCL* topology [68]
Inverter device stress (peak)	582V	380V
Device voltage at switching instant	100V (turn-on)	380V(turn-off)
Device current (rms)	2.0A	5.5 A
Device current at switching	2.9A(turn-on)	23A(turn-off)
Diode current (avg.)	1.36A (series diode)	1.0A (body diode)
Inverter device r_{dson}	$65m\Omega$	$30m\Omega$
Switching loss (4 devices)	1.0W	2.8W
Conduction loss (4 devices)	2.0W	3.6W
Conduction loss (4 diodes)	7.6W (series diode)	3.6W (body diode)
Rectifier side Diode loss (4 diodes)	12W	12W
Dc inductor loss	7.0W (source side)	4.2W (load side)
Tank inductor (*LCL*) loss	-	3.4W
Total converter loss	28.8W	29.2
Loss in power electronics (w.r.t. P_o)	**2.8%**	**2.9%**
Total cost of devices and diodes	$ 80.75	$ 64.16

Table 2.3. Component part list

Circuit Configuration	Component	Part No.	Manufacturer	Rating
Proposed converter, P_o=1 kW	MOSFET	C3M0065090J	Cree Inc.	900 V, 35 A, 65mΩμ, t_r=25nS
	Series Diode	C4D10120E	Cree Inc.	1200 V, 16A, 1.8V @ 10A, Schottky
	Diode[for rec.]	APT30S20BG	Microsemi Power	45A, 200V, 850mV @ 30A, Fast recovery
	Input DC Inductor	1140-392K-RC	Bourns Inc.	3.9mH, 2.8A, 0.845 Ω
Voltage-fed *LCL* topology P_o=1 kW	MOSFET	IXFK100N65X2	IXYS	650 V, 100 A, 30mΩ, t_fΩ=13nS
	Diode[for rec.]	APT30S20BG	Microsemi Power	45A, 200V, 850mV @ 30A, Fast recovery
	AC inductor [LCL tank]	60A313C	Murata Power Inc	31.4μH, 9.5A, 18mΩ
	DC Inductor [filter]	-	-	200μH, equivalent resistance =0.21 Ω

Table 2.2 lists estimated loss of each component for both proposed topology and voltage fed *LCL* topology for 1*k*W load power. For the comparison, selected circuit component part numbers and brief specification are listed Table 2.3. For simplicity capacitor ESR loss and core loss of inductors are neglected. The voltage rating of VSI devices are same as dc link voltage whereas in current fed topology this is decided by TC side tank capacitors. The current rating of VSI devices are decided by tank input current whereas in current fed topology it is decided by DC inductor current. The RMS current rating of the VSI devices is significantly higher than the proposed topology due highly non-sinusoidal current drawn by the *LCL* tank [67], [68], [42]. VSI devices experience ZVS turn-on but their turn off occurs with significantly higher current with full DC link voltage. In the proposed topology, the devices experience soft turn-off and their turn-on occurs at a voltage much lower than the peak voltage due sinusoidal profile of inverter output voltage. Therefore, the switching loss of VSI topology is slightly higher (f_s=*25k*Hz). In current-fed topology power loss in the inverter side series diodes is significantly higher due to higher average current, compared with the body diode in VSI topology. The estimated overall power converter loss for both the topologies are almost same but due to extra series diode used in current fed topology the total cost of mosfets and diodes are higher. However, in near future suitable reverse blocking IGBTs (RV-IGBT) can eliminate this drawback of the proposed topology. With the inclusion of capacitor ESR loss and inductor core loss, overall converter loss in these topologies will be slightly higher. Considering TC and RC coil loss around 6-7%, the overall power transfer efficiency of DC-DC stage at rated load is around 90%.

2.6.2 SteadyState Results

Fig. 2.8a shows steady state voltage and current waveforms of transmitter and receiver coils for 420W power transfer and Fig. 2.8b shows results for 1 *k*W power. Equations (2.6) and (2.7) show that transmitter coil current, i_1 lags receiver coil current, i_2 by 90^0 and this verifies (2.8). With the given simulation parameters and with 18% coupling, calculated RMS value of v_1 is 551V for 420W power output. Simulation result also gives same value of v_1. From Fig. 2.8a and Fig. 2.8b it is clear that the transmitter coil voltage and current waveforms are very close to sinusoidal. It is because the parallel capacitor, C_t provides much lesser impedance to higher order harmonic currents than transmitter coil; therefore, the coil predominantly receives fundamental component.

Fig. 2.8c and Fig. 2.8d shows steady state results of dc input voltage and current, dc output voltage and current, and bridge rectifier input voltage and current for 420W and 1kW power output respectively. From these figures, it is clear that bridge rectifier input voltage changes polarity when current crosses zero. Therefore, soft commutation and soft recovery of rectifier diodes are achieved resulting in reduced losses.

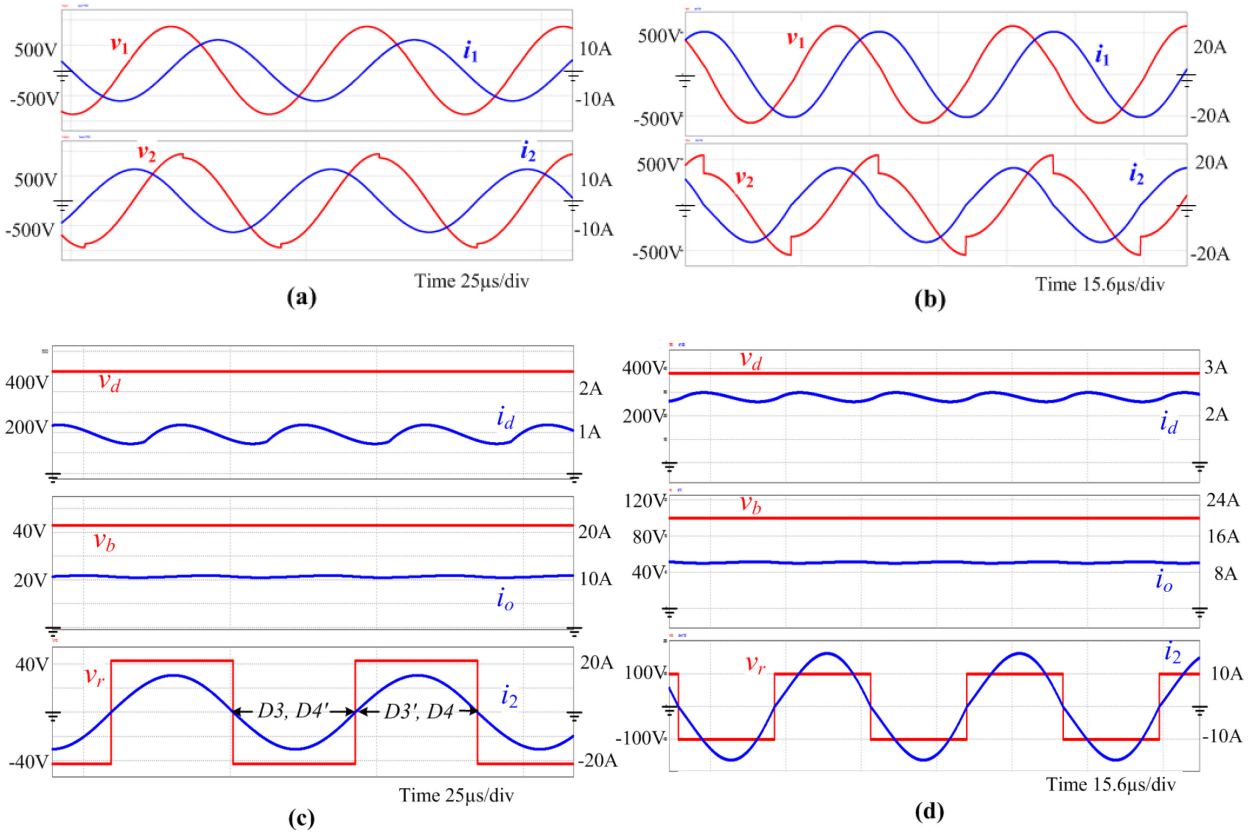


Fig. 2.8 Steady state simulation results:

Transmitter coil voltage, v_1 current, i_1 and Receiver coil voltage, v_2 and current, i_2 for (a) 420W and (b) 1 kW power output;

Input dc voltage, v_d current, i_d output voltage, v_b and current, i_o diode bridge rectifier input voltage, v_r and current, i_d for (a) 420W and (b) 1 kW power output

Fig. 2.9 shows the simulation results demonstrating soft switching of CSI devices. From Fig. 2.9, it is clear that CSI output voltage lags the fundamental component of inverter current. It validates the mathematical analysis given in (2.8) and (2.9). The series diode D_1 blocks the negative voltage before the gate pulse of S_1 is turned-off. This allows the device S_1 to turn-off at zero current. Similarly, other devices also turn-off while the current through the corresponding

devices are zero. Simulation waveforms match closely with the theoretically predicted waveforms and verifies the proposed analysis.

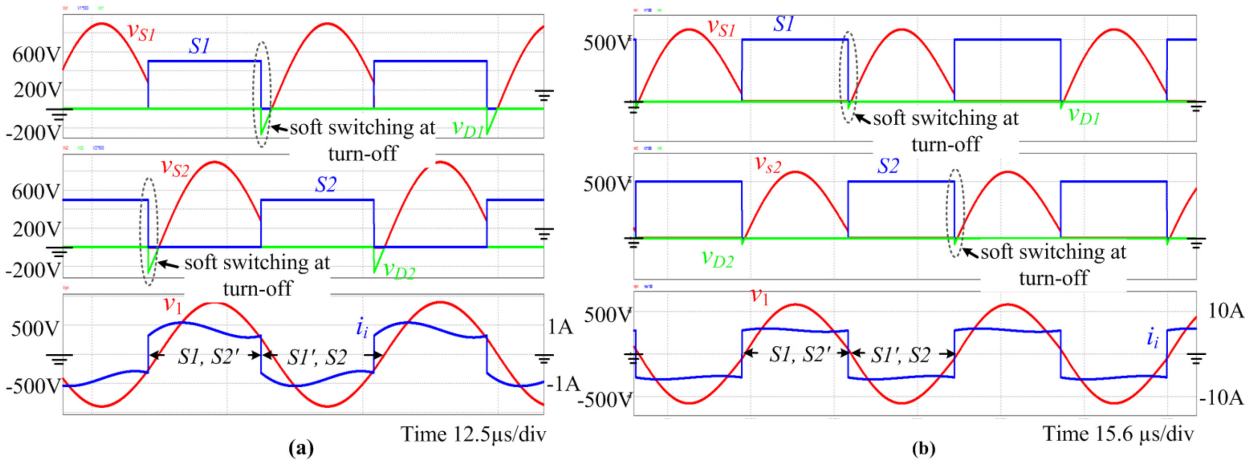


Fig. 2.9 Soft switching at device turn-off: Gate pulse of device S_1, voltage across S_1, v_{S1} and Diode D_1, v_{D1}; Gate pulse of device S_2, voltage across S_2, v_{S2} and Diode D_2, v_{D2}; inverter output voltage, v_1 and current, i_1 for(a) 420W and (b) 1 kW power output.

2.7 Experimental Results

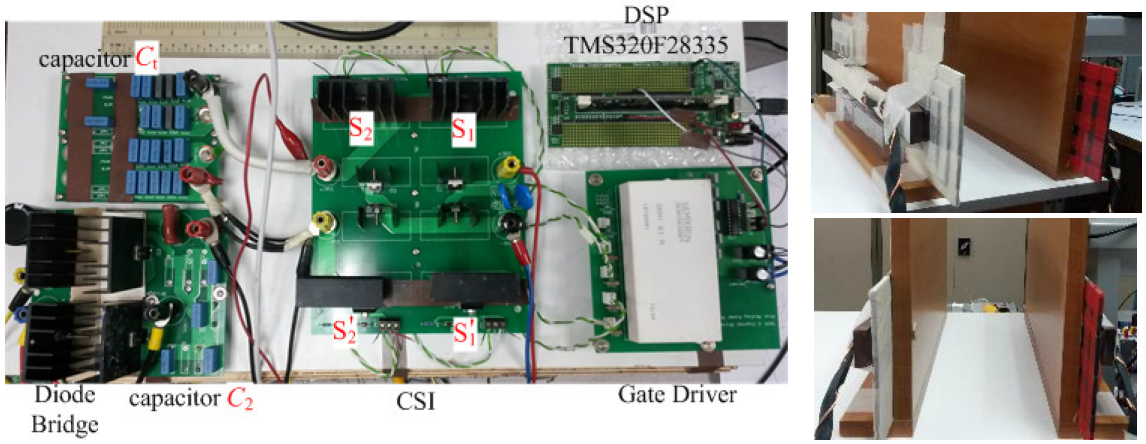
2.7.1 420W Experimental Set-up

A proof-of-concept laboratory prototype rated at 420W is developed to demonstrate and evaluate the concept and performance of current-fed IPT system. Fig. 2.10a shows the experimental set-up. DSP TMS320F28335 is used as digital control platform and SKHI 61 (R) is used to generate the gating pulses for the devices. SiC MOSFET SCT2160KEC [1200V, 22A] is selected for inverter devices. Inverter series diodes are DSEP29-12A [1200V, 15A]. Schottky diodes DSS60-0045B [45V, 30A] are selected for rectifier side diodes. Transmitter and receiver side resonating capacitors (C_t and C_2) are EPCOS 700V RMS ac film capacitors. $10nF$ and $1nF$ capacitors are connected in parallel to realize the required capacitances. The parameter values of the hardware circuit are listed in Table 2.1. Two sets of experimental results with different coefficient of coil coupling are presented in this section.

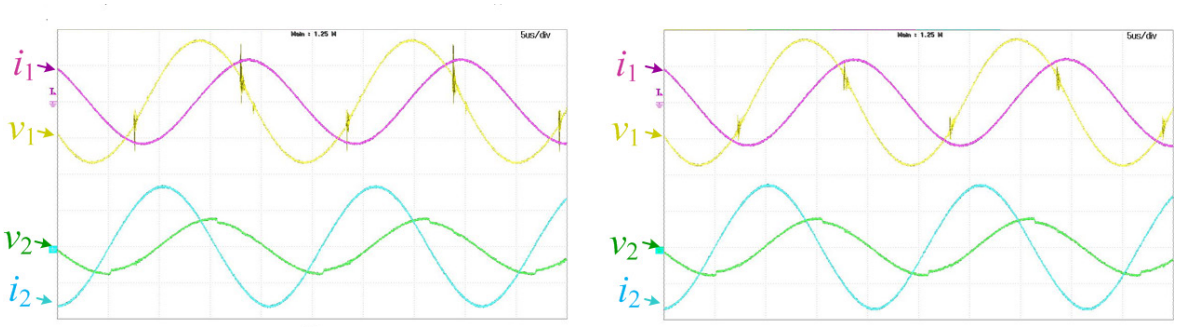
2.7.2 Steady State Results

Fig. 2.10b shows steady-state voltage and current waveforms of transmitter and receiver coils when power output is 420W, battery voltage (V_b) =42V, coefficient of coupling (k) = 18% and

operating duty cycle (D) =0.52. Fig. 2.10b it is clear that transmitter coil current, i_1 lags receiver coil current, i_2 approximately by 90^0 as predicted the same from simulation results. Experimentally measured RMS value of transmitter coil voltage is 560V which is very close to simulation result (551V). This deviation is due to error in parameter measurement and assumption of zero coil resistance. Also, experimentally obtained voltage and current profiles of transmitter coil are almost pure sinusoidal as expected from the analysis and simulation. The measured efficiency of complete dc-dc power transfer stage is around 90% with co-efficient of coupling 18%. The TC to RC power loss (coil-to-coil) is around 6% and other components including device and diode losses are around 4%. Fig. 2.10c shows the experimental results of transmitter coil and receiver coil voltages and currents with k=15%, P_o=420W, V_b=42V and D=0.6. The measured efficiency of the prototype is around 86% at this operating condition.



(a)



(b) (c)

Fig. 2.10 Experimental results: (a) Photograph of experimental set-up with transmitter and receiver coils (bottom) with two different views 200mm apart;

Steady state waveforms of transmitter coil voltage, v_1 [500v/div] current, i_1 [10A/div] and Receiver coil voltage, v_2 [1.0 kv/div] and current, i_2 [10A/div] with IPT pad coupling (b) 18% and (c) 15%.

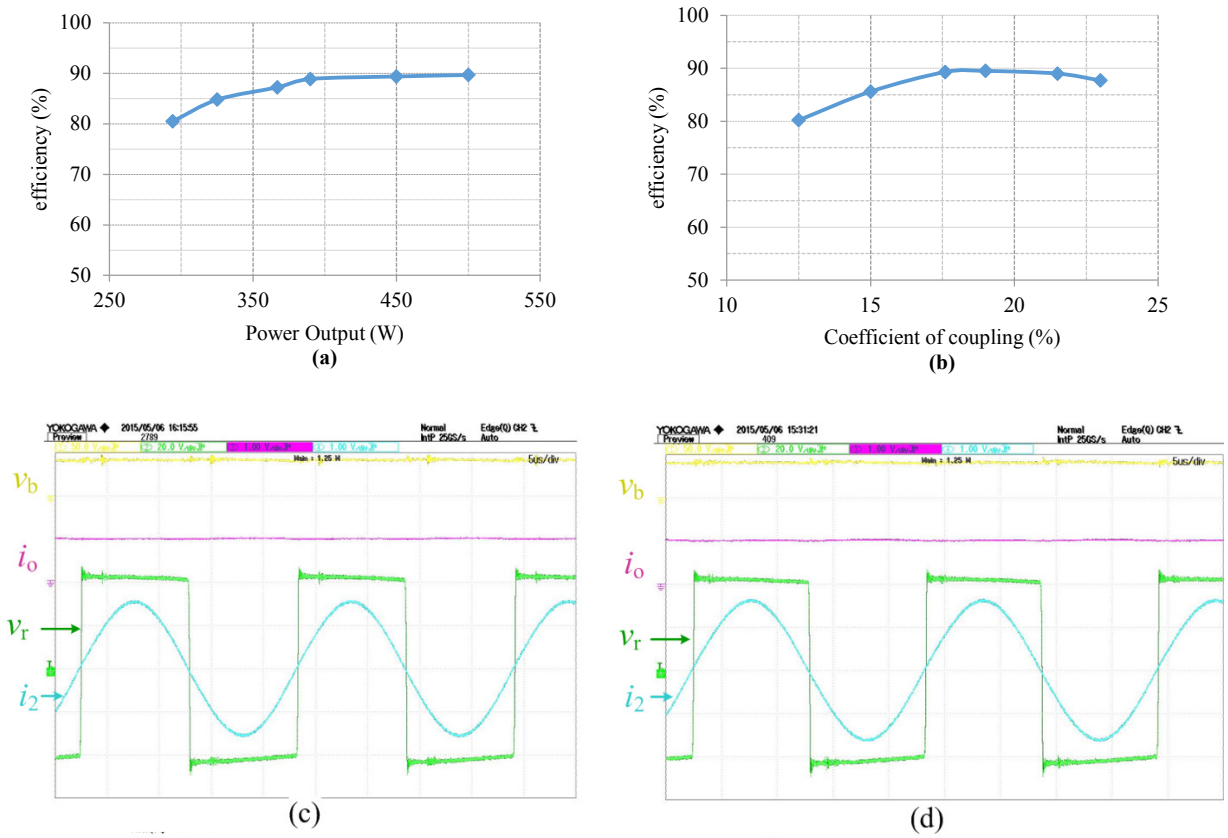


Fig. 2.11 Experimental results: (a) Change in dc-dc stage efficiency under varying power output (fixed coupling=18%) (b) varying coefficient of coupling (fixed output power =420W);

Steady state waveforms: output voltage, v_b [50 V/div], charging current, i_o [10 A/div]; diode bridge rectifier input voltage, v_r [20 V/div] and current, i_d [10 A/div] with IPT pad coefficient of coupling (c) 18% and (d) 15%.

Fig. 2.11a shows efficiency characteristics of the proposed WPT system at coupling factor of 18%. The maximum efficiency of the dc-dc power conversion stage is close to 90%. Fig. 2.11b shows plot of experimentally obtained efficiency verses coefficient of coupling of the coils at 420W fixed power output. From Fig. 2.11b, it is clear that efficiency increases with increase in coefficient of coupling. However, efficiency drops after an operating point where capacitors exactly compensate the required reactive power of the coils due to of over compensation.

Fig. 2.11c and Fig. 2.11d show dc output voltage, output current and bridge rectifier ac input voltage and current when coupling factors are 18% and 15% and inverter duty cycles are 0.52 and 0.6, respectively. These results show that the current-fed topology is also a viable alternative solution for WPT. Also, the soft-commutation and soft-recovery characteristics of the diode bridge

are similar to the simulation results and confirm the minimum reverse recovery loss of the rectifier diodes.

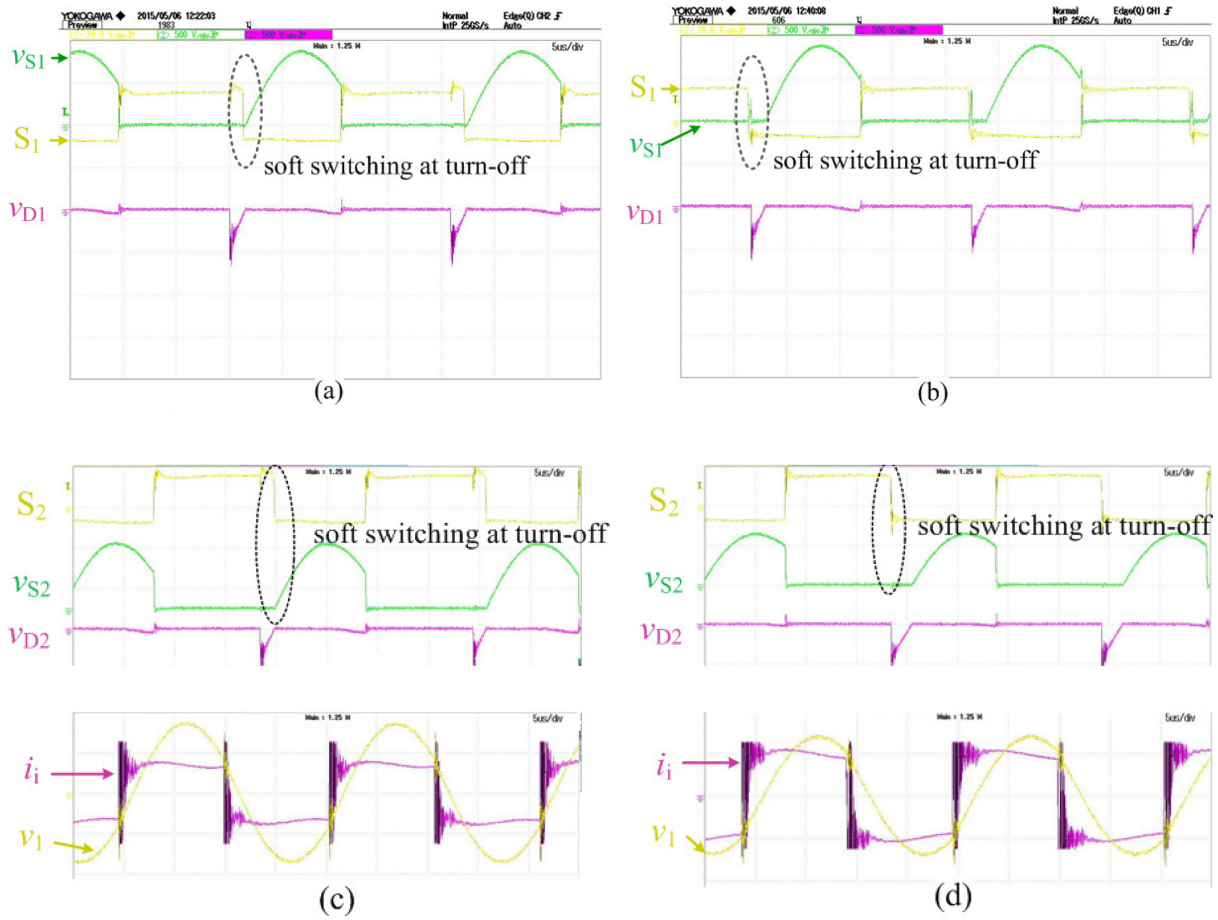


Fig. 2.12 Soft switching at device turn-off: Gate pulse of device S_1, voltage across the device, v_{S1} [200 V/div] and Diode D_1, v_{D1} [200 V/div] with IPT pad coefficient of coupling (a) 15% (b) 18%;

Gate pulse of device S_2, voltage across the device, v_{S1} [200 V/div], Diode D_1, v_{D1} [200 V/div] and Relative phase information of inverter output voltage, v_1 [500 V/div] and current, i_i [100 mV/A] with IPT pad coefficient of coupling (c) 15% (d) 18%

Fig. 2.12a and Fig. 2.12b show soft-switching characteristics of device S_1 for two different misalignments of IPT pads. Fig. 2.12c and Fig. 2.12d show soft-switching characteristics of device S_2 and the voltage and current waveforms at the output of the inverter. Clearly, the inverter output power factor is leading and this is suitable for zero-current turn-off of inverter devices. The series diode D_1 blocks the negative voltage before the gate pulse of S_1 is withdrawn. This leads to zero-current turn-off of device S_1 as shown in Fig. 2.12a and Fig. 2.12b. The same characteristics is observed for device S_2 as shown in Fig. 2.12c and Fig. 2.12d. Therefore, the experimental results

validate the analytical results of zero-current turn-off of devices. Similar characteristics of other inverter devices are observed during experiment. These results confirm the operation and analysis of the proposed topology.

2.8 Conclusions

A new IPT topology using H-bridge current source inverter is studied and analyzed. It is suitable for solar-to-vehicle (S2V), opportunistic charging, and single-phase residential slow charging. This current-fed topology provides an alternative solution of wireless power transfer along with existing voltage-fed topology. The current profile of both the coils are very close to sinusoidal. Input inductor limits the short circuit current during inverter fault and peak current through the semiconductor devices. The topology achieves soft-switching of all semiconductor devices. Design and hardware implementation of the proposed system is demonstrated to evaluate the proposal. The maximum efficiency of complete dc-dc stage obtained from the laboratory prototype is around 90% with co-efficient of coupling of the coupled inductor 18%. Mathematical analysis is verified with the simulation results and shows that the required high transmitter coil current is supplied by resonating capacitor. Therefore, the current stress of CSI devices is limited to peak dc inductor current which is a key benefit of this topology. Complete mathematical analysis, design, and simulation results are reported. In Some applications, the extra dc inductor may not be a preferred choice. However, in an application where the stiff dc current is readily available viz. solar output, there this topology along with the RV-IGBTs as inverter devices can be more advantageous.

Chapter 3 H-bridge Current-Fed IPT Topology with (*C*)(*LC*) Transmitter and (*LC*) Receiver Tank

3.1 Introduction

Although, the IPT topology with parallel *LC* tank at transmitter side have several merits, but it is not suitable for higher power applications due to high voltage stress on inverter devices. Referring to the general power circuit of a parallel compensated IPT topology shown in Fig. 3.1, the capacitor, C_t alone provides the high volume of reactive power consumed by TC. This leads to higher voltage stress on C_t. Clearly, the current-source inverter devices experience this voltage directly. This higher voltage stress is especially prominent when the coils consume higher reactive power. This situation arises when TC to RC coupling is weaker and required power output is higher. This chapter is focused to study these demerits of the parallel *LC* tank at transmitter side, and thereby looking for possible solutions to make it practical.

The IPT coils can be viewed as a two-winding transformer which has high leakage inductance and very low magnetizing inductance compared with the regular iron-core transformers. Clearly, in Fig. 3.1, the parallel capacitor helps to increase the effective magnetizing impedance and also feeds required reactive power consumed by leakage impedance. However, an additional capacitor can be connected in series with the TC to reduce the effective leakage impedance of TC. Therefore, a part of the reactive power will be delivered by series capacitor and remaining part will be supplied by parallel capacitor. This leads to lower voltage stress of inverter devices, thereby making the converter circuit suitable for higher power applications. Also, this series capacitor improves overall voltage gain compared with the topology with only parallel compensation.

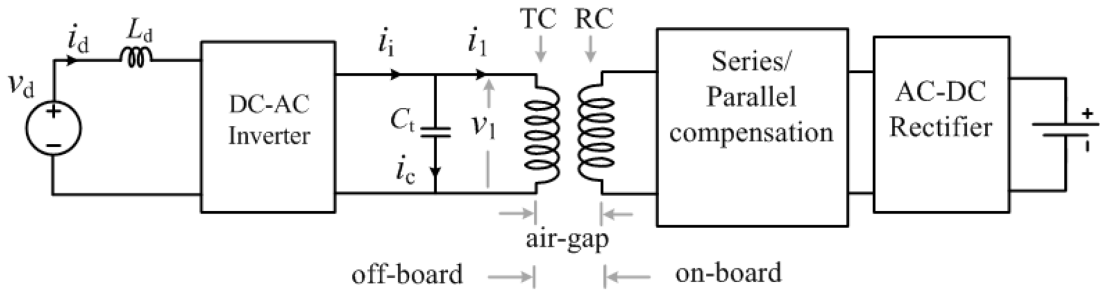


Fig. 3.1 A typical IPT circuit with parallel compensated transmitter

3.2 Proposed IPT Circuit with Lower Voltage Stress of CSI Devices

Fig. 3.2 shows the complete circuit diagram of the improved current-fed IPT topology. The input dc voltage, v_d can be either a dc supply mains or the output of a power factor corrected (PFC) rectifier. To convert this dc to high frequency ac, a full-bridge current-source inverter (CSI) topology is used where the inductor, L_d transforms stiff voltage, v_d to stiff current, i_d. Considering the switching frequency of CSI is sufficiently high and the inductor, L_d is sufficiently large, the CSI injects a square wave current, I_i to next transmitter resonant network stage.

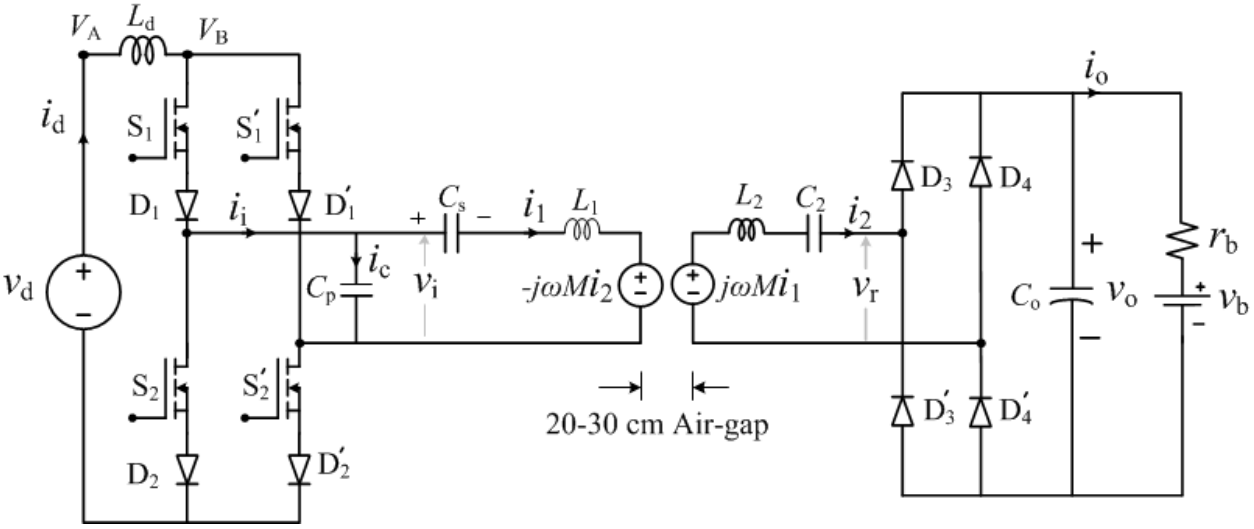


Fig. 3.2 Proposed Wireless Inductive Power Transfer (WIPT) circuit using current-fed converter

In this topology a capacitor, C_s is added in series with the transmitter coil to reduce the effective leakage impedance of transmitter coil. Therefore, parallel capacitor, C_p delivers only a fraction of reactive power consumed by transmitter coil. To reduce the current stress of CSI devices, the selection of C_p and C_s should to be such that the reactive component of the transmitter coil current circulates through C_p, and CSI devices supply only the active component of current.

The RC side compensation is chosen to be series type to ensure least number of components in the secondary side. This is very suitable for EV application because RC side circuitry is placed onboard.

A bipolar pulse width modulation (PWM) scheme is chosen for the inverter devices—i.e., the diagonal pair devices S_1 and S_2', receive identical gating signals. Similarly, other diagonal pair devices S_2 and S_1' are triggered by identical gating signals. An overlap between the two gating

signals is required such that the dc link inductor never gets open. The key message is that all four devices cannot be OFF at a time. Only one diagonal pair is turned-off at a time to pass the current from source to the coils, otherwise all 4 devices are ON during overlap allowing the inductor to store the energy. It is similar to boost converter principle. Referring to Fig. 3.2, when switching signal S_1 is high, inductor, L_d always gets a continuous path irrespective of the status of S_2. Similarly, when S_1 is low i.e. S_1' is high, L_d always gets a continuous path. Similar modulation schemes for CSI topologies are used in [60]. Steady state operation, calculation of circuit parameters and the voltage and current stress of the components are derived in the following sections.

3.3 Steady State Operation

This section reports steady state operation of the proposed converter for one complete inverter switching cycle. A typical gating signals of inverter devices, followed by voltage and currents of circuit elements are shown in Fig. 3.3 and corresponding equivalent converter circuits are shown in Fig. 3.4.

Interval 1 [t_0 - t_1- t_2]: Consider that at time instant t_0, diagonal device pair of the inverter, S_1 and S_2' are in conduction. Also, assume that the inverter output voltage, V_i leads the current, I_i. During time interval t_0 to t_1, devices S_1 and S_2' take the complete inverter current and off-diagonal device pair S_1' and S_2 blocks a voltage with same magnitude as inverter output voltage, V_i as shown in Fig. 3.3. In the receiver side, the RC current, I_2 is positive during the interval t_0 to t_1; therefore, diode pair D_3- D_4' conducts and feeds the output filter capacitor, C_o as shown in equivalent circuit Fig. 3.4a. At time instant t_2, receiver coil current, I_2 changes its polarity and diode pair D_3' - D_4 comes into conduction as shown in Fig. 3.4b equivalent circuit.

Interval 2 [t_2 – t_3- t_4]: At time instant t_2 inverter output voltage, V_i changes polarity before the I_i, because the operating power factor at inverter output is lagging. At time instant t_3, gating signal of devices S_1' and S_2 become high. However, since the voltage across these devices are negative, the devices S_1 and S_2' keeps on conducting as shown in Fig. 3.4b. A negative voltage with same magnitude as V_i appears across the device-diode pairs (S_1'- D_1' and S_2- D_2) and the diodes D_1' and D_2 block this negative voltage as shown in Fig. 3.3 and Fig. 3.4b. Throughout the time interval t_2 to t_4, receiver side diode pair D_3', D_4 conducts as shown in Fig. 3.4b.

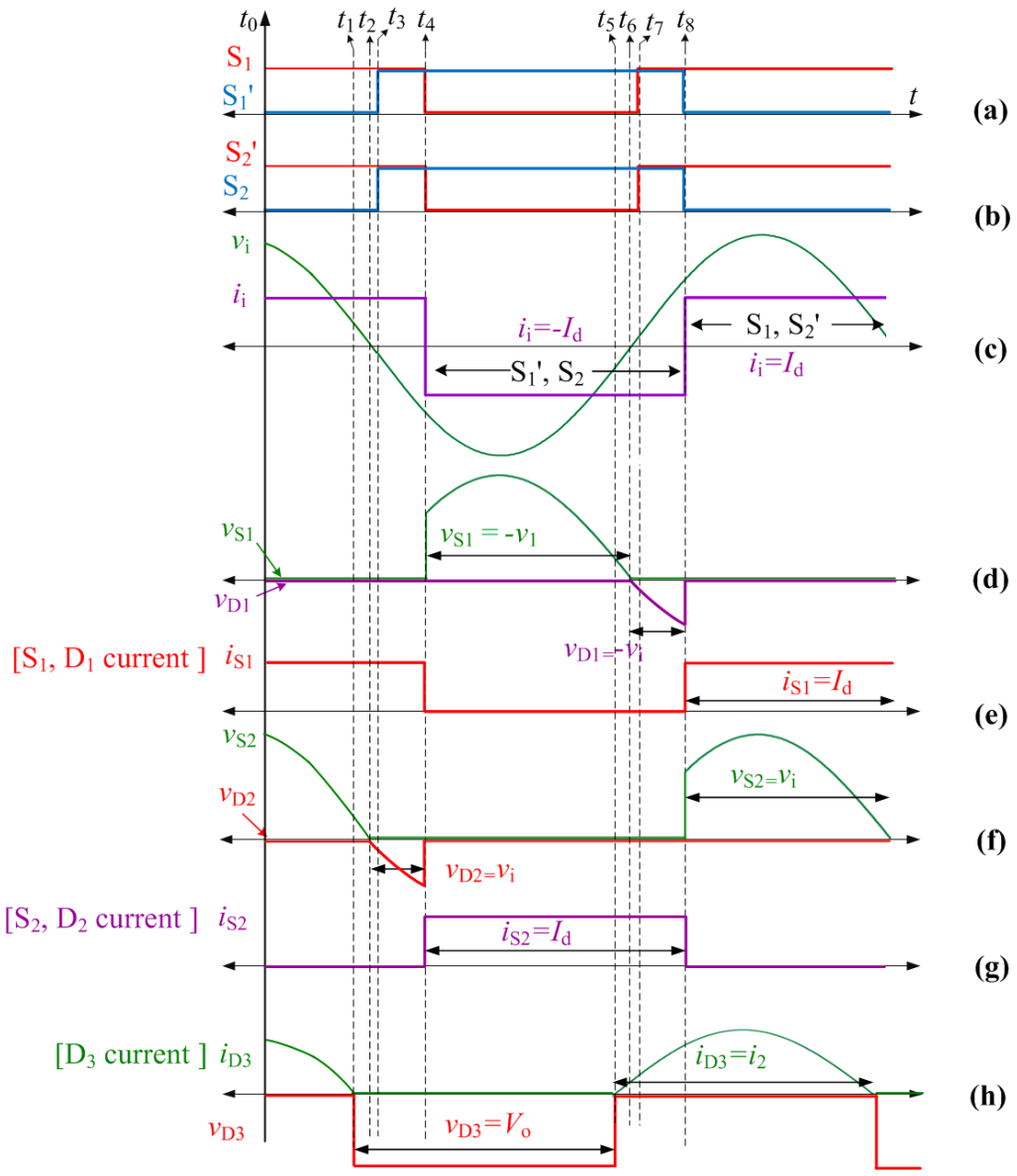


Fig. 3.3 Operating waveforms of the proposed WPT, as shown in Fig. 3.2

Interval 3 [t_4 – t_5]: At time instant t_4 gating signal of devices S_1 and S_2' are removed and immediately devices S_1' and S_2 take the inverter current. Clearly, to achieve zero voltage switching of the inverter devices, the time lag of inverter current I_i from voltage V_i has to be equal or more than the overlap duration of the devices. S_1' and S_2 keep on conducting in the interval t_4 to t_5, where the devices S_1 and S_2' block the positive voltage as shown in the Fig. 3.3 and Fig. 3.4c. During this interval bridge rectifier diodes D_3' and D_4 in the receiver side keep on conducting as shown Fig. 3.4c.

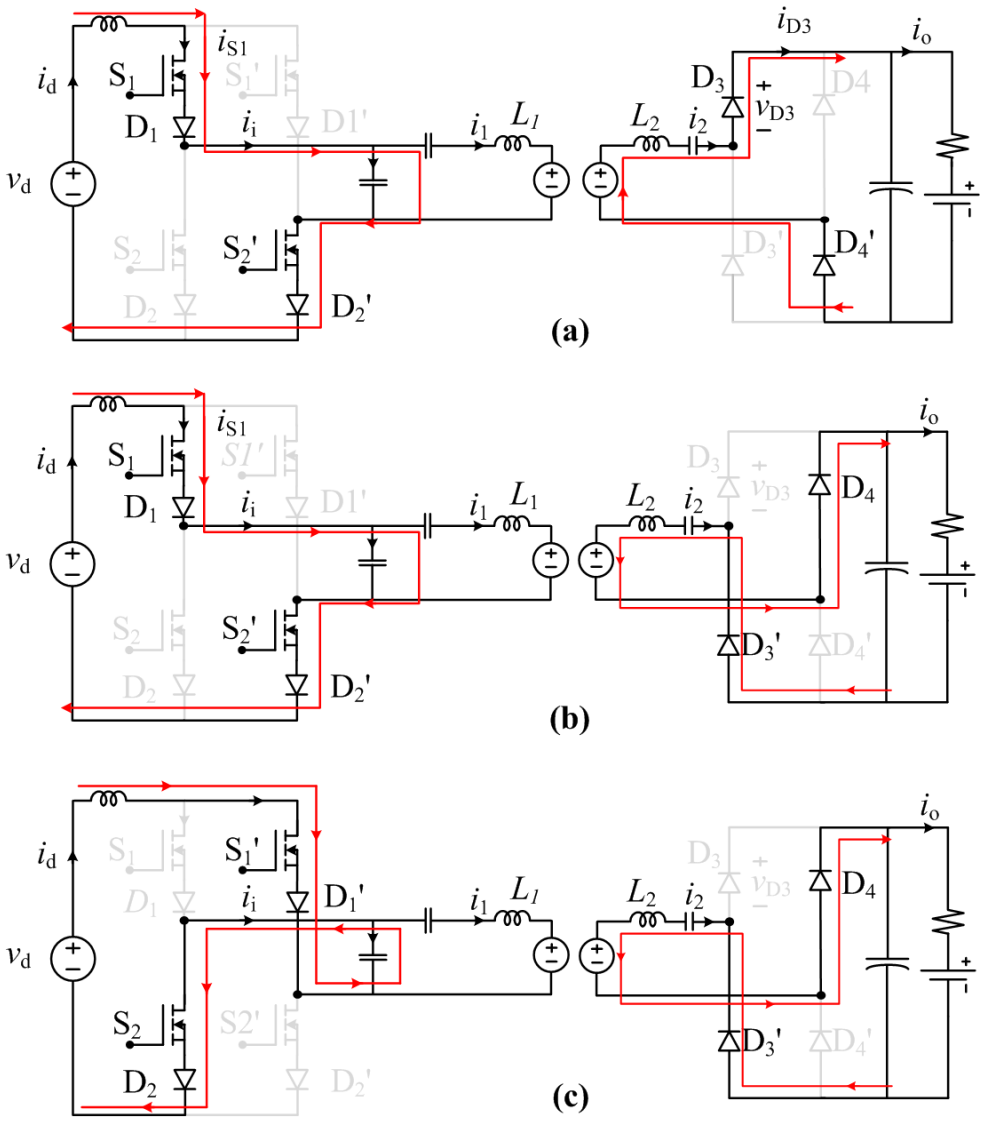


Fig. 3.4 Equivalent circuits during different intervals of operation of the proposed converter for the waveforms shown in Fig. 3.3.

Interval 4 [$t_5 - t_6 - t_7 - t_8$]: At instant t_5 receiver coil current, I_2 polarity changes and diode pair D_3- D_4' starts conducting as shown Fig. 3.4a. At instant t_6 inverter output voltage, V_i polarity changes and the voltage across S_1- D_1 and S_2'- D_2' becomes negative. At instant t_7 device pair S_1 - S_2' are triggered but due to negative voltage across S_1- D_1 and S_2'- D_2', the device pair S_1' - S_2 keeps on conducting. At instant t_8 gating signal of S_1' and S_2 are removed and S_1 and S_2' are forced to take the inverter current and this repeats in every switching cycle.

3.4 Converter design

3.4.1 Design of Compensation Capacitors

Applying Kirchhoff's current law (KCL) at inverter output, the inverter current is given as

$$I_{\mathrm{i}} = I_1 + I_{\mathrm{c}}\,, \qquad (3.1)$$

where, I_1 is transmitter coil current and I_{c} is capacitor, C_{p} current. Replacing these currents with their respective branch voltages and impedances, (3.1) is modified as

$$I_{\mathrm{i}} = \left[\frac{V_{\mathrm{i}} + j\omega M\, I_2}{j\omega L_1 + \frac{1}{j\omega C_{\mathrm{s}}}}\right] + j\omega C_{\mathrm{p}} V_{\mathrm{i}} = \left[\frac{\omega^2 M C_{\mathrm{s}} I_2}{(\omega^2 L_1 C_{\mathrm{s}} - 1)}\right] + j\left[\omega V_{\mathrm{i}}\left(C_{\mathrm{p}} - \frac{C_{\mathrm{s}}}{(\omega^2 L_1 C_{\mathrm{s}} - 1)}\right)\right] \qquad (3.2)$$

where, L_1 is self-inductance of TC; ω is the angular frequency of fundamental component; M is mutual inductance and TC to RC turns ratio is 1:1. From Fig. 3.2 it is clear that without parallel capacitor, C_{p}, the required high amount of TC current would pass through CSI devices. The magnitude of CSI output current is minimized by selecting C_{p} and C_{s} such that the complex part of (3.2) is eliminated.

On the receiver side, voltage injected at the input of the diode bridge is given as

$$V_{\mathrm{r}} = j\omega M I_1 - I_2[j\omega L_2 + \frac{1}{j\omega C_2}] \qquad (3.3)$$

where, C_2 is receiver side series compensation/resonance capacitor. The value of C_2 is chosen such that bridge rectifier input voltage, V_{r} is maximum. This is done by removing the second part of (3.3). From (3.2) and (3.3) required capacitances are calculated as

$$\omega_{\mathrm{t}} = \frac{1}{\sqrt{L_1\left(\frac{C_{\mathrm{p}} C_{\mathrm{s}}}{C_{\mathrm{p}} + C_{\mathrm{s}}}\right)}}\,, \quad \omega_r = \frac{1}{\sqrt{C_2 L_2}} \qquad (3.4)$$

Effective power transfer is achieved by equalizing inverter switching frequency, ω_{s} (=$2\pi f_{\mathrm{s}}$), transmitter coil resonance frequency, ω_{t} and receiver coil resonance frequency, ω_{r}.

3.4.2 Derivation of Device Voltage and Current Rating

To simplify the calculation, coil resistance and device losses are neglected, which is reasonable because the coil voltage predominantly depends on self and mutual inductances. Clearly, in the

receiver side the voltage rating of the diodes, D_3, D_4, D_3' and D_4' are the same as battery voltage, V_b. The current waveform of the receiver coil is very close to sinusoidal because it passes through the series resonance circuit. Therefore, the peak and RMS current rating of the diodes are given as

$$\hat{I}_D = \frac{\pi}{4} I_o , \qquad I_D = \frac{\pi}{2\sqrt{2}} I_o , \qquad (3.5)$$

where, I_o is average battery charging current.

The current ratings of transmitter side devices and diodes are same as dc link current, I_d. Maximum blocking voltage of the devices and the series diodes are dependent on peak voltage of capacitor, C_p. Fig. 3.5 shows ac side equivalent circuit of the proposed current-fed IPT circuit. The rectifier circuitry including active load—i.e., battery is replaced by equivalent voltage source, V_r. Since, the internal resistance of rechargeable battery is in the order of $m\Omega$ or fraction of ohm; therefore, the voltage drop across it is negligible compared with the battery voltage. Owing to sinusoidal profile of rectifier input current, I_2, only fundamental component of V_r is involved in active power transfer. It is clear from Fig. 3.5 that I_2 and V_r are in same phase because the receiver side diode bridge toggles the conduction of diode pairs just after the change of I_2 polarity. To derive the voltage and current stress on circuit components, consider that the current, I_2 or voltage, V_r is the reference phasor. Applying power balance and using Fourier series analysis, RMS value of equivalent load voltage and receiver coil current are derived as

$$V_r = \frac{2\sqrt{2}}{\pi} V_o ; \quad I_2 = \frac{\pi}{2\sqrt{2}} I_o . \qquad (3.6)$$

Applying Kirchhoff's voltage law (KVL) in the receiver side loop, transmitter coil current is calculated as

$$I_1 = -j \frac{2\sqrt{2}}{\pi} \frac{V_o}{\omega_s M} . \qquad (3.7)$$

Applying KVL and KCL in transmitter side and using (3.6) and (3.7), RMS value of voltage across TC and voltage across series capacitor, C_s is derived as

$$V_1 = \frac{2\sqrt{2}}{\pi}\left(\frac{L_1}{M}\right)V_o - j\frac{\pi}{2\sqrt{2}}\omega_s M I_o \tag{3.8}$$

$$V_s = -\frac{2\sqrt{2}}{\pi}.\frac{V_o}{{\omega_s}^2 C_s M} \tag{3.9}$$

Applying KVL at TC side resonant tank circuit, RMS value of inverter output voltage, V_i is calculated by adding (3.8) and (3.9) as

$$V_i = \frac{2\sqrt{2}}{\pi}\frac{V_o}{\omega_s M}\left(\omega_s L_1 - \frac{1}{\omega_s C_s}\right) - j\frac{\pi}{2\sqrt{2}}\omega_s M I_o \tag{3.10}$$

Applying KCL, inverter output current is derived as

$$I_i = \frac{\pi}{2\sqrt{2}}{\omega_s}^2 M C_p I_o - j\frac{2\sqrt{2}}{\pi}.\frac{V_o C_p}{M}\left(\frac{1}{\omega_s C_s} + \frac{1}{\omega_s C_p} - \omega_s L_1\right) \tag{3.11}$$

From (3.10) and (3.11) power factor at the inverter output is derived as

$$\cos\varphi = \cos(\varphi_i - \varphi_v) = \cos\left[\tan^{-1}\left\{\frac{\pi^2}{8R_o}\frac{{\omega_s}^2 M^2}{\left(\omega_s L_1 - \frac{1}{\omega_s C_s}\right)}\right\} - \tan^{-1}\left\{\frac{8R_o}{\pi^2}.\frac{1}{{\omega_s}^2 M^2}\left(\frac{1}{\omega_s C_s} + \frac{1}{\omega_s C_p} - \omega_s L_1\right)\right\}\right] \tag{3.12}$$

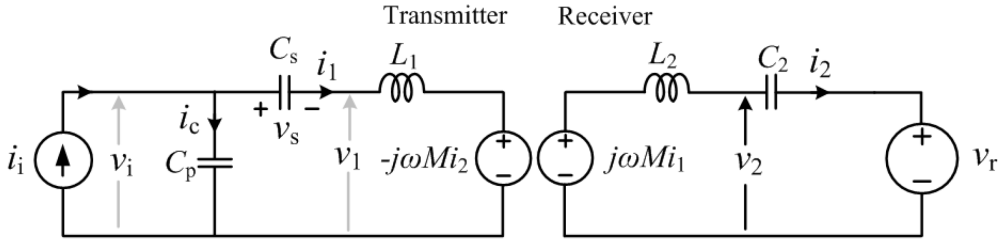


Fig. 3.5 AC equivalent circuit of the proposed CSI based WPT

From (3.12) it is clear that if C_p and C_s are selected using (3.4) then the power factor at inverter output is leading and it gives soft-switching at turn-off of inverter devices. Therefore, the parallel capacitor, C_p is calculated using (3.12) such that at rated output power inverter output is slightly lagging which enables soft-switching at device turn-on. This modified value of capacitor, C_p for soft switching at device turn-on is slightly lower than the value calculated using (3.4). From (3.10) and (3.11), CSI peak device voltage and both peak and RMS current ratings are derived as

$$\hat{V}_{\mathrm{sw}} = \hat{V}_{\mathrm{i}} \approx \frac{4}{\pi}.\frac{V_o}{\omega_{\mathrm{s}} M}\left(\omega_{\mathrm{s}} L_1 - \frac{1}{\omega_{\mathrm{s}} C_{\mathrm{s}}}\right), \qquad \hat{I}_{\mathrm{sw}} = I_{\mathrm{sw}} \approx \frac{\pi^2}{8}{\omega_{\mathrm{s}}}^2 M C_{\mathrm{p}} I_o \tag{3.13}$$

3.4.3 Soft-switching of CSI Devices

From (3.4) and (3.12) it is clear that if the parallel capacitor, C_{p} is chosen slightly lower than the value calculated from (3.4), then inverter output voltage, V_{i} leads the current, I_{i}. However, if the transmitter side circuit is not properly selected, then depending upon the parameter values, V_{i} lags, leads or stays in phase with I_{i}. Since, lagging power factor gives ZVS at device turn-on; therefore, in this section soft-switching operation is described when I_{i} lags V_{i}.

Fig. 3.6 shows soft-switching of device S_1 and S_2. At instant t_0, inverter output voltage, V_{i} changes polarity and at instant t_1 gating signal of S_2 and S_1' become high. Since, during interval t_0 to t_1 a negative voltage with same magnitude of V_{i} appears across device-diode pairs S_2-D_2 and S1'-D_1'; therefore, diodes D_2 and D_1' block this negative voltage and device pair S_1- S_2' keeps on conducting as shown in Fig. 3.6a. At instant t_2 gating signal of S_1 is removed and device pair S_2-S_1' are forced to take the inverter current from device pair S_1- S_2'. Therefore, ZVS at device turn-on of S_2 and S_1' are achieved as shown in Fig. 3.6a. Similarly, at instant t_3 inverter output voltage changes its polarity and a negative voltage appears across device-diode pairs S_1- D_1 and S_2'-D_2'. At this point diodes block the negative voltage. Therefore, a similar ZVS turn-on characteristics of devices S_1 and S_2' is achieved as shown in Fig. 3.6b. Similarly, soft switching at device turn-off and hard switching at device turn-on is achieved if the power factor at inverter output is leading.

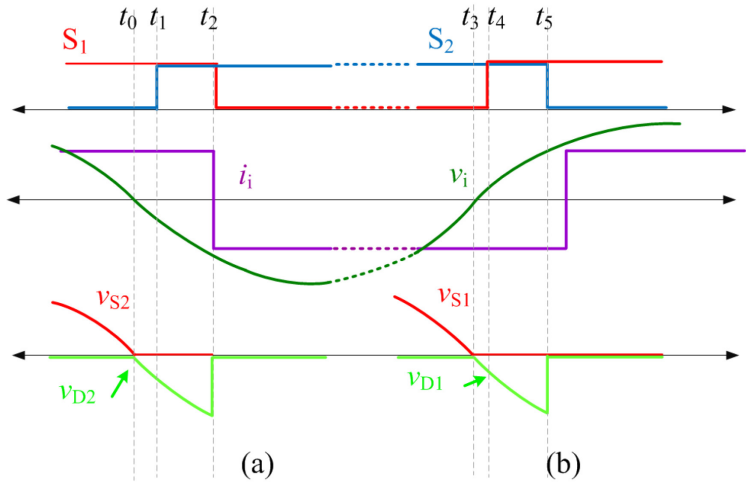


Fig. 3.6 Soft-switching at device turn off: (a) soft-switching of device S_2; (b) soft-switching of device S_1.

3.5 Voltage Gain

In order to calculate voltage gain of the dc-dc wireless power transfer stage, volt-sec balance is applied on the dc inductor, L_{d}. Referring to Fig. 3.2, average voltage, V_{A} at the input side node of L_{d} is same as input dc voltage, V_{d}. Average voltage at the other side of inductor—i.e., H-bridge inverter side node voltage is calculated as

$$V_{\mathrm{B}} = \frac{1}{\pi}\int_{\varphi}^{\pi+\varphi} \hat{V}_{\mathrm{i}}.\sin\omega t\,.\,dt \;= \frac{2\sqrt{2}}{\pi} V_{\mathrm{i}} \cos\varphi = \frac{8}{\pi^2}\frac{V_o}{\omega_{\mathrm{s}} M}\left(\omega_{\mathrm{s}} L_1 - \frac{1}{\omega_{\mathrm{s}} C_{\mathrm{s}}}\right)\cos\varphi\,. \qquad (3.14)$$

During steady state, both node voltages of inductor are same, i.e. $V_A = V_B$. Hence, voltage gain of dc-dc wireless power transfer stage is derived using (3.14) as

$$G_{\mathrm{v\_CLC}} = \frac{V_{\mathrm{o}}}{V_{\mathrm{d}}} = \frac{\pi^2}{8}.\frac{\omega_{\mathrm{s}} M}{\cos\varphi}.\frac{1}{\left(\omega_{\mathrm{s}} L_1 - \frac{1}{\omega_{\mathrm{s}} C_{\mathrm{s}}}\right)} \qquad (3.15)$$

From (3.15) it is clear that without presence of series capacitor, C_s, the voltage gain of the converter is derived as

$$G_{\mathrm{v\_LC}} = \frac{V_o}{V_{\mathrm{d}}} = \frac{\pi^2}{8}.\frac{1}{\cos\varphi}.\frac{M}{L_1} \qquad (3.16)$$

Considering same power factor at inverter output, the ratio of these two voltage gains are derived as

$$\frac{G_{\mathrm{v\_CLC}}}{G_{\mathrm{v\_LC}}} = \frac{\omega_{\mathrm{s}} L_1}{\left(\omega_{\mathrm{s}} L_1 - \frac{1}{\omega_{\mathrm{s}} C_{\mathrm{s}}}\right)} \qquad (3.17)$$

From (3.18) it is clear that another advantage of this proposed *CLC* tank is improved voltage gain compared with only parallel *LC* tank at TC side.

3.6 Selection of IPT Coils

Similar to earlier UU type IPT coils are chosen to verify the analysis and performance of this IPT topology. This type of coils are frequently used by Korea Advanced Institute of Science and Technology (KAIST). Considering the main focus of this research is to verify the power electronic converter and control and not on IPT couplers; therefore, detailed design is not carried out here.

The coil design and size optimization of the pads are detailed in [16], [9]. The predominant loss in these large air gap coils is the copper loss. From transmitter coil current and receiver coil current expressions given in (3.6) and (3.7), the copper loss in the coils is calculated as

$$P_{\mathrm{cu1}} = \frac{8}{\pi^2} \times \left(\frac{V_o}{\omega_s M}\right)^2 r_1 \tag{3.18}$$

$$P_{\mathrm{cu1}} = \frac{\pi^2}{8} \times {I_o}^2 r_2 \tag{3.19}$$

where, r_1 and r_2 are transmitter and receiver coil ac resistances, respectively. Using, (3.18) and (3.19) the coil-to-coil efficiency is derived as

$$\eta_{\mathrm{coil}} = \frac{1}{1 + \frac{8}{\pi^2}\frac{V_o}{I_o (M\omega_s)^2} r_1 + \frac{\pi^2}{8}\frac{I_o}{V_o} r_2}. \tag{3.20}$$

From (3.20), it is clear that coil-to-coil power transfer efficiency increases with increase in impedance due to mutual coupling ($M \times \omega_s$) and reduction in coil ac resistance.

3.7 Simulation Results

The IPT circuit shown in Fig. 3.2 is simulated using PSIM 9.3. Simulation models for two power ratings rated at 3kW and 420W were developed. Parameter values used for the simulation are listed in Table 3.1. Two sets of simulation results are presented in this section; one set is for 420W power output to verify the experimental results. All the selected circuit parameters for 420W power output are exactly same as experimental proof-of-concept hardware prototype. Other set is for 3*k*W rated power, which demonstrates the feasibility of the proposed converter for higher power applications such as EVs. The IPT pad parameters—viz., self-inductances and mutual inductance values for 3*k*W system are selected from [48] and listed in third column of Table 3.1. In order to control the battery charging current, fixed switching frequency and variable duty cycle modulation is adopted for the inverter.

3.7.1 Comparison Between (*LC*) and (*C*)(*LC*) Tank

Table 3.2 lists and compares different circuit parameters between the current-fed topology with *LC* resonant tank at TC and proposed *CLC* topology. The parameters in Table 3.2 for 420W power output are calculated and verified by the simulation and experimental results. However, for 3 *k*W

Table 3.1. Selected circuit parameters

Parameters	Selected Values (for 420W prototype)	Selected Values (for 3*k*W)	Unit
Input DC voltage, v_d	250	400	volt
DC link inductor, L_d	5	4	*m*H
Self-inductance, L_1, L_2	207.8, 208.3	177, 177	μH
Mutual inductance, M	11.3	40	μH
Capacitors, C_p, C_s, C_2	90, 94, 47	485, 504, 252	*n*F
Switching frequency, f_s	50.95	25	*k*Hz
Battery voltage, v_b	42	250	volt
Battery internal resistance	100	200	*m*Ω
Output filter capacitor, C_o	350	350	μF
Coil turns ratio	1:1(24turns each)	1:1	-
Unloaded quality factor of TC and RC	266, 267	195, 195	-

Table 3.2. Comparison of various parameters with V_o= 250 V, P_o=3kW, f_{sw}=25kHz (V_o= 42 V, P_o=420 W, f_{sw}=50.95kHz)

Parameters	Current-fed IPT circuit with (L)(C) tank in TC P_o=3*k*W (P_o=420W)	Proposed topology P_o=3*k*W (P_o=420W)
Inverter device stress (peak)	1414 V (981 V)	714 V (494 V)
Device current (RMS)	6.1A (1.41A)	6.0A (1.40A)
VA at inverter output	7787 (1246)	3858 (622)
Inverter device R_{dson}	320 *mΩ* (0.95 *Ω*)	160*mΩ* (380*mΩ*)
Device loss (each)	13.0 W(2.02 W)	6.81 W (1.05 W)
Total cost of inverter devices including series diodes	$ 119.9 ($ 59.0)	$ 59.4 ($ 32.9)
Total cost of tank capacitors	$ 58.4 ($ 8.62)	$ 66.57 ($ 21.98)
Coil to coil efficiency	-	92.1% (87.5%)
DC-DC stage efficiency (excluding coil-coil efficiency)	-	96.4% (96.6%)
Overall DC-DC stage efficiency	87.6% (84.2%)	88.8% (84.5%)

power output the results are only verified with the simulation. The current ratings of the inverter devices for both the topologies are almost same, whereas the voltage rating of the proposed topology is close to half of the conventional *LC* resonant tank network. Hence, the inverter volt-amp (VA) rating with *CLC* tank is also almost half. The part number and major specifications of the selected semiconductor devices and film capacitor are listed in Appendix. Device losses are calculated considering soft-switching at turn-on, because depending upon the power factor at the inverter output, both of the converter devices experience either soft turn-on or turn-off with lagging and leading power factor respectively. Since, the inverter device voltage stress of the proposed topology is lower; therefore, device power loss in the proposed topology is considerably lower and the approximate price of the inverter semiconductors is also lesser.

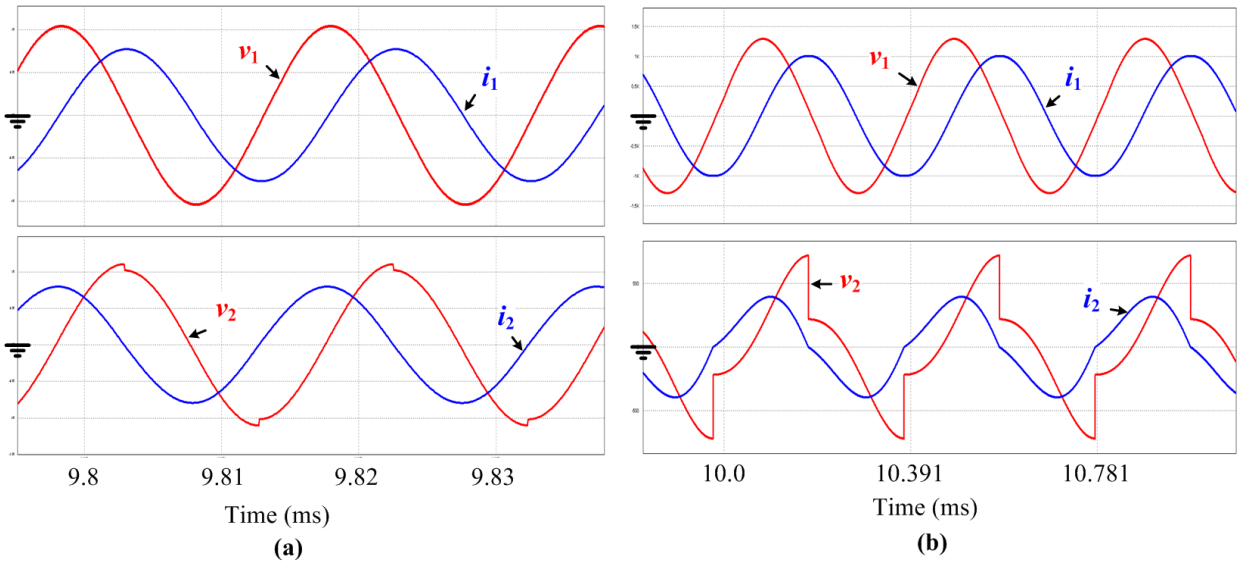


Fig. 3.7 Simulation results: Steady state waveforms of TC voltage, v_1 current, i_1 and RC voltage, v_2 and current, i_2 (a) 420W power output [scales: 500v/div, 10A/div] (b) 3 kW power output [scales: 500v/div, 25A/div]

The resonant tank capacitors are selected from Cornell Dubilier Electronics, in order to get least ESR. The coupling coefficient of the lab prototype is around 0.054 with 200mm air gap and the coupling coefficient of the 3kW system is taken around 0.226, because generally for *k*W level IPT systems the coefficient of coupling is more than 0.2 [48], [42]. The unloaded quality (Q)-factor for 420W system is 266 and for 3kW system it is 195. From (3.20) the calculated coil to coil efficiency of the 420W system is around 87.5 % whereas for 3kW system it is 92.1%. Higher efficiency can

be obtained with higher quality factor coils. However, this leads to thicker IPT coils, which are generally made from expensive litz wires.

3.7.2 Steady State Results

Fig. 3.7a shows steady state voltage and current waveforms of transmitter and receiver coils for 420W power transfer and corresponding circuit parameters listed in second column of Table 3.1. Fig. 3.7b shows the simulation results for 3 *k*W power output. Equations (3.6) and (3.7) show that transmitter coil current, I_1 lags receiver coil current, I_2 by 90^0. Also, from (3.8), transmitter coil voltage, V_1 lags I_1. Since, the mutual inductance is very low; therefore, the real part of (3.8) predominantly determines the voltage magnitude. Fig. 3.7 verifies this analytical predictions. With the given simulation parameters, calculated RMS value of V_1 is 712V for 420W power output. Simulation result also gives the same value of V_1. Fig. 3.7 shows that the transmitter coil voltage and current waveforms are very close to sinusoidal. It is because the parallel capacitor, C_p provides much lesser impedance to higher order harmonic currents than TC. Therefore, TC predominantly receives fundamental component.

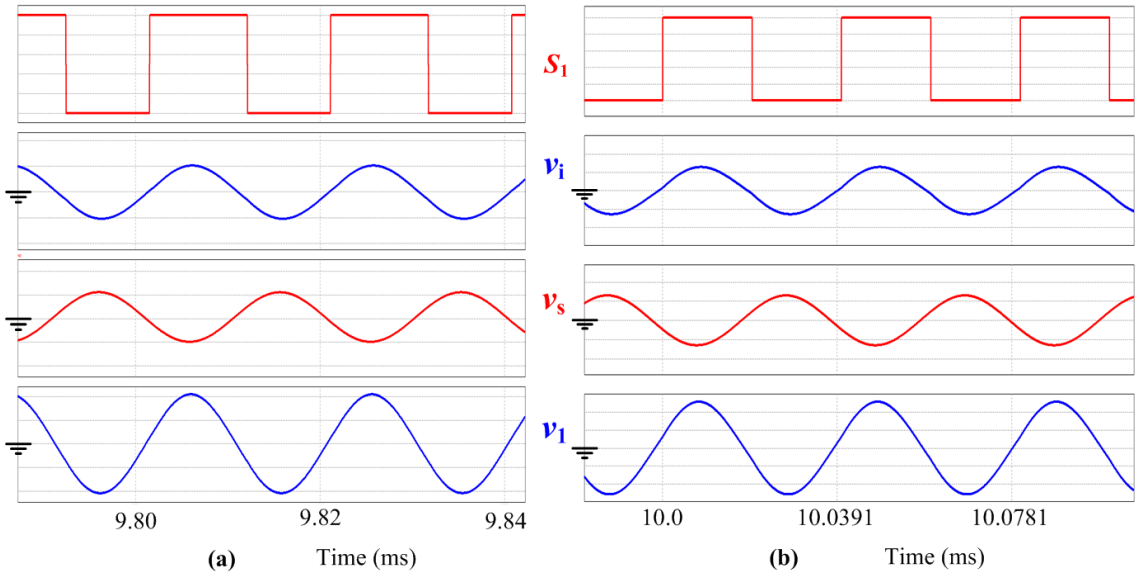


Fig. 3.8 Simulation results: Steady state waveforms of gating signal of device S_1, inverter output voltage v_i [500v/div], series capacitor voltage, v_{cs} [500v/div] and transmitter coil voltage, v_1 [500v/div] (a) 420W power output (b) 3 kW power output

Fig. 3.8 shows the simulation results of the different voltage waveforms of the resonant tank elements of transmitter network. Since the impedance of the capacitor, C_s is half of the impedance

of TC self-inductance at resonance frequency; therefore, parallel capacitor, C_p experiences approximately half of the TC voltage, V_1. This is mathematically derived in (3.8), (3.9) and (3.10).

Table 3.3 Variation of component ratings due to misalignment, P_o=420W, V_o=42V, I_o=10A, f_s=50.95kHz

Components	Coupling 5.5% M= 11.3μH	Coupling 5.2% M=10.8μH	Coupling 4.9% M=10.2μH	Coupling 4.5% M=9.5μH
Parallel capacitor voltage, V_i	351 V	367 V	388 V	416 V
Series Capacitor voltage, V_s	347 V	363 V	385 V	413 V
TC Coil voltage, V_1	712 V	729 V	772 V	829 V
Inverter current, I_i	1.23	1.19	1.14	1.10
RC Coil voltage, V_2	379 V	379 V	379 V	379 V
Voltage across C_2, V_{C2}	738 V	738 V	738 V	738 V

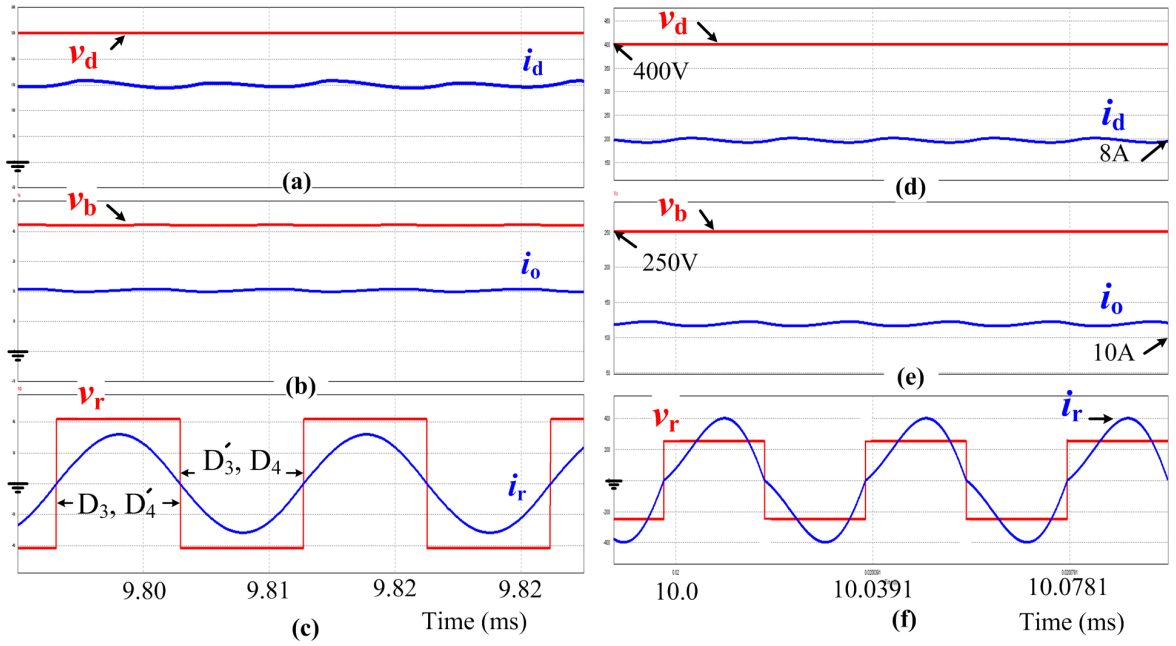


Fig. 3.9 Steady state waveforms for 420W/ 3kW power output: (a)/ (d) Input dc voltage, v_d [50v/div]and current, i_d [0.5A/div for (a) and 2A/div for (d)]; (b)/ (e) output voltage, v_b [10v/div for (b) and 50v/div for (e)] and current, i_o [5A/div]; (c)/ (f) diode bridge rectifier input voltage, v_r [20v/div for (c) and 200v/div for (f)] and current, i_d [10A/div].

Simulation results shown in Fig. 3.8 verify this mathematical analysis. This is a major advantage of this *CLC* topology where the inverter devices get half of the transmitter coil voltage stress,

whereas the device voltage stress is exactly same as transmitter coil voltage in case of simple parallel *LC* topology. Table 3.3 shows variation of component ratings due to misalignment when the operating conditions are P_o=420W, V_o=42V, I_o=10A, and f_s=50.95kHz.

Fig. 3.9a and Fig. 3.9b show steady state dc input voltage, input current waveforms and dc output voltage, output current waveforms for 420W power output. Fig. 3.9d and Fig. 3.9e show those waveforms for 3 *k*W power output. Fig. 3.9c and Fig. 3.9f show voltage and current waveforms at diode bridge rectifier ac input for 420W and 3 *k*W power output respectively. From Fig. 3.9c and Fig. 3.9f it is clear that bridge rectifier input voltage changes its polarity when current crosses zero; therefore, soft commutation and soft recovery of rectifier diodes is achieved resulting in reduced losses.

Fig. 3.10 shows the simulation results of soft-switching for CSI devices. From Fig. 3.10 it is clear that CSI output voltage leads the fundamental component of inverter output current. These results validate the mathematical analysis of (3.8) and (3.9). It is clear that the series diode D_1 blocks the negative voltage before the gate pulse of S_1 is turned-on. This allows the device S_1 to turn on when voltage across it is zero. Similarly, other devices also turn-on while the voltage across the corresponding devices is zero.

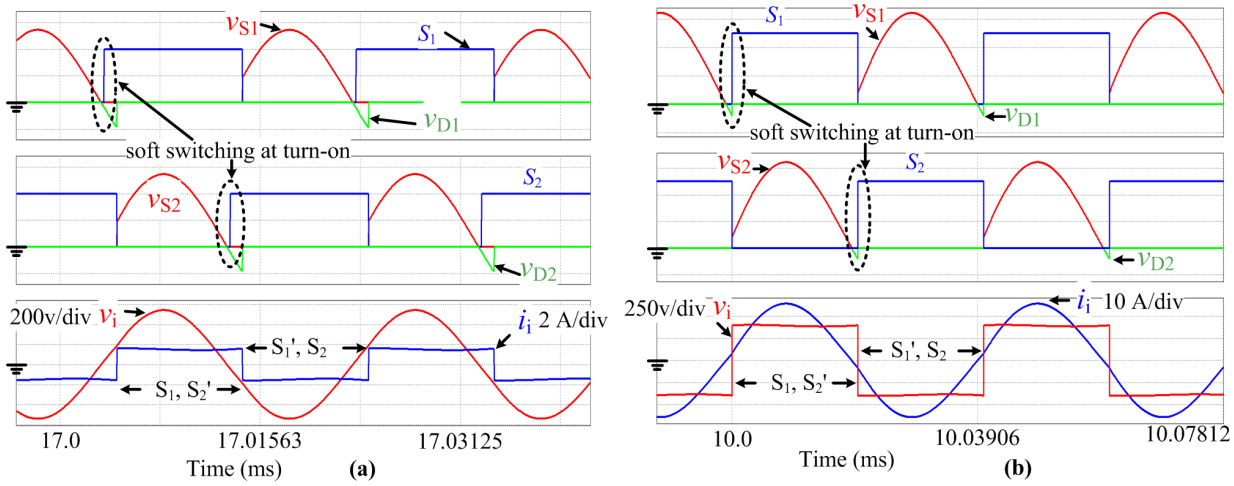


Fig. 3.10 Soft switching at device turn-on: Gate pulse of device S_1, voltage across S_1, v_{s1} and Diode D_1, v_{D1} [200v/div]; Gate pulse of device S_2, voltage across S_2, v_{s2} and Diode D_2, v_{D2} [200v/div]; inverter output voltage, v_i and current, i_i (a) 420W power output (b) 3 kW power output.

3.8 Experimental Results

A proof-of-concept laboratory prototype rated at 420 W has been developed in the laboratory as shown in Fig. 3.11. DSP TMS320F28335 is used as digital control platform and gate driver SKHI 61(R) is used to drive the inverter devices. Parameter values of the hardware circuit are listed in second column of Table 3.1. Two sets of experimental results are presented in this section to verify the mathematical analysis, design, and simulation results. One set is with 200mm air gap without horizontal misalignment and the other one is with 150mm air gap and 50mm horizontal misalignment.

Fig. 3.12a shows steady state voltage and current waveforms of transmitter and receiver coil with 420W power output and battery terminal voltage 42V. The air gap of the IPT pad is 200mm with no horizontal misalignment. Transmitter coil current, i_1 lags receiver coil current, i_2 approximately by 90^0 which are predicted from analysis and simulation results. Experimentally measured RMS value of transmitter coil voltage is 725V, which is very close to simulation result (712V). This deviation is due to error in parameter measurement and elimination of coil resistances. Also, experimentally obtained voltage and current profile of transmitter coil are almost pure sinusoidal which are expected from the analysis and simulation.

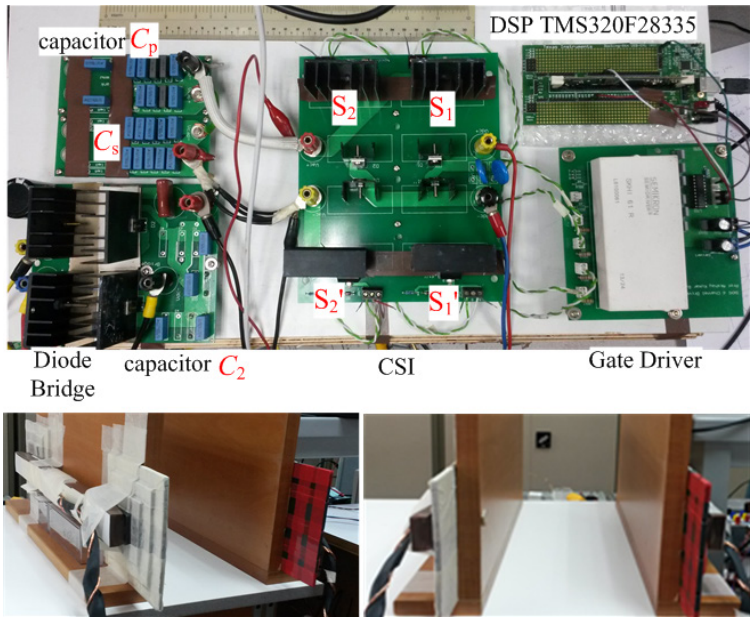


Fig. 3.11 Photograph of experimental set-up with transmitter and receiver coils (two different views) 200mm apart.

Fig. 3.12b shows the experimental results of TC and RC voltages and currents for 420W power output. IPT coil vertical and horizontal misalignments are 150mm and 50mm respectively and corresponding coupling factor is 8.2%. The measured efficiency of the lab prototype is around 84.5% with this operating condition. From (3.7) and (3.8) it is clear that for a given load the higher coupling reduces the magnitude of TC voltage and current. Since, for a given air gap length, higher coupling is achieved with larger pad size; therefore, with larger pad size and suitably designed capacitors, this topology is expected to give higher efficiency. For instance, the estimated efficiency for 3 *k*W power output is nearly 89% as given in Table 3.2, where the coefficient of coupling is 22.6%.

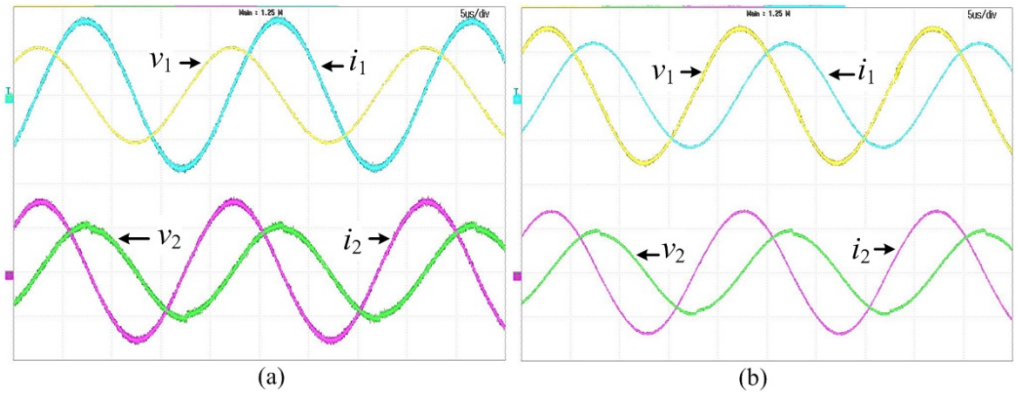


Fig. 3.12 Experimental results: Steady state waveforms of transmitter coil voltage, v_1 [1*k*V/div] current, i_1 [10A/div] and Receiver coil voltage, v_2 [1*k*V/div] and current, i_2 [10A/div] with IPT pad (a) vertical distance 200mm, without horizontal misalignment (b)vertical distance 150mm, horizontal misalignment 50mm

Fig. 3.13 shows gating signal of device S_1, voltage waveforms of capacitor C_s, capacitor C_p and transmitter coil for two different IPT coil misalignments. These results verify the mathematical analysis given in (3.8), (3.9) and (3.10)—i.e., the series capacitor voltage, V_{cs} is approximately half of the coil voltage V_1 with 180^0 phase difference. Therefore, the voltage across the parallel capacitor, V_i is half of the transmitter coil voltage, V_1 with same phase. Similarly, if the value of the series capacitor impedance is higher—viz., two third of impedance of transmitter coil, then the parallel capacitor would experience only one third of the TC voltage. These results validate the suitability of the topology in high power application.

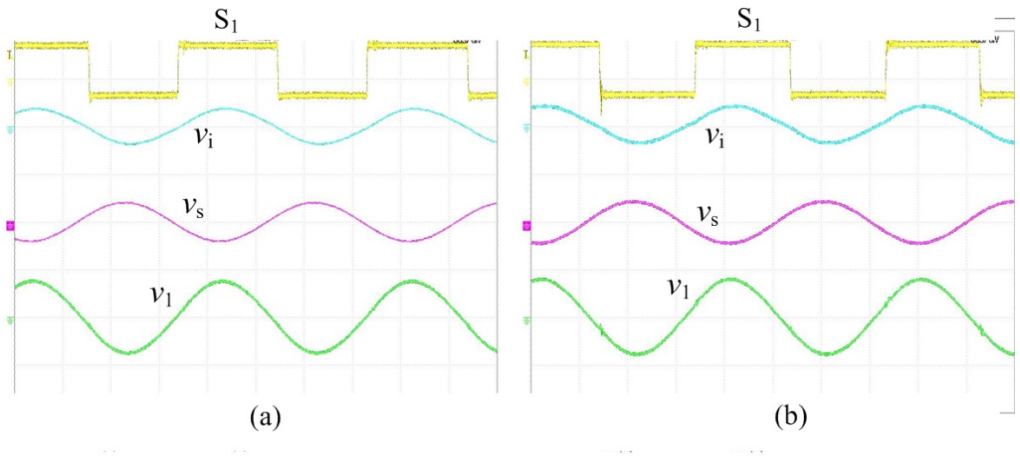


Fig. 3.13 Experimental results: Steady state waveforms of gating signal of device S_1, inverter output voltage v_i [1kV/div], series capacitor voltage, v_{cs} [1kV/div] and transmitter coil voltage, v_1 [1kV/div] (a) vertical distance 200mm, without horizontal misalignment (b)vertical distance 150mm, horizontal misalignment 50mm

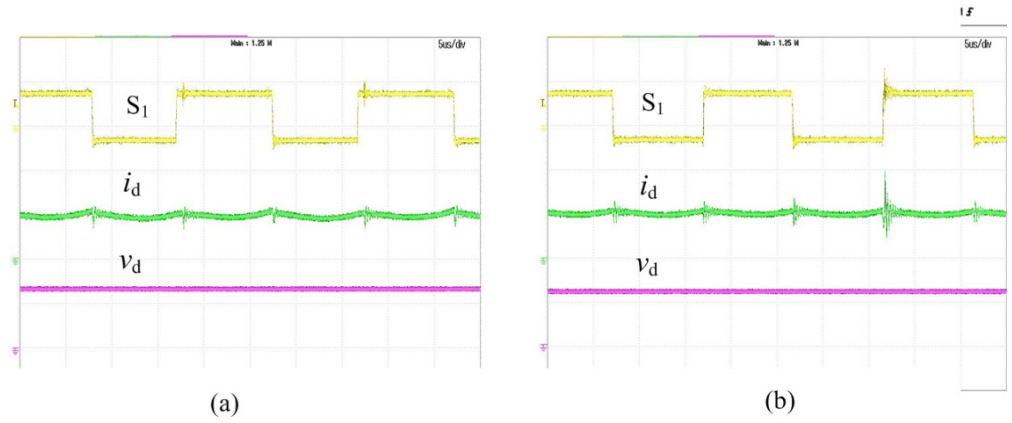


Fig. 3.14 Steady state waveforms: Gate pulse of device S_1, input DC voltage, v_d [200 V/div] and current, i_d [2 A/div] with IPT pad (a) vertical distance 200mm, without horizontal misalignment (b)vertical distance 150mm, horizontal misalignment 50mm

Fig. 3.14a and Fig. 3.14b show steady state waveforms of device S_1 gate pulse, dc input current and voltage for output power 420W. The average value of the dc input current is around 2 A for IPT coil airgap 200mm and 2.04A for 150mm airgap. Since this dc link current decides the rating of the CSI devices, therefore the main advantage of this topology is low device current stress.

Fig. 3.15a shows dc output voltage, current and bridge rectifier ac input voltage and current for 420W power output with IPT pad vertical distance 200mm and no horizontal misalignment. Fig. 3.15b shows results for 420W power output with coil vertical distance 150mm and horizontal

misalignment 50mm. The soft-commutation and soft recovery characteristics of the diode bridge is similar to the simulation results and verify minimum reverse recovery loss of the rectifier diodes. These results show that the current-fed topology is also a viable solution for wireless power transfer.

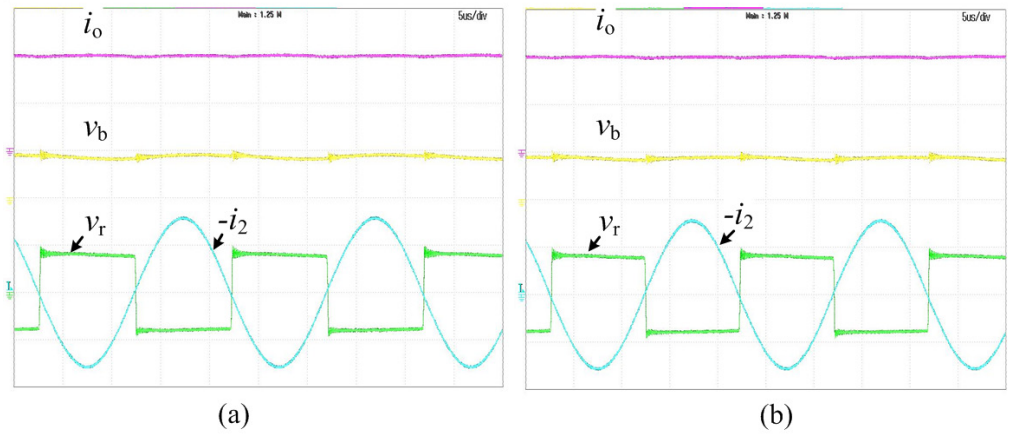


Fig. 3.15 Steady state waveforms: output voltage, v_b [50 V/div], charging current, i_o [5 A/div]; diode bridge rectifier input voltage, v_r [50 V/div] and current, i_d [10 A/div] with IPT pad (a) vertical distance 200mm, without horizontal misalignment (b)vertical distance 150mm, horizontal misalignment 50mm

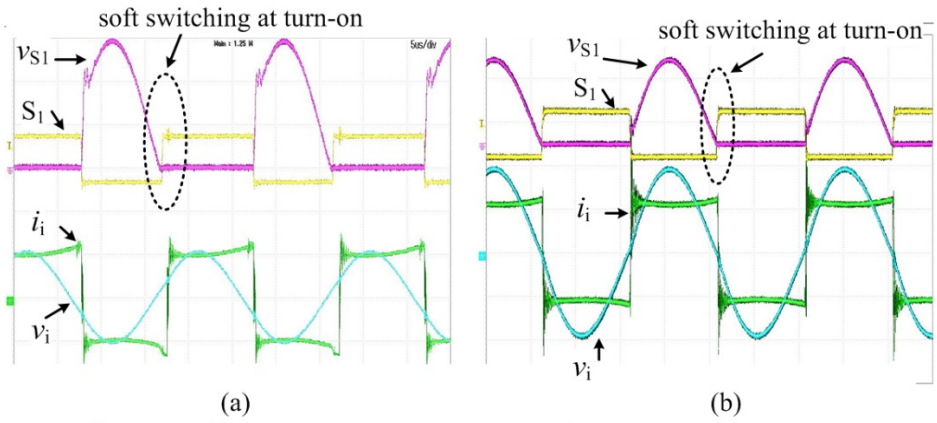


Fig. 3.16 Soft switching at device turn-on: Gate pulse of device S_1, voltage across the device, v_{S1} [200 V/div], inverter output current, i_i [2 A/div] and voltage v_i [200 V/div] with IPT pad (a) vertical distance 200mm, without horizontal misalignment (b)vertical distance 150mm, horizontal misalignment 50mm.

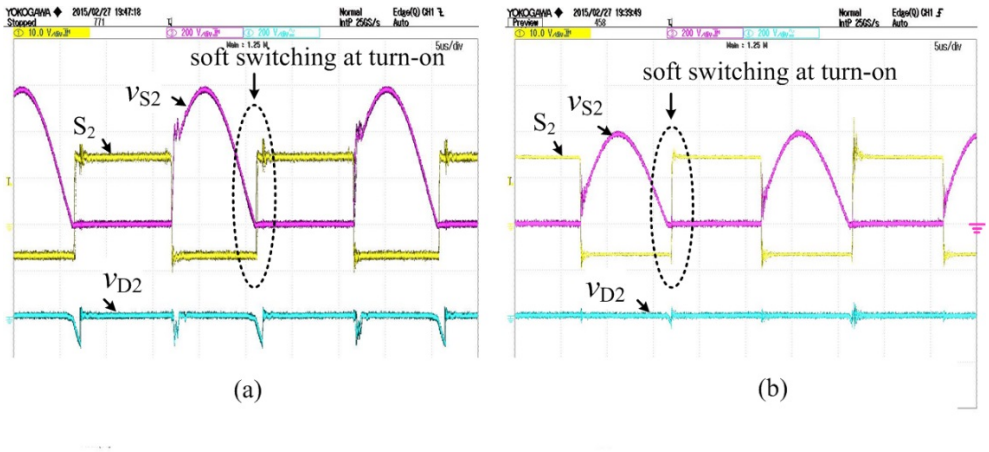


Fig. 3.17 Soft switching at device turn-on: Gate pulse of device S_2, voltage across the device, v_{s1} [200 V/div] and Diode D_1, v_{D1} [200 V/div] with IPT pad (a) vertical distance 200mm, without horizontal misalignment (b)vertical distance 150mm, horizontal misalignment 50mm.

Fig. 3.16 shows soft-switching characteristics of device S_1 along with inverter output voltage and current waveforms for two different misalignments of IPT coil. Fig. 3.16 verifies that the selection of transmitter side parallel capacitor, C_p according to (3.12) provides lagging power factor at inverter output. For this reason, the series diode D_1 starts blocking the negative voltage before the gate pulse is applied to device S_1. Since, the voltage appeared across device S_1 zero at turn on of the device; therefore, soft-switching is achieved at turn-on. These experimental results validate the analytical prediction of soft-switching of inverter devices. Similar characteristics of other inverter devices are observed during experiment. Fig. 3.17 shows soft-switching waveforms of the device S_2 which exactly matches with the simulation result.

3.9 Conclusions

A new IPT topology using current-fed *CLC* tank network at transmitter side and series *LC* tank at receiver side is reported in the Chapter. Along with all the merits of current-fed converter used in IPT technology, the proposed topology reduces volt-amp (VA) loading on inverter and reduces voltage stress at inverter output by adding a capacitor in the series of the transmitter coil. This leads to lower voltage stress of inverter devices, lower switching loss and overall converter cost. Therefore, this topology eliminates the limitations of conventional current fed converter in higher power applications. Simulation results show that the required high reactive current in the transmitter coil is supplied by the parallel compensation capacitor. Hence, the current stress of CSI

devices is limited to the peak dc inductor current, which is a major advantage of this topology. Soft-switching at turn-on of CSI devices ensures lower switching loss. Also, soft recovery of the rectifier diodes eliminates reverse recovery loss. All the analysis and simulation are verified by the experimental results on a proof-of-concept 420W laboratory built prototype. Nearly 89% efficiency is obtained.

Chapter 4 Small Signal Modelling and Closed Loop Control of H-bridge Current-fed IPT Topologies

4.1 Introduction

Along with derivation of innovative power converter topologies, dynamic modelling and closed loop control are also integral part for practical implementation of the converters. In Chapter 2 and 3, two new IPT topologies have been reported, where the inverter is current-fed full bridge type. In those chapters, the main emphasis have been given on deriving suitable topology, steady-state operation, converter design, and soft-switching etc. Also, steady-state performance results with bipolar modulation scheme have been reported. This Chapter primarily focuses on small signal modelling and closed loop control of the topologies presented in Chapter 2 and 3.

4.1.1 Existing Control Technique for Parallel Compensated Topologies

The resonant converts can either be controlled through fixed switching frequency variable duty cycle method or by variable switching frequency fixed duty cycle method. Owing to load dependent resonance of *LC* parallel rank at transmitter side, control is generally carried out either by frequency modulation [69], [35] or dynamically varying tank capacitances [34], while keeping the duty cycle fixed at 50%. It helps to tune inverter switching frequency exactly at resonant point of tank network, which shifts due to load and other circuit parameter variations. Also, this operation ensures unity displacement power factor (PF) at inverter output—i.e., the relative phase angle of the fundamental component of voltage and current is zero. This is commonly known as zero phase angle (ZPA) operation. ZPA operation with VSI and CSI are shown in Fig. 4.1. The merits of ZPA operations are as follows.

i. Unity displacement PF operation at inverter output ensures least volt-amp (VA) loading on inverter.
ii. It results in least voltage and current ratings, and lower power loss of inverter devices.
iii. For CSI topology, ZPA operation facilitates zero voltage switching (ZVS) of inverter devices, whereas the devices of VSI topology experiences zero current switching (ZCS).

However, the demerits of control through variable switching frequency or dynamically varying compensation capacitor are as follows.

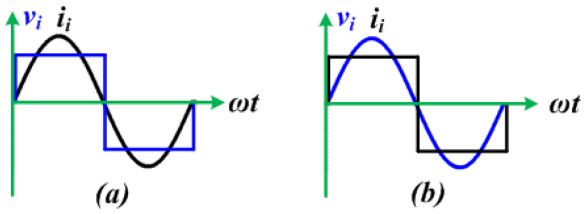


Fig. 4.1 Ideal inverter output voltage and current profiles at ZPA operating point for (a) voltage source inverter (VSI) (b) current source inverter (CSI)

i. Since, the inverter control is fully focused on tuning the system at ZPA operating point; therefore, the load requirement is fulfilled by additional dc-dc converter at the load side.
ii. Parallel tuned IPT topology with current-fed push-pull inverter requires additional control effort to start-up.
iii. Frequency bifurcations due to presence of multiple ZPA operating points is another challenge [69].
iv. Dynamic tuning by varying tank capacitance is complex and impractical due to additional devices, capacitors, control and driving circuitries as shown in Fig. 4.2 [34].

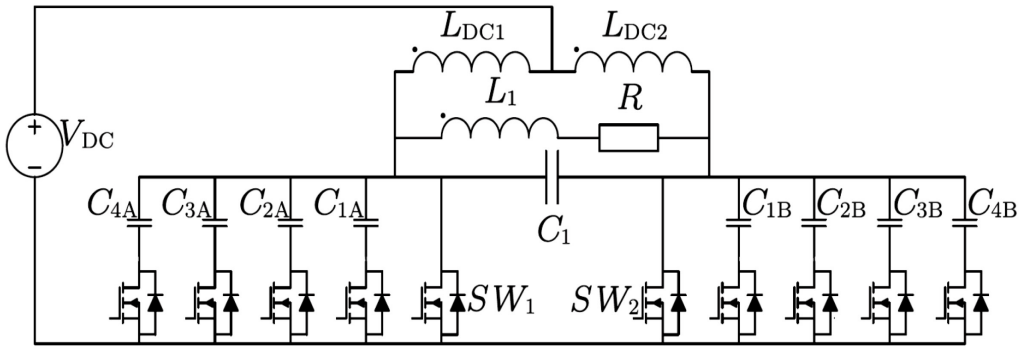


Fig. 4.2 Push–pull circuit with switchable capacitors [34]

4.1.2 Fixed Frequency Variable Duty Cycle Control

The primary reason for adopting dynamic tuning technique for parallel compensated IPT topologies is that the resonant tank is load dependent [62], [69]. Although, variable duty cycle with fixed inverter switching frequency control is popular for most power electronic converters, but due to load dependent resonance, it is never adopted for this systems. This Chapter proposes a novel design technique to achieve load independent characteristics for parallel compensated IPT topologies. This proposed design is based on passive selection of compensation elements. The merits of this load independent design are as follows.

i. It achieves load independent characteristics of tank network without any complex dynamic control.
ii. The control effort of the inverter is focused on meeting load demand, thereby eliminating additional chopper stage for control of load power.
iii. Conventional fixed frequency variable duty cycle control is possible.
iv. Usual small signal modelling approach is suitable for modelling and control of the converter.

4.1.3 Small Signal Modelling

To perform dynamic modelling of a power converter, identification of low frequency poles and zeros are required. This is usually carried out by deriving system transfer function. Small signal modelling of power converter is a simple and very effective method to derived transfer functions. The first step of modeling is identification of inputs and outputs. Next step is derivation of all the dynamic expressions of the state-variables. Owing to switching, the converter circuits are usually non-linear and the state-variables may have more than one expressions based on different switching intervals. State-space averaging technique is frequently used to simplify these dynamic expressions, which is carried out by averaging the state variables over a switching time period. Using these average state-space expressions, state-variable matrices (A, B, C, and D) are formed, and thereby the system transfer function is derived.

4.1.4 Chapter Organization

Since, this Chapter has several parts; therefore, the Chapter organization is included to clarify the overall structure. Owing to different modulation scheme, the steady-state operation is presented first. Next, a novel load independent resonant tank design is reported, which enables usual fixed frequency variable duty cycle control. Thereafter, the small signal analysis, controller design and model verifications etc. are reported. Finally, experimental results obtained from a 1.6kW lab-built prototype are reported to verify ZPA operation, steady state operations, and dynamic performances with unipolar PWM.

One important point to note that the steady-state operation, load independent resonant tank design and small signal modeling for both $(L)(C)$ transmitter and $(C)(LC)$ transmitter topologies follow similar method. Therefore, to avoid unnecessary repetitions, only detailed design of

(*C*)(*LC*) topology is reported and only final design expressions of (*L*)(*C*) is included. However, experimental verifications for both the topologies are reported.

4.2 Selected IPT Topology

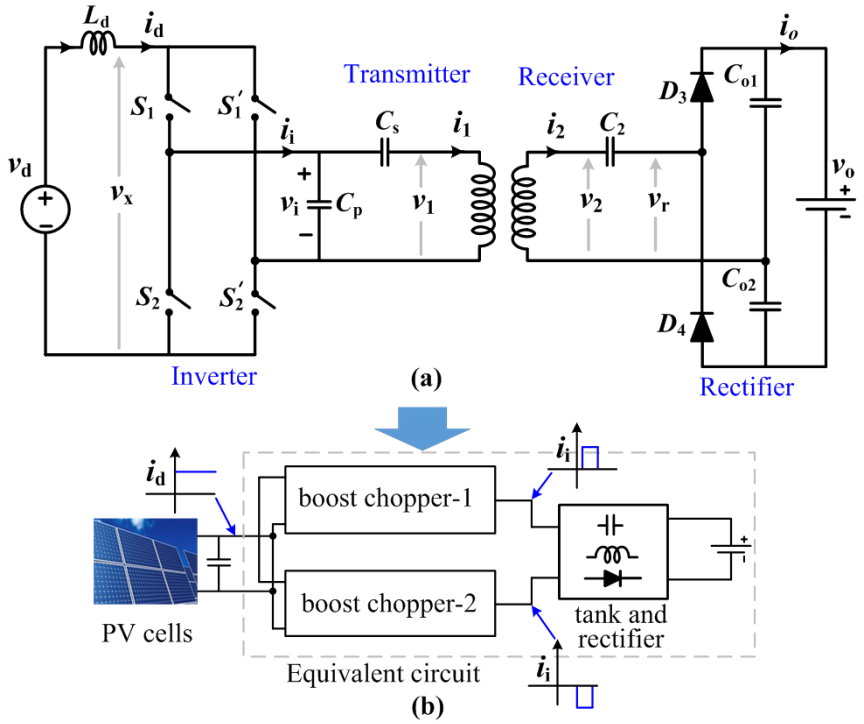


Fig. 4.3 (a) IPT Topology with parallel-series compensation at TC side and series compensation at RC side, (b) possible applications

Although, the selected topology for dynamic modelling shown in Fig. 4.3a is very similar to earlier Chapters, but it has some improvements. The rectifier circuit is voltage doubler. It provides twice voltage-gain compared with full-bridge rectifier with only two diodes. Also, compared with bipolar PWM scheme used earlier, the unipolar PWM scheme makes the steady-state operation significantly different. With unipolar PWM, effective boost mode operation of full-bridge current-fed inverter is fully realized. The performance of the inverter with unipolar PWM is equivalent to two boost choppers, where one chopper is responsible for feeding positive current pulse to tank network and other one feeds negative current pulse to tank as shown in Fig. 4.3b. Although, this converter can be used in several applications, but it is especially suitable for directly extracting power from sources, such as solar PV.

4.2.1 Steady State Operation with Unipolar PWM

Unlike voltage source inverter, in this boost derived inverter the complementary switching signals are given between top devices (S_1-S_1') and between bottom devices (S_2-S_2'). This arrangement enables to get a characteristics exactly like boost chopper. A slight overlap between the complementary switching signals are always maintained to provide continuous path for input inductor current. Fig. 4.4 shows equivalent circuits during different switching intervals and Fig. 4.5 shows important voltage and current waveforms with a typical unipolar PWM. Because the secondary side voltage doubler converter simply provides passive rectification; therefore, this part is not elaborated. Simply, based on the polarity of RC current, i_2, each rectifier diodes conducts accordingly and feeds load.

Interval 1 (t_0-t_1): During this interval, devices S_1 and S_2' are ON and S_2 and S_1' are OFF. In this interval, the source inductor, L_d is directly connected to the TC side tank network as shown in Fig. 4.4a. This is similar to turn-off interval of conventional boost converter. Owing to presence of parallel capacitor, the inverter output voltage is very close to sinusoidal, but the current, i_i is quasi-square. Clearly, the voltage and current profiles of remaining tank elements are also sinusoidal as shown in Fig. 4.5. The voltage and current expressions for this duration are given as

$$L_d \frac{di_d}{dt} = v_d - v_i\,, \qquad (4.1)$$

$$i_i = i_d, \qquad v_x = v_i\,. \qquad (4.2)$$

Interval 2 (t_1-t_4): The first part of this interval has slight overlap (t_1-t_2) between S_1-S_1' as shown in Fig. 4.5. At instant t_1, the voltage across the incoming device S_1' is positive; therefore, it immediately takes inverter current, commutating device S_1. This transfer of inverter current at t_1 leads to hard turn-on of S_1'. Gate-pulse of S_1 is withdrawn at instant t_2, but the current through S_1 is already zero. Therefore, zero-current-switching (ZCS) turn-off of S_1 is achieved. The duration of overlap (t_1-t_2) is solely dependent on turn-on and turn-off delay of the devices. It should be sufficient enough to allow turn-on and turn-off of incoming and outgoing devices, but small enough to have insignificant impact on overall performance of the converter.

Referring to Fig. 4.5, till time instant t_3, devices S_1' and S_2' carry complete inverter current and the corresponding equivalent circuit is shown in Fig. 4.4b. At instant t_3 switching overlap of bottom devices (S_2-S_2') starts. Owing to presence of negative voltage, the incoming device S_2 does not take

the inverter current immediately at instant t_3. Therefore, during overlap time (t_3-t_4), S_1' and S_2' keeps on conducting and this enables zero voltage switching (ZVS) turn-on of device S_2.

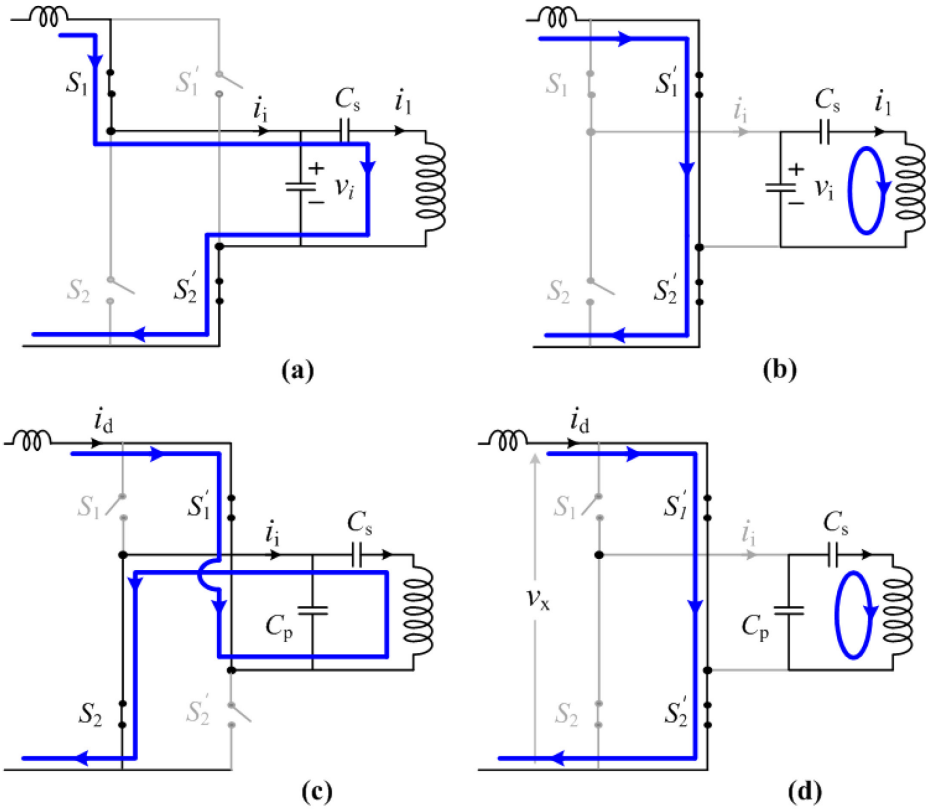


Fig. 4.4 Equivalent circuits during steady state operation

Throughout the interval t_1-t_4, the input inductor is directly connected across the source, which is equivalent to turn-on period of regular boost chopper. The voltage and current expressions during this interval is given as

$$L_{\mathrm{d}} \frac{di_{\mathrm{d}}}{dt} = v_{\mathrm{d}} \,, \qquad (4.3)$$

$$i_{\mathrm{i}} = 0, \qquad v_{\mathrm{x}} = 0 \,. \qquad (4.4)$$

Interval 3 (t_4-t_5): At instant t_4 overlap period ends when gate pulse of S_2' withdrawn. Device S_2' experiences hard turn-off at instant and t_4 and from this time onward S_1' and S_2 takes the inverter current as shown in the equivalent circuit Fig. 4.4c. Similar to interval 1, in this interval the source is directly connected to the inverter output side network, which is similar to turn-off interval of conventional boost converter. Voltage and current expressions for this duration are given as

$$L_{\mathrm{d}}\frac{di_{\mathrm{d}}}{dt} = v_{\mathrm{d}} + v_{\mathrm{i}}\,, \qquad (4.5)$$

$$i_{\mathrm{i}} = -i_{\mathrm{d}}, \qquad v_{\mathrm{x}} = -v_{\mathrm{i}}\,. \qquad (4.6)$$

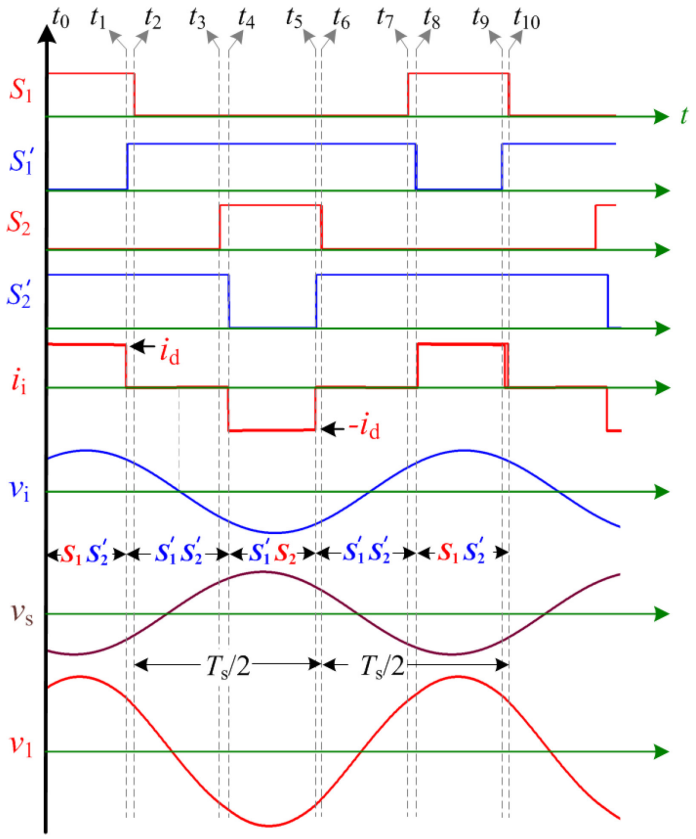


Fig. 4.5 Steady state operating waveforms

Interval 3 *(t_5-t_8):* At instant t_5 S_2' is given pulse and it immediately stats conducting commutating device S_2, owing to presence of positive voltage across S_2'. This leads to hard turn-on of S_2'. But, due to transfer of the current from S_2 before withdrawing its gate pulse leads to ZCS at turn-off. Although, at instant t_7 S_1 is triggered, but due to presence of negative voltage, it does not take the inverter current and devices S_1' and S_1' keeps on conducting as shown in the equivalent circuit Fig. 4.4d. Therefore, S_1 experiences ZVS turn-on at instant t_7. At instant t_8 gate pulse of S_1' is withdrawn and S_1 is forced to take inverter current and the corresponding equivalent circuit is same as Fig. 4.4a. The voltage and current expressions during interval t_5-t_8 is same as (4.3) and (4.4).

This completes one complete inverter switching cycle. Steady state operation of the IPT topology with (L)(C) transmitter and (LC) receiver tank is exactly similar; therefore, it is not repeated.

4.3 Proposed Load Independent Tank Design

In this section, a brief description of existing load dependent compensation is reported and then the proposed load independent compensation technique for (*C*)(*LC*) transmitter and (*LC*) receiver tank is detailed. Owing to similar design method, only the crucial design expressions of (*L*)(*C*) transmitter and (*LC*) receiver tank is reported.

4.3.1 (*C*)(*LC*) Transmitter and (*LC*) Receiver Tank

Fig. 4.6 shows the transformer equivalent circuit of the selected series-parallel/parallel converter, when the RC side parameters are referred to TC side with superscript symbol ‘′’. In presence of *LC* series compensation, the conventional design approach chooses RC compensation as

$$C_2 = {}^{1}/_{\omega_s^2 L_2}\ , \qquad (4.7)$$

where, ω_s is resonance frequency or the inverter switching frequency and L_2 is self-inductance of RC. Using (4.7) and applying KCL and KVL, the required value of parallel capacitor at TC side is derived as

$$C_{\mathrm{p}} = \frac{L_1 - \dfrac{1}{\omega_s^2 \times C_{\mathrm{s}}}}{\dfrac{\omega_s^4 M^4}{R_{\mathrm{eq}}^2} + \omega_s^2 \left(L_1 - \dfrac{1}{\omega_s^2 \times C_{\mathrm{s}}}\right)^2}, \qquad (4.8)$$

where, R_{eq} is equivalent load impedance at rectifier input. Owing to this load dependent compensation, either the inverter switching frequency has to vary dynamically or C_{p} has to change dynamically to operate the converter at resonant point. Fig. 4.7a shows the magnitude and phase of input impedance of a typical parallel-series/series converter with this conventional design. The circuit parameters are listed in Table 4.1. Clearly, resonant point shifts with the change of load power. Therefore, fixed switching frequency operation fails to operate the system efficiently. This is especially prominent at light load due to large power factor angle at inverter output as shown in Fig. 4.7a. However, Fig. 4.7a shows that there exist a load independent resonance frequency, which can enable simple fixed frequency operation of the inverter.

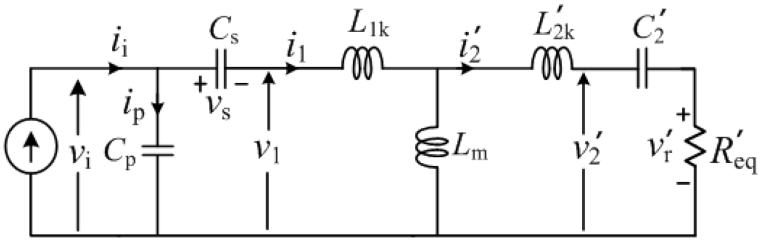


Fig. 4.6 Equivalent circuit with respect to the transmitter side

Table 4.1. Selected circuit parameters

Parameters	Values
Self-inductances of TC and RC	131.5 μH, 137.5 μH
Mutual inductance, M	30 μH
Compensation capacitors, C_p, C_s, C_2	154 nF, 154 nF, 81.2 nF
Switching frequency, f_s	50 kHz
Rated load power, P_o	1600 W
Rated input voltage, v_d	200 V
Rated output voltage, v_o	450 V
Input inductor, L_d	1.4 mH
Output capacitors, C_{o1}, C_{o2}	15 μF, 15 μF

To determine this particular operation, a rigorous mathematical analysis of Fig. 4.6 circuit is performed. Since, selection of RC side compensation using (4.7) leads to load dependent resonance; therefore, in this proposed method, $\omega_s L_2 = 1/\omega_s C_2$ simplification is not done. The input impedance of the Fig. 4.6 circuit—i.e., output impedance of inverter is derived as

$$Z_i = \frac{1}{Y_{re} + jY_{im}} = \left[j\omega L_m // \left\{ R'_{eq} + j\left(\omega L'_{2k} - \frac{1}{\omega C'_2} \right) \right\} + j(\omega L_{1k} - \frac{1}{\omega C_s}) \right] // \frac{1}{j\omega C_p}, \quad (4.9)$$

where, the equivalent magnetizing and leakage impedances of the coupled coils are derived as

$$\begin{aligned} L_{1k} &= L_1 - nM, \\ L_m &= nM, \\ L_{2k} &= L_2 - {}^{M}/_{n}, \end{aligned} \quad (4.10)$$

and TC to RC turns ratio is n. From (4.9) the complex (imaginary) part of input impedance is derived as

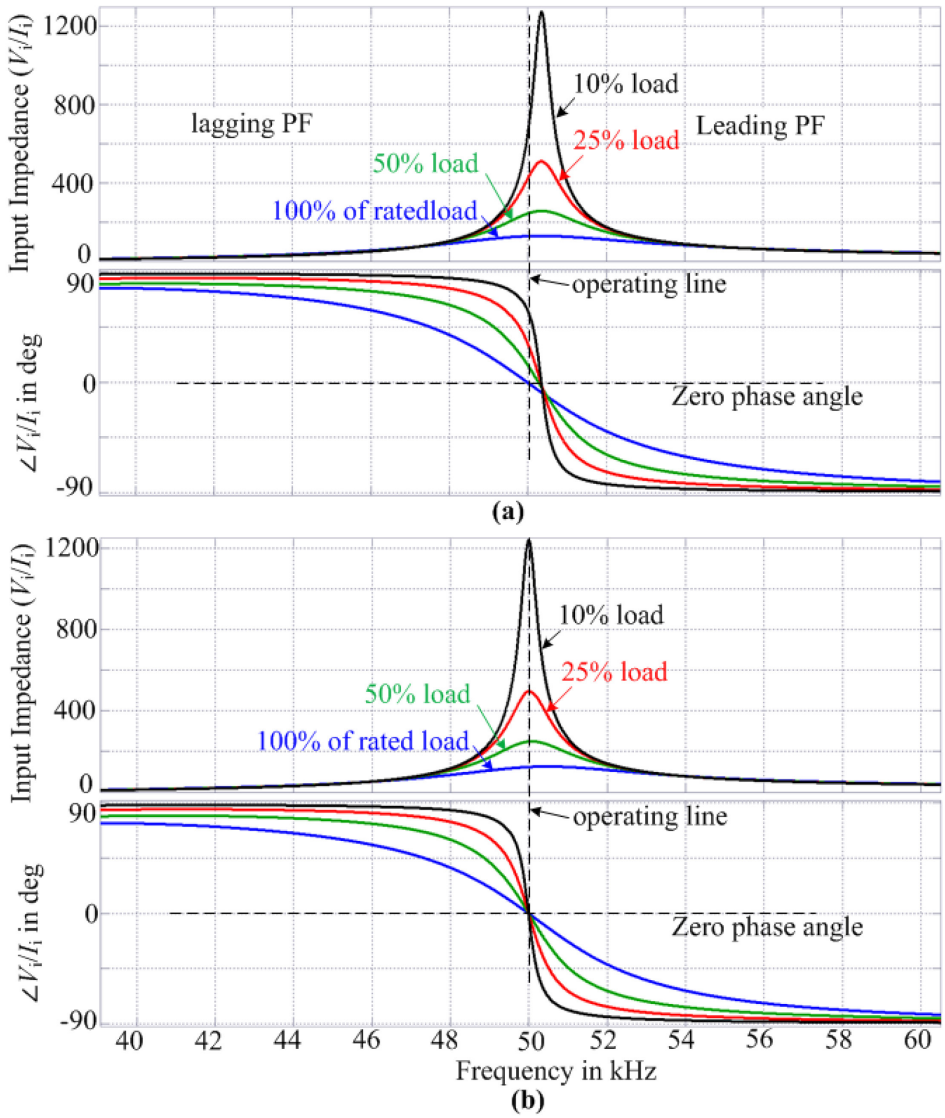


Fig. 4.7 ZPA operation with (a) existing design and (b) proposed design

$$Y_{\text{im}} = \frac{1}{t^2 + R_{\text{eq}}'^2\{X_{\text{m}} + (X_{1\text{k}} - X_{\text{s}})\}^2}\Big[R_{\text{eq}}'^2\{X_{\text{m}} + (X_{1\text{k}} - X_{\text{s}})\}\big[\{X_{\text{m}} + (X_{1\text{k}} - X_{\text{s}})\}/X_{\text{p}} - 1\big] - t\big[X_{\text{m}} - (X_{2\text{k}}' - X_2') + t/X_{\text{p}}\big]\Big] \quad (4.11)$$

where, all 'X' represents the impedance of particular element, e.g. $X_{\text{m}}=\omega L_{\text{m}}$, $X_2' = 1/\omega C_2'$ etc. and

$$t = X_{\text{m}}(X_{2\text{k}}' - X_2') + X_{\text{m}}(X_{1\text{k}} - X_{\text{s}}) + (X_{1\text{k}} - X_{\text{s}})(X_{2\text{k}}' - X_2') \quad (4.12)$$

From (4.11) it is clear that to make Y_{im} zero, the two parts of the equation has to be zero individually, i.e.

$$R_{\mathrm{eq}}'^{2}\{X_{\mathrm{m}}+(X_{1\mathrm{k}}-X_{\mathrm{s}})\}\left[\{X_{\mathrm{m}}+(X_{1\mathrm{k}}-X_{\mathrm{s}})\}/X_{\mathrm{p}}-1\right]=0, \quad (4.13)$$

$$t\left[X_{\mathrm{m}}-(X_{2\mathrm{k}}'-X_{2}')+t/X_{\mathrm{p}}\right]=0. \quad (4.14)$$

From (4.13) the first condition for resonance is derived as

$$\left[\{X_{\mathrm{m}}+(X_{1\mathrm{k}}-X_{\mathrm{s}})\}/X_{\mathrm{p}}-1\right] \quad (4.15)$$

This expression directly provides the value of TC side compensation capacitors as

$$C_{\mathrm{p}}//C_{\mathrm{s}}={}^{1}/_{\omega_{s}^{2}L_{1}} \quad (4.16)$$

The second condition of resonance in (4.14) has two parts. Since, making second part of (4.14) zero leads to C_2=0; therefore, the first part of it has to be zero, i.e. t=0. Considering, t=0 and using (4.12) and (4.16), the second condition leads to the appropriate value of RC side compensation capacitor as

$$X_{2}'=X_{2\mathrm{k}}'-\frac{X_{\mathrm{m}}(X_{1\mathrm{k}}-X_{\mathrm{s}})}{X_{\mathrm{m}}+(X_{1\mathrm{k}}-X_{\mathrm{s}})}. \quad (4.17)$$

Clearly, both the conditions derived in (4.16) and (4.17) do not contain load impedance. Therefore, this passive selection of components leads to load independent resonance. To verify the performance of this newly designed tank, the input impedance and phase is plotted in Fig. 4.7b. Clearly, the power factor at inverter output always remain unity, irrespective of wide load variations. This operation directly reduces the control effort of inverter compared with existing dynamic tuning methods. Therefore, inverter control is fully focus on meeting load demand, where the existing parallel compensated typologies require extra dc-dc chopper at the output side to achieve it.

4.3.2 (*L*)(*C*) Transmitter and (LC) Receiver Tank

Fig. 4.8 shows transformer equivalent circuit of the (*L*)(*C*) transmitter and (LC) receiver tank network, referred to transmitter side. Following the same design steps, the load independent compensation circuit parameters are derived. The final expressions are given as

$$C_{\mathrm{t}}={}^{1}/_{\omega_{s}^{2}L_{1}} \quad (4.18)$$

$$C_2' = \left[\omega_s \left(X_{2k}' - \frac{X_m X_{1k}}{X_m + X_{1k}}\right)\right]^{-1} \qquad (4.19)$$

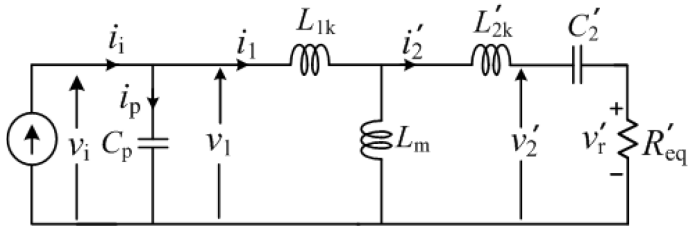


Fig. 4.8 Equivalent circuit with respect to the transmitter side

4.4 Proposed Two-loop Control

This section reports the complete small-signal modelling and controller design of (*C*)(*LC*) transmitter and (*LC*) receiver tank. Mathematically derived model is verified by the results obtained from frequency response analyzer (FRA). However, owing to similar design methods for (*L*)(*C*) transmitter and (*LC*) receiver tank, only final control to output transfer functions and the controller design are reported.

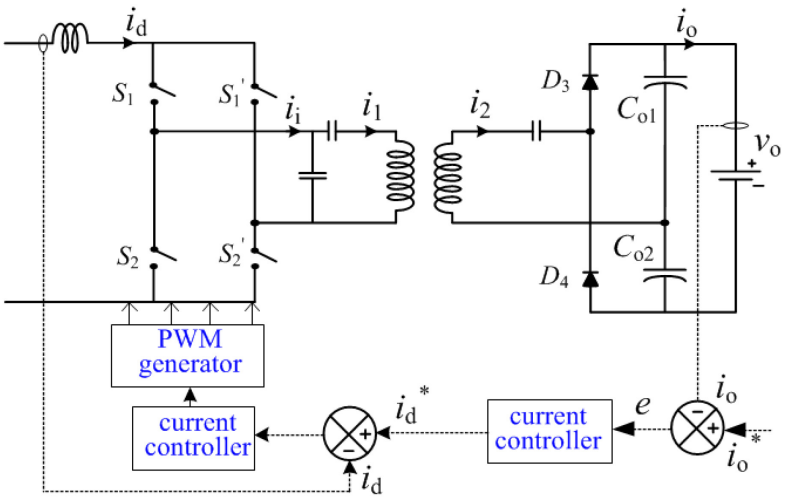


Fig. 4.9 Proposed control strategy for the PS/S topology

The converter circuit is controlled through two loop control method, where the outer output current loop meets the load demand and inner input current loop controls the input inductor current. Fig. 4.9 shows complete control loop diagram and this control scheme is same for both the IPT topologies. This type of two loop control for current-fed full bridge topology in fuel-cell

applications have been reported in [70], [71], [72]. The advantage of this two-loop control is that the stability margin of the system is very high. Also, using the faster inner current control loop the power transmission can be reduced abruptly from full load to very light load. This feature is very useful for practical implementation. Furthermore, this control of source current with boost-derived inverter can provide a single stage solution, where direct source current control using boost-chopper is required for effective extraction of energy from sources e.g. solar PV. The derivation of open-loop transfer function and controller design for both topologies are given as follows.

4.4.1 (*C*)(*LC*) Transmitter and (*LC*) Receiver Tank

4.4.1.1 Inner input current loop

The input to this loop is the duty cycle of the inverter and the output is inductor current. Fig. 4.10 shows a typical voltage and current waveform at the current-source inverter output where the voltage profile is sinusoidal and current is quasi-square. '*d*' is the duty cycle of the device S_1 or S_2 and 'α' represents phase-lag of current with respect to voltage. Although, the system is designed to achieve unity power factor at inverter output, but parameter variation of tank elements may lead to slight drift. This practical aspect is considered in modeling of the converter. The dynamic expression of the input inductor voltage is given as

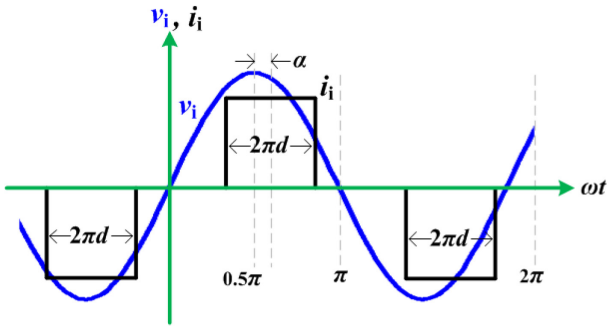


Fig. 4.10 Inverter output voltage and current waveform

$$L_d \frac{di_d}{dt} = v_d - v_x. \qquad (4.20)$$

Considering the duty cycle of inverter device S_1 as $0 \leq d \leq 0.5$, the instantaneous input voltage of the inverter in terms of output RMS voltage is derived as

$$v_{\mathrm{x}} = \frac{2\sqrt{2}}{\pi} V_{\mathrm{i}} \times \cos\alpha \times \sin\pi d\,. \qquad (4.21)$$

The storage elements (L_1, L_2, C_{s}, C_{p}, C_2) in the tank network predominantly carry fundamental component of switching frequency. Therefore, their dynamics are much faster compared with the dc side parameters. Considering negligible power losses in tank network, the power balance expression is given as

$$V_{\mathrm{i}}\, I_{\mathrm{i}} \times \cos\alpha = V_{\mathrm{r}} I_2\,. \qquad (4.22)$$

Since, the inverter output voltage is very close to sinusoidal, the active power transfer occurs only with fundamental component of I_{i}. Therefore, (4.22) is modified as

$$V_{\mathrm{i}} \cos\alpha = \frac{V_{\mathrm{r}} \left(\frac{V_{\mathrm{r}}}{R_{\mathrm{eq}}}\right)}{I_{\mathrm{i}}} = \left(\frac{V_{\mathrm{r}}}{I_{\mathrm{i}}}\right)^2 \times \frac{I_{\mathrm{i}}}{R_{\mathrm{eq}}} = \frac{A^2}{R_{\mathrm{eq}}}\left[\frac{2\sqrt{2}}{\pi} i_{\mathrm{d}} \times \sin\pi d\right], \qquad (4.23)$$

where, $A = V_{\mathrm{r}}/I_{\mathrm{i}}$= gain of the tank network at operating frequency. Feeding (4.21) and (4.23) in (4.20), the dynamic expression is modified as

$$L_d \frac{di_{\mathrm{d}}}{dt} = v_d - \frac{4\,A^2}{\pi^2 R_{\mathrm{eq}}} \times i_{\mathrm{d}}(1 - \cos 2\pi d)\,. \qquad (4.24)$$

Introducing small perturbations ($\tilde{\imath}_{\mathrm{d}}$, $\tilde{v}_{\mathrm{d}}$, $\tilde{d}$), around an equilibrium point (I_{d}, V_{d}, D) and neglecting second order terms, the small signal dynamic expression is derived from (4.24) as

$$L_{\mathrm{d}} \frac{d\tilde{\imath}_{\mathrm{d}}}{dt} = \tilde{v}_{\mathrm{d}} - \frac{4\,A^2}{\pi^2 R_{\mathrm{eq}}}\left[\tilde{\imath}_{\mathrm{d}}(1 - \cos 2\pi D) + 2\pi\, I_{\mathrm{d}}\, \tilde{d} \sin 2\pi D\right] \qquad (4.25)$$

Applying Laplace transformation, the control to output transfer function of inner loop is derived from as

$$G_{\mathrm{i}}(s) = \frac{\tilde{\imath}_{\mathrm{d}}(s)}{\tilde{d}(s)} = -\frac{\frac{8\,A^2}{\pi\, R_{\mathrm{eq}}} I_{\mathrm{d}} \sin 2\pi D}{sL_{\mathrm{d}} + \frac{4\,A^2}{\pi^2 R_{\mathrm{eq}}}(1 - \cos 2\pi D)} \qquad (4.26)$$

This simple first order system can be easily compensated using integral or PI controller to achieve the required closed performances. Fig. 4.11 shows the frequency response of $G_{\mathrm{i}}(s)$ for a set of circuit parameters listed in Table 4.1. An integrator with gain 7.9 is used to achieve phase

margin of 87.8^0 and the corresponding gain cross-over frequency is 727 rad/s. This indicates a closed loop settling time around 5.5ms.

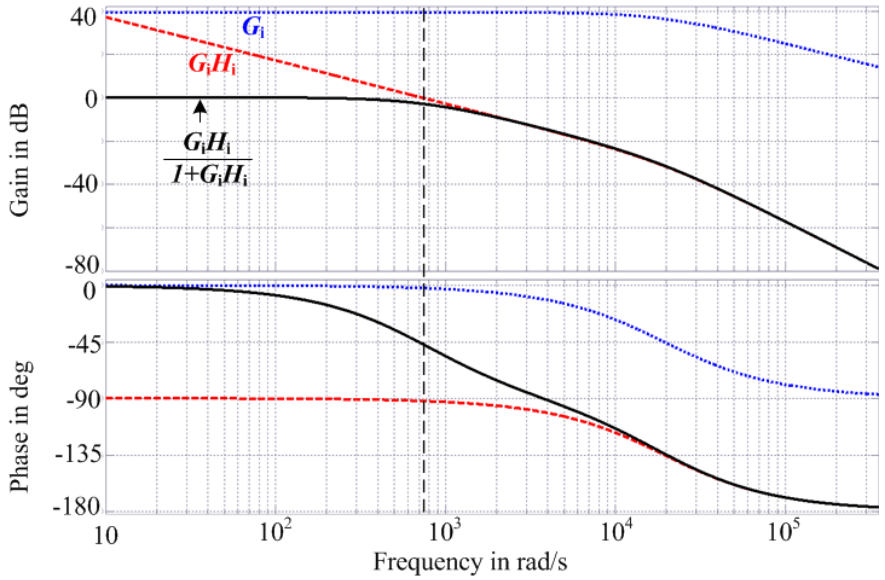


Fig. 4.11 Inner loop frequency response

4.4.1.2 Outer output current loop

The input to the outer loop is i_d and the output is load current, i_o. The outer loop control to output transfer function can be split as

$$G_o(s) = \frac{\tilde{\imath}_o(s)}{\tilde{\imath}_d(s)} = \frac{\tilde{\bar{I}}_\iota(s)}{\tilde{\imath}_d(s)} \cdot \frac{\tilde{\bar{V}}_r(s)}{\tilde{\bar{I}}_\iota(s)} \cdot \frac{\tilde{\imath}_o(s)}{\tilde{\bar{V}}_r(s)} = G_{inv} G_t G_{rec}. \tag{4.27}$$

These three transfer functions are inverter, resonant tank and rectifier transfer functions respectively. In (4.27), the dc side parameters are considered as average value over an inverter switching cycle, where the ac side parameters are amplitude of that switching cycle. Extracting fundamental component of the quasi-square shaped current in Fig. 4.10 and introducing small perturbation, the inverter transfer function is derived as

$$G_{inv} = \frac{\tilde{\bar{I}}_\iota(s)}{\tilde{\imath}_d(s)} = \frac{4}{\pi} \sin \pi D \tag{4.28}$$

Applying Kirchhoff's current and voltage laws (KCL and KVL) in impedance network diagram shown in Fig. 4.6, the tank network gain is derived as

$$\frac{\widetilde{\widehat{V}}_{\mathrm{r}}(s)}{\widetilde{\widehat{I}}_{\iota}(s)} = G_{\mathrm{t}} = \left[\left(1 + sC_{\mathrm{p}}Z_1\right)\left\{\frac{1}{R'_{\mathrm{eq}}} + \frac{1}{sM}\left(1 + \frac{Z_2}{R'_{\mathrm{eq}}}\right)\right\} + sC_{\mathrm{p}}\left(1 + \frac{Z_2}{R'_{\mathrm{eq}}}\right)\right]^{-1}, \quad (4.29)$$

where,

$$\begin{aligned} Z_1 &= sL_{1\mathrm{k}} + 1/sC_{\mathrm{p}}\,, \\ Z_2 &= sL'_{2\mathrm{k}} + 1/sC'_2\,. \end{aligned} \quad (4.30)$$

The gain of the resonant tank for different load impedance (R_{o}) is plotted in Fig. 4.12. The relation between A and G_{t} is that A indicates value of G_{t} at rated load and operating frequency—i.e., $A = G_{\mathrm{t}}(\omega_{\mathrm{s}})$ at rated load.

The dynamic expressions of the output capacitors for a given inverter switching cycle are given as

$$C_{\mathrm{o1}}\frac{dv_{\mathrm{o1}}}{dt} = 0.5\langle i_2\rangle - i_{\mathrm{o}}\,, \quad (4.31)$$

$$C_{\mathrm{o2}}\frac{dv_{\mathrm{o2}}}{dt} = 0.5\langle i_2\rangle - i_{\mathrm{o}}\,, \quad (4.32)$$

where, C_{o1} and C_{o2} are two output capacitors, v_{o1} and v_{o2} are their voltages respectively. All these state variables are considered to be average values over a switching cycle. Since, i_2 is switching frequency ac quantity and its average value over a switching cycle is zero; therefore, half cycle average of i_2 i.e. $\langle i_2\rangle$ is considered. Assuming, C_{o1}=C_{o2}=C_{o}, the dynamic expression is derived by adding (4.31) and (4.32) as

$$C_{\mathrm{o}}\frac{d(E + i_{\mathrm{o}}r_{\mathrm{b}})}{dt} = \frac{2}{\pi}\frac{\widehat{V}_{\mathrm{r}}}{R_{\mathrm{eq}}} - 2i_{\mathrm{o}}\,, \quad (4.33)$$

where, r_{b} and E are battery internal resistance and e.m.f. respectively. Introducing small perturbations and applying Laplace transformation, the gain expression is derived as

$$\frac{\tilde{\imath}_{\mathrm{o}}(s)}{\widetilde{\widehat{V}}_{\mathrm{r}}(s)} = \frac{2}{\pi} \times \frac{1/R_{\mathrm{eq}}}{sC_{\mathrm{o}}r_{\mathrm{b}} + 2}\,. \quad (4.34)$$

Therefore, the overall plant transfer function is derived as

$$G_{\mathrm{o}}(s) = \frac{8}{\pi^2}\frac{A}{R_{\mathrm{eq}}}\sin\pi d \times \frac{1}{sC_{\mathrm{o}}r_{\mathrm{b}} + 2} \quad (4.35)$$

The value of tank network gain at operating switching frequency, A_t is obtained from Fig. 4.12. The bode plot of the plant transfer function is shown in Fig. 4.13. A PI controller following gains is used to compensate the system

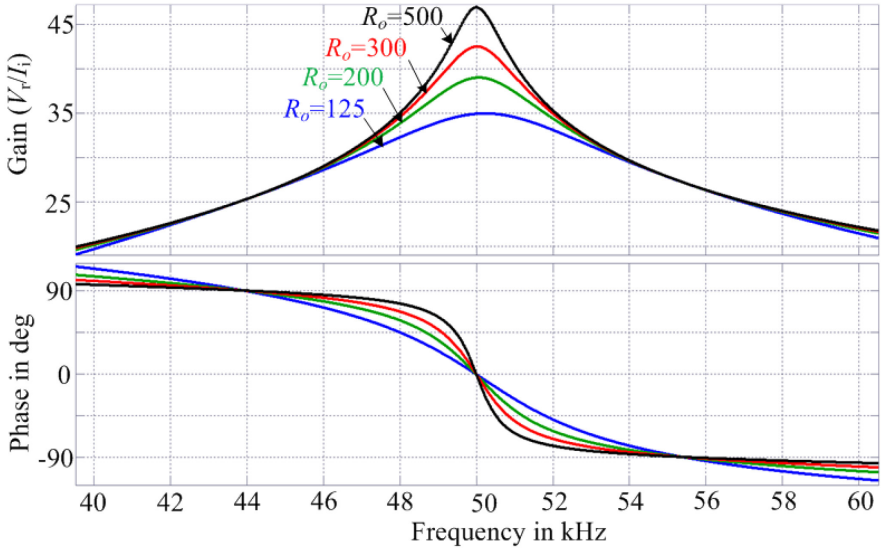


Fig. 4.12 Tank network gain in dB

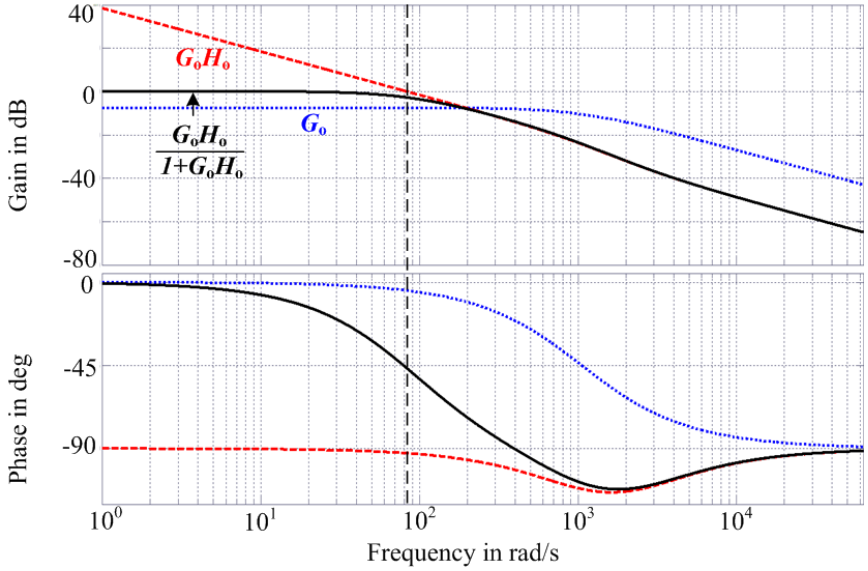


Fig. 4.13 Outer loop frequency response

$$H_o = 0.08 + 200/s\,. \qquad (4.36)$$

The frequency responses of both uncompensated and compensated systems are shown in Fig. 4.13. The phase margin of the compensated system is 87.4^0 and gain crossover frequency is 87.4rad/s, which indicates a closed loop settling time around 45ms.

4.4.1.3 Model verification

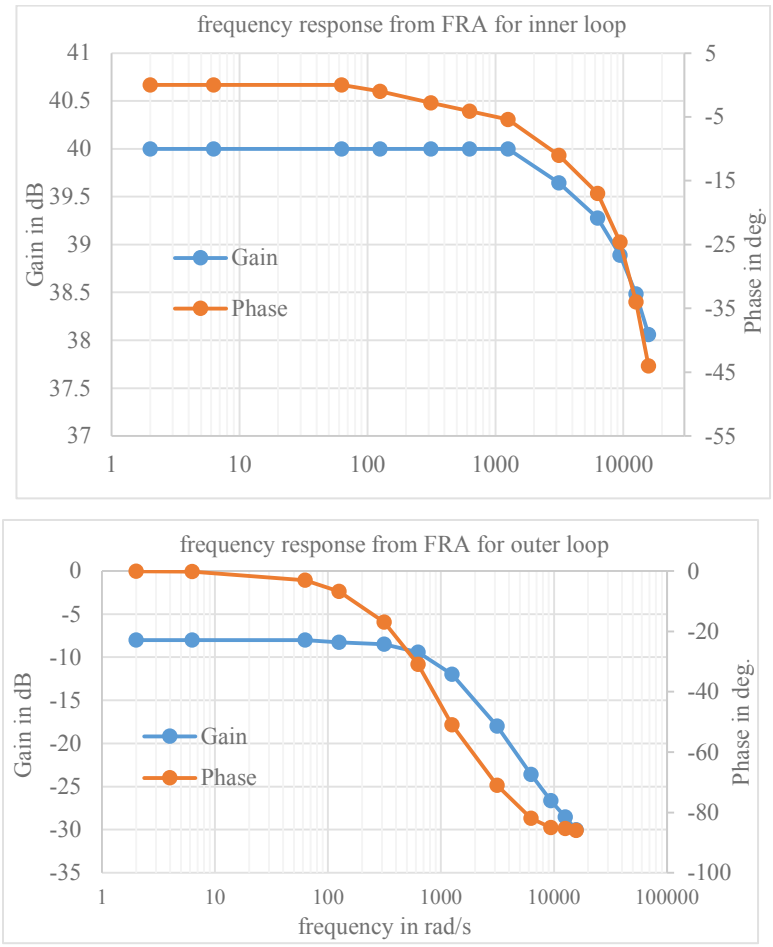


Fig. 4.14 Frequency responses obtained from FRA, (top) Open loop response of Inner loop, (bottom) Open loop response of outer loop

The transfer functions derived in (4.26) are (4.35) are verified using frequency response analyzer (FRA) in PowerSIM. Fig. 4.14a and 11b shows actual frequency response obtained from FRA for both the inner and outer loops respectively. For inner loop the gain $[\tilde{\imath}_{\mathrm{d}}(s)/\tilde{d}(s)]$ and phase are obtained by adding a variable frequency signal,

$$\tilde{d} = 0.01 \sin \omega t \qquad (4.37)$$

with inverter duty cycle D. The low frequency gain of G_{i}, obtained from Fig. 4.14a is 40dB, whereas the theoretical gain calculated from (4.26) is 39.3dB. Also, the phase plots obtained from both the methods follow similar characteristics. This verifies the mathematical model derived theoretically where the range of frequency is around $0<\omega<0.1\omega_{\mathrm{s}}$.

Similarly, for outer loop a small variable frequency sinusoidal signal,

$$\tilde{\imath}_{\mathrm{d}} = 0.5 \sin \omega t \qquad (4.38)$$

added with I_{d} to get outer loop gain and phase plots as shown in Fig. 4.14b. The low frequency gain of G_{o} calculated mathematically is 7.6dB, whereas Fig. 4.14b provides 8dB. Also, the calculated pole frequency of the system is at 1.06 *k*rad/s, whereas the approximate pole frequency obtained from FRA is almost same. These results validates the accuracy of the derived plant transfer functions.

4.4.2 (*L*)(*C*) Transmitter and (LC) Receiver Tank

4.4.2.1 Inner Loop

Following the same design steps, the inner loop plant transfer function of (*L*)(*C*) transmitter and (LC) receiver tank network is derived as

$$G_{\mathrm{i,LC}}(s) = \frac{\tilde{\imath}_{\mathrm{d}}(s)}{\tilde{d}(s)} = -\frac{\frac{8\,B^2}{\pi\,R_{\mathrm{eq}}} I_{\mathrm{d}} \sin 2\pi D}{sL_{\mathrm{d}} + \frac{4\,B^2}{\pi^2 R_{\mathrm{eq}}}(1 - \cos 2\pi D)} \qquad (4.39)$$

where, B is the gain of (*L*)(*C*) transmitter and (*LC*) receiver tank network at operating frequency.

Table 4.2. Selected Circuit Parameters

Parameters	Values
Compensation capacitors, C_{p}, C_2	77 *n*F, 81.2 *n*F
Rated load power, P_{o}	800 W
Rated output voltage, v_{o}	160 V

An integral controller with integral gain 25 is used to compensate the system and corresponding bode plots and stability margins are shown in Fig. 4.15. The circuit parameters are listed in Table 4.2 and the coil parameters are same as listed in Table 4.1. The phase margin of the compensated system is 88.6^0 and gain crossover frequency is 1142rad/s. This indicates a closed loop settling time around 3.5ms.

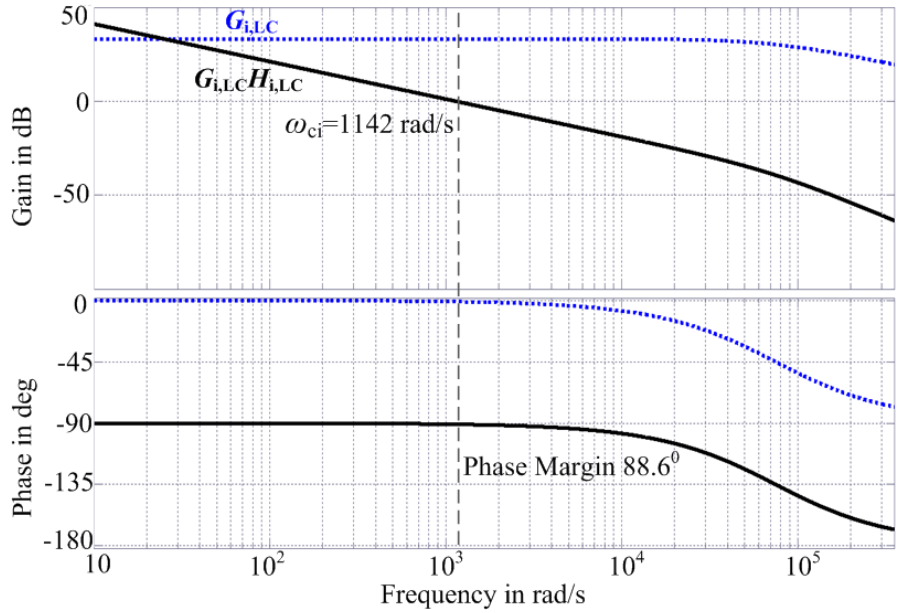


Fig. 4.15 Bode plot of inner input current loop

4.4.2.2 Outer Loop

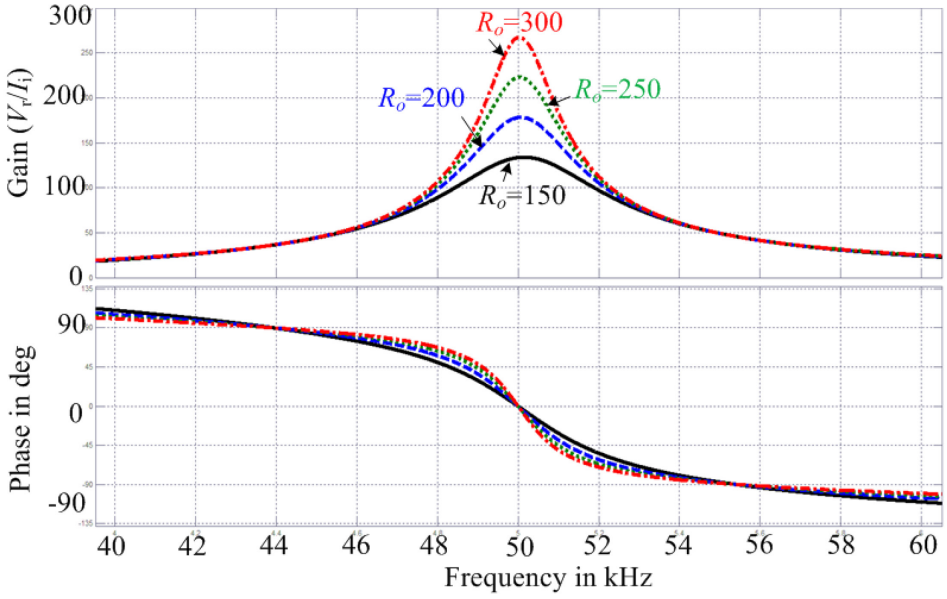


Fig. 4.16 Resonant tank gain for different load

Similar to earlier, the outer loop transfer function can be split into three parts—i.e., inverter, resonant tank, and rectifier transfer functions. From (4.27) it is clear that only resonant tank transfer function is different here, which is derived as

$$G_{\mathrm{t,LC}} = \frac{\widetilde{\widehat{V}}_{\mathrm{r}}(s)}{\widetilde{\widehat{I}}_{\iota}(s)} = \left[\left(1 + sC_{\mathrm{p}}sL_{1\mathrm{k}}\right)\left\{\frac{1}{R'_{\mathrm{eq}}} + \frac{1}{sM}\left(1 + \frac{sL'_{2\mathrm{k}} + 1/sC'_2}{R'_{\mathrm{eq}}}\right)\right\}\right. \quad (4.40)$$
$$\left. + sC_{\mathrm{p}}\left(1 + \frac{sL'_{2\mathrm{k}} + 1/sC'_2}{R'_{\mathrm{eq}}}\right)\right]^{-1}.$$

Frequency response of $G_{\mathrm{t,LC}}$ is shown in Fig. 4.16 for different load impedances (R_{o}). The relation between B and $G_{\mathrm{t,LC}}$ is that B indicates the value of $G_{\mathrm{t,LC}}$ at rated load and operating frequency—i.e., $B = G_{\mathrm{t,LC}}(\omega_{\mathrm{s}})$ at rated load.

The overall outer loop control transfer function is derived as

$$G_{\mathrm{o,LC}}(s) = \frac{\widetilde{\iota_{\mathrm{o}}}(s)}{\widetilde{\widehat{V}}_{\mathrm{r}}(s)} = \frac{8}{\pi^2}\frac{B}{R_{\mathrm{eq}}}\sin\pi d \times \frac{1}{sC_{\mathrm{o}}r_{\mathrm{b}} + 2} \quad (4.41)$$

Fig. 4.17 shows bode plot of outer loop plant transfer function. A PI Controller with following transfer function is used to get desired performance of the closed loop system.

$$H_{\mathrm{o,LC}}(s) = 0.05 + 130/\mathrm{s} \quad (4.42)$$

The phase margin of compensated system is 85.20 and gain crossover frequency 114.3rad/s indicates a closed loop settling time 35ms. Compensated system bode plot is shown in Fig. 4.17.

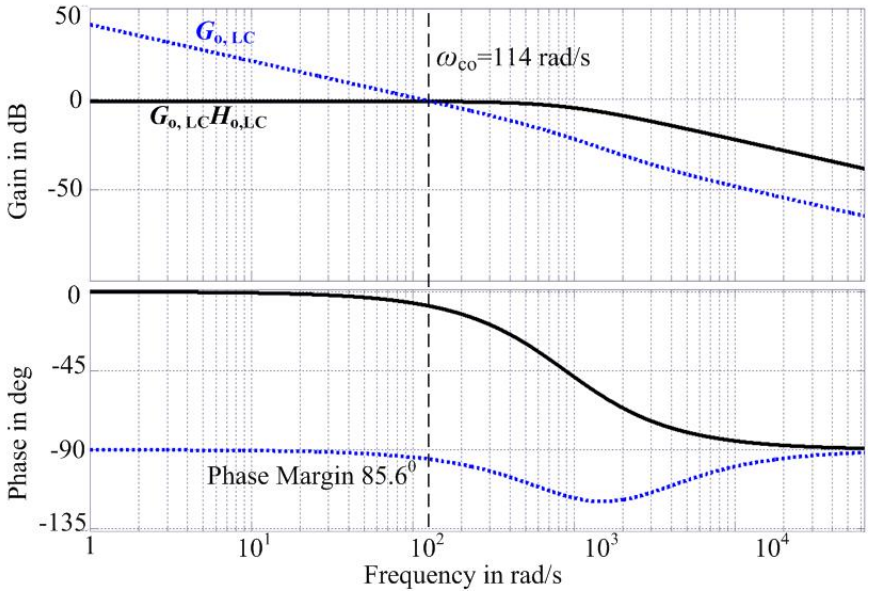


Fig. 4.17 Frequency response of outer loop

4.5 Experimental Results

To verify the performance of the proposed design and closed loop control of the two converters, a 1.6kW lab-prototype is developed and experimental results are reported in this Section. Fig. 4.18 shows the experimental set-up where the inverter and compensation circuit components are same as earlier. The voltage daoubler rrectifier diodes are fast recovery diodes with part number 40EPF06. IPT coils are circular type with 55cm diameter and TC to RC airgap is around 25cm. The coils are made from 4.5 sq. mm litz wire. Since, the main focus of this Chapter is to verify the performance of converter circuit; therefore, this standard circular coil is selected, and coil design and optimization is not elaborated. Details of this circular coil design can be found in [52].

Experimental results have three subsections. First subsection reports the results to verify the proposed ZPA operation. Second and third subsections report steady-state and dynamic response results of the two IPT topologies, respectively.

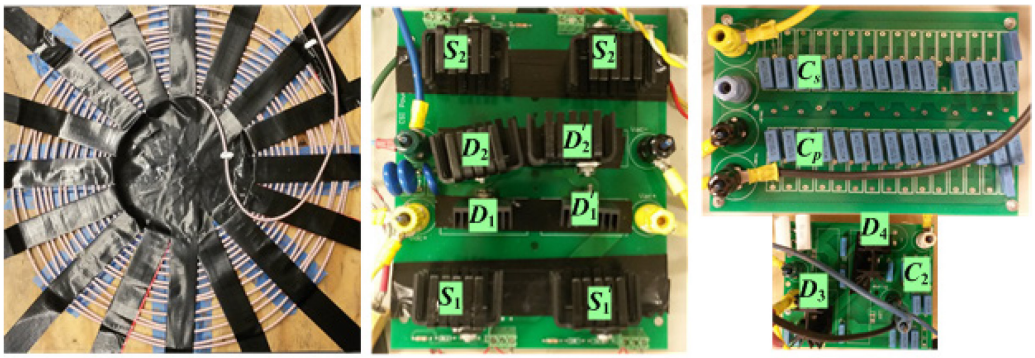


Fig. 4.18 1.6 kW experimental set-up built in laboratory

4.5.1 Verification of Load-Independent ZPA Operation

This subsection reports the experimental results to verify ZPA operation of *CLC* transmitter and *LC* receiver tank

4.5.1.1 With Resistive Load

Fig. 4.19 and Fig. 4.20 show the experimental results for 1*k*W and 550W power output when load resistances are 21Ω and 41Ω respectively. It is clear from Fig. 4.19a and Fig. 4.20a that irrespective of change in load the proposed design is capable of maintaining ZPA operation. Therefore, inverter needs to supply the least amount of VA for a given load. This fixed frequency

operation is very convenient, whereas variable frequency operation involves complex circuitry and detection of frequency bifurcation, etc. Also, with this parallel compensated primary, the voltage at the inverter output, v_i is sinusoidal and this voltage directly appears across the inverter devices. Therefore, this unity power factor or ZPA operation directly facilitates ZVS turn-on and turn-off of inverter devices. Fig. 4.19b and Fig. 4.20b show the coil voltage and current profiles. These results show that parallel tank in primary side ensures high quality voltage and current profiles.

Fig.4.21 verifies the proposed load independent ZPA operation when there is an input disturbance. The dc link voltage of the inverter is reduced from 300V to zero, within 500ms. The zoomed waveforms of these results clearly show that the resonant tank is capable to operate at ZPA during this wide input disturbances.

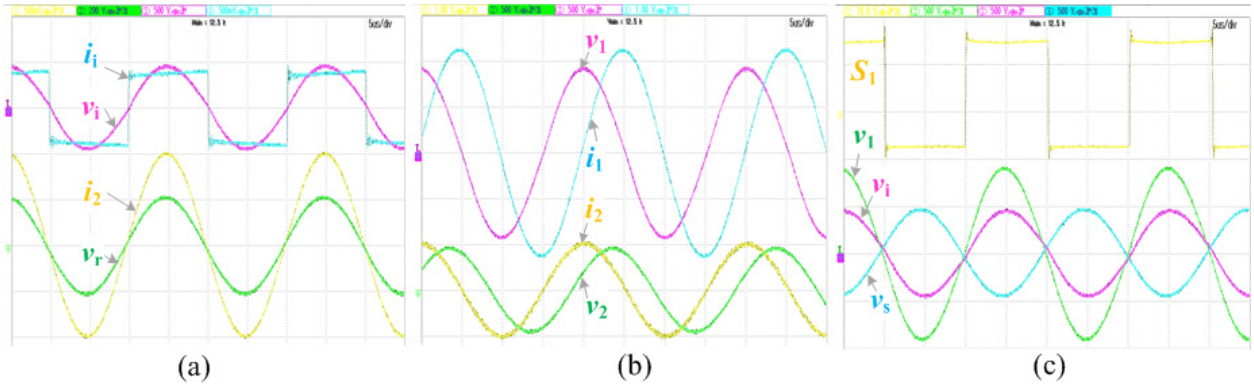


Fig. 4.19. ZPA operation at 50 *k*Hz, R_{eq}=21Ω, P_o=1*k*W (a) inverter output voltage (500v/div), current (5A/div), load voltage (200v/div) and current (5A/div); (b) primary and secondary coil voltages (500v/div) and currents (10A/div); (c) gating signal of S_1 and voltages across primary side tank network elements (500v/div)

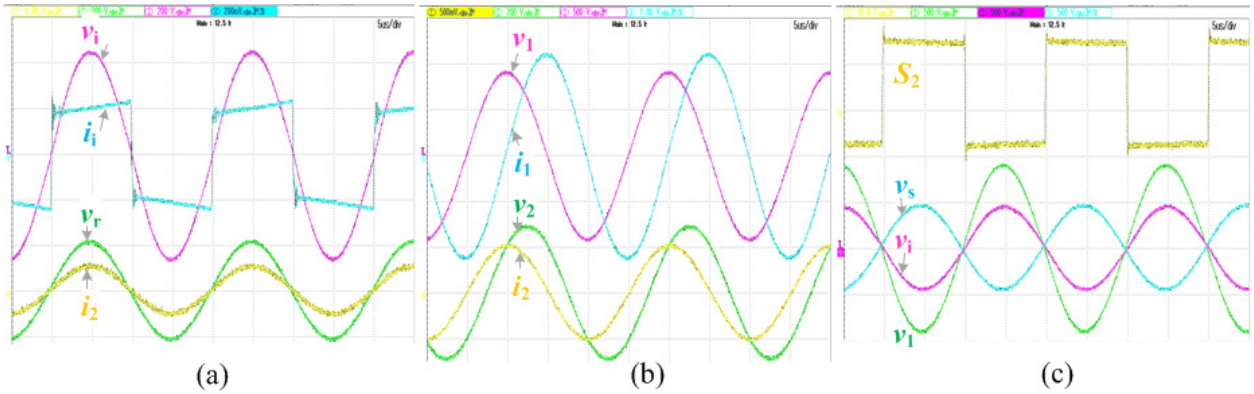


Fig. 4.20. ZPA operation at 50 *k*Hz, R_{eq}=41Ω, P_o=550W (a) v_i (200v/div) and i_i (2A/div), v_r (200v/div) and i_2 (10A/div); (b) v_1 (500v/div) and i_1 (10A/div) and v_2 (200v/div) and i_2 (5A/div); (c) gating signal of S_2 and voltages across primary side tank network elements (500v/div)

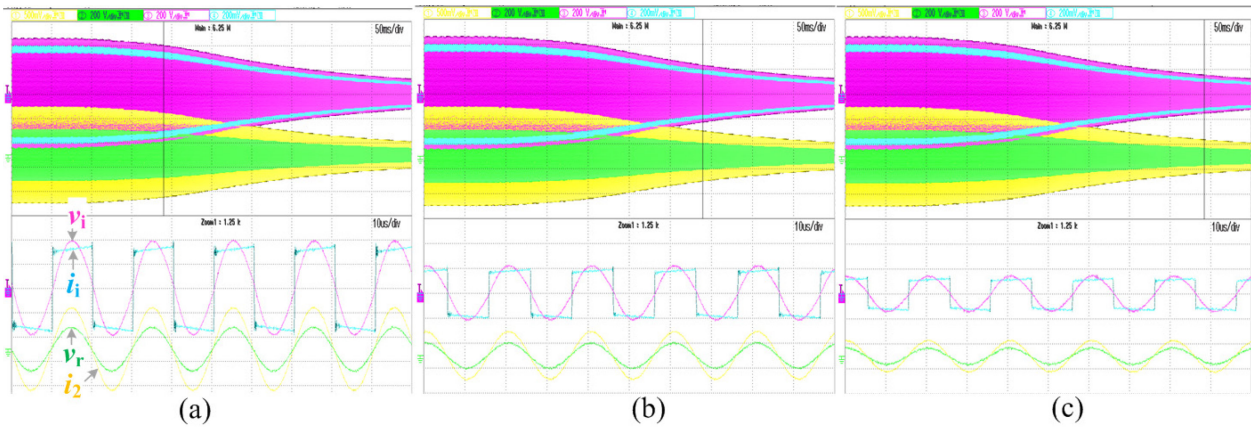


Fig.4.21 Verification of ZPA operation with input disturbance when input dc link voltage, v_d is reduced from rated value (300V) to zero: v_i [200v/div], i_i [2A/div], v_r [200v/div], i_2 [5A/div]

4.5.1.2 With Stiff-voltage Load

Fig.4.22 and Fig.4.23 show experimental results for 1*k*W and 500W power output, respectively, where load type is stiff dc voltage, connected after the rectifier. This is like a battery connected at the rectifier output. These results further verify that the proposed design for achieving ZPA is insensitive to load change. Fig.4.24 shows the performance of the converter when source voltage is changed from 150V to 300V within 50ms. The zoomed view of Fig.4.24—before, during and after the disturbance show that inverter operates always at unity displacement power factor. Therefore, inverter mainly supplies the real power and it ensures least voltage and current rating of the devices.

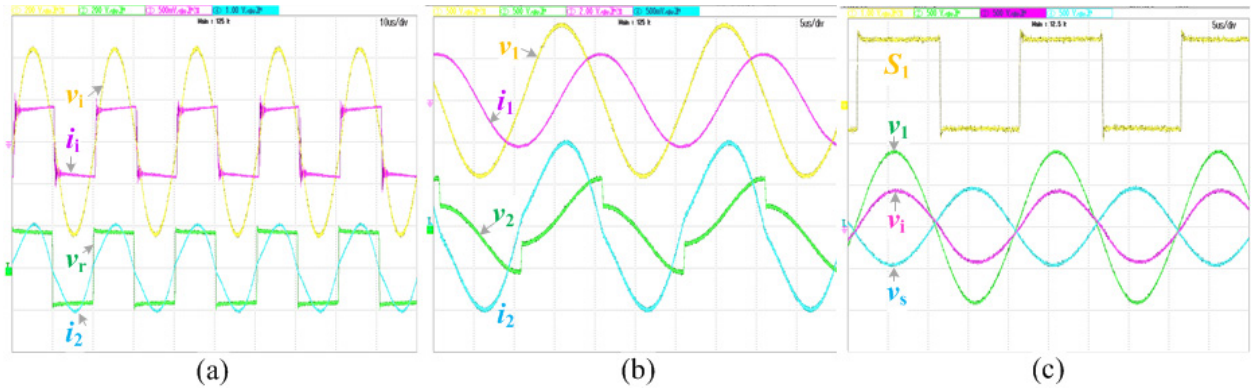


Fig.4.22 ZPA operation at 50 *k*Hz, V_o=175V, P_o=1kW (a) v_i (200v/div) and i_i (5A/div), v_r (200v/div) and i_2 (10A/div); (b) v_1 (500v/div) and i_1 (20A/div) and v_2 (500v/div) and i_2 (5A/div); (c) gating signal of S_2 and voltages across primary side tank network elements (500v/div)

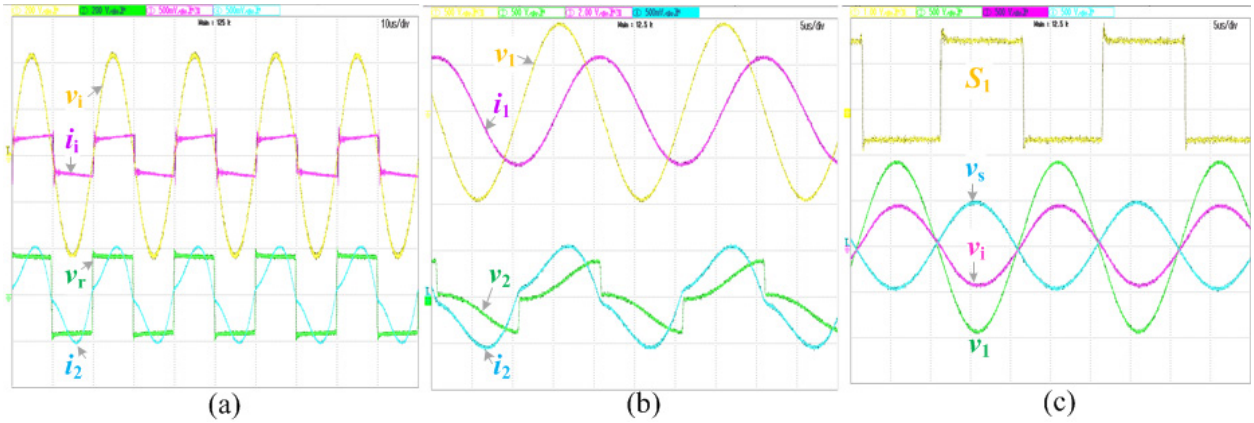


Fig.4.23 ZPA operation at 50 *k*Hz, V_o=175V, P_o=500W (a) v_i (200v/div) and i_i (5A/div), v_r (200v/div) and i_2 (5A/div); (b) v_1 (500v/div) and i_1 (20A/div) and v_2 (500v/div) and i_2 (5A/div); (c) gating signal of S_2 and voltages across primary side tank network elements (500v/div)

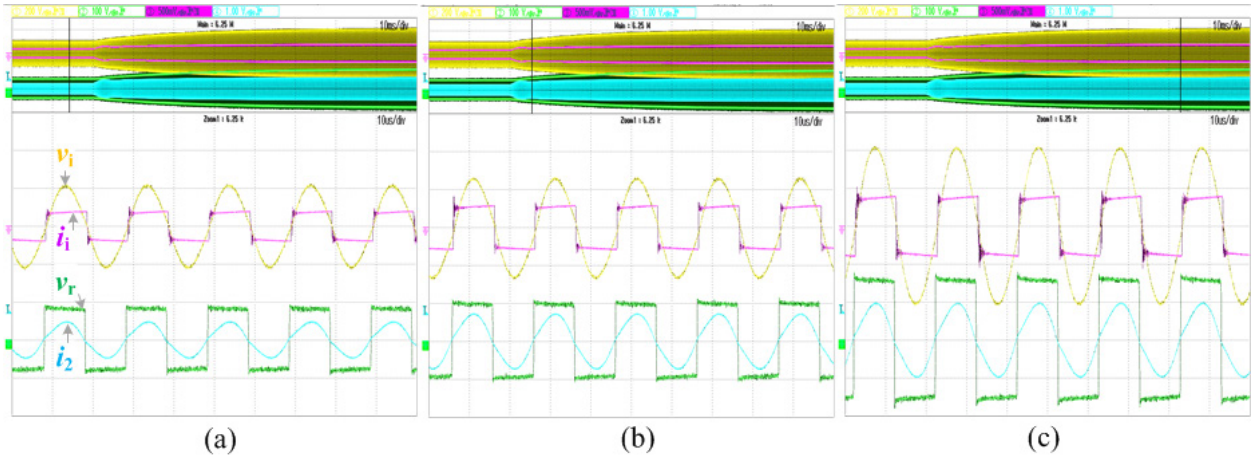


Fig.4.24 Verification of ZPA operation with input disturbance when input dc link voltage, v_d is reduced from rated value (300V) to half: v_i [200v/div], i_i [5A/div], v_r [100v/div], i_2 [10A/div]

4.5.2 Results with parallel *CLC* tank

Although, steady-state results of parallel *CLC* tank are reported in Chapter 3, but unipolar PWM scheme modifies the operation and performance significantly. The boost mode operation of current-fed inverter is properly realized with unipolar PWM. Therefore, the steady state operation is briefly reported first, followed by detailed dynamic performance results.

4.5.2.1 Steady State Operation with Unipolar PWM

Fig. 4.25, Fig. 4.26 and Fig. 4.27 show steady state experimental results for 1.6kW (100%), 800W (50%) and 320W (20%) power output. Fig. 4.25a, Fig. 4.26a and Fig. 4.27a show voltage and current profiles at inverter output and rectifier input. Clearly, even with wide load variations,

the inverter output voltage remains very close to sinusoidal where the current is quasi-square. This profile is expected from analysis that the parallel capacitor, C_p provides much lower impedance to higher order harmonics of i_i compared with TC path. Also, the rectifier input current is continuous even at light load. Since it passes through a *LC* series tuned circuit; therefore, the profile is close to sinusoidal. This verifies the assumption of power balance expression given in (4.22) that the active power at inverter output and rectifier input are due to fundamental component.

Fig. 4.25b, Fig. 4.26b and Fig. 4.27b show voltage and current profiles of TC and RC for three different loading conditions, respectively. Clearly, the coil currents, especially TC current is highly sinusoidal. This is desired in IPT system, because higher order harmonics in coils does not involve in active power transfer, but increases power loss and electromagnetic interference.

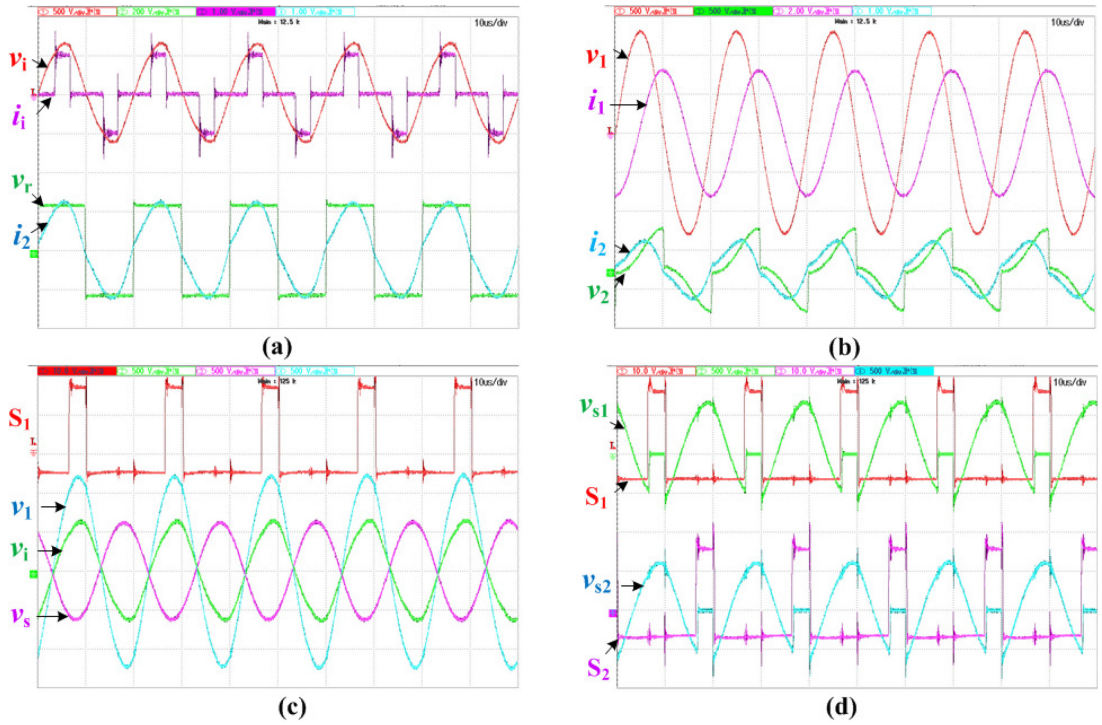


Fig. 4.25 Steady state operation at P_o=1610W **(a)** v_i [500v/div], i_i [10A/div], v_r [200v/div], i_2 [10A/div] **(b)** v_1 [500v/div], i_1 [20A/div], v_2 [500v/div], i_2 [20A/div] **(c)** S_1 and voltage across TC side tank elements [500v/div] **(d)** gating signals and voltages across device S_1 and S_2 [500v/div]

Fig. 4.25c, Fig. 4.26c and Fig. 4.27c show voltage across different tank elements in TC side and gating signal of S_1. These results show the merit of parallel-series tank over conventional parallel tank at TC side. The series capacitor, C_s directly reduces the leakage impedance of the coil;

therefore, the parallel capacitor, C_p provides only a fraction of reactive power consumed by TC. This directly reduces the magnitude of inverter output voltage, which leads to lower device voltage stress and higher output to input voltage gain.

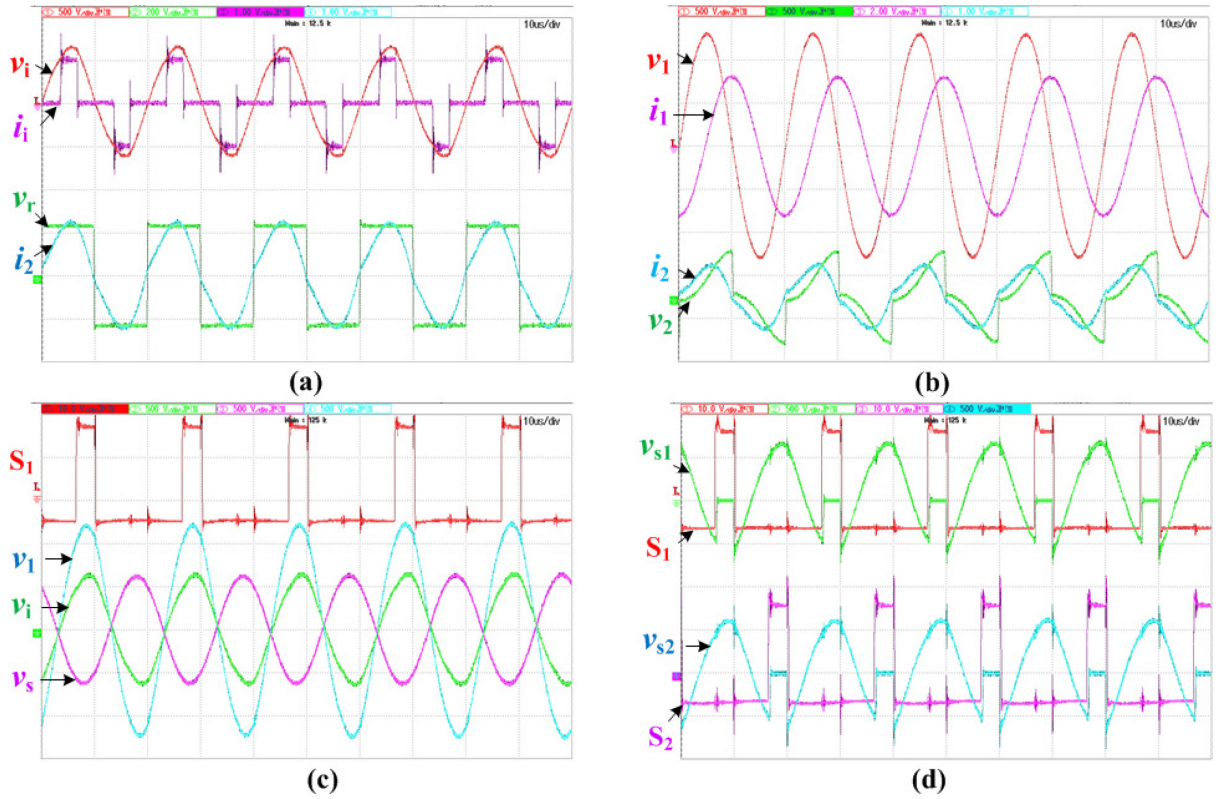


Fig. 4.26 Steady state operation at P_o=800W **(a)** v_i [200v/div] and i_i [5A/div], v_r [200v/div], i_2 [10A/div] **(b)** v_1 [500v/div], i_1 [20A/div], v_2 [200v/div], i_2 [10A/div] **(c)** S_1 and voltage across TC side tank elements [500v/div] **(d)** gating signals and voltages across device S_1 and S_2 [500v/div]

Fig. 4.25d, Fig. 4.26d and Fig. 4.27d show soft switching characteristics of inverter devices S_1 and S_2. Clearly, when S_1 is triggered, the voltage across it is negative. Therefore, S_1' keeps on conducting until the overlap region of S_1 and S_1' gets over. This leads to ZVS turn-on of S_1 and hard turn-off S_1'. At the end of this overlap period, the gating signal of S_1' becomes low and inverter current is transferred to from S_1' to S_1. In the other side however, S_1' receives turn-on signal when the voltage across it is positive. This results in immediate current transfer from S_1 to S_1'. Therefore, during this overlap period, the current through S_1 is zero and at the end of this period, the gating signal of S_1 is withdrawn when current is zero. This leads to ZCS turn-off of S1 and hard turn on of S_1'. Similar soft-switching characteristics of S_2 is observed in experimental results.

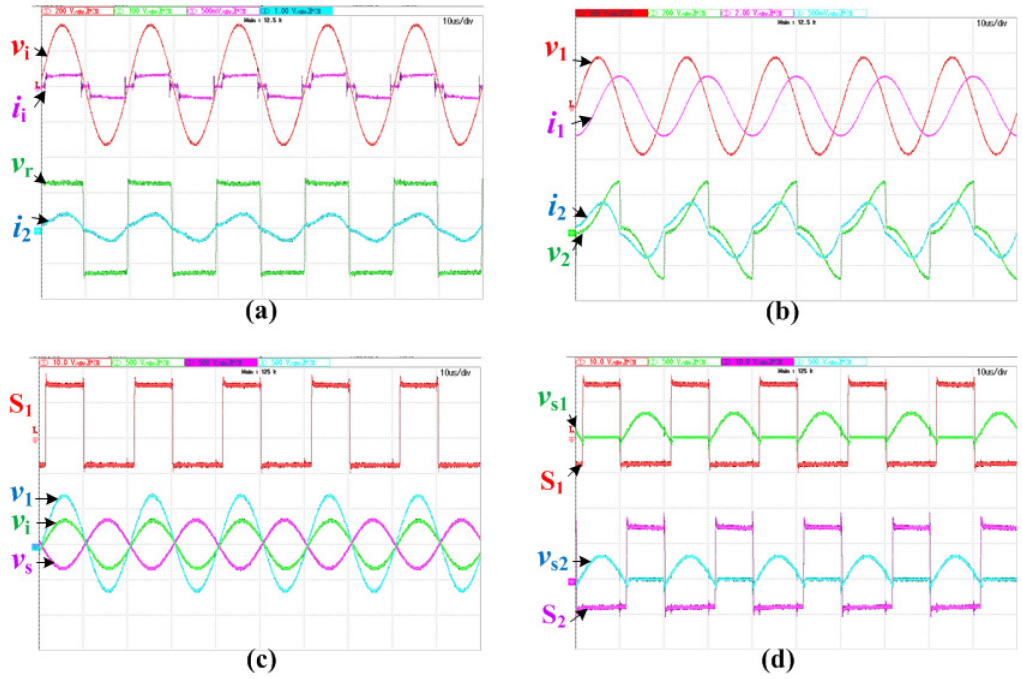


Fig. 4.27 Steady state operation at 20% of rated P_o [320W] **(a)** v_i [200v/div] and i_i [5A/div], v_r [100v/div] and i_2 [10A/div] **(b)** v_1 [500v/div], i_1 [20A/div], v_2 [200v/div] and i_2 [5A/div] **(c)** gating signal of S_1 and voltage across TC side tank elements [500v/div] **(d)** gating signals and voltages across device S_1 and S_2 [500v/div]

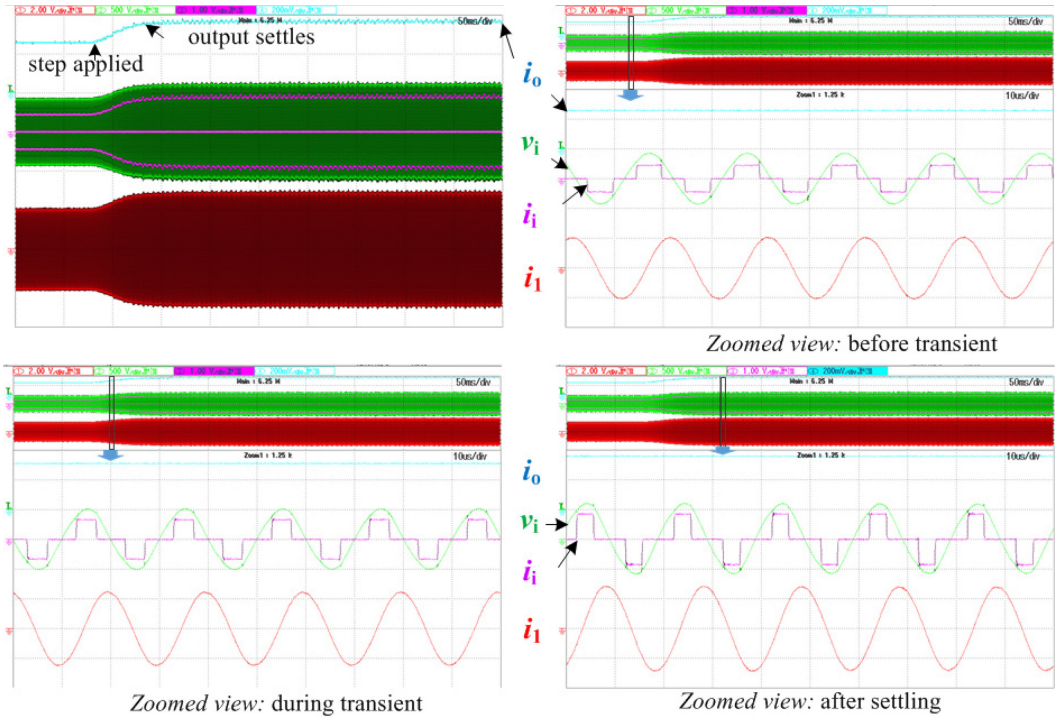


Fig. 4.28 Transient response results: step response for a load step command form 50% to 100% of rated load; load current [2A/div], inverter output voltage [500v/div] and current [10A/div], TC coil current [20A/div]

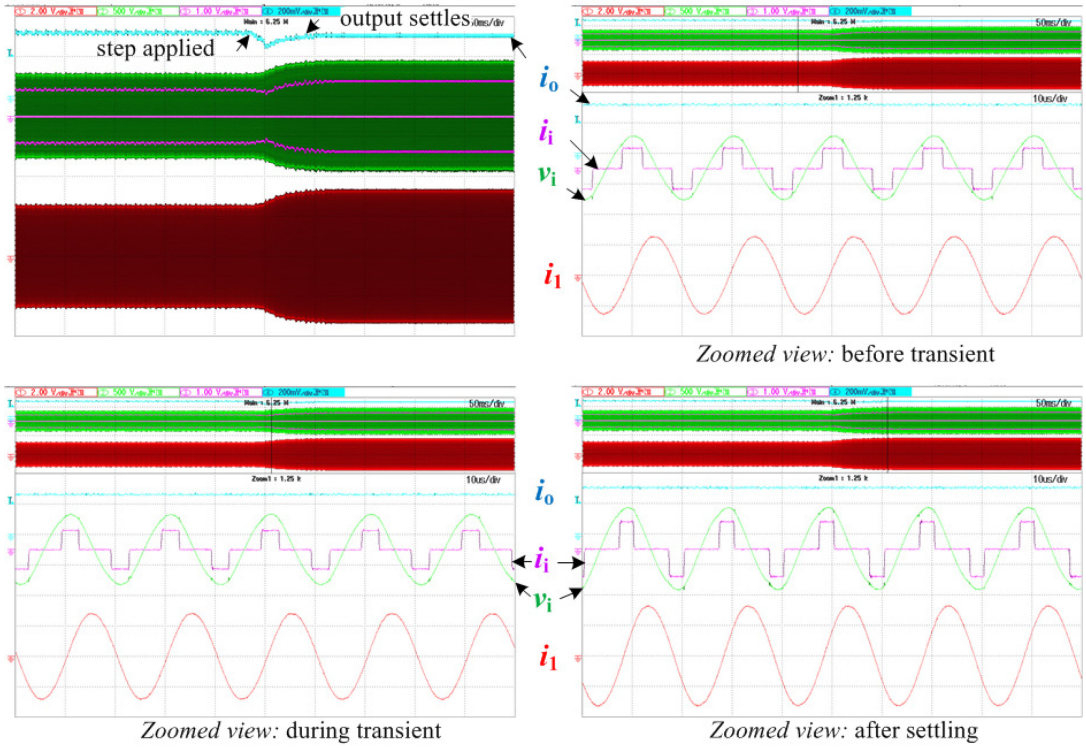


Fig. 4.29 Response in presence of disturbance when a 25% step change [175V-225V] in source voltage occurs: input voltage [100v/div], output current [2A/div], inverter output voltage [500v/div] and current [10A/div]

4.5.2.2 Transient Response Results

Fig. 4.28 shows dynamic performance of the proposed system when a 50% step command from 50% to 100% of rated load is given to output current reference. The output settles after around 45ms. This verifies the modelling, design and performance of the closed loop system. The zoomed view of this result before, during and after this transient shows the performance of the proposed converter design. Clearly, the inverter voltage is very close to sinusoidal and the current is quasi-square, while the inverter displacement power factor is unity. Therefore, the active power flow through inverter occurs only by fundamental component. Also, unity P.F. ensure least VA loading of inverter, thereby ensuring least rating and conduction loss of the devices. During this operation, the TC current profile remains very close to sinusoidal.

Fig. 4.29 and Fig. 4.30 show the performance of the closed loop system in presence of input and output disturbances respectively. In Fig. 4.29, a 25% step rise in input voltage from 175V to 225V is applied to the converter. This sudden increase in input voltage leads to slight rise in output current, which is restored to previous value within the settling time of outer loop. The zoomed

waveforms confirm the performance of the tank network that the inverter supplies least amount of VA required for given load. In Fig. 4.30, the load impedance is suddenly increased such that with same output current reference, the system has to deliver double power. Clearly, due to this abrupt reduction in load impedance the output current reduces at first, but the closed loop restores it. The zoomed waveform repeatedly shows the excellent performance of the load independent resonant tank.

To verify the performance of inner loop and to reduce power transfer abruptly during emergency situations, a step commend is directly given to inner input current loop as shown Fig. 4.31. The step change command in the i_d reference value (i_d^*) is around 85%. This leads to reduction in output power from rated to 15% of rated power. The input inductor current settles approximately in 5.5ms. This verifies the performance of the inner loop and suitability of two loop control method. The zoomed waveform shows the suitability of the proposed design of resonant tank that even at light load the inverter needs to supply only the active part of power.

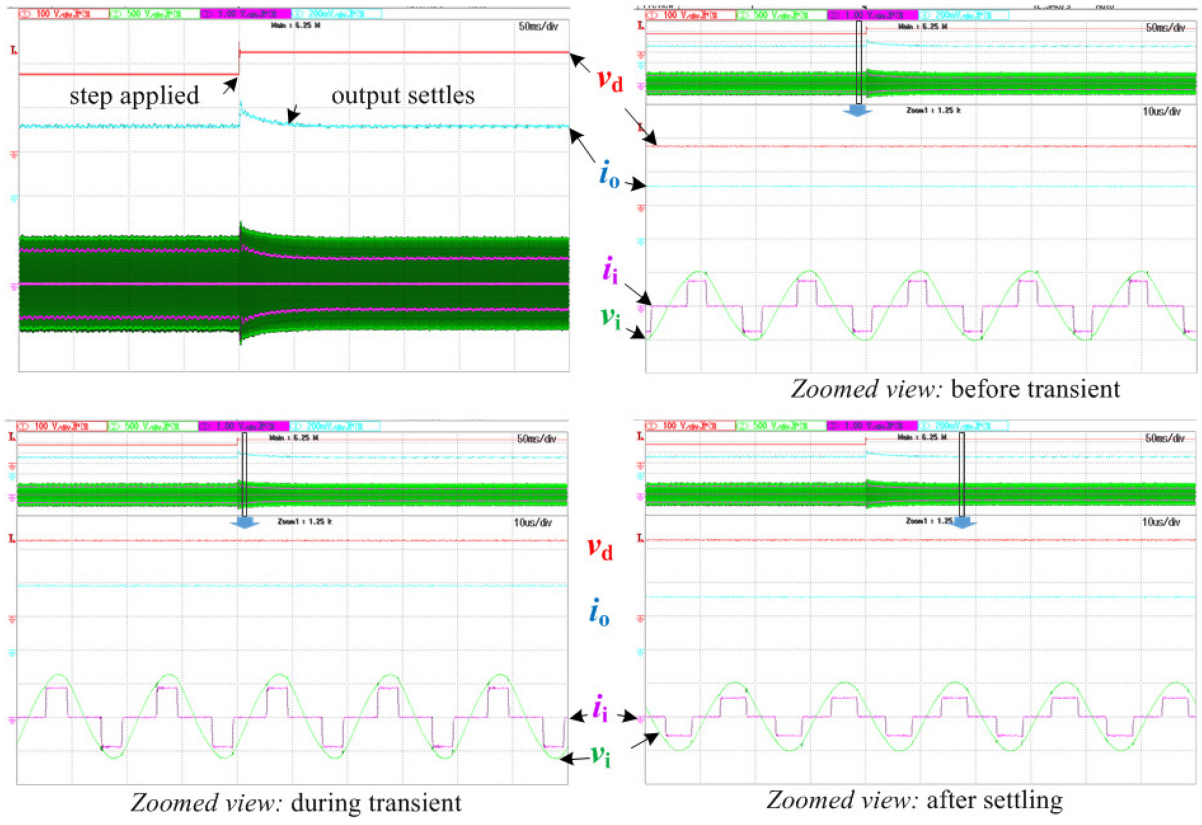


Fig. 4.30 Response in presence of disturbance when a 50% step change of load impedance occurs: output current [2A/div], inverter output voltage [500v/div] and current [10A/div] and TC coil current [10A/div]

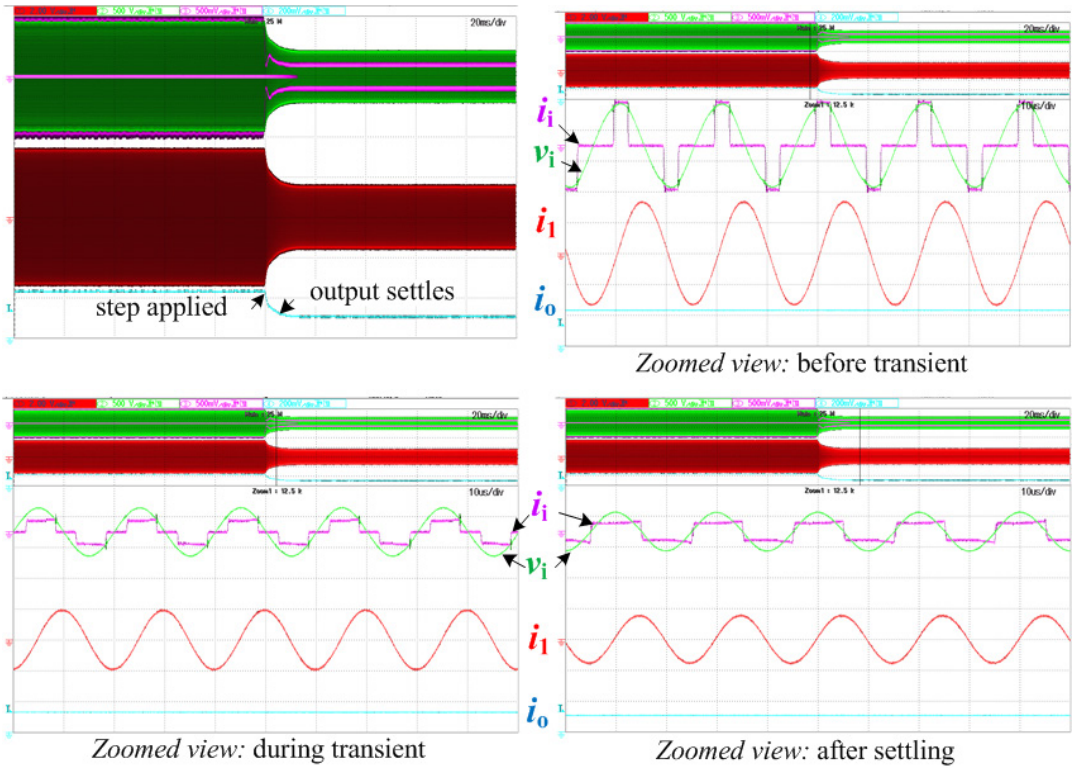


Fig. 4.31 Performance of inner loop when a step commend from 100% to 15% of rated input current applied: inverter output voltage [500v/div] and current [10A/div], TC coil current [10A/div] and output current [2A/div],

4.5.3 Results with Parallel *LC* Tank

This subsection briefly presents the steady state and dynamic response results of IPT topology with parallel resonant tank.

4.5.3.1 Steady State Results with Unipolar PWM

Fig. 4.32, Fig. 4.33 and Fig. 4.34 show steady state performance results of (*L*)(*C*) transmitter and (*LC*) receiver compensated IPT topology. The inverter modulation scheme is unipolar type. Owing to higher voltage stress on inverter devices, the rated power is only 800W, with the same IPT coil and inverter devices. Fig. 4.32, Fig. 4.33 and Fig. 4.34 show results for 800W (100%), 400W (50%) and 160W (20%) power outputs, respectively. Clearly, the inverter output current is quasi-square. Zero state of this quasi-square wave increases with higher power. This is exactly like a conventional boost-chopper. The inverter output voltage, v_i is very close to sinusoidal, even with wide load variations. Therefore, the earlier assumption that only fundamental component of i_i in involved in active power transfer. Also, the relative phase difference between i_i (fundamental) and

v_i are zero, which verifies the effectiveness of load independent tank design. Therefore, the inverter need to supply the least amount of VA to tank network for given load power. This ensures least voltage and current ratings of inverter devices, thereby enabling lowest conduction loss of devices and compact size of converter.

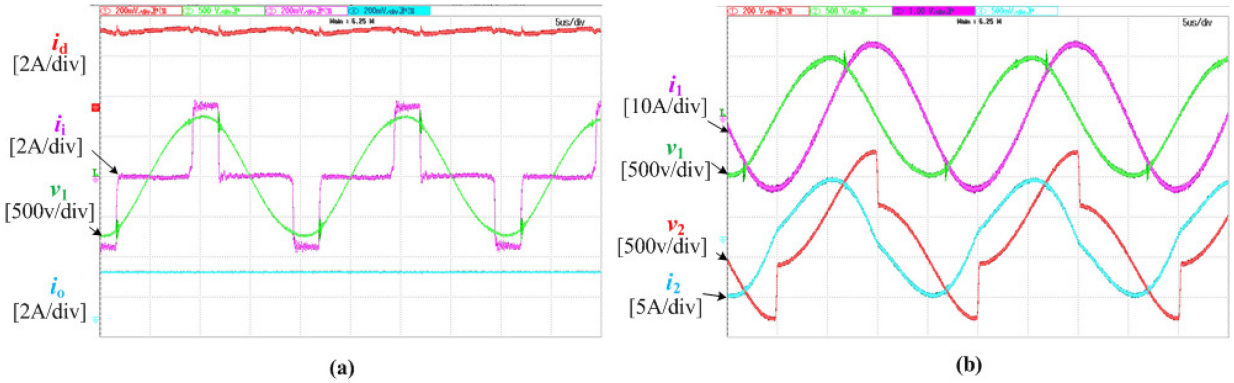


Fig. 4.32 Steady state operation at P_o= 800W

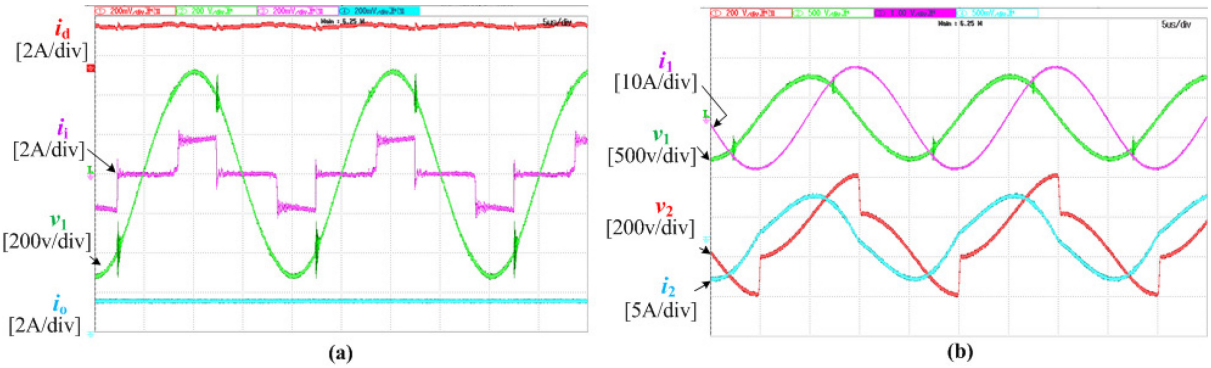


Fig. 4.33 Steady state operation at P_o= 400W

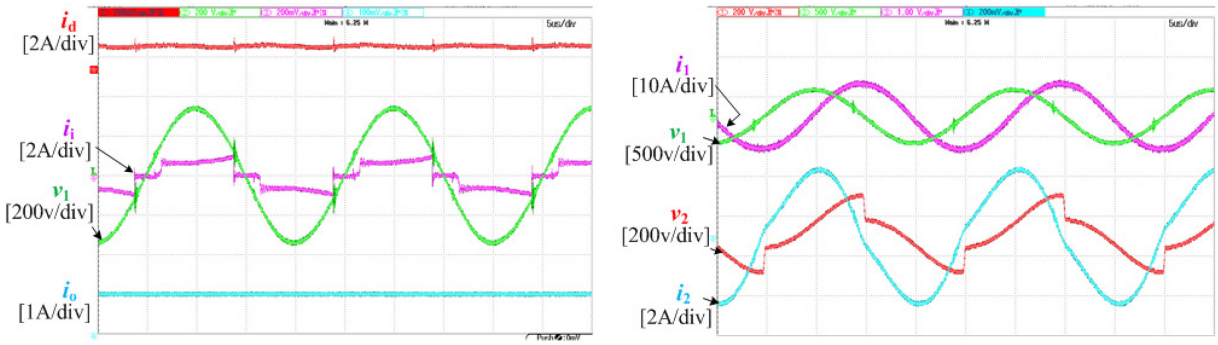


Fig. 4.34 Steady state operation at P_o= 160W

Fig. 4.32b, Fig. 4.33b and Fig. 4.34b show steady state results of TC and RC voltages and currents. Clearly, like earlier, the TC coil receives very close to sinusoidal voltage due to presence of parallel capacitor, C_t. The sinusoidal profile of v_1 results in sinusoidal profiles of i_1, v_2 and i_2.

4.5.3.2 Dynamic Performance

Fig. 4.35 shows dynamic performance of the closed loop system, when a step-down command is applied to output current reference such that power reduces from 800W to 400W. The output reaches to desired new operating point with zero steady state error and settles in around 35ms after the step command. The zoomed views of this result—before, during and after the transient show the switching frequency view. Clearly, inverter output voltage is sinusoidal, and the current is quasi-square. This verifies the assumption that active power flow occurs predominantly due to fundamental component. Also, unity displacement PF at inverter output with this wide load variations clearly shows the effectiveness of load independent resonant tank design. Primary coil current remains very close to sinusoidal throughout this operation as shown in Fig. 4.35.

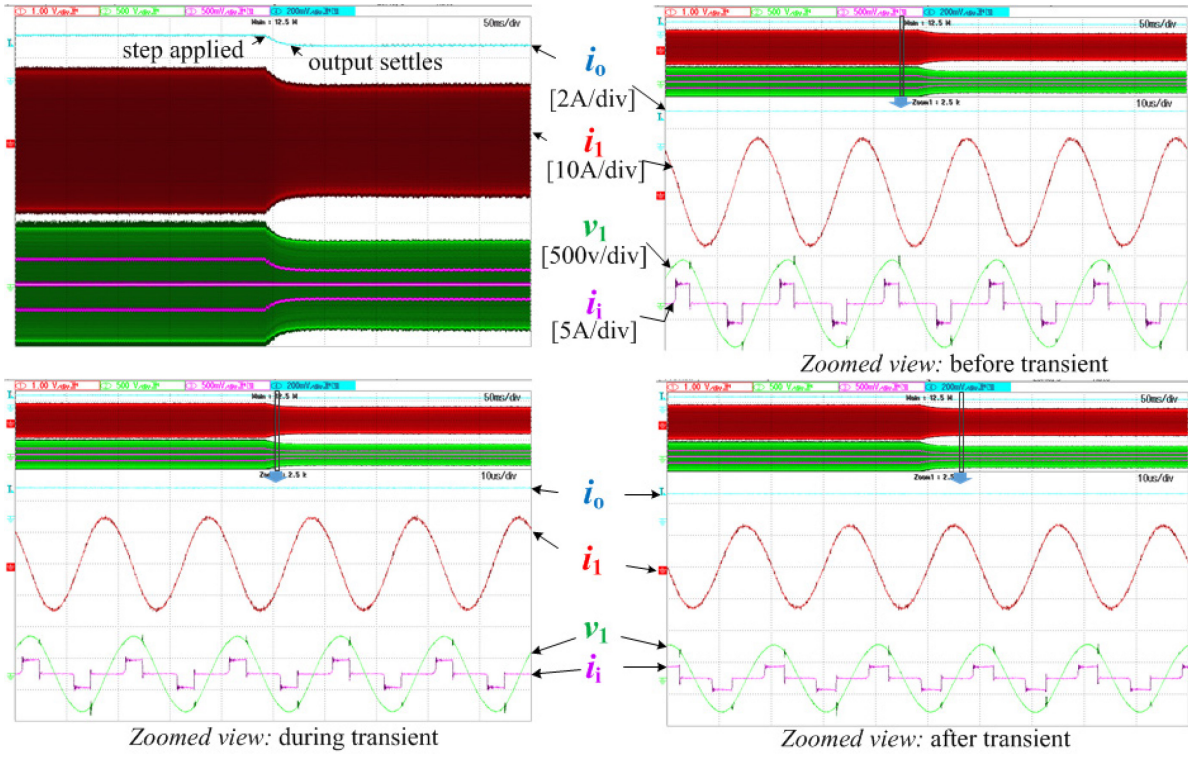


Fig. 4.35 Step response in presence of a step-down command applied to output current reference

Fig. 4.36 shows performance of the closed loop system in presence of an input disturbance. This is done by abruptly increasing input voltage of the converter from 175V to 225V (25% of rated v_d). Immediately, a slight increase in output current observed due to more power injection from input. However, the output current is restored to its original value within the designed settling time

of outer loop. This verifies the performance of the closed loop system. The zoomed views of this result validates the effectiveness of load independent resonant tank design.

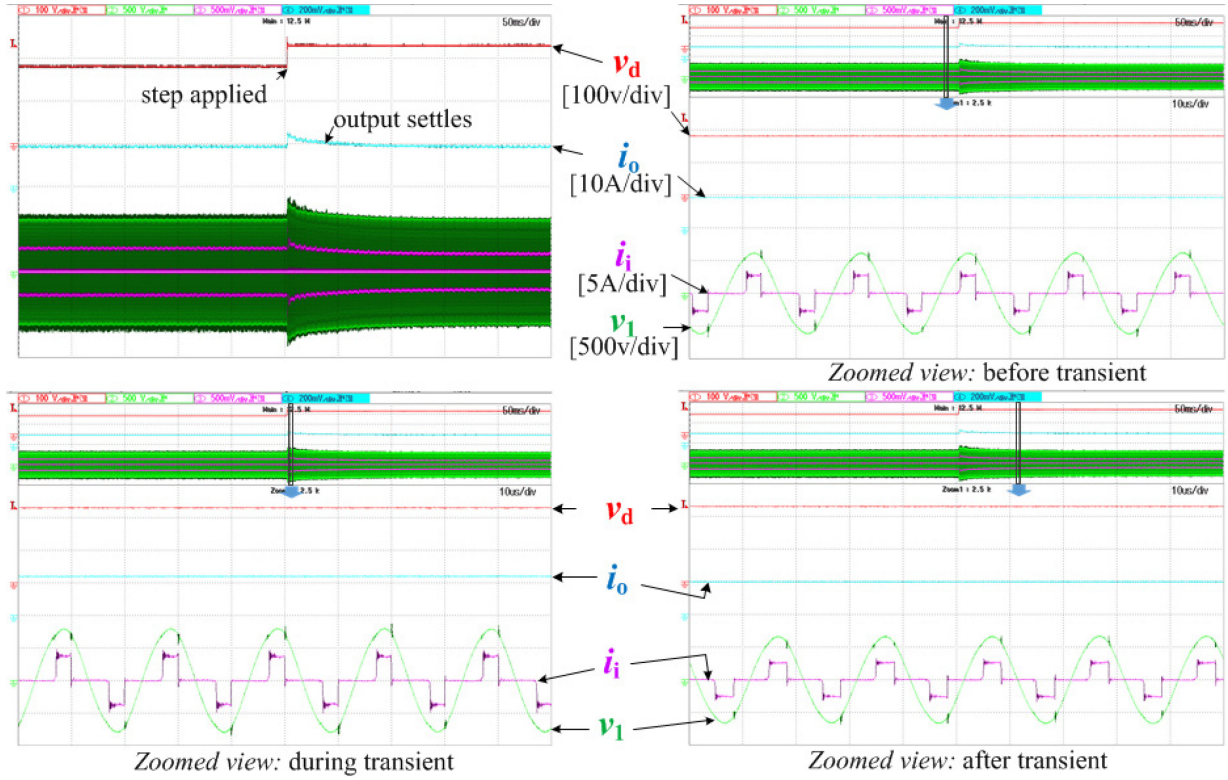


Fig. 4.36 Closed loop performance in presence of 25% input voltage disturbances (175 to 225V)

4.6 Conclusion

This Chapter reports a new load independent design technique for parallel-series/series tank network, fed from a full-bridge inverter. Conventional parallel compensated tanks are controlled through variable switching frequency to operate the tank network at resonant point, where an extra chopper at output side fulfills the load requirements. However, the proposed design is capable to operate at resonant point without any dynamic tuning. Owing to passive selection of tank elements and conventional fixed frequency variable duty cycle control, converter operation is simple and practical. Therefore, the load requirements are directly met by inverter, thereby eliminating dc-dc chopper stage. This design repeatedly shows lower voltage and current ratings of inverter devices for a given load due to least VA loading on inverter. This ensures lower conduction loss and efficient design. The control goals are achieved through two loop method where the inner input current loop controls the source current and outer output current loop meets load requirements.

The detailed steady-state operation, converter design, small-signal modelling and control is reported and verified using frequency response analyzer. Experimental results obtained from a 1.6kW lab- prototype validates the proposed design, small signal modelling and closed loop control of the converter.

Chapter 5 Bidirectional IPT Topology with Current-Fed Half-Bridge (*C*)(*LC*)–(*LC*) Configuration

5.1 Introduction

EVs can operate either as electric loads or as energy sources. Unidirectional EV chargers can charge EV battery, but it cannot inject energy in the grid. A bidirectional charger is required to support energy injection from vehicle to grid (V2G). Many researchers have investigated potential benefits of V2G concepts. The main merits are reported as follows [67].

i. V2G-capable vehicles offer a possible backup for renewable power sources including wind and solar power, supporting efficient integration of intermittent power production.

ii. V2G systems can provide additional opportunities for grid operators, such as reactive power support, active power regulation, load balancing by valley filling, peak load shaving, and current harmonic filtering etc.

iii. These systems can improve grid efficiency, stability, reliability, and generation dispatch.

iv. They reduce utility operating costs and even potentially generate revenue.

v. CO_2 emissions are reduced etc.

Bidirectional wireless IPT technology promises a very convenient, safe and reliable method to enable V2G operation. Bidirectional IPT (BD-IPT) topology with VSI topologies have been reported in [19], [43], [73], [74]. The resonant tanks (i.e., compensation networks) are generally dual sided *LCL* [42] [43] or dual sided *LCCL* [73], [74] type. The active power flow control is achieved with phase shift modulation of VSI. These reported works have been proved the suitability of wireless technology in V2G applications. However, one major demerit of BD-IPT with VSI topology is that the inverter current profile is highly non-sinusoidal, where the voltage is square shaped as shown in Fig. 5.1. Therefore, the VA loading on inverter for a given load is quite high due to extra reactive power flow. The parallel compensated IPT topology, fed from a CSI have very close to sinusoidal voltage at inverter output and current is square shaped. Therefore, by operating the inverter close to unity PF, lower VA loading on current source inverter is ensured.

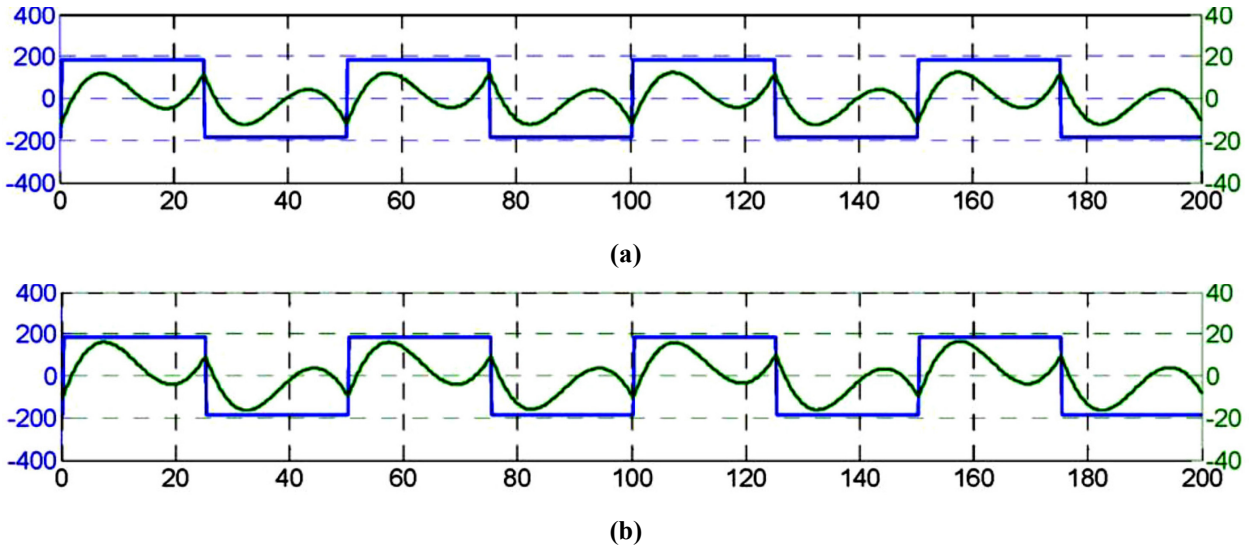


Fig. 5.1 Typical voltage (blue) and current (green) waveforms at VSI output for (a) 600W and (b) 900W power output [42]

The objective of this chapter is to propose and analyze in detail a bidirectional IPT topology with current-sharing and voltage doubling feature. Proposed IPT topology can transfer power both from grid-to-vehicle (G2V) and from vehicle-to-grid (V2G). This is the first attempt to implement bidirectional IPT system with current-fed topology with current-sharing voltage doubler configuration. Dc link inductor provides natural short circuit protection and limits the peak and circulating current through the components. Current sharing (i.e., half-bridge CSI) configuration further reduces the average and peak current through the components resulting into reduced conduction losses. Current-fed circuit also offers voltage gain and the voltage doubler add 2x additional gain. Proposed converter is analyzed and detailed design procedure is reported.

This Chapter is organized as follows. Section 5.2 introduces the proposed bidirectional topology and explain in detail the G2V and V2G operation. Systematic design of converter and component selection are presented in Section 5.3 and 5.4. Section 5.5 demonstrates experimental results of circuit operation, and performance for both G2V and V2G operating modes. Section 5.6 concludes this research work.

5.2 Proposed Bidirectional IPT Topology

Fig. 5.2 shows the proposed bidirectional IPT topology, where the transmitter side converter is half-bridge CSI and receiver side converter is half-bridge VSI. During G2V operation—i.e., EV

battery recharging operation, the current-fed converter acts as an inverter and the VSI acts as a voltage doubler passive rectifier. The resonant tank for this operation remains same as earlier, i.e., *CLC* transmitter and *LC* receiver. The main reason for choosing half-bridge CSI structure in bi-directional power transfer is that the number of active devices are only four, whereas with full-bridge CSI structure it will be eight. Similarly, in the receiver side, half-bridge VSI require only half number of active devices, compared with full-bridge VSI.

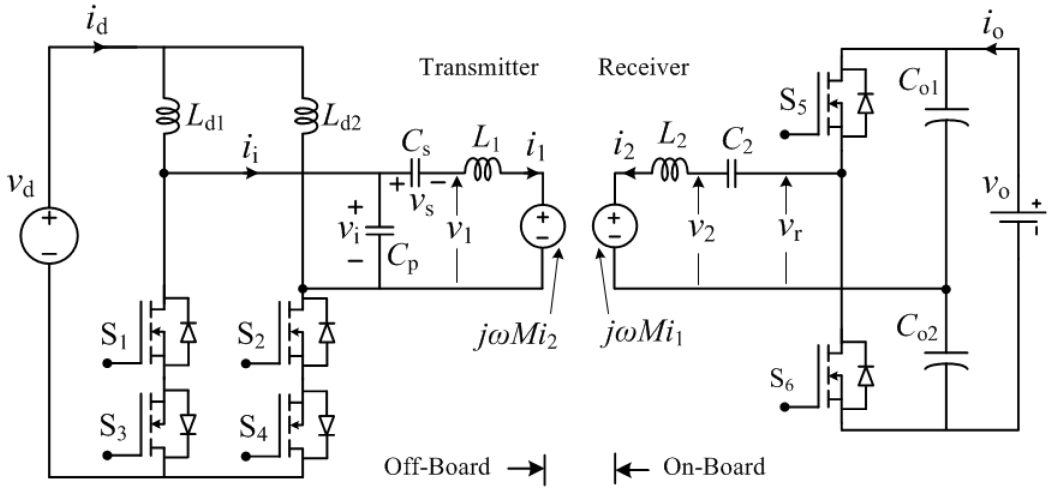


Fig. 5.2 Bidirectional WPT topology using current-fed half bridge converter.

During V2G operation, the vehicle side converter acts as a half bridge VSI and the grid side converter acts as a passive current-doubler rectifier. Although, during V2G mode, the vehicle side IPT should be called as transmitter and the grid side coil should be termed as receiver, but to avoid complexity, the names are not interchanged. The voltage across and current through the devices are named as $v_{S1} \sim v_{S6}$ and $i_{S1} \sim i_{S6}$, respectively and these parameters for their body diodes are named as $v_{D1} \sim v_{D6}$ and $i_{D1} \sim i_{D6}$, respectively. The steady state operation of the converter for both the operating modes are reported as follows.

5.2.1 Steady state operation of G2V

During this operation, the devices, S_1 and S_2 of half-bridge CSI are given switching frequency pulse and S_3 and S_4 are kept OFF permanently. In the receiver side, the body diodes (D_5 and D_6) of S_5 and S_5 devices make the converter as passive voltage-doubler rectifier. To explain the steady-state operation of the proposed converter, consider that the inverter devices, S_1 and S_2 are operating at fixed 50% duty cycle and power is controlled by frequency modulation. Ideally, the duty cycle

of S_1 and S_2 are 0.5 and their gating signals are complimentary. However, to make sure the continuity of stiff dc link current, I_d, a slight overlap between gating signals of S_1 and S_2 is maintained. The operating power factor at CSI output is considered to be lagging to achieve zero-voltage switching (ZVS) at device turn-on. However, soft-switching at device turn-off is also possible if this power factor is leading.

Interval I **(t_0-t_1-t_2):** Consider that at $t = t_0$, device S_1 is ON and S_2 is OFF. In this condition device S_1 takes complete dc link current, I_d as shown in Fig. 5.3 and Fig. 5.4a. During interval, t_0-t_1-t_2 a positive voltage with same magnitude as v_i appears in the second leg of the inverter i.e., on S_2-D_4. S_2 blocks this positive voltage. The voltages and currents of transmitter side elements are given as

$$i_{S1}\,,\;\; i_{D3} = i_{d1} + i_{d2}\,, \qquad (5.1)$$

$$L_{d1}\frac{di_{d1}}{dt} = v_d - v_i\,, \qquad L_{d2}\frac{di_{d2}}{dt} = v_d\,, \qquad (5.2)$$

where, i_{d1} and i_{d2} are currents through inductor L_{d1} and L_{d2}, respectively. During interval t_0-t_1, receiver side rectifier diode, D_5 rectifies the RC current, i_2. For this duration, the voltages and currents of RC side elements are given as

$$v_{D6} = v_{o1} + v_{o2}\,, \qquad (5.3)$$

$$i_{D5} = i_2\,, \qquad (5.4)$$

$$C_{o1}\frac{dv_{o1}}{dt} = i_2 + i_o\,, \qquad C_{o2}\frac{dv_{o2}}{dt} = i_o\,, \qquad (5.5)$$

where, v_{o1} and v_{o2} are the voltages across capacitor C_{o1} and C_{o2}, respectively. At instant t_1, RC current becomes zero as shown in Fig. 5.3 and diode D_5 turns off at zero current. Therefore, zero reverse recovery of diode D_5 is achieved. During interval t_1-t_2, diode D_6 rectifies the RC current, i_2 as shown in Fig. 5.4b equivalent circuit. The voltage and current expressions for this period are given as

$$v_{D5} = v_{o1} + v_{o2}\,, \qquad (5.6)$$

$$i_{D6} = i_2\,, \qquad (5.7)$$

$$C_{o1}\frac{dv_{o2}}{dt} = i_o\,, \qquad C_{o2}\frac{dv_{o1}}{dt} = i_2 + i_o\,. \qquad (5.8)$$

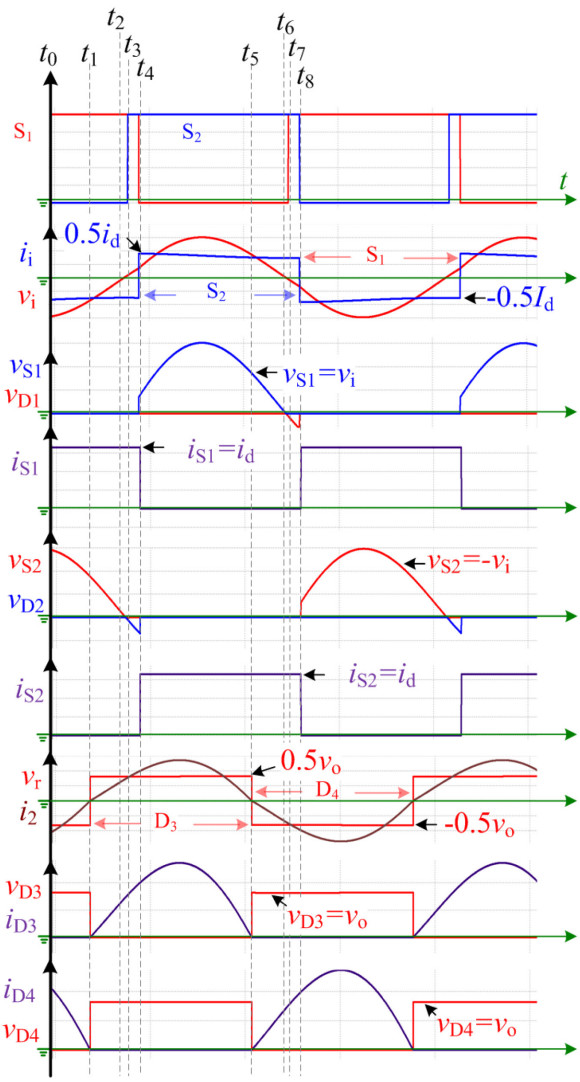


Fig. 5.3 Steady state waveforms of the converter during grid to vehicle operation

Interval II **(t_2-t_3):** At instant t_2, inverter output voltage changes polarity before current, because the inverter power factor is lagging. From this instant, the second leg of the inverter (S_2-D_4) gets a negative voltage and D_4 blocks this voltage. The equivalent circuit during interval t_2-t_3 remains same as shown in Fig. 5.4b. The voltage and current expressions during this interval are same as (5.1), (5.2) and (5.6) - (5.8).

Interval III **(t_3-t_4):** t_3-t_4 interval is switching overlap period of the devices S_1 and S_2. At instant t_3, device S_2 is triggered, but because the voltage across this leg (S_2-D_4) is negative, the first leg of inverter (S_1-D_3) keeps on conducting. Thus, ZVS turn-on is achieved for S_2. At instant t_4, S_1 is turned-off and immediately total dc link current, I_d is transferred to S_2-D_4 as shown in Fig. 5.4c.

The first leg of the inverter (S_1-D_3) gets a positive voltage at this instant and S1 blocks this voltage. In practical, the switching overlap interval (i.e., t_3-t_4) is very short, typically less than 0.5μs but sufficient enough to turn-on S_2.

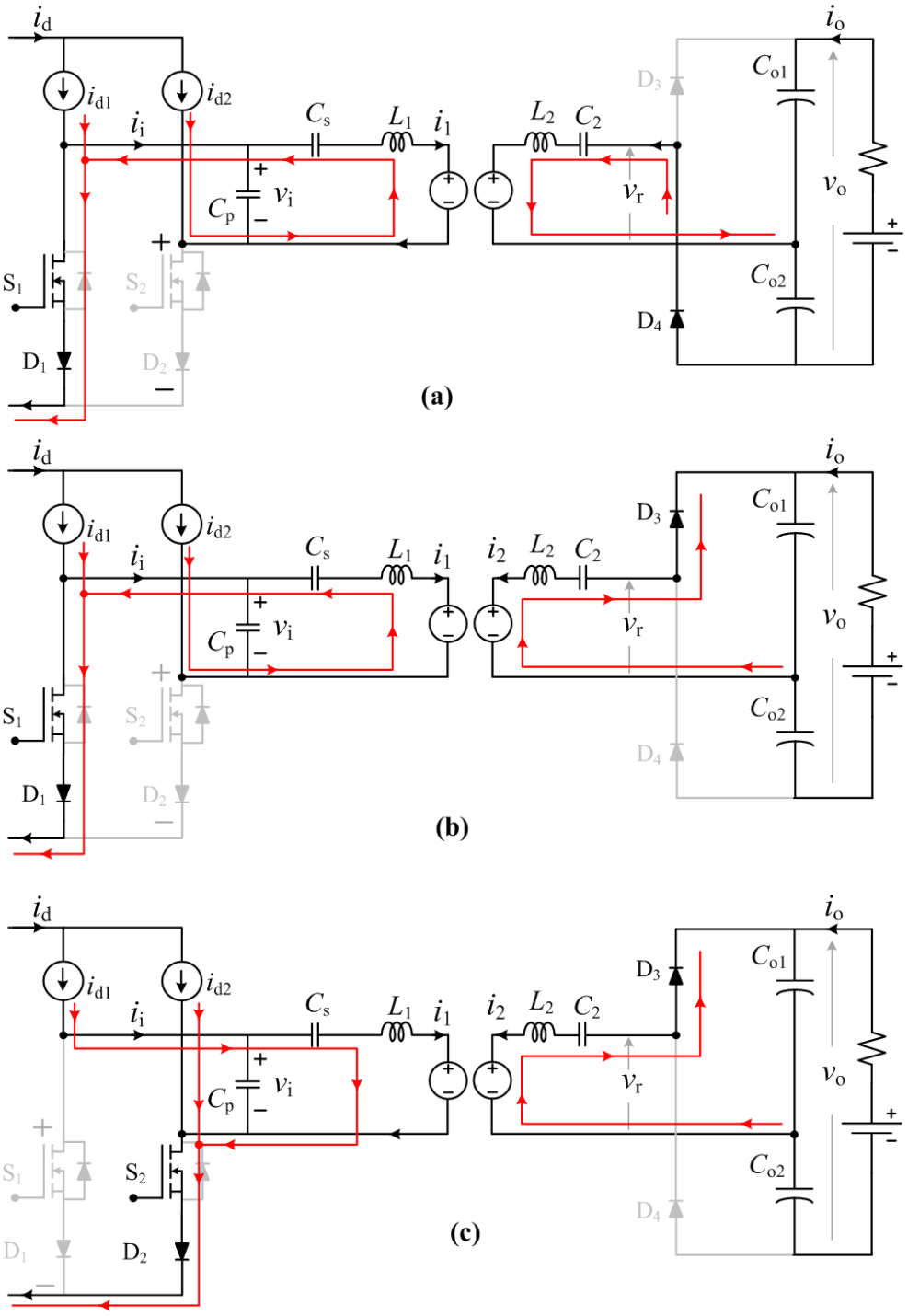


Fig. 5.4 Equivalent circuit diagrams for different switching intervals

Interval IV **(t_4- t_5):** At t_4 device S_1 is turned off and S_2 takes full dc link current, I_d as shown in Fig. 5.4c. During interval t_4- t_5, the receiver side equivalent circuit remains same as earlier and diode D_6 keeps on conducting. The voltage and current expressions for this interval are given as

$$i_{S2}\,,\quad i_{D4} = i_{d1} + i_{d2}\,, \tag{5.9}$$

$$L_{d1}\frac{di_{d1}}{dt} = v_d\,,\quad L_{d2}\frac{di_{d2}}{dt} = v_d - v_i\,. \tag{5.10}$$

Interval V **(t_5- t_6- t_7- t_8):** At instant t_5, RC current polarity changes and diode D_5 commutates diode D_6. At instant t_6, inverter output voltage polarity changes and a negative voltage appears across S_1-D_3 and diode D_1 takes this voltage. At instant t_7, S_1 is triggered but due to presence of negative voltage across S_1-D_1, the second leg (S_2-D_4) keeps on conducting. This leads to soft turn-on of device S_1. At instant t_8 the gating signal of S_2 is withdrawn and S_1 takes complete dc link current, I_d as shown in Fig. 5.3.

5.2.2 Steady state operation of V2G

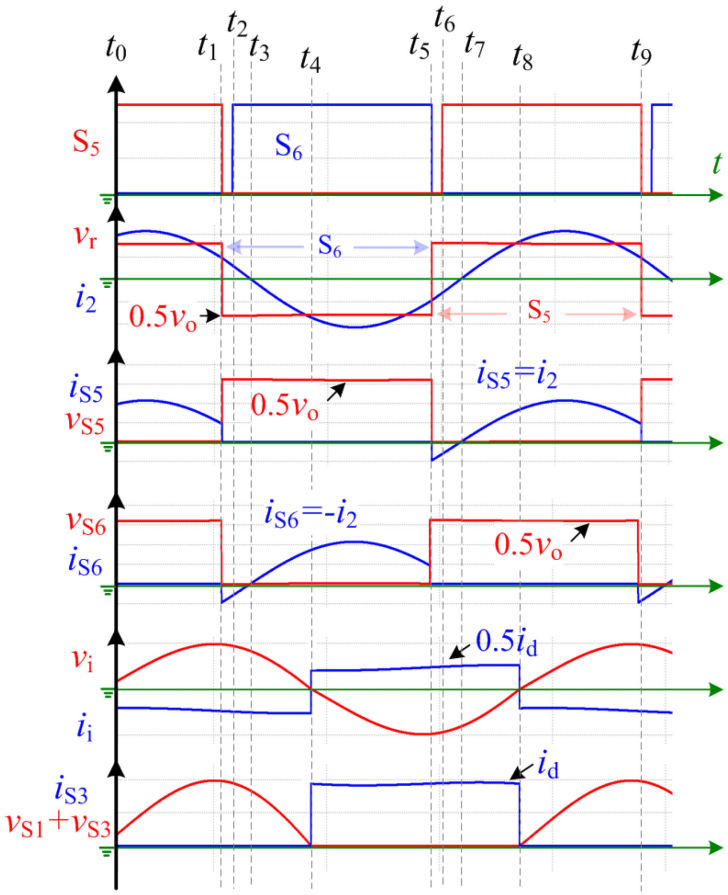


Fig. 5.5 Steady state waveforms of the converter during vehicle to grid operation

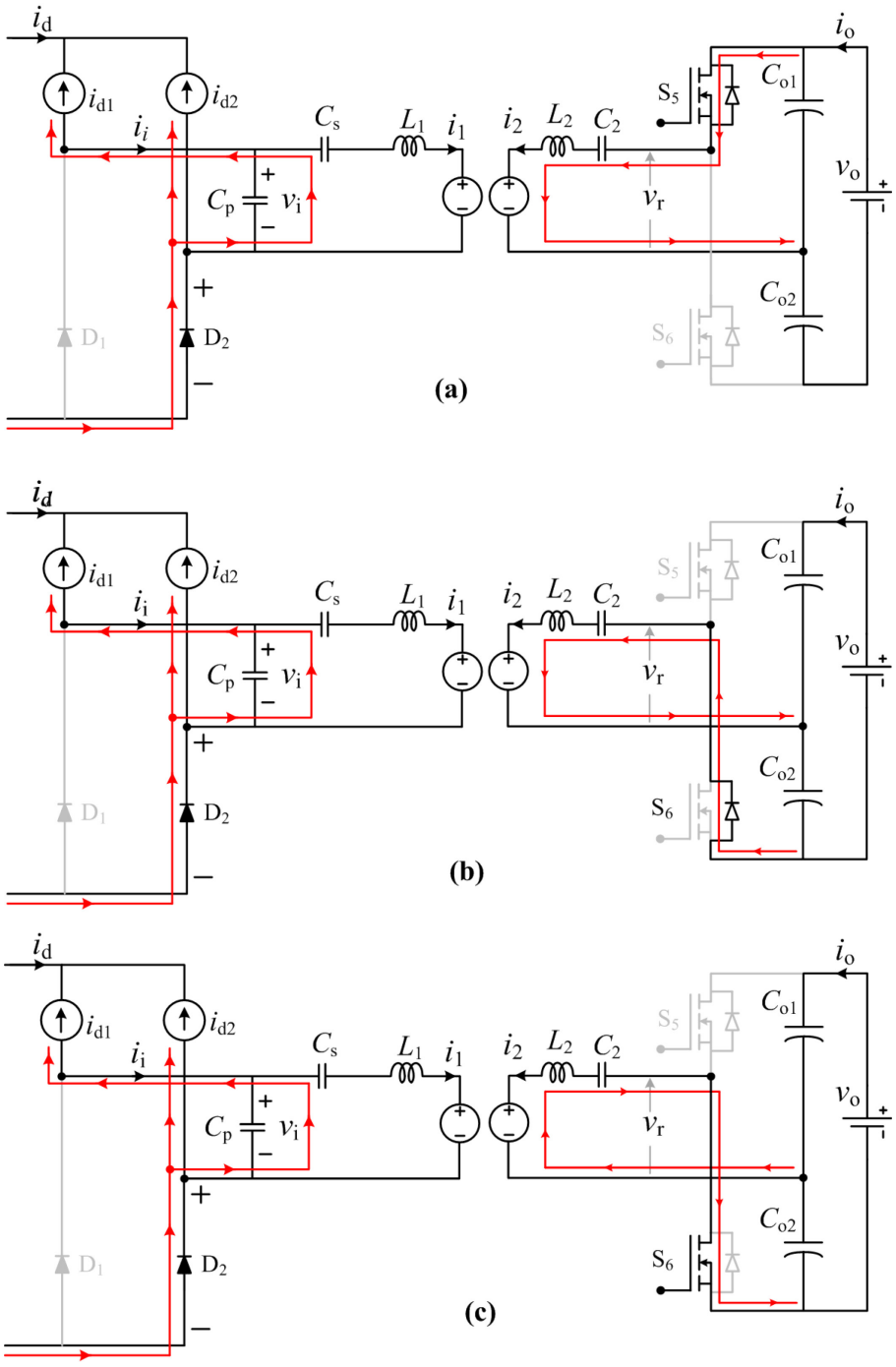


Fig. 5.6 Equivalent circuit diagrams for different switching intervals during V2G operation (a) t_0-t_1 interval, (b) t_1-t_2- t_3 interval and (c) t_3-t_4 interval

During V2G operation, the inverter (i.e., half bridge VSI) duty cycle is kept fixed at 0.5 and power flow is controlled by frequency modulation of the VSI. This helps to achieve soft switching of the inverter devices irrespective load change. A slight dead band is always maintained between

inverter devices S_5 and S_6 to prevent short-circuiting the battery. During this operation, the grid side converter acts as a passive rectifier. This is done by keeping S_3 and S_4 permanently ON and S_1 and S_2 OFF, where only body diodes D_1 and D_2 act as rectifier diodes. Fig. 5.5 shows the V2G operating waveforms during steady state and Fig. 5.6 shows equivalent circuit diagram of each switching intervals. During steady state, the operating power factor at VSI output is considered to be lagging to achieve ZVS turn-on of S_5 and S_6.

Interval I (t_0-t_1): During interval t_0-t_1, device S_5 is ON and S_6 is OFF. A positive voltage with a magnitude of $0.5v_o$ appears at the output of VSI. Due to presence of series *LC* resonant tank, a sinusoidal current flows through the RC as shown in Fig. 5.5. Fig. 5.6a shows the equivalent circuit. In this duration the voltage and current expressions of RC side components are same as (5.3)-(5.5). During this interval, ac side voltage of grid side converter is positive and body diode D_2 is forward biased as shown in Fig. 5.6a equivalent circuit. The TC side voltage and current expressions are same as (5.9) and (5.10).

Interval II (t_1-t_2-t_3): Interval t_1-t_2 is dead band period of the devices S_5 and S_6. Owing to lagging power factor of VSI, current, I_2 does not change direction at instant t_1. Thus, at t_1 instant, I_2 starts flowing through the body diode of S_6 as shown in Fig. 5.6b. After the dead time (i.e., at t_2 instant), the device S_6 is turned-on at zero voltage. The body diode of S_6 (i.e. D_6) keeps on conducting till the coil current I_2 changes polarity at instant t_3. Throughout this interval the RC side voltage and current expressions are same as (5.6) - (5.8).

Interval III (t_3-t_4-t_5): At instant t_3, the polarity of RC current, I_2 changes and device S_6 starts conducting. The equivalent circuit of interval t_3-t_4 is shown in Fig. 5.6c. During the interval t_0-t_4, the body diode D_2 conducts due to positive polarity of v_i. At instant t_4, the polarity of voltage v_i becomes negative. Therefore, the body diode D_2 is reverse biased and D_1 becomes forward biased and takes complete dc link current, I_d. At instant t_5, device S_6 is turned-off and dead time of S_5 and S_6 begins. S_5 turns-on at instant t_6 when the voltage across it is zero. Therefore, this device experiences ZVS at turn-on. This sequence of operation repeats in each switching time period.

5.3 Design Procedure and Considerations

This section reports detailed derivation of voltage and current ratings of all the converter circuit elements.

5.3.1 Component ratings of G2V operation

Fig. 5.7a shows ac side equivalent circuit of the proposed converter where the input and output are modeled as current source and voltage source, respectively. Applying power balance and considering active power flows in ac side is due to fundamental component only, rms values of ac side voltage and current expressions are given as

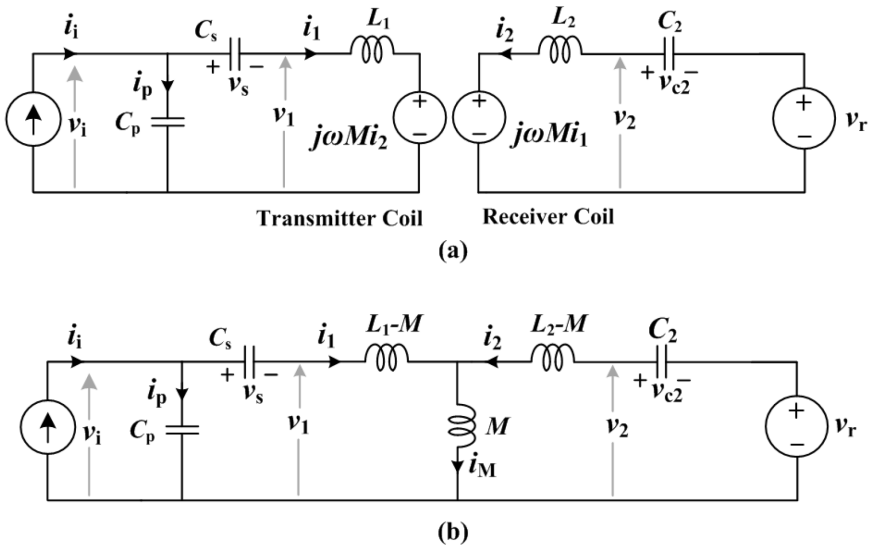


Fig. 5.7 Ac side equivalent circuit of the bidirectional IPT topology (a) coupled inductor model (b) transformer model

$$V_{\mathrm{r}}.I_2 = V_o.I_o \ , \quad (5.11)$$

$$I_2 = \frac{\pi}{2\sqrt{2}}.(2.I_o) = \frac{\pi}{\sqrt{2}}.I_o \ , \quad (5.12)$$

$$V_{\mathrm{r}} = \frac{\sqrt{2}}{\pi}.V_o \ . \quad (5.13)$$

During G2V operation, rectifier input voltage, V_{r} and current, I_2 lies in same phase, because the polarity of V_{r} changes immediately after the change of I_2 polarity. During G2V operation, voltage V_{r} phase is considered as reference phasor. Applying KCL at TC side network, inverter output current is derived as

$$I_{\mathrm{i}} = I_1 + I_{\mathrm{p}} = \left[\frac{\omega^2 M C_{\mathrm{s}} I_2}{(\omega^2 L_1 C_{\mathrm{s}} - 1)}\right] + j\left[\omega V_{\mathrm{i}}\left(C_{\mathrm{p}} - \frac{C_{\mathrm{s}}}{(\omega^2 L_1 C_{\mathrm{s}} - 1)}\right)\right], \quad (5.14)$$

where, M is mutual inductance between TC and RC. Applying KVL at the RC side network, the input voltage at the RC side converter is given as

$$V_{\mathrm{r}} = j\omega M I_1 + I_2\left[j\omega L_2 + \frac{1}{j\omega C_2}\right]. \quad (5.15)$$

The value of C_{p} and C_{s} are chosen such that inverter output current, I_{i} magnitude is lower and C_2 is chosen such that bridge input voltage, V_{r} is maximum. This is done by eliminating second term in both (5.14) and (5.15). From (5.14) and (5.15), the required capacitances are calculated as

$$\omega_{\mathrm{t}} = \frac{1}{\sqrt{L_1\left(\frac{C_{\mathrm{p}}C_{\mathrm{s}}}{C_{\mathrm{p}}+C_{\mathrm{s}}}\right)}}, \qquad \omega_{\mathrm{r}} = \frac{1}{\sqrt{C_{\mathrm{r}}L_2}}. \quad (5.16)$$

Effective power transfer is achieved by equalizing inverter switching frequency, ω_{s} (=$2\pi f_{\mathrm{s}}$), TC and RC tank resonance frequencies. Applying KVL in the receiver side loop, transmitter coil current is calculated as

$$I_1 = -\frac{1}{\omega_{\mathrm{s}}M}\left[\frac{\pi}{\sqrt{2}}I_o\left(\omega_{\mathrm{s}}L_2 - \frac{1}{\omega_{\mathrm{s}}C_2}\right) + j\frac{\sqrt{2}}{\pi}V_o\right]. \quad (5.17)$$

Applying KVL and KCL in transmitter side and using (5.16) and (5.17), the RMS value of voltage across TC and series capacitor, C_{s} are derived as

$$V_1 = \frac{\sqrt{2}}{\pi}\frac{L_1}{M}V_o - j\frac{\pi}{\sqrt{2}}I_o\left[\frac{L_1}{M}\left(\omega_{\mathrm{s}}L_2 - \frac{1}{\omega_{\mathrm{s}}C_2}\right) - \omega_{\mathrm{s}}M\right], \quad (5.18)$$

$$V_{\mathrm{s}} = -\frac{1}{{\omega_{\mathrm{s}}}^2 M C_s}\left[\frac{\sqrt{2}}{\pi}V_o - j\frac{\pi}{\sqrt{2}}I_o\left(\omega_{\mathrm{s}}L_2 - \frac{1}{\omega_{\mathrm{s}}C_2}\right)\right]. \quad (5.19)$$

Applying KVL, rms value of inverter output voltage, V_{i} is calculated using (5.18) and (5.19) as

$$V_{\mathrm{i}} = \frac{\sqrt{2}}{\pi}\frac{V_o}{\omega_{\mathrm{s}}M}\left(\omega_{\mathrm{s}}L_1 - \frac{1}{\omega_{\mathrm{s}}C_{\mathrm{s}}}\right) - j\frac{\pi}{\sqrt{2}}I_o\left[\left(\omega_{\mathrm{s}}L_2 - \frac{1}{\omega_{\mathrm{s}}C_2}\right)\left(\frac{L_1}{M} - \frac{1}{{\omega_{\mathrm{s}}}^2 M C_{\mathrm{s}}}\right) - \omega_{\mathrm{s}}M\right]. \quad (5.20)$$

The voltage rating of the devices of half-bridge CSI are same as the peak voltage of v_{i}. The rms current through the devices and body diodes are given as

$$I_{\mathrm{S1}},\ I_{\mathrm{S2}},\qquad I_{\mathrm{D3}},\qquad I_{\mathrm{D4}} = \sqrt{0.5}\,I_{\mathrm{d}}. \quad (5.21)$$

$$\hat{V}_{S1}\,, \qquad \hat{V}_{S2} = \sqrt{2}\,V_i\,. \quad (5.22)$$

The peak blocking voltage and average current through the RC side converter devices and body diodes are given as

$$\hat{V}_{S5}\,, \qquad \hat{V}_{S6} = V_o\,. \quad (5.23)$$

$$\bar{I}_{D5}\,, \quad \bar{I}_{D6} = 0.5\frac{2\sqrt{2}I_2}{\pi} = I_o\,. \quad (5.24)$$

Owing to same equivalent circuit as earlier, the voltage gain of the tank network during G2V operation is not repeated here and it can be found in earlier Chapters.

5.3.2 ZVS Conditions during G2V Operation

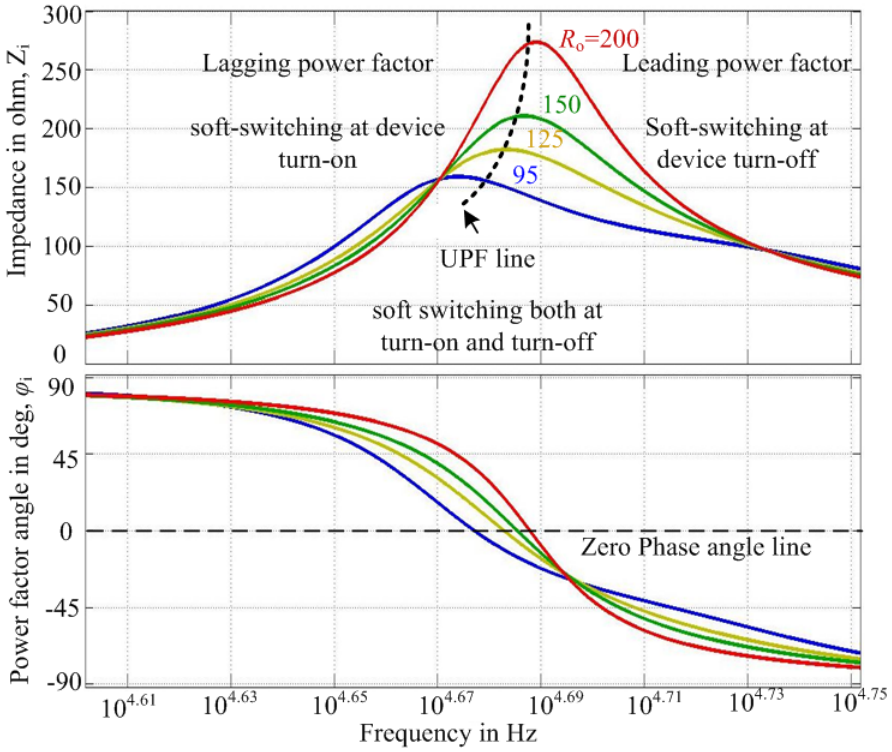


Fig. 5.8 Inverter output Impedance ($|Z_i|$) and phase angle ($\angle Z_i$) plot for different V_o/I_o ratio.

During G2V operation, the output power cannot be controlled through fixed frequency variable duty cycle modulation. This is because the basic switching devices during G2V operation are only S_1 and S_2. Due to current source at the input of the inverter, the minimum duty cycle of the devices are limited to 0.5. Increasing duty cycle does not help to change power flow, because the effective duty cycle remains 0.5 even when the devices receive more than 0.5 duty cycle. Therefore, keeping

duty cycle fixed at 0.5, the inverter switching frequency can be varied to achieve the desired output power. The impedance at the output of the inverter (i.e., input to the TC tank network) is derived as

$$Z_{\mathrm{i}} = \frac{V_{\mathrm{i}}}{I_{\mathrm{i}}} = \frac{1}{j\omega_{\mathrm{s}}C_{\mathrm{p}}} // \left[\left\{j\omega_{\mathrm{s}}(L_1 - M) + \frac{1}{j\omega_{\mathrm{s}}C_{\mathrm{s}}}\right\} + \left\{j\omega_{\mathrm{s}}M // \left(j\omega_{\mathrm{s}}(L_2 - M) + \frac{1}{j\omega_{\mathrm{s}}C_2} + R_{\mathrm{eo}}\right)\right\}\right]. \quad (5.25)$$

where, R_{eo} (=v_{r}/i_2) is equivalent load impedance at rectifier input. For different values of load (R_{o}), magnitude and phase (φ_{i}) of Z_{i} is plotted in Fig. 5.8. The power at the output of the inverter is derived as

$$P_{\mathrm{inv}} = {I_{\mathrm{i}}}^2 . Re(Z_{\mathrm{i}}) = {I_i}^2 |Z_{\mathrm{i}}| \cos\varphi_{\mathrm{i}} = \left(\frac{I_{\mathrm{d}}}{2} . \frac{2\sqrt{2}}{\pi}\right)^2 |Z_{\mathrm{i}}| \cos\varphi_{\mathrm{i}} . \quad (5.26)$$

The dc link current, I_{d} is constant in current-fed converter and this is ensured by previous stage converter or power factor correction (PFC) rectifier. Therefore, power transferred through the proposed converter is proportional to real part of the tank input impedance. In order to achieve ZVS at device turn-on the converter needs to be operated at lagging power factor side. From Fig. 5.8 it is clear that when the inverter switching frequency is decreased from unity PF line, input impedance is reduced. Therefore, power transferred to load is also reduced.

5.3.3 Component Ratings of V2G Operation

The ac side equivalent circuit of the converter remains same during V2G operation as shown in Fig. 5.7a. Applying power balance and considering active power flow is due to fundamental component only, rms values of voltage and current expressions are given as

$$I_{\mathrm{i}} = \frac{2\sqrt{2}}{\pi} . \frac{I_{\mathrm{d}}}{2} = \frac{\sqrt{2}}{\pi} . I_{\mathrm{d}} , \quad (5.27)$$

$$V_{\mathrm{i}} = \frac{\pi}{\sqrt{2}} . V_{\mathrm{d}} , \quad (5.28)$$

$$R_{\mathrm{ei}} = \frac{V_{\mathrm{i}}}{-I_{\mathrm{i}}} = \frac{\pi^2}{2} . \frac{V_{\mathrm{d}}}{-I_{\mathrm{d}}} , \quad (5.29)$$

where, R_{ei} (=$v_{\mathrm{i}}/i_{\mathrm{i}}$) is the equivalent load resistance during V2G operation. Like the G2V operation, in V2G operation the rectifier input voltage, V_{i} and current, I_{i} lies in same phase and their phasors are considered as reference phasor. Using (5.28) the parallel capacitor, C_{p} current is derived as

$$I_{\mathrm{p}} = \frac{V_{\mathrm{i}}}{\left(\frac{1}{j\omega C_{\mathrm{p}}}\right)} = j\frac{\pi}{\sqrt{2}}\omega_{\mathrm{s}} C_{\mathrm{p}} V_{\mathrm{d}}\,. \quad (5.30)$$

Applying KCL and using (5.27) and (5.30), the TC current and series capacitor voltage, v_{s} are derived as

$$I_1 = -\frac{\sqrt{2}}{\pi}.I_{\mathrm{d}} - j\frac{\pi}{\sqrt{2}}\omega_{\mathrm{s}} C_{\mathrm{p}} V_{\mathrm{d}}\,, \quad (5.31)$$

$$V_{\mathrm{s}} = -\frac{\pi}{\sqrt{2}}\frac{C_{\mathrm{p}}}{C_{\mathrm{s}}}V_{\mathrm{d}} + j\frac{\sqrt{2}}{\pi}\frac{I_{\mathrm{d}}}{\omega_{\mathrm{s}} C_{\mathrm{s}}}\,. \quad (5.32)$$

Applying KVL at TC tank network, the voltage across TC and current through the RC are derived as

$$V_1 = -\frac{\pi}{\sqrt{2}}V_{\mathrm{d}}\left(1 + \frac{C_{\mathrm{p}}}{C_{\mathrm{s}}}\right) - j\frac{\sqrt{2}}{\pi}\frac{I_{\mathrm{d}}}{\omega_{\mathrm{s}} C_{\mathrm{s}}}\,, \quad (5.33)$$

$$I_2 = \frac{1}{\omega_{\mathrm{s}} M}\left[\frac{\sqrt{2}}{\pi}I_{\mathrm{d}}\left(\omega_{\mathrm{s}} L_1 - \frac{1}{\omega_{\mathrm{s}} C_{\mathrm{s}}}\right) - j\frac{\pi}{\sqrt{2}}V_{\mathrm{d}}\left(1 + \frac{C_{\mathrm{p}}}{C_{\mathrm{s}}} - {\omega_{\mathrm{s}}}^2 L_1 C_{\mathrm{p}}\right)\right]. \quad (5.34)$$

Using (5.31) and (5.34) and applying KVL at the receiver side, the rms value of voltage across RC is derived as

$$V_2 = \frac{\pi}{\sqrt{2}}V_{\mathrm{d}}\left[{\omega_{\mathrm{s}}}^2 M C_{\mathrm{p}} + \frac{L_2}{M}\left(1 + \frac{C_{\mathrm{p}}}{C_{\mathrm{s}}} - {\omega_{\mathrm{s}}}^2 L_1 C_{\mathrm{p}}\right)\right] \quad (5.35)$$
$$+ j\frac{\sqrt{2}}{\pi}I_{\mathrm{d}}\left[\frac{L_2}{M}\left(\omega_{\mathrm{s}} L_1 - \frac{1}{\omega_{\mathrm{s}} C_{\mathrm{s}}}\right) - \omega_{\mathrm{s}} M\right].$$

Using (5.34) the RMS voltage across capacitor C_2 is derived as

$$V_{\mathrm{C2}} = -\frac{1}{{\omega_{\mathrm{s}}}^2 M C_2}\left[\frac{\pi}{\sqrt{2}}V_{\mathrm{d}}\left(1 + \frac{C_{\mathrm{p}}}{C_{\mathrm{s}}} - {\omega_{\mathrm{s}}}^2 L_1 C_{\mathrm{p}}\right) + j\frac{\sqrt{2}}{\pi}I_{\mathrm{d}}\left(\omega_{\mathrm{s}} L_1 - \frac{1}{\omega_{\mathrm{s}} C_{\mathrm{s}}}\right)\right]. \quad (5.36)$$

The peak blocking voltage of voltage doubler devices are same as given in (5.24). The rms current rating of this devices are given as

$$I_{\mathrm{S5}}\,, \qquad I_{\mathrm{S6}} = \frac{1}{\sqrt{2}}I_2\,. \quad (5.37)$$

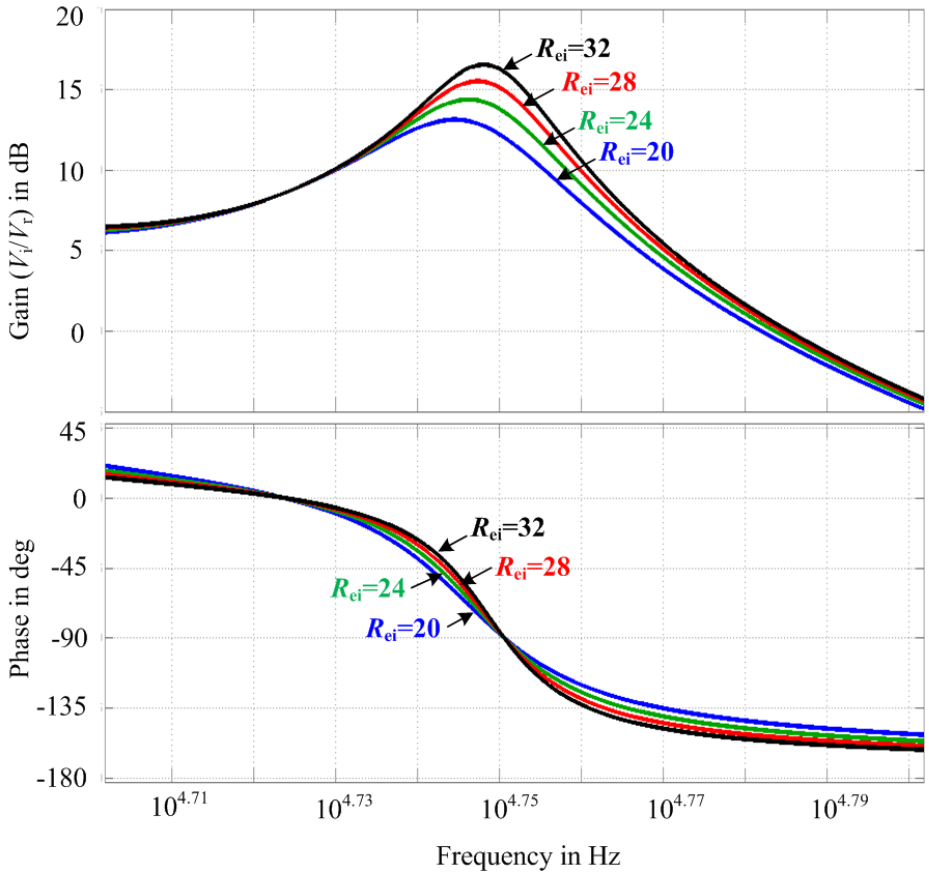


Fig. 5.9 Voltage gain (V_i/V_r) and phase ($\angle V_i/V_r$) plot of the proposed converter during V2G operation.

During this V2G operation, the peak blocking voltage of rectifier devices are same as peak of ac side voltage v_i. The average current through the body diodes are given as

$$\overline{I_{D1}}\,,\ \overline{I_{D2}} = 0.5I_d\,. \quad (5.38)$$

The transformer equivalent circuit shown in Fig. 5.7 is used to derive voltage gain during V2G operation. The voltage across magnetizing impedance branch is calculated as

$$V_M = V_i + I_1 Z_1 = V_i + V_i Z_1 \left(\frac{1}{R_{ei}} + sC_p\right). \quad (5.39)$$

The voltage at the ac side of inverter (i.e., VSI) circuit is calculated as

$$V_r = V_M + I_2 Z_2 = V_i \left[(1 + Z_1 Y)\left(1 + \frac{Z_2}{sM}\right) + Z_2 Y\right], \quad (5.40)$$

where,

$$Y = \frac{1}{R_{ei}} + sC_p\,. \quad (5.41)$$

Fig. 5.9 shows the voltage gain (V_i/V_r) and phase ($\angle V_i/V_r$) plot during V2G operation for different loads.

5.3.4 ZVS conditions during V2G operation

To achieve soft switching of all VSI devices irrespective of load, variable frequency fixed duty cycle control technique is used during V2G operation. From Fig. 5.7b equivalent circuit, the impedance at the ac side of voltage doubler circuit is derived as

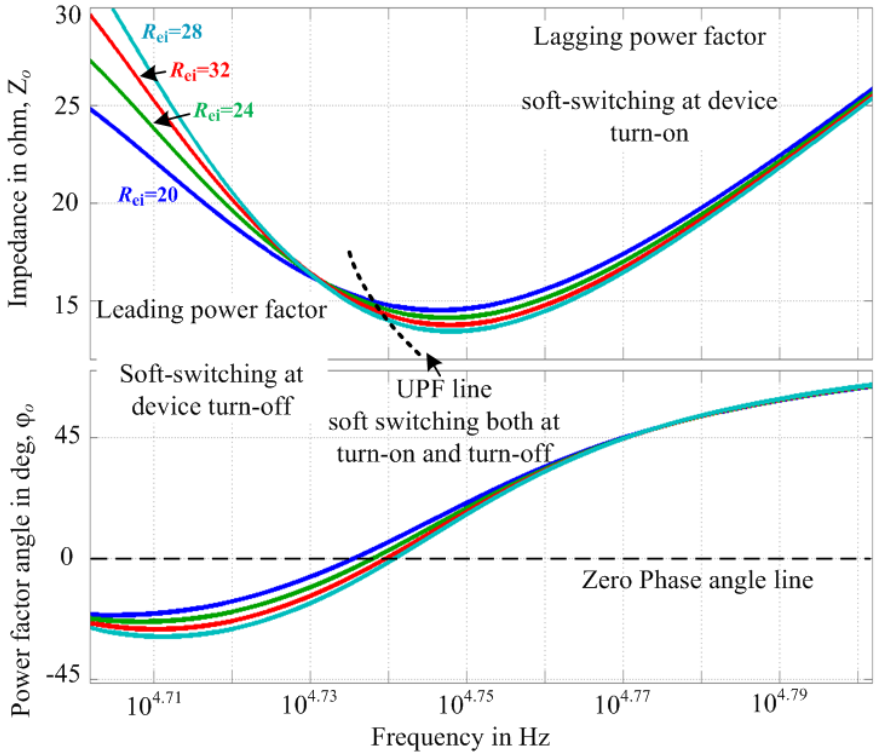


Fig. 5.10 Plot of impedance ($|\boldsymbol{Z_o}|$) and phase angle ($\angle \boldsymbol{Z_o}$) plot for different loads

$$Z_{\mathrm{o}} = \frac{V_{\mathrm{r}}}{I_2} = \frac{1}{j\omega_{\mathrm{s}}C_2} + j\omega_{\mathrm{s}}(L_2 - M) \qquad (5.42)$$

$$+ j\omega_{\mathrm{s}}M // \left[j\omega_{\mathrm{s}}(L_1 - M) + \frac{1}{j\omega_{\mathrm{s}}C_{\mathrm{s}}} + \left(R_{\mathrm{ei}} // \frac{1}{j\omega_{\mathrm{s}}C_{\mathrm{p}}} \right) \right].$$

Fig. 5.10 shows the plot of the magnitude and phase of this impedance for different equivalent load impedances. The power injected from the VSI circuit is given as

$$P_{\mathrm{V2G}} = \frac{{V_{\mathrm{r}}}^2}{\mathrm{Re}(Z_o)} = \frac{{V_{\mathrm{r}}}^2}{|Z_{\mathrm{o}}|\cos\varphi_{\mathrm{o}}} = \frac{1}{|Z_o|\cos\varphi_{\mathrm{o}}} \left(\frac{\sqrt{2}}{\pi} V_o \right)^2. \qquad (5.43)$$

From Fig. 5.10, it is clear that around the resonant point the power flow is maximum and power flow reduces when operating frequency shifts from the resonant point. Keeping the operating switching frequency higher than the resonance frequency ensures lagging power factor operation. This leads to ZVS turn-on of devices S_5 and S_6 irrespective of load change.

5.4 Design example

To implement this bidirectional converter, appropriate values of coil parameters are required to be determined. Using the coil parameters (L_1, L_2 and M), remaining circuit parameters are determined from earlier expressions. Total power transfer between the coupled coils is derived as

$$S = j\omega_s M I_1 I_2 = j\omega_s M \times \frac{\pi}{\sqrt{2}} I_o \times \frac{1}{\omega_s M}\left[\frac{\pi}{\sqrt{2}} I_o \left(\omega_s L_2 - \frac{1}{\omega_s C_2}\right) - j\frac{\sqrt{2}}{\pi} V_o\right]. \quad (5.44)$$

Table 5.1. Specifications for the design example

Parameters	Selected Values
Rated output power	1.2 kW
Switching frequency range	40 *kHz* - 60 *kHz*
Rated switching frequency	50 *kHz*
CSI input dc current, I_d	7.0 A
Output/ battery voltage, v_o	325 *V* (rated)

At close to resonant point, the part $[\omega_s L_2 - 1/\omega_s C_2]$ in (5.44) becomes close to zero and complex part becomes zero. In this condition the real power transfer from TC to RC is given as

$$P = \frac{\pi}{\sqrt{2}} \omega_s M I_o I_1 . \quad (5.45)$$

For easier explanation, a design example of a 1.2 *k*W IPT system is reported and this system is used for experimental verification. The specifications of the target system are listed in Table 5.1. In the 1.2*k*W experimental prototype, the battery voltage and rated charging currents are considered to be 325V and 3.7A, respectively. Also, the switching frequency corresponding to the resonant point is around 50 *k*Hz. From (5.45), it is clear that if I_1 is reduced, then M is increased. Higher value of I_1 indicates thicker coil size and higher value of M indicates larger coil size for a

given airgap. Therefore, there has to be a trade-off between coil current, I_1 and coupling inductance, M. For the prototype, I_1 is chosen to be 11A (RMS). Therefore, for 1.2kW power, the required mutual inductance, M is calculated to be 42 μH. In the IPT coil prototype, 20% coupling is desired and this determines self-inductance of TC around 211μH. Since, the operating principle of the coupled coils are similar to two winding transformer; therefore, TC to RC turns ratio near unity provides better performance. In the prototype, TC to RC turns ratio is selected to be unity.

Table 5.2. Circuit parameters

Components	G2V Rating	V2G Rating	Selected devices/ Prototype Rating
Mutual inductance	42 μH	42 μH	43 μH
TC current, self-inductance	11A 211 μH	12 211 μH	12 A 211 μH
RC current, self-inductance	8A 211 μH	10A 211 μH	12 A 211 μH
MOSFET (CSI side) Body diode	533V peak 4.9A RMS -	530V peak - 3.5A(Avg.)	Part no.-SCT2160KE 1.2 kV, 22 A, $R_{ds,on}$= 208$m\Omega$
MOSFET(vehicle side) Body diode	325V peak - 3.7A(avg.)	325V peak 8.4A RMS -	Part no.-15EWL06FNTR 600V, 15A, V_f=1.05 V @ 15 A
Capacitor, C_s	96 nF, 360 V RMS	96 nF, 390 V RMS	500V ac Cornel Doubler film, 100 nF
Capacitor, C_p	96 nF, 375 V RMS	96 nF, 377 V RMS	500V ac Cornel Doubler film, 100 nF
Capacitor, C_2	48 nF, 530 V RMS	48 nF, 660 V RMS	2×500V ac Cornel Doubler film, 48 nF
DC link inductor L_{d1}, L_{d2}	1.7 mH 1.7 mH	1.2 mH 1.2 mH	1.2 mH 1.2 mH
Output caps, C_{o1}, C_{o2}	224μF, 224μF	224μF, 224μF	300 μF, 300 μF

The TC and RC side tank capacitors are calculated using (5.16) and listed in Table 5.2. The voltage and current ratings of the devices and body diodes are calculated using (5.21)-(5.24), (5.37) and (5.38) for both G2V and V2G operations. The inductances of dc link inductors at close to unity power factor of CSI is given as

$$L_{\mathrm{d1}}\,, \qquad L_{\mathrm{d2}} = \frac{V_{\mathrm{d}} \times T_{\mathrm{s}}}{2\Delta I_{\mathrm{d1}}}\,, \quad (5.46)$$

where, $T_s = 1/f_{\mathrm{s}}$ and ΔI_{d1} is peak to peak current ripple in inductor L_{d1} current. Also, the capacitances of output capacitors are calculated as

$$C_{o1}\,, \qquad C_{o2} = \frac{T_{\mathrm{s}}/2 \times I_o}{\Delta V_{o1}}\,, \quad (5.47)$$

where, ΔV_{o1} peak to peak voltage ripple across capacitor C_{o1}. The dc link inductor values L_{d1} and L_{d2} are calculated considering a 20% ripple in inductor current and output capacitors C_{o1} and C_{o2} are calculated considering 5% voltage ripple at output voltage, V_{o}.

5.5 Experimental Results

A proof-of-concept hardware prototype rated at 1.2kW is developed to verify the analysis and operation of the proposed converter. Selected components are listed in Table 5.2. Fig. 5.11 shows the picture of the prototype. SKHI 61(R) is used as MOSFET gate driver and DSP TMS320F28335 is used as digital control platform. The IPT coils are UU shaped and it is similar to the coil used in Chapter 2 and 3. During G2V operation, an electronic load set at constant voltage (CV) mode is used to emulate 325V EV battery. During V2G operation this part is replace by a dc power supply.

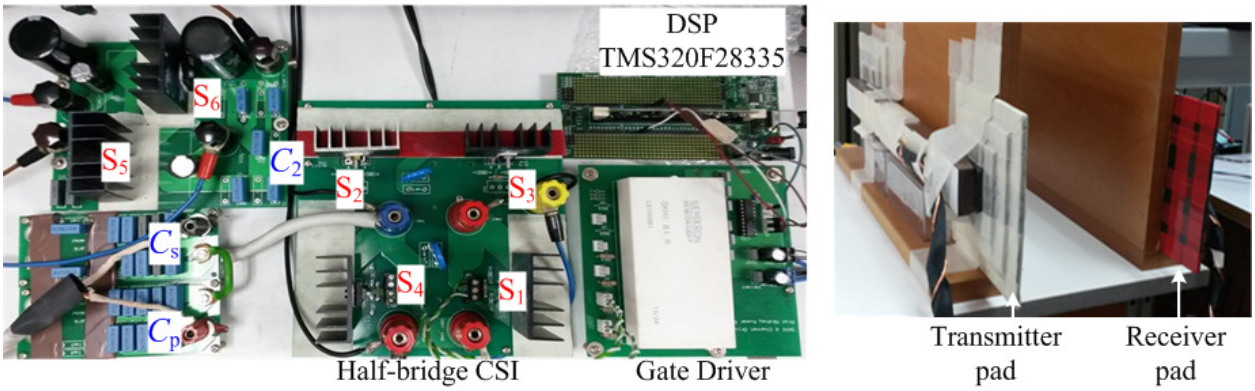


Fig. 5.11 Photograph of 1.2kW experimental set-up

5.5.1 G2V Operation

Fig. 5.12 and Fig. 5.13 show experimental results of G2V operation for 1.15kW and 900W power output and corresponding switching frequencies of the inverter are 47.2 kHz and 46.6 kHz, respectively. The duty cycle of the inverter devices is kept fixed to 0.52. Fig. 5.12a and Fig. 5.13a show the profiles of the voltage and current of the coils. It is clear that the TC and RC receives

almost pure sinusoidal voltage and current. Fig. 5.12b and Fig. 5.13b show voltage profiles of TC side tank network. From these waveforms, it is clear that the inverter output voltage, V_i is a fraction of TC voltage (V_1), where V_i directly determines the device voltage rating of CSI. Therefore, this is a major advantage of the proposed converter over simple parallel LC tank at TC side that inverter devices get lower voltage stress. From (5.18), (5.19) and (5.20) it is clear that this is achieved because of the presence of the series capacitor C_s.

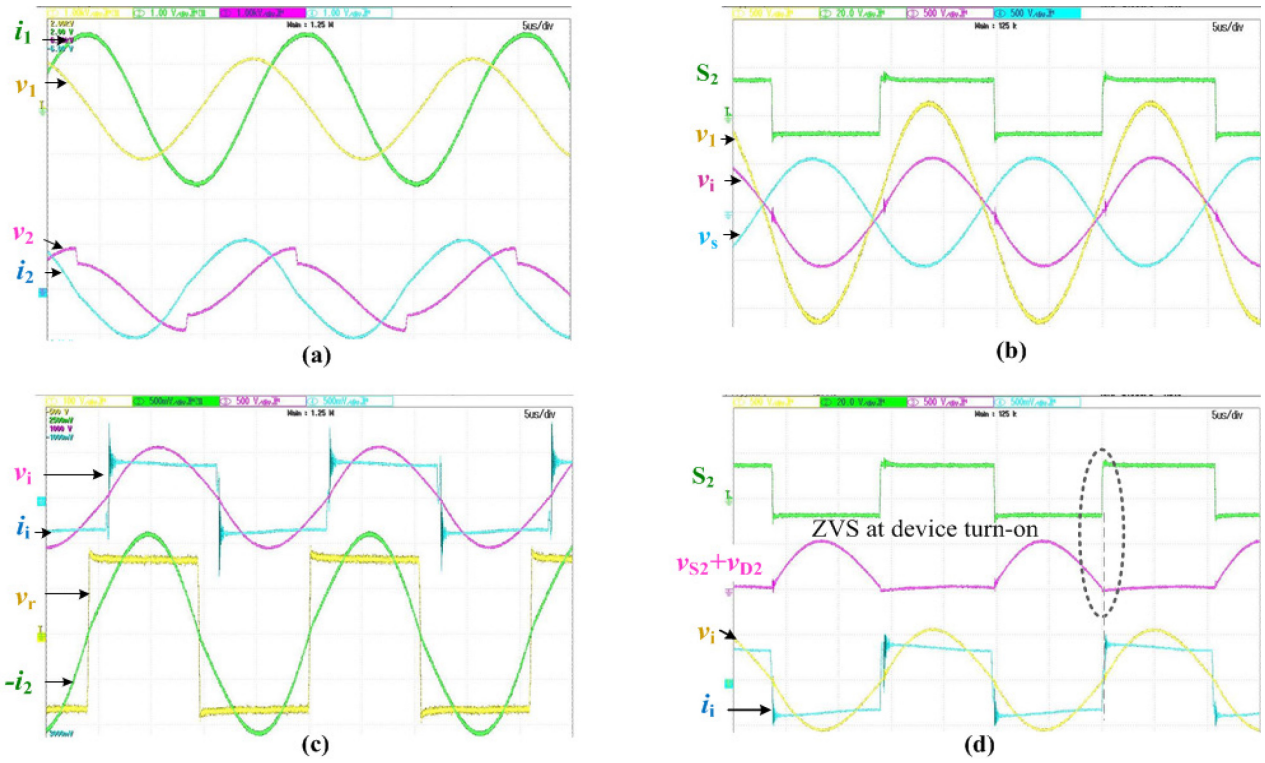


Fig. 5.12 Experimental results of G2V operation at f_s=47.2 kHz, P_o=1.15kW, V_o=325V (a) i_1 [10A/div], v_1 [1.0 kV/div], i_2 [10A/div], v_2 [1.0 kV/div]; (b) v_1, v_i, v_s [500V/div]; (c) v_i [500V/div], i_i [5A/ div], v_r [100V/div], i_2 [5A/ div]; (d) ZVS turn on of S2, v_{S2}+v_{S4} [500V/div], v_i [500V/div], i_i [5A/ div]

Fig. 5.12c and Fig. 5.13c shows the profiles of ac side voltages and currents of the inverter and rectifier during G2V operations. From these results it is clear that the power factor of the TC side converter is slightly lagging and this is suitable for ZVS turn-on of the devices. Also RC side rectifier voltage and current profiles are in the same phase and this ensures soft recovery of the diodes D_5 and D_6. Fig. 5.12d and Fig. 5.13d confirms ZVS turn-on of the TC side inverter devices because of lagging power factor operation. At the instant when S_1or S_2 is turned-on, the voltage

across the corresponding leg devices i.e. S_1-S_3 or S_2-S_4 are slightly negative. Devices S_3 or S_4 blocks this voltage and devices S_1 or S_2 are turned-on at zero voltage.

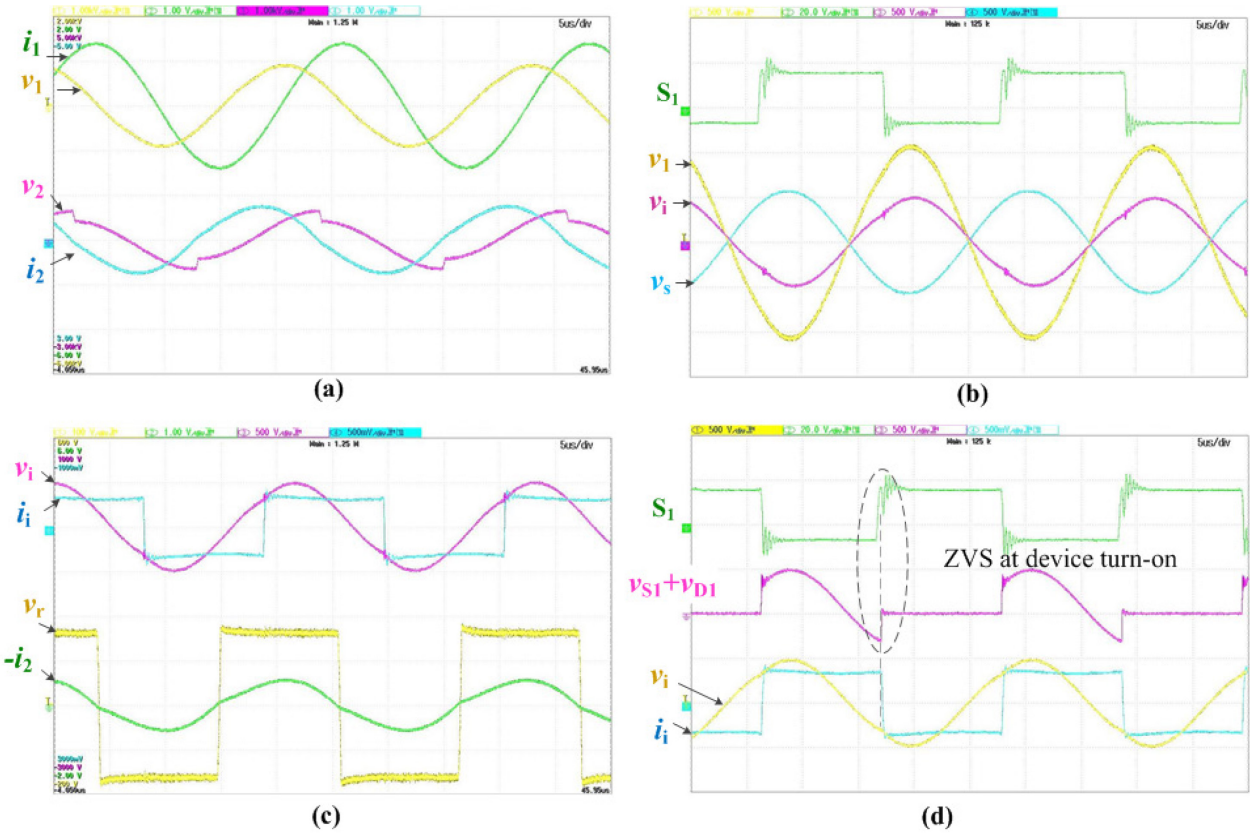


Fig. 5.13 Experimental results of G2V operation at f_s=46.6 kHz, P_o=900W, V_o=325V **(a)** i_1 [10A/div], v_1 [1.0 kV/div], i_2 [10A/div], v_2 [1.0 *k*V/div]; **(b)** v_1, v_i, v_s [500V/div]; **(c)** v_i [500V/div], i_i [5A/ div], v_r [100V/div], i_2 [10A/ div]; **(d)** ZVS turn on of S_1, v_{S2}+v_{S4} [500V/div], v_i [500V/div], i_i [5A/ div]

Fig. 5.14 shows experimental results of G2V operation at 975W power transfer and corresponding switching frequency is 50 kHz. From Fig. 5.8 it is clear that this operating region is in leading power factor region. Fig. 5.14 results validates this operation and the inverter devices S_1 and S_2 experience soft-switching at turn-off due to leading power factor at inverter output. This operation is significant if the inverter devices are selected as IGBTs to ensure zero turn off loss.

Fig. 5.15 shows plot of efficiency verses output power during grid to vehicle operation. The transmitter and receiver coil unloaded coupling factors are 250 and 200 respectively—i.e., the internal resistances are 0.26Ω and 0.32Ω respectively. At rated load the coil to coil power loss is

around 4.8% of rated power input and this is more than 60% of overall power loss. Therefore, major efficiency improvement is possible by using optimum sized and shaped coils.

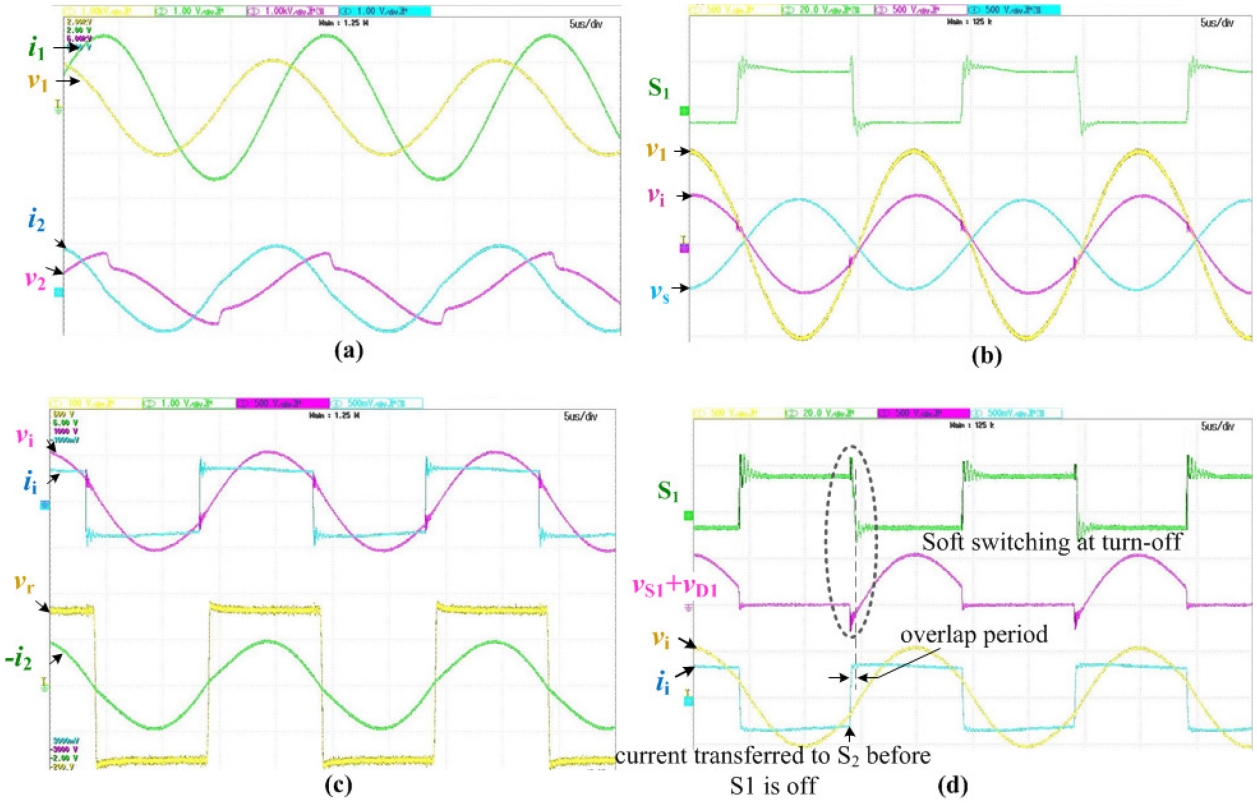


Fig. 5.14 Experimental results of G2V operation at f_s=50 kHz, P_o=975W, V_o=325V **(a)** i_1 [10A/div], v_1 [1.0 kV/div], i_2 [10A/div], v_2 [1.0 kV/div]; **(b)** v_1, v_i, v_s [500V/div]; **(c)** v_i [500V/div], i_i [5A/ div], v_r [100V/div], i_2 [10A/ div]; **(d)** ZVS turn on of S_1, v_{S2}+v_{S4} [500V/div], v_i [500V/div], i_i [5A/ div]

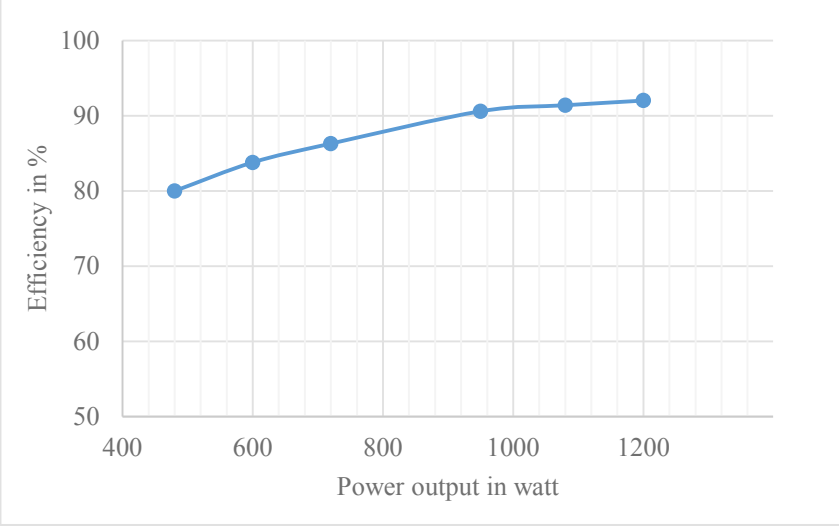


Fig. 5.15 Plot of efficiency verses output power during grid to vehicle operation

5.5.2 V2G Operation

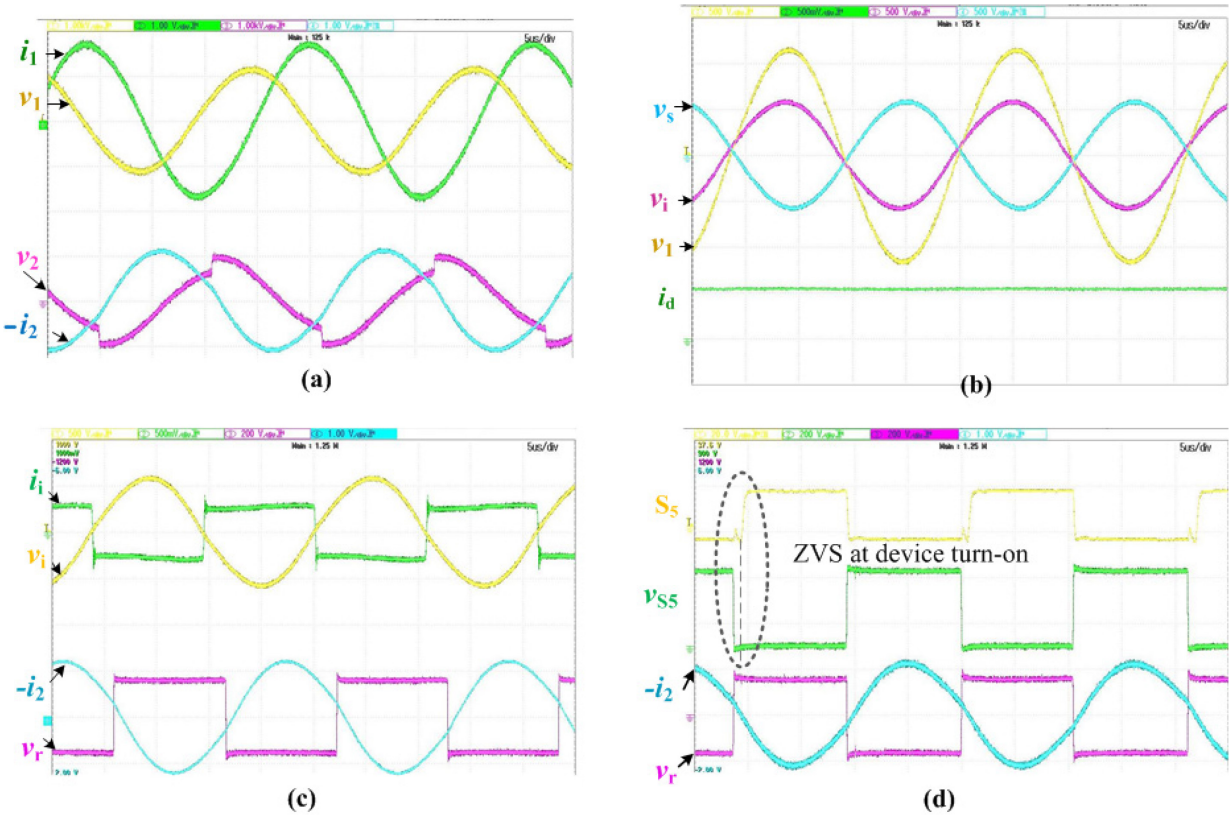


Fig. 5.16 Experimental results of V2G operation at f_s=55.5 kHz, P_o=950W, V_o=325V **(a)** TC and RC currents and voltages, i_1 [10A/div], v_1 [1.0 kV/div], i_2 [10A/div], v_2 [1.0 kV/div]; **(b)** Voltage across TC side tank components, v_1, v_i, v_s [500V/div] i_d [2A/div]; **(c)** Voltages and currents at inverter output and rectifier input, v_i [500V/div], i_i [5A/ div], v_r [200V/div], i_2 [5A/ div]; **(d)** v_{S5} [200V/div], v_r [200V/div], i_2 [10A/ div].

Fig. 5.16 and Fig. 5.17 show the experimental results of V2G operations for 950W and 760W and corresponding switching frequencies are 55.5 *k*Hz and 57.5 *k*Hz, respectively. During V2G operation, the vehicle side voltage doubler circuit operates as VSI with a fixed duty cycle 0.5. Both Fig. 5.16a and Fig. 5.17a show that the coil voltages and currents are almost harmonic free. Fig. 5.16b and Fig. 5.17b show the voltage profiles of TC (V_1), series capacitor (V_s), and parallel capacitor (V_i). Form these results, it is clear that parallel capacitor voltage, V_i receives only a fraction of TC voltage, V_1. Since the voltage V_i directly determines the voltage rating of the converter devices; therefore, the proposed topology is capable of reducing device voltage during V2G operation.

From Fig. 5.16c and Fig. 5.17c, it is clear that the ac side voltage and current profiles of grid side converter are in the same phase due to passive rectification. Also, ac side voltage and current

profiles of voltage doubler is slightly lagging and this is suitable for ZVS turn-on of the devices S_5 and S_6. Fig. 5.16d and Fig. 5.17d shows the ZVS turn-on of inverter device S_5. Similar to device S_5, device S_6 also experiences ZVS at tuen-on.

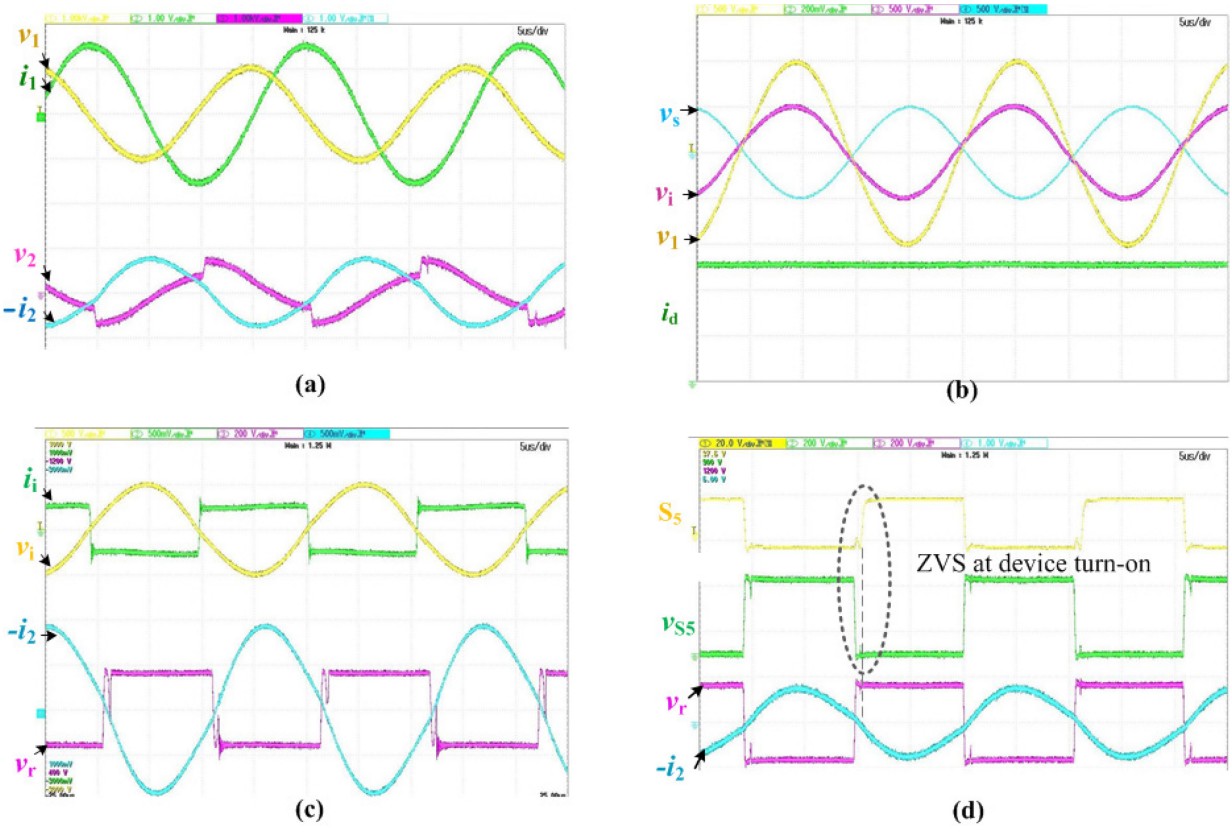


Fig. 5.17 Experimental results of V2G operation at f_s=57.5 kHz, P_o=760W, V_o=325V **(a)** i_1 [10A/div], v_1 [1.0 *k*V/div], i_2 [10A/div], v_2 [1.0 *k*V/div]; **(b)** v_1, v_i, v_s [500V/div] i_d [2A/div]; **(c)** v_i [500V/div], i_i [5A/ div], v_r [200V/div], i_2 [10A/ div]; **(d)** Soft-switching, v_{S5} [200V/div], v_r [200V/div], i_2 [10A/ div]

Fig. 5.18 shows the plot of efficiency verses output power during vehicle to grid operation. Similar to G2V operation, the wireless coil to coil power transfer contributes major power loss in the converter circuit. The proof-of-concept hardware is not optimized for packaging, volume, and components. Therefore, the obtained efficiency is close to 92%. Compared with the maximum reported efficiency 95% [75], [76] this converter efficiency is less. Efficiency can be further improved by using improved quality factor coils. The experimental results match closely with the analytically predicted waveforms. The performance is observed to be satisfactory.

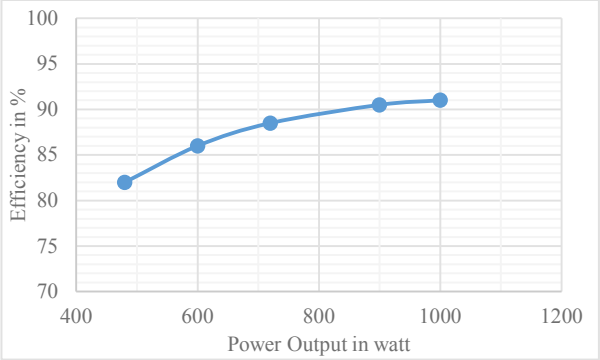


Fig. 5.18 Plot of efficiency verses output power during vehicle to grid operation.

5.6 Conclusions

The contribution and focus of this research is to propose, analyze, and develop a new power electronics system for wireless power transfer with G2V and V2G capability. A new current-fed topology with bidirectional ability and current-sharing and voltage doubling features has been proposed. The proposed topology is analyzed with a new series-parallel (*CLC*) tank network. The proposed tank network reduces the device rating of grid side devices and permits the use of devices with low on-state resistance and cost compared to usual parallel *LC* tank. Bidirectional wireless IPT is designed and developed using proposed current-fed inverter and *CLC* tank configuration. This is the first attempt to implement bidirectional IPT with current-fed circuit and demonstrate G2V and V2G operation. Keeping inverter output power factor lagging, ZVS turn-on of the inverter devices are always ensured irrespective of load variation. Complete mathematical analysis and systematic design is reported. Experimental results verify the reported analysis and design and demonstrate the operation and performance.

Chapter 6 IPT Topology using Direct Ac-Ac Converter with Active Source Current Waveshaping

6.1 Introduction

Generally, power in IPT system is processed through multiple power processing stages as shows in Fig. 6.1. This system is most popular because all control goals very effectively achieved through this system. The first stage, unity power factor (UPF) rectifier maintains high quality source current while maintain a fixed dc bus voltage. The next dc-ac inverter stage produces high frequency ac for transferring power wirelessly while ensuring load requirements and soft switching

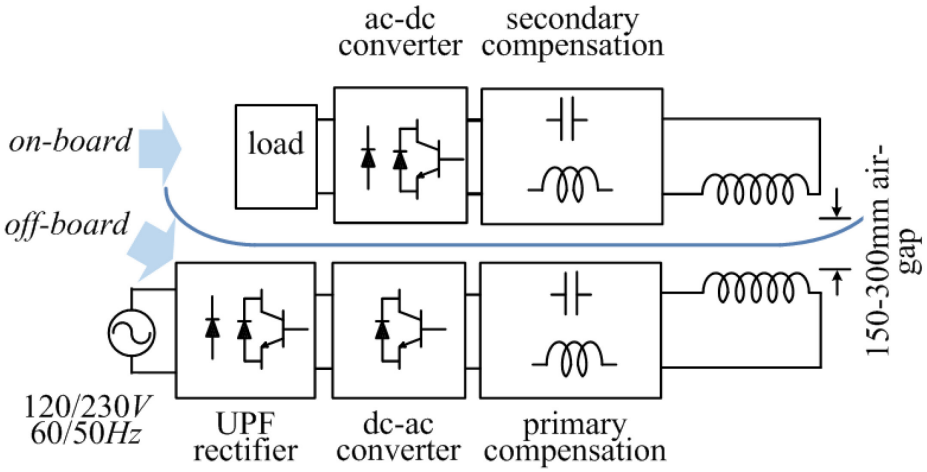


Fig. 6.1 A typical multi-stage inductive power transfer system for EV charging applications.

of inverter devices. The compensation in both the primary (or transmitter) and secondary (or receiver) coil is mandatory if the coil coupling is significantly low (generally coupling factor below 30% [62]). The last stage is ac-dc passive rectification stage. In some research, this ac-dc is done through active reification for improved performance and to meet stringent load requirements. Compared with conventional wired systems, wireless circuitry is larger, bulky and less efficient. This is primarily due to wireless coils. However, because of significant airgap between the coils, the coils must be large enough to get sufficient coupling for effective power transfer. Since, this research primarily focuses on power electronics; therefore, this part of work attempts to improve converter topology for mitigating these limitations.

6.1.1 Solutions with Direct Ac-Ac Converters

Recent research on IPT area shows that the first two power processing stages i.e. the UPF rectifier and high frequency dc-ac inverter can be replaced by a single stage direct ac-ac converter [27] - [31]. The possible advantages of this single stage power conversion are as follows.

i. Higher efficiency,
ii. Lower component count,
iii. Compact and
iv. Elimination of short lived bulky dc capacitor. This is possible with a consideration that the load accepts rectified sinusoidal current. However, in case the load does not accept this current profile then a reasonable size dc capacitor can be connected at the output of the converter.

Although, these points are very attractive but there are challenges associated with the control requirements. The direct ac-ac converter has to meet the following three major control requirements

i. high quality source current,

ii. load power and

iii. soft switching of inverter devices etc.

6.1.2 Existing Single Stage IPT Topologies

[29] shows variable switching frequency 50% fixed duty cycle charge control technique for three phase to single phase matrix converter. The required number of devices are less and the control technique ensures soft switching of all the ac-ac converter devices. [31] primarily focuses on zero current switching through energy-injection and free oscillation control of direct matrix converter for single-phase and three-phase inputs respectively. The reported frequency modulation is solely targeted to achieve ZCS of all the converter devices. It uses zero crossing detector (ZCD) to detect zero crossing of high frequency transmitter coil current. However, the input power quality and source current control aspects are not included in the reported energy-injection and free oscillation control method. [30] Presents phase shift modulation of 3-phase to single phase matrix converter for a series-series compensated IPT converter. The required number of semiconductor devices are less and overall converter efficiency is high. Major emphasis is given to achieve proper switching

strategy of matrix converter, followed by detailed converter loss analysis considering the load is a resistor connected in series with RC. Therefore, source current waveshaping, load requirements and dynamic performance aspects of the converter are not considered. Although, [27] reports input power quality aspects with a buck derived matrix converter topology for resistive load, but due to very low voltage available near zero crossing of input voltage, high quality source current cannot be maintained. The major challenges for achieving power factor correction with the existing matrix converter based IPT topologies are reported as follows.

6.1.3 Challenges with Existing Single Stage IPT to Achieve Unity P.F.

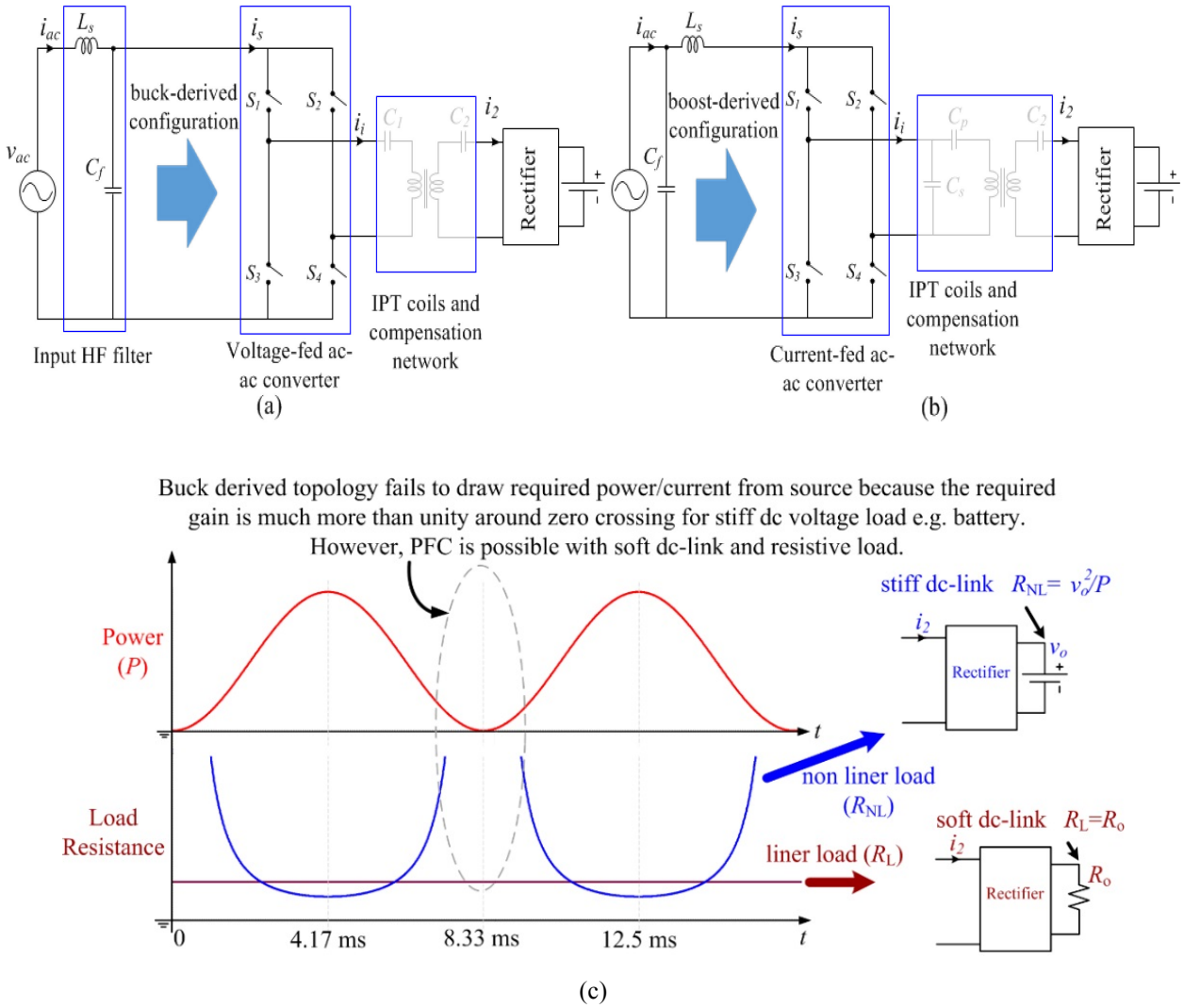


Fig. 6.2 (a) General powertrain of existing IPT topology with direct ac-ac converter, (b) Required structure of single stage IPT topology (c) profiles of input power and corresponding equivalent impedance for resistive and battery type load for UPF operation

In conventional multi-stage IPT topologies shown in Fig. 6.2 the converter before the resonant tank is generally voltage source inverter (VSI). VSI imposes to select primary tank network as series *LC* [2], [14], [21], [22], [23] *LCL* [46], [62] or *LCCL* [47], [62] etc. Generally, these same tanks are used to realize the IPT topology with direct ac-ac converter because their properties are well established in the literature [27] - [30]. However, when these tanks are used in single stage direct ac-ac converter, the input to the converter is required to be stiff voltage.

Fig. 6.2a shows general structure of exiting direct matrix converter topologies where the main converter has buck derived configuration when viewed from source side. Most of the existing study have been carried out considering the load is resistive and it is connected either directly with RC side tank or at the output of rectifier [27], [29], [30]. Therefore, the matrix converter perceives the load as linear load as shown in Fig. 6.2c. These topologies will fail to control input current when a stiff dc voltage load such as battery is connected at rectifier output. This is because the equivalent load impedance varies significantly with this type of load as shown in Fig. 6.2c. The practical interpretation is that the buck derived ac-ac converter topology does not get sufficient input voltage around zero crossing to feed power to high voltage output dc bus. This challenge is similar with regular buck-derived PFCs that near zero crossing of source voltage it fails to boost the input voltage to the required output voltage. Like regular buck derived PFCs, the source current quality with the existing ac-ac converters are highly compromised. Clearly, the boost derived topology will be suitable for this application to achieve power factor correction as shown in Fig. 6.2b.

6.1.4 Scope of Current-fed Topologies in Single stage IPT

Current-fed full-bridge and half-bridge resonant IPT converters are reported for EV applications [77], [78], [79] and current-fed push-pull resonant IPTs are reported for biomedical implants [55], [56], [69]. The advantage of push-pull configuration in IPT application is that only two controlled devices or MOSFETs are required in the converter circuit. The gate driver circuit is very simple because the source terminals of both the MOSFETS are connected to a common point as DC input ground terminal [69], [80]. Generally, control of these converters is done through variable switching frequency fixed duty cycle method. The switching frequency is solely determined by the inverter output voltage, v_i and it is done by sensing zero crossing of v_i. This helps to achieve both ZVS turn-on and turn-off of both the devices [69], [80].

6.1.4.1 Challenges with Existing Current-fed Push-Pull Converter

In an IPT powertrain where input to the matrix converter is line frequency ac, the existing push-pull converter will find challenges due to requirement of extra control for maintaining source current quality. Since, this converter is generally controlled through variable switching frequency (f_s) where the f_s is solely determined by the converter output voltage zero-crossing; therefore, it is challenging to add extra constraint to the controller such as source current waveshaping. Although there is an inductor at input to the push-pull converter, but the boost mode operation is not possible due to fixed 50% duty cycle. Other challenge of this control method is to start-up the converter because of zero voltage at inverter output. Other limitations include detection of ZVS operating points and avoiding frequency bifurcation (multiple zero phase angle points) [69]. Also, zero crossing of inverter output voltage is a single operating point. Therefore, exact detection of that point and turning on one MOSFET and turning off the other MOSFET without the delay of sensor and control is a challenge. If this control is not done accurately then the parallel capacitor at the converter output gets short circuited through MOSFETs and body diode of other MOSFET [77]. For, higher power applications the inverter output voltage magnitude is high and it rises sharply after zero crossing. Therefore, if the MOSFETs are not turned-on and turned-off exactly at zero crossing then the tank capacitor will be short circuited through MOSFET and body diode. This will result significant power loss. For these reasons, the application of these topologies are generally limited to low power such body implants [55], [56], [77].

6.2 Proposed IPT for Unity P.F. Operation

Fig. 6.3 shows complete circuit of the proposed IPT topology where TC side tank is parallel-series (CLC) and RC side is series LC type. The basic operation of this converter is like a boost derived PFC. When the current through the source inductor, L_s is required to be raised then ac-ac converter is switched such that L_s directly gets connected to source voltage, v_{ac} through converter devices. During other times, the L_s is connected to transmitter side tank network through ac-ac converter devices. Because the input to the ac-ac converter is stiff current; therefore, the transmitter side tank network is required to be parallel. Parallel tank has several advantages in IPT systems. The high volume of reactive component of current passes through the parallel capacitor, C_p without flowing though the inverter devices; therefore, inverter device current stress is generally lower. Also, the coil current profile is very close to sinusoidal because the parallel capacitor, C_p offers

much lower impedance to higher order harmonics compared to Transmitter coil (TC). Input inductor, L_s provides natural short circuit protection during inverter fault [77], [79]. Moreover, compared with conventional parallel LC tank, the proposed converter has an extra series capacitor connected with TC to reduce the device voltage stress and to improve the quality of TC current. Also, with parallel tank the lagging power factor for ZVS of inverter devices are obtained below resonance frequency whereas for series tank it is achieved above resonance frequency.

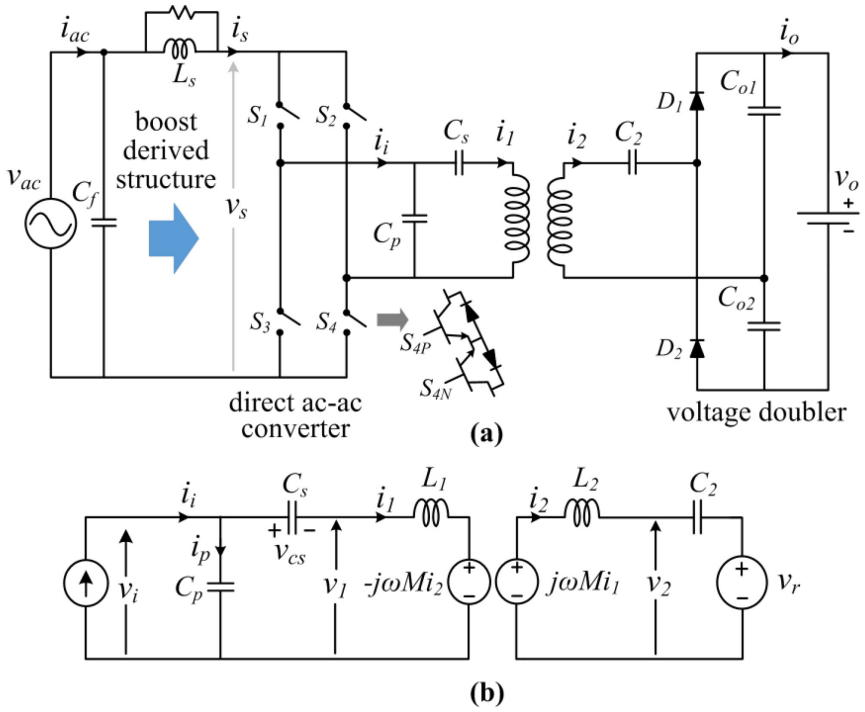


Fig. 6.3 (a) Proposed ac-ac converter for IPT applications and (b) equivalent circuit of the resonant tank network

In the receiver side a capacitor, C_2 is connected in series with receiver coil (RC) to achieve the required compensation and this ensures least number of components in RC side. The rectifier in RC side is selected to be a voltage doubler to achieve higher voltage gain while reducing the number of rectifier diodes.

6.2.1 Performance Comparisons with Existing Topologies

Table 6.1 lists several important aspects of different IPT topologies with direct ac-ac converter reported in literature. This gives a clear picture of the contributions of this research work compared with other reported IPT topology with matrix converter. With this understanding, the preferred selection of ac-ac converter will be a current-source topology.

Table 6.1. Qualitative comparison of different IPT topologies with direct ac-ac converter reported in literature

Topology	**TC and RC tank configuration**	**Control technique**	***f*s (kHz)**	**Load demand fulfilled**	**Dynamic model Reported**	**Achieved high quality source current**	**Soft switching**	**Power level**
Single stage 3phase [29]	TC: LC series RC: LC parallel	Variable f_s;	12.3; ZCD required	Yes, using Power Regulation Control Mode	No	THD 14.3%, P.F. 0.59-0.67	Yes, ZCS of all devices	267 W
SiC-based matrix converter [30]	TC: (LC) RC: (LC)	Fixed f_s phase shift modulation	50	Not reported	No	No	Not achieved	300 W
Direct ac–ac Converter for IPT [31, 81]	TC: (LC) RC: Not reported	Variable f_s; energy-injection and free oscillation	30; ZCD required	Not reported	No	Not reported	Yes, ZCS of all devices	10 W
Matrix Converter with LCLC tank [27]	TC: LCCL RC: LCCL	Fixed f_s and variable duty cycle modulation	20; ZCD required	Yes, with phase shift control	No	Yes, but only for R load	Not reported	1 *k*W
Proposed boost derived ac-ac converter [82]	TC: parallel-series (CLC) RC: LC series	Fixed f_s and variable duty cycle	50	Yes, using output current loop	Yes	Yes, THD <5% PF: UPF	Yes, ZVS & ZCS of two devices	1.2*k*W

6.3 Steady State Operation of the Proposed Topology

To explain the operation, consider that S_1-S_4 are matrix converter devices i.e. two devices connected in reverse direction to achieve bi-directional voltage and current controlling facility. During positive half of the input voltage, v_{ac} only 4 devices are given switching frequency pulses. These devices are named as S_{1P}-S_{4P} respectively. Similarly, during negative half of input voltage, remaining 4 devices of ac-ac converter are given switching frequency pulses and these are named as S_{1N}-S_{4N} respectively. Here only one switching cycle of ac-ac converter during positive half of source voltage is presented in detail. Operation of the converter during negative half of source voltage is exactly similar where S_{1N}-S_{4N} takes the position of S_{1P}-S_{4P} respectively. During positive half of source voltage S_{1N}-S_{4N} are kept permanently off whereas, during negative half cycle of

source voltage S_{1P}-S_{4P} are kept off permanently. It is confirmed that operating the inverter at lagging power factor region ensures ZVS turn-on of the devices [78]. Therefore, in the steady state operation, ac-ac converter output voltage, v_i is considered to be leading with respect to current, i_i. To achieve the control goals, unipolar modulation scheme is adopted i.e. turn on time of S_1 and S_3 are same but phase shifted by 180^0. Similarly, turn on time of S_2 and S_4 are same but phase shifted by 180^0. Also, a slight overlap between complementary device pairs S_1 –S_2 and S_3-S_4 is always maintained to provide continuous current path to input inductor, L_s. Compared with voltage fed converter, one difference is that the complementary switching signals are not given within the leg devices, rather it is given to two top devices and two bottom devices. This technique is usual for current-fed inverters.

Interval 1 (t_0-t_1): During this interval ac-ac converter devices S_{1P} and S_{4P} are on. Therefore, the input inductor current, i_s flows through the transmitter coil (TC) side tank network. Fig. 6.4 shows voltage and current waveforms of different circuit components and Fig. 6.5a shows equivalent circuit of this switching interval. The voltages and currents of TC side components are given as

$$L_s \frac{di_s}{dt} = v_{ac} - v_i, \qquad i_{S1} = i_{s4} = i_s. \tag{6.1}$$

During this interval, in the receiver side the RC current is rectified by diode D_2. The voltages and currents of RC side elements are given as

$$v_{D1} = v_{o1} + v_{o2}, \qquad i_{D2} = i_2, \tag{6.2}$$

$$C_{o1} \frac{dv_{o1}}{dt} = -i_o, \qquad C_{o2} \frac{dv_{o2}}{dt} = i_2 - i_o., \tag{6.3}$$

Interval 2 (t_1-t_5): interval t_1-t_2 is switching overlap period between devices S_{1P} and S_{2P}. The duration of overlap period is almost negligible compared with one complete switching cycle but sufficient enough to transfer the input current from incoming to outgoing device. Since the voltage across S_{2P} is positive at time instant t_2; therefore, S_{2P} immediately starts conducting and current through S_{1P} is transferred even before its gate pulse is removed. Thus, at instant t_1 device S_{2P} experience hard turns-on whereas at instant t_2 S_{1P} experience zero current turn off. The equivalent circuit of this interval is shown in Fig. 6.5b. The voltages and currents of TC side components are given as

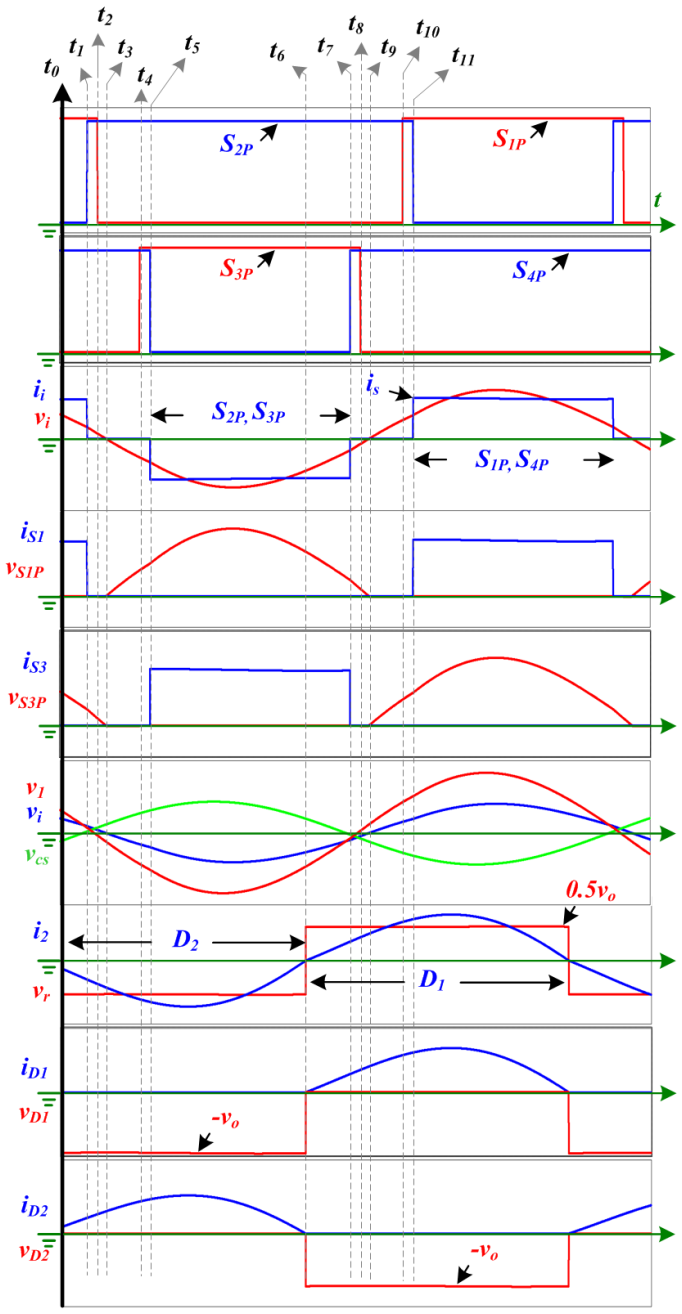


Fig. 6.4 Steady state operating waveforms of one switching cycle during positive half of source voltage.

$$L_s \frac{di_s}{dt} = v_{ac}, \qquad i_{S3} = i_{s2} = i_s. \tag{6.4}$$

At instant t_2, the gate pulse of S_{1P} is removed. However, the equivalent circuit of the converter remains same as Fig. 6.5b because current commutation from device S_{1P} to device S_{2P} is already occurred. At instant t_4 the overlap period of S_{3P} and S_{4P} starts. However, at this instant the converter output voltage, v_i is negative and the voltage across S_3 is negative. Although S_{3P} is triggered but

S_{3N} blocks this negative voltage present across S_3. Thus, S_{4P} keeps on conducting without transferring current i_i to S_{3P}. Therefore, S_{3P} is switched on at zero voltage. The overlap period of S_{3P} and S_{4P} gets over at instant t_5 and the equivalent circuit of the converter from t_1 to t_5 remains same as Fig. 6.5b. This interval (t_1-t_5) is similar to conventional boost converter turn on period.

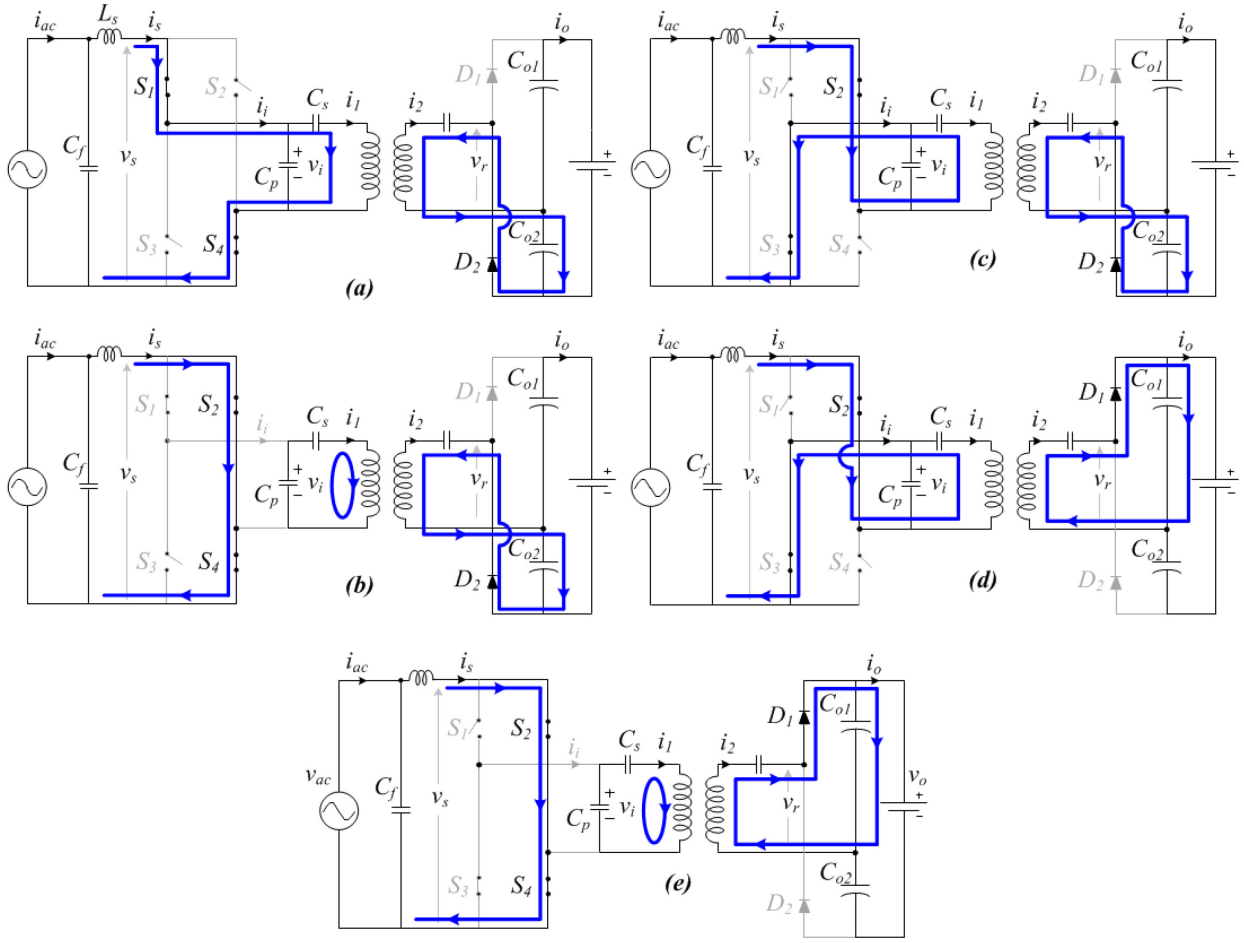


Fig. 6.5 Equivalent circuit during different interval of operations.

Interval 3 (t_5-t_6): At instant t_5 gating signal of S_{4P} is removed and it experiences hard turn off. Although the voltage across S_{3P} is negative but source inductor current, i_s forces S_{3P} to conduct because i_s has no alternate path. In this interval t_5-t_6 the source current flows through the TC tank network. The equivalent circuit of the converter circuit is shown in Fig. 6.5c. It is clear that this interval is similar to turn off time period of conventional boost converter where input inductor is directly connected to output. The current and voltage expressions of this interval are given as

$$L_s \frac{di_s}{dt} = v_{ac} + v_i \,, \qquad i_{S2} = i_{s3} = i_s. \tag{6.5}$$

Interval 4 (t_6-t_7): Although at time instant t_6 there is no switching transition in TC side but the current through the RC changes its polarity at this instant. Thus, the rectifier diode D_1 commutates D_2 and rectifies the RC coil current. The equivalent circuit of this interval is shown in Fig. 6.5d. the voltage and current expressions of receiver side components during this interval are given as

$$v_{D2} = v_{o1} + v_{o2} \,, \qquad i_{D1} = i_2 \,, \tag{6.6}$$

$$C_{o1} \frac{dv_{o1}}{dt} = i_2 - i_o, \qquad C_{o2} \frac{dv_{o2}}{dt} = -i_o, \tag{6.7}$$

Interval 5 (t_7-t_{11}): At instant t_7 S_{4P} is triggered and the interval t_7-t_{11} is switching overlap period. Similar to interval 2 the device S_{4P} immediately commutates S_{3P} because of the positive voltage present across S_{4P}. Therefore, S_{4P} experiences hard turn on at instant t_7 and S_{3P} experiences ZCS turn off at instant t_8. It is clear that S_{1P} and S_{3P} experiences both turn on and turn off soft switching whereas both S_{2P} and S_{4P} experiences hard turn on and hard turn off. The equivalent circuit of the converter during interval t_7 to t_{11} is shown in Fig. 6.5e. The steady state operation of the converter circuit repeats in this order.

6.4 Converter Design

In this section, a general converter design procedure is reported and later a specific design example is presented.

6.4.1 Tank Network Parameter Design

For a conventional transmitter parallel and receiver series tank network the required compensation capacitances to achieve zero phase angle (ZPA) at ac-ac converter output are derived as [62]

$$C_2 = \frac{1}{\omega_o^2 \times L_2}, \tag{6.8}$$

$$C_p = \frac{L_1}{\frac{\omega_o^4 M^4}{R_{oeq}^2} + \omega_o^2 L_1^2}. \tag{6.9}$$

where, ω_o is the resonance frequency in rad/s, L_1, L_2 and M are self-inductances of TC, RC and mutual inductance of the coils respectively. R_{oeq} is equivalent load resistance at the ac side of

rectifier. However, in the proposed topology one extra capacitor is connected in series with TC to improve the performance of conventional transmitter parallel and receiver series compensated IPT circuit. Therefore, in presence of series capacitor, C_s the required parallel capacitor value modifies as

$$C_p = \frac{L_1 - \frac{1}{\omega_o^2 \times C_s}}{\frac{\omega_o^4 M^4}{R_{oeq}^2} + \omega_o^2 \left(L_1 - \frac{1}{\omega_o^2 \times C_s}\right)^2}. \tag{6.10}$$

In this work, the value of series capacitor, C_s is chosen such that at resonance frequency the effective value of impedance offered by TC self-inductance becomes half. Therefore, the simplified value of parallel capacitor becomes

$$C_p = \frac{0.5L_1}{\frac{\omega_o^4 M^4}{R_{oeq}^2} + 0.25\omega_o^2 L_1^2}. \tag{6.11}$$

6.4.2 Voltage and Current Ratings

Applying Kirchhoff's Current Law (KCL) at RC side of Fig. 6.3b converter equivalent circuit, the rectifier input current in terms of output current is derived as

$$I_2 = \frac{\pi}{\sqrt{2}}.I_o\,, \tag{6.12}$$

Applying power balance between output and input of the rectifier and using (6.12), the rectifier input ac voltage RMS is derived as

$$V_r = \frac{2\sqrt{2}}{\pi} \times \frac{V_o}{2} = \frac{\sqrt{2}}{\pi} \times V_o\,. \tag{6.13}$$

Since, this RC side rectifier is a passive rectifier; therefore, the voltage V_r and current I_2 are in same phase and these phasors are considered as reference phasors. Referring to the coupled inductor equivalent circuit of the coupled IPT coils as shown in Fig. 6.3b and applying Kirchhoff's Voltage Law (KVL) at RC side loop, the TC current is derived as

$$I_1 = -j\frac{V_r}{\omega_o M}. \tag{6.14}$$

Using this current expression and adding the induced voltage in TC due to RC current, the TC voltage is derived as

$$V_1 = \frac{L_1}{M} V_r - j \frac{\omega_o M}{R_{oeq}} V_r \,. \tag{6.15}$$

Using (6.14) and (6.15) and applying KVL and KCL at the TC tank network, the ac-ac converter output voltage and current are derived as

$$V_i = \left(\frac{L_1}{M} - \frac{1}{\omega_o^2 M C_s}\right) V_r - j \frac{\omega_o M}{R_{oeq}} V_r, \tag{6.16}$$

$$I_i = \frac{\omega_o^2 M C_p}{R_{oeq}} V_r + j \frac{V_r}{\omega_o M} \left(\omega_o^2 C_p L_1 + \frac{C_p}{C_s} - 1\right). \tag{6.17}$$

6.4.3 Soft switching

Referring to steady state operation, to achieve ZVS turn-on and ZCS turn-off of converter devices S_1 and S_3, the operating power factor of ac-ac converter output is required to be lagging. Therefore, it is important to know the operating power factor of converter. From Fig. 6.3b equivalent circuit the impedance at the input of tank network is derived as

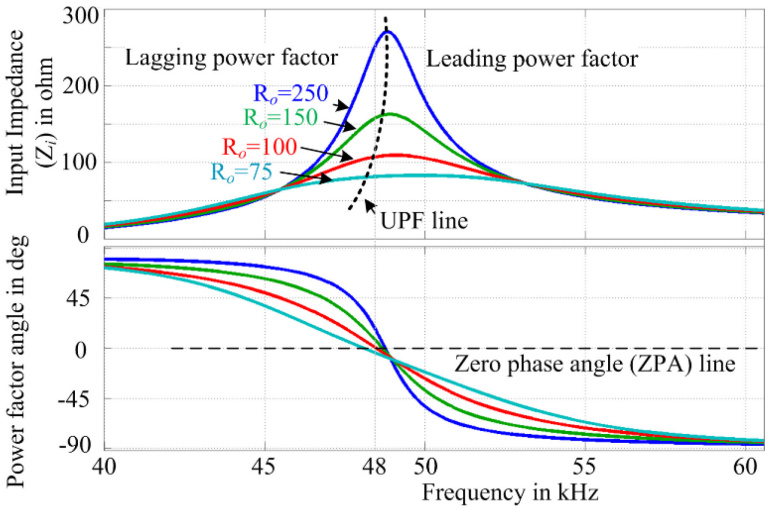


Fig. 6.6 Variation of tank network input impedance with switching frequency

$$Z_i = \frac{1}{j\omega C_p} // \left[\left\{j\omega(L_1 - M) + \frac{1}{j\omega C_p}\right\} + \left\{j\omega M // \left(j\omega(L_2 - M) + \frac{1}{j\omega C_p} + R_{oeq}\right)\right\}\right]. \tag{6.18}$$

Fig. 6.6 shows the variation of tank network input impedance and phase angle with change in operating frequency. From the figure it is clear that below the resonance frequency the operating power factor is lagging and in the other side it is leading power factor. This is an advantage of this tank network that the lagging power factor operation is achieved below the resonance frequency whereas for series LC tank it occurs above the resonance frequency.

6.4.4 Design Example

Referring to Fig. 6.3 equivalent circuit, the total volt-amp (VA) transferred from transmitter to receiver coil is given as

$$VA_{TC-RC} = (-j\omega_o M I_2) \times I_1. \tag{6.19}$$

Using (6.12) the real power transferred from TC to RC is derived from (6.19) as

$$P_{TC-RC} = \frac{\pi}{\sqrt{2}} \omega M I_o I_1 \,. \tag{6.20}$$

From (6.20) it is clear that the amount of real power transferred wirelessly from coil to coil is directly dependent on operating frequency, coil mutual inductance and TC coil current. Generally, during design of the converter the rated real power transfer is given and output current, I_o is calculated using it. Also, considering the availability of semiconductor devices, power level and other given standards the ac-ac converter switching frequency is known. Therefore, only two design parameters are unknown i.e. M and TC coil current, I_1. In the reported IPT converter designs generally choose a suitable value of TC coil current based on litz wire current carrying capacity. This selection directly impact on mutual inductance and IPT pad size. Once the mutual inductance is known, the coil self-inductance is determined from the actual coil. Generally, for a given M, the longer airgap distance leads to larger IPT coil and for shorter airgap the coil size is smaller. The remaining tank circuit parameters and voltage and current ratings of converter devices and diodes are calculated from the general expressions presented before. The maximum current ripple of the input ac inductor, L_s is possible when converter operates at full duty cycle and input ac voltage is at peak value. Therefore, the inductance of input inductor is given as

$$L_s = \frac{\sqrt{2}\, V_{ac} \times T_s}{2\Delta I_s}, \tag{6.21}$$

where, $T_s = 1/f_s$ and ΔI_s is peak to peak current ripple in inductor, L_s current. Also, the capacitances of output capacitors are calculated as

Table 6.2. Circuit parameters

Parameters	Selected Values
Input voltage, V_{ac}	200V ac, 60 *Hz*
Rated output power	1200 W
Switching frequency	48 *k*Hz
TC coil inductance, L_1	132 μH
RC coil inductance, L_2	137 μH
Mutual inductance, M	29.5μH
Tank capacitors, C_p, C_s, C_2	155 *n*F, 155 *n*F, 82 *n*F
Input inductor, L_s	1.3 *m*H
Input filter capacitor, C_f	2.2 μF
Output capacitors, C_{o1}, C_{o2}	5 μF
Output voltage	270V dc
Inner loop controller, H_i	$\frac{0.3}{\frac{s}{15000}+1}$
Outer loop controller, H_o	$\frac{25}{s}$

$$C_{o1} = C_{o2} = \frac{T_s/2 \times I_o}{\Delta V_{o1}} = \frac{T_s/2 \times I_o}{\Delta V_{o2}}, \qquad (6.22)$$

where, ΔV_{o1} and ΔV_{o2} are peak to peak voltage ripple across capacitor C_{o1} and C_{o2} respectively. The input inductor L_s is calculated considering a 20% ripple in inductor current and output capacitors C_{o1} and C_{o2} are calculated considering 5% switching frequency ripple at output voltage, V_o. Table 6.2 lists the designed circuit parameters for a 1.2kW IPT system with a supply voltage 200V, 60Hz ac. This system is used later for experimental verification.

6.5 Proposed Closed-loop Control Technique

6.5.1 Two Loop Control

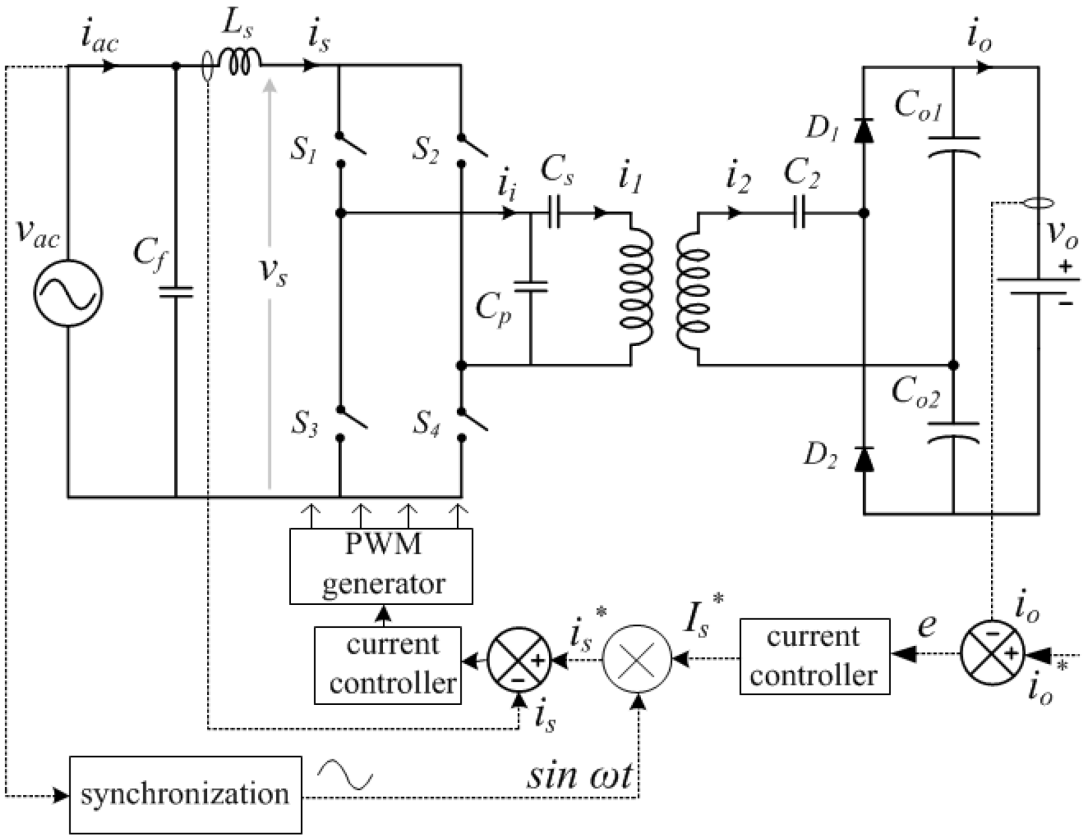


Fig. 6.7 Block diagram of complete control loop.

The proposed IPT topology is controlled though two loop control method. From steady state operation it is clear that the basic operation of this ac-ac converter is similar to a boost converter. When devices in same leg are O_N simultaneously i.e. either S_1-S_3 or S_2-S_4 are O_N it is similar to boost converter device turn-on interval. Similarly, when either diagonal (S_1-S_4) or off-diagonal (S_2-S_3) device pairs are O_N then the converter input gets directly connected to the output capacitor and it is equivalent to boost converter turn-off time interval.

The outer output current loop is used to regulate the converter output current whereas the inner input inductor current loop is used to achieve unity power factor at ac-ac converter input. The detailed control loop diagram is presented Fig. 6.7. The input voltage polarity determines which device set will be triggered. When input voltage polarity is positive, devices S_{1P}-S_{4P} are triggered and similarly, S_{2N}-S_{4N} are triggered when input voltage is negative.

6.5.2 Inner Input Current Control Loop

The input of the inner loop is duty cycle and output is source side inductor current, i_s. The dynamic expression of inductor current for a switching cycle is given as

$$L_s \frac{di_s}{dt} = v_{ac} - v_s \,, \tag{6.23}$$

where, v_{ac} is source voltage and v_s is voltage at ac-ac converter input. All these state variables are average value over a converter switching cycle. Fig. 6.8a shows typical voltage and current waveform at ac-ac converter output. Considering the duty cycle of ac-ac converter device S_1 is 'd' ($0 \le d \le 0.5$), the converter average input voltage in terms of output RMS voltage is derived as

$$v_s = \frac{2\sqrt{2}}{\pi} V_i \times cos\ \alpha \times \sin \pi d \,. \tag{6.24}$$

where, α is power factor angle at ac-ac converter output. Since, the resonant tank is designed such that the ac-ac converter output power factor is close to unity. Therefore, for simplicity in derivation, $cos\ \alpha$ is considered unity. Considering small perturbations ($\tilde{\imath}_s$, $\tilde{v}_{ac}$, $\tilde{V}_i$, $\tilde{d}$) around the equilibrium points (i_s, v_{ac}, V_i, d)

$$L_s \frac{d(i_s + \tilde{\imath}_s)}{dt} = (v_{ac} + \tilde{v}_{ac}) - \frac{2\sqrt{2}}{\pi}\left(V_i + \tilde{V}_i\right) \times \sin \pi\left(d + \tilde{d}\right). \tag{6.25}$$

Therefore, applying Laplace transformation, the control to output transfer function for inner loop is derived as

$$G_i(s) = \frac{\tilde{\imath}_s(s)}{\tilde{d}(s)} = -\frac{2\sqrt{2}\, V_i \cos \pi d}{\pi} \times \frac{1}{sL_s} \,. \tag{6.26}$$

For a typical value of converter output voltage and duty cycle obtained from steady state operation, the frequency response of G_i is plotted in Fig. 6.8b. A first order transfer function, H_i is used to get a phase margin around 45^0 and 40 dB attenuation at switching frequency. Fig. 6.8b shows bode plot of compensated plant transfer function, G_iH_i and closed loop transfer function, G_iH_i /(1+ G_iH_i). The gain crossover frequency is around 11 *k*rad/s and this indicates closed loop settling time around 0.36 ms.

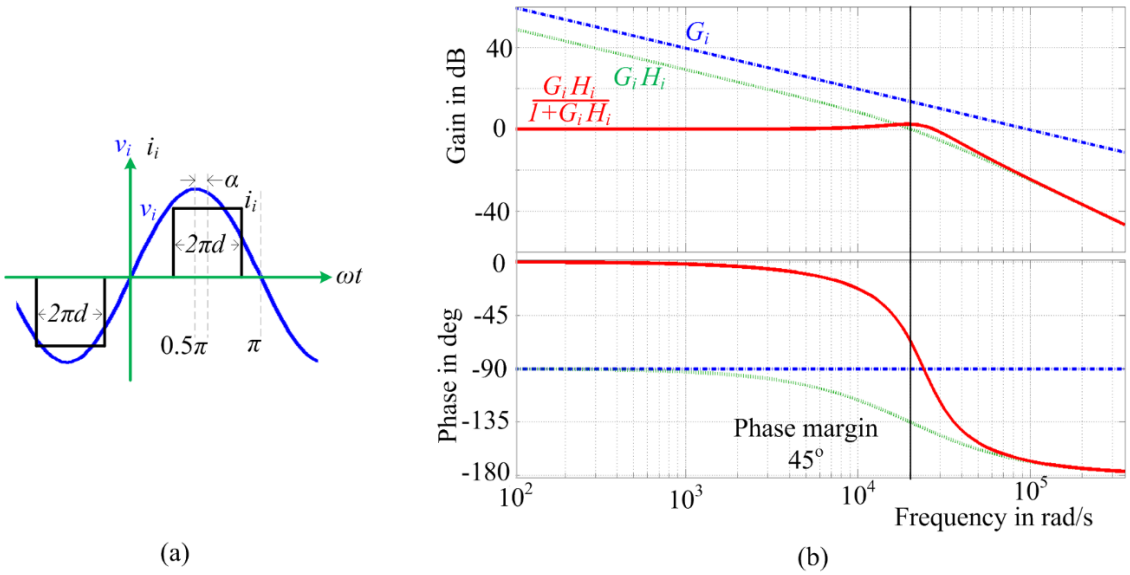


Fig. 6.8 (a) Ac-ac converter output voltage and current waveforms (b) Bode plot of inner current loop

6.5.3 Outer output voltage control loop

The input to this outer loop is line frequency ac current, i_s and the output is output voltage for resistive load or output current for a battery load. For simplicity, the outer loop plant transfer function is split as

$$G_o(s) = \frac{i_o(s)}{v_r(s)} \times \frac{v_r(s)}{i_i(s)} \times \frac{i_i(s)}{i_s(s)}. \qquad (6.27)$$

In (6.27) the three parts represent rectifier, resonant tank and ac-ac converter transfer functions respectively. To derive the voltage gain of the tank, a transformer equivalent circuit of the tank network is drawn as shown in Fig. 6.9. Form Fig. 6.9 the voltage across magnetizing inductance is derived as

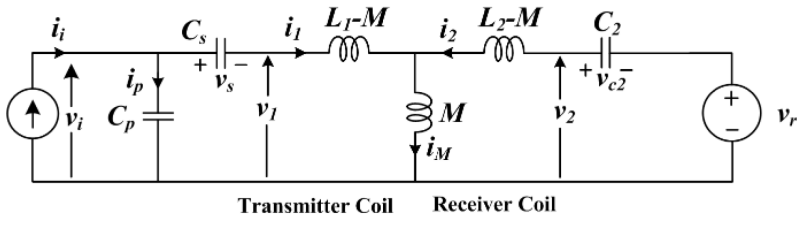


Fig. 6.9 Transformer equivalent circuit of the tank network

$$V_M = V_r - I_2 Z_2 = V_r - \frac{V_r}{R_{oeq}} Z_2 , \qquad (6.28)$$

where, $s = j\omega$ and R_{oeq} is equivalent load resistance at the input of voltage doubler circuit. Applying power balance at the input and output of voltage doubler circuit, R_{oeq} in terms of output resistance is calculated as

$$R_{oeq} = \frac{2}{\pi^2}.\frac{V_o}{I_o} = \frac{2}{\pi^2}R_o\,, \tag{6.29}$$

$$Z_2 = s(L_2 - M) + \frac{1}{sC_2}. \tag{6.30}$$

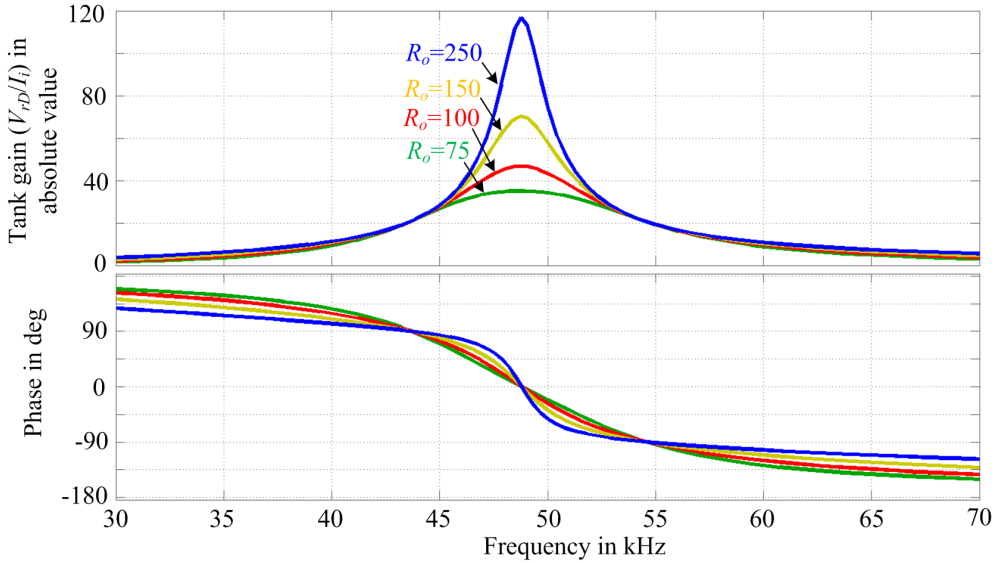


Fig. 6.10 Frequency response of the tank network

Therefore, using (6.28) the current fed converter output voltage is derived as

$$V_i = V_M + I_1 Z_1 = V_r\left(1 + \frac{Z_2}{R_{oeq}}\right) + V_r\left\{\frac{1}{sM}\left(1 + \frac{Z_2}{R_{oeq}}\right) + \frac{1}{R_{oeq}}\right\}Z_1\,, \tag{6.31}$$

where,

$$Z_1 = s(L_1 - M) + \frac{1}{sC_s}. \tag{6.32}$$

The voltage gain expression of the tank network is (V_r/V_i). However, the input to the tank network is actually I_i. Thus, the gain of the tank network is (V_r/I_i) and it is derived as

$$I_i = sC_pV_i + I_1 = V_r\left[(1 + sC_pZ_1)\left\{\frac{1}{sM}\left(1 + \frac{Z_2}{R_{oeq}}\right) + \frac{1}{R}\right\} + sC_p\left(1 + \frac{Z_2}{R_{oeq}}\right)\right]. \tag{6.33}$$

Fig. 6.10 shows the gain (V_r/I_i) and phase ($\angle V_r/I_i$) plot of the tank network of the proposed converter for different equivalent load resistances.

The dynamic expressions of the output capacitors are given as

$$C_{o1}\frac{dv_{o1}}{dt} = 0.5\langle i_2\rangle - i_o\,, \tag{6.34}$$

$$C_{o2}\frac{dv_{o2}}{dt} = 0.5\langle i_2\rangle - i_o\,, \tag{6.35}$$

where, C_{o1} and C_{o2} are two output capacitors and v_{o1} and v_{o2} are their voltages respectively. All these state variables are considered to be average values over a converter switching cycle. Since, i_2 is switching frequency ac quantity and its average value over a switching cycle is zero; therefore, half cycle average of i_2 as $\langle i_2\rangle$ is considered here. Considering C_{o1}=C_{o2}=C_o, the dynamic expression is derived by adding (6.34) and (6.35) as

$$C_oR_o\frac{di_o}{dt} = \frac{\langle v_r\rangle}{R_{oeq}} - 2i_o\,. \tag{6.36}$$

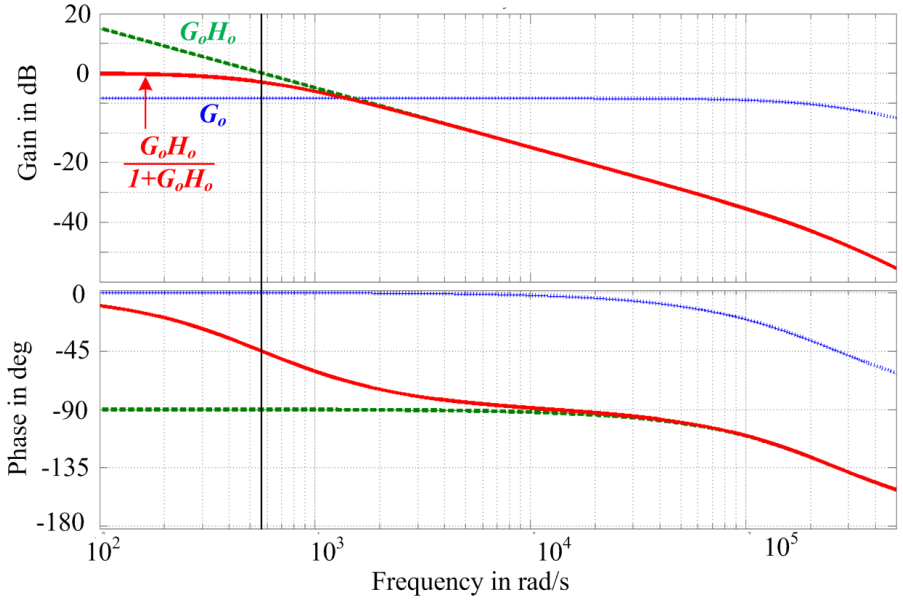


Fig. 6.11 Bode plot of outer loop

Applying Laplace transformation the gain expression is derived as

$$\frac{i_o(s)}{\langle v_r\rangle(s)} = \frac{\pi^2}{8R_o}\times\frac{1}{sC_oR_o+2}, \tag{6.37}$$

The ac-ac converter output current, i_i is a quasi-square wave with an amplitude of i_s as shown in Fig. 6.8a. Extracting fundamental component from the Fourier series of i_i, the ac-ac converter output to input current gain expression is given as

$$\langle i_i \rangle = \frac{8}{\pi^2} i_s \sin \pi d \,. \tag{6.38}$$

Therefore, the overall system transfer function is derived as

$$G_o(s) = \frac{k}{R_o} \sin \pi d \times \frac{1}{sC_o R_o + 2}, \tag{6.39}$$

where, *k* represents tank gain at operating switching frequency and it is obtained from Fig. 6.11. The bode plot of the plant transfer function is shown in Fig. 6.11. A simple integrator listed in Table 6.2 is used to get gain crossover frequency around 5.5 rad/s and attenuation to second harmonic (120 Hz) around 40dB. This design indicates a closed loop settling time around 0.75s.

6.6 Experimental Results

To verify the operation and control of the proposed IPT circuit a scale down proof-of-concept lab- prototype is built and experimental results are presented in this section. The circuit parameters are listed in Table 6.2.

6.6.1 Experimental Set-up

The ac-ac converter devices are mosfets with manufacturer part number C2M0080120D. The tank capacitors are all Epcos make, 700V RMS film capacitors. The IPT coils are circular type and the airgap between the TC and RC is around 25 cm. Since, the major focus of this research is to verify the performances of the proposed converter and not the IPT coil design; therefore, the details of circular coil design are not included here and it can be found in [62], [52]. It is already proven that the leakage magnetic flux can be kept well within the specified limit with the use of proper aluminum shielding [52]. However, when this IPT pad is used for direct ac-ac converter, there might be some low frequency (60Hz, 120Hz) flux present around the coil surroundings. Nonetheless, from fundamental point of view this pulsating low frequency leakage flux cannot impact any object when the switching frequency leakage flux i.e. the flux responsible for effective power transfer is kept within regulated limit. This is because the RMS values of induced voltage in this foreign object due to TC and RC are given as

$$V_{1\mathrm{F}} = 2\pi f M_{1\mathrm{F}} I_1 \quad \text{and} \quad V_{2\mathrm{F}} = 2\pi f M_{2\mathrm{F}} I_2 \tag{6.40}$$

respectively, where, M_{1F} and M_{2F} are mutual coupling of the foreign object with TC and RC respectively and *f* is frequency of pulsating flux . Therefore, the impact of this low frequency

pulsating magnetic field is about 1000 times lower than the switching frequency field. This is very similar to a case when a conductor carries line frequency current and a low frequency magnetic field exist around the conductor. This does not have significant impact on regular devices working nearby.

The rectifier side diodes are 400V fast recovery diodes and manufacturer part number is SCS215KGC. The ac-ac converter mosfets are driven with Semikron make SKHI 61(R) gate driver with rated switching frequency 50 kHz. Fig. 6.12 shows experimental set-up and 60 cm diameter circular coil.

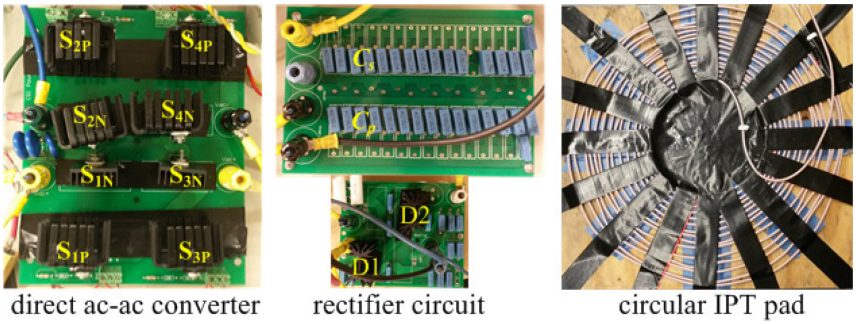


Fig. 6.12 Experimental set-up.

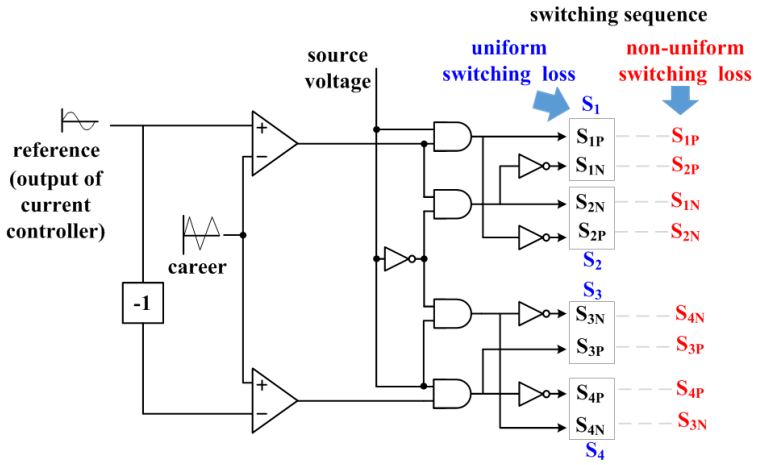


Fig. 6.13 Switching sequence generation circuit for uniform switching loss distribution

6.6.1.1 Balancing Uneven Power Loss of Inverter Devices

From practical implementation point of view, non-uniform power loss distribution leads to uneven structure of the converter in terms of heat sink design. Therefore, a simple logic circuit can be used such that during positive half cycle of line frequency the devices $S_1$and S_3 experience soft

switching and during negative half cycle S_2 and S_4 experience soft switching. Therefore, this will make the converter size regular and suitable for practical implementation. Fig. 6.13 shows this logic structure where the usual switching sequence is shown in red color and it leads to soft switching of S_1 and S_3 and hard switching of S_2 and S_4, repeatedly. However, during the negative half of input voltage the switching sequence can be interchanged as shown with blue color in Fig. 6.13, leading to uniform switching loss distribution among all the four sets of devices.

6.6.1.2 Gate Pulse Sequence

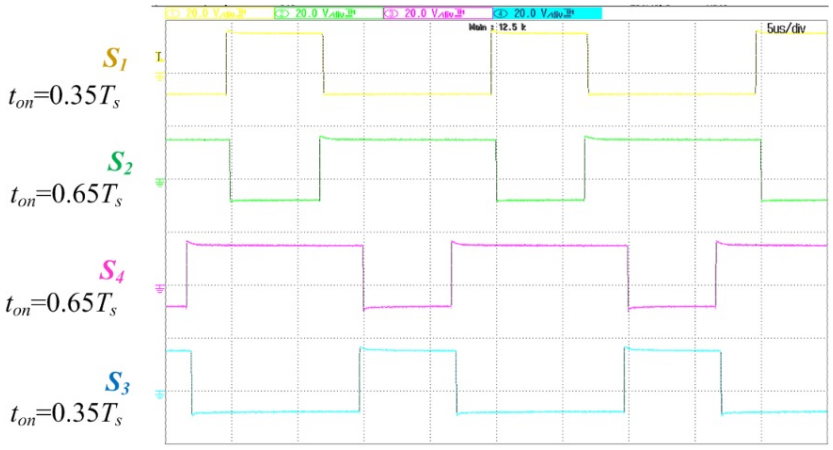


Fig. 6.14 Gate pulse sequence.

Fig. 6.14 shows typical gating signals of the proposed ac-ac converter devices when duty cycle of S_1 (or S_3) is D=0.35. The overlap duration between the complementary gating signals S_1 and S_2 are around 250nS and this is enough to turn on and turn off the mosfets. The overlap time is mainly dependent on turn-on time of incoming and turn-off time of outgoing devices and vice versa. This overlap time should be small enough such that converter duty cycle utilization is close to 100% but long enough to successfully turn-on and turn-off the incoming and outgoing devices respectively. In the experimental setup, the devices are MOSFETs; therefore, this duration is significantly less. However, with IGBT based converter circuit this overlap time will be slightly longer due to comparatively larger device turn-on and turn-off time. S_1 and S_3 have same length turn on time but 180^0 phase shifted. Similarly S_2 and S_4 have same duty cycle but 180^0 phase shifted. From Fig. 6.14 it is clear that only when S_1 and S_3 are on, the ac-ac converter input is connected to TC side tank network. Rest of the time the input inductor, L_s is directly connected across the source through the second leg of the ac-ac converter devices. Input voltage polarity is

used to determine whether to provide switching frequency pulses to positive device sets (S_{1P}-S_{4P}) or negative device sets (S_{1N}-S_{4N}).

6.6.2 Results with Resistive Load

Fig. 6.15 through Fig. 6.20 shows experimental results of the converter when the load is resistive whereas Fig. 6.21 through Fig. 6.24 shows results when load is stiff dc voltage. Since all the results have a line frequency and switching frequency components; therefore, line frequency views are shown in the middle figures whereas switching frequency views of the waveforms are shown in two sides. The zoomed view in the left side of every figure shows zoomed view at line frequency peak whereas the right-side figure shows zoomed view at off-peak of line frequency.

Fig. 6.15 shows experimental results of source voltage, current, ac-ac converter output voltage and current for 1200W power output and corresponding input voltage is 200V, 60Hz ac and output voltage is 300V dc. Since, ac-ac converter input current predominantly contains line frequency and switching frequency components; therefore, the small input filter is sufficient enough to filter out the switching frequency components. The total harmonic distortion (THD) of the source current is around 4.0% and it is well within IEEE 519-1992 specified standard (5%). From Fig. 6.15a and Fig. 6.15c zoomed waveform it is clear that the ac-ac converter out current waveform is a quasi-square but the voltage is very close to sinusoidal.

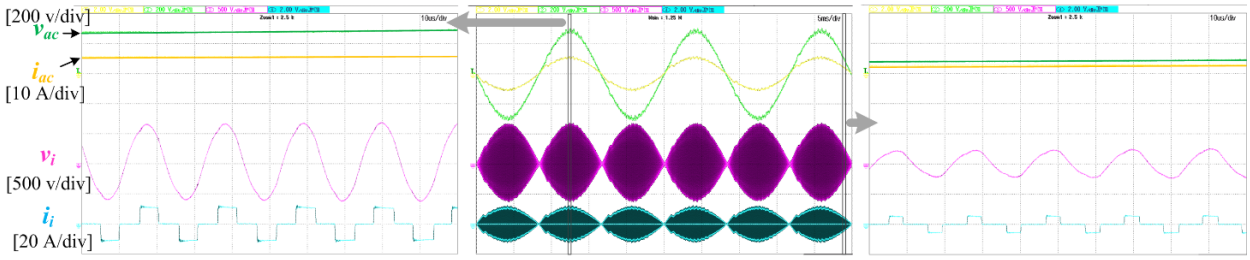


Fig. 6.15 Experimental results of grid voltage, current and ac-ac converter output voltage and current waveforms when V_{ac}=200V ac, P_o=1.2kW, V_o=300V (a) zoomed view at line frequency peak (b) line frequency view (c) zoomed view at off peak of line frequency.

Fig. 6.16 shows the voltage and current waveforms of both the transmitter and receiver coils. Fig. 6.16a and Fig. 6.16c zoomed waveforms show switching frequency view at around source voltage peak (90^0) and 45^0 from zero crossing respectively. Due to presence of parallel capacitor, the TC coil voltage and current profiles are very close to sinusoidal. Compared with

parallel capacitor in conventional parallel LC tank the parallel capacitor, C_p in proposed CLC tank offers much lower impedance to higher order harmonics. This is because the capacitance value of C_p in CLC tank is approximately twice than that of simple parallel LC tank.

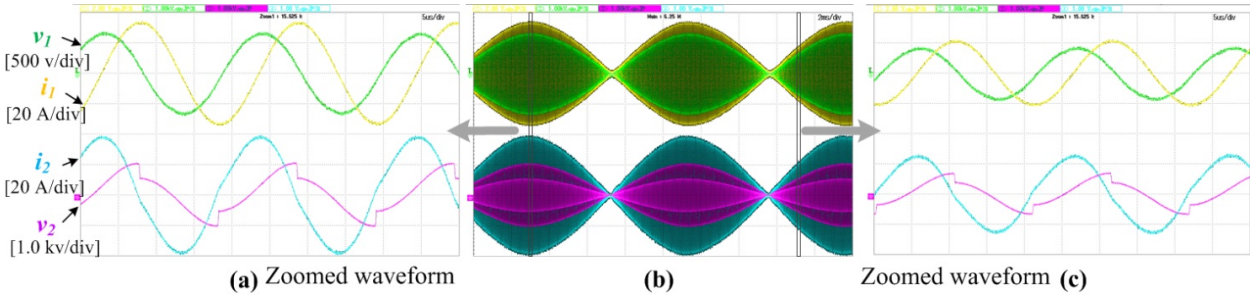


Fig. 6.16 Experimental results: Transmitter and receiver coil voltages and currents at when V_{ac}=200V ac, P_o=1.2kW, V_o=300V

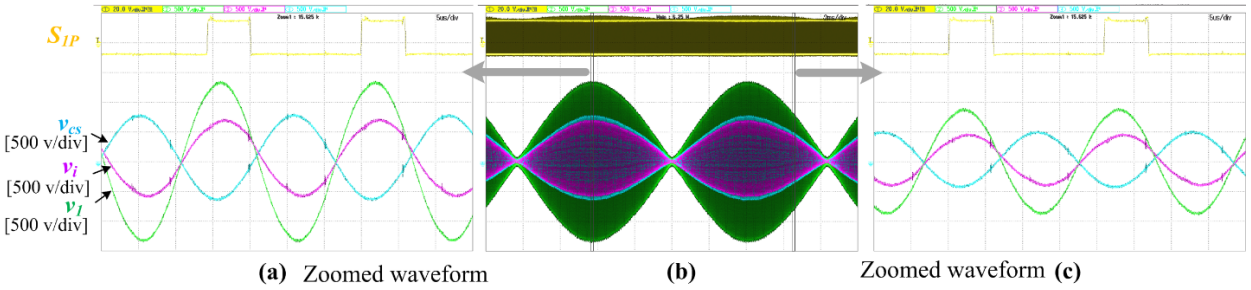


Fig. 6.17 Experimental results: Gate pulse of device S_{1P} and voltages across different elements (C_s, C_p, TC) in the TC side tank network.

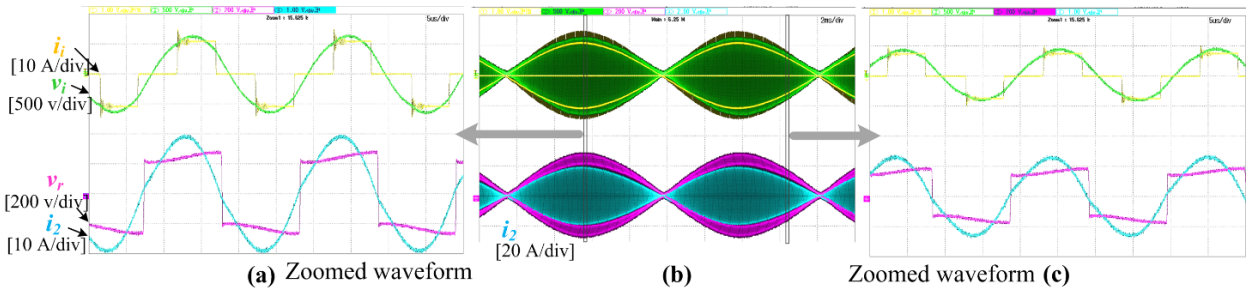


Fig. 6.18 Experimental results: Input and output voltages and currents of the resonant tank network.

Fig. 6.17 shows gating signal of S_{1P} and voltages across TC side tank elements. These results show the advantage of CLC tank network over simple parallel LC tank. Without the presence of series capacitor, C_s the converter devices would get directly TC coil voltage which is quite high.

However, since the series capacitor C_s partially compensates the TC coil leakage impedance; therefore, parallel capacitor has to provide only remaining amount of reactive power to TC coil. Thus, the converter devices get only v_i and it is a faction of TC coil voltage, v_1 as shown in Fig. 6.17.

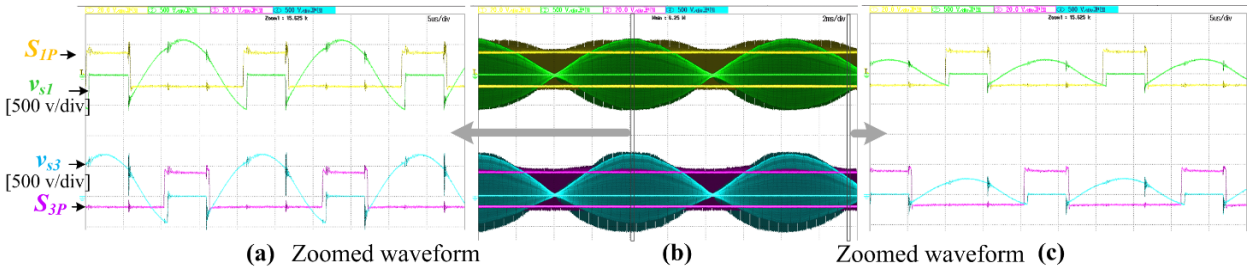


Fig. 6.19 Experimental results: Soft switching of ac-ac converter devices S_{1P} and S_{3P}.

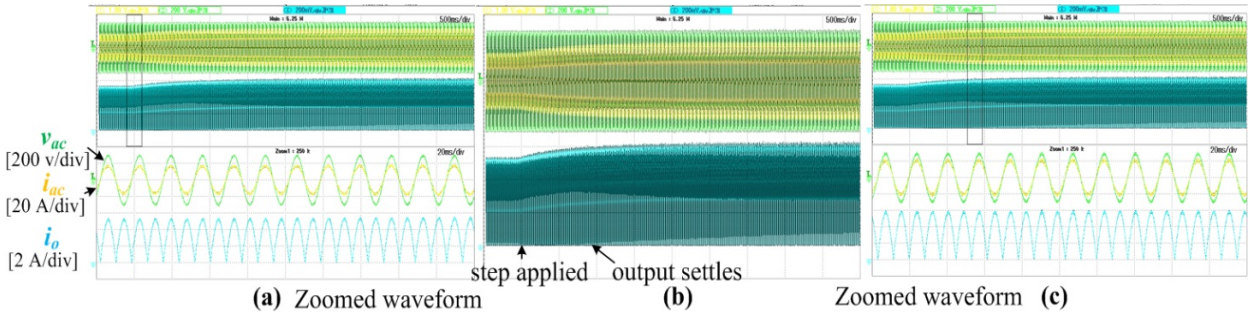


Fig. 6.20 Dynamic response of the proposed converter for a load step from 70% of rated load to rated load.

Fig. 6.18 shows input and output voltages and currents of proposed CLC primary and LC series secondary tank network. The operating power factor at the ac-ac converter output is lagging and it is suitable for soft switching operation. Also, in the receiver side the rectifier diodes turns-on and turns-off at zero current. This ensures zero reverse recovery of these rectifier diodes. There is some surge current present in the ac-ac converter output current. Fig. 6.18 experimental results show this current profile with full bandwidth of digital storage oscilloscope (DSO). However, in Fig. 6.15 the bandwidth of DSO is kept at 20MHz to show exact line frequency envelope profile of the ac-ac converter output current. However, without this setting this current profile is not very clear.

Fig. 6.19 shows soft switching performance of converter devices S_{1P} and S_{3P}. In lagging power factor the device S_{1P} is triggered when voltage across the device S_1 is negative and this negative voltage is blocked by S_{1N}. Therefore, device S_{1P} does not start conducting immediately and this

results ZVS of S_{1P}. However, after the overlap period the complementary device of S_1 i.e. S_2 is turned off and S_1 is force to take the input current, i_s. Also before turn-off of S_1, the complementary device, S_2 is triggered to maintain required overlap. Since, voltage across S_2 is positive; therefore, *S2* immediately commutates S_1. Thus, device S_1 turns off at zero current. During this operation the device S_2 experiences hard switching both during turn-on and turn-off. Similar soft switching turn-on and turn-off characteristics is obtained for device S3 as shown in Fig. 6.19.

Fig. 6.20 shows dynamic response of the converter when a load step commend form 70% of rated load (0.84 *k*W) to rated load (1.2 *k*W) is applied. From Fig. 6.20 it is clear that the outer loop is capable of meeting the load requirements while inner input current loop ensures high quality source current. The load current settles at around 0.75s and this verifies the dynamic model of the converter. Since, there is no bulky electrolytic capacitor to filter out the second harmonic; therefore, the load current contains second harmonics. These results are significant when the load is resistive such as lighting load. In case of a fault or other emergency such as living object detection (LOD) function detects an intrusion into the active region then the load power has to be reduced abruptly from full load to light load. In this situation the control command can be directly applied to inner input current control loop for faster response and safety. Below figure shows simulation results of this situation where a step change in input current magnitude is applied from rated magnitude to 10%. The system settles within around 0.36 ms and this the closed loop settling time of the inner loop. Although, the current quality deteriorates at light load but total demand distortion (TDD) is calculated to be 4.6% and it is well within IEEE 512-1992 standards. There are several techniques to improve the performance of the converter at light load similar to boost derived PFCs such as on/off control and Digital Phase Leading Filter Current Compensation (PLFCC) [83], [84], [85] etc. However, these topics are another broad area of research; therefore, it can be considered as future research.

Literature study shows that this rectified sinusoidal current is acceptable for several battery charging applications [86]. However, in case the load does not accept this current profile then a reasonable size dc capacitor can be connected at the output of the converter. The proposed analysis and experimental results shows that the converter is capable to deliver power in either cases. The first part of experimental results shows the load current as rectified sinusoidal and the later part of experimental results show the ripple free dc load current.

6.6.3 Results with Stiff Voltage Load

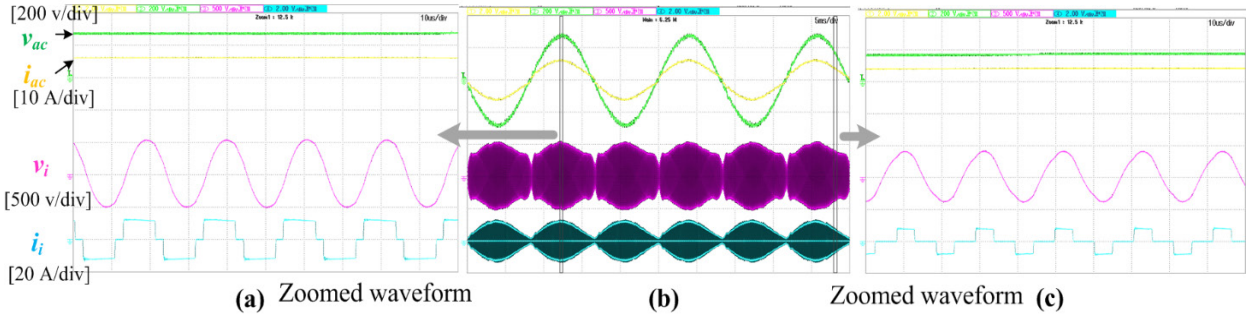


Fig. 6.21 Experimental results of grid voltage, current and ac-ac converter output voltage and current waveforms when V_{ac}=200V ac, P_o=1260W, V_o=270V stiff dc (a) zoomed view at line frequency peak (b) line frequency view (c) zoomed view at off peak of line frequency.

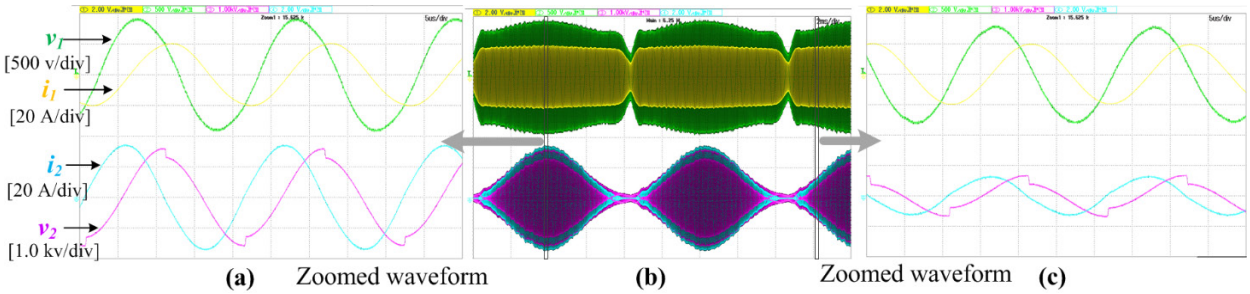


Fig. 6.22 Transmitter and receiver coil voltages and currents at when V_{ac}=200V ac, P_o=1.2kW, V_o=270V stiff dc.

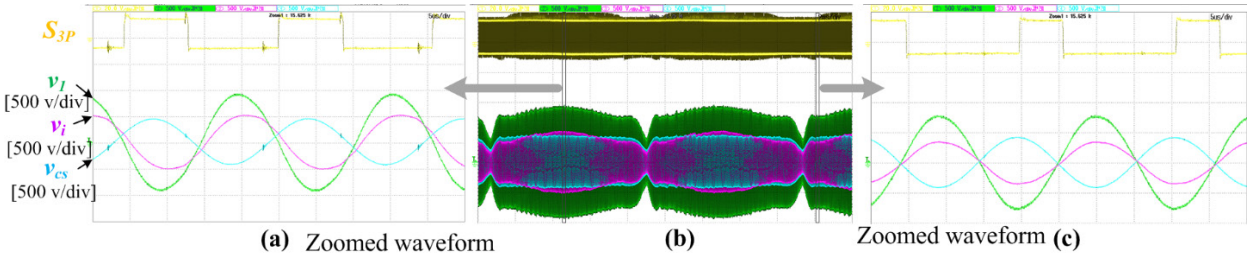


Fig. 6.23 Gate pulse of device S_{3p} and voltages across different elements (C_s, C_p, TC) in the TC side tank network.

To verify the performance of the converter for battery charging applications a stiff dc voltage load is connected at the converter output. Fig. 6.21 shows experimental results of grid voltage, current and ac-ac converter output voltage and current waveforms when V_{ac}=200V ac, P_o=1260W, V_o=270V fixed dc. It is clear that inner input current loop is capable of maintain high quality grid current. The THD of this current is calculated to be around 4.5% and it is well within IEEE 519-1992 specified standards. From Fig. 6.21a it is seen that unlike resistive load, here the ac-ac

converter output voltage does not follow line frequency sinusoidal envelope. This voltage does not reduce significantly towards the zero crossing of line frequency. This is because the load is stiff dc voltage and to pump the charge to this high dc voltage towards line frequency zero crossing, the TC side has to maintain significant amount of voltage. This fact is evident from Fig 19a and 19c zoomed waveform of i_i that towards zero crossing the boosting feature of ac-ac converter becomes high. This phenomenon of the converter is very similar to boost derived PFCs.

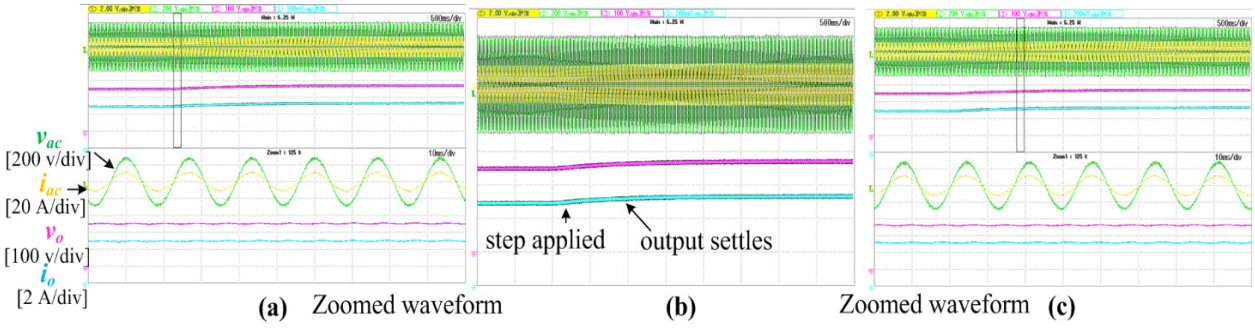


Fig. 6.24 Dynamic performance of the converter for a step change in output current reference from 4.4A to 5.5A

Fig. 6.22 shows TC and RC voltages and current profiles. Similar to earlier results, the TC coil receives very high quality sinusoidal current. As discussed, the TC side coil voltage and current envelope does not follow the sinusoidal trend of the line frequency because of stiff dc output voltage. Fig. 6.23 shows gating signal of device S_{2P} and voltages across TC tank network elements. Similar to earlier, the magnitude of voltage across parallel capacitor, V_i is a fraction of TC voltage V_1 because of the presence of series capacitor, C_s. Since, V_i directly determines ac-ac converter device voltage stress; therefore, CLC tank is superior in terms of inverter device voltage rating.

From Fig. 6.21 and Fig. 6.23 it is clear that unlike resistive load, the duty cycle of the ac-ac converter devices vary significantly throughout the line frequency. The duty cycle of device S_1 and S_3 slowly reduces when input voltage moves from peak to zero. From steady state operation interval II it is clear that current through the S_1 is transferred to S_2 before the gate pulse of S_1 is withdrawn. Therefore, S_1 experiences soft turn off and S_2 experiences hard turn on. Again, in interval II of steady state operation the device S4 keeps on conducting when S_3 is given getting pulse. This leads to soft turn on of S_3 and hard turn on S_4.

Fig. 6.24 shows dynamic performance of the converter when a step change in load current reference is given from 4.4A to 5.5A. The outer output current loop is capable to meet load demand

within the designed settling time i.e. around 0.75s while the inner loop maintains the high quality source current.

6.7 Conclusions

The contribution and focus of this research is to propose, analyze, and develop a new power electronics system using direct ac-ac converter for wireless power transfer applications. Compared with existing buck derived ac-ac converters for IPT systems, the proposed ac-ac converter topology is boost derived. This ac–ac converter is fed from a current source; therefore, it is very much like boost derived PFC topology. This enables to achieve high quality source current by controlling the source inductor current. To match compatibility between ac-ac converter and tank network, a parallel-series (CLC) tank network in TC side is selected. This CLC tank improves the overall performance of the converter viz. lower device voltage stress and high-quality TC current etc. The proposed two loop control scheme is simple and capable of meeting all the control goals. The outer output current control loop meets dynamic load demand while the faster inner input current loop ensures UPF at source. Detailed steady state operation, dynamic model and design of converter circuit is reported. The experimental results obtained from 1.2 *k*W proof-of-concept scale down lab-prototype verifies the analysis and performance of the proposed converter.

Chapter 7 Conclusions and Future Research

This chapter concludes the thesis. The summary and conclusions of each Chapter are given in Section 7.1, contributions of the thesis are summarized in Section 7.2, and guidelines for future research are given in Section 7.3.

7.1 Summary and Conclusions

Inductive power transfer (IPT) technology provides a very convenient, safe, efficient, and reliable way of transferring electrical power wirelessly. The existing research on IPT primarily focuses on voltage source inverter technology, where current-source technology has received very limited attention. This research provides a comprehensive overview of compensation networks and converter topologies of existing IPT systems. A series *LC* compensated primary fed from a VSI experiences severe instability issue during light load or absence of secondary coil. Also, high amplitude primary coil current is directly drawn from VSI due to its series structure. Although, *LCL* or *LCLC* tank fed from a VSI does not experience these issues and has high tolerance to coil misalignment, they draw non-sinusoidal current from the inverter. This leads to higher VA loading and subsequent higher power loss in the inverter. Although, the extra ac inductor in these tanks is quite small, it is highly sensitive to effective wireless power transfer. Therefore, the inductor must be designed and manufactured with very high precision, which incurs additional cost. Considering these limitations, this thesis provides concept study and feasibility analysis of current-fed power electronics for an IPT system, where the primary application is EV charging.

In Chapter 2, the reasons for using current-fed push-pull inverter with parallel *LC* tuned IPT topology only in low power applications have been discussed. In view of this, a new IPT topology has been proposed, where the inverter is full-bridge CSI and the compensations in primary and secondary sides are parallel and series types, respectively. Compared with the existing IPT topology, the proposed system does not have startup and frequency bifurcation issues. The other merits of the this topology are that the parallel tank network ensures lower inverter device current stress, very close to sinusoidal coil current, soft-switching of inverter devices, and natural short circuit protection during inverter fault. A detailed analysis of converter design and soft-switching conditions has been provided. Simulation and experimental results have also been included to verify the analysis and performance of the converter.

Chapter 3 shows that due to a weak coupling between IPT coils, the primary side parallel capacitor experiences high voltage stress in higher power levels, and this voltage directly appears on inverter devices. To overcome this, a modified IPT topology fed from a CSI is proposed, where the primary compensation is parallel-series type and secondary compensation is series type. A detailed analysis of the steady-state operation, converter design, soft-switching conditions, small-signal-modelling, and closed-loop control is provided to justify the improvements. To verify analytical predictions, numerical simulation is performed in PSIM 10. Experimental results obtained from a 420W lab-built prototype verifies the analysis and simulation.

Chapter 4 discusses the small-signal modelling and closed-loop control of both the proposed topologies. However, compared with the bipolar modulation scheme used in earlier chapters, the unipolar modulation scheme used for closed-loop control helps to achieve all the control goals easily. Unlike dynamic tuning techniques, used for parallel resonant tank, a novel load independent tuning technique is proposed to reduce the control effort of CSI. This ensures least VA loading on the inverter, irrespective of any load change and without any dynamic tuning. The closed loop-control with load independent tuning for both the current-fed resonant converters has been analysed in detail and simulated. Experimental results for each possible case of both the topologies have been presented, where the scale-down proof-of-concept lab-prototype is rated for 1.6*k*W.

Chapter 5 proposes a bidirectional IPT topology using current-fed resonant converter. To the best of the author's knowledge, this is the very first study of V2G capable IPT topology with CSI. It has current-sharing feature in grid side converter and voltage doubling feature in vehicle side converter. Keeping the inverter output power factor lagging, ZVS turn-on of the inverter devices is always ensured, irrespective of load variation. A detailed analysis of the steady-state operation and converter design for both G2V and V2G modes is provided. Experimental results obtained from a 1.2*k*W lab-prototype have been reported to verify the analysis and performances of bidirectional IPT circuit.

Chapter 6 explores the major benefit of current-fed technology in single-stage IPT converters. The chapter very systematically establishes that voltage-fed ac-ac converters cannot control source (grid) current due its to buck-derived configuration. Therefore, current-fed ac-ac converter is the only solution to achieve all the control goals of single stage IPT—maintaining UPF at source, effective transfer of power, soft-switching of ac-ac converter devices, and meeting dynamic load

demand. To justify the claims, a new single-stage IPT topology with current-fed ac-ac converter has been proposed. A detailed report on the steady-state operation, converter design, small signal modelling and two-loop control to meet all the control goals has been provided. Experimental results obtained from a 1.2*k*W grid-connected lab-prototype verifies the suitability of this single-stage IPT topology for practical use.

7.1 Contributions

The thesis contributions have been explained in Section 1.7. They can be summarized as follows:

i. A new parallel *LC*-tuned IPT topology fed from a full-bridge CSI has been proposed, where the secondary side has series *LC* compensation. The system is controlled through fixed frequency variable duty cycle modulation and does not experience any start-up and frequency bifurcation issues. A detailed report on steady-state operation, converter design, small-signal modelling, closed-loop control, and soft-switching criteria is provided.

ii. Considering the limitation of parallel *LC* tank on primary side for higher power applications, a modified parallel-series (*CLC*) compensation technique is proposed. Retaining all the merits of earlier topology, this topology reduces the CSI voltage stress significantly, thereby making it more suitable for EV applications. A detailed report on steady-state operation, converter design, small-signal modelling, closed-loop control, soft-switching criteria, simulation, and experimental results is provided.

iii. Understanding the need for V2G operation of EVs in future smart grid applications, a new bidirectional IPT topology has been proposed for the first time using current-fed converter technology. It has a current-sharing feature in grid side converter and voltage doubling feature in vehicle side converter. A detailed analysis, converter design, soft-switching criteria, and experimental results have been provided.

iv. Based on the literature survey, this thesis clearly establishes the necessary requirement for current-fed technology in single-stage IPT systems. Existing single-stage IPT topology derived from VSI fails to draw high quality current from grid. Therefore, a new single-stage IPT topology using current-fed direct ac-ac converter has been proposed and

analyzed to justify the claims. A detailed analysis, converter design, dynamic modelling, closed loop control, and experimental results has been provided.

v. All these studies and results conclude that current-fed technology is certainly a viable solution for wireless inductive power transfer for medium power applications.

7.2 Scope of Future Work

Based on the research done in this thesis, the recommendations for future research are as follows:

7.2.1 Single-Stage Universal Wireless IPT System with V2G Capability

In this thesis, unidirectional, bidirectional, and single-stage power converter topologies are addressed. However, if all these three possibilities are combined in a single converter, then that system will be very suitable for practical use. This will increase flexibility, and reduce cost of the charger. IPT chargers will be quite expensive, especially due to large size coils, ferrite cores, thick litz wires and other coil accessories. Therefore, a universal IPT charger with V2G capability will not only reduce manufacturing cost due to mass production, but also increases flexibility by accepting power both from ac grid and solar PV. To explain this concept, Fig. 7.1 is included, where input to the charger is either ac grid or solar PV. Also, it will be able to participate in V2G, thereby making it a single charger solution.

Although, voltage-fed technology is most popular in IPT technology, but it this single stage solution, VSI may not be a preferred choice. However, current-fed technology can easily perform those tasks, and this is briefly described here.

Grid to vehicle (G2V) operation: This part is clearly explained in Chapter 6 that due to buck derived structure of voltage fed ac-ac converter topology, power factor correction is not possible. Clearly, current-fed ac-ac converter is the most suitable solution to meet all the control goals.

Solar to vehicle (S2V) operation: A single stage S2V power converter requires maximum power point tracking from solar PV. Traditionally, this is done using boost or boost derived converters. Again, due to buck derived structure of VSI (*w.r.t.* dc side), it will not be preferred a choice. Therefore, the current-fed converter will be the appropriate choice.

Vehicle to grid (V2G): During this operation, the vehicle side converter acts as inverter and grid side converter act as a rectifier. If the vehicle side converter is built with active devices to enable inversion mode, then selection of voltage-fed topology in vehicle side will ensure this operation. The primary side converter can be either current-fed or voltage-fed type.

With these considerations, a possible power converter structure to achieve all the operating modes can be derived as shown in Fig. 7.1. However, detailed converter analysis, design, closed-loop control, and experimental verification can be taken as future research work.

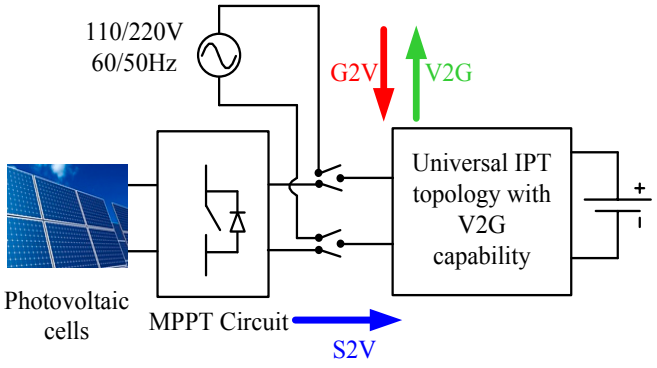


Fig. 7.1. Universal IPT charger with V2G capability

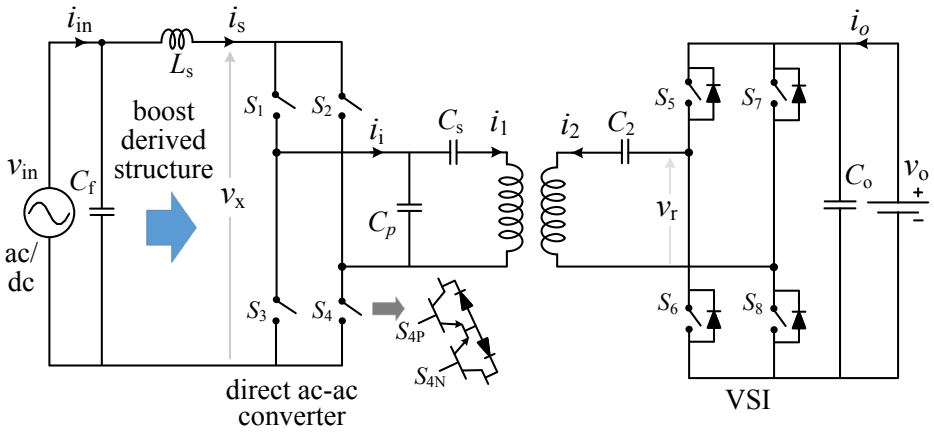


Fig. 7.2 Possible single stage universal IPT topology with V2G capability

7.2.2 Dynamic Model and Control of Bidirectional IPT

In Chapter 5, steady-state analysis and performance of a current-fed IPT topology is proposed. The converter control is carried out through frequency modulation of CSI during G2V operation, and through frequency modulation of VSI during V2G operation. However, detailed closed-loop

control and performances are not addressed. Therefore, this part can be taken as possible future research work.

7.2.3 Test with RV-IGBTs

The proposed current-fed IPT topologies require reverse blocking switching devices for successful operation. At present, the research on reverse blocking IGBTs are ongoing, and there is a lack of wide availability of these devices in terms of ratings, e.g., voltage, current, and maximum switching frequency etc. Therefore, the present research is carried out with power MOSFETs with a series diode. However, the reported dc-dc current-fed IPT topologies will receive much more attention, if the devices are replaced with RV-IGBTs. The performance and experimental verification with RV-IGBTs can be taken as potential future research work.

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Appendix

Table A: Selected components for computation of the different parameters in Table 3.2

Circuit Configuration	Component	Part No.	Rating
Proposed converter, P_o=420 W	MOSFET	IPA65R380E6	650 V, 10.6 A
	Diode[for inv.]	SCS208AMC	650 V, 8.0 A
	Capacitors	940C20S47K-F	500 V AC, 47 nF
		940C20S22K-F	500 V AC, 22 nF
		940C30S47K-F	750 V AC, 47 nF
	Diode[for rec.]	DSS60-0045B	45V, 30A
Proposed converter, P_o=3 kW	MOSFET	SCT2160KEC	1200 V, 22 A
	Diode [for inv.]	DSEP29-12A	1200V, 15 A
	Capacitors	940C30S1K-F	750 V AC, 10 nF
		940C30S15K-F	750 V AC, 15 nF
		940C30S47K-F	750 V AC, 47 nF
		940C30P1K-F	750 V AC, 100 nF
		940C30P15K-F	750 V AC, 150 nF
	Diode[for rec.]	STTH6004W	400V, 30A
Converter with LC resonance tank at TC, P_o=420 W	MOSFET	IXTH12N150	1500 V, 6 A
	Diode[for inv.]	FFPF10F150STU	1500 V, 5 A
	Capacitors	940C20S47K-F	750VAC,47 nF
	Diode[for rec.]	DSS60-0045B	45V, 30A
Converter with LC resonance tank at TC, P_o=3 kW	MOSFET	SCT2160KEC	1200 V, 22 A,
	Diode[for inv.]	DSEP29-12A	1200V, 15 A
	Capacitors	940C30P1K-F	750 V AC, 100 nF
		940C30P15K-F	750 V AC, 150 nF
	Diode[for rec.]	STTH6004W	400V, 30A, V_f=1.2

List of Publications

Journal Publications:

[1] S. Samanta, and A. K. Rathore, “Analysis and Design of Load Independent ZPA Operation for P/S, PS/S, P/SP and PS/SP Tank Networks in IPT Applications” in *IEEE Transactions on Power Electronics* DOI: 10.1109/TPEL.2018.2794623.

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[8] S. Samanta, and A. K. Rathore, “Concept Study and Feasibility Analysis of Current-fed Power Converter for Wireless Power Transfer System,” *Unver review in IEEE Transactions on Industry Applications.*

Conference Publications:

[1] S. Samanta, and A. K. Rathore, "Analysis and Design of Load Independent ZPA Operation for P/S and PS/S Tank Networks in IPT Applications" *Presented in IEEE Applied Power Electronics Conference and Exposition (APEC) 2018*, San Antonio, TX, USA.

[2] S. Samanta, and A. K. Rathore, "A New Inductive Power Transfer Topology Using Direct AC-AC Converter with Active Source Current Control" *2017 IEEE Industry Applications Society Annual Meeting*, Cincinnati, OH, USA, 2017, pp. 1-8.

[2] S. Samanta, and A. K. Rathore, "A Novel Zero Voltage Switching Inductive Power Transfer Topology Using Current-fed Converter for EV Battery Charging Applications," *IEEE Applied Power Electronics Conference and Exposition (APEC) 2017*, Tampa, Florida, USA.

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